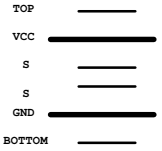
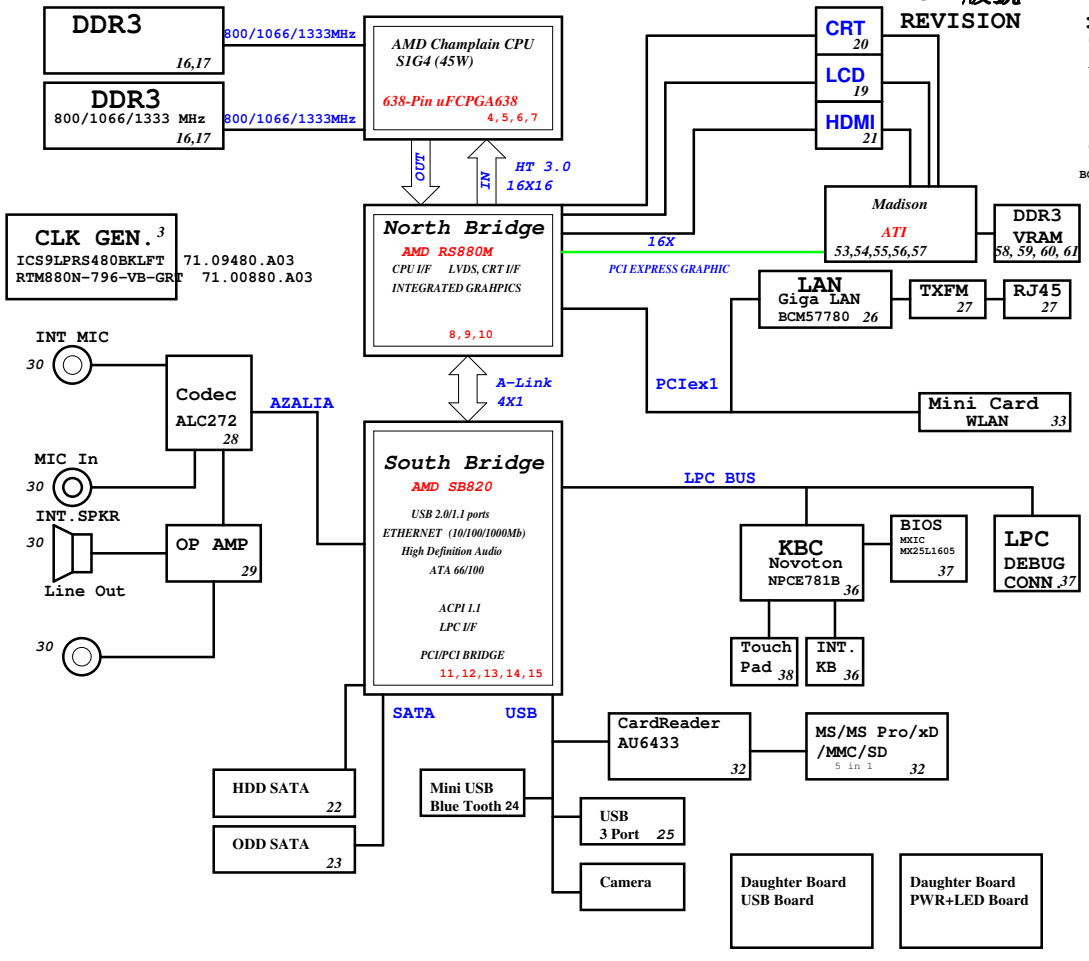
HM42-DN Block Diagram

Project code: 91.4HD01.001
PCB P/N : 48.4GX01.0SA
PCB 版號 : 09919 SA
REVISION : PCB STACKUP





SYSTEM DC/DC RT8223 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 47	
5V_S5	1D5V_S3(14A)
RT9026 47	
5V_S5	0D75_S3(1.2A)

SYSTEM DC/DC RT8209E 48	
INPUTS	
DCBATOUT	1D1V_S0(11A)
RT9025 48	
3D3V_S5	1D1V_S5(1.4A)

RT9025 49	
5V_S5	1D1V_VGA
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
RT9025 49	
1D5V_S3	1D05V_S0 (1.4A)

CHARGER BQ24745 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 1 of 63

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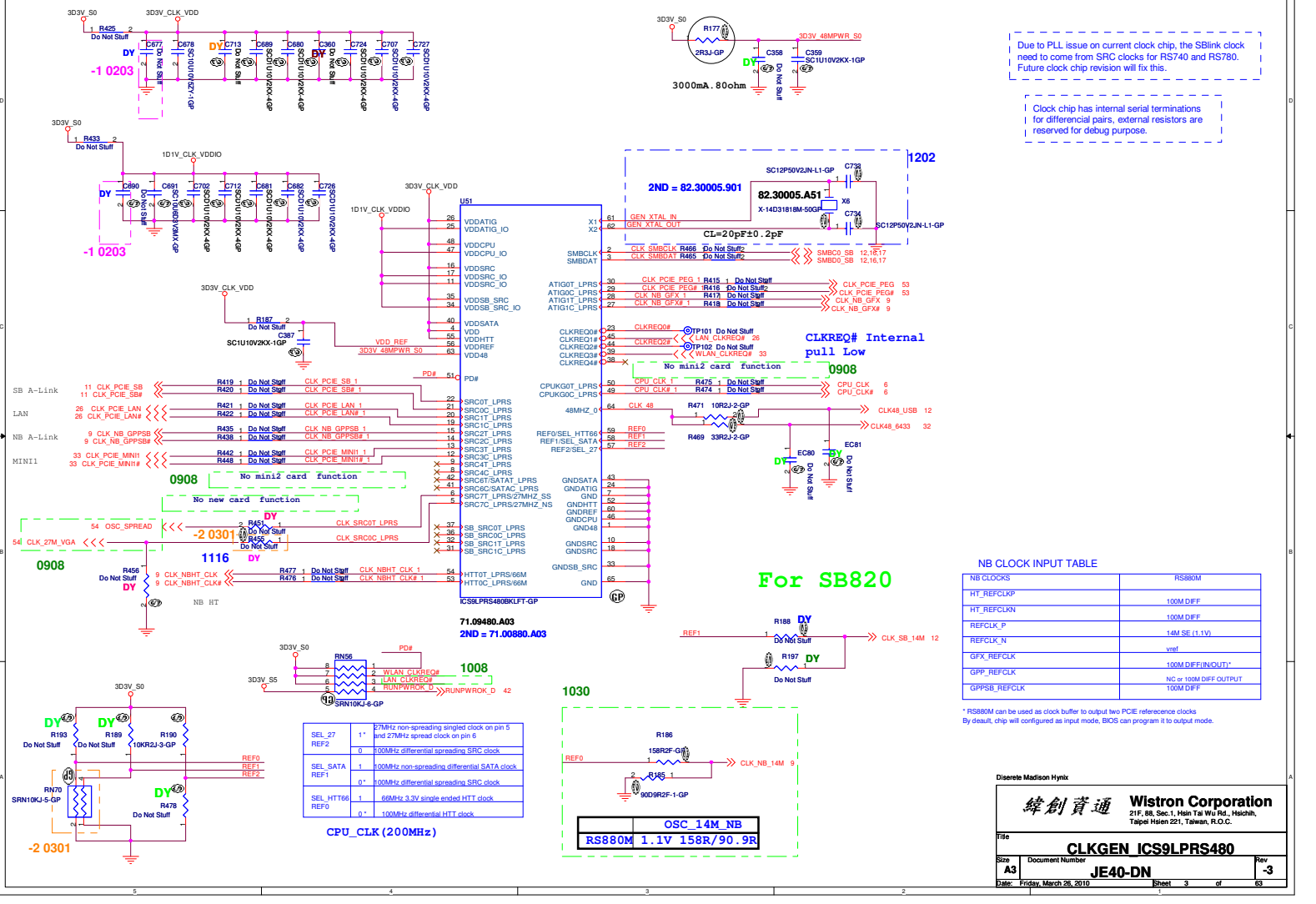
Taipei Hsien 221, Taiwan, R.O.C.

Title	History	
Size: A3	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 2 of 63	



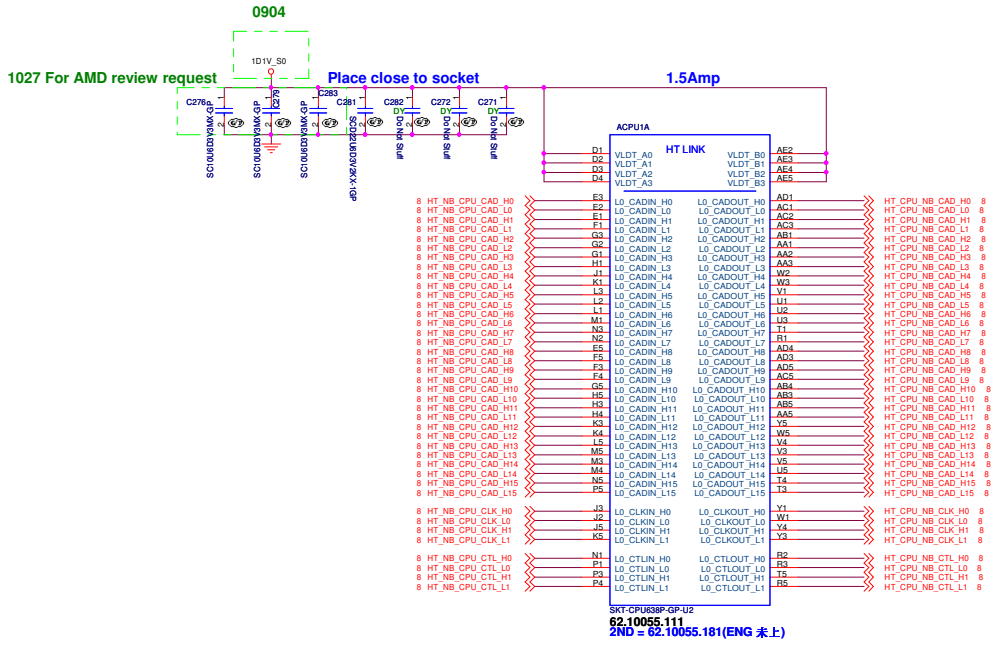
SEL_27 REF2	1 *	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0 *	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

CPU_CLK(200MHz)

NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS com program it to output mode.



SKT-BGA638H176

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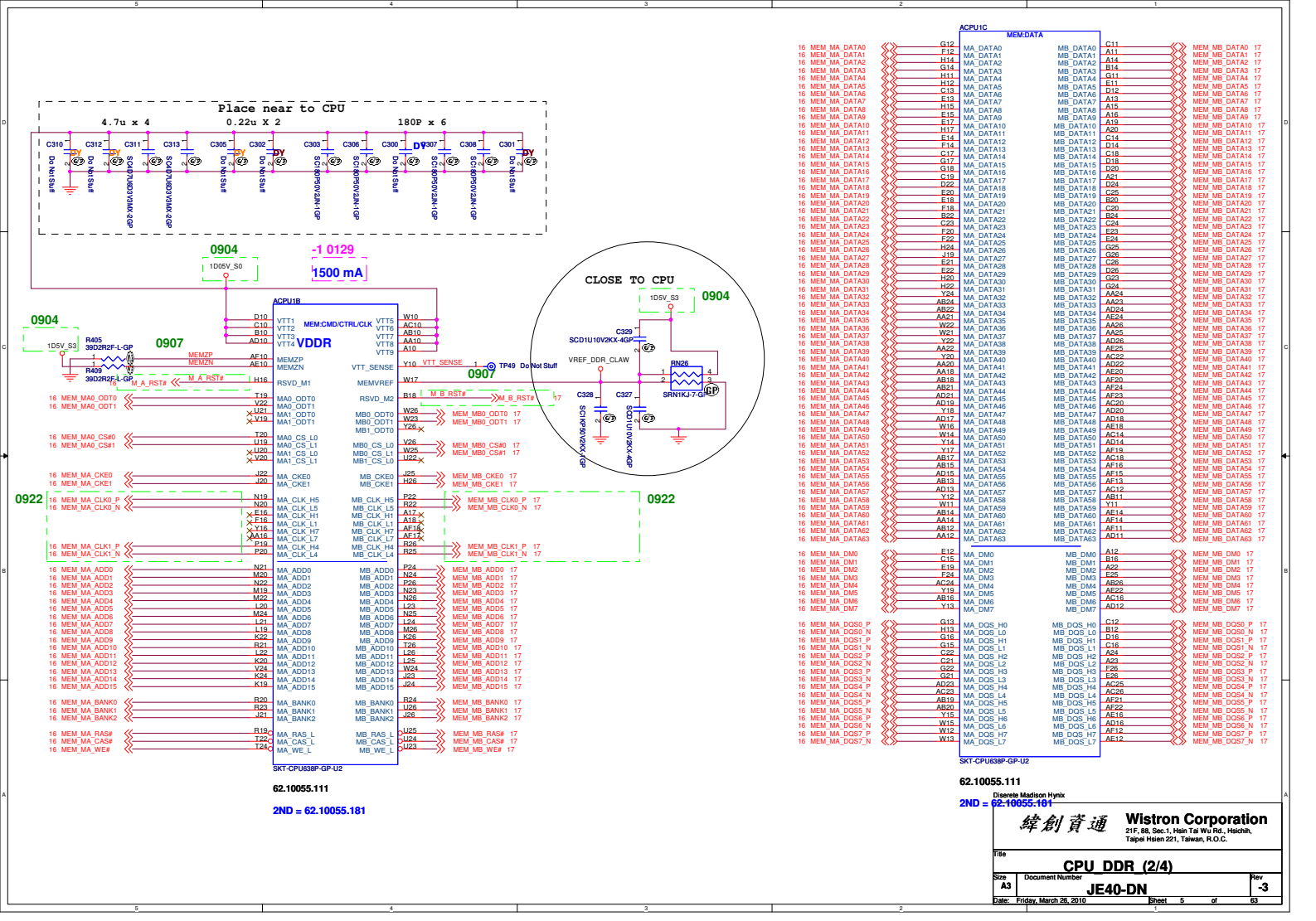
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU_HT_LINK I/F_(1/4)**	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 4 of 63	



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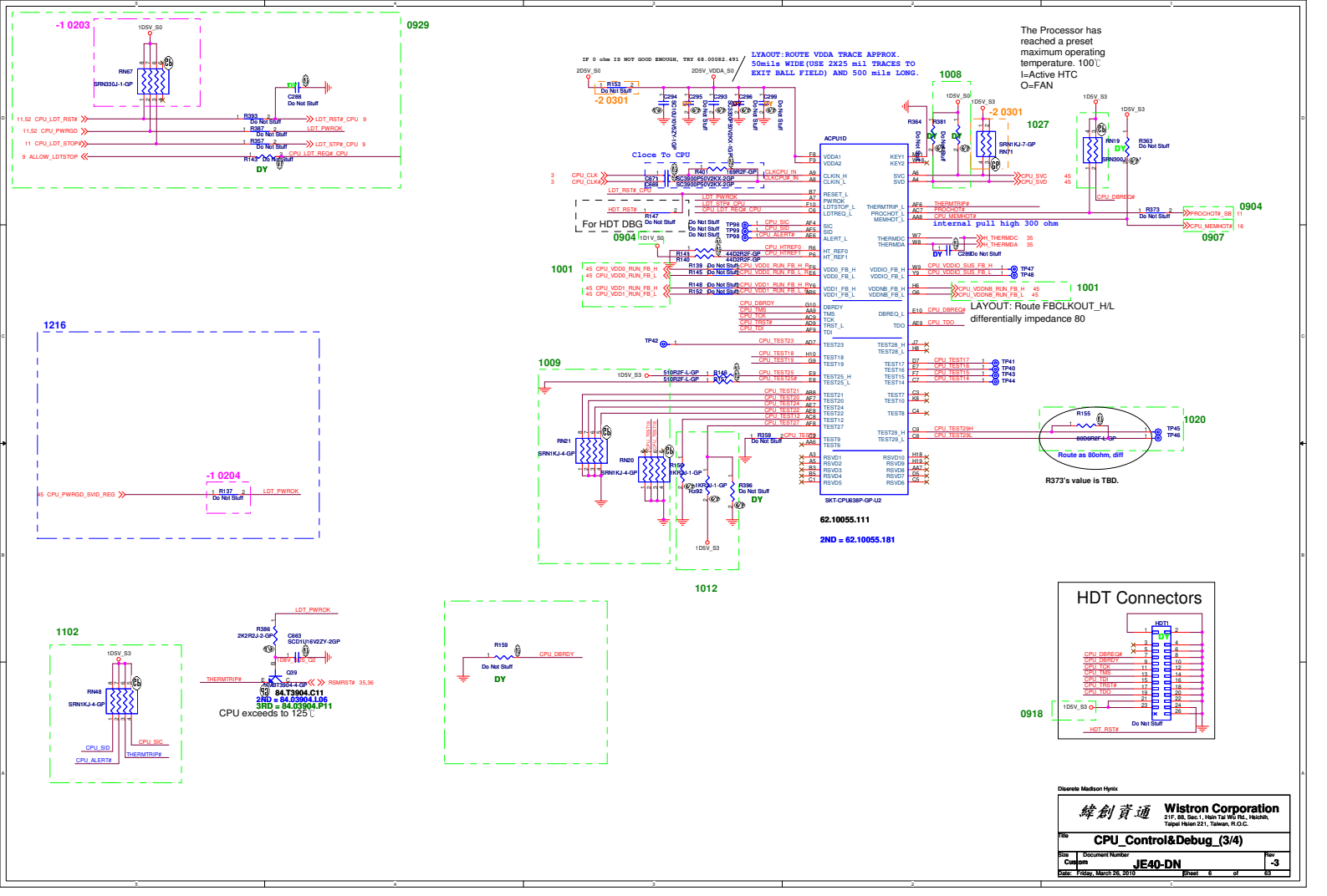
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_DDR_(2/4)**

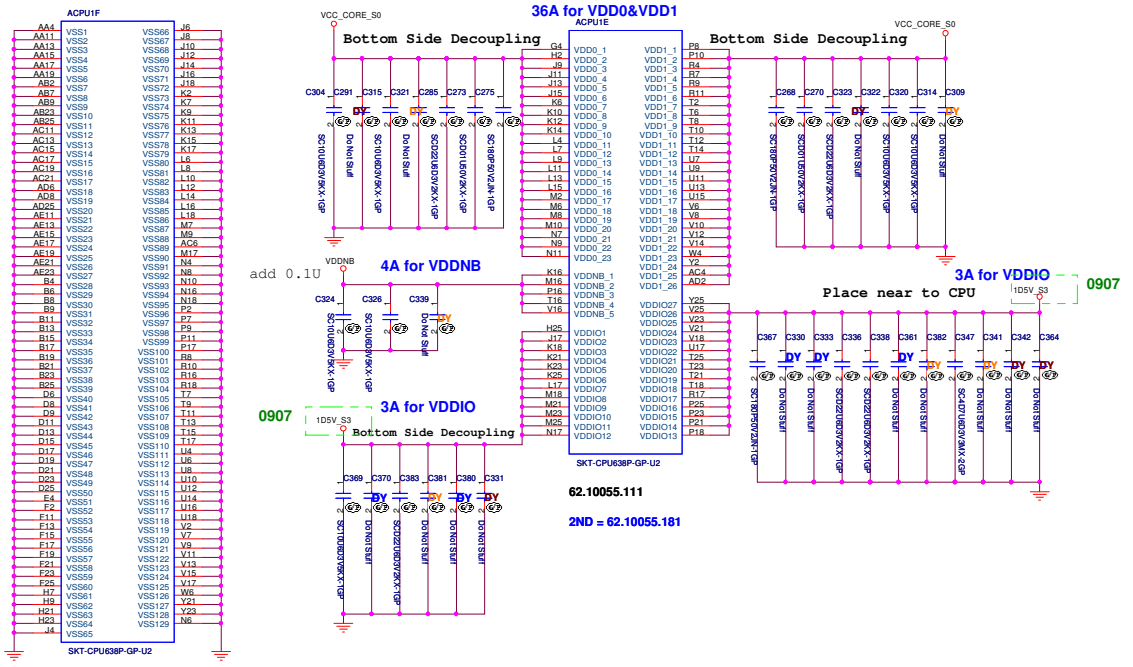
Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 5 of 63



Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU_Control&Debug_(3/4)**	
Size: Custom	Document Number: **JE40-DN**	Rev: **-3**
Date: Friday, March 26, 2010	Sheet 6 of 53	



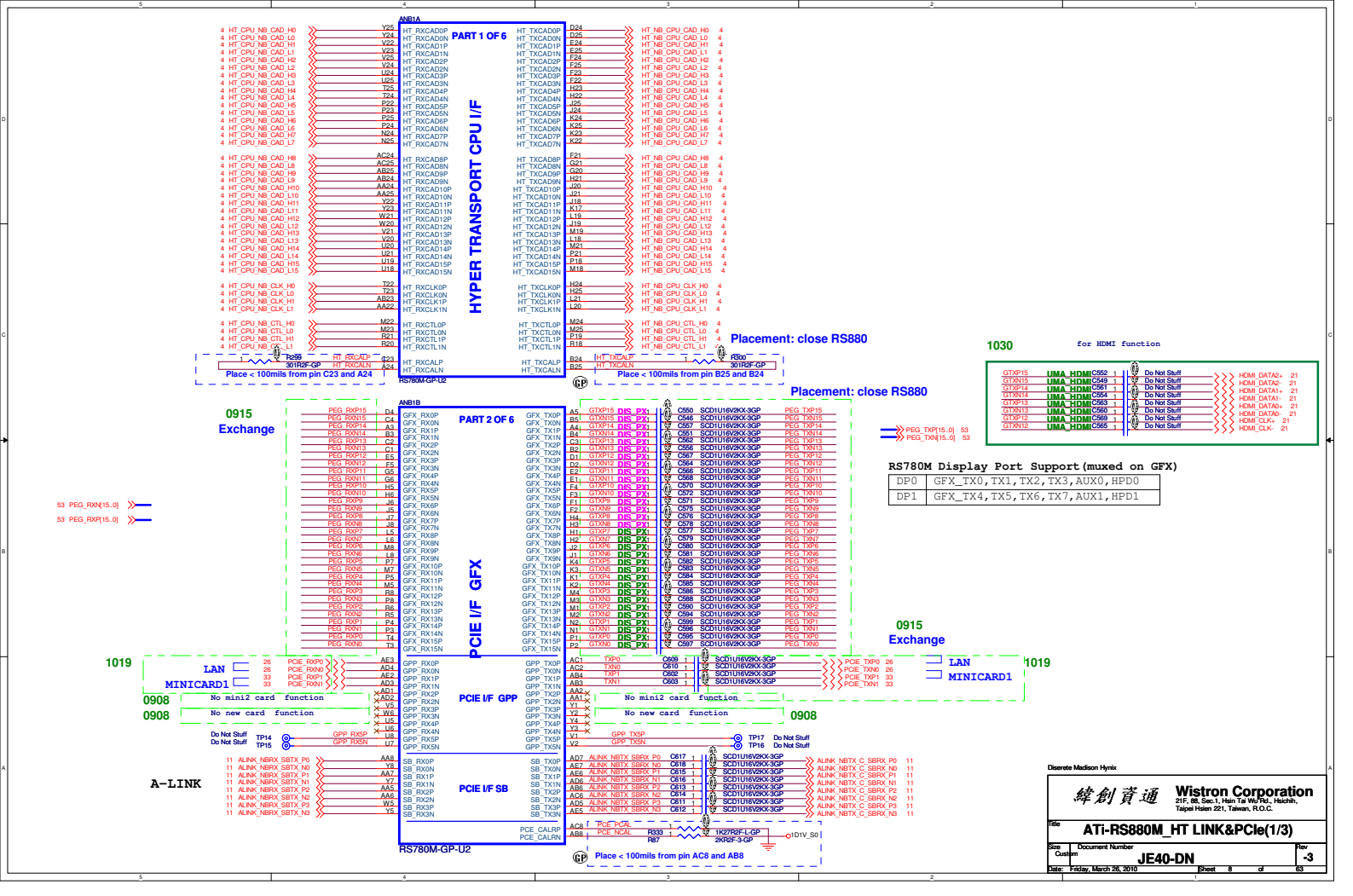
Diserete Madison Hynix

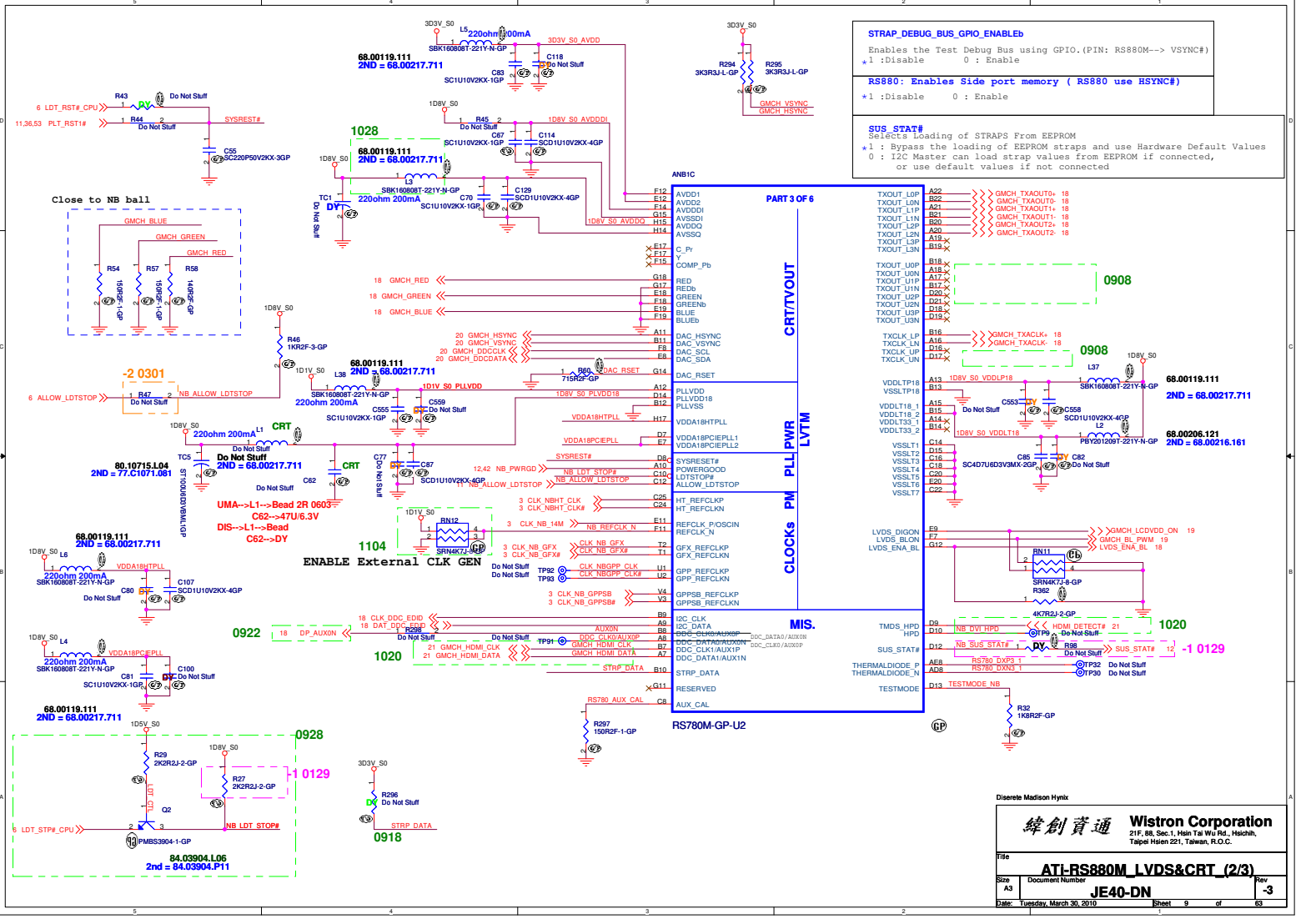
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

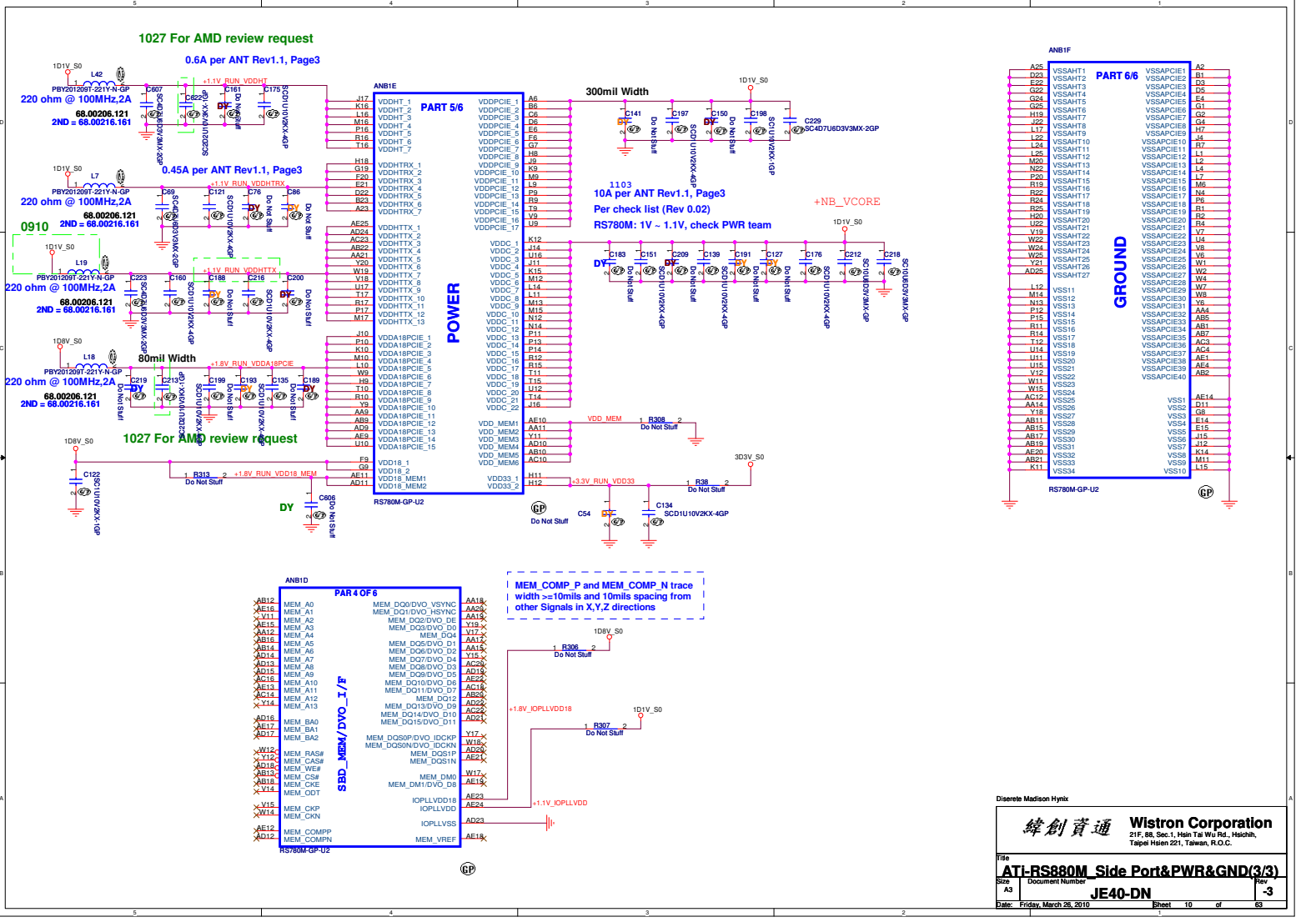
Title: **CPU_Power_(4/4)**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 7 of 63


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS880
1030
for HDMI function
0915
Exchange
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
1019
LAN
MINICARD1
0908
No mini2 card function
No new card function
A-LINK
Place < 100mils from pin AC8 and AB8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size Custom
Document Number
JE40-DN
Rev -3
Date: Friday, March 26, 2010
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC#)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (RS880 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL PWR LVTM
CLOCKs PM
MIS.
RS780M-GP-U2
Close to NB ball
ENABLE External CLK GEN
UMA-->L1-->Bead 2R 0603
C62-->47U/6.3V
DIS-->L1-->Bead
C62-->DY
68.00119.111
2ND = 68.00217.711
80.10715.L04
2ND = 77.C1071.001
68.00206.121
2ND = 68.00216.161
84.03904.L06
2nd = 84.03904.P11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS880M_LVDS&CRT_(2/3)
Size A3
Document Number JE40-DN
Rev -3
Date: Tuesday, March 30, 2010
Sheet 9 of 63



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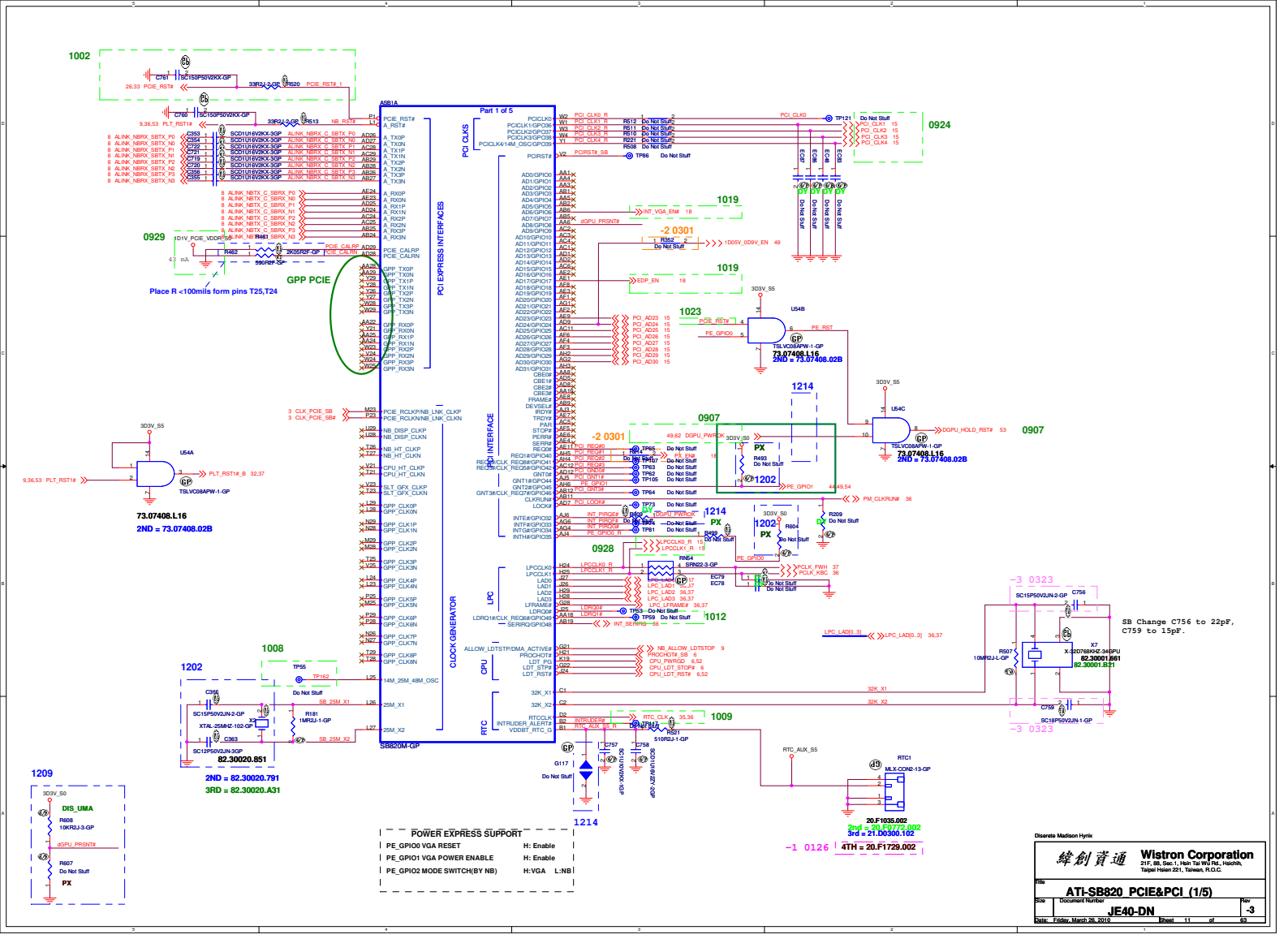
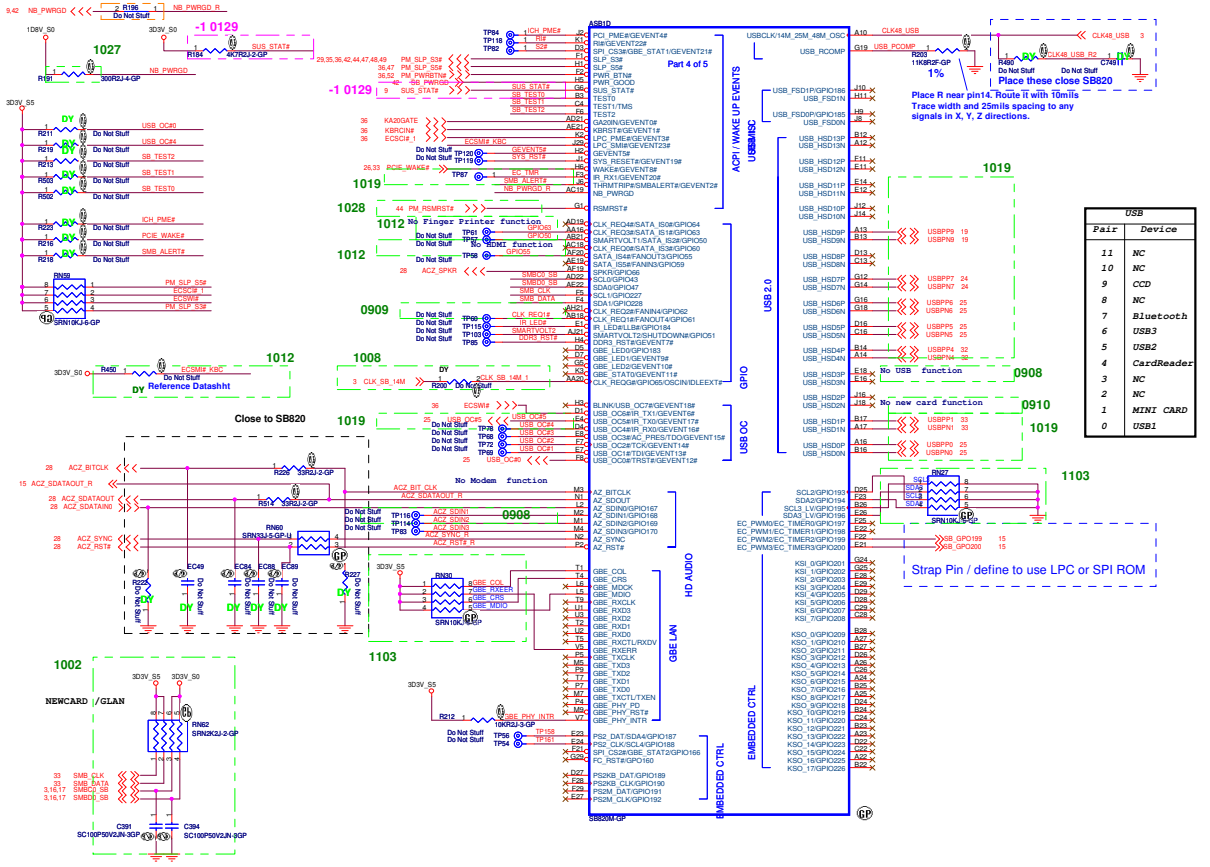
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS880M_Side Port&PWR&GND(3/3)**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 10 of 63


SB820M-GP
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
GPP PCIE
Place R <100mils form pins T25,T24
73.07408.L16
2ND = 73.07408.02B
82.30020.851
2ND = 82.30020.791
3RD = 82.30020.A31
POWER EXPRESS SUPPORT
PE_GPIO0 VGA RESET H: Enable
PE_GPIO1 VGA POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH(BY NB) H:VGA L:NB
SB Change C756 to 22pF, C759 to 15pF.
Wistron Corporation
ATI-SB820 PCIE&PCI (1/5)
JE40-DN
Date: Friday, March 26, 2010
Sheet 11 of 63



USB	
Pair	Device
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	NC
1	MINI CARD
0	USB1

OCP5#

OCP0#

Discrete Madison Hynix

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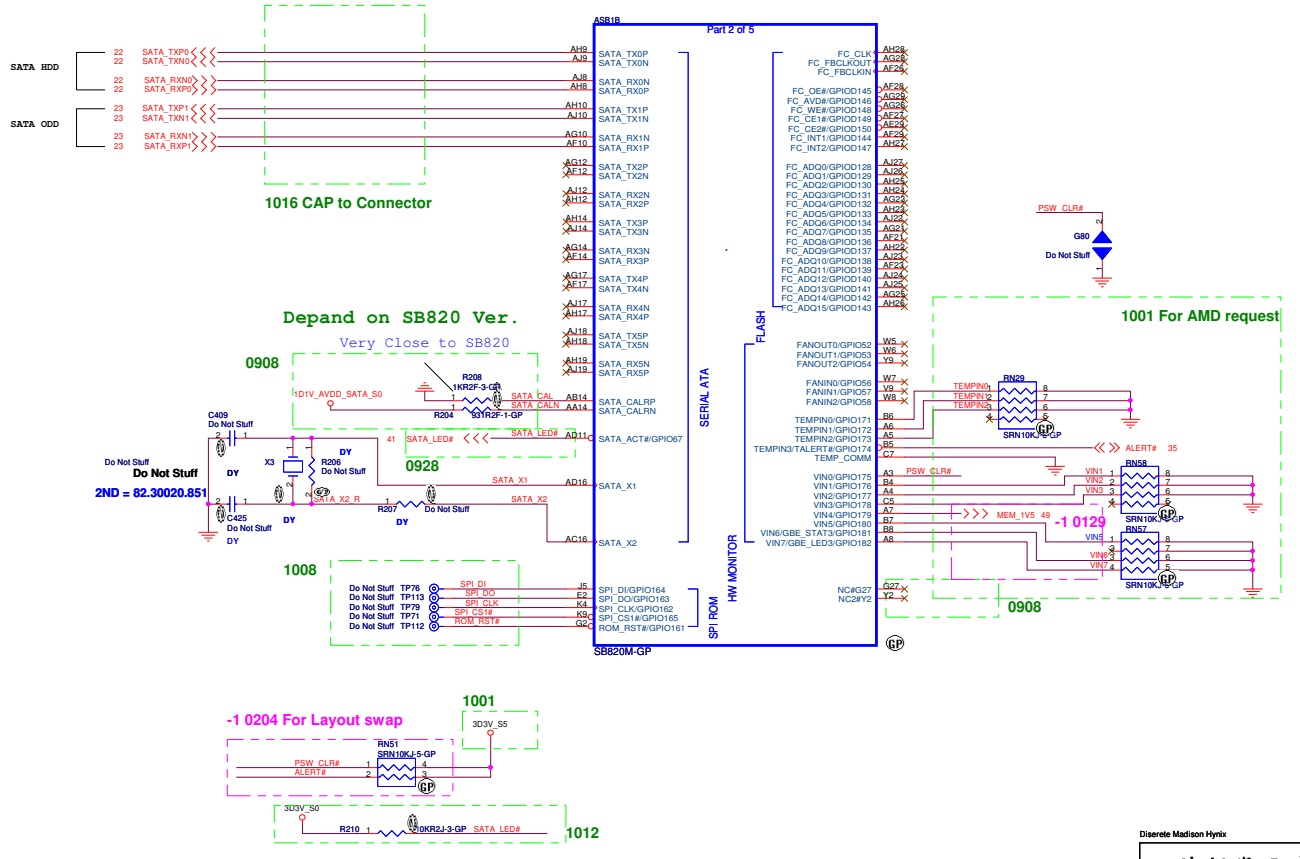
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB820 USB&GPIO (2/5)

Size: Custom | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 12 of 63



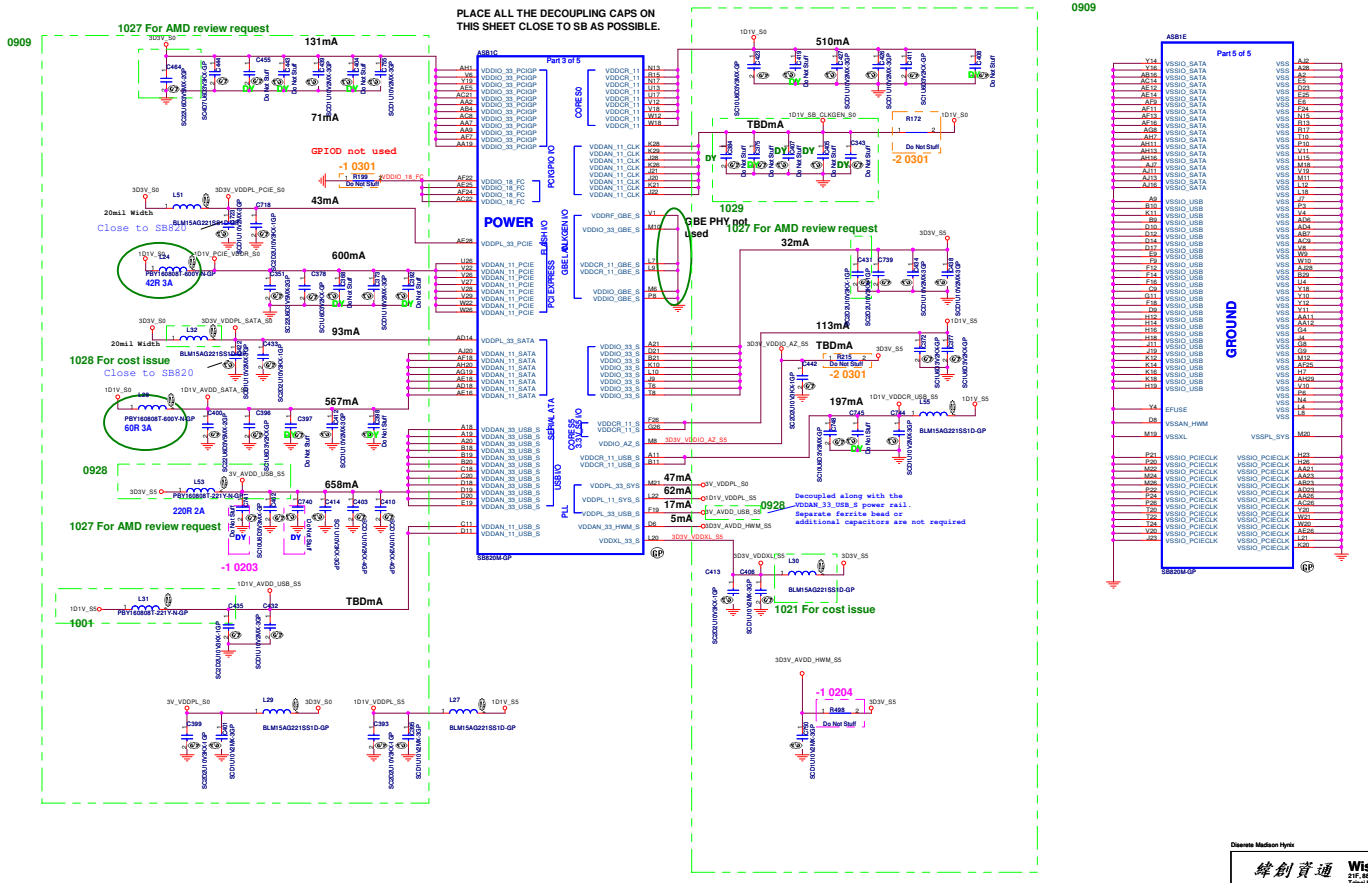
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB820 SATA-IDE (3/5)**

Size	Document Number	Rev
A3	JE40-DN	-3

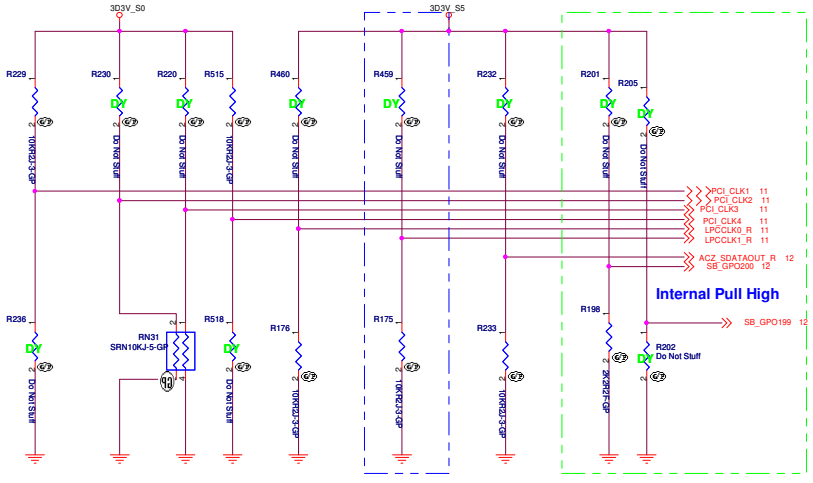
Date: Friday, March 26, 2010 Sheet 13 of 63


PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.
0909
1027 For AMD review request
131mA
71mA
GPIOD not used
-1 0301
Do Not Stuff
43mA
20mil Width
Close to SB820
42R 3A
600mA
93mA
1028 For cost issue
Close to SB820
60R 3A
567mA
0928
658mA
220R 2A
1027 For AMD review request
-1 0203
TBDmA
1001
POWER
GBE PHY not used
1029
510mA
TBDmA
-2 0301
1027 For AMD review request
32mA
113mA
TBDmA
-2 0301
197mA
47mA
62mA
17mA
5mA
0928
Decoupled along with the
VDDAN_33_USB_S power rail.
Separate ferrite bead or
additional capacitors are not required
1021 For cost issue
-1 0204
Do Not Stuff
GROUND
Part 5 of 5
SB820M-GP
Discrete Madison Hynix
Wistron Corporation
2nF, 6/8, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB820 POWER&GND (4/5)
Size Document Number Rev
Custom JE40-DN -3
Date: Friday, March 26, 2010 Sheet 14 of 63

REQUIRED STRAPS

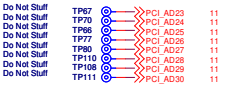
REQUIRED SYSTEM STRAPS

1115



1002

DEBUG STRAPS



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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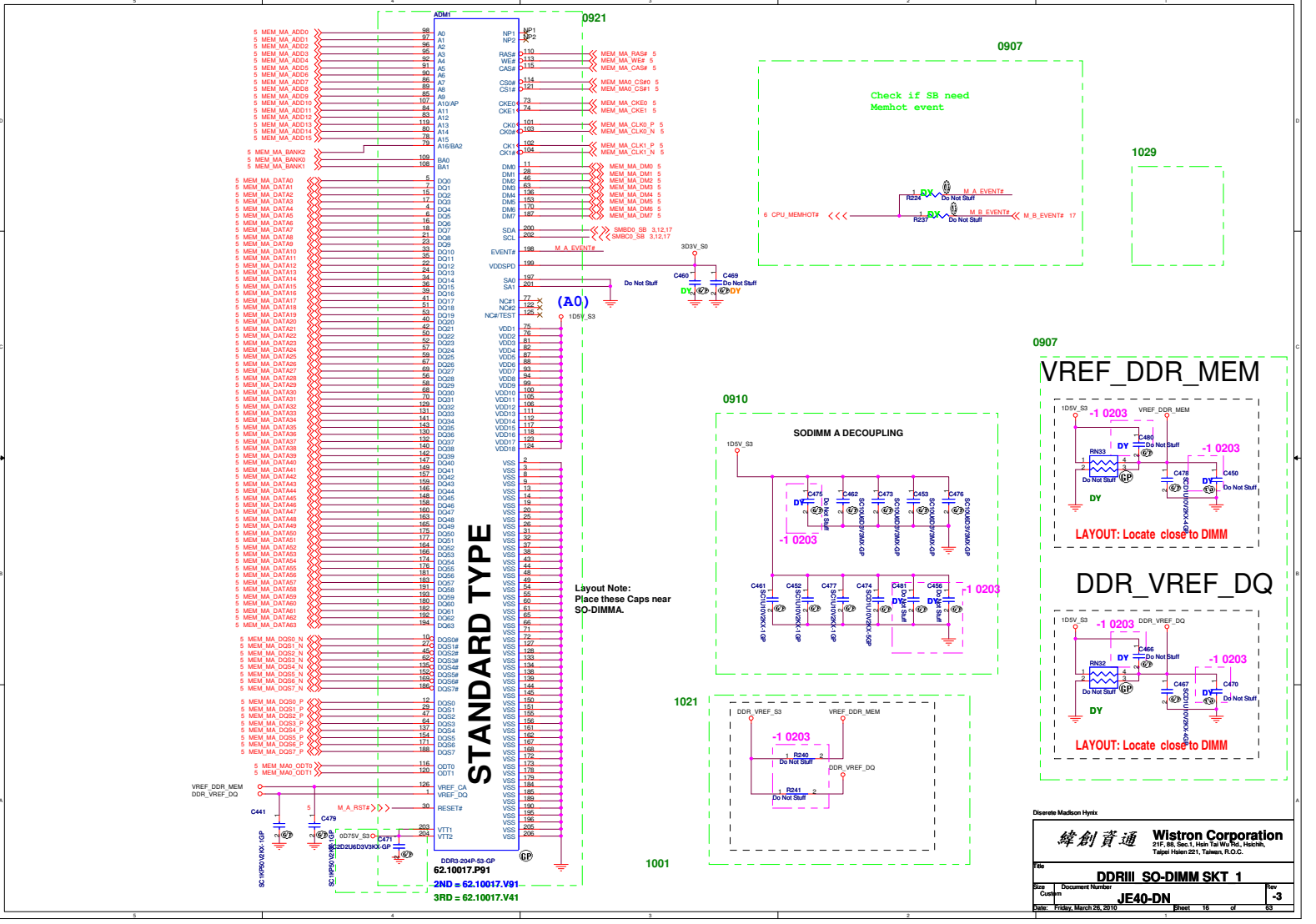
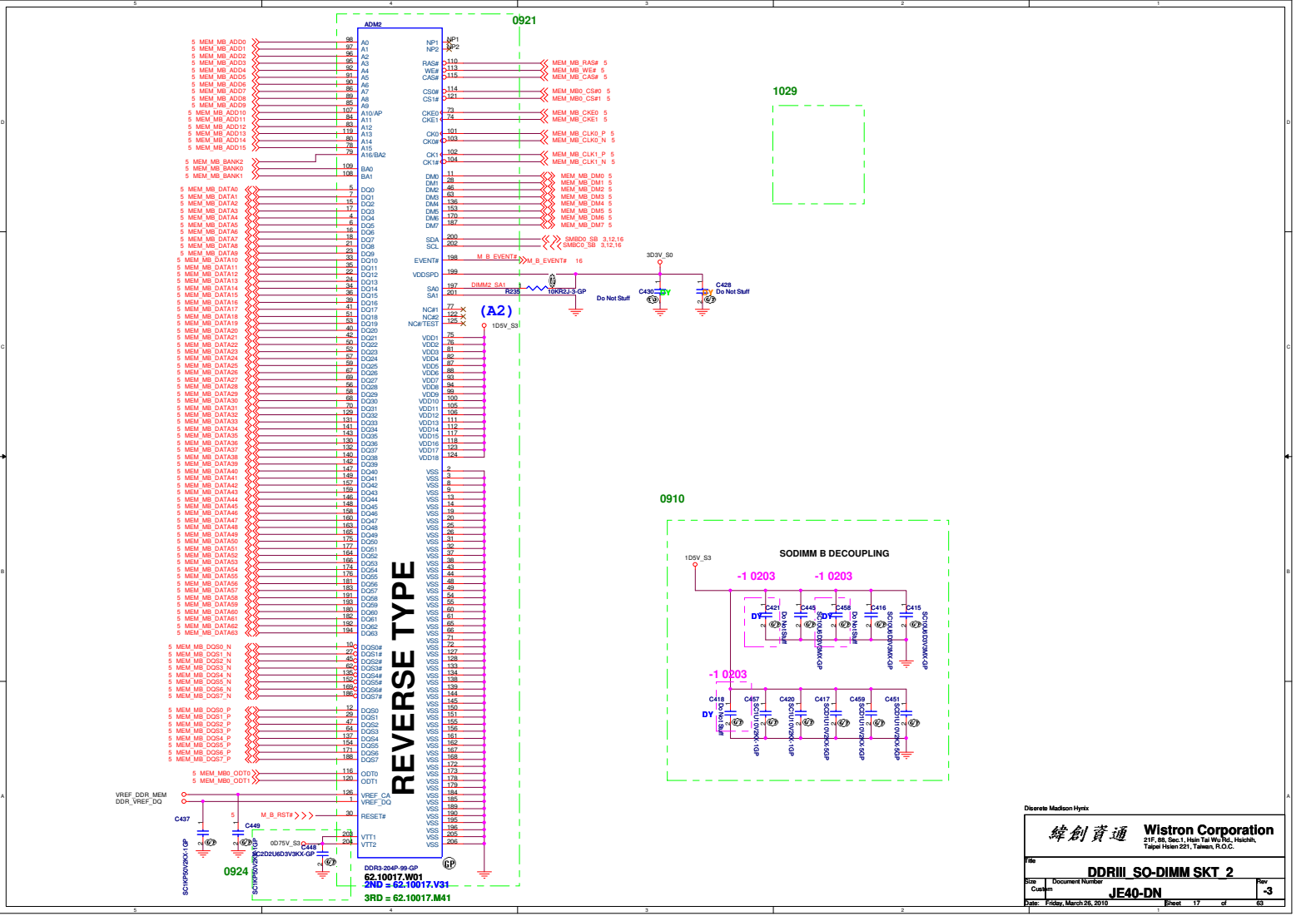
Taipei Hsien 221, Taiwan, R.O.C.

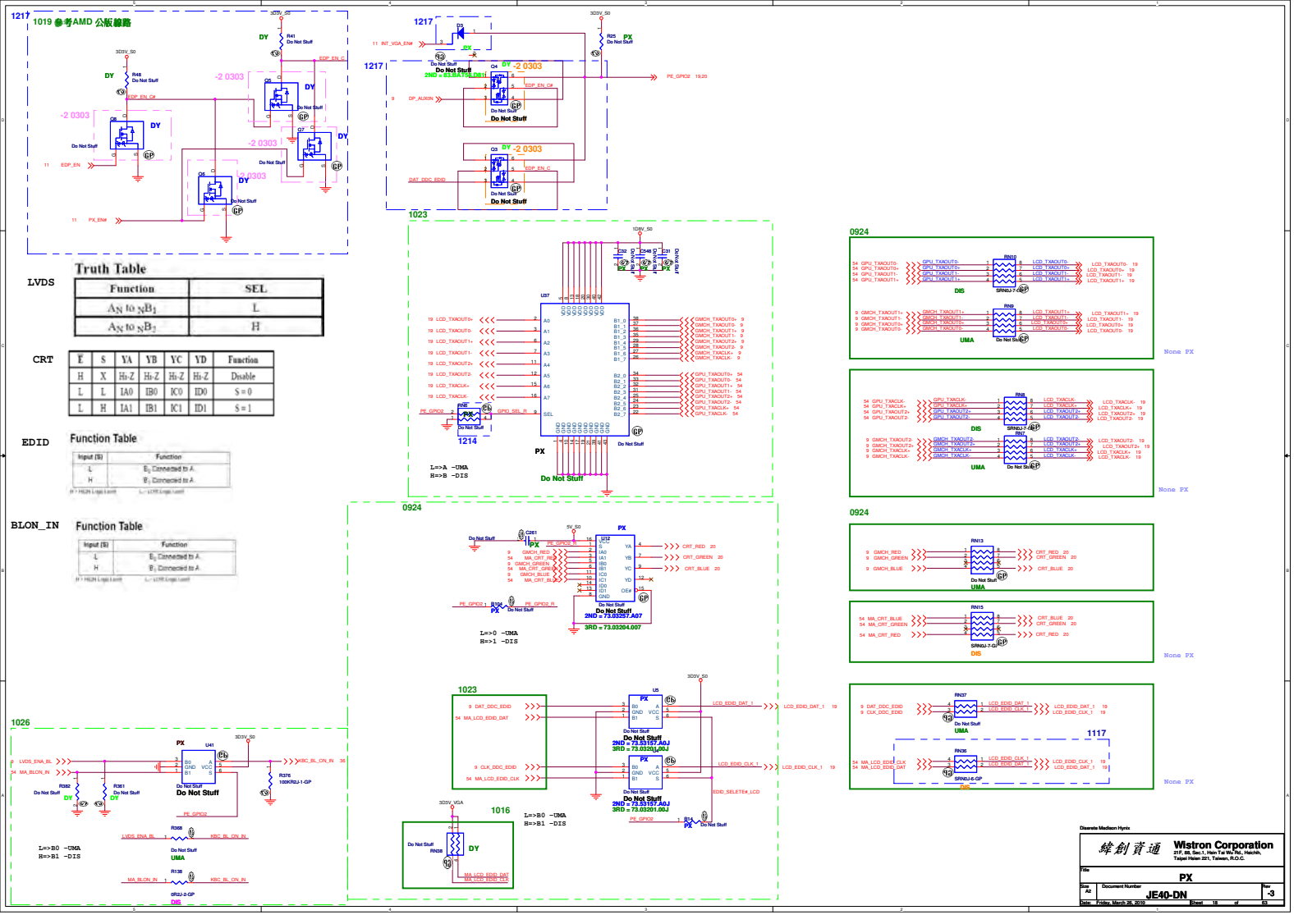
Title: ATI-SB820 STRAPPING (5/5)

Size: A3 | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 15 of 63


ADM1
STANDARD TYPE
DDR3-204P-S3-GP
62.10017.P91
2ND = 62.10017.V91
3RD = 62.10017.V41
0921
0907
Check if SB need
Memhot event
1029
0910
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
1021
1001
VREF_DDR_MEM
LAYOUT: Locate close to DIMM
DDR_VREF_MEM
DDR_VREF_DQ
Do Not Stuff
-1 0203
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII SO-DIMM SKT 1
JE40-DN
-3
Date: Friday, March 26, 2010
Sheet 16 of 63


ADM2
0921
1029
0910
REVERSE TYPE
(A2)
SODIMM B DECOUPLING
-1 0203
DDR3-204P-99-GP
62.10017.W01
2ND = 62.10017.V31
3RD = 62.10017.M41
0924
Do Not Stuff
Diserete Madison Hynix
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII_SO-DIMM SKT_2
JE40-DN
Size Custom
Document Number
Rev -3
Date: Friday, March 26, 2010
Sheet 17 of 63



LVDS

Truth Table

Function	SEL
A_N to $_NB_1$	L
A_N to $_NB_2$	H

CRT

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B_1 Connected to A
H	B_2 Connected to A

H = HIGH Logic Level L = LOW Logic Level

BLON_IN

Function Table

Input (S)	Function
L	B_1 Connected to A
H	B_2 Connected to A

H = HIGH Logic Level L = LOW Logic Level

LCD/INVERTER/CCD CONN

Change PX

0922

1028 for EMC request

0923

-1 0125

1005

0929 del CCD CON

-1 0208

1026

Reserve direct connector to KBC

-1 0125

1016

1005

JV42_DN SA

JV42_DN_PX SA

2ND = 20.F1289.040

20.F1093.040

JV42_DN_SA

define same as SJM50-PU,can use SJM50 Cable

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

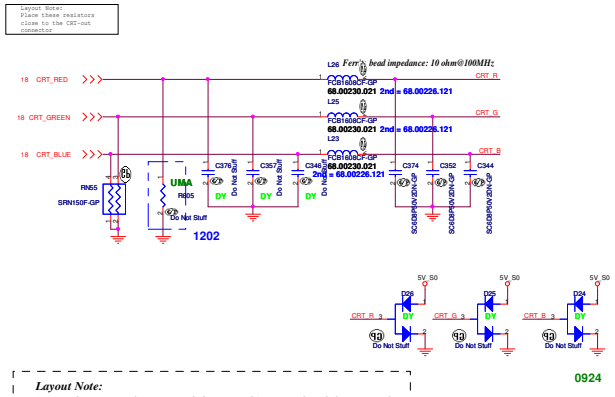
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

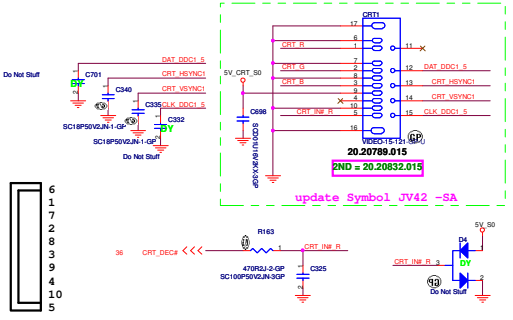
Size: Custom | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 19 of 63



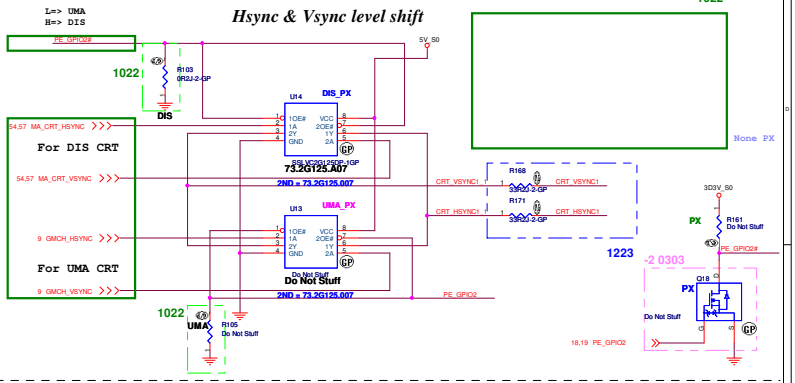
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



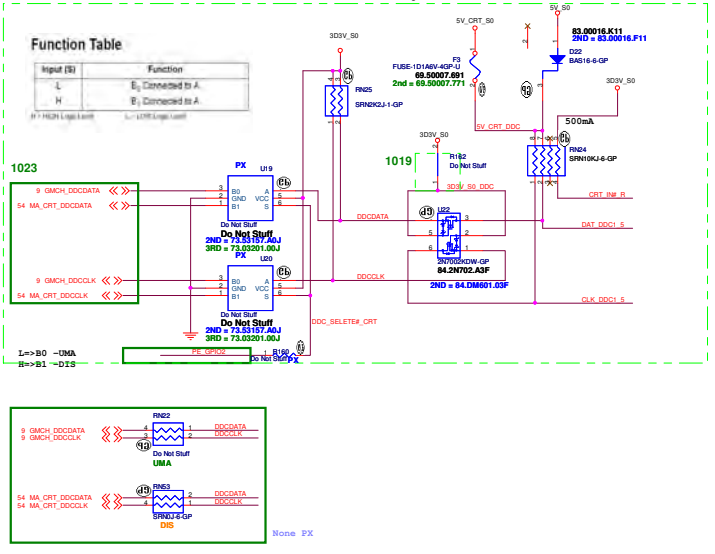
1012

Hsync & Vsync level shift



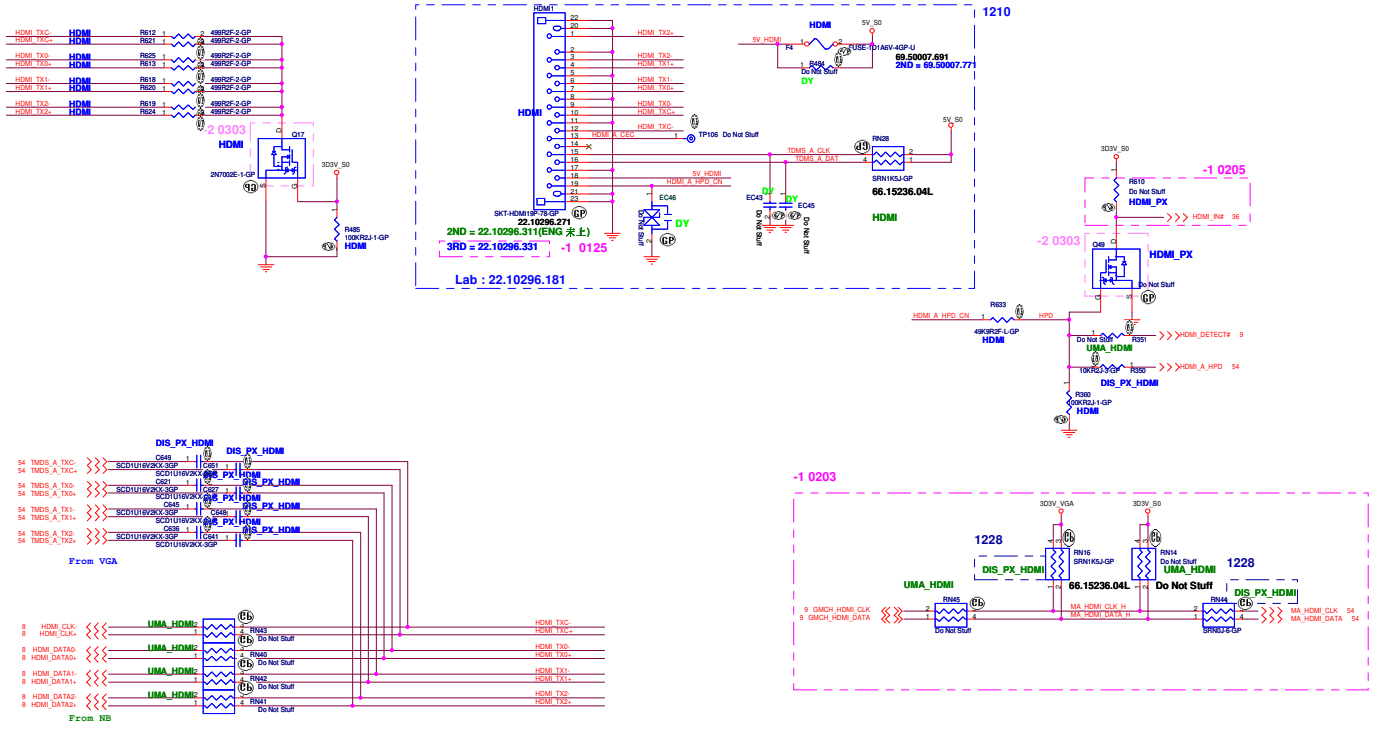
0924

DDC_CLK & DATA level shift



Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CRT Connector**
Size / Document Number	**JE40-DN**
Rev	-3
Date: Friday, March 26, 2010	Sheet 28 of 63

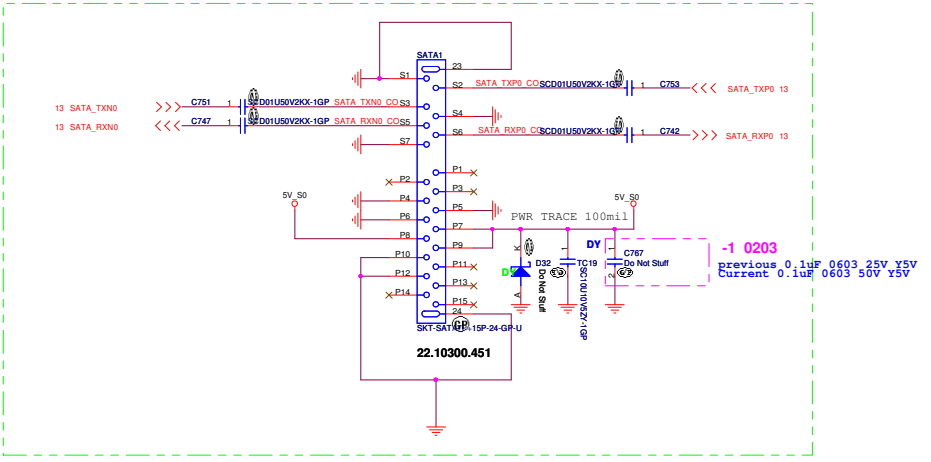


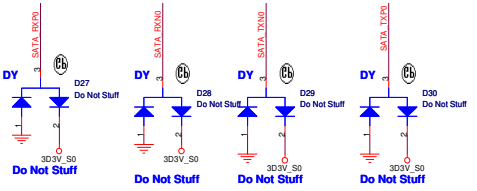
Discrete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Connector	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 21 of 63	

SATA Connector

0923

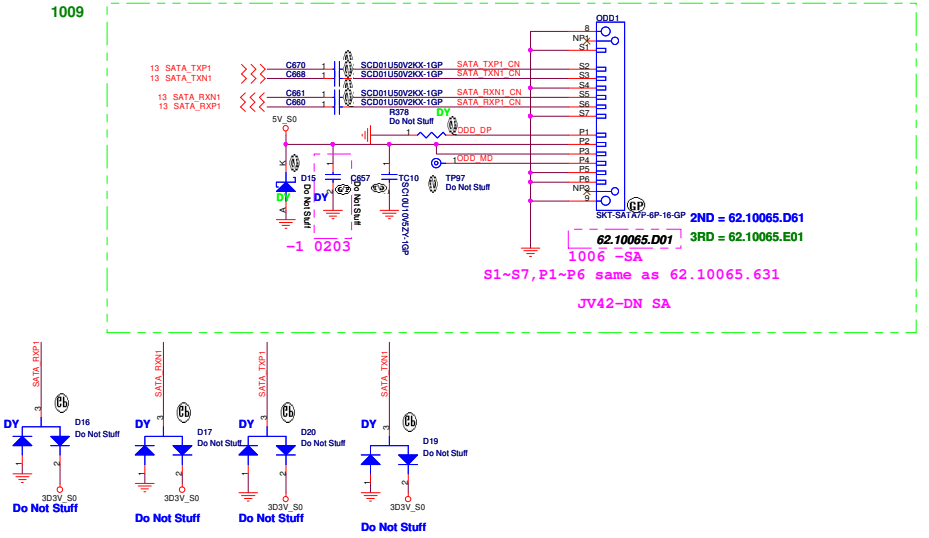




Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 22 of 63	

ODD Connector



Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

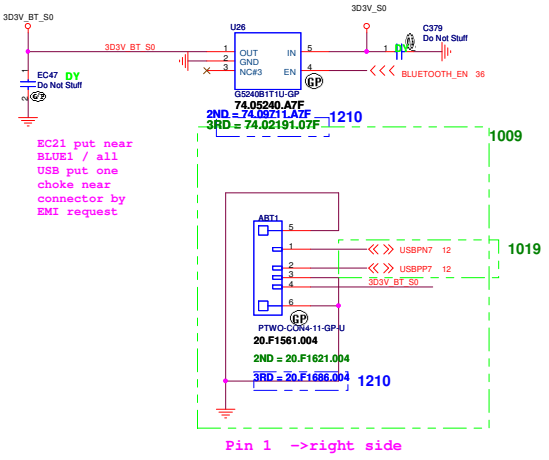
Title: ODD

Size | Document Number: JE40-DN | Rev: -3

Date: Friday, March 26, 2010 | Sheet 23 of 63

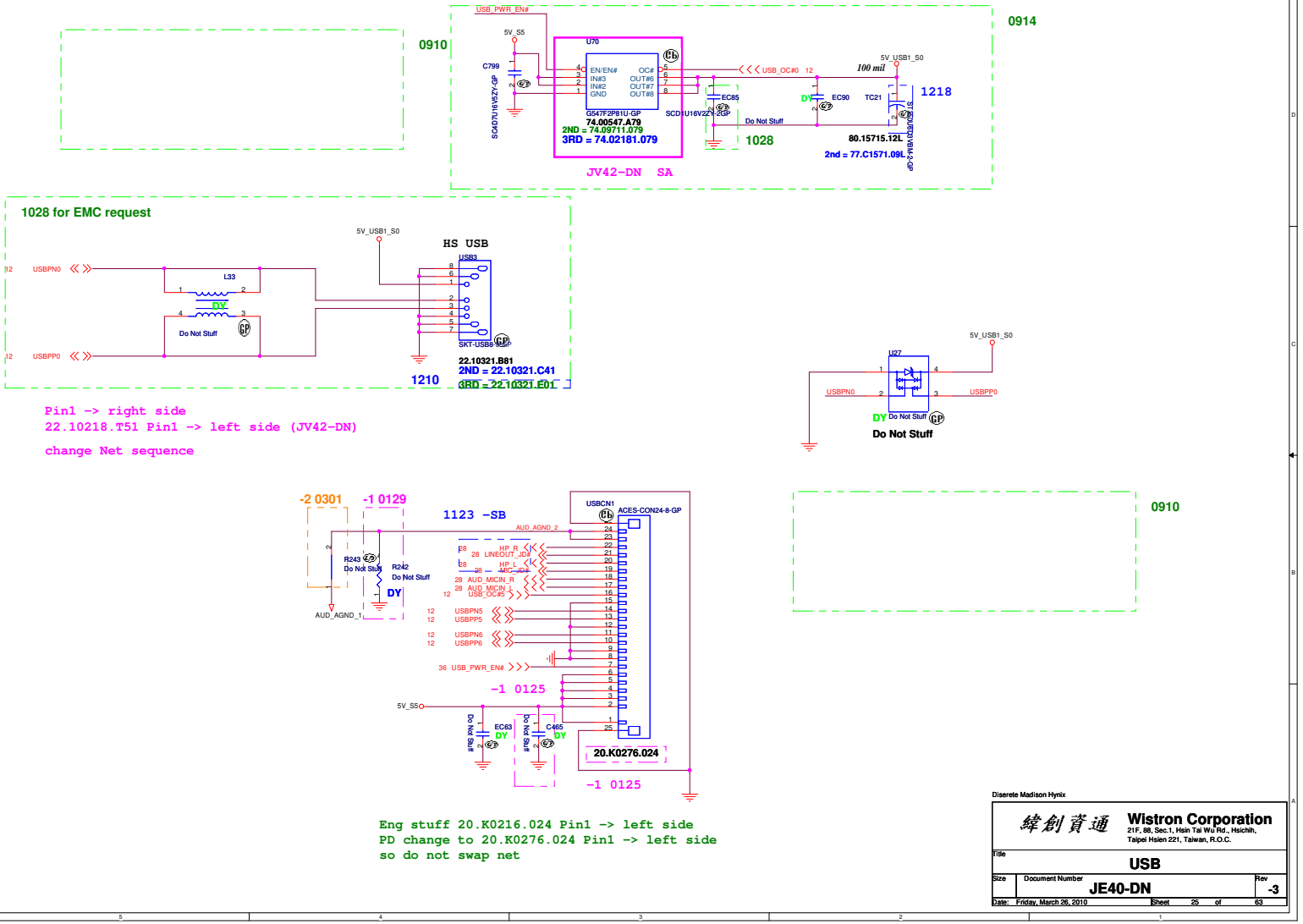
BLUETOOTH MODULE

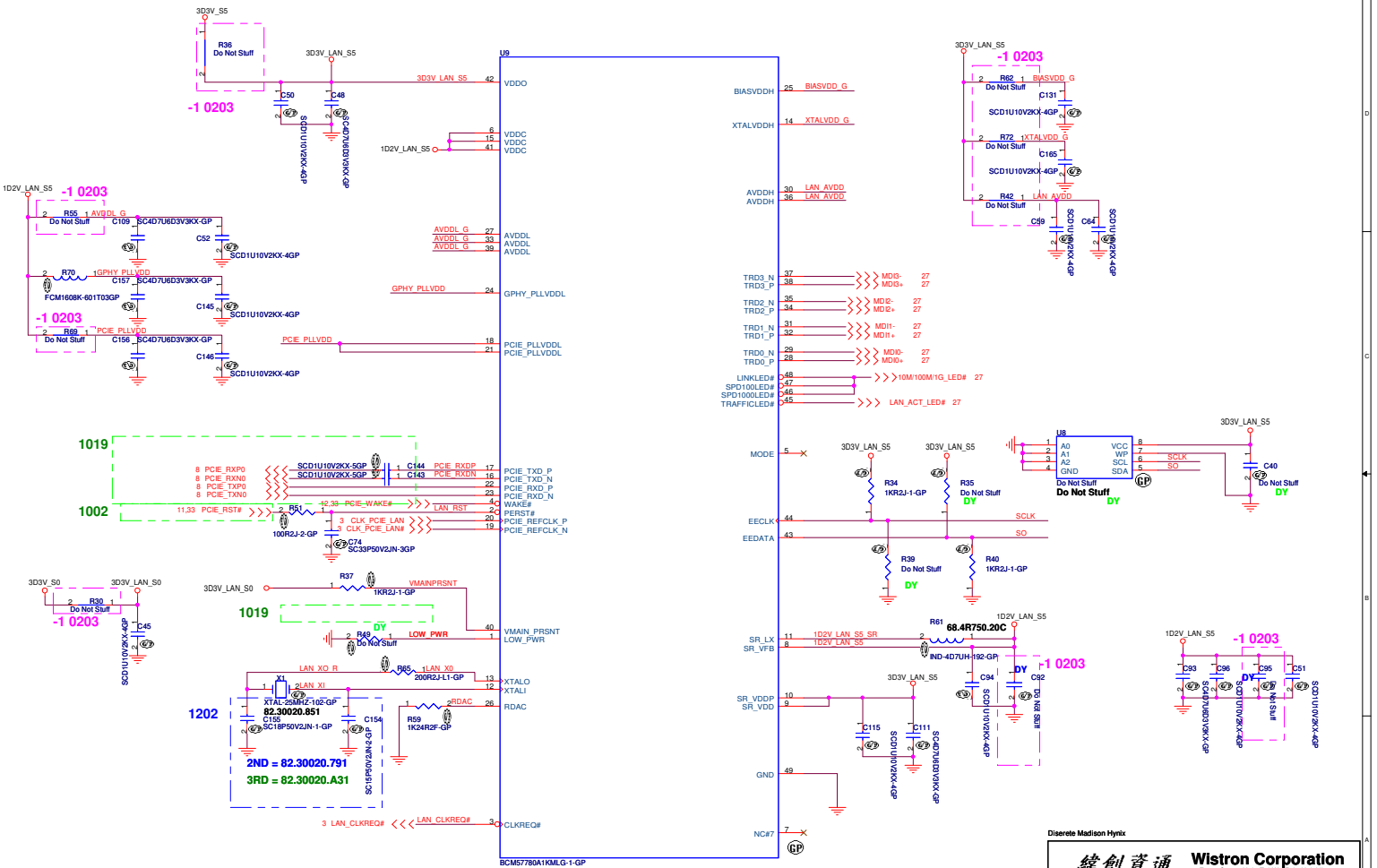
1.5A / High Active Voltage 2V



Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**BLUETOOTH**	
Size	Document Number **JE40-DN**	Rev **-3**
Date: Friday, March 26, 2010	Sheet 24 of 63	


0910
0914
USB_PWR_EN#
5V_S5
C799
SC4D7U16V6ZY-GP
U70
EN/EN#
IN#3
IN#2
GND
OC#
OUT#6
OUT#7
OUT#8
G547F2PB1U-GP
74.00547.A79
2ND = 74.09711.079
3RD = 74.02181.079
JV42-DN SA
USB_OC#0 12
100 mil
5V_USB1_S0
EC85
SCD1U16V2ZY-2GP
Do Not Stuff
1028
DY
EC90
TC21
1218
80.15715.12L
2nd = 77.C1571.09L
1028 for EMC request
5V_USB1_S0
HS USB
USB3
USBPN0
USBPP0
L33
DY
Do Not Stuff
SKT-USB8-GP
22.10321.B81
2ND = 22.10321.C41
3RD = 22.10321.E01
1210
Pin1 -> right side
22.10218.T51 Pin1 -> left side (JV42-DN)
change Net sequence
5V_USB1_S0
U27
USBPN0
USBPP0
DY Do Not Stuff
Do Not Stuff
-2 0301
-1 0129
1123 -SB
AUD_AGND_2
R243
Do Not Stuff
R242
Do Not Stuff
DY
AUD_AGND_1
USBCN1
ACES-CON24-8-GP
HP_R
LINEOUT_JD#
HP_L
MIC_JD#
AUD_MICIN_R
AUD_MICIN_L
USB_OC#5
USBPN5
USBPP5
USBPN6
USBPP6
USB_PWR_EN#
-1 0125
5V_S5
EC83
C465
DY
Do Not Stuff
20.K0276.024
-1 0125
0910
Eng stuff 20.K0216.024 Pin1 -> left side
PD change to 20.K0276.024 Pin1 -> left side
so do not swap net
Diserete Madison Hynix
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB
Size
Document Number
JE40-DN
Rev
-3
Date: Friday, March 26, 2010
Sheet 25 of 63



71.57780.M04

Diserete Madison Hynix

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM57780**

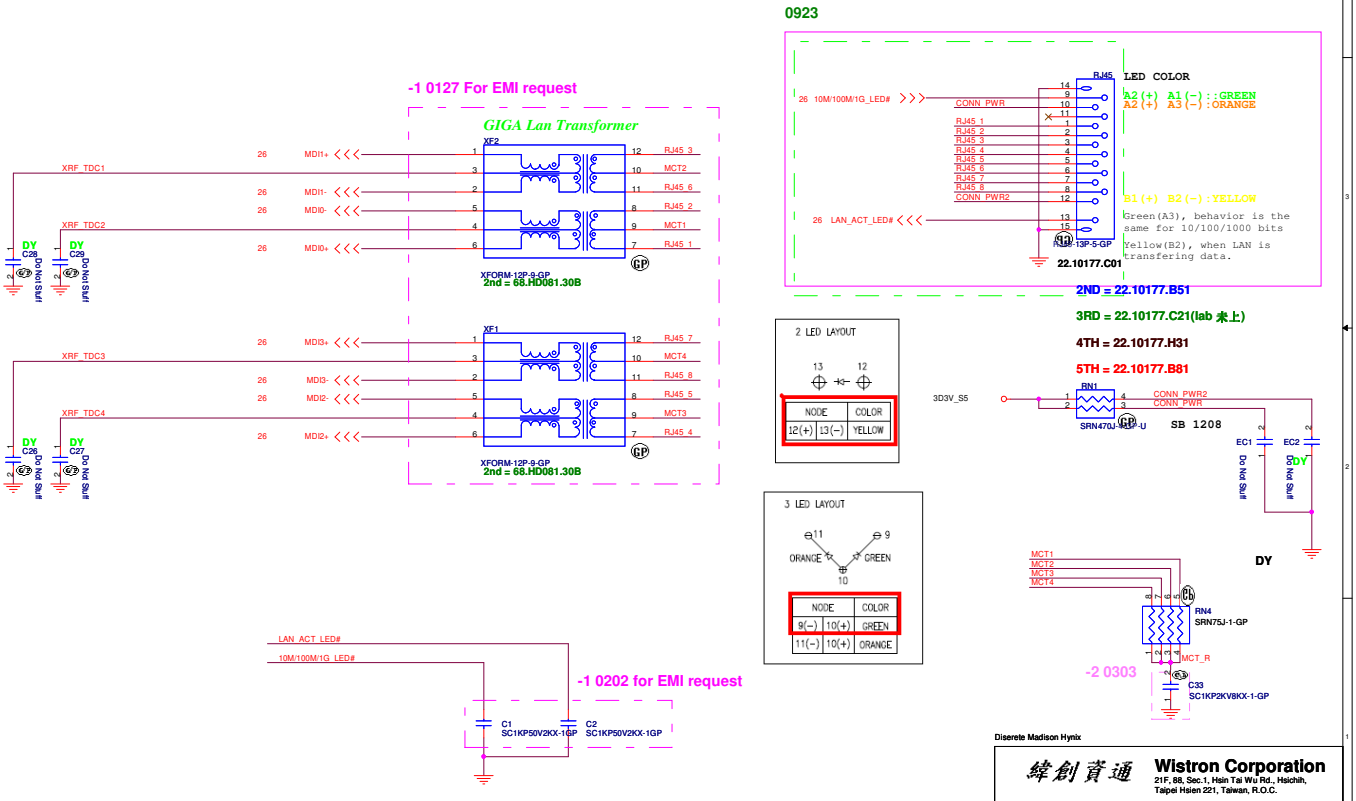
Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 26 of 63

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

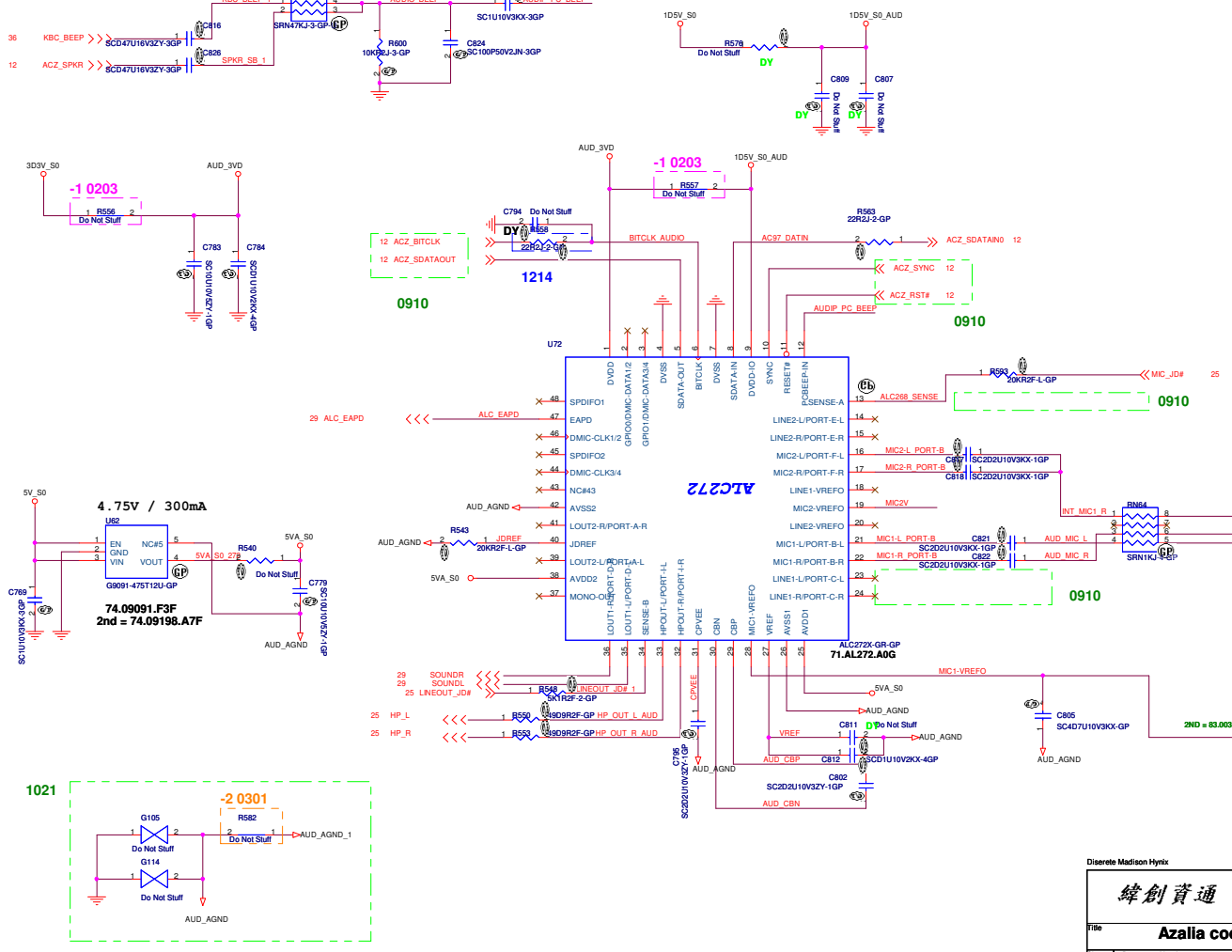
LAN Connector



Diserete Madison Hynix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	LAN CONN	
Size A3	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 27 of 63	



Diserete Madison Hynix

Wistron Corporation
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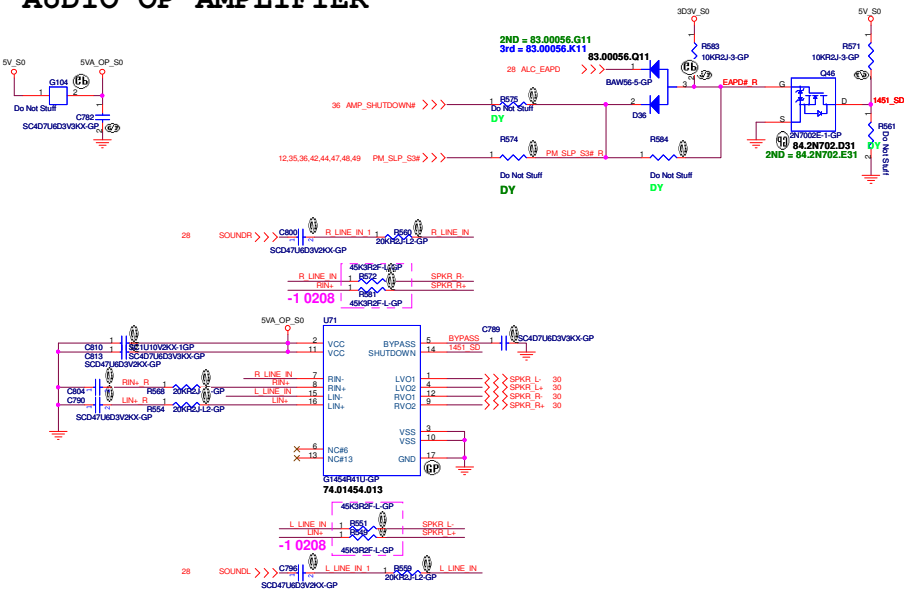
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC272**

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 28 of 63

AUDIO OP AMPLIFIER

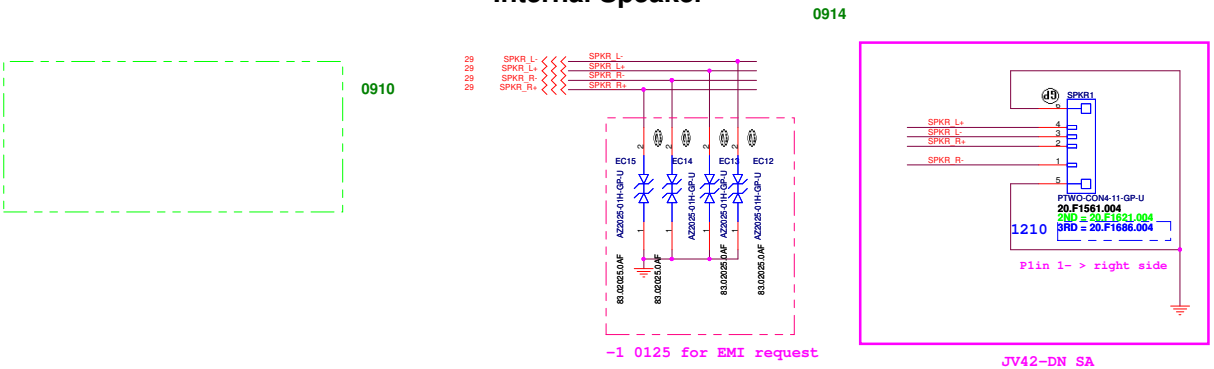



```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W
```

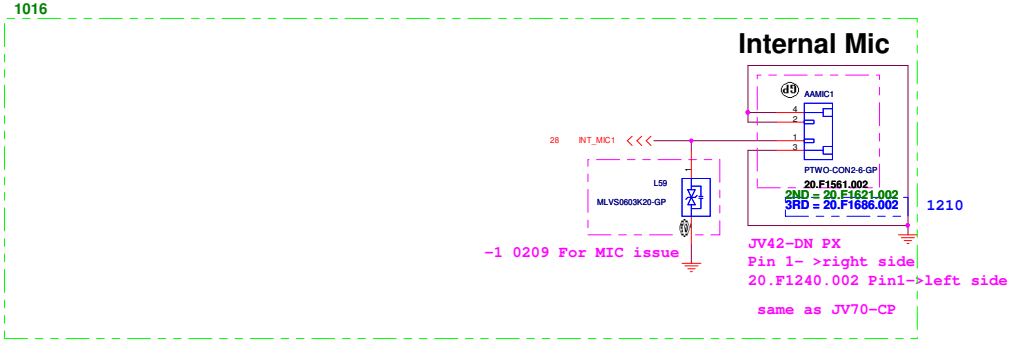
Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 29 of 63	

Internal Speaker



LINE OUT



Diserete Madison Hynix

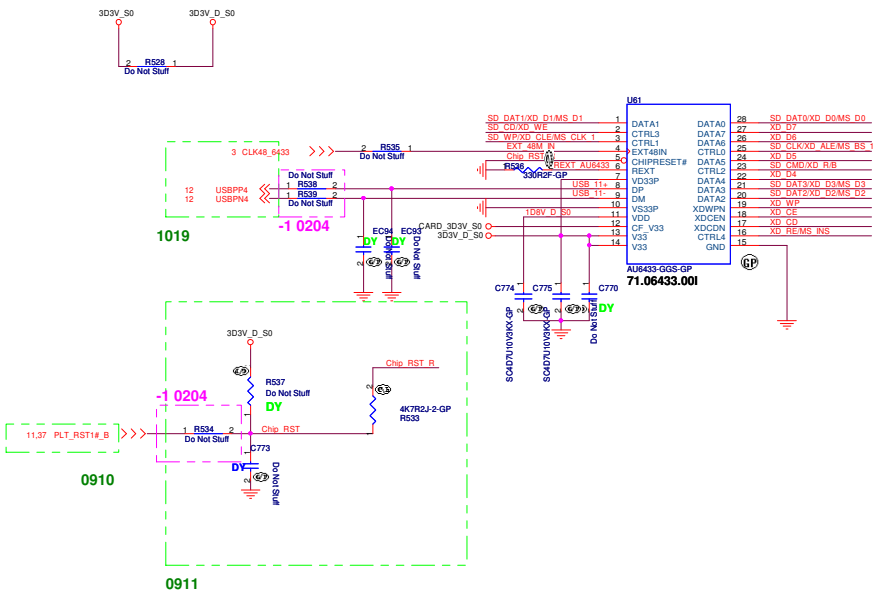
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 30 of 63	

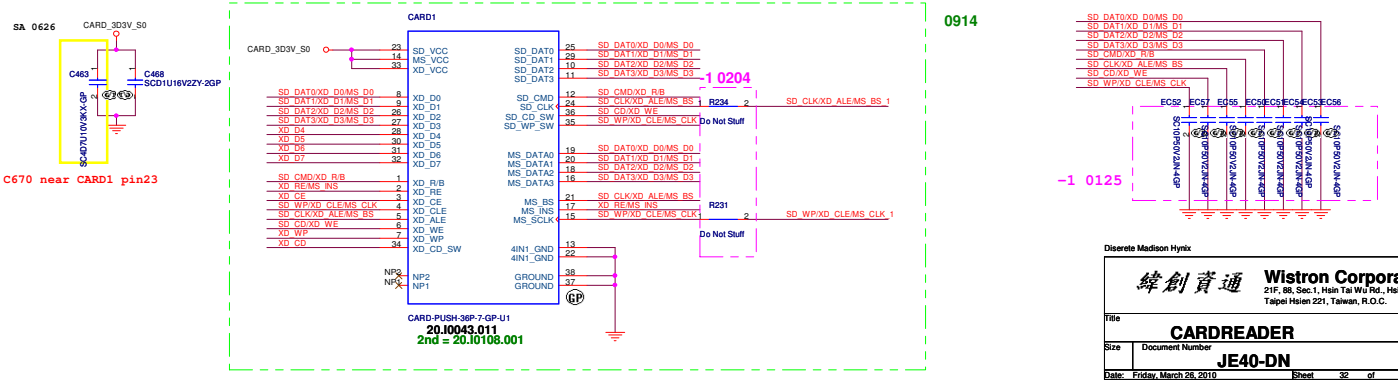
No Modem Function

Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MDC	
Size	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 31 of 63	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



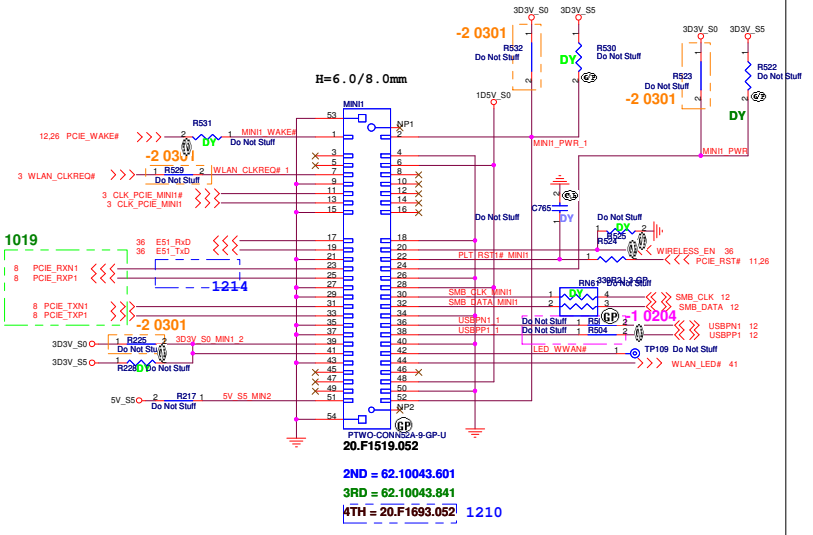
Diserete Madison Hynix

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

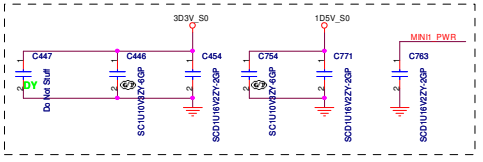
Title	CARDREADER		
Size	Document Number: JE40-DN		Rev: -3
Date: Friday, March 28, 2010	Sheet 32 of 63		

Mini Card Connector(WLAN)

0923



Place near MINI1



No Mini Card Function (Robson2 and 3G)

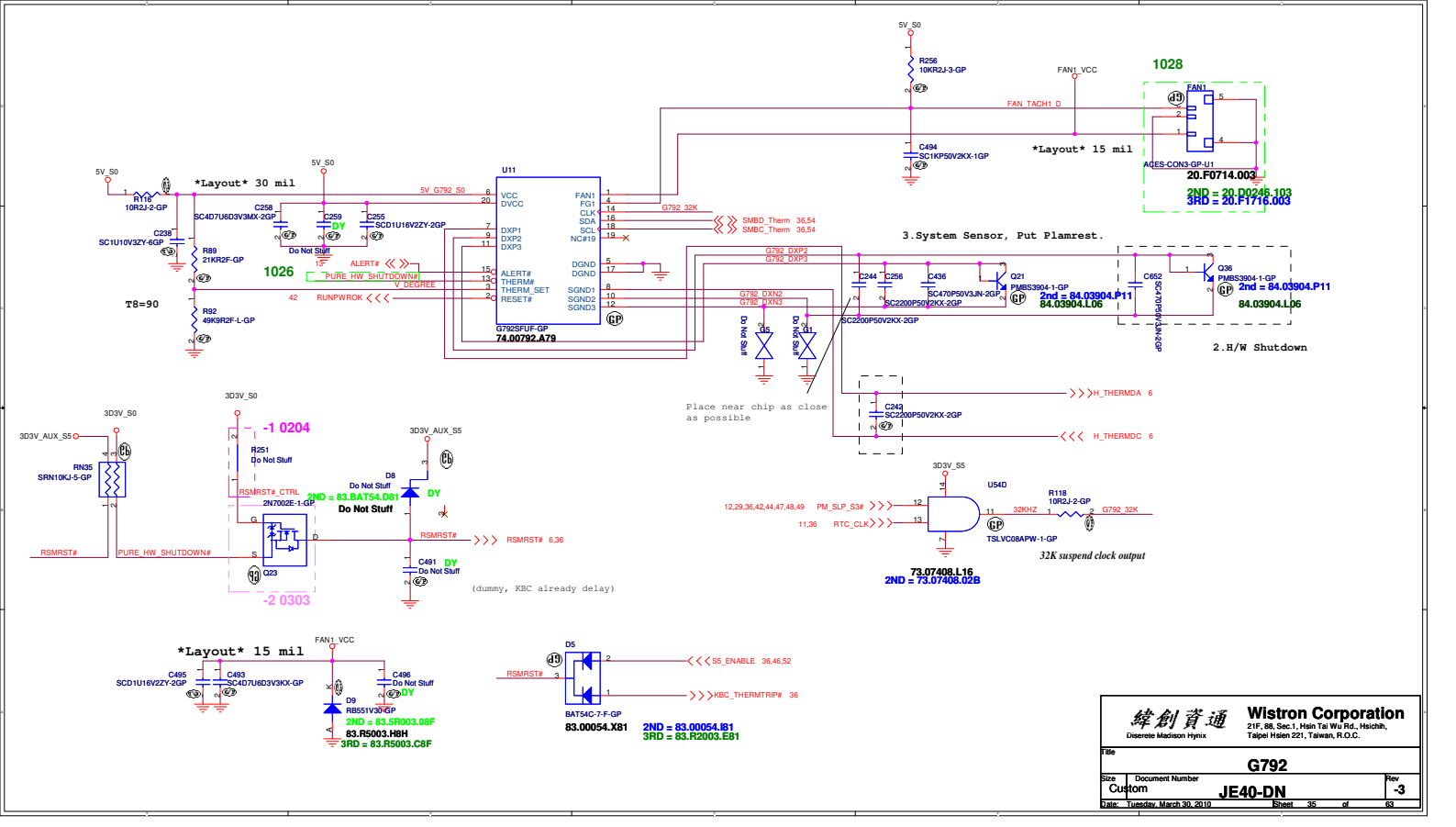
Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 33 of 63	

No NEWCARD Function

Diserete Madison Hynix

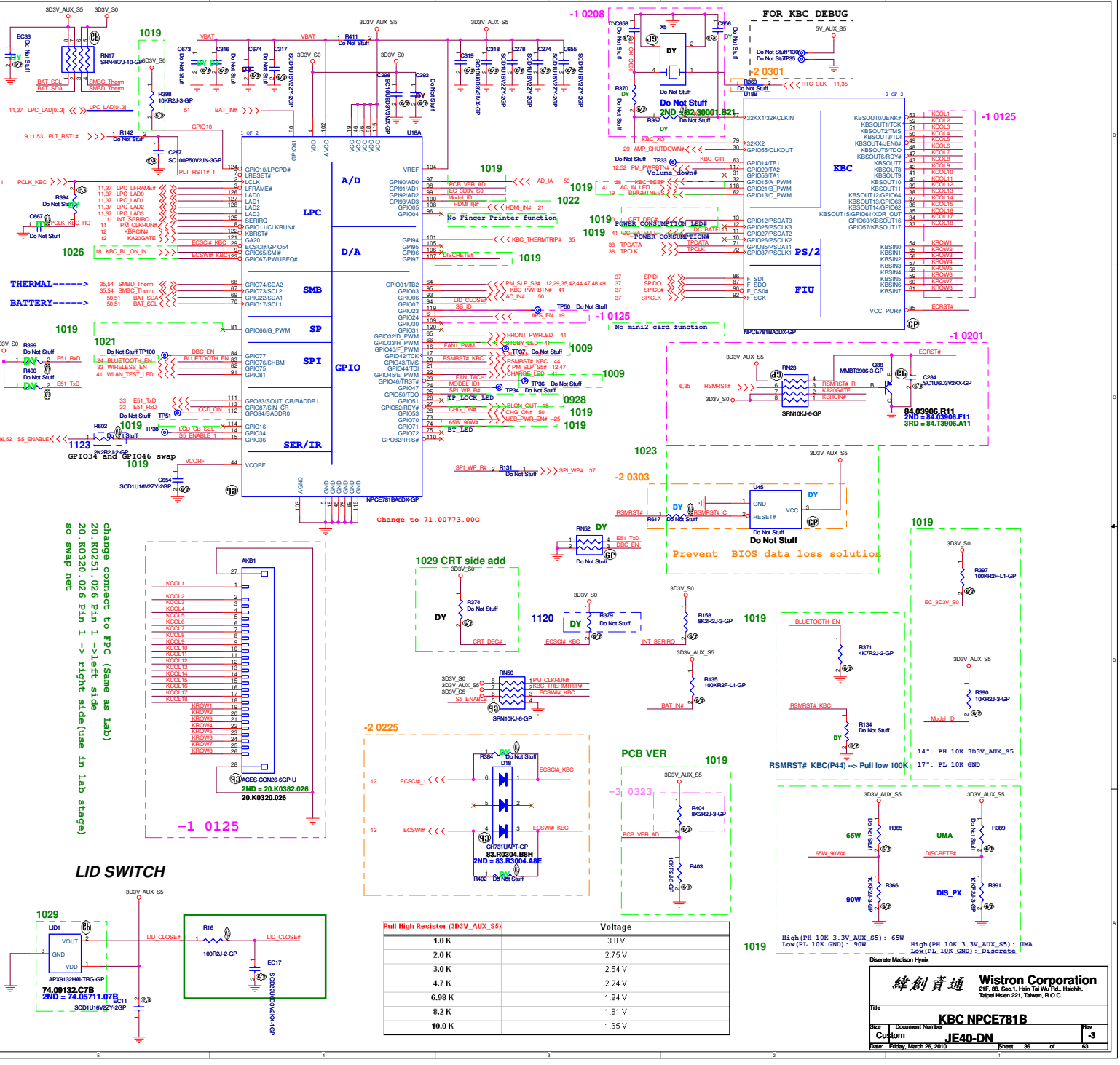
緯創資通	**Wistron Corporation** 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**NEW CARD**
Size / Document Number	**JE40-DN** / Rev **-3**
Date: Friday, March 26, 2010	Sheet 34 of 63



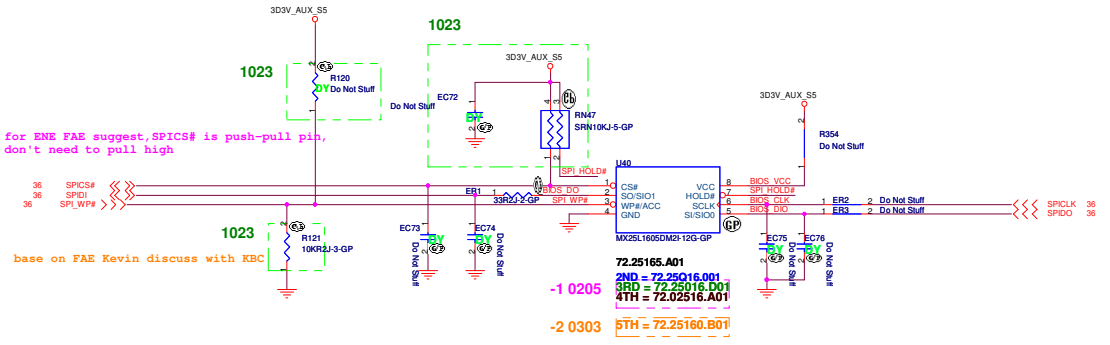
緯創資通
Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G792	
Size: Custom	Document Number: JE40-DN	Rev: -3
Date: Tuesday, March 30, 2010	Sheet 35 of 63	



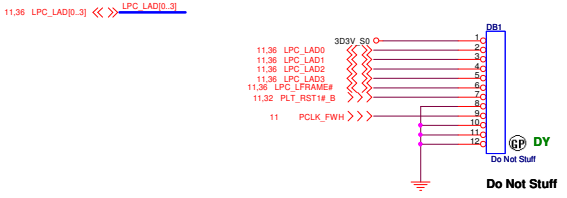
Pull-High Resistor (3D3V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V



3rd 4th source LAB ENG未上

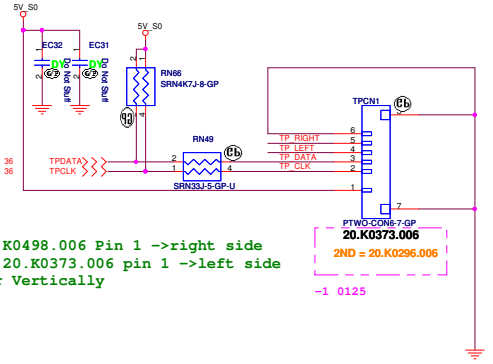
16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD

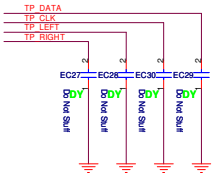


Diserete Madison Hynix

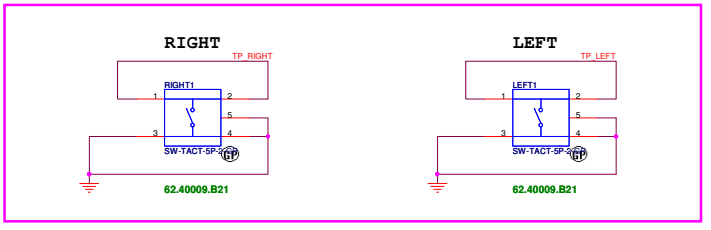
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BIOS	
Size A3	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 37 of 63	



Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically



-1 0205



No Finger printer Function

Diserete Madison Hynix

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD

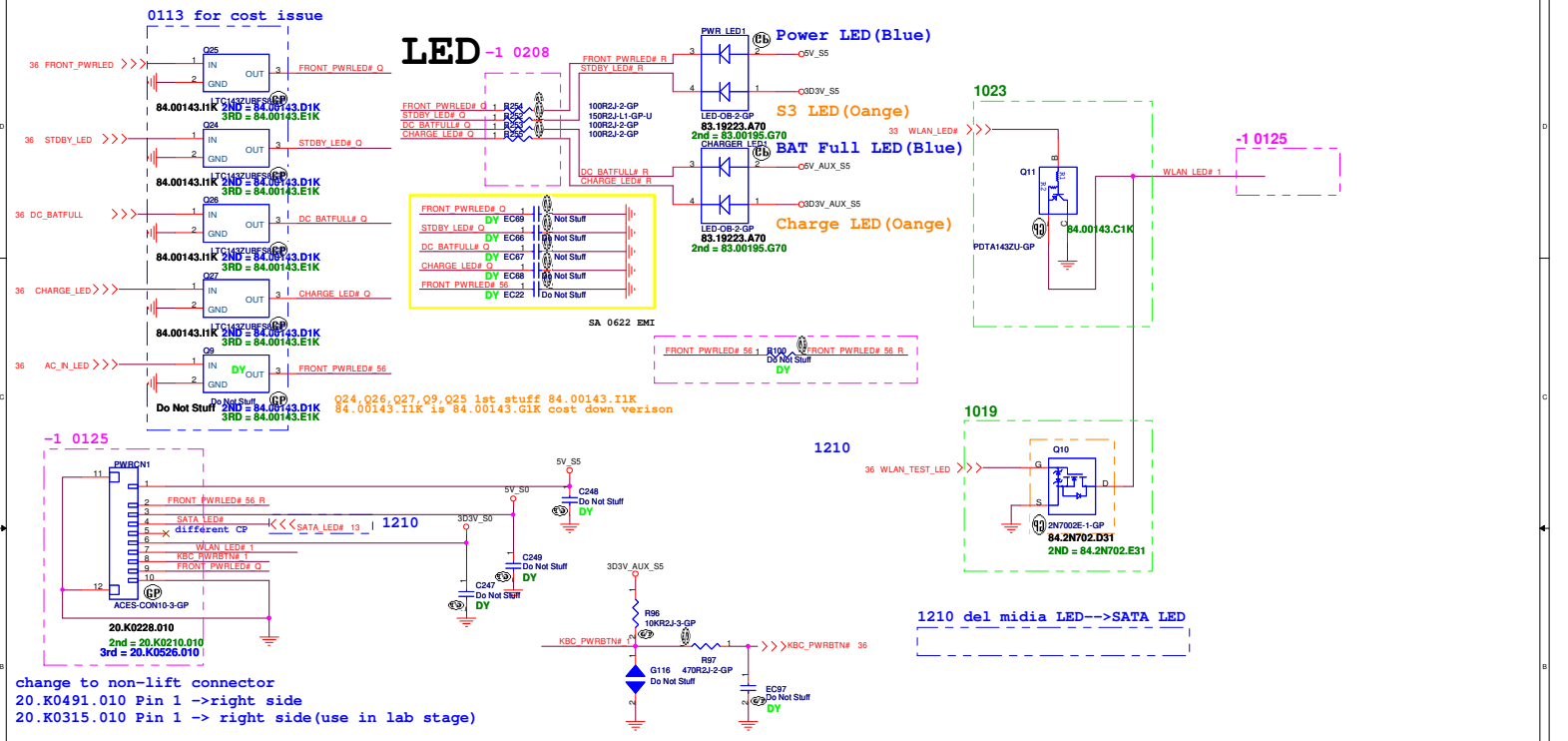
Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 38 of 63

NONE BOARD

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	NONE BOARD	
Size A3	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 39 of 63	

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SWITCH	
Size: A2	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 40 of 63	



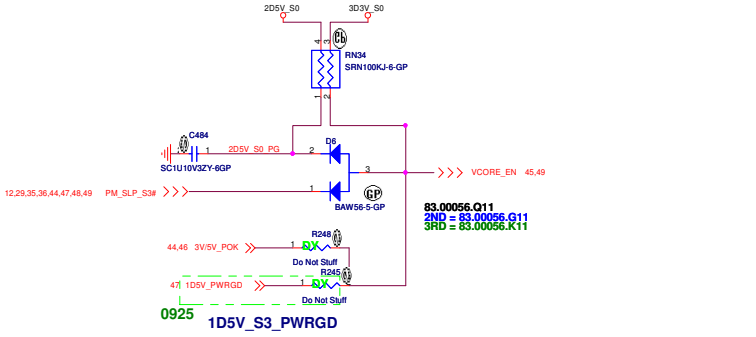
Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	SATA_LED#	HDD
Pin 5	NA	
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

緯創資通 **Wistron Corporation**
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

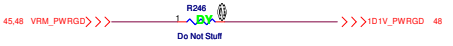
Title: **LED**

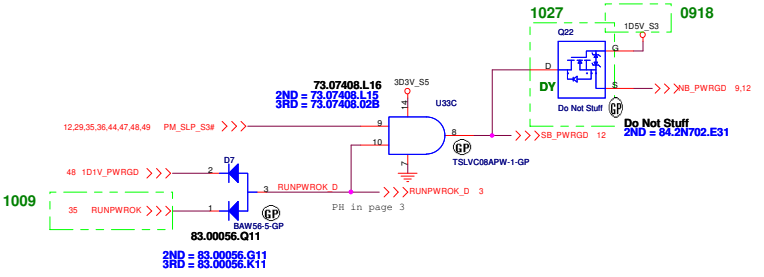
Size: A3 | Document Number: **JE40-DN** | Rev: -3

Date: Friday, March 26, 2010 | Sheet 41 of 63



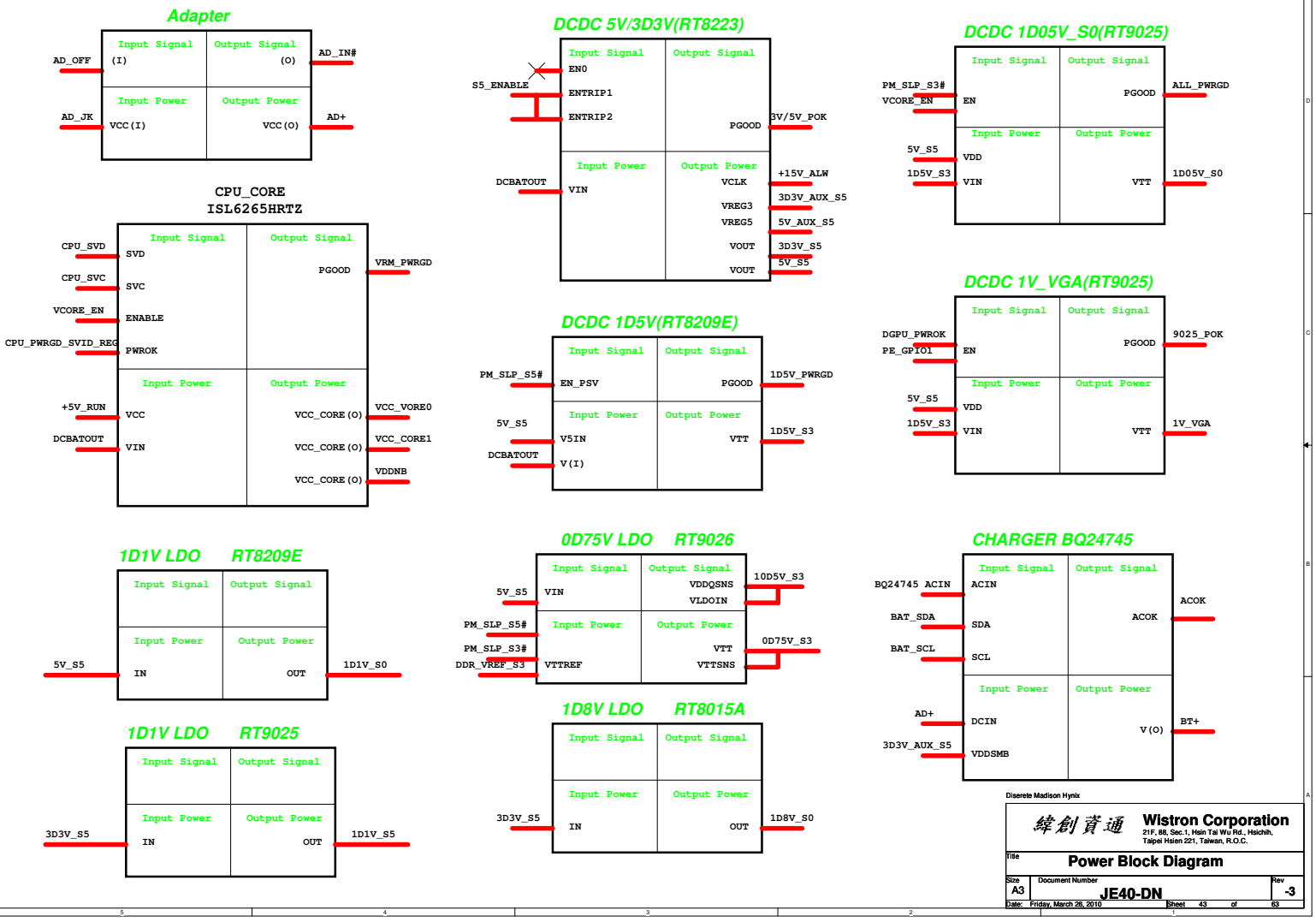
P/H @ 1D8V_S3 PAGE





Diserete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	POWER ON LOGIC	
Size A3	Document Number JE40-DN	Rev -3
Date: Friday, March 26, 2010	Sheet 42 of 63	



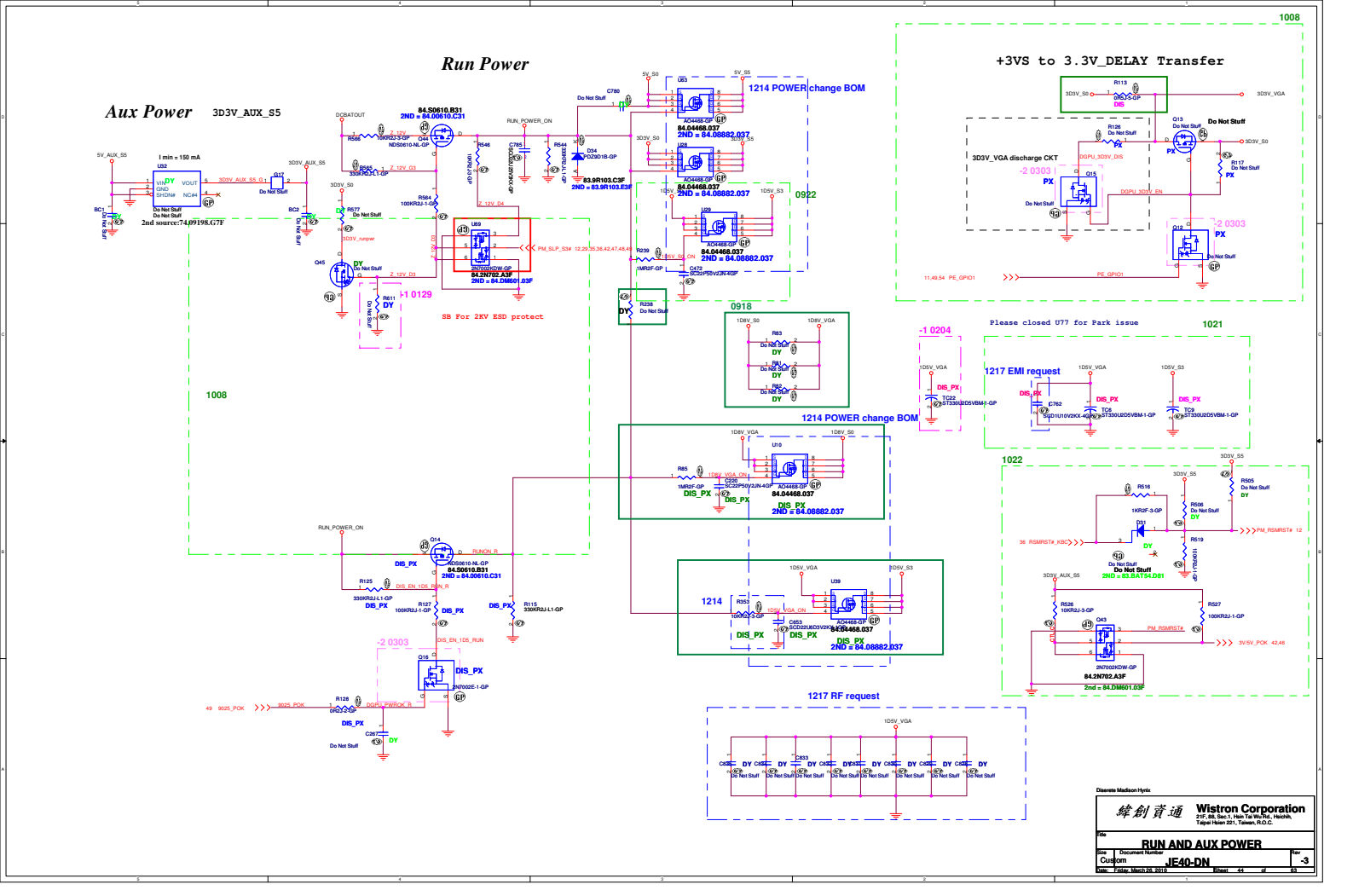
Diserete Madison Hynix

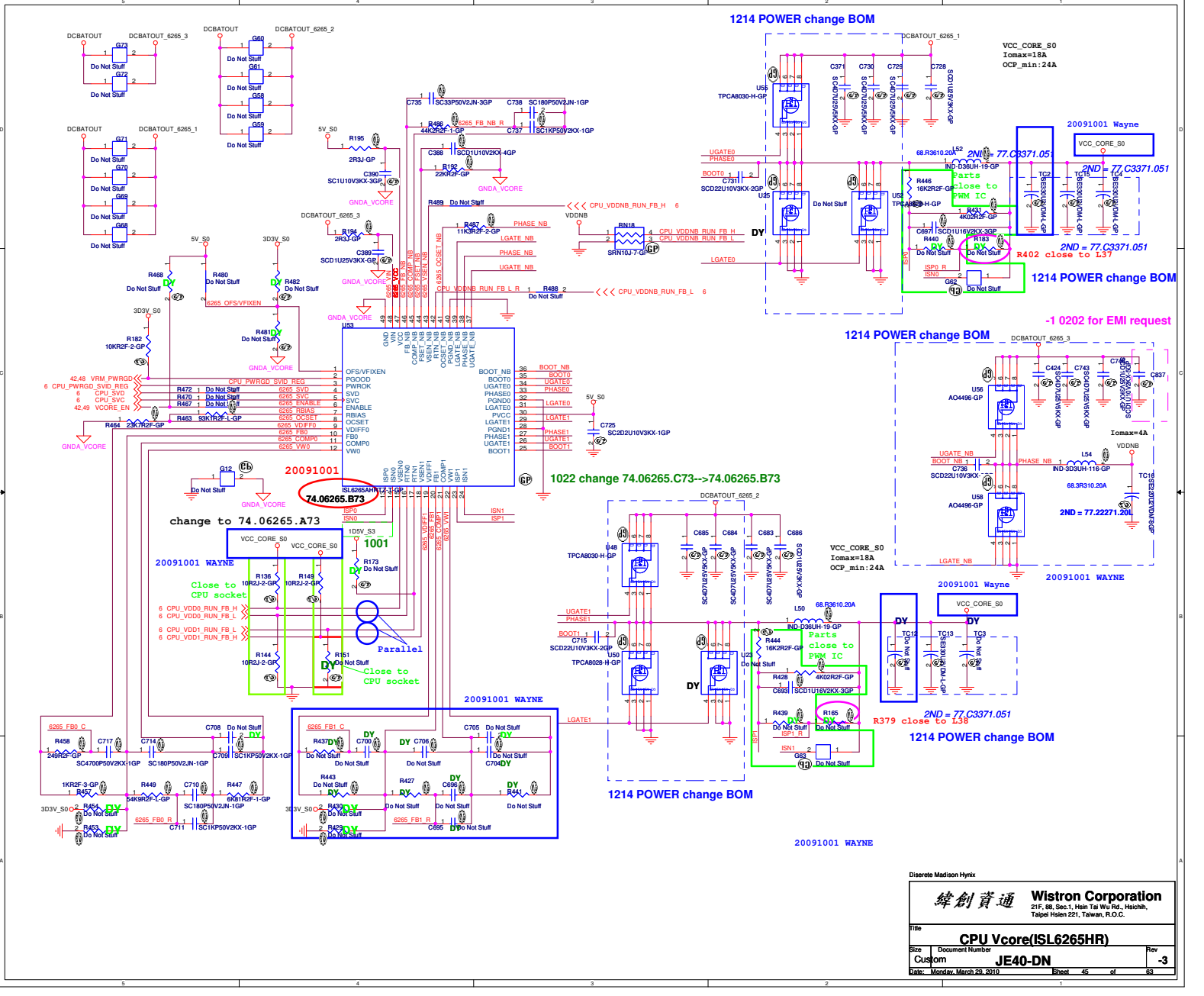
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

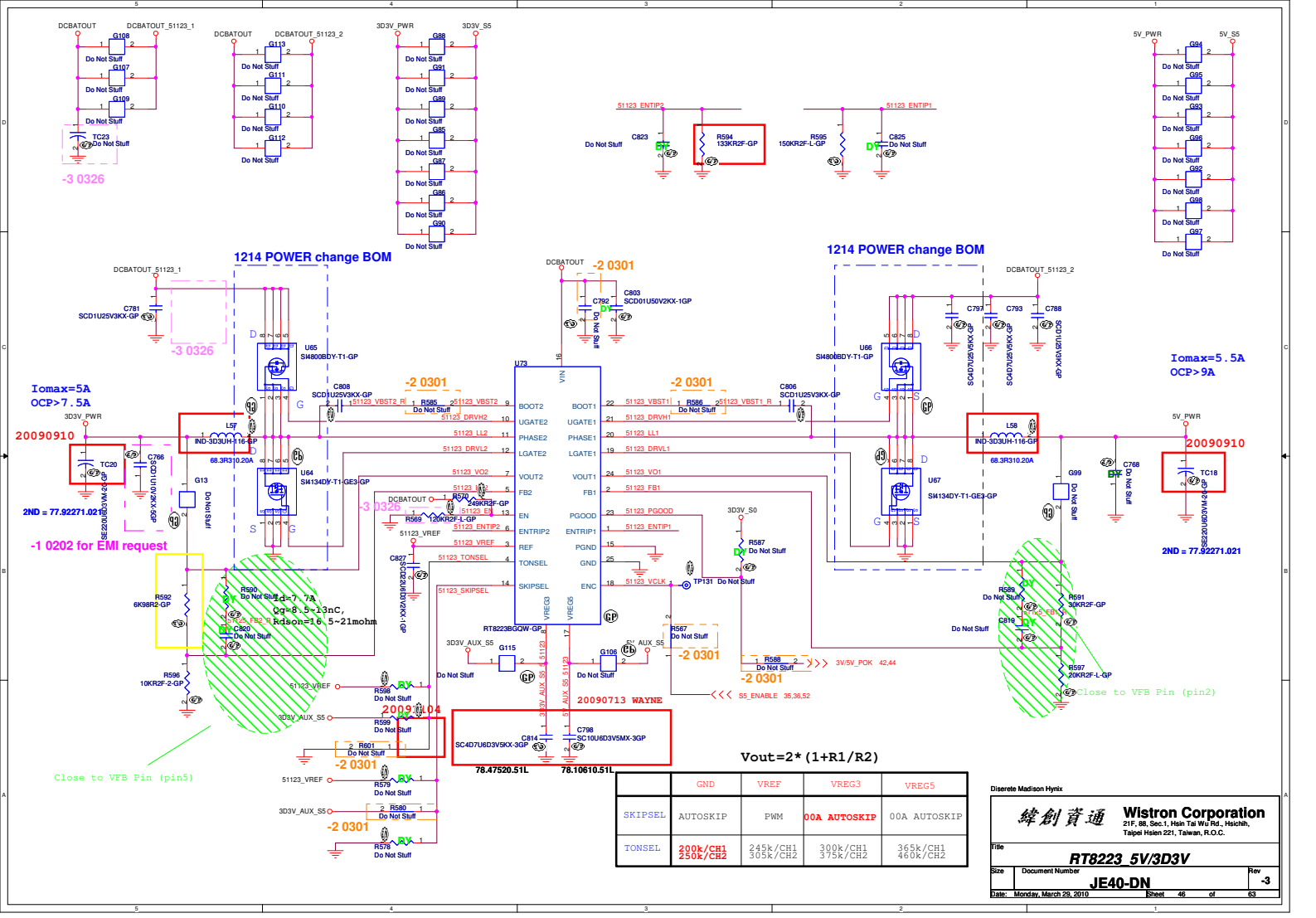
Title: Power Block Diagram

Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 43 of 63


Run Power
Aux Power
3D3V_AUX_S5
+3VS to 3.3V_DELAY Transfer
3D3V_VGA discharge CKT
1214 POWER change BOM
1217 EMI request
1217 RF request
Please closed U77 for Park issue
SB For 2KV ESD protect
Wistron Corporation
RUN AND AUX POWER
JE40-DN


1214 POWER change BOM
VCC_CORE_S0
Iomax=18A
OCP_min:24A
20091001 Wayne
2ND = 77.C3371.051
Parts close to PWM IC
R402 close to L37
-1 0202 for EMI request
Iomax=4A
2ND = 77.22271.20L
20091001 WAYNE
1022 change 74.06265.C73-->74.06265.B73
20091001
74.06265.B73
change to 74.06265.A73
1001
Close to CPU socket
Parallel
R379 close to L38
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore(ISL6265HR)
Size
Custom
Document Number
JE40-DN
Rev
-3
Date: Monday, March 29, 2010
Sheet 45 of 63



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

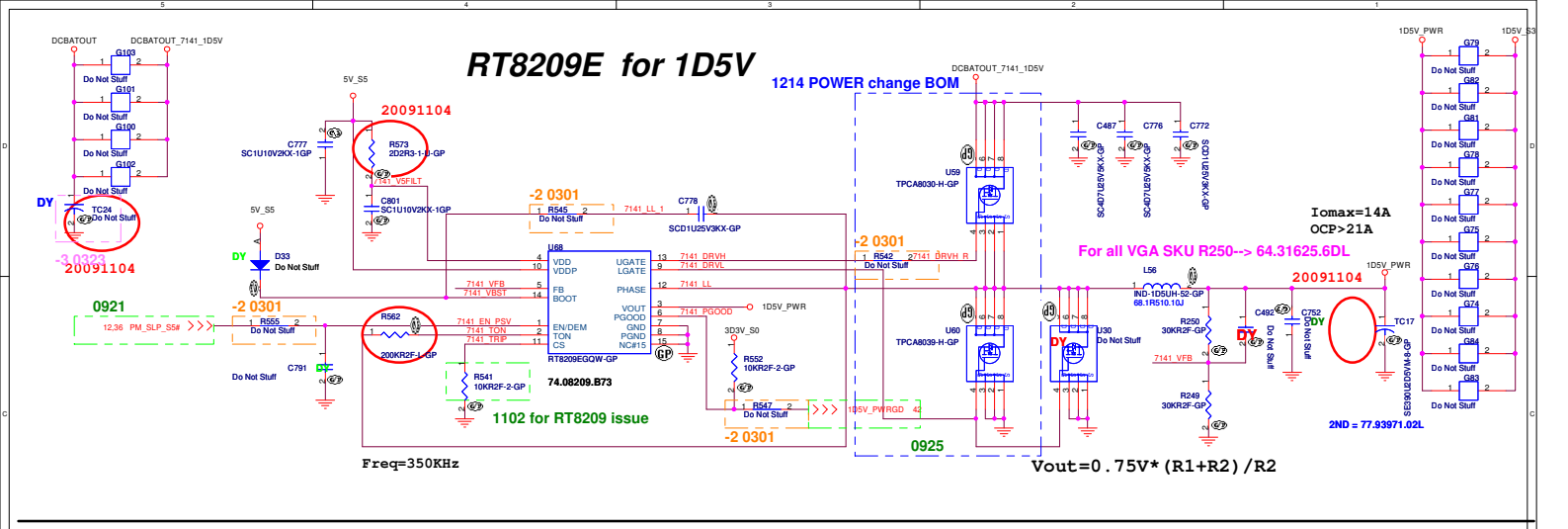
Diserete Madison Hynix

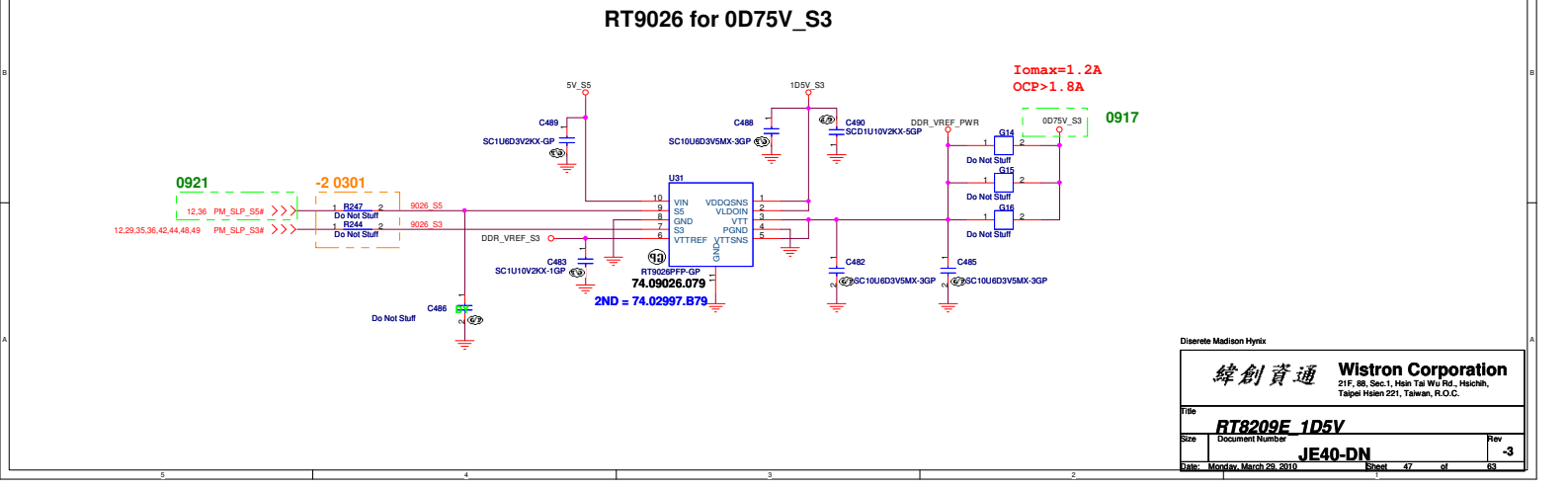
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

Size: | Document Number: JE40-DN | Rev: -3

Date: Monday, March 29, 2010 | Sheet 46 of 63



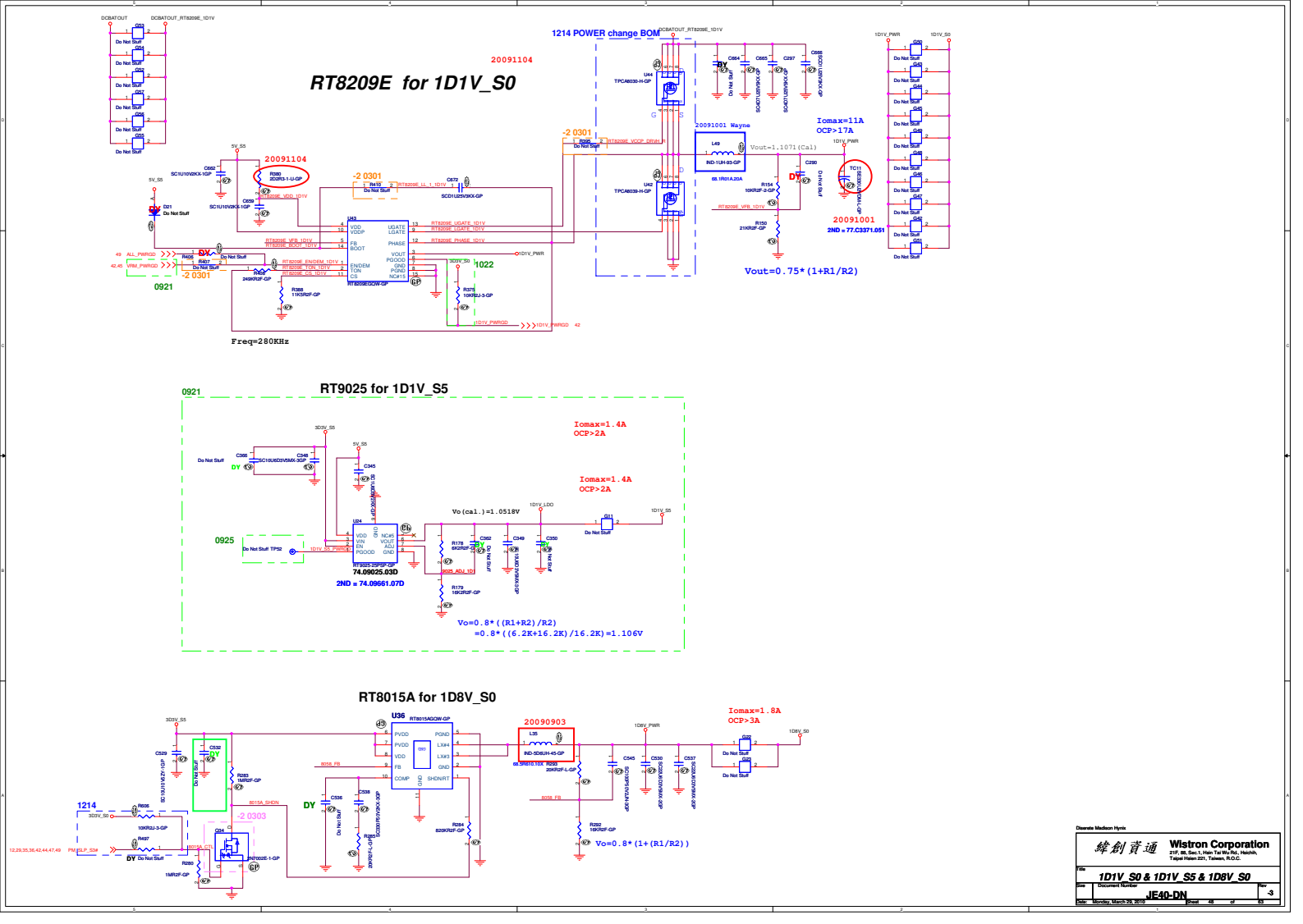


Diserete Madison Hynix

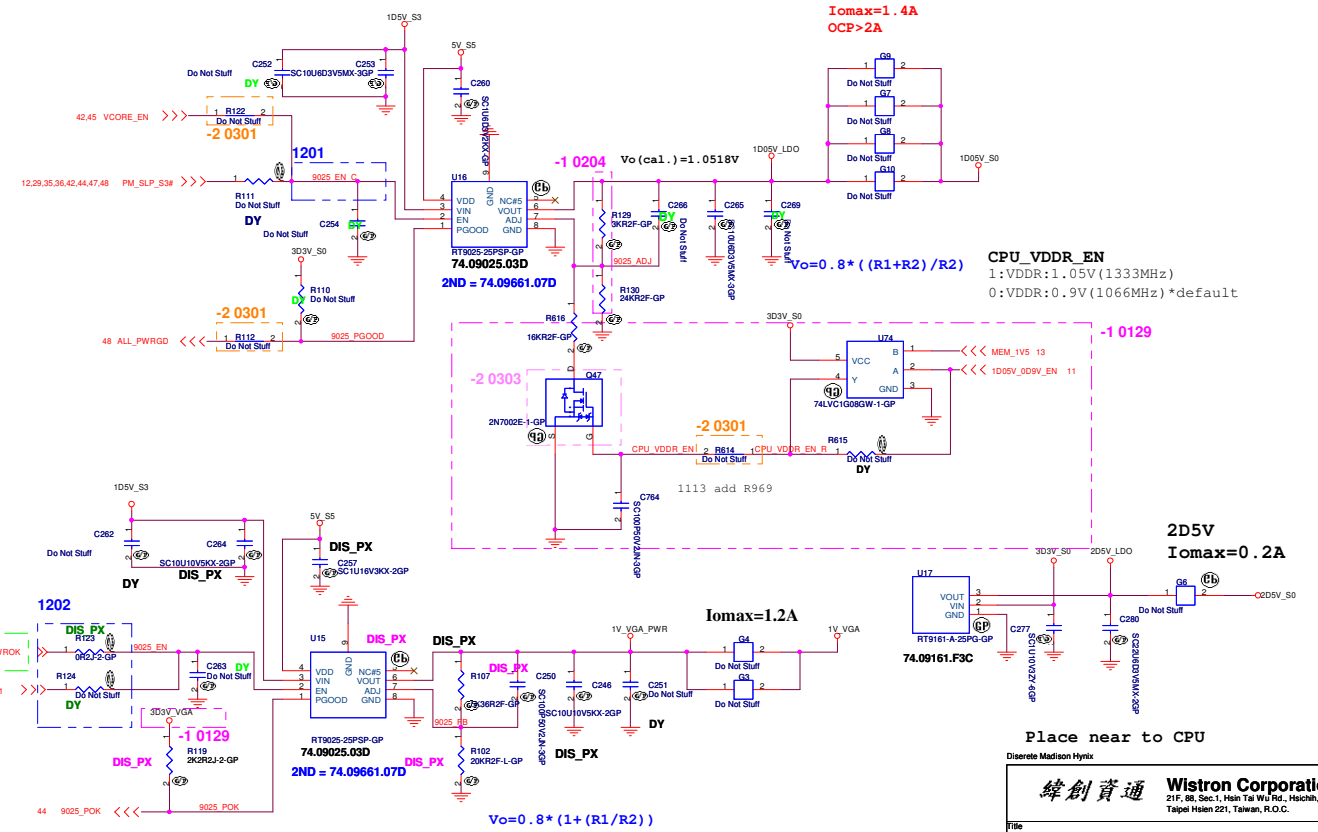
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

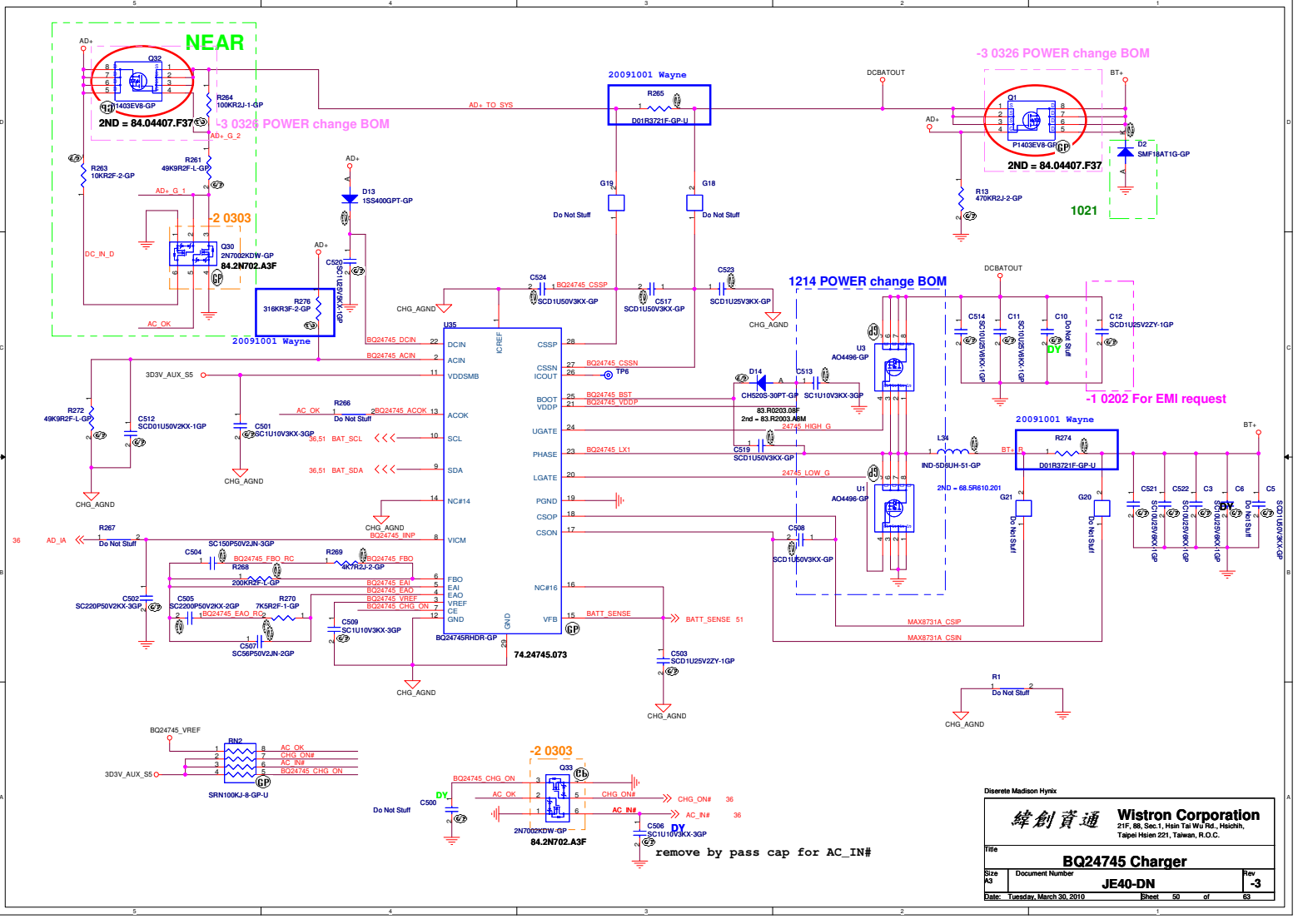
Title	RT8209E_1D5V	
Size	Document Number: JE40-DN	Rev: -3
Date: Monday, March 29, 2010	Sheet 47 of 63	

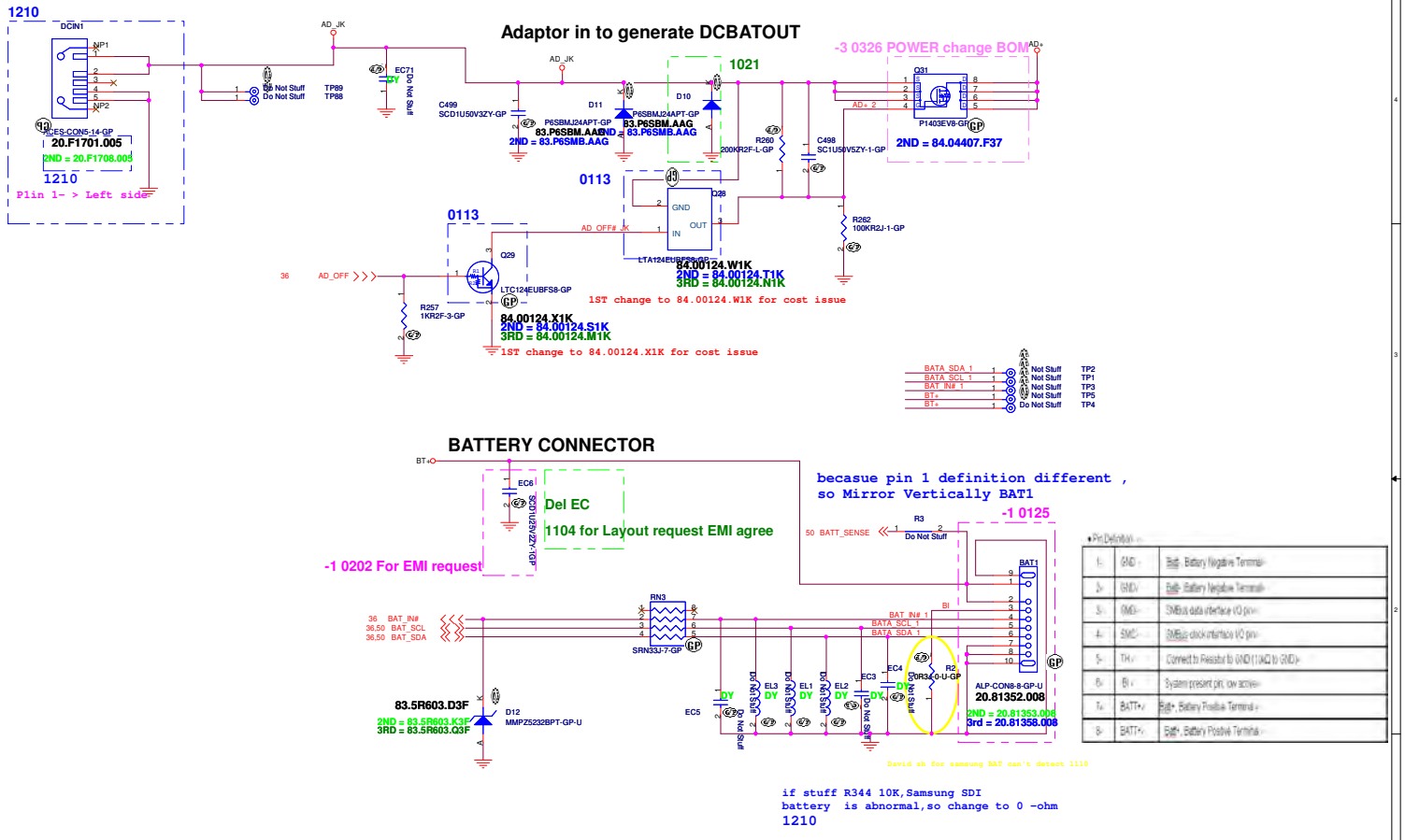
0917


RT8209E for 1D1V_S0
20091104
1214 POWER change BOM
20091001 Wayne
Iomax=11A
OCP>17A
Vout=1.1071(Cal)
Vout=0.75*(1+R1/R2)
Freq=280KHz
0921
1022
-2 0301
DY
RT9025 for 1D1V_S5
Iomax=1.4A
OCP>2A
Vo(cal.)=1.0518V
Vo=0.8*((R1+R2)/R2)
=0.8*((6.2K+16.2K)/16.2K)=1.106V
2ND = 74.09661.07D
74.09025.03D
0925
RT8015A for 1D8V_S0
Iomax=1.8A
OCP>3A
20090903
Vo=0.8*(1+(R1/R2))
1214
-2 0303
Wistron Corporation
1D1V_S0 & 1D1V_S5 & 1D8V_S0
JE40-DN
Monday, March 29, 2010

RT9025 for 1D05V_S0




NEAR
Q32
P1403EV8-GP
2ND = 84.04407.F37
-3 0326 POWER change BOM
R264
100KR2J-1-GP
R263
10KR2F-2-GP
R261
49K9R2F-L-GP
-2 0303
Q30
2N7002KDW-GP
84.2N702.A3F
R276
316KR3F-2-GP
20091001 Wayne
D13
1SS400GPT-GP
C520
SC1U25V5KX-GP
AD+ TO SYS
R265
D01R3721F-GP-U
G19
G18
Do Not Stuff
C524
SCD1U50V3KX-GP
C517
SCD1U50V3KX-GP
C523
SCD1U25V3KX-GP
DCBATOUT
BT+
Q1
P1403EV8-GP
2ND = 84.04407.F37
D2
SMF18AT1G-GP
R13
470KR2J-2-GP
1021
1214 POWER change BOM
U3
AO4496-GP
U1
AO4496-GP
D14
CH520S-30PT-GP
83.R0203.08F
2nd = 83.R2003.A6M
C513
SC1U10V3KX-3GP
C519
SCD1U50V3KX-GP
L34
IND-5D8UH-51-GP
2ND = 68.5R610.201
C514
SC10U25V6KX-1GP
C11
SC10U25V6KX-1GP
C10
DY
C12
SCD1U25V2ZY-1GP
-1 0202 For EMI request
R274
D01R3721F-GP-U
G21
G20
C521
SC10U25V6KX-1GP
C522
SC10U25V6KX-1GP
C3
SC10U25V6KX-1GP
C6
C5
SCD1U50V3KX-GP
C508
SCD1U50V3KX-GP
MAX8731A_CSIP
MAX8731A_CSIN
U35
IC/REF
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745RHDR-GP
74.24745.073
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSP
BQ24745_CSSN
TP6
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BQ24745_ACOK
BAT_SCL
BAT_SDA
BQ24745_IINP
BQ24745_FBO
BQ24745_EA
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BATT_SENSE
AC_OK
R266
Do Not Stuff
R272
49K9R2F-L-GP
C512
SCD1U50V2KX-1GP
C501
SC1U10V3KX-3GP
CHG_AGND
3D3V_AUX_S5
R267
Do Not Stuff
SC150P50V2JN-3GP
C504
R268
200KR2F-L-GP
R269
49K9R2J-2-GP
C502
SC220P50V2KX-3GP
C505
SC2200P50V2KX-2GP
R270
7K5R2F-1-GP
C507
SC56P50V2JN-2GP
C509
SC1U10V3KX-3GP
C503
SCD1U25V2ZY-1GP
R1
Do Not Stuff
AD_IA
RN2
SRN100KJ-8-GP-U
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q33
2N7002KDW-GP
84.2N702.A3F
C500
C506
SC1U10V3KX-3GP
CHG_ON#
remove by pass cap for AC_IN#
Diserete Madison Hynix
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number
JE40-DN
Rev -3
Date: Tuesday, March 30, 2010
Sheet 50 of 63



Pin Definition		
1-	GND	Batt. Battery Negative Terminal
2-	GND	Batt. Battery Negative Terminal
3-	GND	SMBus data interface I/O pin
4-	SMC	SMBus clock interface I/O pin
5-	TH	Connect to Resistor to GND (1KΩ to GND)
6-	BI	System present pin, low active
7-	BATT+	Batt+, Battery Positive Terminal
8-	BATT+	Batt+, Battery Positive Terminal

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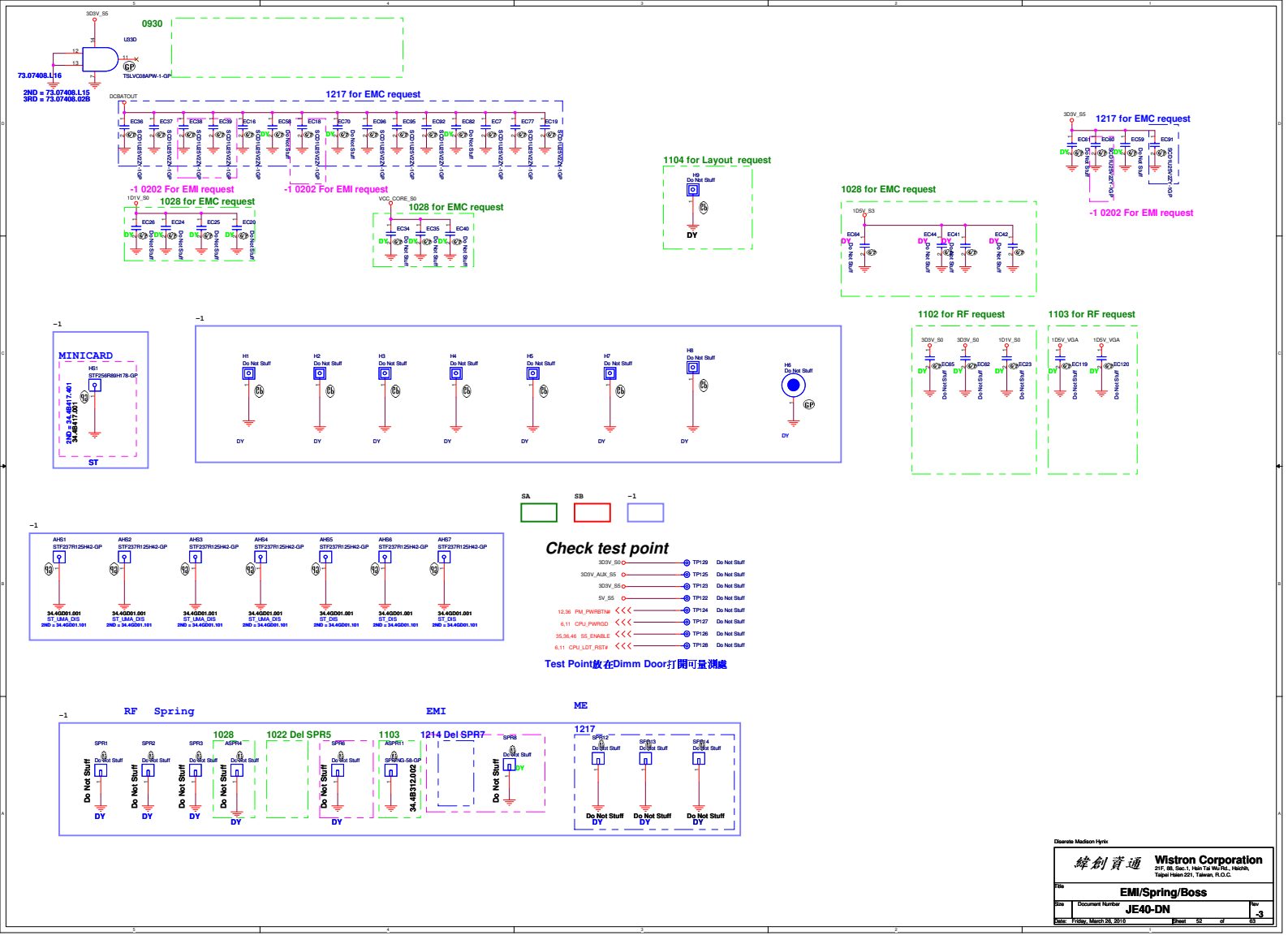
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

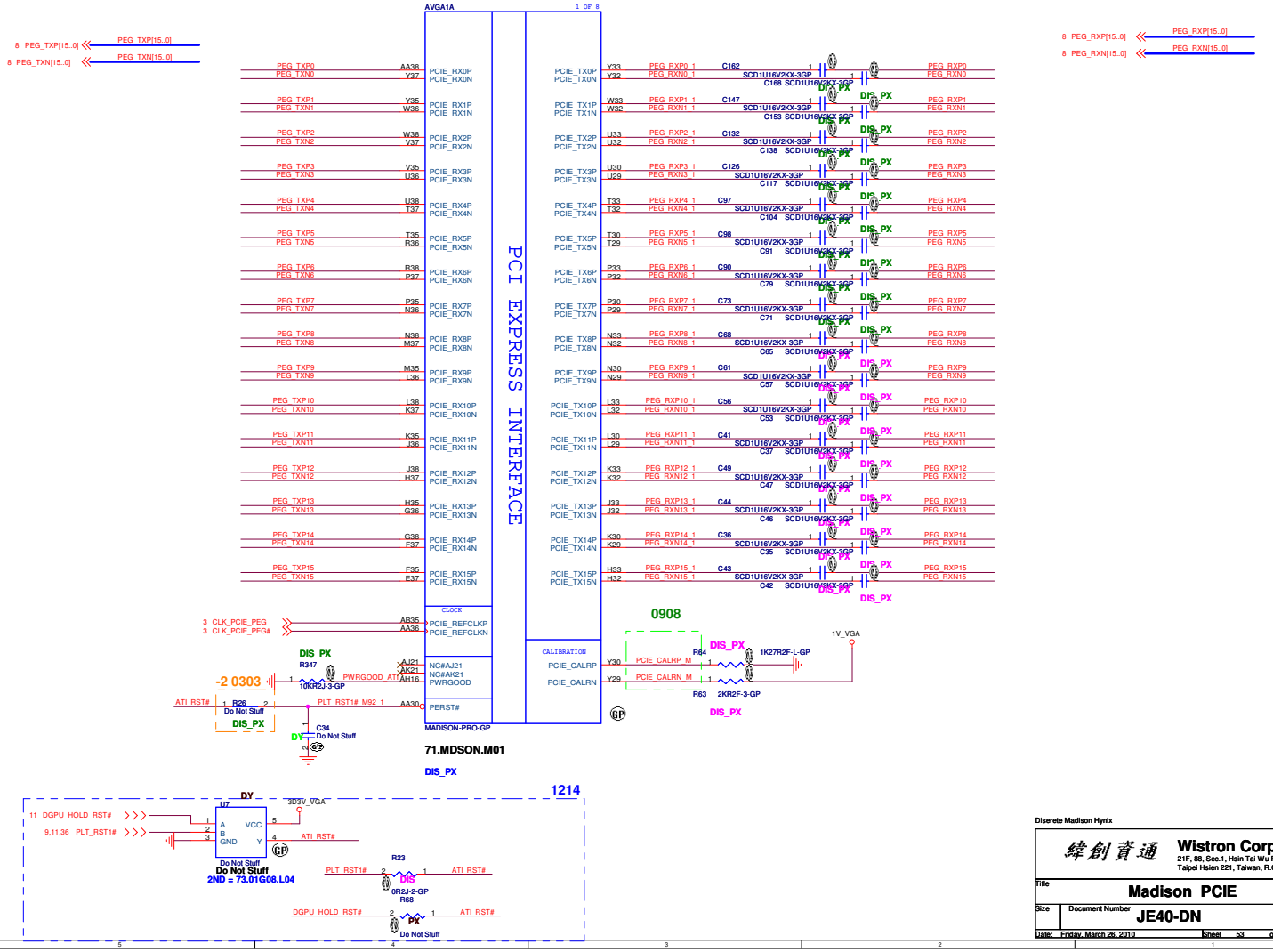
Size	Document Number	Rev
	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 51 of 63



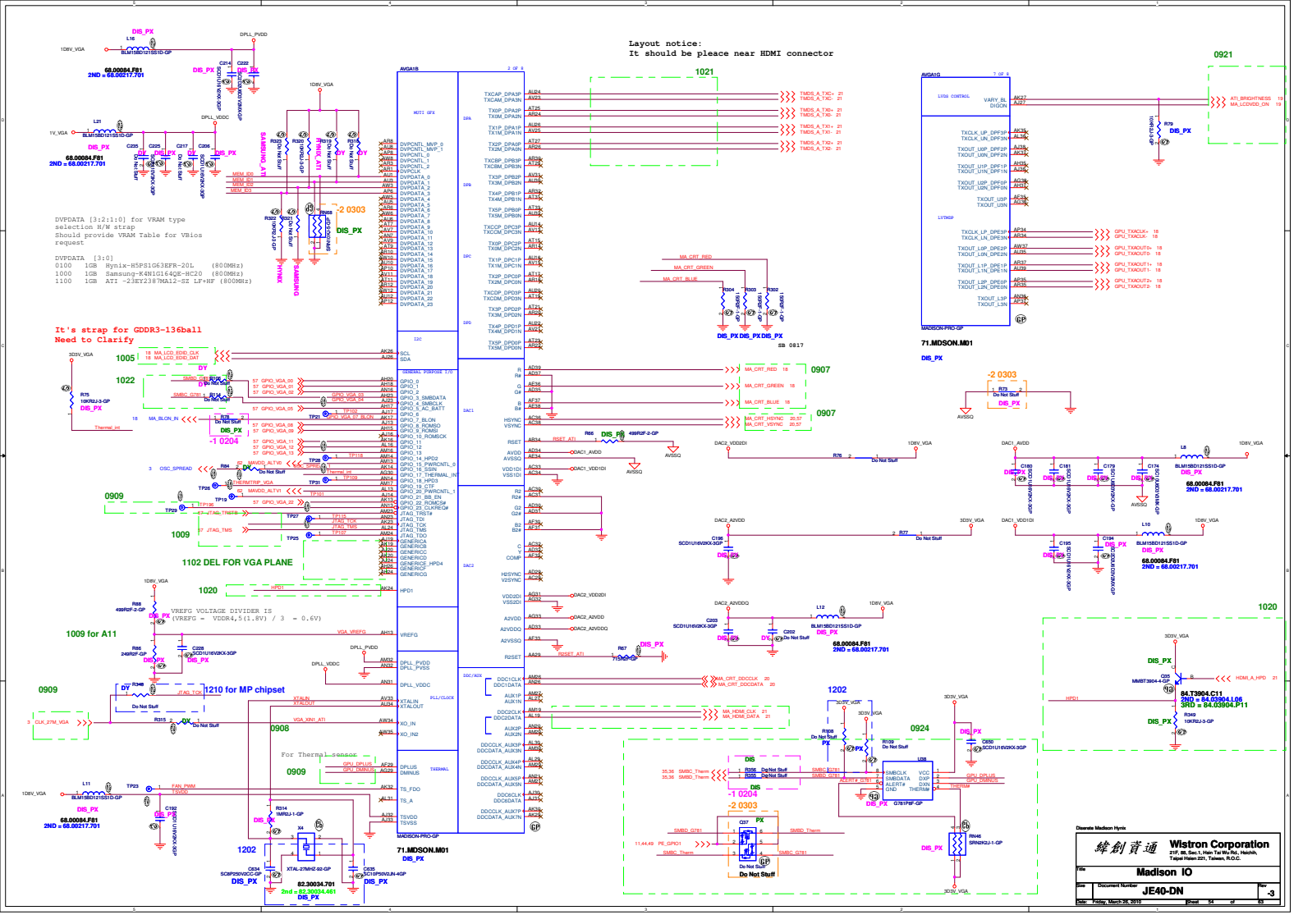
Disarate Madison Hynix

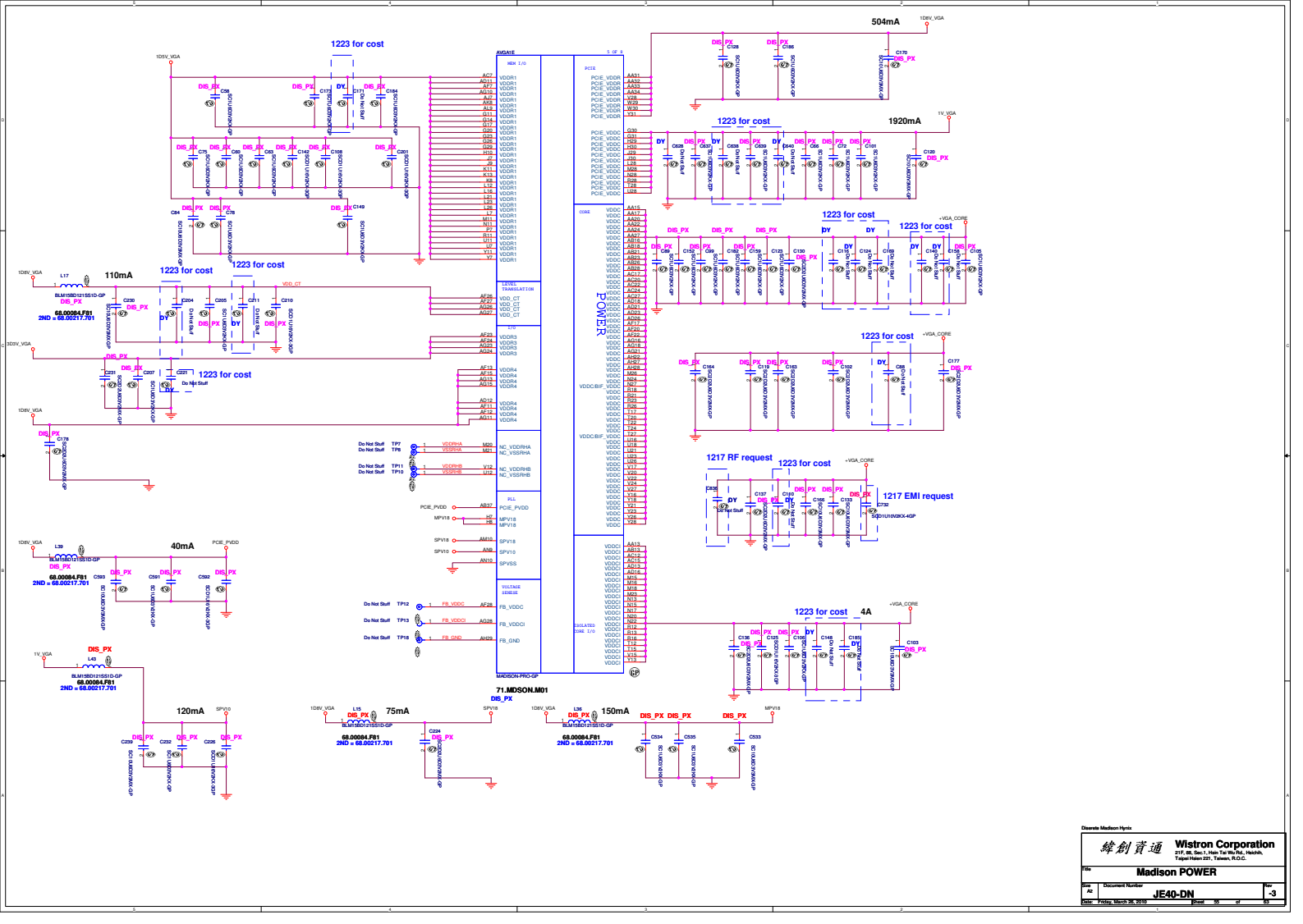
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	EMI/Spring/Boss	
Size	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 52 of 63	



Diserete Madison Hynix

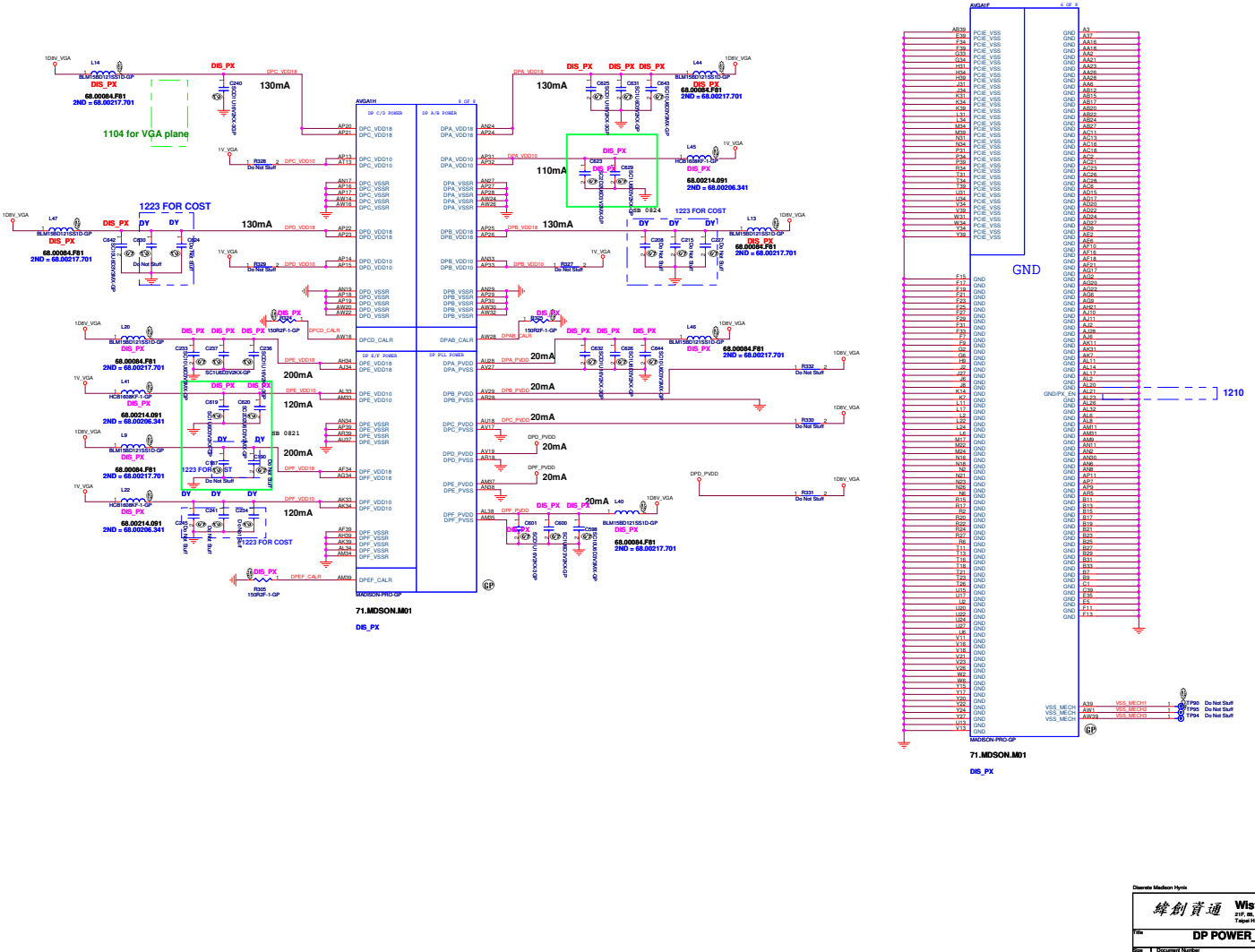
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Madison PCIE**	
Size	Document Number **JE40-DN**	Rev **-3**
Date: Friday, March 26, 2010	Sheet 53 of 63	


Layout notice:
It should be pleace near HDMI connector
DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request
DVPDATA [3:0]
0100 1GB Hynix-H5PS1G63EFR-20L (800MHz)
1000 1GB Samsung-K4N1G164QE-HC20 (800MHz)
1100 1GB ATI -23EY2387MA12-SZ LF+HF (800MHz)
It's strap for GDDR3-136ball
Need to Clarify
1102 DEL FOR VGA PLANE
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
1009 for A11
1210 for MP chipset
For Thermal sensor
71.MDSON.M01
82.30034.701
84.T3904.C11
Wistron Corporation
Madison IO
JE40-DN



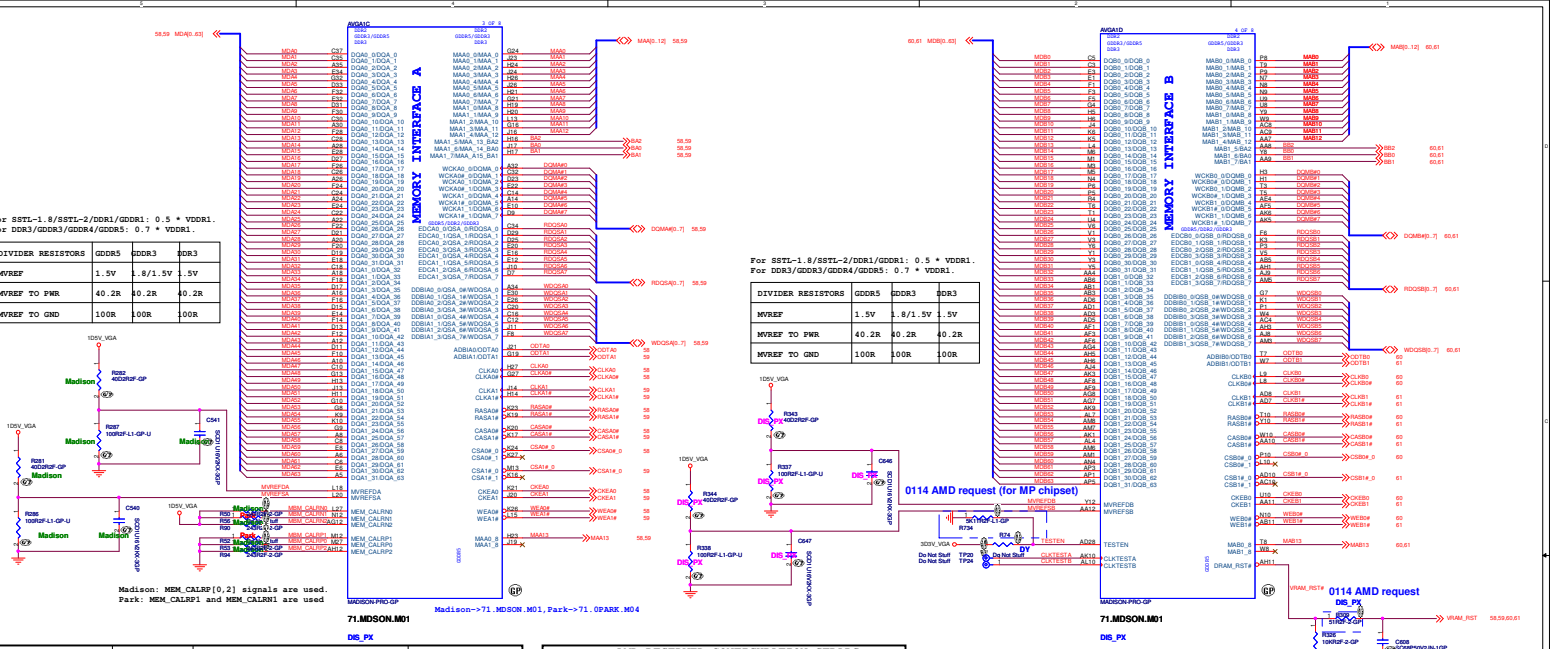
Discrete Madison Hynix

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title:	Madison POWER	
Size: A0	Document Number: JE40-DN	Rev: -3
Date: Friday, March 26, 2010	Sheet 05 of 53	



Diasnete Madison Hynix

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DP POWER_GND			
Size: A2	Document Number: JE40-DN		Rev: -3
Date: Friday, March 26, 2010	Sheet 56 of 63		



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

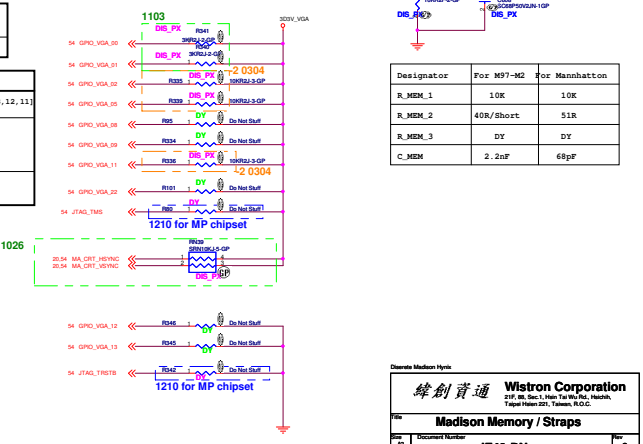
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PMRS_ENB (Internal PD)	GPIO0	PCE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	51R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Discrete Madison Hynix

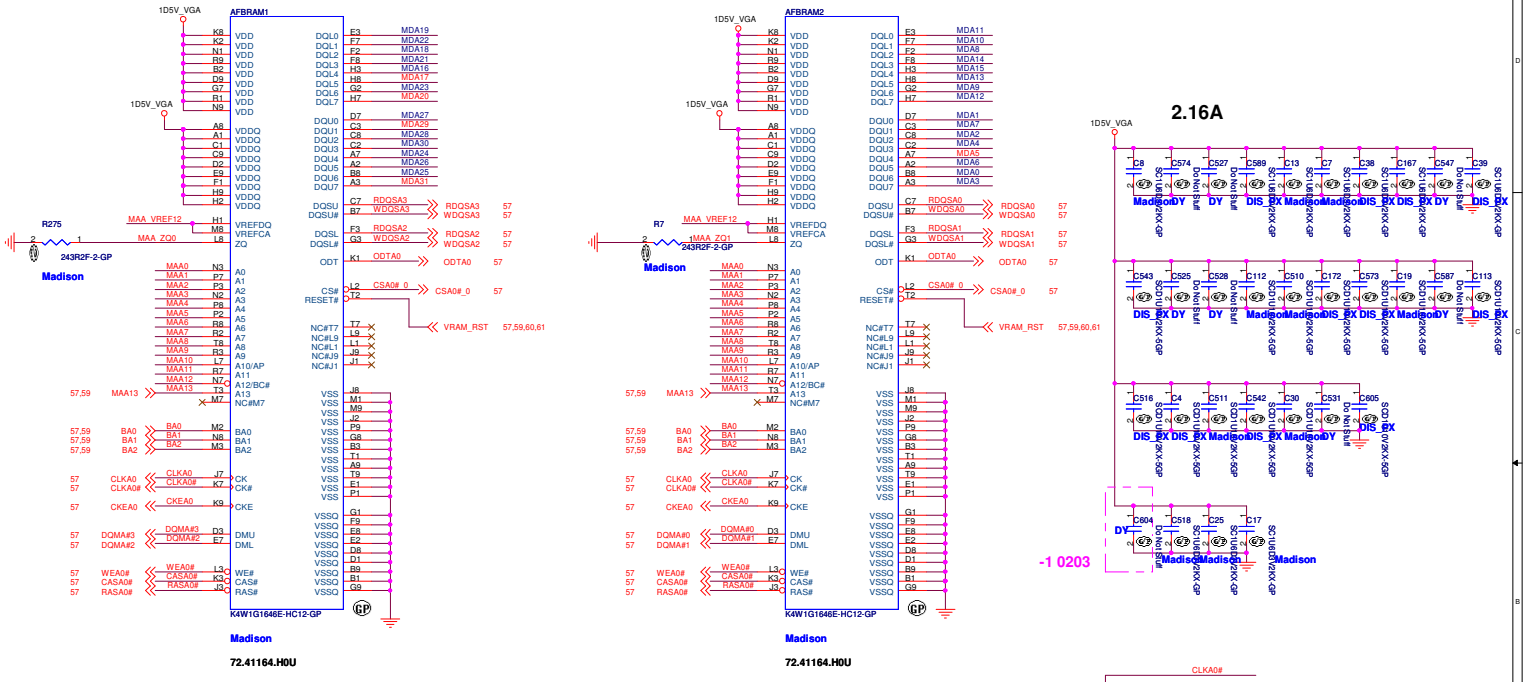
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

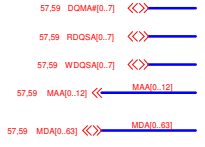
Size	Document Number	Rev
A2	JE40-DN	-3

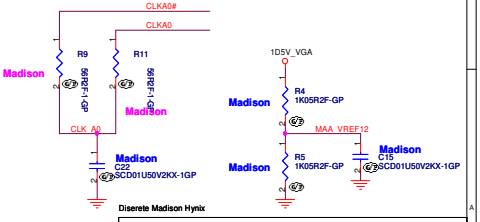
Date: Friday, March 26, 2010 Sheet 57 of 63

DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





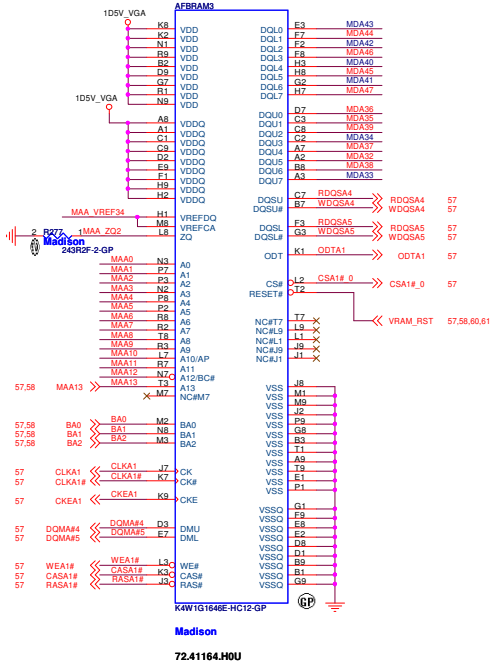
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

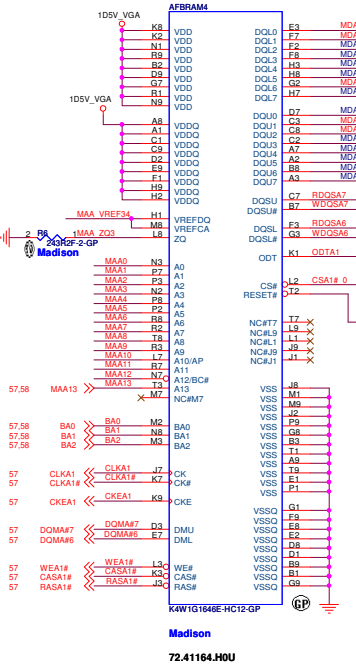
Title: VRAM(1/4)

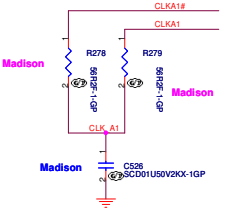
Size	Document Number	Rev
A3	JE40-DN	-3

Date: Friday, March 26, 2010 Sheet 58 of 63

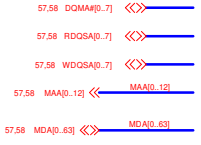
DDR3

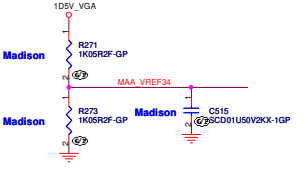






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

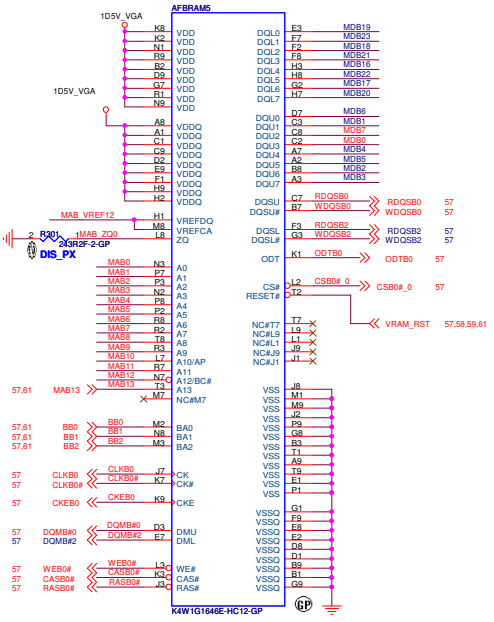


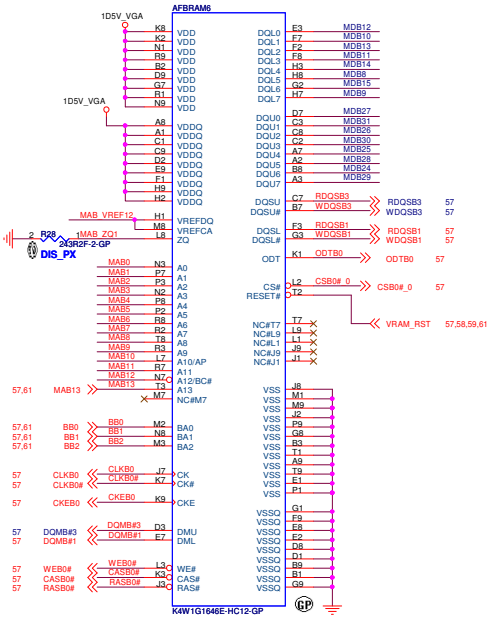


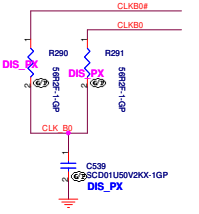
Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(2/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 59 of 63	

DDR3







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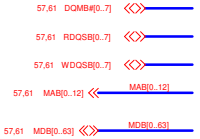
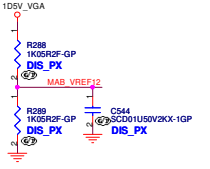
HYNIX: 72.51G63.C0U

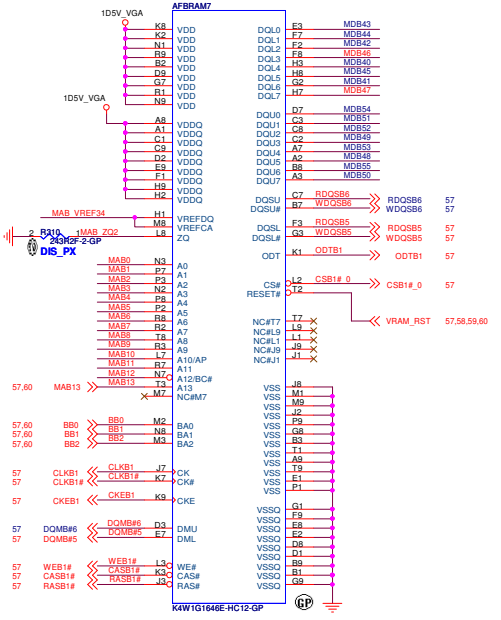


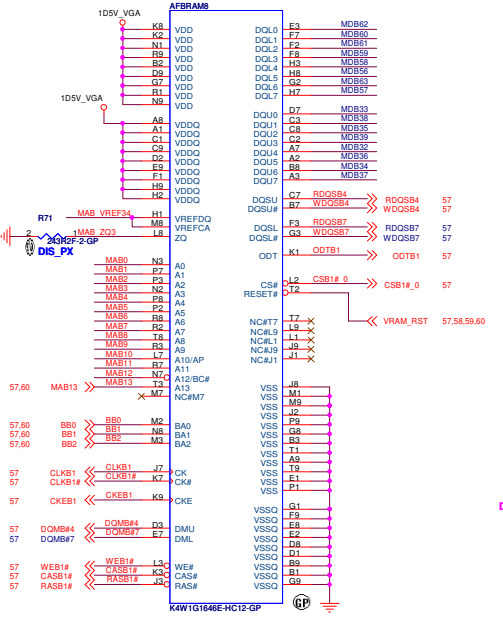


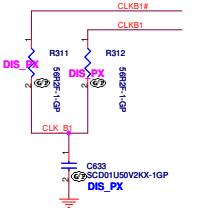
Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(3/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 60 of 63	

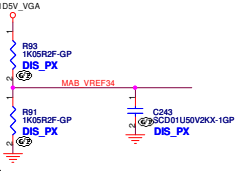
DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



57,60 DQMB#[0..7]

57,60 RDQSB[0..7]

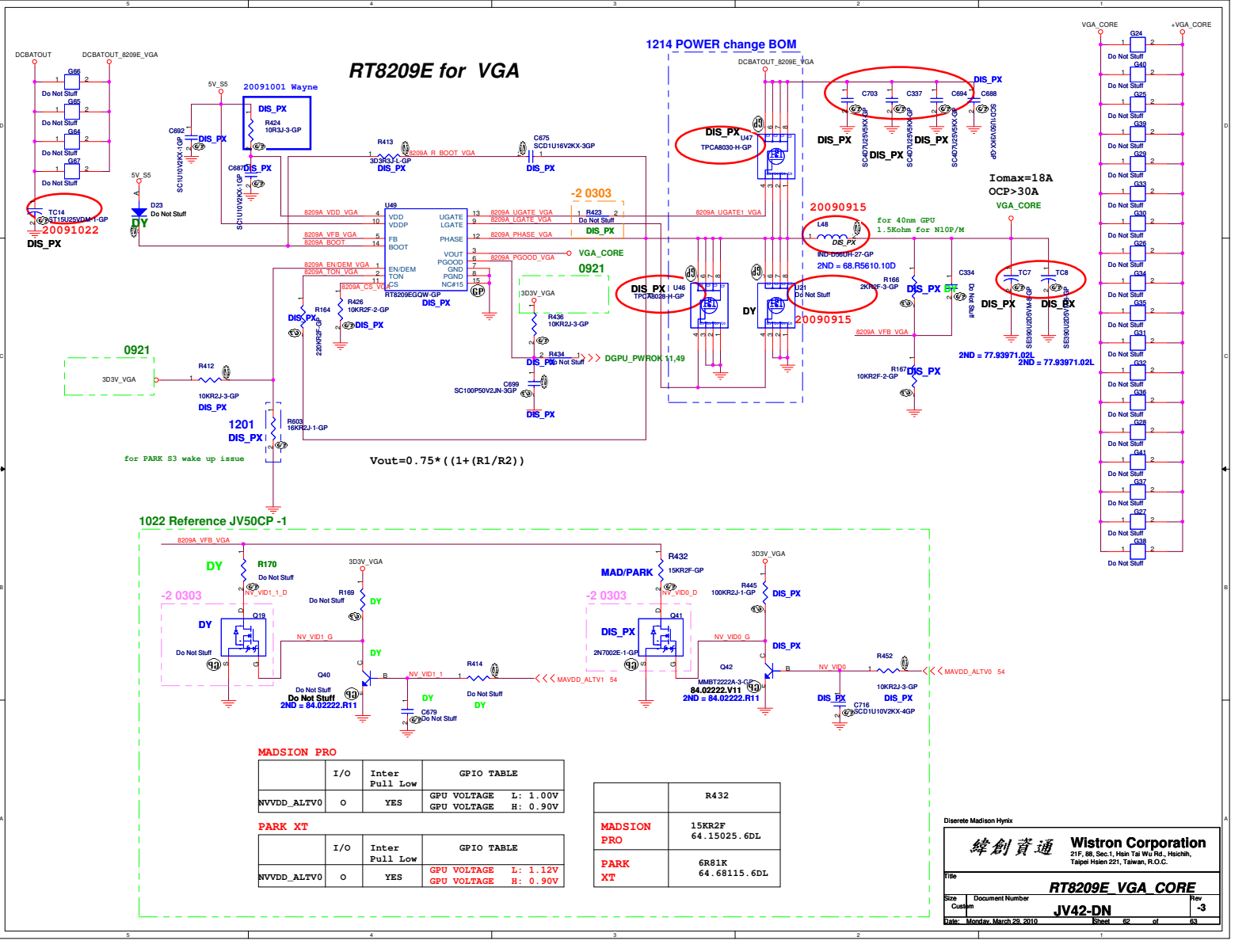
57,60 WDQSB[0..7]

57,60 MAB[0..12] — MAB[0..12]

57,60 MDB[0..63] — MDB[0..63]

Diserete Madison Hynix

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(4/4)***	
Size A3	Document Number **JE40-DN**	Rev -3
Date: Friday, March 26, 2010	Sheet 61 of 63	



	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

	R432
MADSION PRO	15KR2F 64.15025.6DL
PARK XT	6R81K 64.68115.6DL

Diserete Madison Hynix

NB

RS780-->RS880M

71.RS780.M02-->71.RS880.M02

SB

SB820M-1-GP

71.SB820.00U-->71.SB820.M03

SATA_CALRP

A11: 80歐姆 1% resistor to GND

A12: TBD歐姆 1% resistor to GND

SATA_CALRN

A11:A11: 931歐姆1% resistor to VDDAN_11_SATA

A12: TBD歐姆 1% resistor to VDDAN_11_SATA.

VGA

Madison--> PN:71.MDSON.M01

Park--> PN:71.0PARK.M04

VRAM

Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004

ATI--> VRAM FBRAM1~8 PN: VR.1GB0T.002

CRT

UMA-->L1-->2R 0603

C62-->47U/6.3V

DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)

C62-->DY

PX--> 133 歐姆 (R58 63.10334.1DL R402H16 133R2F-GP)

R605(MAD/PARK/PX)

Madison-->R605 64.15005.6DL R402H16150R2F-L-GP

Park -->R605 64.15005.6DL R402H16150R2F-L-GP

PX -->R605 64.15005.6DL R402H16150R2F-L-GP

HDMI

UMA -->R612 R613 R618 R619 R620 R621 R624 R625 64.71505.6DL R402H16715R2F-2-GP

R432(MAD/PARK)

Madison-->15KR2F 64.15025.6DL

Park-->R432 64.68115.6DL R402H16 6.81KR2F

BOM

1st -> All SKU

R250

Madison-->R250 64.32425.6DL R402H16 32K4R2F

Park -->R250 64.32425.6DL R402H16 32K4R2F

PX -->R250 64.32425.6DL R402H16 32K4R2F

Diserete Madison Hynix

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Title	NOTE	
Size A3	Document Number JV42-DN	Rev -3
Date: Monday, March 29, 2010	Sheet 63 of 63	