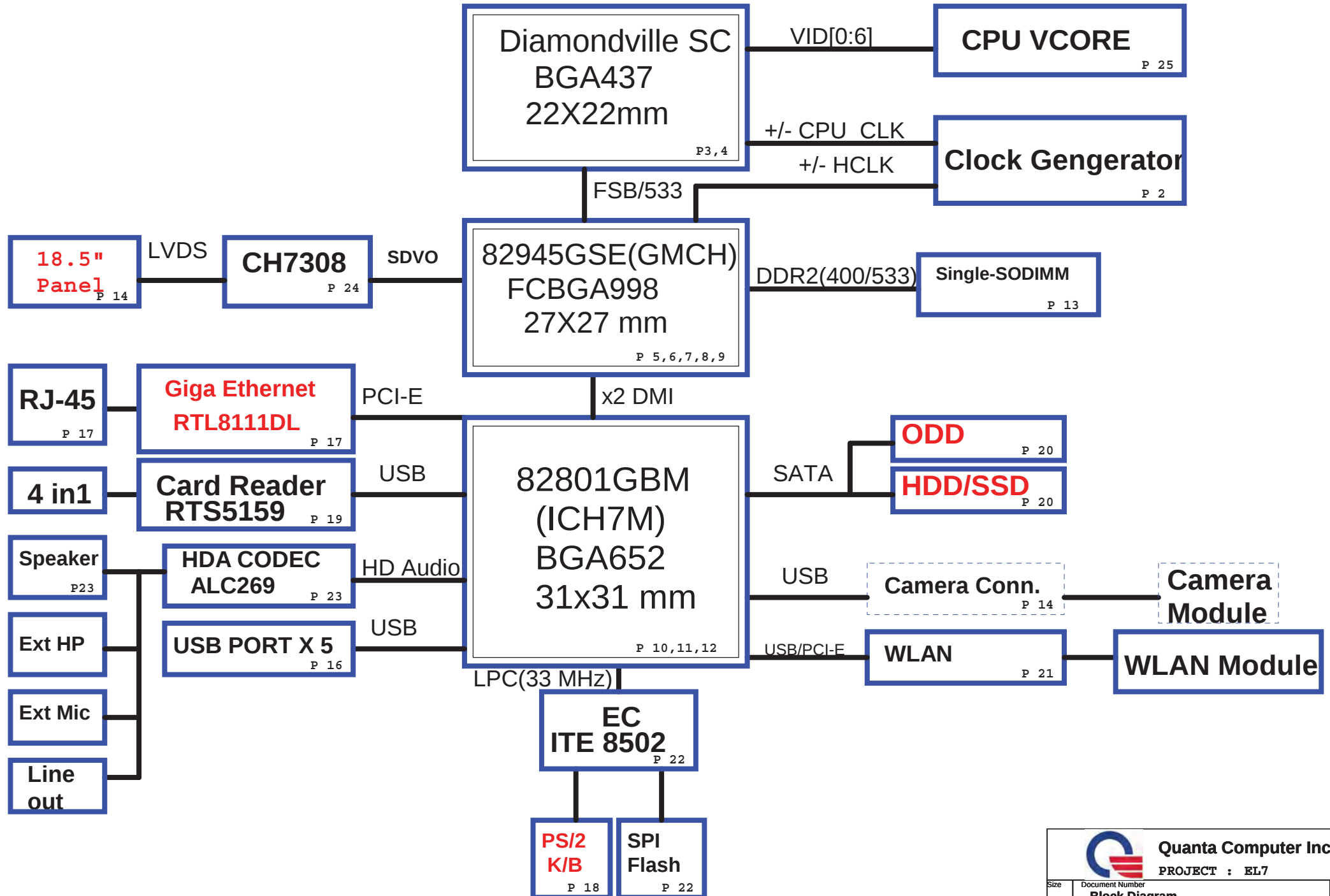
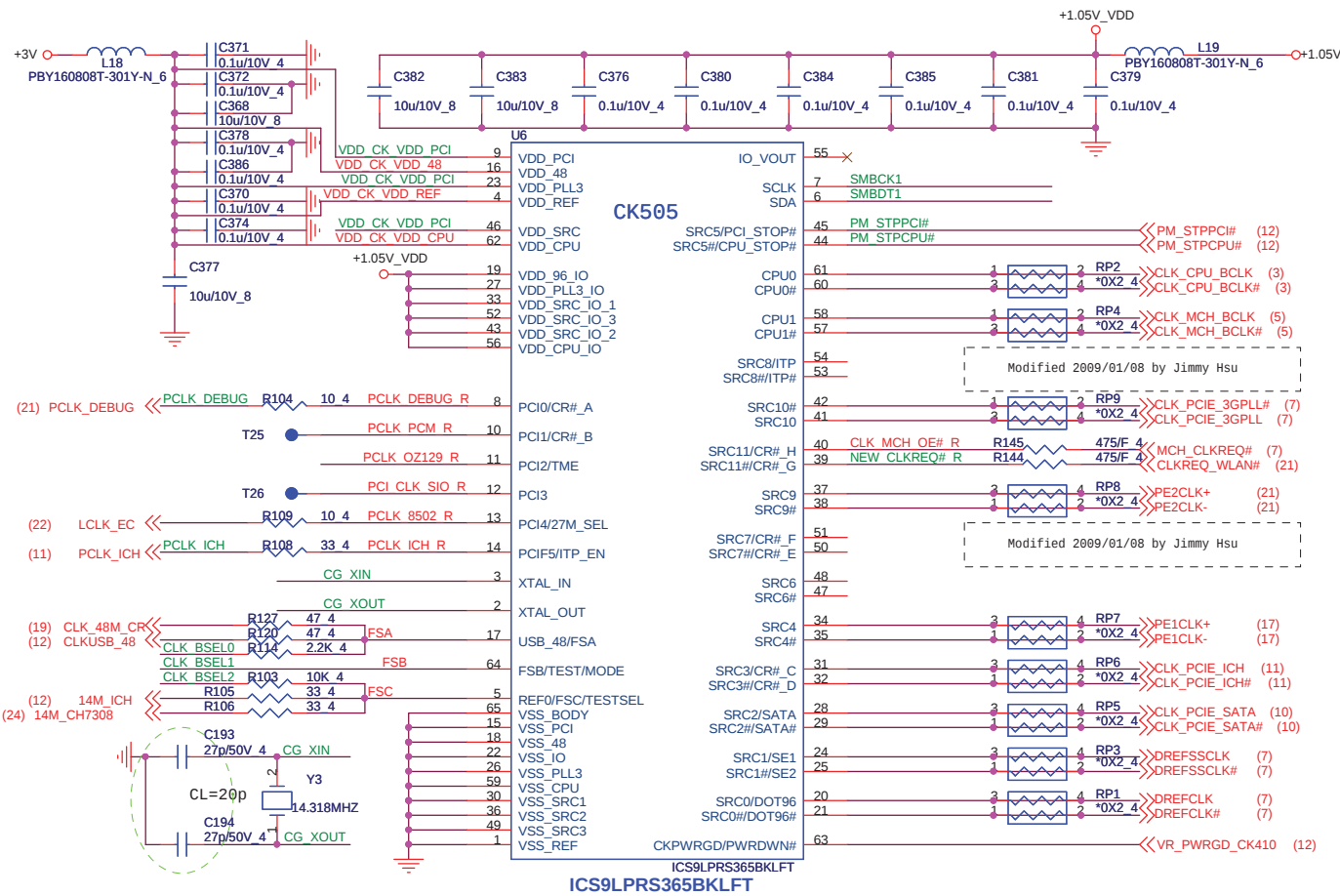


Clapton (EL7) AIO Block Diagram

01



Clock Generator



To SB

To CPU

To NB

To 3G

To NB

To WLAN

CLK To 3G

To LAN

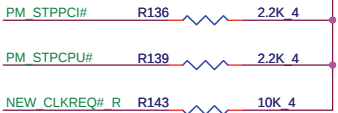
To SB

To SB

To NB

To NB

To NB



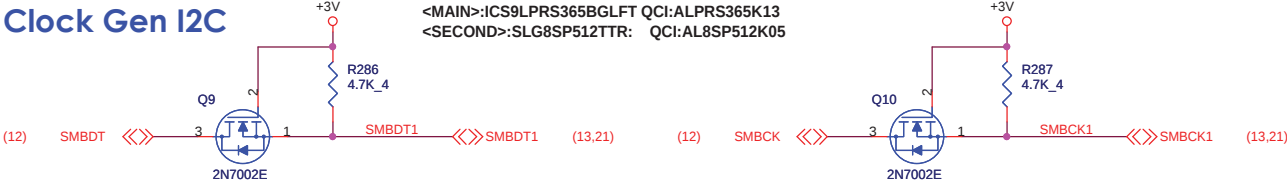
SEL2 SEL1 SEL0 Frequency select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	Reserved		

Default

	ICS9LPRS365 (ALPRS365K13)	RTM8751-606 (AL060875K06)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 24/25 IS 27MHz	PIN 20/21 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	internal PD	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

Clock Gen I2C



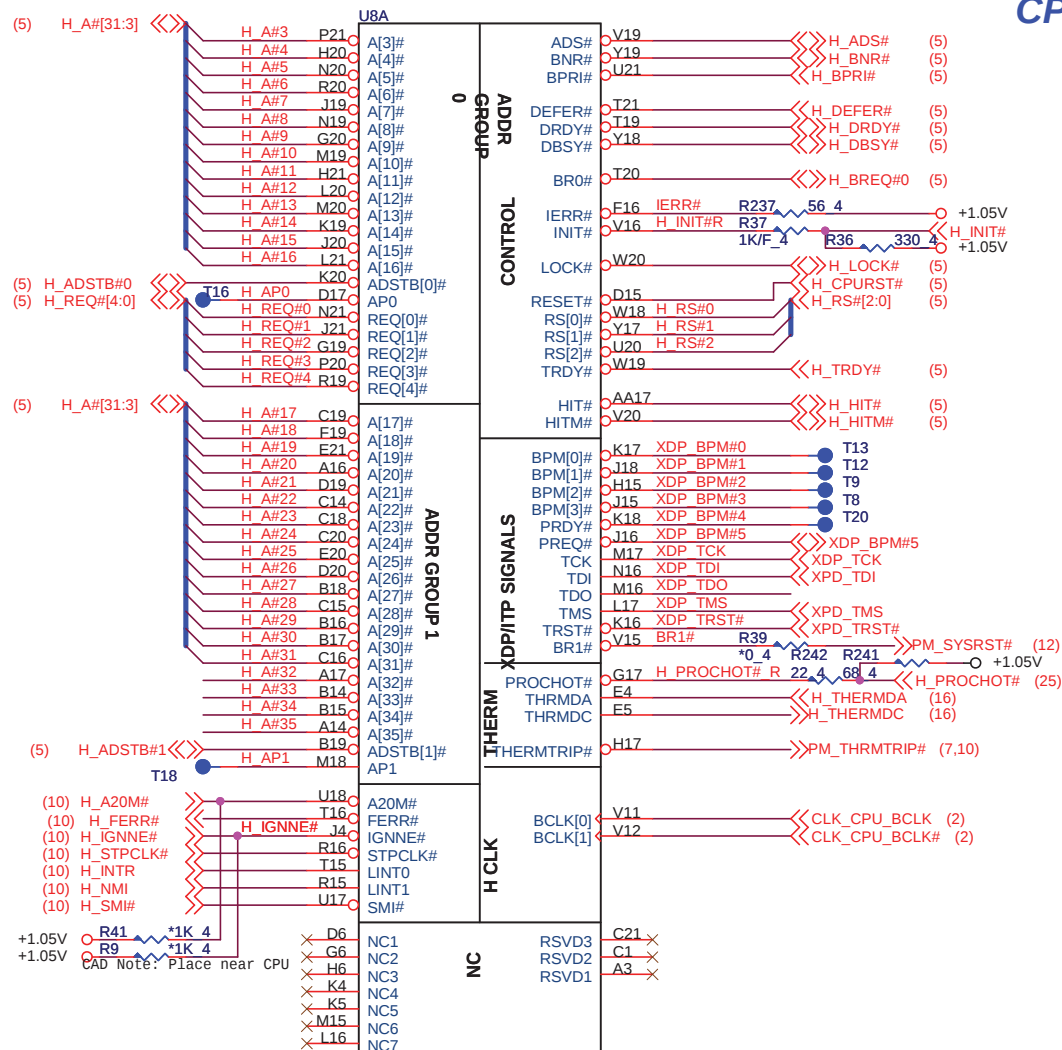


Quanta Computer Inc.
PROJECT : EL7

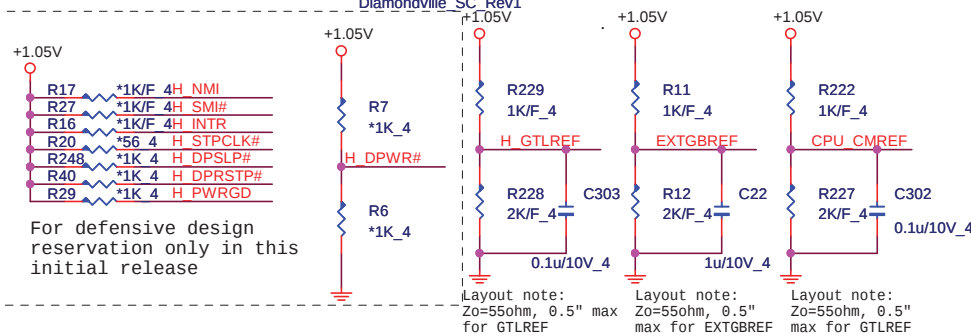
Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date:	Friday, April 24, 2009	Sheet 2 of 34

CPU

03



CPU P/N: AJSLB73VT01



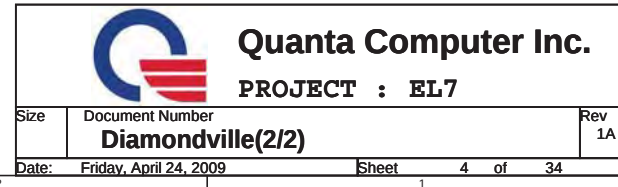
Quanta Computer Inc.

PROJECT : EL7

Size Document Number
Diamondville(1/2)

Date: Friday, April 24, 2009 Sheet 3 of 34

Rev 1A



(3) H_D#[63:0] <<>

U9A

H_D#0 C4
H_D#1 F6
H_D#2 H9
H_D#3 H6
H_D#4 E7
H_D#5 E3
H_D#6 C2
H_D#7 C3
H_D#8 K9
H_D#9 F5
H_D#10 J7
H_D#11 K7
H_D#12 H8
H_D#13 E5
H_D#14 K8
H_D#15 J8
H_D#16 J2
H_D#17 J3
H_D#18 N1
H_D#19 M5
H_D#20 K5
H_D#21 J5
H_D#22 H3
H_D#23 J4
H_D#24 N3
H_D#25 M4
H_D#26 M3
H_D#27 N8
H_D#28 N6
H_D#29 K3
H_D#30 N9
H_D#31 M1
H_D#32 V8
H_D#33 V9
H_D#34 R6
H_D#35 T8
H_D#36 R2
H_D#37 N5
H_D#38 N2
H_D#39 R5
H_D#40 U7
H_D#41 R8
H_D#42 T4
H_D#43 T7
H_D#44 R3
H_D#45 T5
H_D#46 V6
H_D#47 V3
H_D#48 W2
H_D#49 W1
H_D#50 V2
H_D#51 W4
H_D#52 W7
H_D#53 W5
H_D#54 V5
H_D#55 AB4
H_D#56 AB8
H_D#57 W8
H_D#58 AA9
H_D#59 AA8
H_D#60 AB1
H_D#61 AB7
H_D#62 AA2
H_D#63 AB5

H_XRCOMP A10
H_XSCOMP A6
H_XSWING C15
H_YRCOMP J1
H_YSCOMP K1
H_YSWING H1

H_XRCOMP
H_XSCOMP
H_XSWING
H_YRCOMP
H_YSCOMP
H_YSWING

HOST

HA3#
HA4#
HA5#
HA6#
HA7#
HA8#
HA9#
HA10#
HA11#
HA12#
HA13#
HA14#
HA15#
HA16#
HA17#
HA18#
HA19#
HA20#
HA21#
HA22#
HA23#
HA24#
HA25#
HA26#
HA27#
HA28#
HA29#
HA30#
HA31#

F8 H_A#3
D12 H_A#4
C13 H_A#5
A8 H_A#6
E13 H_A#7
E12 H_A#8
J12 H_A#9
B13 H_A#10
A13 H_A#11
G13 H_A#12
A12 H_A#13
D14 H_A#14
E14 H_A#15
J13 H_A#16
E17 H_A#17
H15 H_A#18
G15 H_A#19
G14 H_A#20
A15 H_A#21
B18 H_A#22
B15 H_A#23
E14 H_A#24
H13 H_A#25
C14 H_A#26
A17 H_A#27
E15 H_A#28
H17 H_A#29
D17 H_A#30
G17 H_A#31

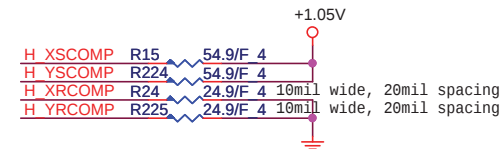
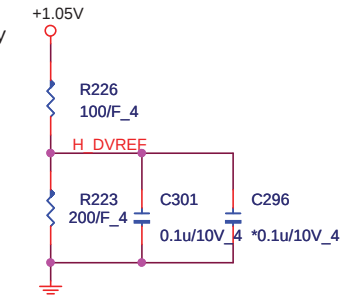
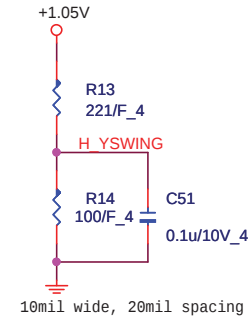
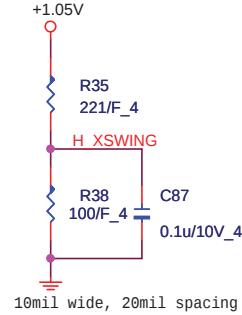
<<> H_A#[31:3] (3)

HADS# F10 <<> H_ADS# (3)
HADSTB0# C12 <<> H_ADSTB#0 (3)
HADSTB1# H16 <<> H_ADSTB#1 (3)
H_AVREF E2 H_DVREF
HBNR# B9 <<> H_BNR# (3)
HBPR1# C7 <<> H_BPRI# (3)
HBREQ0# G8 <<> H_BREQ#0 (3)
HCPURST# B10 <<> H_CPURST# (3)
HDVREF E1 H_DVREF

H_CPURST# has T topology

HCLKN AA6 <<> CLK_MCH_BCLK# (2)
HCLKP AA5 <<> CLK_MCH_BCLK (2)
HDBSY# C10 <<> H_DBSY# (3)
HDEFER# C6 <<> H_DEFER# (3)
HDINV0# H5 H_DINV#0 <<> H_DINV#0 (3)
HDINV1# J6 H_DINV#1 <<> H_DINV#1 (3)
HDINV2# T9 H_DINV#2 <<> H_DINV#2 (3)
HDINV3# U6 H_DINV#3 <<> H_DINV#3 (3)
HDPWR# G7 <<> H_DPWR# (3)
HDRDY# E6 <<> H_DRDY# (3)
HDSTBN0# E3 H_DSTBN#0 <<> H_DSTBN#0 (3)
HDSTBN1# M8 H_DSTBN#1 <<> H_DSTBN#1 (3)
HDSTBN2# T1 H_DSTBN#2 <<> H_DSTBN#2 (3)
HDSTBN3# AA3 H_DSTBN#3 <<> H_DSTBN#3 (3)
HDSTBP0# E4 H_DSTBP#0 <<> H_DSTBP#0 (3)
HDSTBP1# M7 H_DSTBP#1 <<> H_DSTBP#1 (3)
HDSTBP2# T2 H_DSTBP#2 <<> H_DSTBP#2 (3)
HDSTBP3# AB3 H_DSTBP#3 <<> H_DSTBP#3 (3)

HHIT# C8 <<> H_HIT# (3)
HHITM# B4 <<> H_HITM# (3)
HLOCK# C5 <<> H_LOCK# (3)
HREQ0# G9 H_REQ#0 <<> H_REQ#[4:0] (3)
HREQ1# E9 H_REQ#1
HREQ2# G12 H_REQ#2
HREQ3# B8 H_REQ#3
HREQ4# E12 H_REQ#4
HRS0# A5 H_RS#0 <<> H_RS#[2:0] (3)
HRS1# B6 H_RS#1
HRS2# G10 H_RS#2
HCPUSLP# E8 <<> H_CPUSLP# (3,10)
HTRDY# E10 <<> H_TRDY# (3)



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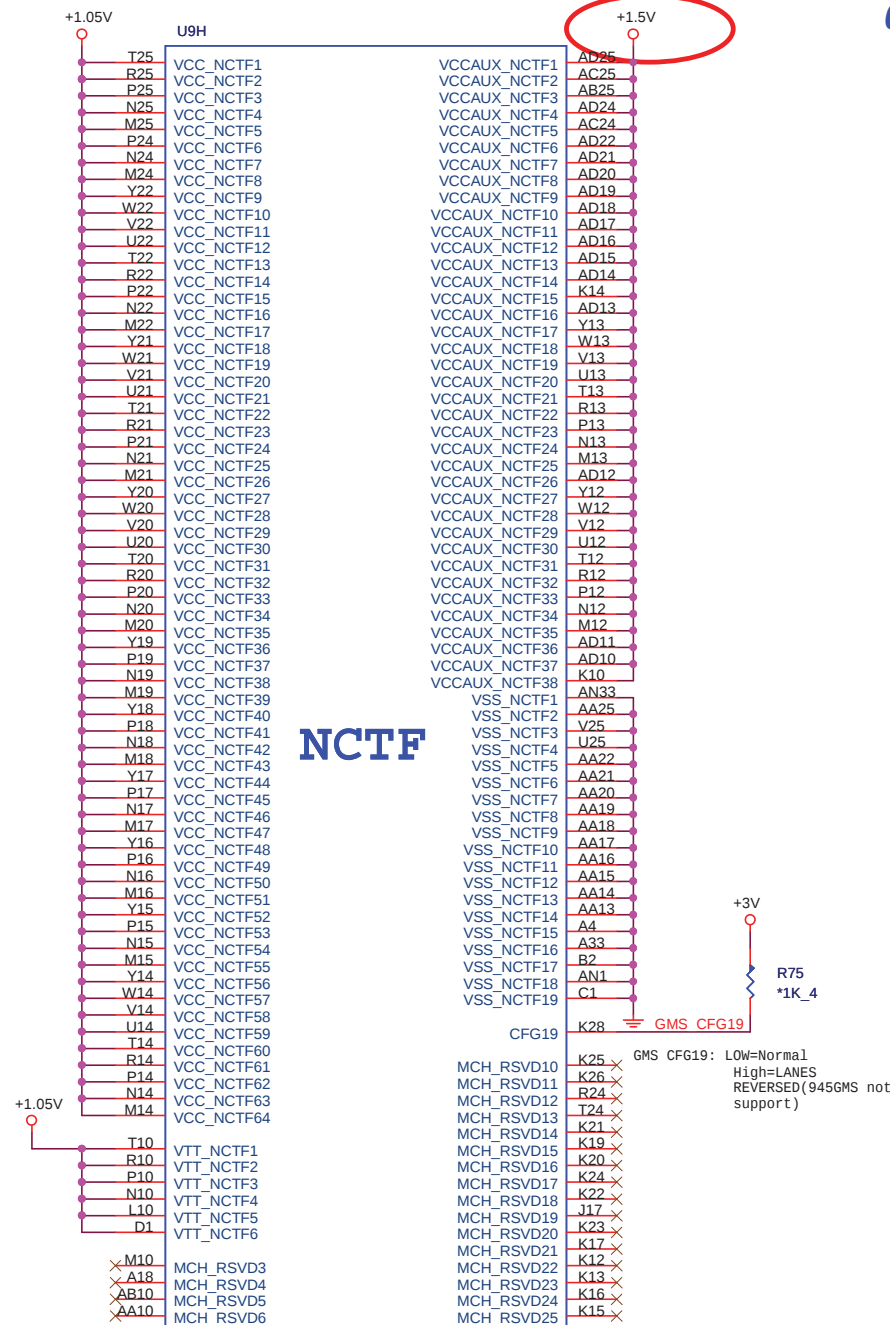
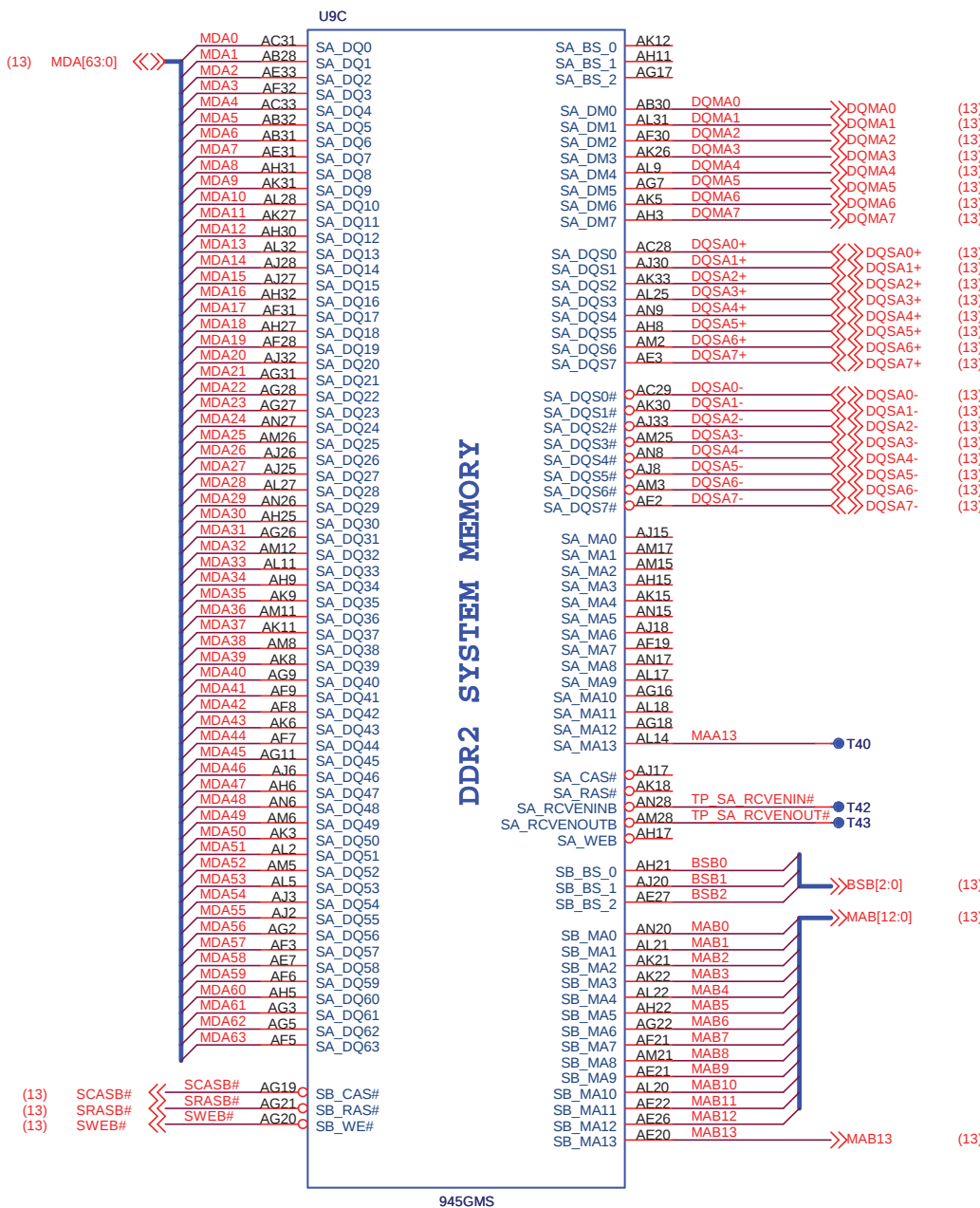
PROJECT : EL7

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	945GMS HOST	1A
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945GMS DDR

06

DDR2 SYSTEM MEMORY



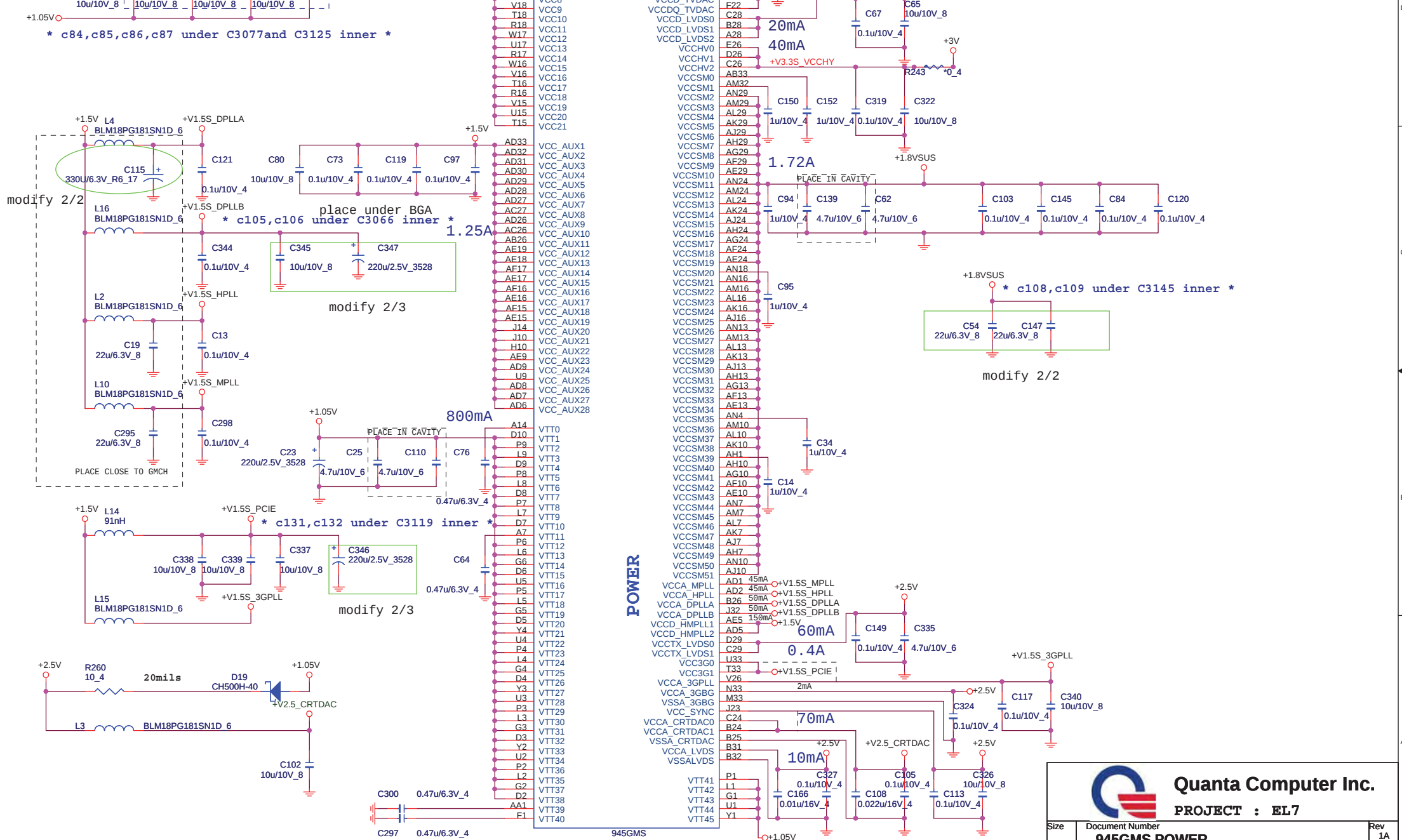
NB P/N: AJSLB2R0T00

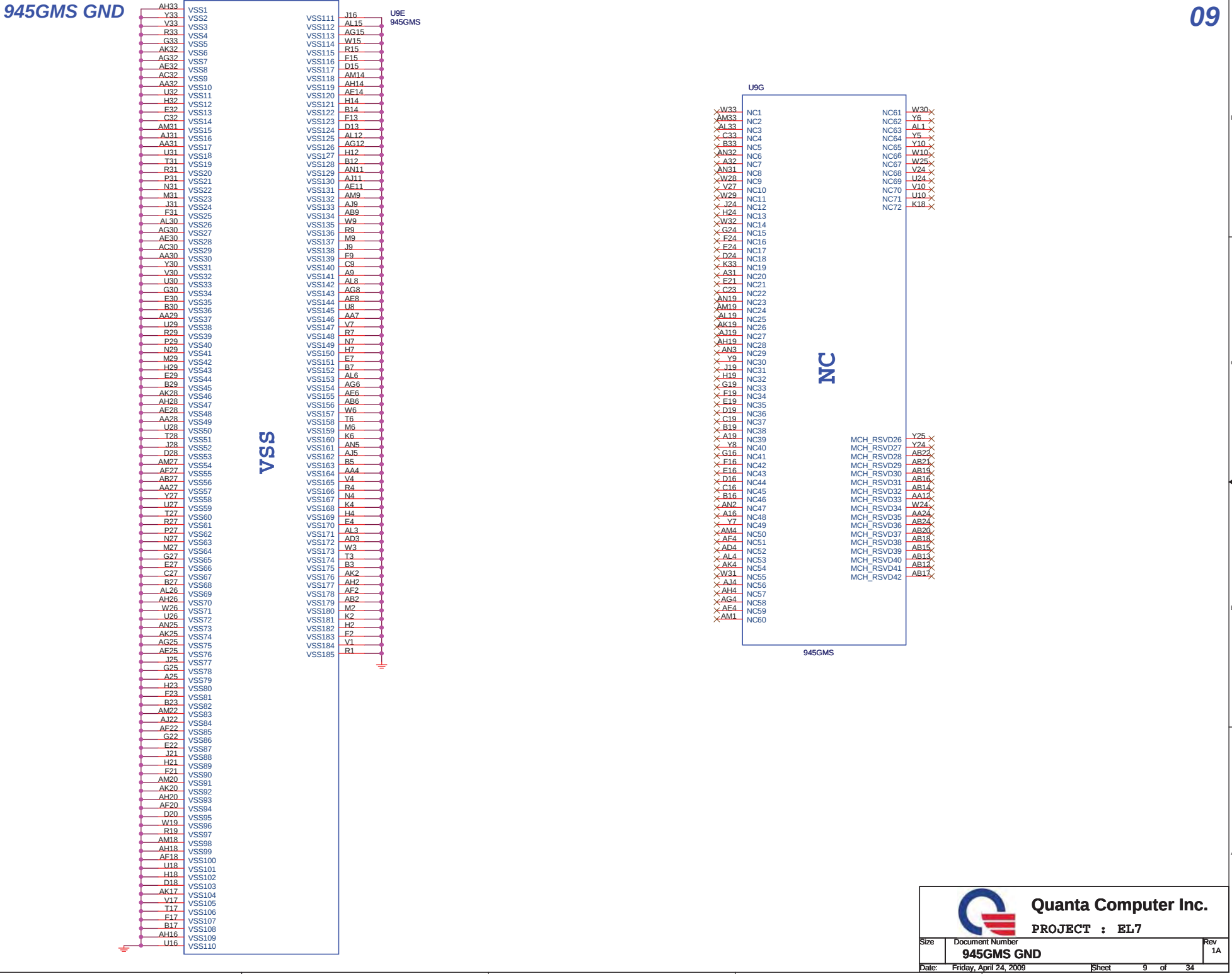


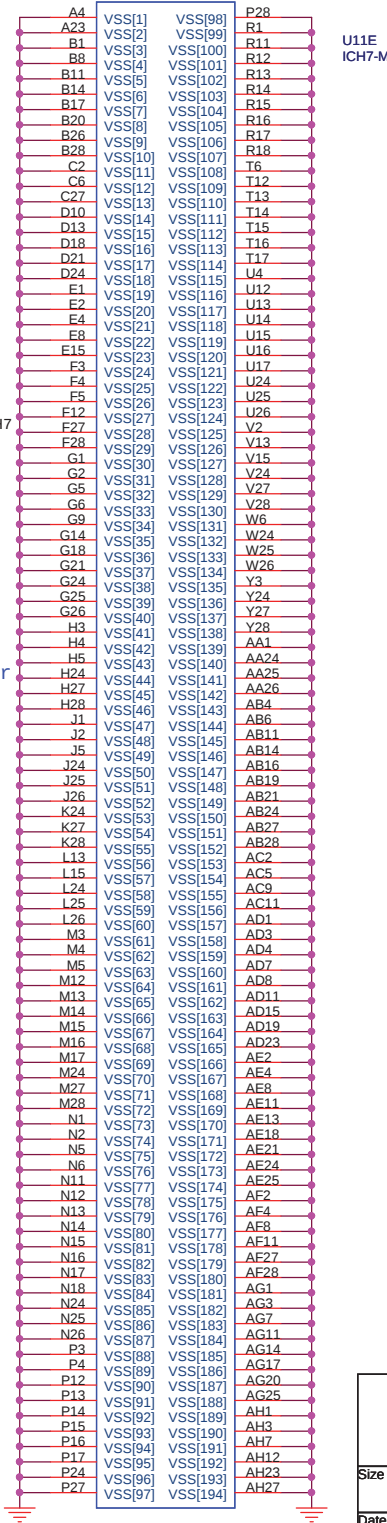
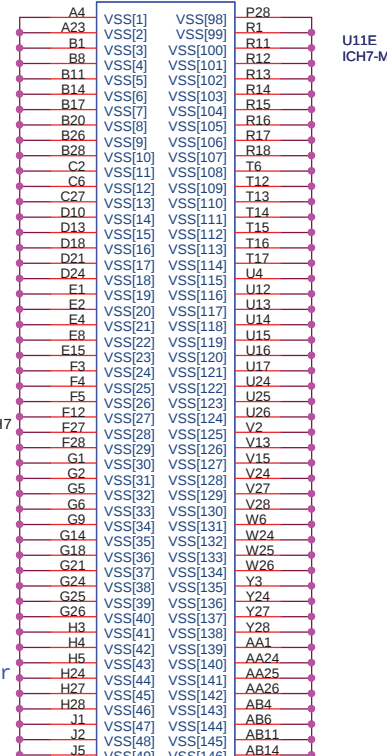
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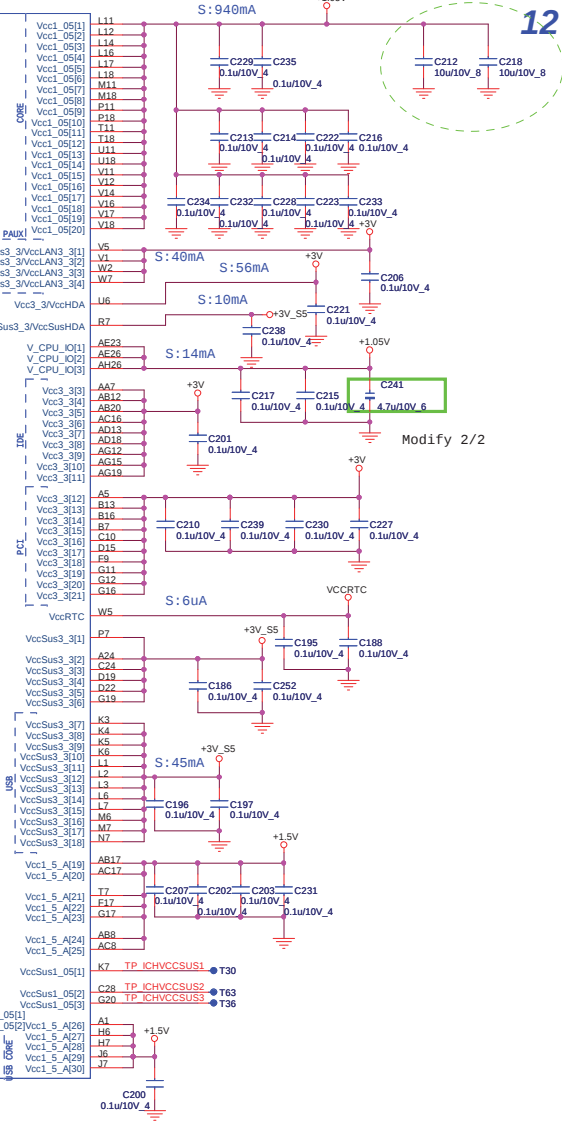
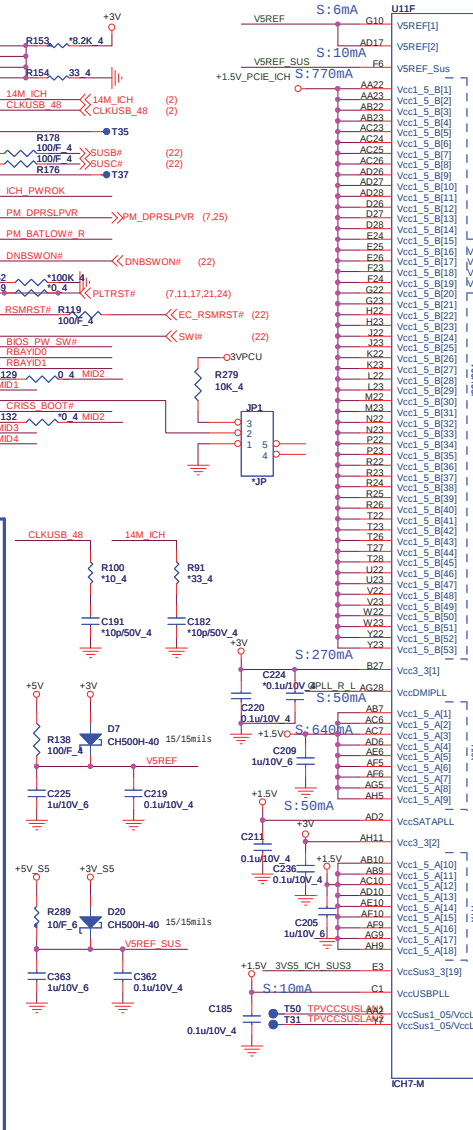
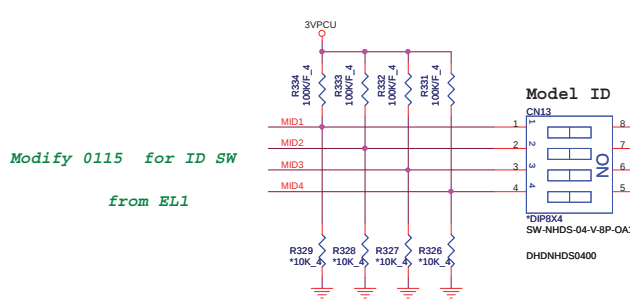
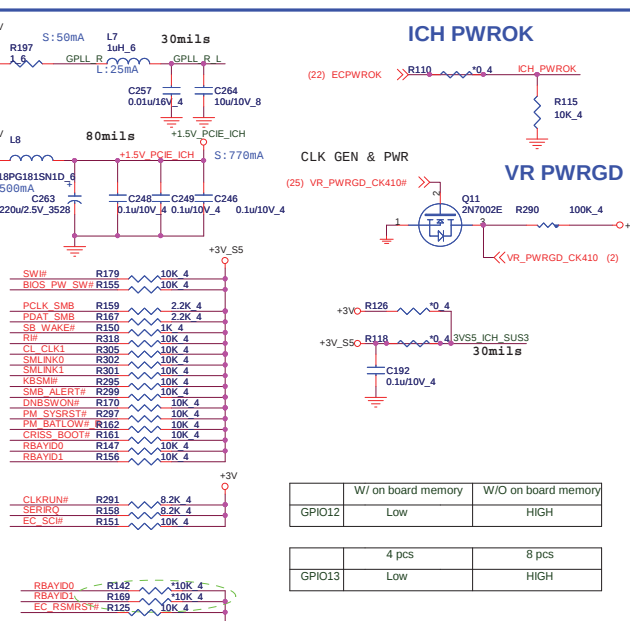
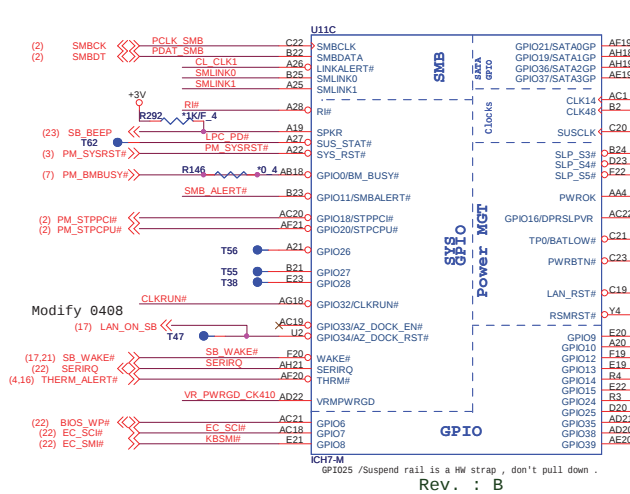
PROJECT : EL7

Size	Document Number	Rev
	945GMS DDR	1A
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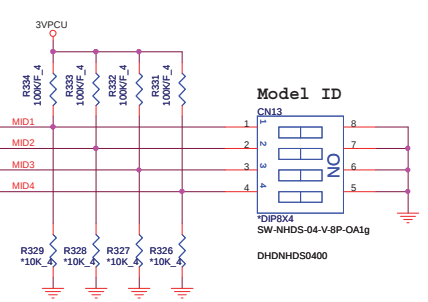






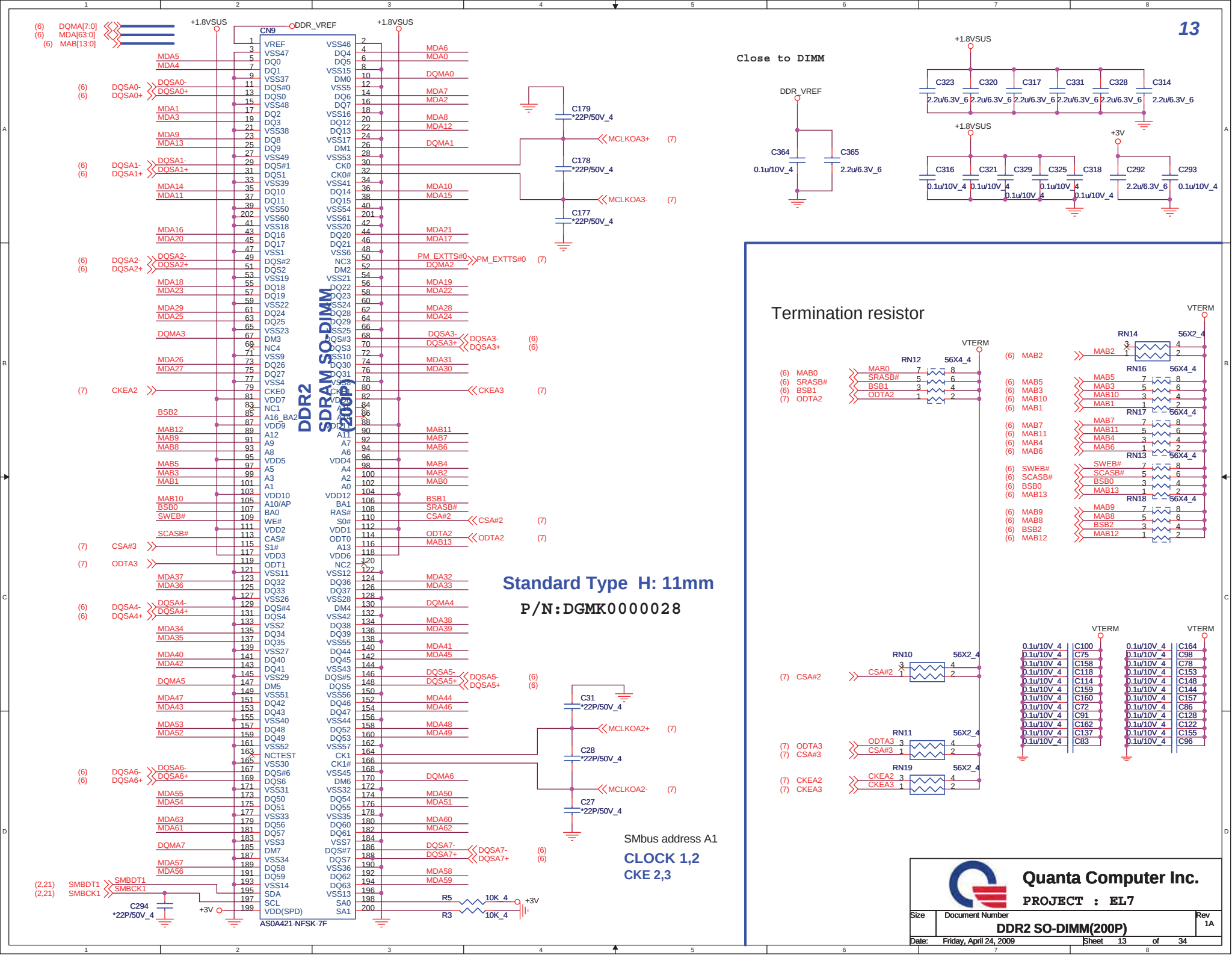


Modify 0115 for ID SW
from EL1

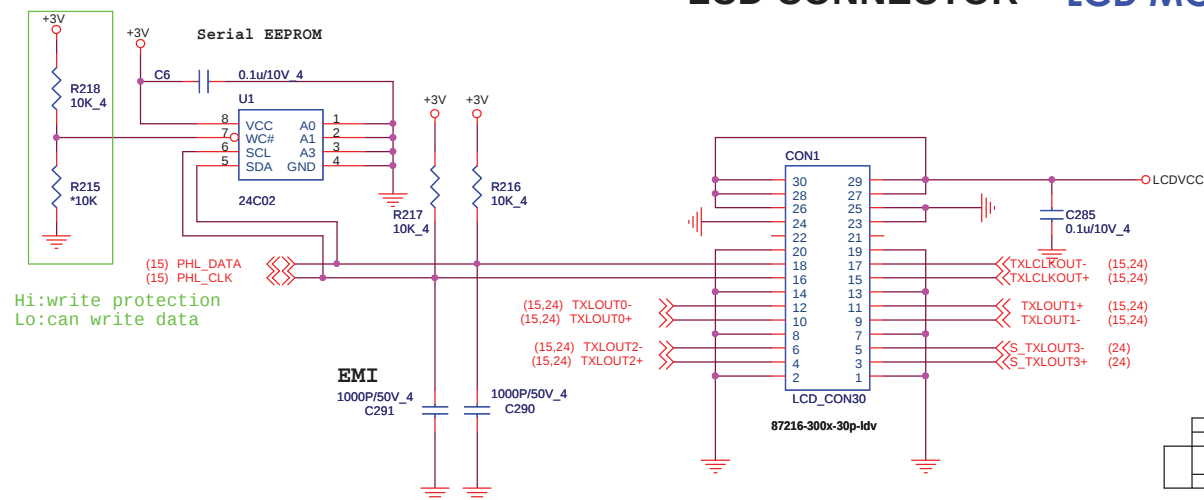


GP15	GP14	GP38	GP39
MID1	MID2	MID3	MID4
1	1	1	1
1	0	1	0
0	1	0	1
0	0	0	0

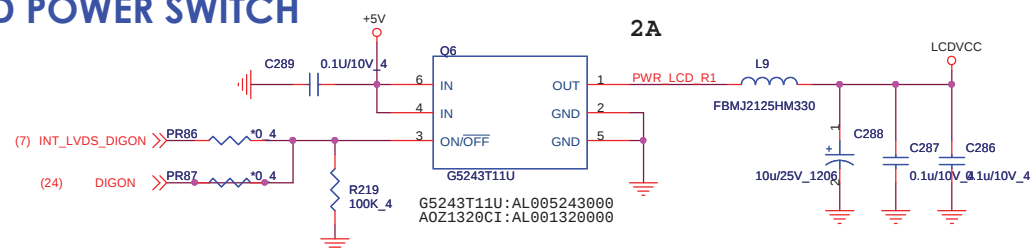
OFF=1= Hi On= 0= Low



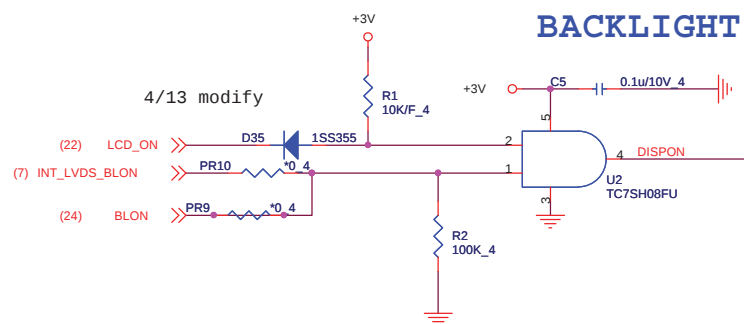
LCD CONNECTOR **LCD MODULE**



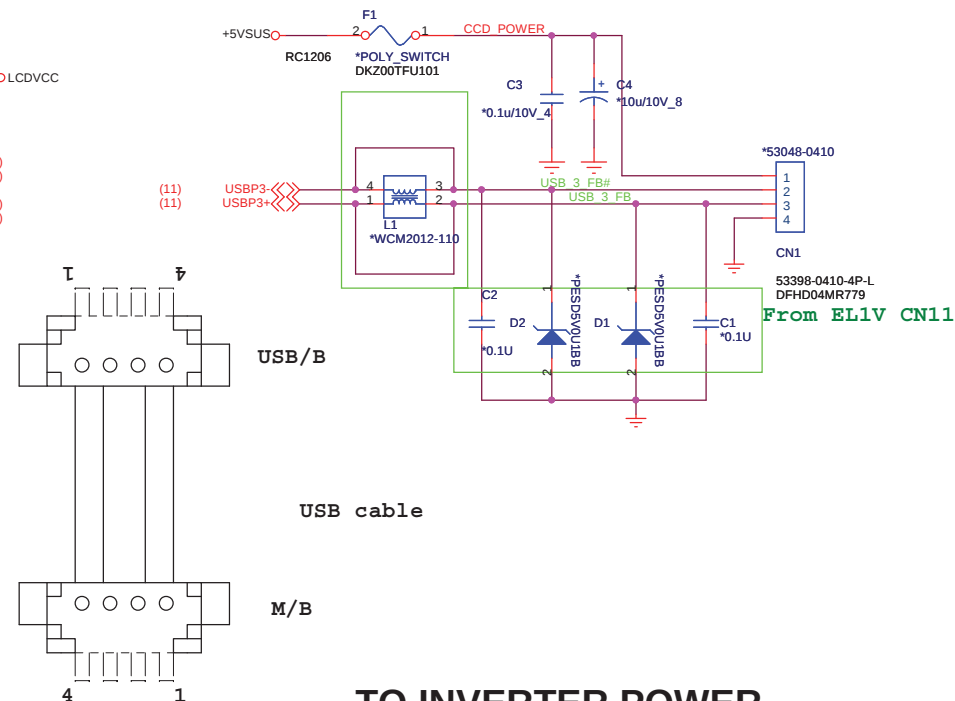
LCD POWER SWITCH



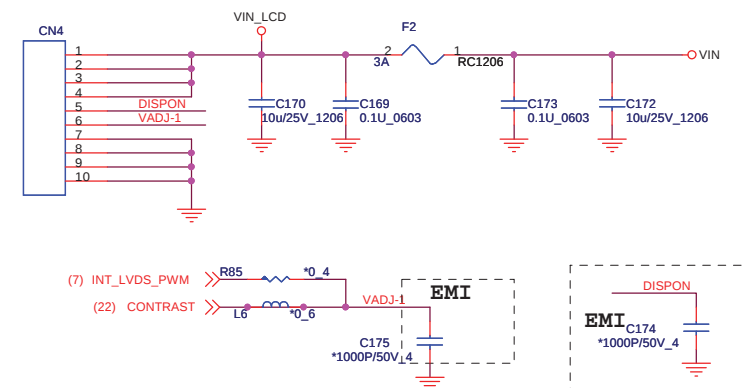
BACKLIGHT CONTROL

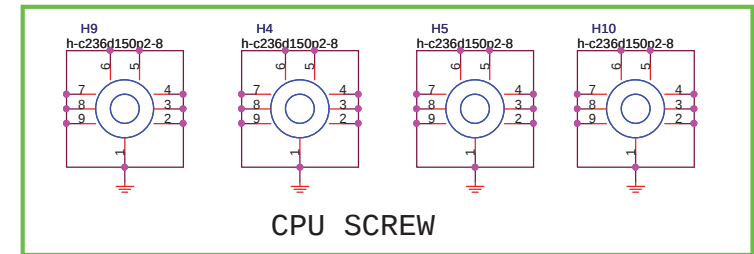
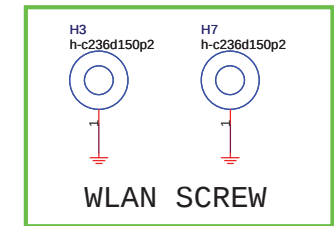
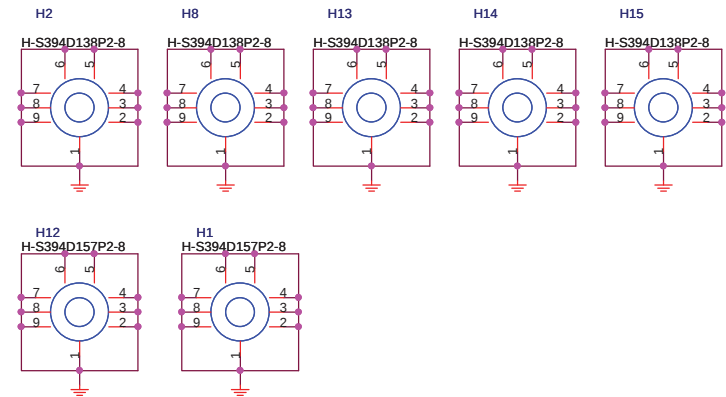
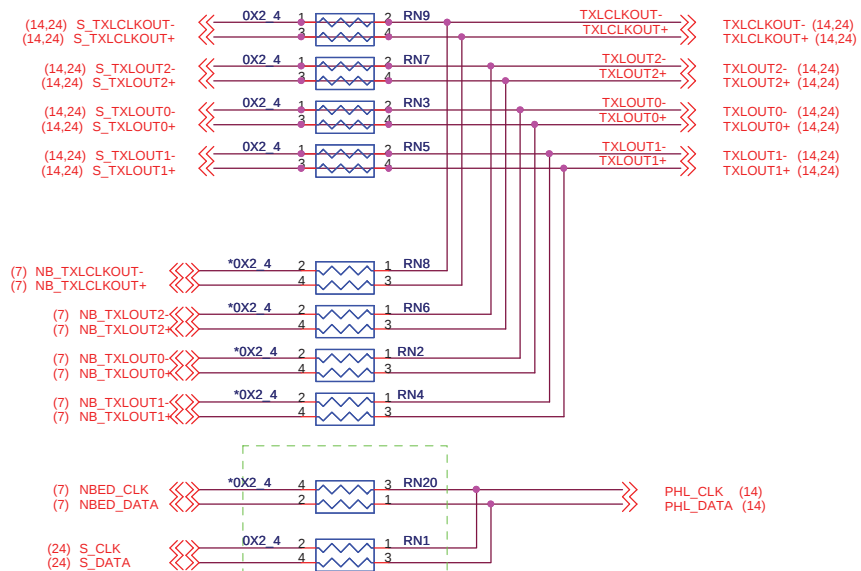


CAMERA POWER



TO INVERTER POWER





Modify footprint 2009/03/05 by Jimmy:h-c236d150p2-8
NUT is the same as JRI:MBJR1003010



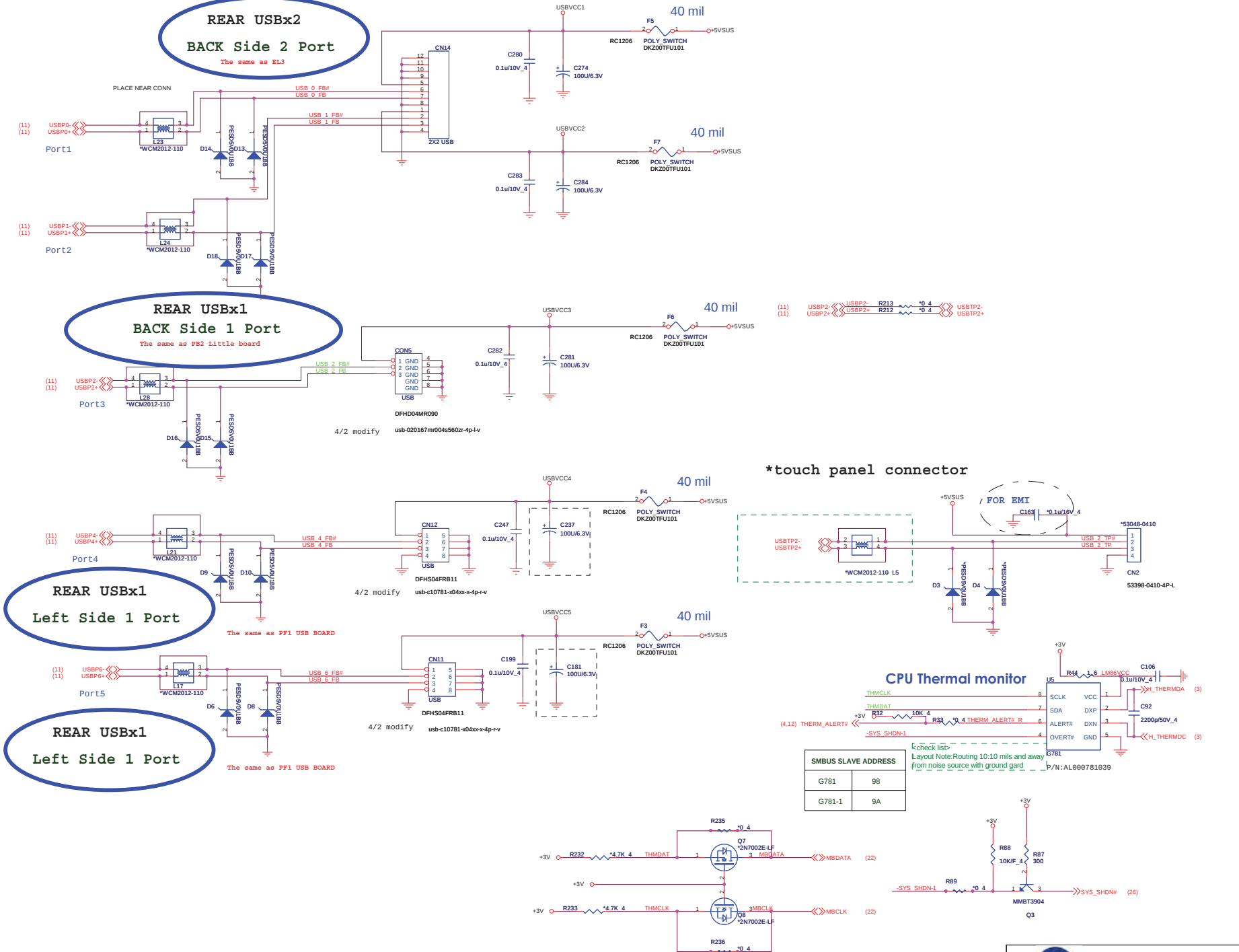
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LVDS Bridge/HOLES

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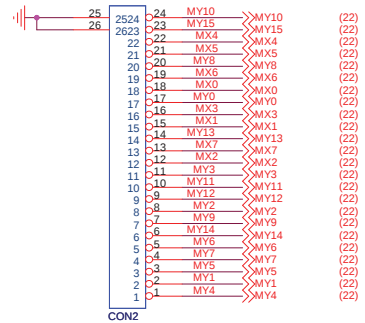




KEYBOARD For debug

(22) MY[15..0] >>> MB Side
(22) MX[7..0] >>> MB Side

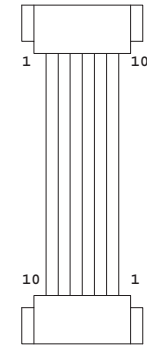
*88502-2401-24P-L



From EL1V

TOP Side

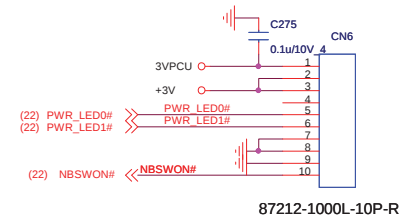
MB Side



TOP Side

SWITCH/B Side

Power SW



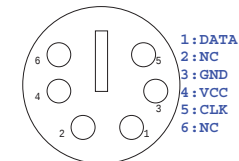
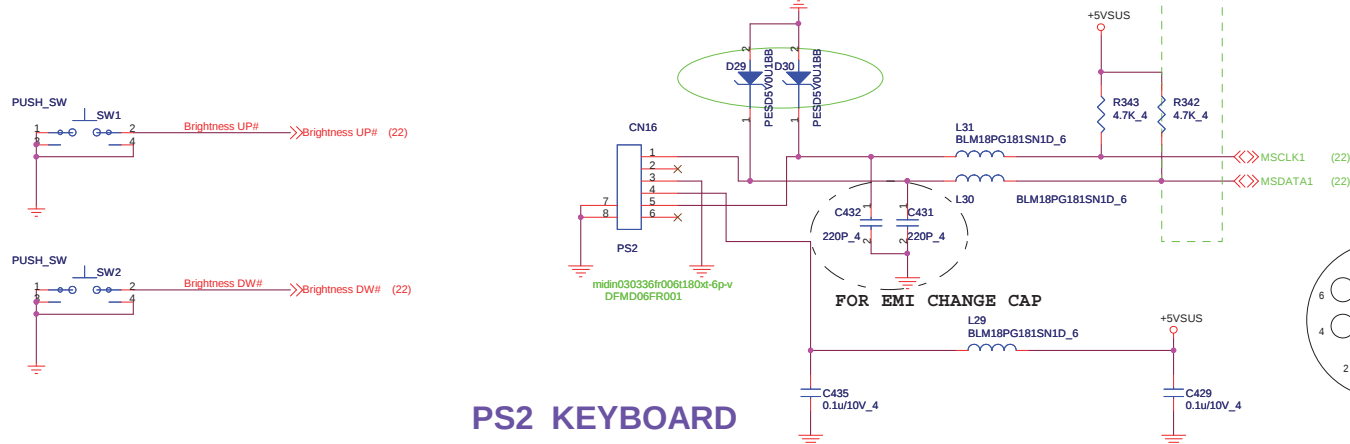
Modify 2209/03/02 :the same as CN4

Brightness Control

PS2 MOUSE

Green

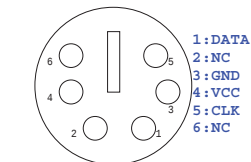
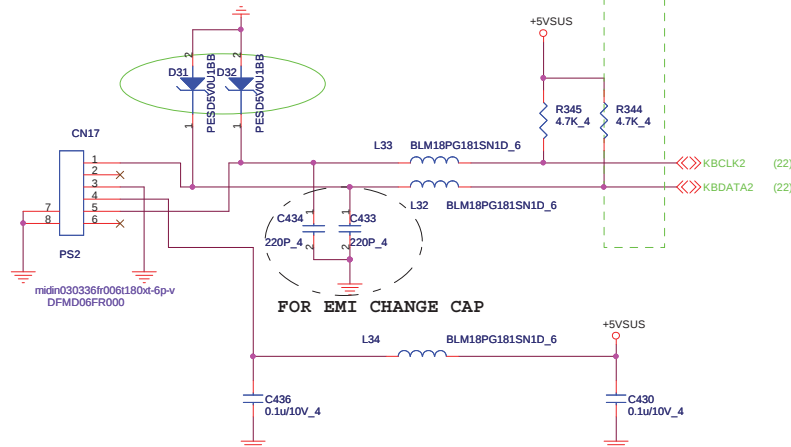
close to conn to version:A

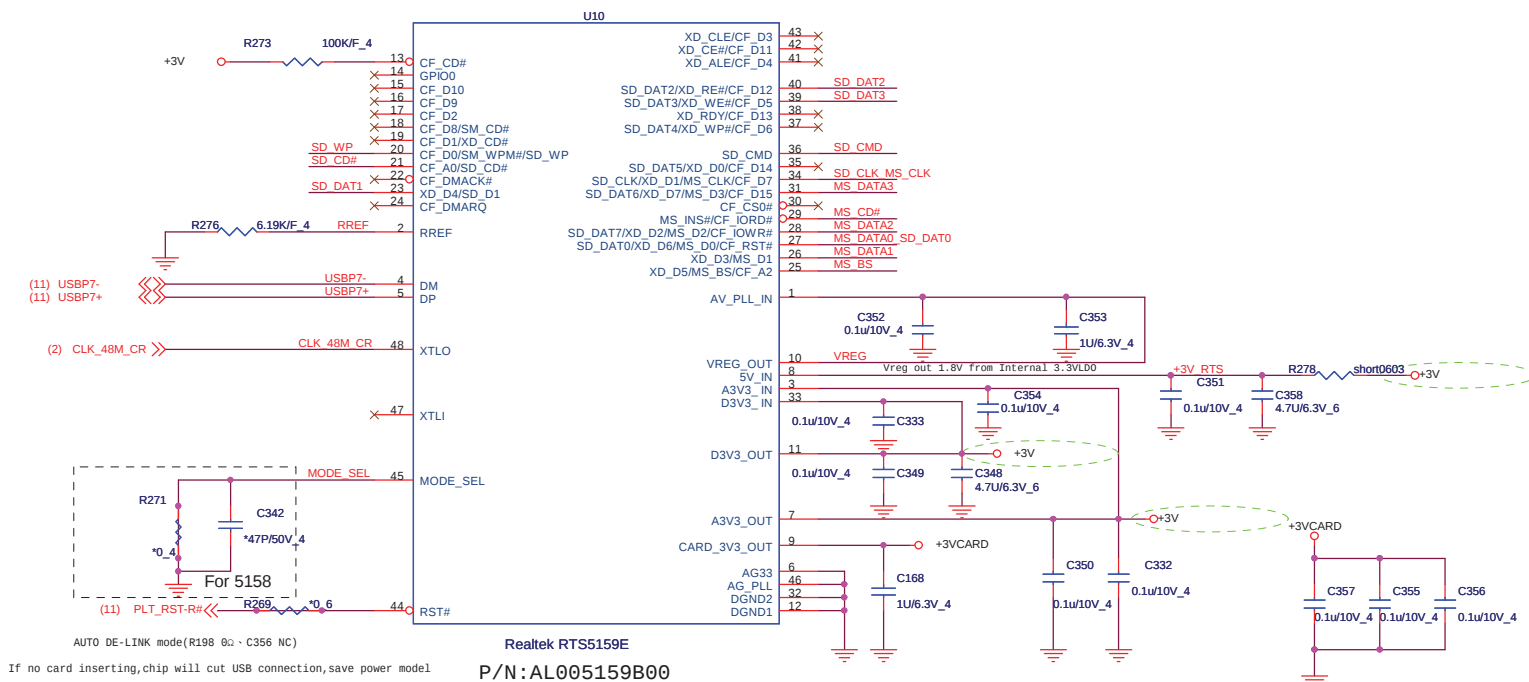


PS2 KEYBOARD

Purple

close to conn to version:A

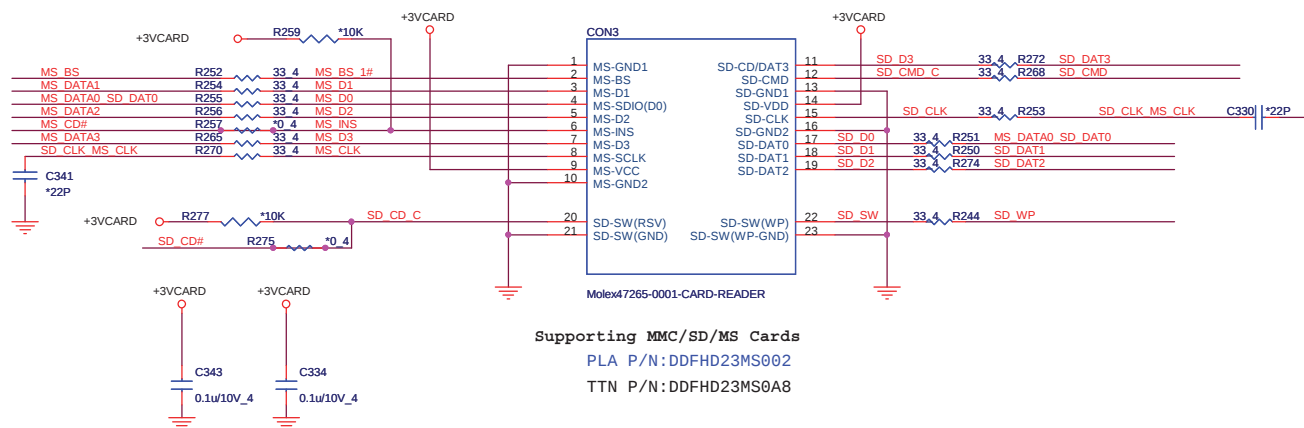




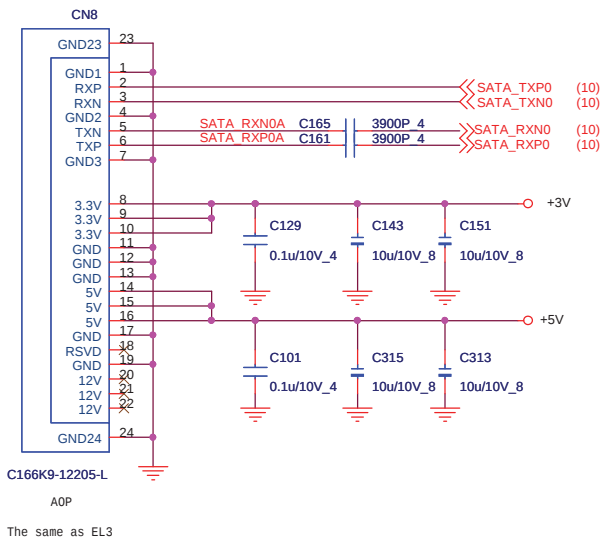
	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2			XD_WP
SP3			XD_CD#
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7		MS_D0	XD_D6
SP8		MS_D2	XD_D2
SP9		MS_INS#	
SP10		MS_D3	XD_D7
SP11		MS_SCLK	XD_D1
SP12			XD_D0
SP13			XD_WP#
SP14			XD_RB#
SP15			XD_WE#
SP16			XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

4 IN 1 CONN

From PB2

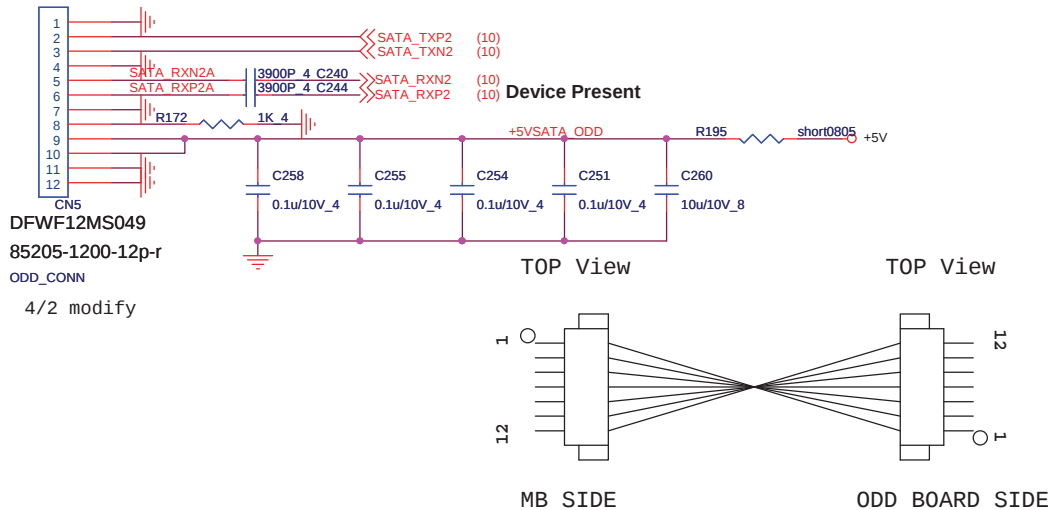


SATA HDD



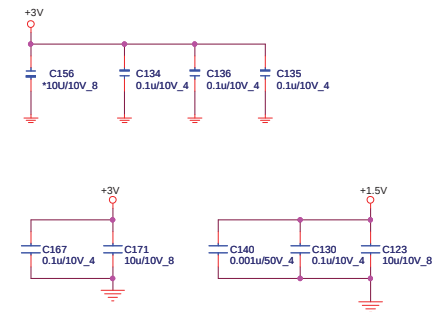
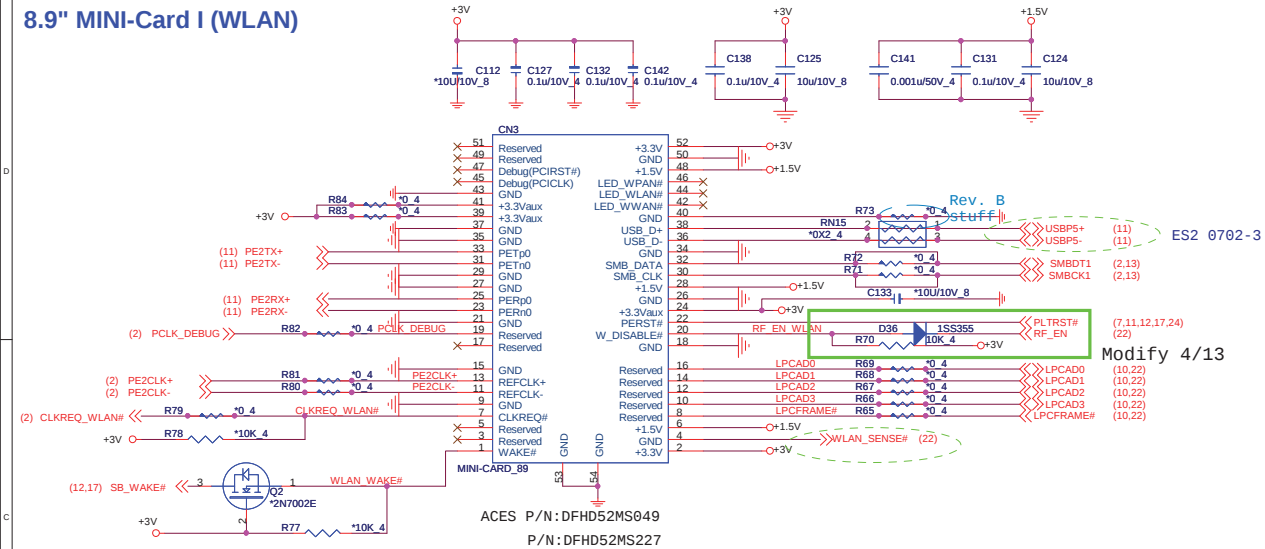
SATA ODD

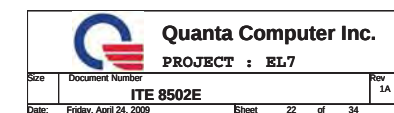
Check New ODD CONN Pin Define.

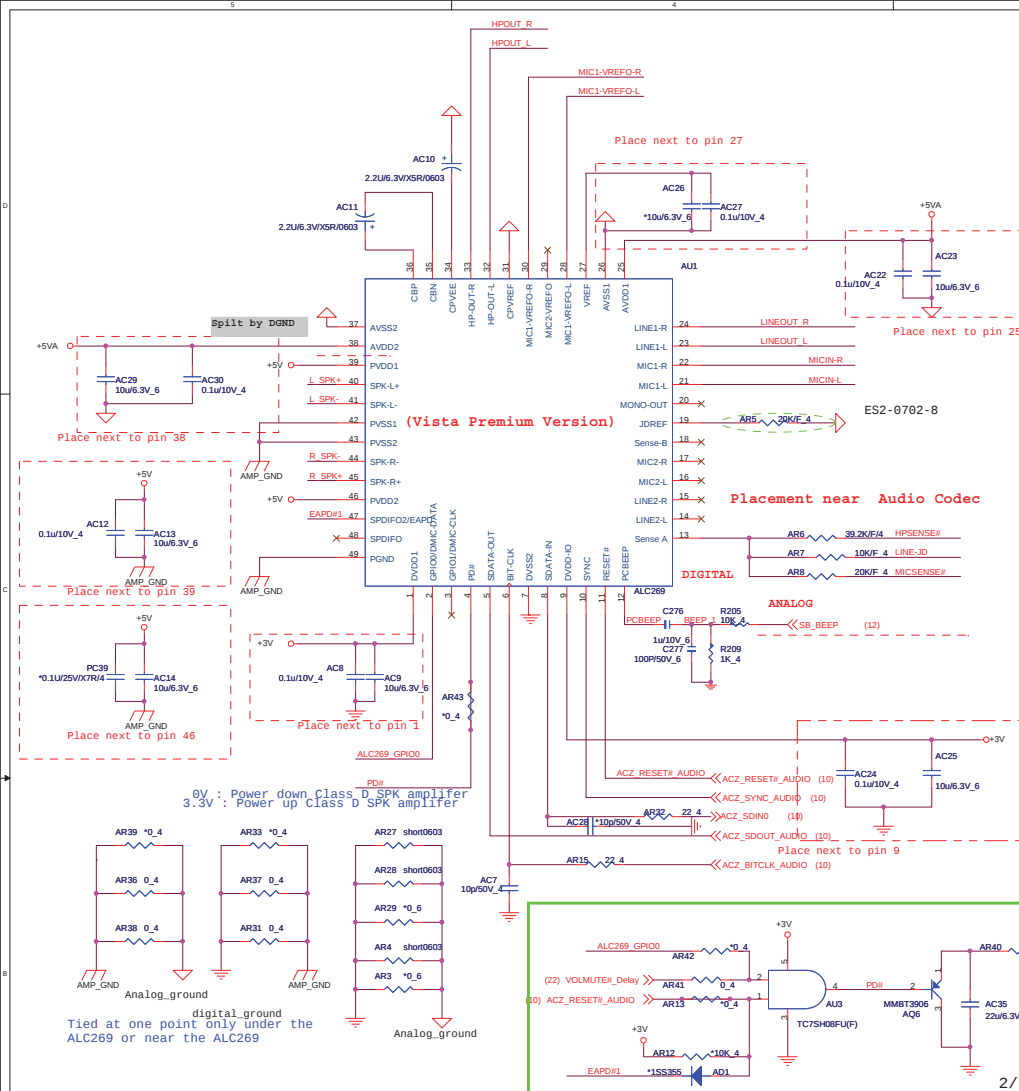


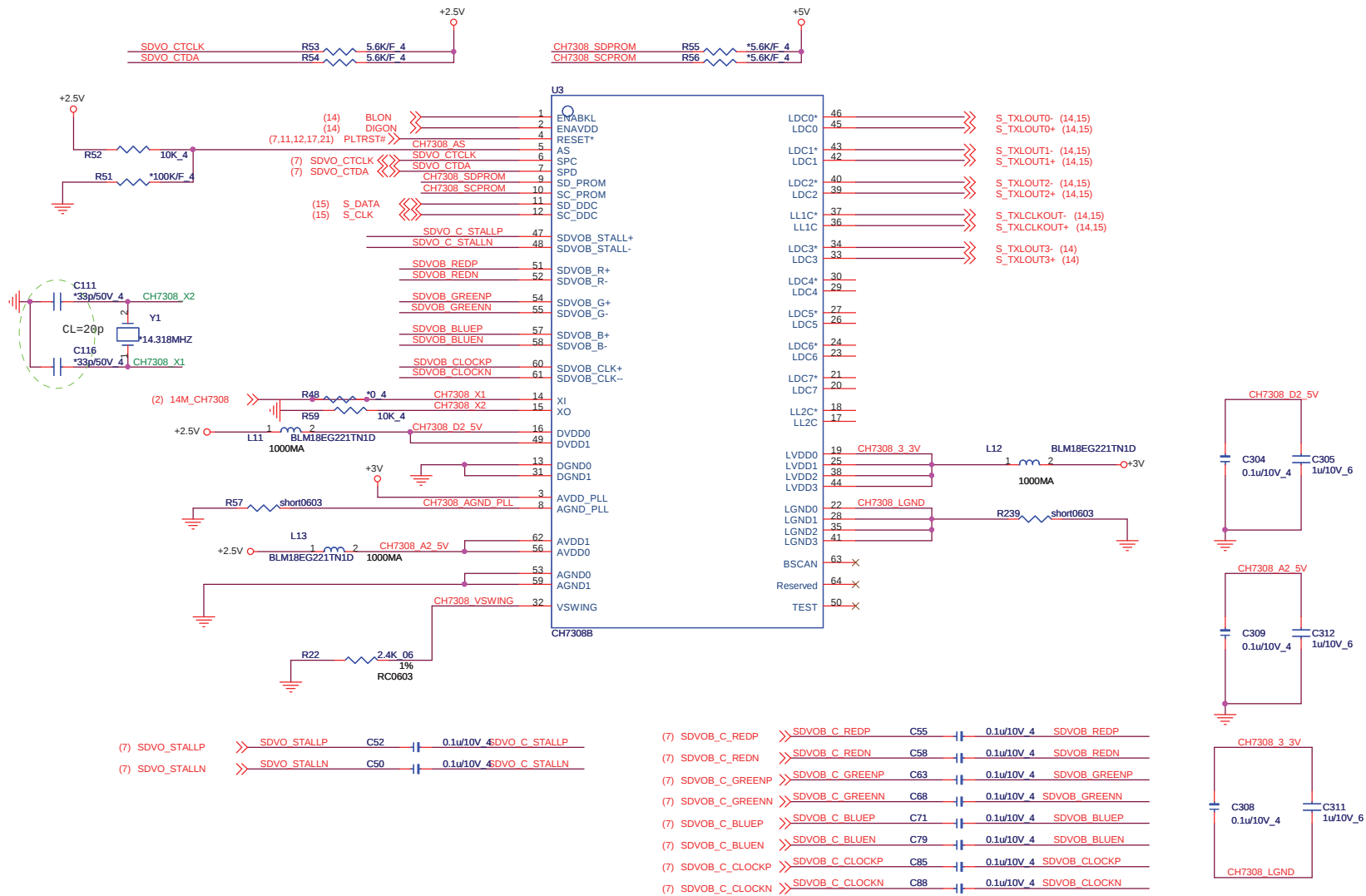
ZT4 card connector

8.9" MINI-Card I (WLAN)







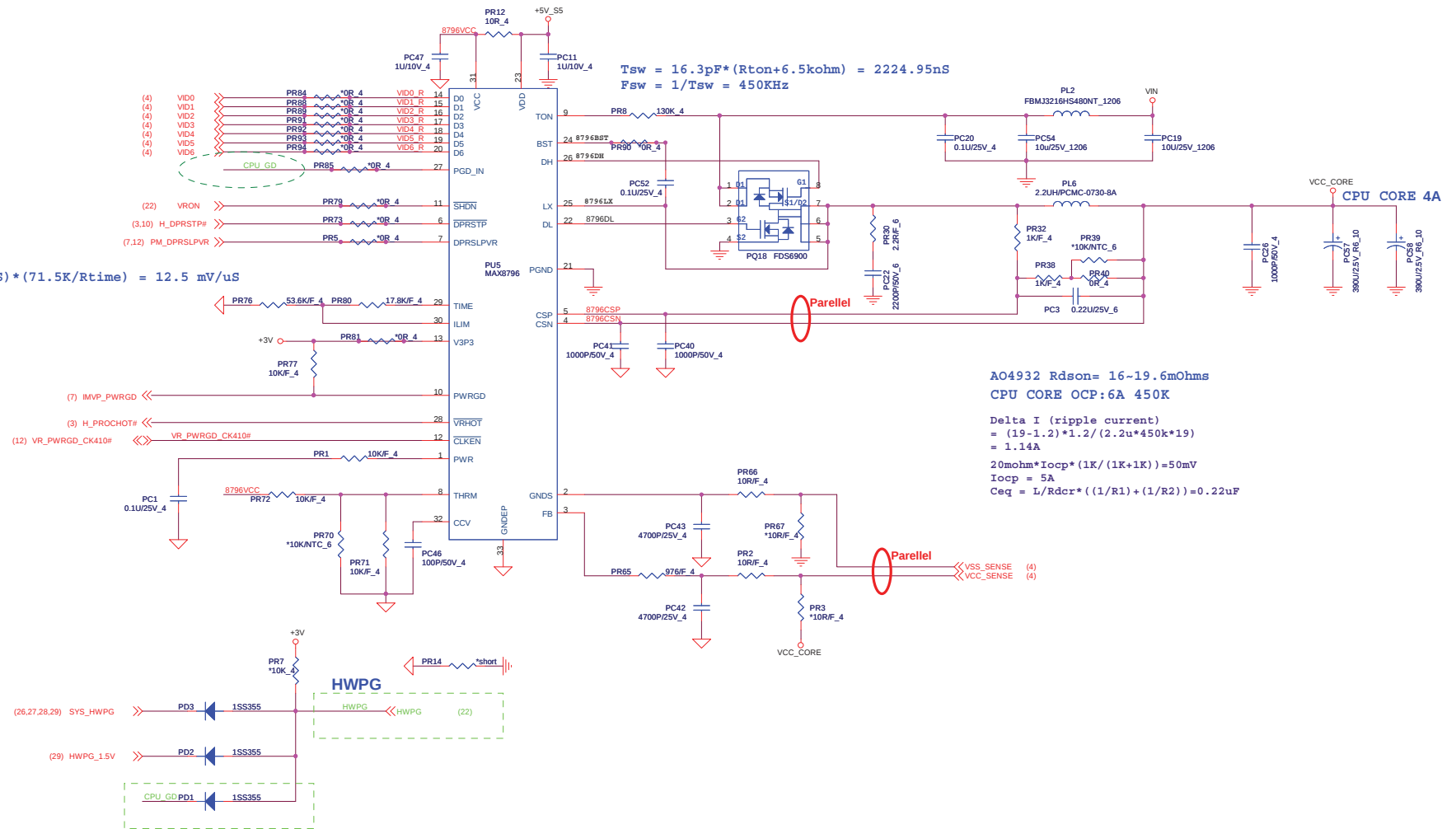


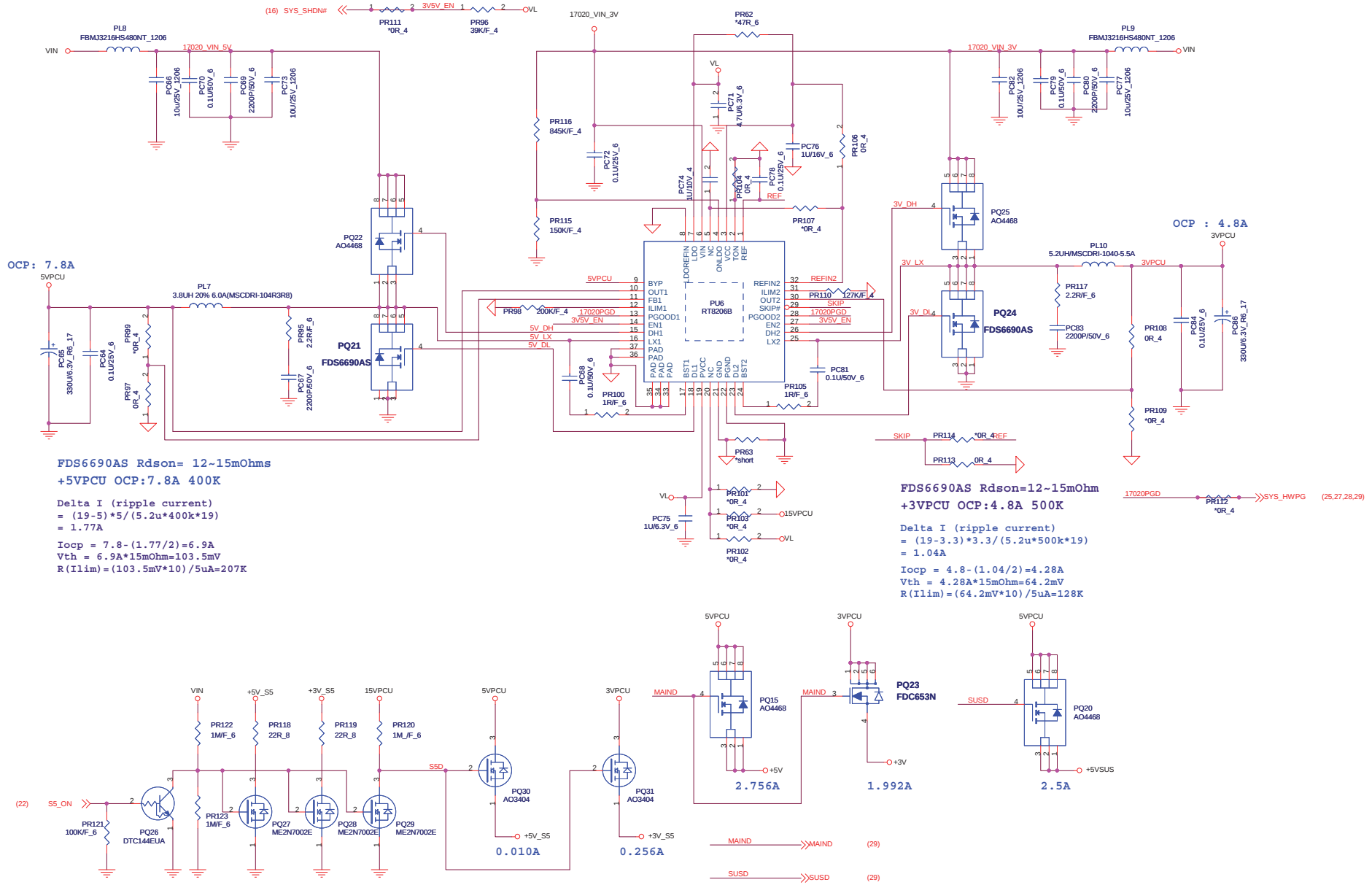
Close to GMCH

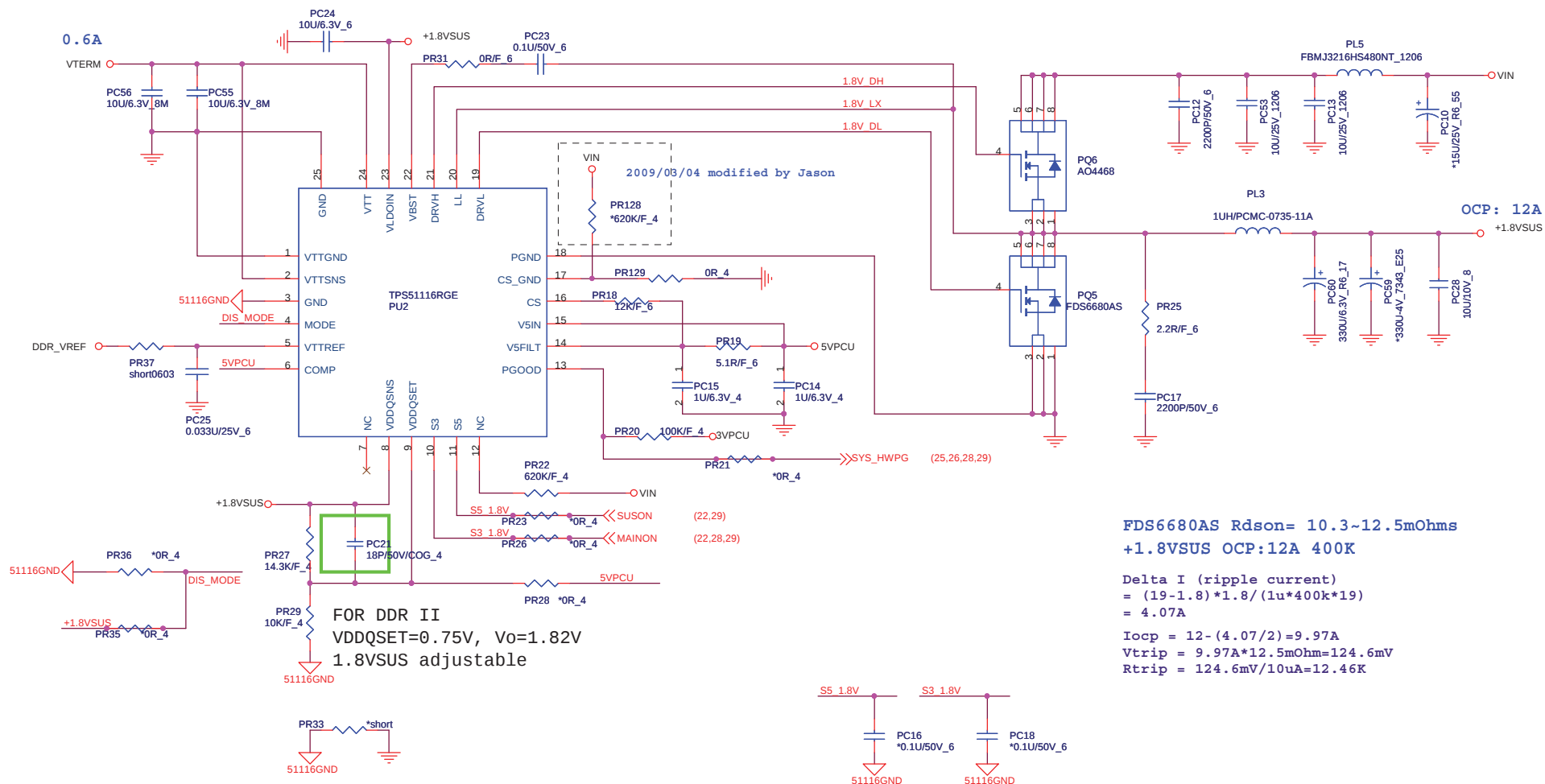


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PROJECT : EL7

$$20\text{mohm} \cdot I_{ocp} \cdot (1K / (1K + 1K)) = 50\text{mV}$$
$$I_{ocp} = 5A$$
$$C_{eq} = L / R_{dcr} \cdot ((1/R_1) + (1/R_2)) = 0.22\mu F$$




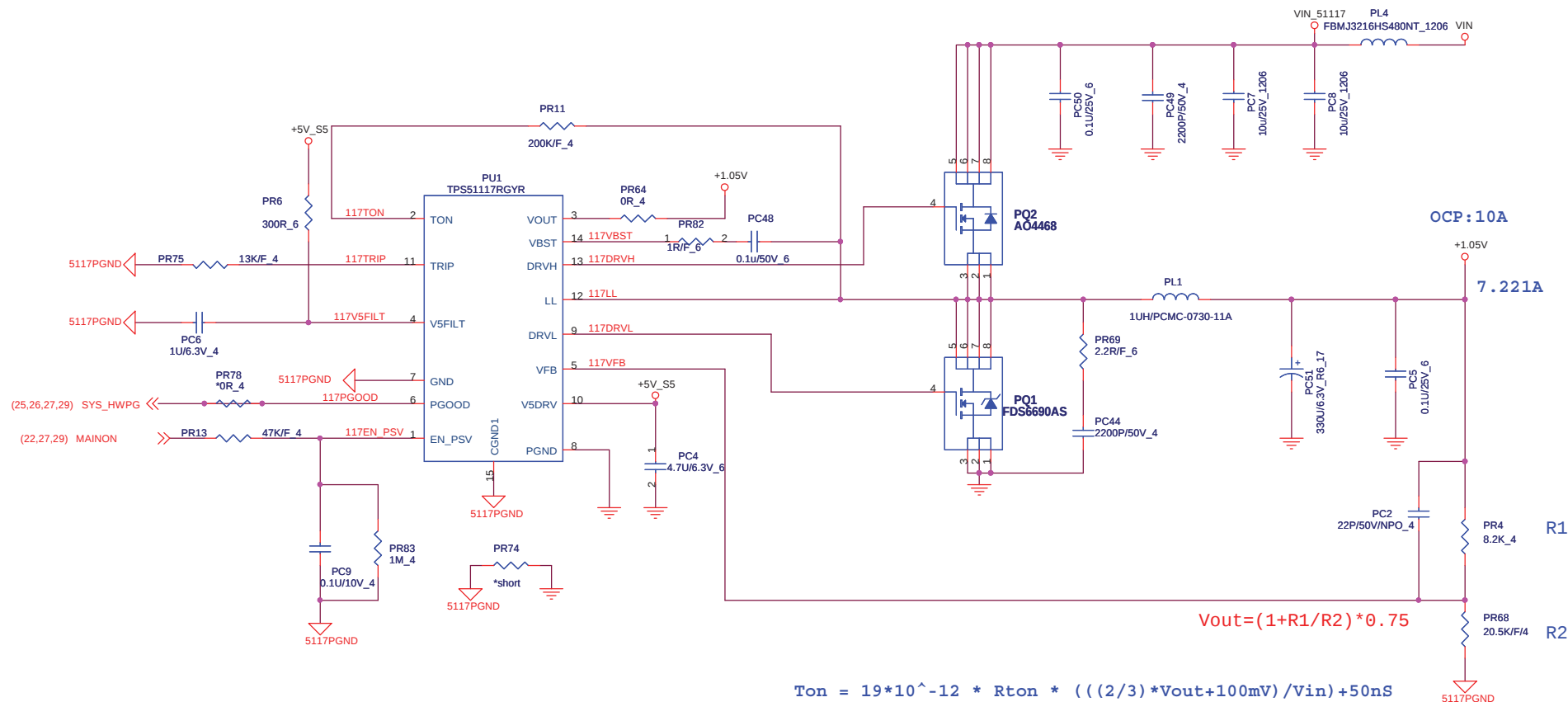


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	TPS51116REGR/1.8VSUS	1A

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$$\begin{aligned}
 T_{on} &= 19 \cdot 10^{-12} \cdot R_{ton} \cdot ((2/3) \cdot V_{out} + 100mV) / V_{in} + 50ns \\
 &= 210ns \\
 f &= (1/T_{on}) \cdot (V_{out}/V_{in}) \\
 &\approx 263Hz
 \end{aligned}$$

FDS6690AS $R_{dson} = 12 \sim 15m\Omega$
 +1.05V OCP:10A 263K

$$\begin{aligned}
 \Delta I \text{ (ripple current)} &= (19 - 1.05) \cdot 1.05 / (1u \cdot 263k \cdot 19) \\
 &= 3.77A
 \end{aligned}$$

$$\begin{aligned}
 I_{ocp} &= 10 - (3.77/2) = 8.16A \\
 V_{trip} &= 8.16A \cdot 15m\Omega = 122.4mV \\
 R_{trip} &= 122.4mV / 10uA = 12.24K
 \end{aligned}$$

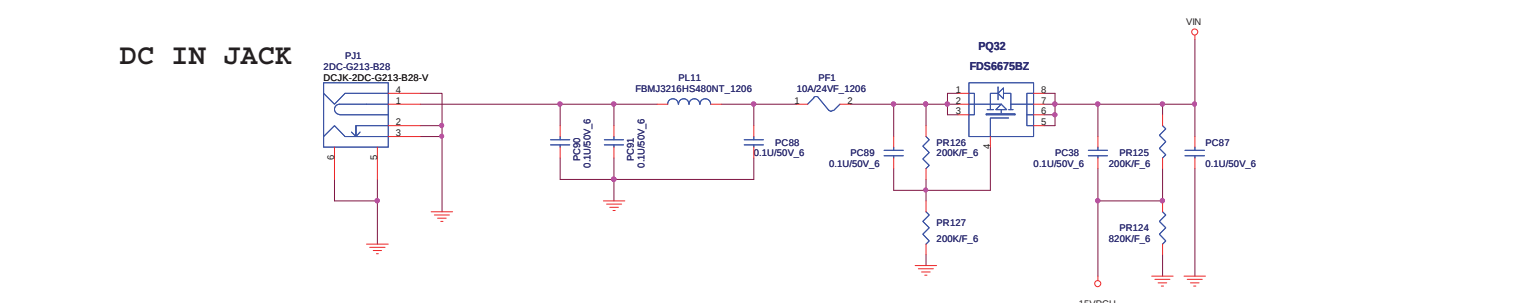


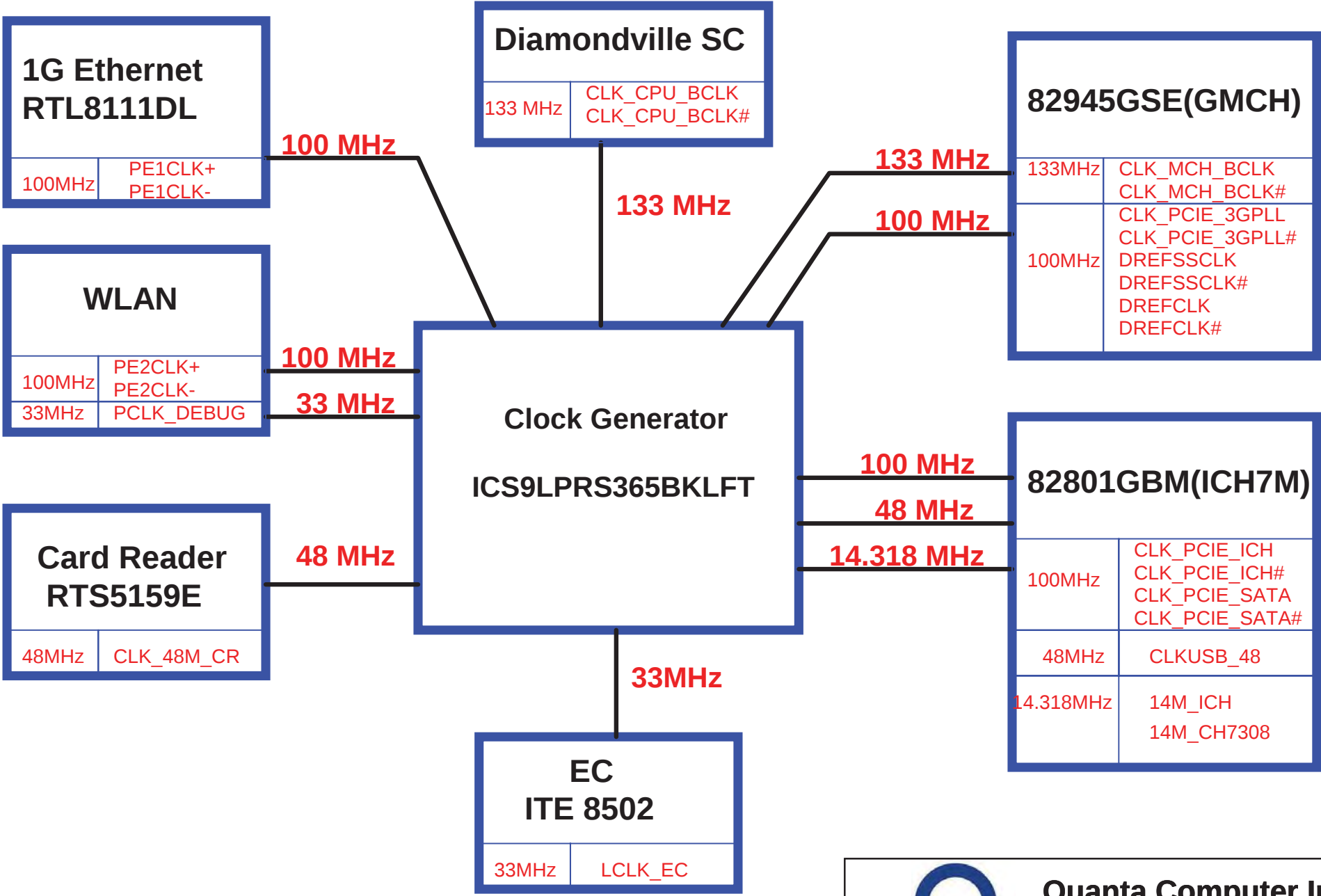
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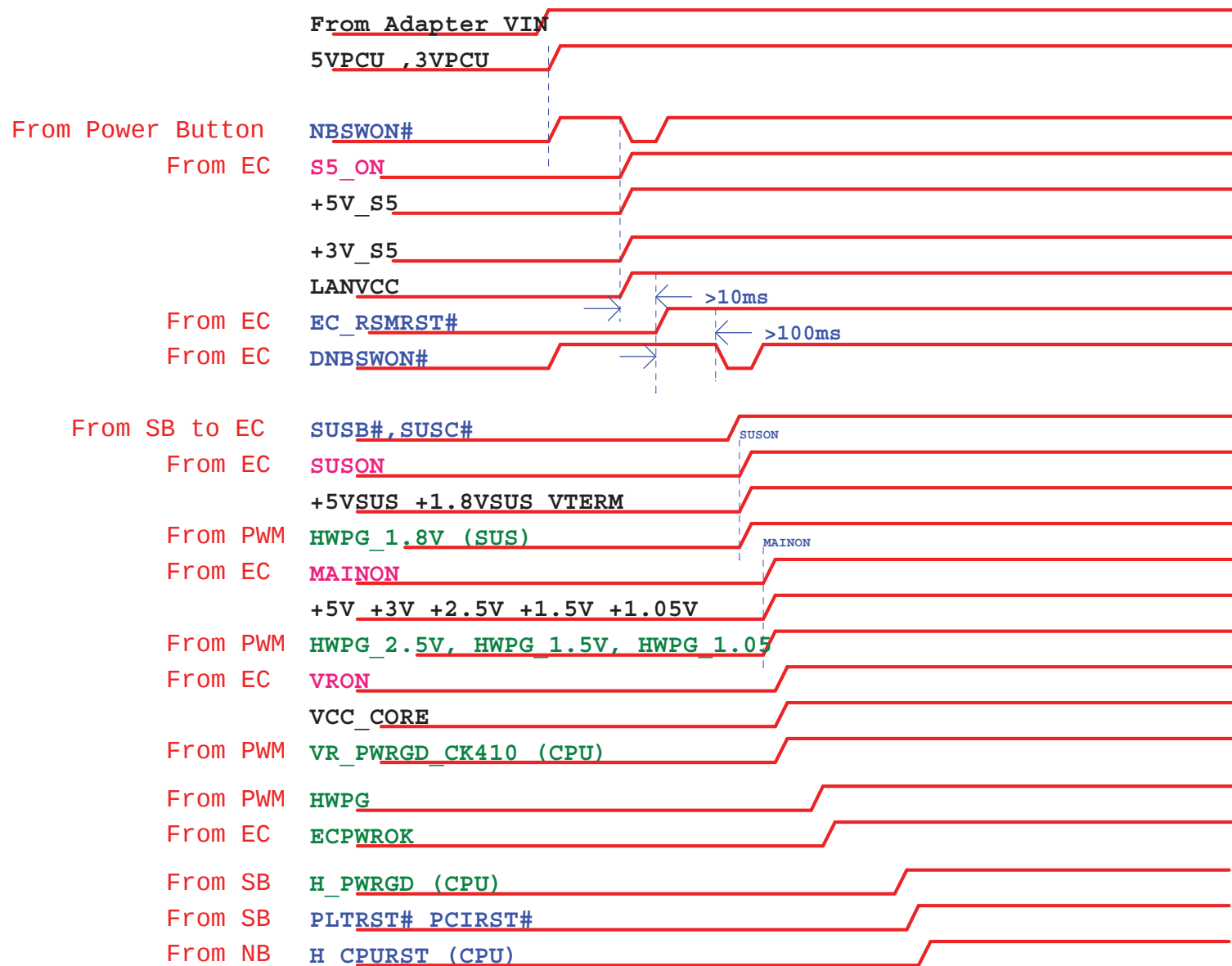
Size	Document Number	Rev
	VCCP 1.05V(TPS51117)	1A

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Power On Sequence

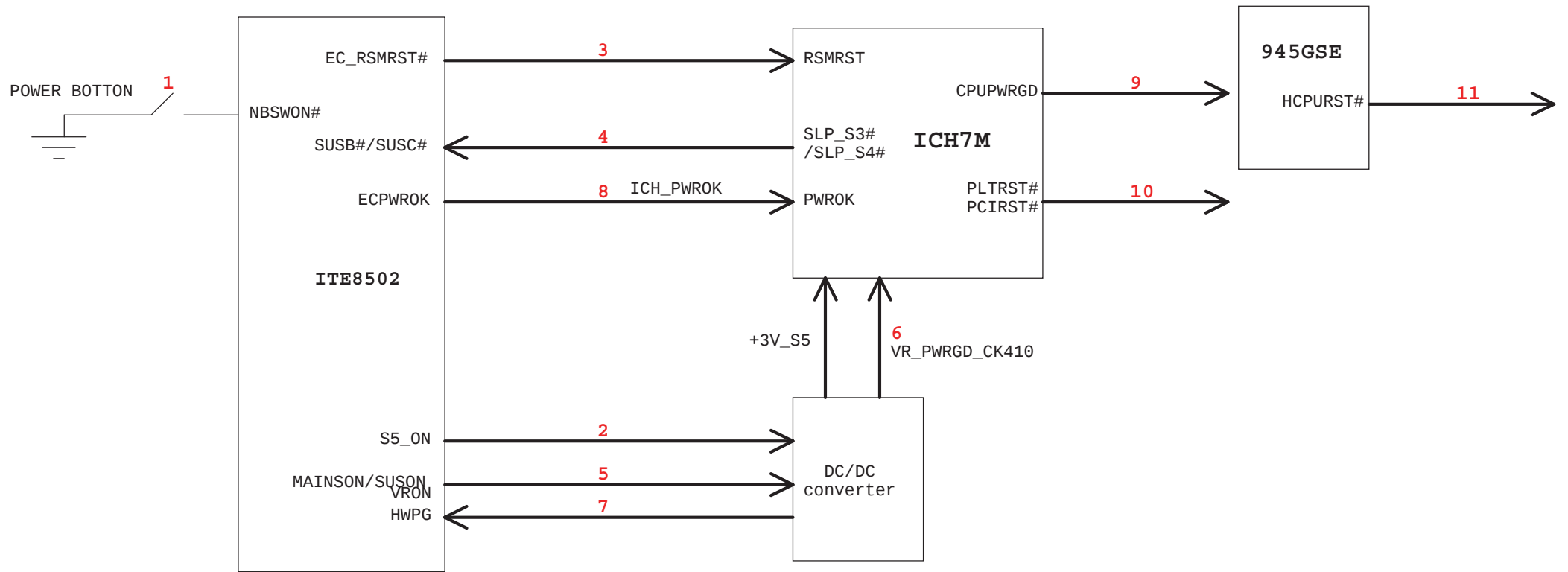


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PROJECT : EL7

Size	Document Number	Rev
	EL7 Power On Sequence	1A

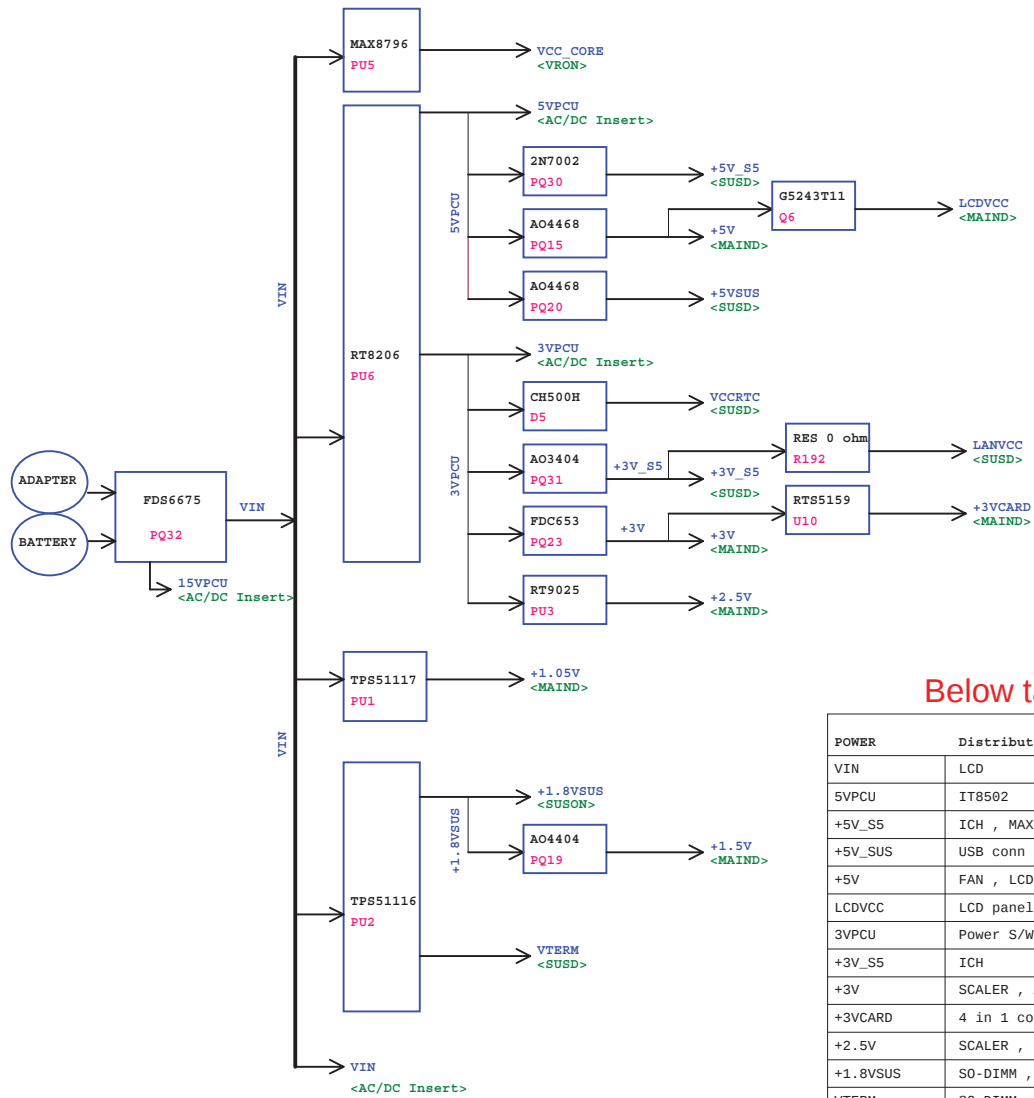
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Size	Document Number	Rev
	Power On Diagram	1A
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Below table need be modify (waiting other schematic ready)

POWER	Distribution
VIN	LCD
5VPCU	IT8502
+5V_S5	ICH , MAX8796 , TPS51117
+5V_SUS	USB conn , PS/2 mouse K/B conn , CAMERA
+5V	FAN , LCD , SATA HDD , SATA ODD , ALC269 , ICH
LCDVCC	LCD panel
3VPCU	Power S/W , IT8502 , ICH
+3V_S5	ICH
+3V	SCALER , ALC269 , IT8502 , CLK gen , MCH , ICH , SO-DIMM , EDID EEPROM , SATA HDD , SSD , WLAN , Power S/W , G781 , RTL8111 , RTS5159
+3VCARD	4 in 1 conn
+2.5V	SCALER , MCH
+1.8VSUS	SO-DIMM , MCH , TPS51116
VTERM	SO-DIMM
+1.5V	CPU , MCH , ICH , WLAN
+1.05V	CLK gen , CPU , MCH , ICH
VCC_CORE	CPU
LANVCC	RTL8111

DATE	Modify Description List	Note
2009 0302 VER:B	1.PAG23 SPK Change ACN1 :the same as CN1 or CN2 (53398-0410-4P-L) 2.PAG18 SW Change CN6:the same as CN4 (87212-1000L-10P-R) 3.PAG20&PG18 Remove SSD module ,H6 and H11 4.PAG12 Signal MID2 change form GPIO35 to GPIO14 5.Change caps or resistors footprints with "-C" to non "-C" 6.PAG16 Chage C274,C281 and C284 to CC3528	
2009 0303 VER:B	1.PAG16 delete R129,R132,R181,R185 of USB 2.PAG25 Short 0 Ohm resistor:PR84,PR88,PR89,PR91,PR92,PR93,PR94,PR85,PR79,PR73,PR5,PR81,PR90 3.PAG26 Short 0 Ohm resistor:PR104,PR111,PR112 4.PAG29 Short 0 Ohm resistor:PR49,PR51 5.PAG22 Modify EC Pin3 to VCCRTC 6.PAG29 Solve +1.5 discharge circuit short problem 7.PAG23 Modify AL6,AL7,AL8,AL9,AC31,AC32,AC33,AC34 8.PAG12 Change GPIO6 to BIOS_WP#,delete R164,R165 9.PAG22 ADD BIOS PROTECT Circuit	
2009 0305 VER:B	1.PAG18 Change L29,L30,L31,L32,L33,L34 to BLM18PG181SN1D_6(The same as L10) 2.PAG27 Add PR129	
2009 0413 VER:C	1.PAG16 Chage C237,C181 to CC3528 2.PAG20 Chage CN5 footprint to 85205-1200-12p-r (DFWF12MS049) 3.PAG14 Add D35 U2 pin connector to EC U14_124 LCD_ON 4.PAG17 Add D33,D34 GPIO34 LAN_ON_SB and LAN_ON_EC U12 pin28 5.PAG21 Add D36,R70 6.PAG22 Add U20,C437	