ZY6D SYSTEM BLOCK DIAGRAM

BOM MARK

E@ EXT VGA 璁ゲ
268@ AUDIO 268 璁ゲ
D@ DOCK
D2@ DDR2 璁ゲ
SP@ 疯 (EXT VGA OR DDR2)
ED2@ EXT VGA & DDR2 璁ゲ
CB@ CARDBUS 璁ゲ
NSF@ Non ASF 璁ゲ

I@ INT VGA 璁ゲ
888@ AUDIO 888璁ゲ
D3@ DDR3 璁ゲ
ND@ NON DOCK 璁ゲ
ID2@ INT VGA & DDR2 璁ゲ
ED3@ EXT VGA & DDR3 璁ゲ
ID3@ INT VGA & DDR3 璁ゲ
ASF@ ASF 璁ゲ
NCB@ NON CARDBUS 璁ゲ

LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI

X'TAL 14.318MHZ
CLOCK GENERATOR
ICS: ICS9LPRS365BGLFT
SELGO: SLG8SP512K05
P2

Penryn 479 uFCPGA P3,P4
CPU Thermal Sensor P3

FSB 667/800/1067 Mhz

DDRII SO-DIMM 0 SO-DIMM 1 P16
Dual Channel DDR2 667/800 MHz

NB Cantiga PM965 P5,P6,P7,P8,P9,P10,P11
CRT Page:19
LVDS Page:19

X4 DMI interface

HDD (SATA)*2 P25
ODD (SATA) P25
SATA0
SATA1
SATA4

SB ICH9M P12,P13,P14,P15
X'TAL 32.768KHZ

PCI-Express
PCIE-4
WLAN P23
PCIE-6
X'TAL 25M
BROADCOM 10/100/1G LAN 5764M P21
SWITCH CIRCUIT Page:22
LAN Page: 33
Transformer P22
RJ45 P22

USB 2.0
USB Port x 4 USB0~3 P25
CCD USB7 P19

Azalia
Int MIC P27
Azalia Audio Controller ALC268 & 888 P27
Audio Amplifier P27 & 28
Connector
Speaker P28
Phone Jack P28
SPDIF P28
Line in P28
MIC Jack P28

LPC
EC (WPC8769LDG) P32
X'TAL 32.768K
SPI ROM P32
Touch Pad P32
K/B COON. P32

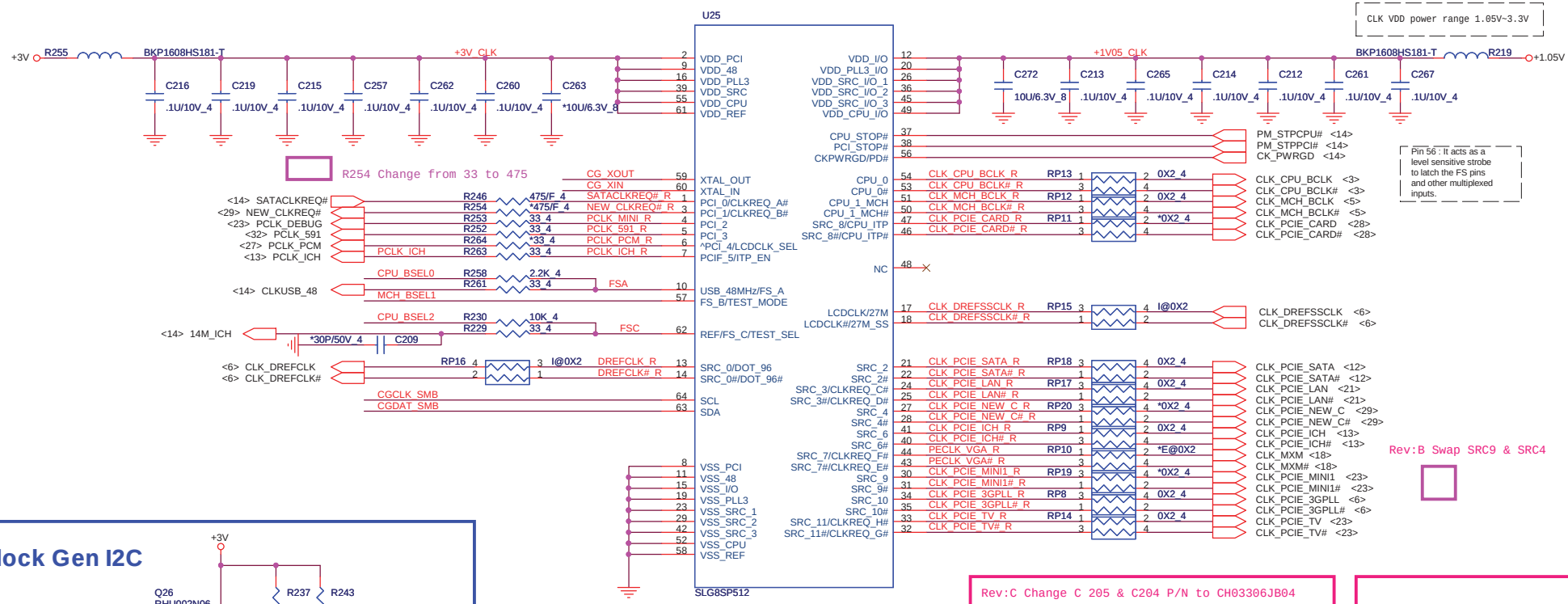
Fan Header P31

Quanta Computer Inc.
PROJECT : ZY6D

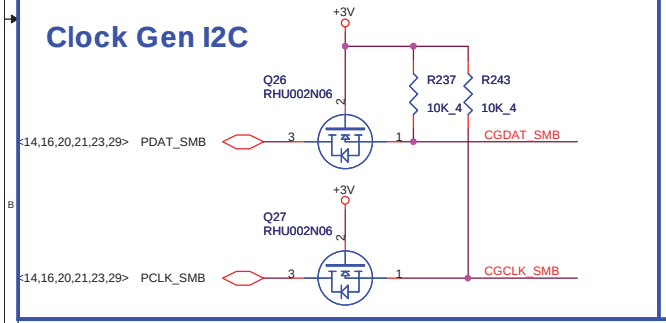
Size	Document Number	Rev
	Block Diagram	1A

Date: Thursday, August 28, 2008 Sheet 1 of 40

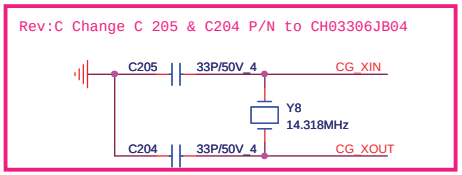
Clock Generator



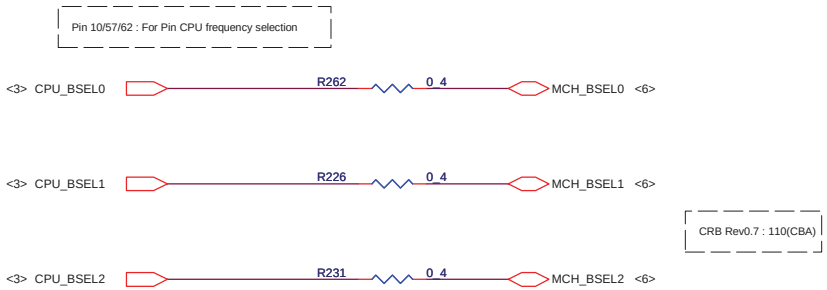
Clock Gen I2C



	QCI P/N
SLG8SP512	AL8SP512K05
ICS9LPRS365BGLFT	ALPRS365K13



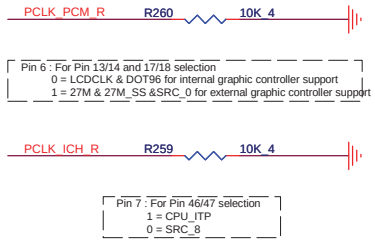
CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

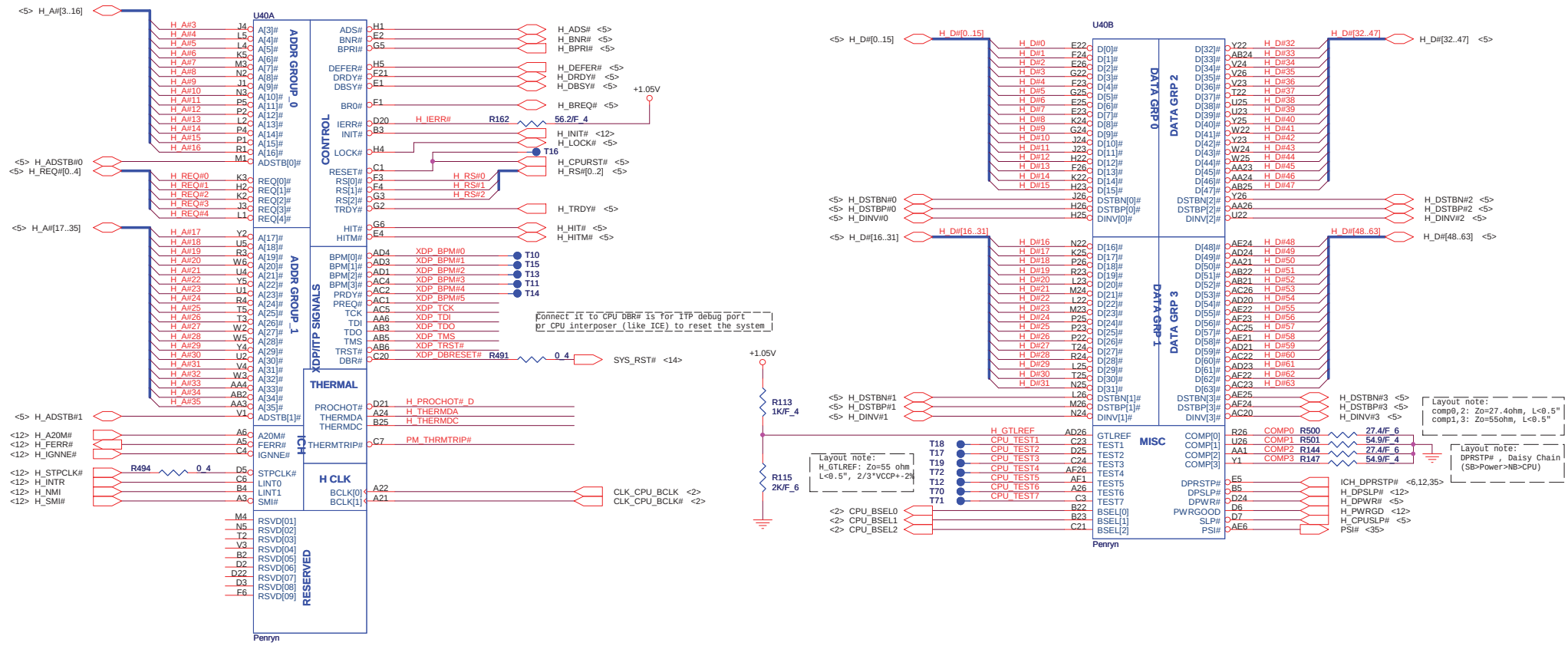
Strap table



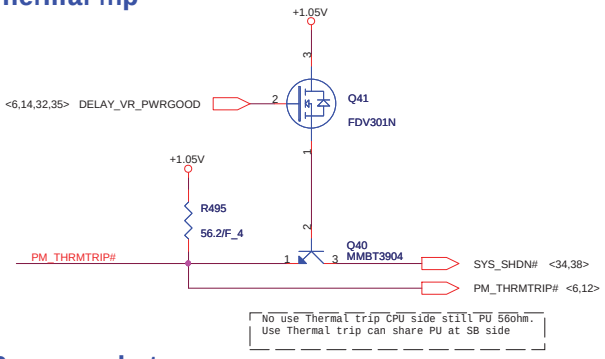
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

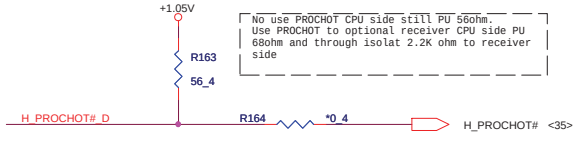
Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	1A
Date: Thursday, August 28, 2008	Sheet 2 of 40	



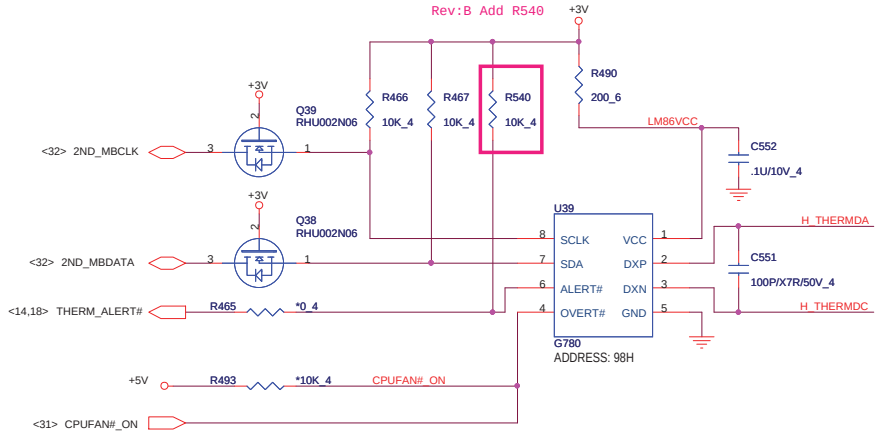
Thermal Trip



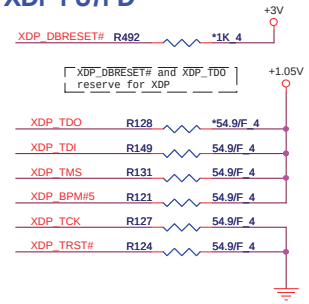
Processor hot



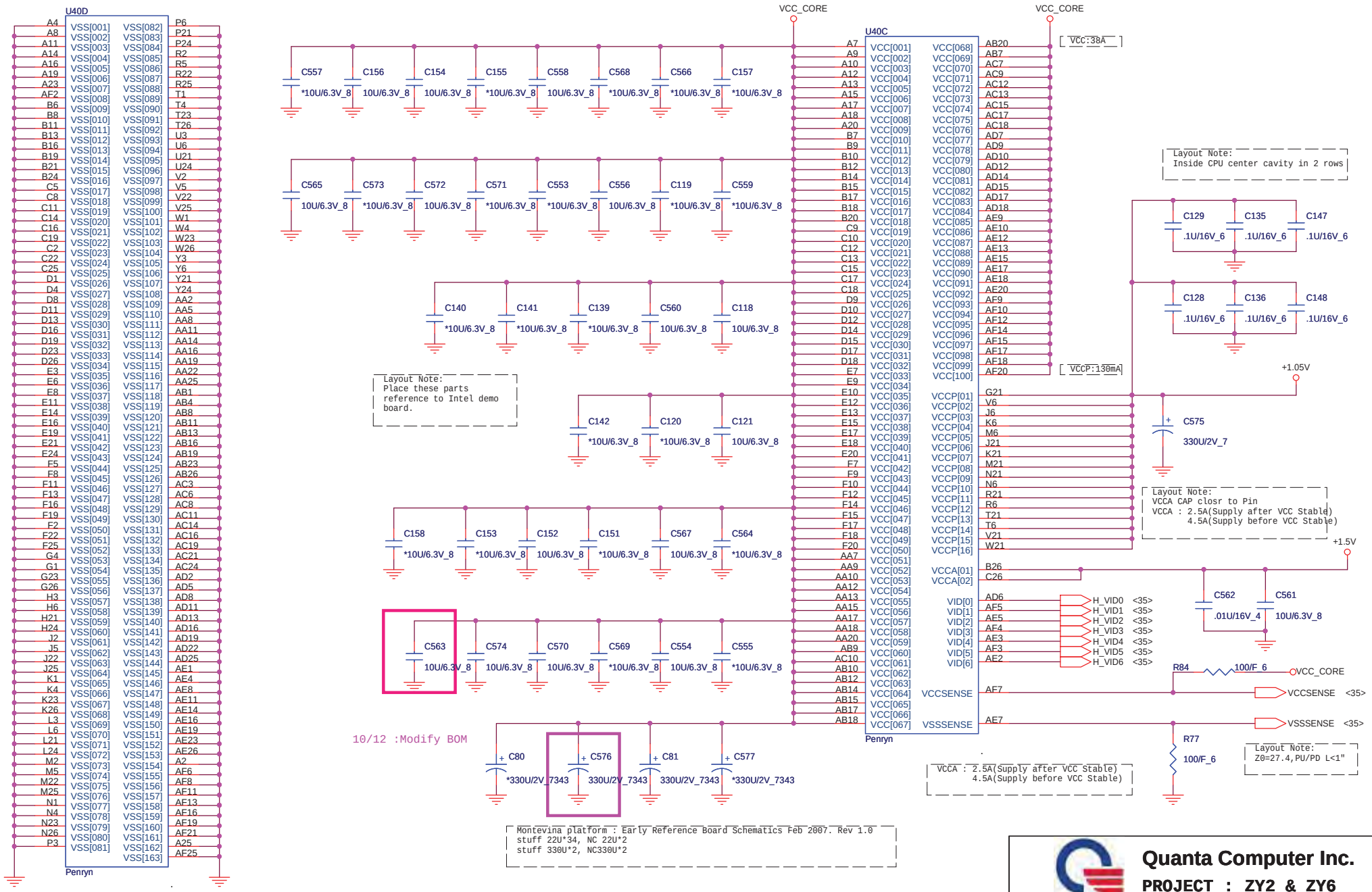
CPU Thermal monitor



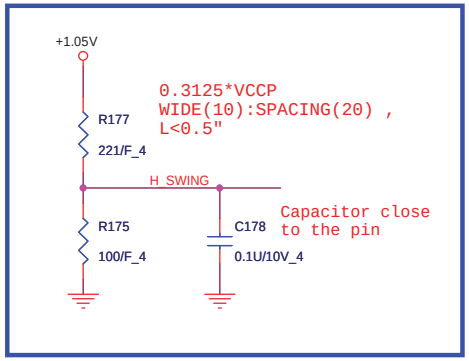
XDP PU/PD

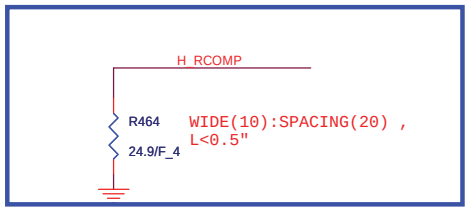


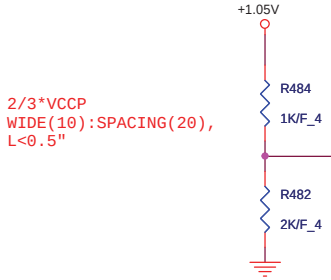
Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: CPU Host Bus	Rev: 1A
Date: Thursday, August 28, 2008	Sheet 3 of 40	

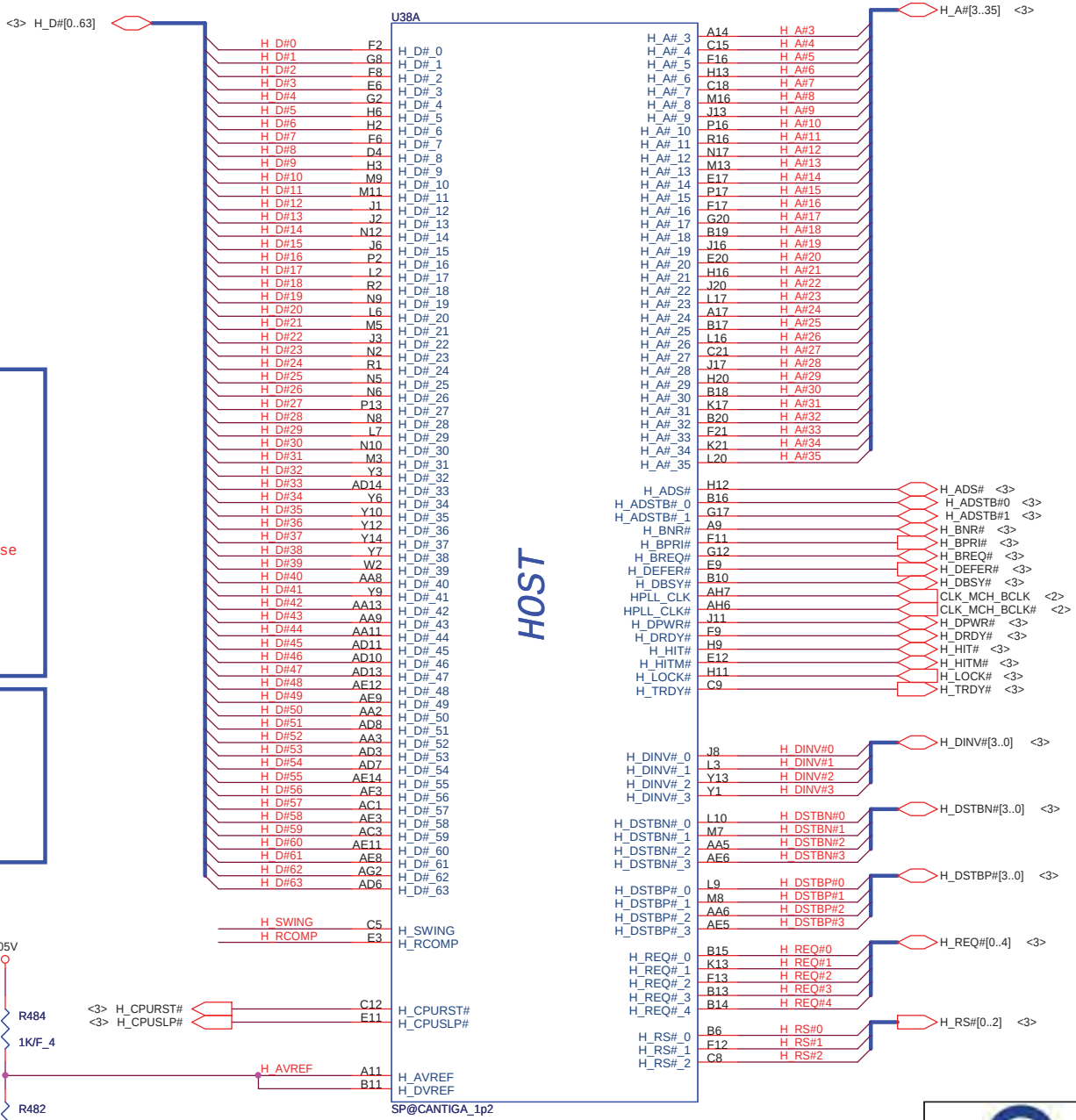

U40D
VSS[001] VSS[002] VSS[003] VSS[004] VSS[005] VSS[006] VSS[007] VSS[008] VSS[009] VSS[010] VSS[011] VSS[012] VSS[013] VSS[014] VSS[015] VSS[016] VSS[017] VSS[018] VSS[019] VSS[020] VSS[021] VSS[022] VSS[023] VSS[024] VSS[025] VSS[026] VSS[027] VSS[028] VSS[029] VSS[030] VSS[031] VSS[032] VSS[033] VSS[034] VSS[035] VSS[036] VSS[037] VSS[038] VSS[039] VSS[040] VSS[041] VSS[042] VSS[043] VSS[044] VSS[045] VSS[046] VSS[047] VSS[048] VSS[049] VSS[050] VSS[051] VSS[052] VSS[053] VSS[054] VSS[055] VSS[056] VSS[057] VSS[058] VSS[059] VSS[060] VSS[061] VSS[062] VSS[063] VSS[064] VSS[065] VSS[066] VSS[067] VSS[068] VSS[069] VSS[070] VSS[071] VSS[072] VSS[073] VSS[074] VSS[075] VSS[076] VSS[077] VSS[078] VSS[079] VSS[080] VSS[081] VSS[082] VSS[083] VSS[084] VSS[085] VSS[086] VSS[087] VSS[088] VSS[089] VSS[090] VSS[091] VSS[092] VSS[093] VSS[094] VSS[095] VSS[096] VSS[097] VSS[098] VSS[099] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163]
Penryn
VCC_CORE
C557 C156 C154 C155 C558 C568 C566 C157
*10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8 *10U/6.3V_8 *10U/6.3V_8
C565 C573 C572 C571 C553 C556 C119 C559
10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8 *10U/6.3V_8
C140 C141 C139 C560 C118
*10U/6.3V_8 *10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 10U/6.3V_8
Layout Note:
Place these parts
reference to Intel demo
board.
C142 C120 C121
*10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8
C158 C153 C152 C151 C567 C564
*10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8
C563 C574 C570 C569 C554 C555
10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8 10U/6.3V_8 *10U/6.3V_8
10/12 :Modify BOM
C80 C576 C81 C577
*330U/2V_7343 330U/2V_7343 330U/2V_7343 *330U/2V_7343
U40C
VCC[001] VCC[002] VCC[003] VCC[004] VCC[005] VCC[006] VCC[007] VCC[008] VCC[009] VCC[010] VCC[011] VCC[012] VCC[013] VCC[014] VCC[015] VCC[016] VCC[017] VCC[018] VCC[019] VCC[020] VCC[021] VCC[022] VCC[023] VCC[024] VCC[025] VCC[026] VCC[027] VCC[028] VCC[029] VCC[030] VCC[031] VCC[032] VCC[033] VCC[034] VCC[035] VCC[036] VCC[037] VCC[038] VCC[039] VCC[040] VCC[041] VCC[042] VCC[043] VCC[044] VCC[045] VCC[046] VCC[047] VCC[048] VCC[049] VCC[050] VCC[051] VCC[052] VCC[053] VCC[054] VCC[055] VCC[056] VCC[057] VCC[058] VCC[059] VCC[060] VCC[061] VCC[062] VCC[063] VCC[064] VCC[065] VCC[066] VCC[067] VCC[068] VCC[069] VCC[070] VCC[071] VCC[072] VCC[073] VCC[074] VCC[075] VCC[076] VCC[077] VCC[078] VCC[079] VCC[080] VCC[081] VCC[082] VCC[083] VCC[084] VCC[085] VCC[086] VCC[087] VCC[088] VCC[089] VCC[090] VCC[091] VCC[092] VCC[093] VCC[094] VCC[095] VCC[096] VCC[097] VCC[098] VCC[099] VCC[100]
VCCP[01] VCCP[02] VCCP[03] VCCP[04] VCCP[05] VCCP[06] VCCP[07] VCCP[08] VCCP[09] VCCP[10] VCCP[11] VCCP[12] VCCP[13] VCCP[14] VCCP[15] VCCP[16]
VCCA[01] VCCA[02]
VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]
VCCSENSE
VSSSENSE
Penryn
VCC_CORE
VCC:38A
VCCP:130mA
Layout Note:
Inside CPU center cavity in 2 rows
C129 C135 C147
.1U/16V_6 .1U/16V_6 .1U/16V_6
C128 C136 C148
.1U/16V_6 .1U/16V_6 .1U/16V_6
+1.05V
C575
330U/2V_7
Layout Note:
VCCA CAP closr to Pin
VCCA : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
+1.5V
C562 C561
.01U/16V_4 10U/6.3V_8
H_VID0 <35>
H_VID1 <35>
H_VID2 <35>
H_VID3 <35>
H_VID4 <35>
H_VID5 <35>
H_VID6 <35>
R84 100/F_6 VCC_CORE
VCCSENSE <35>
VSSSENSE <35>
R77 100/F_6
Layout Note:
Z0=27.4,PU/PD L<1"
VCCA : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
CPU Power
Rev
1A
Date: Thursday, August 28, 2008
Sheet 4 of 40

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06









Quanta Computer Inc.

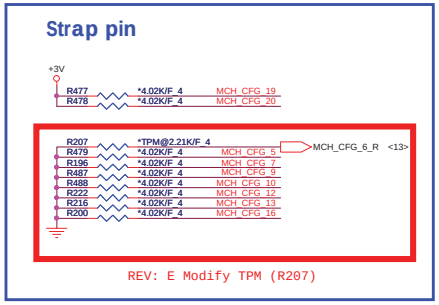
PROJECT : ZY2 & ZY6

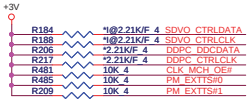
Size	Document Number	Rev
	GMCH HOST	1A
Date: Thursday, August 28, 2008	Sheet 5 of 40	

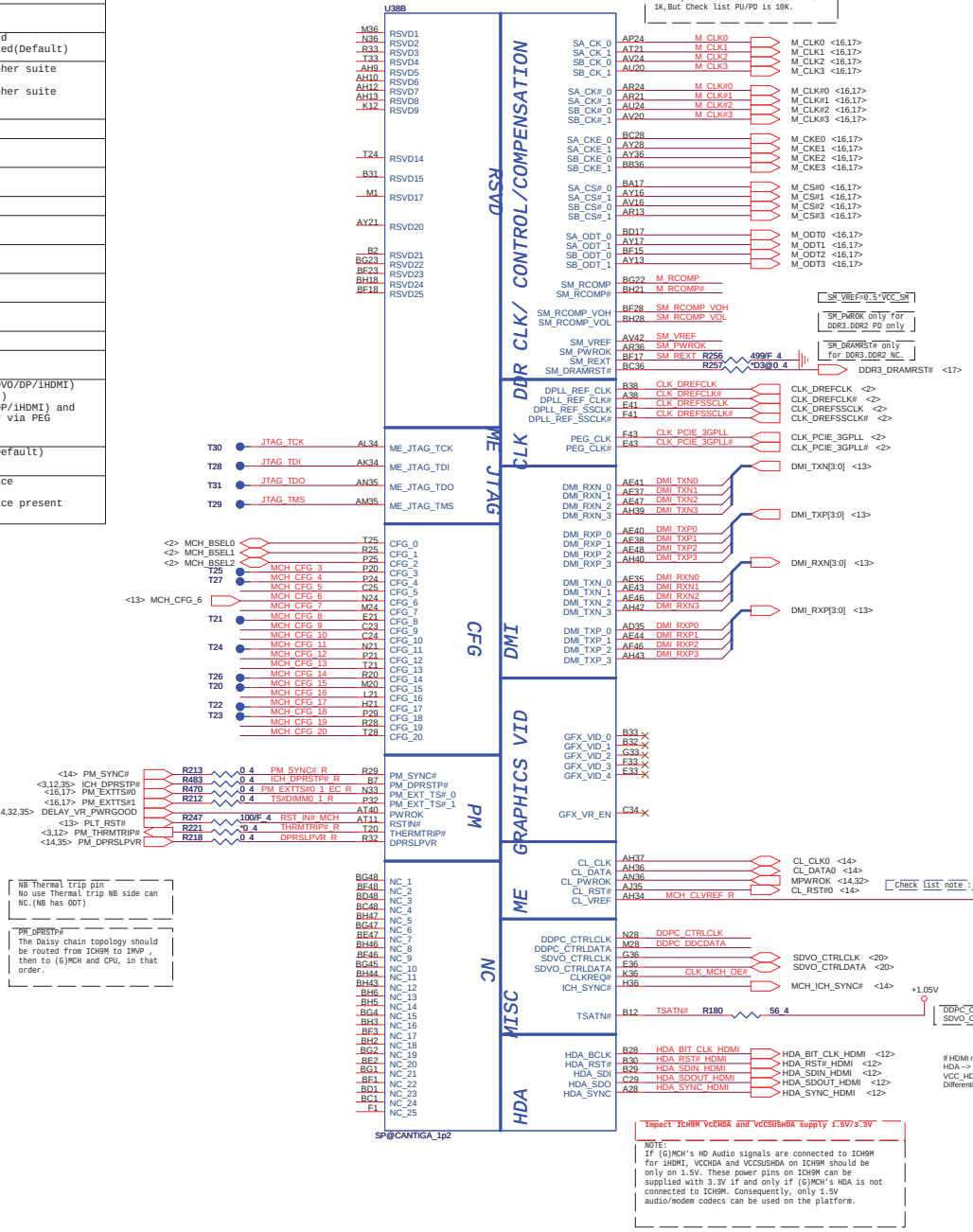
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

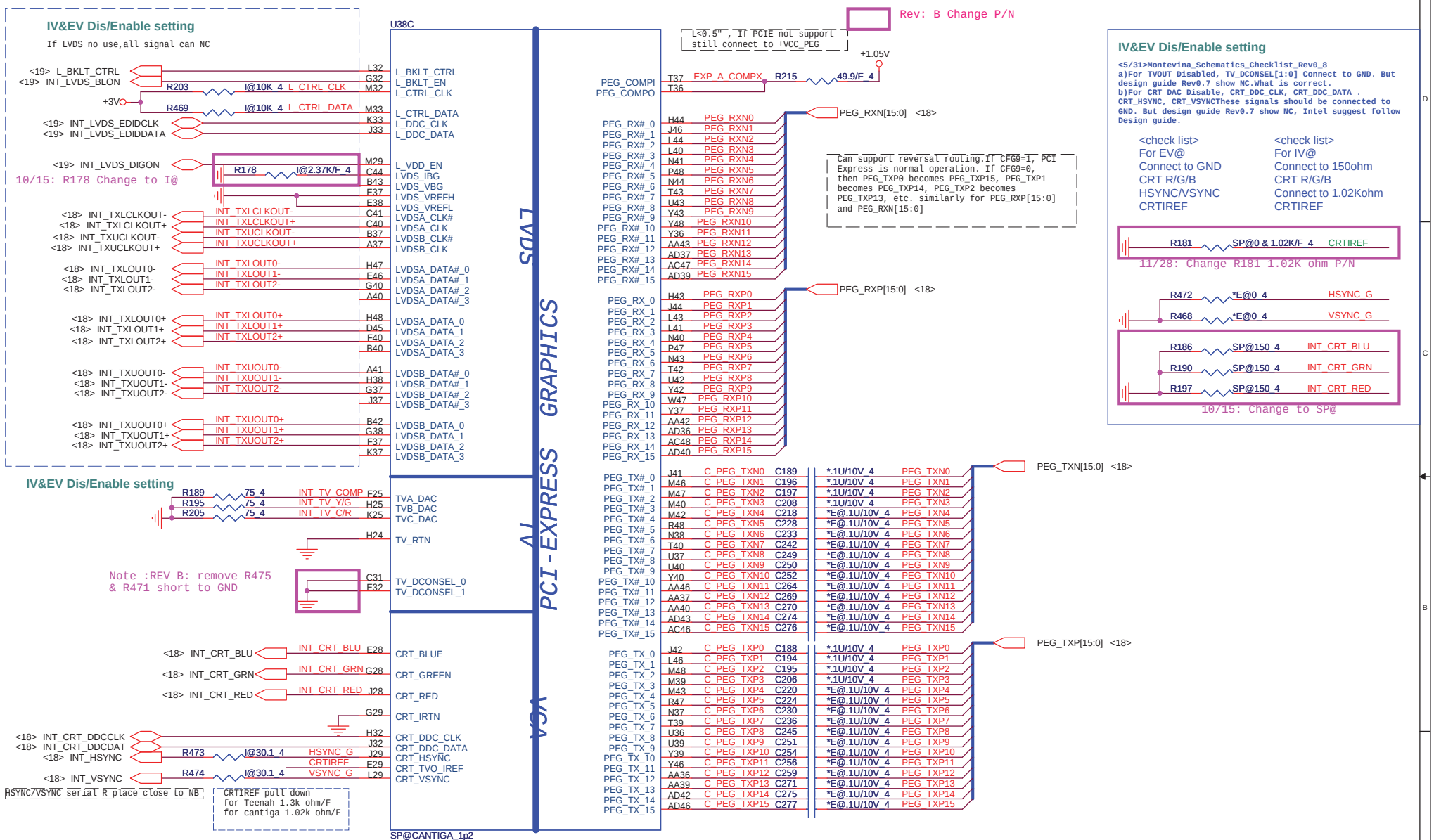
Strap pin

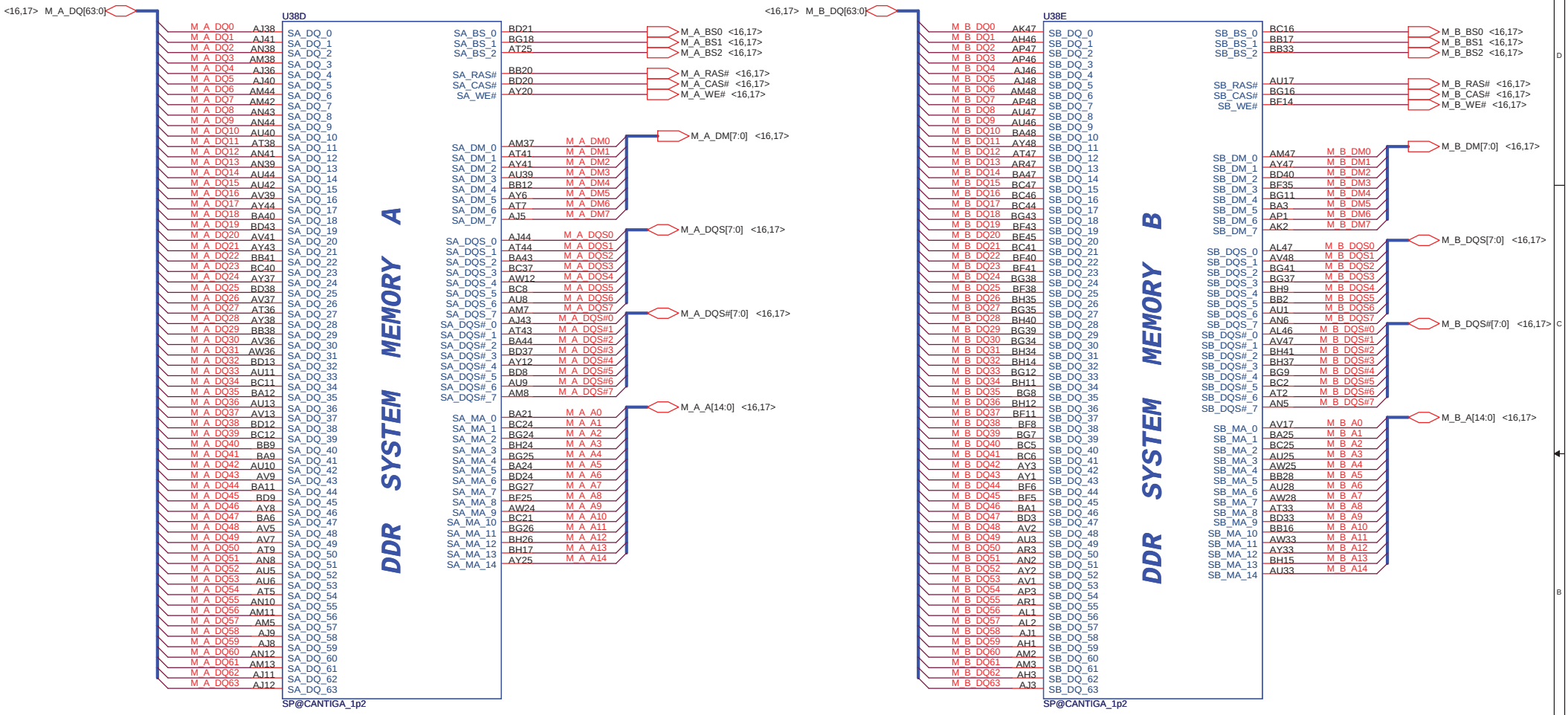






Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size | Document Number: GMCH DMI | Rev: 1A
Date: Thursday, August 28, 2008 | Sheet 6 of 40


IV&EV Dis/Enable setting
If LVDS no use,all signal can NC
U38C
Rev: B Change P/N
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3
LVDS
TVA_DAC
TVB_DAC
TVC_DAC
TV_RTN
TV_DCONSEL_0
TV_DCONSEL_1
TV
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
VGA
PCI-EXPRESS GRAPHICS
SP@CANTIGA_1p2
PEG_COMPI
PEG_COMPO
EXP_A_COMPX
R215
49.9/F_4
+1.05V
L<0.5" , If PCIE not support still connect to +VCC_PEG
PEG_RXN[15:0] <18>
PEG_RXP[15:0] <18>
PEG_TXN[15:0] <18>
PEG_TXP[15:0] <18>
Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]
IV&EV Dis/Enable setting
<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.
<check list> For EV@ Connect to GND CRT R/G/B HSYNC/VSYNC CRTIREF
<check list> For IV@ Connect to 150ohm CRT R/G/B Connect to 1.02Kohm CRTIREF
R181 SP@0 & 1.02K/F_4 CRTIREF
11/28: Change R181 1.02K ohm P/N
R472 *E@0_4 HSYNC_G
R468 *E@0_4 VSYNC_G
R186 SP@150_4 INT_CRT_BLU
R190 SP@150_4 INT_CRT_GRN
R197 SP@150_4 INT_CRT_RED
10/15: Change to SP@
10/15: R178 Change to I@
Note :REV B: remove R475 & R471 short to GND
HSYNC/VSYNC serial R place close to NB
CRTIREF pull down for Teenah 1.3k ohm/F for cantiga 1.02k ohm/F
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
GMCH VGA
Rev 1A
Date: Thursday, August 28, 2008
Sheet 7 of 40



Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: GMCH DDRII	Rev: 1A
Date: Thursday, August 28, 2008	Sheet 8 of 40	

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

+VDR_SUS
C519 22U/6V_8
C521 22U/6V_8
C244 0.1U/10V_4
C518 330U/2V_7
Place on the edga

U38G
VCC_SM_1 … VCC_SM_42/NC
VCC SM POWER

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

+1.05V_AXG
VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60
VCC GFX NCTF

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCA_HPLL, VCA_MPLL, VCCA_PEG_PLLVCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

VCC_AXG_1 … VCC_AXG_42
VCC GFX

+1.05V_AXG
R242 I@10/F_4
R238 I@10/F_4
VCC_AXG_SENSE
VSS_AXG_SENSE

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

SP@CANTIGA_1p2

1.8V
Internal connect to power

VCC_SM_LF1 … VCC_SM_LF7
VCC SM LF

C268 1U/10V_4
C239 .1U/10V_4
C255 .22U/6V_4
C253 .22U/6V_4
C238 .47U/6V_4
C266 1U/6V_4
C258 1U/6V_4

+1.05V
C231 1U/10V_4
C225 .22U/6V_4
C226 .22U/6V_4
C210 22U/6V_8
C524 330U/2V_7
Place close to the GMCH

U38F
VCC_1 … VCC_35
VCC CORE POWER

+1.05V
+1.05V_AXG
R227 I@0_8
R228 I@0_8

IV&EV Dis/Enable setting
SP@:INT 1 U
EXT 0 ohm
Design guide(Table 72)
For INT VGA disable.VCC_AXG power can connect to GND

+1.05V_AXG
C191 I@330U/2.5V_7343
C192 I@330U/2.5V_7343
C200 I@.47U/6V_4
C237 SP@0_6
C217 I@10U/10V_8
C201 I@22U/6V_8
C247 I@.1U/10V_4
C203 I@.1U/10V_4
Place close to the GMCH
Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

+1.05V
VCC_NCTF_1 … VCC_NCTF_44
VCC NCTF

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A
Date: Thursday, August 28, 2008	Sheet 9 of 40	

Power consumption reference to Intel 644135 Cantiga chipset EDS Volume1. Section 10

IV&EV Dis/Enable setting Design guide Table 72

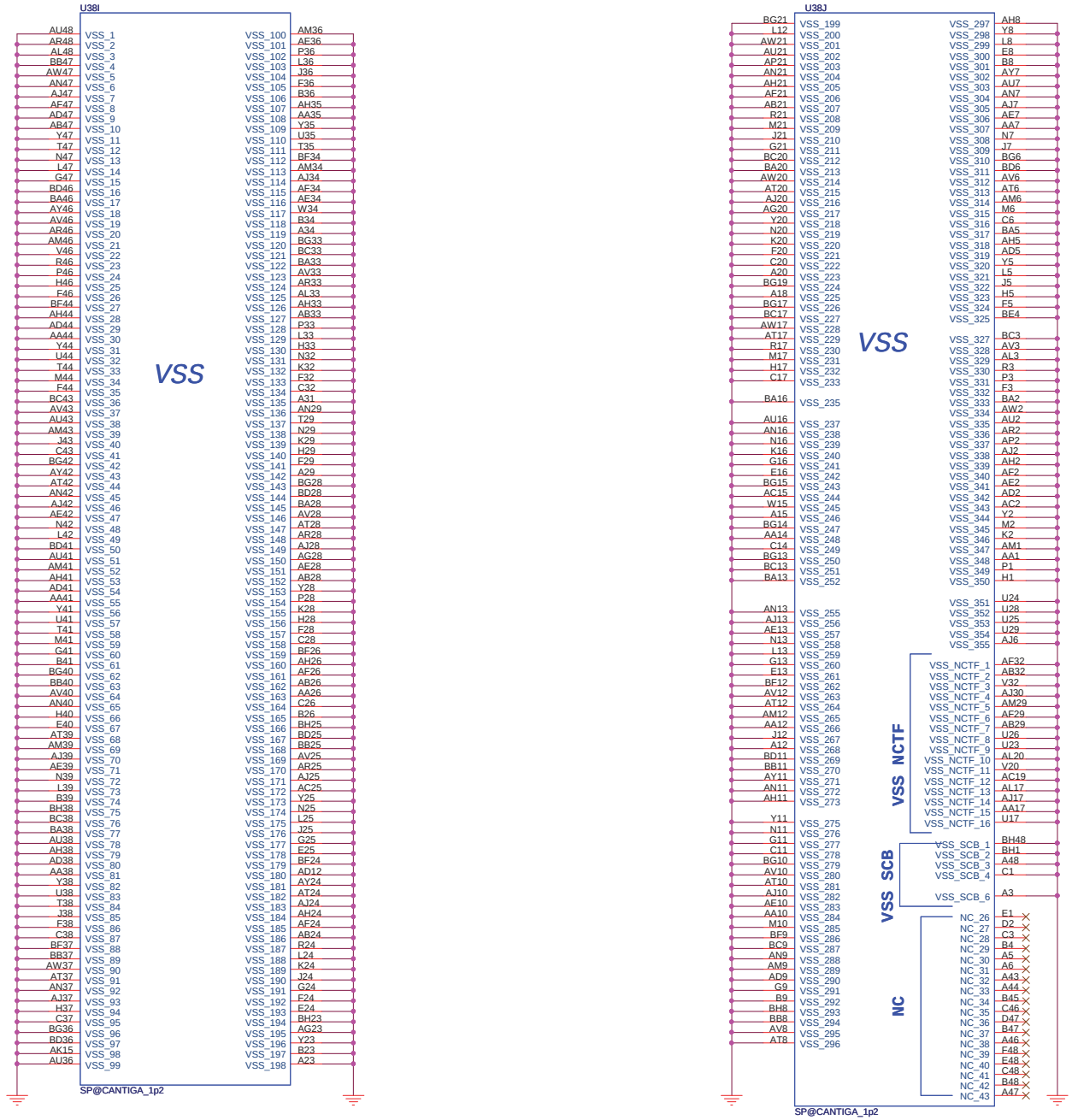
External Graphics (GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

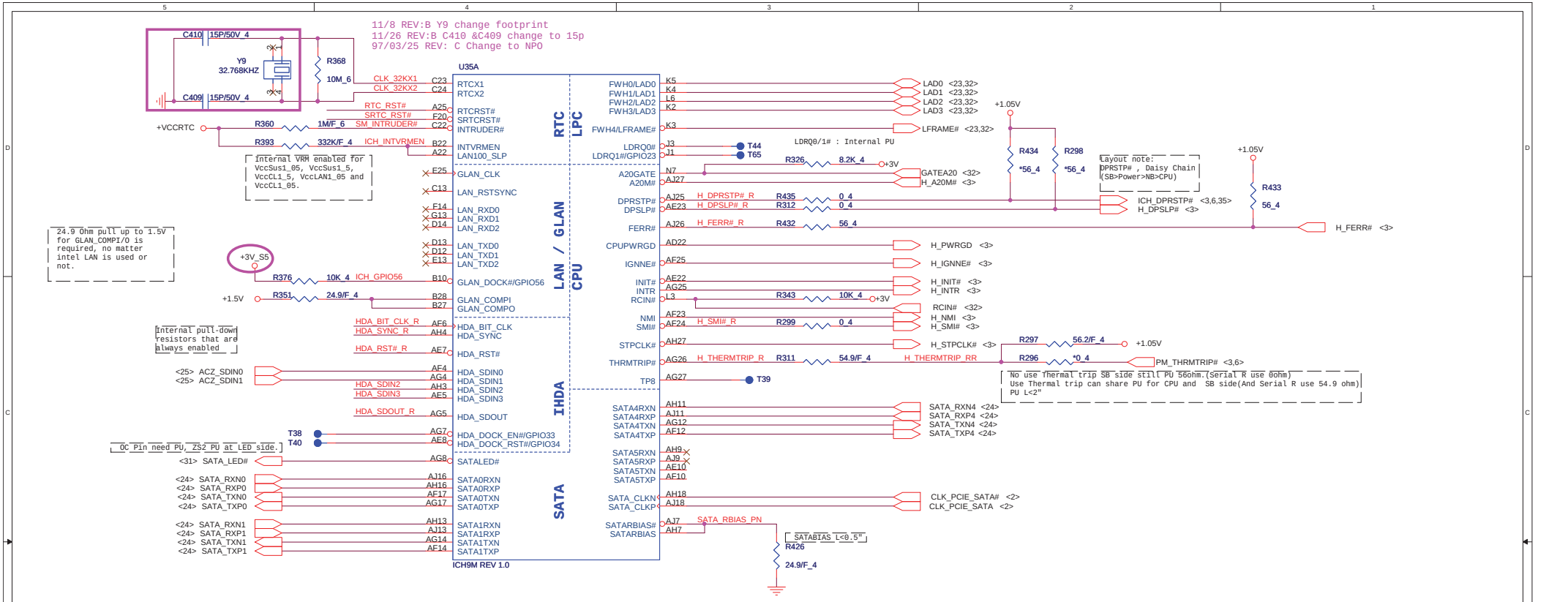
Power Rail Differences between the Teenah and Cantiga Chipset Family

Power Net Name	Cantiga(V)	Tennah(V)	Tennah Current
VCC_AXG_# VCC_AXG_NCTF_#	1.05V	1.25V	6326.84mA Cantiga use
VCCA_PEG_BG	1.5V	3.3V	400uA
VCCA_DPLLA	1.05V	1.25V	100mA
VCCA_DPLLB	1.05V	1.25V	100mA
VCCA_SM_#	1.05V	1.25V	1065mA
VCCA_HPLL	1.05V	1.25V	50mA
VCCA_MPLL	1.05V	1.25V	150mA
VCCA_SM_CK_#	1.05V	1.25V	35mA
VCCA_PEG_PLL	1.05V	1.25V	100mA
VCC_AXF_#	1.05V	1.25V	495mA
VCCD_HPLL	1.05V	1.25V	250mA
VCCD_PEG_PLL	1.05V	1.25V	100mA

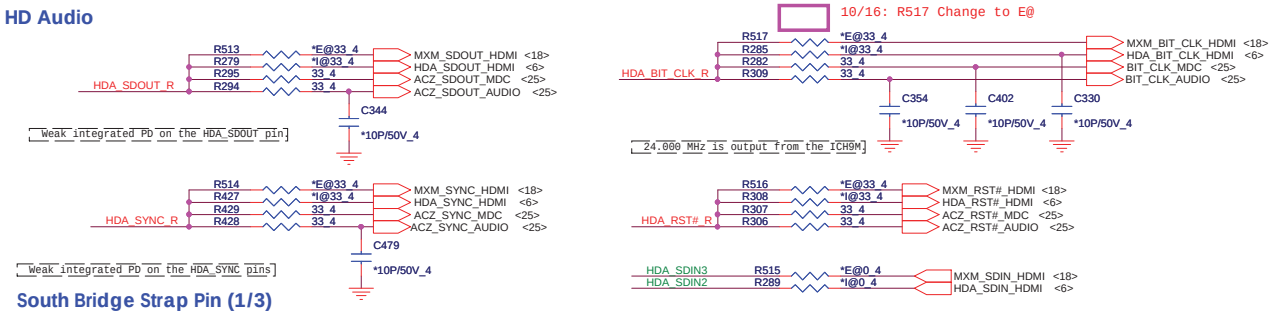
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size: Document Number: GMCH POWER Rev: 1A
Date: Thursday, August 28, 2008 Sheet 10 of 40



Quanta Computer Inc.			
PROJECT : ZY2 & ZY6			
Size	Document Number		Rev
	GMCH VSS		1A
Date: Thursday, August 28, 2008		Sheet 11 of 40	



HD Audio

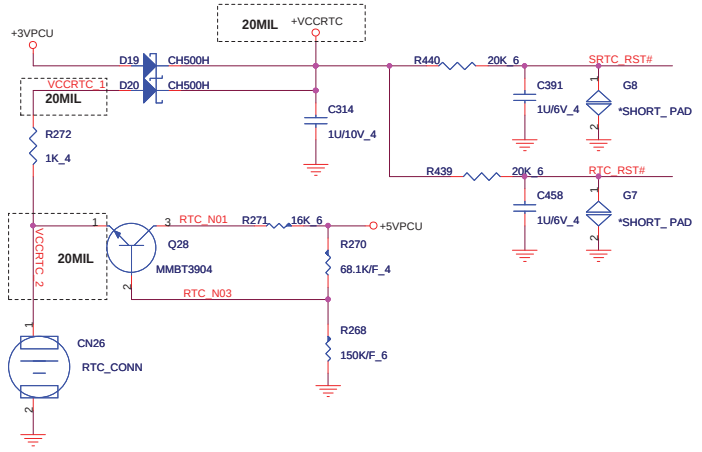


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	<14> ICH_TP3 — ICH_TP3 — R406 *1K_4	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	HDA_SDOUT_R — R310 *1K_4 — +3V	

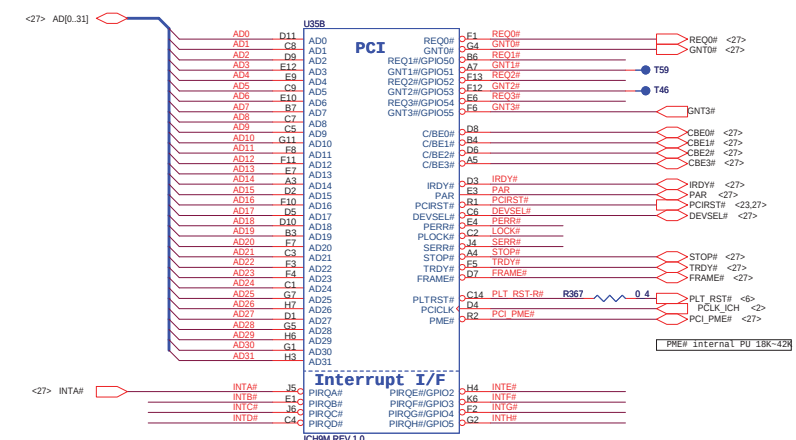
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

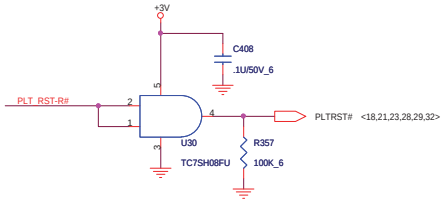
RTC

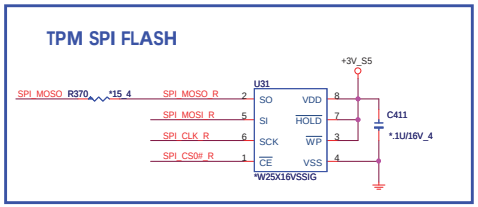


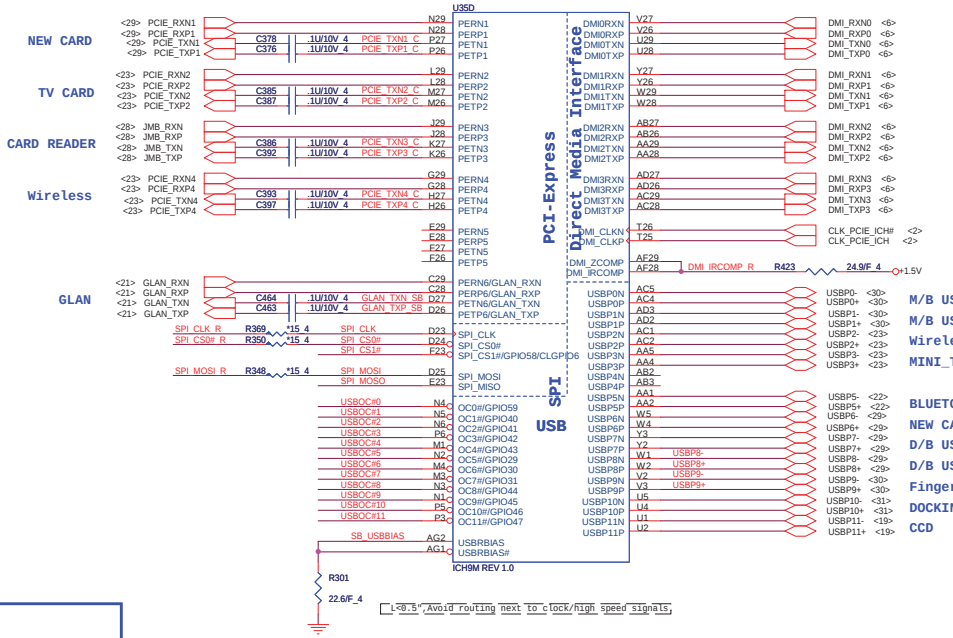
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M HOST	1A
Date: Thursday, August 28, 2008	Sheet 12 of 40	



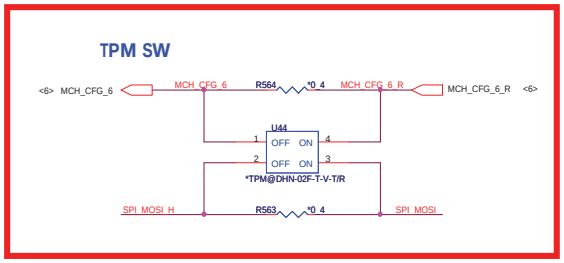


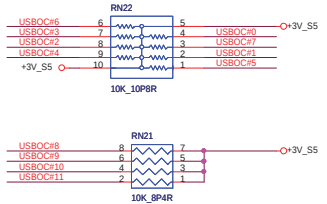


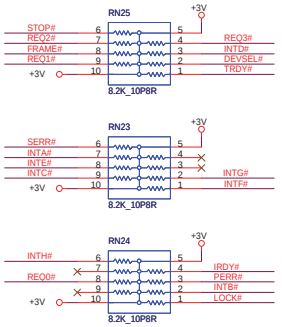


TM & AS	Y
LOW COST	N

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T





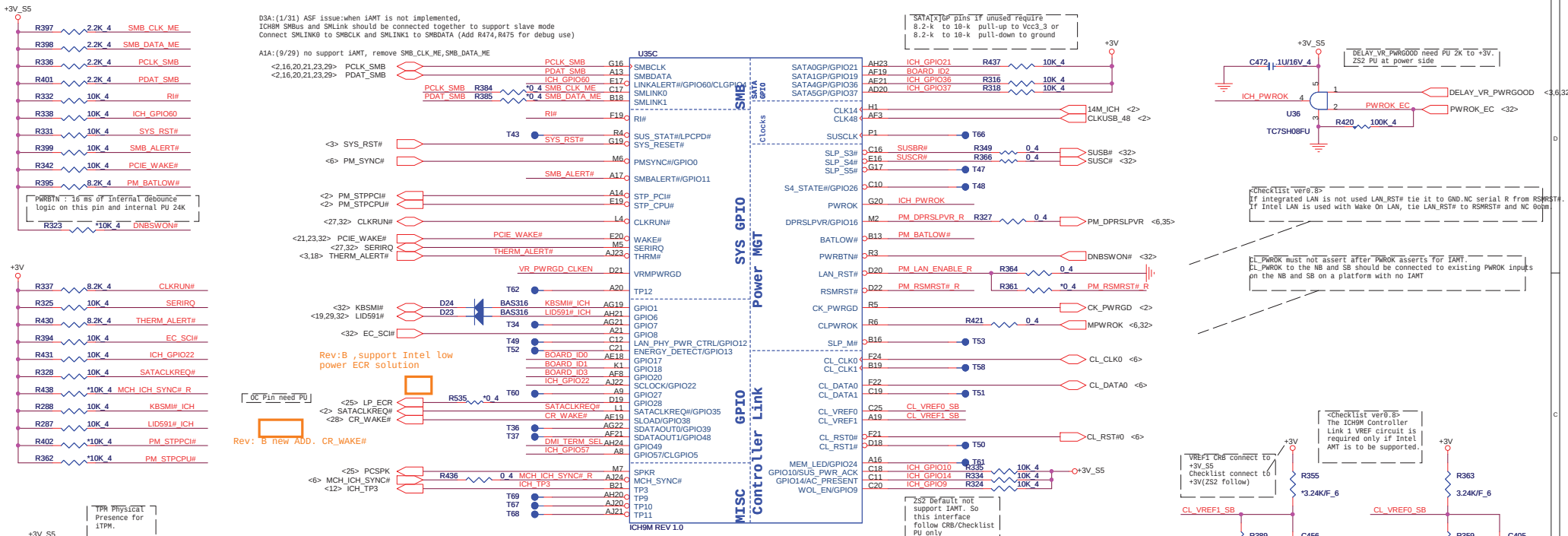


South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R347 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_H R329 *TPM@10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default)	GNT0# R344 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / LPC	SPI_CS1# R340 *1K_4

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A
Date: Thursday, August 28, 2008	Sheet 13 of 40	



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R346 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R400 *1K_4

Board ID	ID3	ID2	ID1	ID0
ZY2	0	0	0	0
ZY6	0	0	1	0
ZY2 LOW COST	0	0	0	1
ZY6 LOW COST	0	0	1	1
ZY2 eMachine	0	1	0	0
ZY6 eMachine	0	1	1	0

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M GPIO	1A

Date: Thursday, August 28, 2008 Sheet 14 of 40

Power consumption reference to Intel
642879_ICH9_Family_EDS_Rev_1.5

2~3.456v
3.6uA_G3

5V
2mA

5V
2mA_S0
1mA_S3/S4/S5

1.5V
646mA

1.5V
47mA

VCC1_5_A
1.5V
1342mA

1.5V
11mA

1.05V , Powered by VCC1_05 in S0

3.3V
19mA_S0 ,
78mA_S3/S4/S5

1.5V
23mA

1.5V
80mA

3.3V
1mA

1.05V
1634mA

1.5V
23mA

1.05V
50mA

VCCP
2mA

VCC3_3
3.3V
308mA

1.5V / 3.3V
11mA

1.5V / 3.3V
11mA_S0 , 1mA_S3/S4/S5

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

3.3V
212mA_S0 , 53mA_S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

3.3V
19mA_S0 , 73mA_S3/S4/S5

If use SB MAC for LAN function. And support wake up need connect to relation power.

ZS2 Default not support INT HDMI interface

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

Check list:
0.1U for Pin AF1

Checklist stuff 22U,but CRB no

330 Ohms@ 100 MHz , 0805

5 Ohms @ 100 MHz , 0.7A

500 mA, 20%

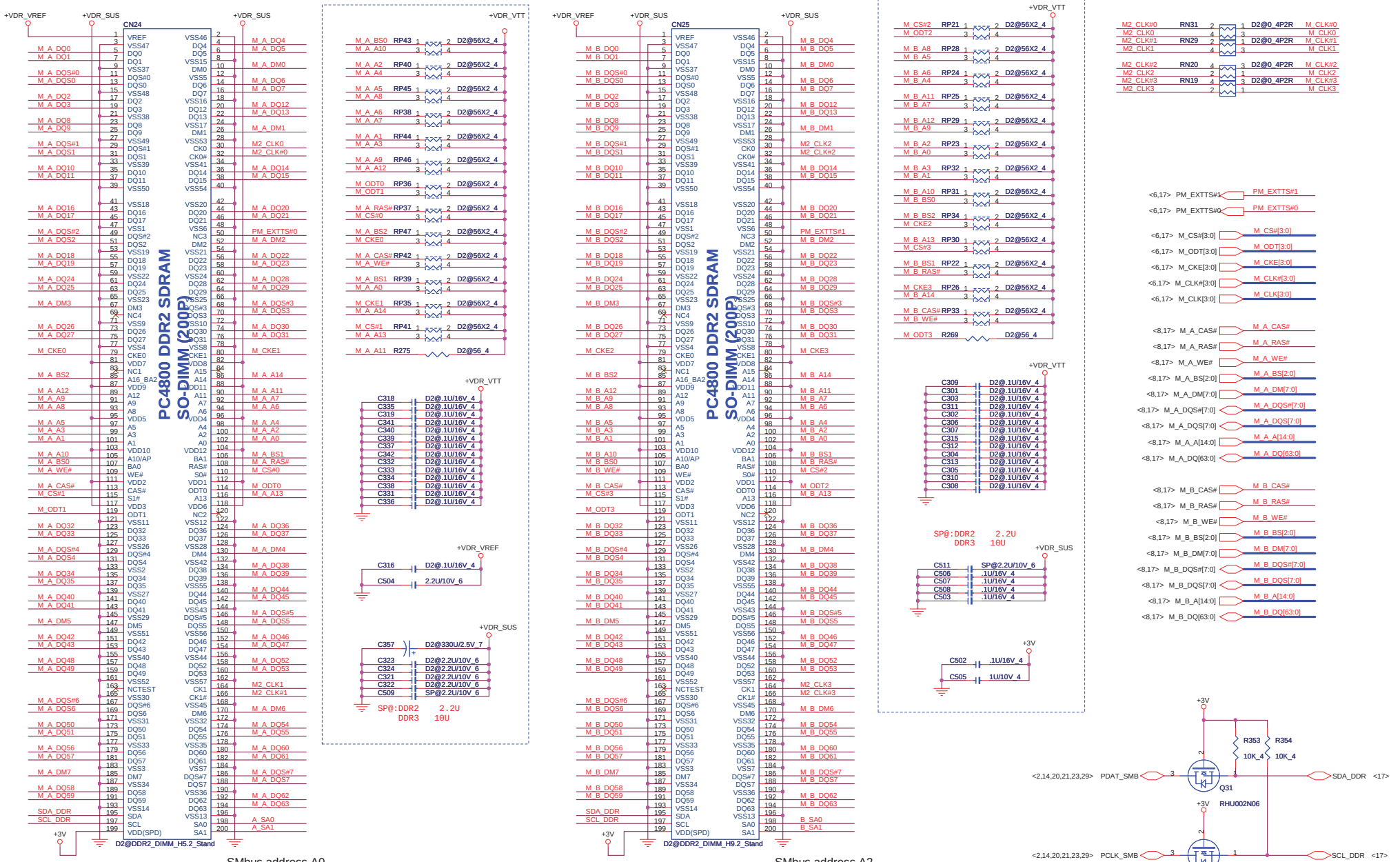
U35F
ICH9M REV 1.0

U35E
ICH9M REV 1.0

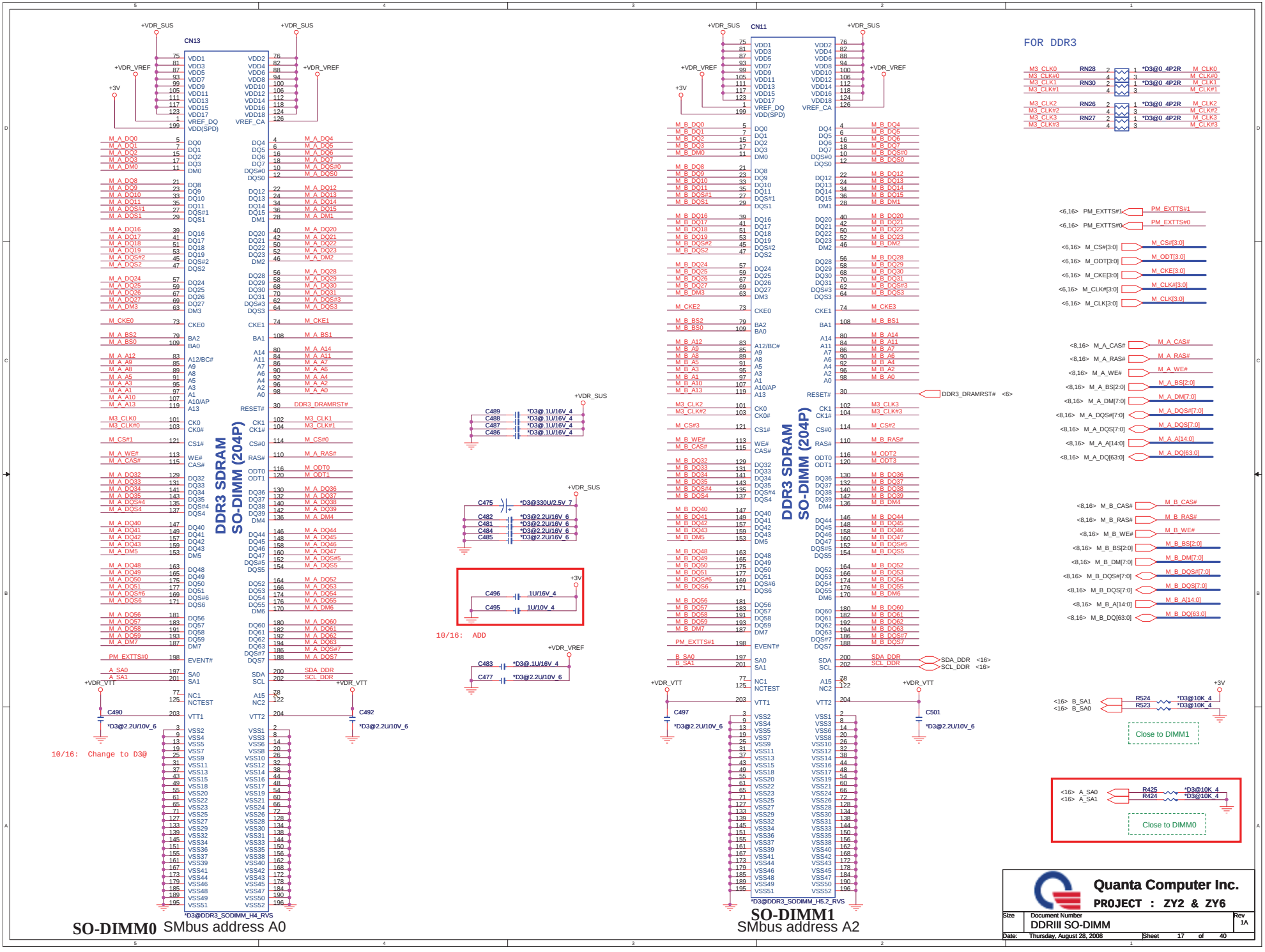
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

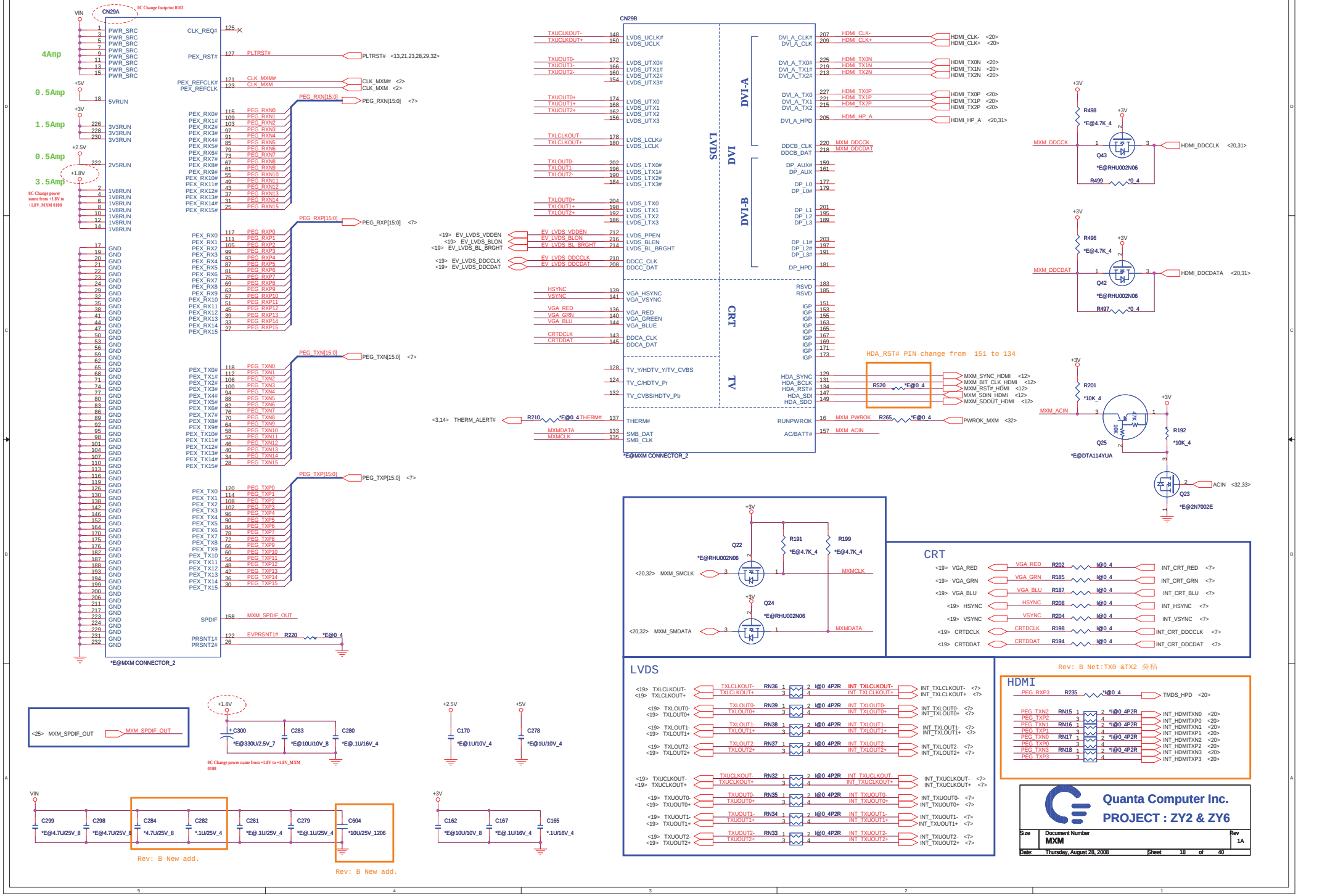
Size	Document Number	Rev
	ICH9 POWER	1A

Date: Thursday, August 28, 2008 Sheet 15 of 40



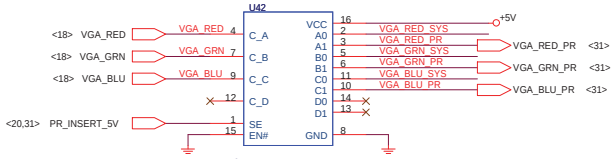
Quanta Computer Inc.			
PROJECT : ZY2 & ZY6			
Size	Document Number		Rev
	DDRII SO-DIMM		1A
Date: Thursday, August 28, 2008		Sheet 16 of 40	

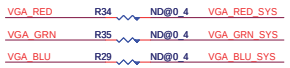

CN13
DDR3 SDRAM SO-DIMM (204P)
+VDR_SUS
+VDR_VREF
+3V
+VDR_VTT
*D3@DDR3_SODIMM_H4_RVS
C490
*D3@2.2U/10V_6
C492
*D3@2.2U/10V_6
10/16: Change to D3@
C489
C488
C487
C486
*D3@.1U/16V_4
C475
*D3@330U/2.5V_7
C482
C481
C484
C485
*D3@2.2U/16V_6
C496
C495
.1U/16V_4
10/16: ADD
C483
C477
*D3@2.2U/16V_6
CN11
DDR3 SDRAM SO-DIMM (204P)
DDR3_DRAMRST# <6>
SDA_DDR <16>
SCL_DDR <16>
C497
C501
*D3@DDR3_SODIMM_H5.2_RVS
FOR DDR3
M3_CLK0
M3_CLK#0
M3_CLK1
M3_CLK#1
RN28
RN30
*D3@0_4P2R
M_CLK0
M_CLK#0
M_CLK1
M_CLK#1
M3_CLK2
M3_CLK#2
M3_CLK3
M3_CLK#3
RN26
RN27
M_CLK2
M_CLK#2
M_CLK3
M_CLK#3
<6,16> PM_EXTTS#1
<6,16> PM_EXTTS#0
PM_EXTTS#1
PM_EXTTS#0
<6,16> M_CS#[3:0]
<6,16> M_ODT[3:0]
<6,16> M_CKE[3:0]
<6,16> M_CLK#[3:0]
<6,16> M_CLK[3:0]
M_CS#[3:0]
M_ODT[3:0]
M_CKE[3:0]
M_CLK#[3:0]
M_CLK[3:0]
<8,16> M_A_CAS#
<8,16> M_A_RAS#
<8,16> M_A_WE#
<8,16> M_A_BS[2:0]
<8,16> M_A_DM[7:0]
<8,16> M_A_DQS#[7:0]
<8,16> M_A_DQS[7:0]
<8,16> M_A_A[14:0]
<8,16> M_A_DQ[63:0]
M_A_CAS#
M_A_RAS#
M_A_WE#
M_A_BS[2:0]
M_A_DM[7:0]
M_A_DQS#[7:0]
M_A_DQS[7:0]
M_A_A[14:0]
M_A_DQ[63:0]
<8,16> M_B_CAS#
<8,16> M_B_RAS#
<8,16> M_B_WE#
<8,16> M_B_BS[2:0]
<8,16> M_B_DM[7:0]
<8,16> M_B_DQS#[7:0]
<8,16> M_B_DQS[7:0]
<8,16> M_B_A[14:0]
<8,16> M_B_DQ[63:0]
M_B_CAS#
M_B_RAS#
M_B_WE#
M_B_BS[2:0]
M_B_DM[7:0]
M_B_DQS#[7:0]
M_B_DQS[7:0]
M_B_A[14:0]
M_B_DQ[63:0]
<16> B_SA1
<16> B_SA0
R524
R523
*D3@10K_4
Close to DIMM1
<16> A_SA0
<16> A_SA1
R425
R424
Close to DIMM0
SO-DIMM0 SMbus address A0
SO-DIMM1 SMbus address A2
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
DDRIII SO-DIMM
Rev 1A
Date: Thursday, August 28, 2008
Sheet 17 of 40


CN29A
0C Change footprint 0103
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
0C Change power name from +1.8V to +1.8V_MXM 0108
*E@MXM CONNECTOR_2
CN29B
*E@MXM CONNECTOR_2
LVDS
DVI
DVI-A
DVI-B
CRT
TV
HDA_RST# PIN change from 151 to 134
CRT
LVDS
HDMI
Rev: B Net:TX0 &TX2 交結
0C Change power name from +1.8V to +1.8V_MXM 0108
Rev: B New add.
Rev: B New add.
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
MXM
Rev
1A
Date: Thursday, August 28, 2008
Sheet 18 of 40

CRT Select

CRT SWITCH

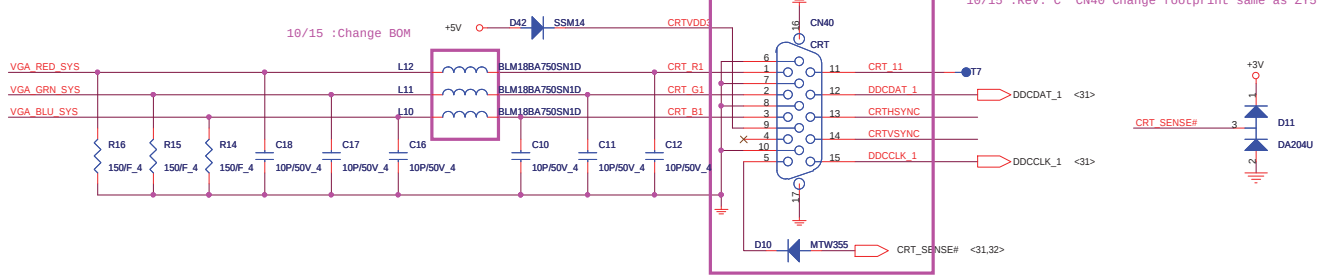


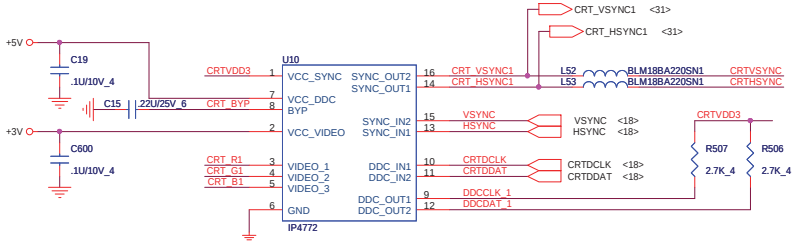


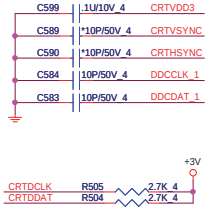
CRT CONNECTOR AND ESD

10/15 :Change BOM

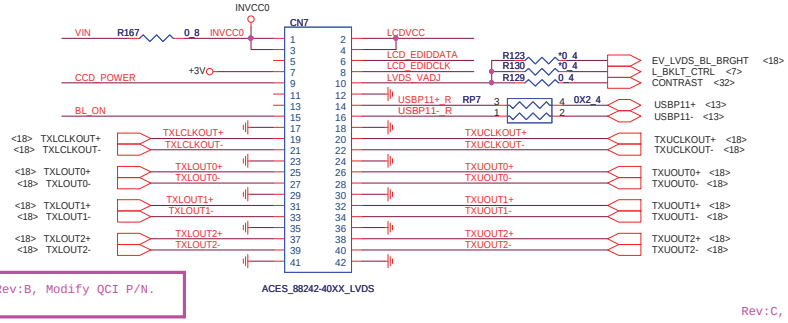
10/15 :Rev: C CN40 Change footprint same as ZY5



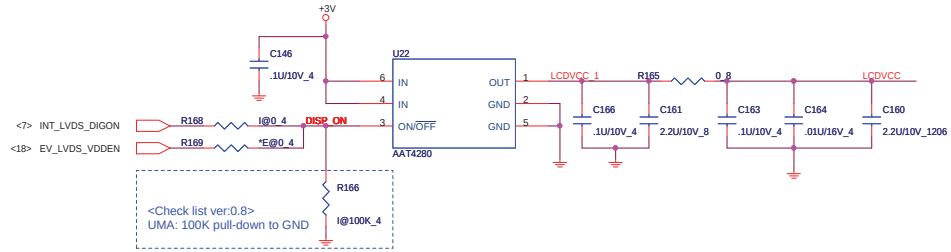




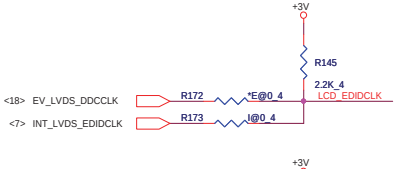
LVDS

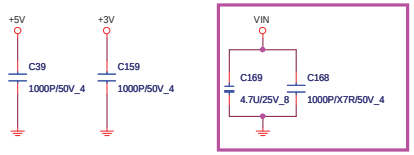


Rev:B, Modify QCI P/N.

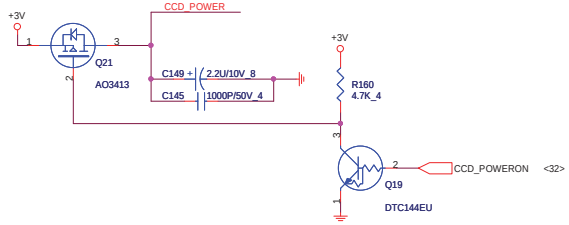


Rev:C, Change to 4.7U 0805

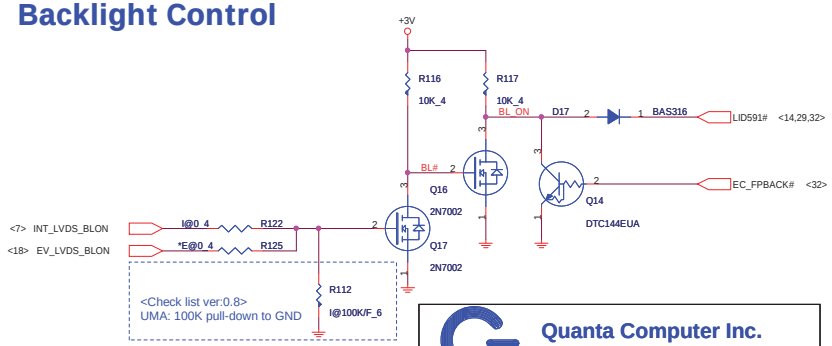




CAMERA MODULE CONNECTOR



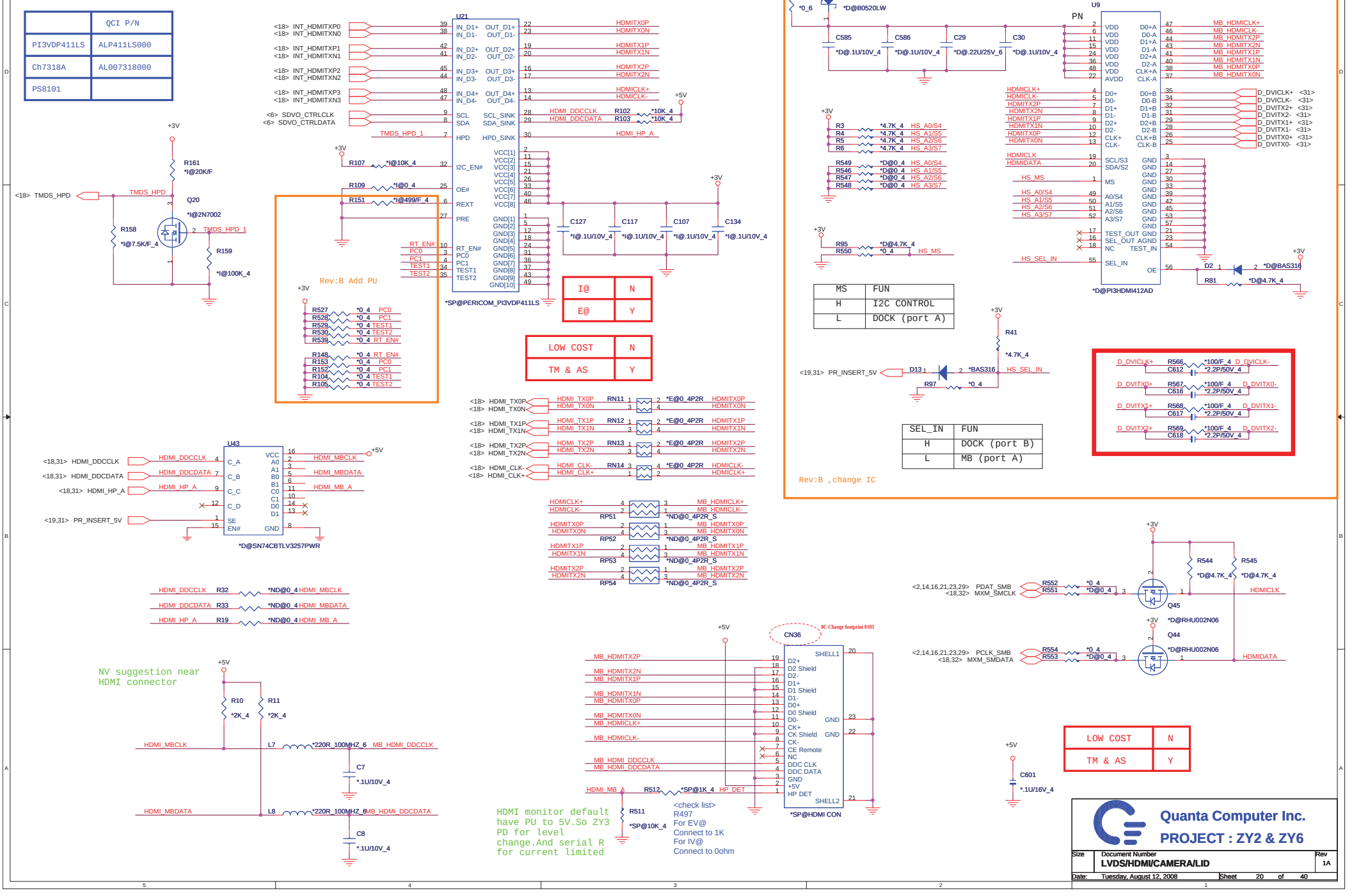
Backlight Control



Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: CRT	Rev: 1A
Date: Thursday, August 28, 2008	Sheet 19 of 40	

DVI-I CONNECTOR (DVI-D)

	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



I@	N
E@	Y

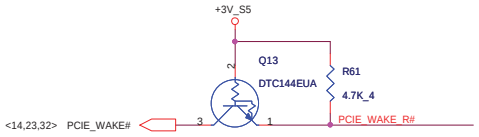
LOW COST	N
TM & AS	Y

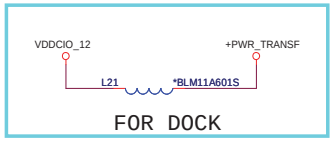
MS	FUN
H	I2C CONTROL
L	DOCK (port A)

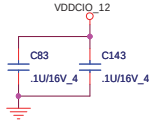
SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)

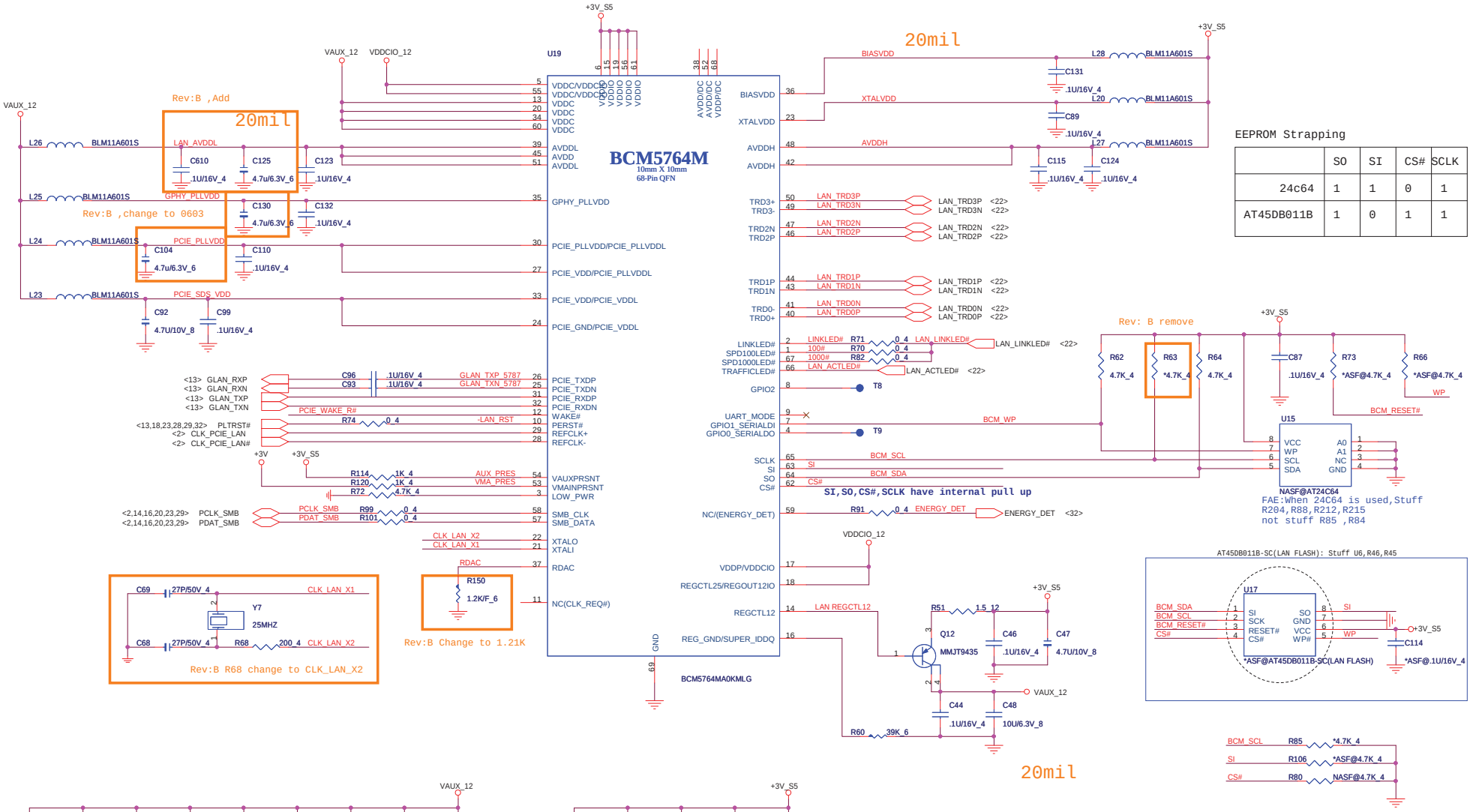
LOW COST	N
TM & AS	Y

LAN



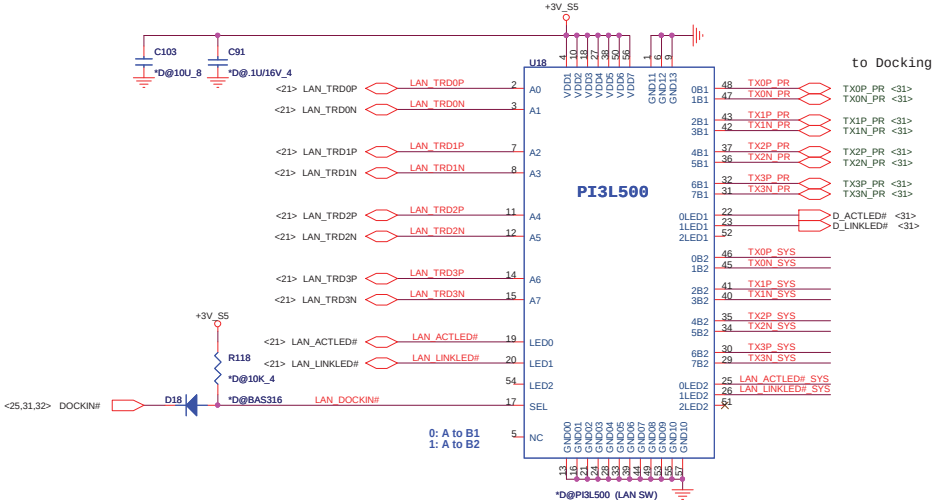


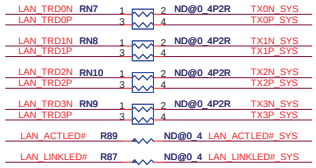




Quanta Computer Inc.			
PROJECT : ZY2 & ZY6			
Size	Document Number		Rev
	BCM5787 & 5764 LAN		1A
Date: Thursday, August 28, 2008		Sheet 21 of 40	

LAN SWITCH

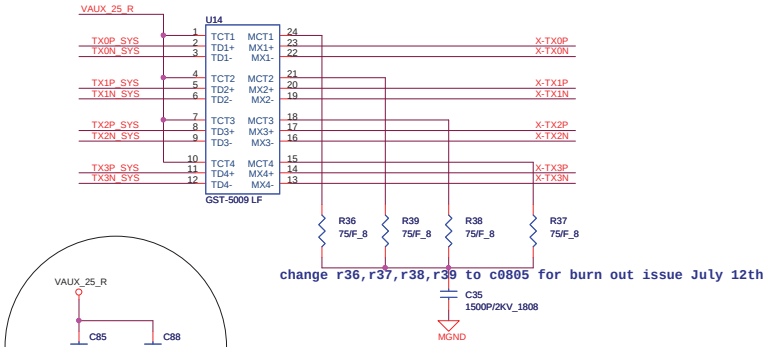


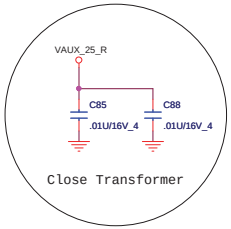


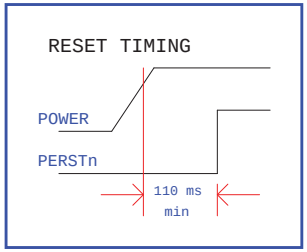
Transfomer

Source 1: DELTA LFE9249 DB0ZR1LAN11

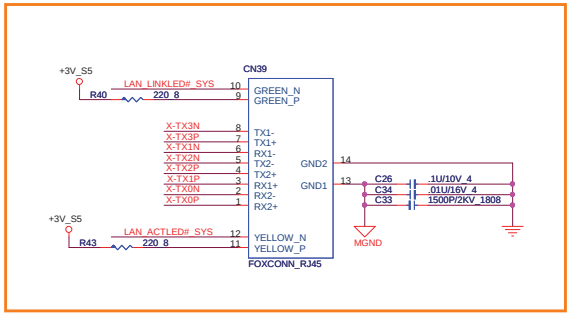
Source 2: Bothand GST5009 DBKN1NLAN03





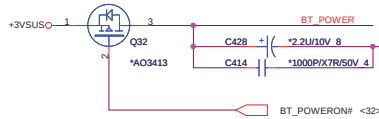


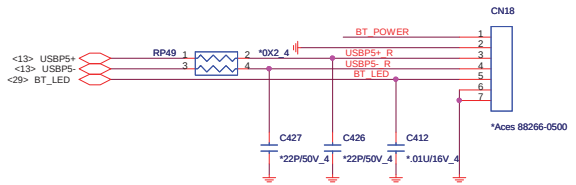
RJ45-11



9/29: change footprint
11/27 :change footprint
11/28 : R43 & R40 Change to 0805
1/31 :Rev: C change PIN define about 9,10,11 & 12

BLUETOOTH MODULE CONNECTOR





Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	1A
Date: Thursday, August 28, 2008	Sheet 22 of 40	

MINI-CARD

MODULE 'A' TV card

MODULE 'B' Wireless card

Double Stack MINI CARD

Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538

MODULE 'A' MODULE 'B'

CN27

+3V R542 *0_8 +3V_MINI_A — +3V_MINI_B R543 0_8 +3V

A_+3.3V / A_+3.3Vaux / A_+3.3V — B_+3.3V / B_+3.3Vaux / B_+3.3V

RF_LED# R536 *0_4 RF_LED# A — RF_LED# B R447 0_4 RF_LED# → RF_LED# <29>

A_LED_WPAN# / A_LED_WLAN# / A_LED_WWAN# — B_LED_WPAN# / B_LED_WLAN# / B_LED_WWAN#

<13> USBP2+ / <13> USBP2- — USBP2+ RP27 3 4 *0X2_4 2 1 — USBP2+_C / USBP2-_C — A_USB_D+ / A_USB_D- — B_USB_D+ / B_USB_D- — USBP3+_C RP57 2 1 0X2_4 3 4 USBP3-_C — USBP3+ <13> / USBP3- <13>

MINI_SMDATA / MINI_SMCLK — A_SMB_DATA / A_SMB_CLK — B_SMB_DATA / B_SMB_CLK — MINI_SMDATA / MINI_SMCLK

<13> PCIE_TXP2 / <13> PCIE_TXN2 / <13> PCIE_RXP2 / <13> PCIE_RXN2 — PCIE_TXP2 / PCIE_TXN2 / PCIE_RXP2 / PCIE_RXN2 — A_PETp0 / A_PETn0 / A_PERp0 / A_PERn0 — B_PETp0 / B_PETn0 / B_PERp0 / B_PERn0 → PCIE_TXP4 <13> / PCIE_TXN4 <13> / PCIE_RXP4 <13> / PCIE_RXN4 <13>

PLTRST# — A_PERST# — B_PERST# → PLTRST# <13,18,21,28,29,32>

<2> CLK_PCIE_TV / <2> CLK_PCIE_TV# — CLK_PCIE_TV / CLK_PCIE_TV# — A_REFCLK+ / A_REFCLK- — B_REFCLK+ / B_REFCLK- → CLK_PCIE_MINI1 <2> / CLK_PCIE_MINI1# <2>

PCIE_WAKE# R R538 *0_4 PCIE_WAKE# R_A — A_CLKREQ# / A_WAKE# — B_CLKREQ# / B_WAKE# — PCIE_WAKE# R_B R537 *0_4 PCIE_WAKE# R

+1.5V — A_+1.5V ×3 — B_+1.5V ×3 — +1.5V

<12,32> LFRAME# — R445 *0_4 — A_LFRAME# R — B_LFRAME# R — R561 0_4 — LFRAME#
<12,32> LAD3 — R444 *0_4 — A_LAD3 R — B_LAD3 R — R559 0_4 — LAD3
<12,32> LAD2 — R443 *0_4 — A_LAD2 R — B_LAD2 R — R558 0_4 — LAD2
<12,32> LAD1 — R442 *0_4 — A_LAD1 R — B_LAD1 R — R560 0_4 — LAD1
<12,32> LAD0 — R441 *0_4 — A_LAD0 R — B_LAD0 R — R562 0_4 — LAD0

Debug

<13,27> PCIRST# — R450 *0_4
<2> PCLK_DEBUG — R448 *0_4
→ C-Link_RST / C-Link_DAT / C-Link_CLK

+3V R446 *SP@0_6 +3V_MINI_R — TV use +3V — C510 .1U/16V_4

RF_EN R557 *0_4 A_RF_EN — A_W_DISABLE# / B_W_DISABLE# — B_RF_EN R556 0_4 → RF_EN <32>

+5V L41 *SP@FBJ3216HS800_12 +5V_TV-CARD — A_BT_CHCLK / A_BT_DATA — B_BT_CHCLK / B_BT_DATA

500mA, 25mil — C494 4.7U/6.3V_6 — C493 .1U/16V_4

GND ×10 — GND ×10

93 94 A/B MODULE Share pin

SP@ single QUASAR-CA0404-071N21_92P

FOR R446 & L41	
LOW COST	N
TM & AS	Y

LC@ LOW COST 噰

+3V_S5 for WWAN card is 2.75A

+3V — C513 4.7U/6.3V_6 — C499 4.7U/6.3V_6 — C491 .1U/16V_4 — C498 .1U/16V_4

+1.5V — C512 .1U/16V_4 — C317 .1U/16V_4 — C500 10U/6.3V_8

+3V — R449 10K_4 — Q35 2N7002 — <2,14,16,20,21,29> PCLK_SMB → MINI_SMCLK

+3V — R451 10K_4 — Q36 2N7002 — <2,14,16,20,21,29> PDAT_SMB → MINI_SMDATA

+3VSUS — Q34 *DTC144EUA — <14,21,32> PCIE_WAKE# → PCIE_WAKE# R

FOR EMI

+5V C605 1U/10V_4 — VCC_CORE C70 1U/10V_4 — VIN C150 1U/25V_6 — +3V C613 .1U/16V_4 — +1.05V C614 .1U/16V_4

+3V_S5

INVCC0 C607 1U/25V_6 — +VDR_SUS C273 1U/10V_4 — +VDR_SUS C394 1U/10V_4 — +1.8V C615 .1U/16V_4

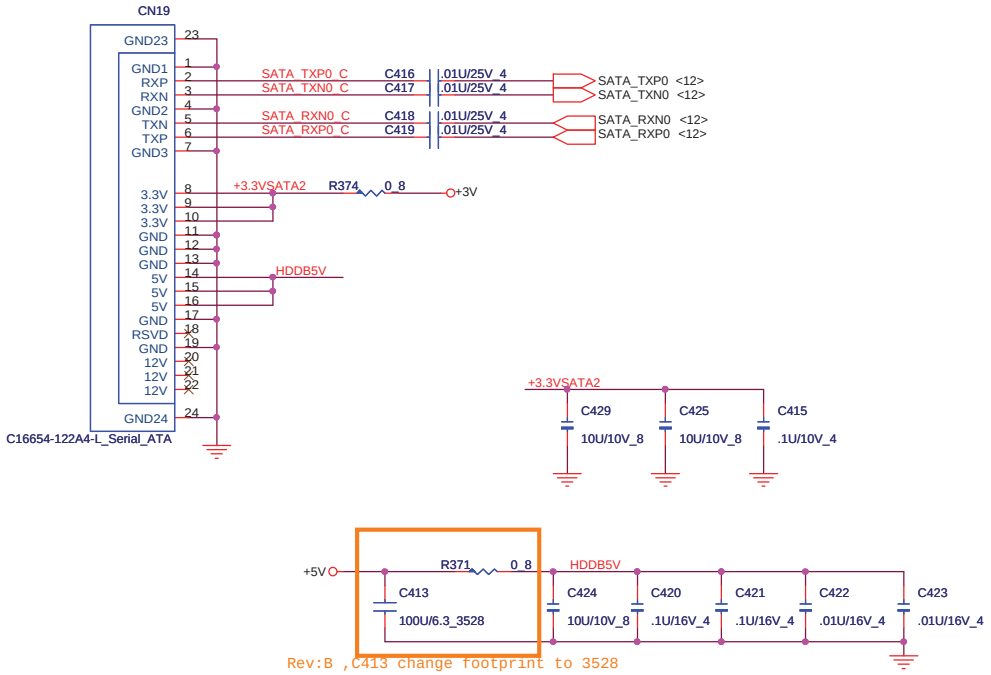
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	MINI PCI-E card/TV/TPM	1A
Date: Tuesday, August 12, 2008	Sheet 23 of 40	

SATA HDD

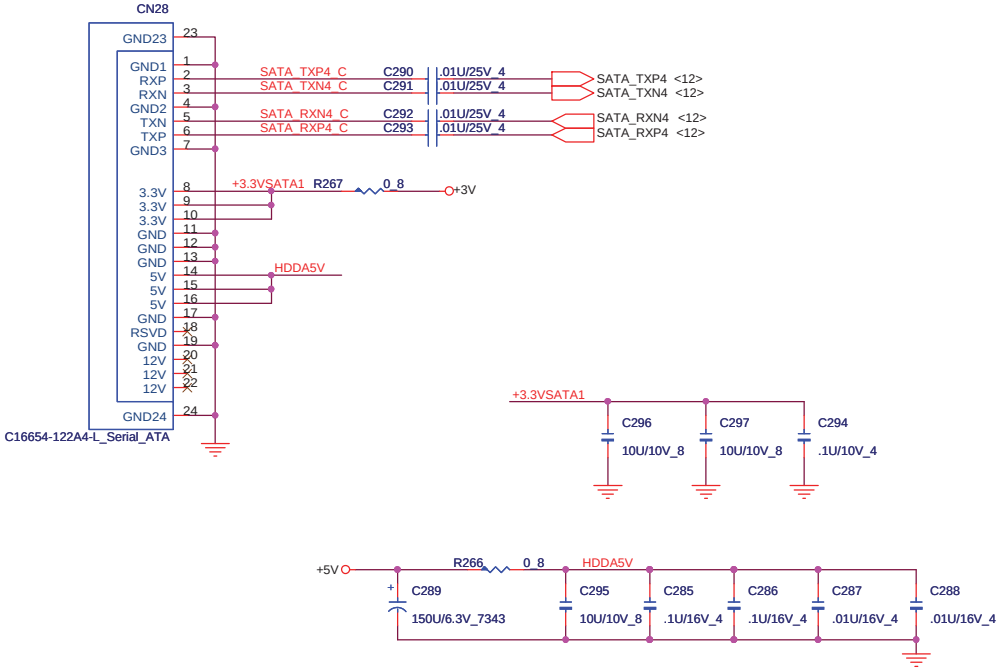
11/8 REV:B Conn. 奔癸秸 CN28 & CN19

Main

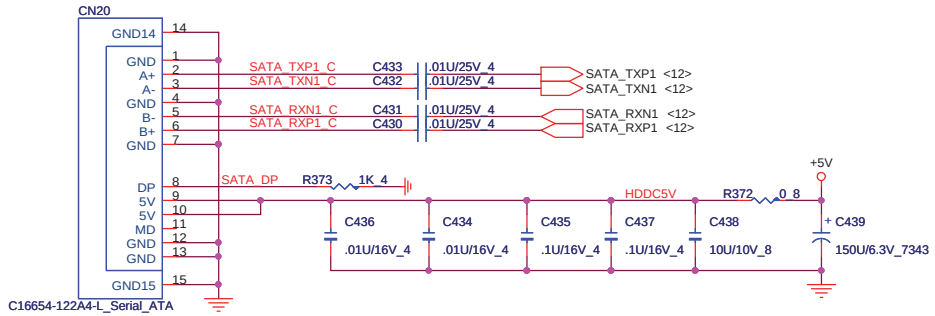


Rev:B ,C413 change footprint to 3528

2ND SATA HDD

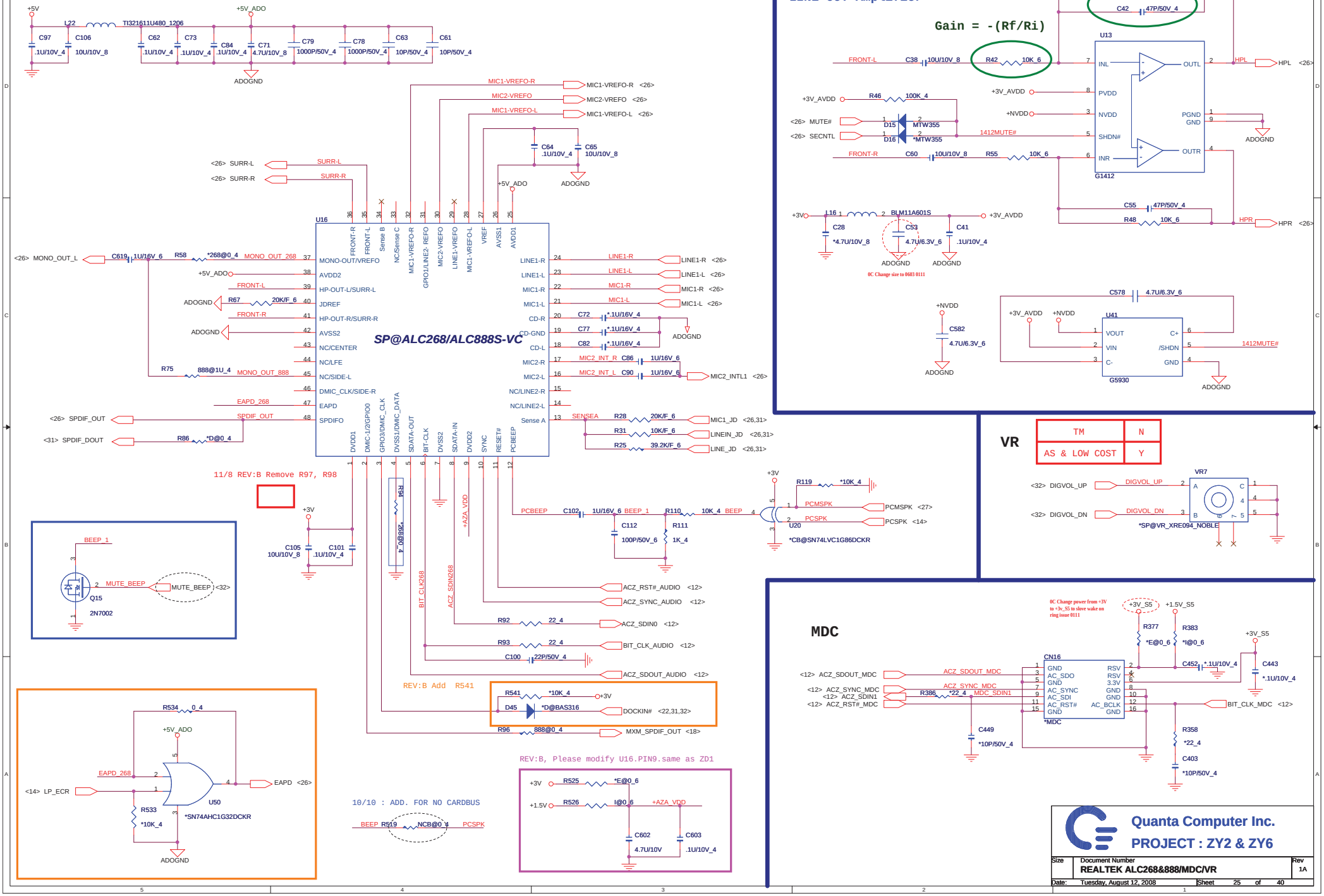


ODD (SATA)

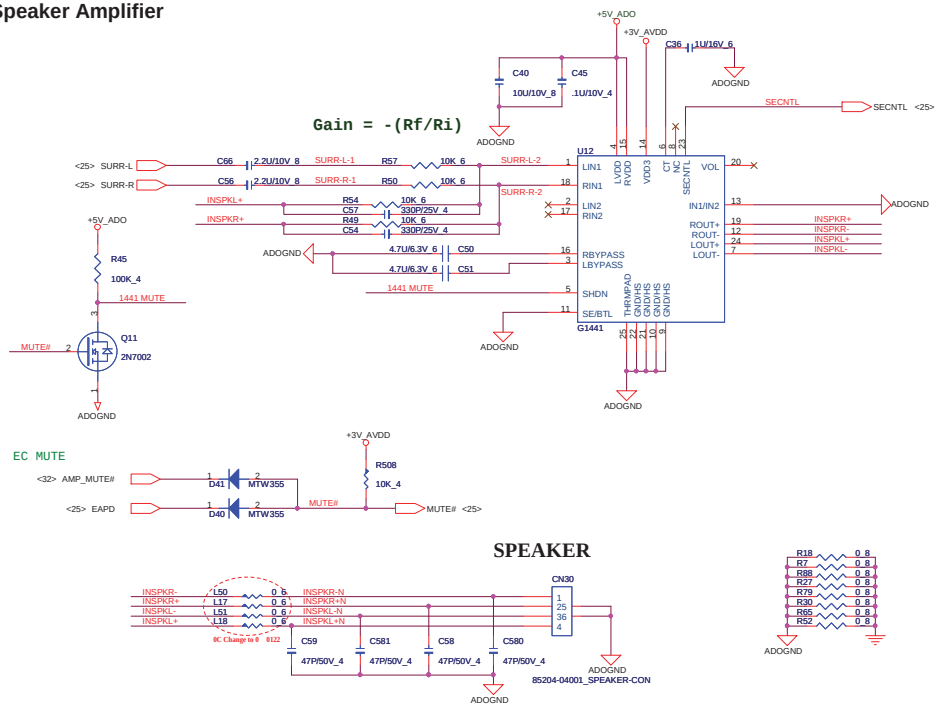


Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: SATA-HDD & ODD	Rev: 1A
Date: Wednesday, August 13, 2008	Sheet 24 of 40	

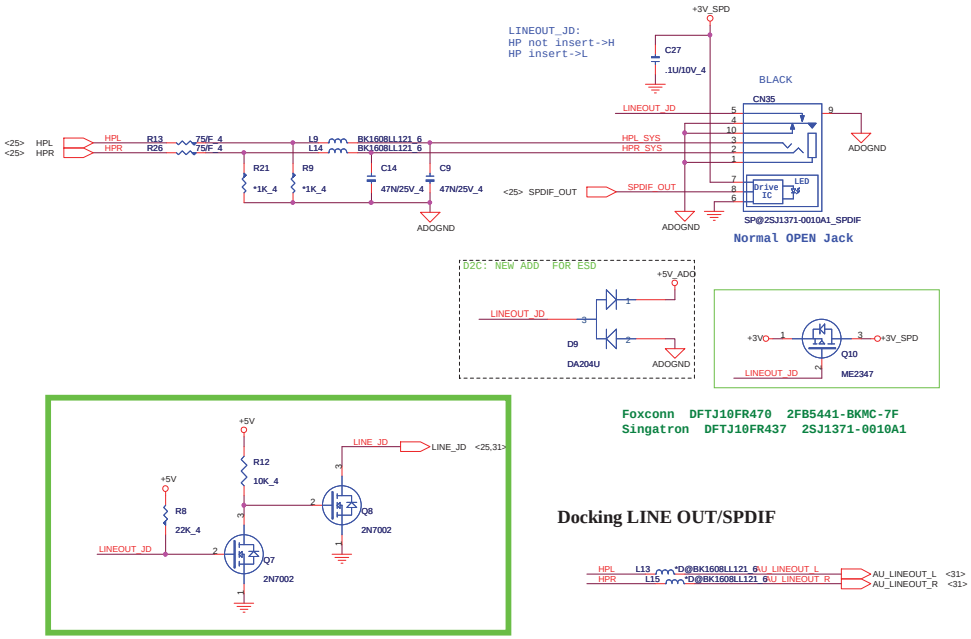
CODEC(ALC268)



Speaker Amplifier

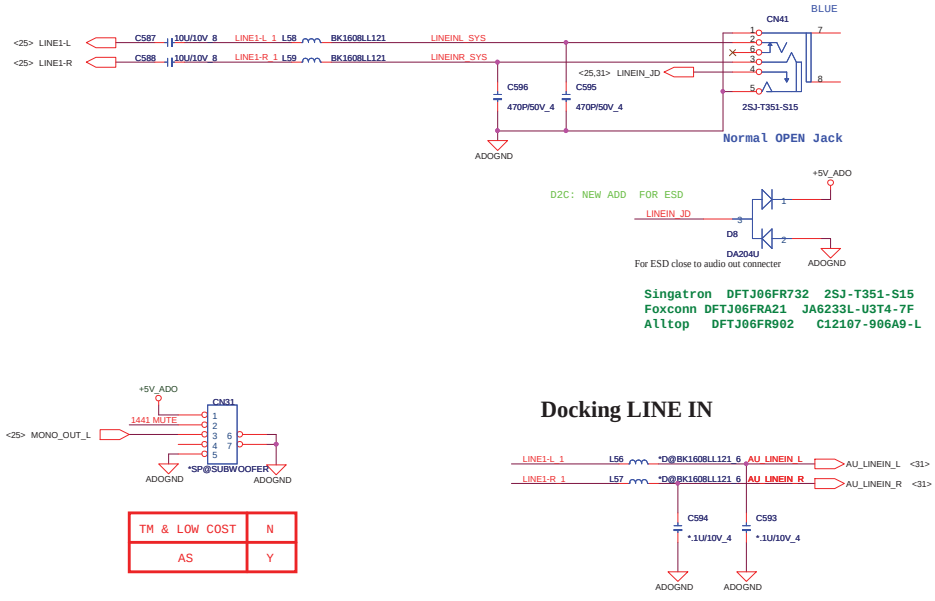


SYSTEM LINE OUT/SPDIF



Docking LINE OUT/SPDIF

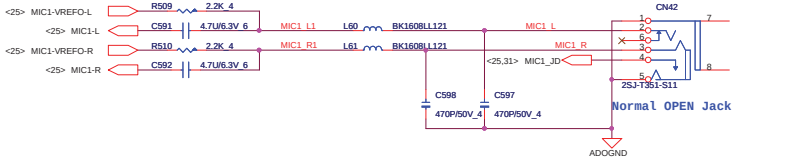
SYSTEM LINE IN/SUBWOOFER



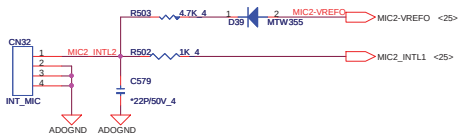
TM & LOW COST	N
AS	Y

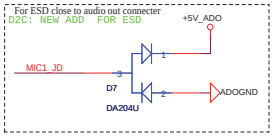
Docking LINE IN

MIC



INT MIC array





Singatron DFTJ06FR741 2SJ-T351-S11
Foxconn DFTJ06FRA39 JA6233L-P3T4-7F
Alltop DFTJ06FR899 C12107-D06A9-L

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Thursday, August 28, 2008	Sheet 26 of 40	

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R239 *CB@100/F_4 PCM_IDSEL

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

O2MICRO OZ2210 8PIN
SINGLE SLOT PARALLEL
POWER SWITCH

PCMCIA SOCKET

CN9

*CB@PCMCIA_SOCKET

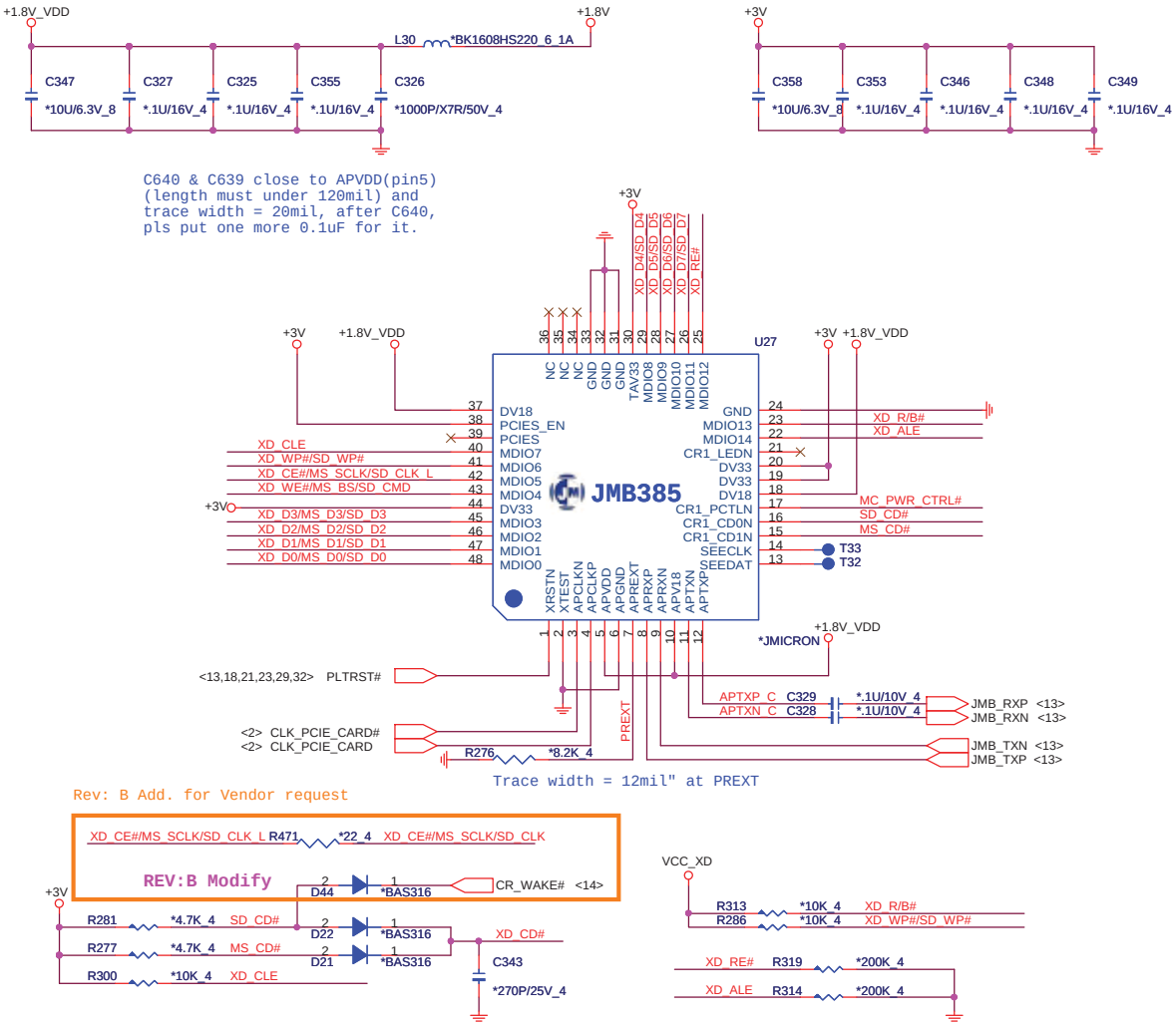
PCMCIA SOCKET

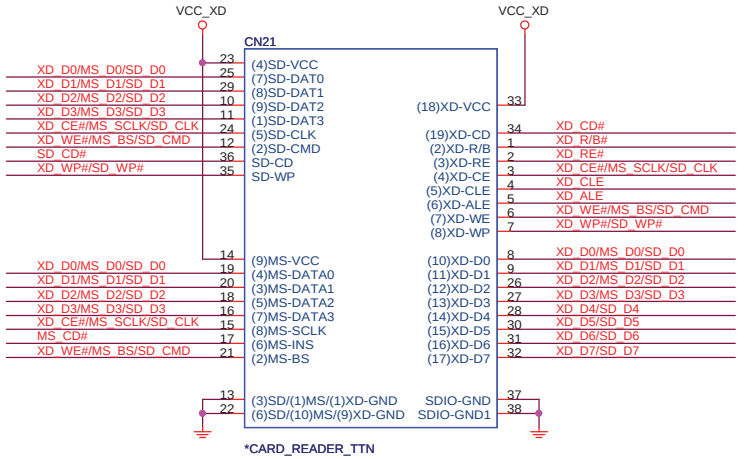
CN44

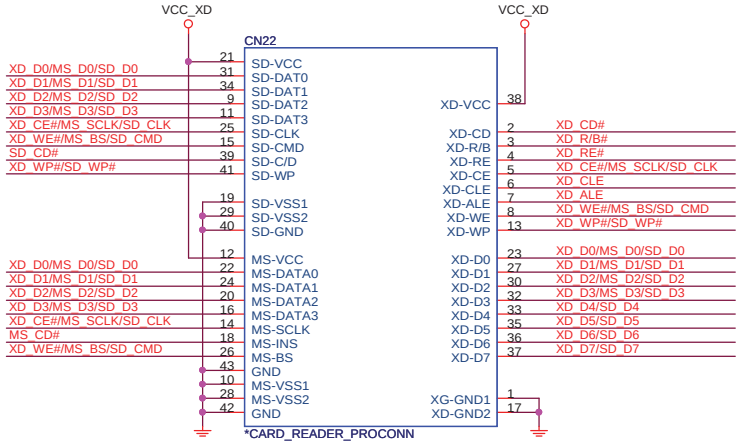
*CB@PCMCIA_SOCKET

Quanta Computer Inc.	
PROJECT : ZY2 & ZY6	
Size	Document Number: PCMCIA(OZ601) — Rev: 1A
Date: Thursday, August 28, 2008	Sheet 27 of 40

7 IN 1 CARD READER

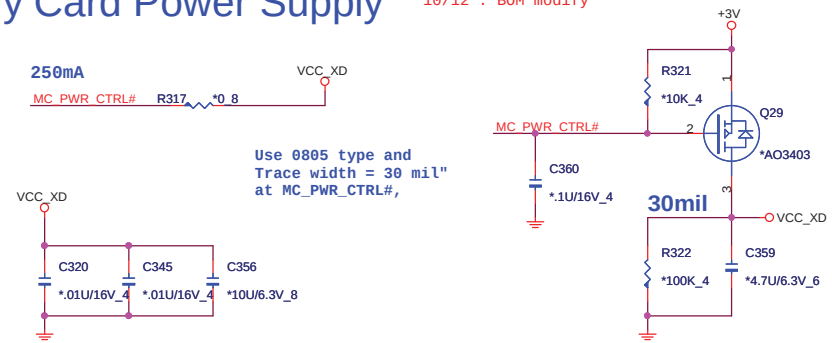






Memory Card Power Supply

10/12 : BOM modify



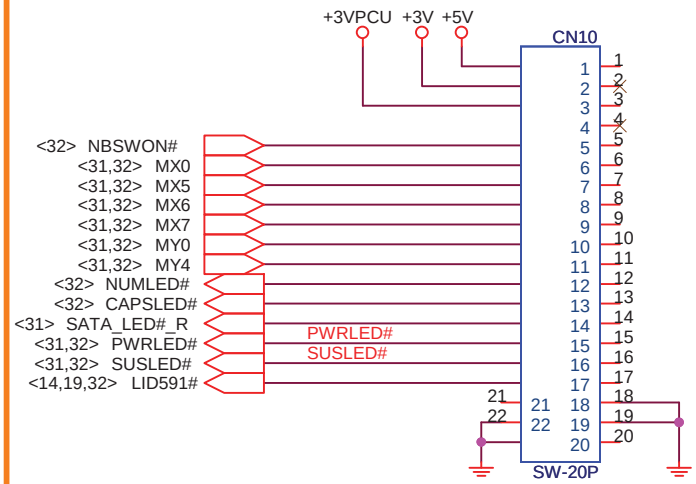
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

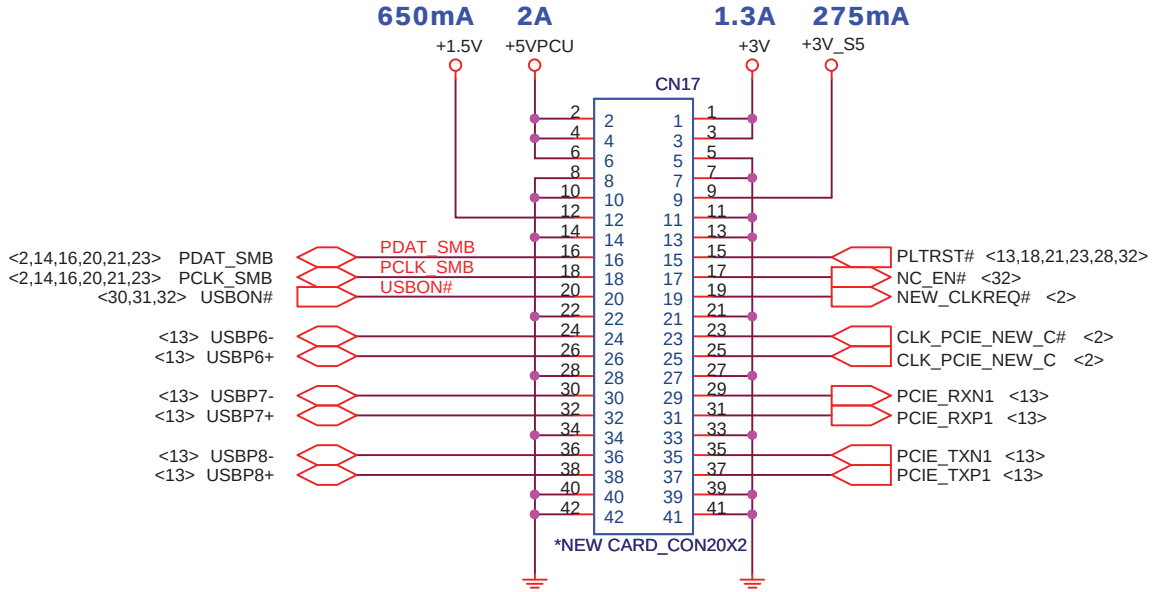
Size	Document Number	Rev
	CARD READER JMB385	1A
Date: Thursday, August 28, 2008	Sheet 28 of 40	

To NEW-CARD & EXT. USB

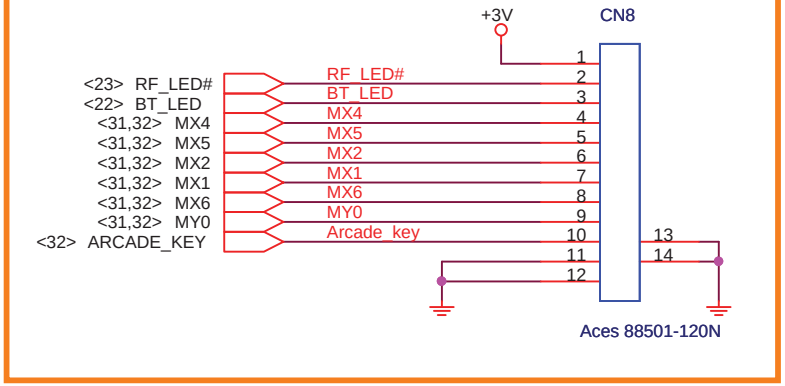
REV:B, CN10 change footprint



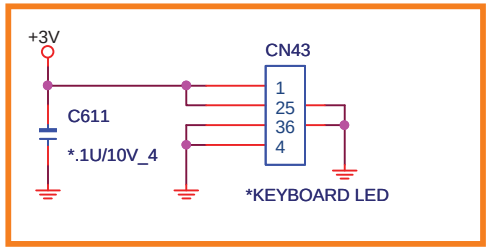
650mA 2A 1.3A 275mA



REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Fnction	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4



Rev:B Add CN43 For backlight KB

Rev:B Change to 蛾 to よPAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395

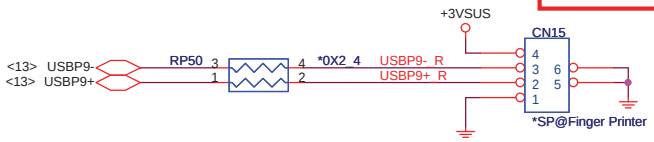
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

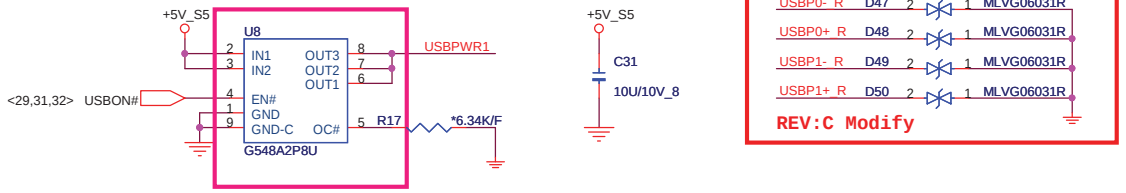
Size	Document Number	Rev
	BTB CONN.	1A
Date: Tuesday, August 12, 2008	Sheet 29 of 40	

Finger Printer

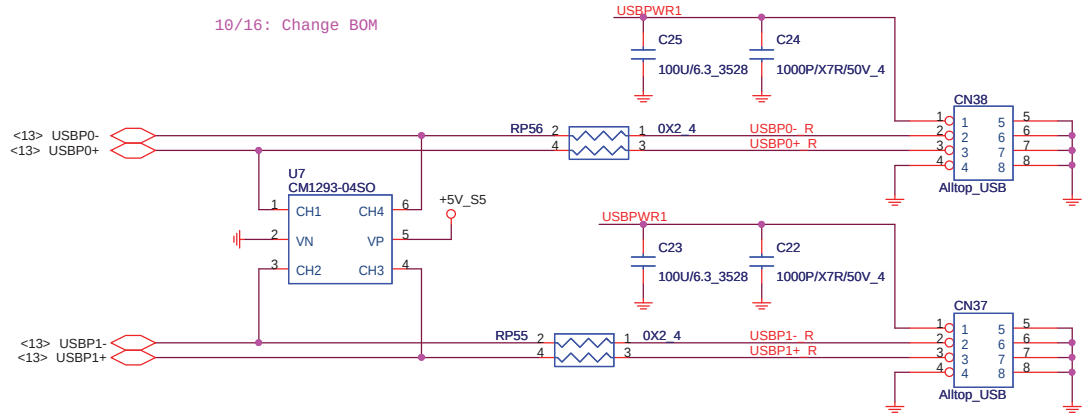
TM & AS	Y
LOW COST	N



USB

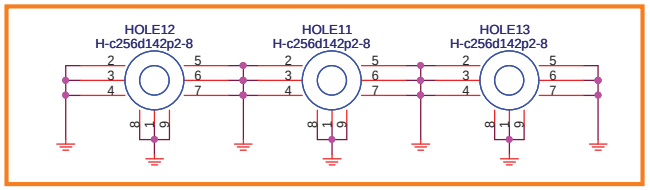


10/16: Change BOM

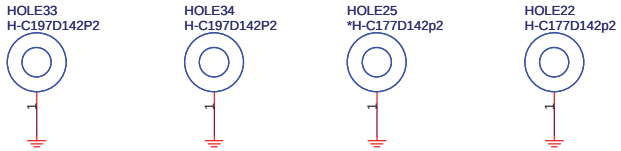


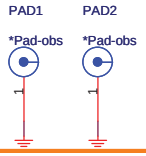
HOLES

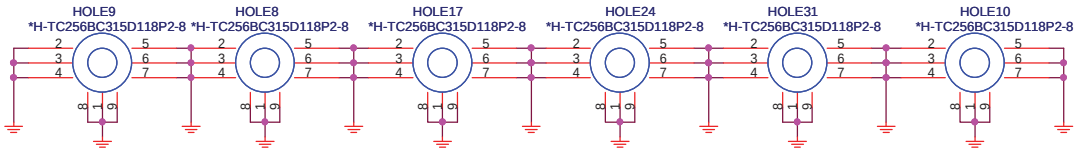
CPU NUT (BOT)



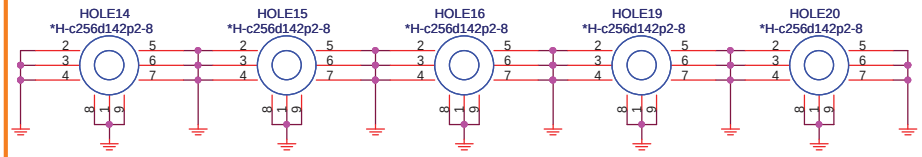
Rev : B Add MINI NUT

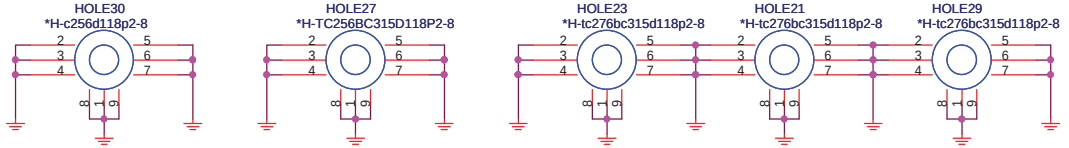




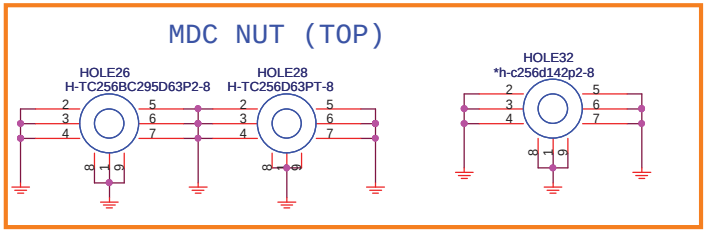


MXM NUT (BOT)

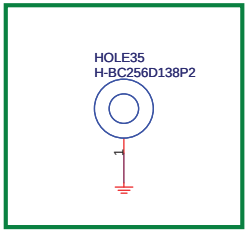




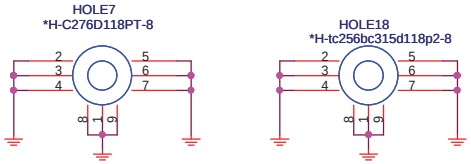
MDC NUT (TOP)



Rev:B New add HOLE32
HOLE26 & 28 Change footprint



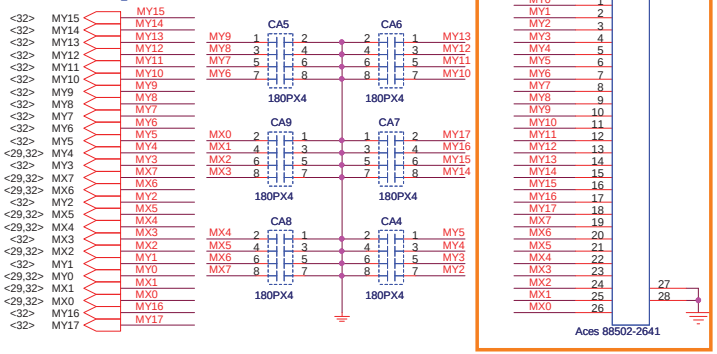
HOLE35 瑞稙 BOT



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

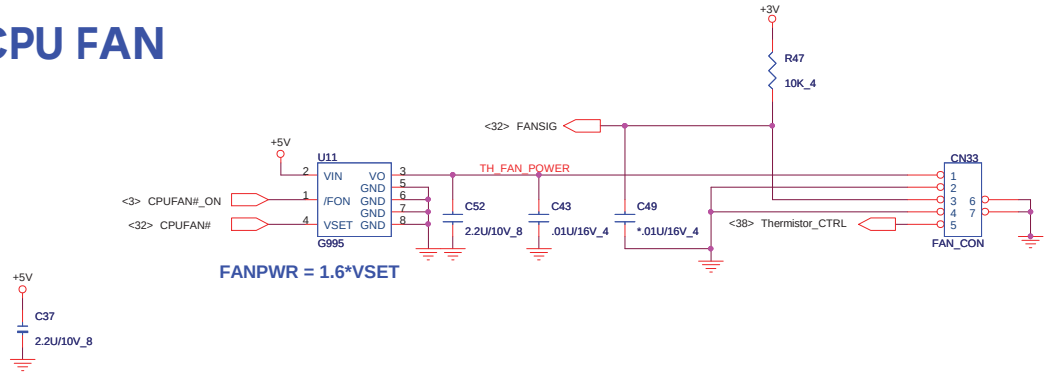
Size	Document Number	Rev
	USB/FINGER PRINTER	1A
Date: Tuesday, August 12, 2008	Sheet 30 of 40	

INT K/B

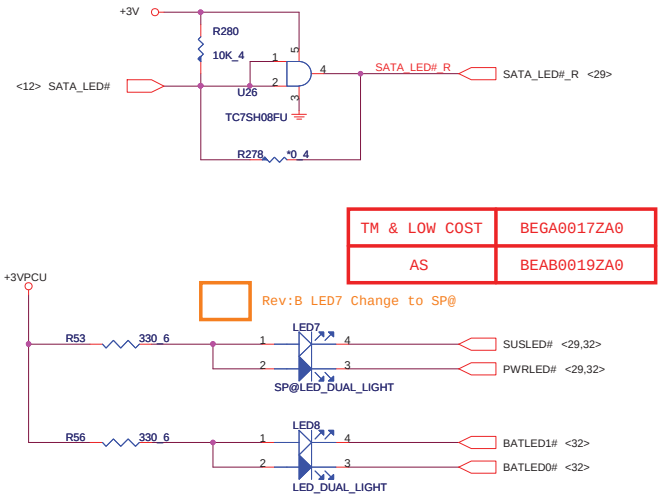


Rev:B change footprint

CPU FAN



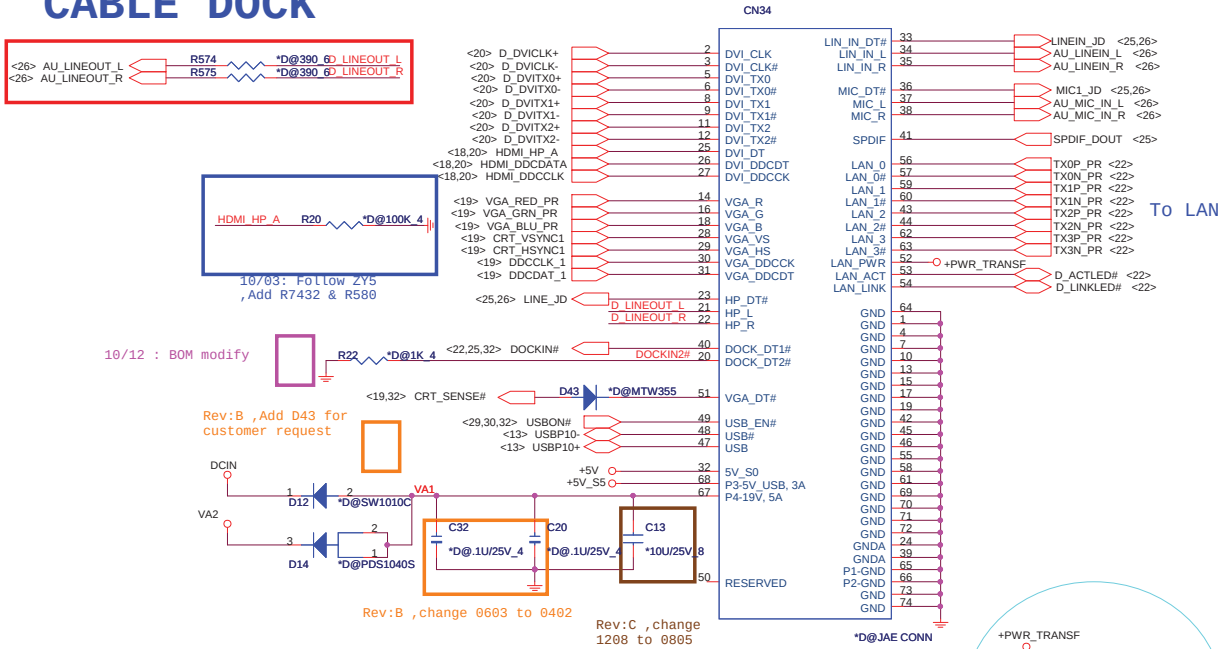
LED

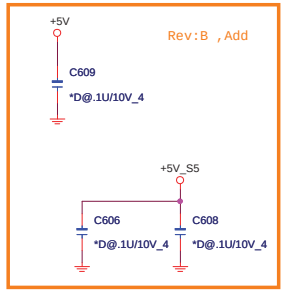


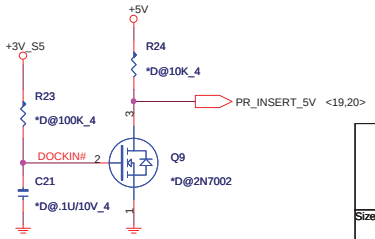
TM & LOW COST	BEGA0017ZA0
AS	BEAB0019ZA0

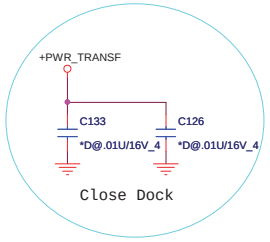
Rev:B LED7 Change to SP@

CABLE DOCK



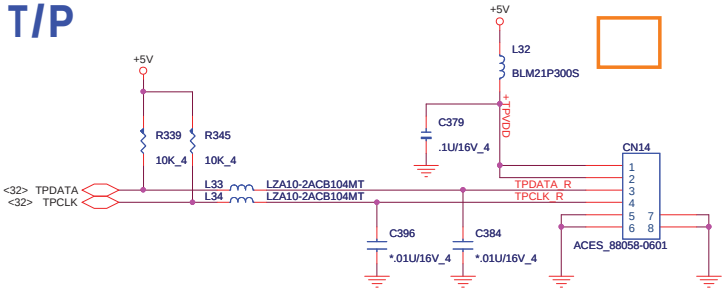






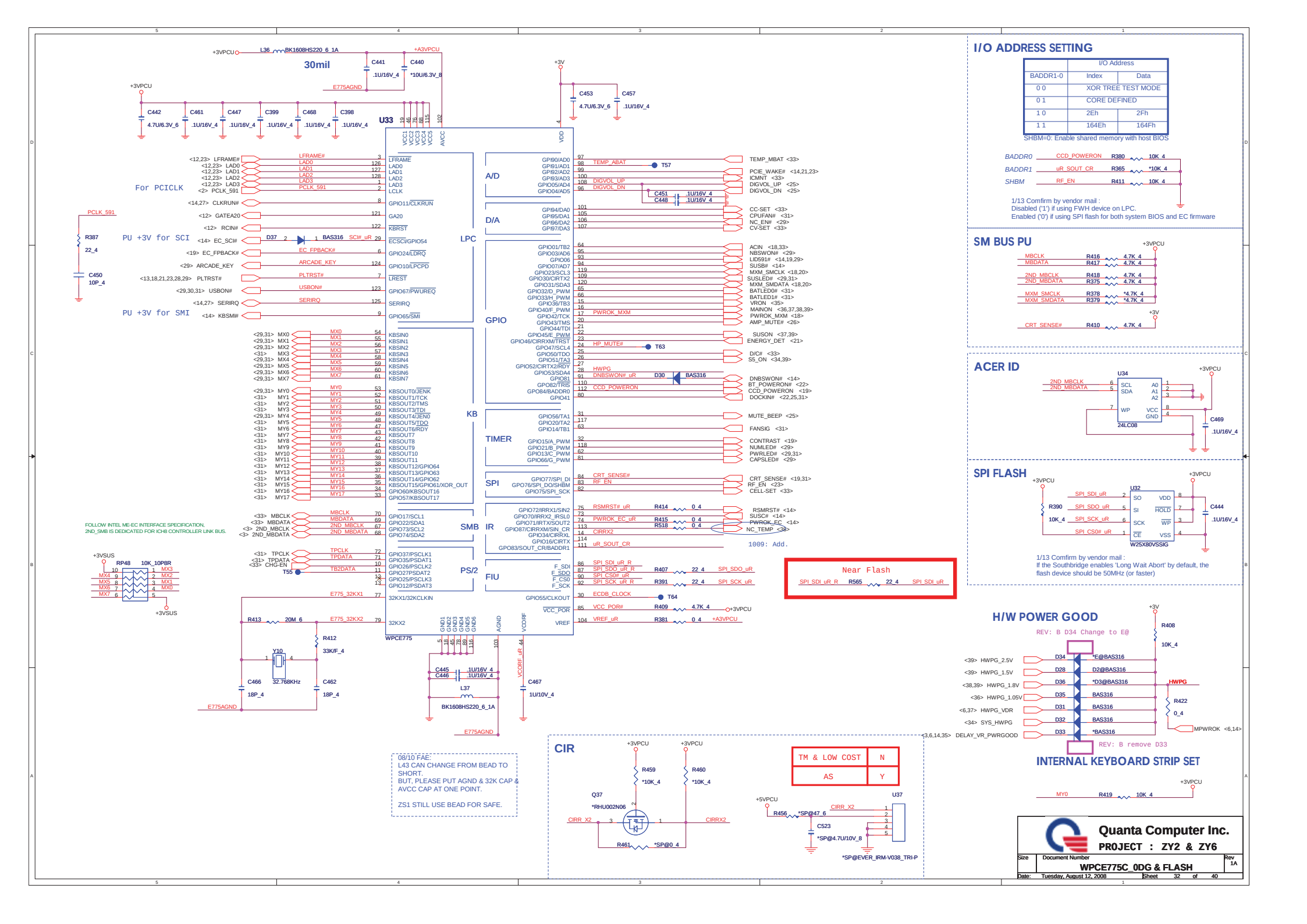
T/P

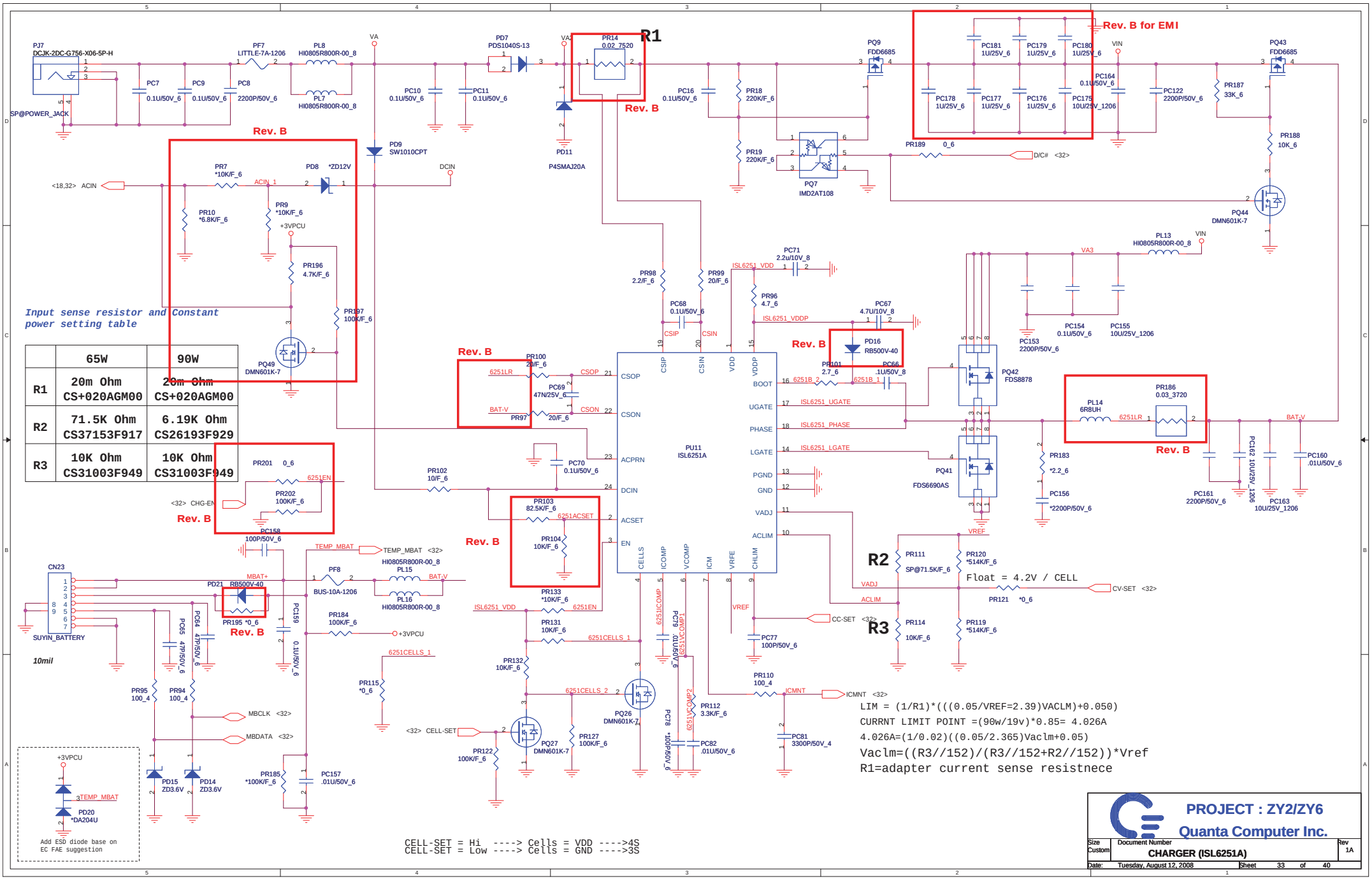
REV:B, CN14 change footprint

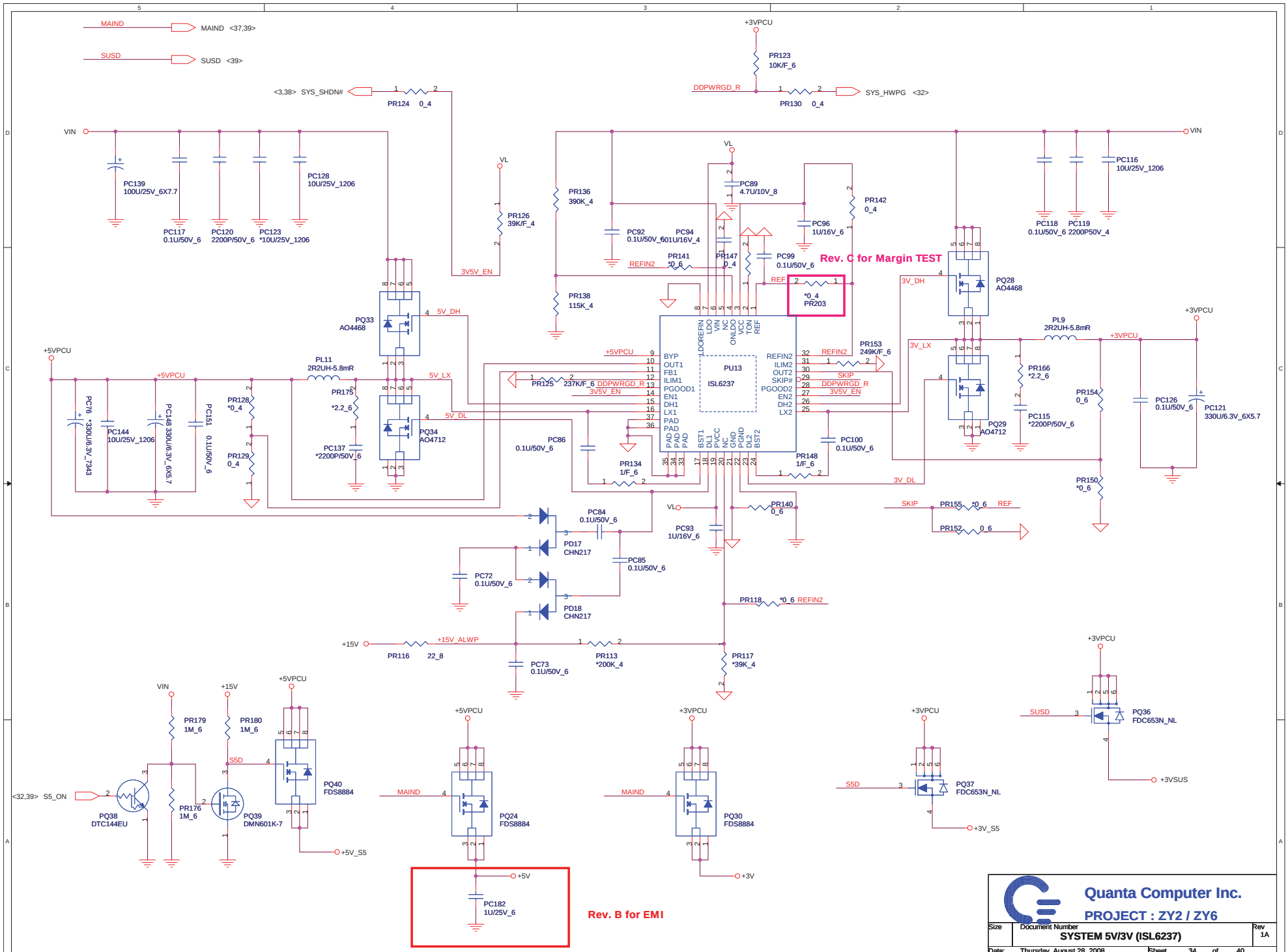


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

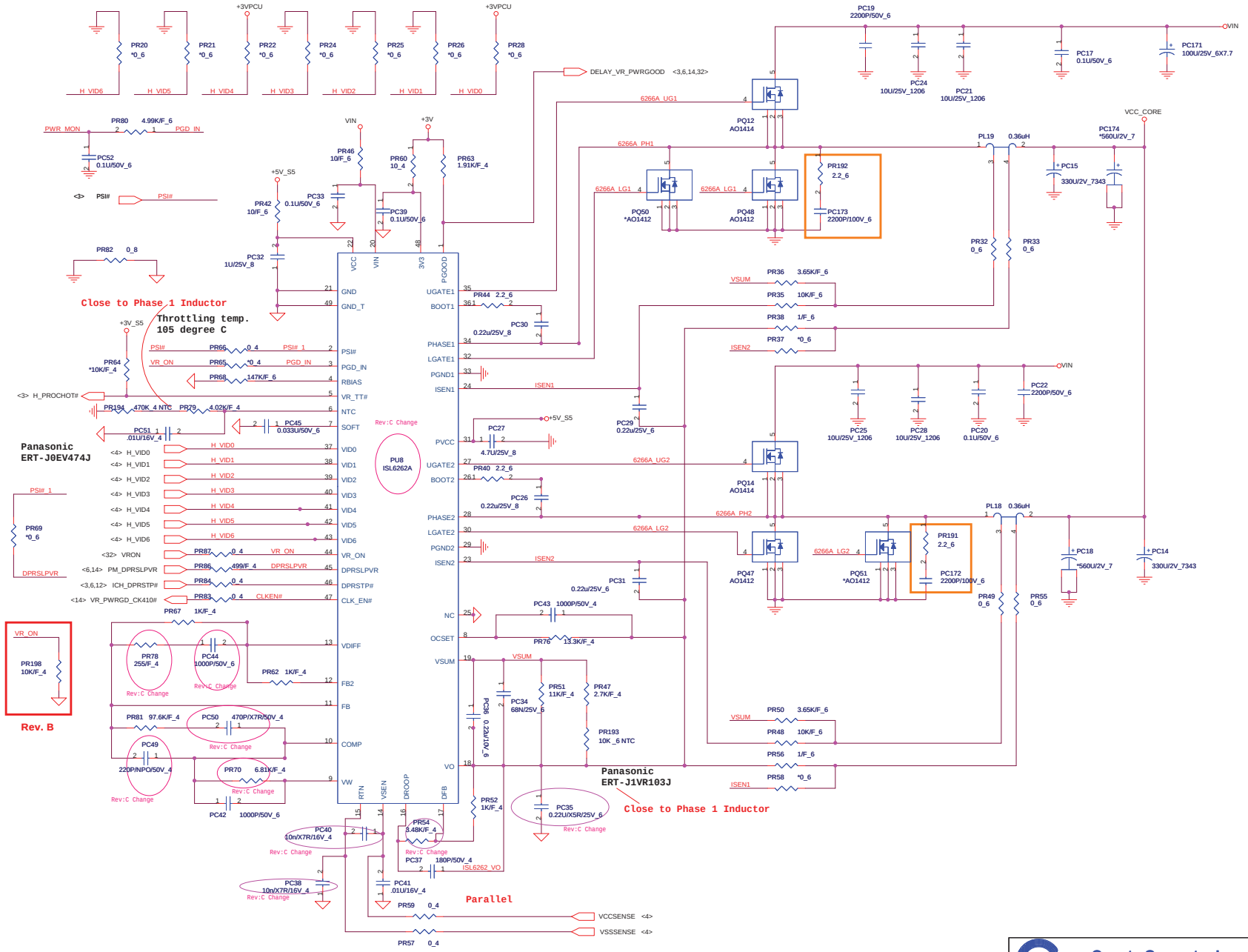
Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	1A
Date: Tuesday, August 12, 2008	Sheet 31 of 40	


U33
WPCE775
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
SMB
IR
PS/2
FIU
For PCICLK
PU +3V for SCI
PU +3V for SMI
30mil
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
08/10 FAE:
L43 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
1009: Add.
Near Flash
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
SM BUS PU
ACER ID
24LC08
SPI FLASH
W25X80VSSIG
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
H/W POWER GOOD
REV: B D34 Change to E@
REV: B remove D33
INTERNAL KEYBOARD STRIP SET
CIR
TM & LOW COST
N
AS
Y
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
WPCE775C_0DG & FLASH
Tuesday, August 12, 2008
Sheet 32 of 40

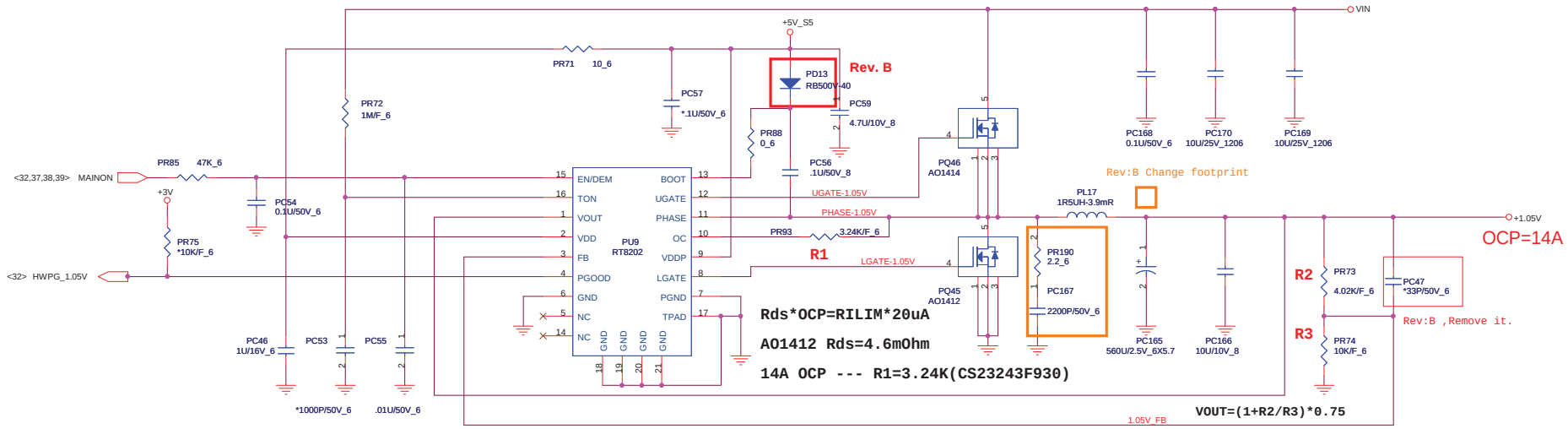

Rev. B for EMI
R1
Rev. B
Input sense resistor and Constant power setting table
65W
90W
R1
20m Ohm CS+020AGM00
20m Ohm CS+020AGM00
R2
71.5K Ohm CS37153F917
6.19K Ohm CS26193F929
R3
10K Ohm CS31003F949
10K Ohm CS31003F949
PU11 ISL6251A
R2
R3
Float = 4.2V / CELL
LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
Add ESD diode base on EC FAE suggestion
10mil
PROJECT : ZY2/ZY6
Quanta Computer Inc.
CHARGER (ISL6251A)
Tuesday, August 12, 2008
33 of 40



Quanta Computer Inc.			
PROJECT : ZY2 / ZY6			
Size	Document Number		Rev
	SYSTEM 5V/3V (ISL6237)		1A
Date: Thursday, August 28, 2008		Sheet 34 of 40	



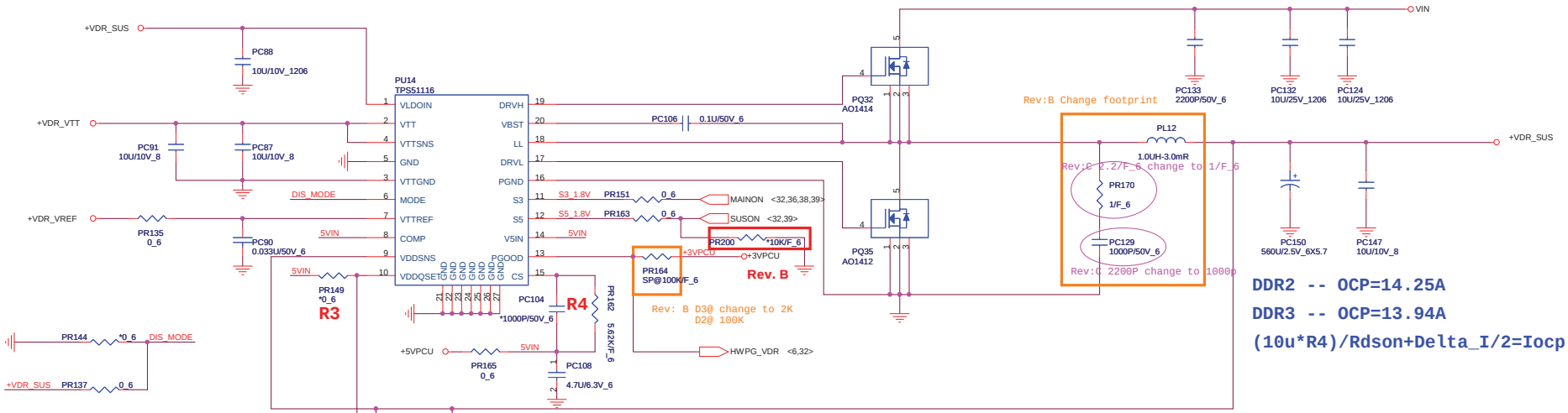
Quanta Computer Inc.			
PROJECT : ZY2 / ZY6			
Size: Custom	Document Number: CPU CORE(ISL6266)		Rev: 1A
Date: Tuesday, August 12, 2008		Sheet 35 of 40	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.		
PROJECT : ZY2 / ZY6		
Size	Document Number: VTT 1.05V (RT8202)	Rev: 1A
Date: Tuesday, August 12, 2008	Sheet 36 of 40	



	DDR2(1.8V)	DDR3(1.5V)
R1	76.8K CS37683F927	75K CS37503F919
R2	110K CS41103F910	76.8K CS37683F927

R1=(100*Vout-R2)K

if tune Vout R3 un-mount, R1 and R2 mount

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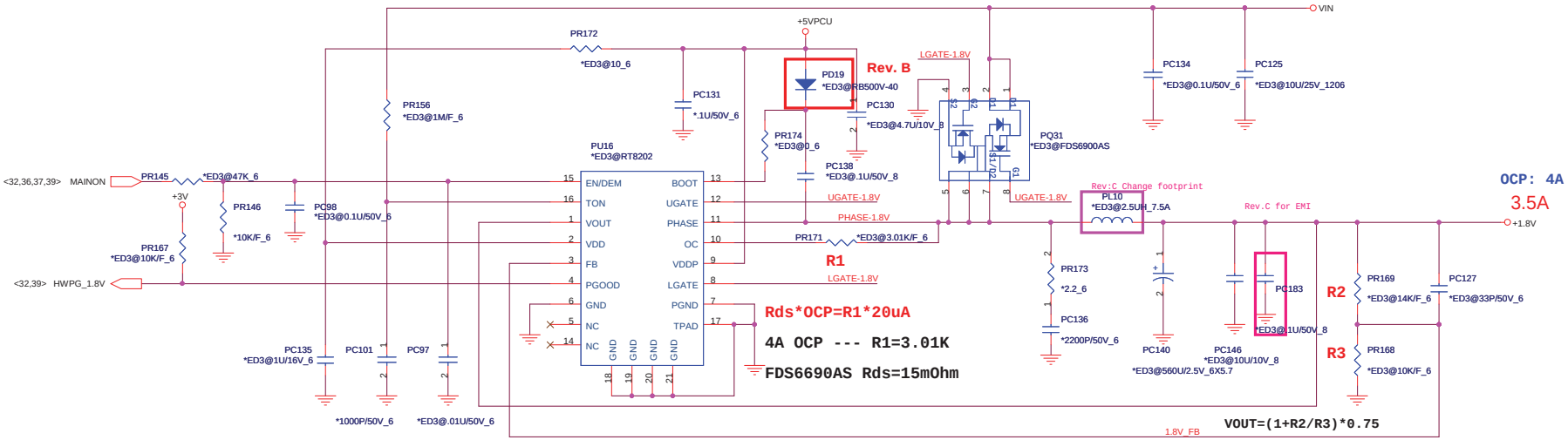
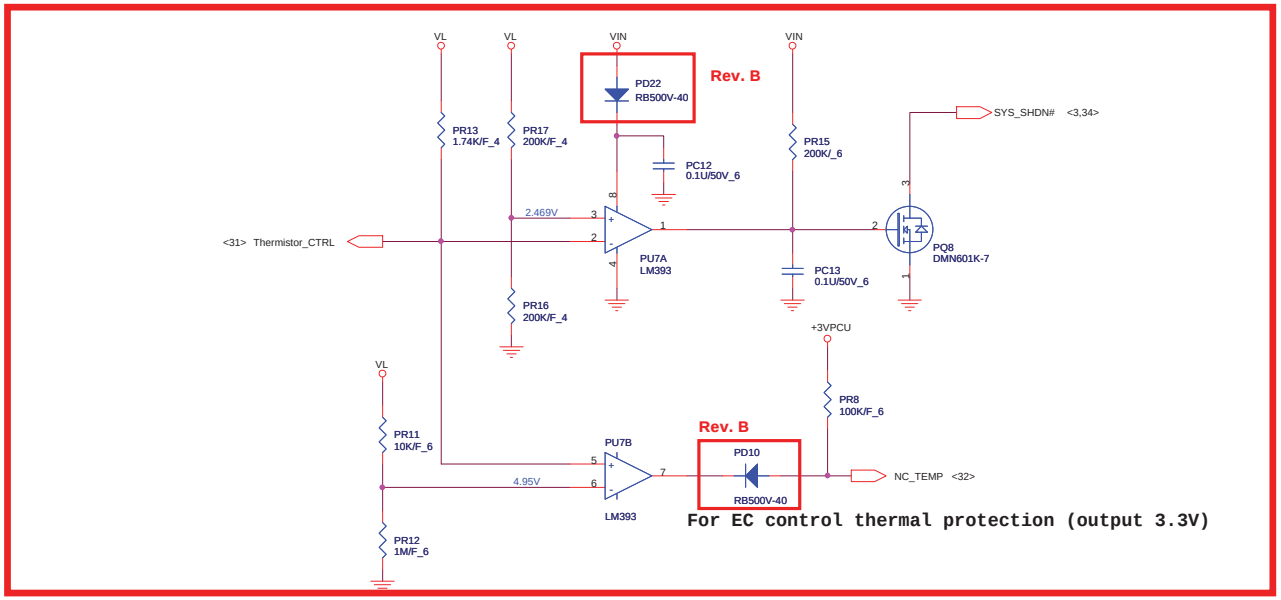
PROJECT : ZY2 / ZY6		
Size	Document Number VDR (TPS51116)	Rev 1A
Date: Tuesday, August 12, 2008	Sheet 37 of 40	



TON=3.85p*RTON*Vout/(Vin-0.5)

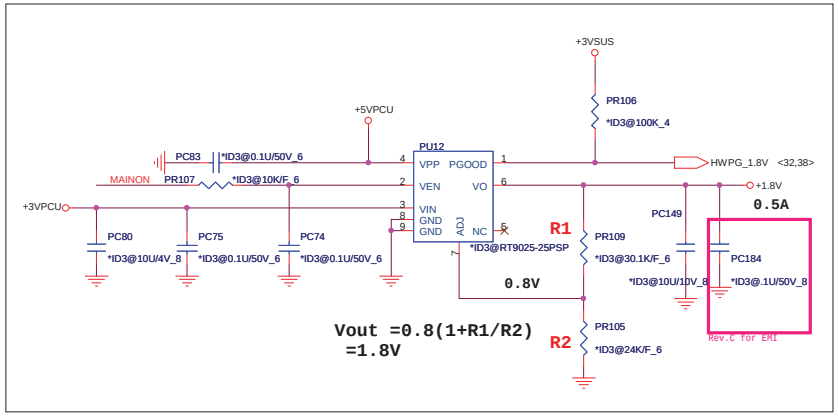
Frequency=Vout/(Vin*TON)

thermal protection --0928

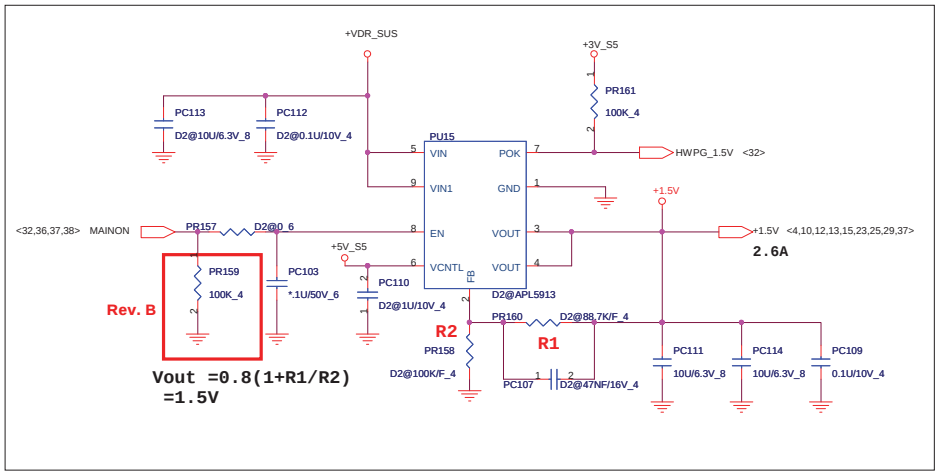


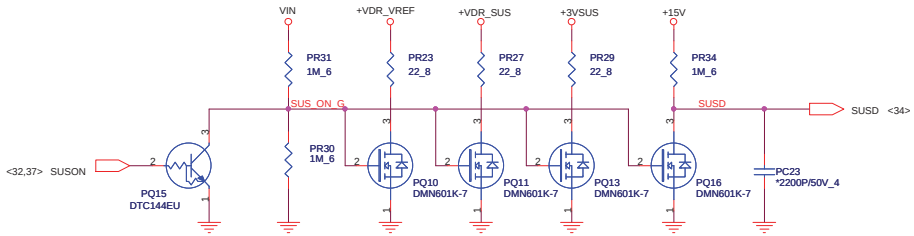
Quanta Computer Inc.		
PROJECT : ZY2 / ZY6		
Size	Document Number: 1.8V (RT8202)	Rev: 1A
Date: Tuesday, August 12, 2008	Sheet 38 of 40	

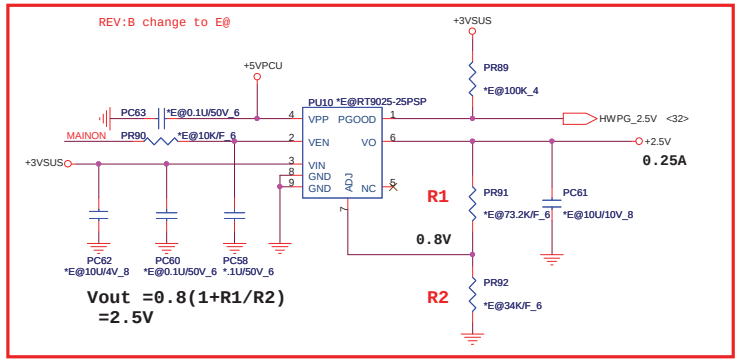
for DDR3 and UMA

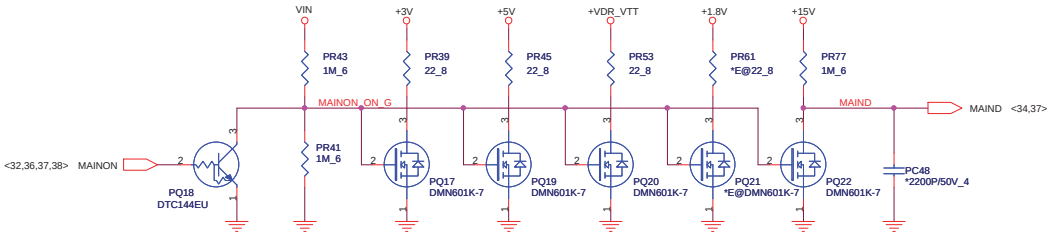


DDR3 -- NC

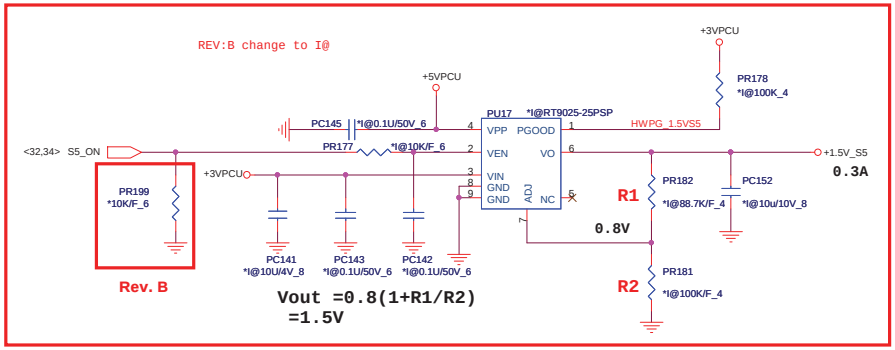


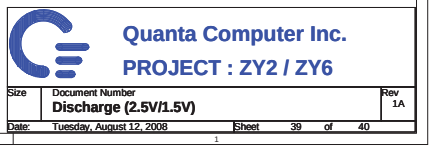




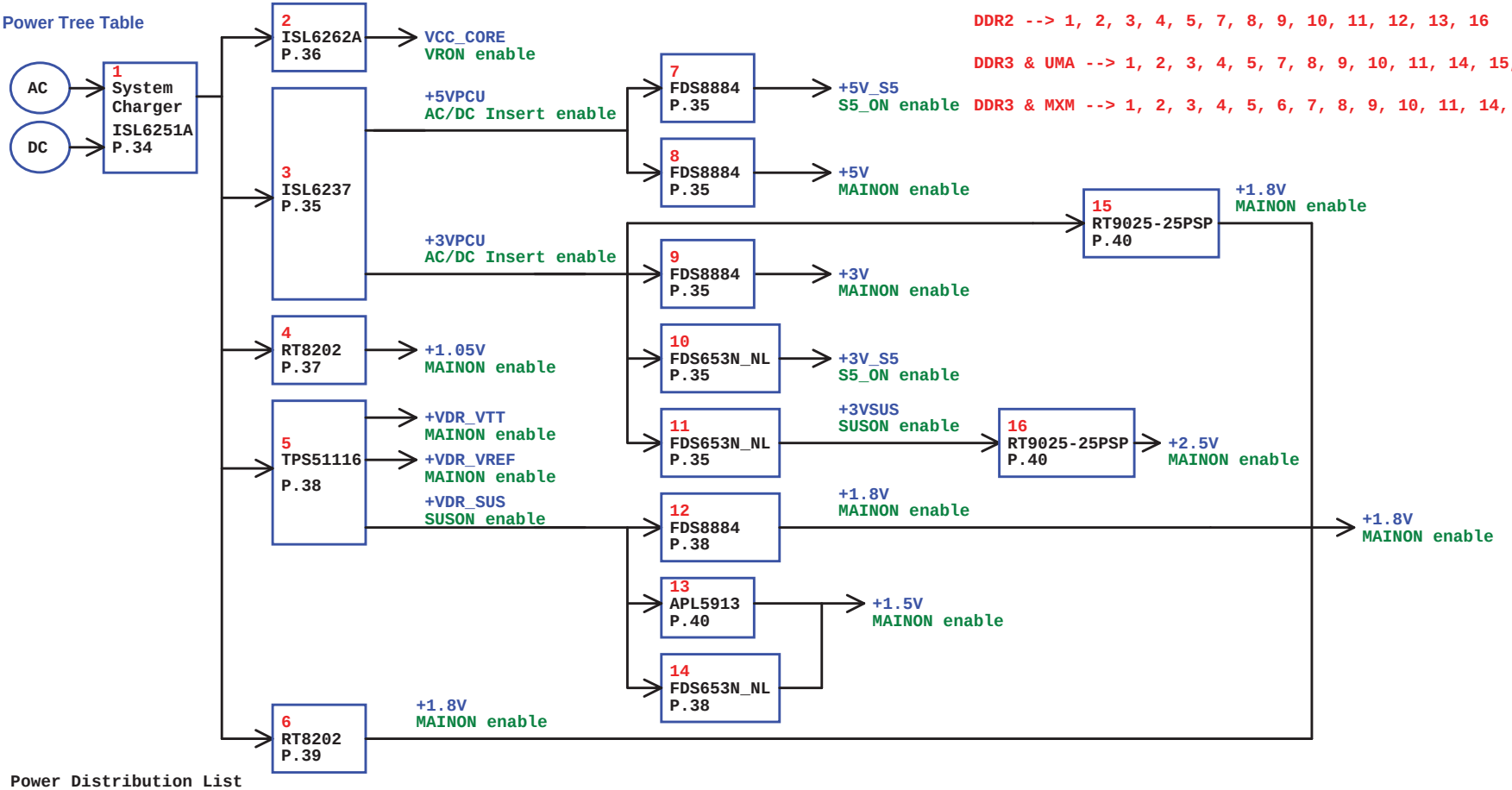


REV:B change to E@





Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

CHANGE LIST

Model	REV	
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : Add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)
	2A	Page19 : change U22 LVDS PWR SW IC to TI for display isuue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 : Change U13 packing from TQFN to TDFN for vendor request
	2B	Page20 : Add R566 ,R567 ,R568 ,R569 ,C612 ,C616 ,C617 ,C618 solve the HDMI EMI issue. Page26 : Change CN41 PIN 7 & 8 from ADOGND to NC solve the ESD issue. Change CN42 PIN 7 & 8 from ADOGND to NC solve the ESD issue. Page30 : Add D47 ,D48, D49 & D50 solve the USB ESD issue. Page31 : Add R574 & R575 (390)solve Docking audio noise issue. Page32 : Add EMI resistor (R565) in SPI flash interface.

MODEL	ZY2	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

PROJECT : ZY2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A

Date: Tuesday, August 12, 2008 Sheet 41 of 41

DOC NO.	PROJECT MODEL :	ZY2	APPROVED BY:		DATE:	2007/ 2/15
	PART NUMBER:		DRAWING BY:		REVISON:	3A