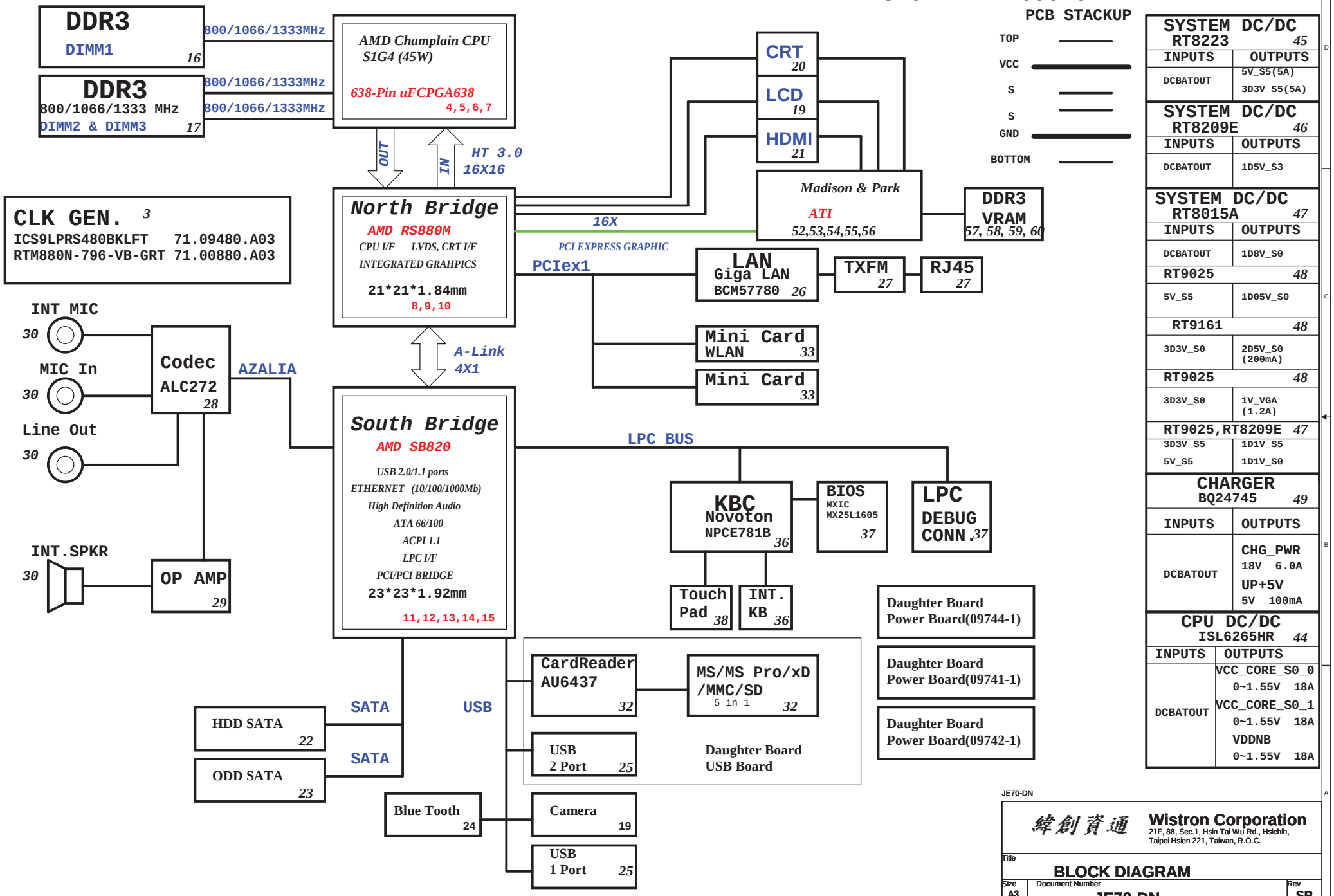
JE70-DN/SJV71-DN/HM72-DN Block Diagram

Project code: 91.4HP01.001
PCB P/N : 48.4HP01.011
REVISION : 09929-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8223 45	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8015A 47	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
RT9025 48	
5V_S5	1D05V_S0
RT9161 48	
3D3V_S0	2D5V_S0 (200mA)
RT9025 48	
3D3V_S0	1V_VGA (1.2A)
RT9025,RT8209E 47	
3D3V_S5 5V_S5	1D1V_S5 1D1V_S0

CHARGER BQ24745 49	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

JE70-DN

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JE70-DN | Rev: SB
Date: Wednesday, March 31, 2010 | Sheet 1 of 63

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EC Functional Strap Definitions

page9

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS880 use HSYNC#)

*1 :Disable 0 : Enable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

Signal	Comment
TEST# pin110	Test Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the device operation mode as follows: **No pull-down resistor: Normal operation mode (XORTR and TRIST strap pins are ignored).** 10 KΩ external pull-down resistor:Test mode (ICT or XOR-Tree Test mode, according to XORTR and TRIST strap pins).
XORTR# pin111	XOR-Tree Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the XOR-Tree Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. **10 KΩ external pull-down resistor:XOR-Tree Test mode .Note: TRIST strap pin must be left unconnected.**
TRIST# pin112	ICT Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the ICT Test mode, if TEST is strapped low: **No pull-down resistor: Not allowed if TEST pin is strapped low.** 10 KΩ external pull-down resistor:ICT Test mode (see Section 3.4.1 on page 53), forces the device to float its output and I/O pins.Note: XORTR strap pin must be left unconnected.
JEN0#, JENK# pin49,53	JTAG Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the JTAG signals to device pins (see Table 4 on page 35 for details). **Both JEN0 and JENK, are pulled to 1 by an internal resistor** The external 10 KΩ pull-down resistor must be connected to GND.
SHBM pin83	Shared Host BIOS Memory. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the state of the shared BIOS memory. **No pull-down resistor:Disable the shared BIOS memory.** 10 KΩ external pull-down resistor:Enable the shared BIOS memory
SDP_VIS# pin41	Port80 (SDP) Visibility Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the Visibility mode for the Port80 (SDP). **No pull-down resistor: SDP in Normal mode** 10 KΩ external pull-down resistor:SDP in Visibility mode.
XOR_OUT pin35	XOR-Tree Output. The device pins are internally connected in a XOR-tree structure

page15

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

page15

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

page12

	USB Pair	USB Device
	12	MINI2 CARD
	11	NC
	10	NC
	9	CCD
	8	NC
	7	Bluetooth
	6	USB3
OCP3#	5	USB2
	4	CardReader
	3	NC
OCP2#	2	USB4
	1	MINI1 CARD
OCP0#	0	USB1

JE70-DN

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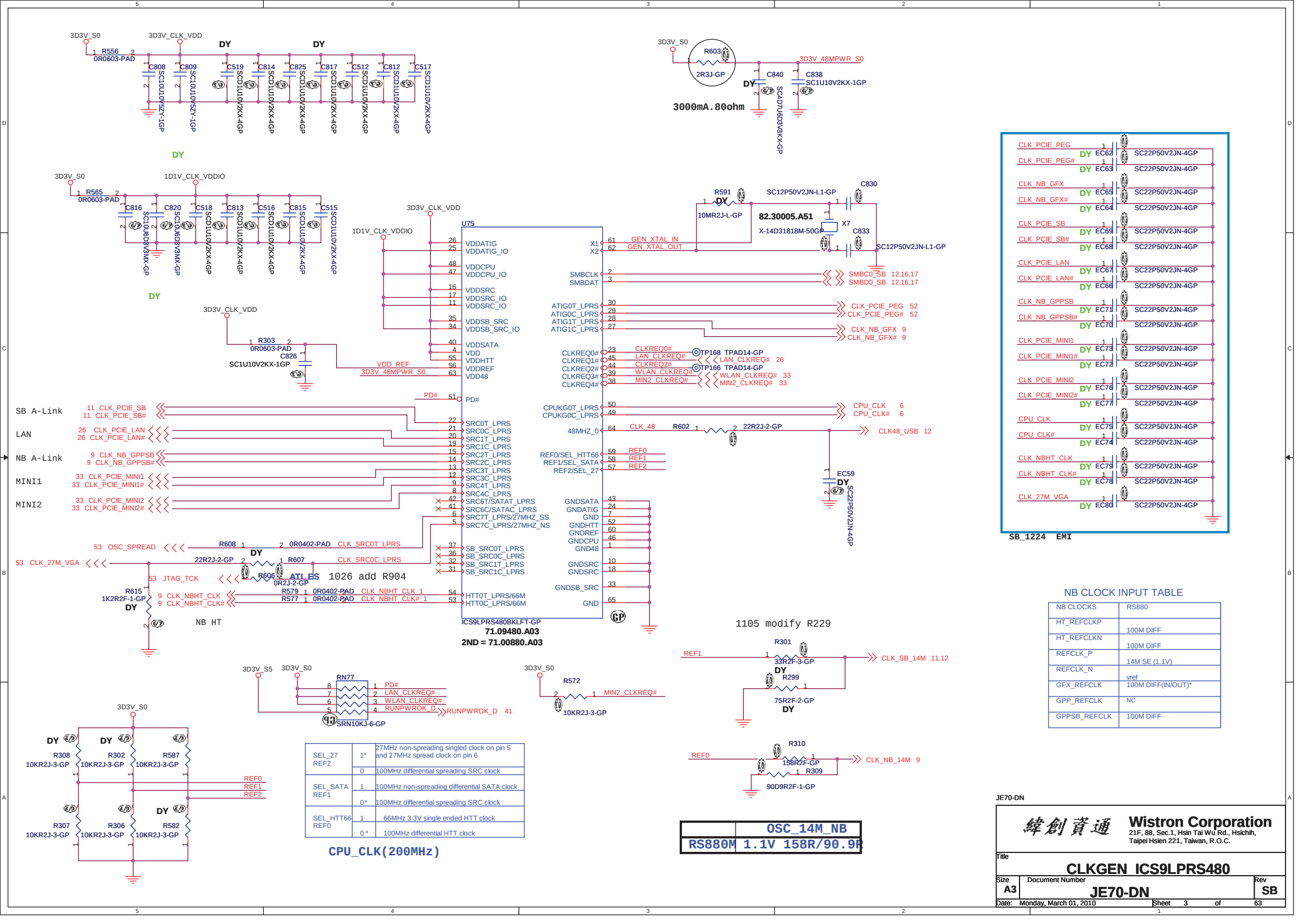
Title: Reference

Size: A3 | Document Number: JE70-DN | Rev: SB

Date: Thursday, November 19, 2009 | Sheet 2 of 63



SEL_27 REF2		
	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

CPU_CLK(200MHz)

	OSC_14M_NB
RS880M	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RS880
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC
GPPSB_REFCLK	100M DIFF

JE70-DN

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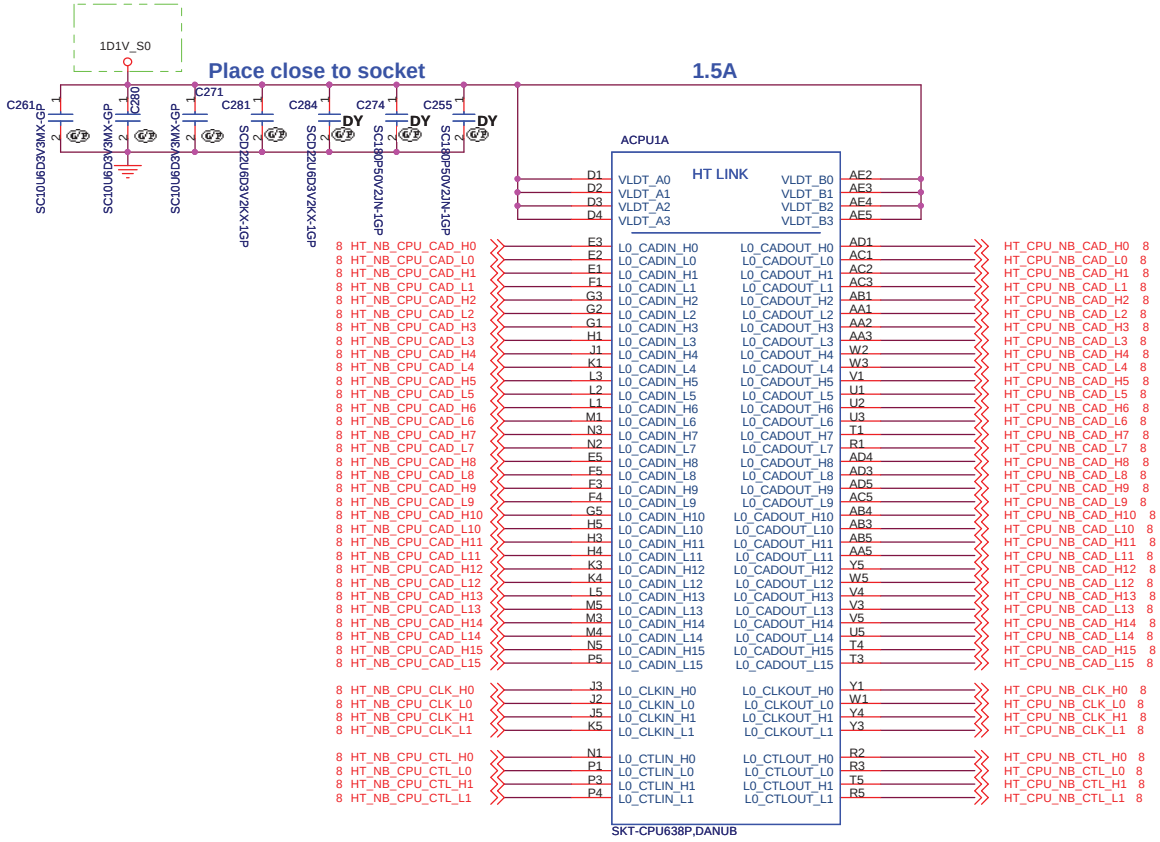
Title: CLKGEN ICS9LPRS480

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Monday, March 01, 2010 Sheet 3 of 63

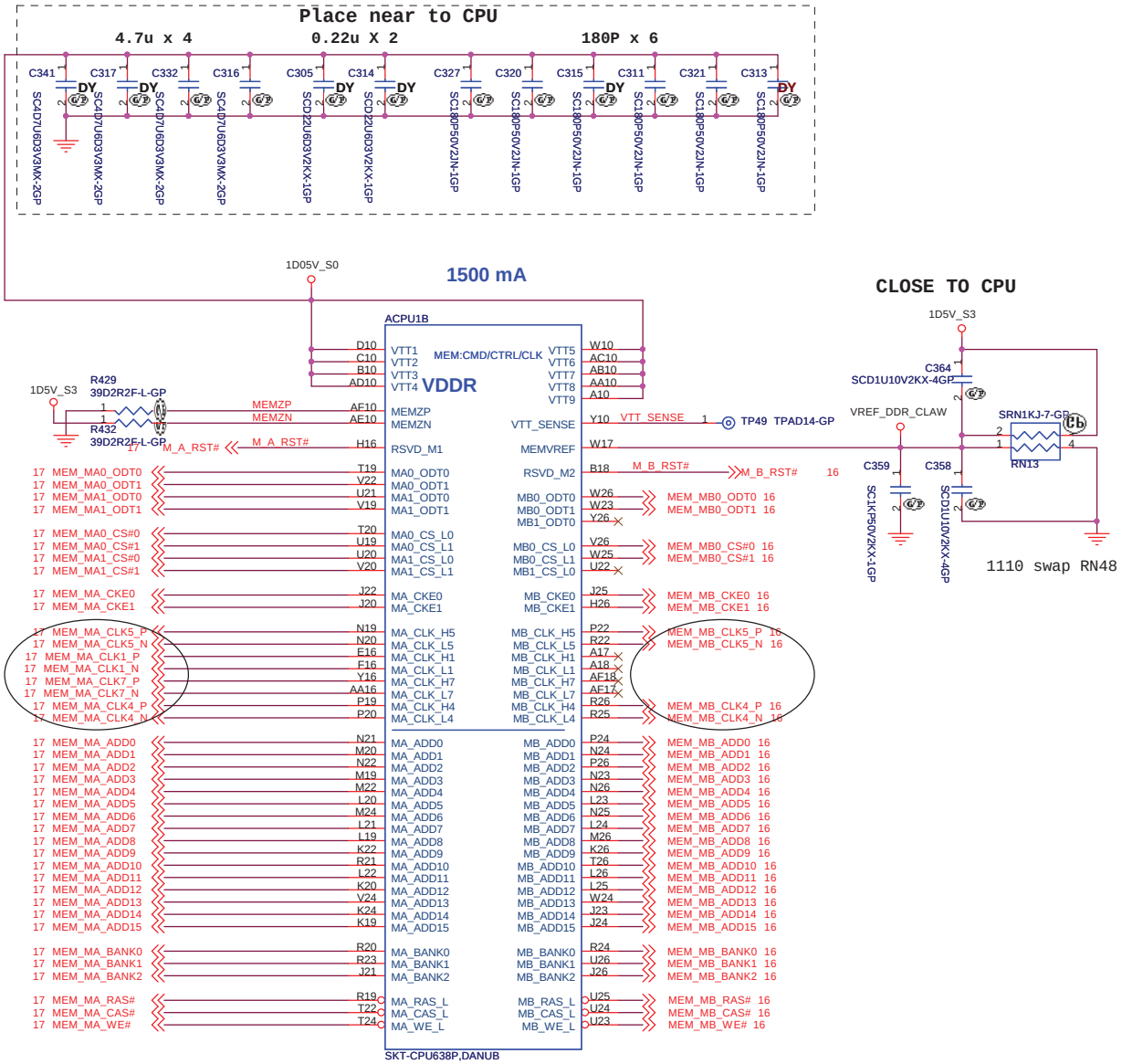


62.10055.111

SKT-BGA638H176

JE70-DN

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CPU HT LINK I/F (1/4)**
Size: A3	Document Number: JE70-DN
Rev: SB	
Date: Monday, March 01, 2010	Sheet 4 of 63



JE70-DN			
緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CPU_DDR (2/4)		
Size: A3	Document Number: JE70-DN	Rev: SB	
Date: Monday, March 01, 2010	Sheet 5 of 63		

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

SB_1218

S1G3&S1G4 not support LDTREQ_L(CPU_LDT_REQ#_CPU)

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

1105 modify Q8,R81,R375,C205

Near CPU PIN

1026 modify R364
1029 delete R364 and add RN127,R946

SB_1218

1102 swap these nets

1026 modify RN42

CPU exceeds to 125℃

Cloce To CPU

For HDT DBG

-1_0211

1026 modify RN84,R612,R611
1029 delete R612

1105 modify R366

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L

differentially impedance 80

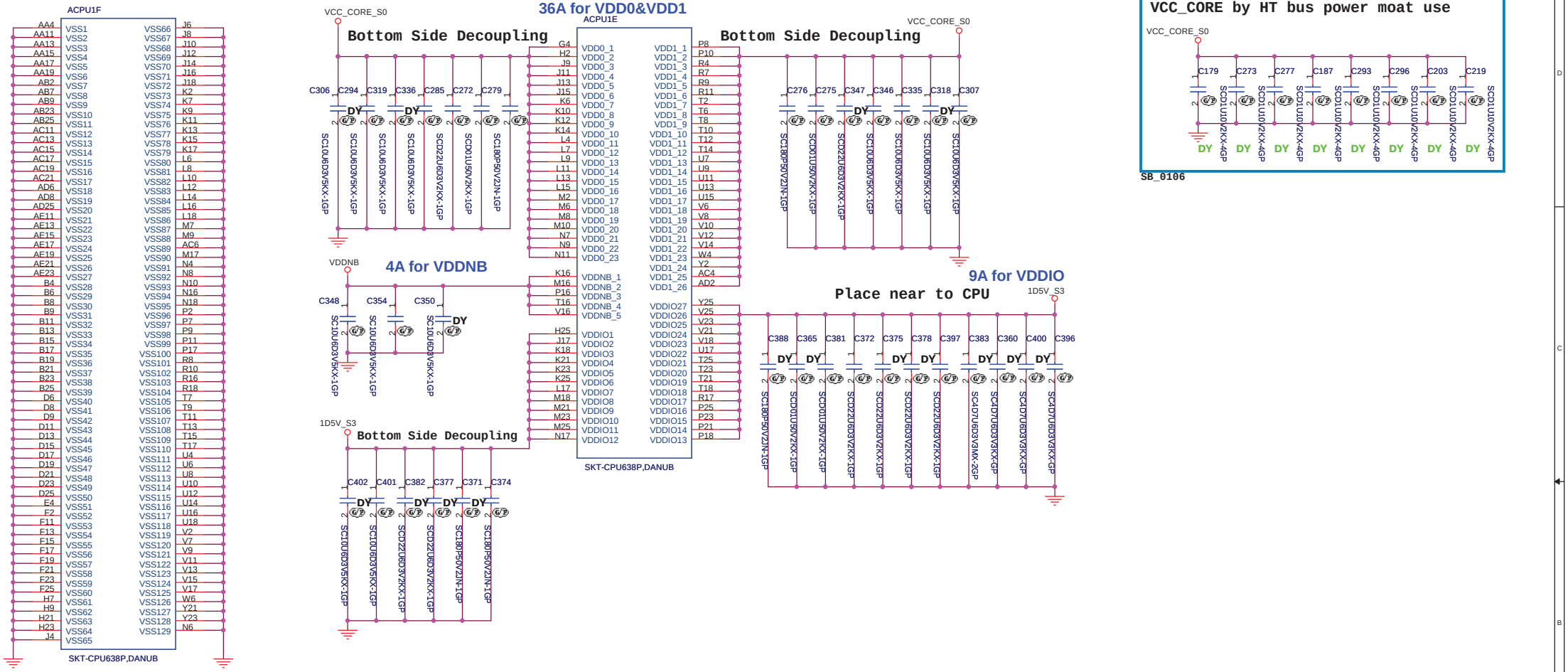
ACPU1D

SKT-CPU638P,DANUB

HDT Connectors

SMC-CONN26A-FP

JE70-DN	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_Control&Debug_(3/4)
Size	A3
Document Number	JE70-DN
Rev	SB
Date:	Tuesday, February 23, 2010
Sheet	6 of 63



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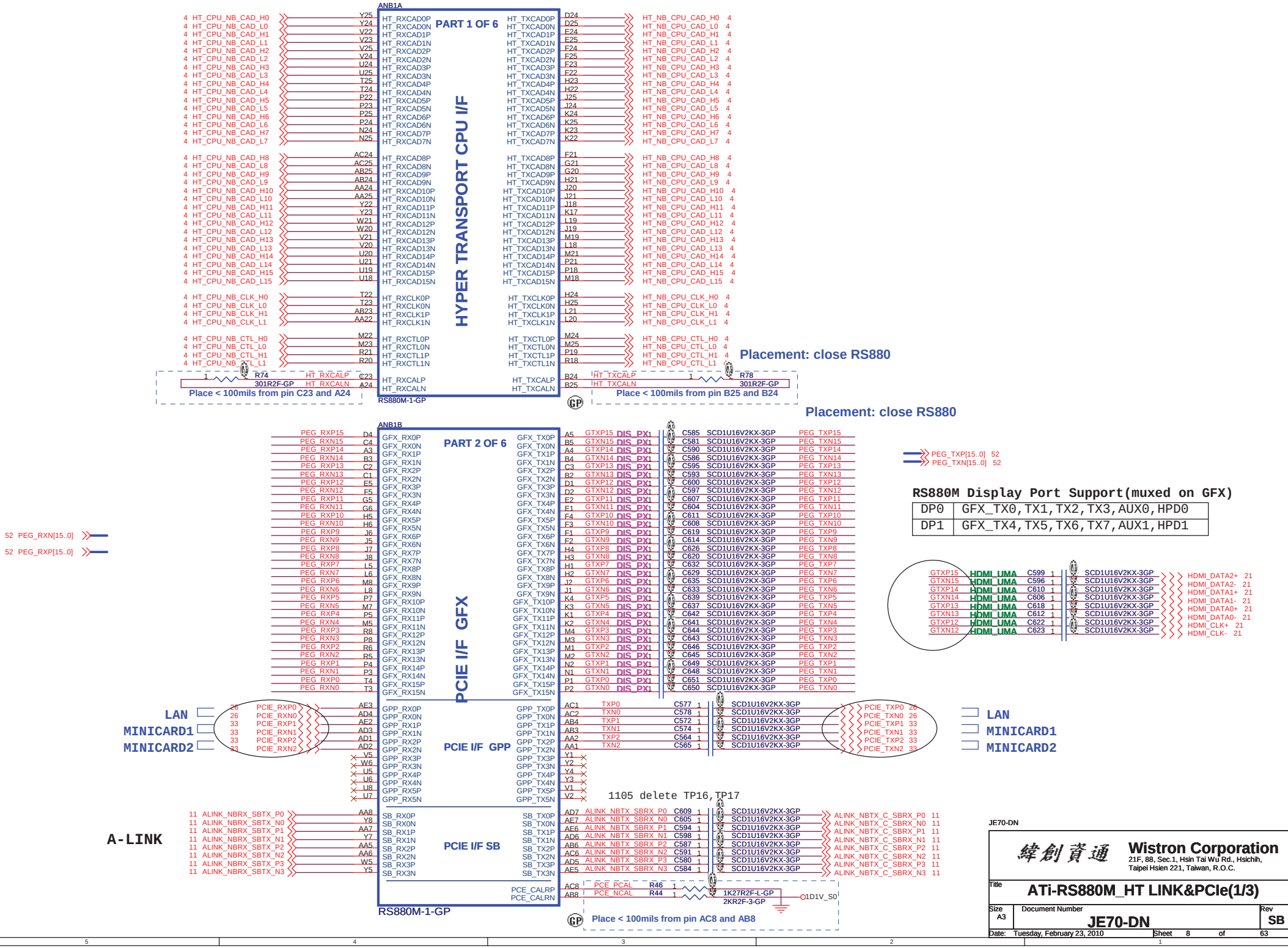
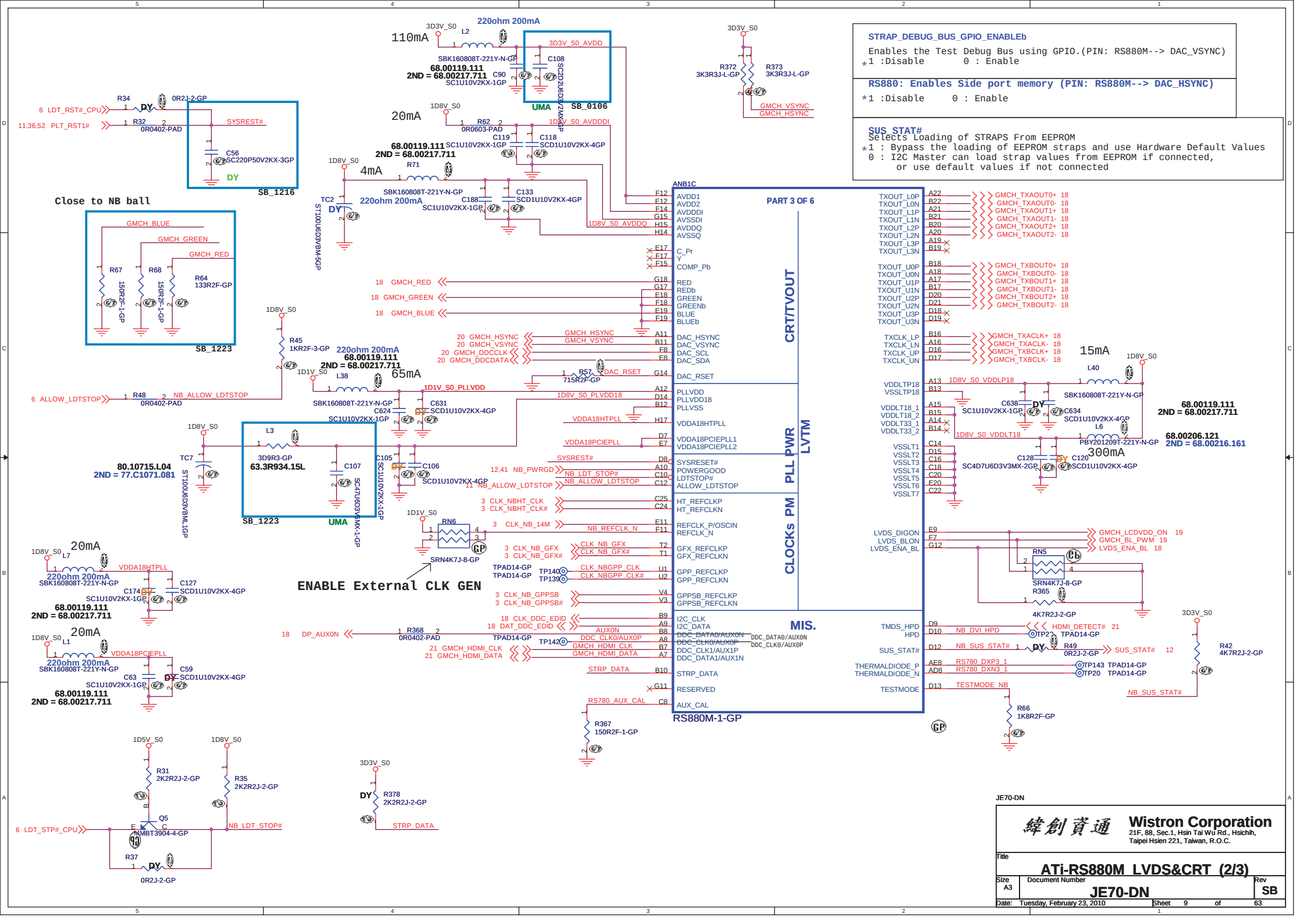
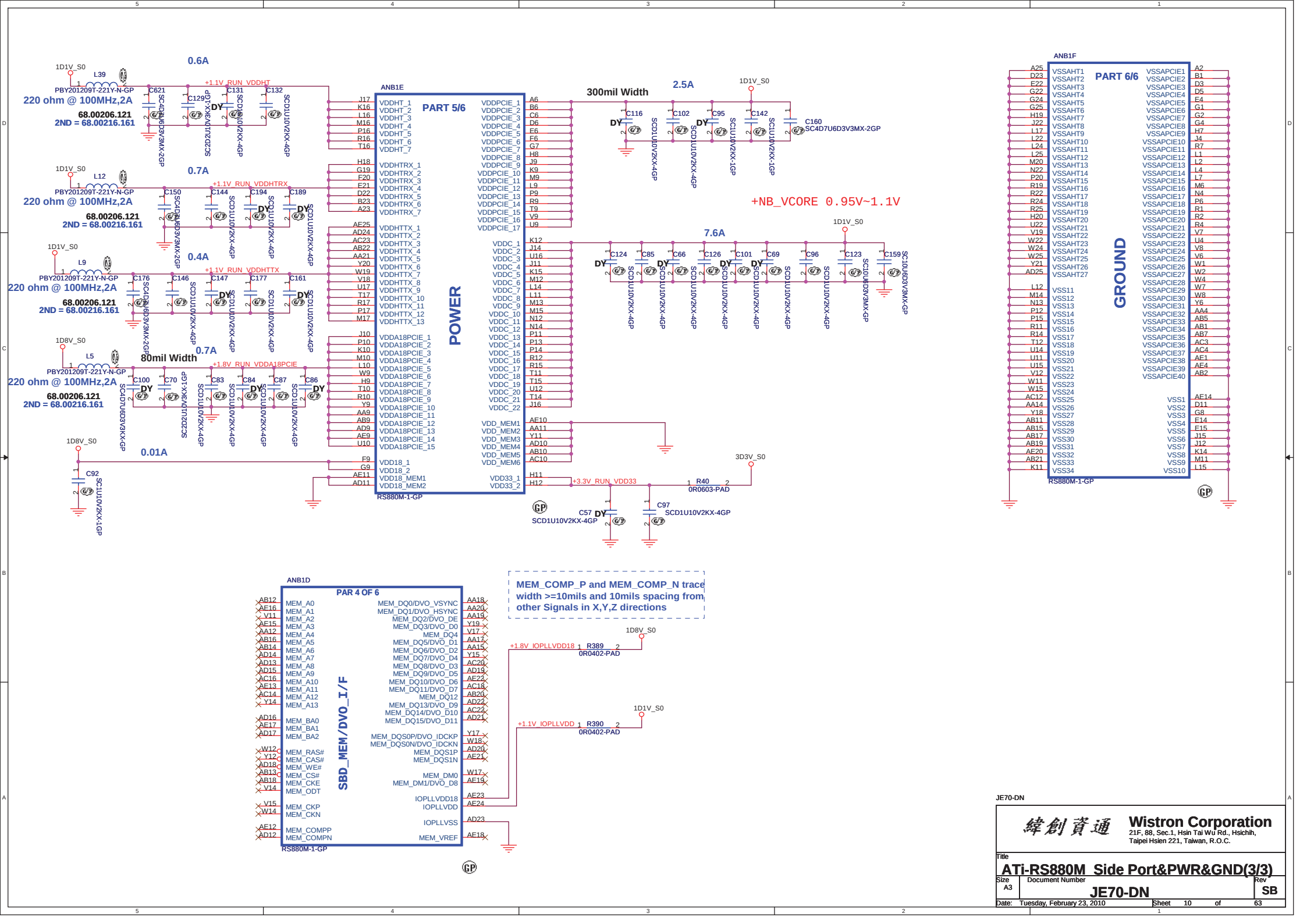
Title: CPU_Power_(4/4)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Wednesday, January 06, 2010 Sheet 7 of 63


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS880M-1-GP
Placement: close RS880
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS880M-1-GP
Placement: close RS880
RS880M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
LAN
MINICARD1
MINICARD2
A-LINK
1105 delete TP16,TP17
Place < 100mils from pin AC8 and AB8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M_HT LINK&PCIe(1/3)
JE70-DN
Size A3
Rev SB
Date: Tuesday, February 23, 2010
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> DAC_VSYNC)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (PIN: RS880M--> DAC_HSYNC)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
ENABLE External CLK GEN
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
CLOCKs PM
MIS.
RS880M-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JE70-DN
ATi-RS880M LVDS&CRT (2/3)
Size A3
Document Number JE70-DN
Rev SB
Date: Tuesday, February 23, 2010
Sheet 9 of 63



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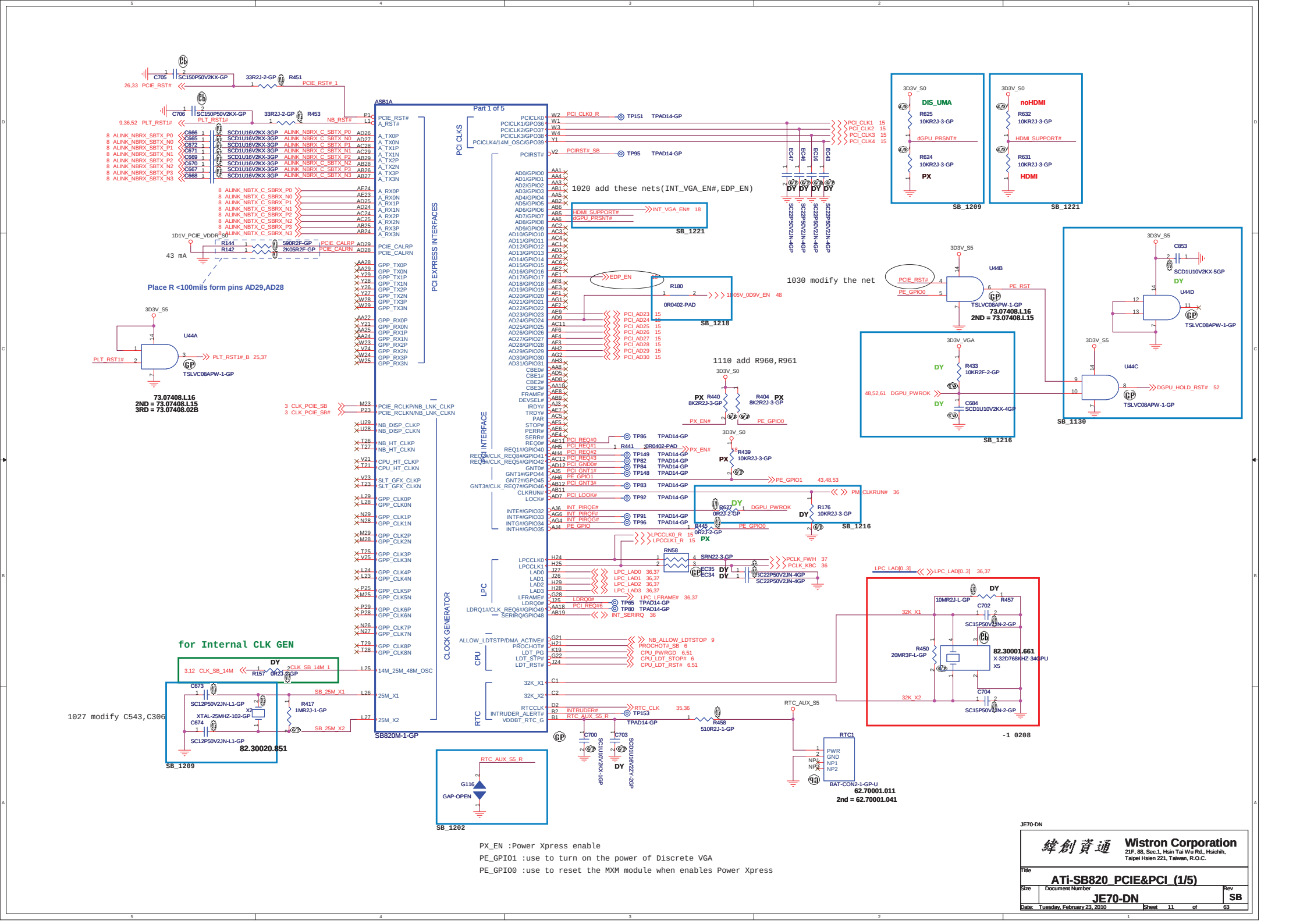
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M Side Port&PWR&GND(3/3)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 10 of 63



JE70-DN

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Title: ATi-SB820_PCIE&PCI_(1/5)

Size	Document Number	Rev
	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 11 of 63

1D8V_S0
3D3V_S0 R158 1 NB_PWRGD 300R2J-4-GP
R182 1 SUS_STAT# 4K7R2J-2-GP

9,41 NB_PWRGD R168 2 0R0402-PAD 1 NB_PWRGD_R

3D3V_S5
DY RN16 1 2 3 4 8 7 6 5 USB_OC#5 USB_OC#4 USB_OC#1 USB_OC#0 SRN2K2J-4-GP
DY RN60 1 2 3 4 8 7 6 5 SB_TEST2 SB_TEST1 SB_TEST0 USB_OC#2 SRN2K2J-4-GP
R179 1 DY 10KR2J-3-GP USB_OC#3
R196 1 DY 10KR2J-3-GP ICH_PME#
R185 1 10KR2J-3-GP PCIE_WAKE#
R186 1 DY 10KR2J-3-GP SMB_ALERT#
RN62 8 7 6 5 1 2 3 4 ECSCI# 1 PM_SLP_S5# PM_SLP_S3# ECSW# SRN10KJ-6-GP

3D3V_S0 R410 1 DY 10KR2J-3-GP ECSMI# KBC
Reference Datashht

Close to SB820

28 ACZ_BITCLK R188 1 33R2J-2-GP
15 ACZ_SDATAOUT_R
28 ACZ_SDATAOUT R452 1 33R2J-2-GP
28 ACZ_SDATAIN0
28 ACZ_SYNC RN61 SRN33J-5-GP 4 3 2 GP
28 ACZ_RST#
R456 10KR2J-3-GP DY EC15 SC12P50V2JN-3GP DY EC45 SC12P50V2JN-3GP DY EC48 SC12P50V2JN-3GP DY EC49 SC12P50V2JN-3GP DY R187 10KR2J-3-GP

3D3V_S5 3D3V_S0
RN63 SRN2K2J-2-GP
33 SMB_CLK
33 SMB_DATA
3,16,17 SMBC0_SB
3,16,17 SMBD0_SB
C309 SC100P50V2JN-3GP DY C312 SC100P50V2JN-3GP DY
SB_0106

TP99 1 ICH_PME# J2
TP155 1 RI# K1
TP102 1 S2# D3
29,35,36,41,43,46,47,48 PM_SLP_S3# PM_SLP_S3# F1
36,46 PM_SLP_S5# PM_SLP_S5# H1
36,51 PM_PWRBTN# F2
41 SB_PWRGD H5
9 SUS_STAT# SUS_STAT# G6
SB_TEST0 B3
SB_TEST1 C4
SB_TEST2 F6
36 KA20GATE AD21
36 KBRCIN# AE21
36 ECSC#_1 K2
ECSMI# KBC J29
TPAD14-GP TP157 GEVENT5# H2
TPAD14-GP TP108 SYS_RST# J1
26,33 PCIE_WAKE# H6
TPAD14-GP TP106 EC_TMR F3
SMB_ALERT# J6
NB_PWRGD_R AC19
43 PM_RSMRST# G1

TPAD14-GP TP81 GPIO6 AD19
TPAD14-GP TP66 GPIO4 AA16
No HDMI function
TPAD14-GP TP78 GPIO39 AB21 AC18 AF20 AE19 AF19
28 ACZ_SPKR
SMBC0_SB AD22
SMBD0_SB AE22
SMB_CLK F5
SMB_DATA F4
TPAD14-GP TP79 CLK_REQ1# AH21
TPAD14-GP TP150 IR_LED# AB18
TPAD14-GP TP146 SMARTVOLT2 F1
TPAD14-GP TP100 DDR3_RST# AJ21 H4
D5 D7 G5 K3
3,11 CLK_SB_14M DY R438 1 0R2J-2-GP 2 CLK_SB_14M_R AA20

36 ECSW# H3 D1
TPAD14-GP TP101 USB_OC#5 E4
TPAD14-GP TP105 USB_OC#4 D4
25 USB_OC#3 USB_OC#3 E8
25 USB_OC#2 USB_OC#2 E7
TPAD14-GP TP90 USB_OC#1 E7
25 USB_OC#0 USB_OC#0 F8

ACZ_BIT_CLK M3
ACZ_SDATAOUT_R N1
TPAD14-GP TP152 ACZ_SDIN1 M2
TPAD14-GP TP160 ACZ_SDIN2 M1
TPAD14-GP TP103 ACZ_SDIN3 M4
ACZ_SYNC_R N2
ACZ_RST#_R P2

3D3V_S5 RN18 1 2 3 4 8 7 6 5 GP SRN10KJ-6-GP
T1 T4 L6 L5 T9 U1 U3 T2 U2 T5 V5 P5 M5 P9 T7 P7 M7 P4 M9 V7

3D3V_S5 R181 1 10KR2J-3-GP 2
TPAD14-GP TP67 E23
TPAD14-GP TP50 E24
F21
G29
D27
F28
F29
E27

ASB1D
PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
Part 4 of 5
ACPI / WAKE UP EVENTS
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXT#
GPIO
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL
SB820M-1-GP

USBCLK/14M_25M_48M_OSC A10
USB_RCOMP G19 USB_PCOMP 1 R169 11K8R2F-GP 1%
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
CLK48_USB 3
R177 1 DY CLK48_USB_R2 1 C367 10KR2J-3-GP SC10P50V2JN-4GP
Place these close SB820
USB_FSD1P/GPIO186 J10
USB_FSD1N H11
USB_FSD0P/GPIO185 H9
USB_FSD0N J8
USB MISC
USB_HSD13P B12
USB_HSD13N A12
USB_HSD12P F11
USB_HSD12N E11
USBPP12 33
USBPN12 33
USB_HSD11P E14
USB_HSD11N E12
USB_HSD10P J12
USB_HSD10N J14
USB_HSD9P A13
USB_HSD9N B13
USBPP9 19
USBPN9 19
USB_HSD8P D13
USB_HSD8N C13
USB_HSD7P G12
USB_HSD7N G14
USBPP7 24
USBPN7 24
USB_HSD6P G16
USB_HSD6N G18
USBPP6 25
USBPN6 25
USB_HSD5P D16
USB_HSD5N C16
USBPP5 25
USBPN5 25
USB_HSD4P B14
USB_HSD4N A14
USBPP4 25
USBPN4 25
USB_HSD3P E18
USB_HSD3N E16
USBPP3 25
USBPN3 25
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17
USB_HSD1N A17
USBPP1 33
USBPN1 33
USB_HSD0P A16
USB_HSD0N B16
USBPP0 25
USBPN0 25
USB 2.0

1020 modify these nets
1105 modify these nets

OCP3#
OCP2#
OCP0#

USB	
Pair	Device
12	MINI2 CARD
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	USB4
2	NC
1	MINI1 CARD
0	USB1

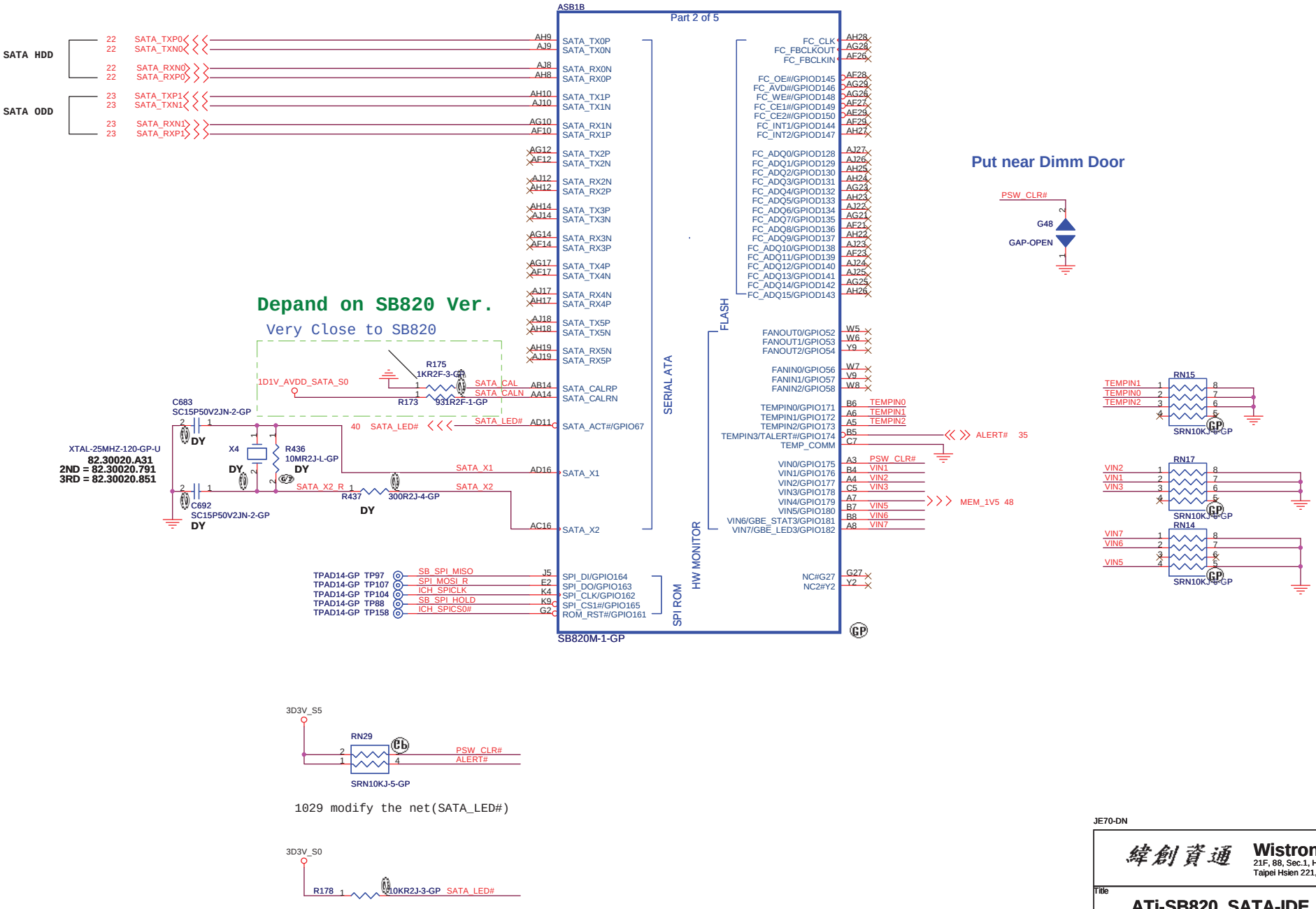
RN59 1 2 3 4 8 7 6 5 GP SRN10K-5-GP
SCL2/GPIO193 D25
SDA2/GPIO194 F23
SCL3_LV/GPIO195 B26
SDA3_LV/GPIO196 E26
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22
EC_PWM3/EC_TIMER3/GPIO200 E21
SB_GPO199 15
SB_GPO200 15
Strap Pin / define to use LPC or SPI ROM

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22
EMBEDDED CTRL

JE70-DN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820 USB&GPIO (2/5)
Size: A3 | Document Number: JE70-DN | Rev: SB
Date: Tuesday, February 23, 2010 | Sheet 12 of 63



JE70-DN

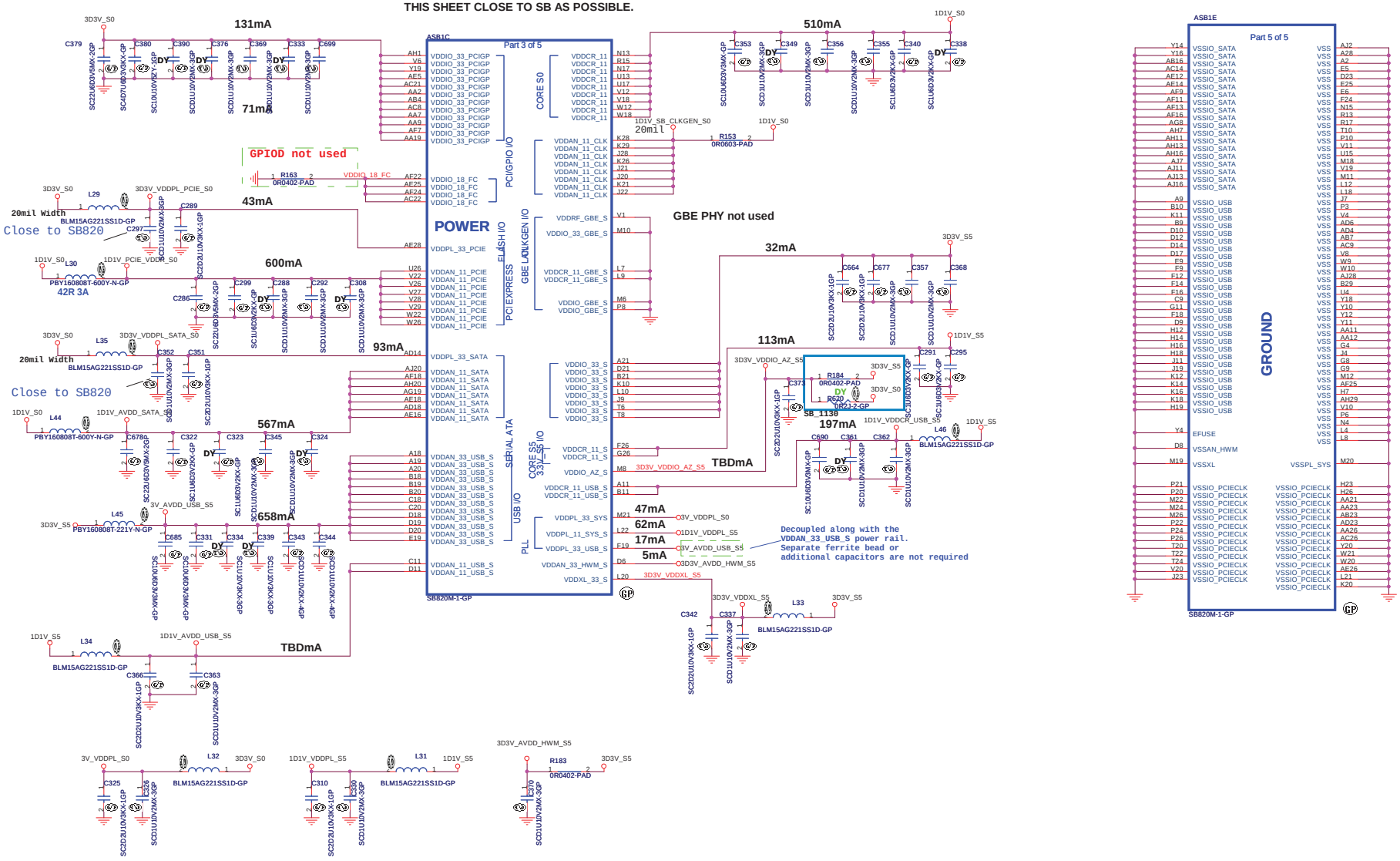
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820 SATA-IDE (3/5)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 13 of 63

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

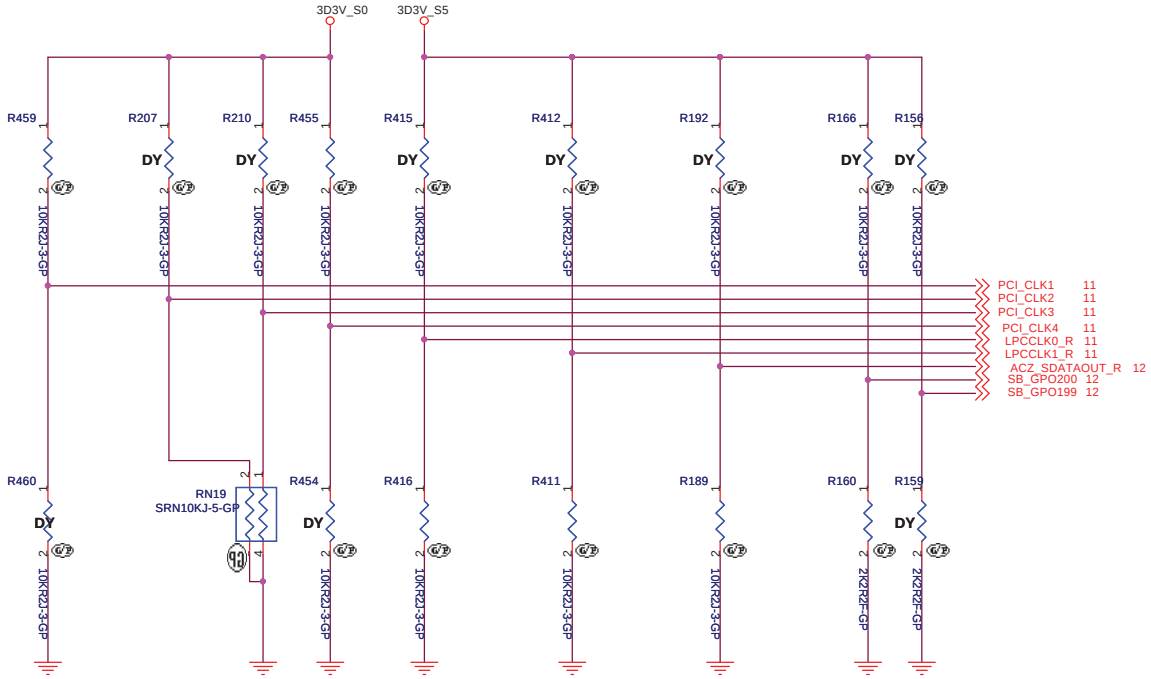


JE70-DN

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ATi-SB820_POWER&GND_(4/5)		
Size: Custom	Document Number: JE70-DN	Rev: SB
Date: Friday, February 12, 2010	Sheet 14 of 63	

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS

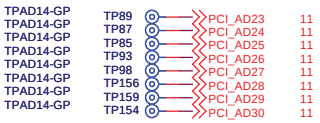


1118 modify R412,R411

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

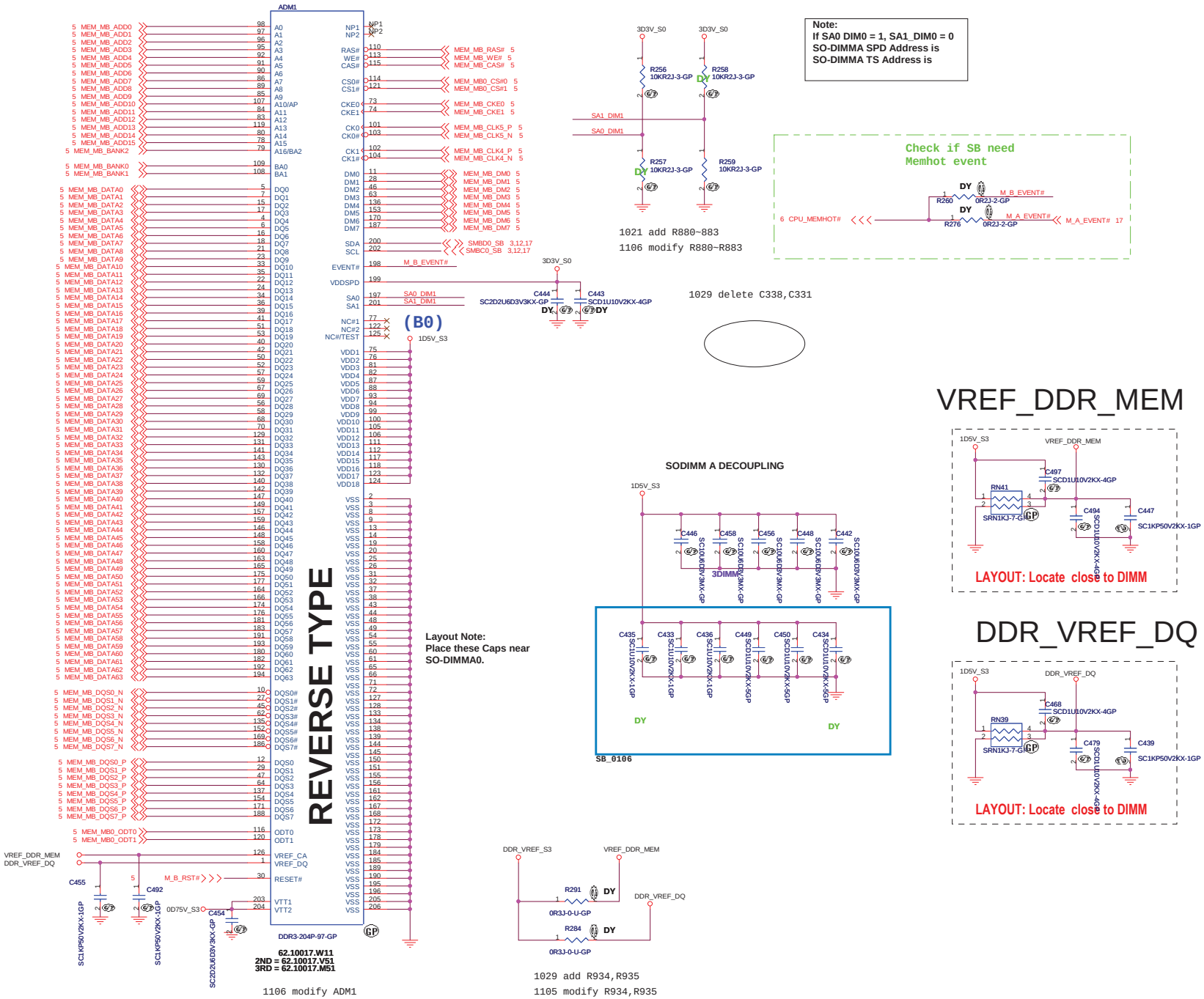
JE70-DN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820 STRAPPING (5/5)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 15 of 63



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Wistron Corporation
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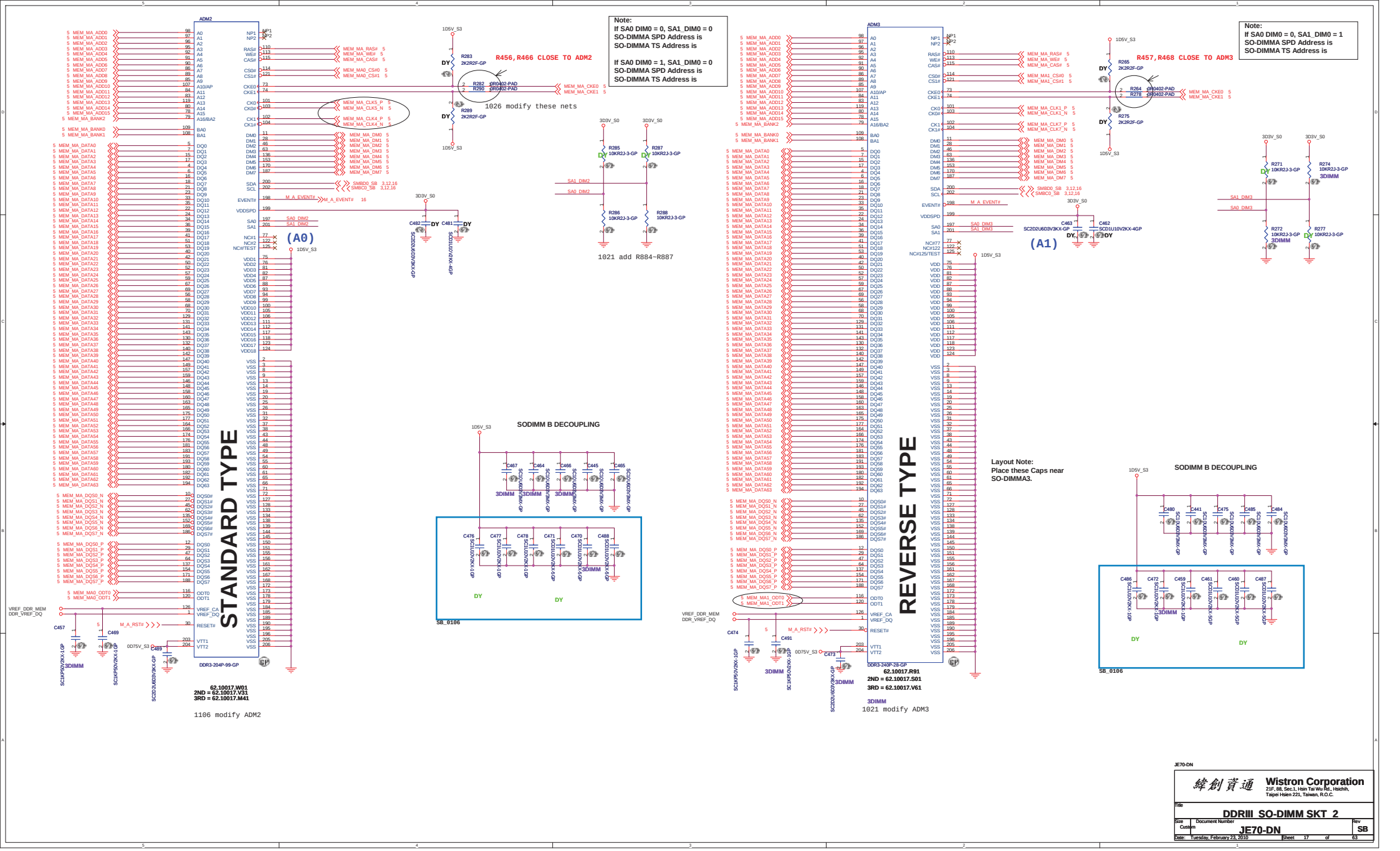
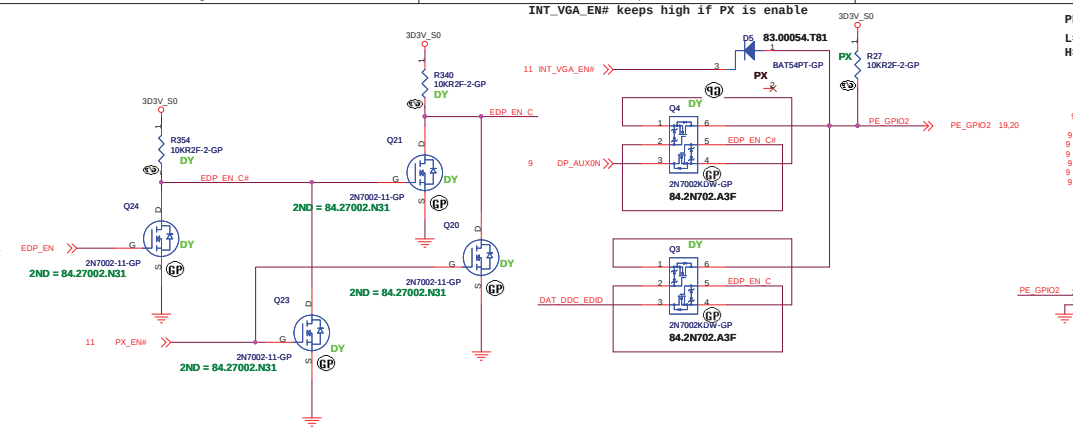
Taipei Hsien 221, Taiwan, R.O.C.

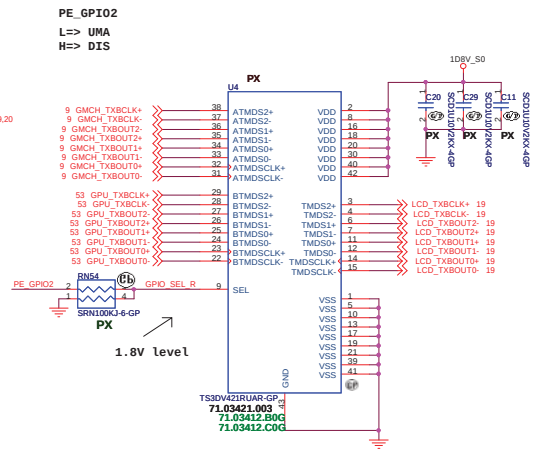
Title: DDRIII_SO-DIMM SKT_1

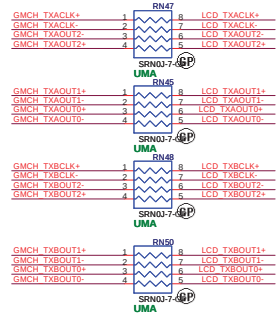
Size	Document Number	Rev
Custom	JE70-DN	SB

Date: Tuesday, February 23, 2010 Sheet 16 of 63


STANDARD TYPE
REVERSE TYPE
(A0)
(A1)
ADM2
ADM3
DDR3-204P-99-GP
DDR3-240P-28-GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is
SO-DIMMA TS Address is
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is
SO-DIMMA TS Address is
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is
SO-DIMMA TS Address is
R456,R466 CLOSE TO ADM2
R457,R468 CLOSE TO ADM3
1026 modify these nets
1021 add R884~R887
SODIMM B DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA3.
62.10017.W01
2ND = 62.10017.V31
3RD = 62.10017.M41
1106 modify ADM2
62.10017.R01
2ND = 62.10017.S01
3RD = 62.10017.V61
1021 modify ADM3
SB_0106
JE70-DN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII SO-DIMM SKT 2
JE70-DN
Date: Tuesday, February 23, 2010
Sheet 17 of 63



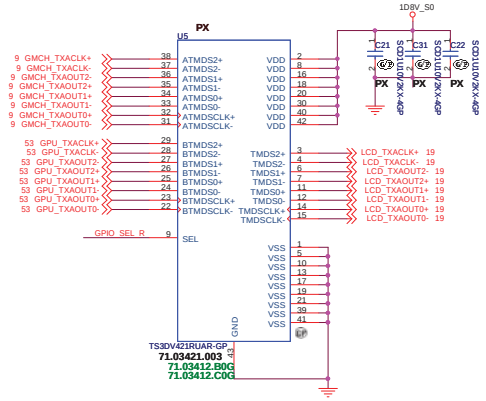


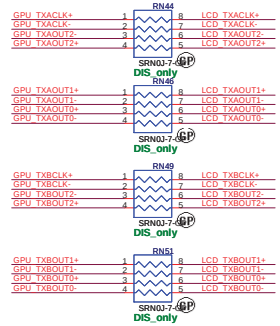


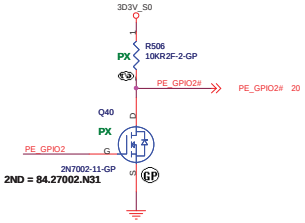
DISPLAY SUPPORT TABLE

	PX_EN#	DP_AUX0N EDP diabled	I2C_DATA EDP diabled	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP(LVDS,EDP,VGA,DP)
MXM only mode	1	X	X	1	MXM(LVDS,EDP,VGA,DP)
Power Express(muxed)	0	0/1	0/1	1	MXM/IGP(LVDS,EDP,VGA);MXM(DP)
Power Express(muxless)	0	X	X	0	IGP(LVDS,EDP,VGA,DP)

PX mode display device auto detection method:
VGA:I2C interface to NB
DP:HPD





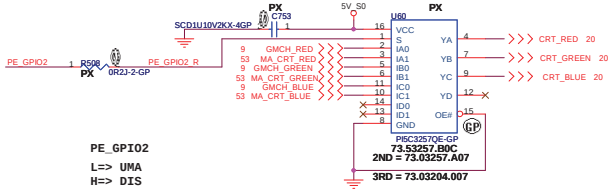


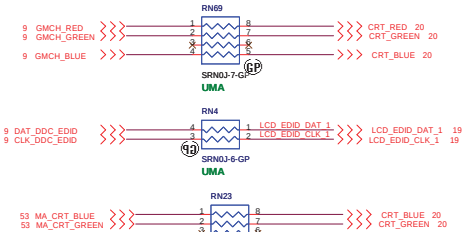
LVDS

Function	SEL
An to nB1	L
An to nB2	H

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



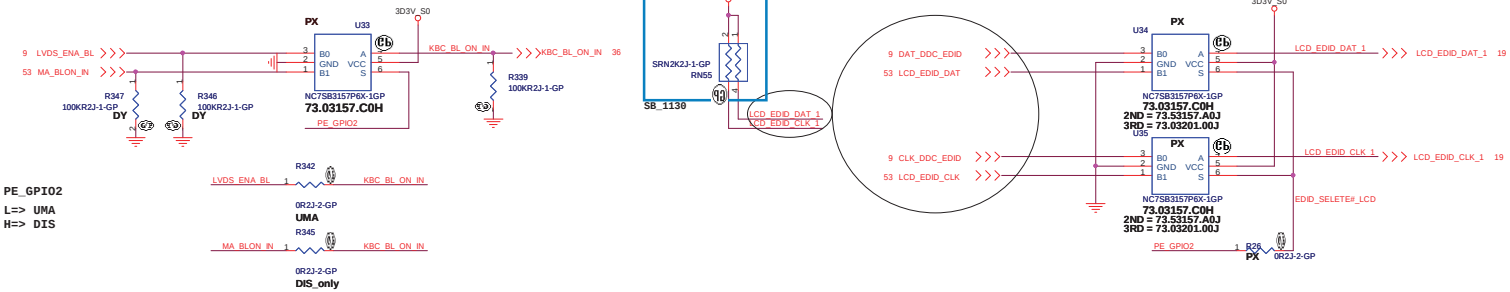


EDID

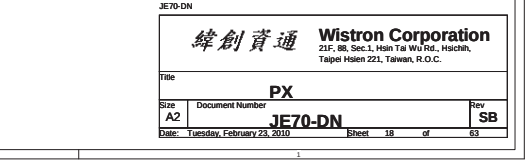
Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level



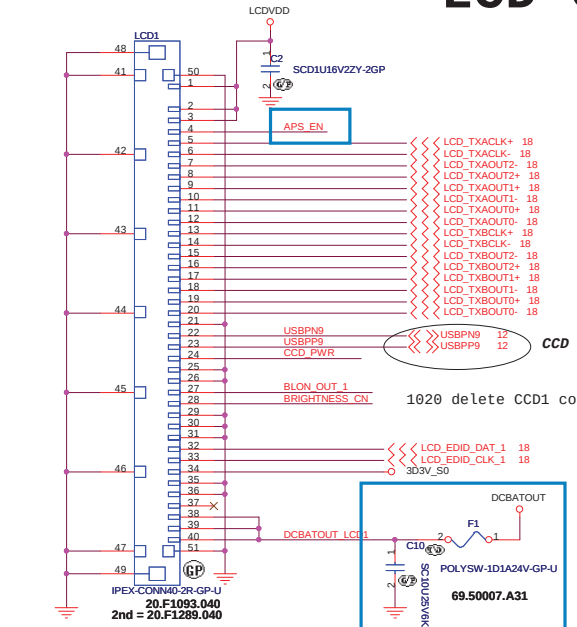
PE_GPIO2
L=> UMA
H=> DIS

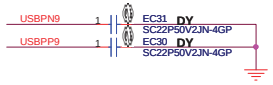


LCD CONN

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

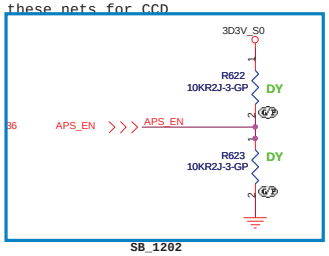
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

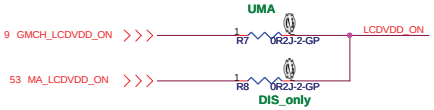


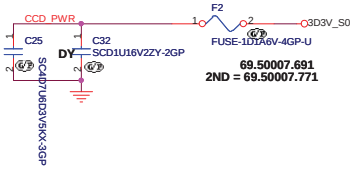


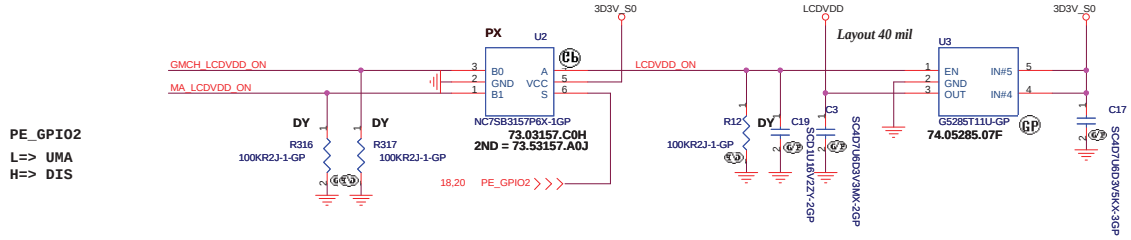
1029 add EC99,EC100

1020 delete CCD1 conn and modify these nets for CCD

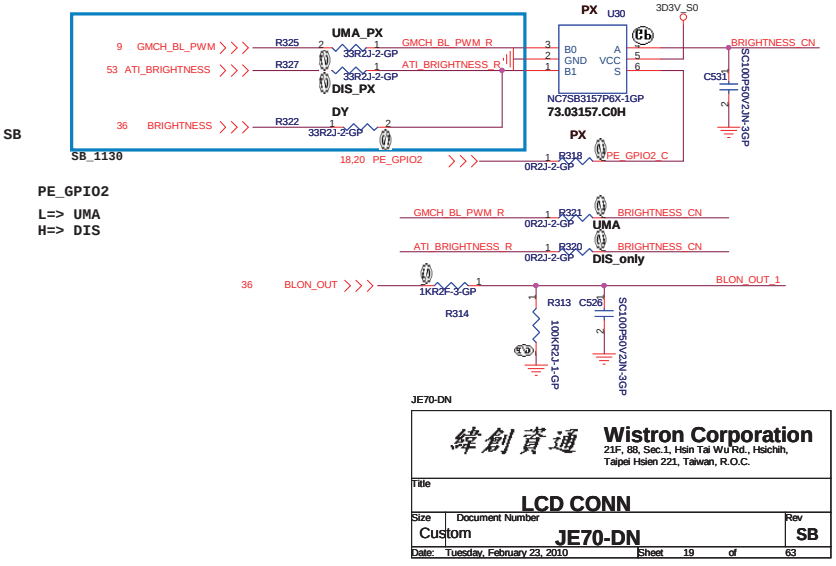








Reserve direct connector to KBC



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Title		
LCD CONN		
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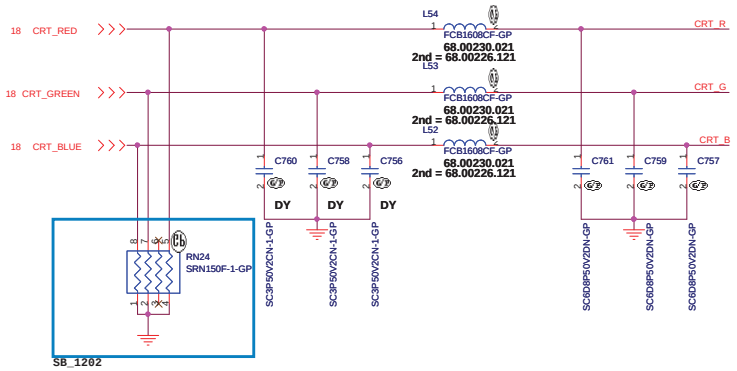
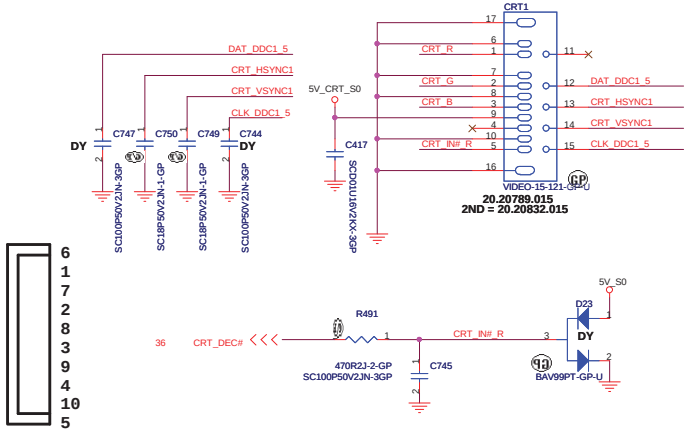
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

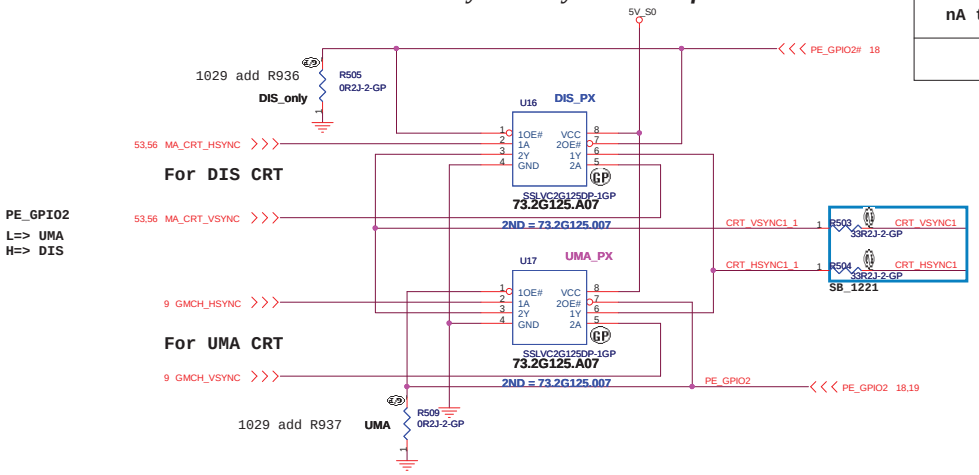
CRT I/F & CONNECTOR



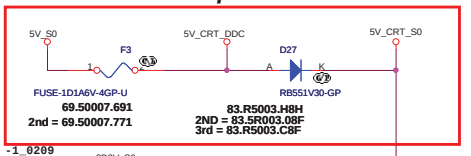
6 1 7 2 8 3 9 4 10 5

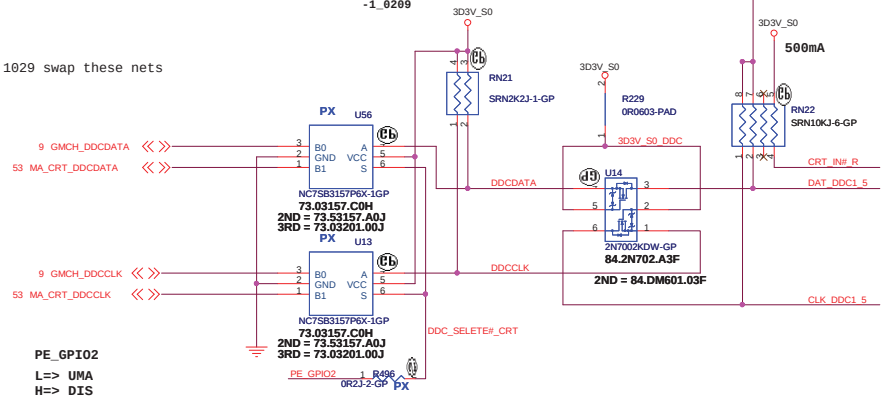
Hsync & Vsync level shift

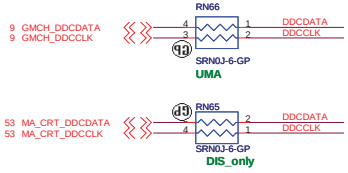
Function	OE#
nA to nY	L
X	H



DDC_CLK & DATA level shift







JE70-DN

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size | Document Number: JE70-DN | Rev: SB

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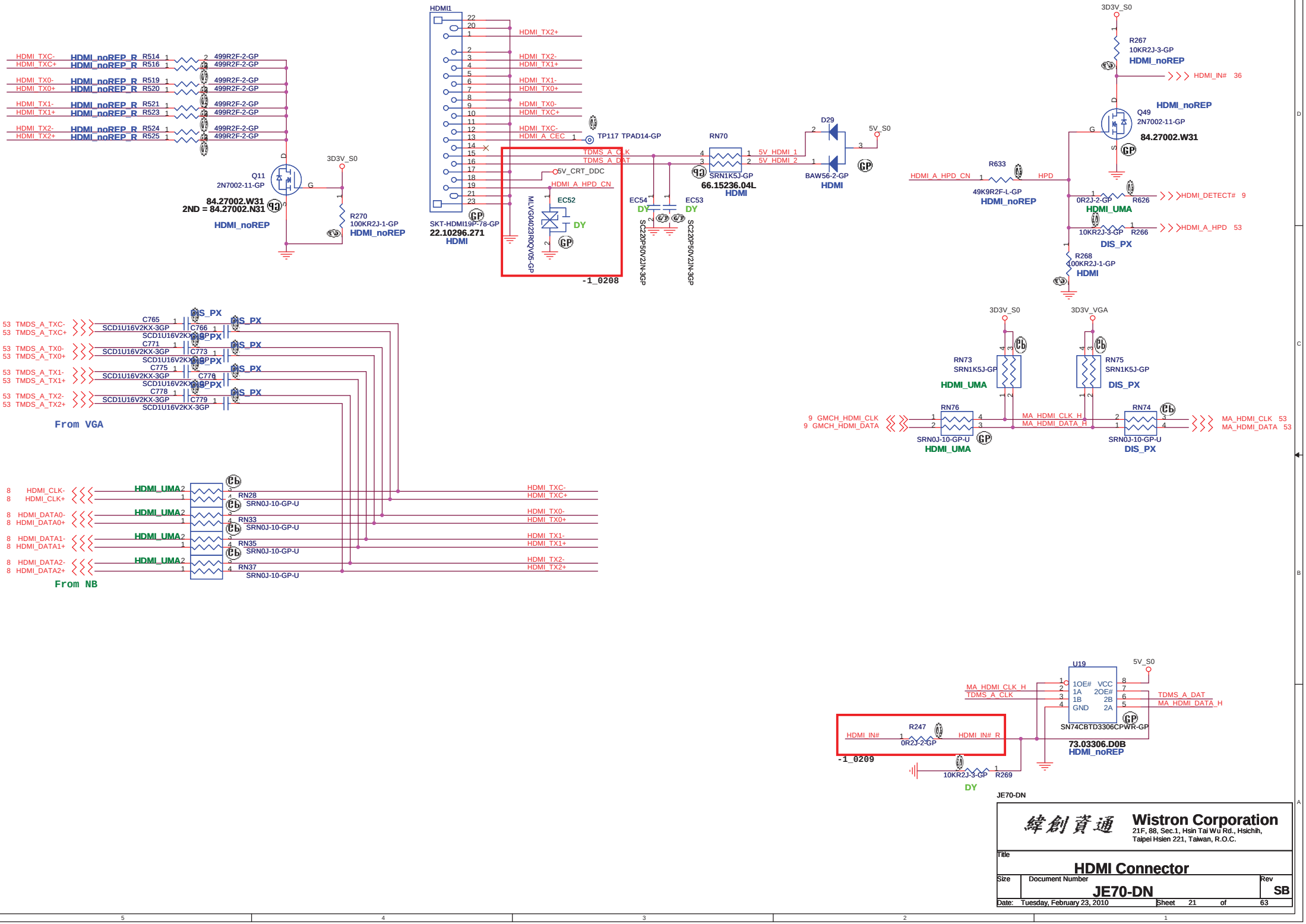
HDMI_TXC-
HDMI_TXC+
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
HDMI_noREP_R R514
HDMI_noREP_R R516
HDMI_noREP_R R519
HDMI_noREP_R R520
HDMI_noREP_R R521
HDMI_noREP_R R523
HDMI_noREP_R R524
HDMI_noREP_R R525
499R2F-2-GP
Q11
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
HDMI_noREP
3D3V_S0
R270
100KR2J-1-GP
HDMI_noREP
HDMI1
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP117 TPAD14-GP
TDMS_A_CLK
TDMS_A_DAT
5V_CRT_DDC
HDMI_A_HPD_CN
SKT-HDMI19P-78-GP
22.10296.271
HDMI
EC52
MLVG0402B200QV05-GP
DY
EC54
EC53
SC220P50V2JN-3GP
RN70
SRN1K5J-GP
66.15236.04L
HDMI
D29
BAW56-2-GP
HDMI
5V_S0
5V_HDMI_1
5V_HDMI_2
-1_0208
3D3V_S0
R267
10KR2J-3-GP
HDMI_noREP
HDMI_IN# 36
Q49
2N7002-11-GP
84.27002.W31
HDMI_noREP
R633
HDMI_A_HPD_CN
HPD
49K9R2F-L-GP
HDMI_noREP
0R2J-2-GP
R626
HDMI_UMA
HDMI_DETECT# 9
10KR2J-3-GP
R266
DIS_PX
HDMI_A_HPD 53
R268
100KR2J-1-GP
HDMI
53 TMDS_A_TXC-
53 TMDS_A_TXC+
53 TMDS_A_TX0-
53 TMDS_A_TX0+
53 TMDS_A_TX1-
53 TMDS_A_TX1+
53 TMDS_A_TX2-
53 TMDS_A_TX2+
C765
C766
C771
C773
C775
C776
C778
C779
SCD1U16V2KX-3GP
SCD1U16V2KX-3GPPX
S_PX
From VGA
3D3V_S0
3D3V_VGA
RN73
SRN1K5J-GP
HDMI_UMA
RN75
SRN1K5J-GP
DIS_PX
RN76
RN74
SRN0J-10-GP-U
9 GMCH_HDMI_CLK
9 GMCH_HDMI_DATA
MA_HDMI_CLK_H
MA_HDMI_DATA_H
MA_HDMI_CLK 53
MA_HDMI_DATA 53
8 HDMI_CLK-
8 HDMI_CLK+
8 HDMI_DATA0-
8 HDMI_DATA0+
8 HDMI_DATA1-
8 HDMI_DATA1+
8 HDMI_DATA2-
8 HDMI_DATA2+
HDMI_UMA
RN28
RN33
RN35
RN37
SRN0J-10-GP-U
From NB
U19
5V_S0
SN74CBTD3306CPWR-GP
73.03306.D0B
HDMI_noREP
R247
0R2J-2-GP
HDMI_IN#
HDMI_IN#_R
-1_0209
10KR2J-3-GP
R269
DY
JE70-DN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
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Date: Tuesday, February 23, 2010
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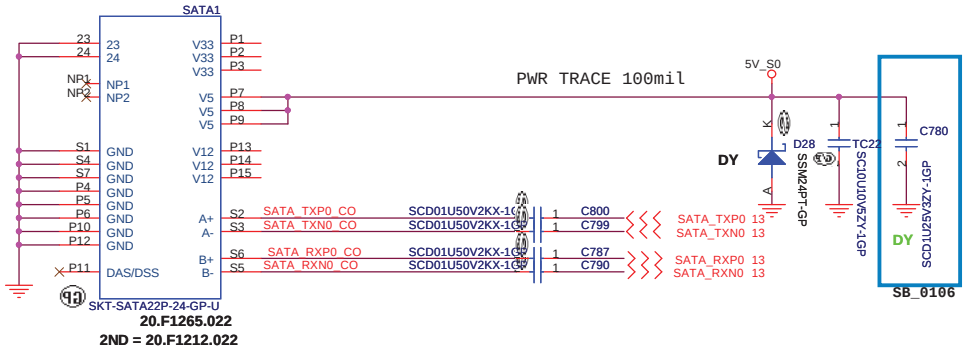
SATA Connector



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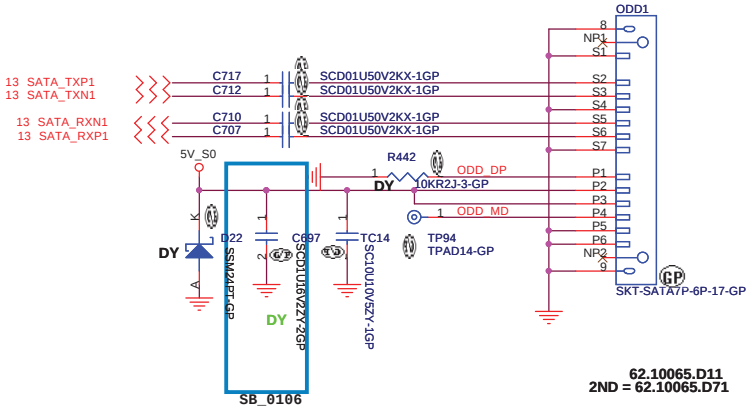
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD		
Size	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet 22 of 63	

ODD Connector



JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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ODD		
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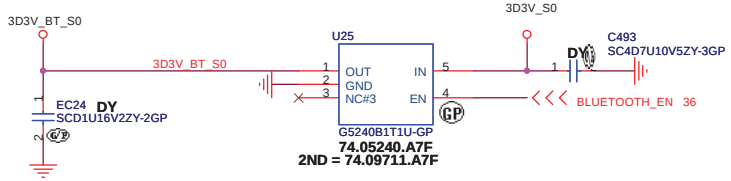
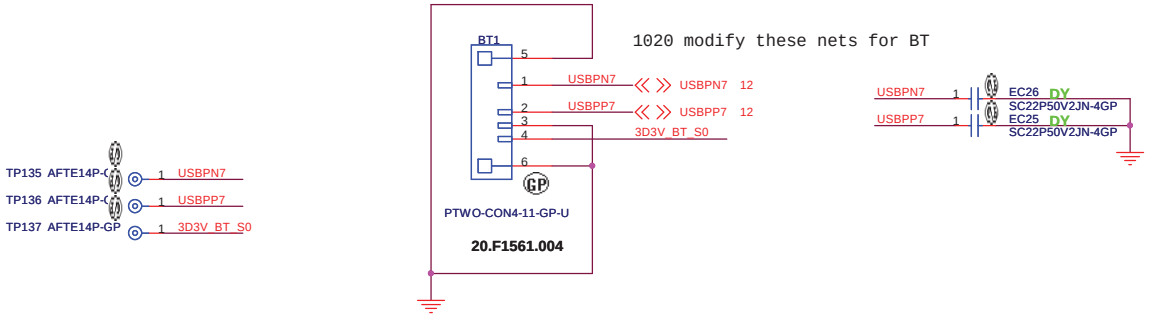
BLUETOOTH MODULE

1.5A / High Active Voltage 2V





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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**BLUETOOTH**
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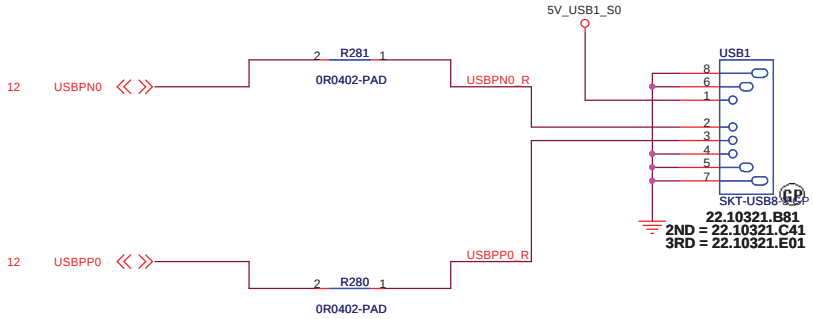

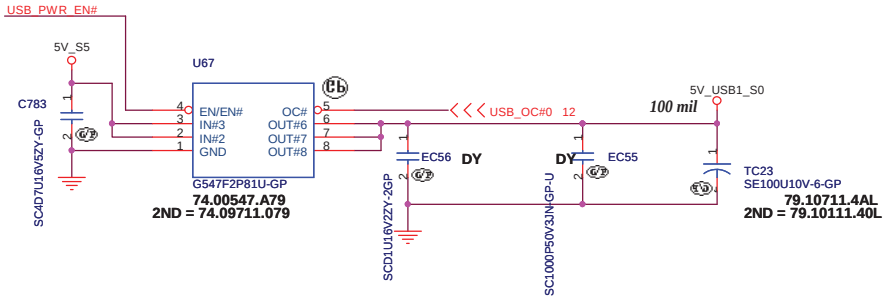

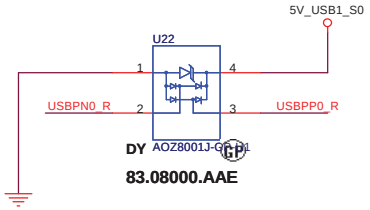

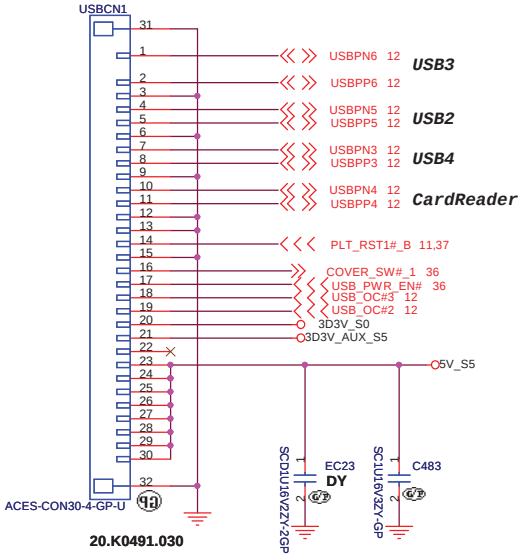

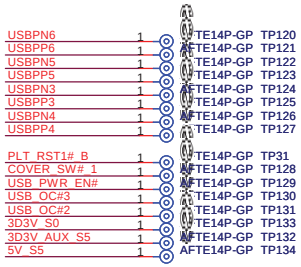

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Title	**USB**	
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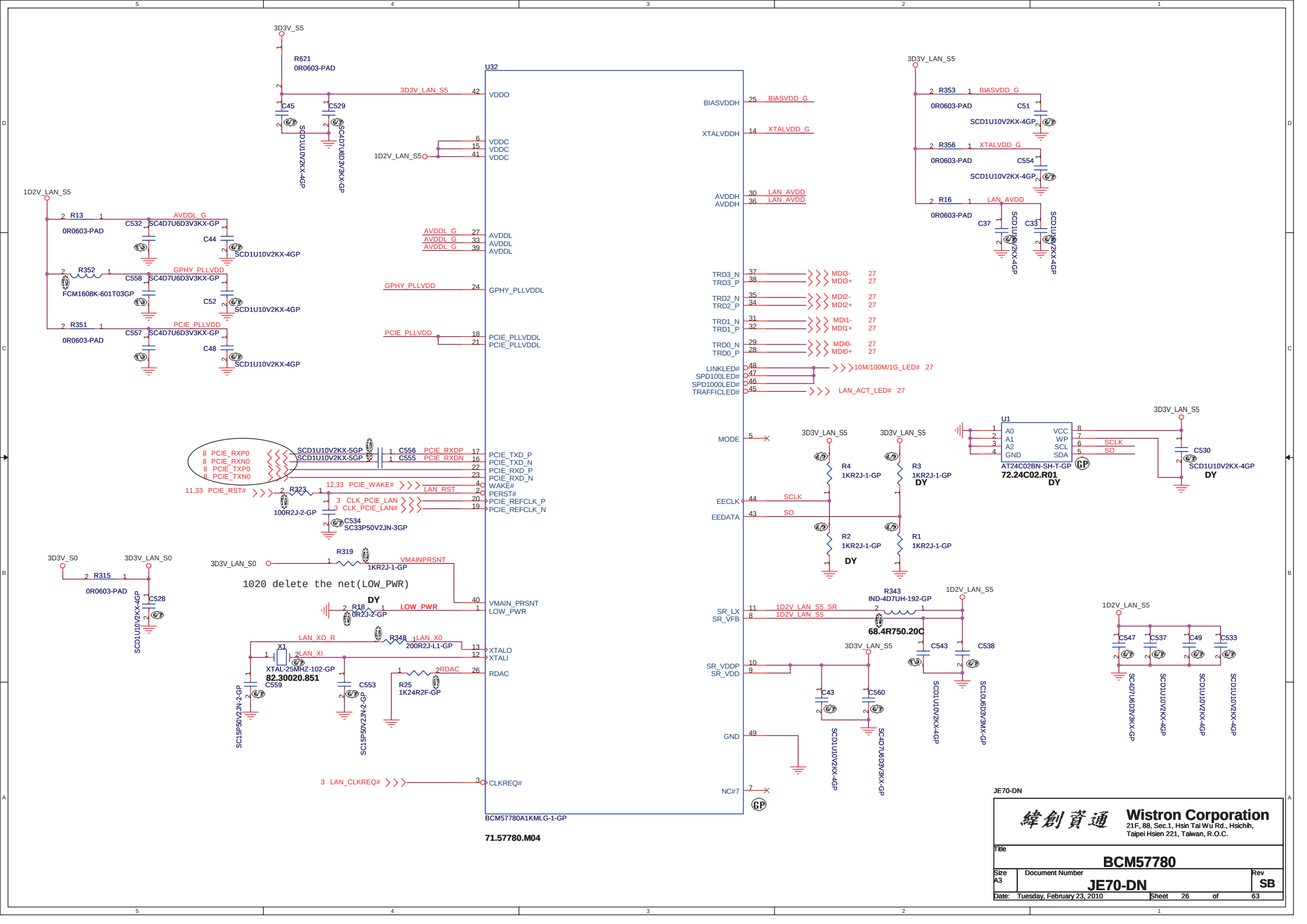
U32
BCM57780A1KMLG-1-GP
71.57780.M04
1020 delete the net(LOW_PWR)
DY
1D2V_LAN_S5
3D3V_LAN_S5
3D3V_S5
3D3V_S0
3D3V_LAN_S0
VDDO
VDDC
AVDDL
GPHY_PLVDDL
PCIE_PLLVDDL
BIASVDDH
XTALVDDH
AVDDH
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
MODE
EECLK
EEDATA
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
NC#7
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
CLKREQ#
XTALO
XTALI
RDAC
VMAIN_PRSNT
LOW_PWR
R621
0R0603-PAD
R13
R352
R351
R323
R319
R315
R18
R348
R25
1K24R2F-GP
R353
R356
R16
R4
R3
R2
R1
1KR2J-1-GP
R343
IND-4D7UH-192-GP
68.4R750.20C
100R2J-2-GP
200R2J-L1-GP
0R2J-2-GP
FCM1608K-601T03GP
XTAL-25MHZ-102-GP
82.30020.851
C45
C529
C532
C44
C558
C52
C557
C48
C528
C559
C553
C556
C555
C534
SC33P50V2JN-3GP
C51
C554
C37
C33
C530
C543
C538
C547
C537
C49
C533
C43
C560
U1
AT24C02BN-SH-T-GP
72.24C02.R01
SCD1U10V2KX-4GP
SCD1U10V2KX-5GP
SC4D7U6D3V3KX-GP
SC1U6D3V3MX-GP
SC15P50V2JN-2GP
SCLK
SO
PCIE_RXP0
PCIE_RXN0
PCIE_TXP0
PCIE_TXN0
PCIE_RST#
PCIE_WAKE#
LAN_RST
CLK_PCIE_LAN
CLK_PCIE_LAN#
LAN_CLKREQ#
LAN_XO_R
LAN_XI
LAN_X0
LAN_AVDD
BIASVDD_G
XTALVDD_G
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
10M/100M/1G_LED#
LAN_ACT_LED#
1D2V_LAN_S5_SR
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BCM57780
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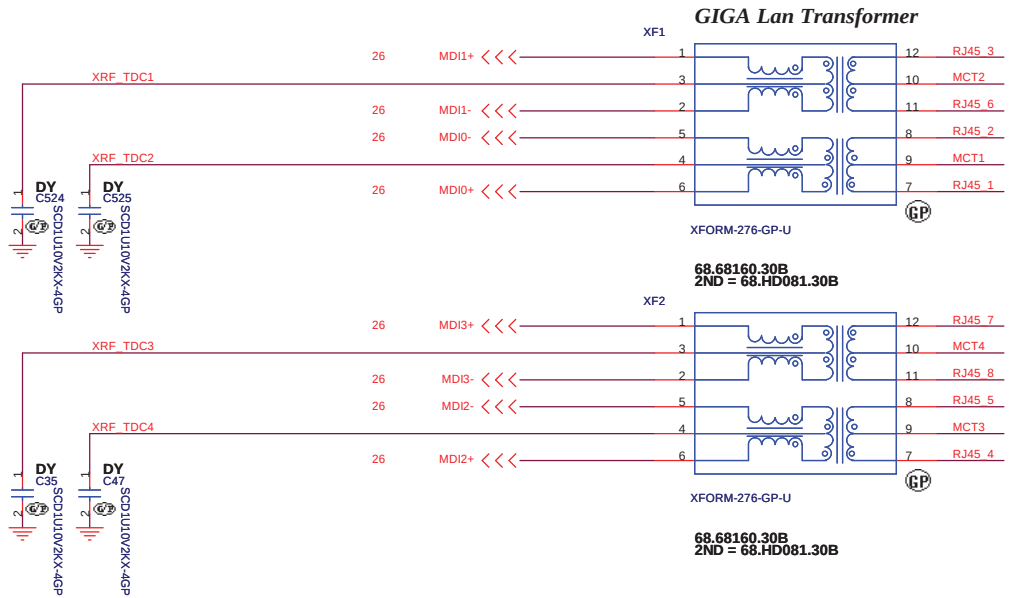
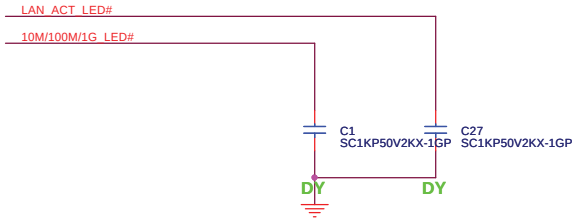
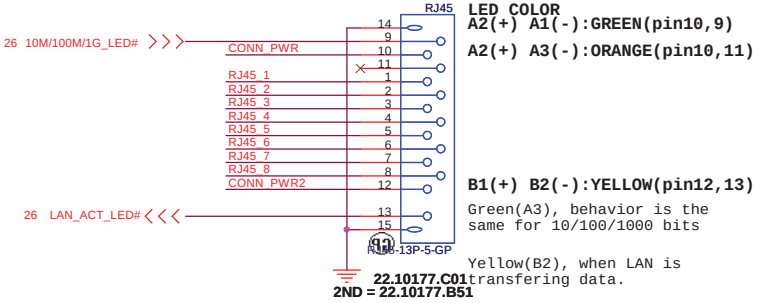
LAN Connector

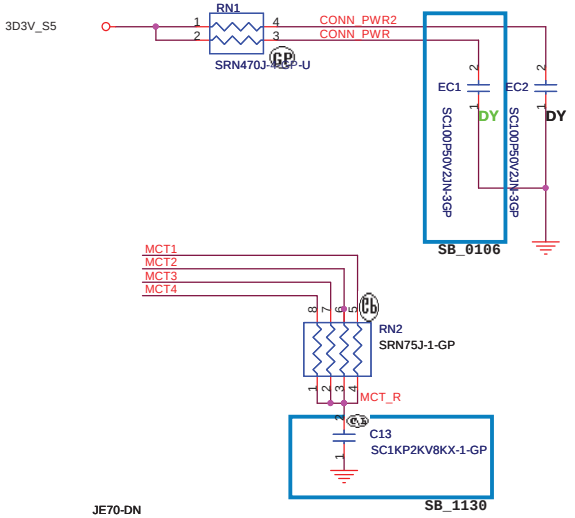
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.









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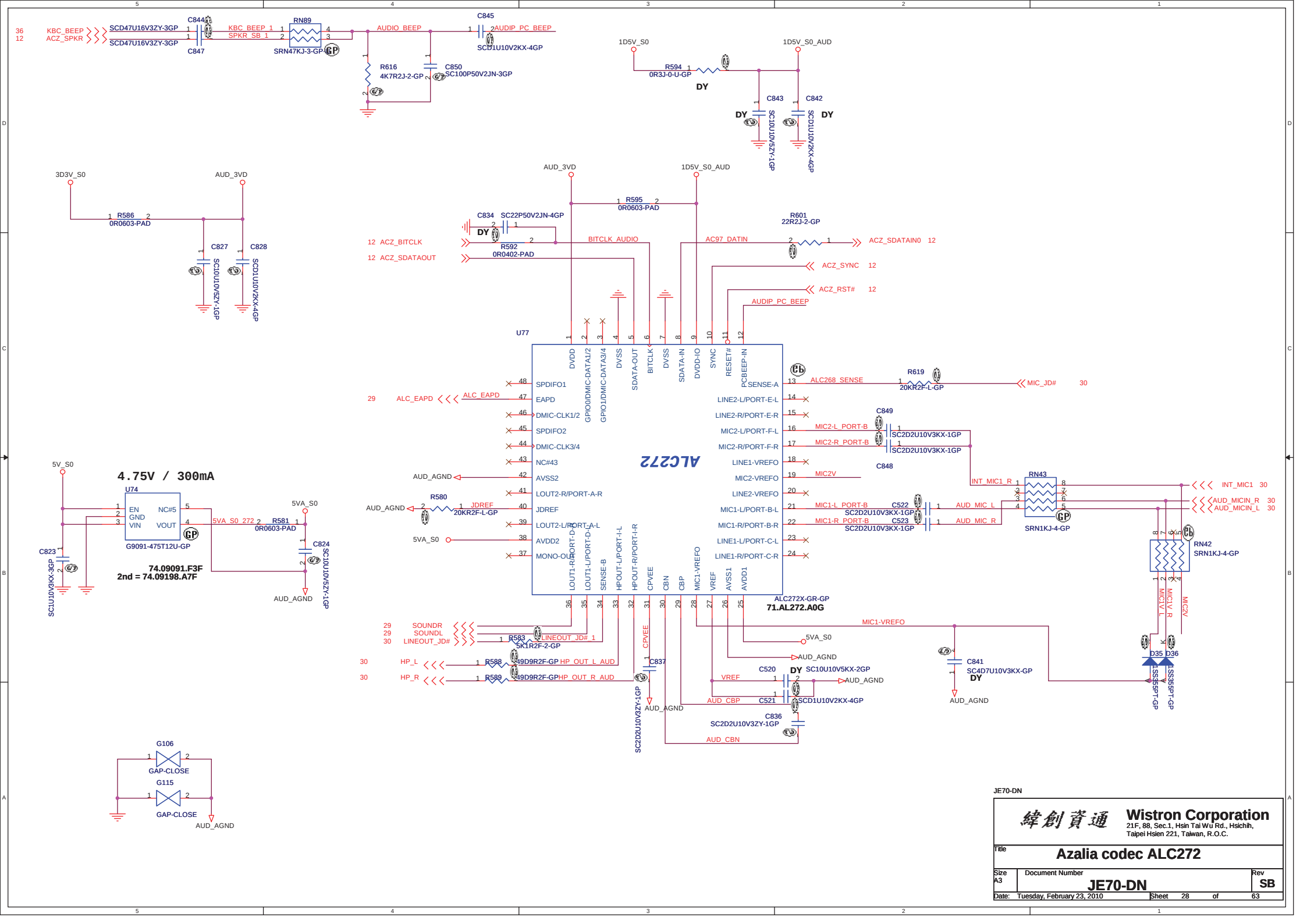

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Title	Azalia codec ALC272	
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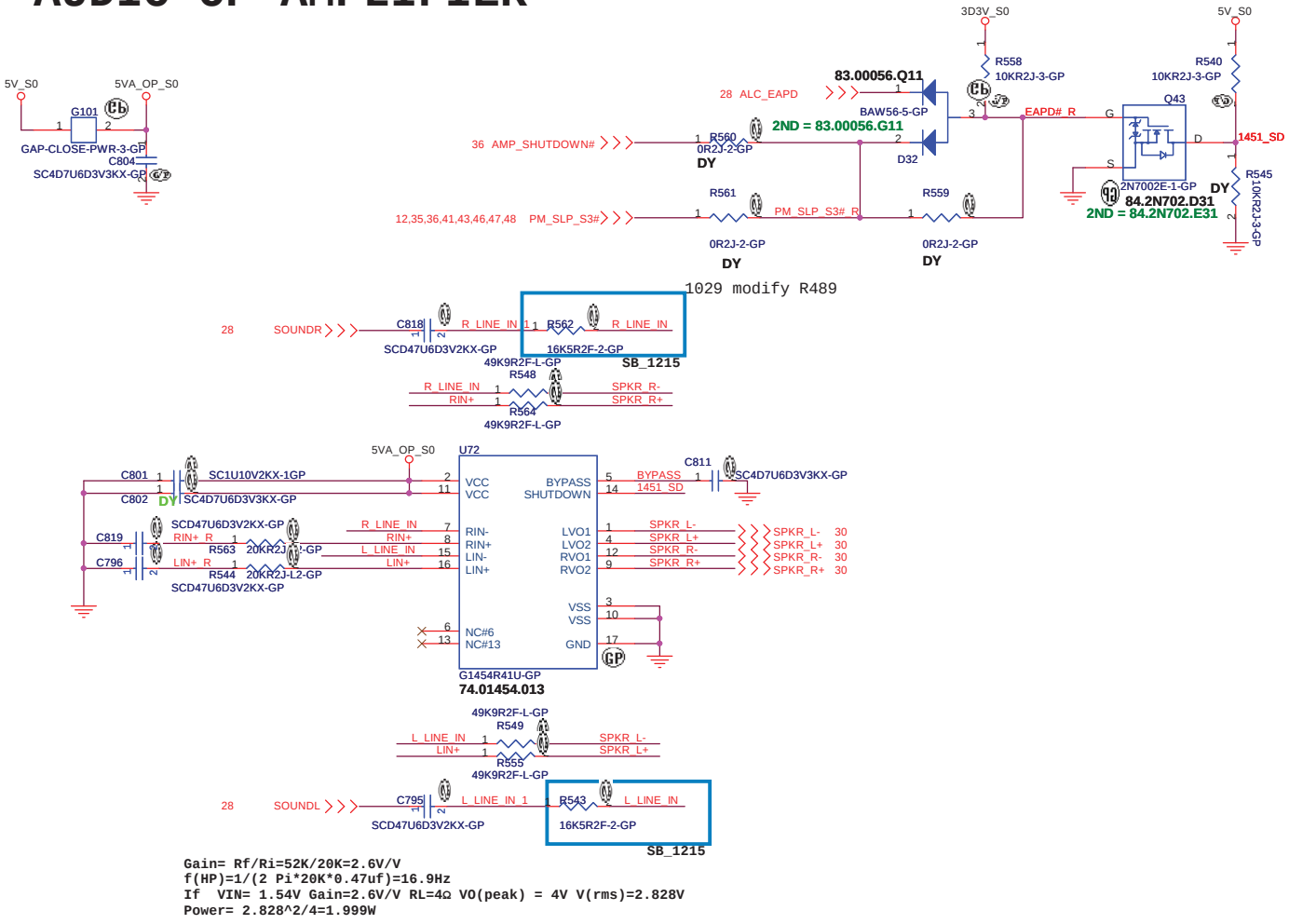
AUDIO OP AMPLIFIER




```
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If  VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W
```

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Title	**AUDIO AMP**	
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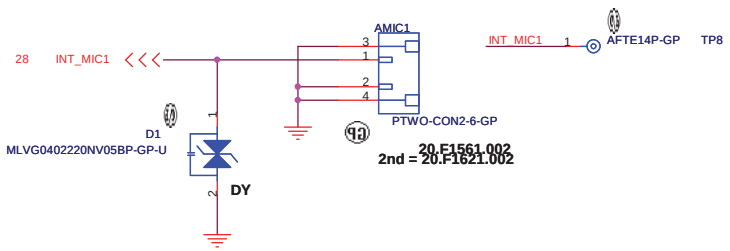
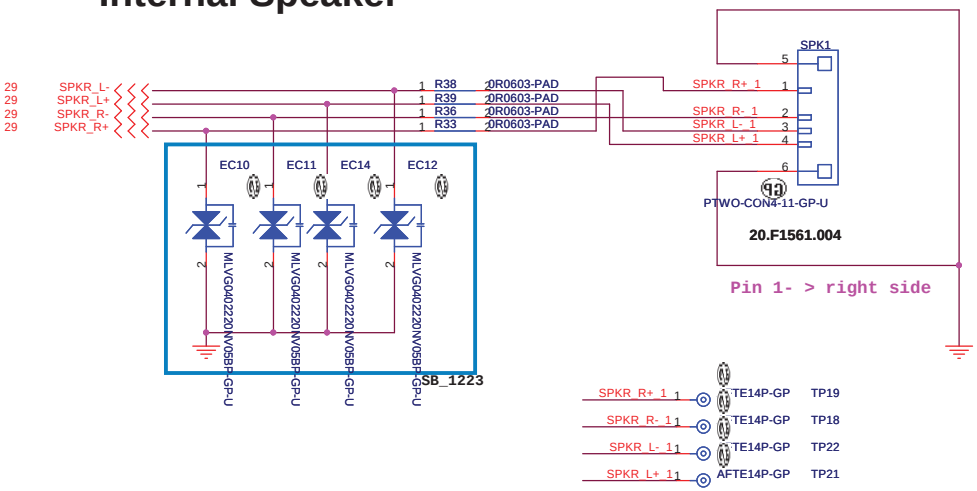
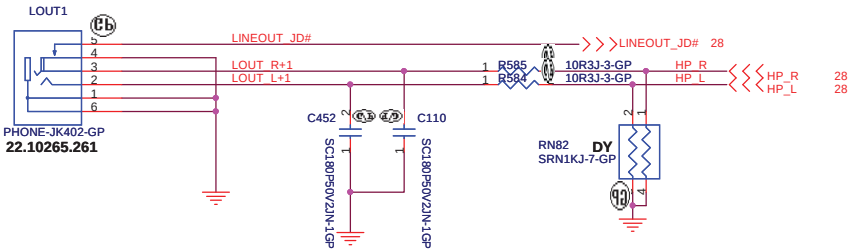
Internal Mic

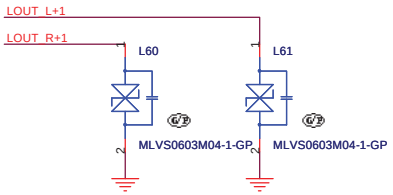


Internal Speaker

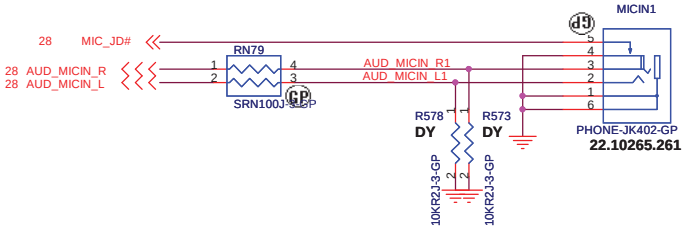


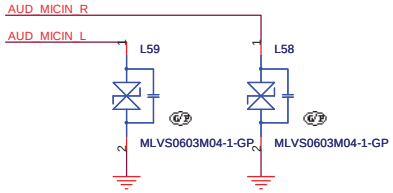
LINE OUT





MIC IN





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Title: AUDIO JACK

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No Modem Function

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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD) on USB board

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Title: **CARDREADER**		
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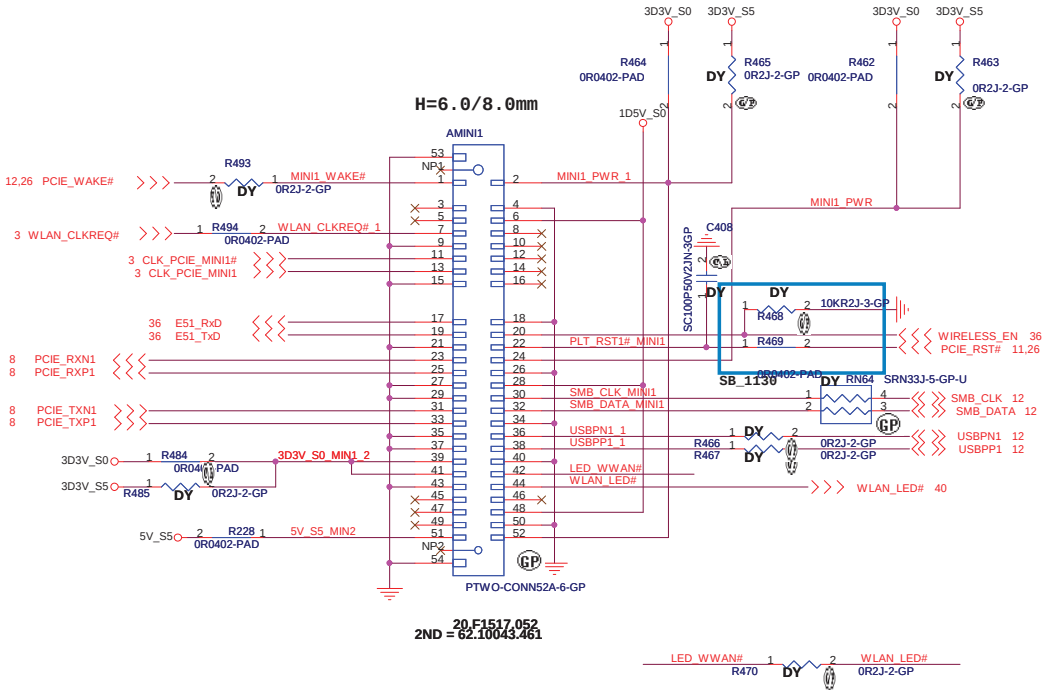
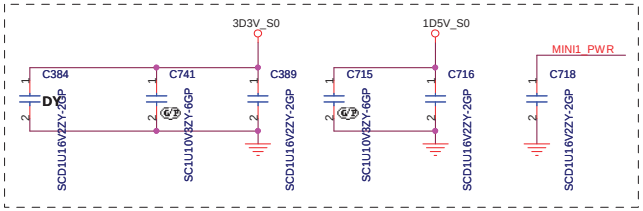
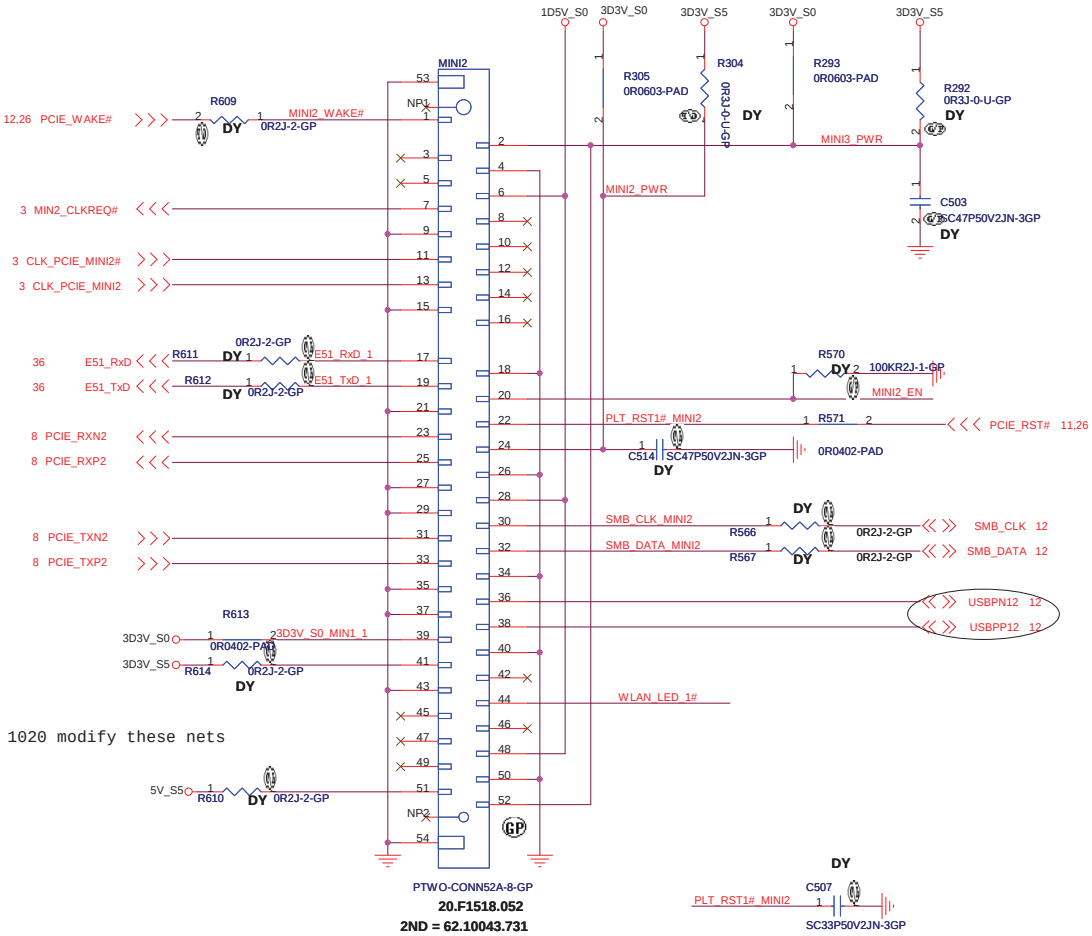
Mini Card Connector(WLAN)



Place near AMINI1

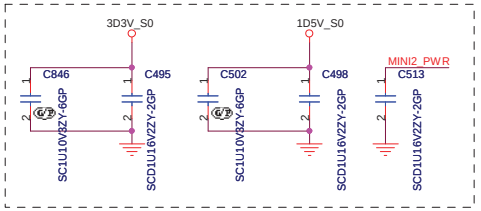


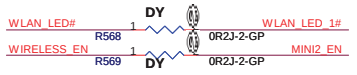
Mini Card Function



1020 modify these nets

Place near MINIC2





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Title: MINI CARD

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No NEWCARD Function

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Title		
NEW CARD		
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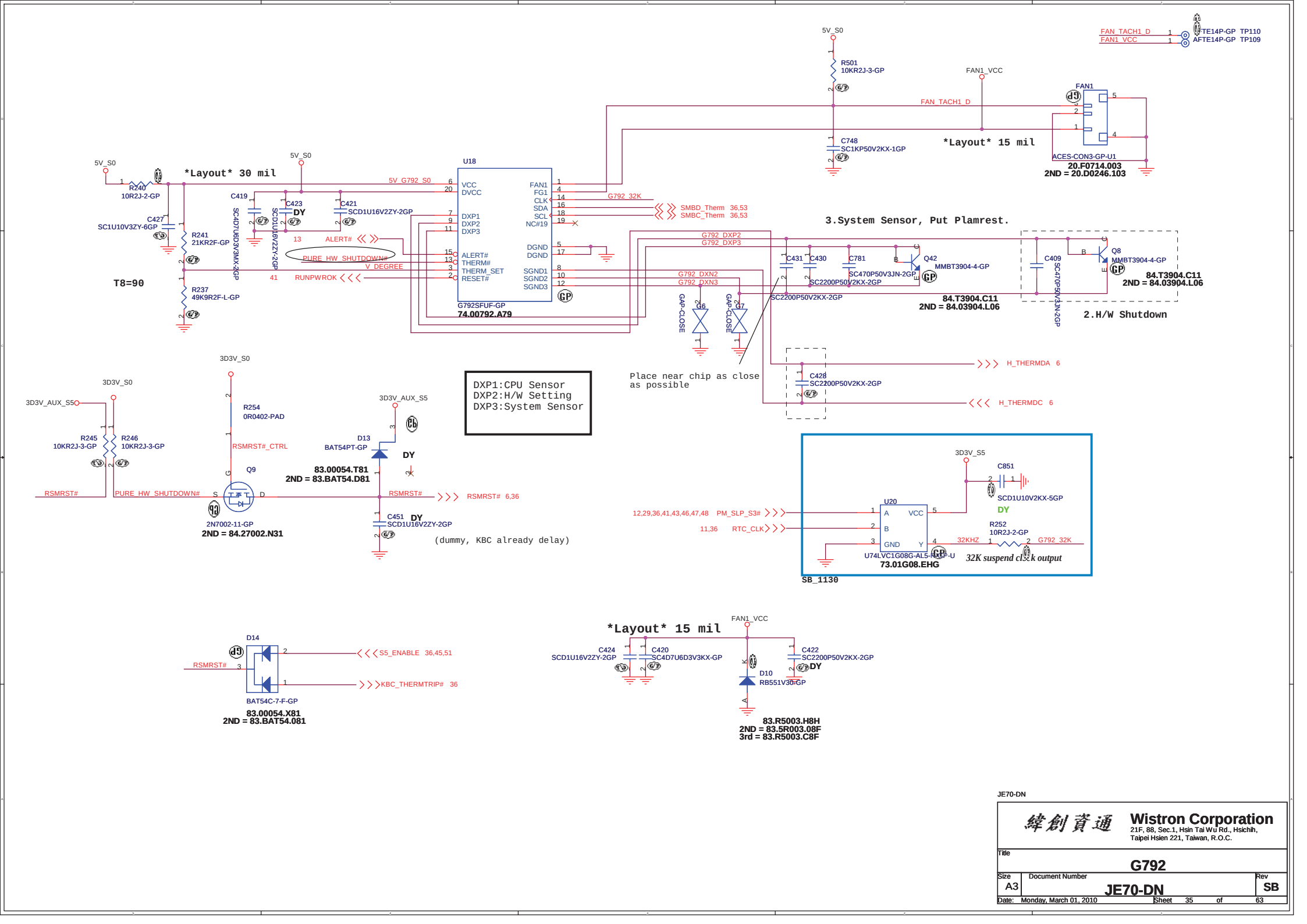

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Title		
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1020 add R134

1029 modify the net(KBC_BL_ON_IN)

1103 add the net(A_MIC_SUPPORT#)

1023 delete R892,R483,R497,R478 and add RN123

1023 swap these nets(KBRCIN#,KA20GATE)

1023 add U101

1023 modify RN89

1111 delete CRT_DEC#

Prevent BIOS data loss solution

FOR KBC DEBUG

Model ID

14": PH 10K 3D3V_AUX_S5

17": PL 10K GND

Change to 71.00773.00G

SB 1126 add TP174

1023 delete R258 and RN122

PCB VER

SA: R250-->1.0K

SB: R250-->2.0K

SC: R250-->3.0K

1 : R250-->4.7K

THERMAL-----> 35,53 SMBD_Therm 35,53 SMBC_Therm

BATTERY-----> 49,50 BAT_SDA 49,50 BAT_SCL

AC_IN_LED

26 K/B 1

Internal KeyBoard Connector

AKB1 20.K0320.026 ACES-CON26-6GP-U

65W UMA 90W DIS_PX

High:65W Low : 90W

High: UMA Low : DIS_PX

U61A GPIO LPC A/D D/A SMB SP SPI SER/IR

U61B KBC PS/2 FIU

NPCE781BA0DX-GP

G690L293T73UF-GP

SRN10KJ-6-GP

SRN10KJ-5-GP

CH731UP-GP

MMBT3906-4-GP

84.T3906.A11

2ND = 84.03906.F11

83.R0304.A8H

2ND = 83.R2002.B8E

Wistron Corporation

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Title: KBC NPCE781B

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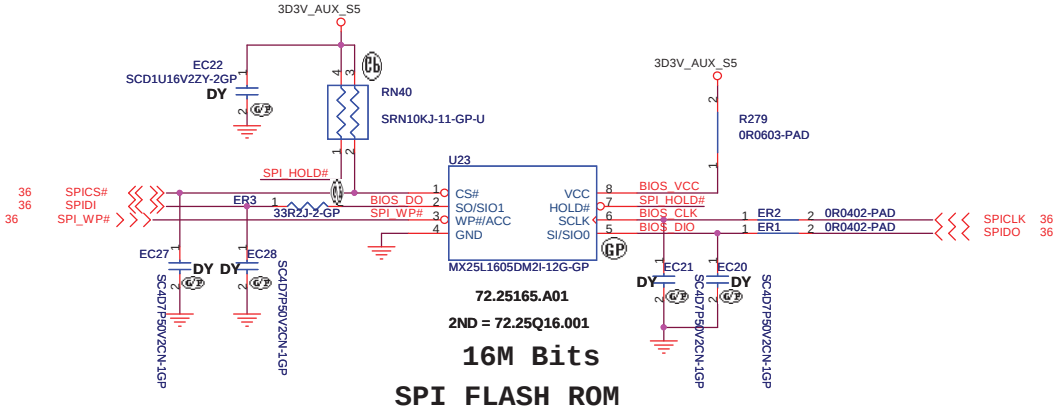
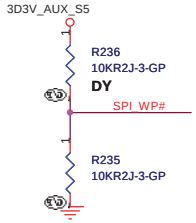
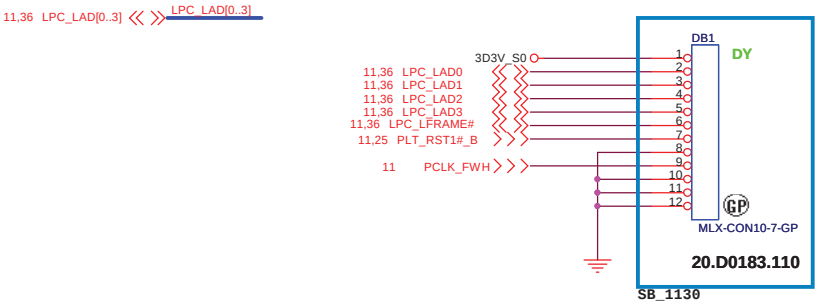




GOLDEN FINGER FOR DEBUG BOARD



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Title		
BIOS		
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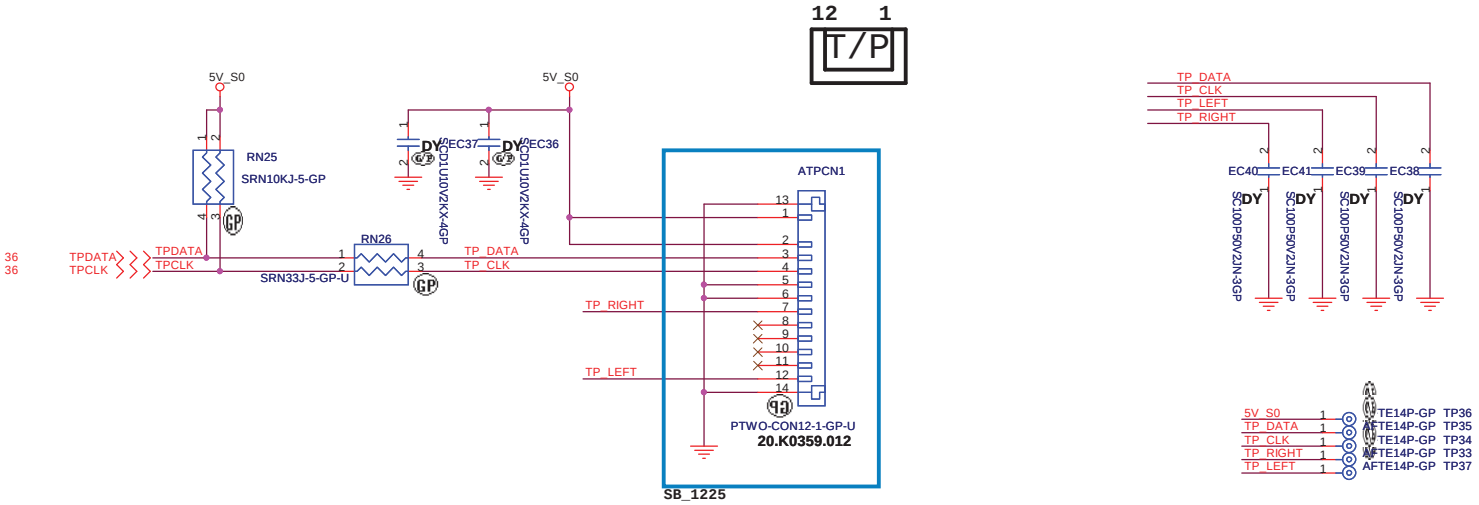

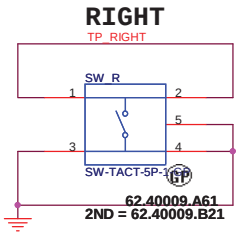

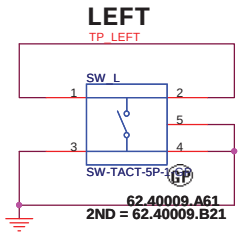

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Title: Touch PAD

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NONE BOARD

緯創資通 Wistron Corporation
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Title: NONE BOARD

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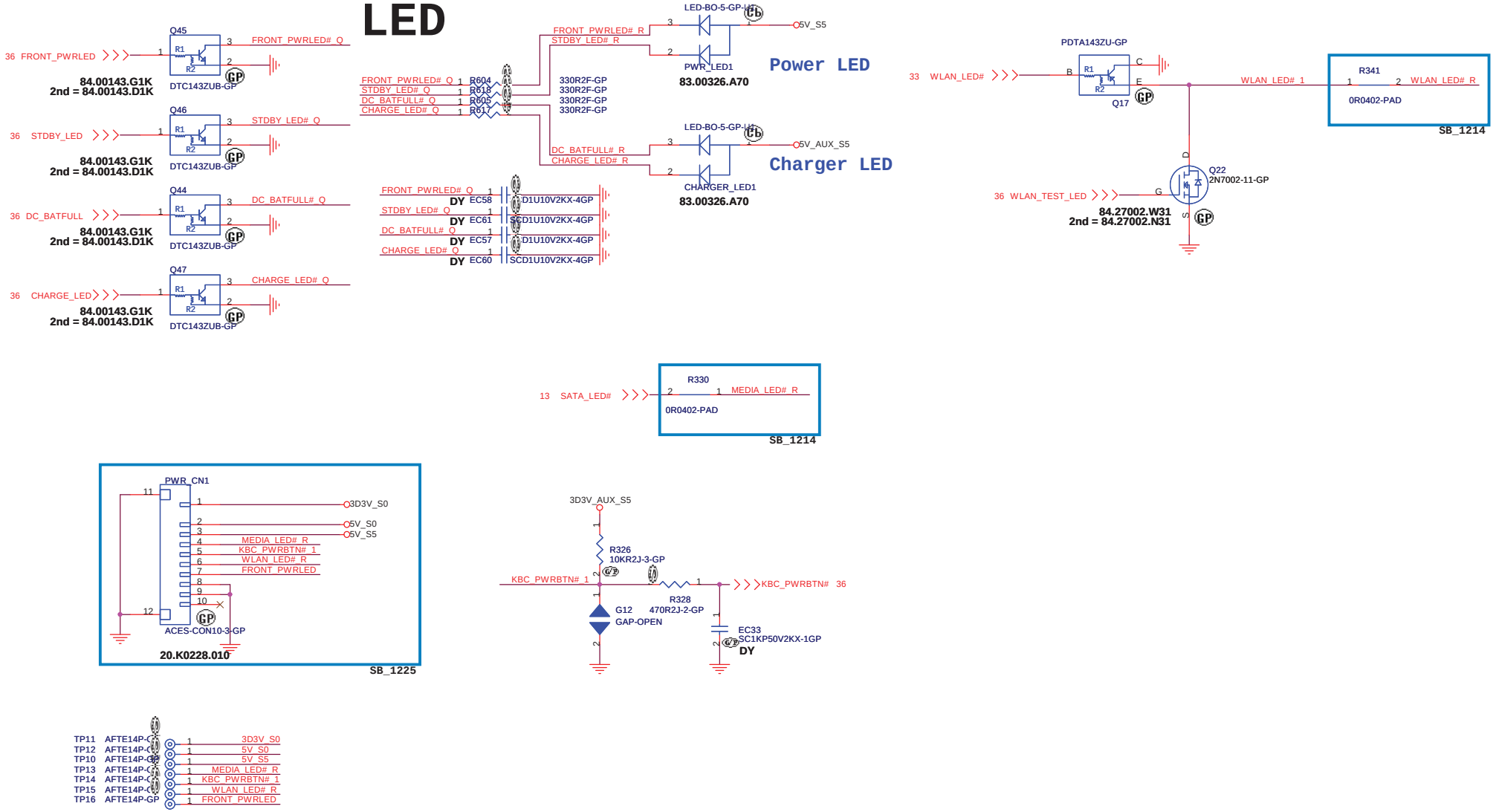
LED



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LED		
Size: A3	Document Number: JE70-DN	Rev: SB
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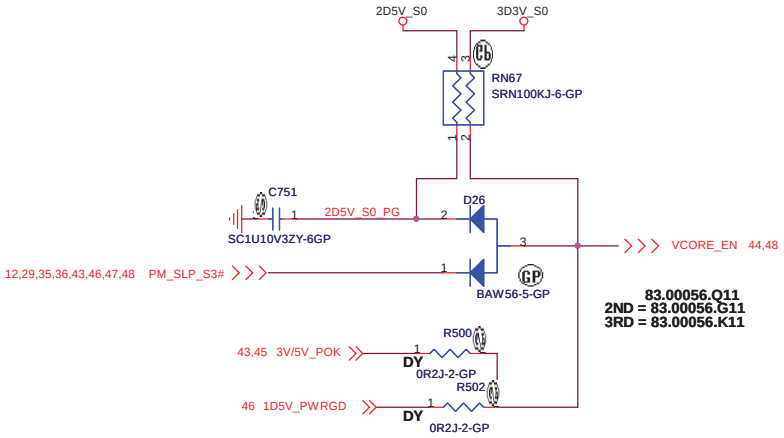
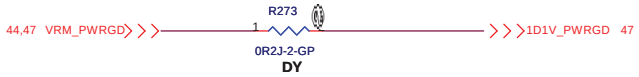
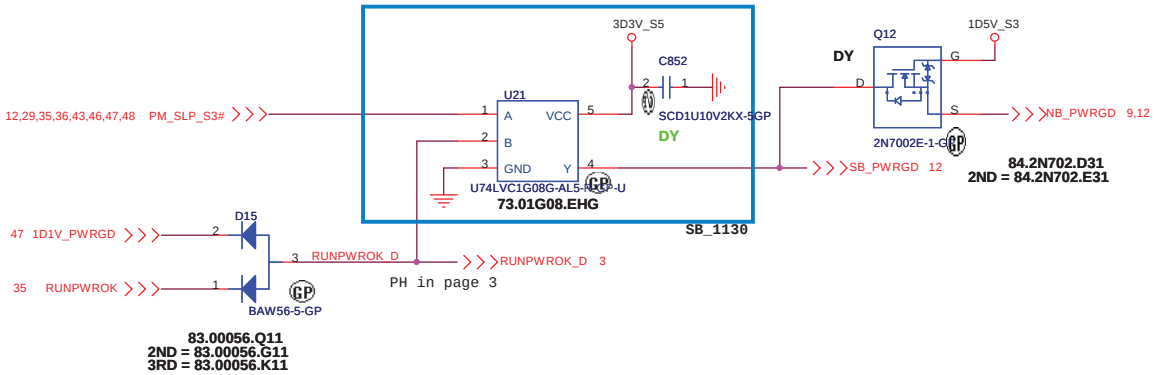


1D5V_S3_PWRGD

P/H @ 1D8V_S3 PAGE





JE70-DN

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Title: **POWER ON LOGIC**

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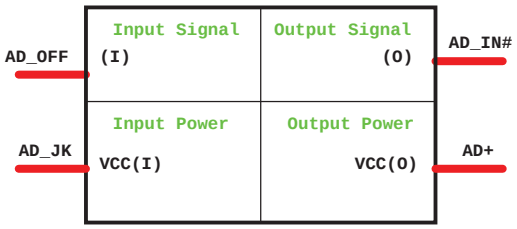
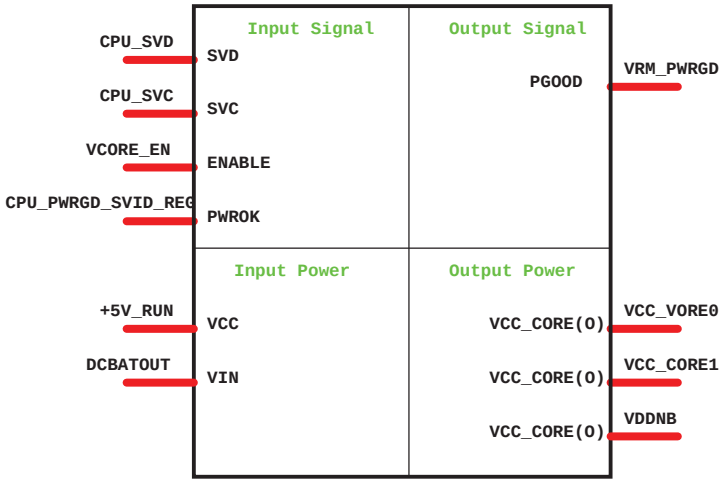
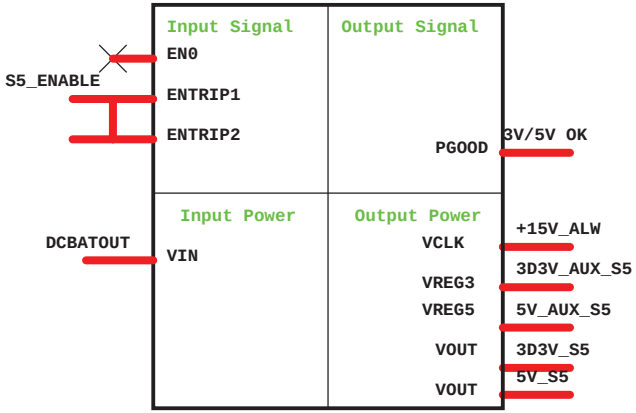
Adapter



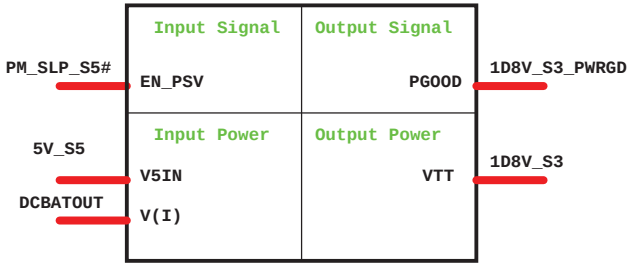
CPU_CORE
ISL6265HRTZ



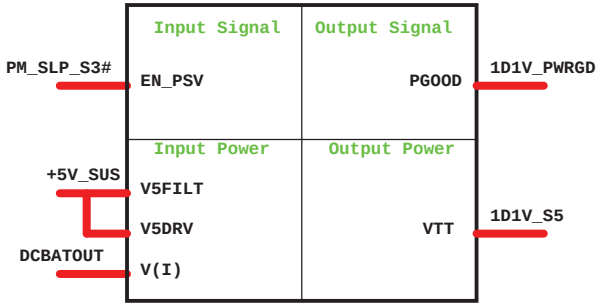
DCDC 5V/3D3V(RT8205A)



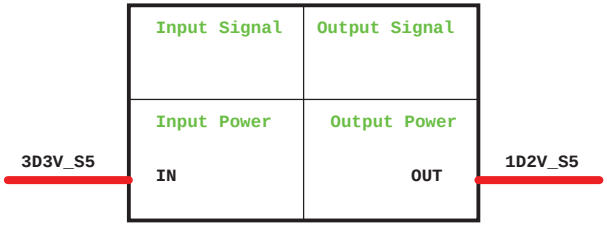
DCDC 1D8V(RT8209B)



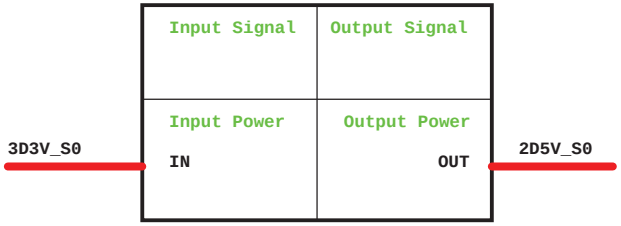
DCDC 1D1V(RT8209)



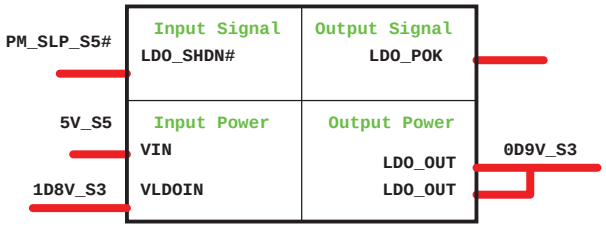
1D2V LDO G9161



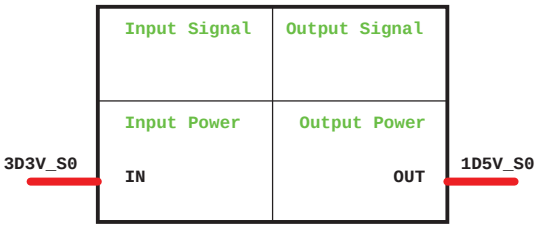
2D5V LDO R9161



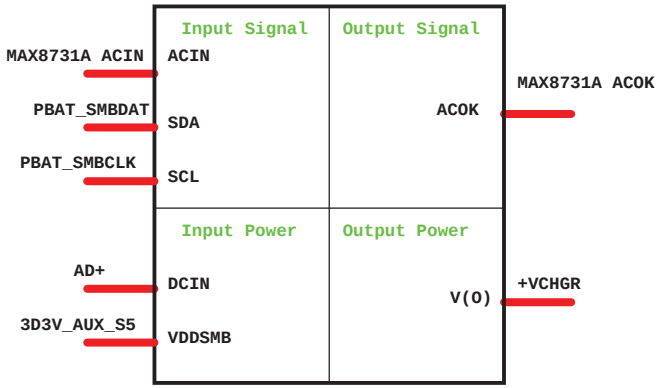
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



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Title: **Power Block Diagram**

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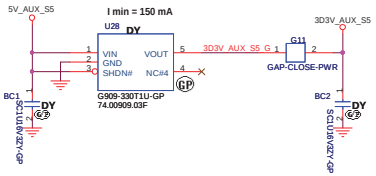
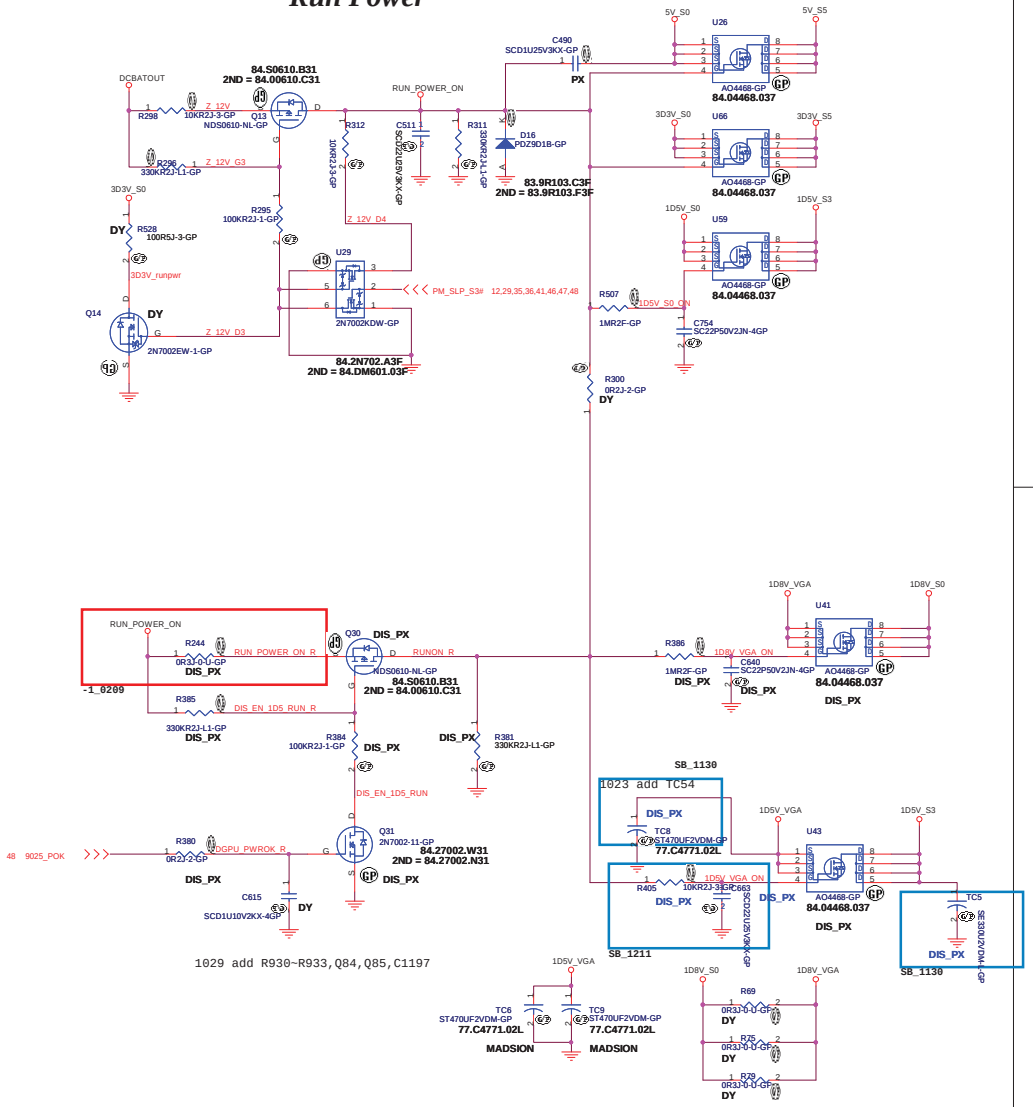
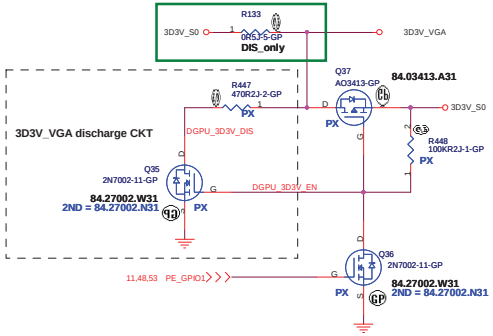
Aux Power 3D3V_AUX_S5

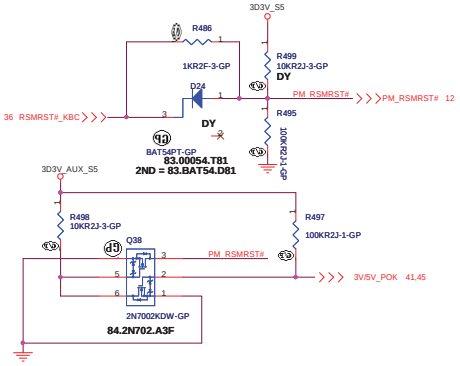


Run Power



+3VS to 3.3V_DELAY Transfer





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Title: RUN AND AUX POWER

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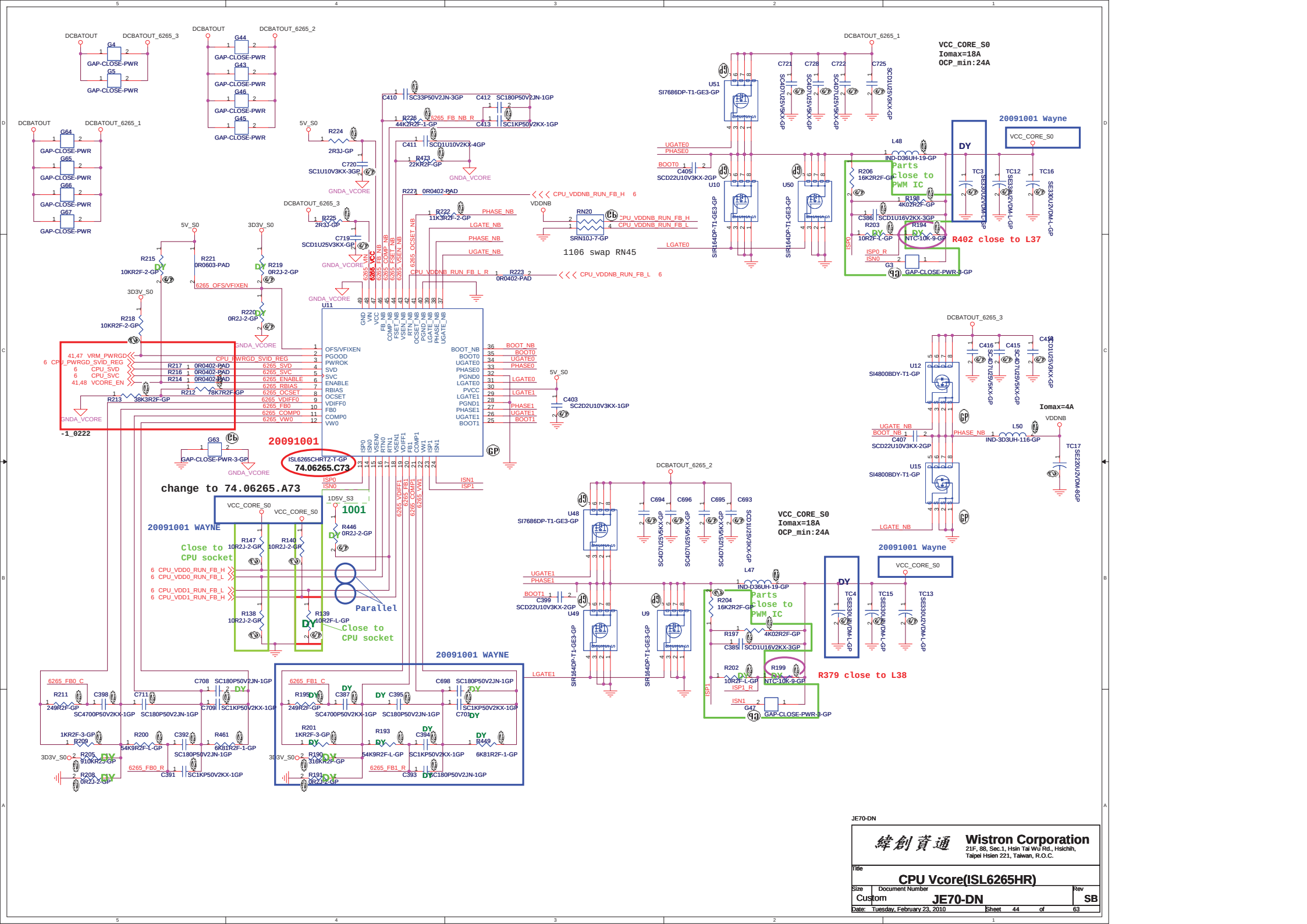
VCC_CORE_S0
Iomax=18A
OCP_min:24A
20091001 Wayne
R402 close to L37
1106 swap RN45
-1_0222
20091001
ISL6265CHRTZ-T-GP
74.06265.C73
change to 74.06265.A73
20091001 WAYNE
Close to CPU socket
Parallel
Close to CPU socket
Iomax=4A
R379 close to L38
Parts close to PWM IC
JE70-DN
Wistron Corporation
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CPU Vcore(ISL6265HR)
Custom
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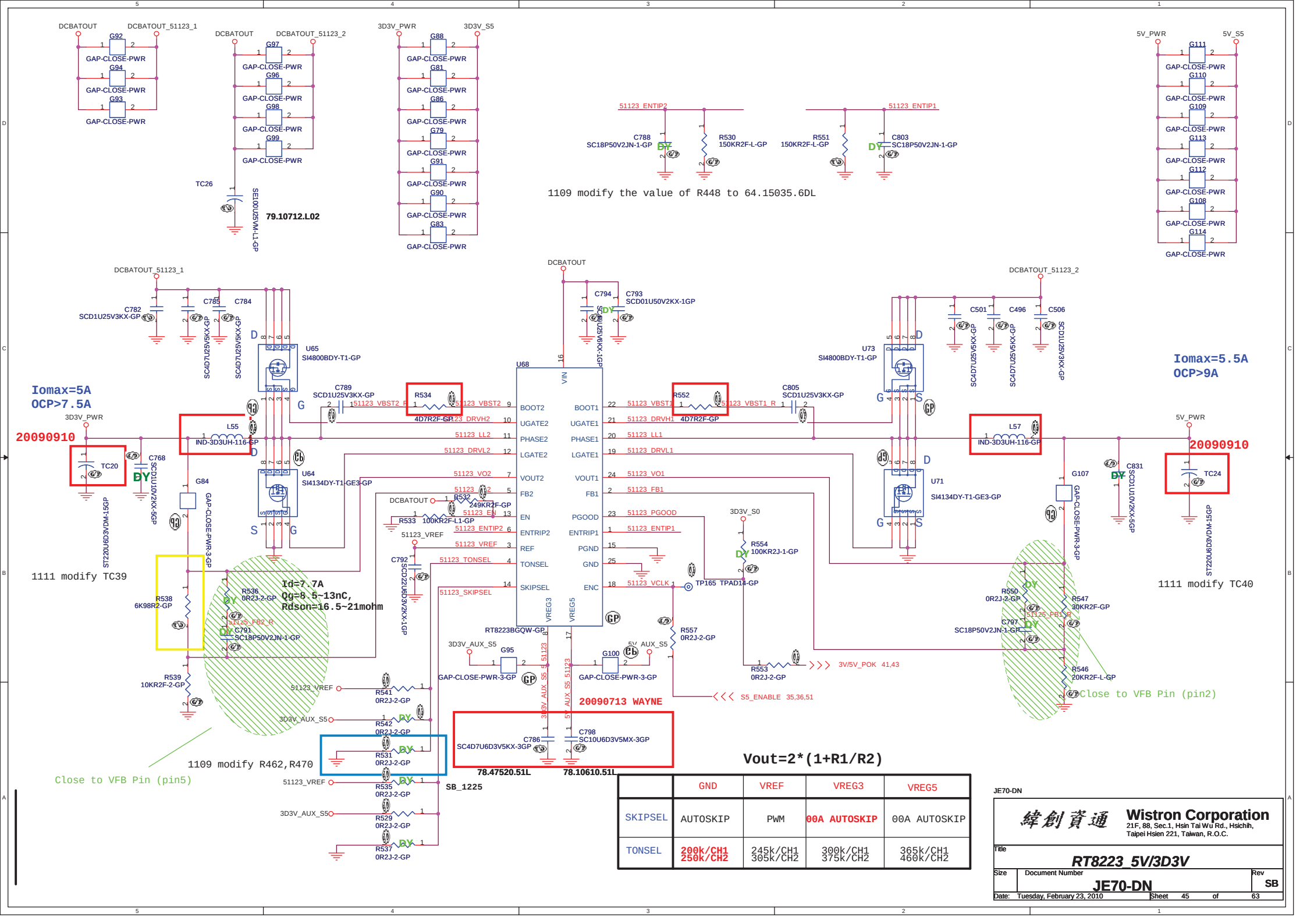

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Title: RT8223_5V/3D3V

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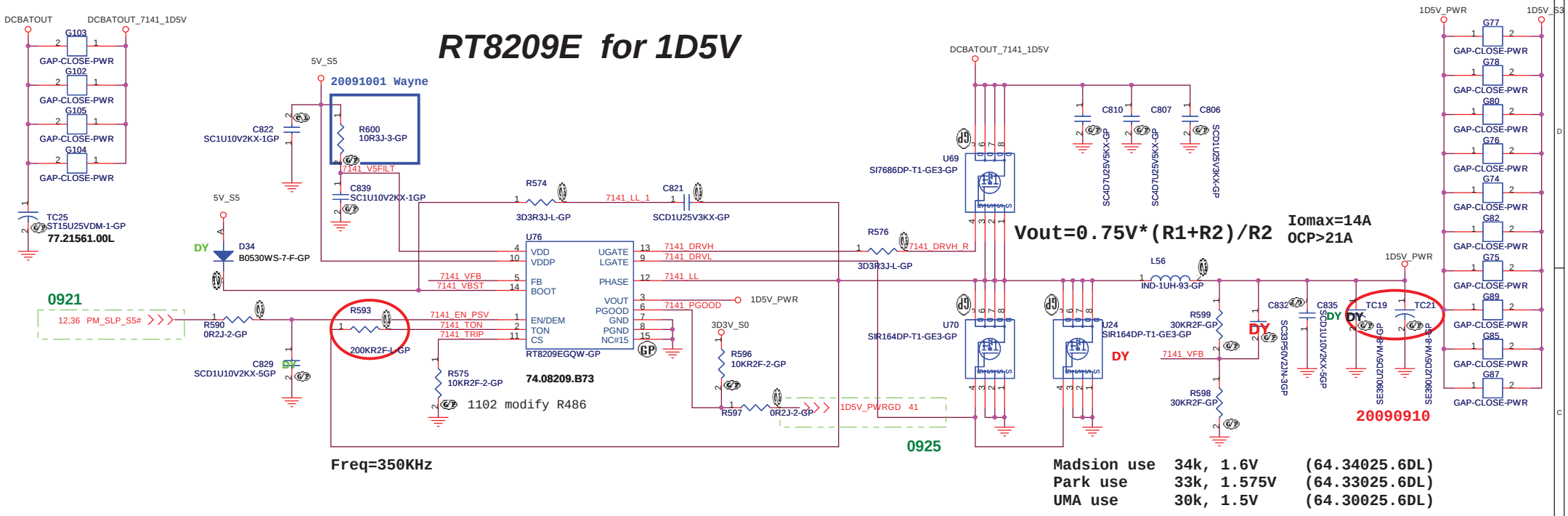
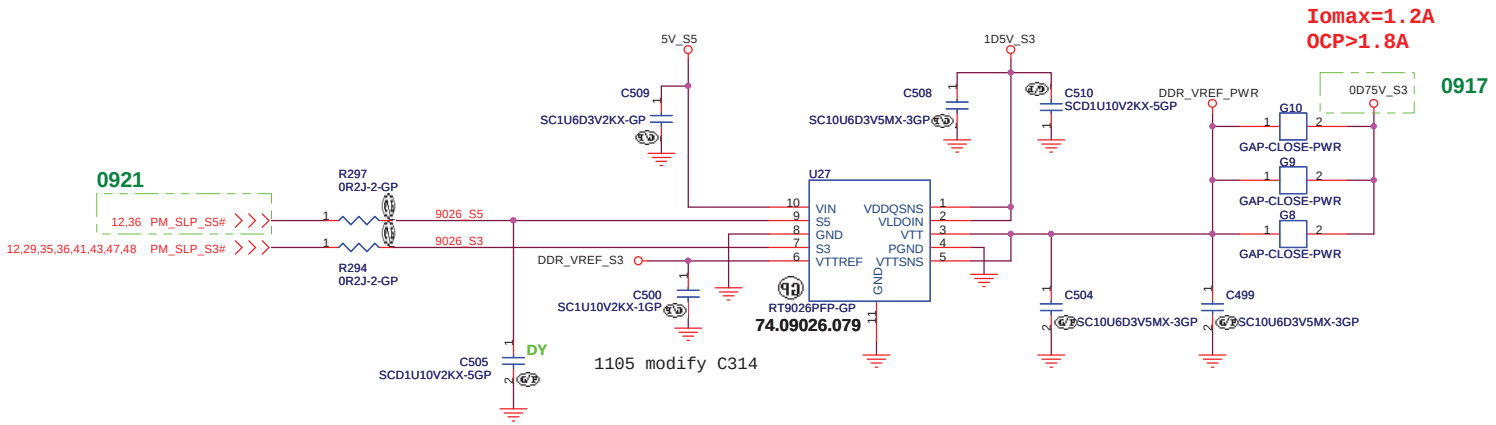
RT8209E for 1D5V



RT9026 for 0D75V_S3



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Title	RT8209E 1D5V	
Size	Document Number	Rev
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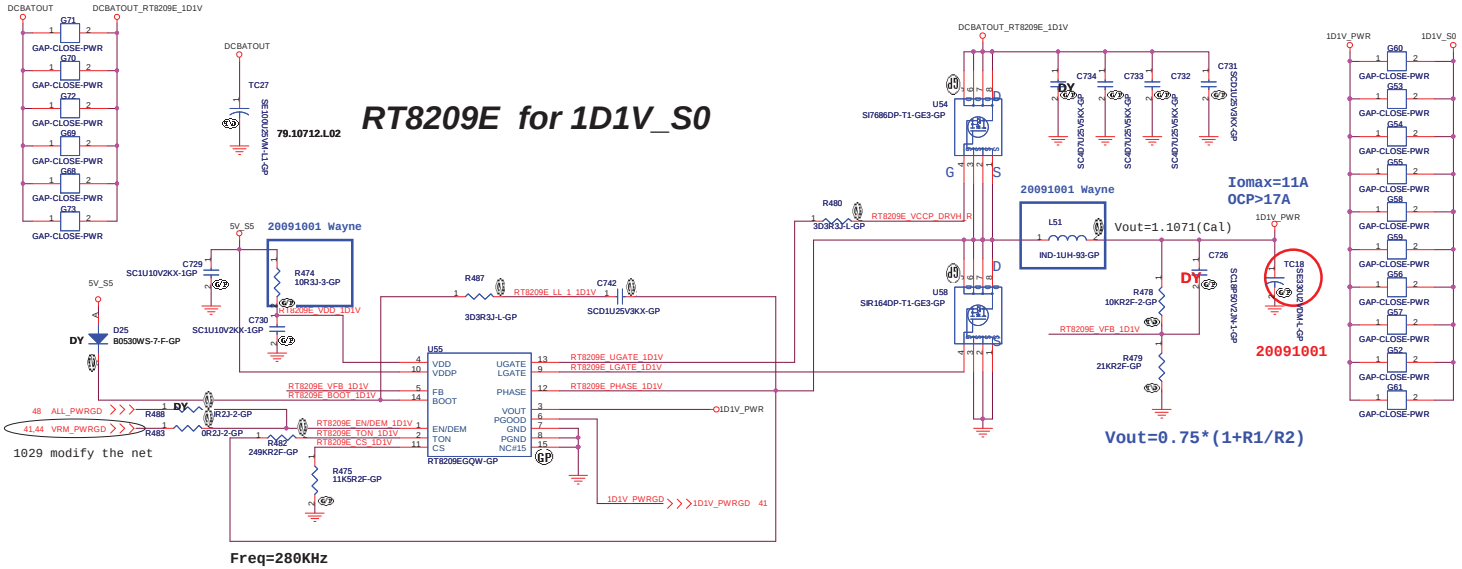

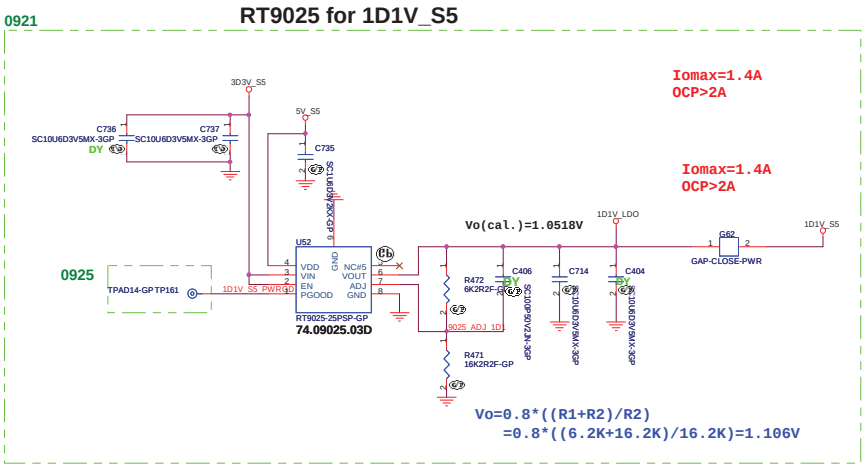

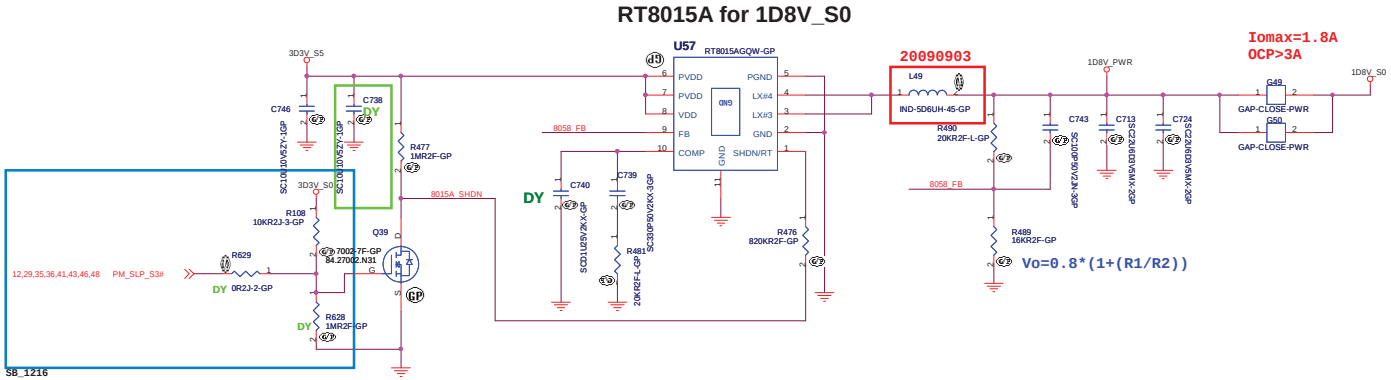

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Title: 1D1V_S0 & 1D1V_S5 & 1D8V_S0

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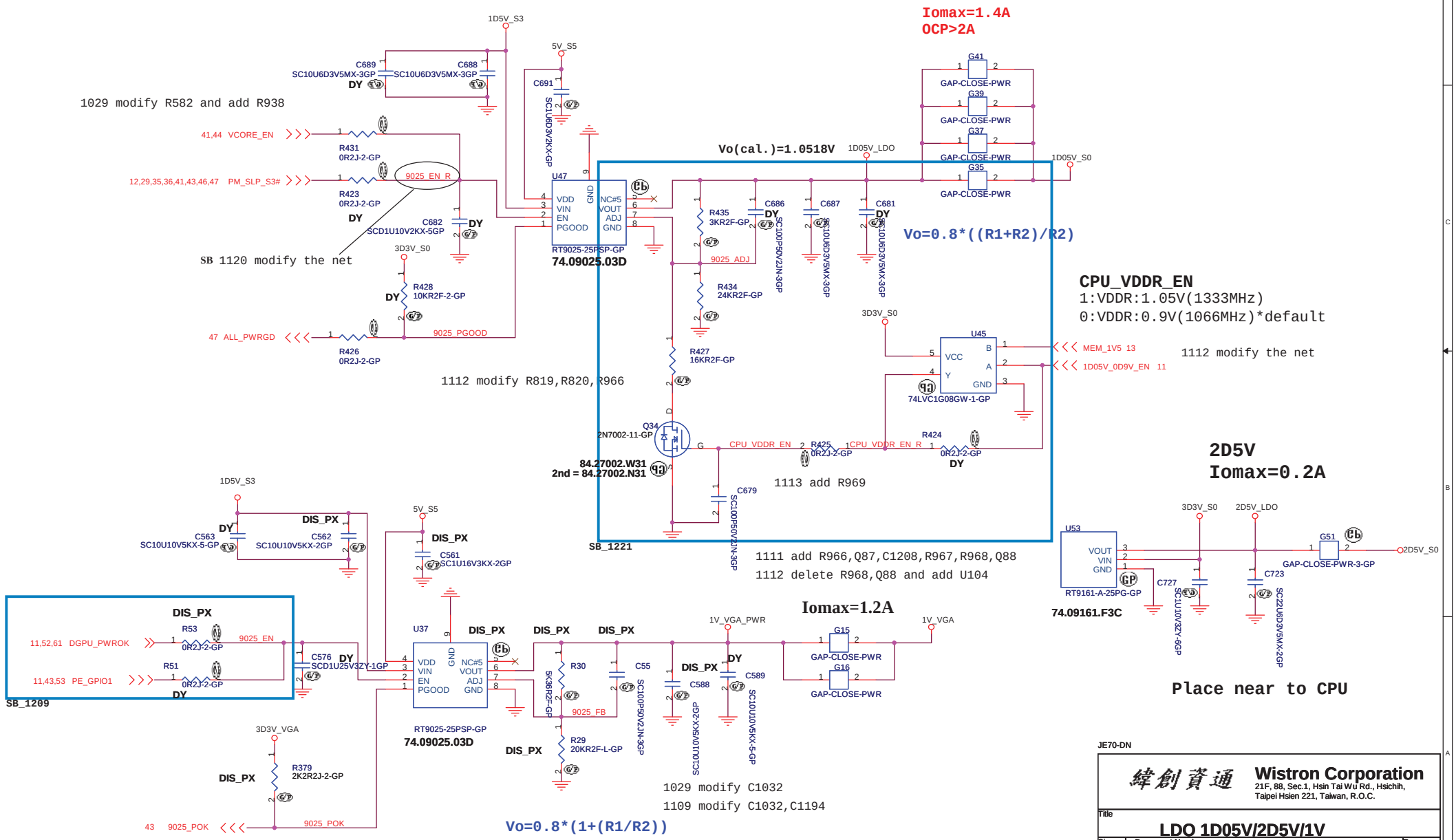
RT9025 for 1D05V_S0



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Title: LDO 1D05V/2D5V/1V

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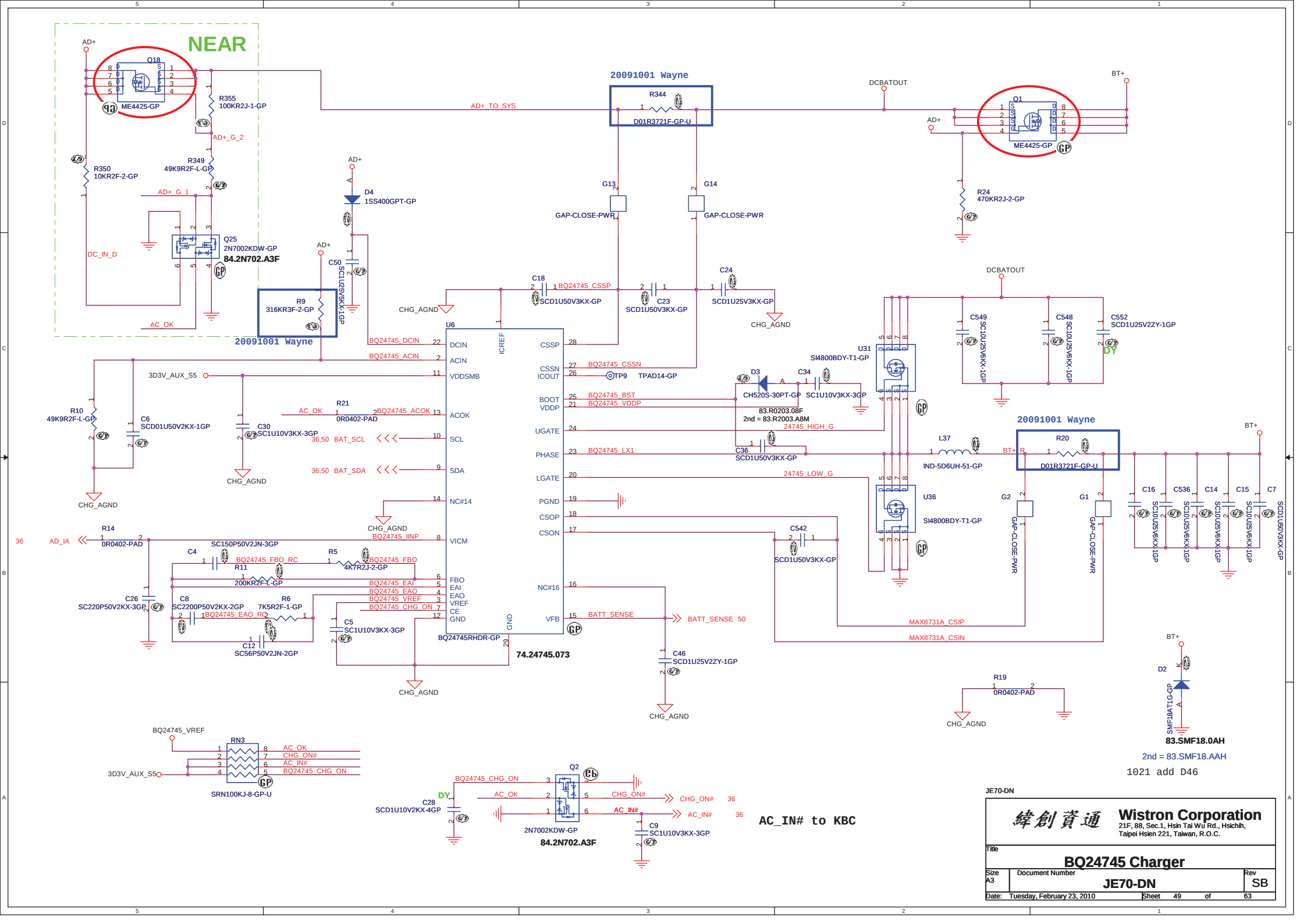

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**BQ24745 Charger**
Size A3 / Document Number	**JE70-DN** / Rev SB
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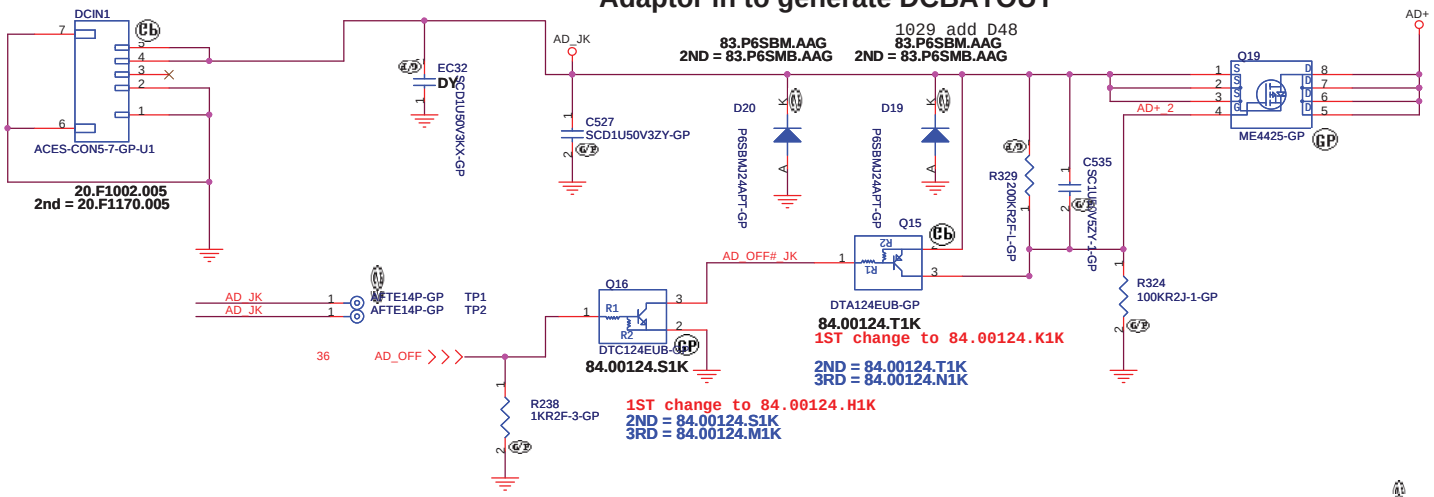
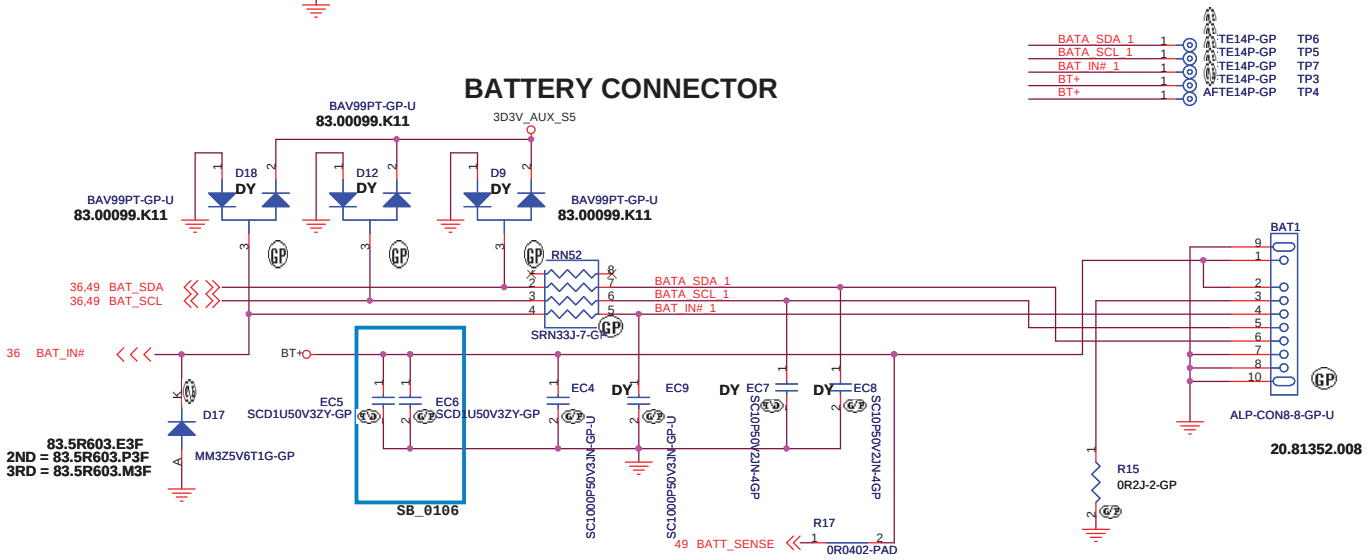
1021 modify DCIN1

1Pin=3A

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

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Title: **AD/BATT CONN**

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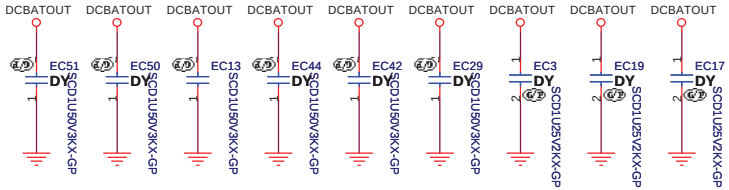
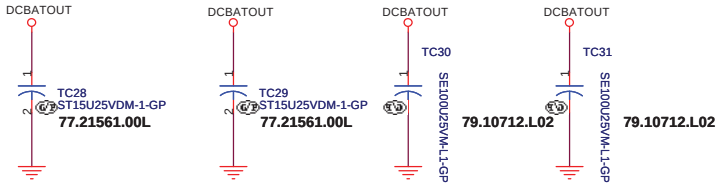
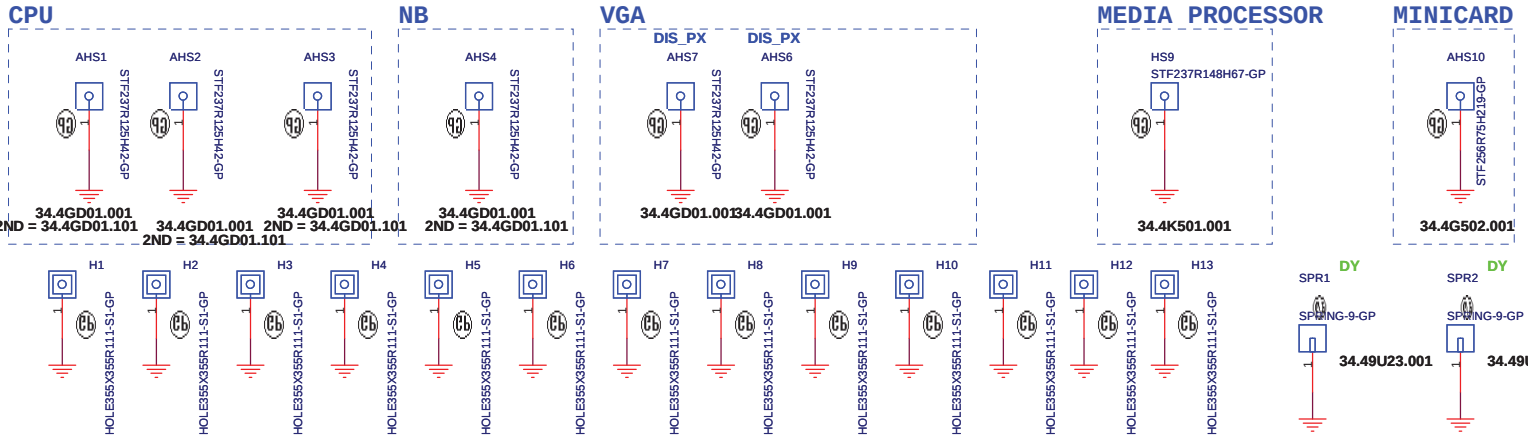
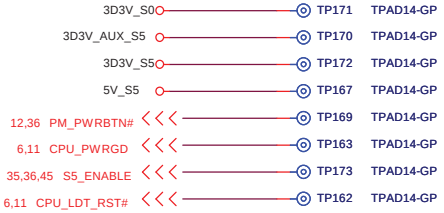






Check test point



Test Point放在Dimm Door打開可量測處

JE70-DN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: EMI/Spring/Boss		
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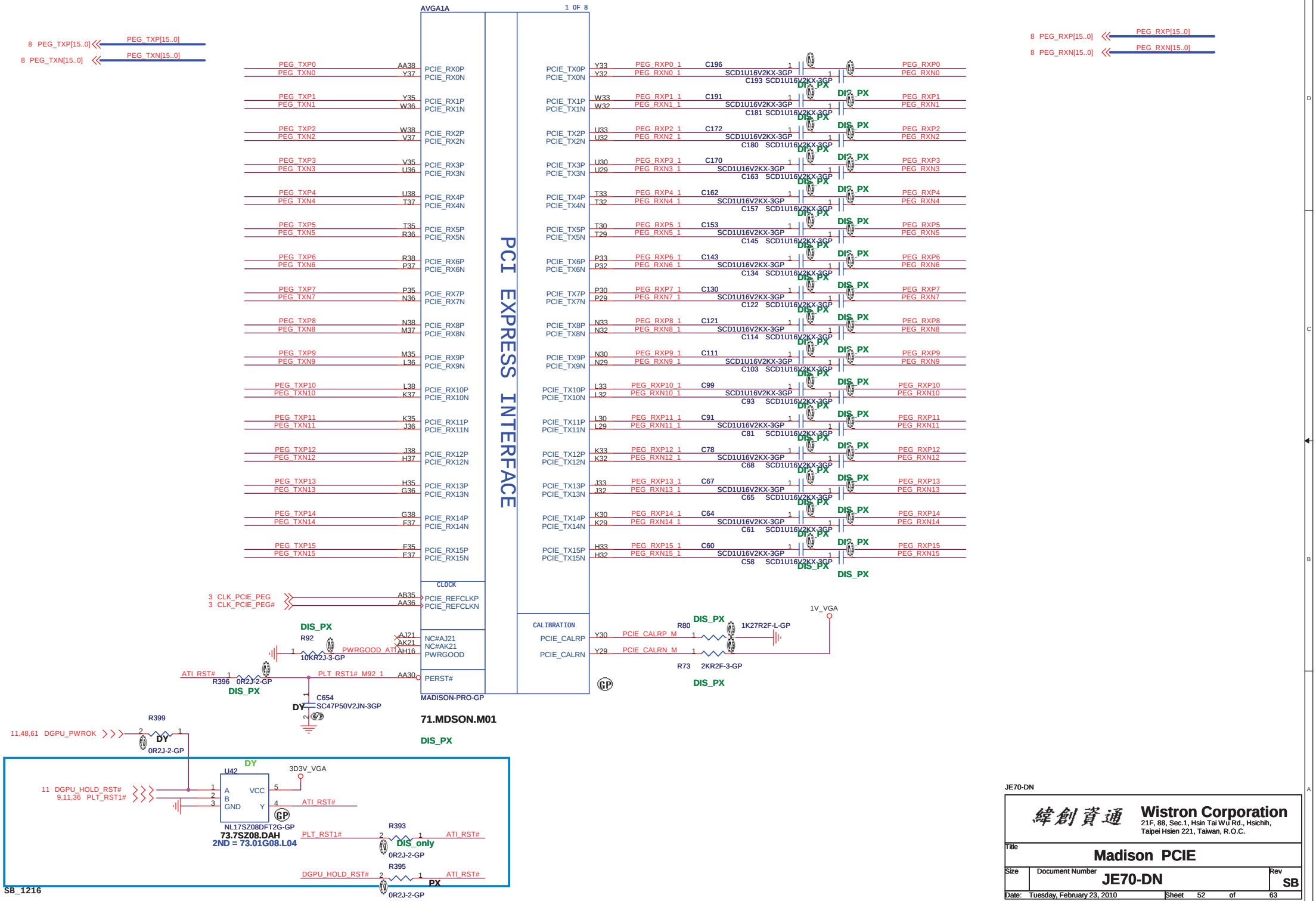
AVGA1A
1 OF 8
PCI EXPRESS INTERFACE
8 PEG_TXP[15..0]
8 PEG_TXN[15..0]
PEG_TXP[15..0]
PEG_TXN[15..0]
8 PEG_RXP[15..0]
8 PEG_RXN[15..0]
PEG_RXP[15..0]
PEG_RXN[15..0]
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
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PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
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PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
CLOCK
PCIE_REFCLKP
PCIE_REFCLKN
3 CLK_PCIE_PEG
3 CLK_PCIE_PEG#
NC#AJ21
NC#AK21
PWRGOOD
PERST#
CALIBRATION
PCIE_CALRP
PCIE_CALRN
MADISON-PRO-GP
71.MDSON.M01
DIS_PX
R92
10KR2J-3-GP
PWRGOOD_ATI
ATI_RST#
R396
0R2J-2-GP
PLT_RST1#_M92_1
C654
SC47P50V2JN-3GP
DY
R399
11,48,61 DGPU_PWROK
U42
NL17SZ08DFT2G-GP
73.7SZ08.DAH
2ND = 73.01G08.L04
3D3V_VGA
11 DGPU_HOLD_RST#
9,11,36 PLT_RST1#
R393
DIS_only
R395
PX
DGPU_HOLD_RST#
R80
1K27R2F-L-GP
R73
2KR2F-3-GP
1V_VGA
SB_1216
JE70-DN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Madison PCIE
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JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro

0 1 0 0 Hynix Orion-die(H5TQ1G63BFR-12C,800MHz)64*16 x 8 pcs1GB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 8 pcs1GB
1 1 0 0 Reserve64*16 x 8 pcs1GB

JV50-CP_JV70-CP_SJV50-CP / Park-XT

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs512MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB

1113 delete TP103,TP122,TP160,TP178

1029 add R940,R941

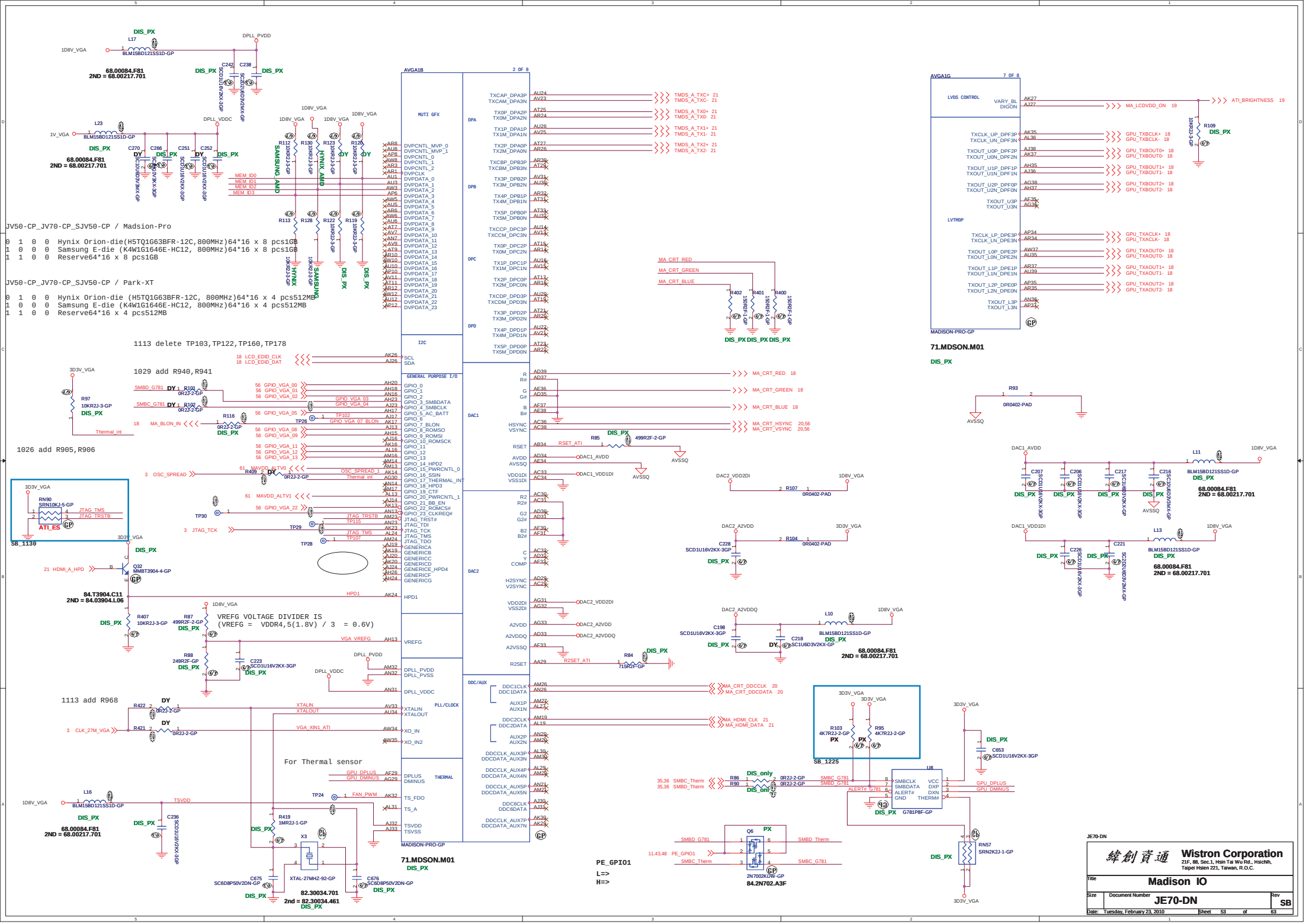
1026 add R905,R906

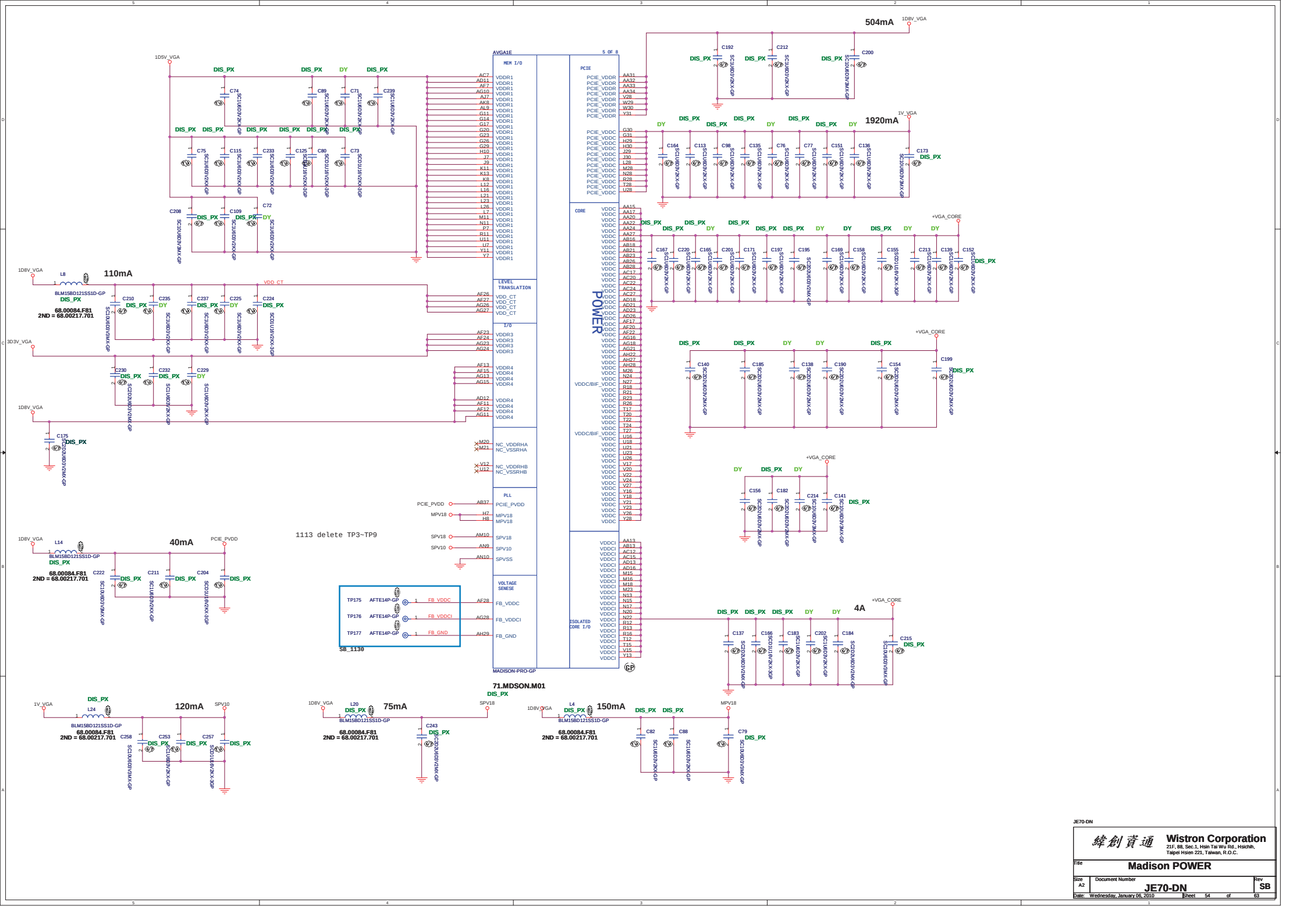
1113 add R968

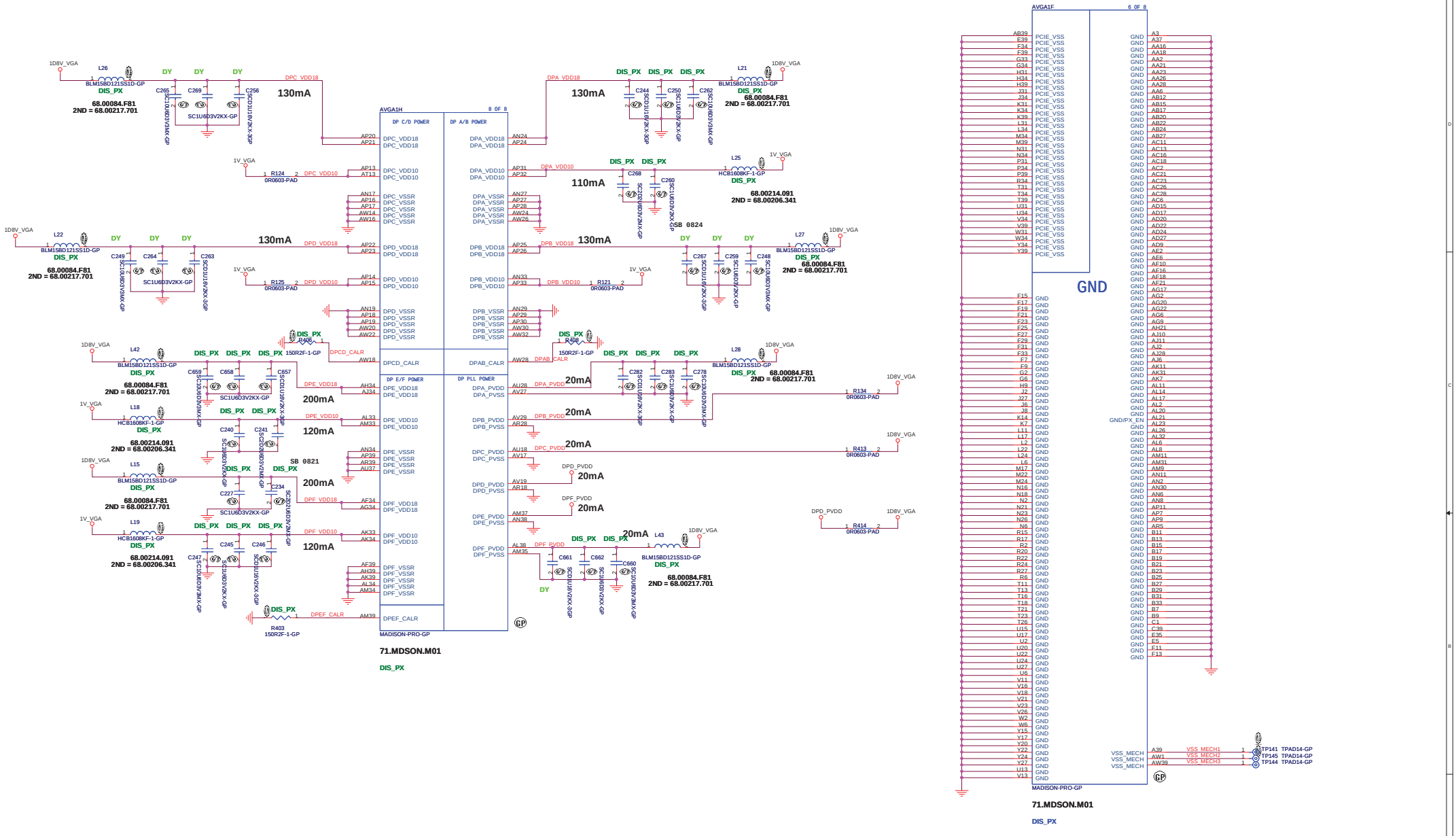
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

PE_GPIO1
L=>
H=>




504mA
1920mA
110mA
40mA
120mA
75mA
150mA
4A
1113 delete TP3~TP9
71.MDSON.M01
SB_1130
MADISON-PRO-GP
POWER
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
JE70-DN
Wednesday, January 06, 2010



JE70-DN

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DP POWER_GND
Size A2	Document Number JE70-DN
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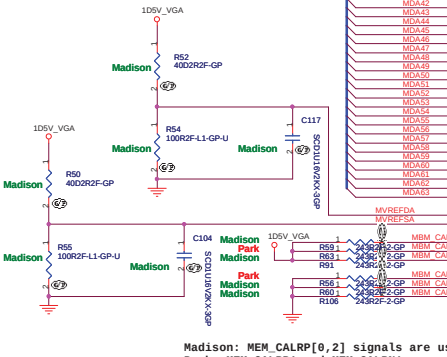
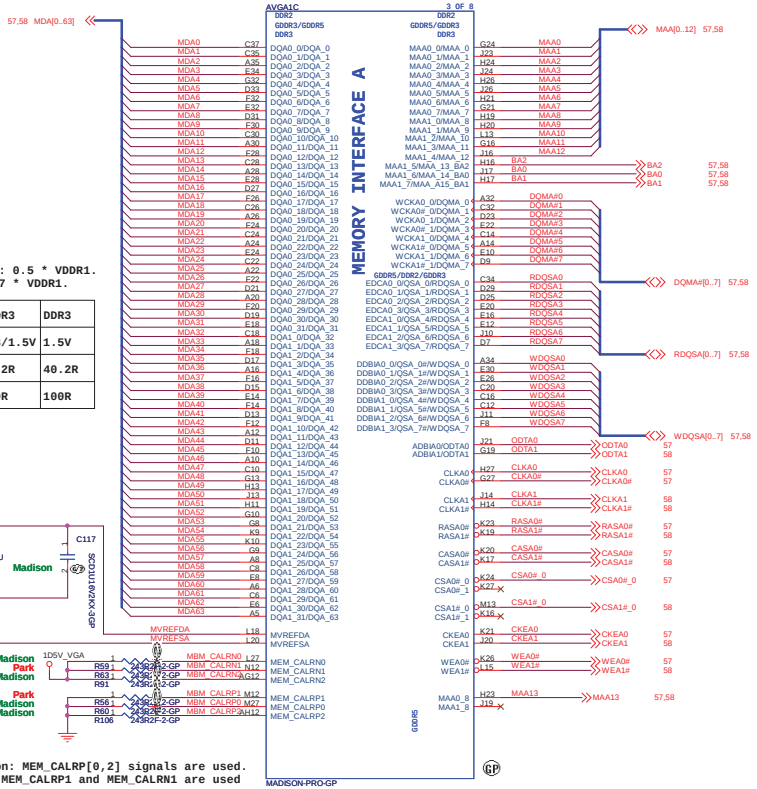
For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

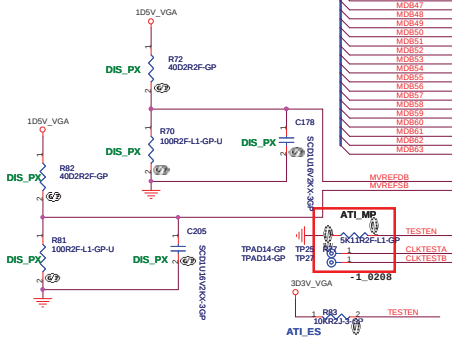


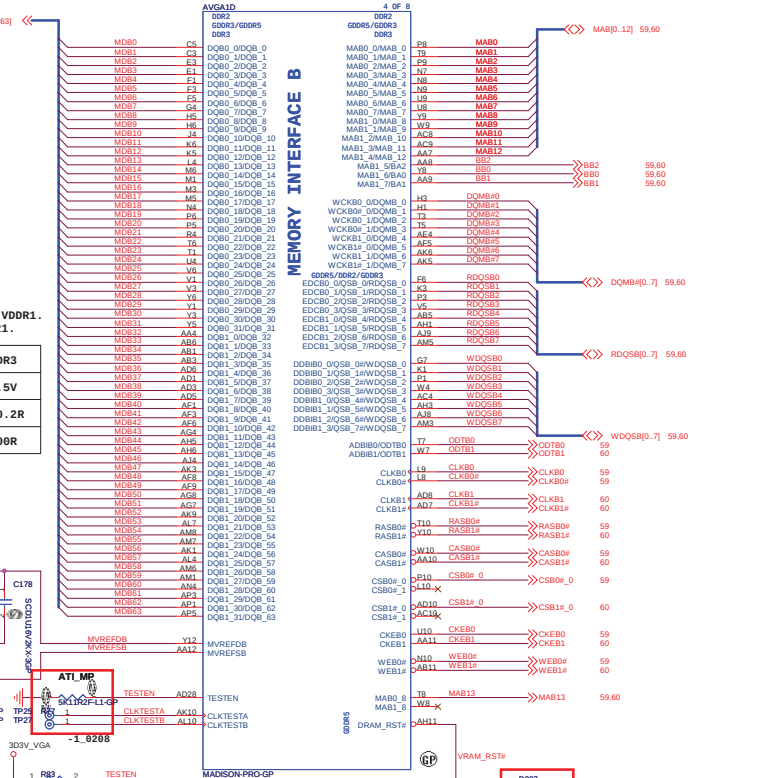
Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

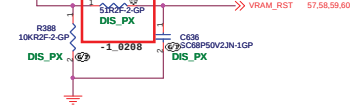


For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R







STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

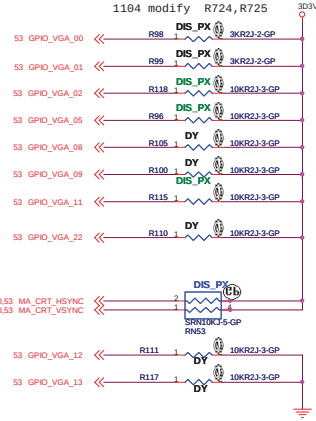
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

1104 modify R724,R725



GPIO_VGA_00 & GPIO_VGA_01
Pull-up resistor value: 3K for Madison/Park, 10K for M96/M92

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

JE70-DN

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Title: Madison Memory / Straps

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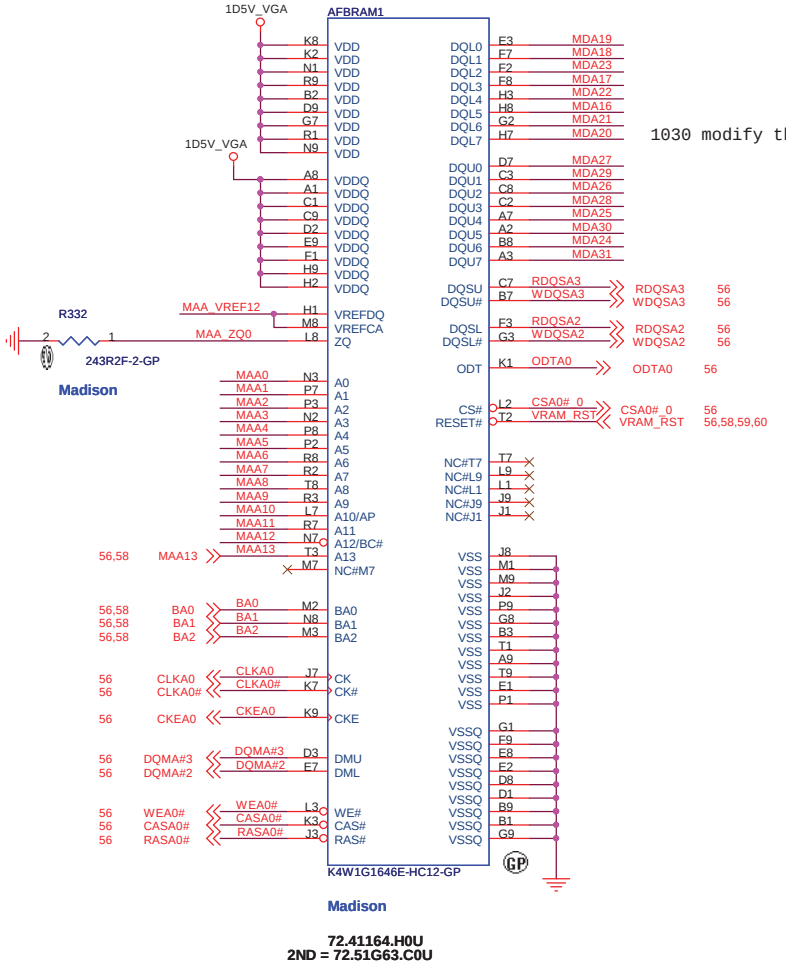
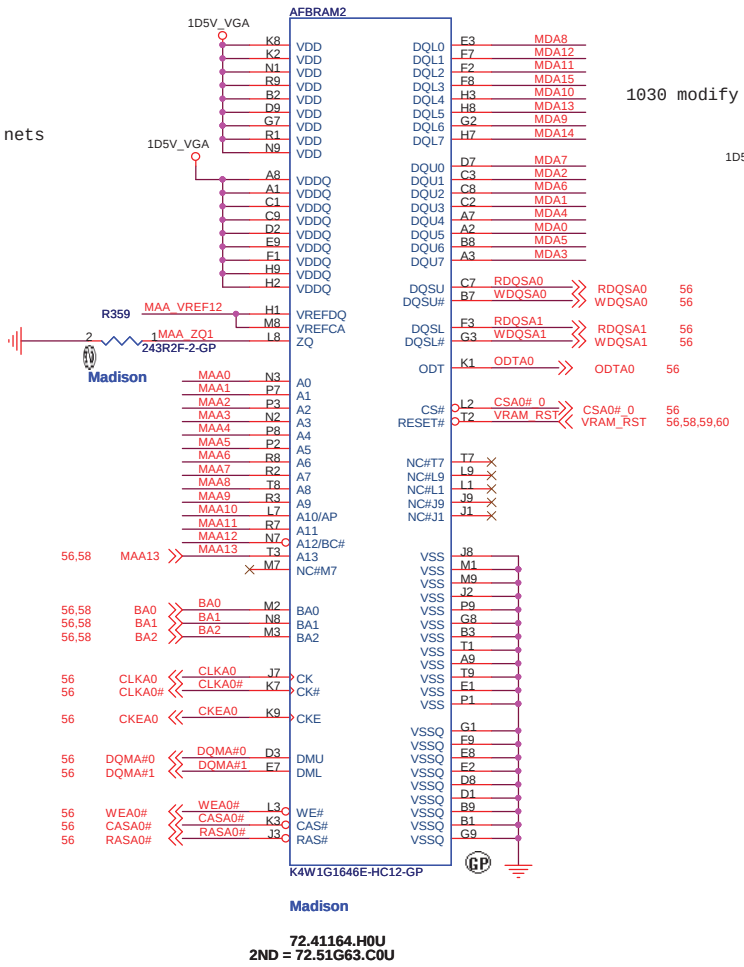
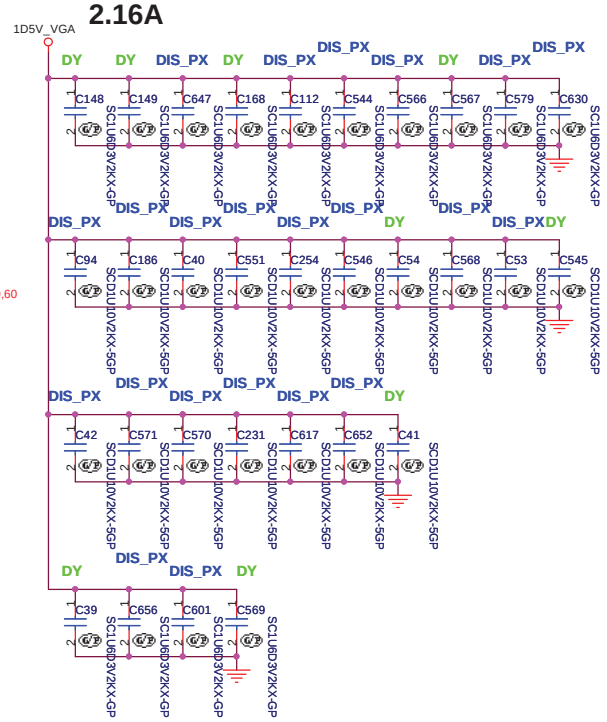
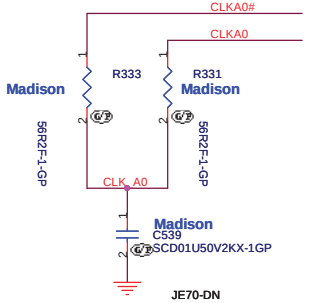
DDR3

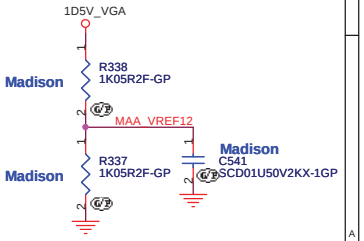


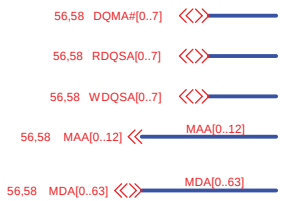




SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)







JE70-DN

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(1/4)***	
Size A3	Document Number **JE70-DN**	Rev **SB**
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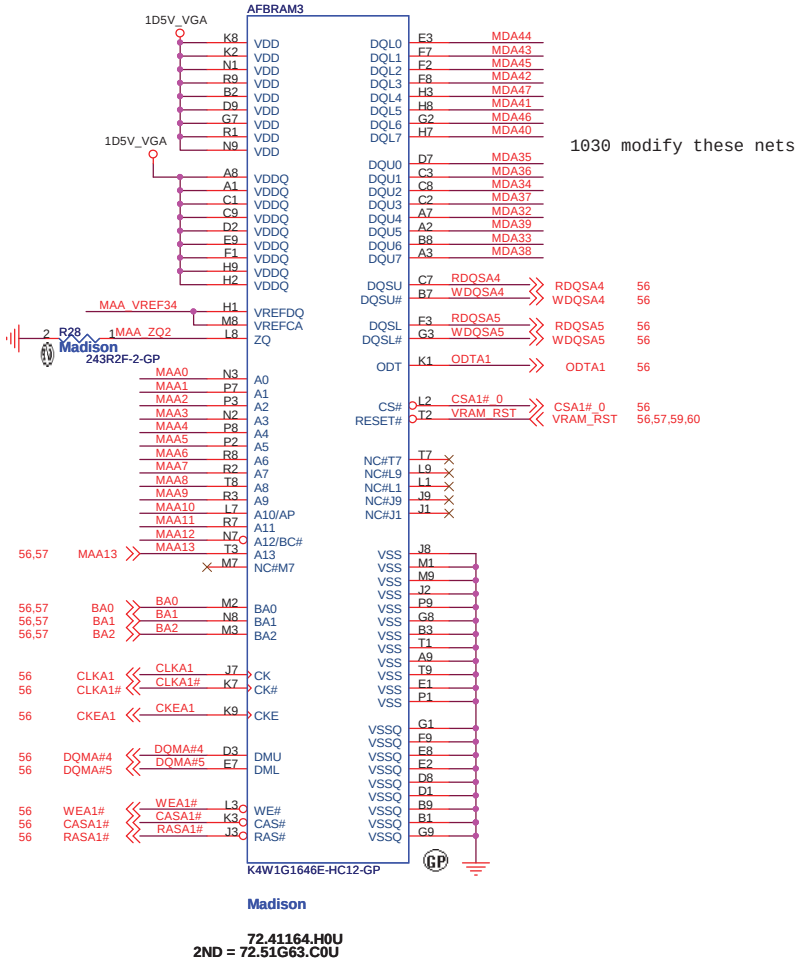
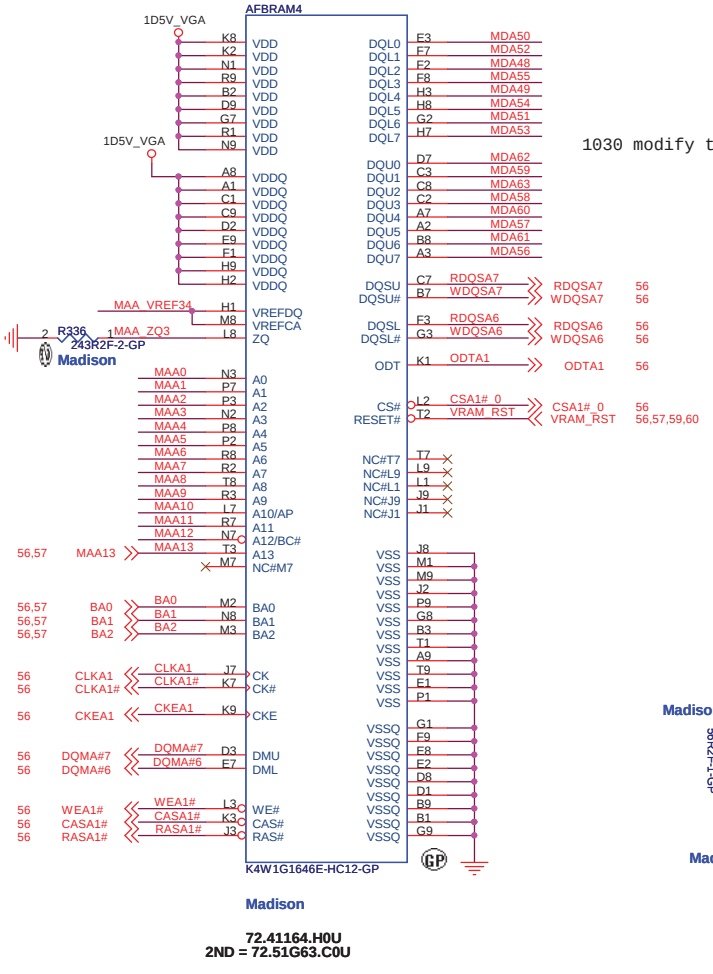
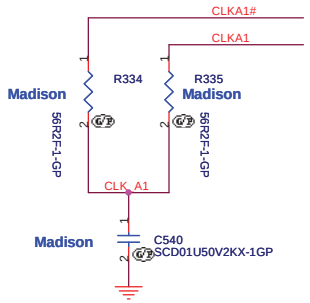
DDR3



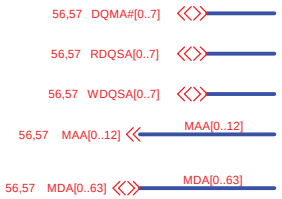
1030 modify these nets

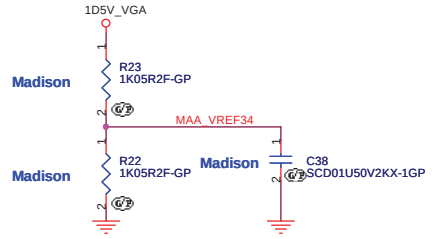


1030 modify these nets



SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





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Title	*VRAM(2/4)*	
Size A3	Document Number **JE70-DN**	Rev SB
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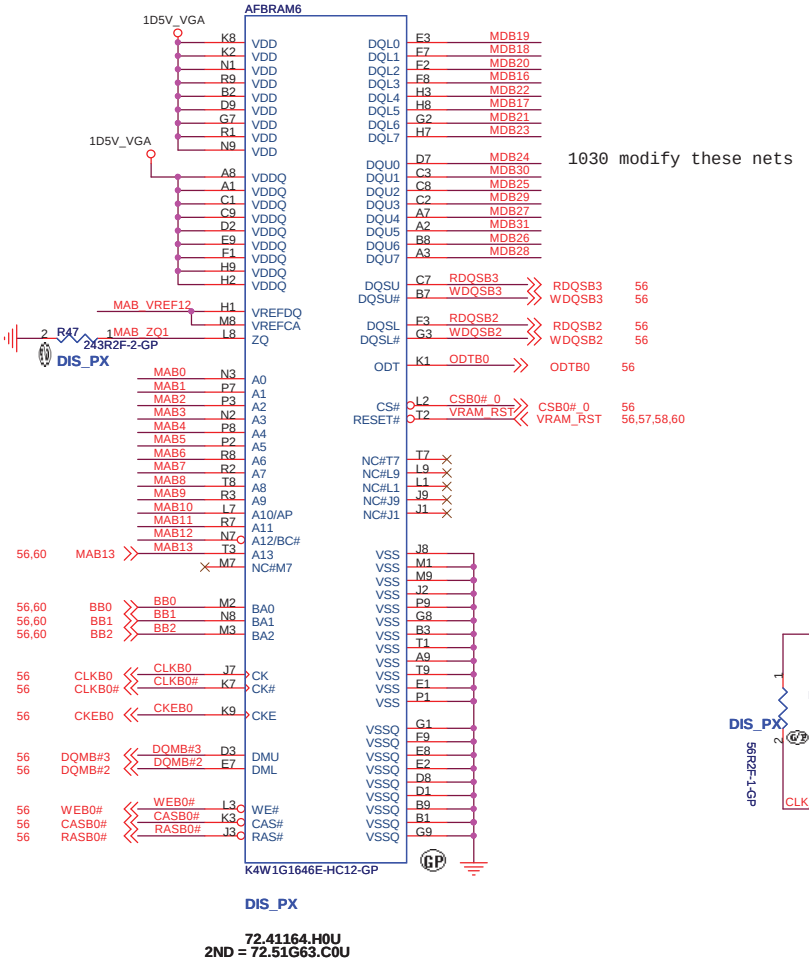
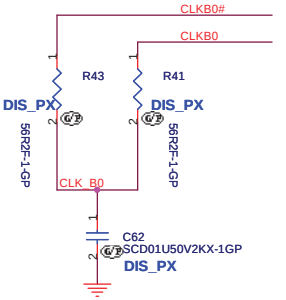
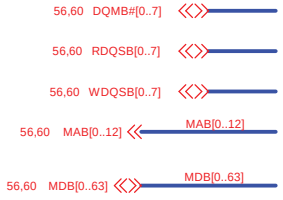
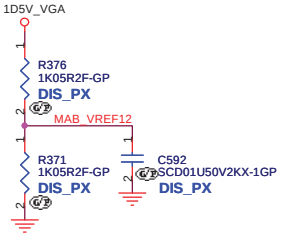
DDR3





SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





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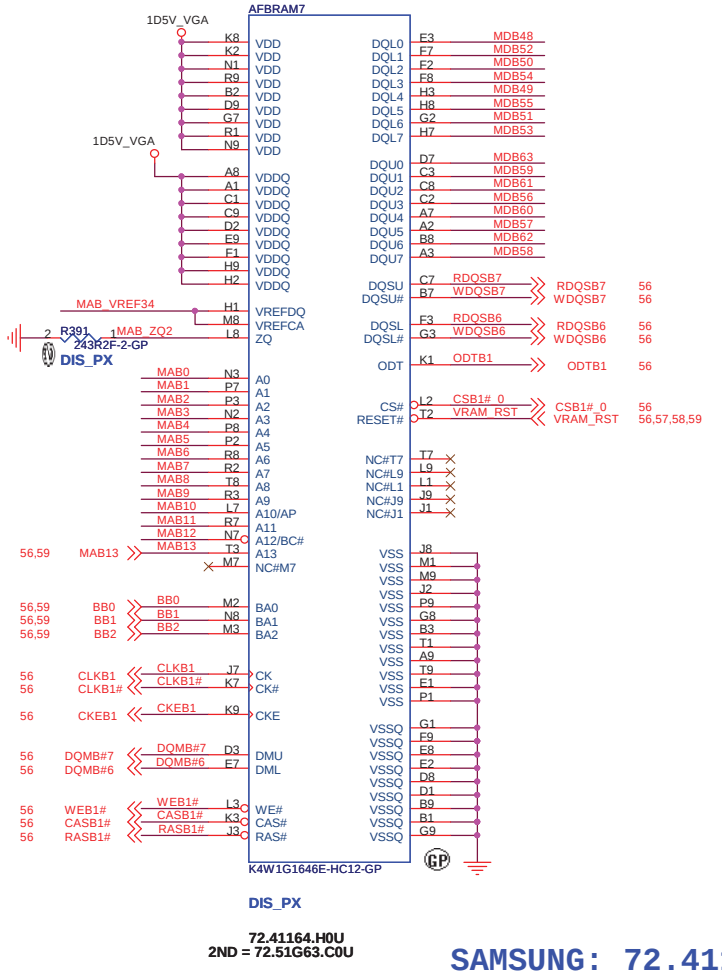
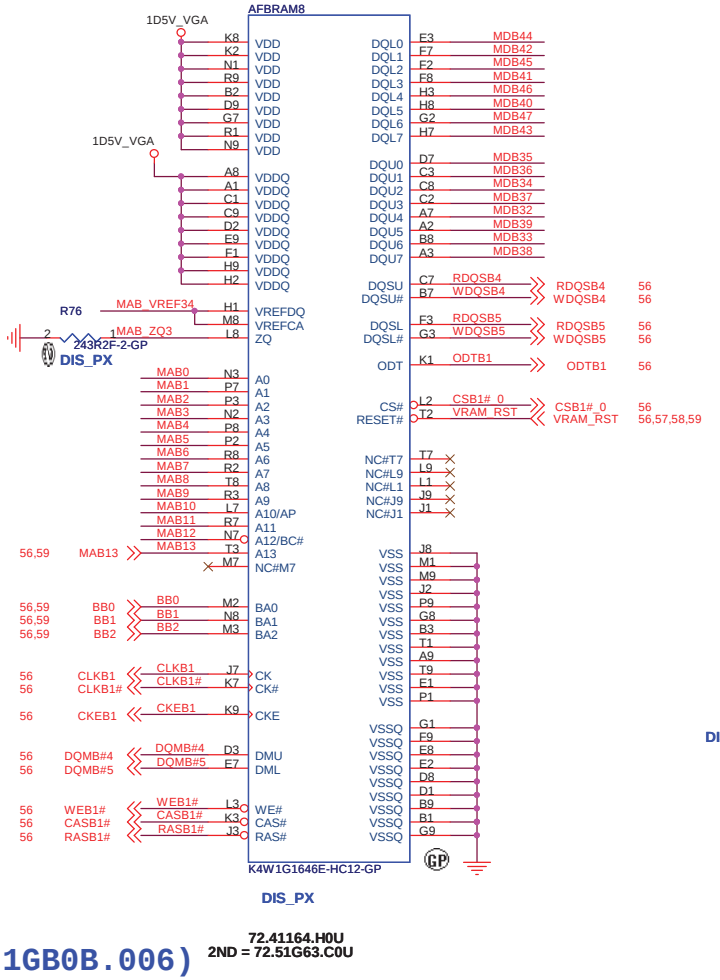
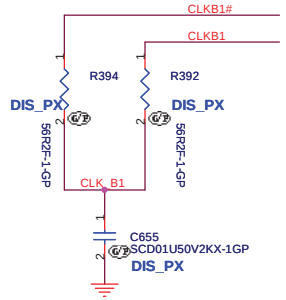
Title	VRAM(3/4)	
Size A3	Document Number JE70-DN	Rev SB
Date: Tuesday, February 23, 2010	Sheet 59 of 63	

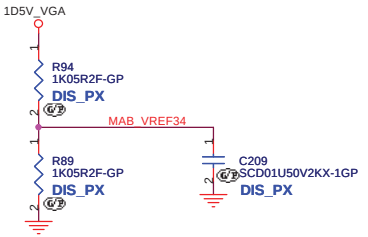
DDR3





SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





56,59 DQMB#[0..7]

56,59 RDQSB[0..7]

56,59 WDQSB[0..7]

56,59 MAB[0..12] MAB[0..12]

56,59 MDB[0..63] MDB[0..63]

JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***VRAM(4/4)***

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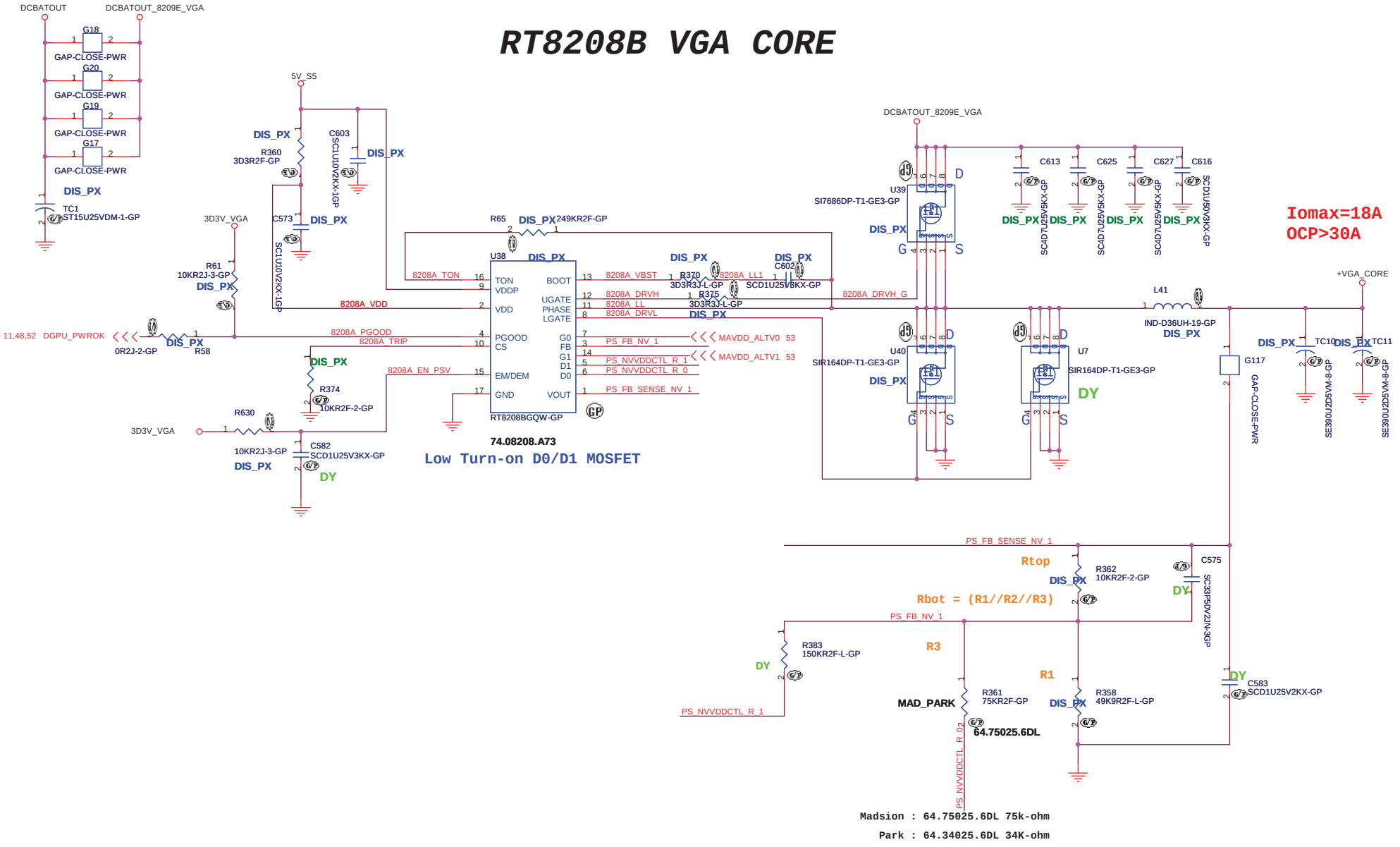
RT8208B VGA CORE



MAVDD_ALTV0	Madison Pro	Park XT
0	1.00V	1.12V
1	0.90V	0.90V

JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E_VGA_CORE

Size: A3 | Document Number: JE70-DN | Rev: SB

Date: Monday, March 01, 2010 | Sheet 61 of 63

1020

Page8: modify these nets for PCIE ports
Page11:add these nets(INT_VGA_EN#,EDP_EN)
Page11:add the net(PX_EN#) and R861
Page11:delete D41,R437,R435
Page12:modify these nets for USB ports
Page14:modify L45,L48,L52,L57,L58,L60
Page18:delete RN95,R423 and add Q73~Q76,R862~R864,D45
Page19:delete CCD1 conn and modify these nets for CCD
Page19:add R865,R866,U100
Page20:add Q77,R867
Page24:add modify these nets for BT
Page25:add modify these nets for USB board
Page26:modify these nets for PCIE port(LAN)
Page26:delete the net(LOW_PWR)
Page33:modify these nets for PCIE ports(MINI1,MINI2)
Page33:modify these part's names
Page33:modify these nets for USB port(MINI2)
Page40:1020 modify PWR_LED1,CHARGER_LED1
Page51:add screw holes

1021

Page5:modify these nets
Page6:delete HDT1 conn and add TP246~255
Page16:modify these nets of ADM1
Page16:add R880~883
Page17:modify these nets of ADM2 and ADM3
Page17:add R884~R891
Page18:add RN114~117
Page23:modify ODD1
Page25:modify the net(COVER_SW#_1)
Page30:modify LOUT1,AMIC1 and MICIN1
Page33:modify AMINI1 and MINI2
Page36:modify these nets and add R873~878
Page38:modify these devices(ATPCN1,SW_R,SW_L)
Page40:modify PWR_LED1,CHARGER_LED1
Page49:add D46
Page50:modify DCIN1, BAT1 and add R879

1021

Page26:modify U6(LAN IC)

1023

Page12:delete R538,R539 and add RN118
Page12:delete R442,R443,R445 and add RN119
Page12:delete R570~R572 and add RN120
Page12:delete C368~C371,C446,C449,C686,C687
Page18:swap these nets
Page21:add R892~R900,Q78
Page25:delete TC29,TC24,EC79,EC83
Page25:modify the net of USBCN1 pin32
Page36:delete R258 and RN89,RN122
Page36:delete R382 and add U101
Page36:delete R892,R483,R497,R478 and add RN123
Page36:delete R410,R416 and add RN121,R892
Page37:add R901,R902
Page40:modify the pin5 define of PWR_CN1 and Q11
Page43:add TC53,TC54,U44
Page61:modify TC52, R295 and add R903,Q79

1026

Page3: add R904 and modify C509,R232,R235
Page6: add R913,RN124
Page6: modify RN42,RN84,R612,R611,R364
Page17:modify these nets
Page19:modify R588
Page21:modify U73 and delete R504
Page22:modify SATA1
Page35:delete R311 and modify FAN1
Page36:modify RN121
Page36:modify AKB1
Page37:modify RN94 and the net(SPI_WP#)
Page43:add R097~R911,D47,Q80
Page53:add R905,R906

1027

Page10:delete C651,R320,R316
Page11:modify C543,C306,C424,C433
Page11:delete R148
Page12:modify the net(PM_RSMRST#)
Page43:modify the net(PM_RSMRST#)

1028

Page3:add the net(LAN_CLKREQ#)to RN70
Page4:modify C704~C706
Page4:modify R401
Page9:delete R576,R578
Page10:modify C62,C91
Page11:delete R207,C337,D5,R208
Page11:delete the net(PCI_REQ#6)
Page12:delete RN120 and add R570
Page13:modify the net(SATA_LED#)
Page14:add C1198,C1199 and modify C815,C811
Page16:add R934,R935
Page18:add U102,R915~R919
Page18:modify R432,U3,U8
Page19:add U103,R920~R922 and delete D35
Page20:add R936,R937 and modify R325,R323,R354
Page21:delete RN8,RN13,RN15,RN19
Page21:modify C819~C821,C823,C824,C826~C828
Page25:add L82,R924,R925
Page29:modify R489
Page30:modify R622,R619 and add RN125
Page36:delete R384 and modify the net(KBC_BL_ON_IN)
Page36:add R926
Page43:delete R583,D33,U74,R340,Q34,R584
Page43:add R930~R933,Q84,Q85,C1197
Page43:add R927~R929,Q8~Q83
Page43:delete R591~R595
Page48:modify these nets(DGPU_PWROK,9025_POK)

1029

Page6:delete R364,R612 and add RN127,R946
Page16:delete C331,C338
Page17:delete C348,C340,C350,C342
Page18:modify these nets
Page19:add EC99,EC100
Page24:add EC101,EC102
Page25:add L82,R924,R925,R939,EC103
Page35:delete D17,D18,U39,U43,R298,R322,R330,R338,R337,C646,C656
Page35:delete U38,R321,R308,R309,R314,C645
Page36:add R945,RN126
Page43:delete U44,R342,C675
Page47:modify the net
Page48:modify R582 and add R938
Page50:add D48
Page53:add R940~R943
Page61:add R944,Q86

1030

Page3:modify these nets
Page8:modify these nets
Page11:modify the net
Page12:add R949
Page14:delete C760,C721,C805,C800,C769,L64 and add R948
Page18:modify these nets
Page30:add R950~R953 and modify EC24,EC51
Page57:swap these nets
Page58:swap these nets
Page59:swap these nets
Page60:swap these nets

1102

Page3:swap these nets
Page6:swap these nets
Page12:swap these nets
Page13:swap these nets
Page18:swap these nets
Page25:modify USBCN1
Page30:modify these names of these nets

1103

Page3:modify X5,C508,C509
Page11:modify R164
Page14:modify L51,L59
Page21:modify these names of nets
Page21:add RN8,RN13,RN15,RN19
Page36:add the net(A_MIC_SUPPORT#)

1104

Page6:delete TP246~255 and add HDT1
Page9:modify the value of RN11
Page24:add AFTP(TP256~TP258)
Page24:add AFTP(TP259~TP263)
Page25:add AFTP(TP264~TP280)
Page35:add AFTP(TP281,TP282)
Page36:add AFTP(TP283~TP307)
Page38:add AFTP(TP308~TP312)
Page40:add AFTP(TP313~TP319)
Page56:modify these values of R724,R725

1105

Page3:delete R191~R194,R198~R200,R204~R206
Page3:delete R214,R213,R187~R190,R220,R222
Page3:add RN128~RN136
Page3:modify R215,R197,R238,R229
Page6:delete R104,R105,R108,R110
Page6:add RN137,RN138,R954
Page6:modify R366
Page6:modify Q8,R81,R375,C205
Page8:delete TP16,TP17,TP20,TP21
Page9:add R955,R956 and modify R29
Page11:delete R144,R141,R137,R138
Page12:add the net(SUS_STAT#) and R957
Page12:modify these nets
Page21:swap these nets
Page28:modify C713,R634 and delete R626
Page33:modify these nets
Page33:modify R879

1106

Page3:modify these values of R169,R170
Page12:add R957,R958
Page12:add these nets(USB_OC#0,USB_OC#2,USB_OC#3)
Page16:modify R880~R883,ADM1
Page17:modify R888,R890,ADM2
Page21:add R959
Page35:modify FAN1
Page35:modify PWR_CN1
Page35:modify ATPCN1
Page36:swap these nets(KBRCIN#,KA20GATE)
Page37:swap RN94
Page44:swap RN45
Page51:add EC104~EC112 for EMI demand

1107

Page3:swap RN129,RN130,RN132
Page6:swap RN137
Page51:add EC104~EC112 for EMI demand

1109

Page45:modify the value of R448 to 64.15035.6DL for Power team demand
Page45:modify R462,R470 for Power team demand
Page46:modify L25 for Power team demand
Page48:modify C1032,C1194

1110

Page5:swap RN48
Page7:add C1200~C1207
Page11:add R960,R961
Page25:modify USB1
Page43:add TC55,TC56
Page52:add R962

1111

Page11:add R965
Page21:modify HDMI1
Page28:add R626
Page33:delete C550,C549 and add R963
Page36:delete RN121 and add R964
Page45:modify TC39,TC40
Page48:add R966,Q87,C1208,R967,R968,Q88

1112

Page13:modify the net
Page48:delete R968,Q88
Page48:modify R819,R820,R966
Page48:modify the net

1113

Page3:delete R170,EC50
Page25:delete R939,TP272,EC103
Page46:modify TC43
Page48:add R969
Page53:add R968
Page53:delete TP103,TP122,TP160,TP178
Page53:delete these TP(TP157,TP145...)
Page54:delete TP3~TP9

1117(Rename)

Page18:swap these nets
Page22:delete D29~D31,D33
Page36:modify RN31
Page61:delete G24~G29
Page61:modify the net

1118

Page14:add R620 and modify R184
Page15:modify R412,R411
Page36:swap AKB1 pin1~pin26

JE70-DN

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Title: HISTORY(1/2)

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SA to SB

1120

Page19: modify these nets
Page48: modify the net(9025_EN)

1124

Page38: modify ATPCN1

1126

Page25: modify these nets
Page36: add TP174