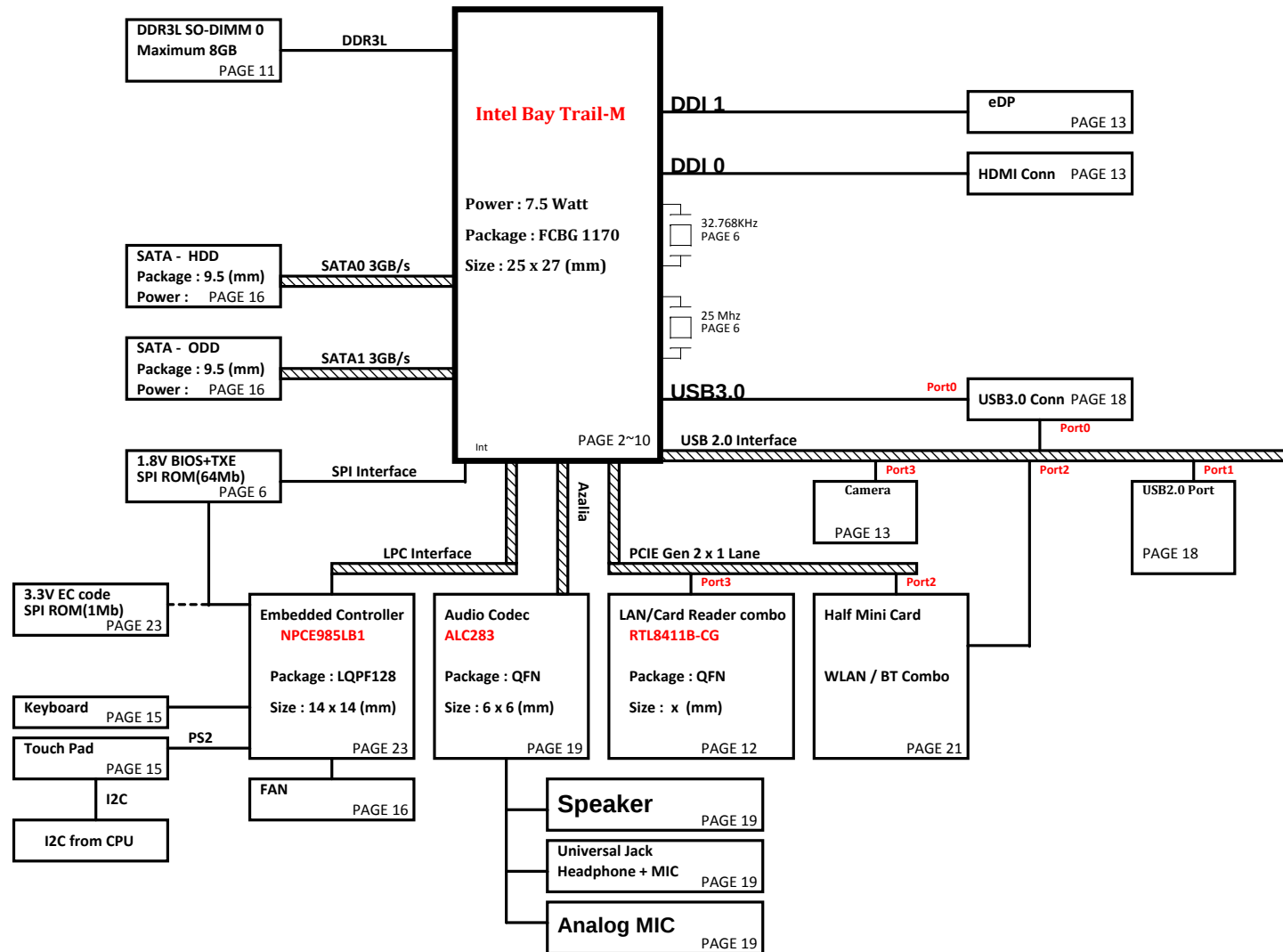


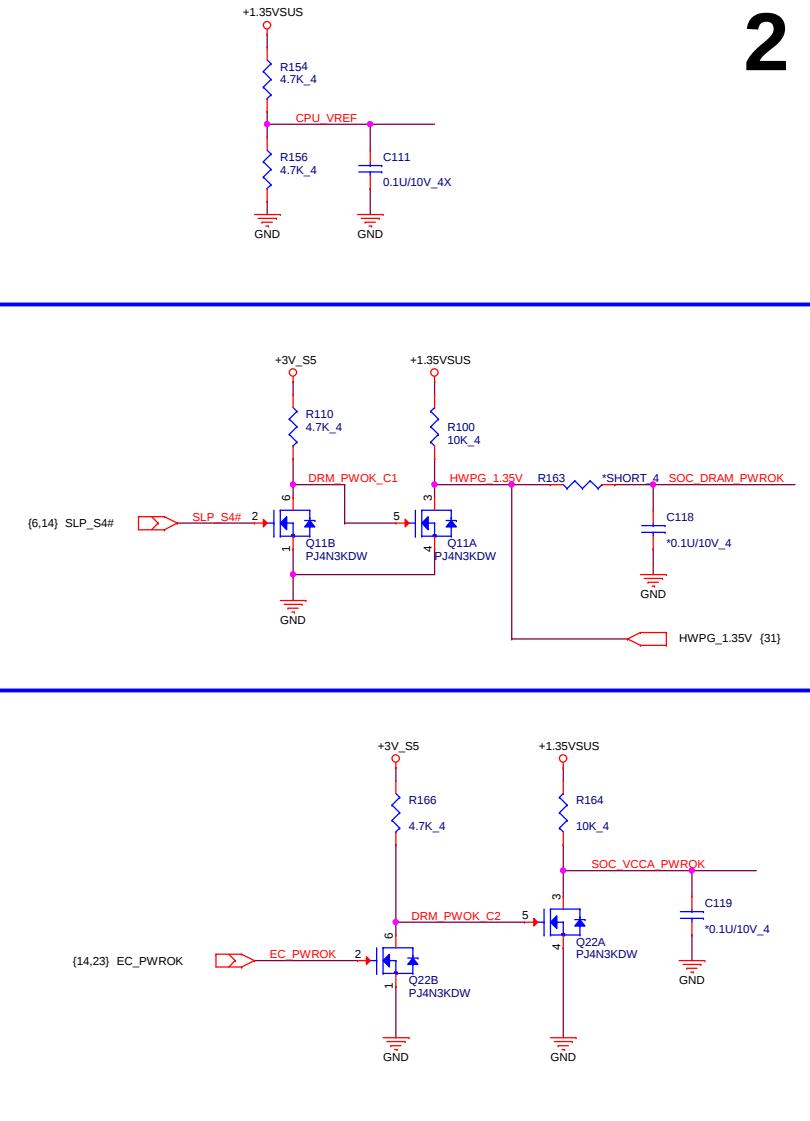
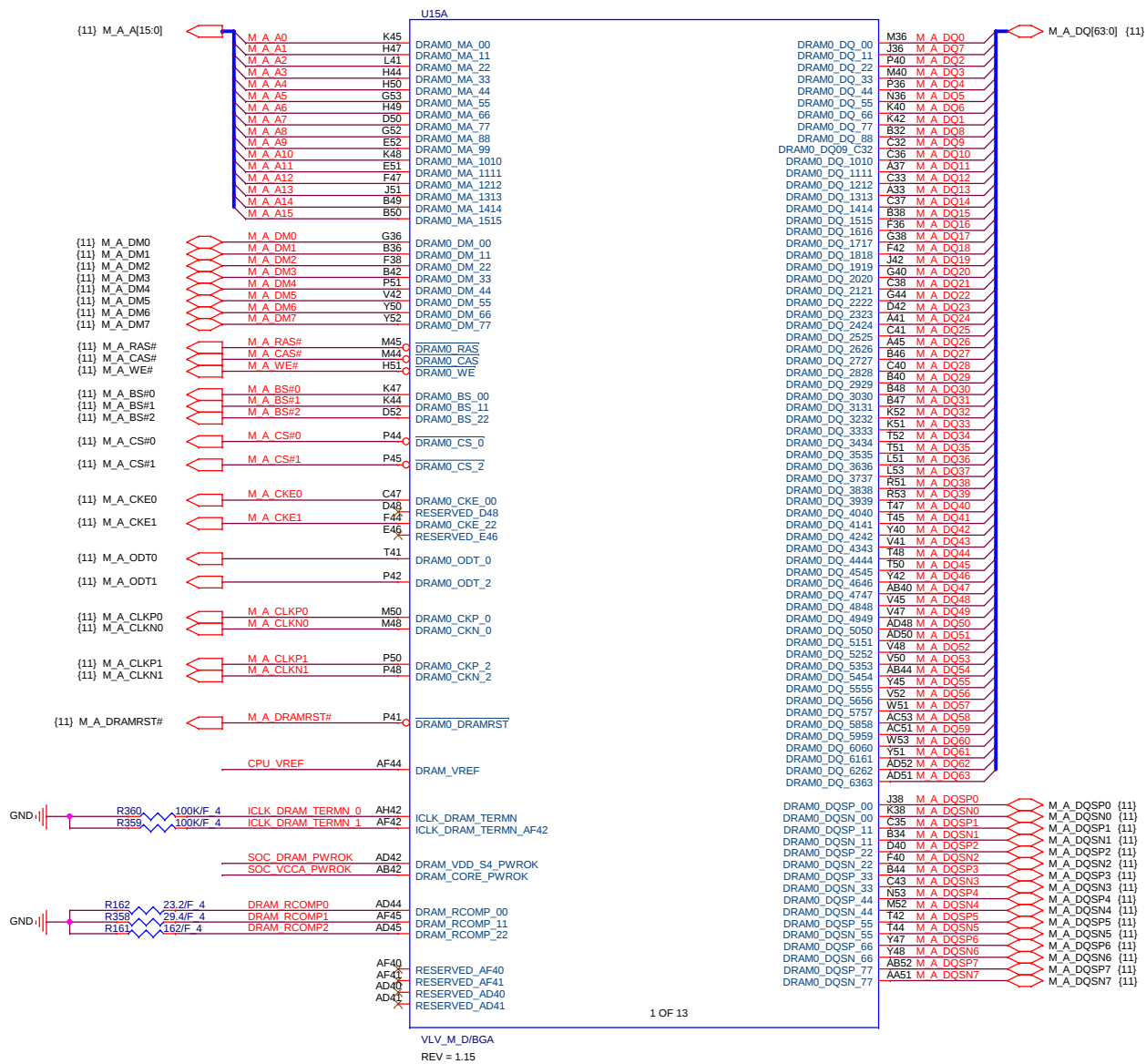
Z8A UMA(14")

Intel Bay Trail-M Platform Block Diagram

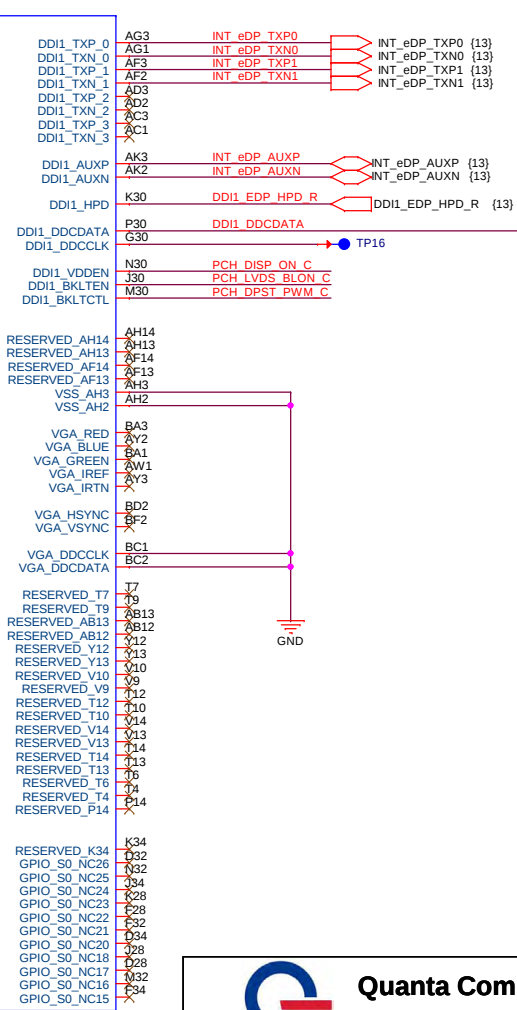
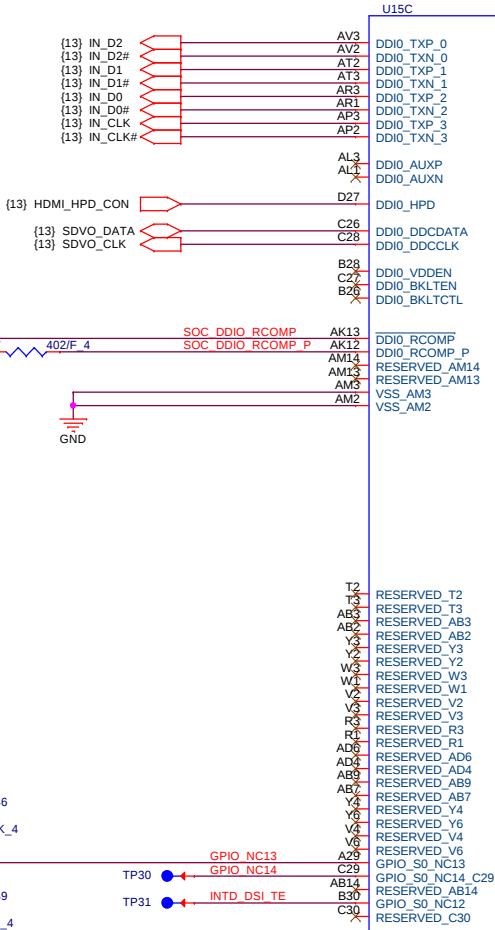
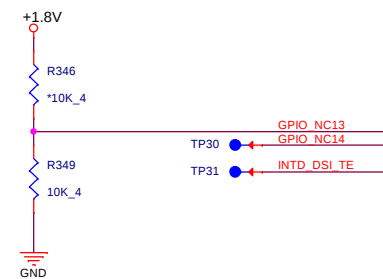
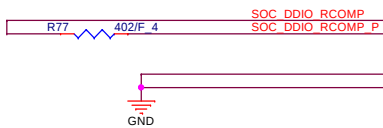
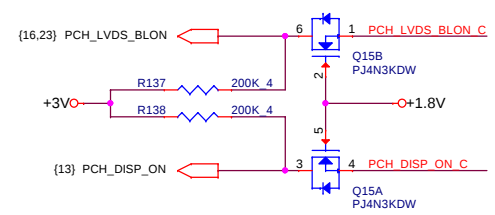
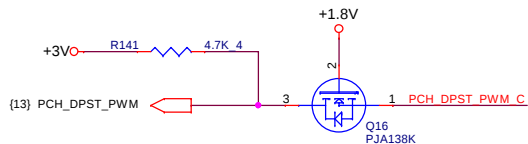
PCB 4L STACK UP

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : SGND
LAYER 4 : BOT





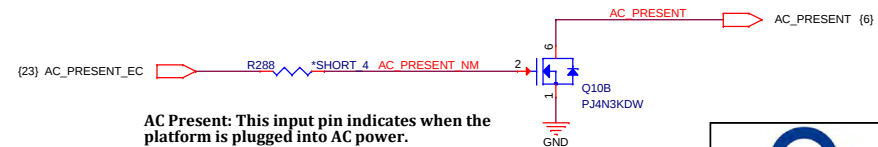
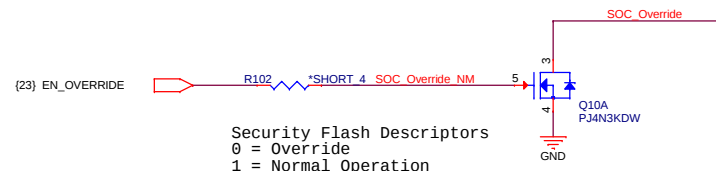
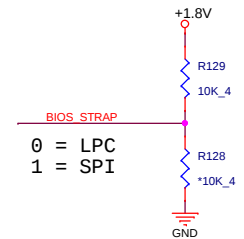
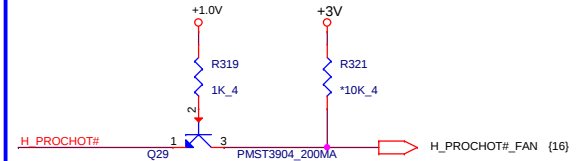
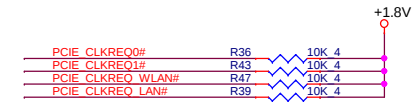
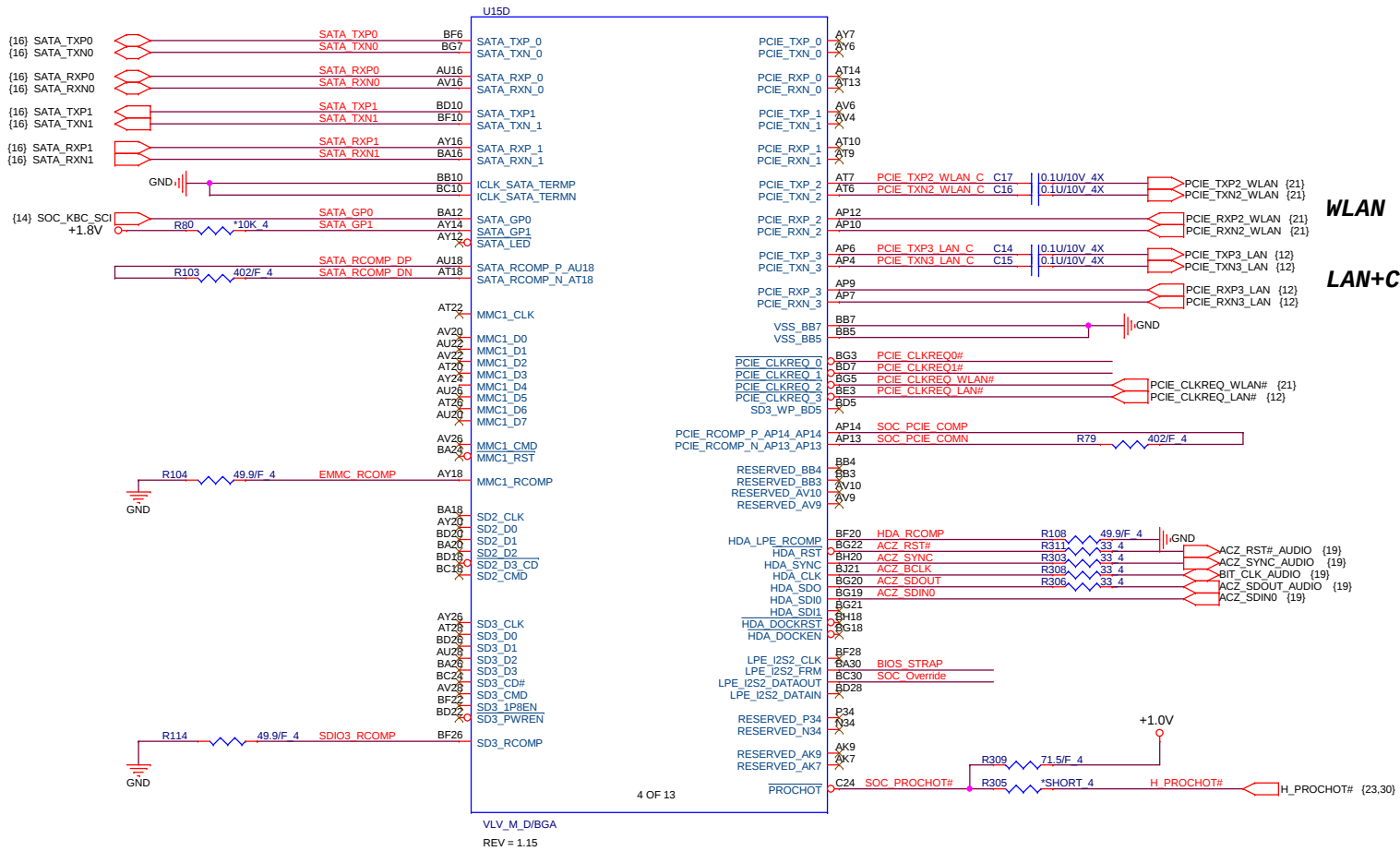
VLV_M_D/BGA
REV = 1.15

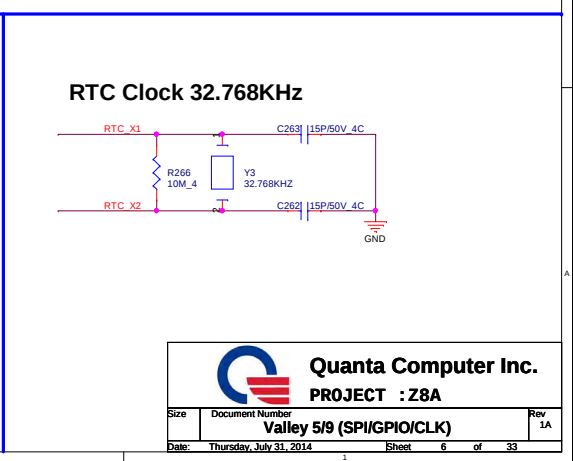
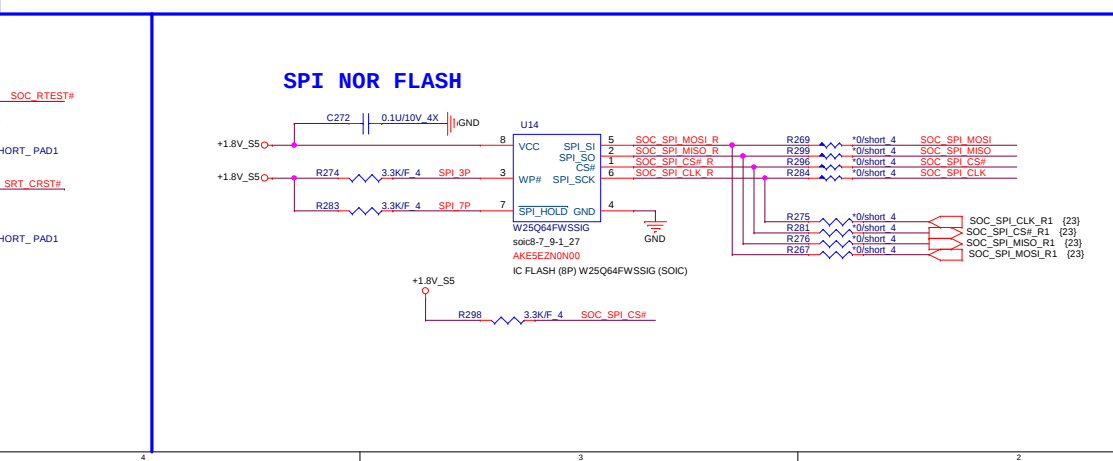
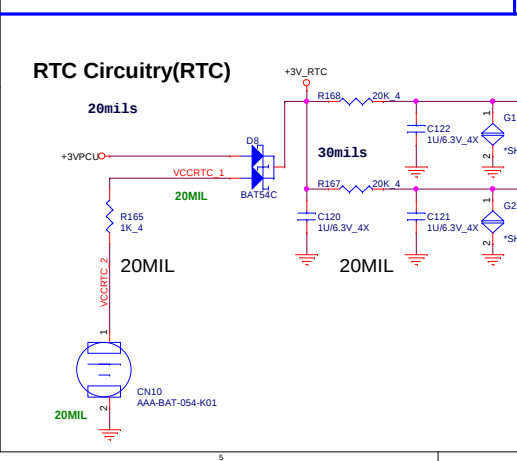
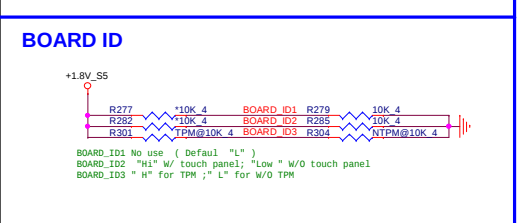
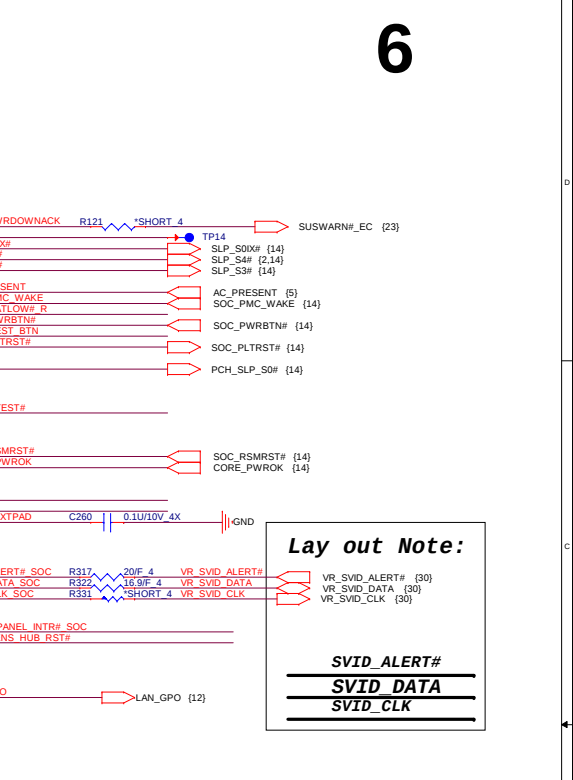
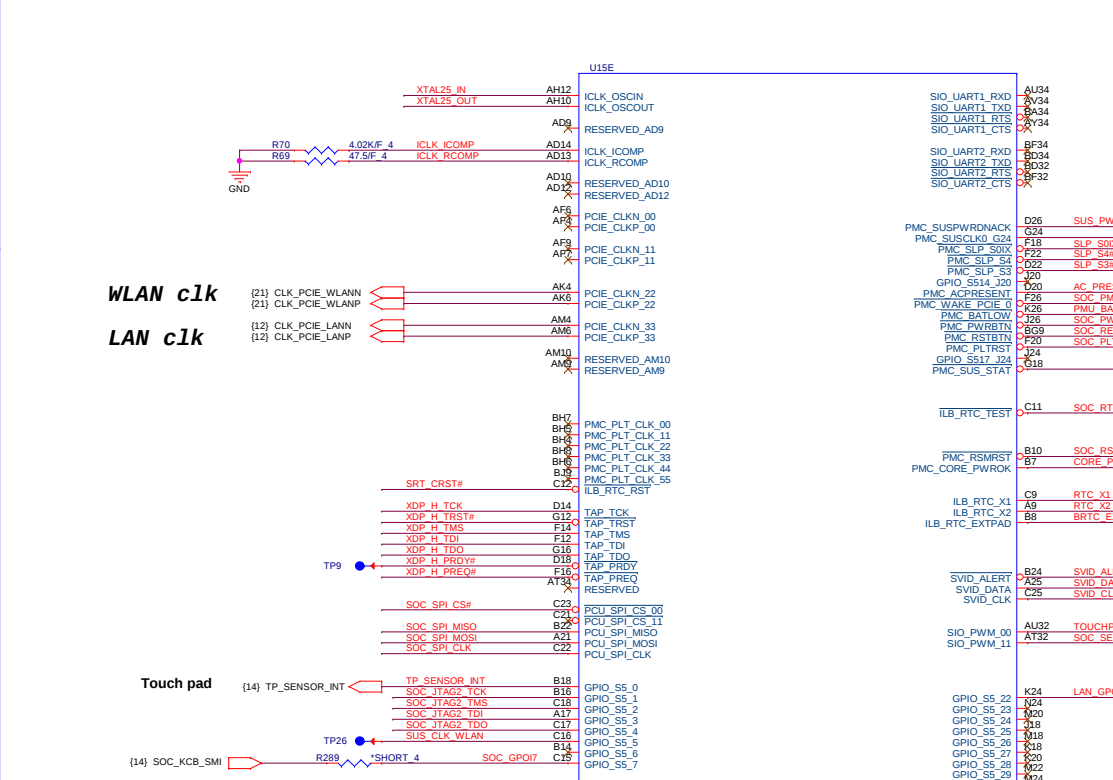
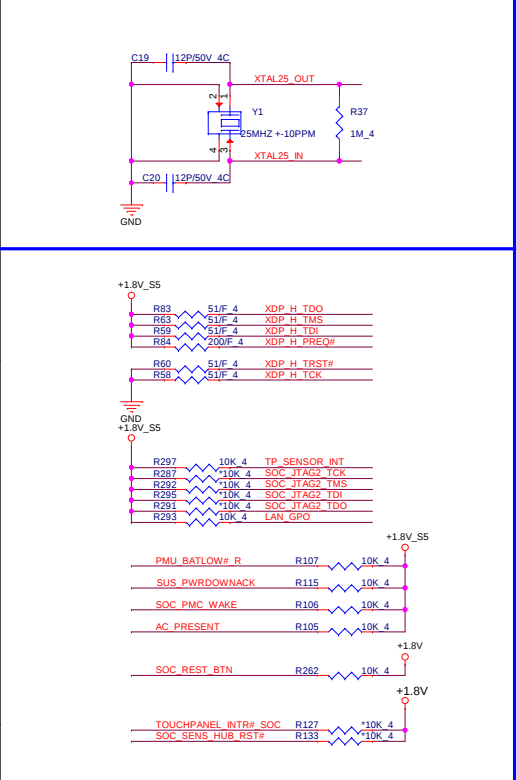




Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number	Rev
	Valley 3/9 (Display)	1A
Date:	Thursday, July 31, 2014	Sheet 4 of 33





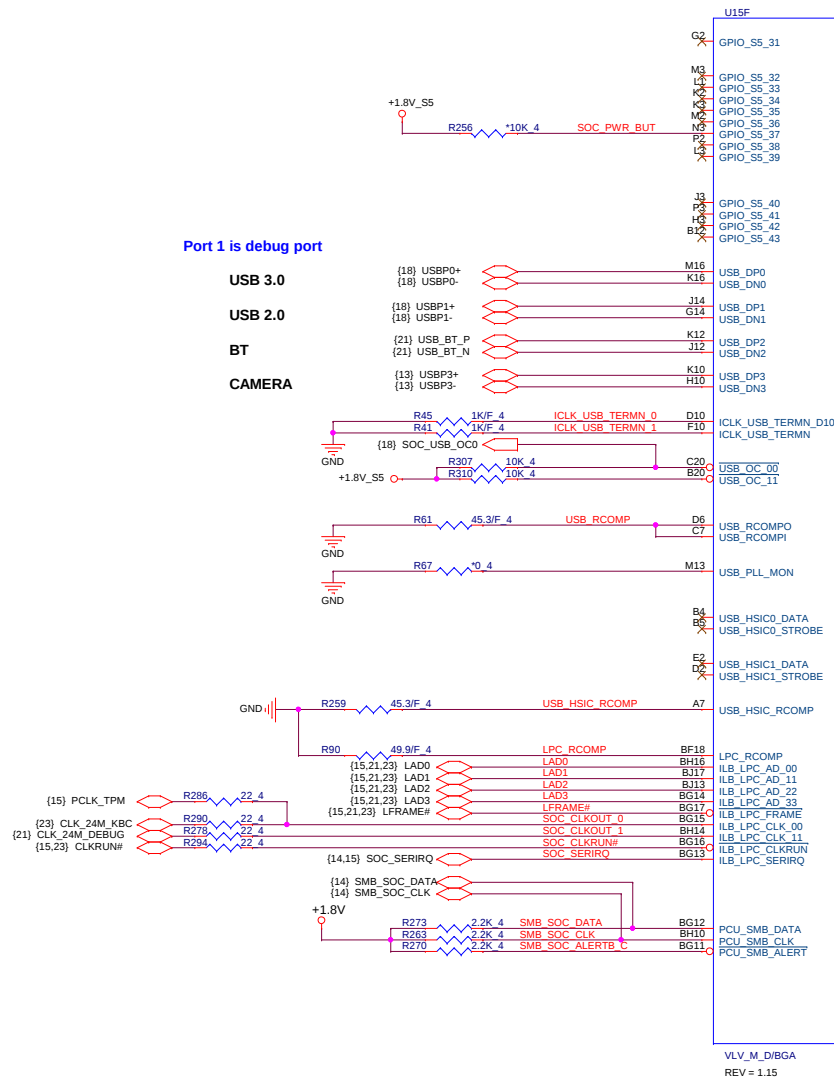
Port 1 is debug port

USB 3.0

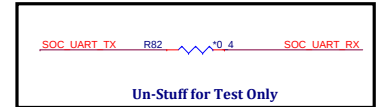
USB 2.0

BT

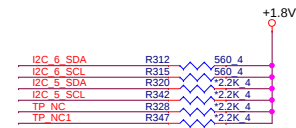
CAMERA



Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted



Un-Stuff for Test Only

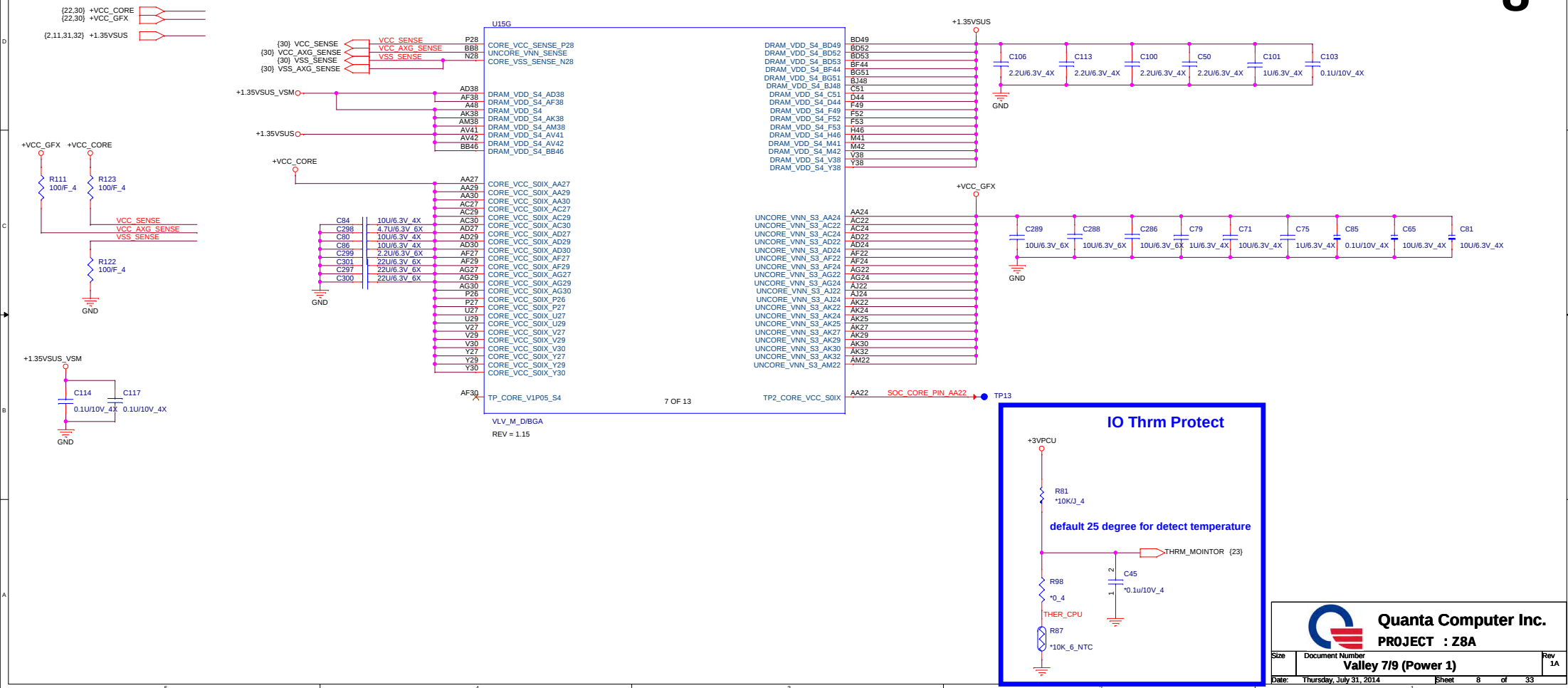


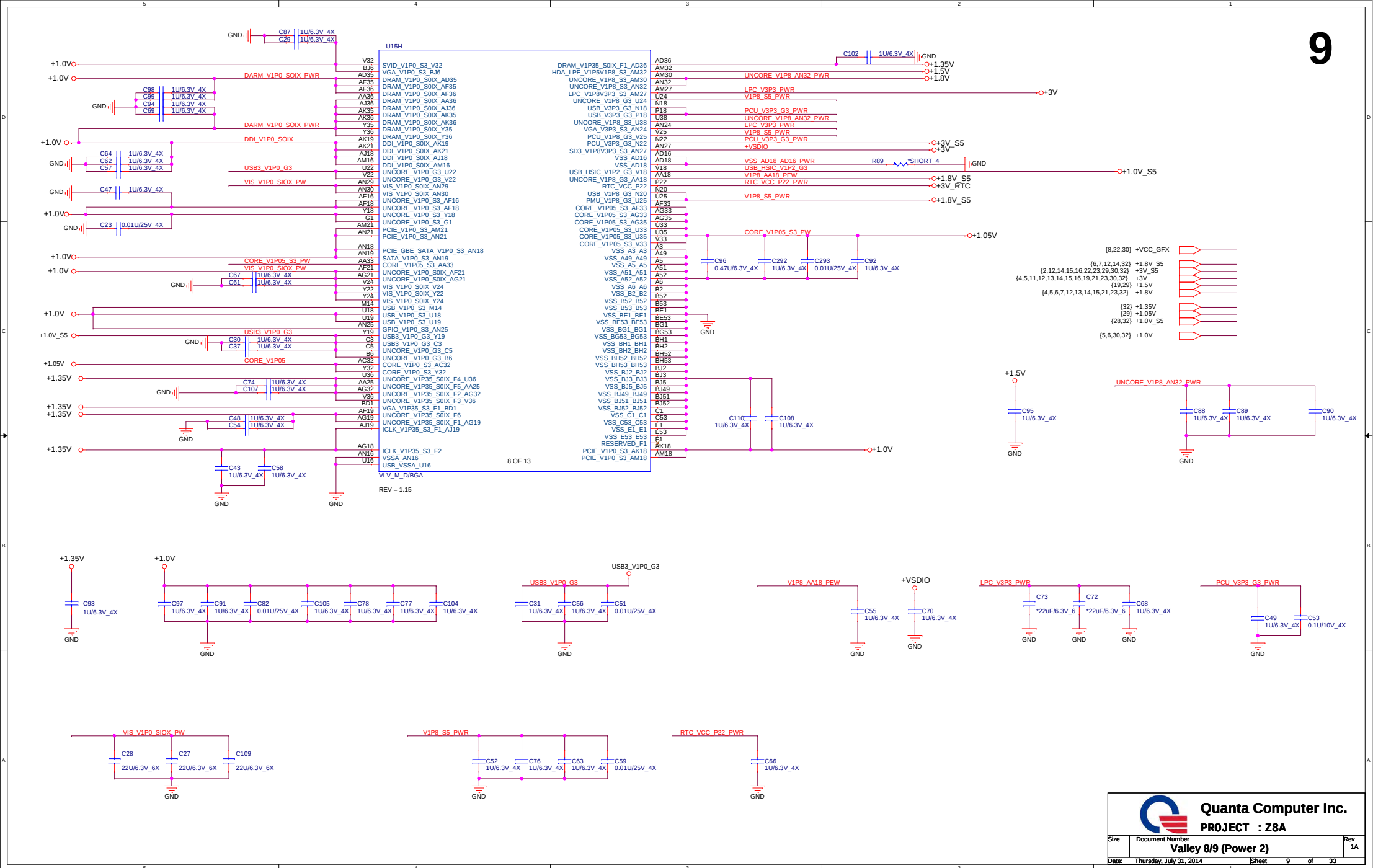
I2C pull up:
Standard/ Fast Mode --> 560 ohm
High speed mode --> CLK- 560 ohm;
DATA- 910 ohm

Quanta Computer Inc.

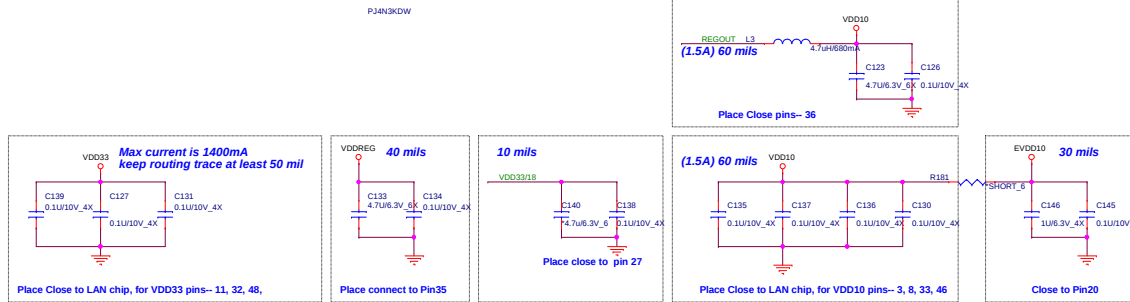
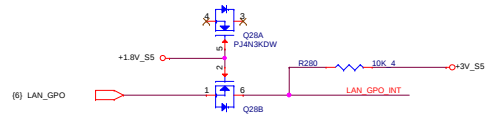
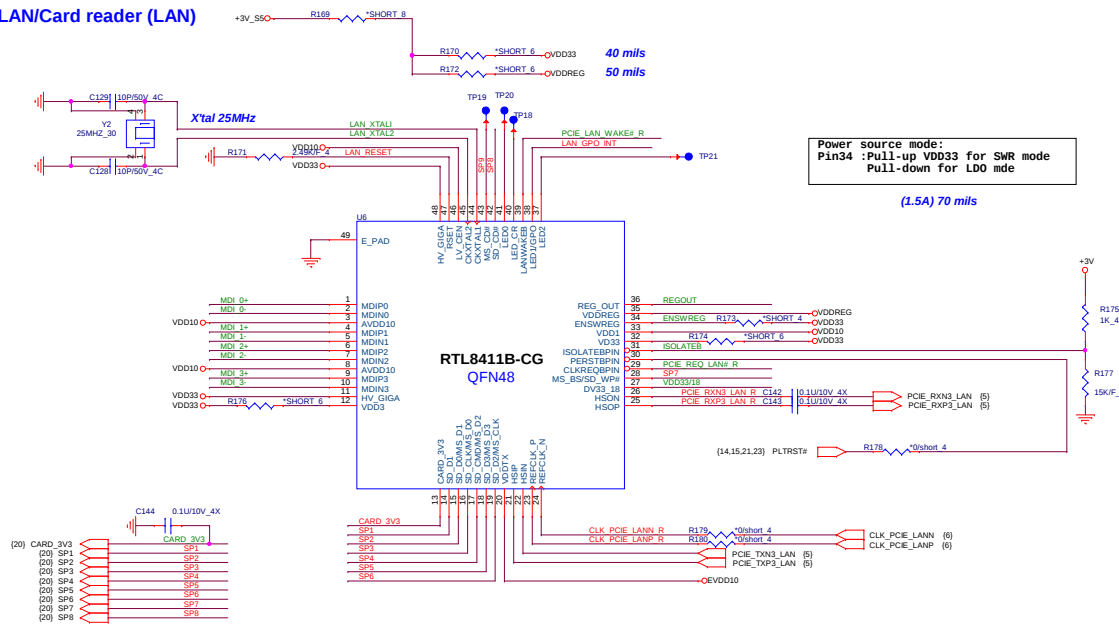
PROJECT : Z8A

Size	Document Number	Rev	1A
Valley 6/9 (USB/LPC/I2C)			
Date:	Thursday, July 31, 2014	Sheet	7 of 33

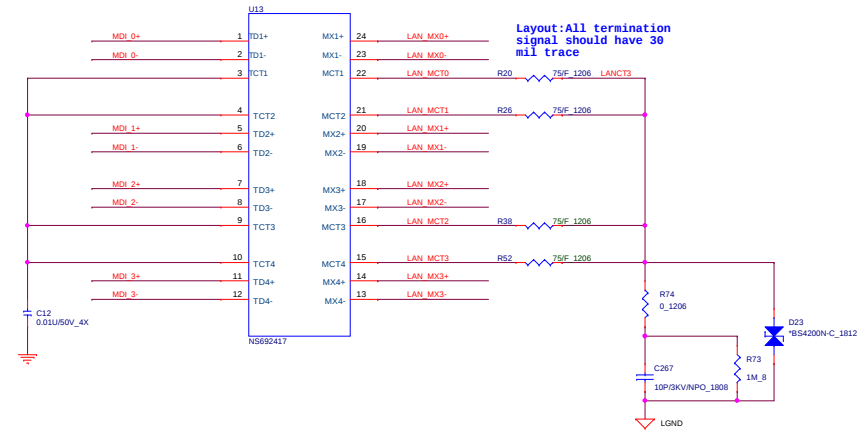




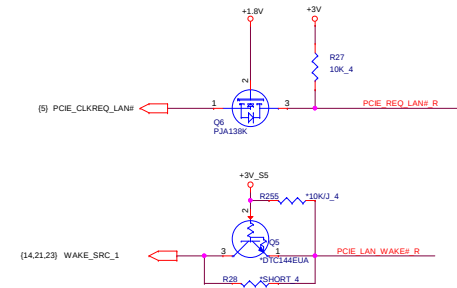
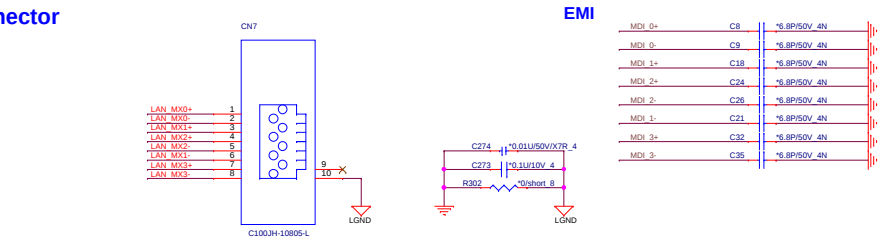
LAN/Card reader (LAN)



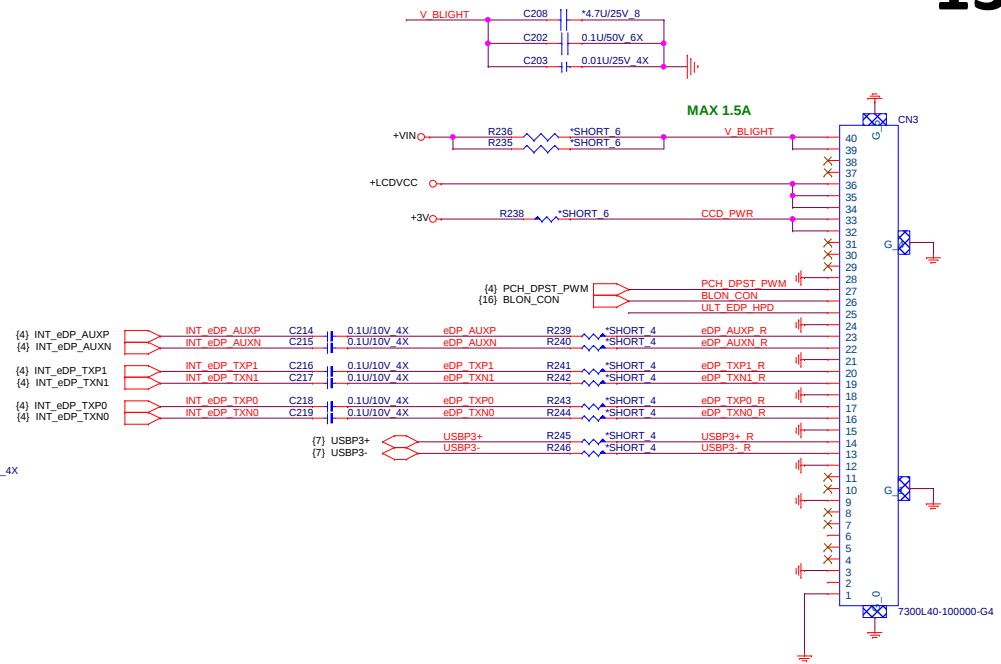
Transformer (LAN)



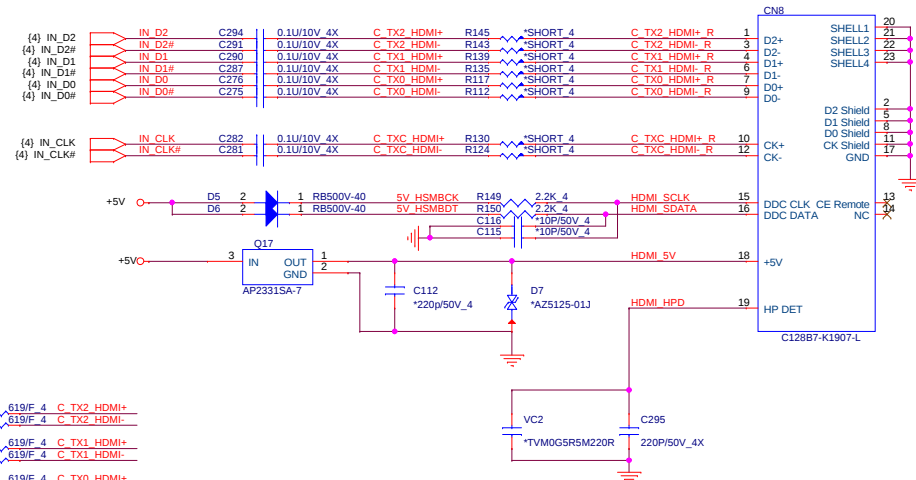
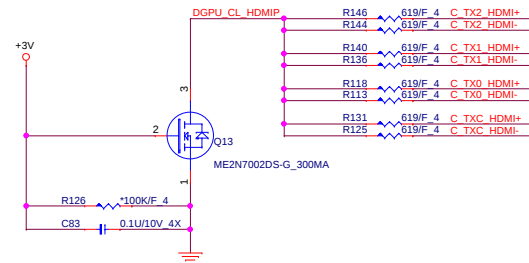
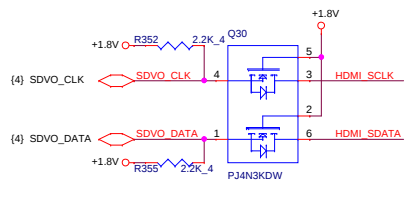
RJ45 Connector

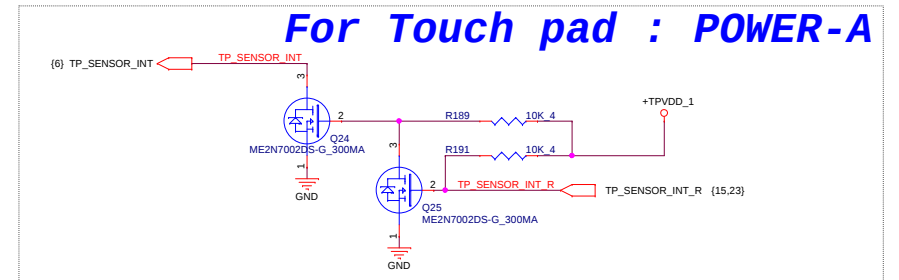
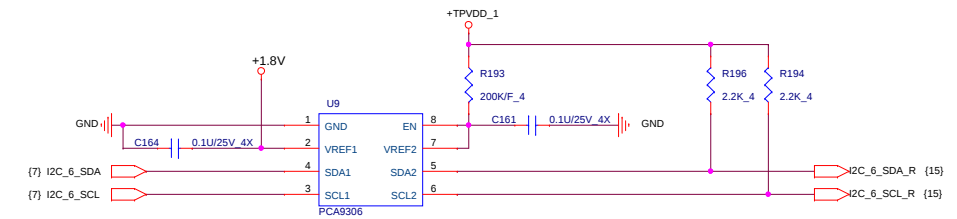
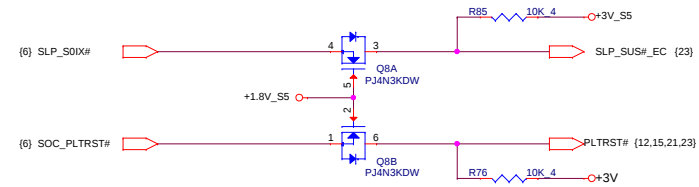
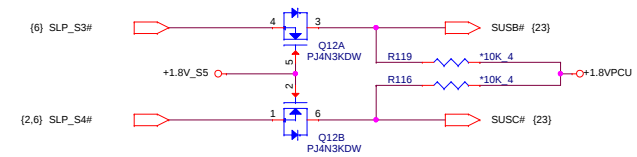
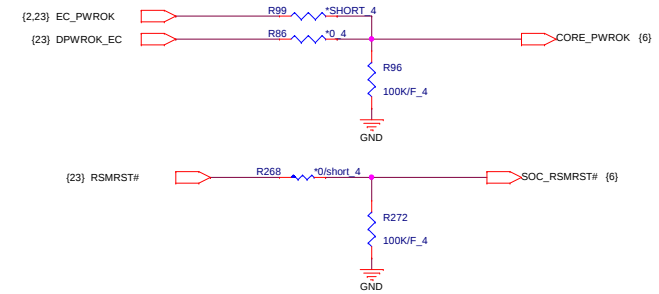
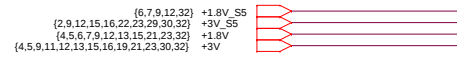
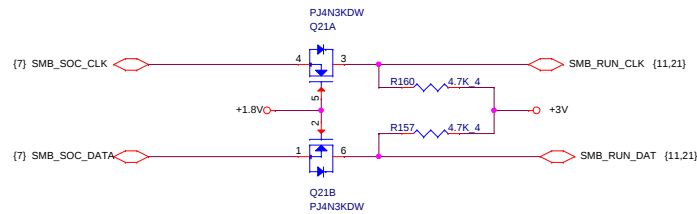
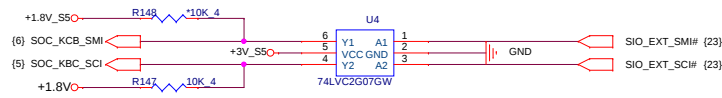
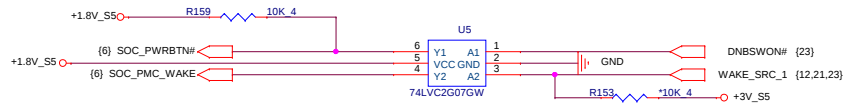
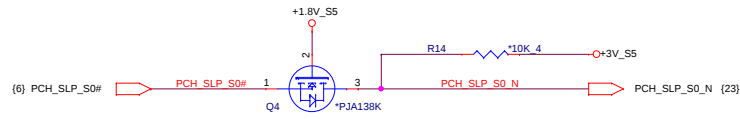
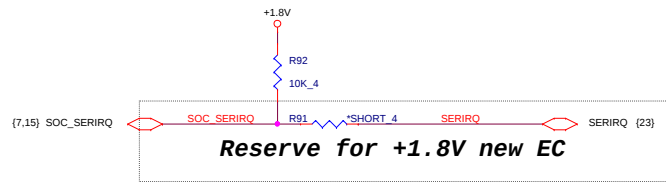


13



HDMI SMBus Isolation

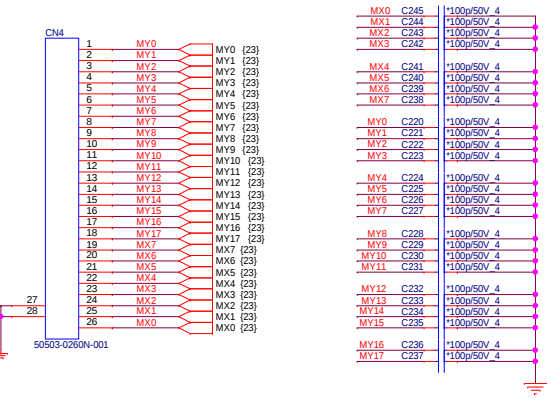




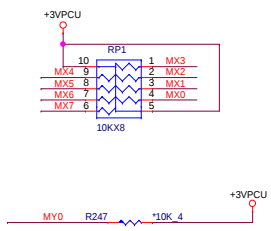
Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number	Rev
	Level Shifter	1A
Date:	Thursday, July 31, 2014	Sheet 14 of 33

KEYBOARD (KBC)



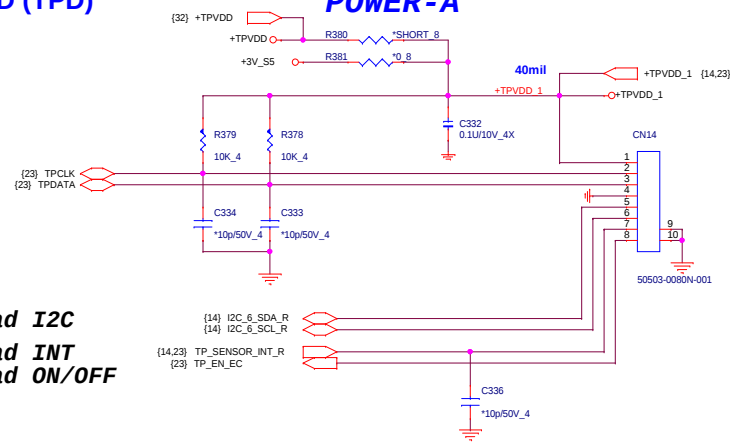
INTERNAL KEYBOARD STRIP SET (KBC)



TOUCH PAD (TPD)

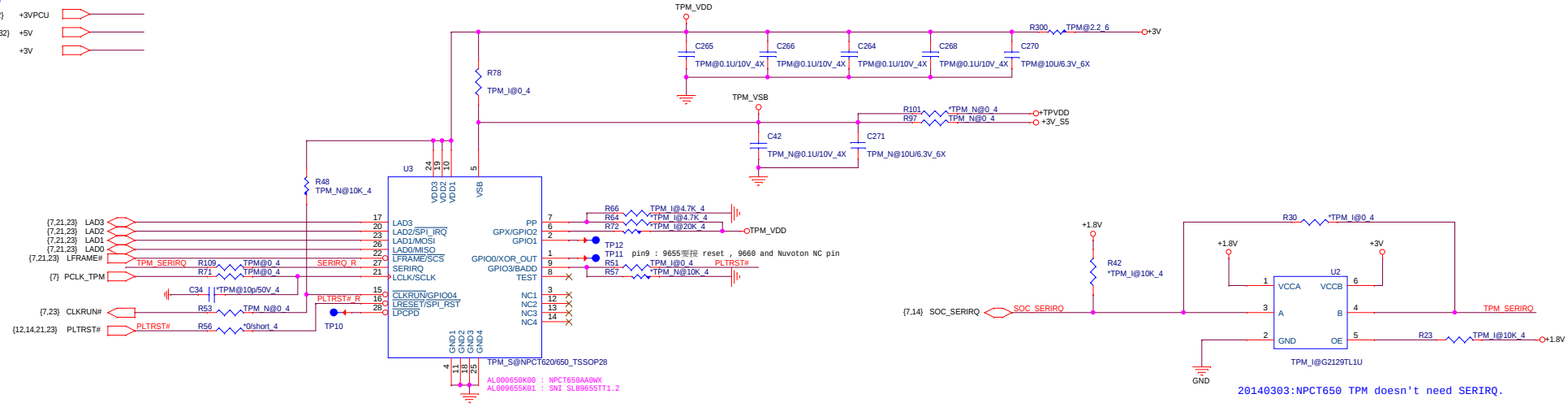
Touch pad I2C
Touch pad INT
Touch pad ON/OFF

POWER-A



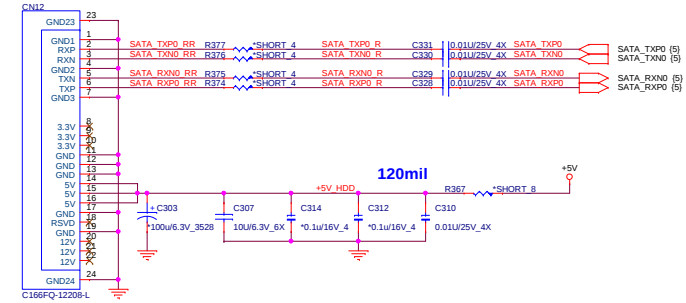
TPM (TPM)

{6,8,16,19,23,25,26,27,32} +3VPCU
{13,16,19,32} +5V
{4,5,9,11,12,13,14,16,19,21,23,30,32} +3V

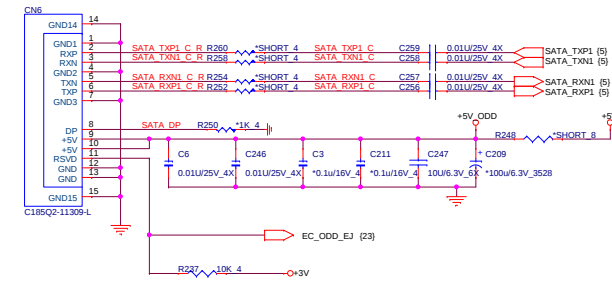


TPM_N for 新唐
TPM_I for 英飛凌---- default

2.5" SATA HDD (HDD)

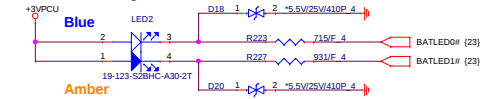


SATA ODD Connector

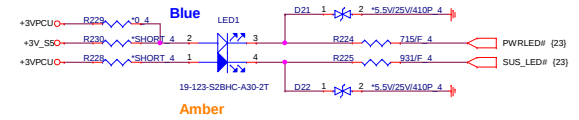


LED/SW (UIF)

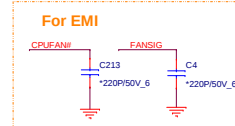
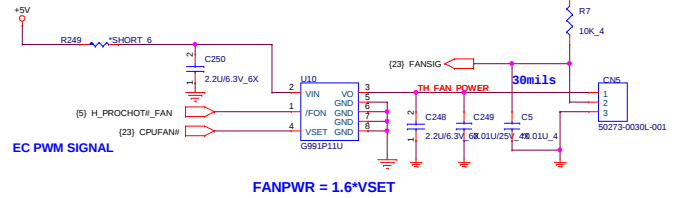
Battery indicator



PWR indicator

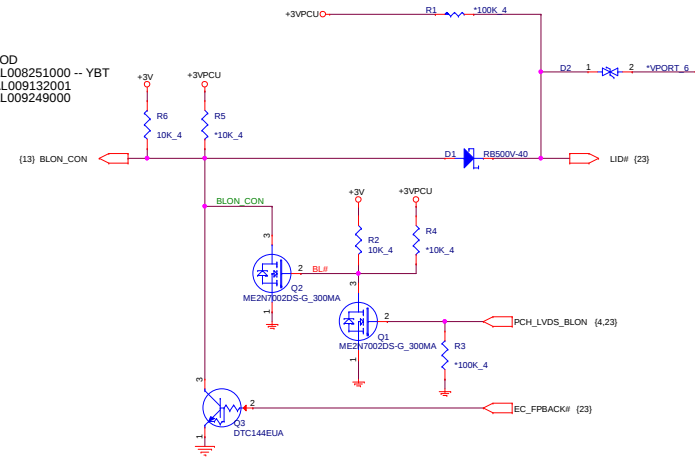


CPU FAN CTRL(THM)

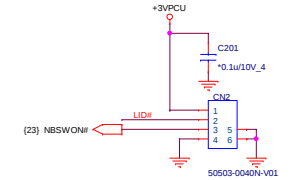


HALL IC (HSR)

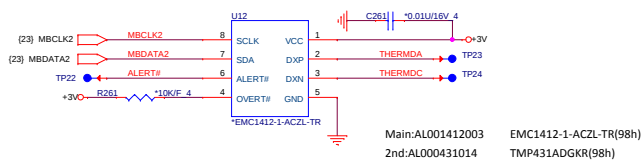
1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



PWR button DB CON



CPU Thermal sensor(THS) / MB Local TEMP



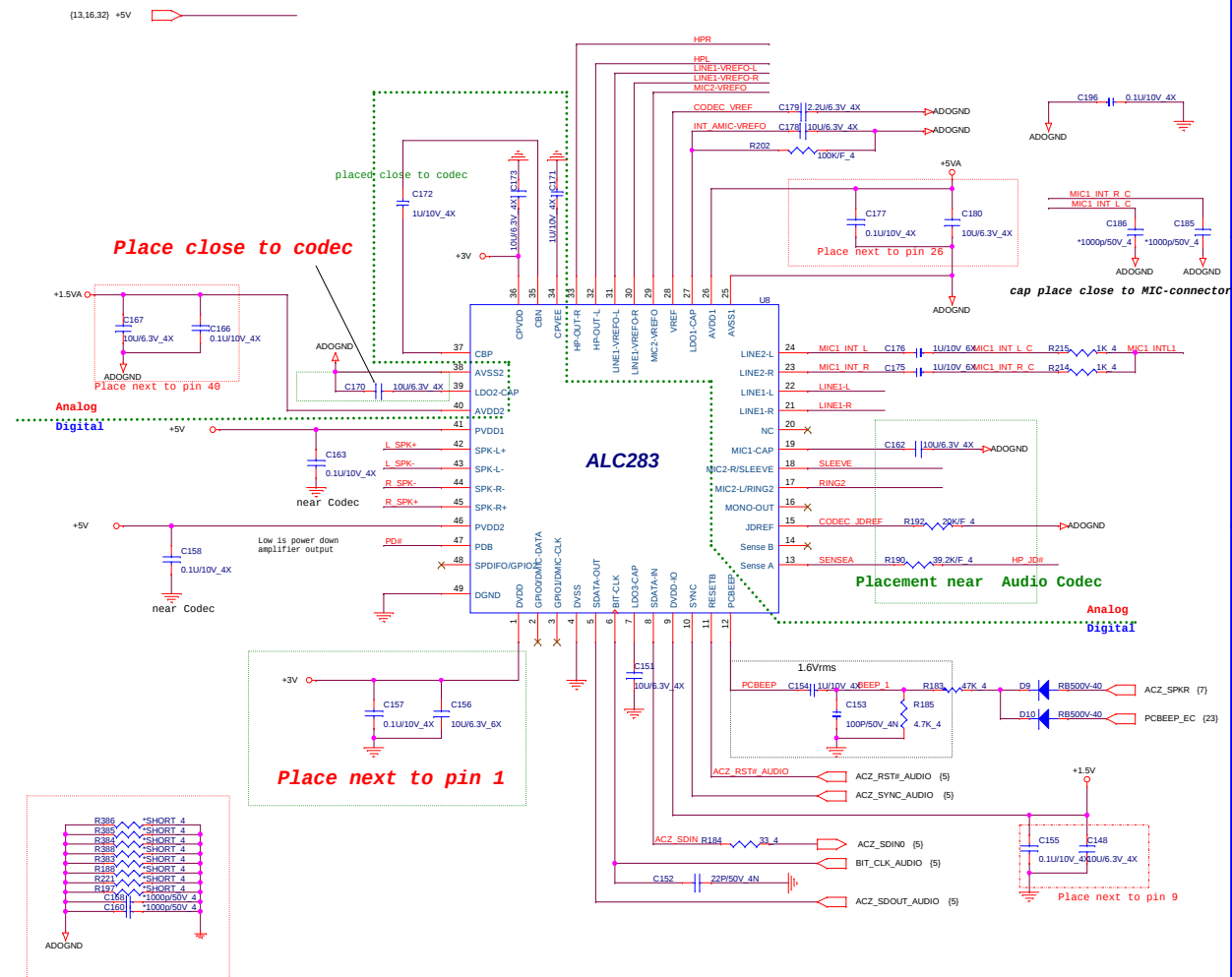
D
C
B
A

D
C
B
A

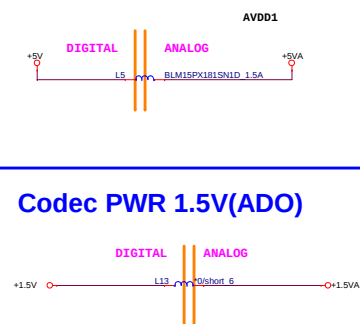
			Quanta Computer Inc.		
			PROJECT : Z8A		
Size	Document Number				Rev
	USB HUB -1				1A
Date:	Thursday, July 31, 2014			Sheet	17 of 33



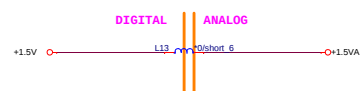
Codec(ADO)



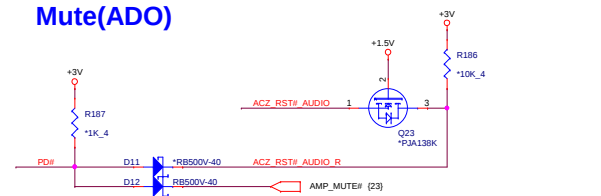
Codec PWR 5V(ADO)



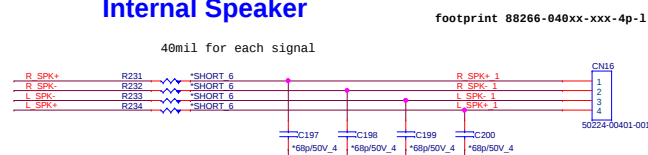
Codec PWR 1.5V(ADO)



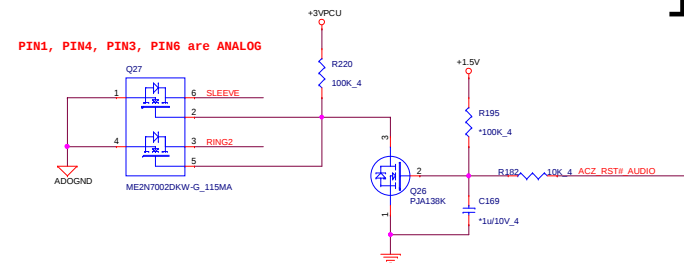
Mute(ADO)



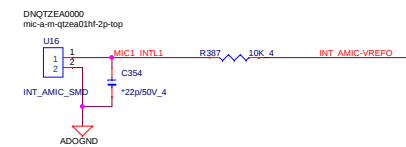
Internal Speaker



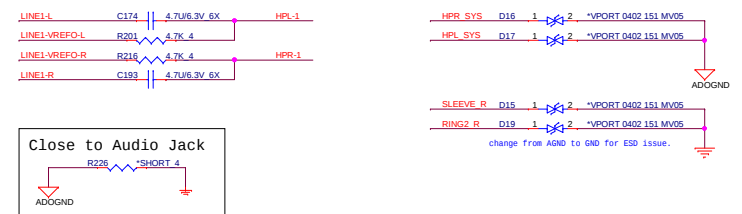
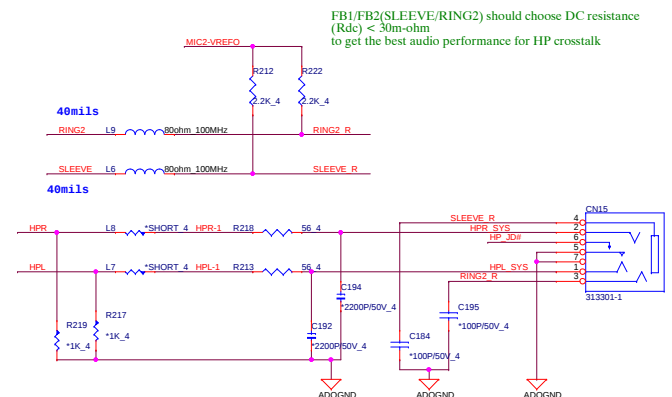
Grounding circuit(ADO)



INT MIC array



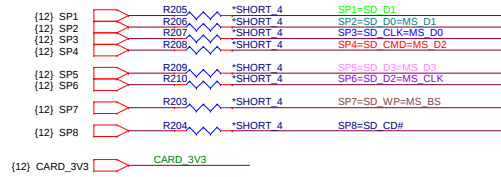
HEADPHONE/MIC/LINE combo



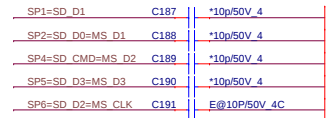
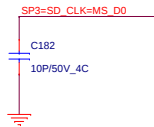
CARD READER CONNECTOR (MMC)

Share Pin

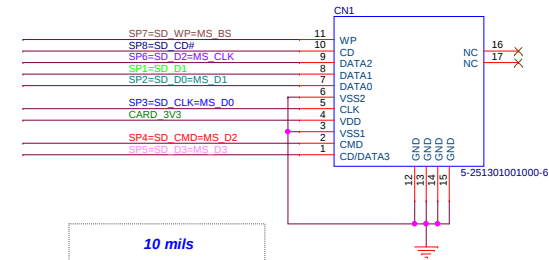
SP1	SD_D1		
SP2	SD_D0	MS_D1	
SP3	SD_CLK	MS_D0	
SP4	SD_CMD	MS_D2	
SP5	SD_D3	MS_D3	
SP6	SD_D2	MS_CLK	
SP7	SD_WP	MS_BS	
SP8	SD_CD#		
SP9		MS_INS#	

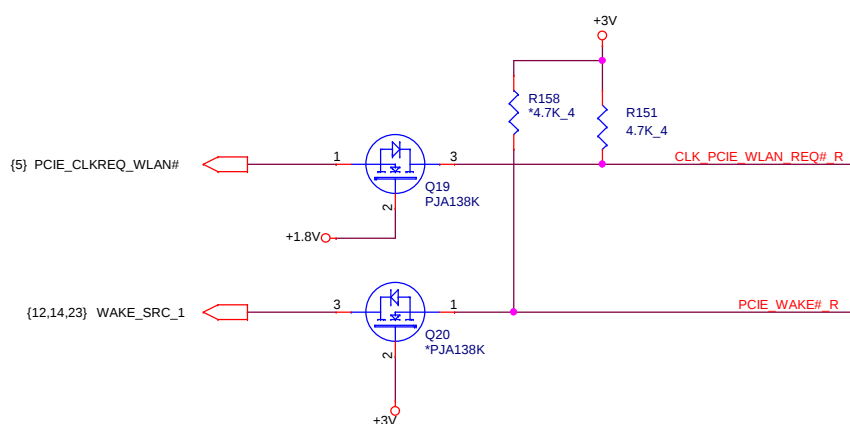
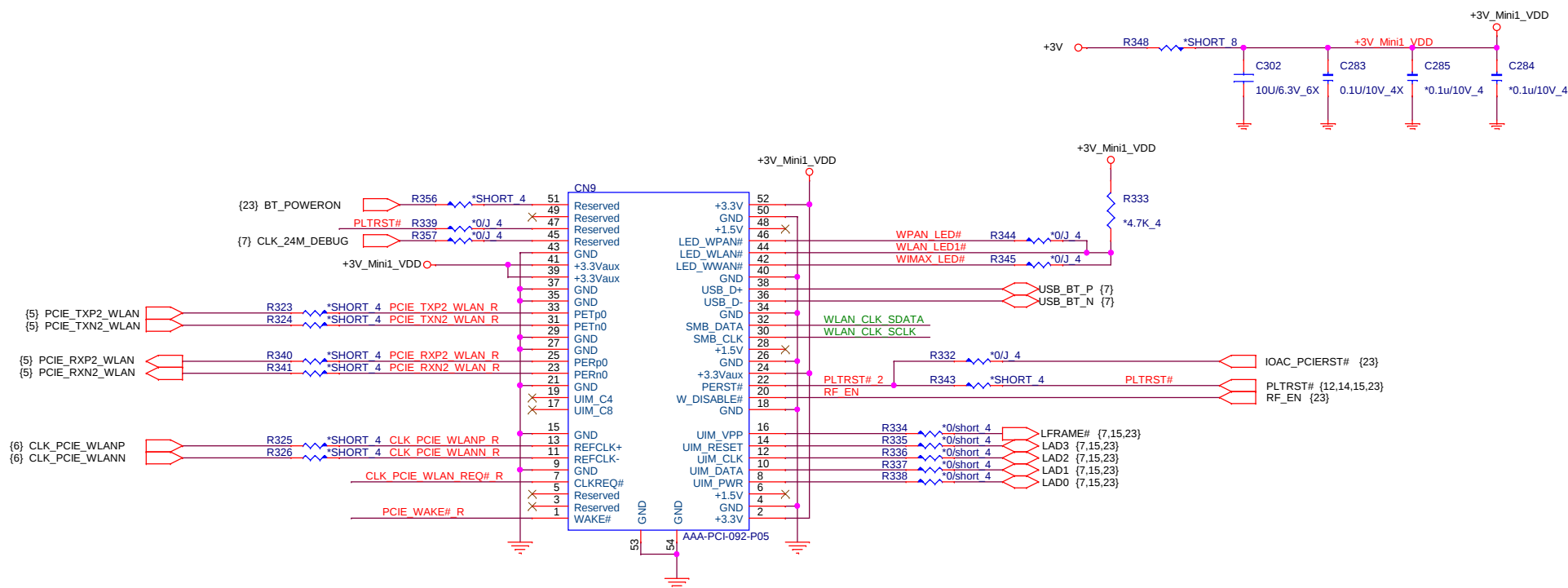


EMI

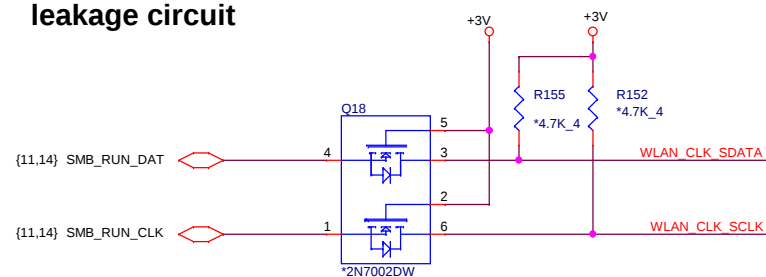


SD/MMC CARD READER (MMC)



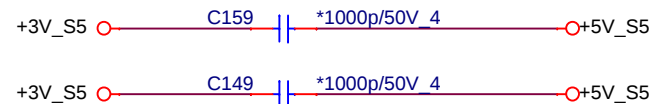
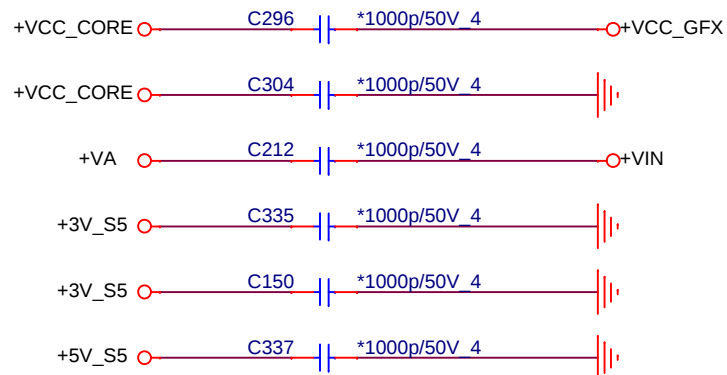
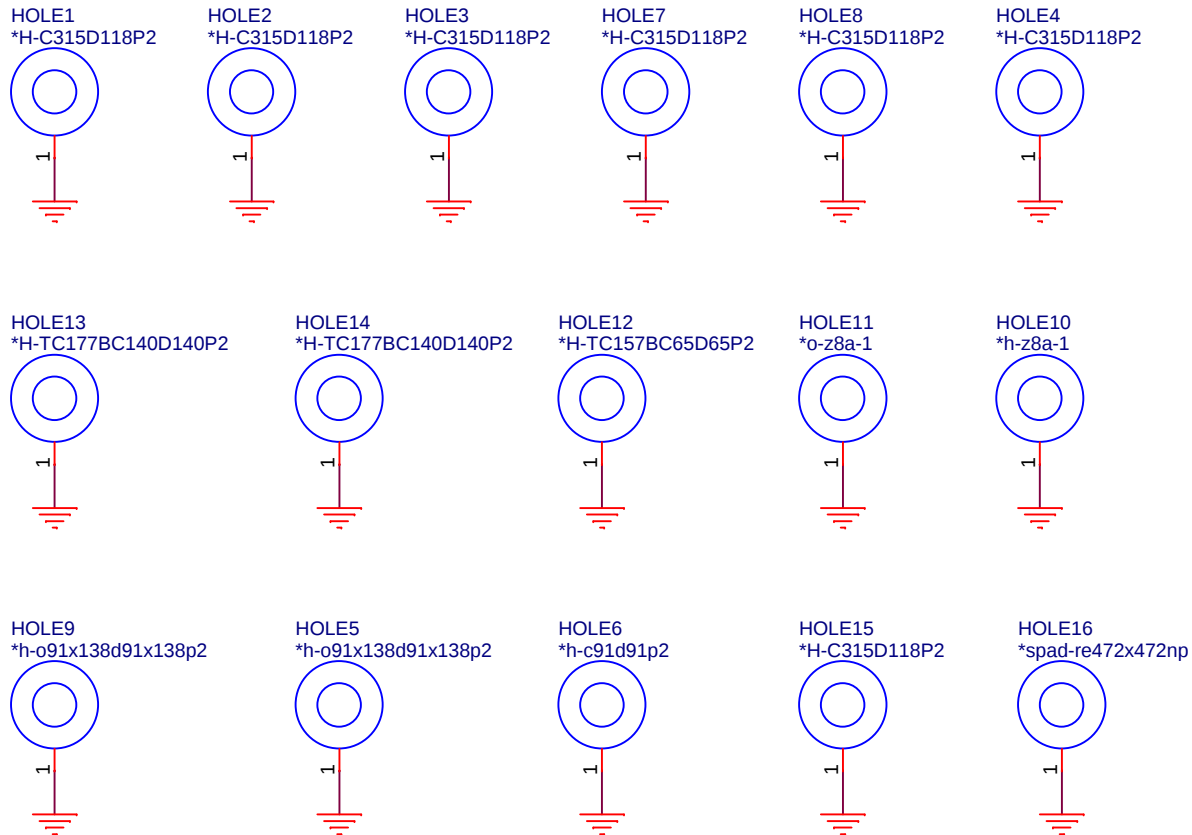


leakage circuit



{4,5,6,7,9,12,13,14,15,23,32} +1.8V

{4,5,9,11,12,13,14,15,16,19,23,30,32} +3V

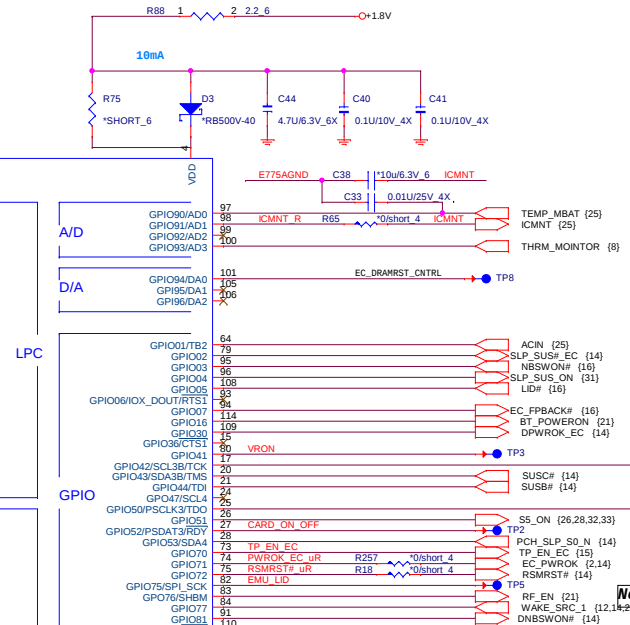




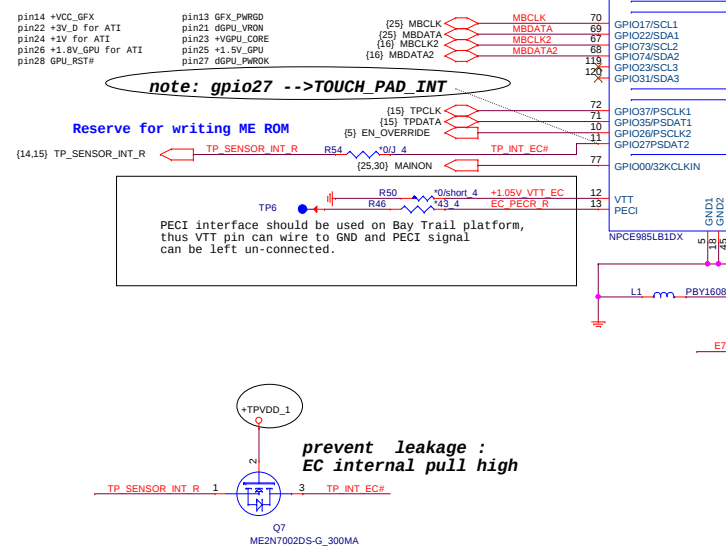
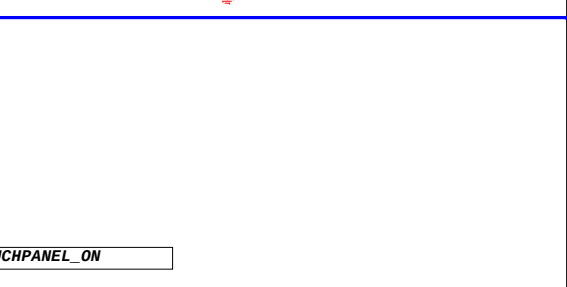
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PROJECT : Z8A

Size	Document Number	Rev
	Thermal / Hole	1A
Date: Thursday, July 31, 2014		Sheet 22 of 33



MBDATA	C1	*10p/50V 4
MBCLK2	C251	*10p/50V 4
MBDATA2	C253	*10p/50V 4
SOC_SPI_CLK_R1	C25	*10p/50V 4

[illegible]

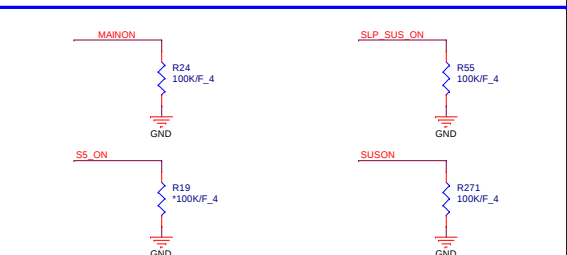
[29.32] HWPG_1.05V

HWPG_1.05V R9 10K_4 +3V_S5

<20130722>Change power from +3V to +3V_S5 for power sequence issue

(28) HWPG_1.0V R16 10K_4 +3V_S5

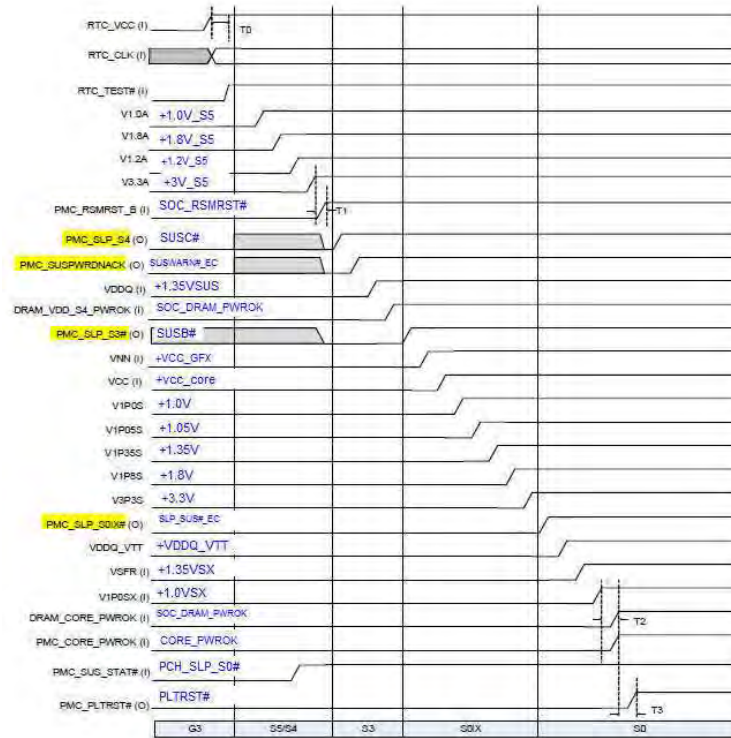
(27) HWPG_1.8V R17 10K_4

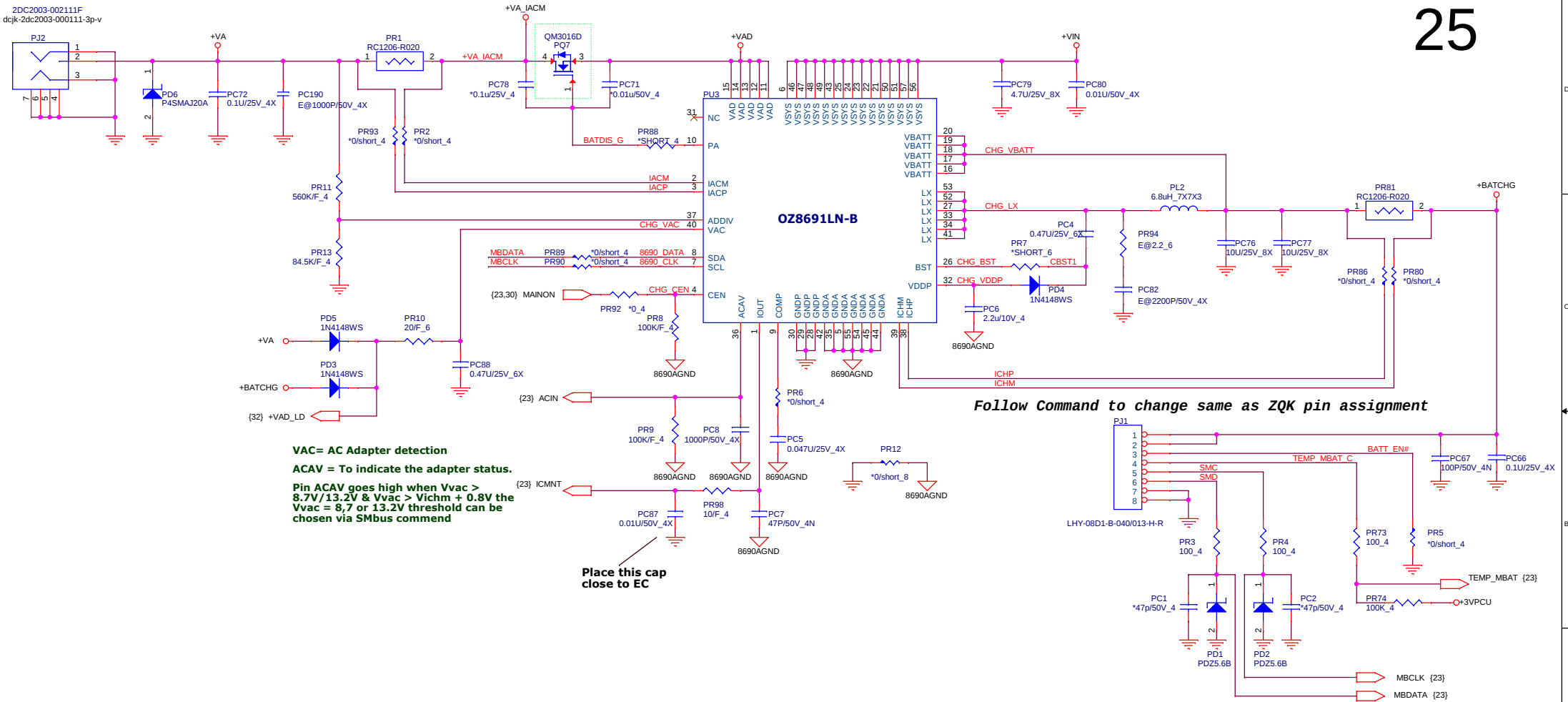


SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

Bay Trail-M S4/S5 to S0 (Power Up) Sequence

24





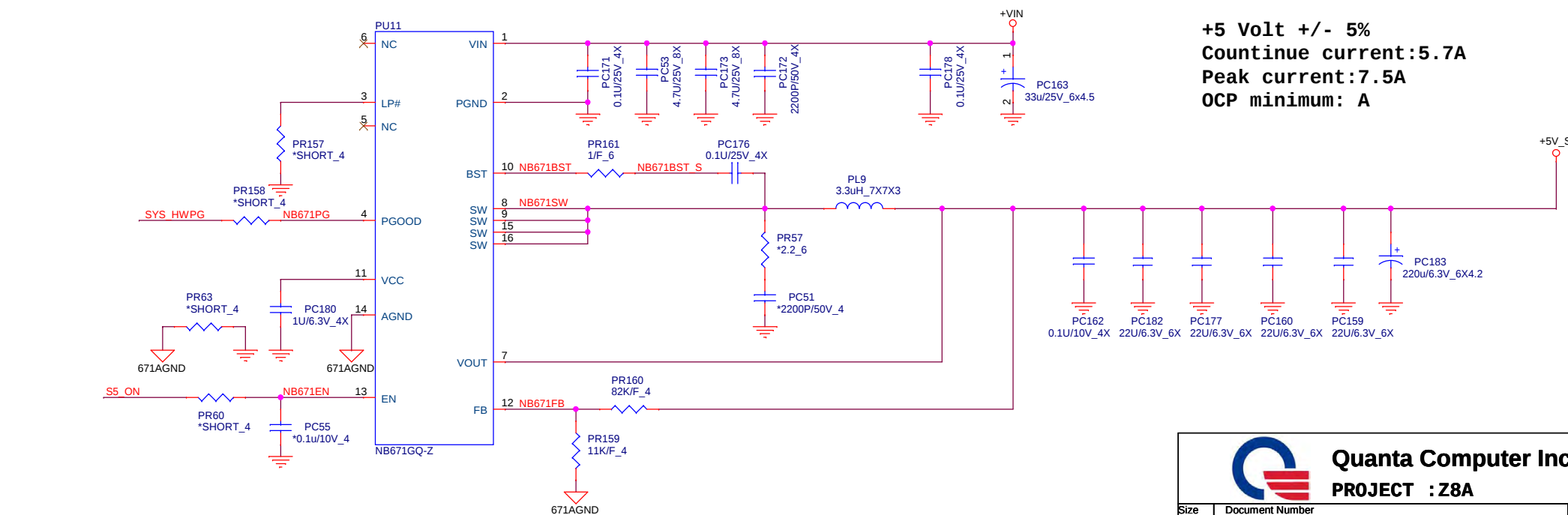
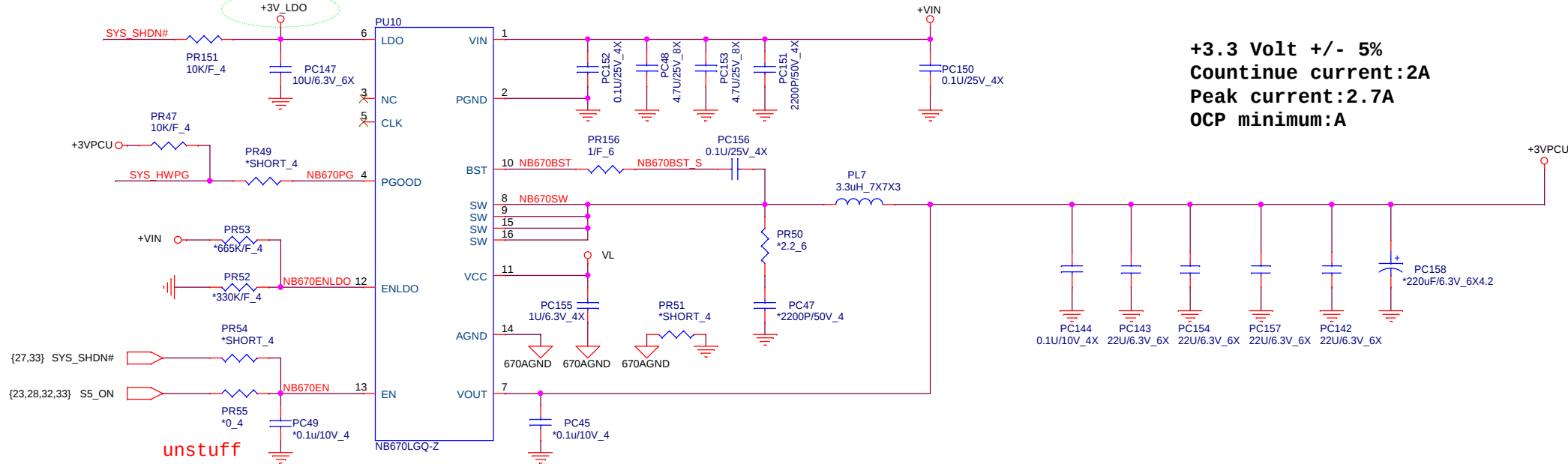
DC/DC +3VPCU/+5V_S5

26

LDO(MAX)=100mA

+3VPCU {6,8,15,16,19,23,25,27,32}

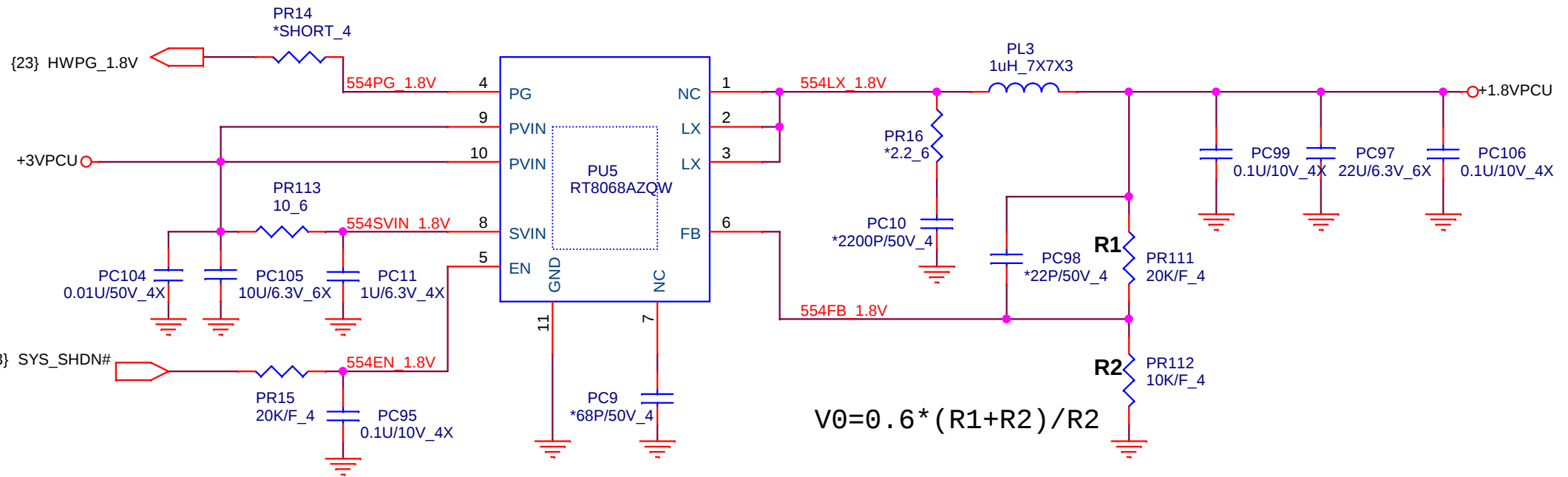
+5V_S5 {18,22,28,29,30,31,32}



Quanta Computer Inc.
PROJECT :Z8A

Size	Document Number	Rev
	3/5VS5 (NB670/NB671)	1A
Date:	Thursday, July 31, 2014	Sheet 26 of 33

+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A



Quanta Computer Inc.
PROJECT : Z8A

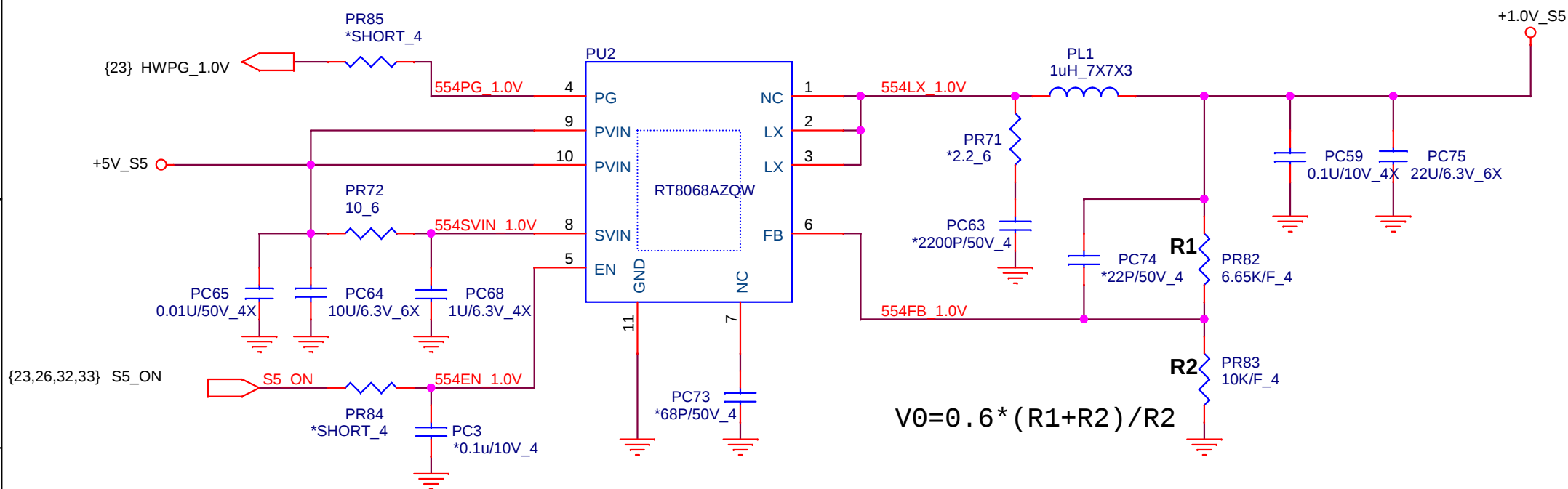
Size	Document Number	Rev
	+1.8VPCU	1A
Date:	Thursday, July 31, 2014	Sheet 27 of 33

{9,32} +1.0V_S5

{18,22,26,29,30,31,32} +5V_S5

{2,9,12,14,15,16,22,23,29,30,32} +3V_S5

+1.0V Volt +/- 5%
Continue current:2.4A
Peak current:3.2A
OCP minimum:A



$$V_0 = 0.6 * (R_1 + R_2) / R_2$$

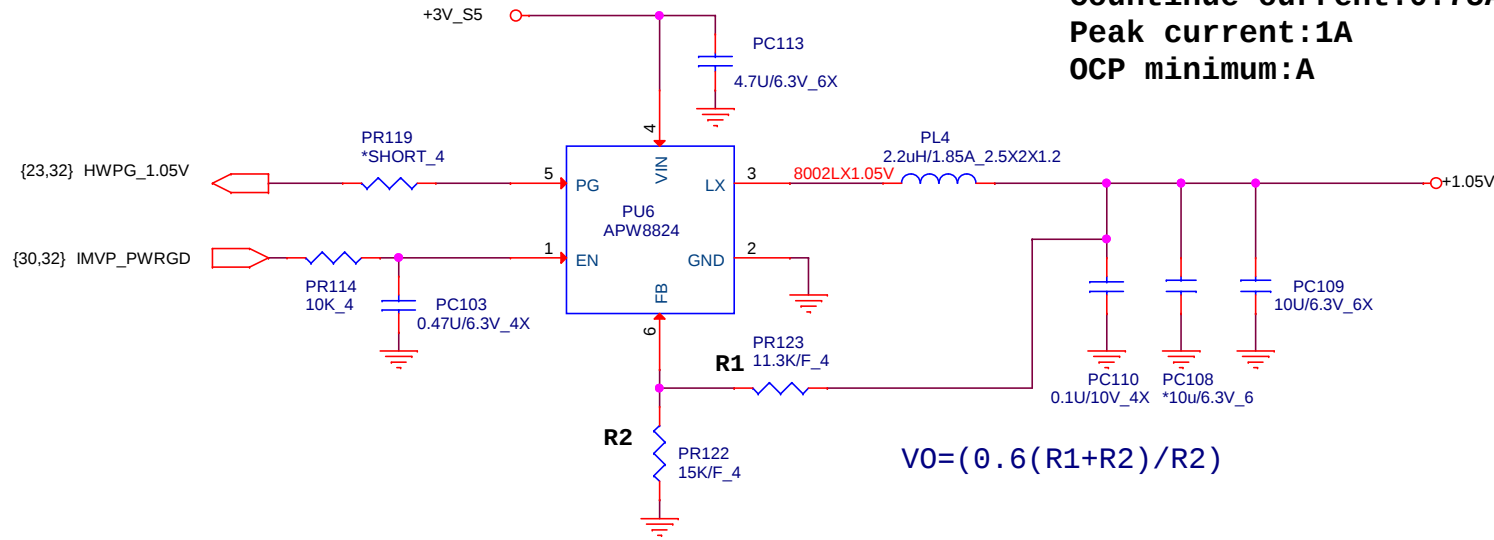


Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number +1.0V	Rev 1A
Date:	Thursday, July 31, 2014	Sheet 28 of 33

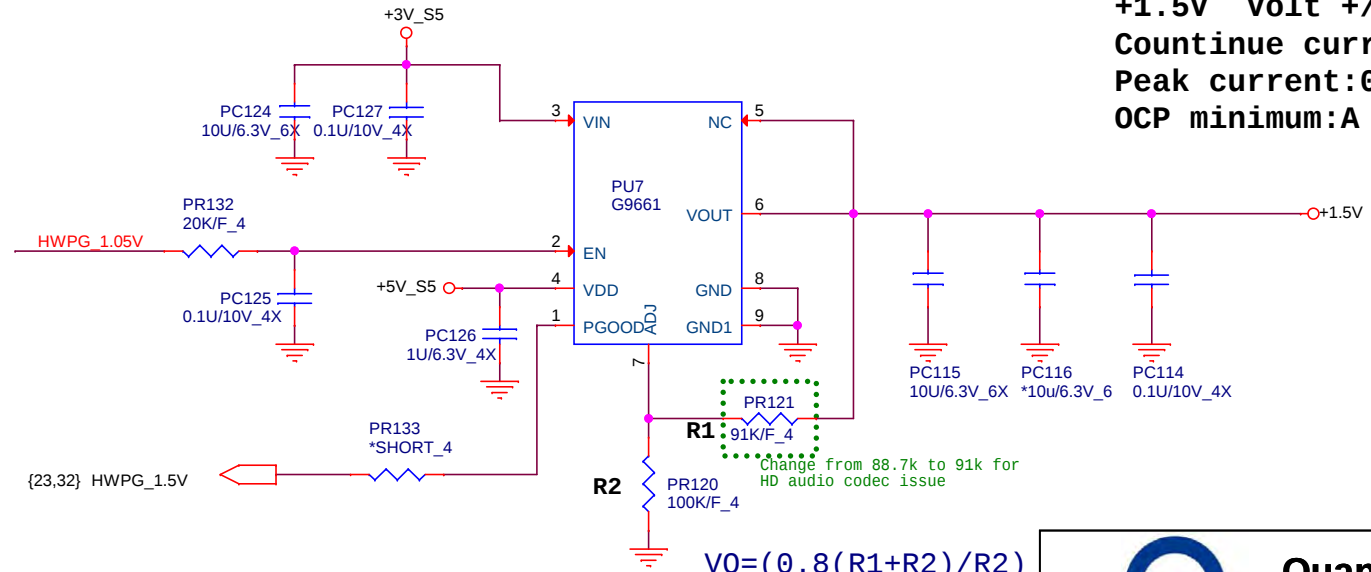
{2,9,12,14,15,16,22,23,30,32} +3V_S5
 {9} +1.05V
 {9,19} +1.5V

+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCp minimum:A



$$V0 = (0.6(R1+R2)/R2)$$

+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCp minimum:A

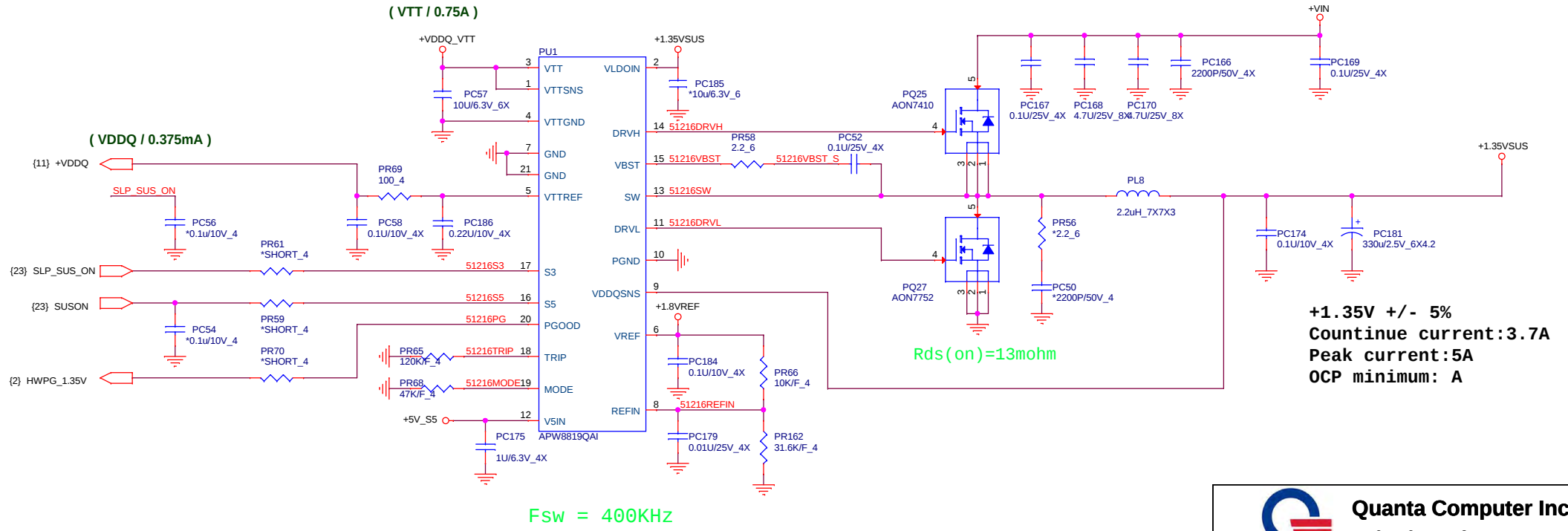


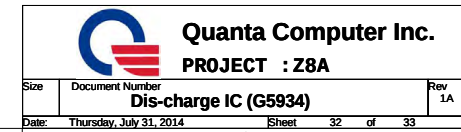
$$V0 = (0.8(R1+R2)/R2)$$

R2 < 120Kohm



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PROJECT : Z8A





[illegible]

33

Thermal protection

Need fine tune
for thermal protect point

Note placement position

The diagram illustrates a thermal protection circuit for EC control, outputting 3.3V. Key components include:

- +VIN Input:** Connected to a diode PD7 (DA2J10100L_100MA) and a resistor PR103 (1M_6).
- MOSFETs:** PQ15 (AO3409), PQ14 (DTC144EUA), PQ13 (ME2N7002DS-G_300MA), and PQ12 (ME2N7002DS-G_300MA).
- Resistors:** PR100 (1.74K/F_4), PR99 (200K/F_4), PR101 (200K/F_4), PR102 (NTC_10K_4), PR103 (1M_6), PR104 (200K_6), and PR105 (*0/short_6).
- Capacitors:** PC92 (0.1U/50V_6X) and PC89 (0.1U/50V_6X).
- Operational Amplifiers:** PU4A (AS393MTR-E1) and PU4B (AS393MTR-E1).
- Control Signals:** S5_ON and SYS_SHDN# {26,27}.

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number	Rev
	Thermal	1A
Date:	Thursday, July 31, 2014	Sheet 33 of 33

33

Thermal protection

Need fine tune
for thermal protect point

Note placement position

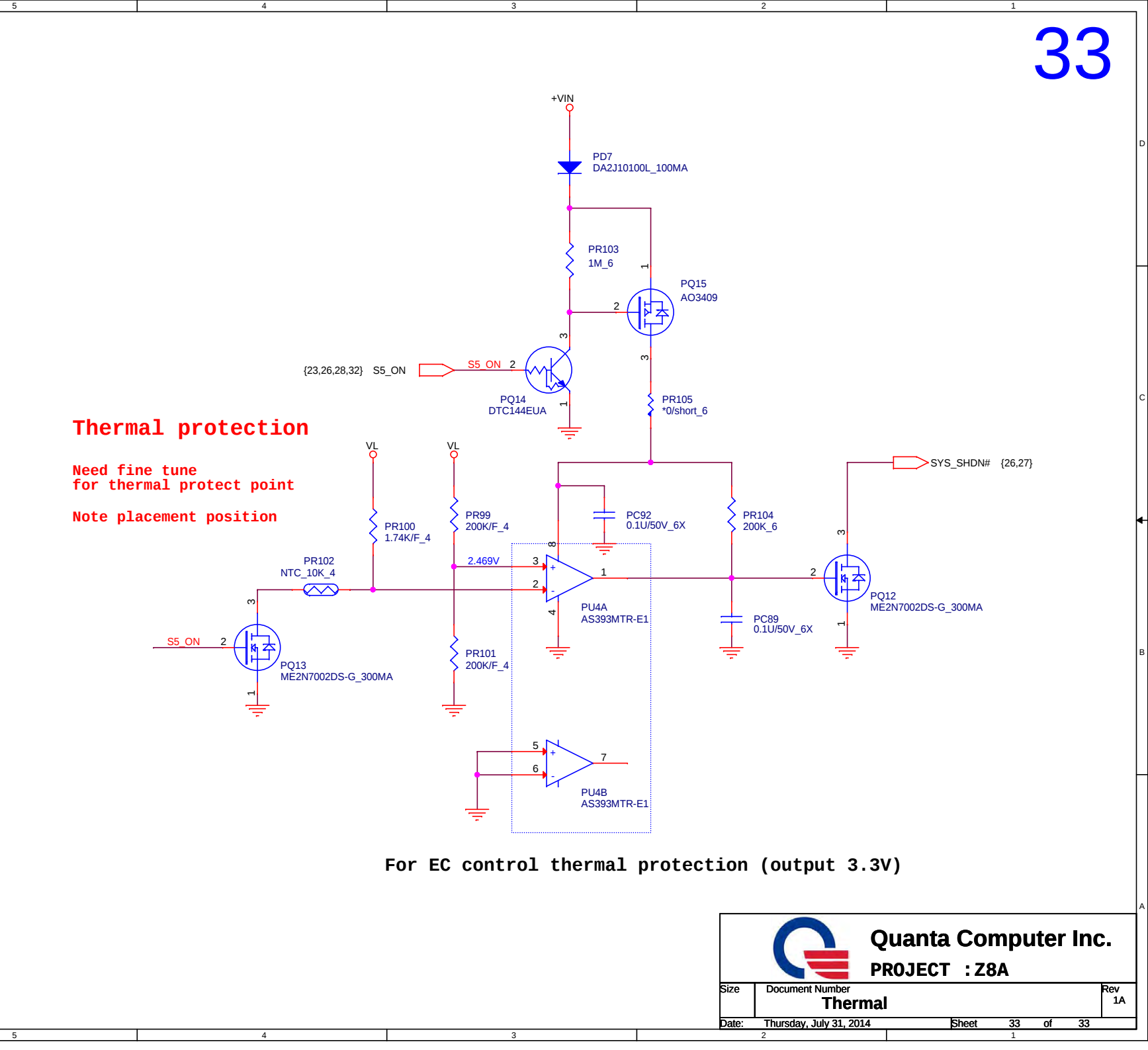
The diagram illustrates a thermal protection circuit for EC control, providing a 3.3V output. Key components and connections include:

- +VIN Input:** Connected to PD7 (DA2J10100L_100MA) diode.
- Resistor Network:** PR103 (1M_6), PR105 (*0/short_6), PR100 (1.74K/F_4), PR99 (200K/F_4), PR102 (NTC_10K_4), and PR101 (200K/F_4).
- Capacitor Network:** PC92 (0.1U/50V_6X) and PC89 (0.1U/50V_6X).
- Comparators:** PU4A and PU4B (AS393MTR-E1).
- MOSFETs:** PQ13 (ME2N7002DS-G_300MA), PQ14 (DTC144EUA), PQ15 (AO3409), and PQ12 (ME2N7002DS-G_300MA).
- Control Signals:** S5_ON, VL, and SYS_SHDN# {26,27}.

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number	Rev
	Thermal	1A
Date:	Thursday, July 31, 2014	Sheet 33 of 33



33

Thermal protection

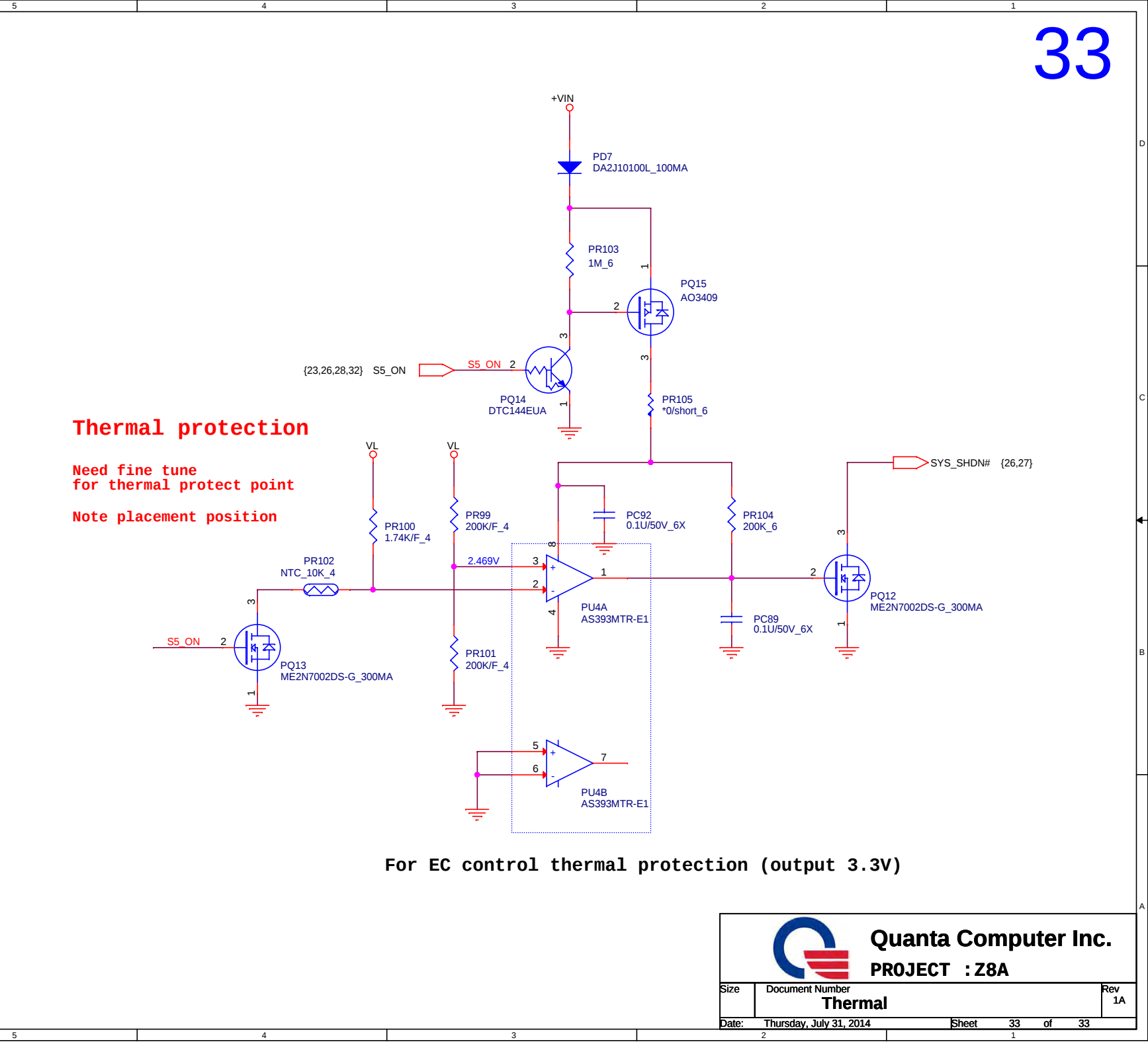
Need fine tune
for thermal protect point

Note placement position

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number	Rev
	Thermal	1A
Date:	Thursday, July 31, 2014	Sheet 33 of 33

[illegible]

33

Thermal protection

Need fine tune
for thermal protect point

Note placement position

The diagram illustrates a thermal protection circuit for EC control, outputting 3.3V. Key components include:

- +VIN Input:** Connected to a diode PD7 (DA2J10100L_100MA) and a resistor PR103 (1M_6).
- MOSFETs:** PQ15 (AO3409), PQ14 (DTC144EUA), PQ13 (ME2N7002DS-G_300MA), and PQ12 (ME2N7002DS-G_300MA).
- Resistors:** PR100 (1.74K/F_4), PR99 (200K/F_4), PR101 (200K/F_4), PR102 (NTC_10K_4), PR103 (1M_6), PR104 (200K_6), and PR105 (*0/short_6).
- Capacitors:** PC92 (0.1U/50V_6X) and PC89 (0.1U/50V_6X).
- Operational Amplifiers:** PU4A (AS393MTR-E1) and PU4B (AS393MTR-E1).
- Control Signals:** S5_ON and SYS_SHDN# {26,27}.

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : Z8A

Size	Document Number	Rev
	Thermal	1A
Date:	Thursday, July 31, 2014	Sheet 33 of 33

[illegible]

Model	REV	CHANGE LIST
Z8A MB	A1A	1.First Release
	C3A	1.Change C19/C20 value from 10P to 12P for crystal Vendor EA suggestion 2.Swap USB3+/USB3- signals to correct pin define for CCD yellow mark issue 3.Change L4 to 90 ohm common mode chock for EMI 4.Change Hole10 and Hole16 footprint for ME DXF update 5.Reverse D24 and D25 ESD components for ESD 6.Add PC190 1000p cap for EMI suggestion 7.Mount PR94 and PC82 for EMI suggestion
	E3A	1.Change R223,R224,R225,R227 value for LED brightness 2.Change Hole5 and Hole6 and Hole9 and Hole10 footprint for ME DXF update

 Quanta Computer Inc. PROJECT : Z8A				DOC NO.	PROJECT MODEL :	Z8A	APPROVED BY:		DATE:
Rev 1A Doc: Thursday, July 31, 2024 Change list					PART NUMBER:		DRAWING BY:		REVISION: