

PEGATRON CONFIDENTIAL

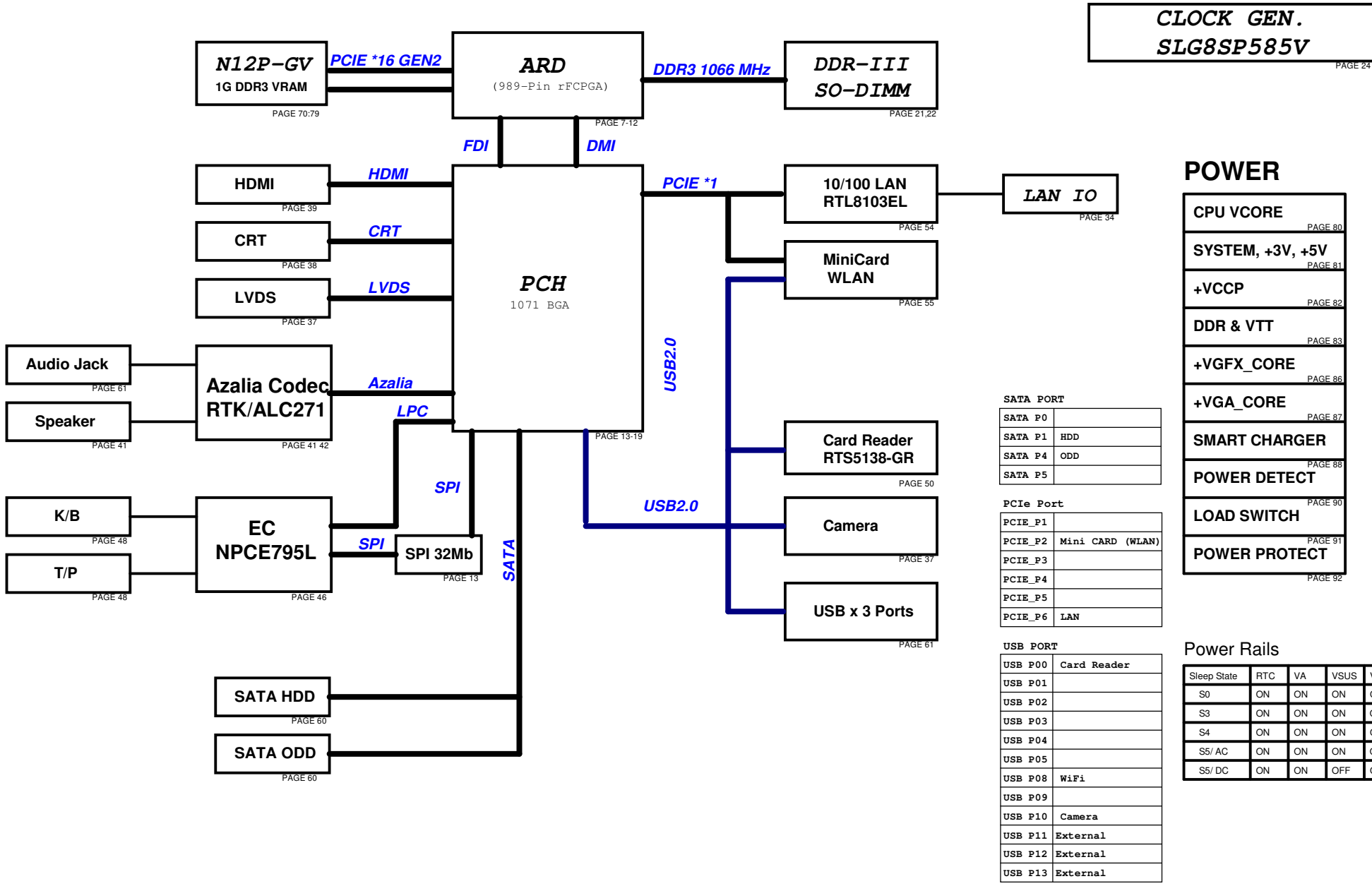
MODEL NAME :

PCB NO :

69- P/N :

AIC70 Schematic
Intel Arrandale rPGA-989
PCH BGA 1071
2011-05-04
REV : R2.0

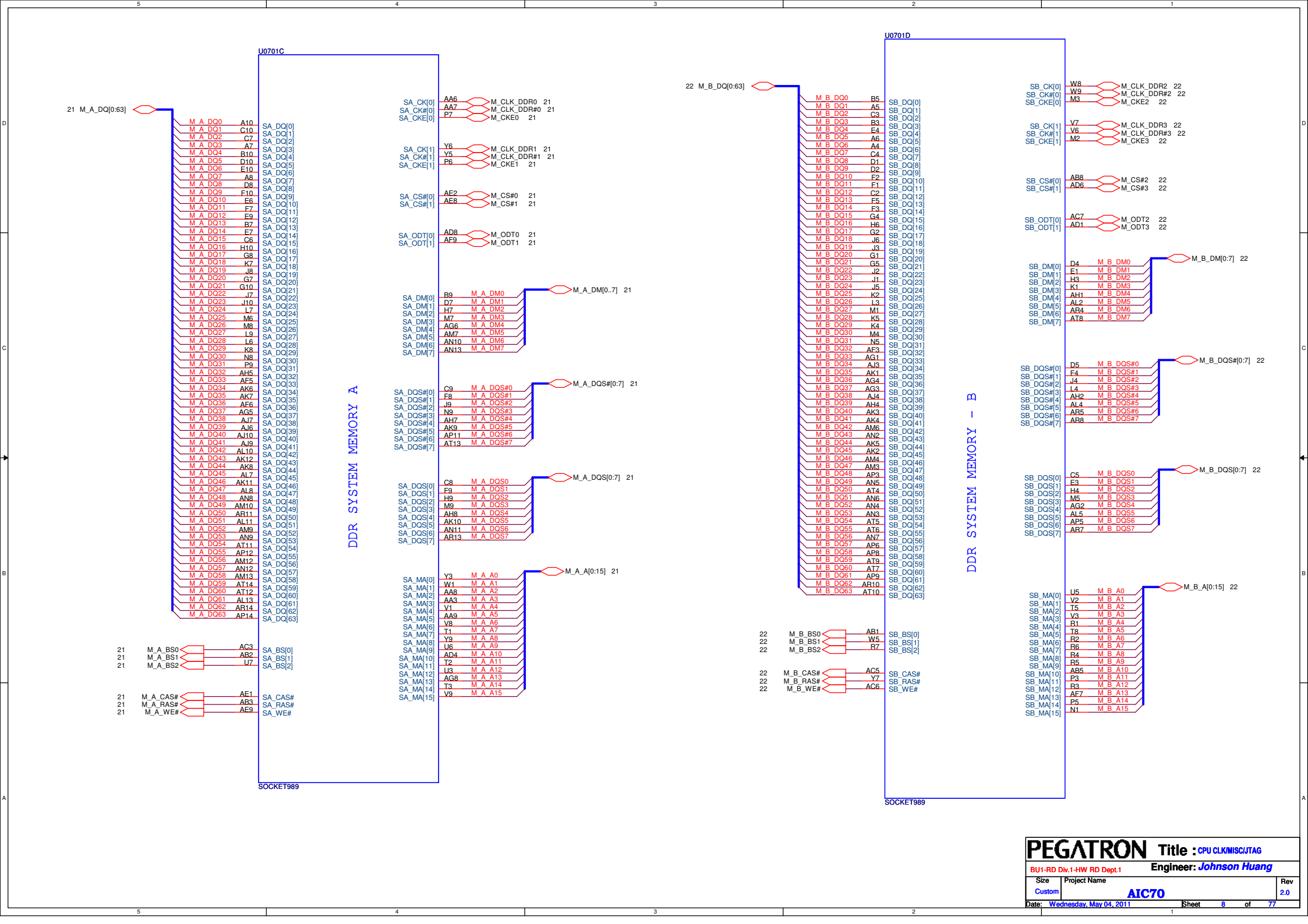
AIC70 BLOCK DIAGRAM

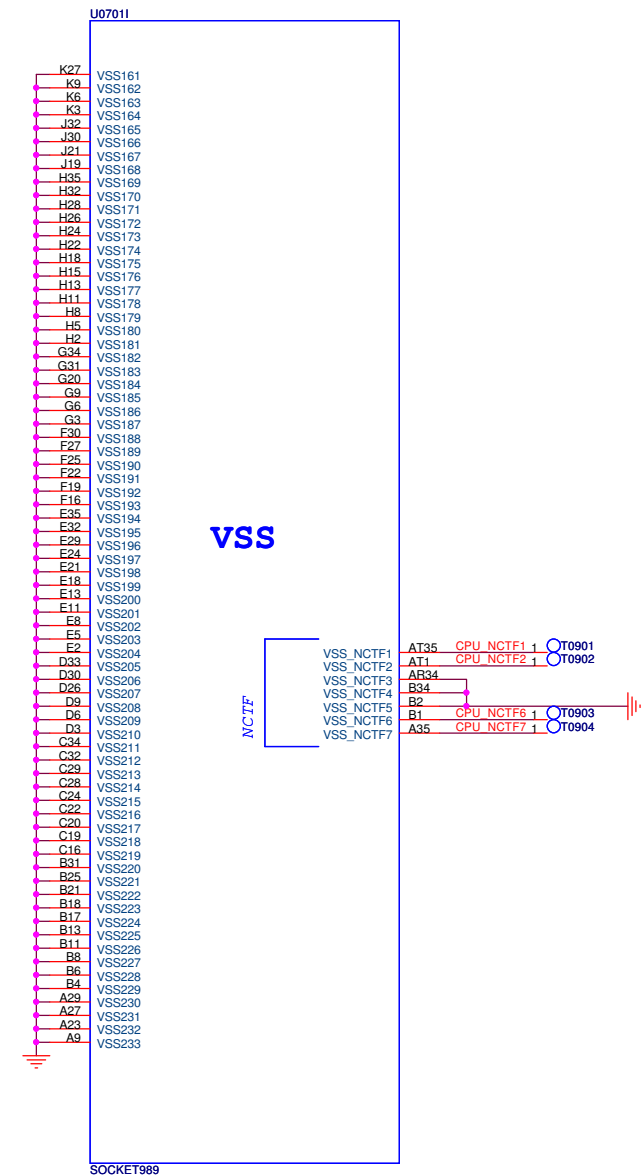
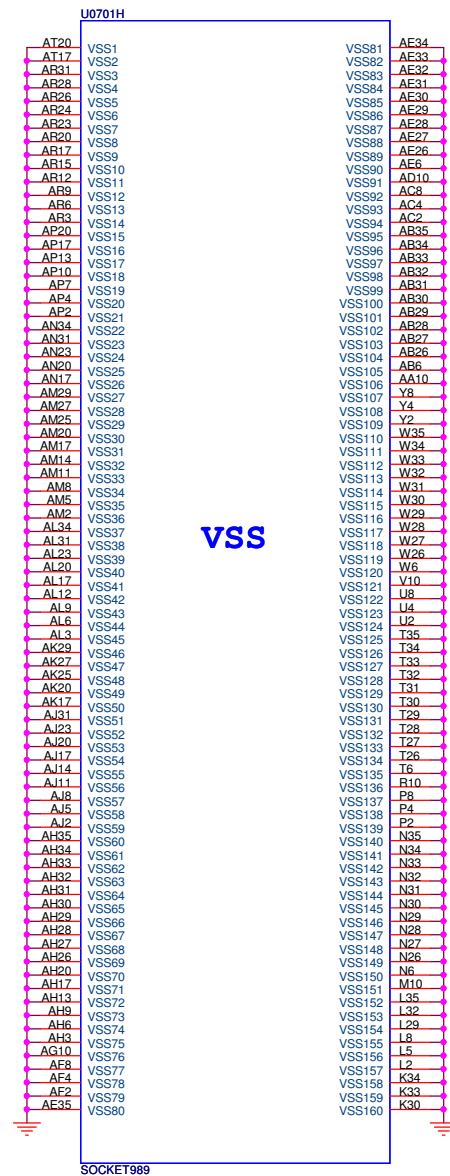


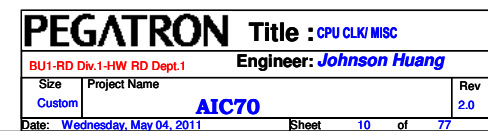
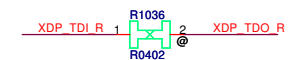
SCHEMATIC INDEX V1.2

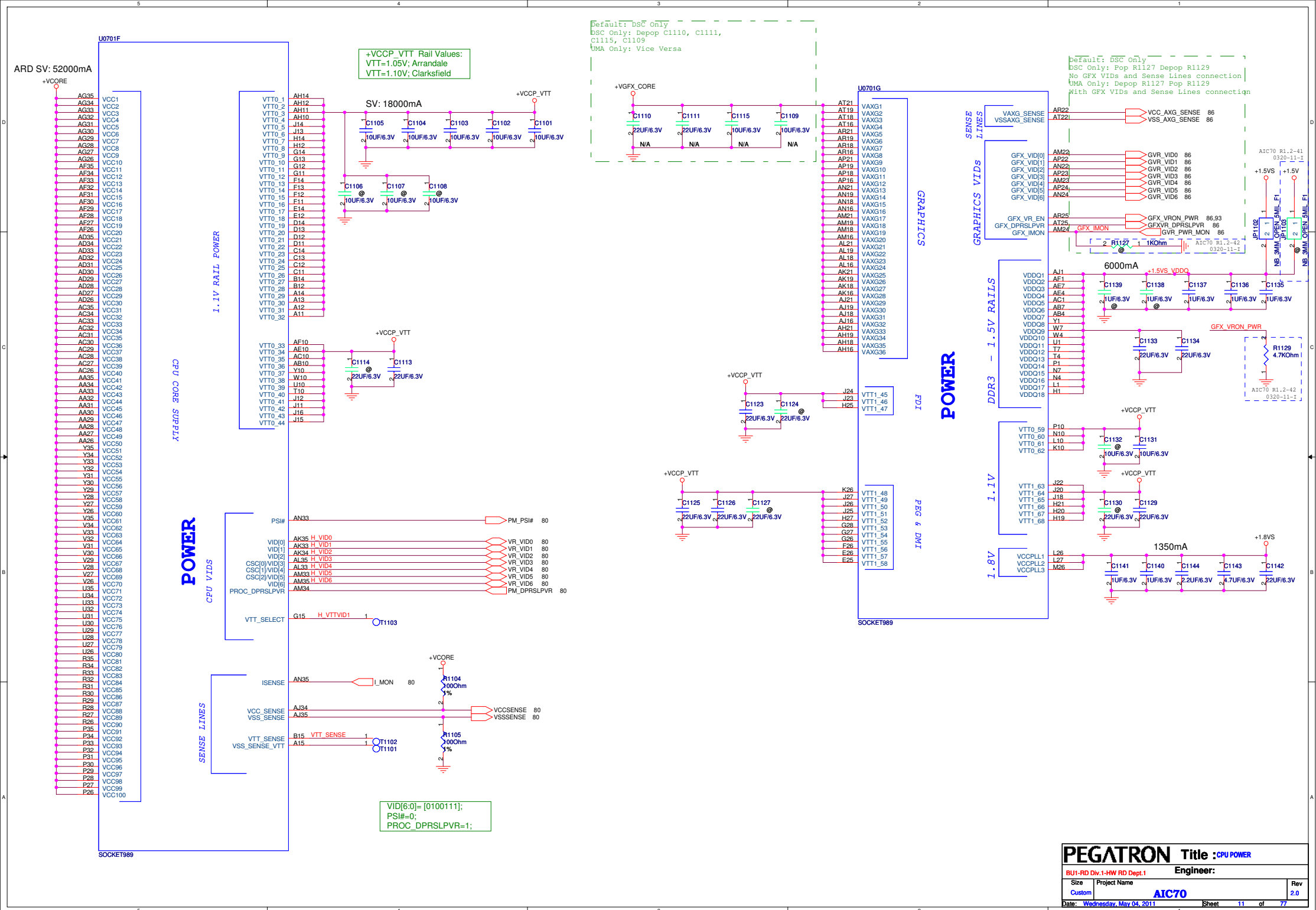
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PAGE#	Description	NOTE



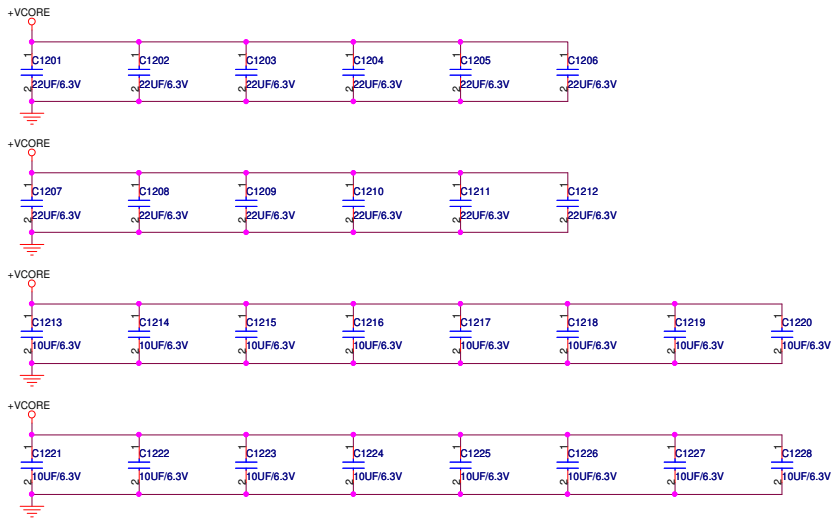


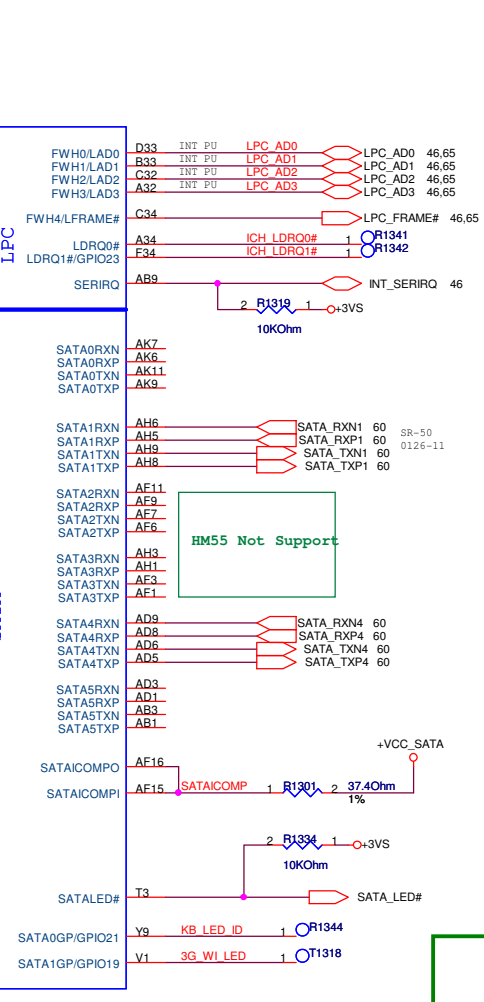
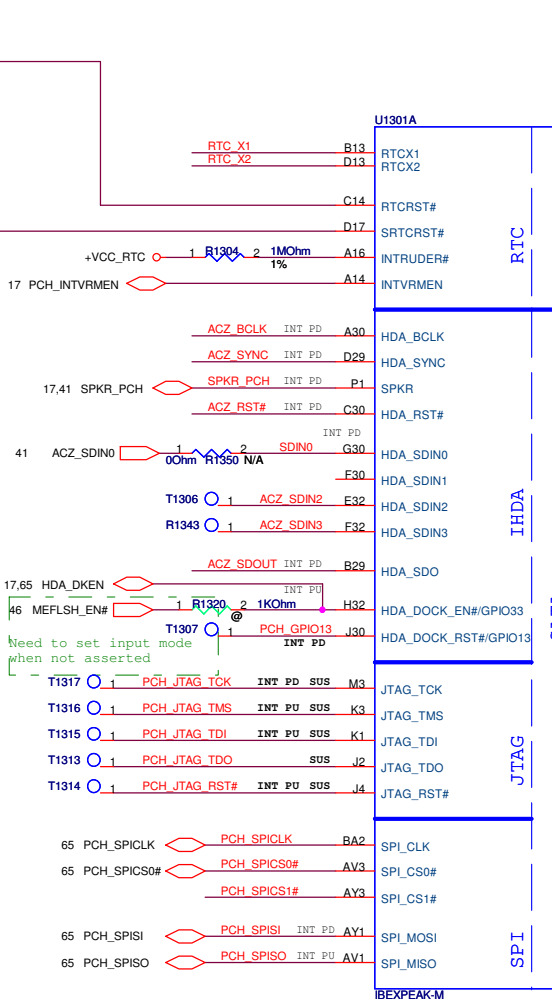
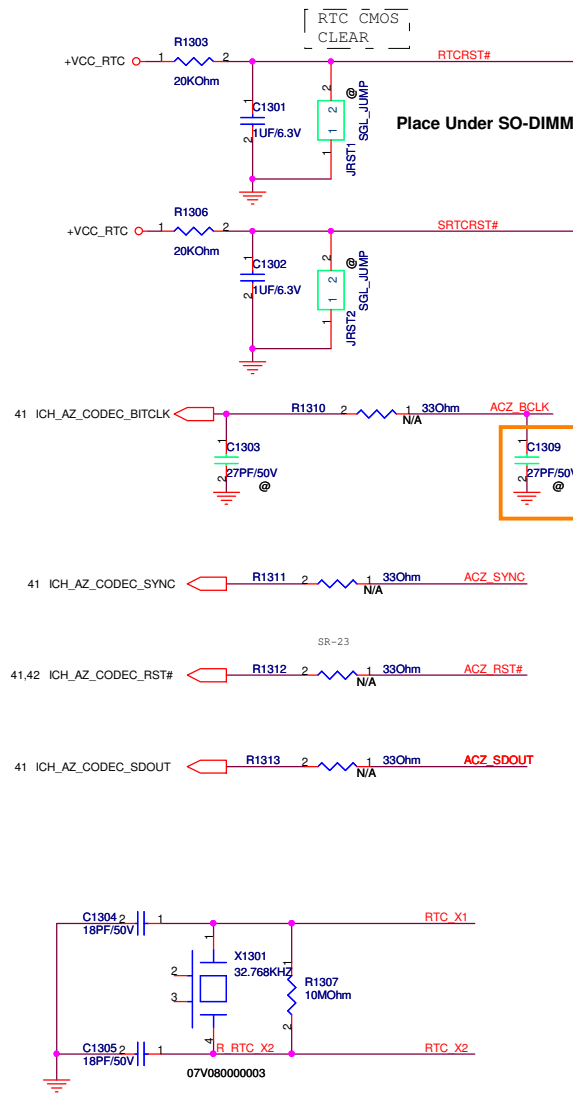




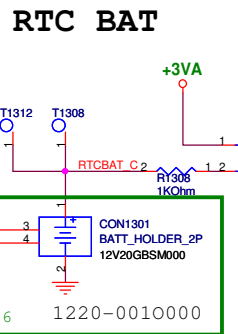
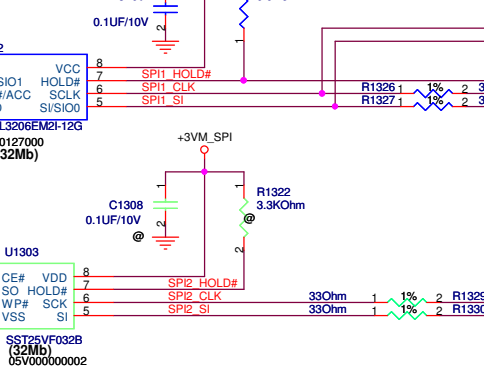
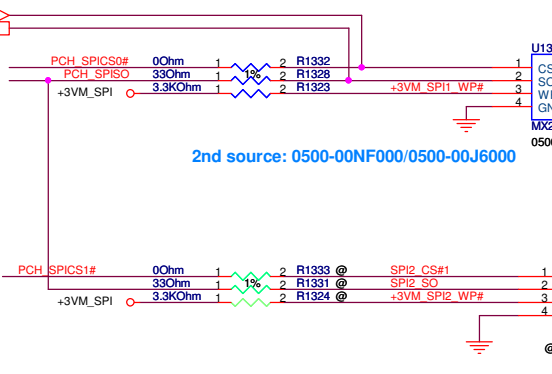
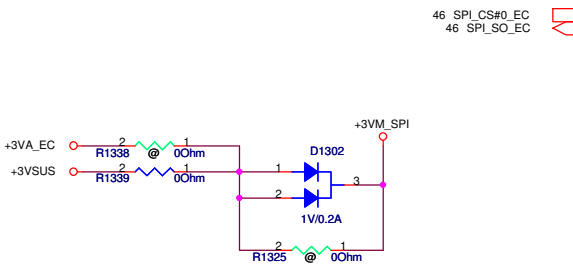
Decoupling guide from INTEL

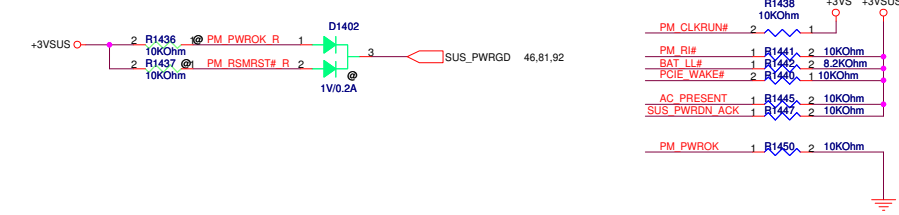
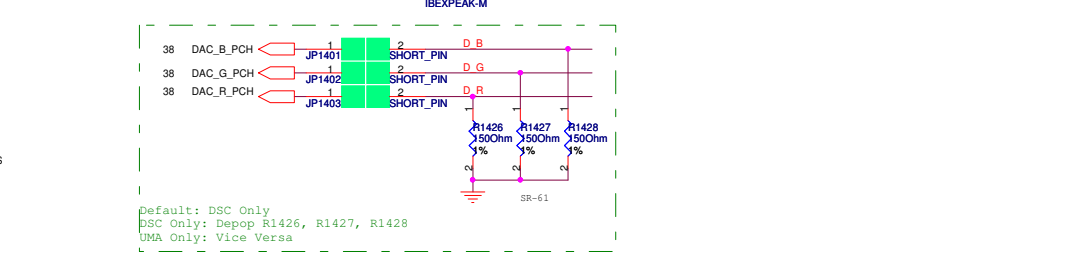
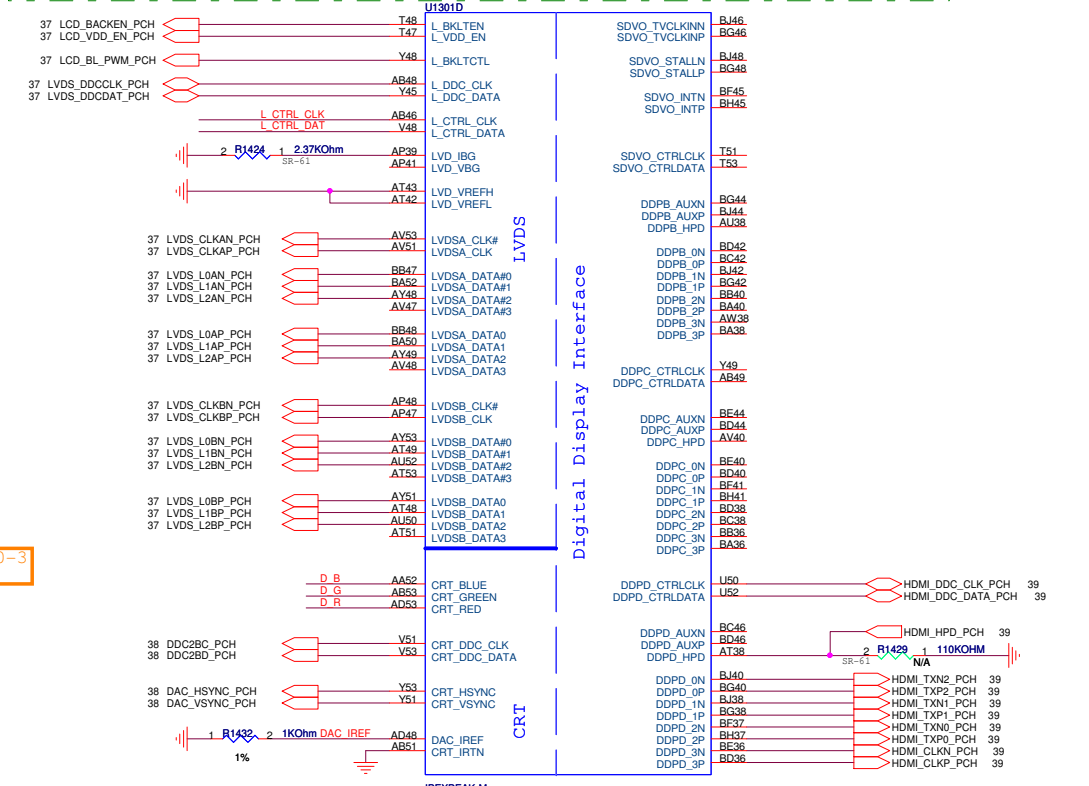
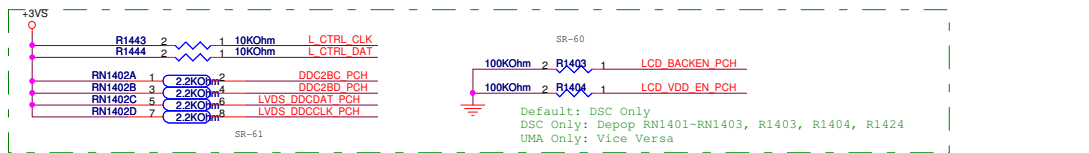
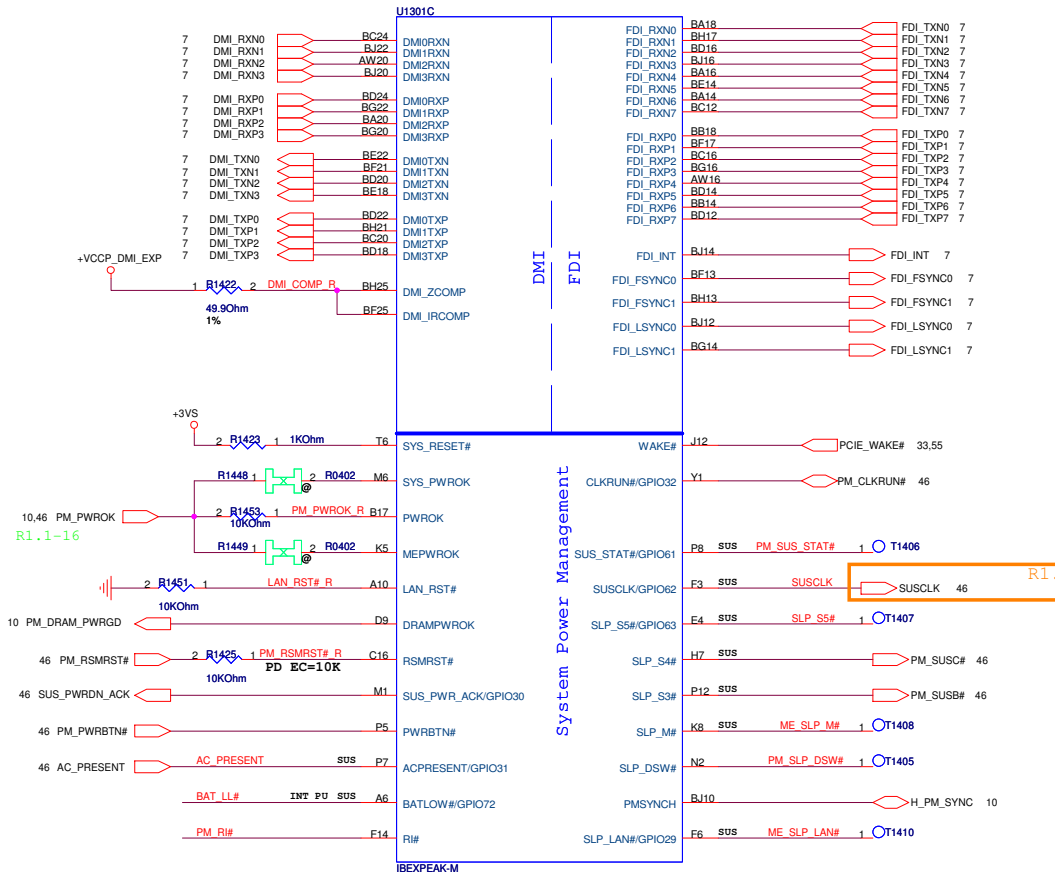
VCORE	10uF	x 16pcs
	22uF	x 12pcs



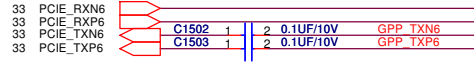
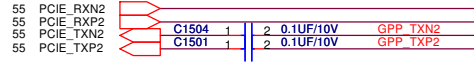


SATA PORT	
SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	eSATA Removed

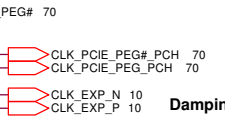
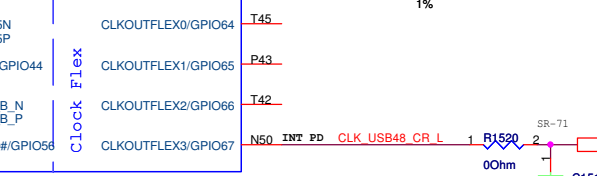
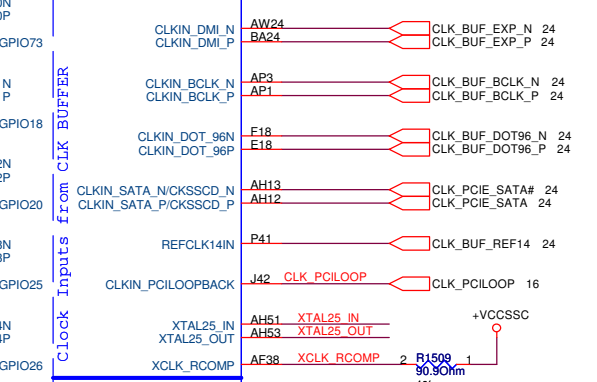
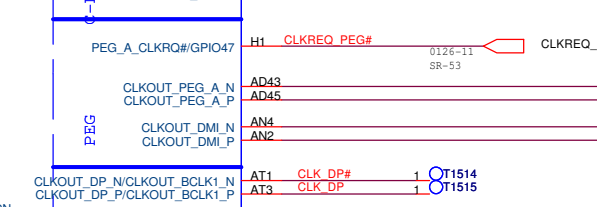
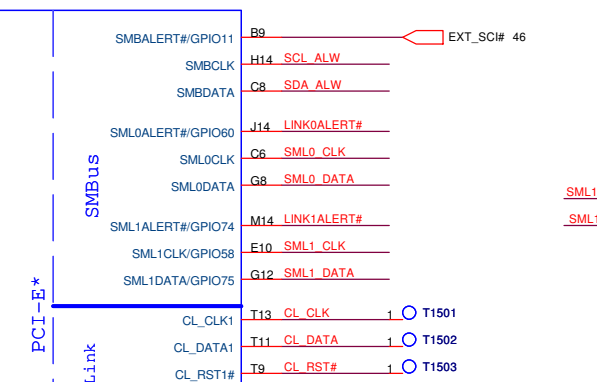
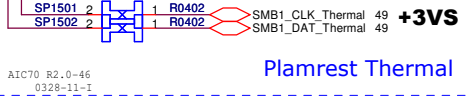
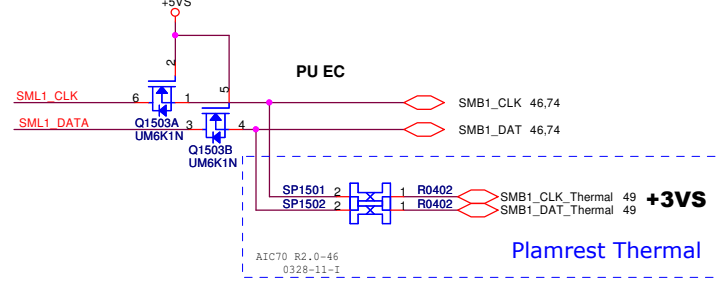
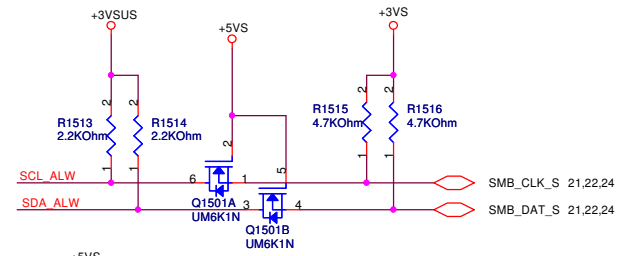
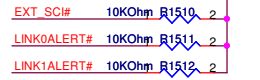
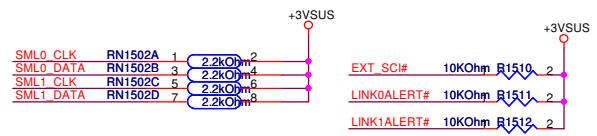
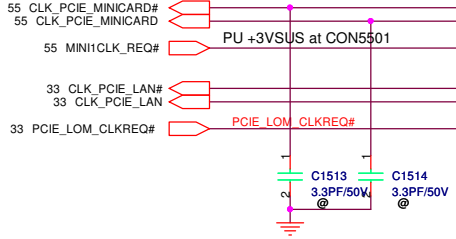
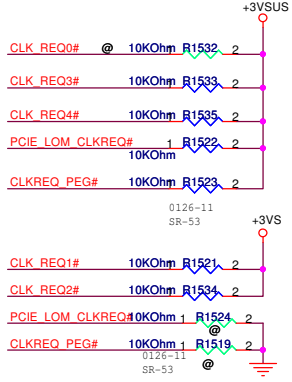




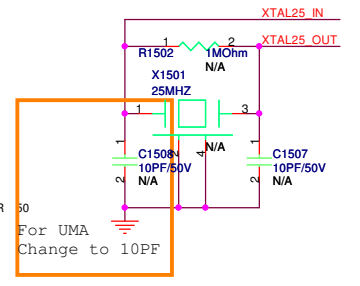
PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN



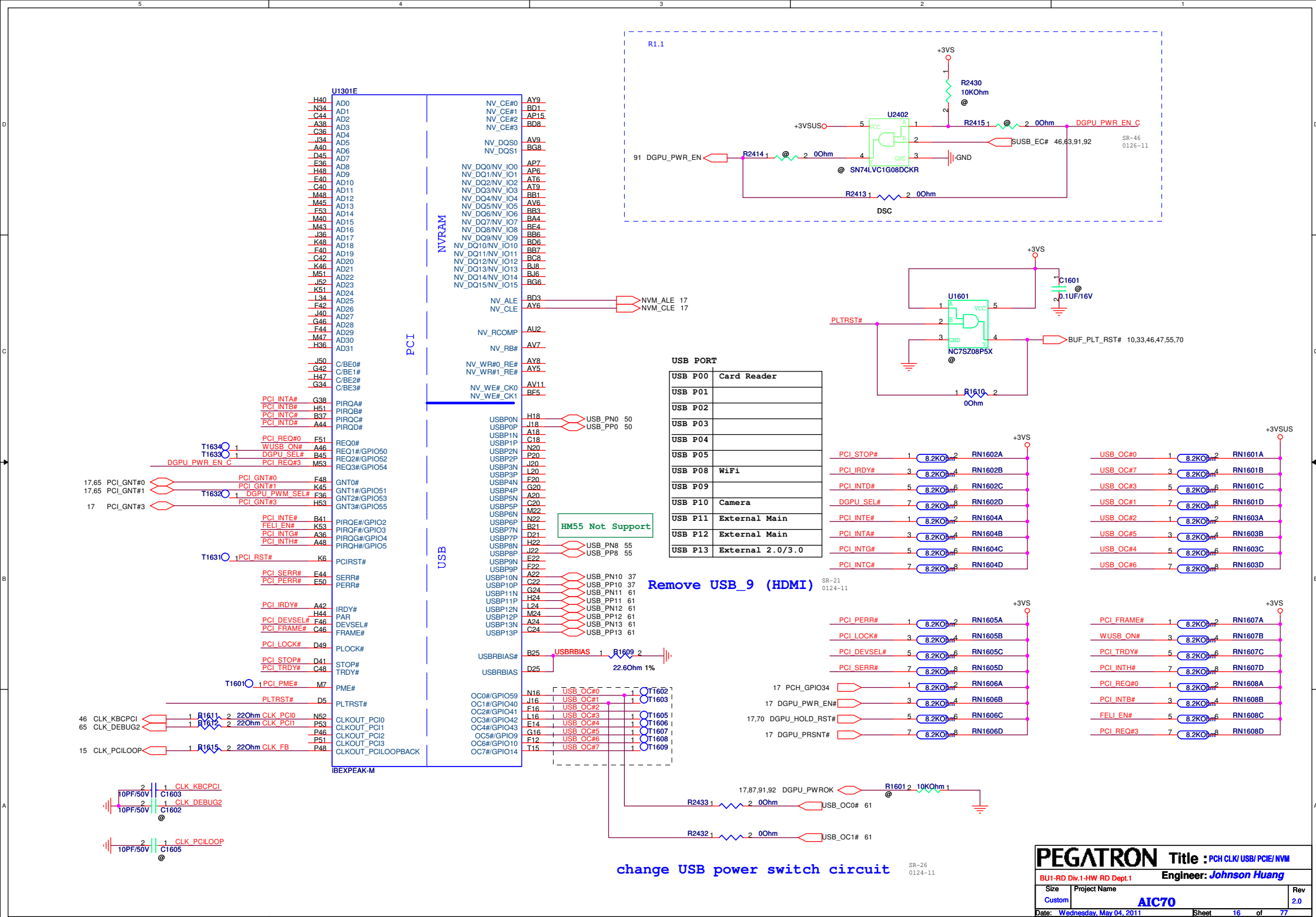
HM55 Not Support

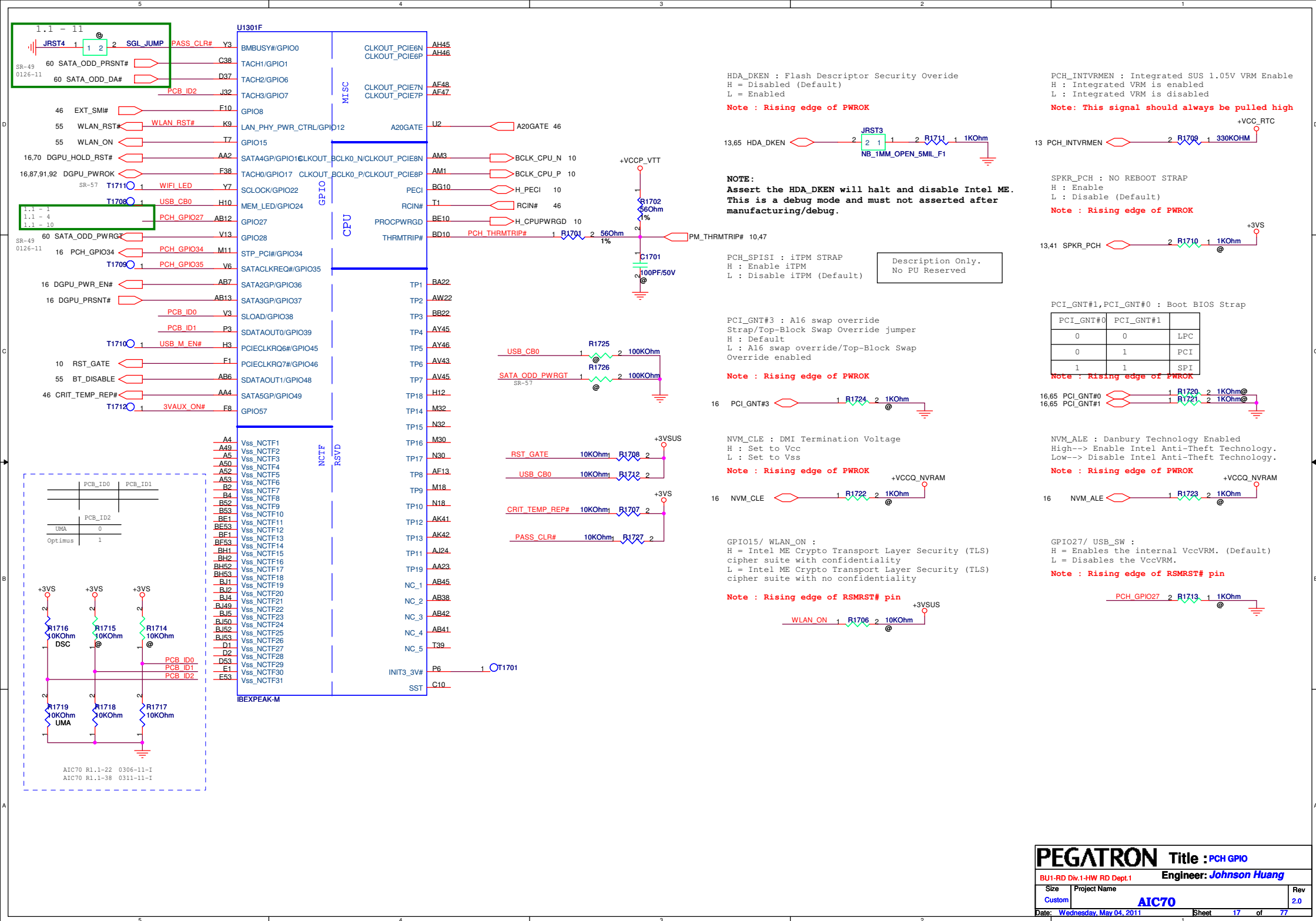


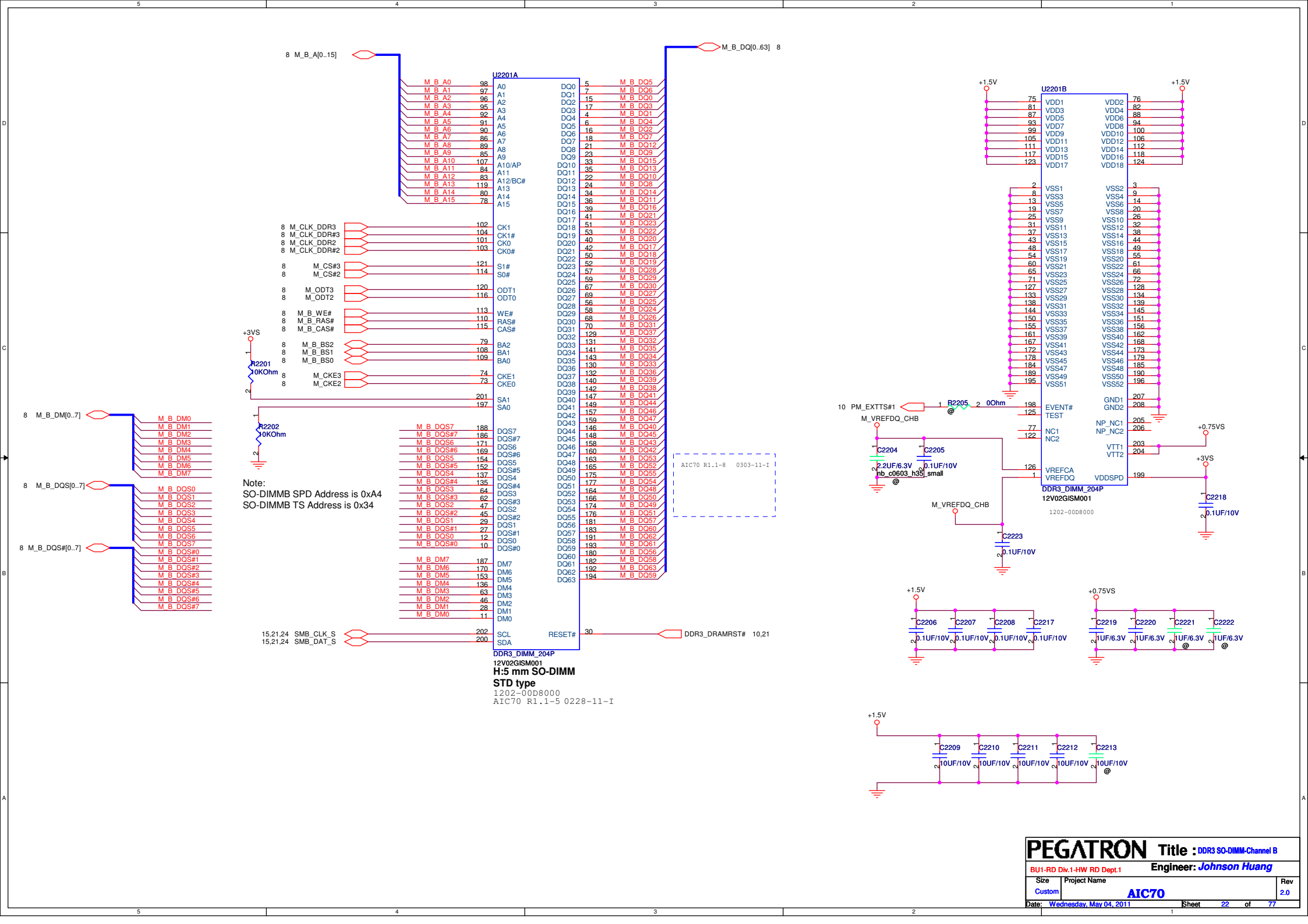
Damping CPU Side

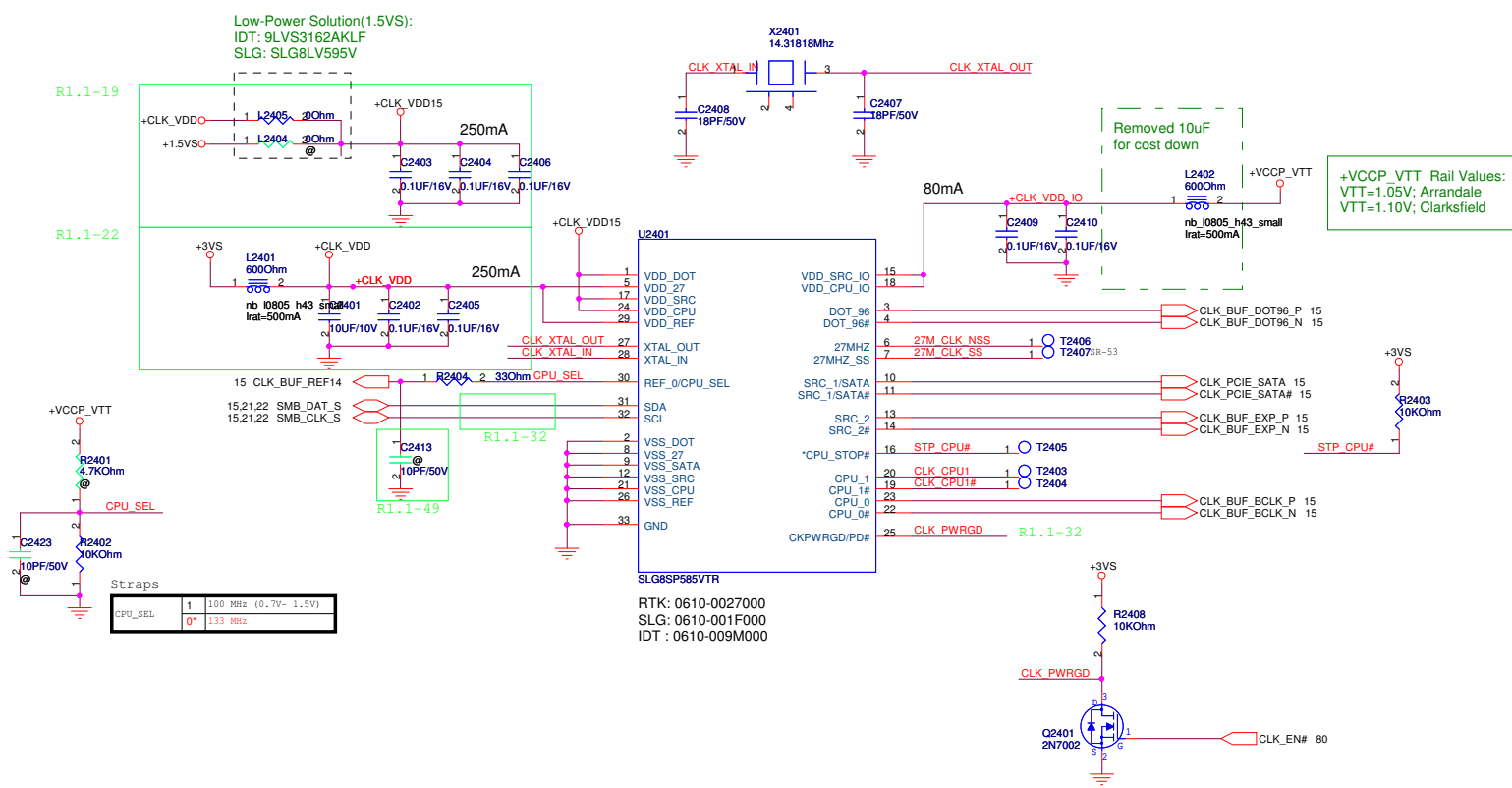


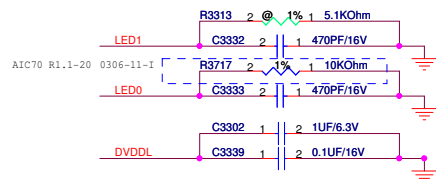
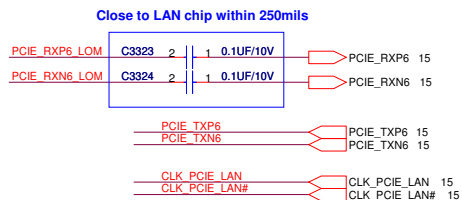
For UMA Change to 10PF



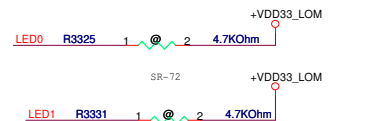








Modify H/W strap setting

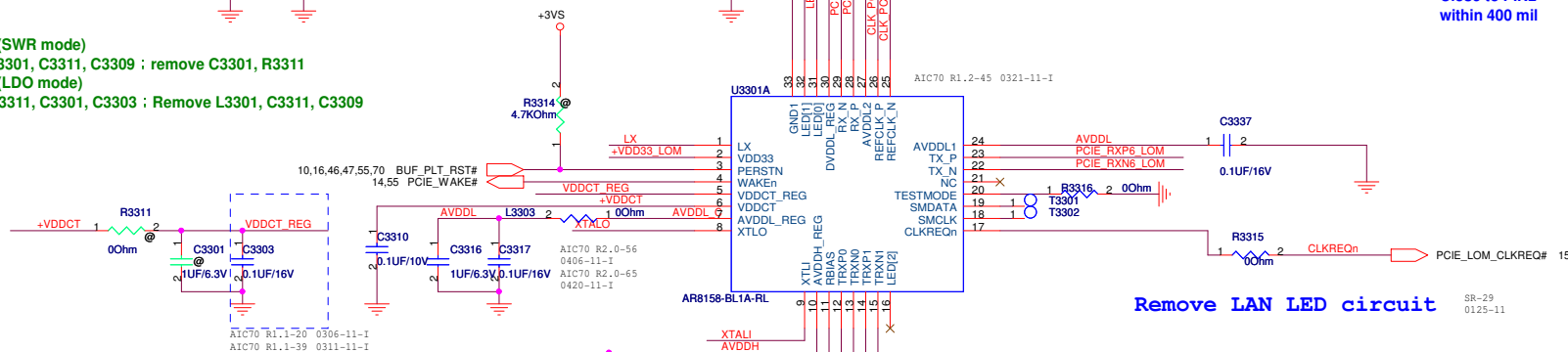
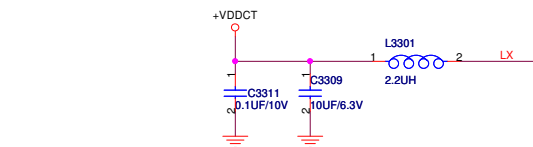


Pow-on strapping

- (1) LED[0]: enable overclocking
pull-high: overclocking (default)
stuff R3326, R3324; Remove R3317, R3325, R3327;
pull-low: un-overclocking
stuff R2, R3325, R3327; Remove R3326, R3324

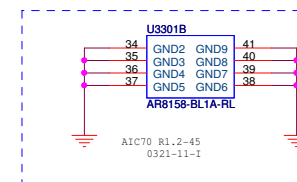
- (2) LED[1]: selection for AR8158's internal VDDCT (SWR/LDO)
pull-high: SWR mode
stuff R3330, R3332; Remove R3313, R3331, R3333;
pull-low: LDO mode
stuff R3313, R3331, R3333; Remove R3330, R3332

AR8158 (SWR mode)
Stuff L3301, C3311, C3309 : remove C3301, R3311
AR8158 (LDO mode)
Stuff R3311, C3301, C3303 : Remove L3301, C3311, C3309



Close to PIN2 within 400 mil

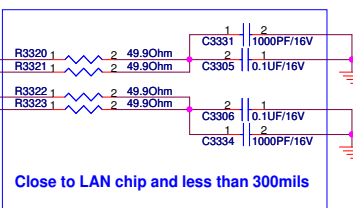
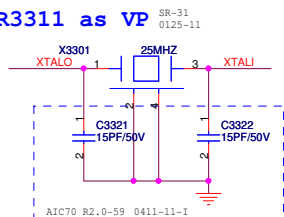
Close to PIN2 within 200 mil



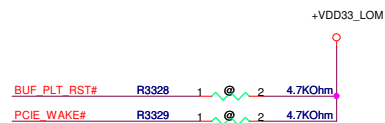
Remove LAN LED circuit

SR-29
0125-11

Modify R3311 as VP



Close to LAN chip and less than 300mils

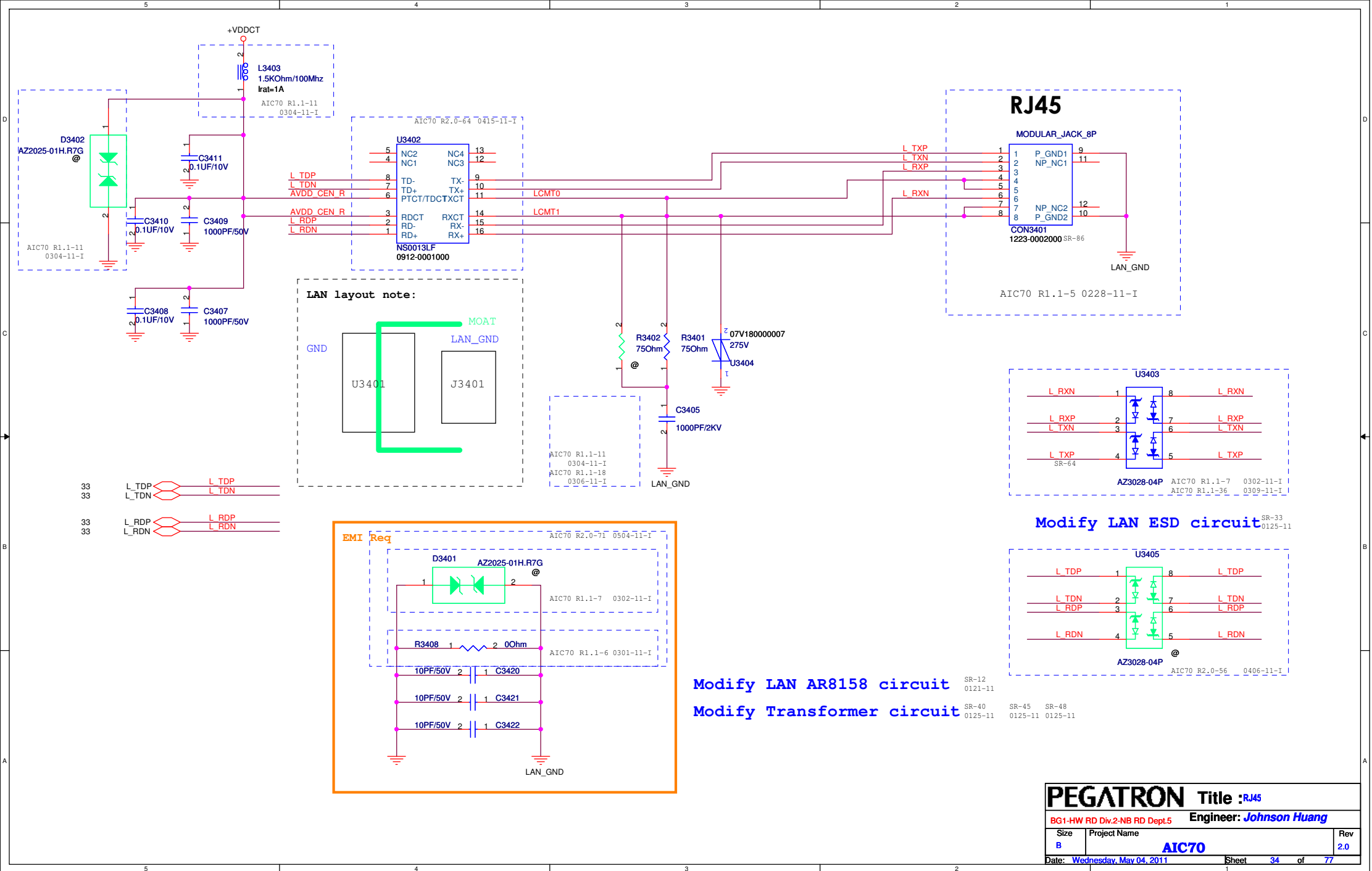


Modify LAN AR8158 circuit

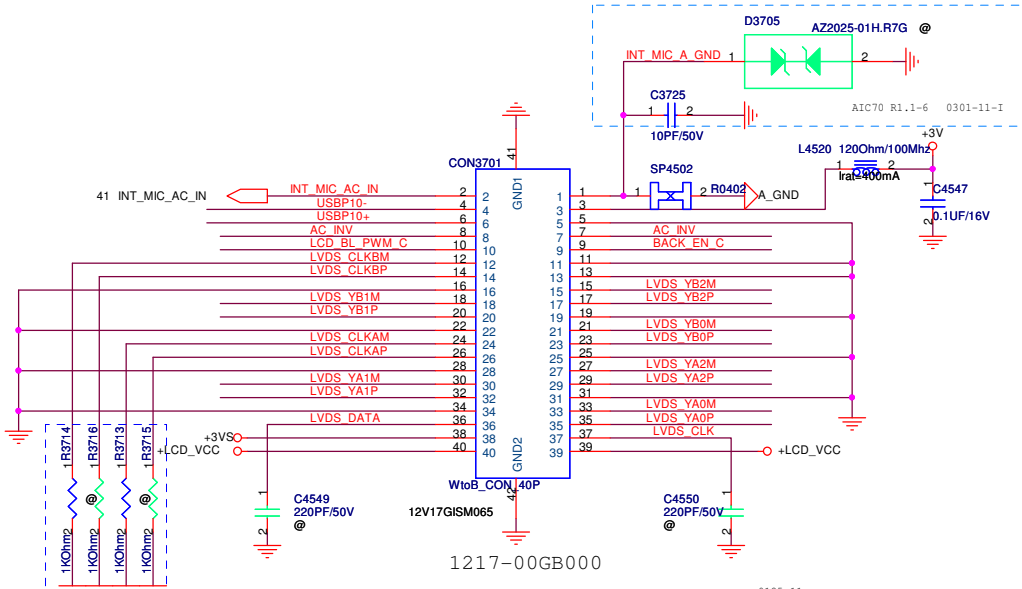
SR-12
0121-11

Change U3301 to AR8158 Part and remover SM BUS

SR-32
0125-11

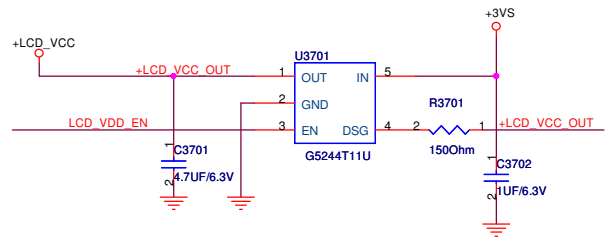
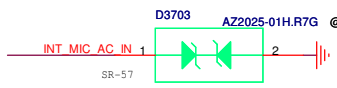
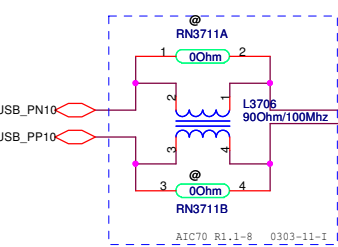
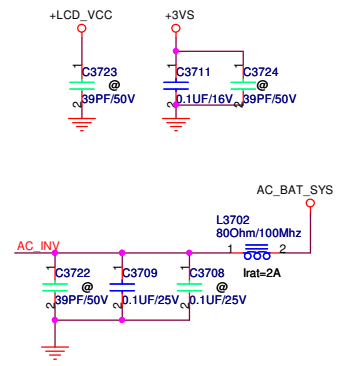
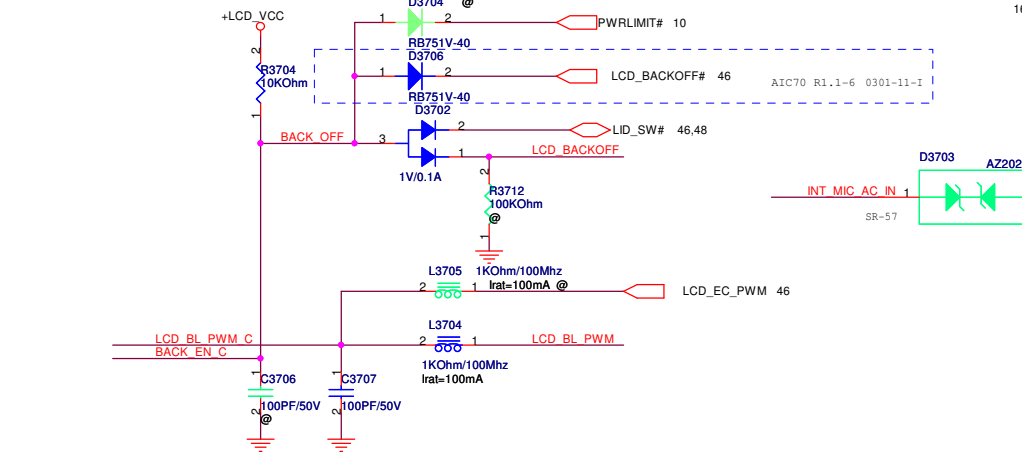


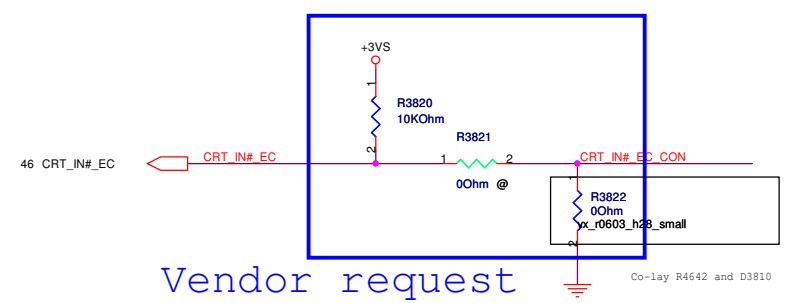
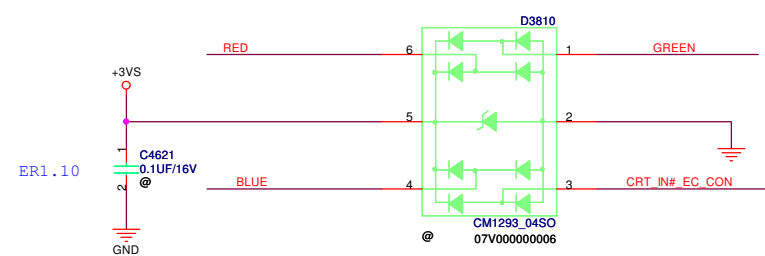
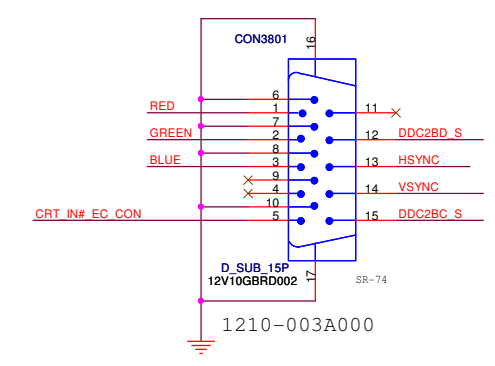
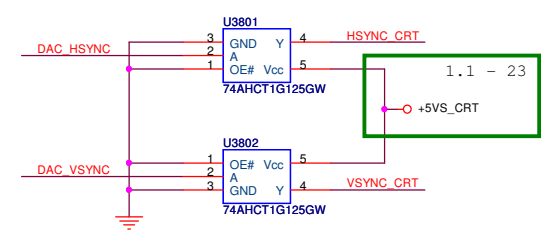
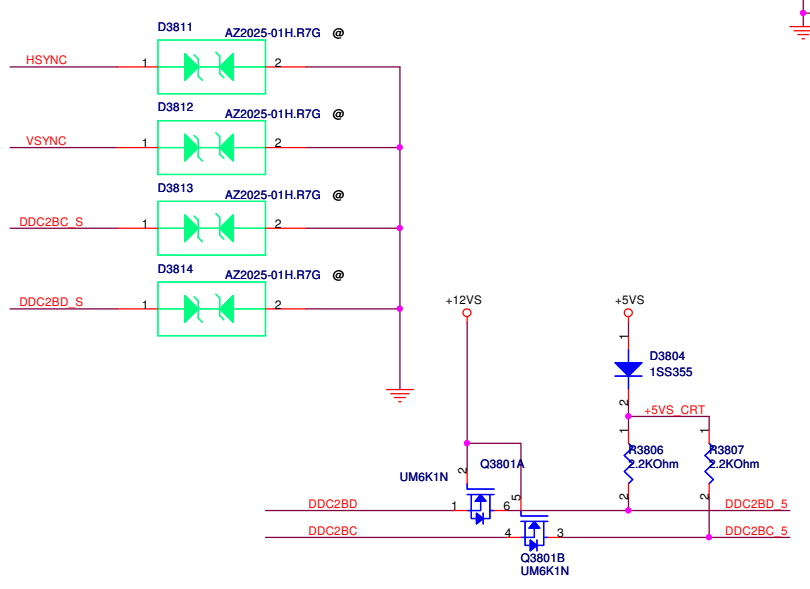
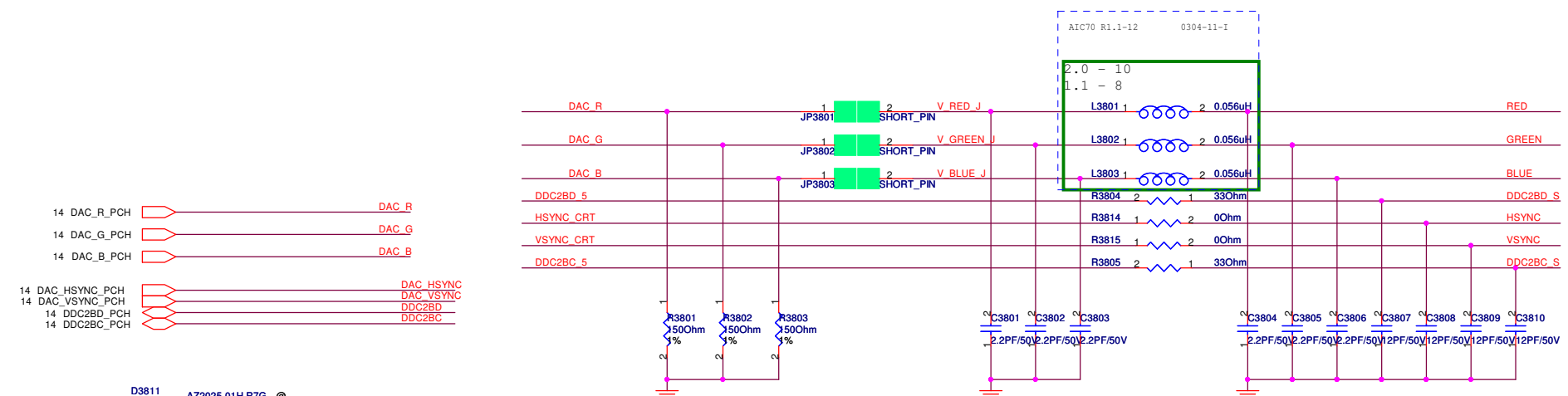
LVDS Conn w/Camera Module & Int Mic



EMI Request

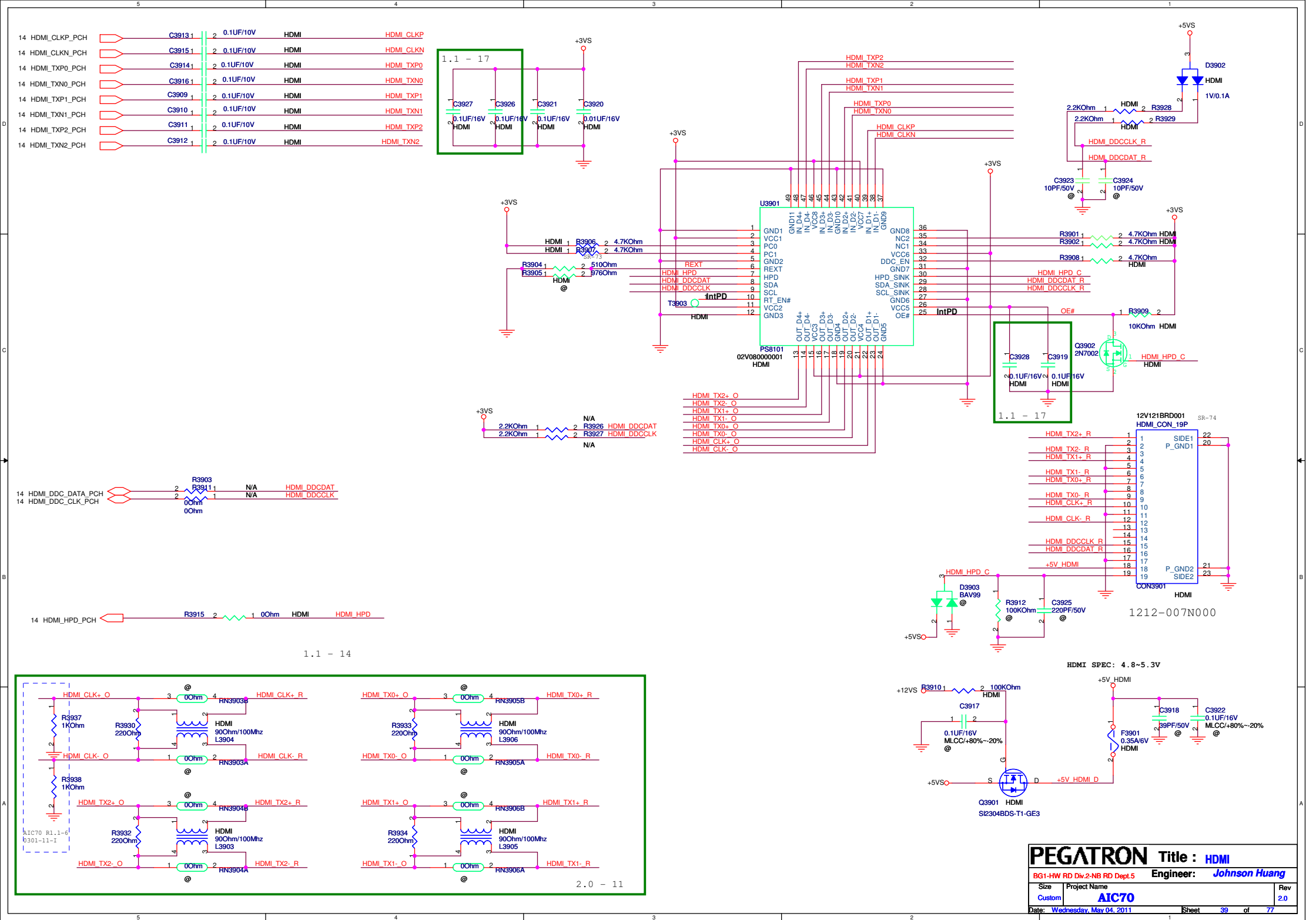
Modify LVDS Pin definition





Del F3801, C3811 ADD CRT IN SR-36 0125-11

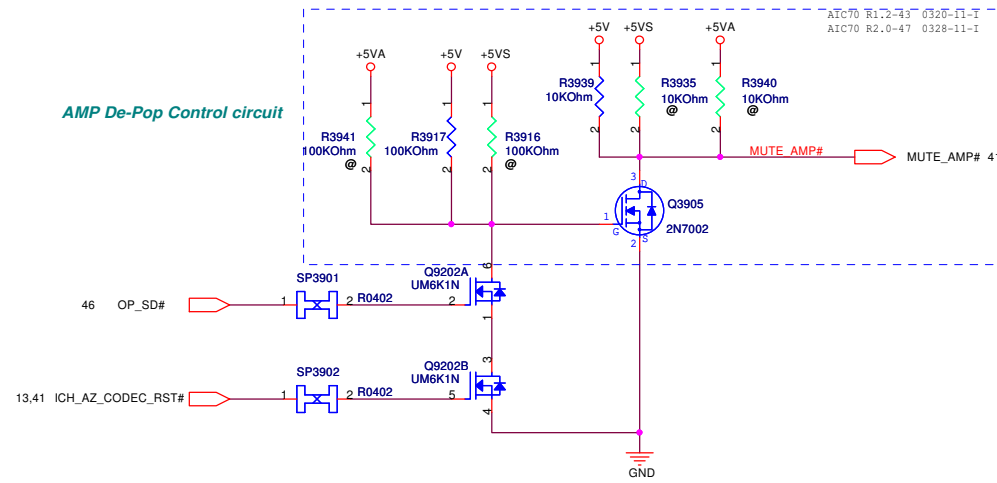
Vendor request





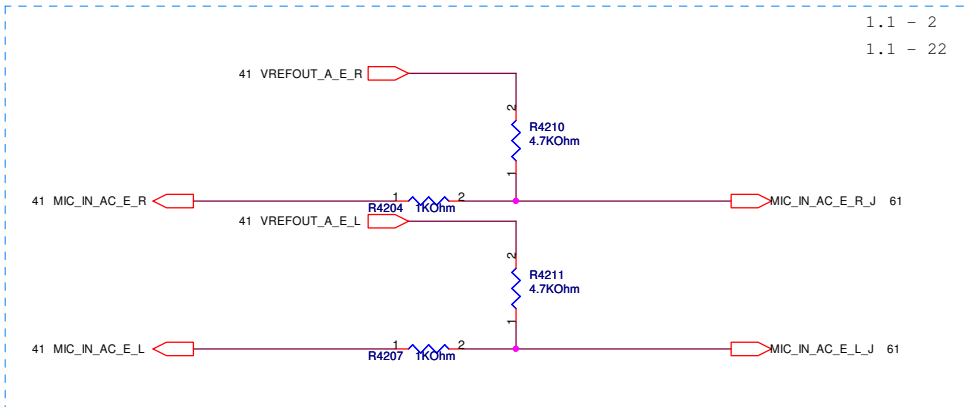
PEGATRON		Title : <i>Display Port</i>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Johnson Huang</i>	
Size Custom	Project Name AIC70		Rev 2.0
Date: <i>Wednesday, May 04, 2011</i>		Sheet 40 of 77	

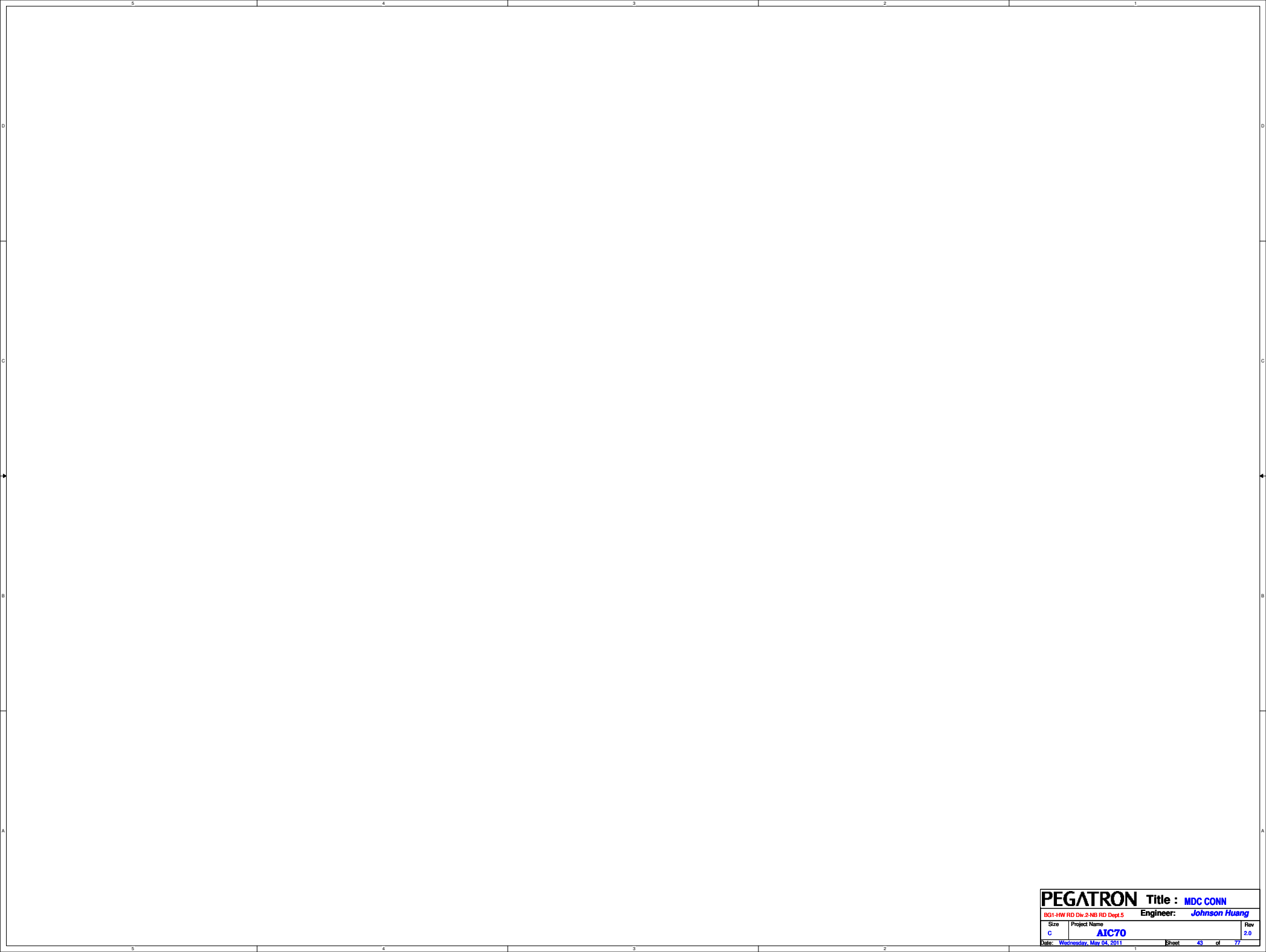
AMP De-Pop Control circuit



Modify De-Pop circuit

SR-43
0125-11





PEGATRON		Title : MDC CONN	
BG1-HW RD Dw.2-NB RD Dept.5		Engineer: Johnson Huang	
Size	Project Name		Rev
C	AIC70		2.0
Date: Wednesday, May 04, 2011		Sheet	43 of 77



Del Entry audio circuit

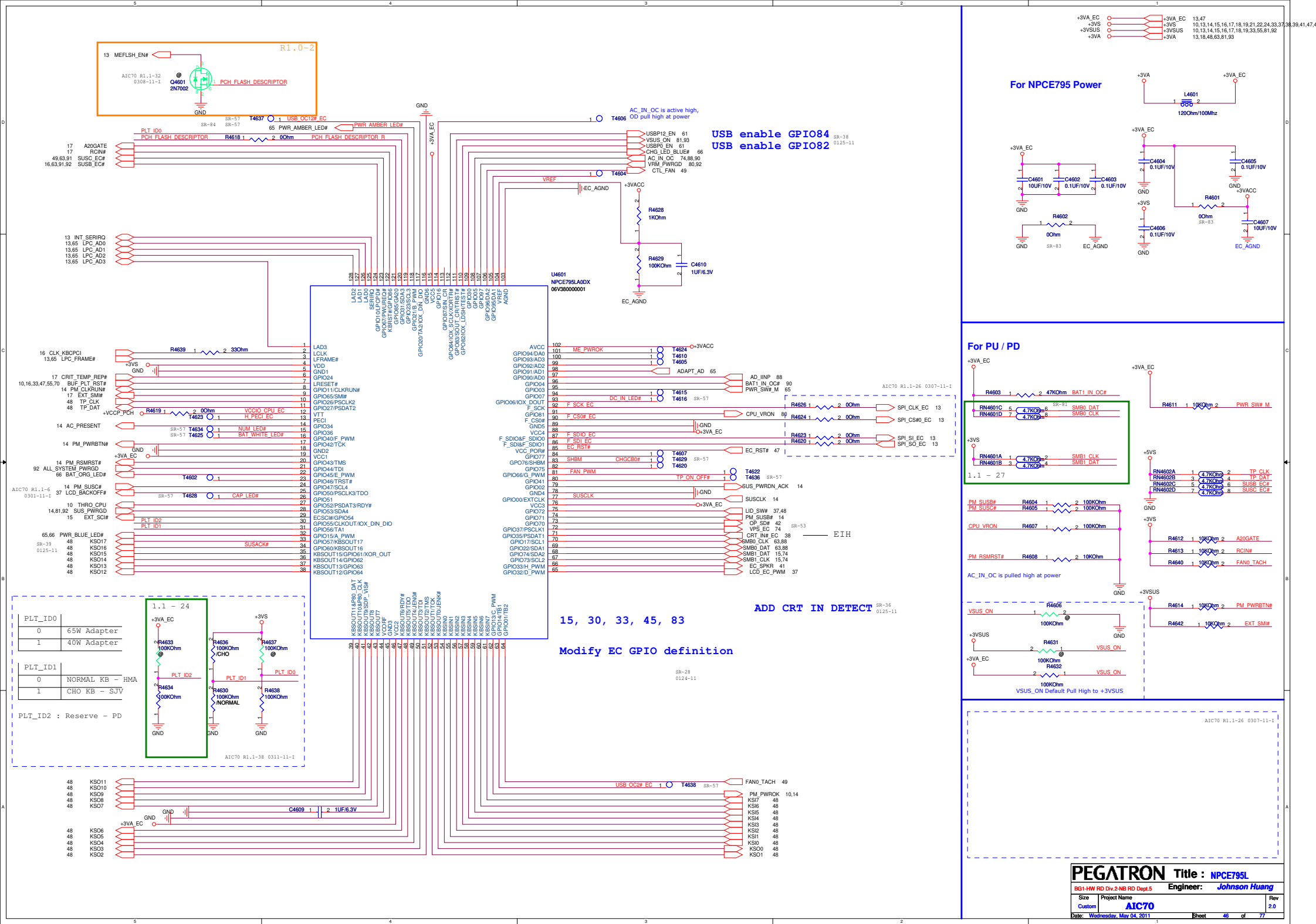
SR-8
0121-11



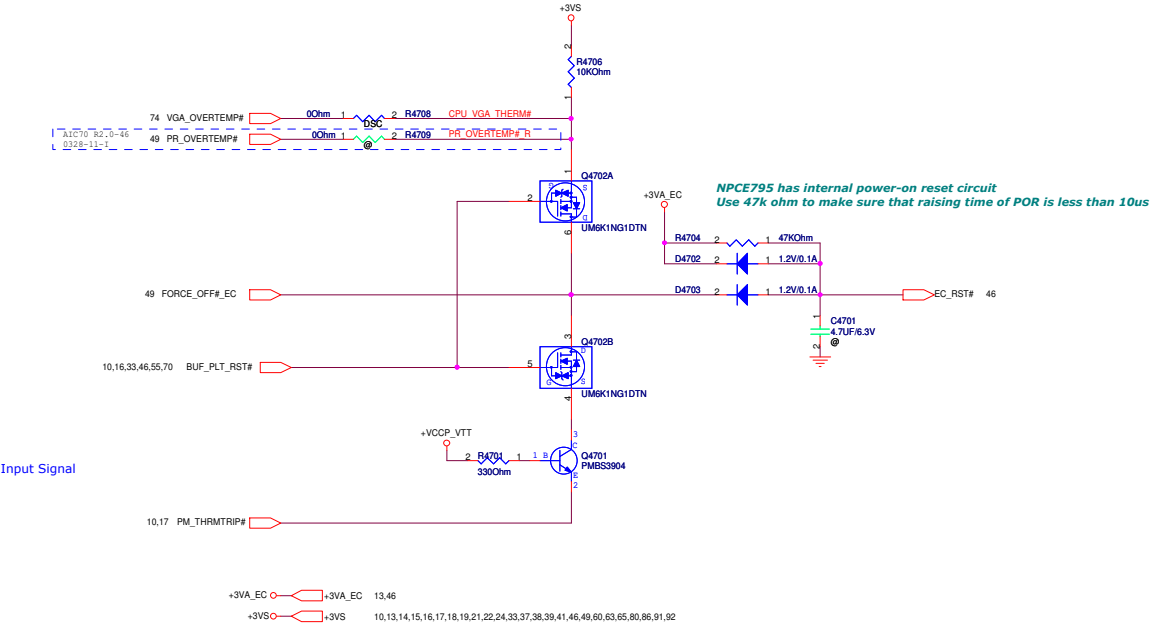
Del Entry audio circuit

SR-8
0121-11

PEGATRON		Title : AUDIO ALC269	
BU1-RD Div.1+HW RD Dept.1		Engineer: Johnson Huang	
Size Custom	Project Name AIC70	Date: Wednesday, May 04, 2011	Rev 2.0
Date: Wednesday, May 04, 2011		Sheet 45 of 77	

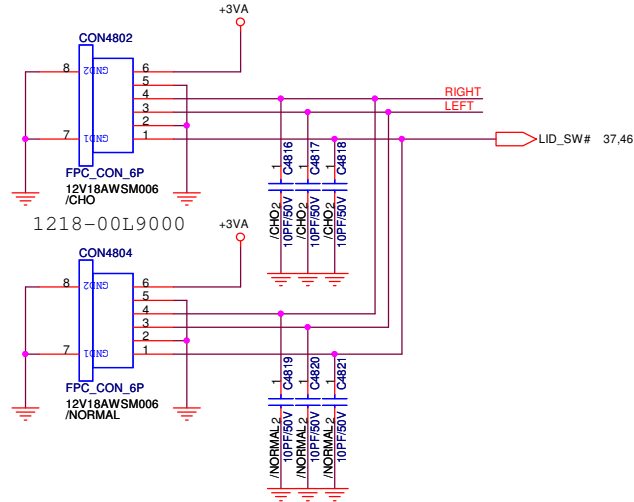


Thermal Policy

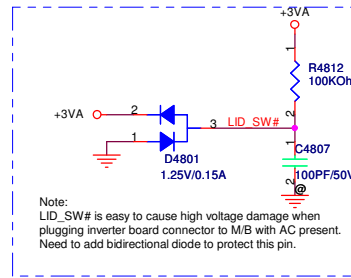


Touch Pad Button/ Hall Sensor

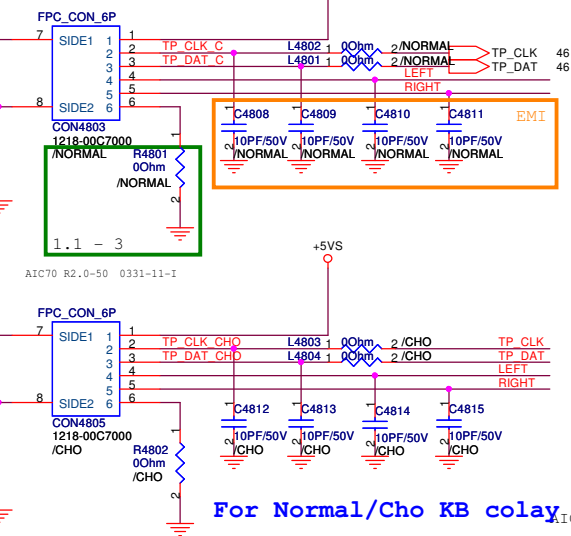
AIC70 R1.1-23 0306-11-I
AIC70 R1.1-35 0309-11-I



close to U4601



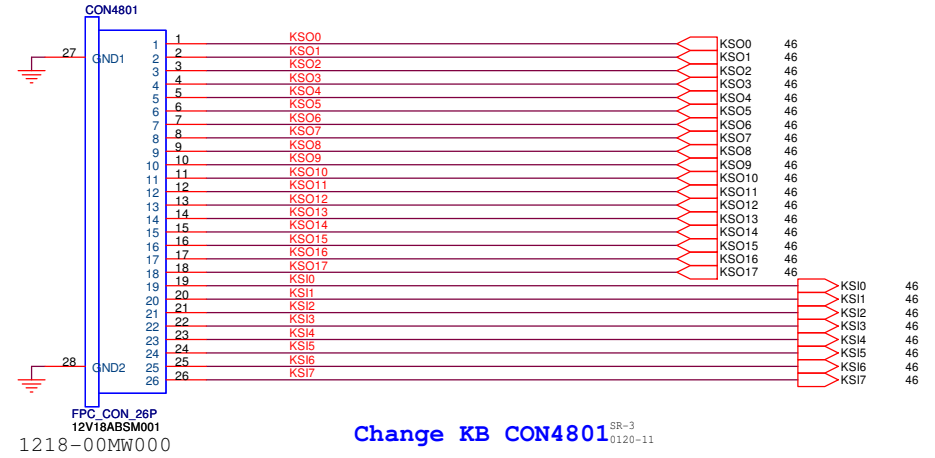
Touch Pad



For Normal/Cho KB colay 0224-11-I
AIC70 R1.1-4

Remove TP button circuit SR-22
0124-11

Keyboard FOR 17"



Change KB CON4801 SR-3
0120-11

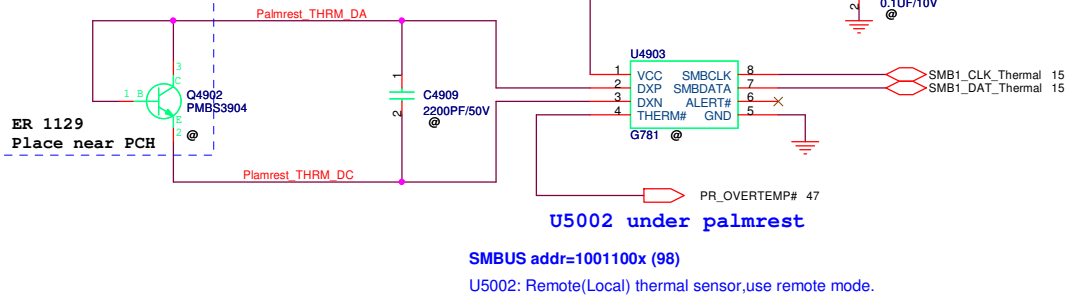
Change KB CON4801 PIN definition SR-25
Reverse KB CON4801 0124-11
SR-19 SR-52
0124-11 0126-11

Remove 15'' KB connector AIC70 R1.1 - 1
0224-11 - I

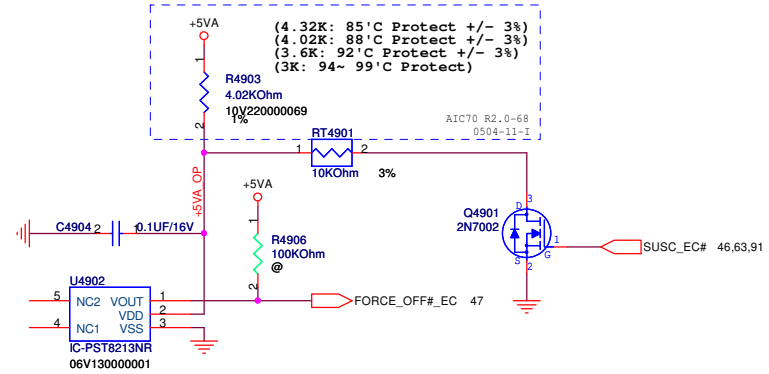
Palm Rest Thermal Sensor

PHILIP PMBS3904

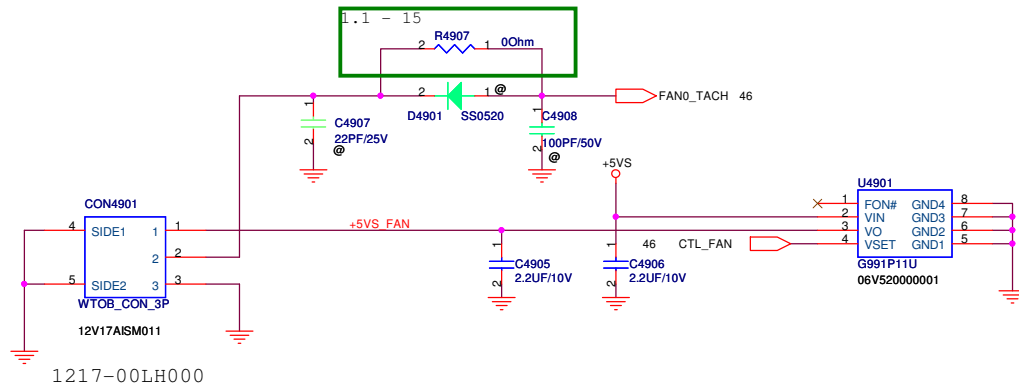
Place in the center of Plamrest.

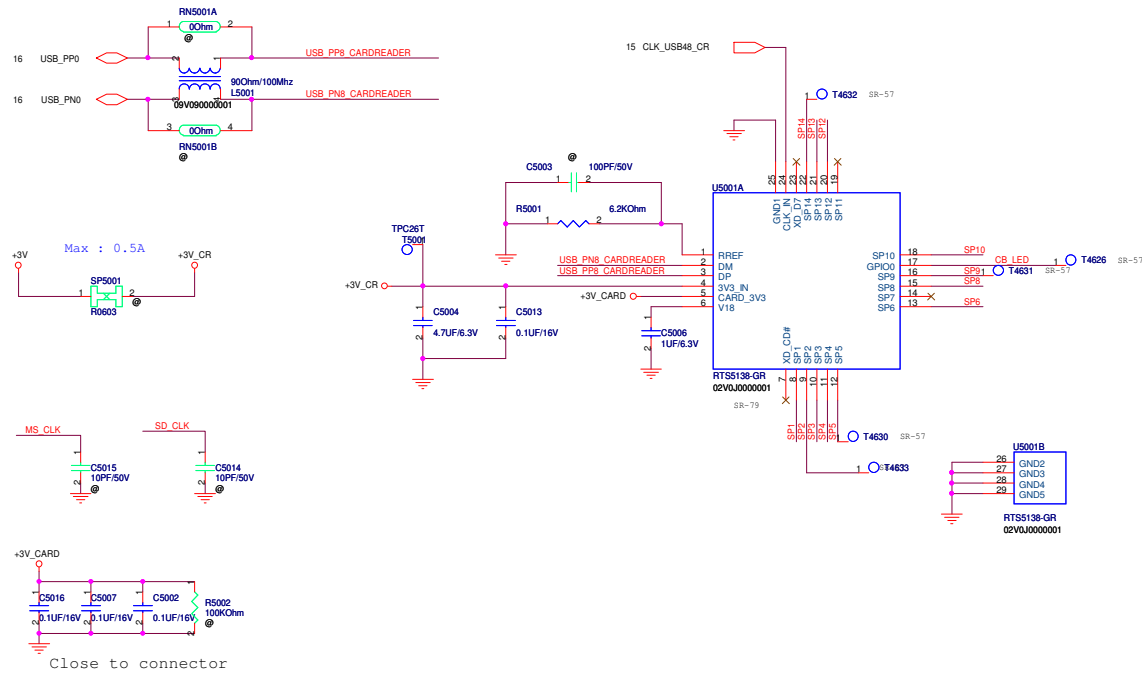


Thermister



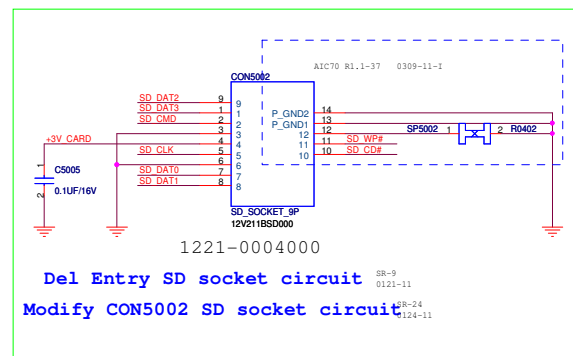
FAN

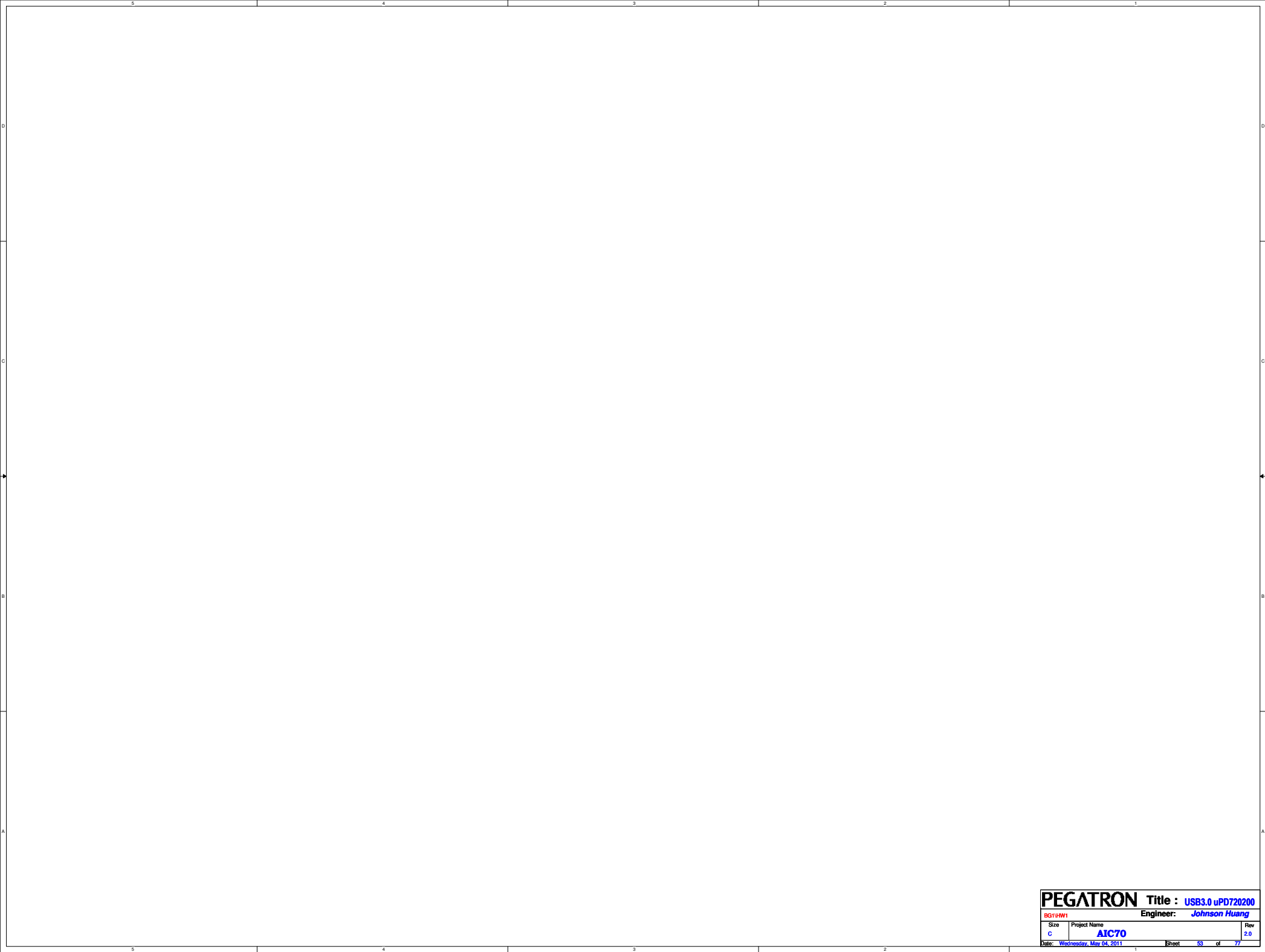




Pin Name	Description
SP1	SDWP# / MCLK
SP2	MS_INS#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD_WP#	MS_CLK
SP2		MS_INS#
SP3	SD_DAT1	
SP4	SD_DAT0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_DAT3	MS_D1
SP13	SD_DAT2	
SP14		MS_BS

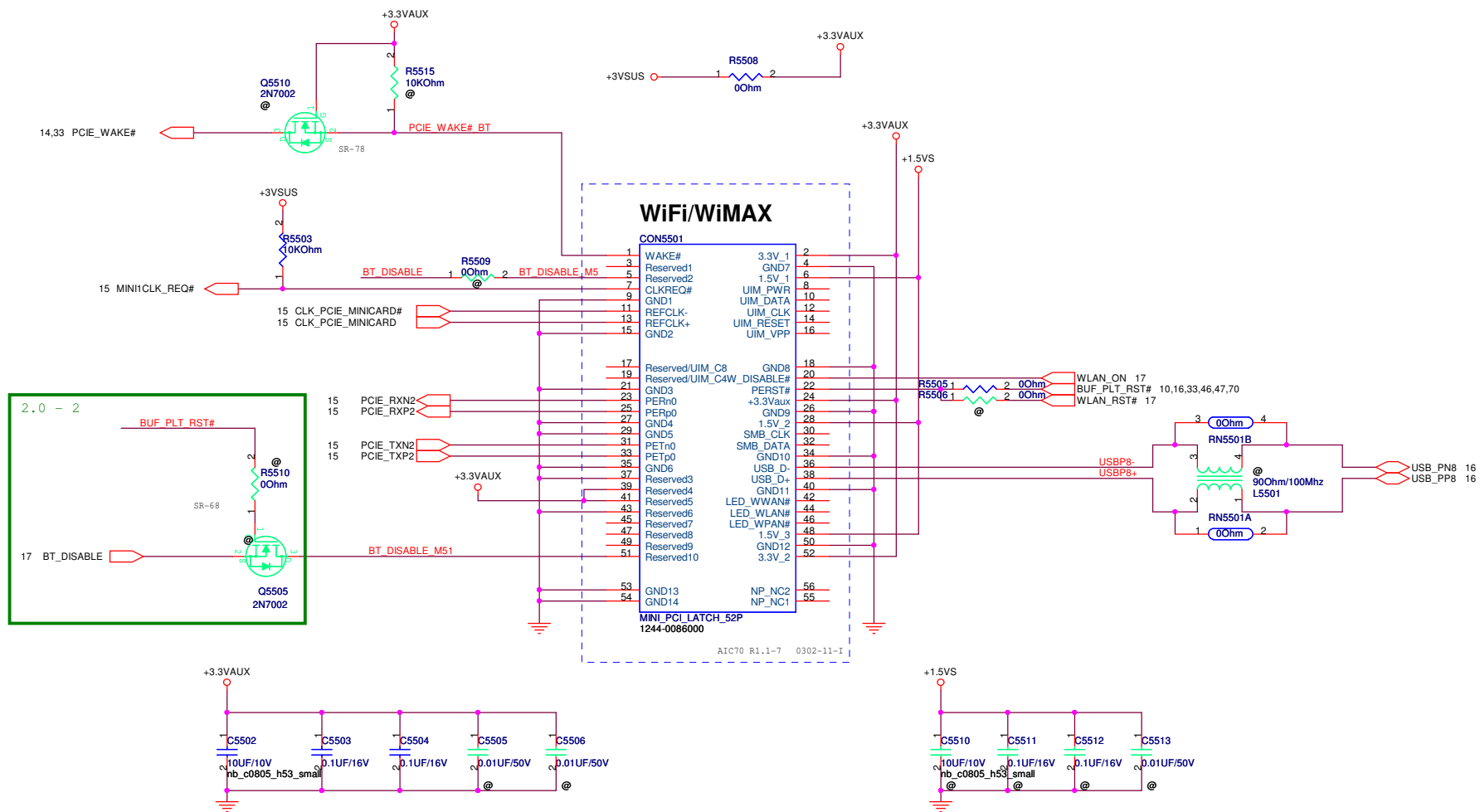




PEGATRON		Title : USB3.0 uPD720200	
BG1VHW1		Engineer: Johnson Huang	
Size	Project Name		Rev
C	AIC70		2.0
Date: Wednesday, May 04, 2011		Sheet	53 of 77



PEGATRON		Title : PCIE NEW CARD	
BU1-RD Div.1+HW RD Dept.1		Engineer: Johnson Huang	
Size	Project Name		Rev
Custom	AIC70		2.0
Date: Wednesday, May 04, 2011		Sheet	54 of 77

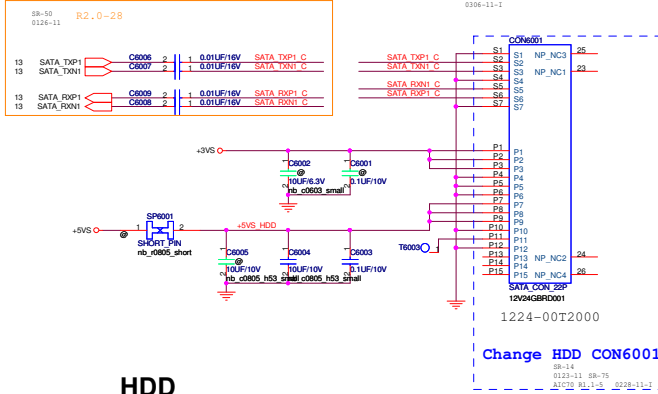
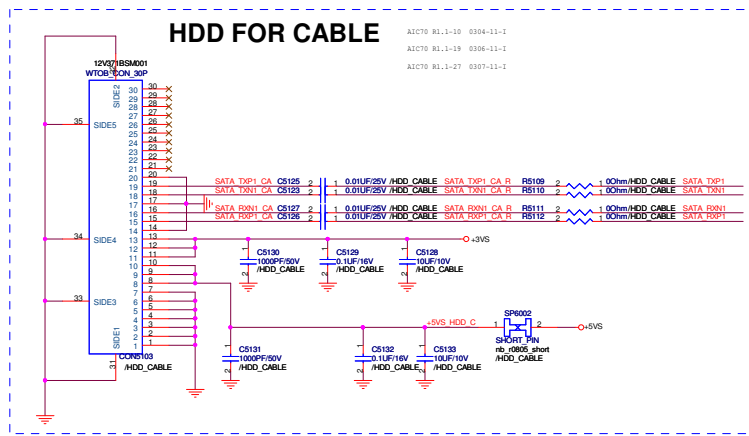




PEGATRON		Title : MINICARD (WWAN)	
BU1-RD Div.1-HW RD Dept.1		Engineer:	
Size	Project Name	Rev	
Custom		2.0	
Date: Wednesday, May 04, 2011		Sheet	56 of 77

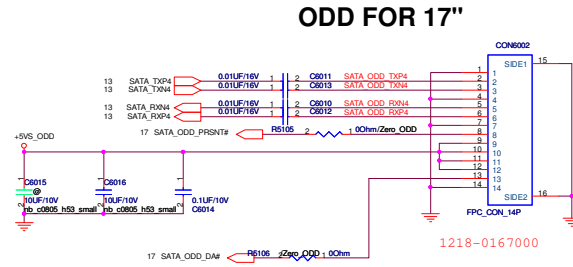


PEGATRON		Title : MINICARD (WUSB /UPCONVERT)	
BU1-RD Div.1+HW RD Dept.1		Engineer: Johnson Huang	
Size	Project Name		Rev
Custom	AIC70		2.0
Date: Wednesday, May 04, 2011		Sheet	57 of 77



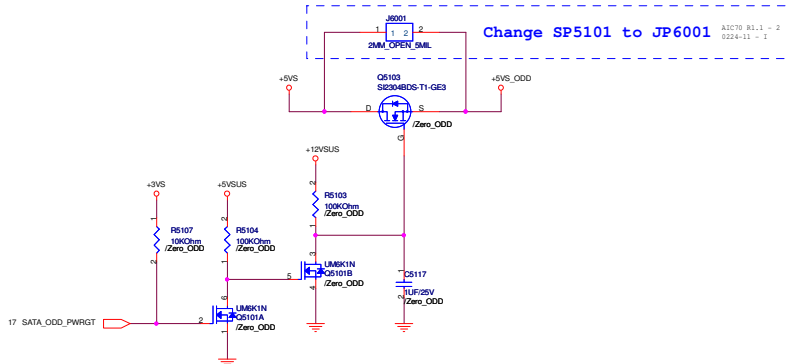
Remove 15'' ODD connector

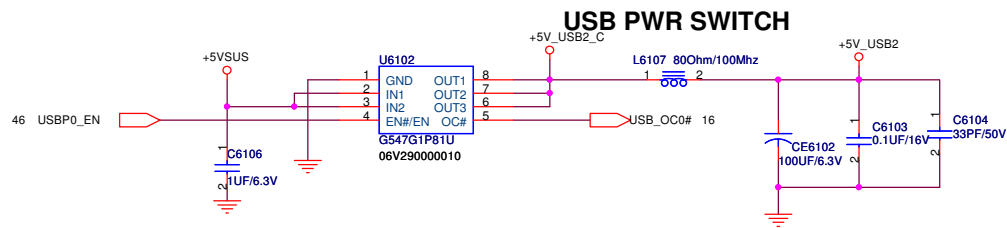
AIC70 R1.1 - 1
0224-11 - 1



ZERO POWER ODD SUPPORT

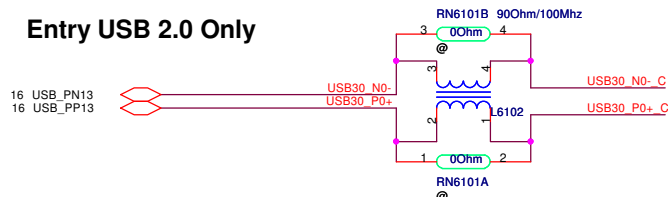
support Hokey turn off ODD power





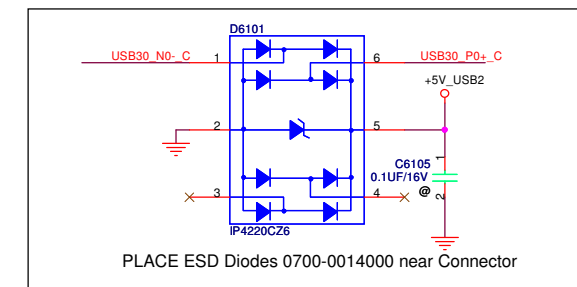
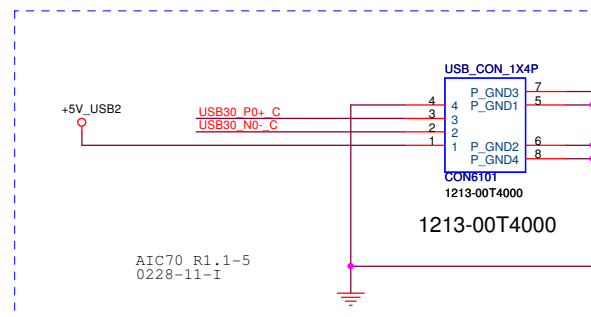
change USB power switch circuit SR~1 0120~11 SR~26 0124~11 SR~34 0125~11

Entry USB 2.0 Only



Modify D6101, RN6101, RN6105, RN6106 SR~30 0125~11

USB 2.0



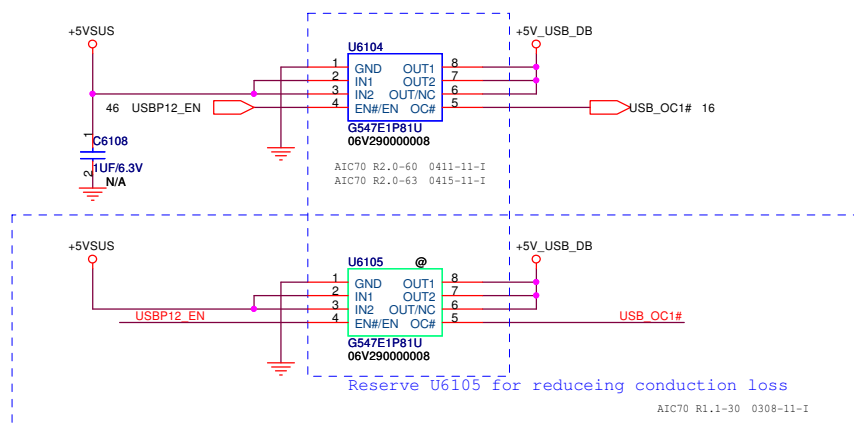
PLACE ESD Diodes 0700-0014000 near Connector

USB Conn. for Entry colay HDMI USB 2.0

Remove USB_9 (HDMI) SR~21 0124~11

USB Power Switch for USB DB Main

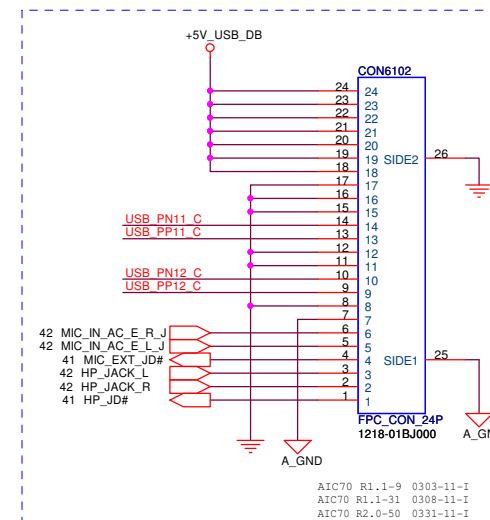
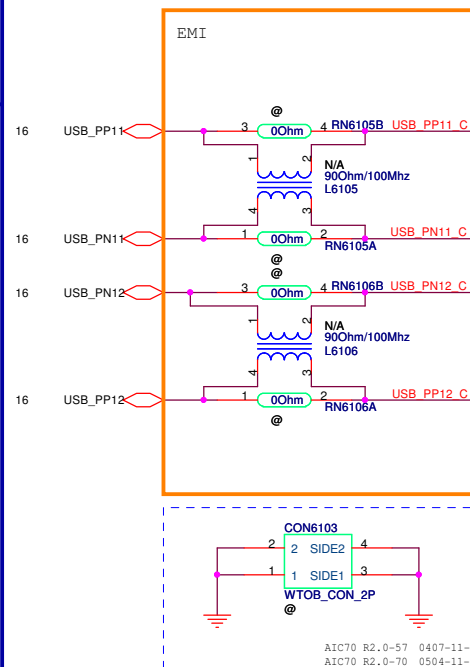
change USB power switch circuit SR~26 0124~12 SR~38 0125~13



Reserve U6105 for reduceing conduction loss

AIC70 R1.1~30 0308~11~I

AUDIO BOARD/w USB2.0 x2



AIC70 R1.1~9 0303~11~I
AIC70 R1.1~31 0308~11~I
AIC70 R2.0~50 0331~11~I

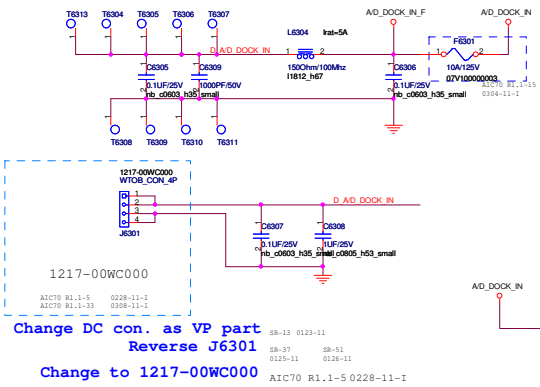
TouchPanel CON

Camera Module CON

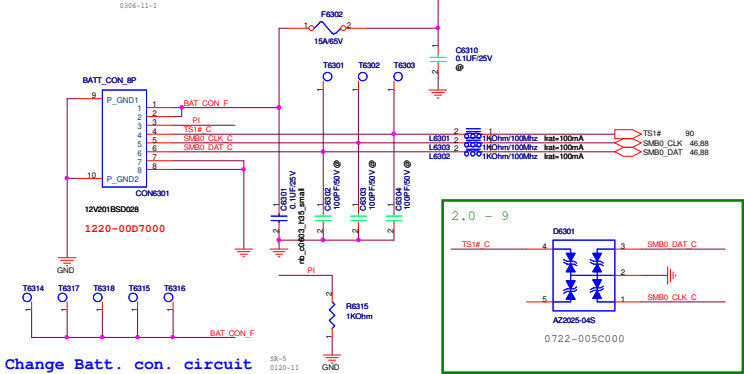
B/T MODULE

FELICA MODULE

DC IN

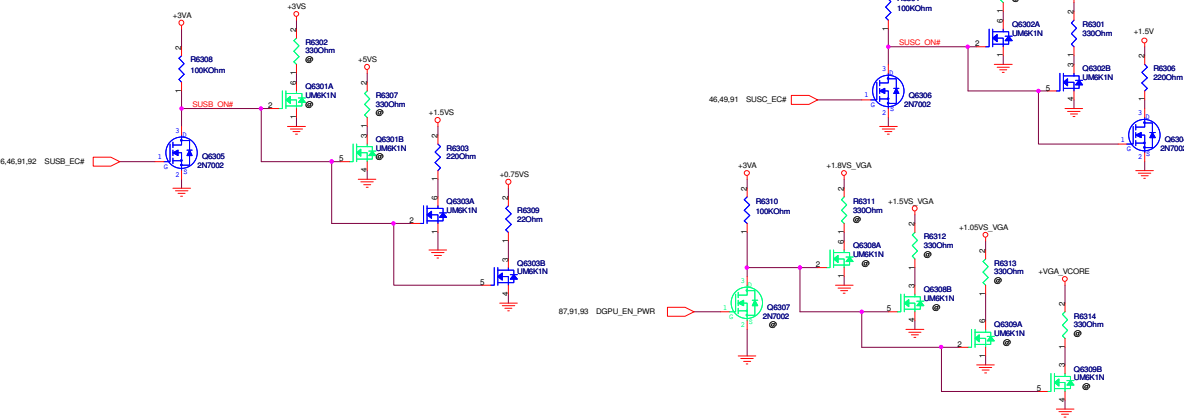


Battery Connector 17"



Remove 15" Battery connector

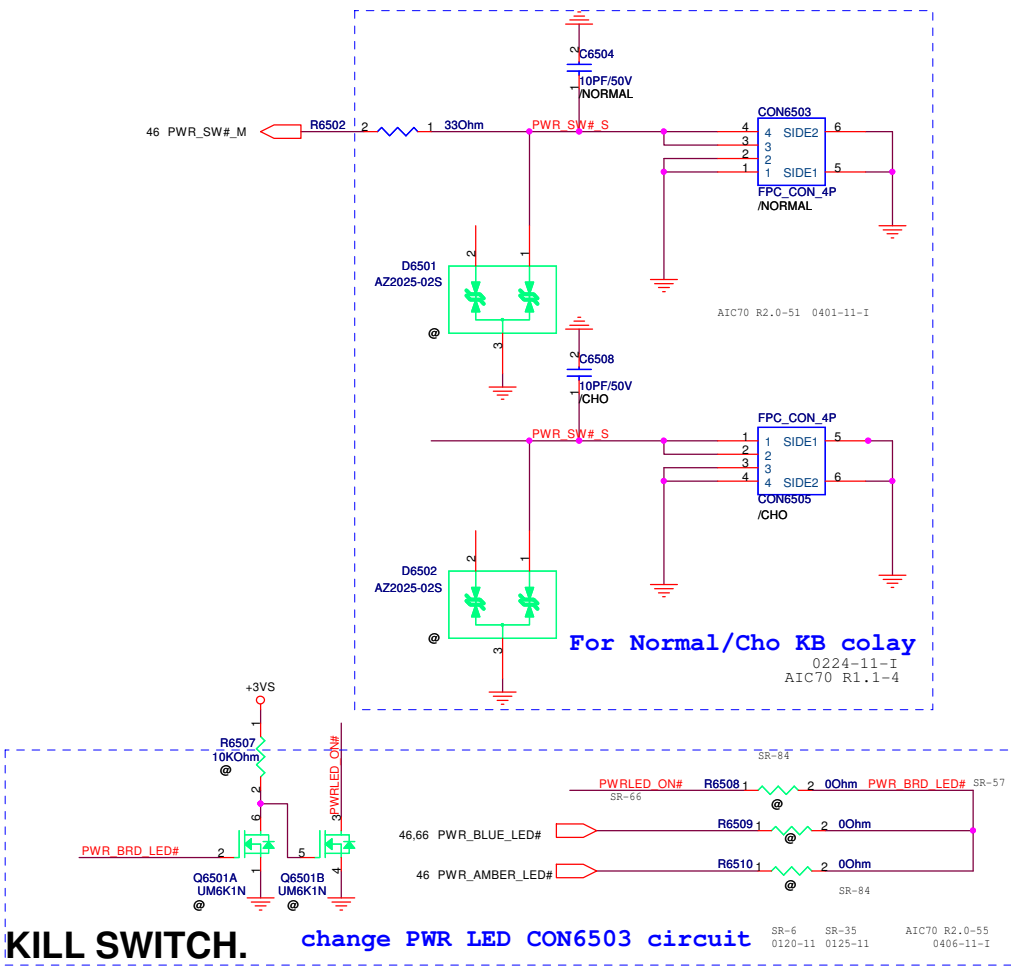
Discharge Circuit





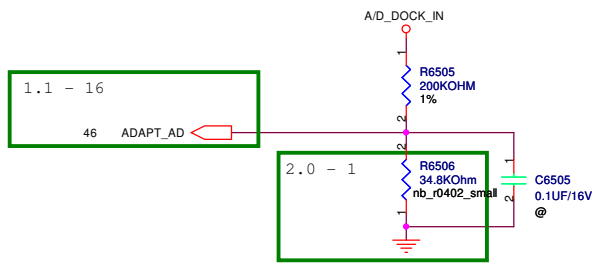
Notes:
BRAIDWOOD right angled Connector (1.8V keyed)
Compatible BRAIDWOOD Modules
1.8V Mobile NVM 4GB 31.60mm x21.5mm
1.8V Mobile NVM 8GB 31.60mm x 21.5mm
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

PWR BRD/ AMBIENT/ HALL CONN. 1.1 - 12 SR-66



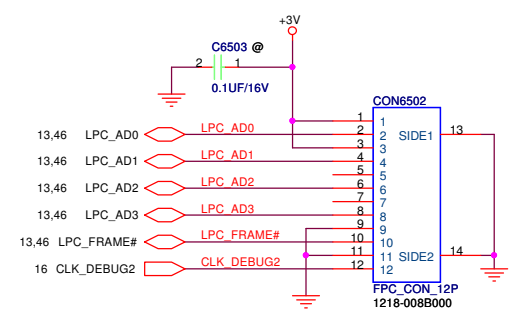
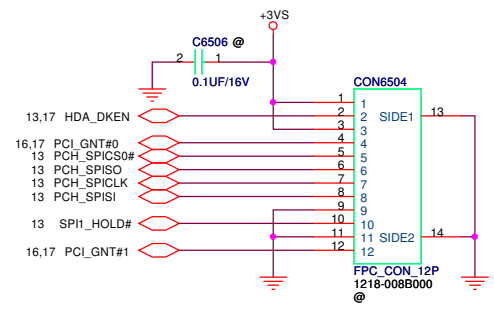
KILL SWITCH. change PWR LED CON6503 circuit

ADAPTOR VOLTAGE DETECTOR.



MODEM MODULE

DEBUG CARD CONN.



LED (Main)

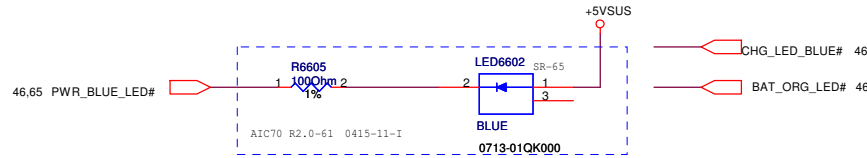
Left

Right

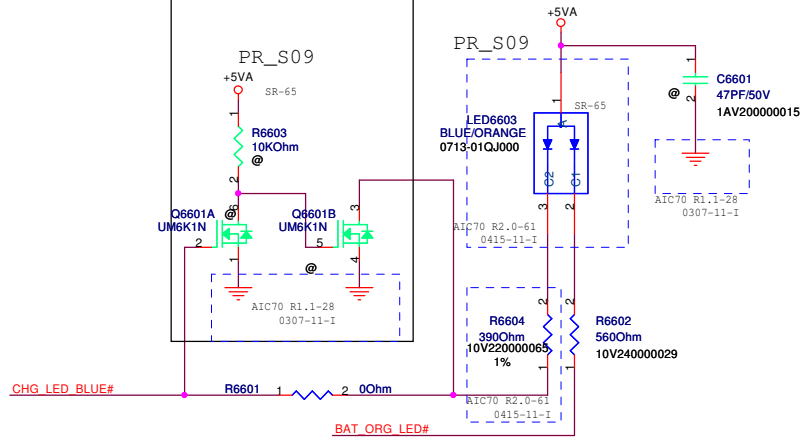


Battery

Power LED



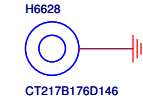
Charger LED



Remover LED circuit SR-18 0124-11

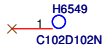
Modify LED circuit SR-28 0124-11 SR-39 0125-11

WLAN NUT

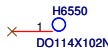


SR-69

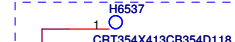
Fix hole



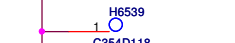
Detail C



Screw Ax10



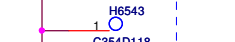
AIC70 R1.1-29 0307-11-I



AIC70 R2.0-52 0401-11-I



AIC70 R2.0-52 0401-11-I



AIC70 R2.0-52 0401-11-I



AIC70 R2.0-52 0401-11-I

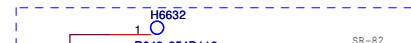


AIC70 R2.0-52 0401-11-I



AIC70 R2.0-52 0401-11-I

Screw Fx2

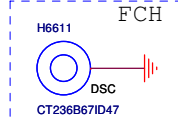


AIC70 R1.1-29 0307-11-I

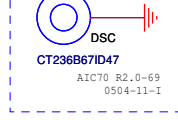


AIC70 R2.0-54 0402-11-I

PCH Local Side Symbol



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I



AIC70 R2.0-69 0504-11-I

PEGATRON Title : LED/ CIR/ FW SCREW

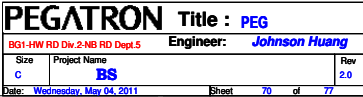
BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

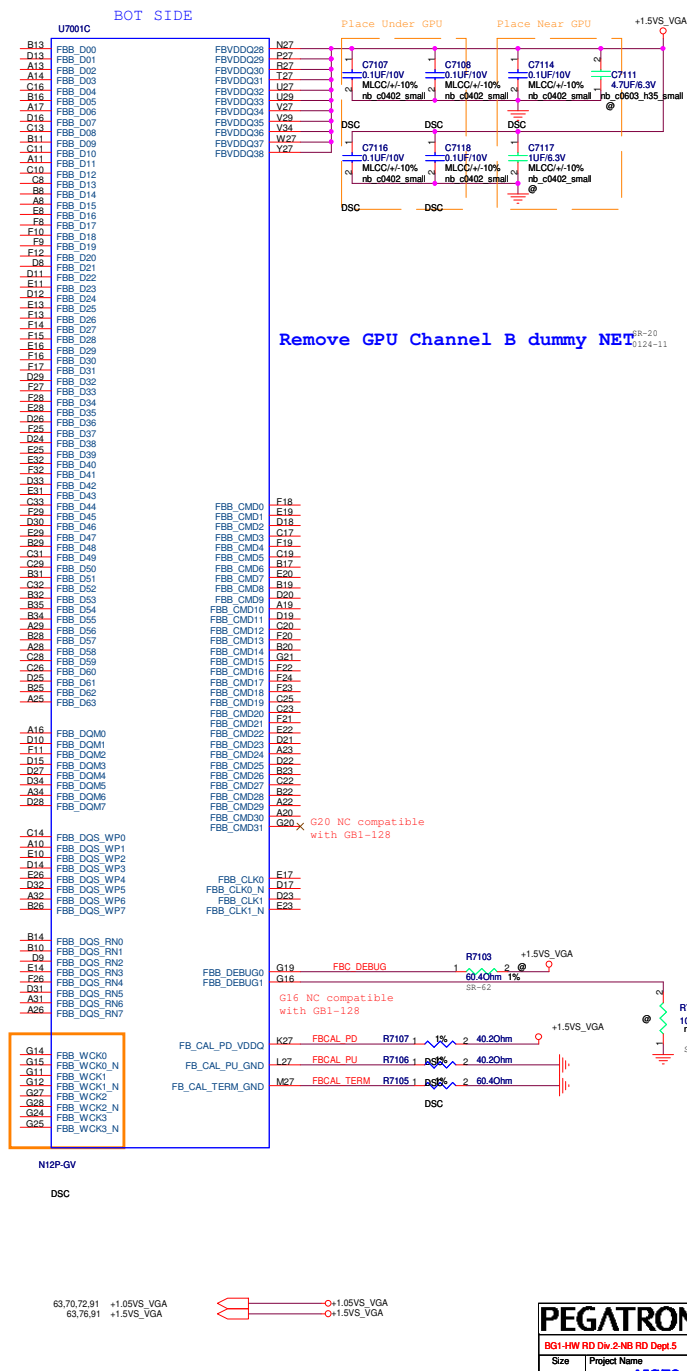
Size Project Name Custom AIC70

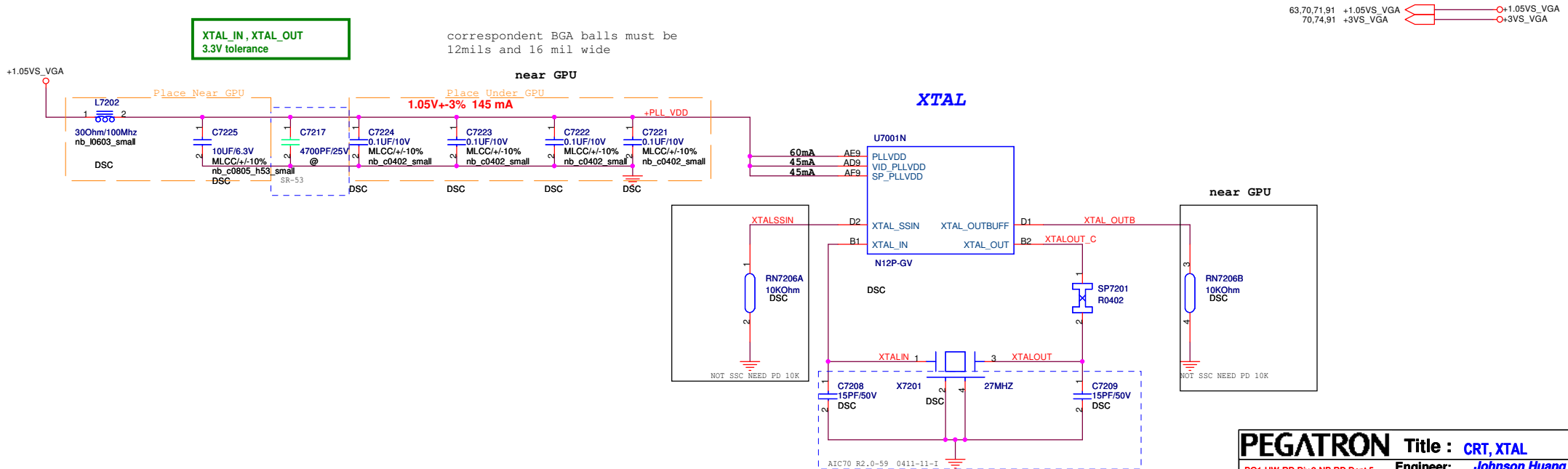
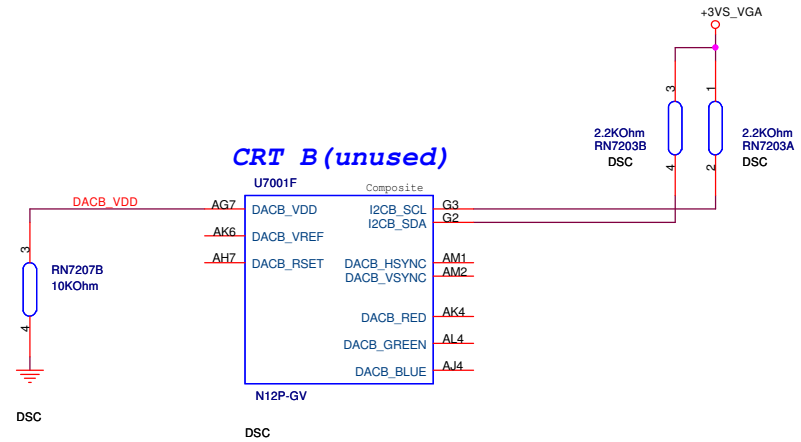
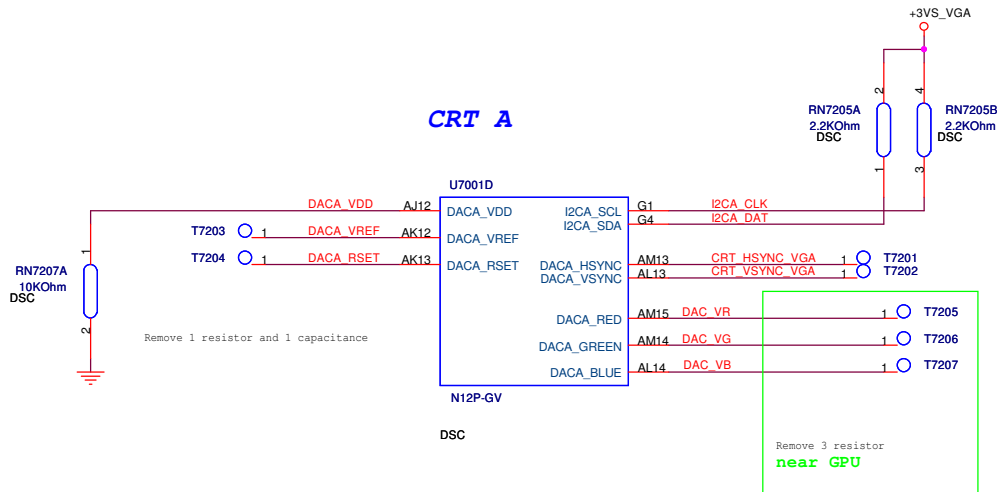
Date: Wednesday, May 04, 2011 Sheet 66 of 77

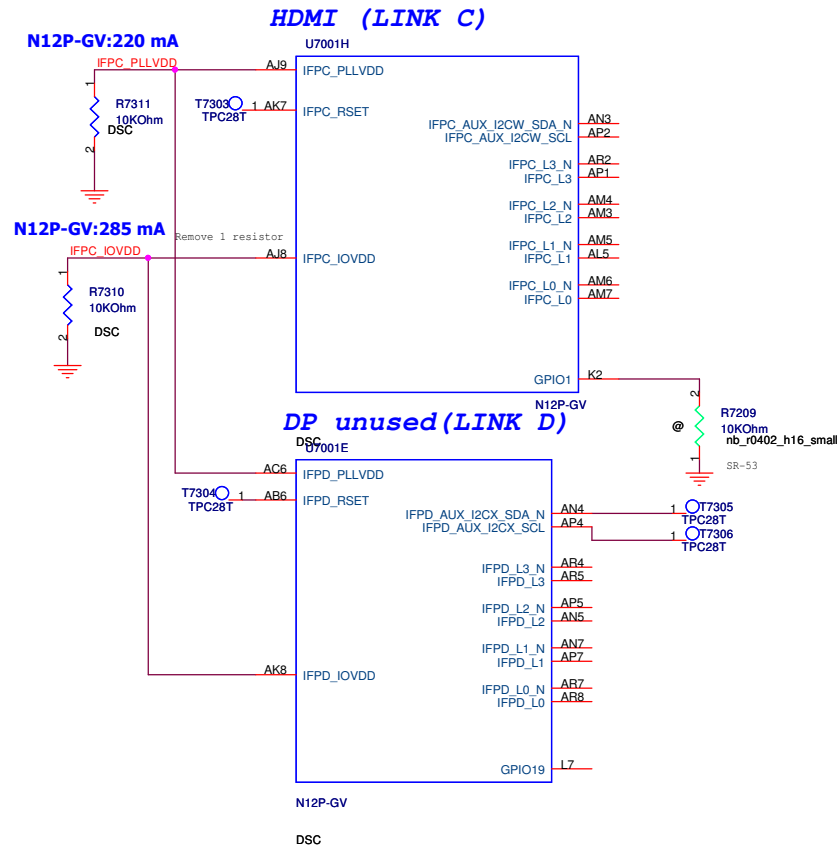
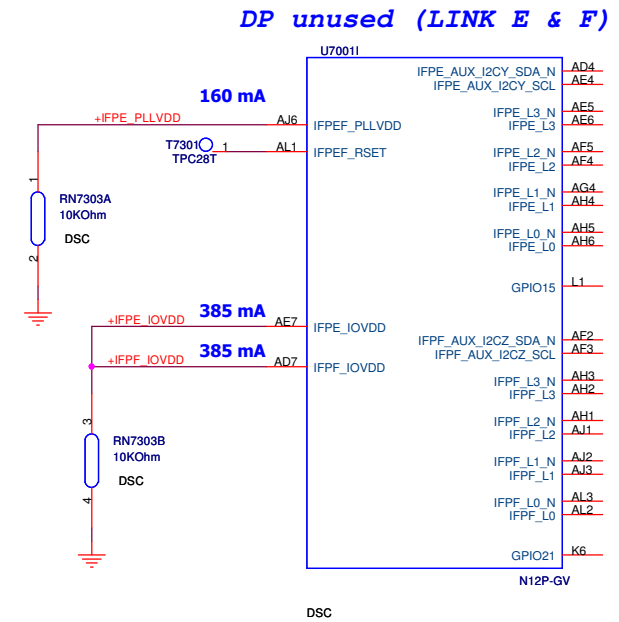
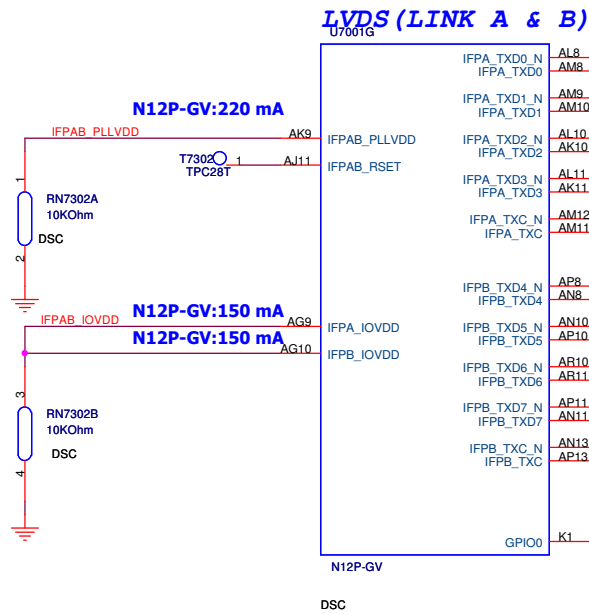


PEGATRON		Title : G-Sensor TSH35TR	
BU1-RD Div.1-HW RD Dept.1		Engineer: Johnson Huang	
Size Custom	Project Name		Rev 2.0
Date: Wednesday, May 04, 2011	Sheet	69	of 77





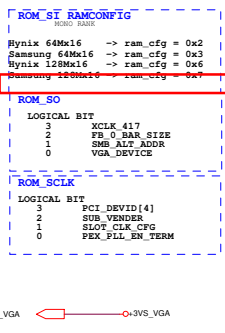
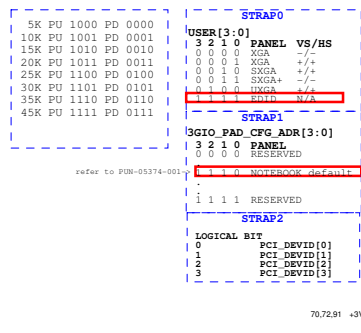
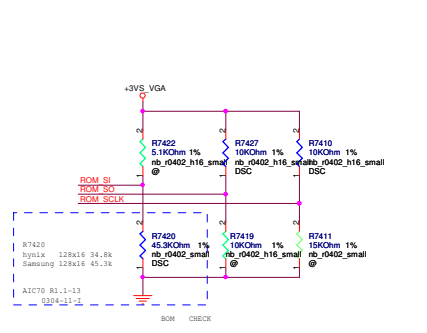
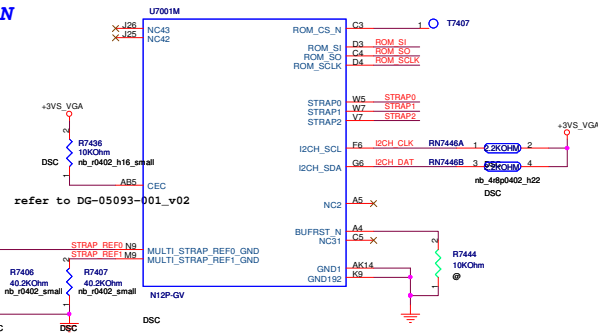




IFPx	A	B	C	D	E	F
TURKEY	LVDS A	LVDS B	HDMI	unused		

63,70,71,72,91 +1.05VS_VGA
63,91 +1.8VS_VGA
70,72,74,91 +3VS_VGA

STRAP PIN

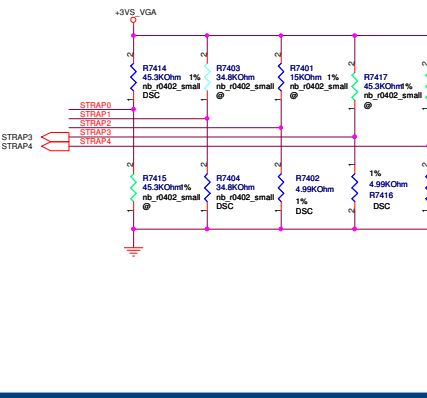
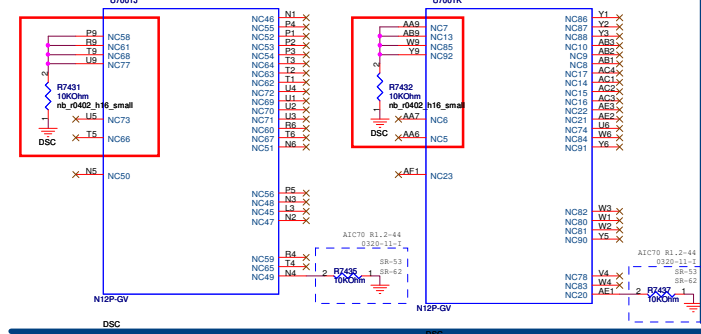


refer to P0M-05374-001

70.72.91 +3VS_VGA

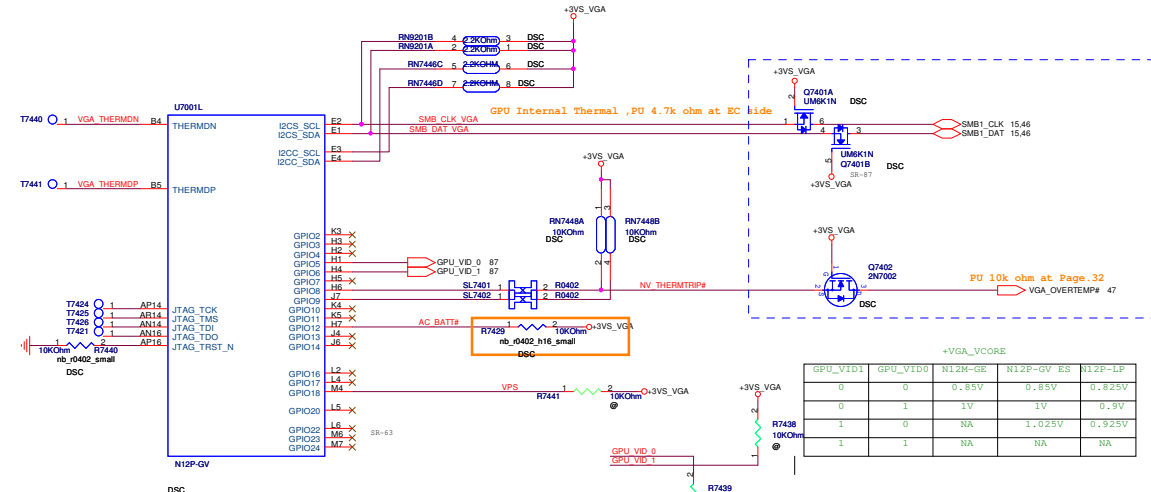
Muti I/O unused

P9,R8,W9,T9 Compatible with G81-128



				N12P-LP QS	N12P-GV ES	N12M-GE QS
	PU	PD	PU	PD	PU	PD
ROM_SO	R7427	R7419	@	10K	@	10K
ROM_SCLK	R7410	R7411	@	15K	@	15K
ROM_SI	R7422	R7420	@	H 64:15K S 64:20K	@	H 64:15K S 64:20K
Strap2	R7401	R7402	25K	@	45K	@
Strap1	R7403	R7404	@	35K	@	35K
Strap0	R7414	R7415	45K	@	45K	@
Strap3	R7417	R7416	@	@	20k	@
Strap4	R7421	R7418	@	@	10k	@

GPIO, THERM, SMBUS, JTAG, LVDS MISC, GPU_VID



GPU_VID1	GPU_VID0	N12M-GE	N12P-GV ES	N12P-LP
0	0	0.85V	0.85V	0.825V
0	1	1V	1V	0.9V
1	0	NA	1.025V	0.925V
1	1	NA	NA	NA

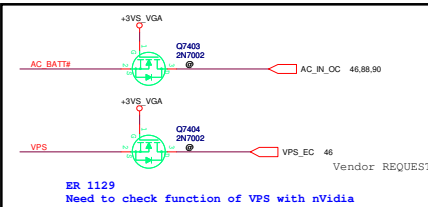
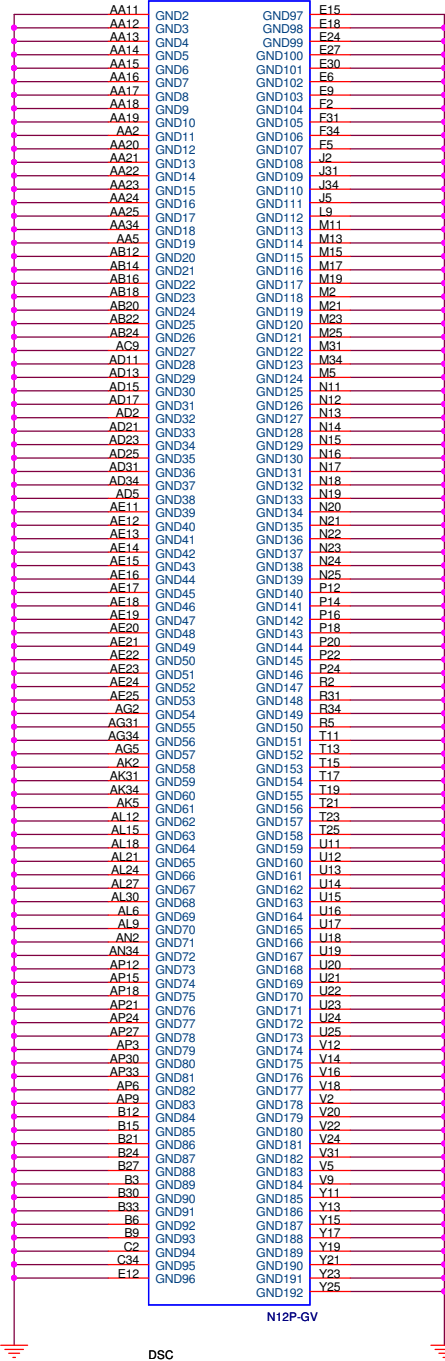


Table 12.1 GPIO Description

GPIO PIN Name	Normal Function	I/O	Functional Description
GPIO0	General Purpose		
GPIO1	HPD_C	I	Hot Plug Detect for IFPC
GPIO2	LCD0_BL_PWM	O	Panel Backlight Brightness Control (PWM capable)
GPIO3	LCD0_VCC	O	Panel Power/Enable
GPIO4	LCD0_BLEN	O	Panel Backlight ON/OFF Control (PWM capable)
GPIO5	GPU_VID0	O	GPU Core VDD VID0
GPIO6	GPU_VID1	O	GPU Core VDD VID1
GPIO7	GPU_VID2	O	GPU Core VDD VID2
GPIO8	OVERT	I/O	Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	SLI_RASTER_SYNC	I/O	SLI Raster Sync
GPIO12	PWR_LEVEL	I	AC Power Detect Input
GPIO13	THERM_LOAD_STEP_DOWN	O	Power Supply Control
GPIO14	THERM_LOAD_STEP_UP	O	Power Supply Control
GPIO15	HPD_E	I	Hot Plug Detect for IFPE
GPIO16	FAN_PWM	O	Programmable Fan Control
GPIO17	Reserved		
GPIO18	Reserved		
GPIO19	HPD_D	I	Hot Plug Detect for IFPD
GPIO20	Reserved		
GPIO21	HPD_F	I	Hot Plug Detect for IFPF
GPIO22	SWAPRDY	I	SLI Swap Ready Signal
GPIO23	3D Vision	O	3D Vision functions
GPIO24	General Purpose		

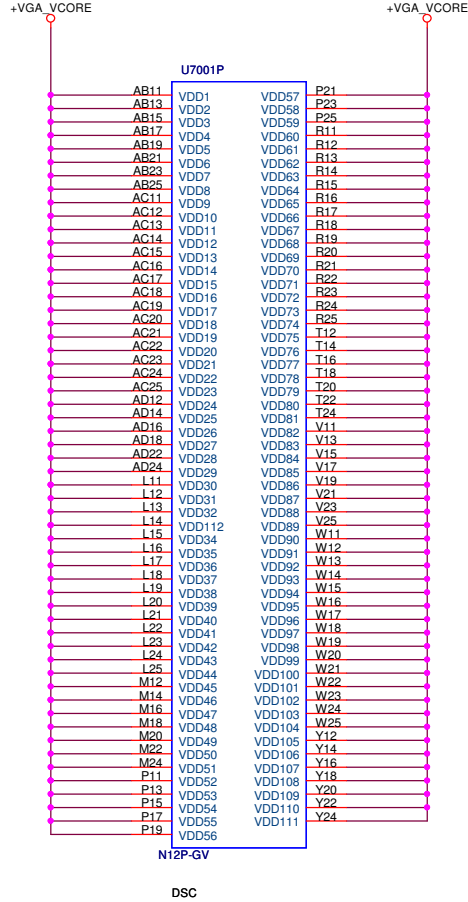
GND

U7001O

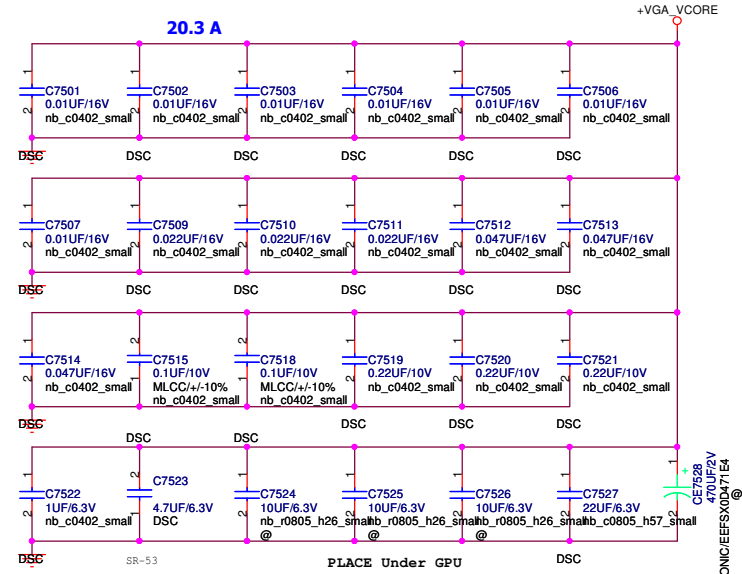


VAG_VCORE

U7001P



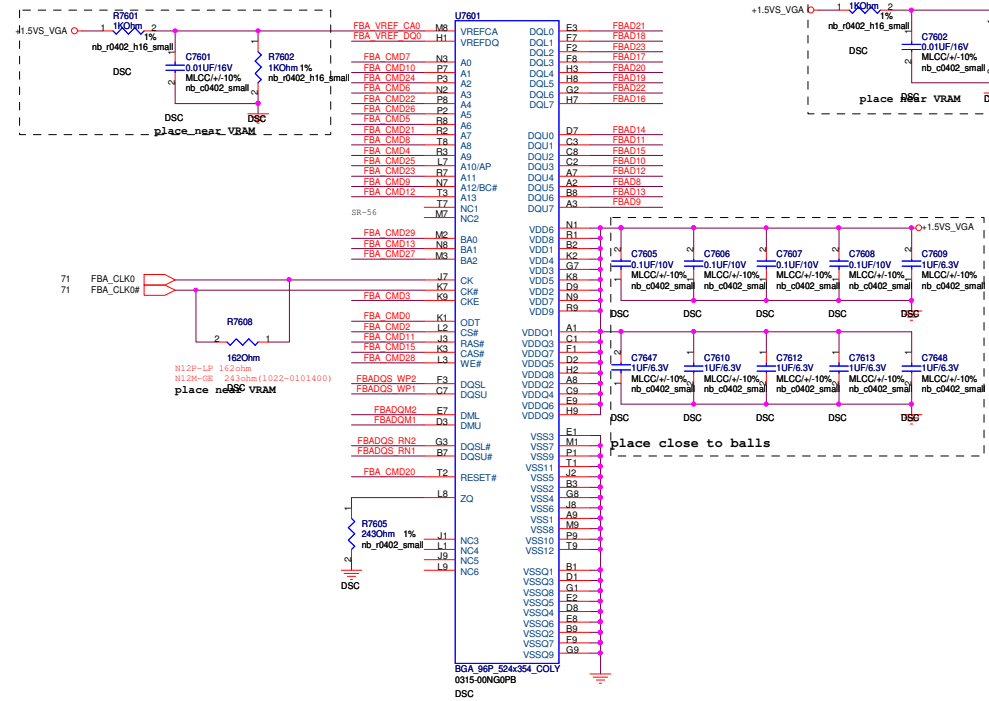
20.3 A



63.87 +VGA_VCORE

VRAM CH A

TOP SIDE



BOT SIDE

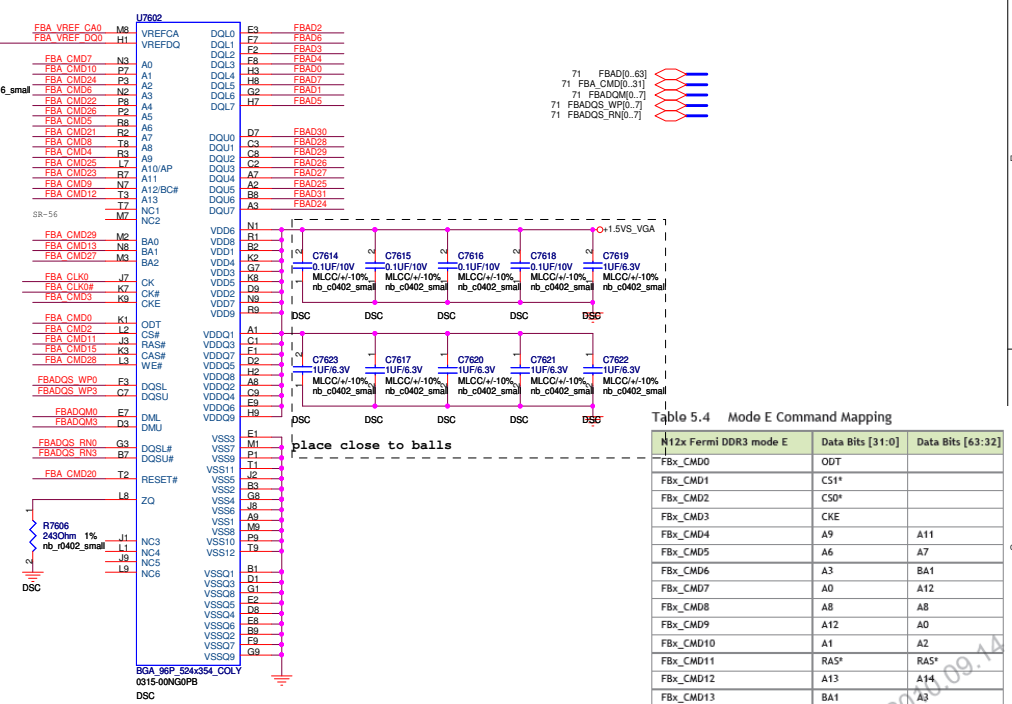
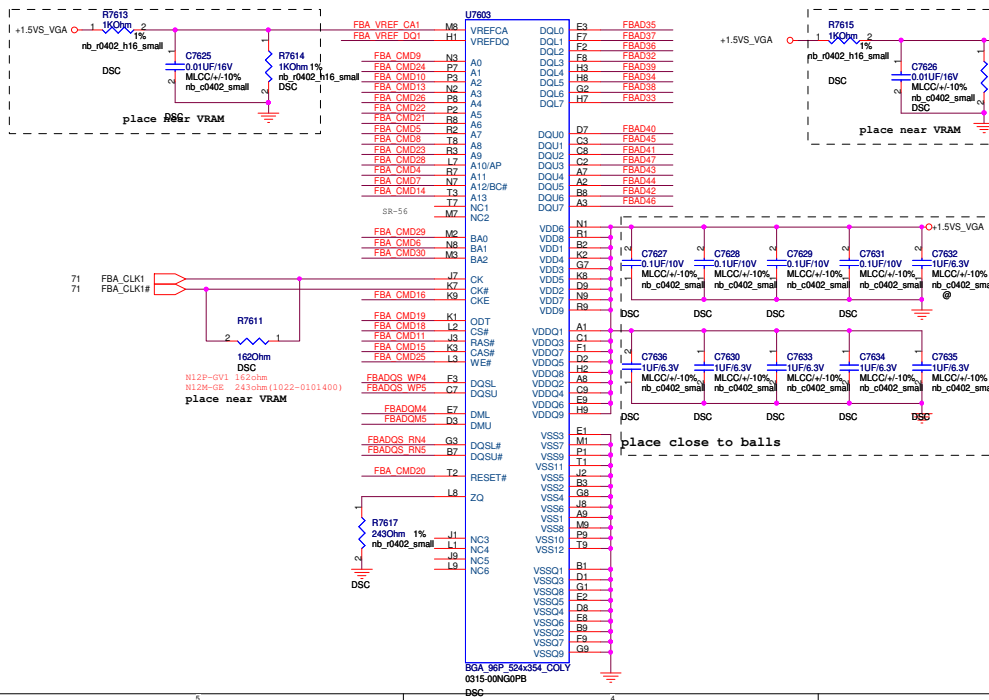


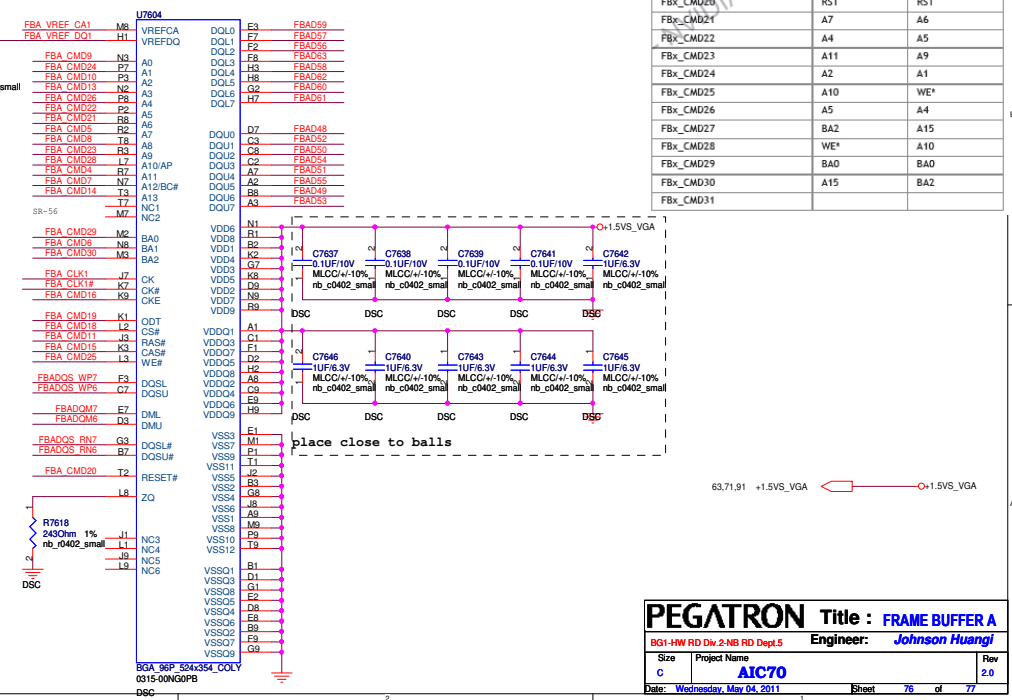
Table 5.4 Mode E Command Mapping

12x8 Fermi DDR3 mode E	Data Bits [31:0]	Data Bits [63:32]
FbxC_CMD0	ODT	
FbxC_CMD1	C51*	
FbxC_CMD2	C50*	
FbxC_CMD3	CKE	
FbxC_CMD4	A9	A11
FbxC_CMD5	A6	A7
FbxC_CMD6	A3	BA1
FbxC_CMD7	A0	A12
FbxC_CMD8	A8	A8
FbxC_CMD9	A12	A0
FbxC_CMD10	A1	A2
FbxC_CMD11	RAS*	RAS*
FbxC_CMD12	A13	A14
FbxC_CMD13	BA1	A3
FbxC_CMD14	A14	A13
FbxC_CMD15	CAS*	CAS*
FbxC_CMD16	CKE	
FbxC_CMD17	C51*	
FbxC_CMD18	C50*	
FbxC_CMD19	ODT	
FbxC_CMD20	RST	RST
FbxC_CMD21	A7	A6
FbxC_CMD22	A4	A5
FbxC_CMD23	A11	A9
FbxC_CMD24	A2	A1
FbxC_CMD25	A10	WE*
FbxC_CMD26	A5	A4
FbxC_CMD27	BA2	A15
FbxC_CMD28	WE*	A10
FbxC_CMD29	BA0	BA0
FbxC_CMD30	A15	BA2
FbxC_CMD31		

TOP SIDE

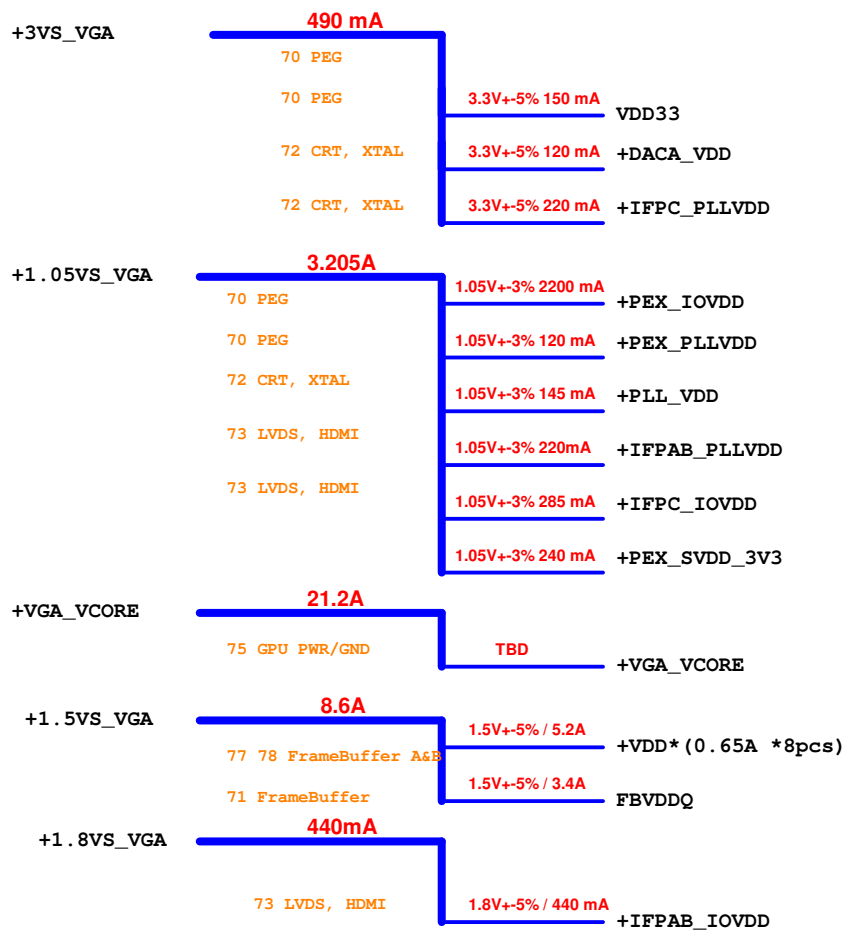


BOT SIDE



Del B channel VRAM * 4 circuit

SR-10
0121-11



N12P-LP Total:40W (w/VRAM)

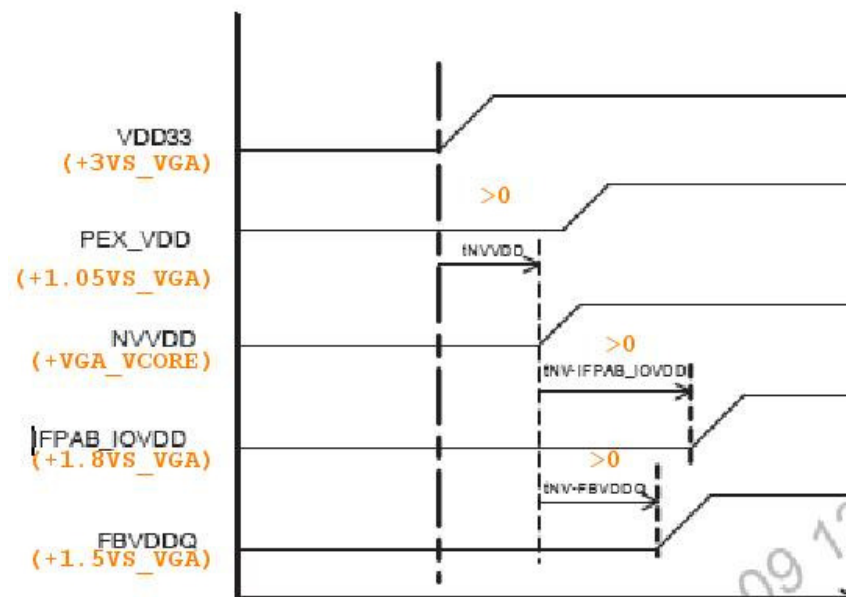
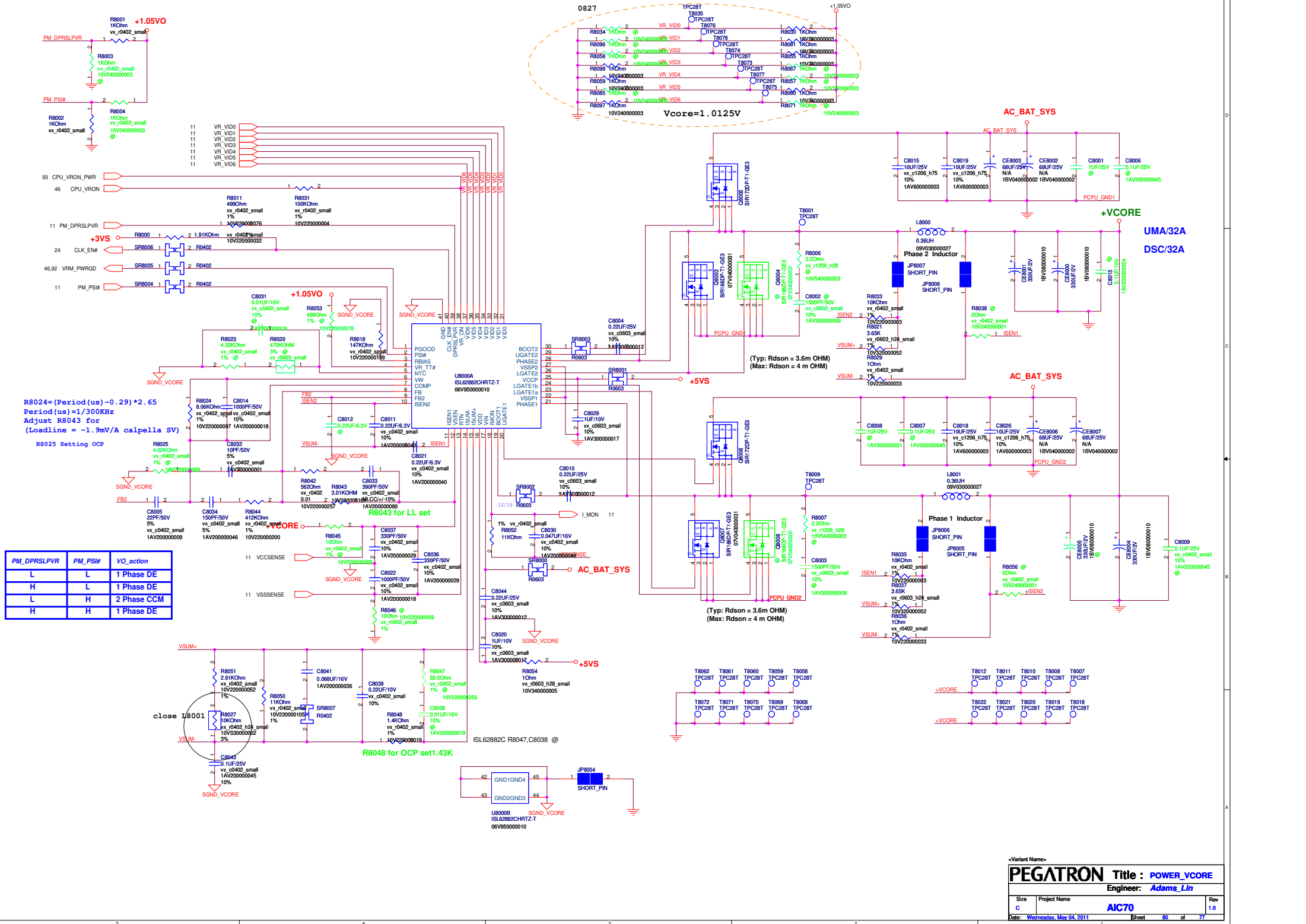


Figure 3.20 Recommended Power On Sequencing Order

Power Up Sequence :
 +3VS_VGA -> +1.05VS_VGA -> +VGA_VCORE -> +1.5VS_VGA -> +1.8VS_VGA

Power Down Sequence :
 +1.8VS_VGA -> +1.5VS_VGA -> +VGA_VCORE -> 1.05VS_VGA -> +3VS_VGA

according to Page 63, DG-05093-001_v02



R8024=(Period(us)-0.29)*2.65
Period(us)=1/300KHz
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

PM_DPRSLPVR	PM_PS#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE



close I8001

VSUM+

VSUM-

SGND_VCORE

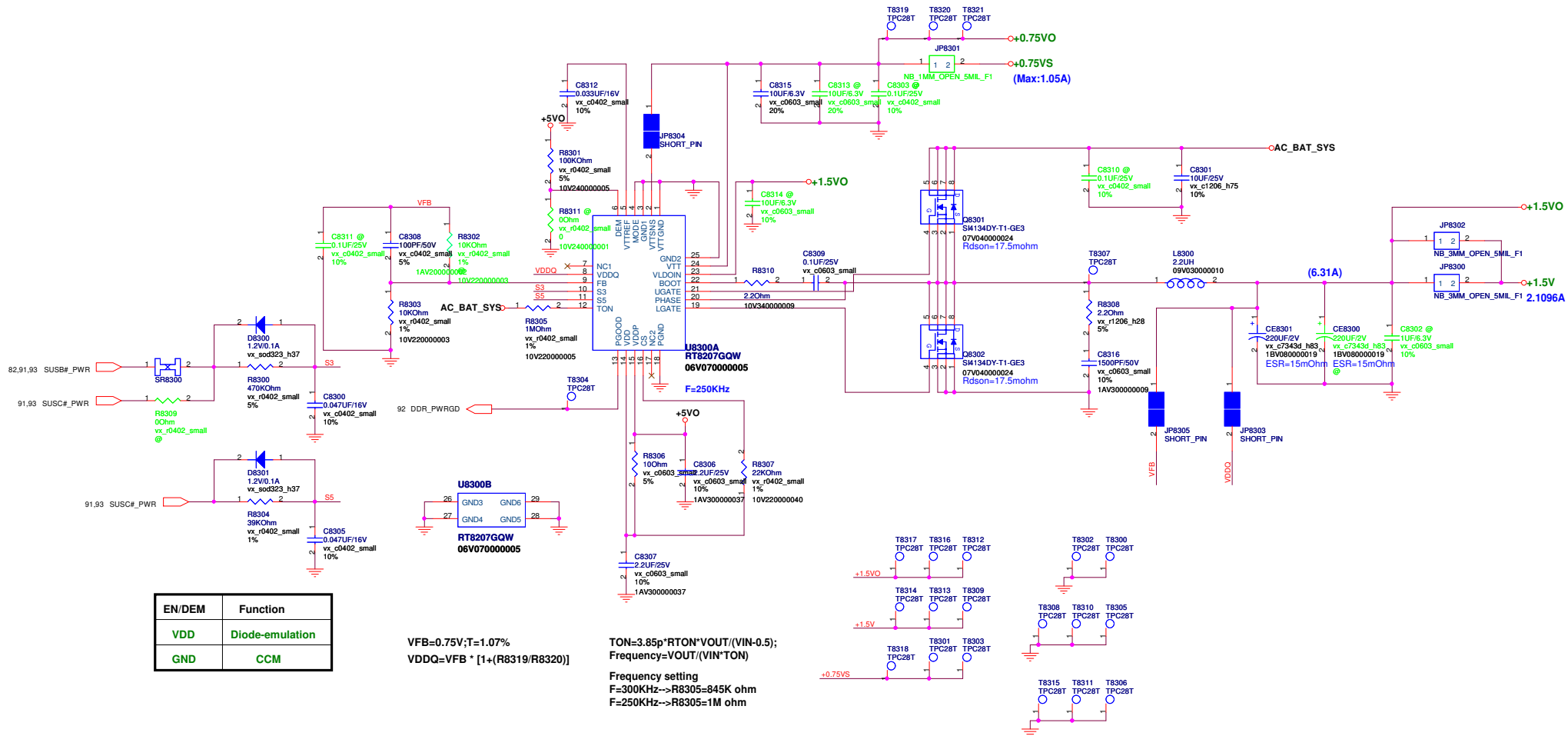
SGND_VCORE

SGND_VCORE

SGND_VCORE

SGND_VCORE

SGND_VCORE



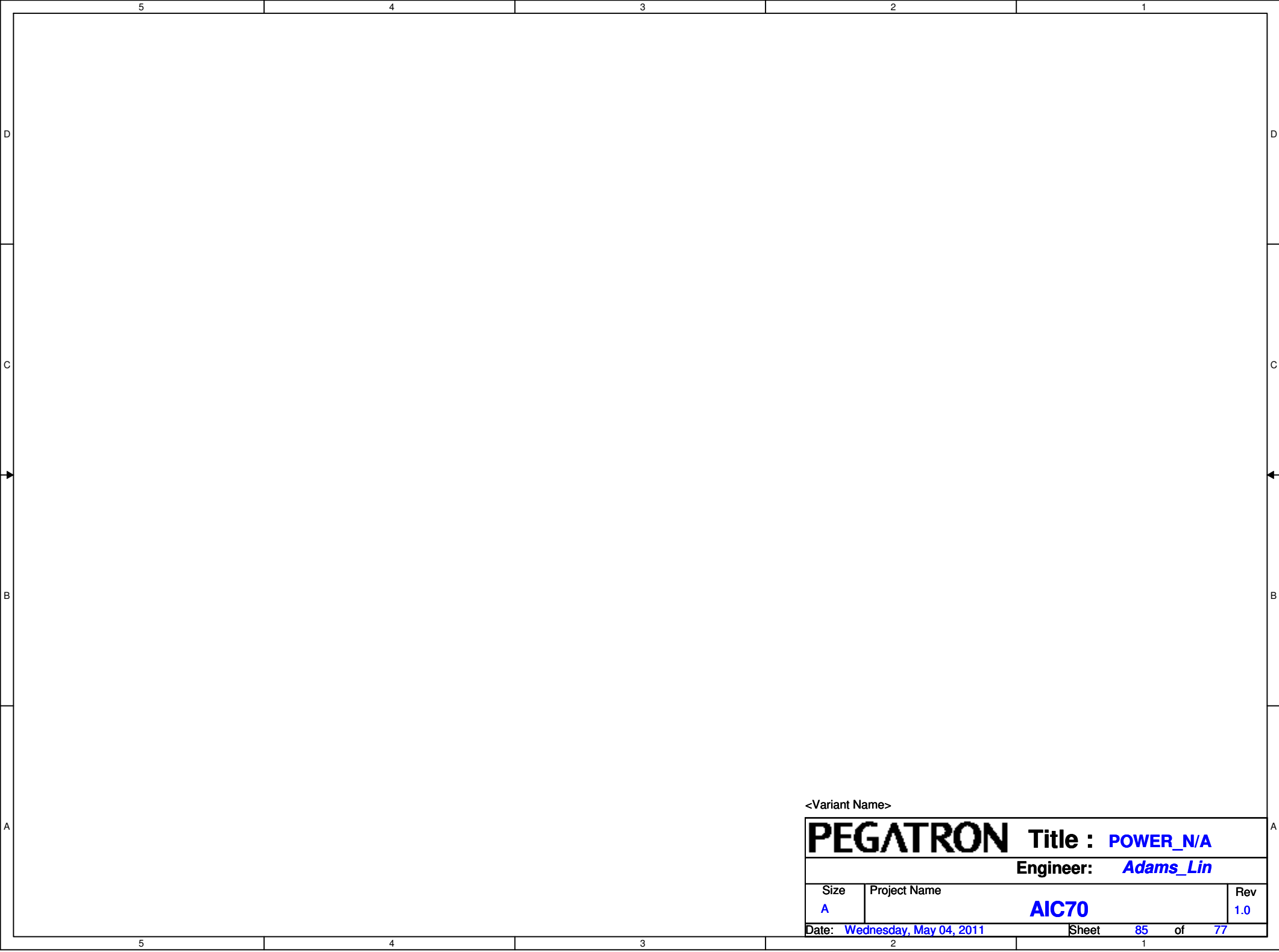
<Variant Name>

PEGATRON Title : **POWER_DDR & VTT**

Engineer: **Adams_Lin**

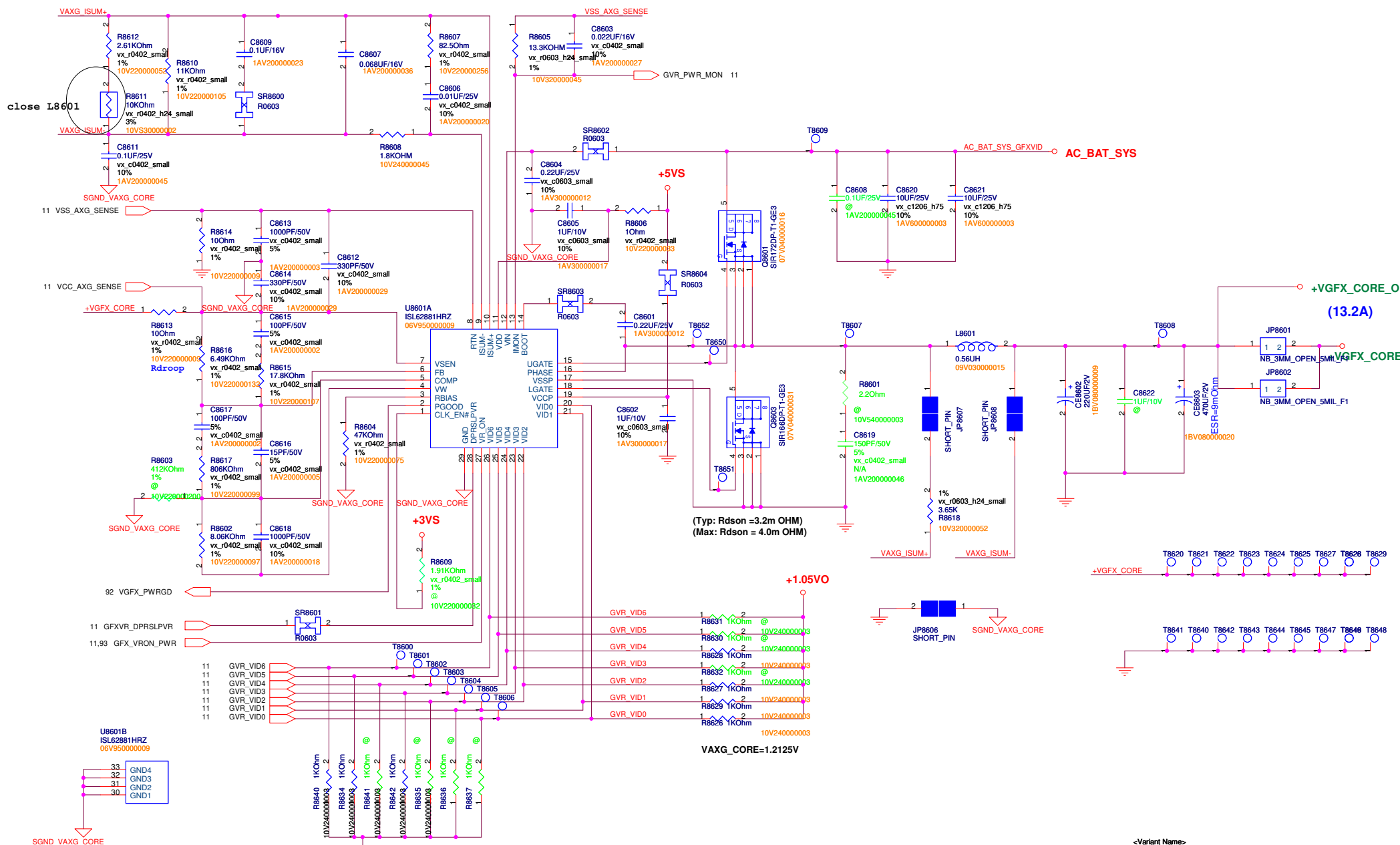
Size	Project Name	Rev
Custom	AIC70	1.0

Date: **Wednesday, May 04, 2011** Sheet **83** of **77**



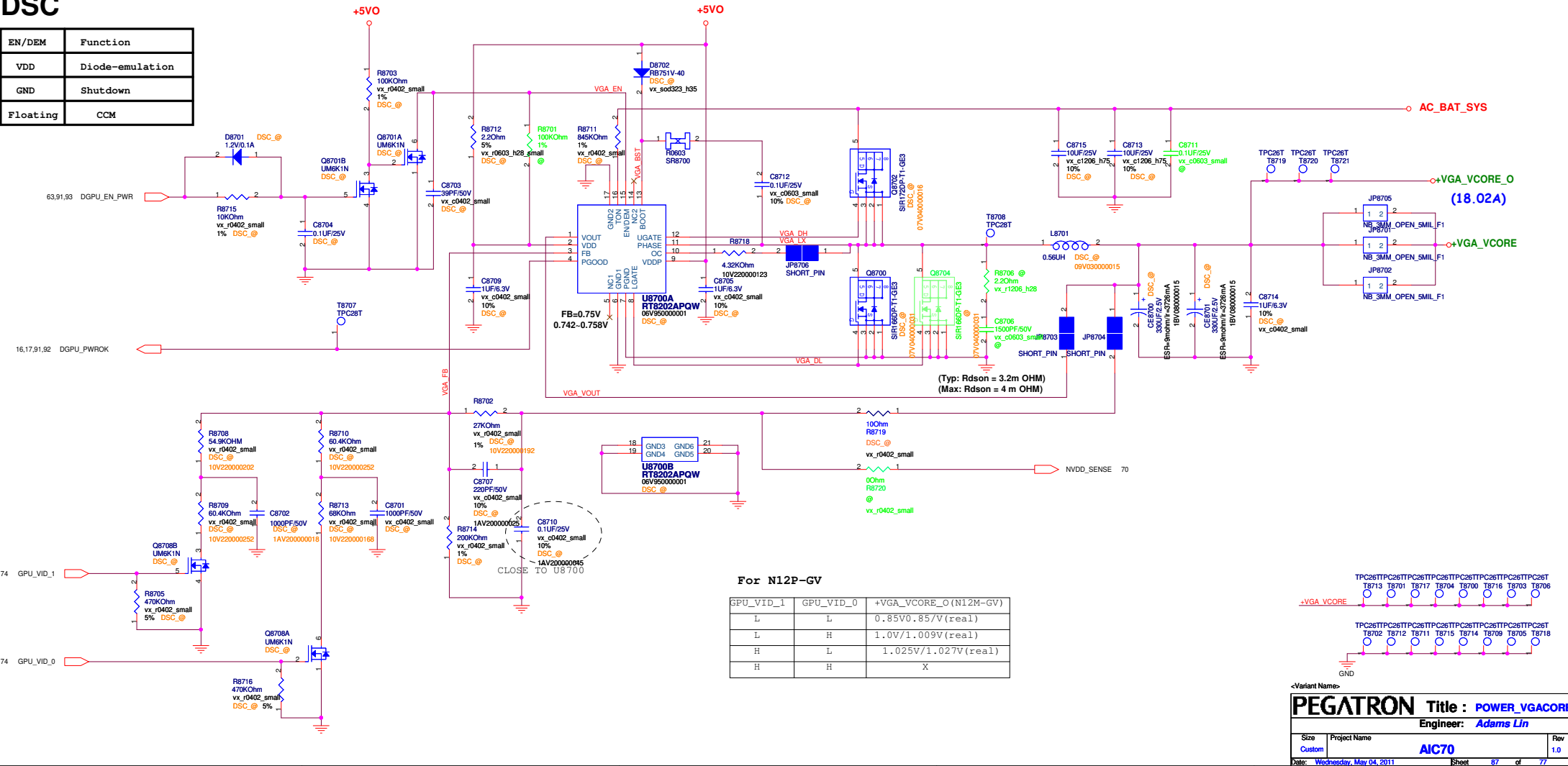
<Variant Name>

PEGATRON		Title : POWER_N/A	
		Engineer: Adams_Lin	
Size A	Project Name AIC70		Rev 1.0
Date: Wednesday, May 04, 2011		Sheet	85 of 77



DSC

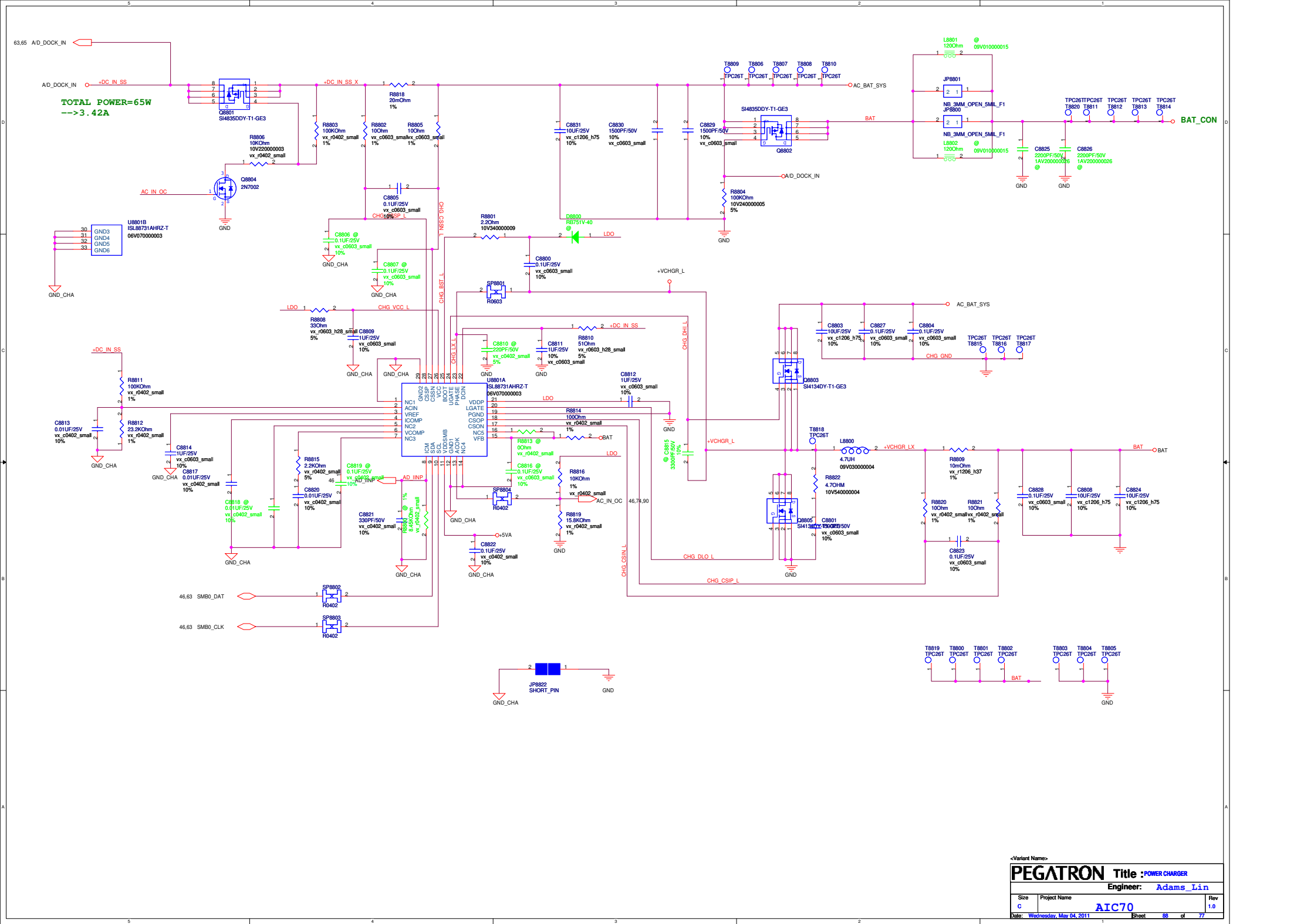
EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



<Variant Name>

PEGATRON Title : POWER_VGACORE	
Engineer: Adams Lin	
Size Custom	Project Name AIC70
Date: Wednesday, May 04, 2011	Rev 1.0

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D

C

B

A

D

C

B

A

5

4

3

2

1

5

4

3

2

1

<Variant Name>

PEGATRON

Title : POWER_N/A

Engineer: *Adams_Lin*

Size
A

Project Name

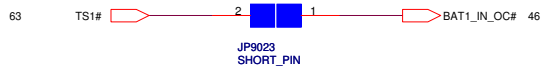
AIC70

Rev	1.0
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Date: Wednesday, May 04, 2011

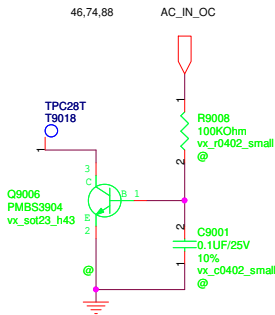
Sheet 89 of 77

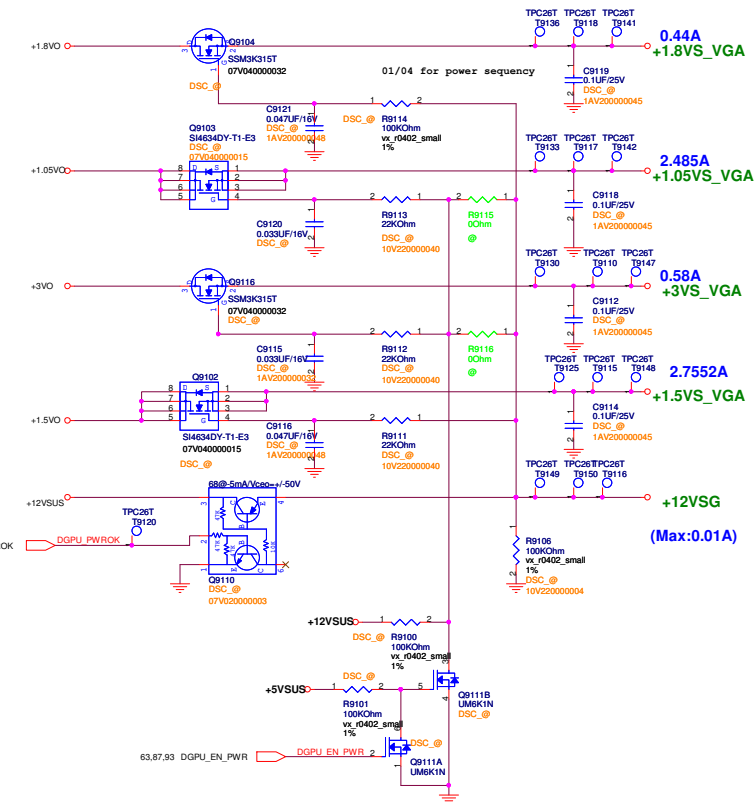
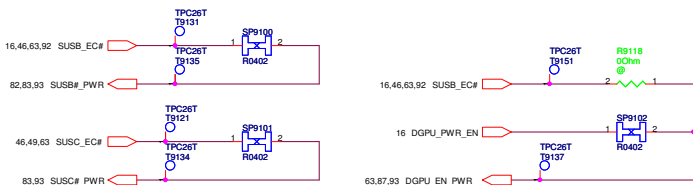
BATTERY IN DETECT



ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component



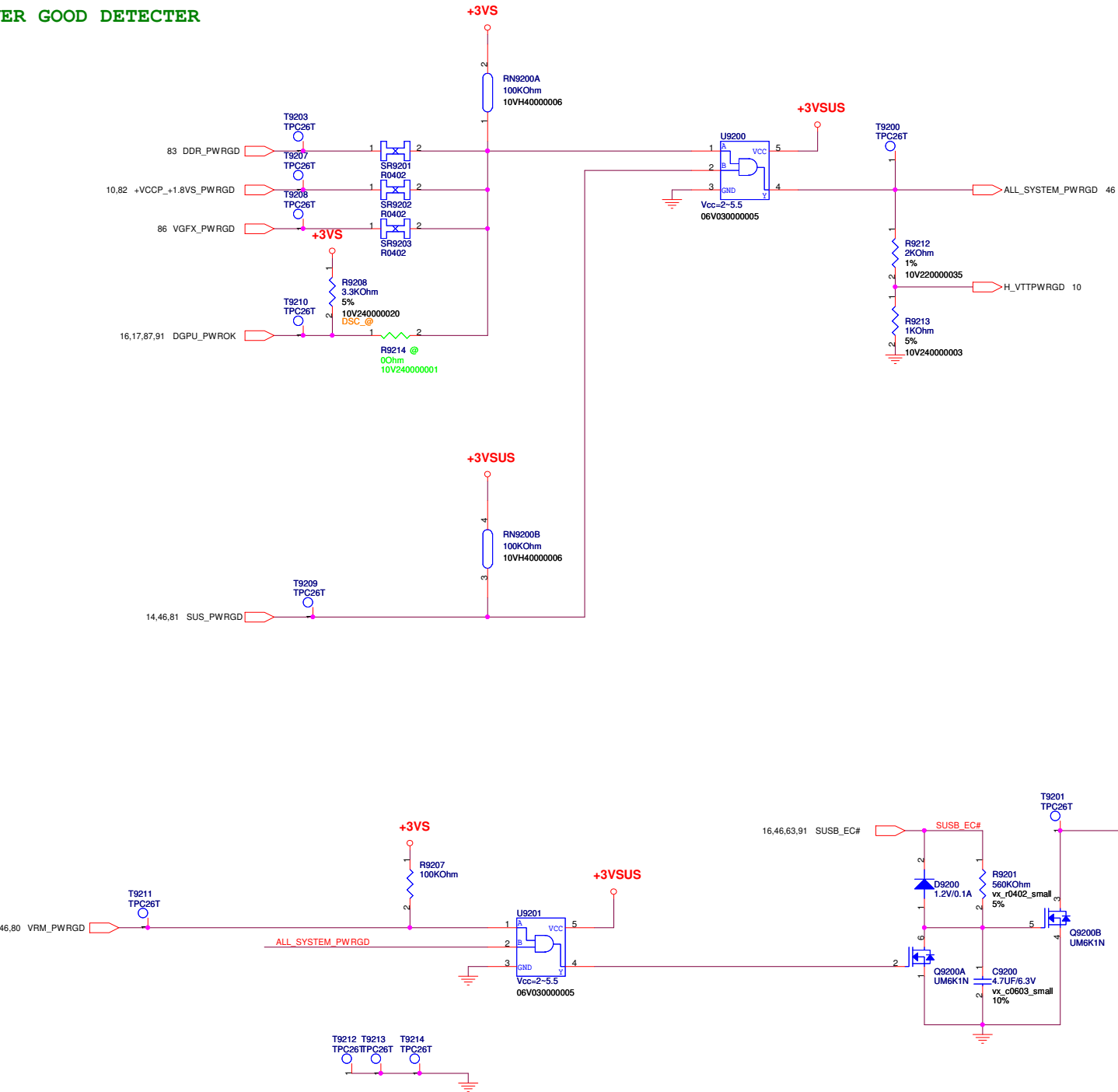


PEGATRON Title :POWER_LOAD SWITCH

Size	Project Name	Rev
Custom	AIC-70	1.0

Date: Wednesday, May 04, 2011 Sheet 91 of 77

POWER GOOD DETECTER



AC_BAT_SYS → AC_BAT_SYS 37,80,81,82,83,86,87,88
BAT_CON → BAT_CON 63,88
BAT → BAT 88

+5VA → +5VA 42,49,66,81,88
+3VA → +3VA 13,18,46,48,63,81

+5VO → +5VO 81,82,83,87,91
+3VO → +3VO 81,91
+1.8VO → +1.8VO 82,91
+1.5VO → +1.5VO 83,91
+1.05VO → +1.05VO 80,82,86,91
+VGFX_CORE_O → +VGFX_CORE_O 86
+VGA_VCORE_O → +VGA_VCORE_O 87
+0.75VO → +0.75VO 83

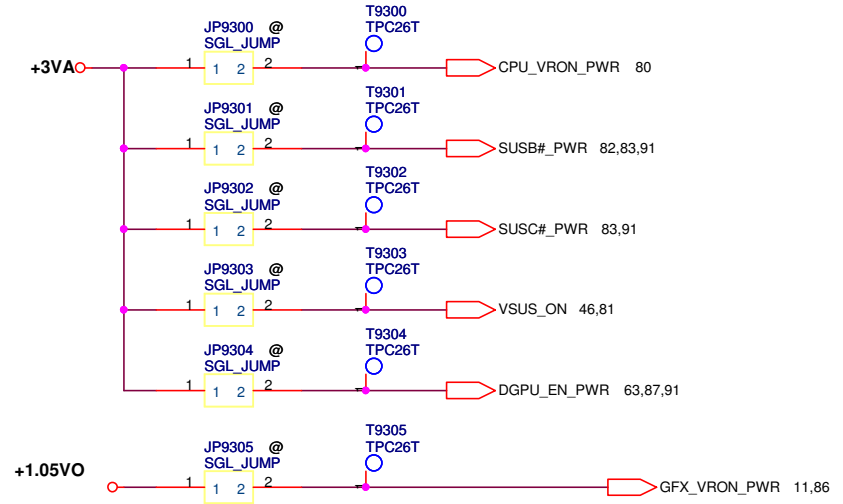
+12VS → +12VS 38,39,91
+5VS → +5VS 15,19,38,39,41,42,46,48,49,60,63,80,86,91
+3VS → +3VS 10,13,14,15,16,17,18,19,21,22,24,33,37,38,39,41,46,47,49,60,63,65,80,86,91,92
+1.8VS → +1.8VS 11,18,19,82
+1.5VS → +1.5VS 10,11,24,55,63,91
+0.75VS → +0.75VS 21,22,63,83

+12VSUS → +12VSUS 60,81,91
+5VSUS → +5VSUS 19,60,61,66,81,91
+3VSUS → +3VSUS 10,13,14,15,16,17,18,19,33,46,55,81,92

+12V → +12V 91
+5V → +5V 42,63,91
+3V → +3V 37,50,63,65,82,91
+1.5V → +1.5V 10,11,21,22,63,83

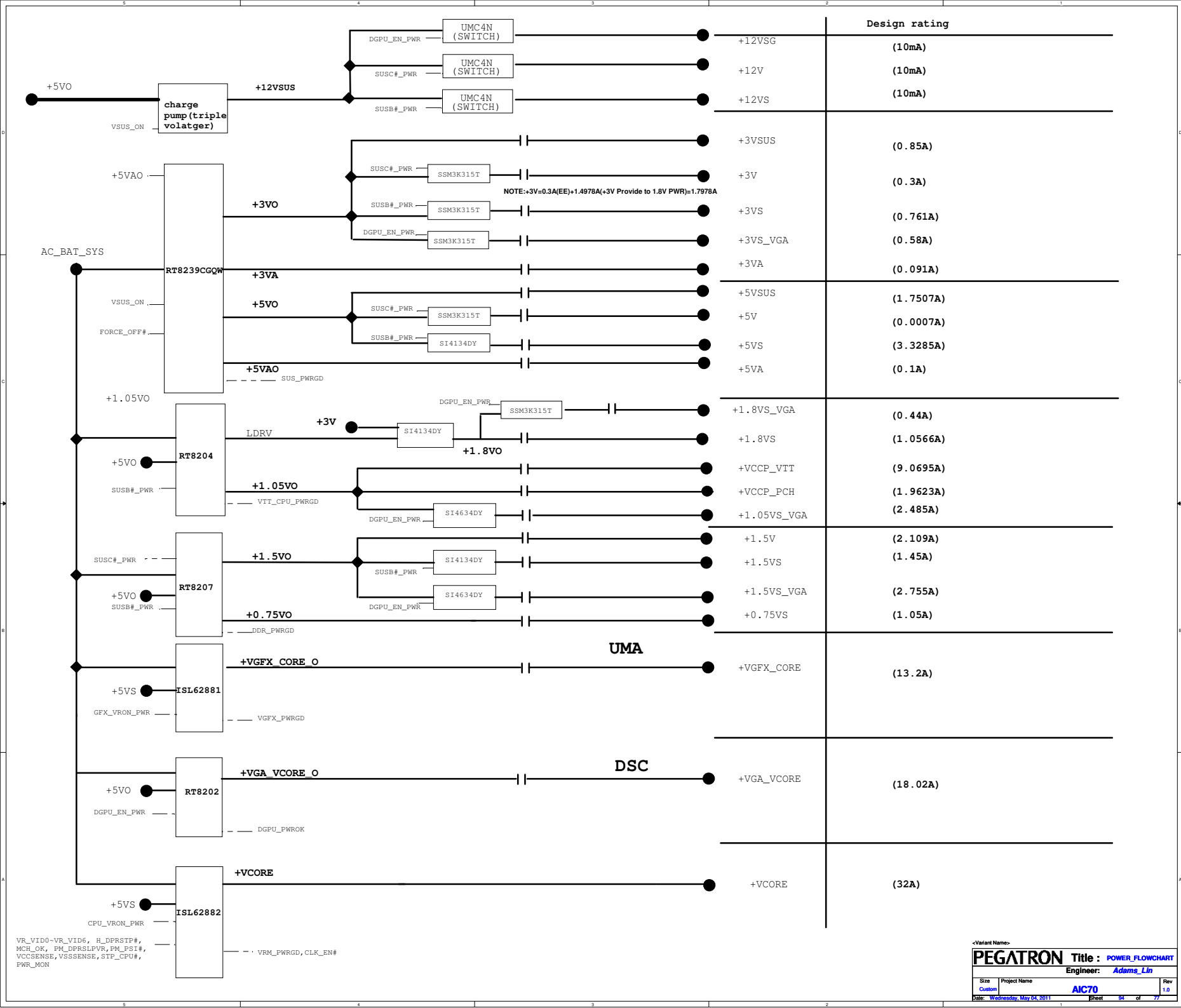
+VGA_VCORE → +VGA_VCORE 63,75,87
+VGFX_CORE → +VGFX_CORE 11,86
+VCORE → +VCORE 11,12,80
+12VSG → +12VSG 91
+3VS_VGA → +3VS_VGA 70,72,74,91
+1.8VS_VGA → +1.8VS_VGA 63,91
+1.5VS_VGA → +1.5VS_VGA 63,71,76,91
+1.05VS_VGA → +1.05VS_VGA 63,70,71,72,91

FOR POWER TEST

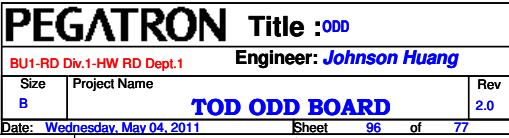


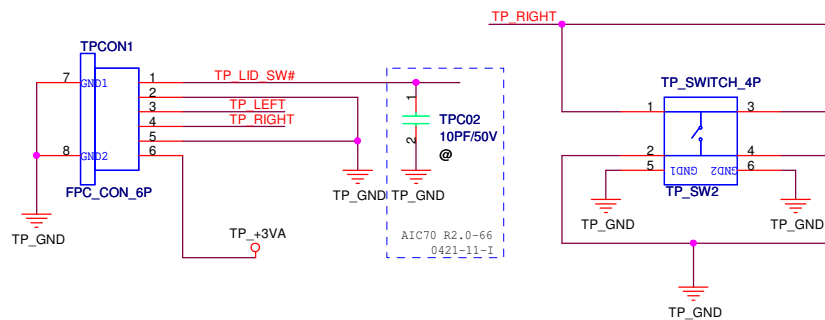
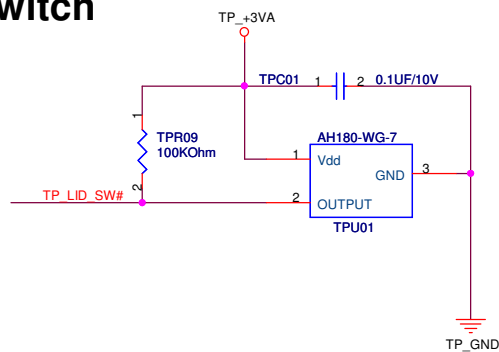
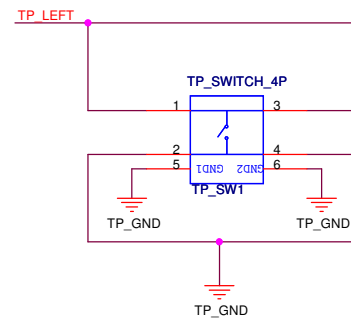
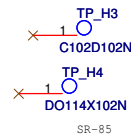
<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Adams_Lin	
Size Custom	Project Name AIC70		Rev 1.0
Date: Wednesday, May 04, 2011		Sheet	93 of 77



Item			Date	Description	Item			Date	Description	Item			Date	Description	Item			Date	Description
SR-1	0120-11	P61, A0410, change USB power switch circuit			SR-71	0128-11	P15, Add C1510 (22pF) for Clock fine-tune			A1C70	R1.1-17	0306-11-1	P99, Add I0C7,I0C7		A1C70	R2.0-41	0415-11-1	P66, Change LED6602 to 0713-01Q0000, LED6603 to 0713-01Q0000, R6605 to 100 ohm, R6604 to 390 ohm	
SR-2	0120-11	Del P67, P68, Add P33, P34 for LAN			SR-72	0128-11	P33, change R3325, R3331 (4.7k ohm)			A1C70	R1.1-18	0306-11-1	P94, Delete C3406		A1C70	R2.0-42	0415-11-1	P49, Change R4903 to 4.32k	
SR-3	0120-11	P48, change KB CON4801			SR-73	0128-11	P39, Un-mount R3907 (HDMI)			A1C70	R1.1-19	0306-11-1	P60, Add SPW002 and use /R0D_CABLE option for HDD cable		A1C70	R2.0-43	0415-11-1	P61, Change U6104 to USB POWER SW, 0547K1P81U; 06V29000008 , nontuff U6105	
SR-4	0120-11	P34, change R345 CON4801			SR-74	0128-11	Change connector by list of 0128-11			A1C70	R1.1-20	0306-11-1	P33, Change R3717 to 10k pull down for disable OC mode and nontuff C3303		A1C70	R2.0-44	0415-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-5	0120-11	P63, change BATT, con, circuit			SR-75	0129-11	Change HDD CON6001(1224-001N000)			A1C70	R1.1-21	0306-11-1	P60, Delete /J7* option		A1C70	R2.0-45	0420-11-1	P33, Change L3303 to 0 ohm	
SR-6	0120-11	P65, A02 change PWR LED CON6503 circuit			SR-76	0129-11	P97 (A02), Change Hotbar 6 Pad (PWR_U01)			A1C70	R1.1-22	0306-11-1	P60, Delete /J7* option		A1C70	R2.0-46	0421-11-1	P98, Reserve TP052	
SR-7	0120-11	P60, change HDD CON6001			SR-77	0129-11	P41-P50 Change VP part			A1C70	R1.1-23	0306-11-1	P17, Add PCB 10 define		A1C70	R2.0-47	0421-11-1	P98, Delete TP_0M3, TP_0M4	
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)			SR-78	0129-11	P55, Add Q5510, R5515 for BT PCI-E wake up event			A1C70	R1.1-24	0306-11-1	P48, Modify TP Bottom optional description		A1C70	R2.0-48	0504-11-1	P49, Change R4903 to 4.02k	
SR-9	0121-11	P50, Del Entry SD socket circuit			SR-79	0130-11	P50, change footprint for U5001 Card reader controller			A1C70	R1.1-25	0307-11-1	P41, Modify speaker optional description and related net name		A1C70	R2.0-49	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-10	0121-11	P77, Del B channel VRAM * 4 circuit			SR-80	0130-11	P66, change CPU74, GPU*2, System screw hole*10			A1C70	R1.1-26	0307-11-1	P1-P99, Midefy schematic optional		A1C70	R2.0-50	0504-11-1	P49, Change R4903 to 4.02k	
SR-11	0121-11	P46, Add EC GPIO35 DGPU_PWR_EN for Power			SR-81	0130-11	P46, change RN4601C (RN9202C)			A1C70	R1.1-28	0307-11-1	P18, Add R3124 for PCB SPT *3VA power		A1C70	R2.0-51	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-12	0121-11	P34, P35, Modify LAN AR8158 (Full)			SR-82	0130-11	P66, change F screw hole *2			A1C70	R1.1-29	0307-11-1	P66, Delete H6538, change H6537,H6633,H6632		A1C70	R2.0-52	0504-11-1	P99, Midefy I0C0603	
SR-13	0123-11	P63, change DC con, as VP part			SR-83	0130-11	P46, change SHORT PIN (R4601, R4602)			A1C70	R1.1-30	0308-11-1	P61, Reserve U6105 for reducing conduction loss		A1C70	R2.0-53	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-14	0123-11	P60, Change HDD CON6001			SR-84	0130-11	P46, P65, change EC GPIO21 (PWR_AMBER_LED#) for PWR Brd.			A1C70	R1.1-31	0308-11-1	P61, Change I0C0603 to 24 pin (1218-00Q0000)		A1C70	R2.0-54	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-15	0123-11	P7-P37 Change VP part			SR-85	0130-11	Modify Sub board screw hole			A1C70	R1.1-32	0308-11-1	P66, Mirror vertically Q4001		A1C70	R2.0-55	0504-11-1	P99, Midefy I0C0603	
SR-16	0124-11	P41 Del Entry speaker R4117-R4120			SR-86	0130-11	P34, Change RJ45 CON3401 1223-00BT000			A1C70	R1.1-33	0308-11-1	P63, Mirror vertically J6301		A1C70	R2.0-56	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-17	0124-11	P38-P39 Change VP part			SR-87	0131-11	P74, Change Q7401B(Q203B)			A1C70	R1.1-34	0309-11-1	P80-P94, Merge power schematic A1C70_R1.1-01103082200.DSN		A1C70	R2.0-57	0504-11-1	P49, Change R4903 to 4.02k	
SR-18	0124-11	P66 Remove LED circuit			SR-88	0131-11	P96, P99, Del Screw hole ODD_J02, change IOW3			A1C70	R1.1-35	0309-11-1	P98, Add TP022		A1C70	R2.0-58	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-19	0124-11	P48, Reverse KB CON4801			SR-89	0131-11	P97, Change Power Board LKD PWR_LED01			A1C70	R1.1-36	0309-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-59	0504-11-1	P99, Midefy I0C0603	
SR-20	0124-11	P71, Remove GPU Channel B dummy NET			SR-90	0131-11	P60, Change 15" ODD CON6505 as VP			A1C70	R1.1-37	0309-11-1	P74, LAN swap on U7403		A1C70	R2.0-60	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-21	0124-11	P16, P61, Remove USB_3 (HDMI)			SR-91	0131-11	P96-P99, Copy from AAR70 (sub board)			A1C70	R1.1-38	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-61	0504-11-1	P49, Change R4903 to 4.02k	
SR-22	0124-11	P48, Remove TP button circuit								A1C70	R1.1-39	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-62	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-23	0124-11	P13, Remove Entry A2 R1318, R1346, R1347, R1348, R1349								A1C70	R1.1-40	0311-11-1	P37, Change PCL_ID		A1C70	R2.0-63	0504-11-1	P99, Midefy I0C0603	
SR-24	0124-11	P50, Modify CON5002 SD socket circuit								A1C70	R1.1-41	0311-11-1	P93, Stuff C3303		A1C70	R2.0-64	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-25	0124-11	P46, Change KB CON4801 PIN definition								A1C70	R1.1-42	0311-11-1	P98, Add TP022		A1C70	R2.0-65	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-26	0124-11	P16, P61, change USB power switch circuit								A1C70	R1.1-43	0311-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-66	0504-11-1	P99, Midefy I0C0603	
SR-27	0124-11	P41, P46, AL0271-05PWR_PC_ICH_Colay								A1C70	R1.1-44	0311-11-1	P74, LAN swap on U7403		A1C70	R2.0-67	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-28	0124-11	P46, P65, Modify LED circuit and EC GPIO definition								A1C70	R1.1-45	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-68	0504-11-1	P49, Change R4903 to 4.02k	
SR-29	0125-11	P33 Remove LAN LED circuit								A1C70	R1.1-46	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-69	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-30	0125-11	P61 Modify D6101, RN6101, RN6105, RN6106								A1C70	R1.1-47	0311-11-1	P37, Change PCL_ID		A1C70	R2.0-70	0504-11-1	P99, Midefy I0C0603	
SR-31	0125-11	P33 Change R3311 as VP								A1C70	R1.1-48	0311-11-1	P98, Add TP022		A1C70	R2.0-71	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-32	0125-11	P33 Change U3301 to AR8158 and delete SM BUS								A1C70	R1.1-49	0311-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-72	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-33	0125-11	P34 Modify LAN ESD circuit								A1C70	R1.1-50	0311-11-1	P74, LAN swap on U7403		A1C70	R2.0-73	0504-11-1	P99, Midefy I0C0603	
SR-34	0125-11	P61, Modify Q6101								A1C70	R1.1-51	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-74	0504-11-1	P49, Change R4903 to 4.02k	
SR-35	0125-11	P65, Modify Q6501								A1C70	R1.1-52	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-75	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-36	0125-11	P38, P46, Del F3801, C3811 Add CRT IN Detect								A1C70	R1.1-53	0311-11-1	P37, Change PCL_ID		A1C70	R2.0-76	0504-11-1	P99, Midefy I0C0603	
SR-37	0125-11	P63, Reverse J6301								A1C70	R1.1-54	0311-11-1	P93, Stuff C3303		A1C70	R2.0-77	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-38	0125-11	P61, P46, change USB power switch and GPIO								A1C70	R1.1-55	0311-11-1	P98, Add TP022		A1C70	R2.0-78	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-39	0125-11	P46,P66, change LED power and Net name								A1C70	R1.1-56	0311-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-79	0504-11-1	P99, Midefy I0C0603	
SR-40	0125-11	P34, Modify Transformer circuit								A1C70	R1.1-57	0311-11-1	P74, LAN swap on U7403		A1C70	R2.0-80	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-41	0125-11	P33, Modify H/W strap setting								A1C70	R1.1-58	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-81	0504-11-1	P49, Change R4903 to 4.02k	
SR-42	0125-11	P37, Modify LVDS PIN definition								A1C70	R1.1-59	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-82	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-43	0125-11	P42, Modify De-Pop circuit								A1C70	R1.1-60	0311-11-1	P37, Change PCL_ID		A1C70	R2.0-83	0504-11-1	P99, Midefy I0C0603	
SR-44	0125-11	P41, Modify Audio Pin 14, 15, 27-31								A1C70	R1.1-61	0311-11-1	P98, Add TP022		A1C70	R2.0-84	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-45	0126-11	P34, Modify Transformer circuit								A1C70	R1.1-62	0311-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-85	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-46	0126-11	P16, GPIO54 DGPU_PWR_EN								A1C70	R1.1-63	0311-11-1	P74, LAN swap on U7403		A1C70	R2.0-86	0504-11-1	P99, Midefy I0C0603	
SR-47	0126-11	U3101, U7001 Keypart no; U4602, F6302 Modify for BOM								A1C70	R1.1-64	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-87	0504-11-1	P49, Change R4903 to 4.02k	
SR-48	0126-11	P34, Modify Transformer circuit								A1C70	R1.1-65	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-88	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-49	0126-11	P63, P60, P7, P48, Add 15" screw circuit BATT, ODD, Keyboard								A1C70	R1.1-66	0311-11-1	P37, Change PCL_ID		A1C70	R2.0-89	0504-11-1	P99, Midefy I0C0603	
SR-50	0126-11	P13, P60 Rename SATA 0 to SATA 1								A1C70	R1.1-67	0311-11-1	P98, Add TP022		A1C70	R2.0-90	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-51	0126-11	P63, Reverse DC-IN J6301 PIN1 as GND								A1C70	R1.1-68	0311-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-91	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-52	0126-11	P48, Reverse KB CON4801								A1C70	R1.1-69	0311-11-1	P74, LAN swap on U7403		A1C70	R2.0-92	0504-11-1	P99, Midefy I0C0603	
SR-53	0126-11	DGPU Sync with R2H31								A1C70	R1.1-70	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-93	0504-11-1	P49, Change R4903 to 4.02k	
SR-54	0126-11	P.76, T7, M7 Setting								A1C70	R1.1-71	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-94	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-55	0126-11	Modify as OPT display output								A1C70	R1.1-72	0311-11-1	P37, Change PCL_ID		A1C70	R2.0-95	0504-11-1	P99, Midefy I0C0603	
SR-56	0127-11	P.76, Cancel T7, M7 Setting								A1C70	R1.1-73	0311-11-1	P98, Add TP022		A1C70	R2.0-96	0504-11-1	P34, Change U3402 P/N to 0912-0001000 (only change P/N)	
SR-57	0127-11	P.46, P50 Modify single net								A1C70	R1.1-74	0311-11-1	P48, Link C4821 Pin1 to CON4804 pin1		A1C70	R2.0-97	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-58	0127-11	P.42 Change R4205, R4206 = 51 ohm								A1C70	R1.1-75	0311-11-1	P74, LAN swap on U7403		A1C70	R2.0-98	0504-11-1	P99, Midefy I0C0603	
SR-59	0127-11	P.14 R1403, R1404 option N/A								A1C70	R1.1-76	0311-11-1	P50, Add SPW002 for CON5002 pin12 connecting to GND		A1C70	R2.0-99	0504-11-1	P49, Change R4903 to 4.02k	
SR-60	0127-11	P.14 R1403, R1404 option N/A								A1C70	R1.1-77	0311-11-1	P46, Change PCL_ID		A1C70	R2.0-100	0504-11-1	P46, Change H6511, H6512 to OSC optional	
SR-61	0127-11	P.14 R1443, R1444, RN1402, R1424, R1426, R1427, R1428 option N/A/ R1429 option /HDMI_UPD_PCH								A1C70	R1.1-78	0311-11-1	P37, Change PCL_ID</						





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