

ZA1 SYSTEM BLOCK DIAGRAM

PWR_SRC	Primary DC system power supply
---------	--------------------------------

```
3VSUS    3.3V switched power rail ( off in S4-S5 )
```

+3V	3.3V switched power rail (off in S3-S5)
-----	---

3VPCU	3V always on power rail
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```
5VSUS      5V switched power rail ( off in S4-S5 )
```

+5V	5V switched power rail (off in S3-S5)
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```
5VPCU    5V always on power rail
```

VCC_CORE1 3.4V/0.94V switched power rail for CPU core voltage (off in S3 S5)

VCC_VID_1.2V power rail regulator from 2.5VSUS for CPU VID (off in S3-S5

```
VCC_VID 1.2V power rail regulator from 2.5VSDS for CPU VID ( 011
-----
```

```
2.5VSUS 2.5V switched power rail for DDR Memory ( off in S4-S5 )
```

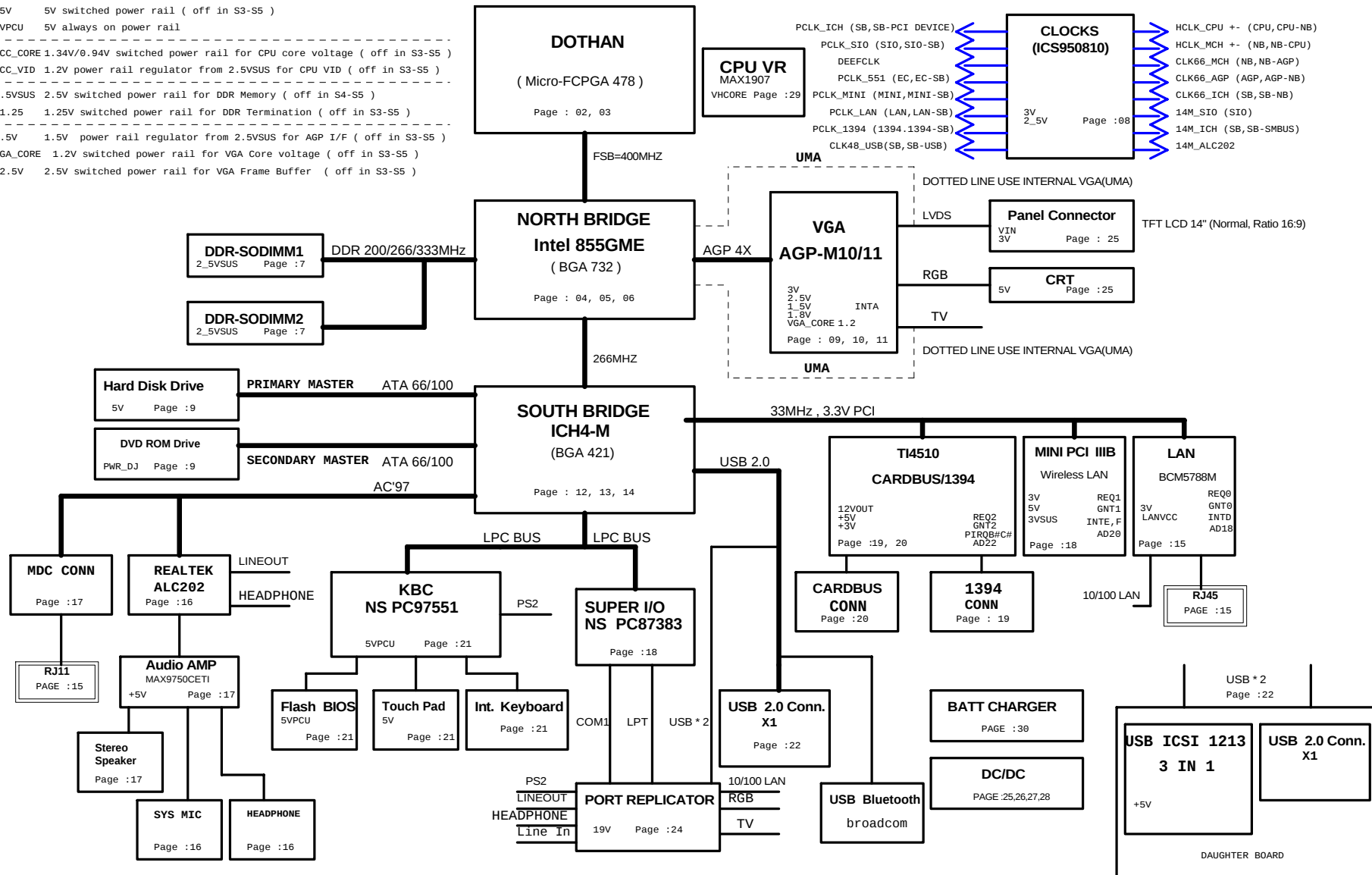
```
+1.25  1.25V switched power rail for DDR Termination ( off in S3-S5 )
```

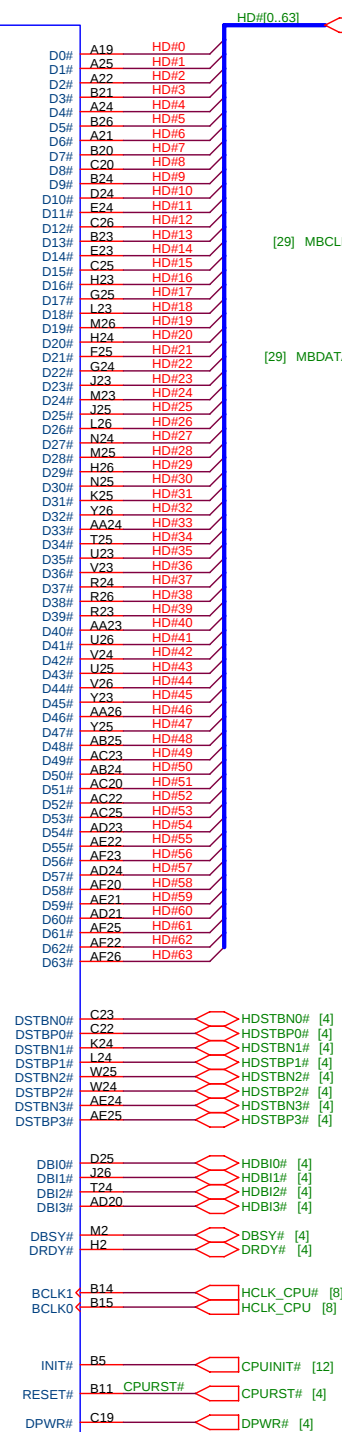
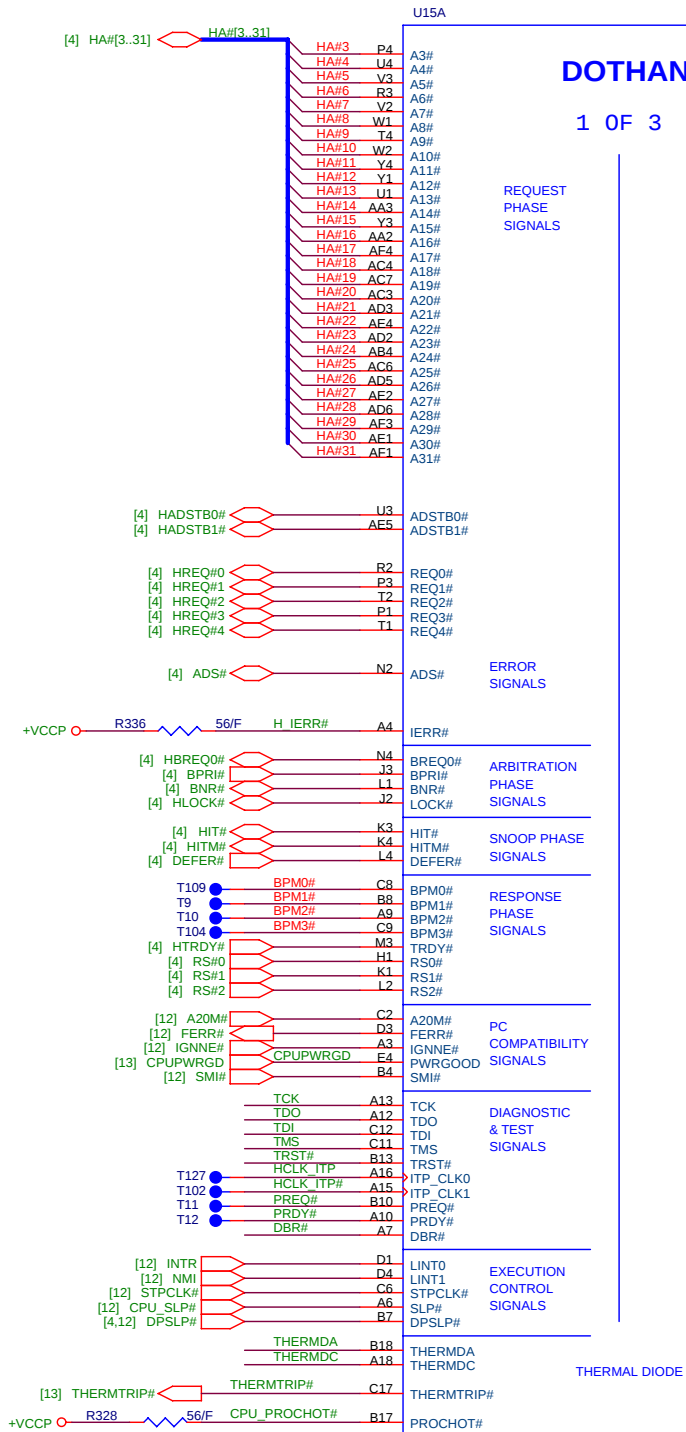
1.5V 1.5V, never rail, regulator from 2.5V/SUS for ACP I/O / off in S2

VGA_CORE 1.2V switched power rail for VGA Core voltage / off in S3 S5

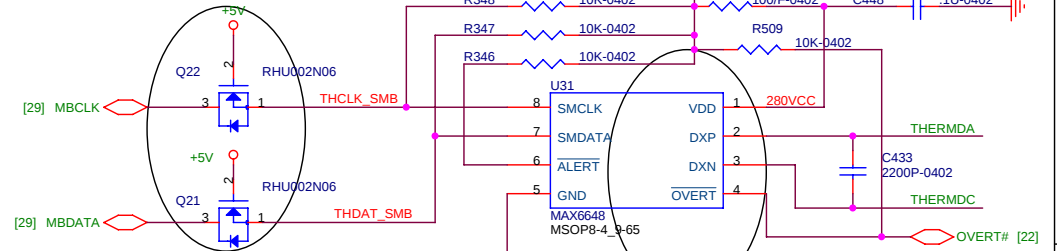
```
VGA_CORE 1.2V Switched power rail for VGA core voltage ( off in S3-S5 )
+3.3V    3.3V switched power rail for VGA Frame Buffer / off in S3-S5
```

+2.5V	2.5V switched power rail for VGA Frame Buffer (off in S3-S5)
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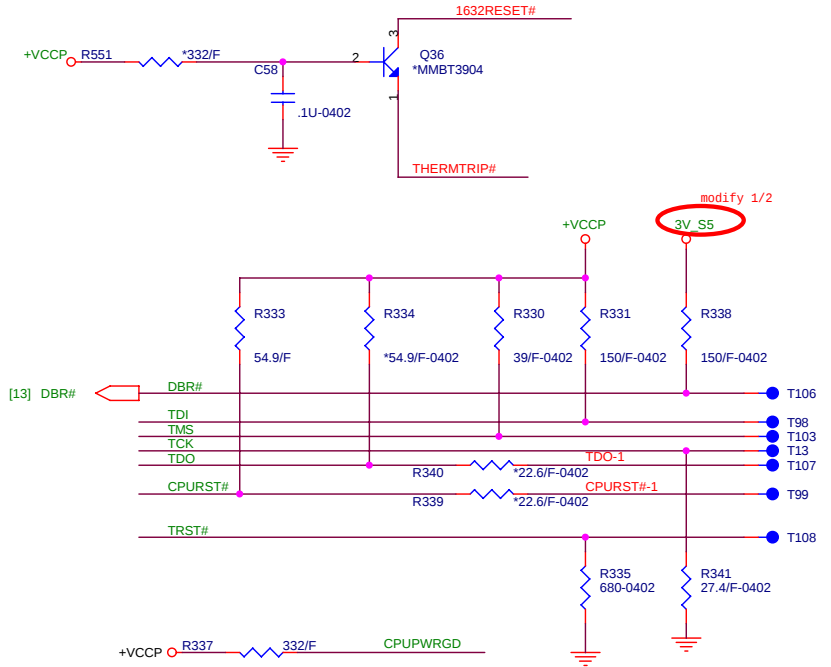


4/10 change 3v to 5v

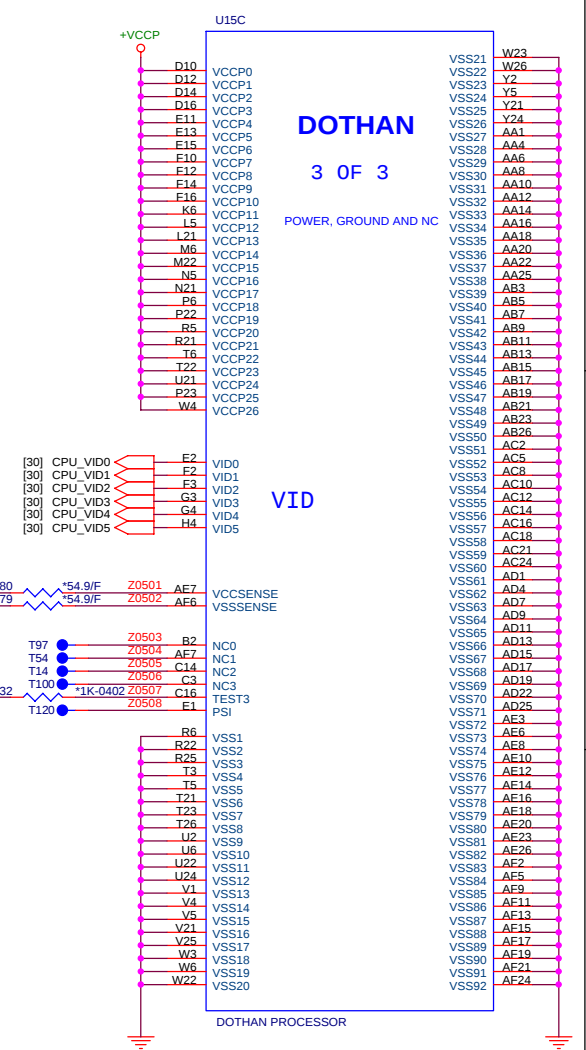
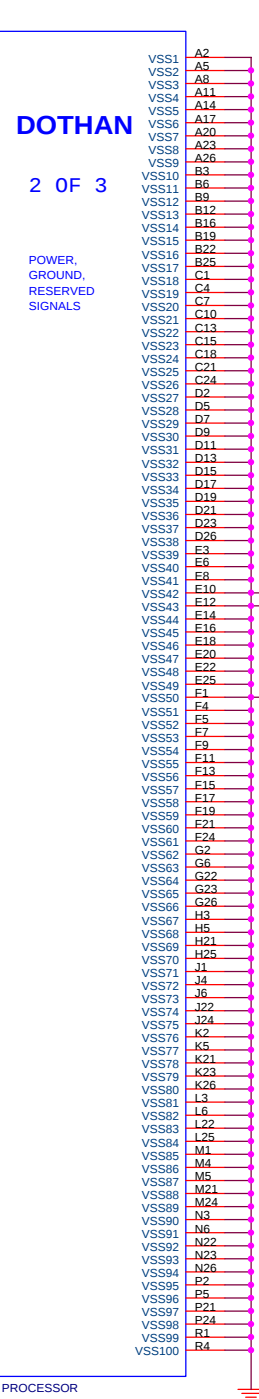
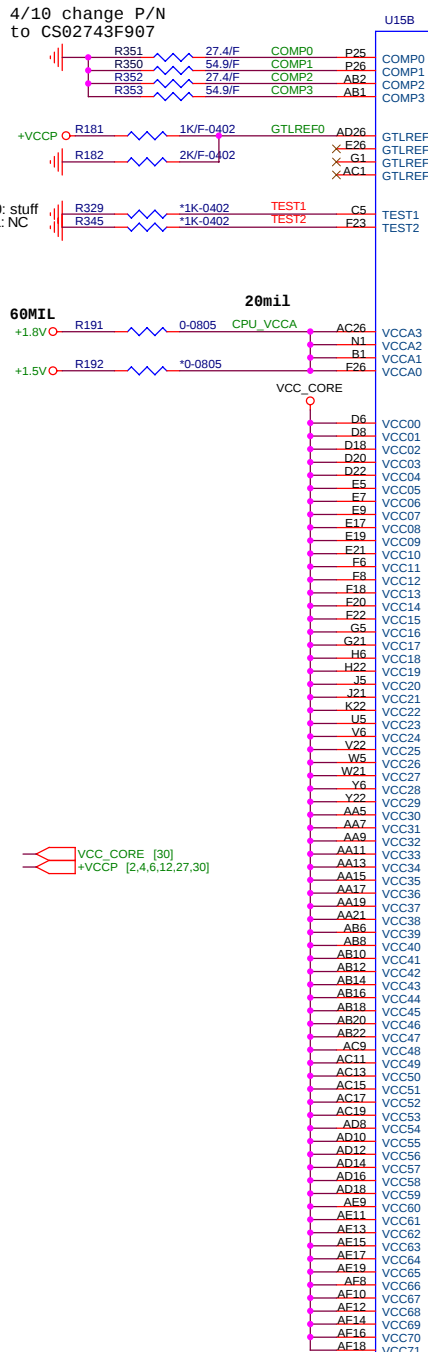
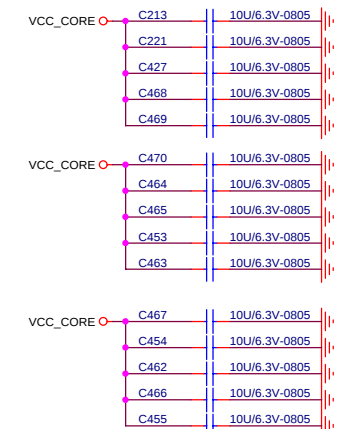
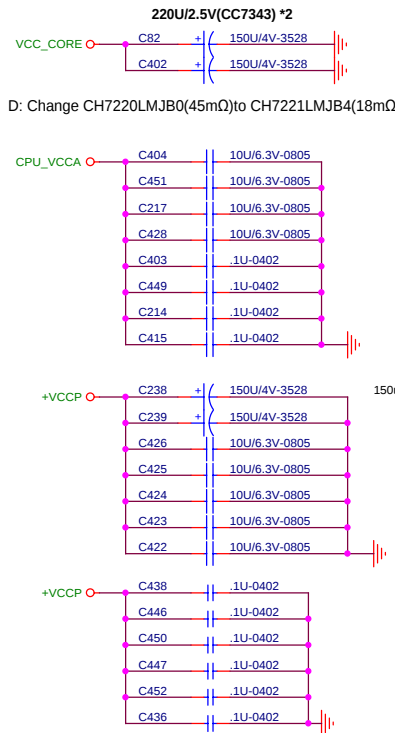


Add for reset function

ok



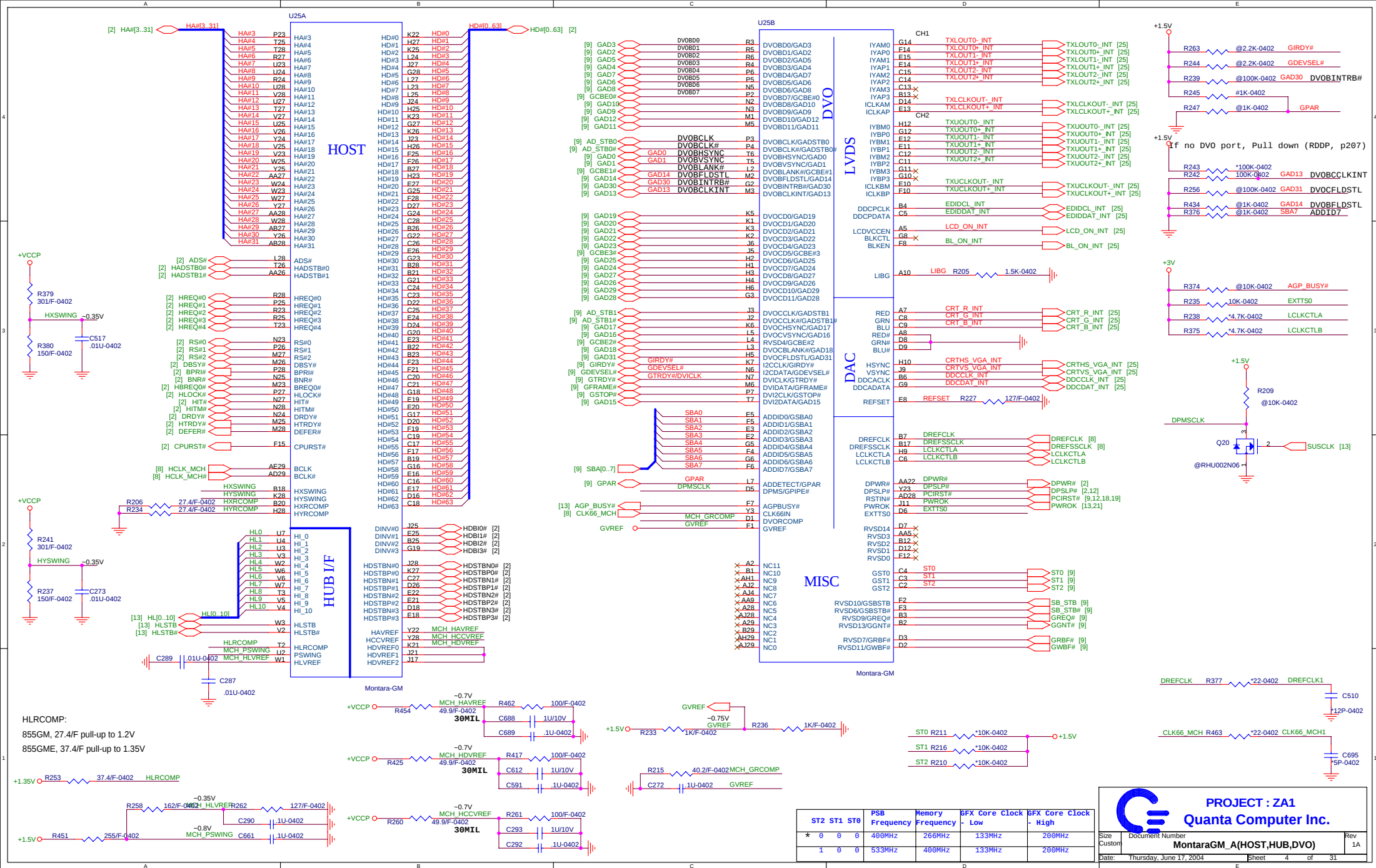
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VCC_CORE: 1.356V-0.844V
, 0.748V(Deeper sleep)

VCCP : 1.05V

VCCA : 1.8V



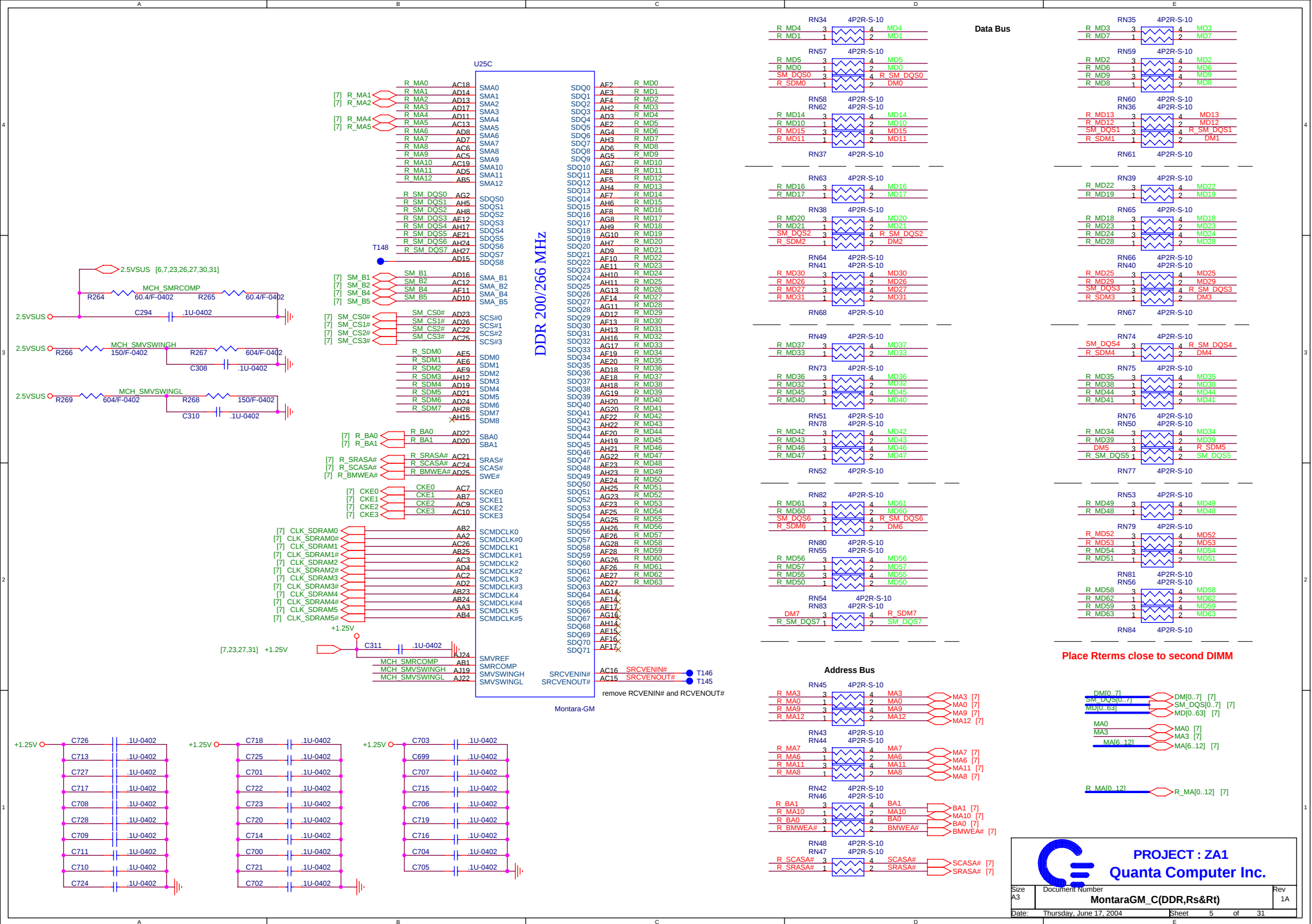
ST2	ST1	ST0	PSB Frequency	Memory Frequency	SFX Core Clock - Low	SFX Core Clock - High
*	0	0	400MHz	266MHz	133MHz	200MHz
1	0	0	533MHz	400MHz	133MHz	200MHz



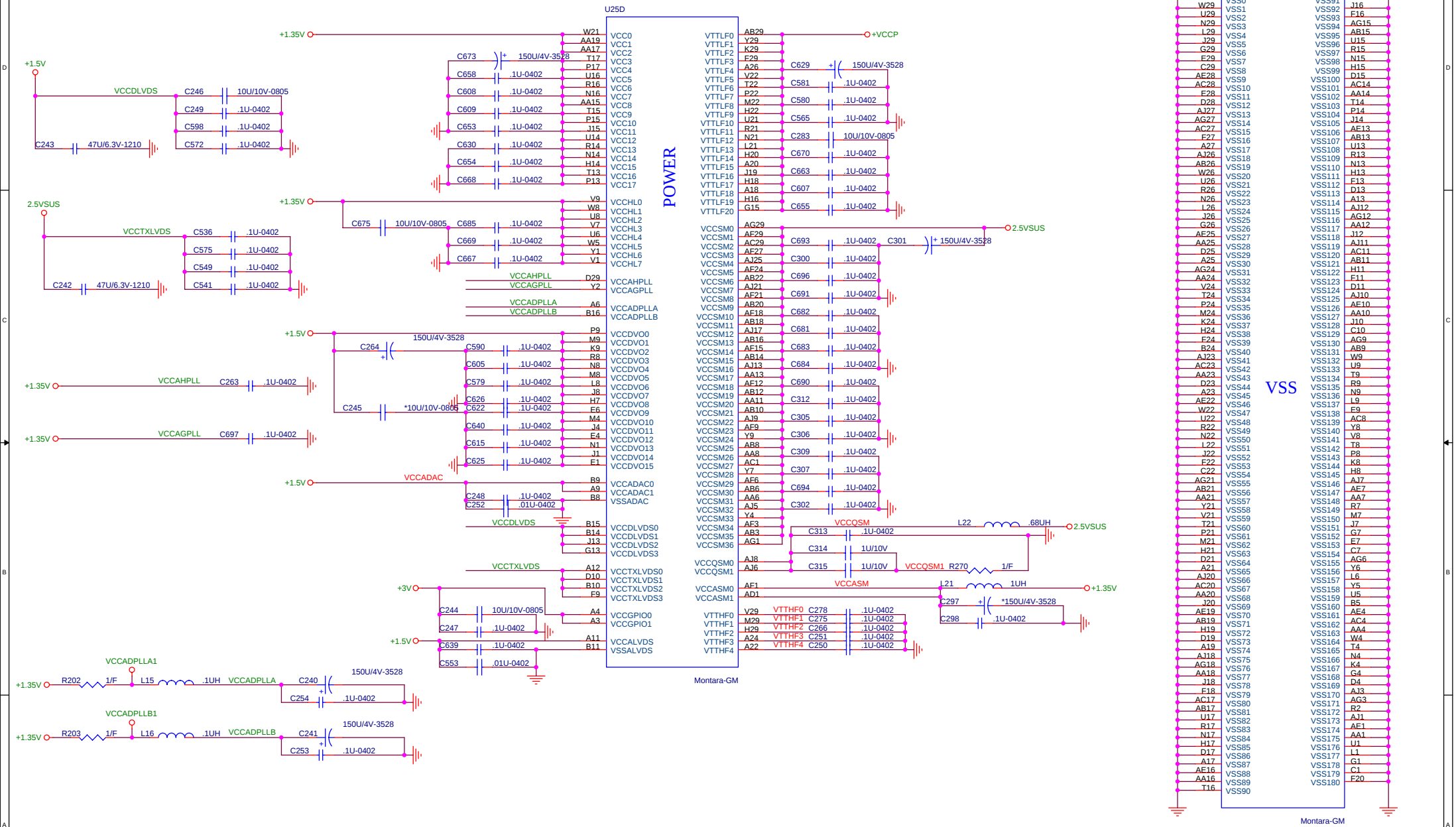
PROJECT : ZA1
Quanta Computer Inc.

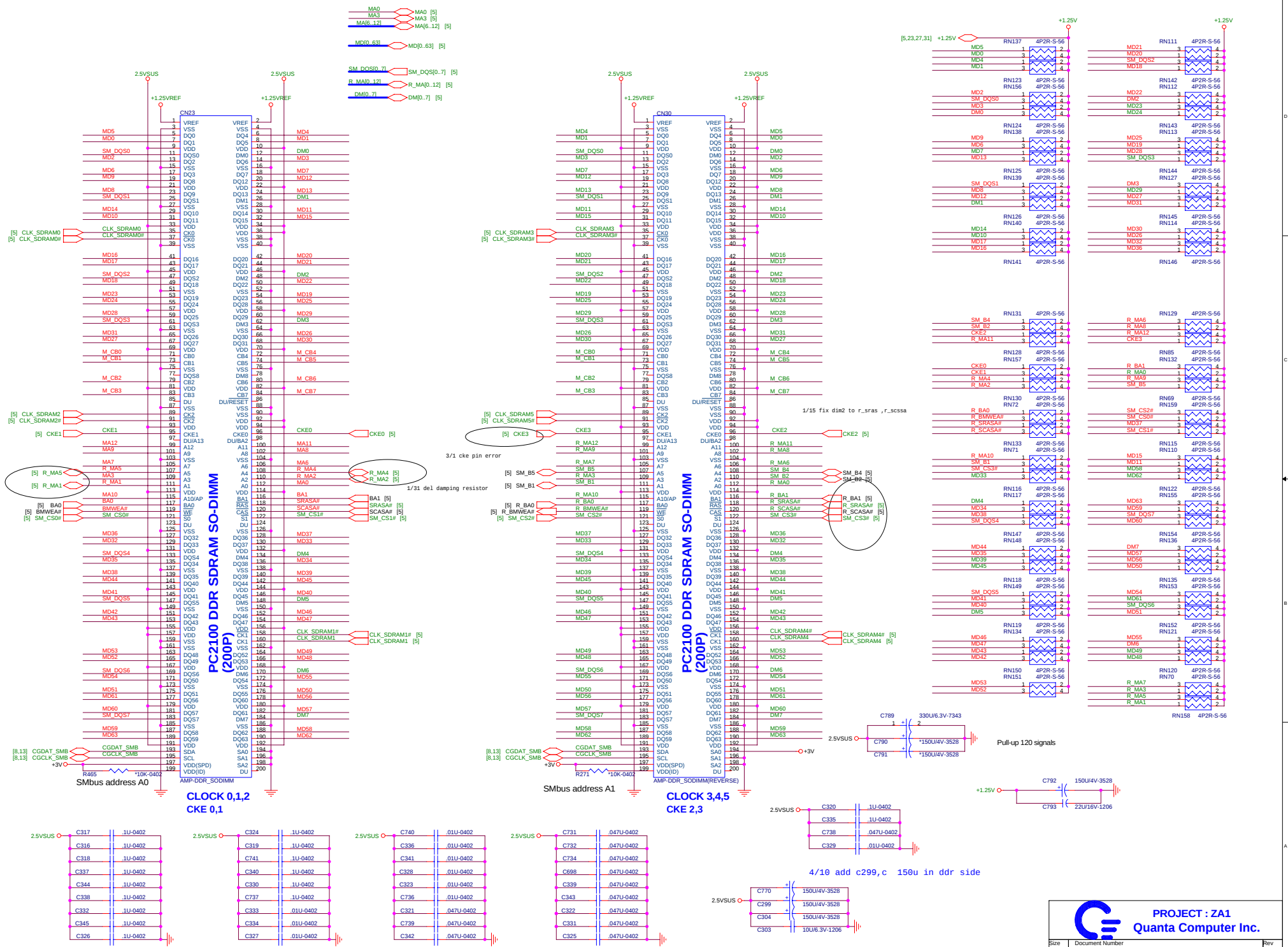
Size Custom Document Number
MontaraGM_A(HOST,HUB,DVO) Rev 1A

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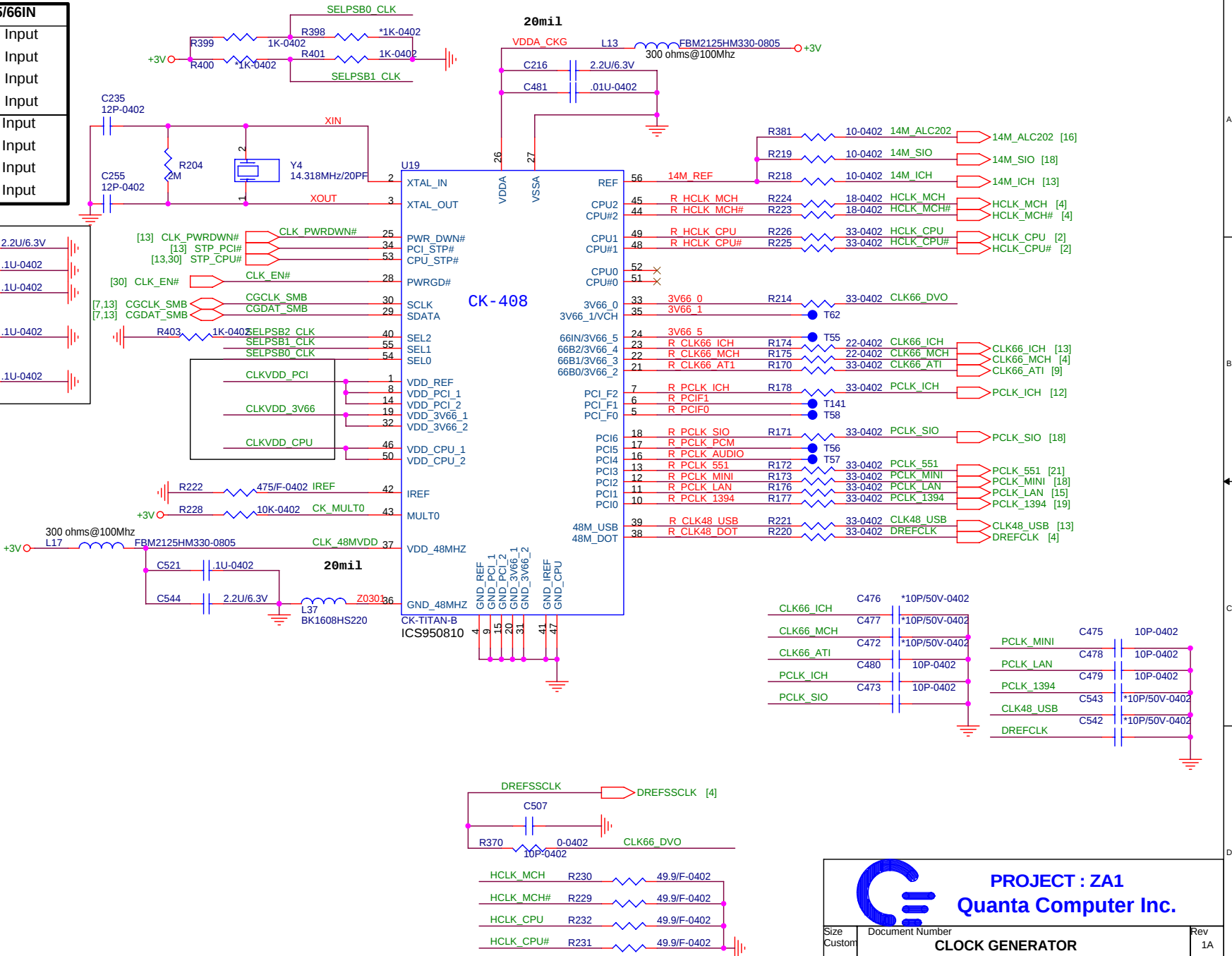
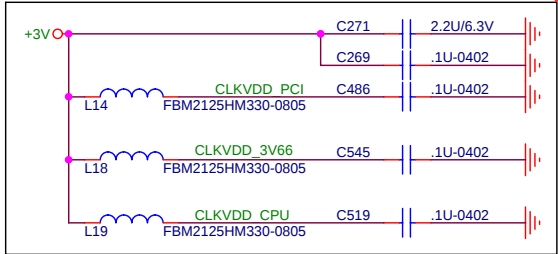


NB: +1.5V 60MIL
NB: +1.35V 60MIL





S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input

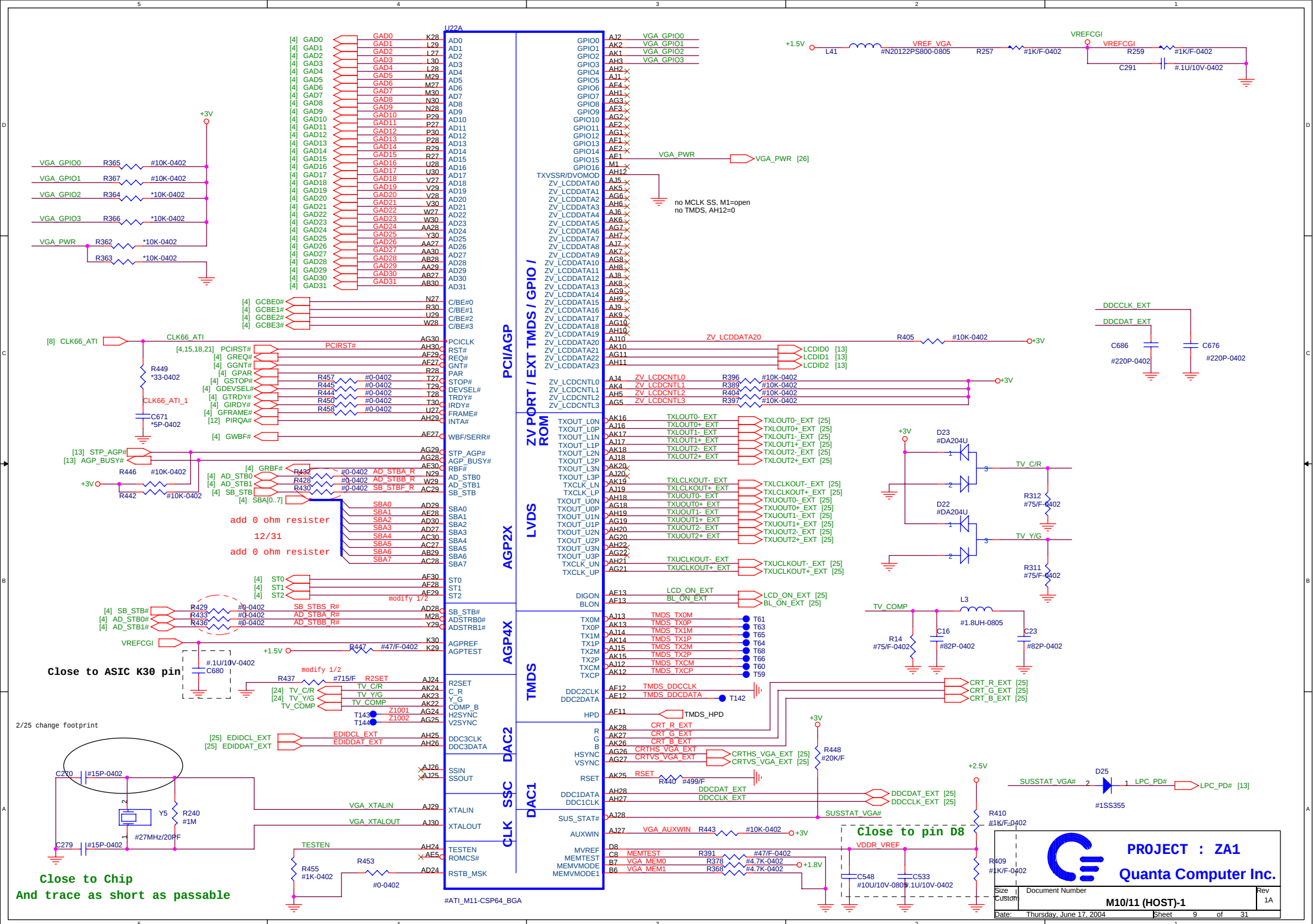


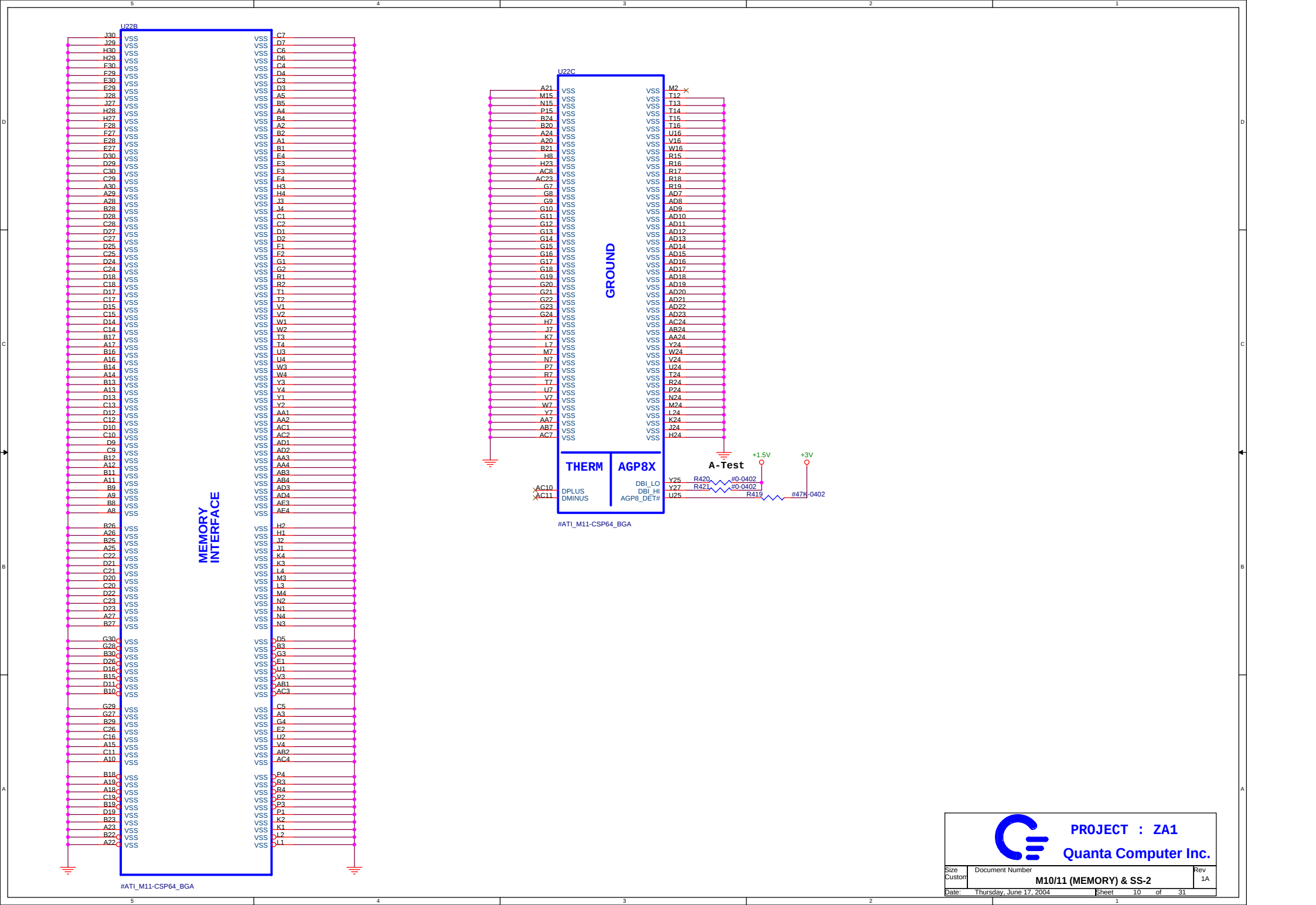


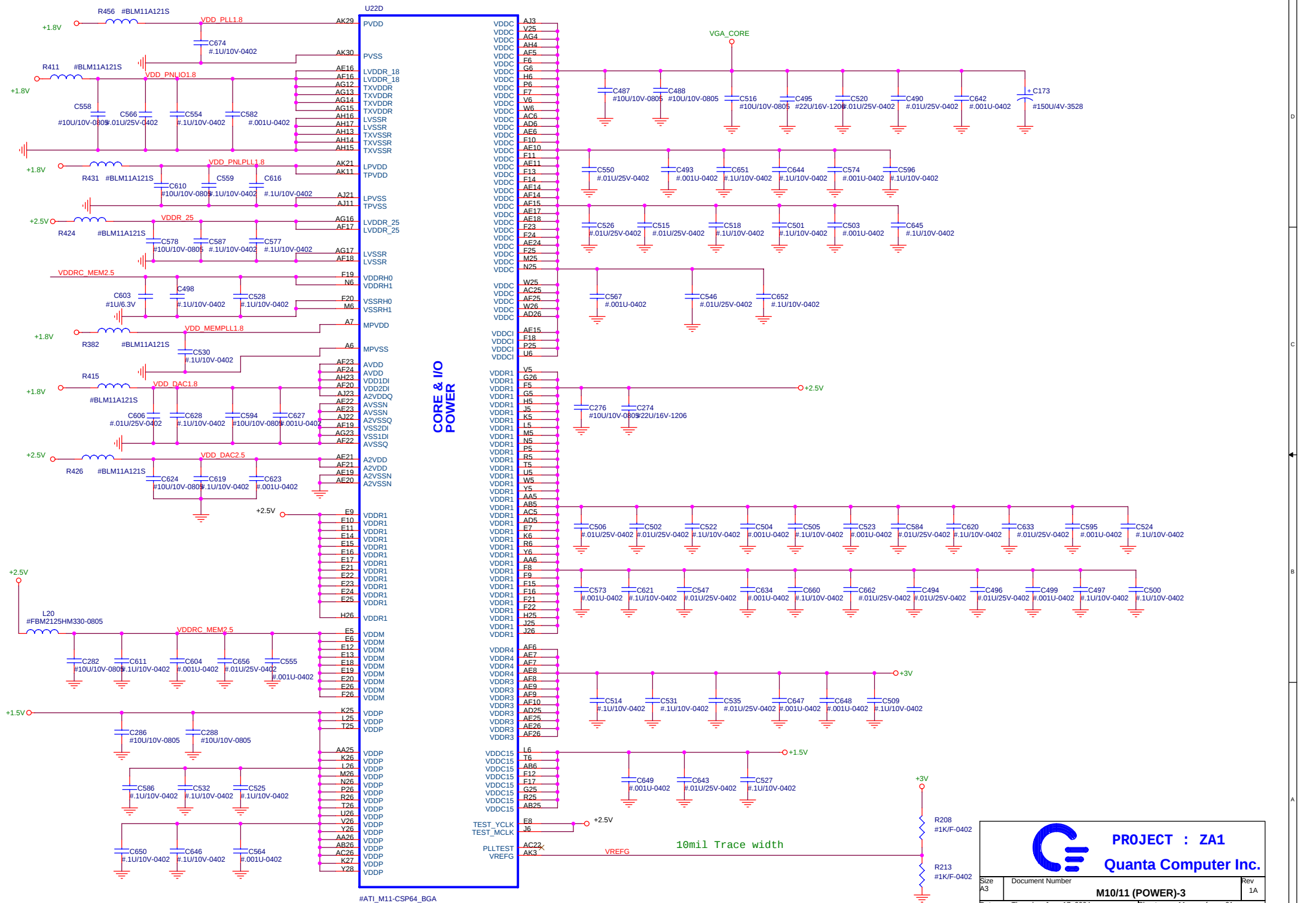
PROJECT : ZA1

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Size Custom	Document Number	Rev 1A
CLOCK GENERATOR		
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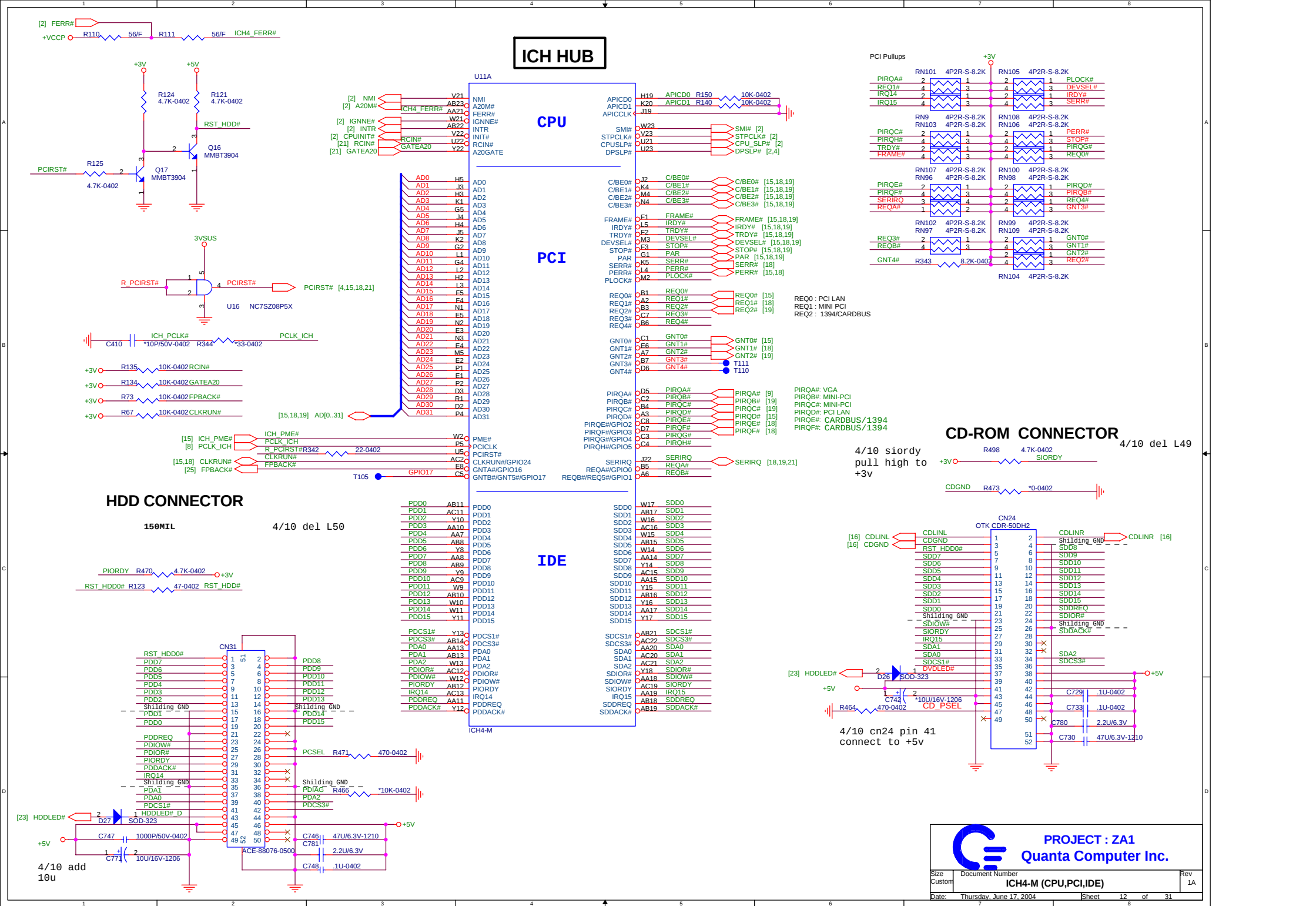






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Size A3	Document Number M10/11 (POWER)-3	Rev 1A
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ICH4_M

USB

HUB LINK

LPC&FWH

AC97&RTC

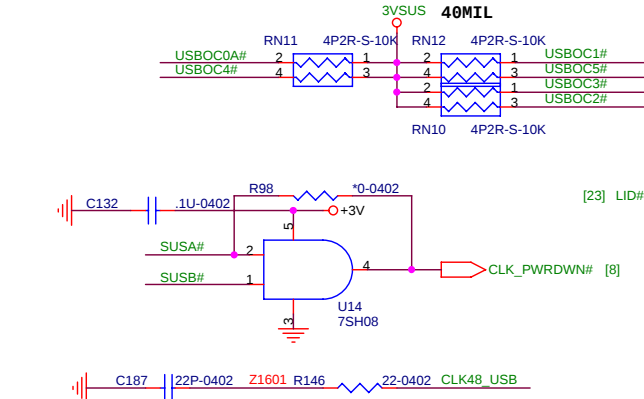
SM

PM

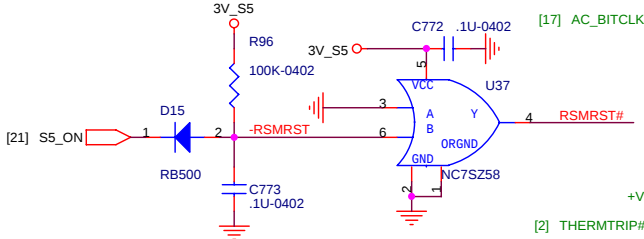
MISC&GPIO

SpeedStep

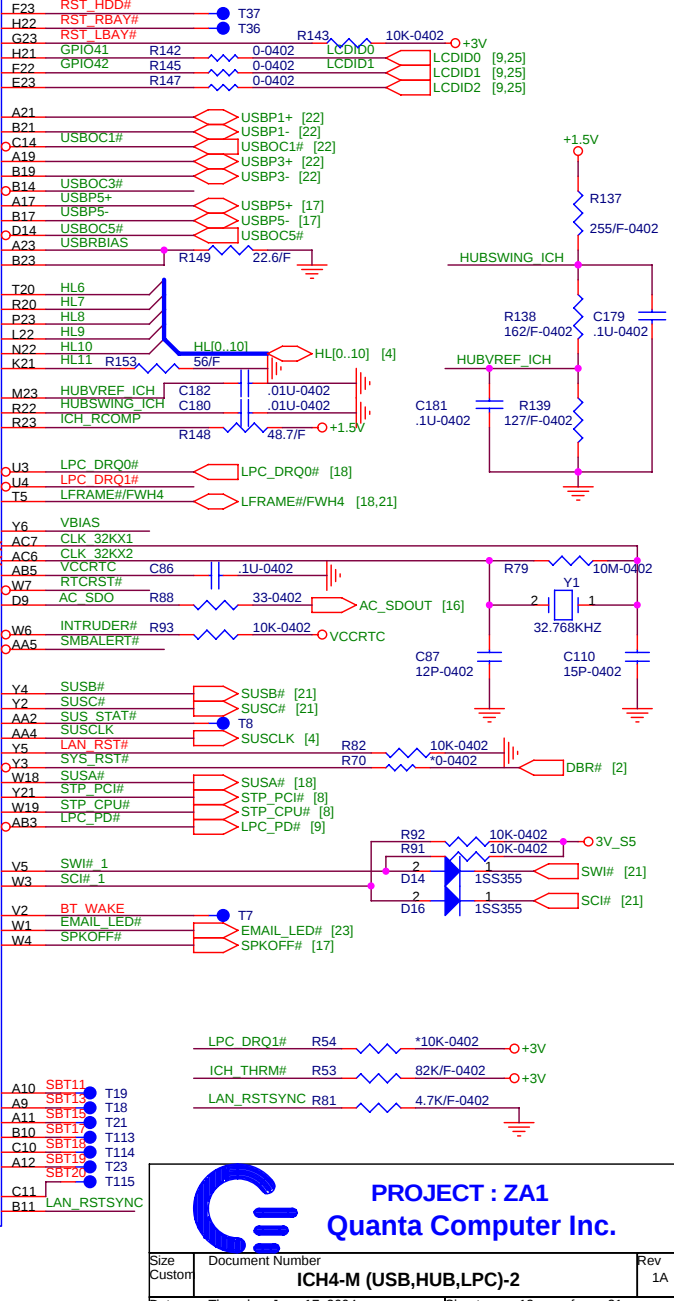
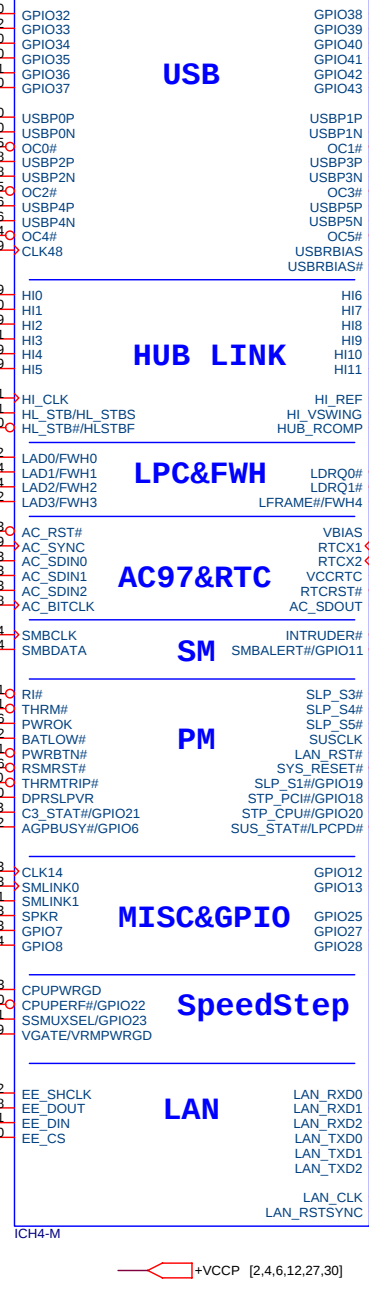
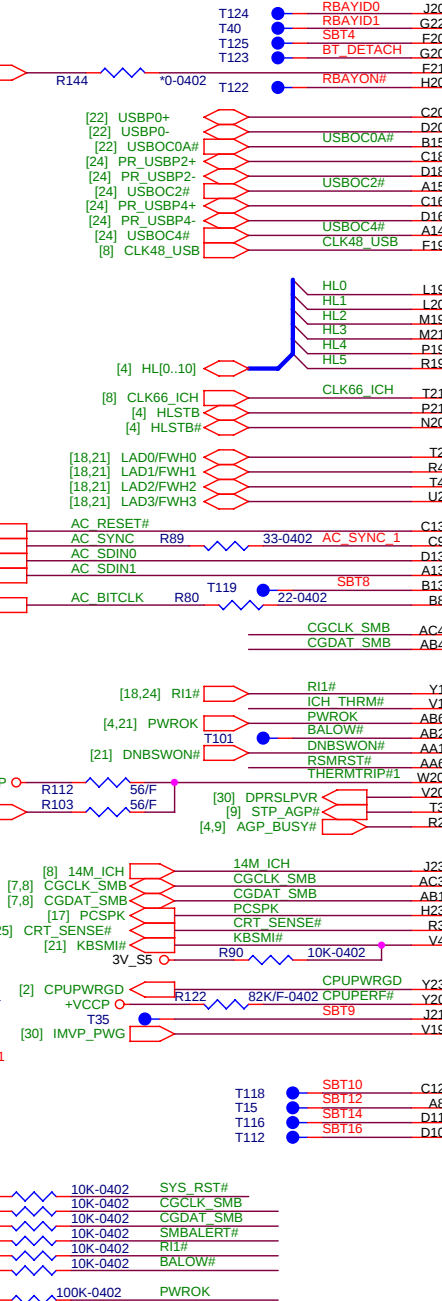
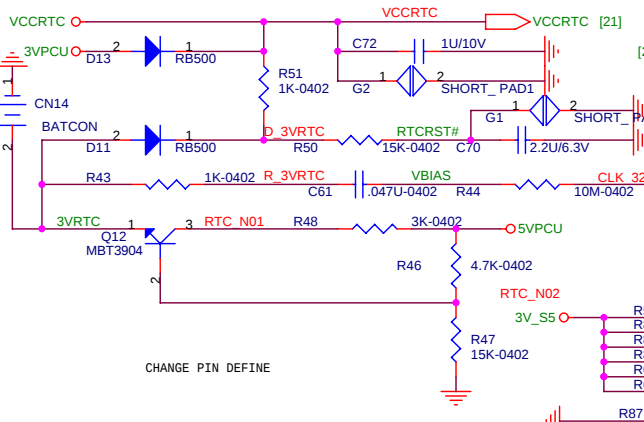
LAN



4/10 change rsmrst ckt

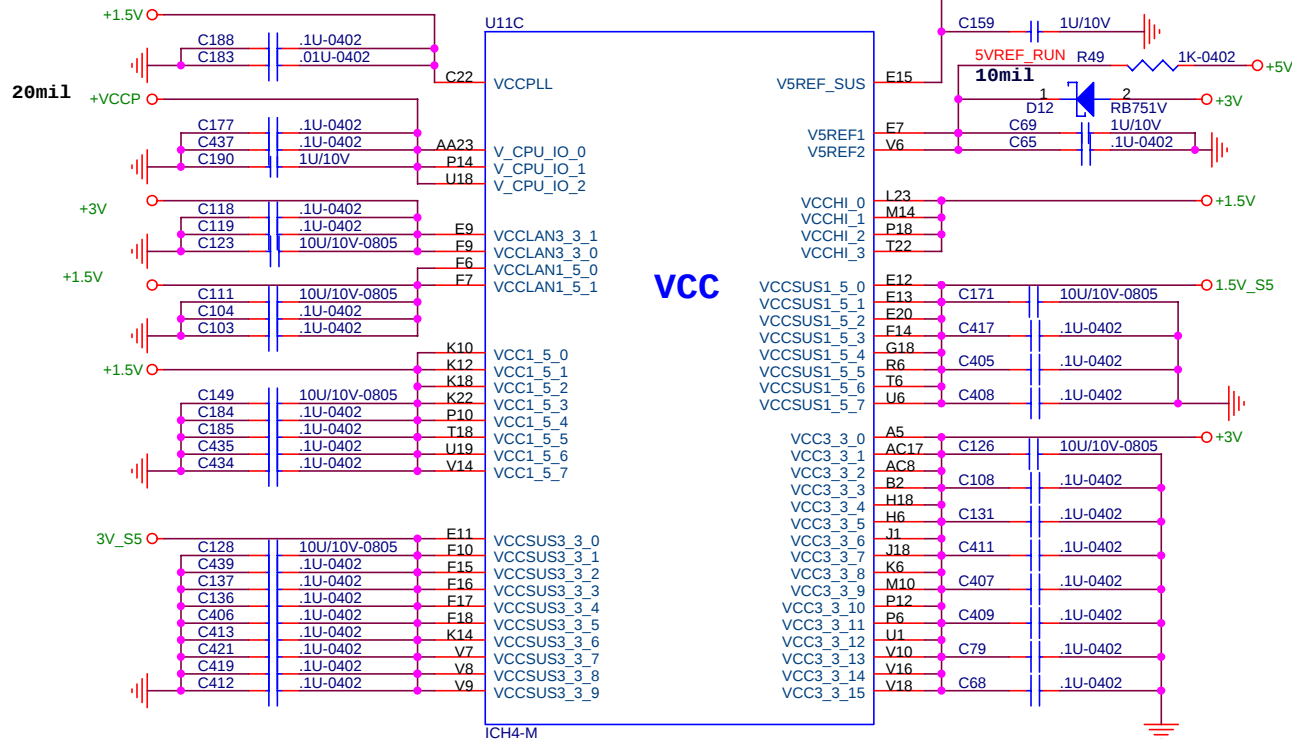


RTC

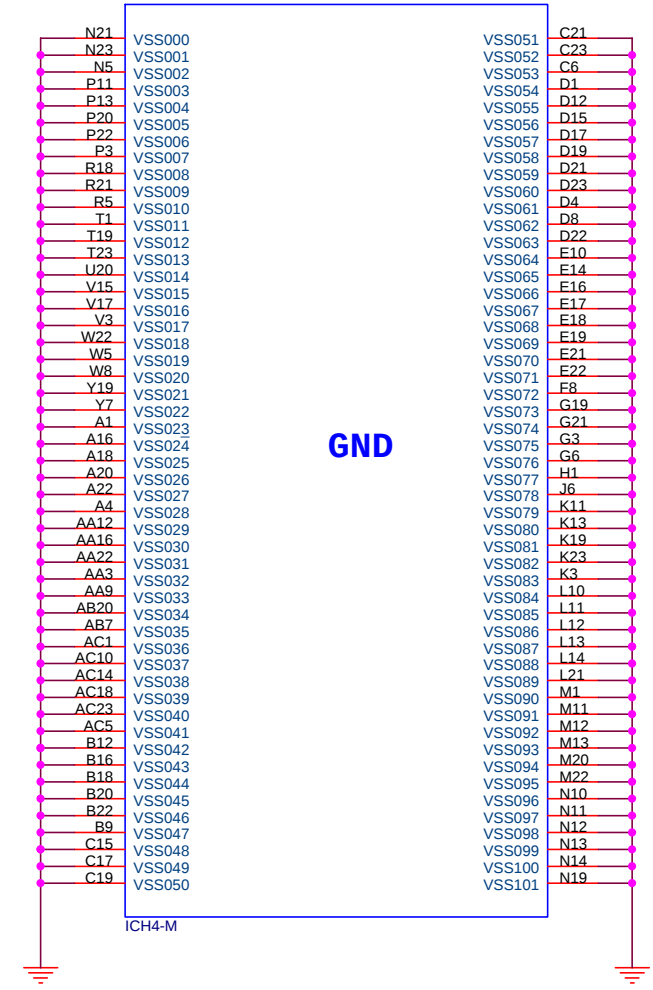


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SB:+1.5V 40MIL
SB:+1.5V_S5 40MIL
SB:+3V_S5 40MIL
SB:+3V 60MIL



U11D



ICH4-M

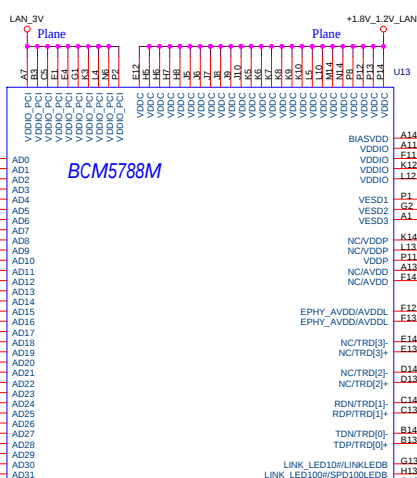
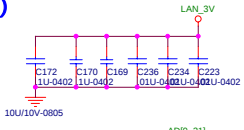
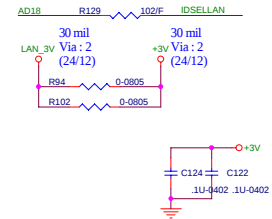


PROJECT : ZA1
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Size Custom	Document Number ICH4-M (POWER&GND)	Rev 1A
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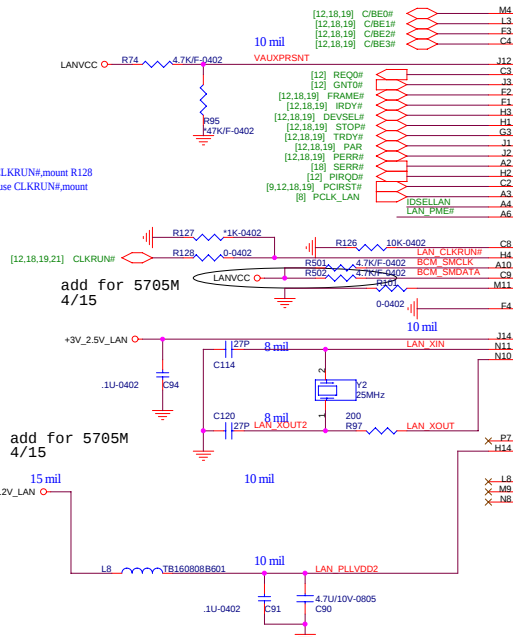
LAN (Boardcom BCM5705M)

ID Select : AD18
Interrupt Pin : PIQRB#
Request indicates : REQ0#
Grant indicates : GNT0#

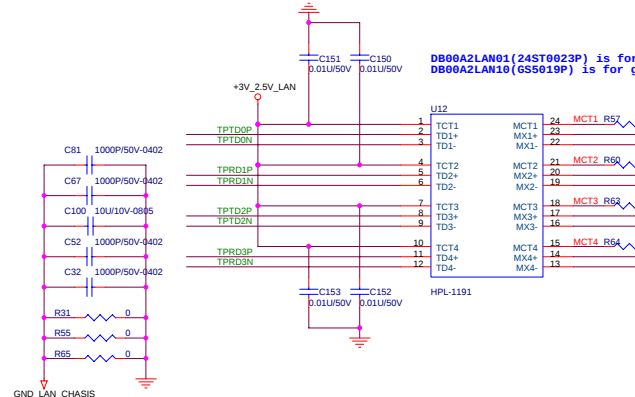
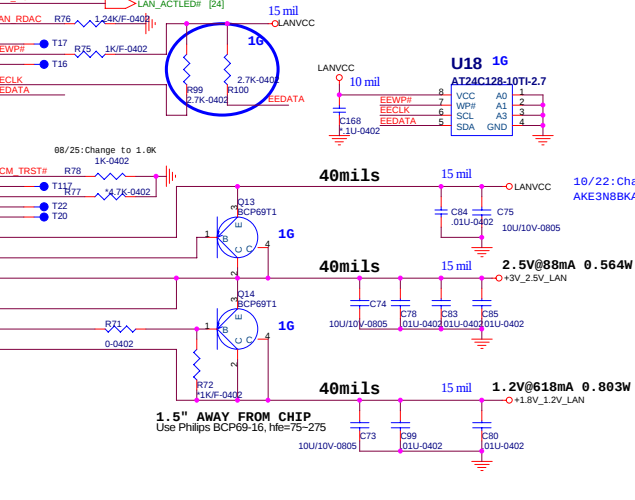
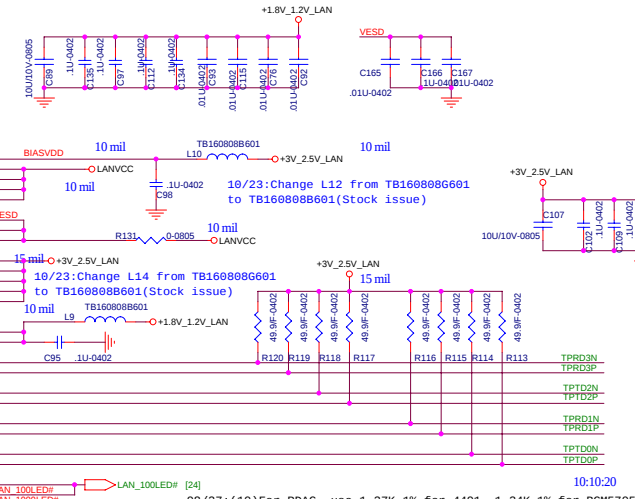
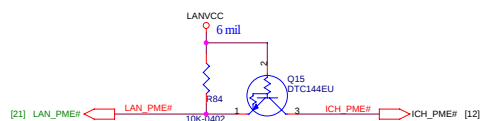


15mm x 15mm
BGA196

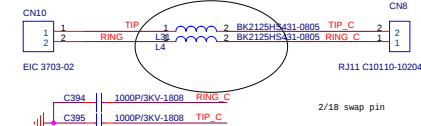
4/10:If use CLKRUN# mount R128
If not use CLKRUN# mount
R127



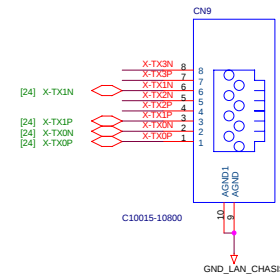
18/23:Change L13 from TB160808G601 to
TB160808B601 (Stock issue)



RJ11

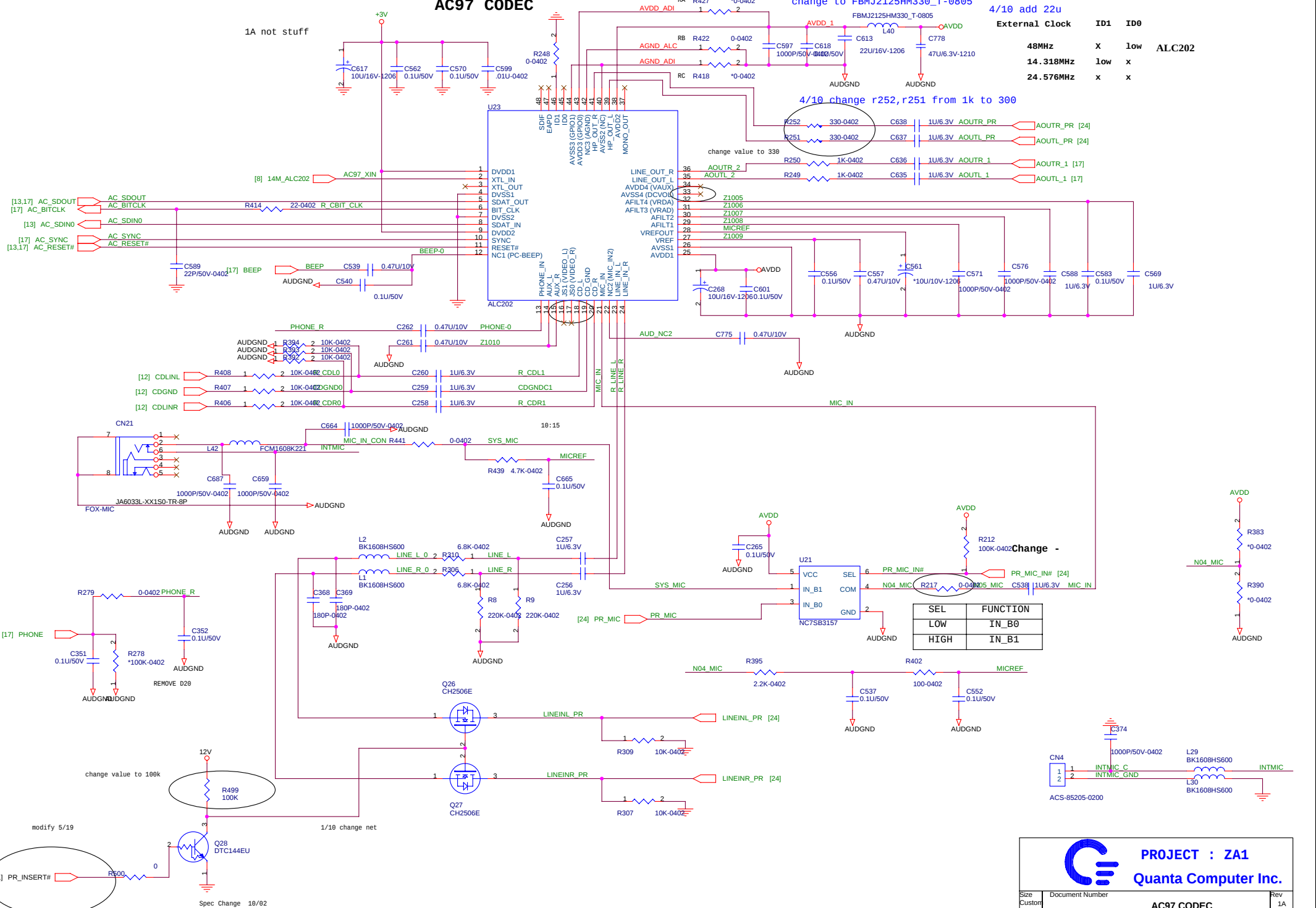
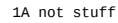


RJ45



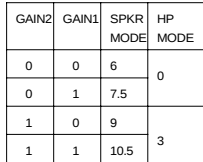
ok

AC97 CODEC



External Clock	ID1	ID0	
48MHz	X	low	ALC202
14.318MHz	low	x	
24.576MHz	x	x	

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



BT CONNECTOR

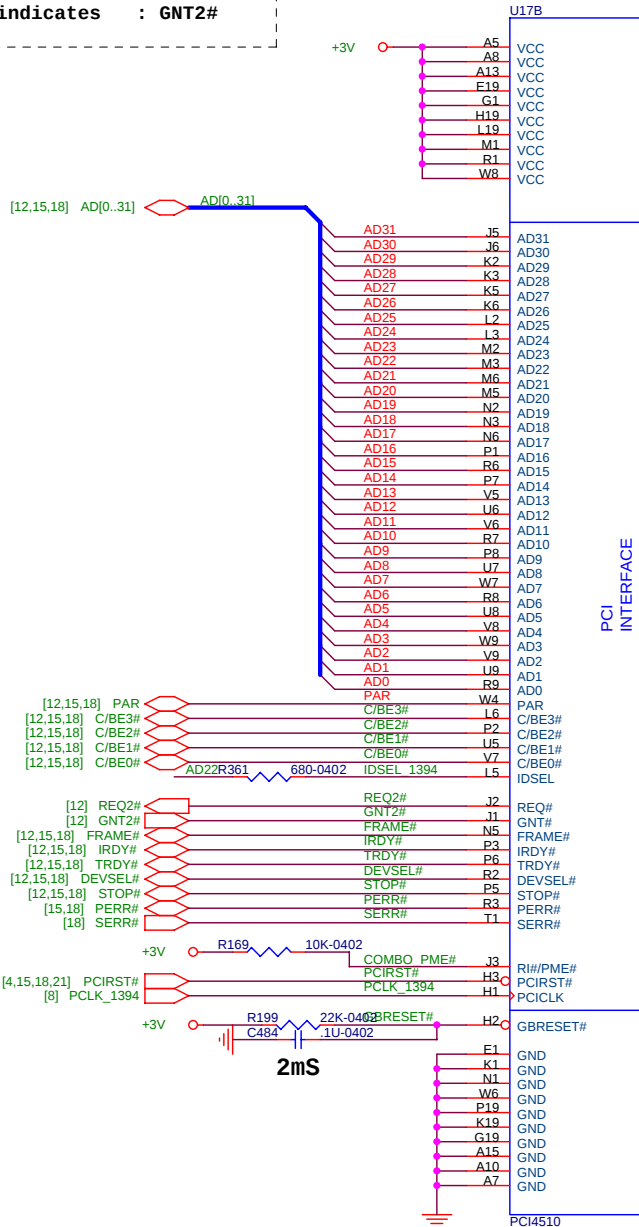
[illegible]

Figure 1: Schematic diagram of the audio interface circuit. The diagram shows a multi-pin connector (CN26) connected to a microcontroller (MOC30) and an audio IC (AC97). The microcontroller pins include MONO_OUT/PC_BEEP, GND, ALUXA_RIGHT, ALUXA_LEFT, CD_RIGHT, CD_LEFT, GND, 3V_AUX, GND, 3V, AC97_SDATA_OUT, AC97_RESET#, AC97_MSTRCLK, and AC97_BITCLK. The audio IC pins include MONO_PWRDN, MONO_PHONE, GND, RESERVED, CD_RIGHT, CD_LEFT, GND, PRIMARY, GND, AC97_SYNC, AC97_SDATA_INB, AC97_SDATA_INA, GND, and AC97_BITCLK. External components include a 3V_MODEM, a 3V supply, a 33F-0402 resistor, a 100F-0402 capacitor, a 10K-0402 resistor, and a 10K-0402 resistor. The audio IC is connected to a PHONE jack and a PHONE [16] signal. The microcontroller is connected to an AC_SYNC signal, an AC_SDATA_IN [13] signal, and an AC_BITCLK [13,16] signal.

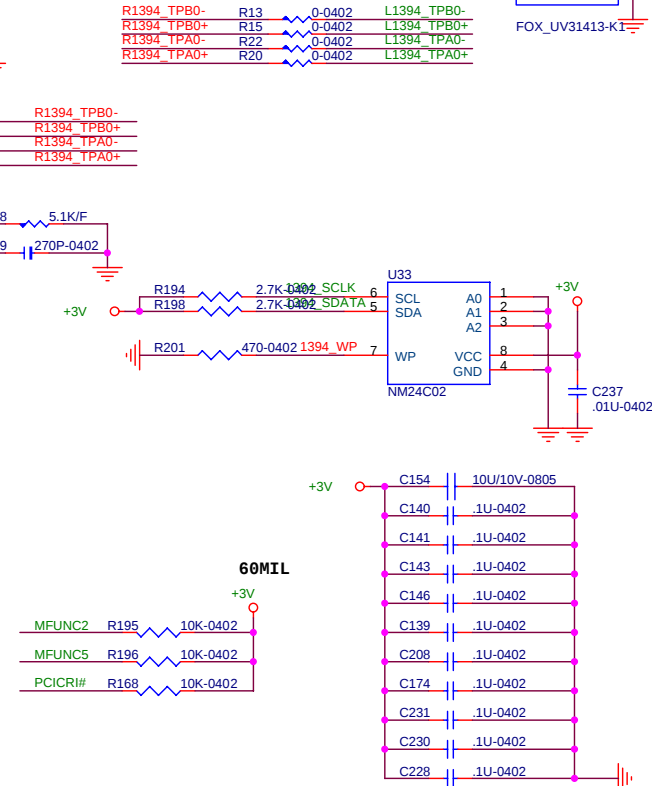
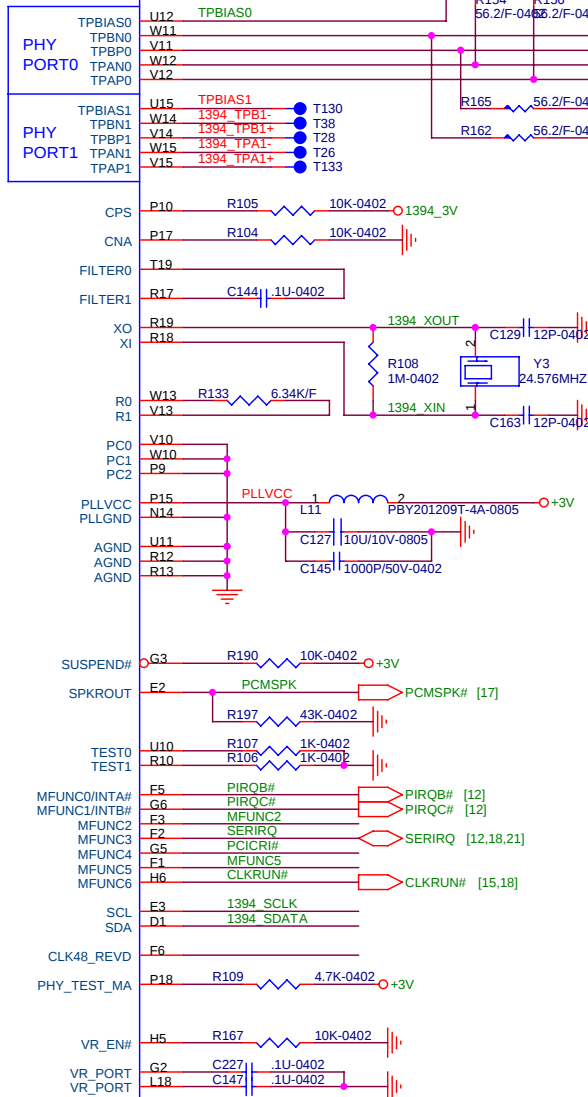
 PROJECT : ZA1
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ID Select : AD22
Interrupt Pin : PIRQ B,C#
Request indicates : REQ2#
Grant indicates : GNT2#

CARDBUS/1394

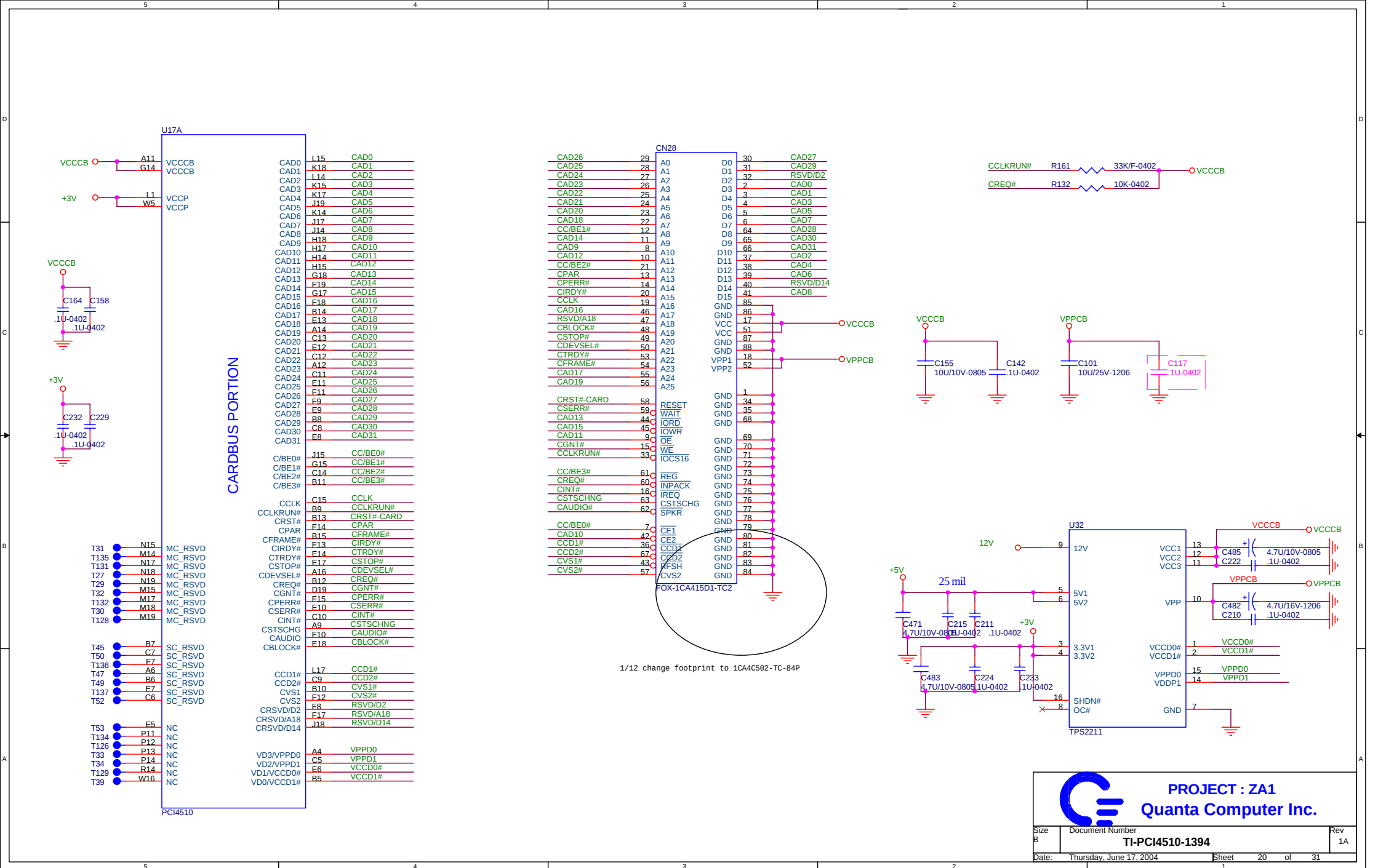


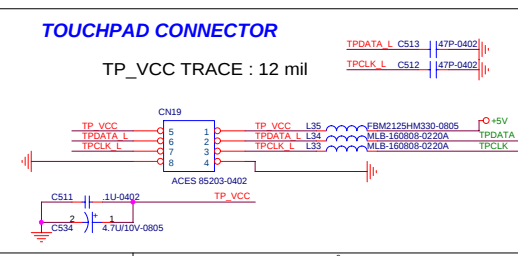
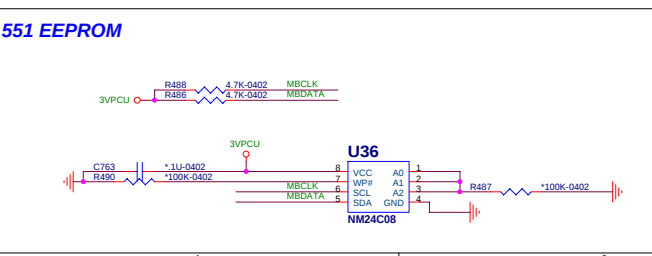
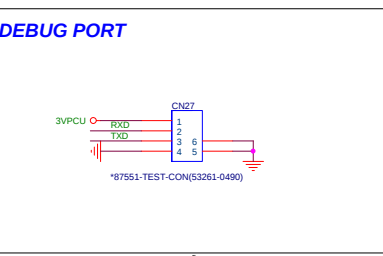
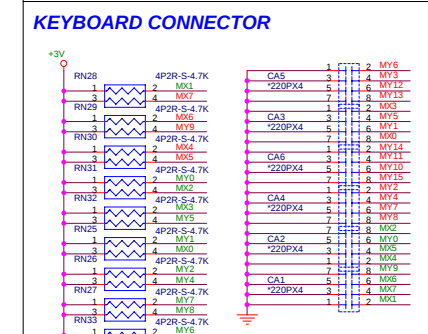
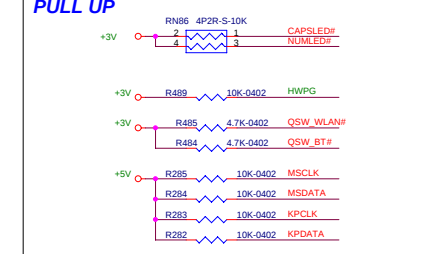
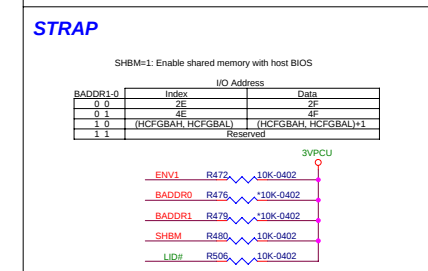
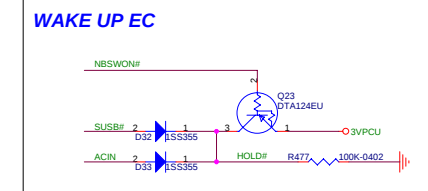
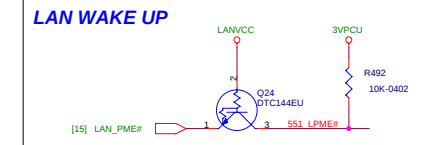
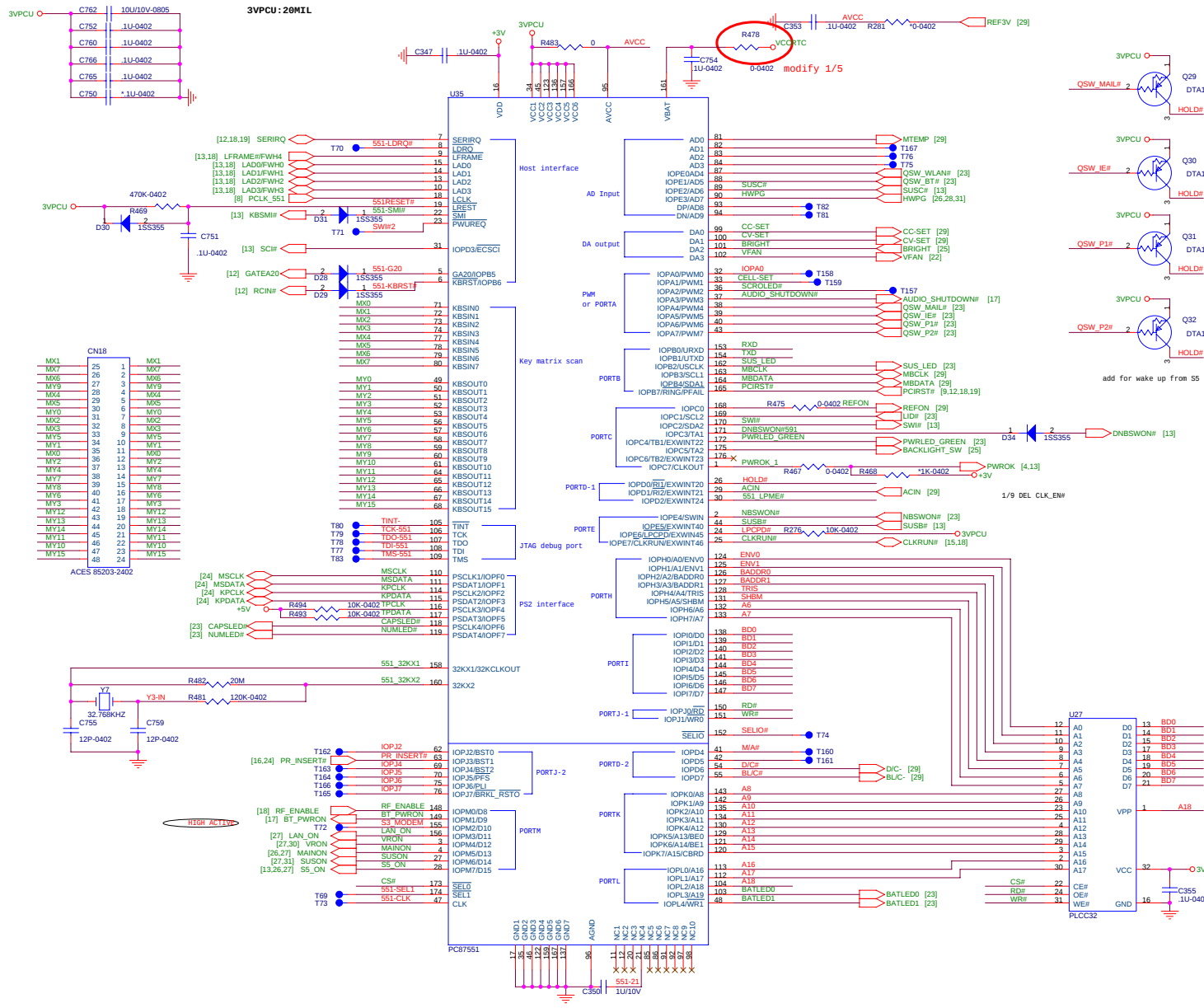
PCI/1394_OHCI PORTION

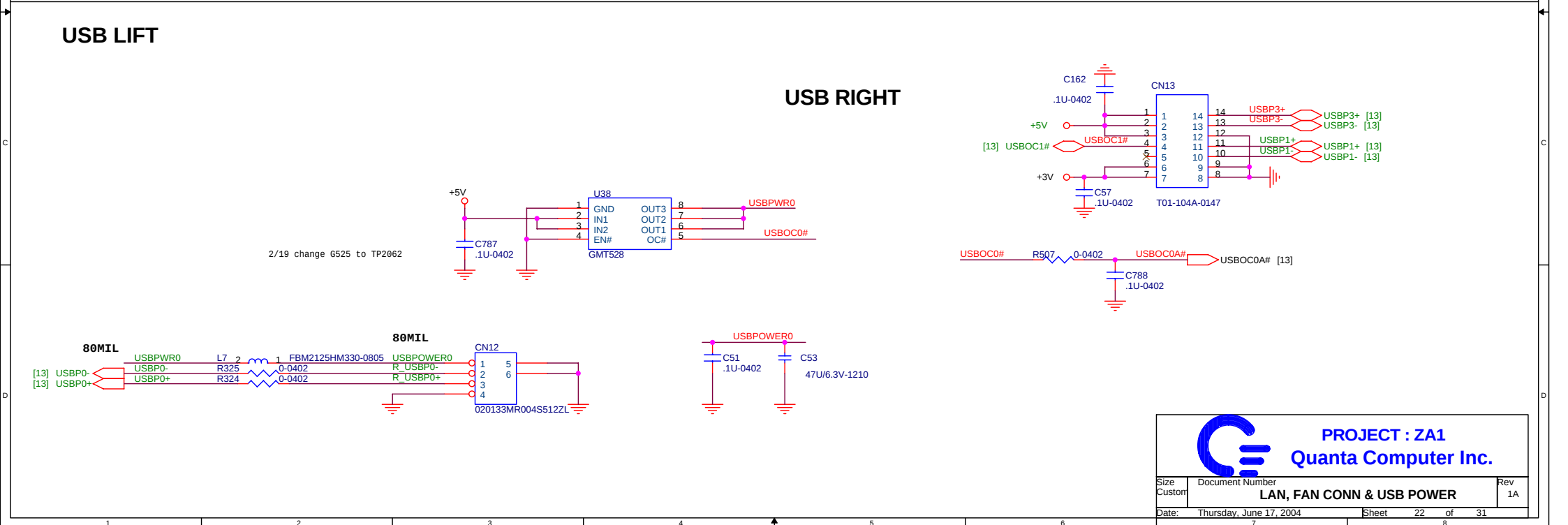
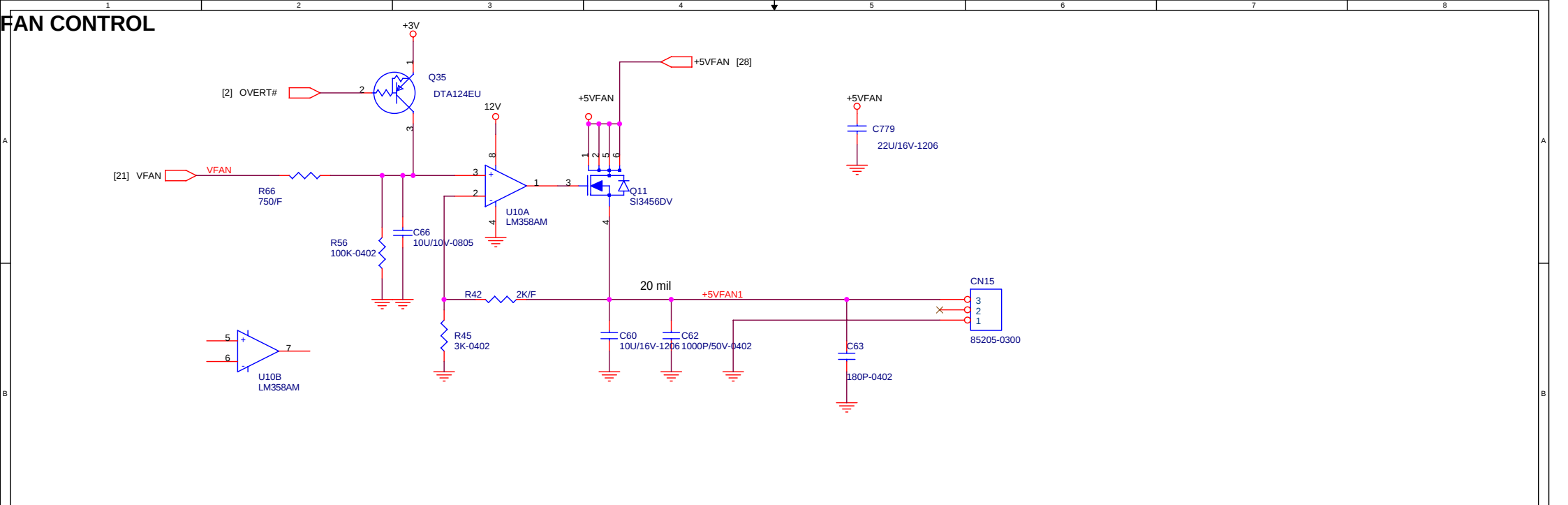


PROJECT : ZA1
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Size B	Document Number	Rev 1A
	TI-PCI4510-1394	
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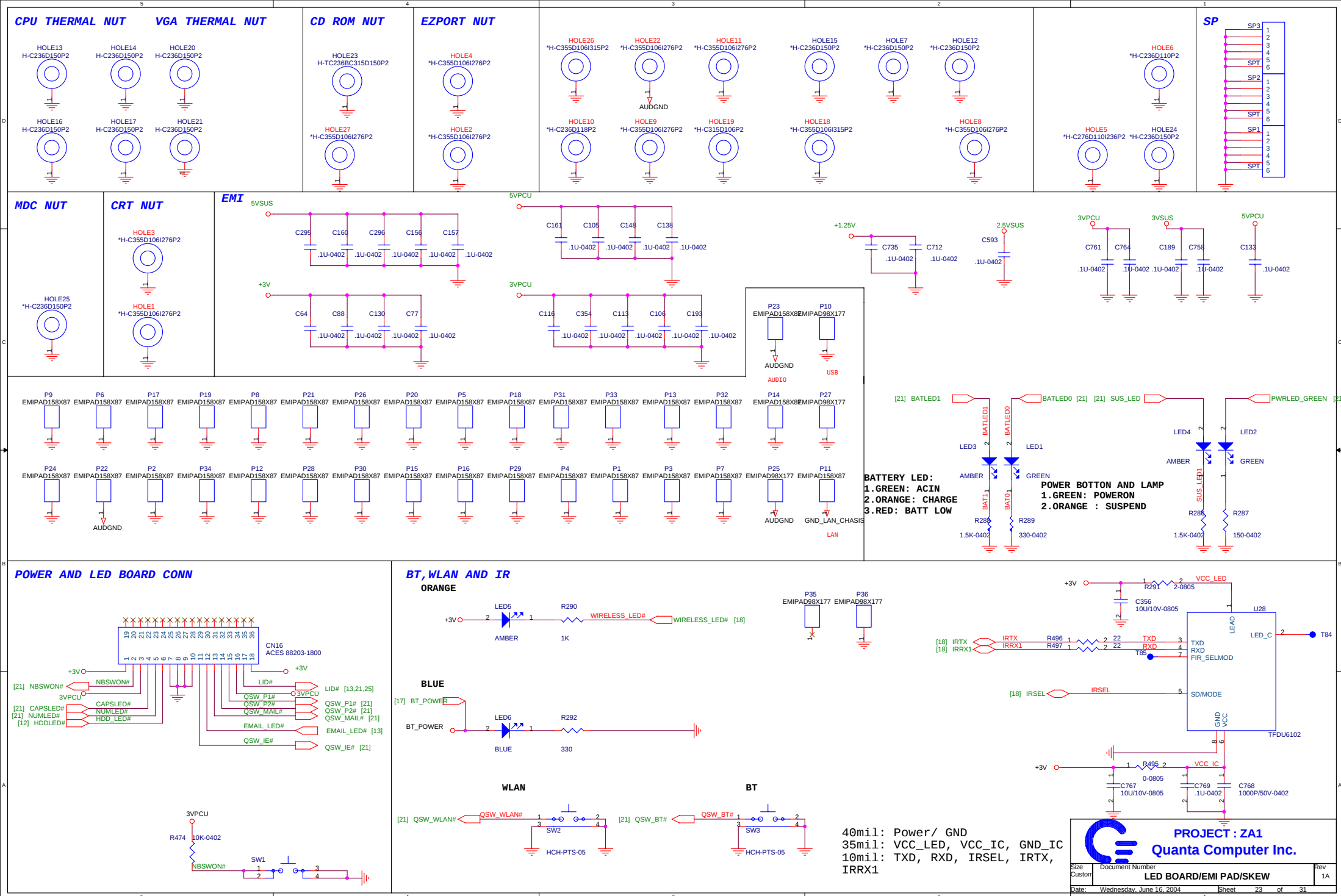


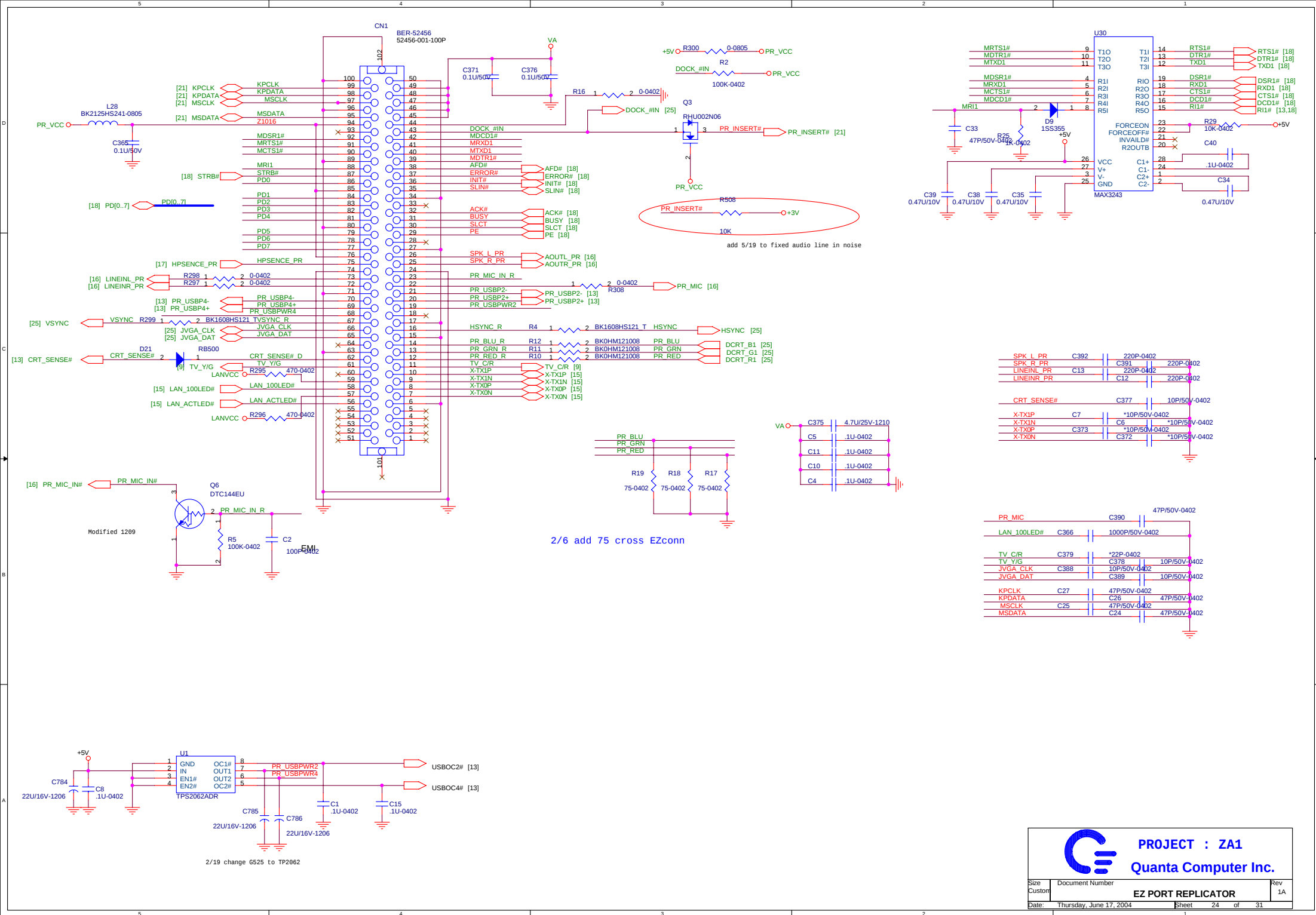


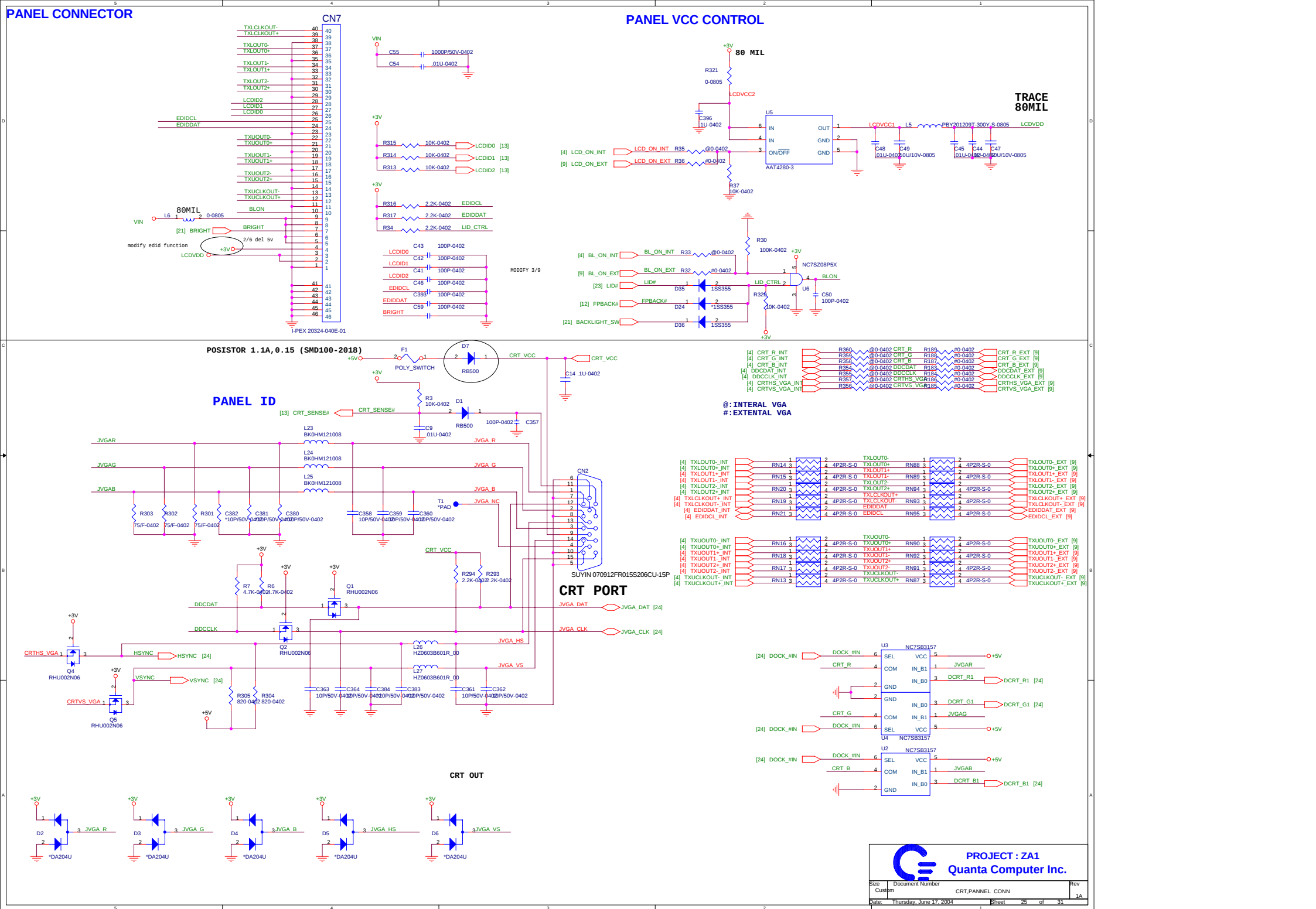


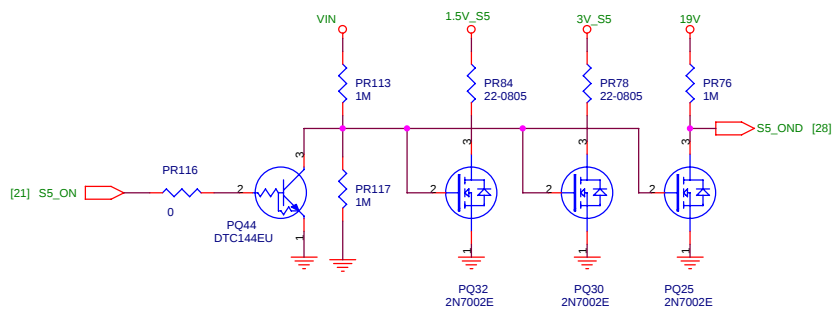
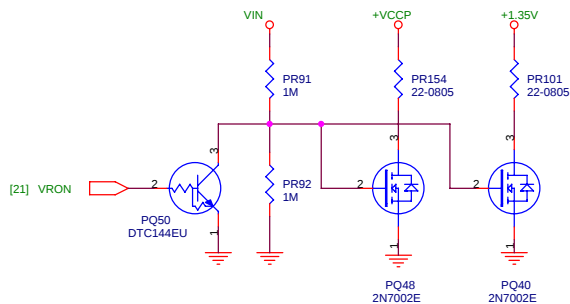
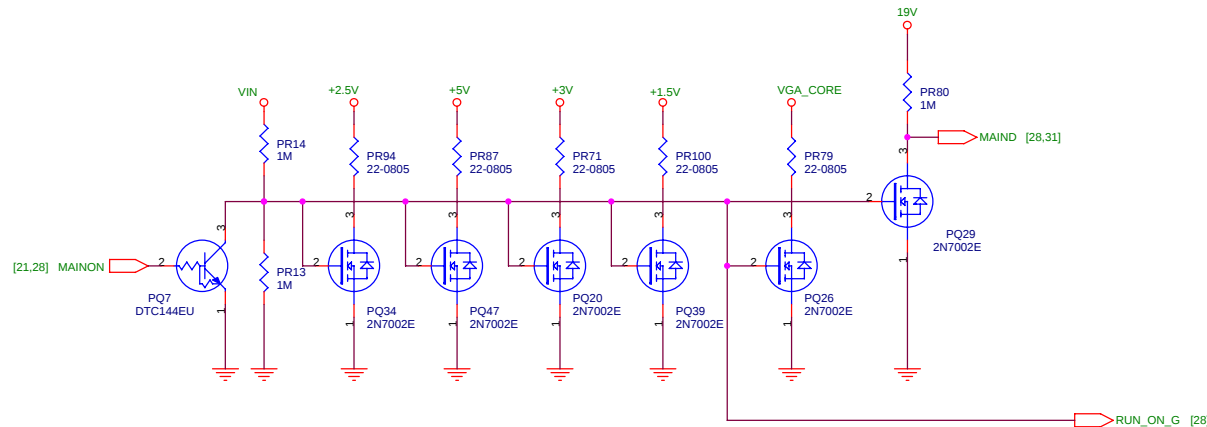
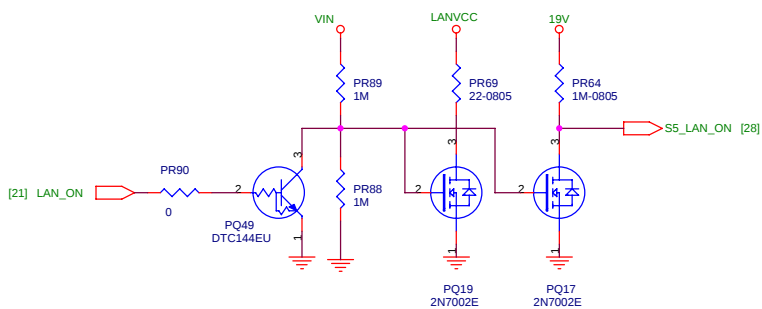
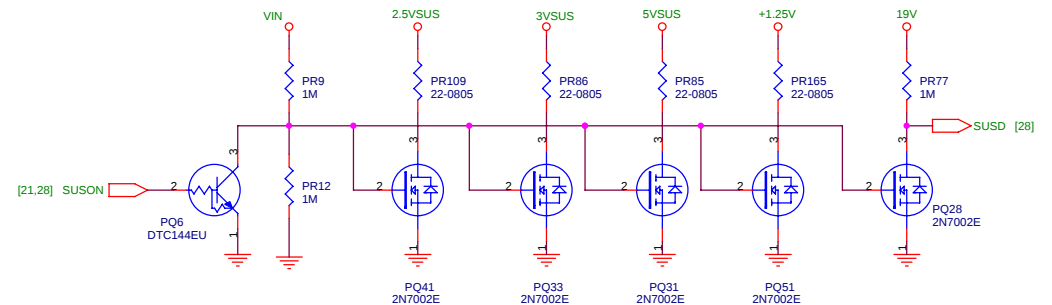
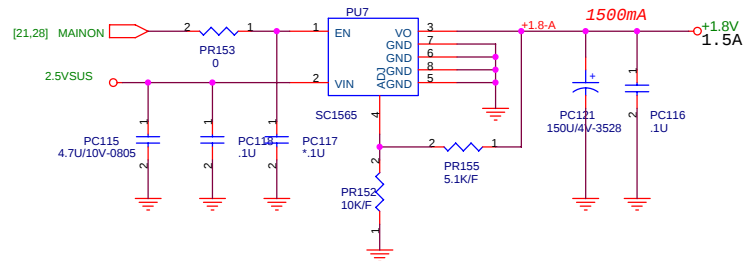
PROJECT : ZA1
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Size Custom	Document Number LAN, FAN CONN & USB POWER	Rev 1A
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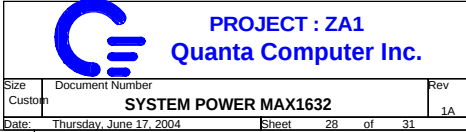


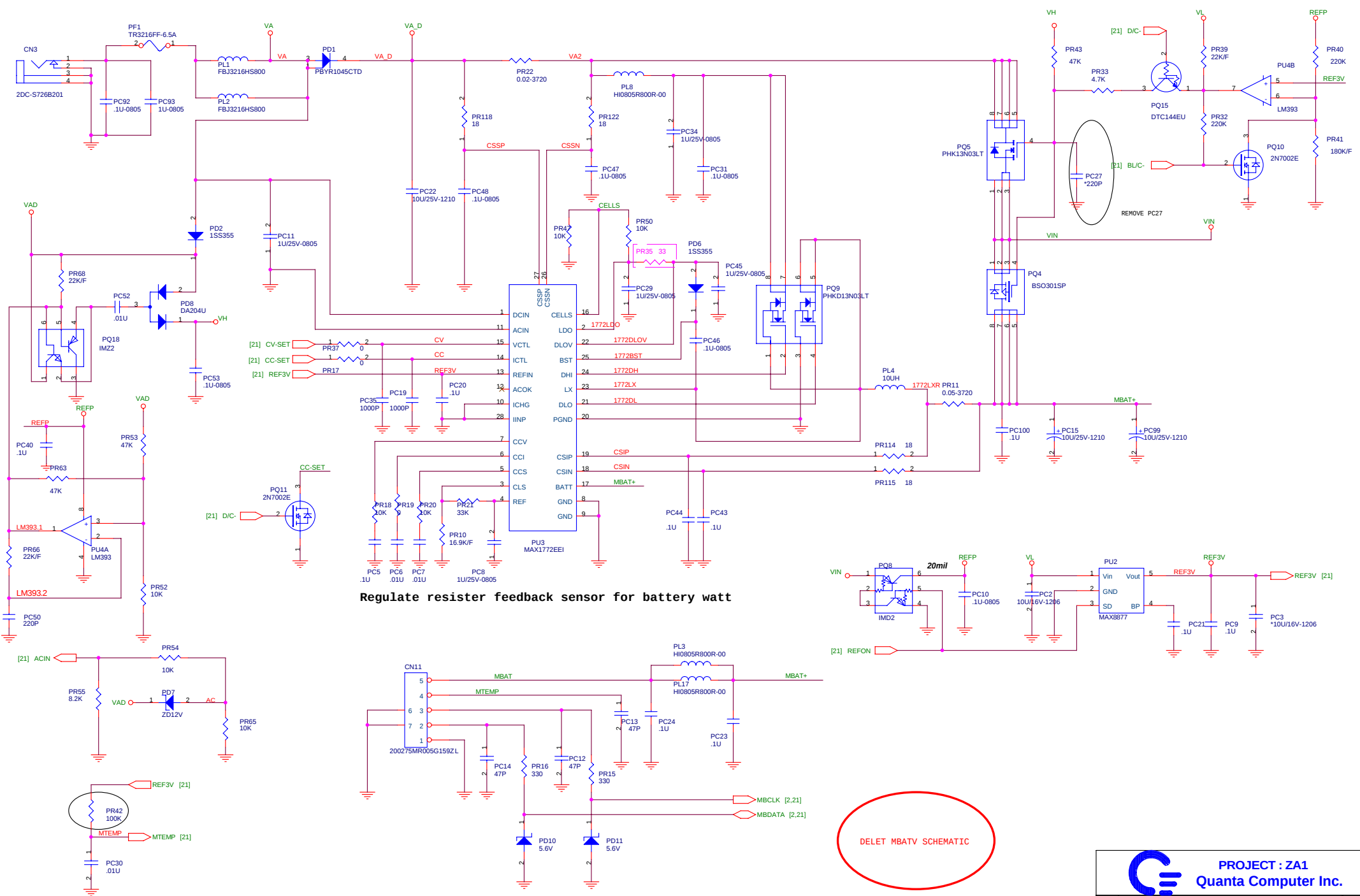




PROJECT : ZA1
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Size	Document Number	Rev
Custom	DISCHG&+1.8V	1A
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Regulate resistor feedback sensor for battery watt

DELET MBATV SCHEMATIC

