

Myna II

Project code: 91.4C201.001
PCB REVISION: 05216-SB

CLK GEN.
IDT CV125
3

Mobile CPU
Dothan
CLE-1.5G / Dothan2.13G
(CPU on board,no socket)
4, 5

G792
19

HOST BUS 533MHz

DDR II
400/533 MHz
11,12

DDR II
400/533 MHz
11,12

Alviso-GM

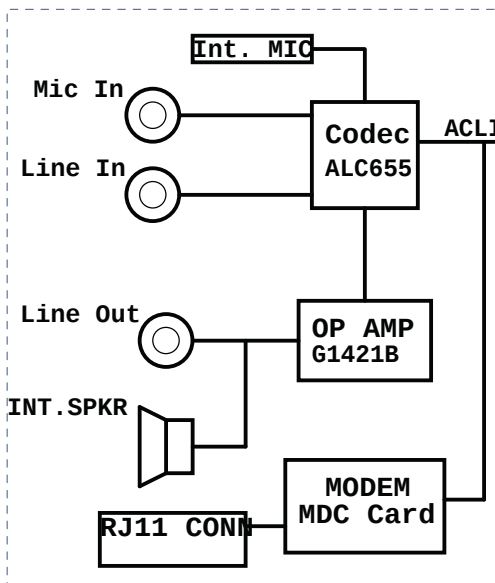
KI.91501.017

6,7,8,9,10

DMI I/F 100MHz

ICH6-M

Ver.: B2, KI.80101.011



IO Board

(co-lay with PCMCIA)

New card
29

PWR SW
TPS2231
29

PCI-E

PATA

two USB port
on IO Board

USB
3 PORT
21

MINI USB
Blue-tooth
21

HDD
20

NS
SIO
87392
31

FIR

KBC
Renesas RE144B
30

Touch
Pad
32

INT.
KB
32

BIOS ROM
4M BITS
PM49F004T-33VC
33

LPC
DEBUG
CONN.
33

PCI BUS

LPC BUS

TI
PCI 7411
1* Slot Cardbus
1* 1394
CardReader
24,25

MS/MS Pro/
xD/ MMC/SD
5 in 1
26

Mini-PCI
802.11A/B/G
(only smaller)
30

LAN
Giga
BCM5788-M
22, 23

TXFM
23

RJ45 CONN
23

PCMCIA I/F

PWR SW
TSP2220A
26

PCMCIA
SLOT
Support
TypeII
26

1394 6pin
Conn
27

CH7307C

53-TMDS

DVI-D
(EZ4 only)
35

RGB CRT

CRT
14

LVDS

LCD
13

TV
(EZ4 only)

SYSTEM DC/DC TPS5130 41,42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO)
SYSTEM DC/DC ISL6227 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
TPS51100DGQ 43	
1D8V_S3	VTT_S0(0.9V)

MAXIM CHARGER MAX8725ETI 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 3.2A UP+5V 5V 100mA

CPU DC/DC ISL6218CV-T 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

Easy Port 4 (124 PIN)

AC IN RJ45-11 SEARIAL PORT CRT PRINTER PS2 MIC LINE IN LINE OUT TV OUT DVI PCIEx2 SMBUS
34, 35

<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Rev
BLOCK DIAGRAM	SB
Size	Document Number
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Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test Straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

- 1.CHECK P5[105V & 105V-AVDD]
- 2.CHECK P8[PM & GM]

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

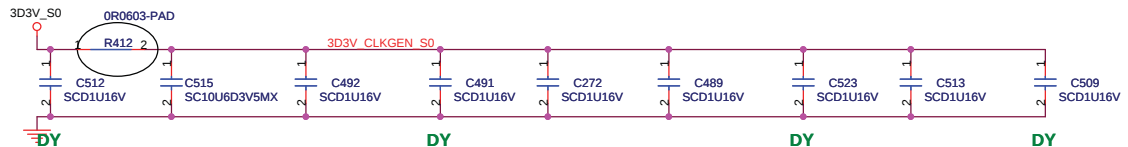
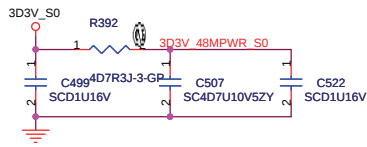
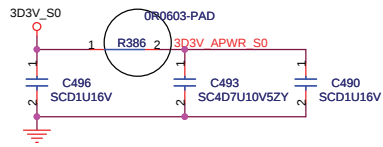
ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

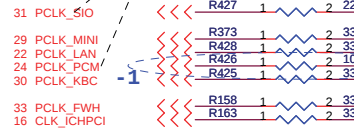
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
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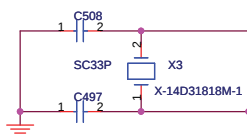


?cost

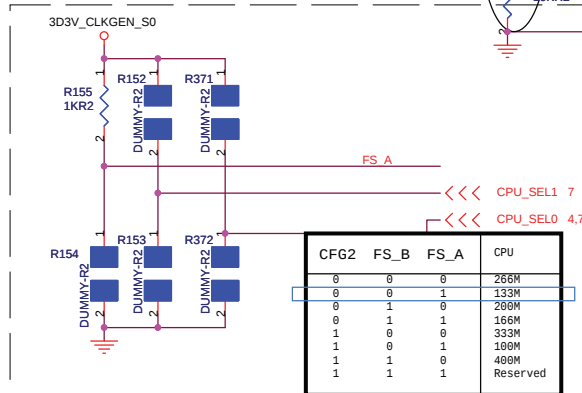
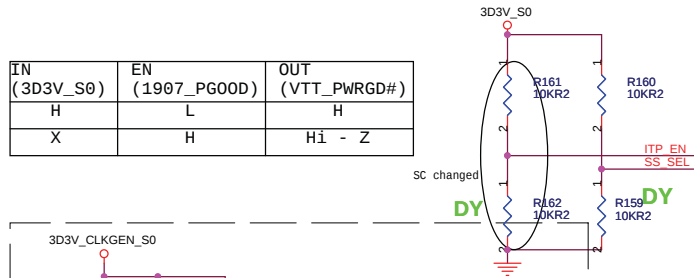
PCLK_PCM & PCLK_SIO
need equal length



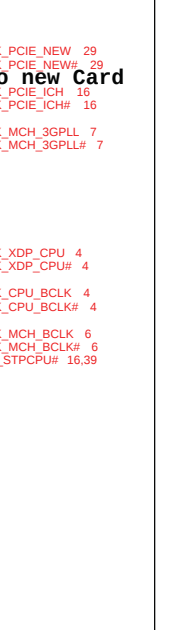
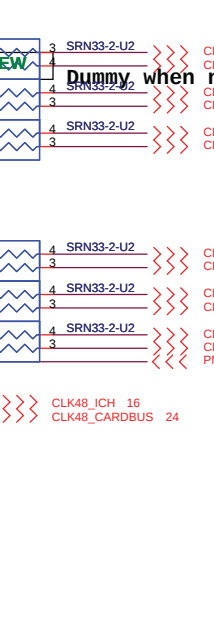
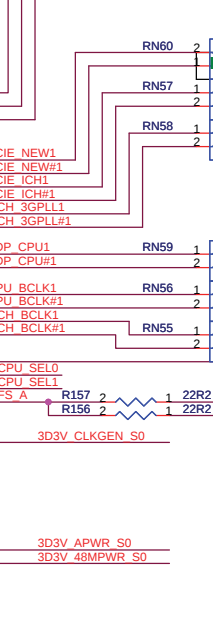
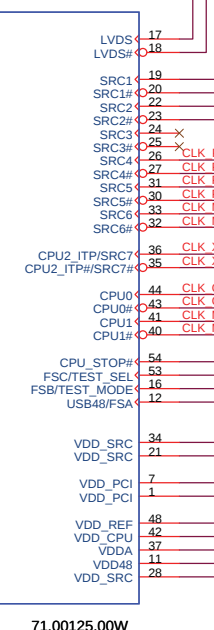
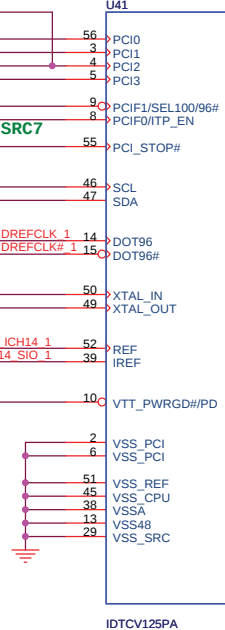
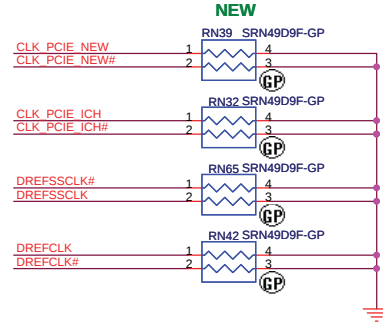
CLK_ICH14 & CLK14_SIO
need equal length



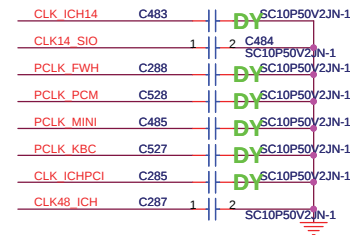
IN (3D3V_S0)	EN (1907_PG00D)	OUT (VTT_PWRGD#)
H	L	H
X	H	H1 - Z



CFG2	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	1	333M
1	1	0	100M
1	1	1	400M
1	1	1	Reserved



EMI capacitor



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Clock Generator - IDT125

Size A3

Document Number

Myna2

Date

Monday, September 26, 2005

Sheet

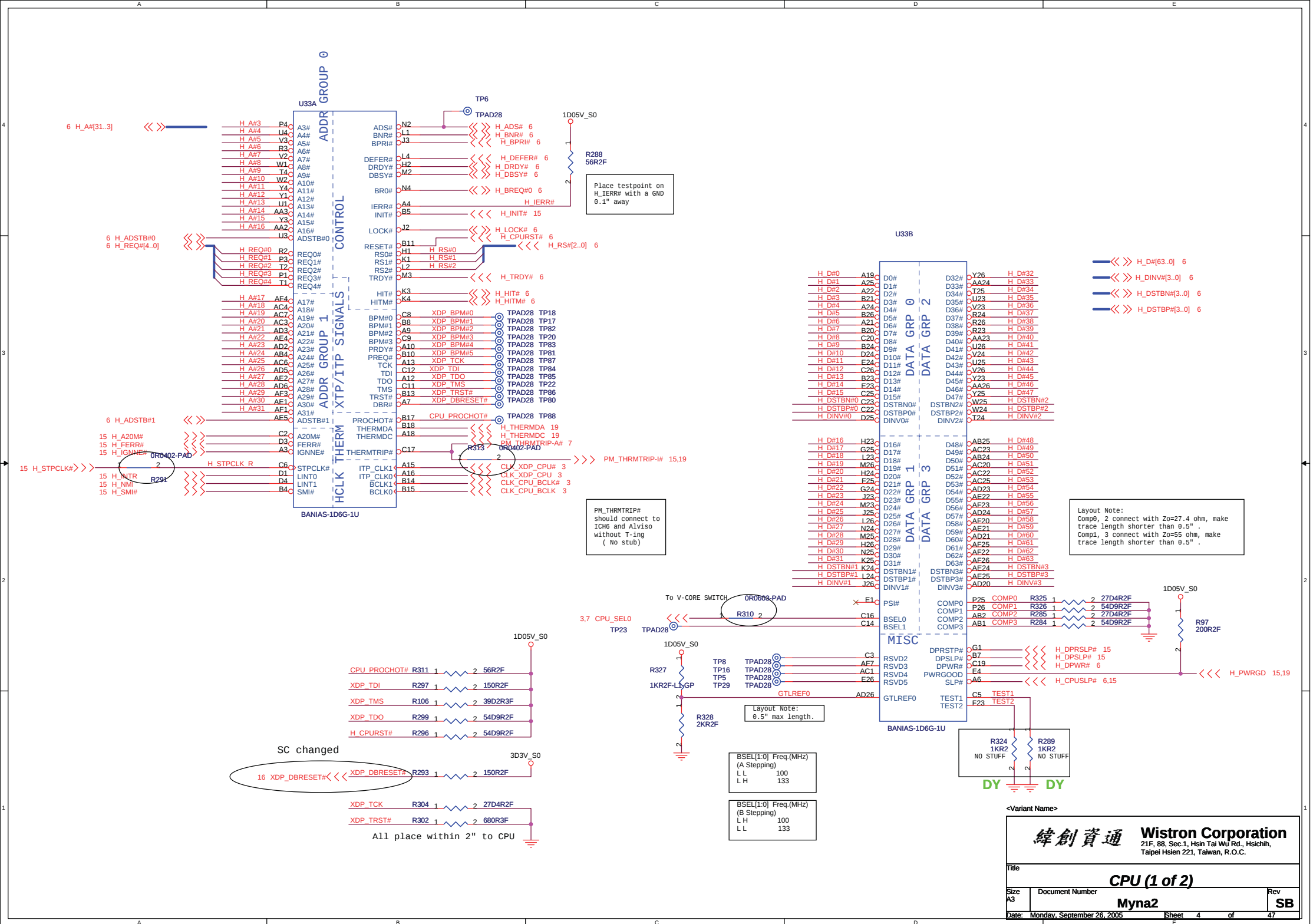
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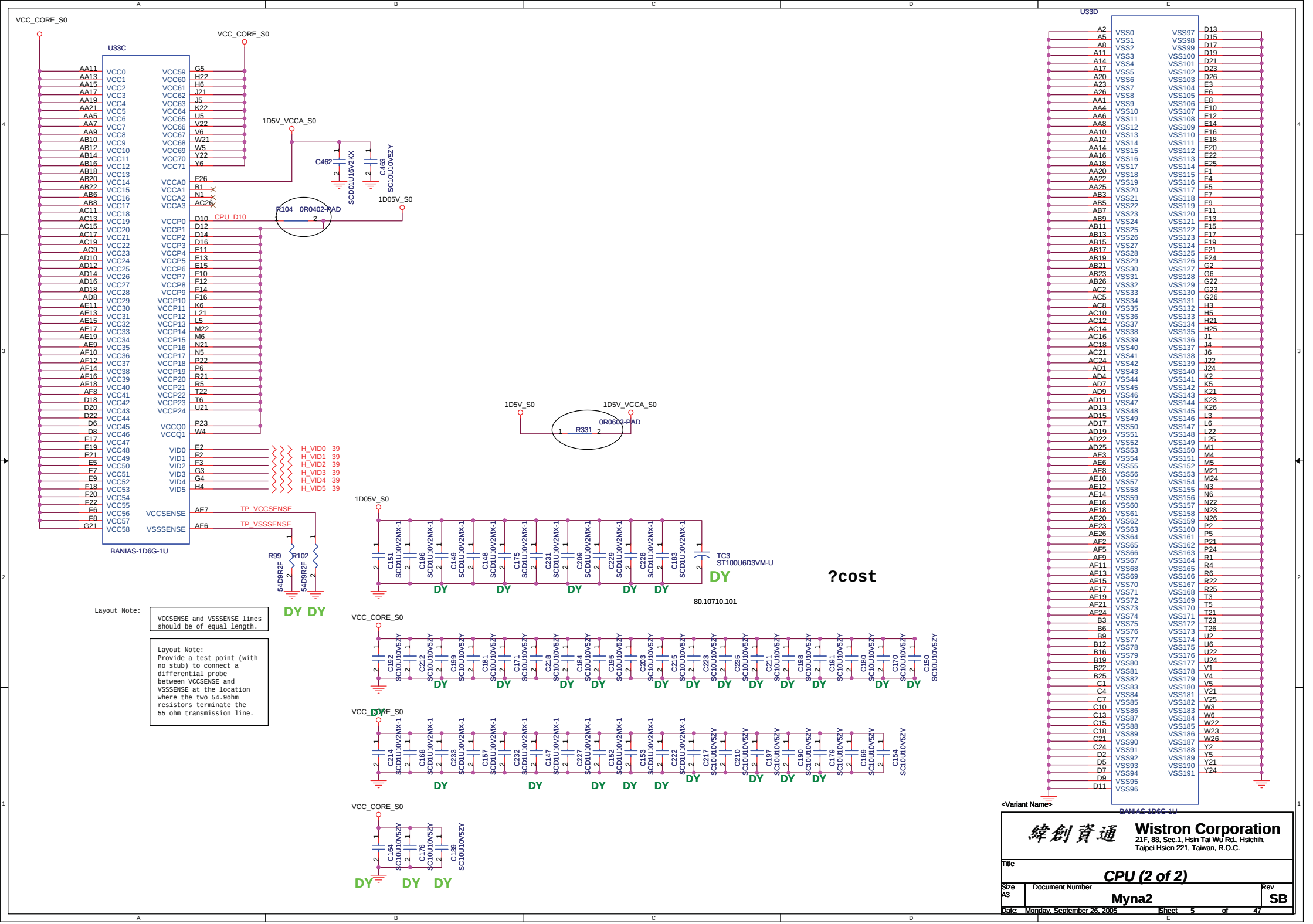
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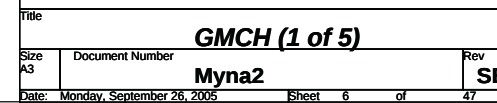
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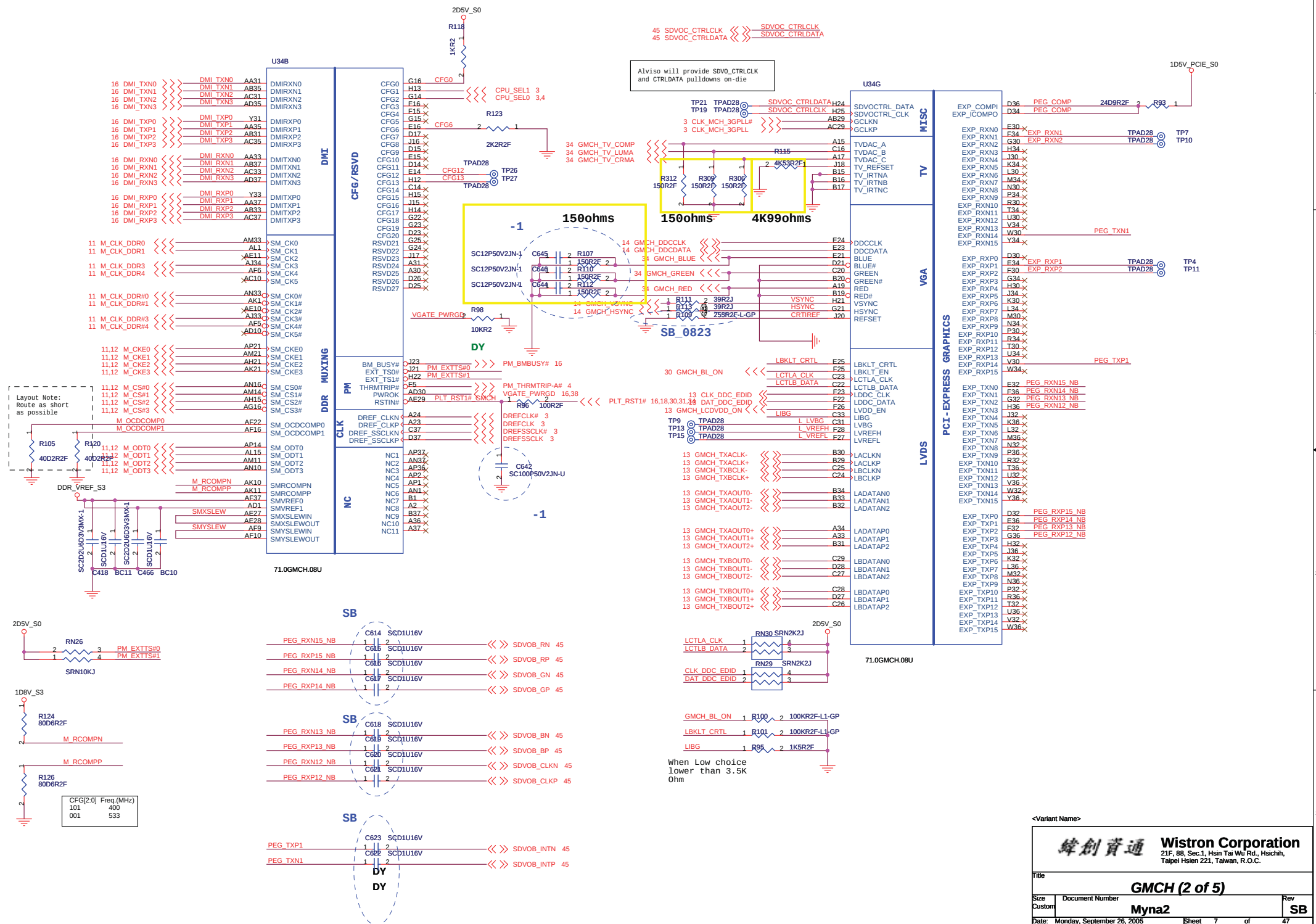
Rev

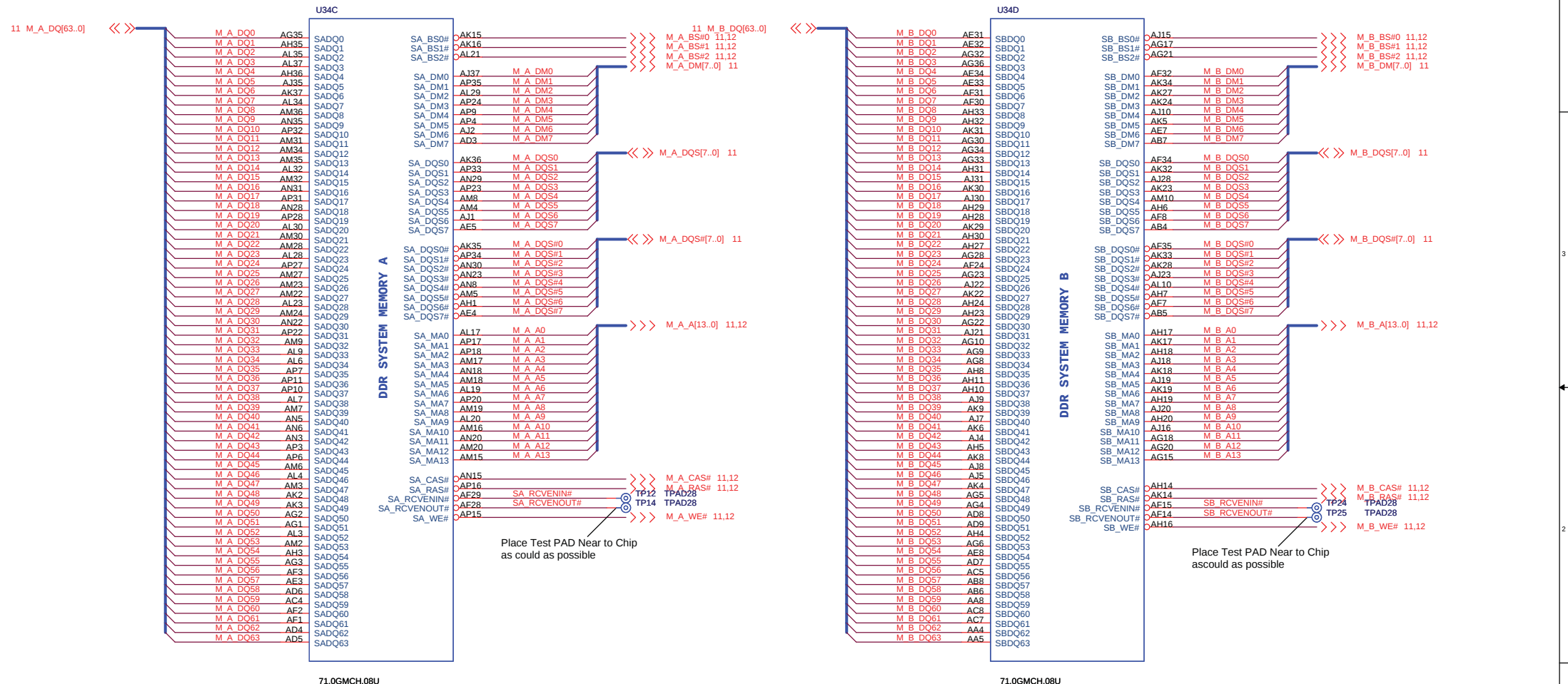
SB

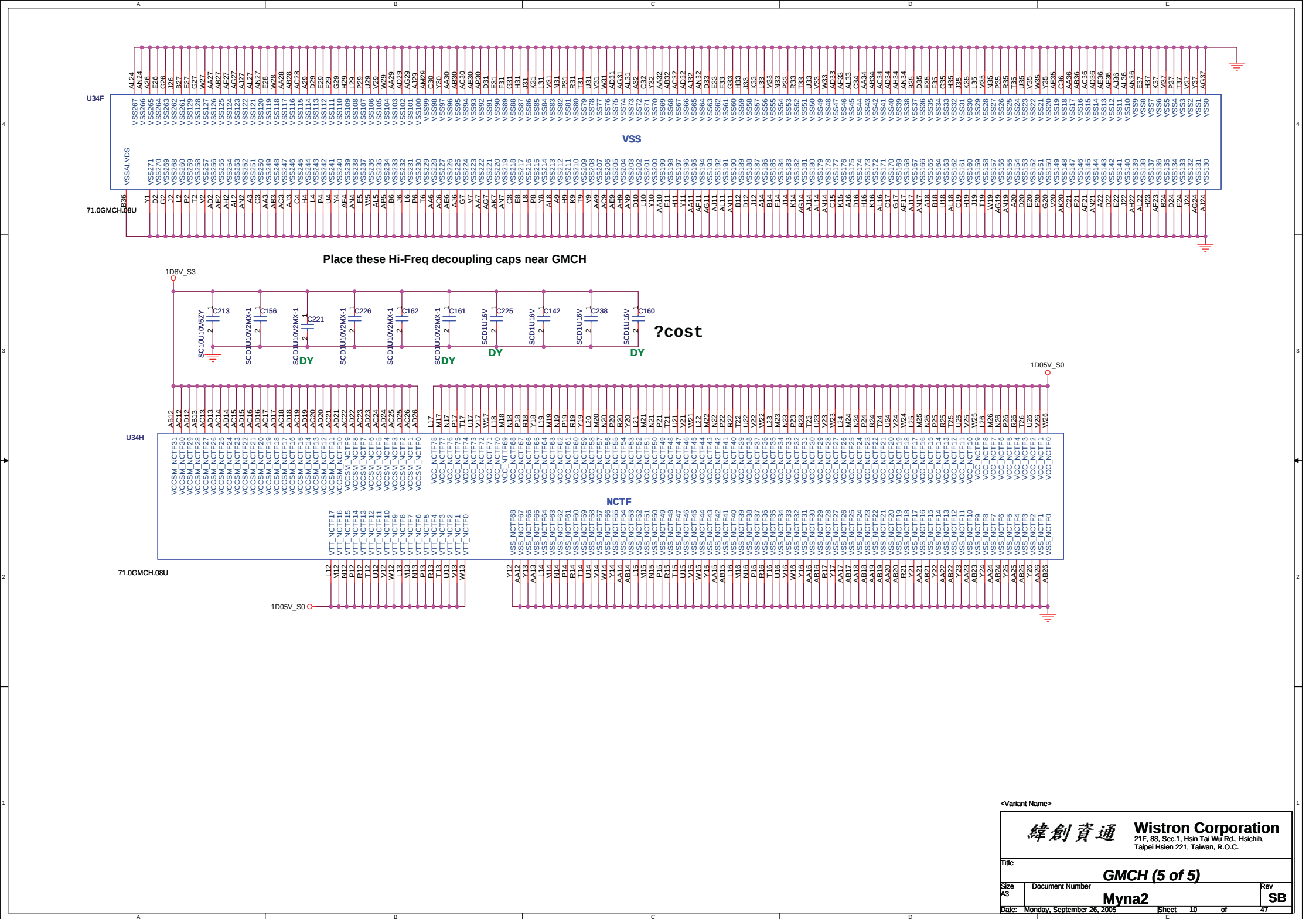


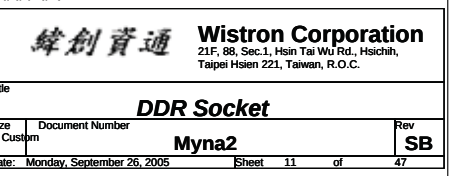




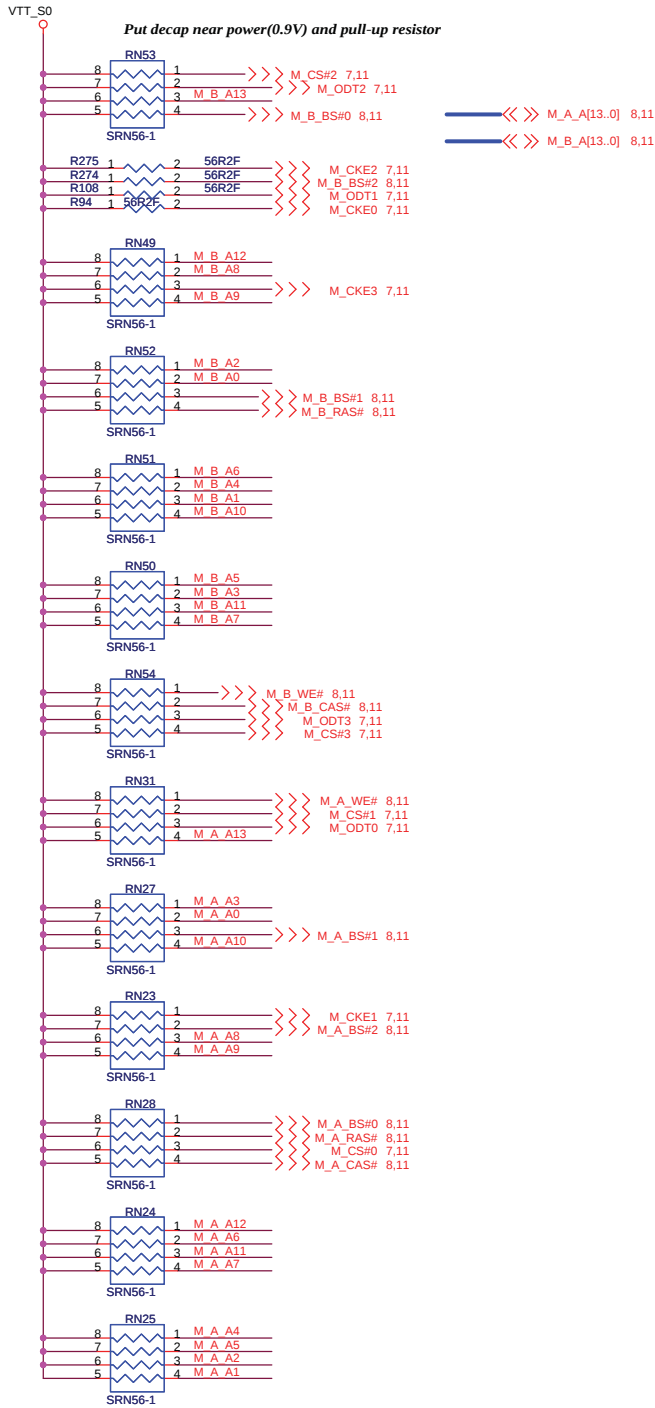




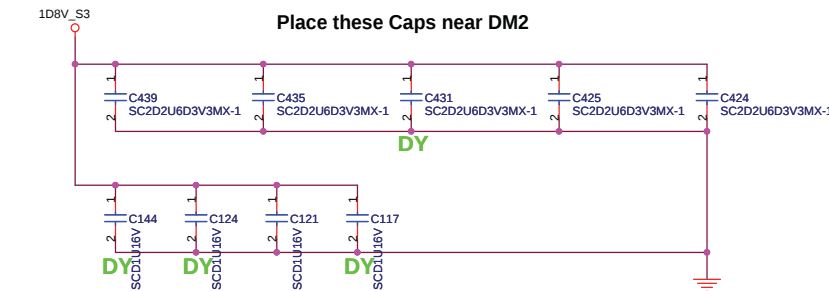
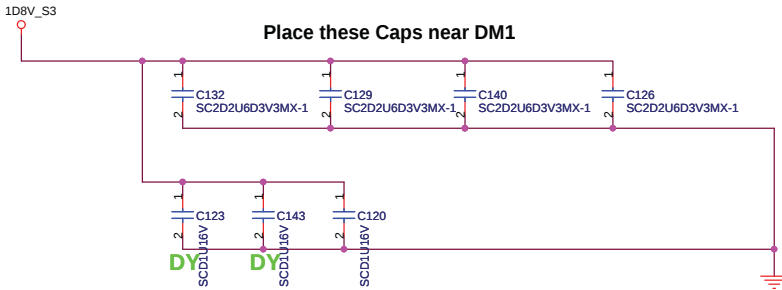
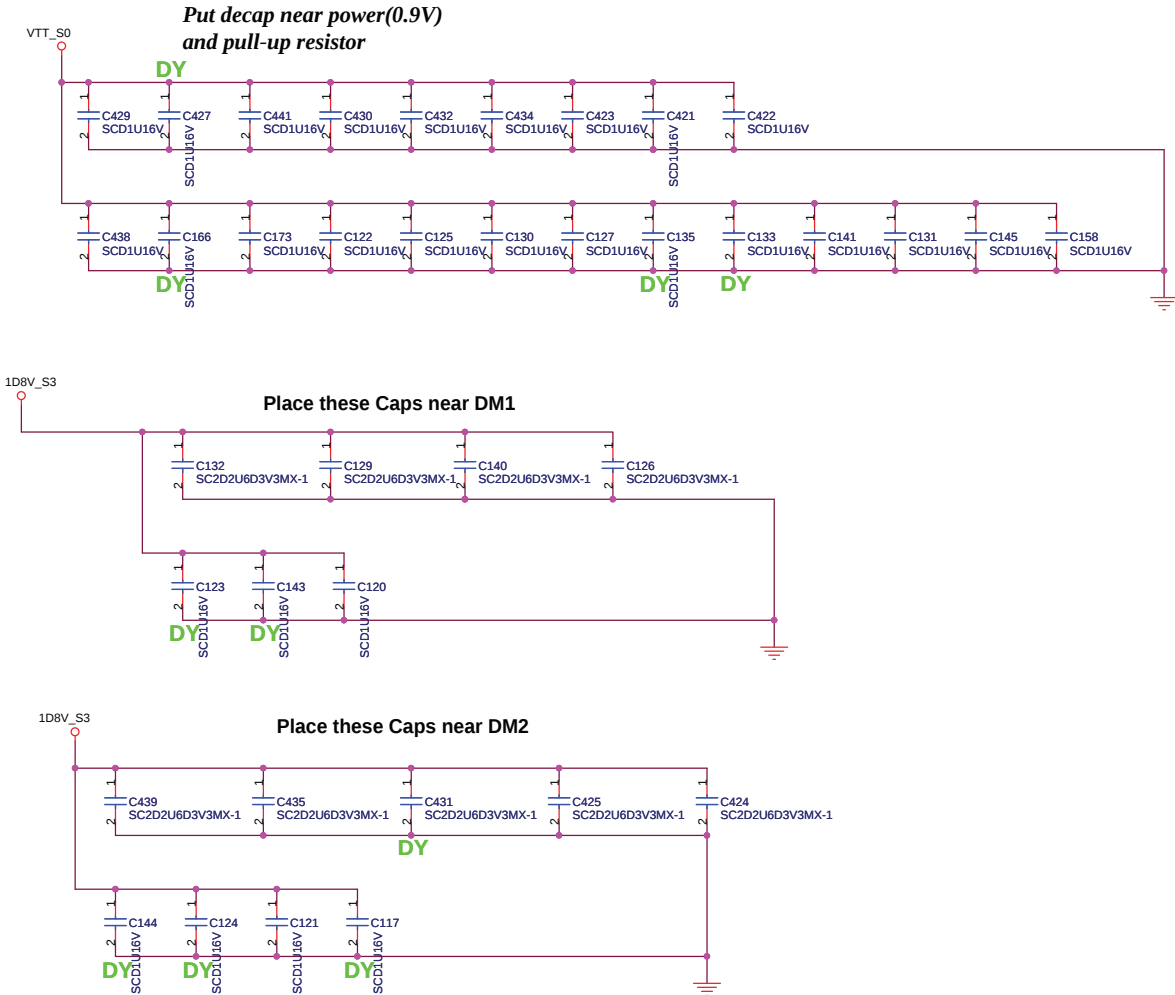


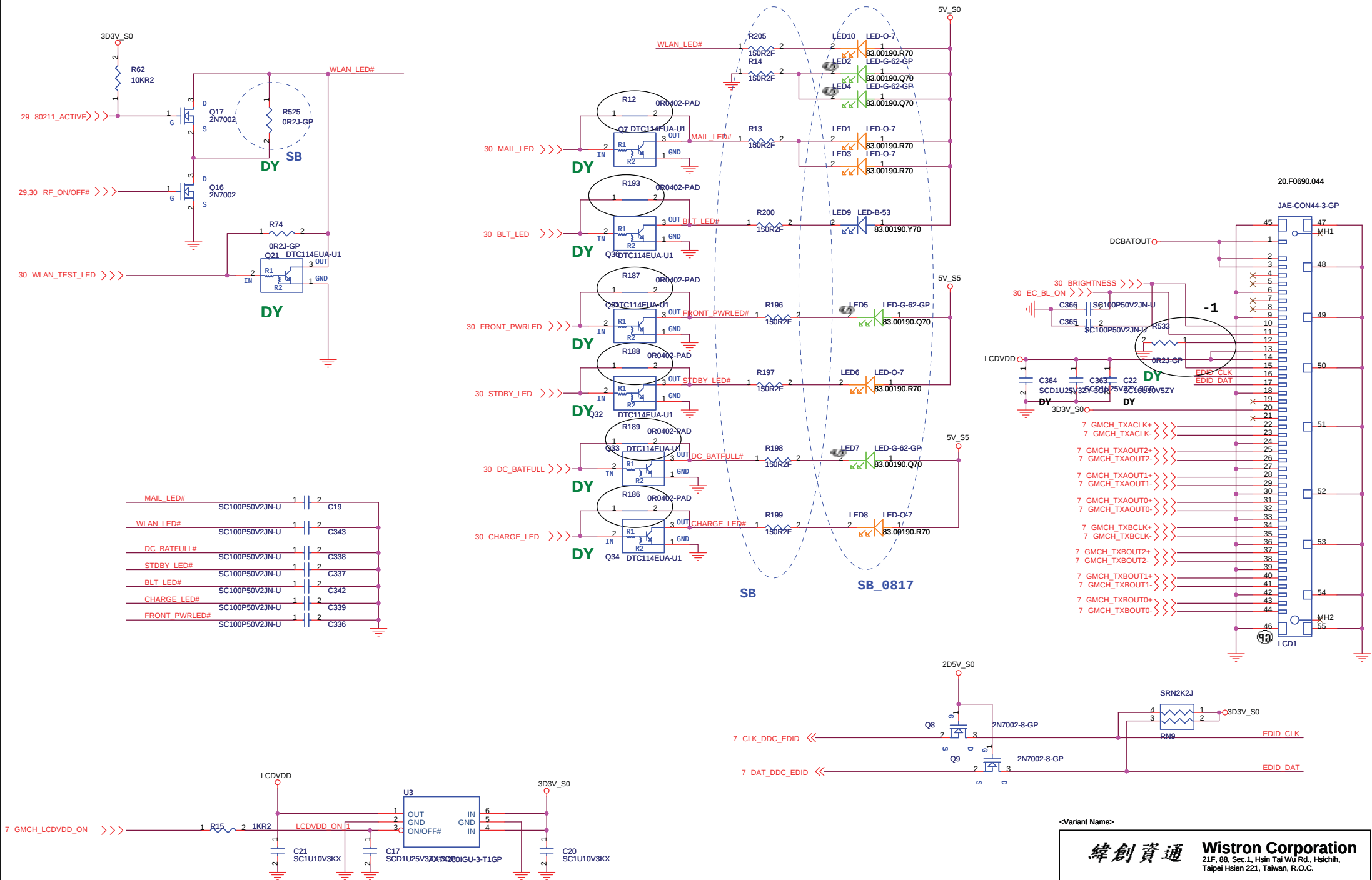


PARALLEL TERMINATION



Decoupling Capacitor

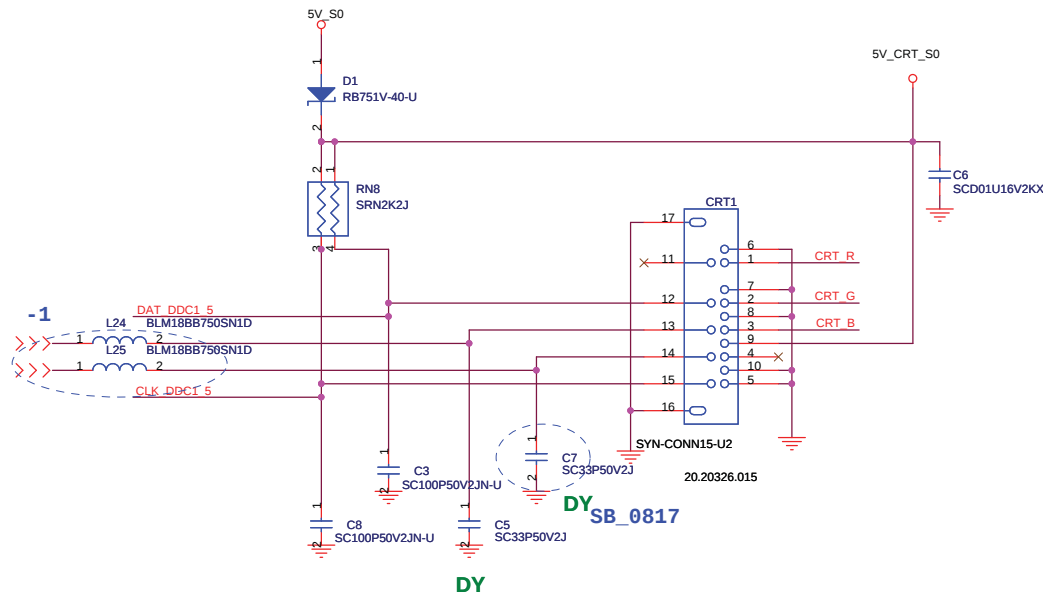
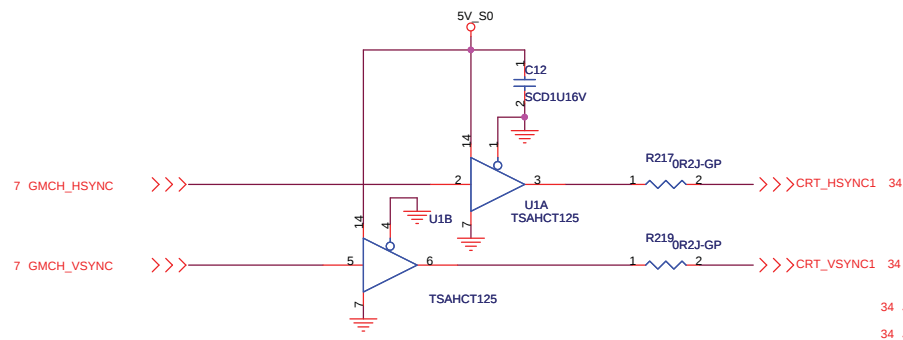
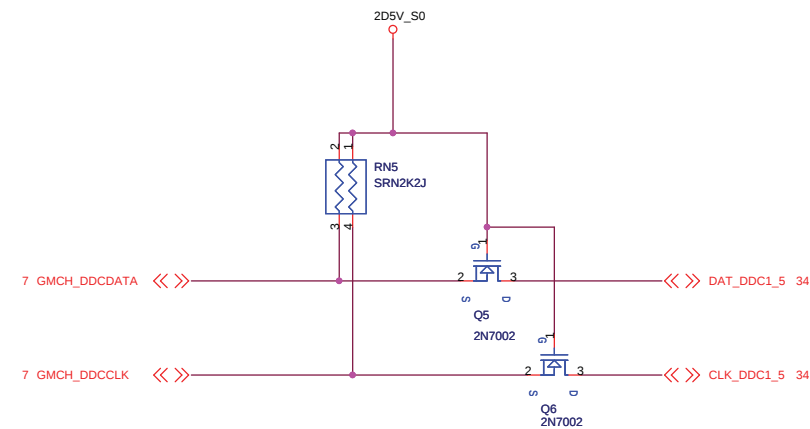
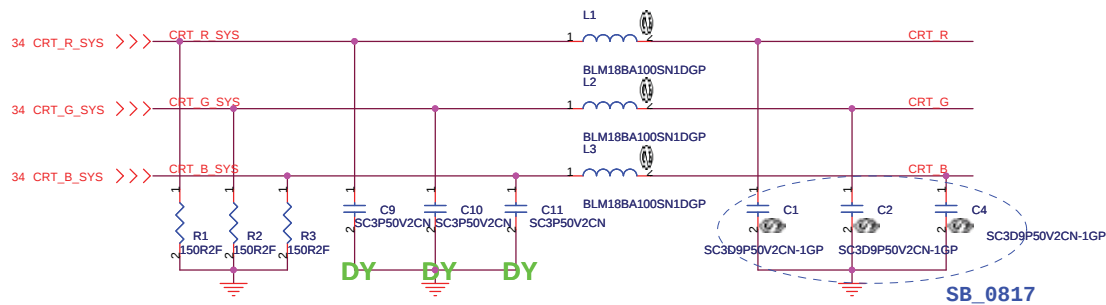




<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title LCD / LEDs		
Size A3	Document Number Myna2	Rev SB
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size
A3

Document Number

Myna2

Rev

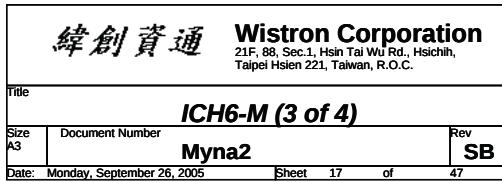
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Date: Monday, September 26, 2005

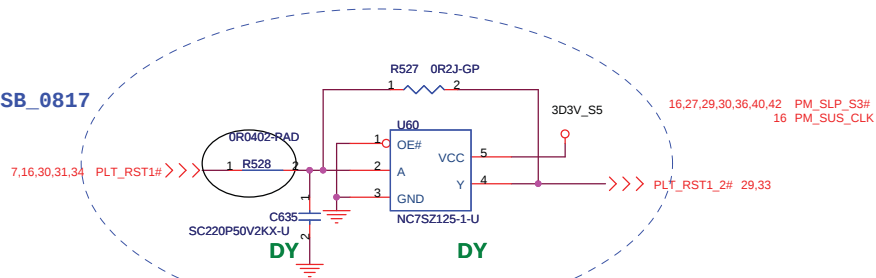
Sheet 14

of

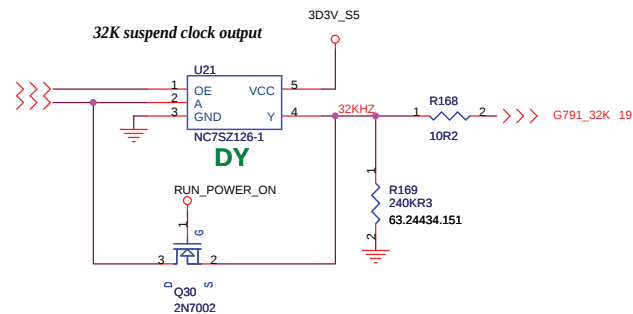
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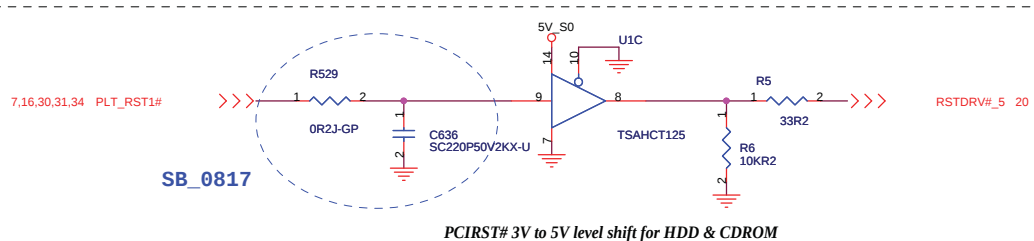
SB_0817



32K suspend clock output

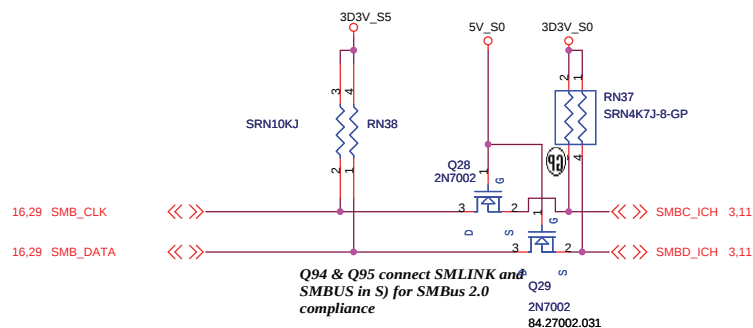


SB_0817

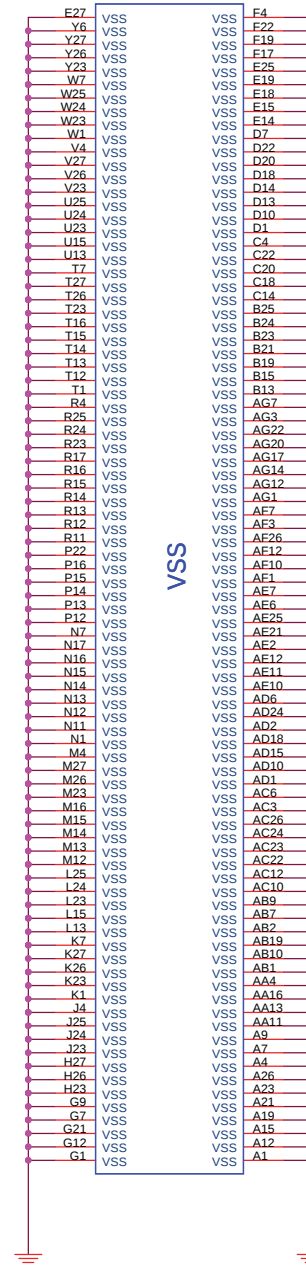


PCIRST# 3V to 5V level shift for HDD & CDROM

SMBUS



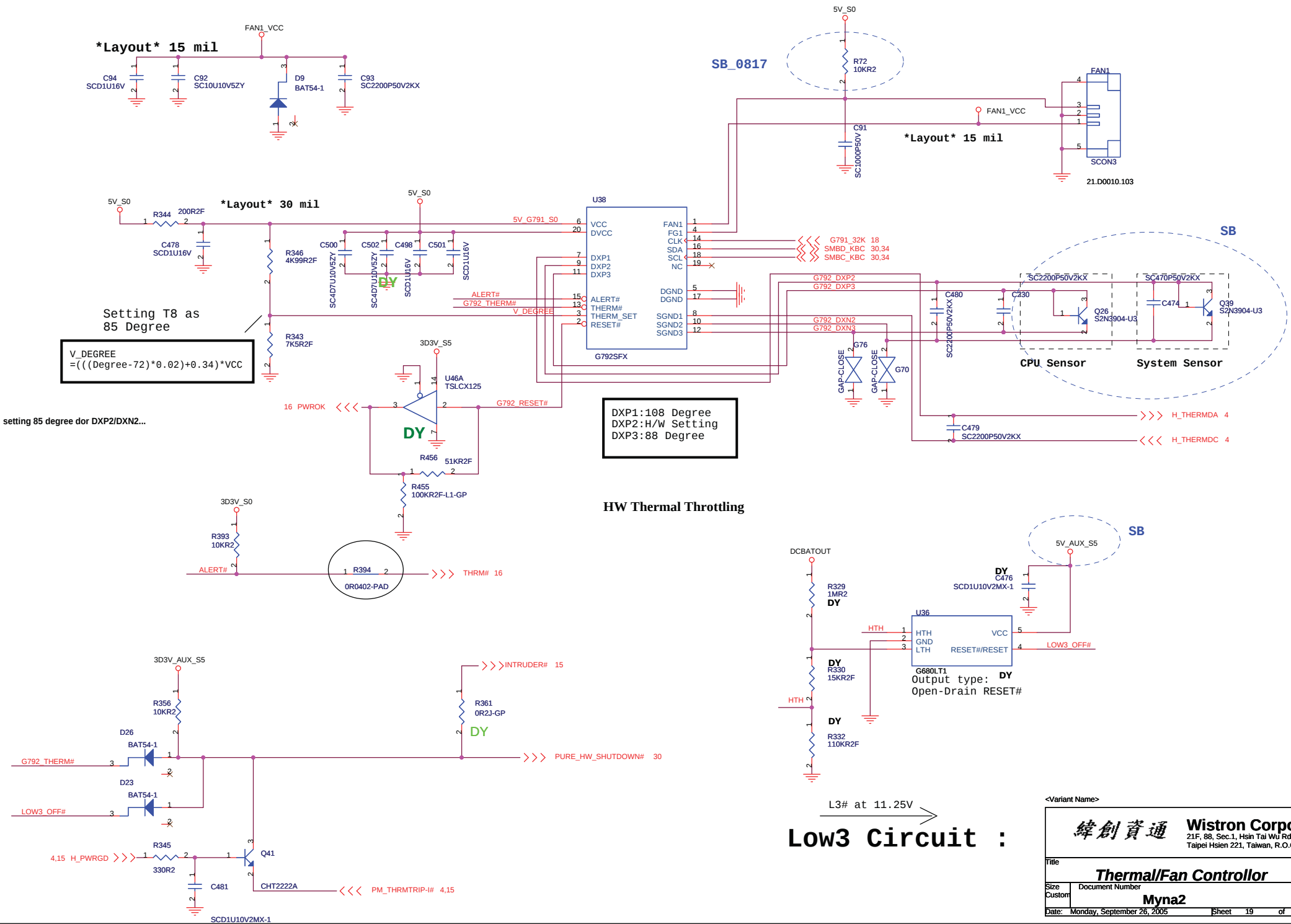
U44D



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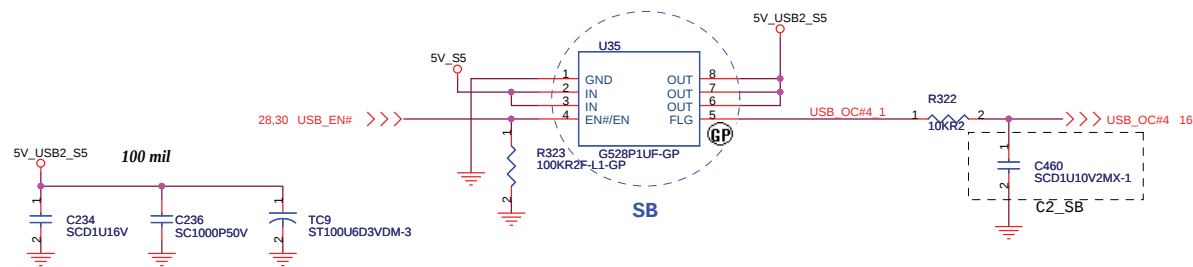
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
ICH6-M (4 of 4)		
Size	Document Number	Rev
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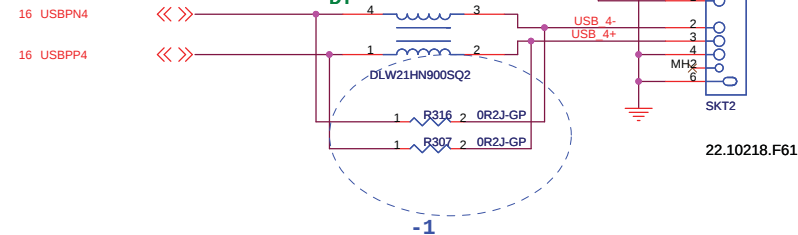
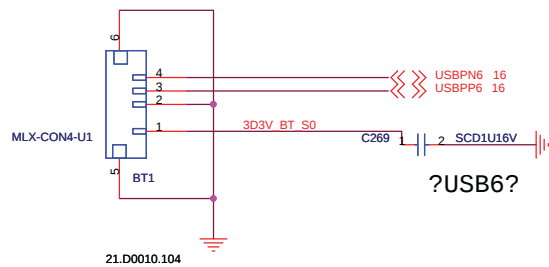
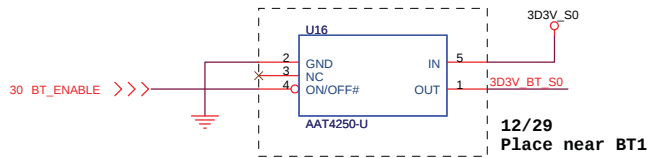


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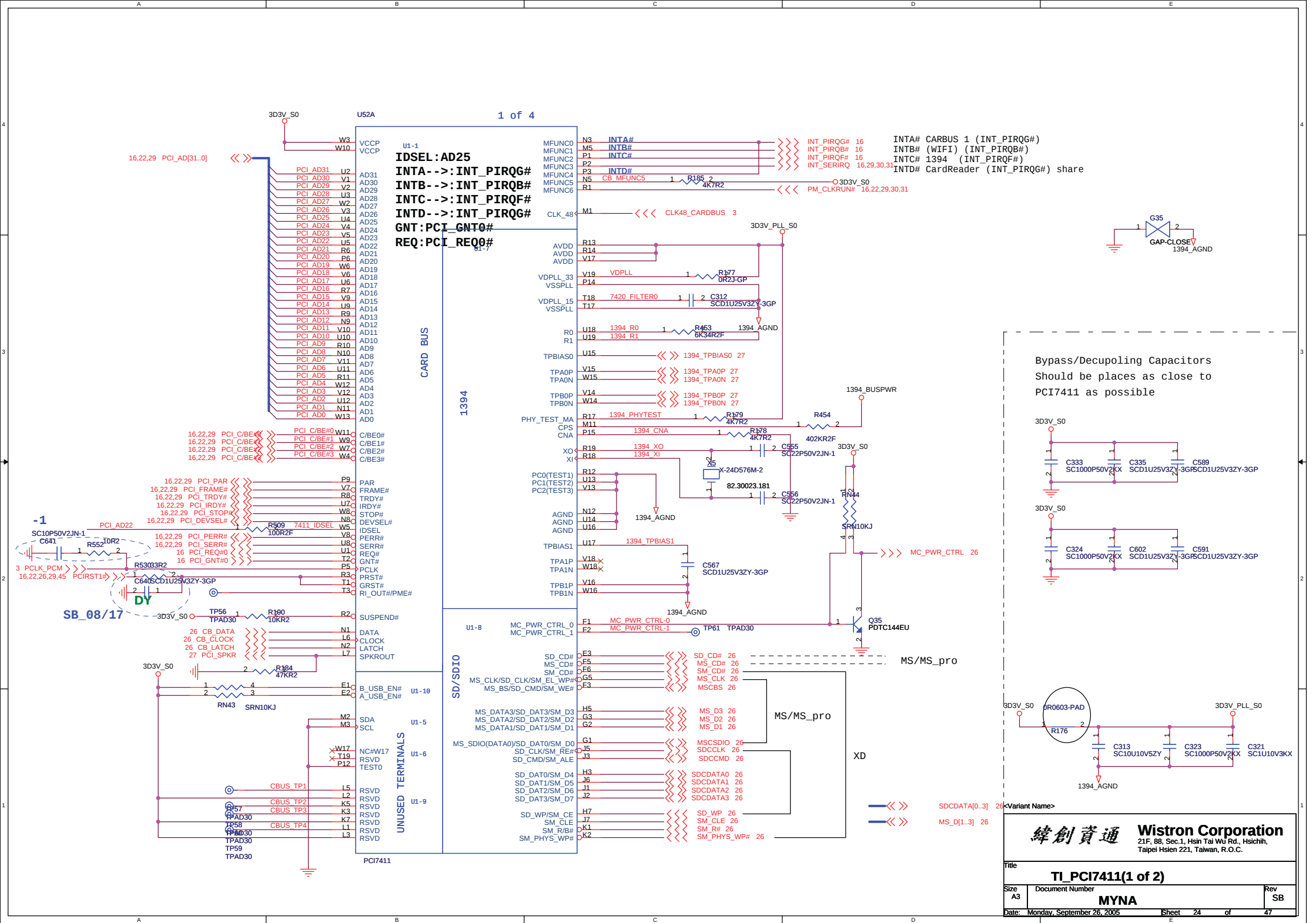
USB PORT

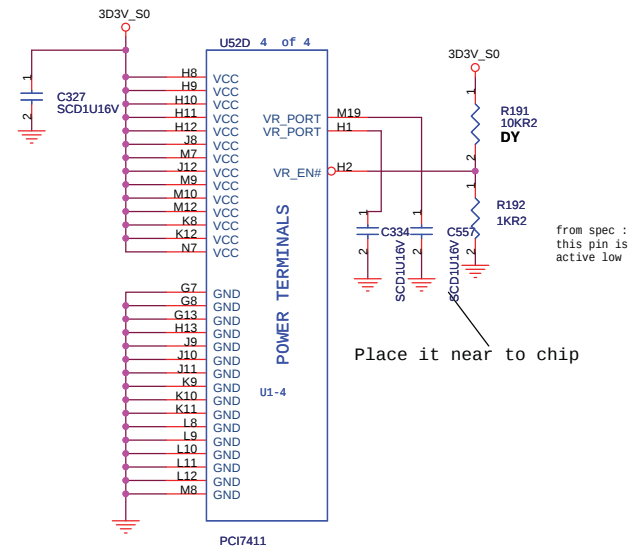
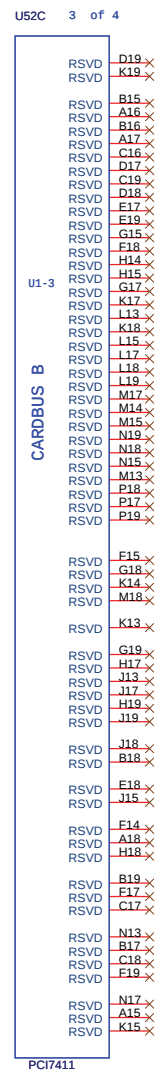
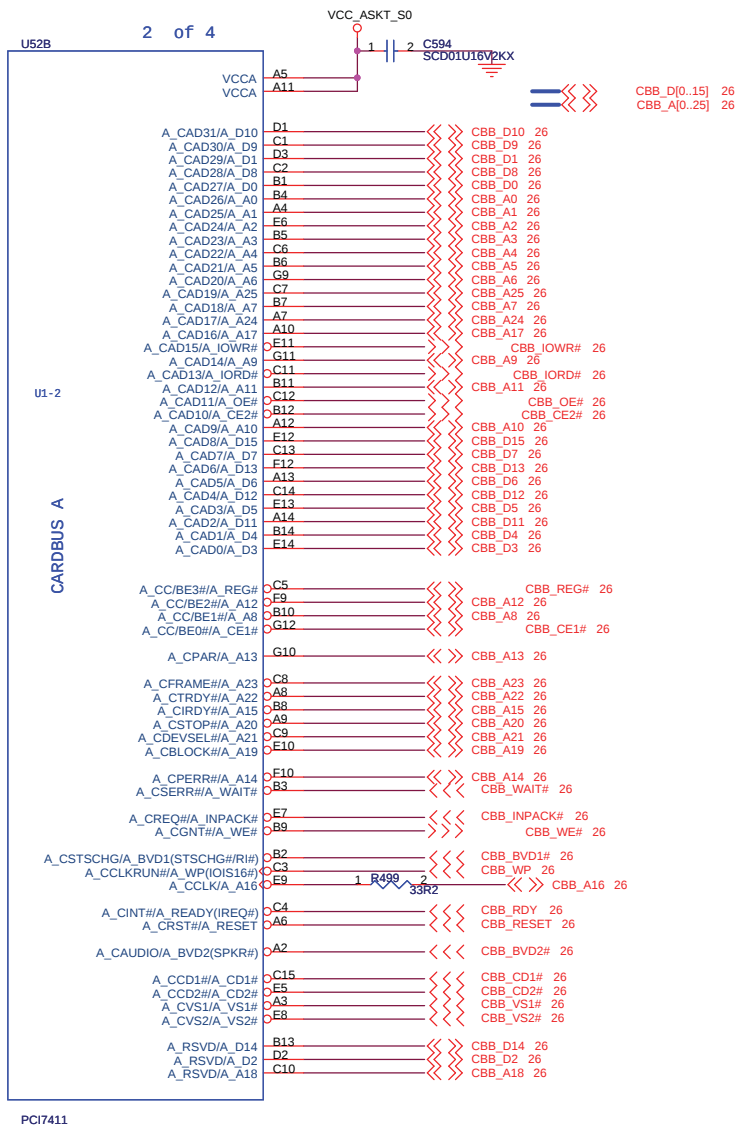


BLUETOOTH MODULE CONNECTOR





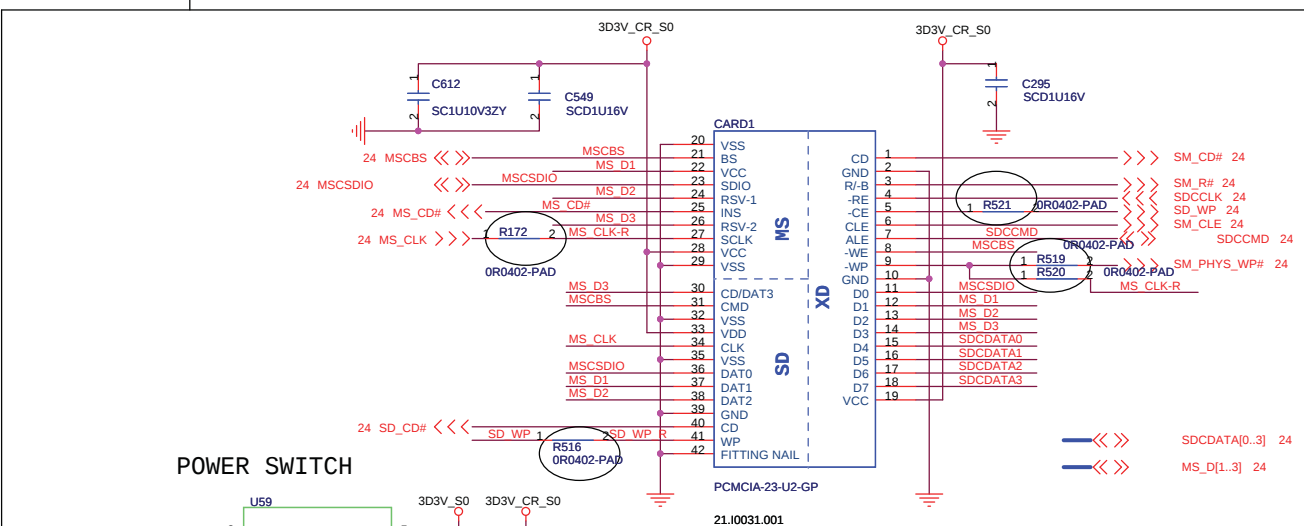
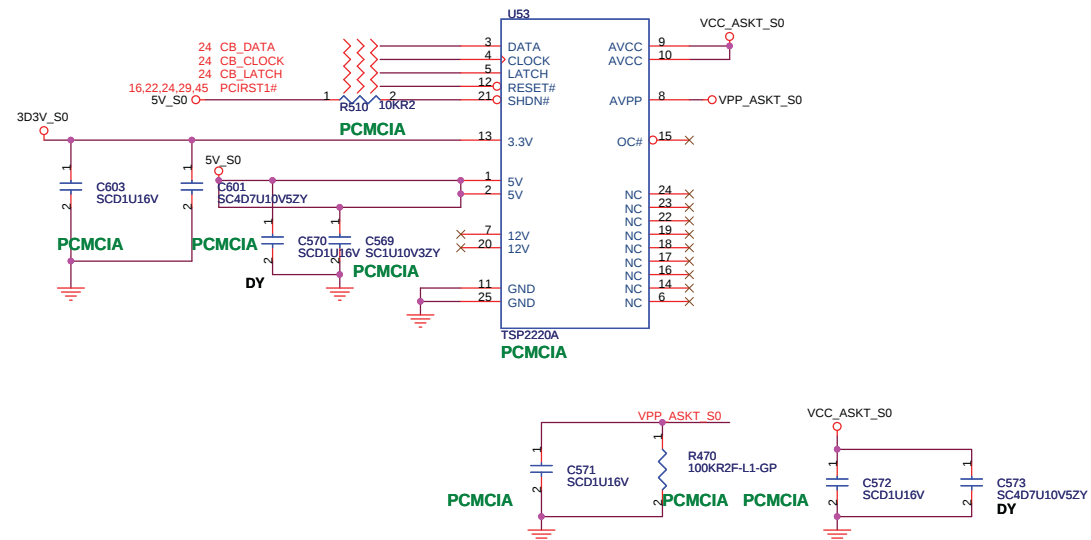
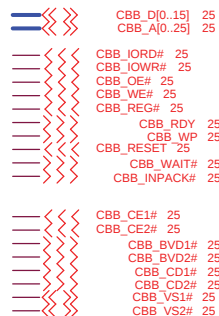
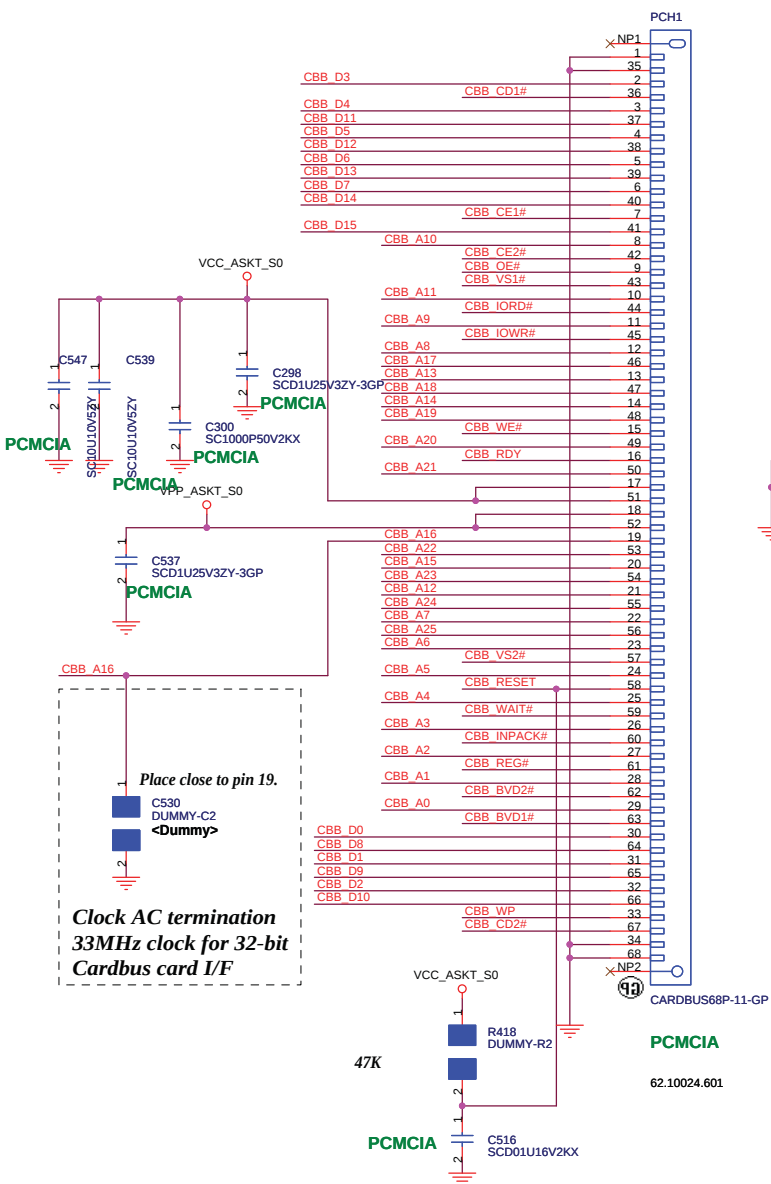




PCMCIA Socket

Cardbus I/F

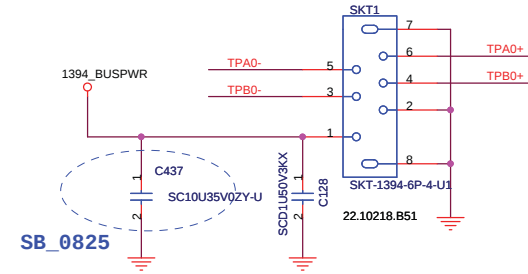
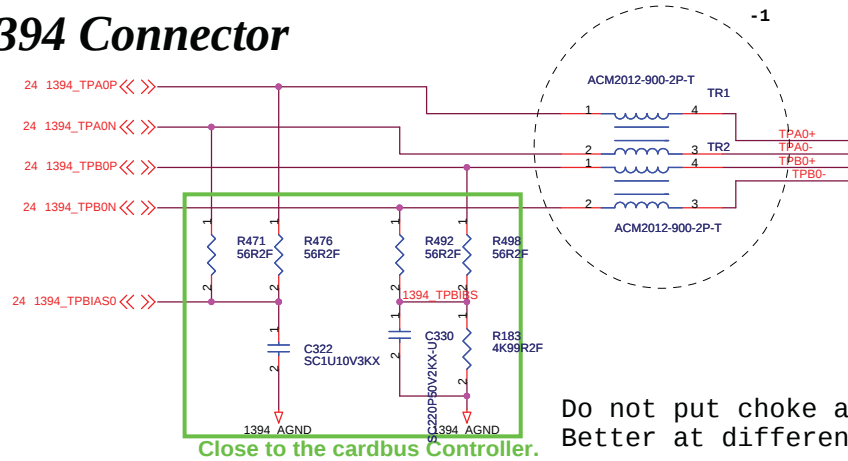
Power switch



POWER SWITCH

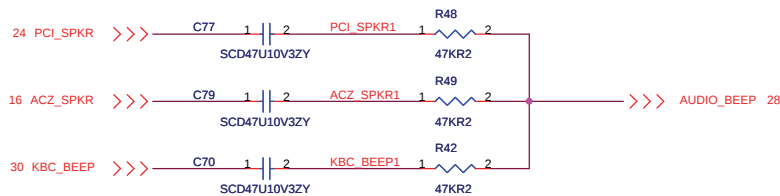
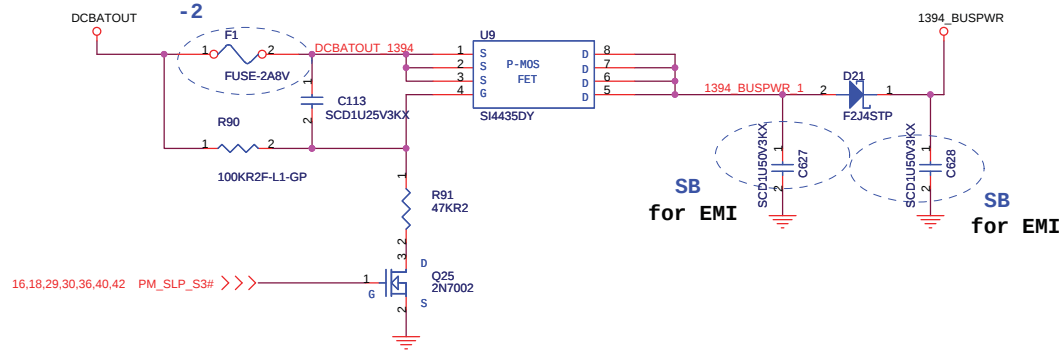
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
PCMCA / 1394 / CARD READER		
Size	Document Number	Rev
A3	Myna2	SB
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1394 Connector



Do not put choke and 0 ohm at same location.
Better at different side.

4/21 External ODD will suck more
than 1.5A when battery mode

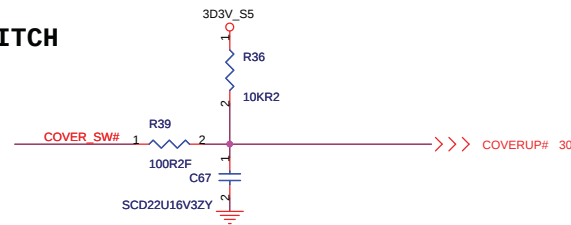


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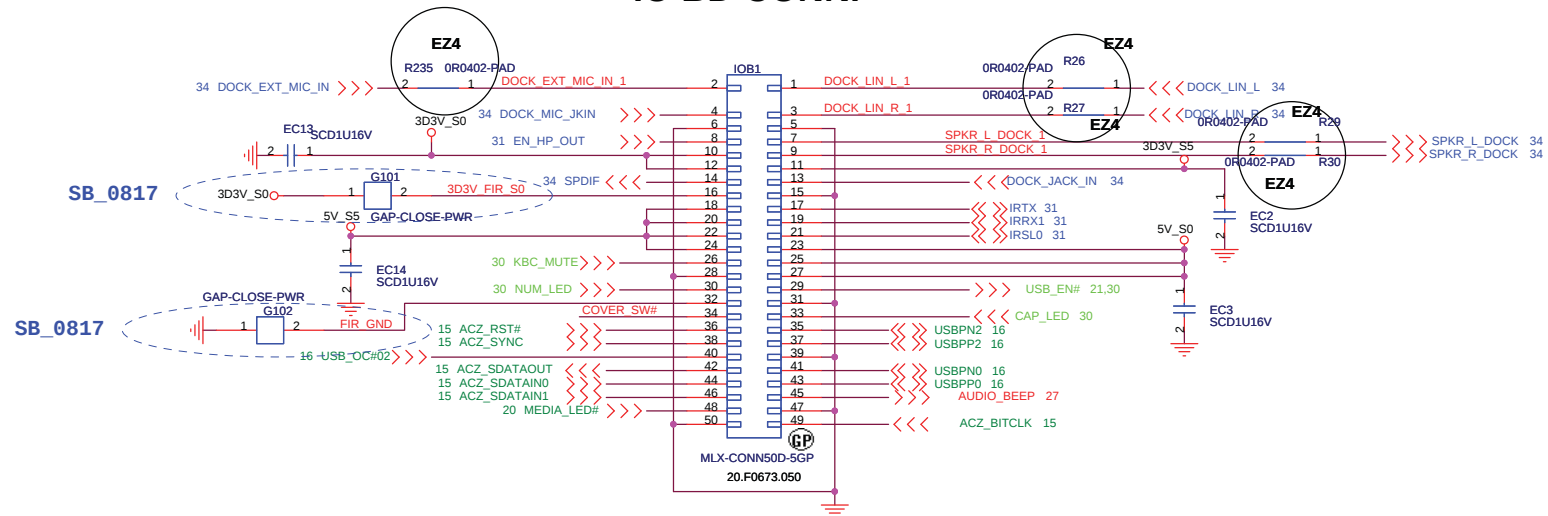
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
1394 Connector		
Size	Document Number	Rev
A3	Myna2	SB
Date:	Monday, September 26, 2005	Sheet 27 of 47

COVER SWITCH



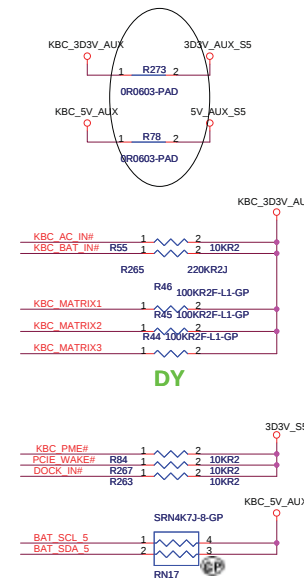
IO BD CONN.



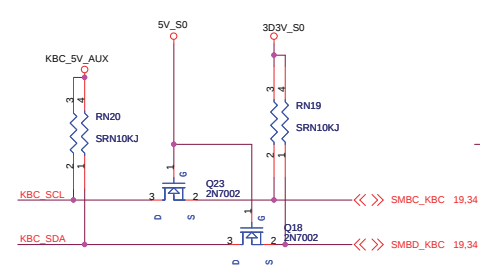
Blue -> Dock or SuperIO
 Light Green -> KBC
 Green -> SouthBridge

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AC'97 CODEC - ALC655			
Size A3	Document Number	Rev	
	Myna2	SB	
Date: Monday, September 26, 2005		Sheet 28 of 47	



71.64211.00G

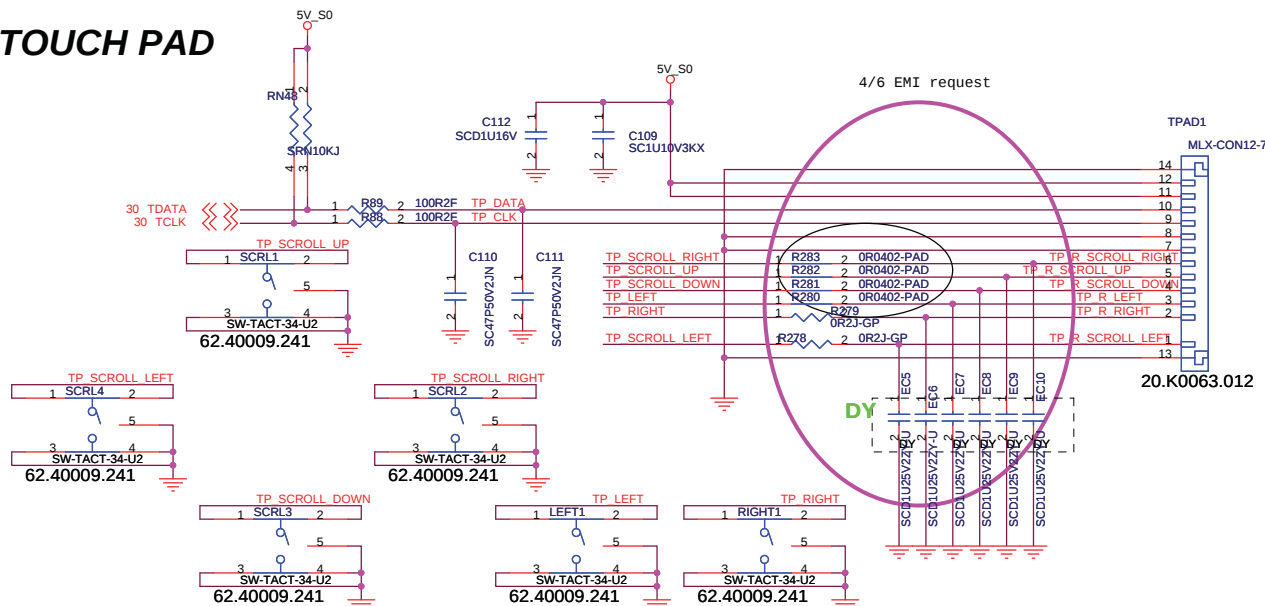
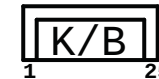


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Title			
KBC H8			
Size	Document Number	Rev	
Custom	Myna2	SB	
Date:	Monday, September 26, 2005	Sheet	30 of 47

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EMI CAPS



? if use Debug Board, remove this R

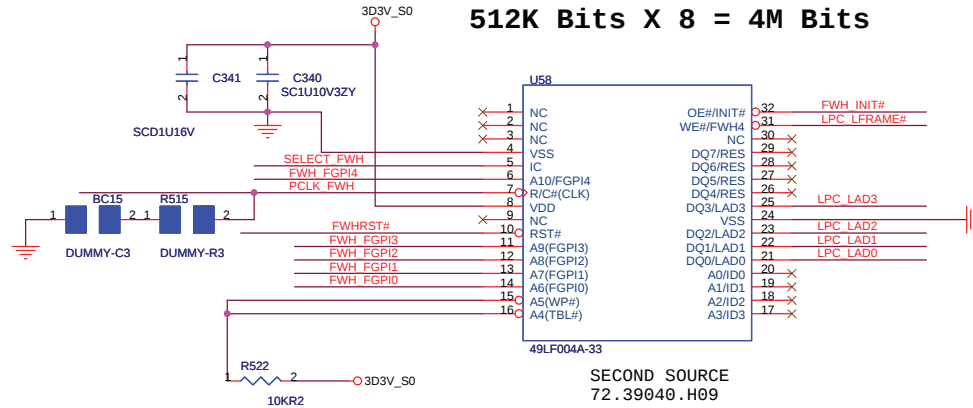
V

Unused FGPI pins must not be float

SB_0817

FLASH ROM

512K Bits X 8 = 4M Bits



SECOND SOURCE
72.39040.H09

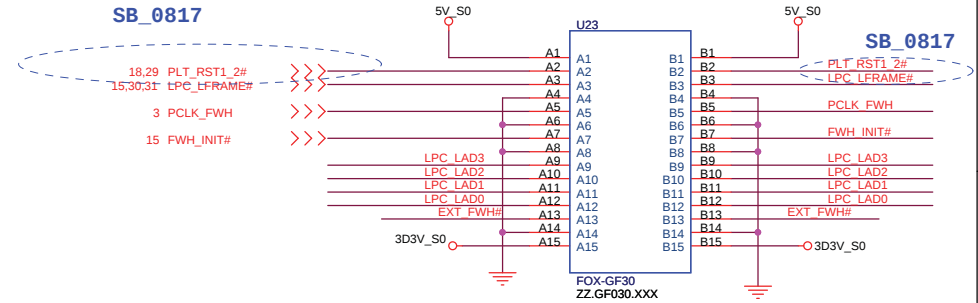
15,30,31 LPC_LAD[0:3] << >>

TOP VIEW

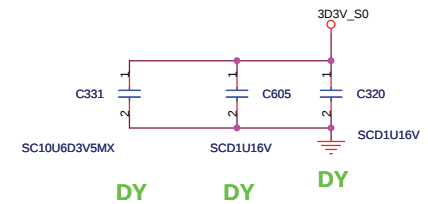
A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

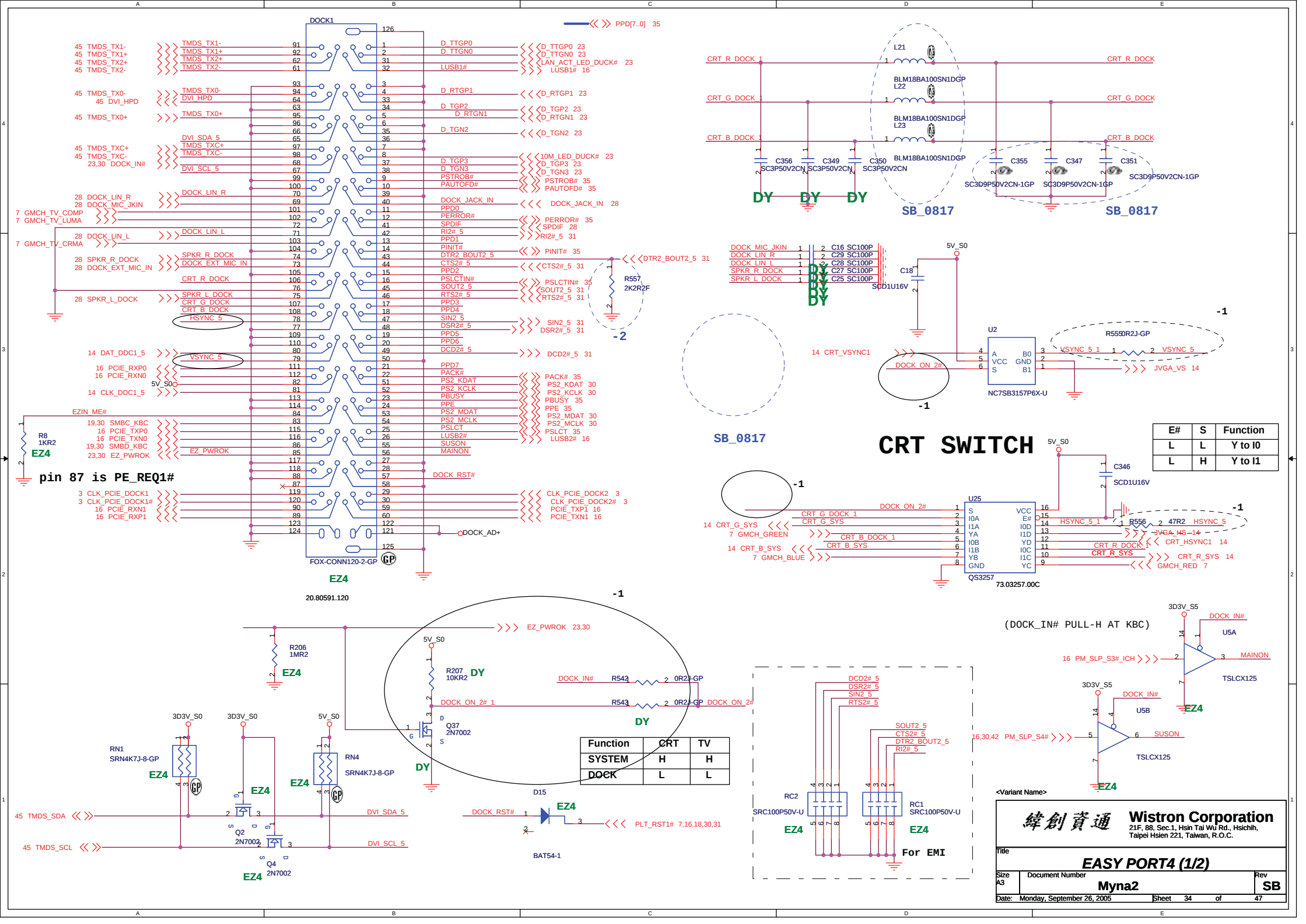
GOLDEN FINGER FOR DEBUG BOARD



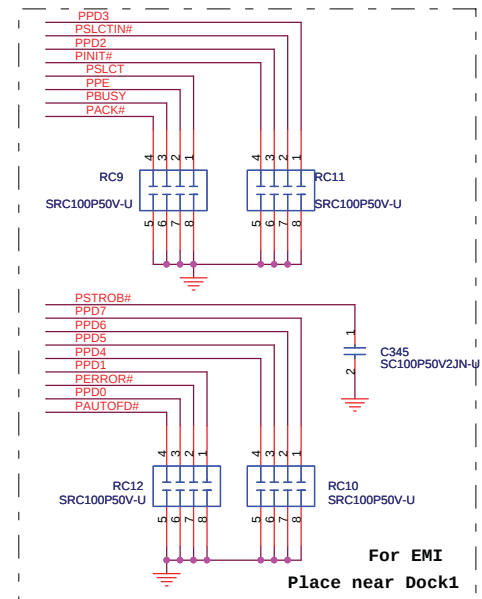
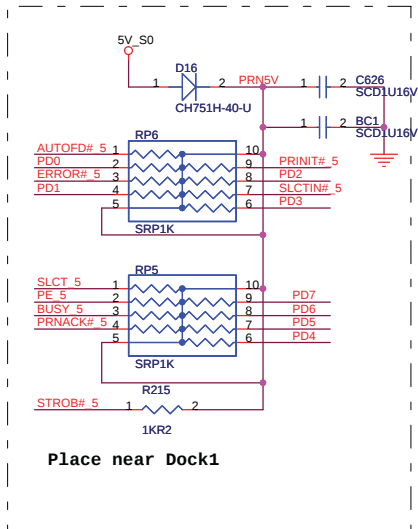
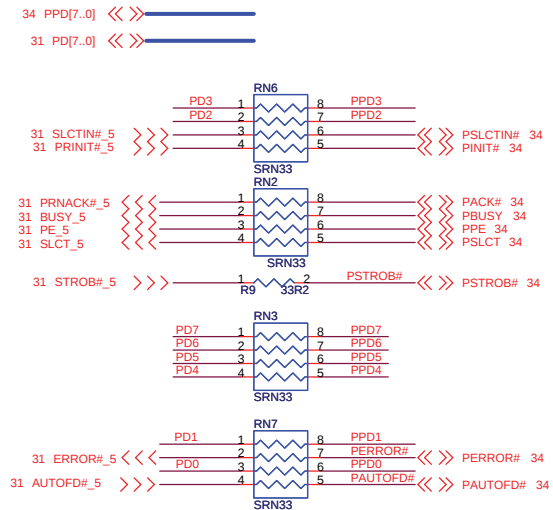
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

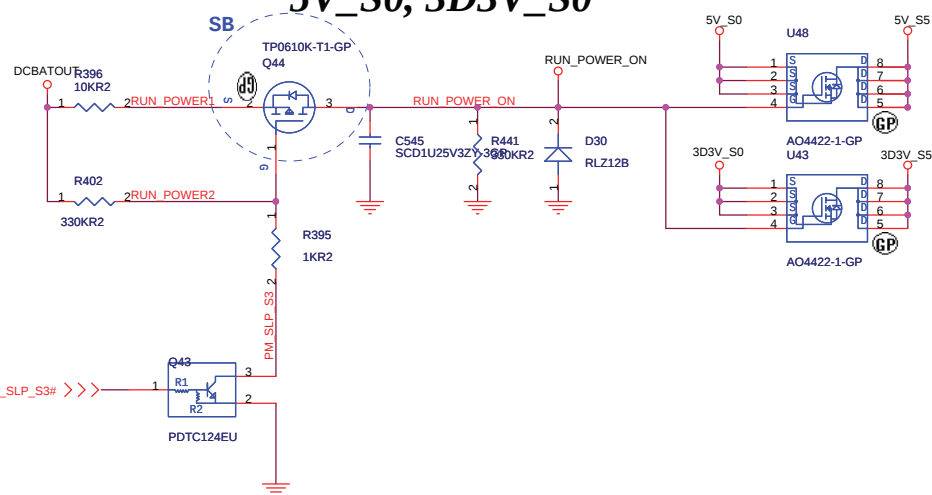


<Variant Name>



PRINT PORT





緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

RUN Power

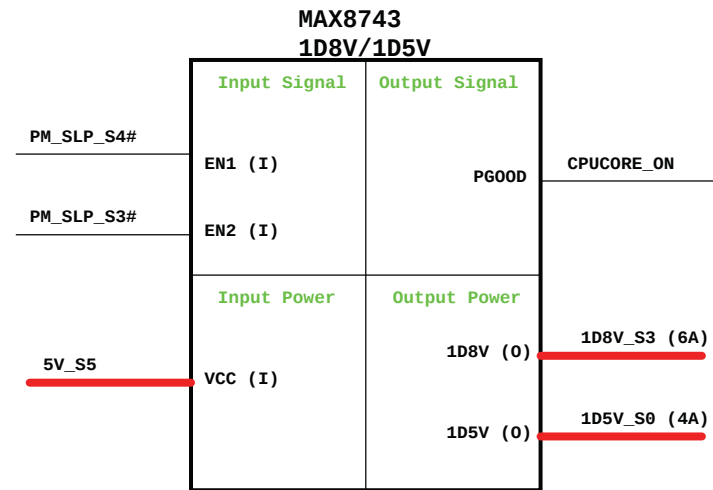
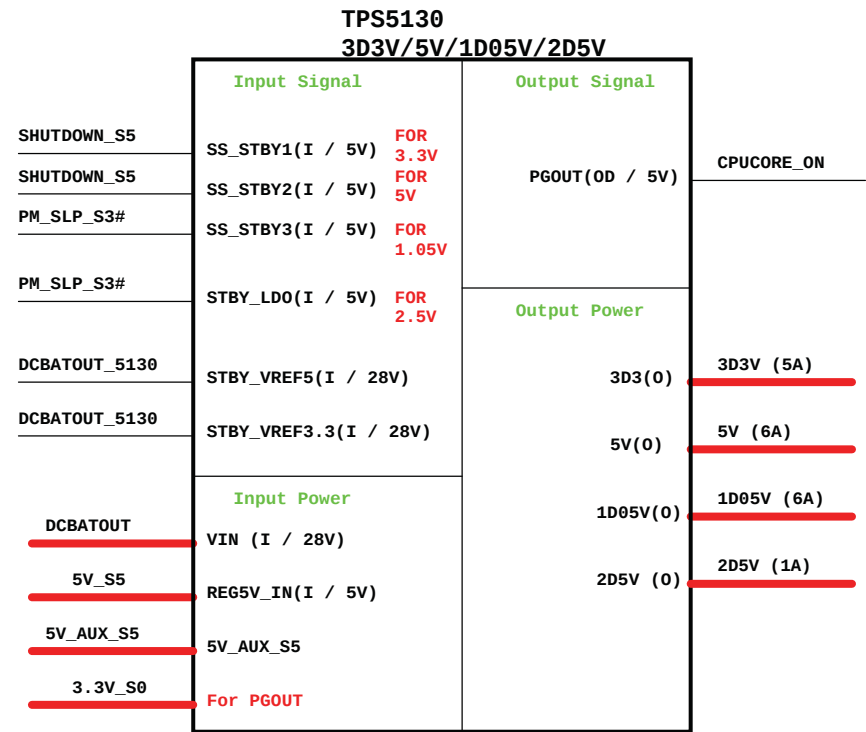
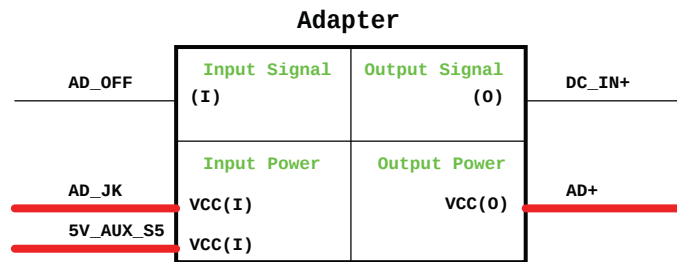
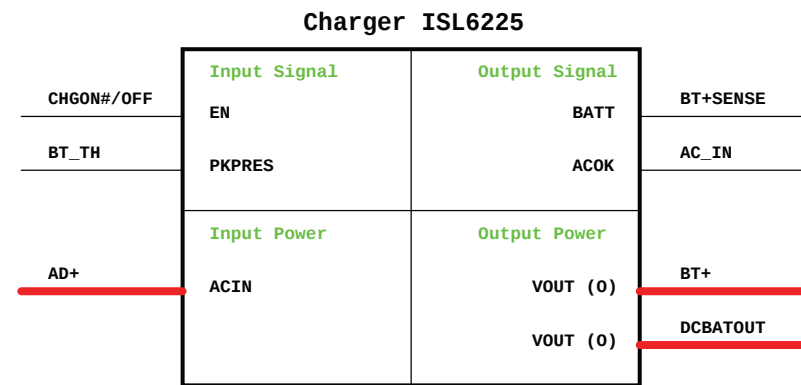
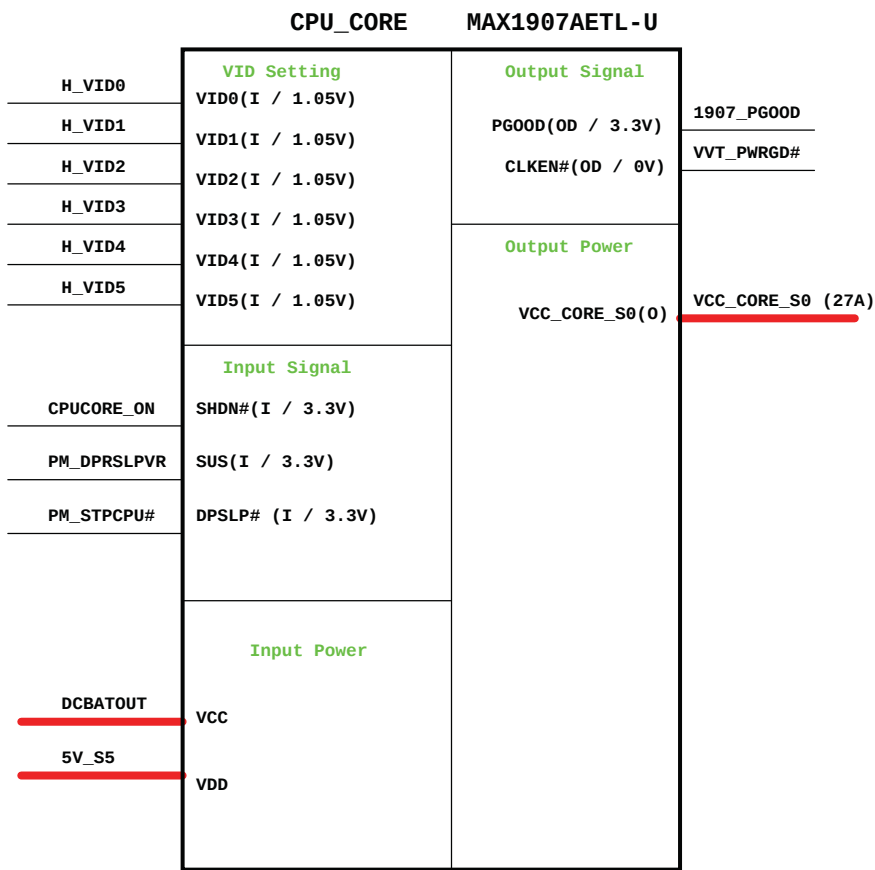
Document Number

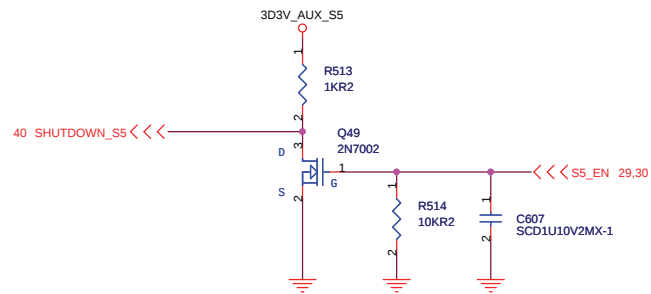
Myna2

Document Number: **Myn2**

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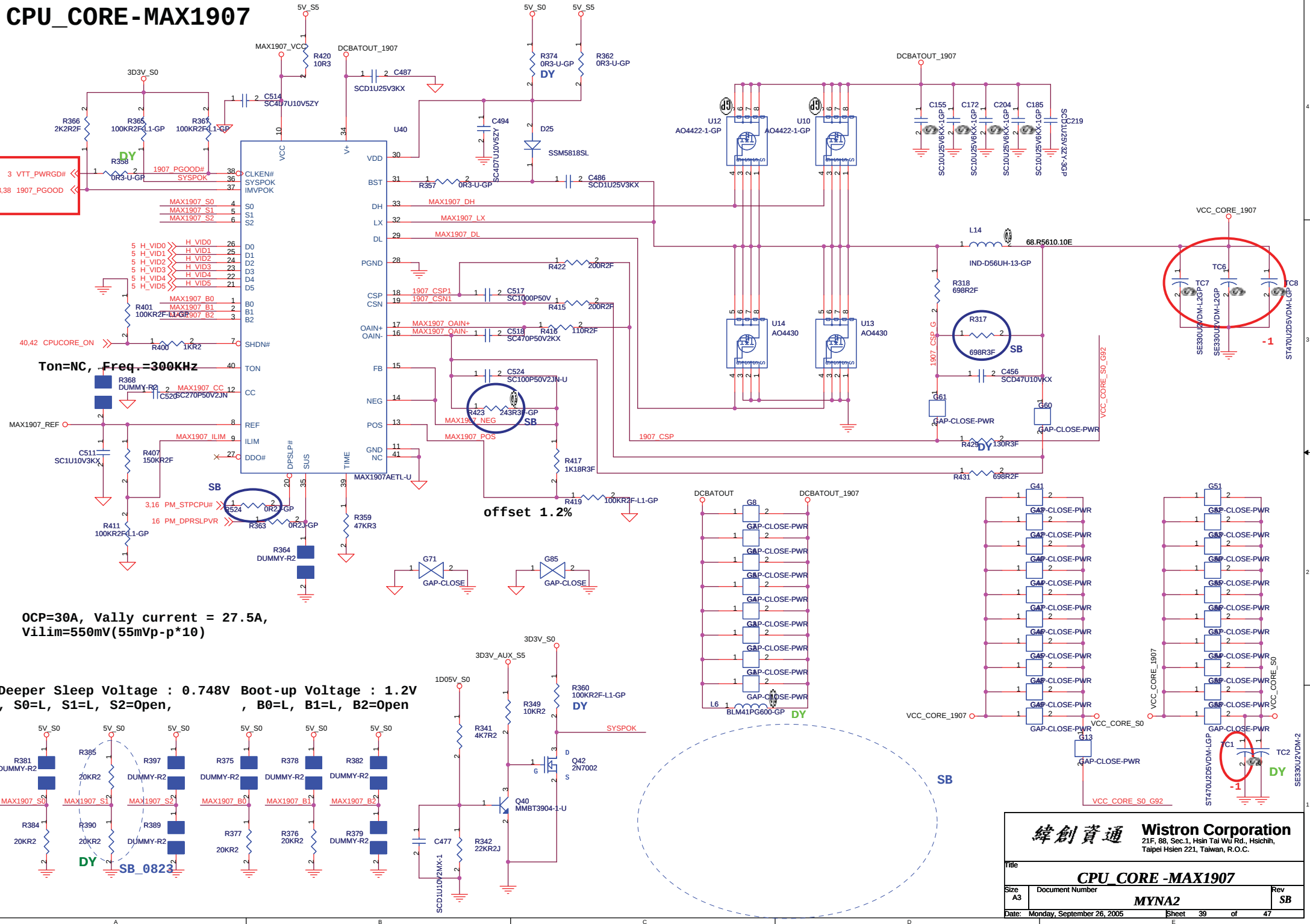


PWRGD for NB and SB



<Variant Name>			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
POWER ON CIRCUIT			
Size	Document Number		Rev
A3	Myna2		SB
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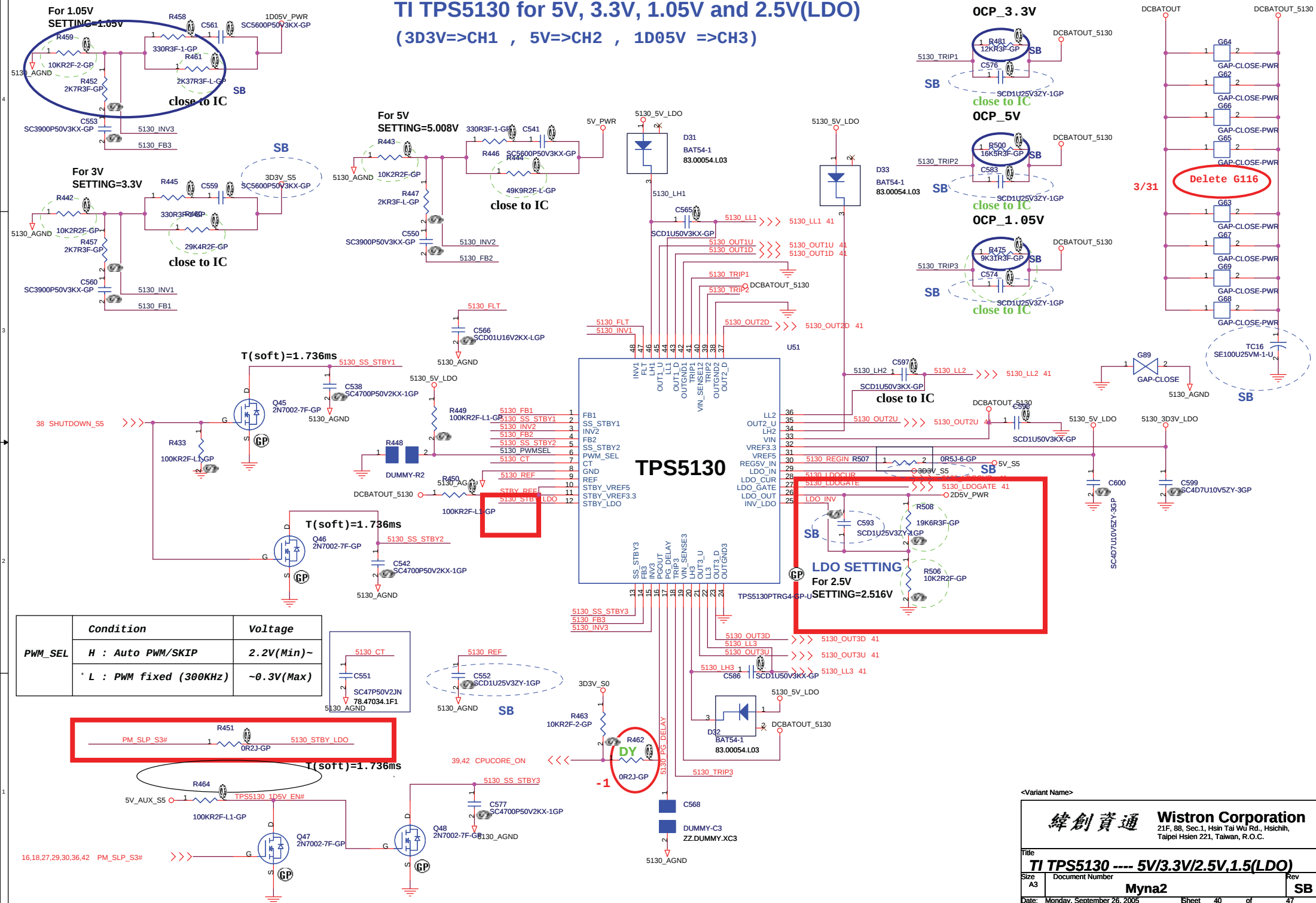
CPU_CORE-MAX1907



緯創資通 **Wistron Corporation**
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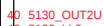
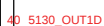
Title			
CPU_CORE -MAX1907			
Size A3	Document Number		Rev
	MYNA2		SB
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TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO) (3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)

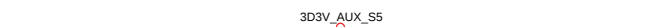


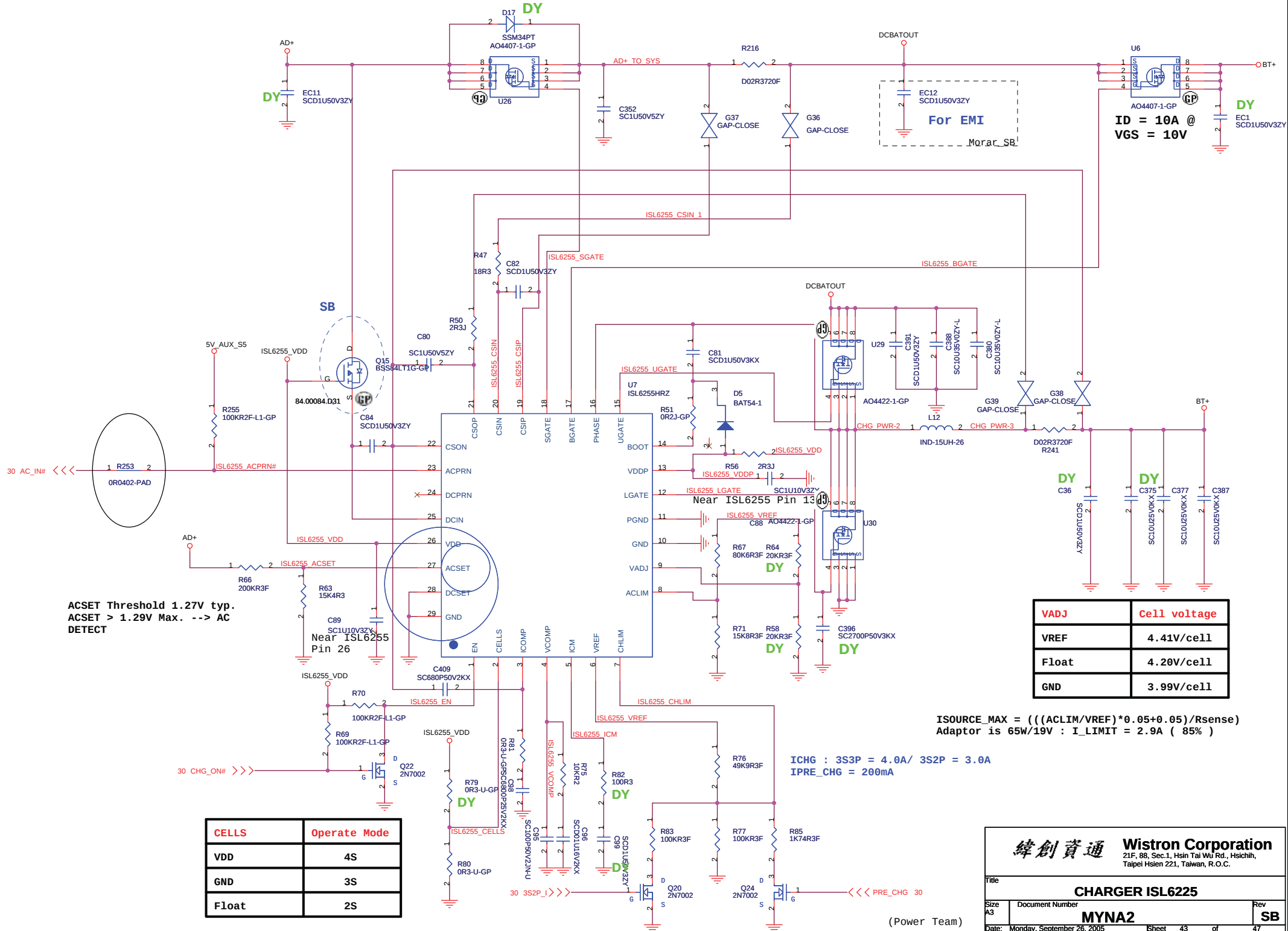
	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)



Aux Power





ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

ICHG : 3S3P = 4.0A/ 3S2P = 3.0A
IPRE_CHG = 200mA

緯創資通

Wistron Corporation

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Title

CHARGER ISL6225

Size A3

Document Number

Rev

Date: Monday, September 26, 2005

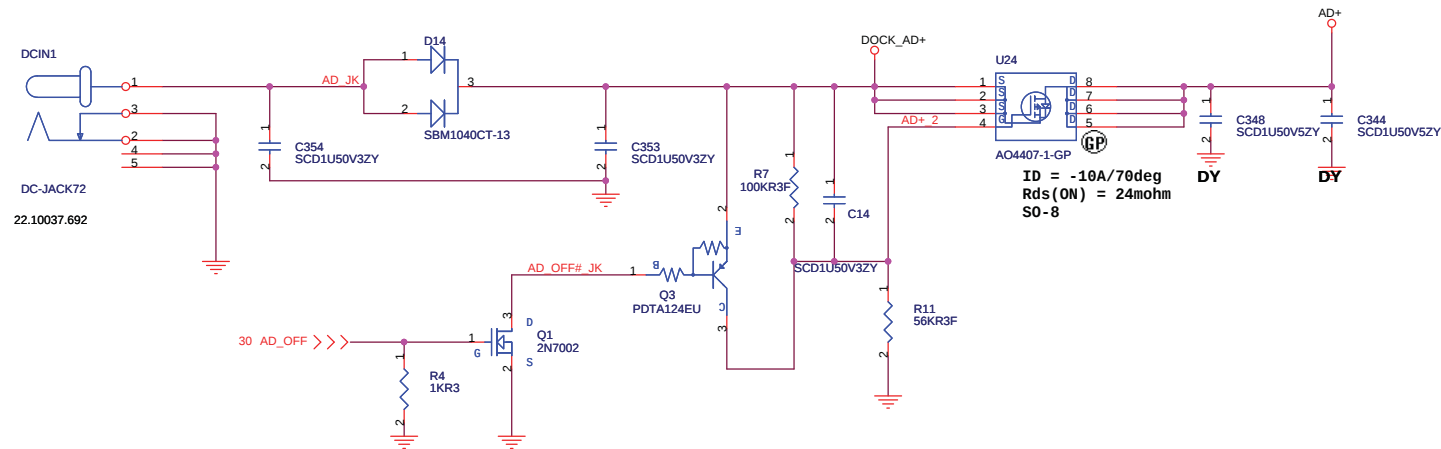
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MYNA2

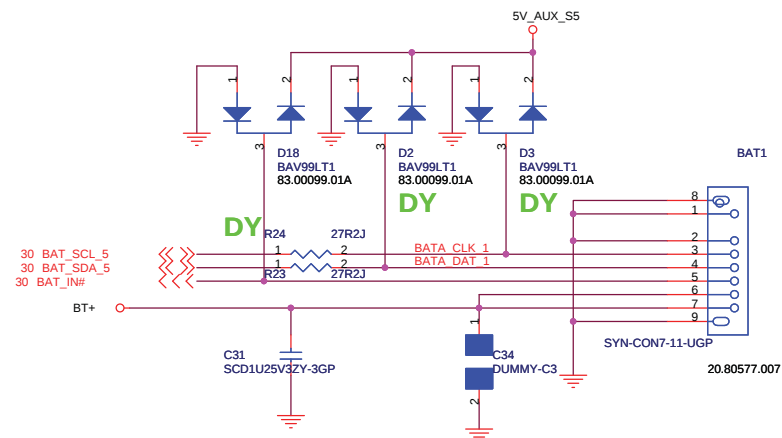
SB

(Power Team)

Adaptor in to generate DCBATOUT

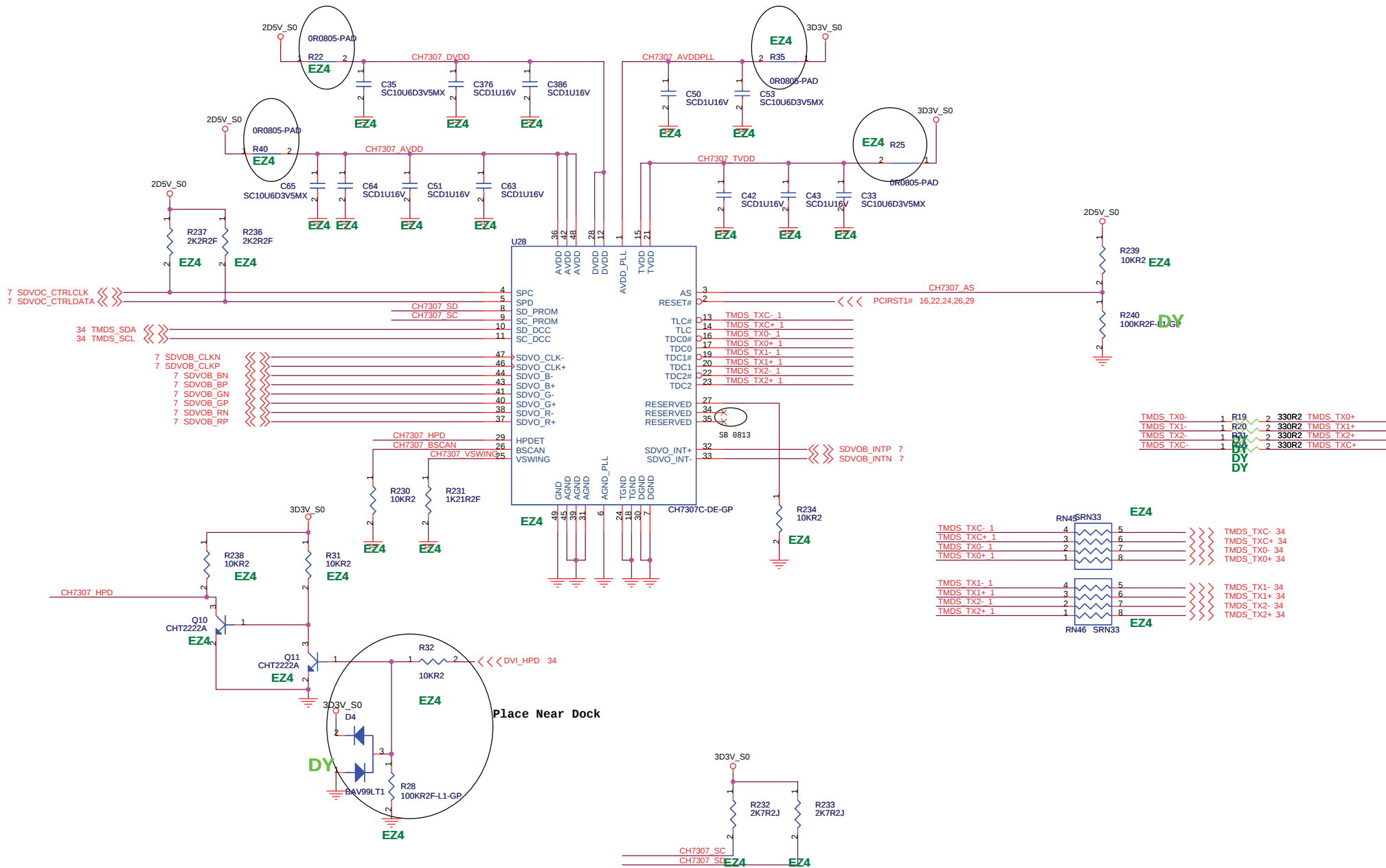


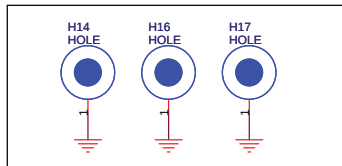
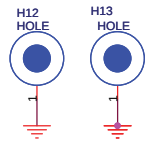
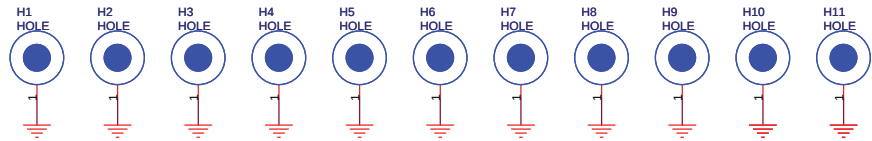
BATTERY CONNECTOR



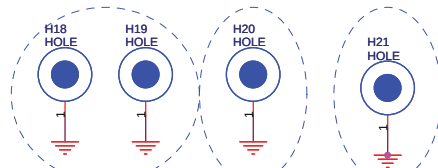
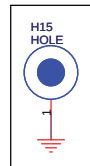
<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AD/BAT CONN			
Size A3	Document Number Myna2		Rev SB
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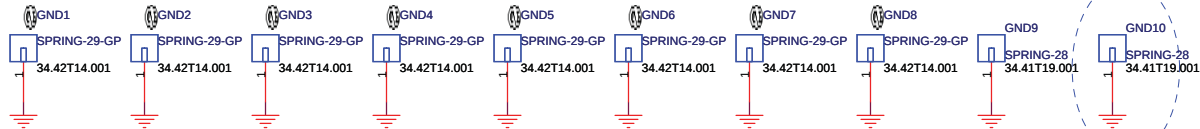
for cpu



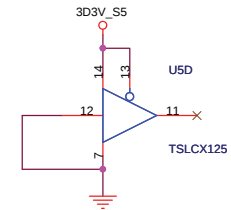
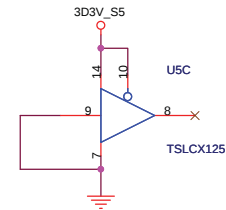
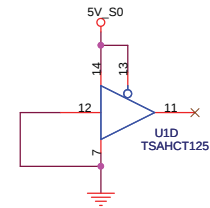
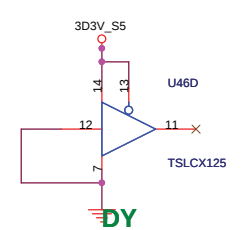
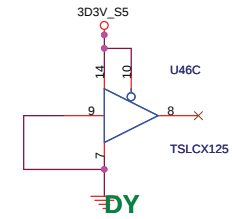
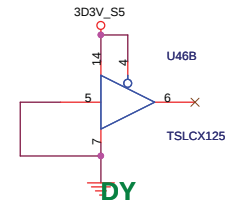
SB

SB_0817

-1



-1



<Variant Name>

緯創資通 Wistron Corporation
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Title		SPRING,BOSS & UNUSED TTL	
Size	Document Number	Rev	SB
A3	Myna2		
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