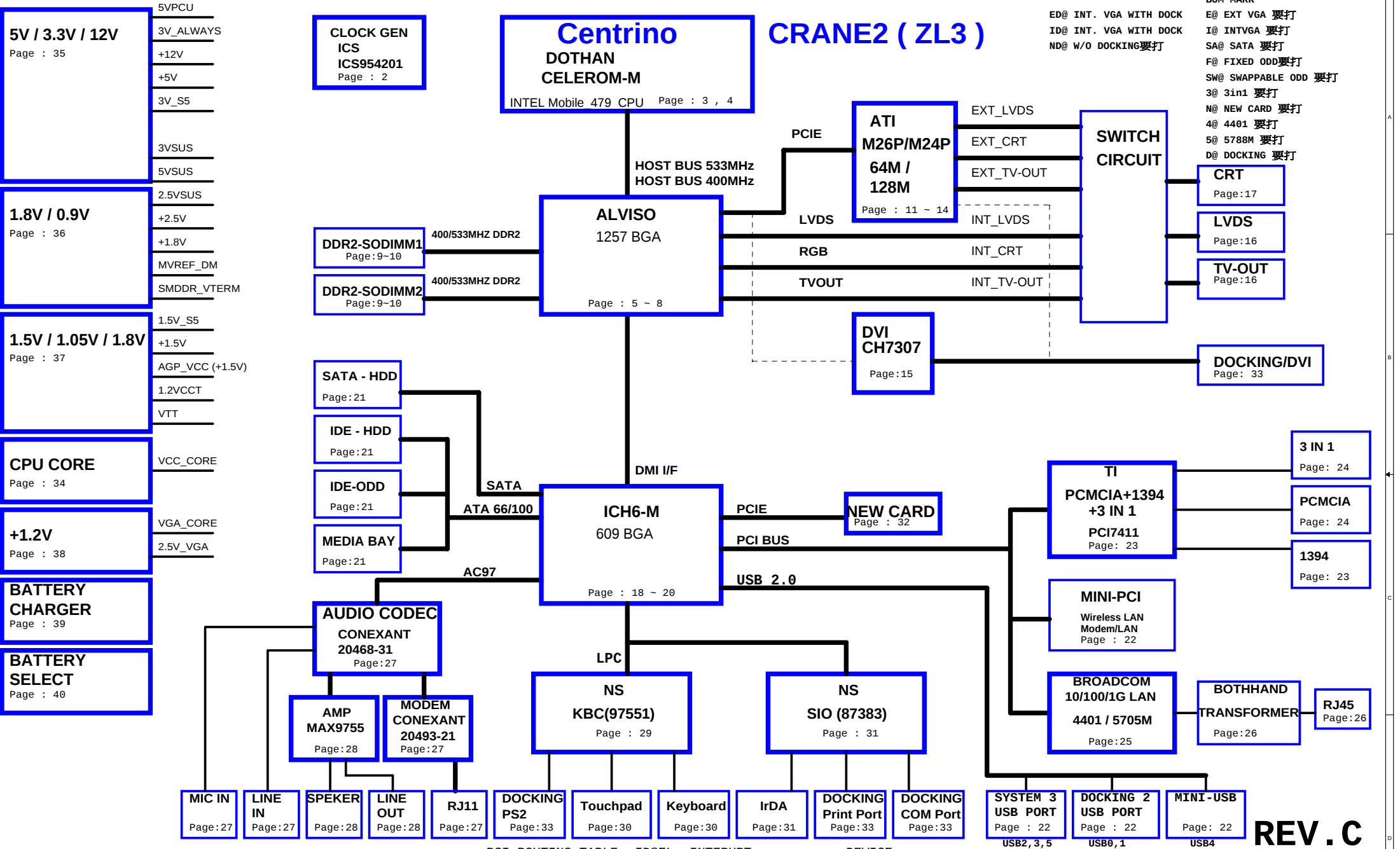




BOM MARK	
E@ EXT VGA 要打	
I@ INTVGA 要打	
SA@ SATA 要打	
F@ FIXED ODD 要打	
SW@ SWAPPABLE ODD 要打	
3@ 3in1 要打	
N@ NEW CARD 要打	
4@ 4401 要打	
5@ 5788M 要打	
D@ DOCKING 要打	

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD24	INTA#	BROADCOM LAN
REQ2# / GNT2#	AD19	INTB# , INTD#	MINI-PCI
REQ1# / GNT1#	AD17	INTC#, INTD#, INTA#	TI 7411

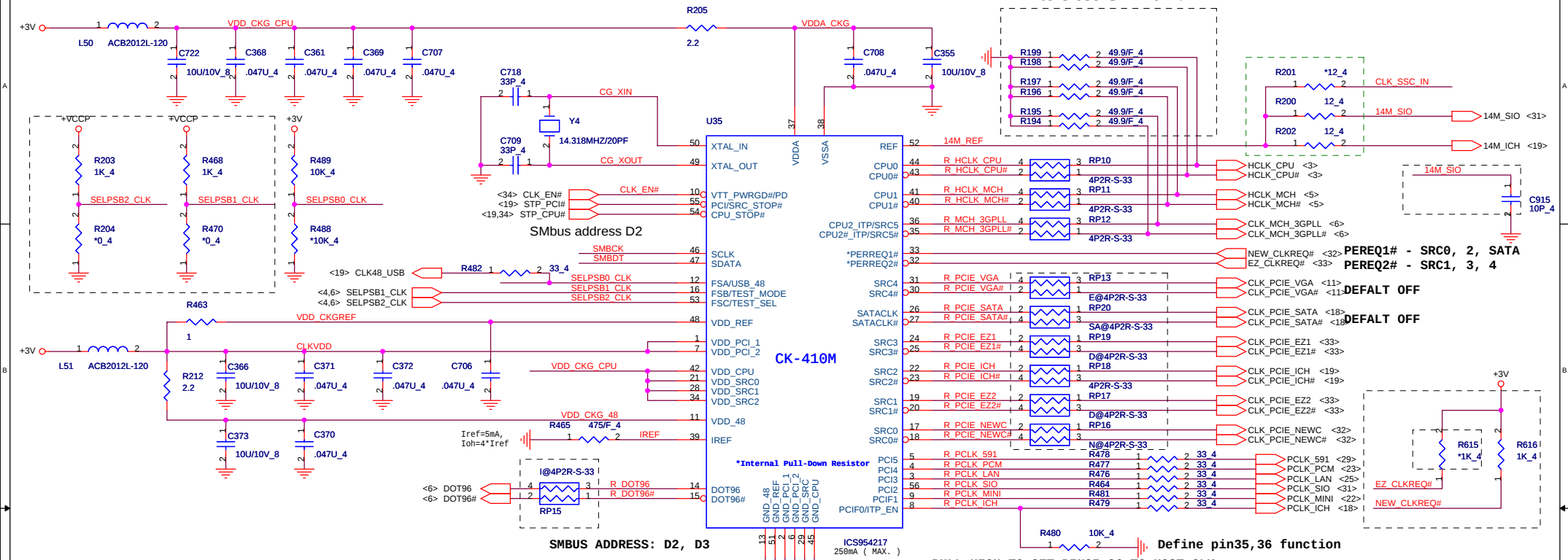


PROJECT : ZL3

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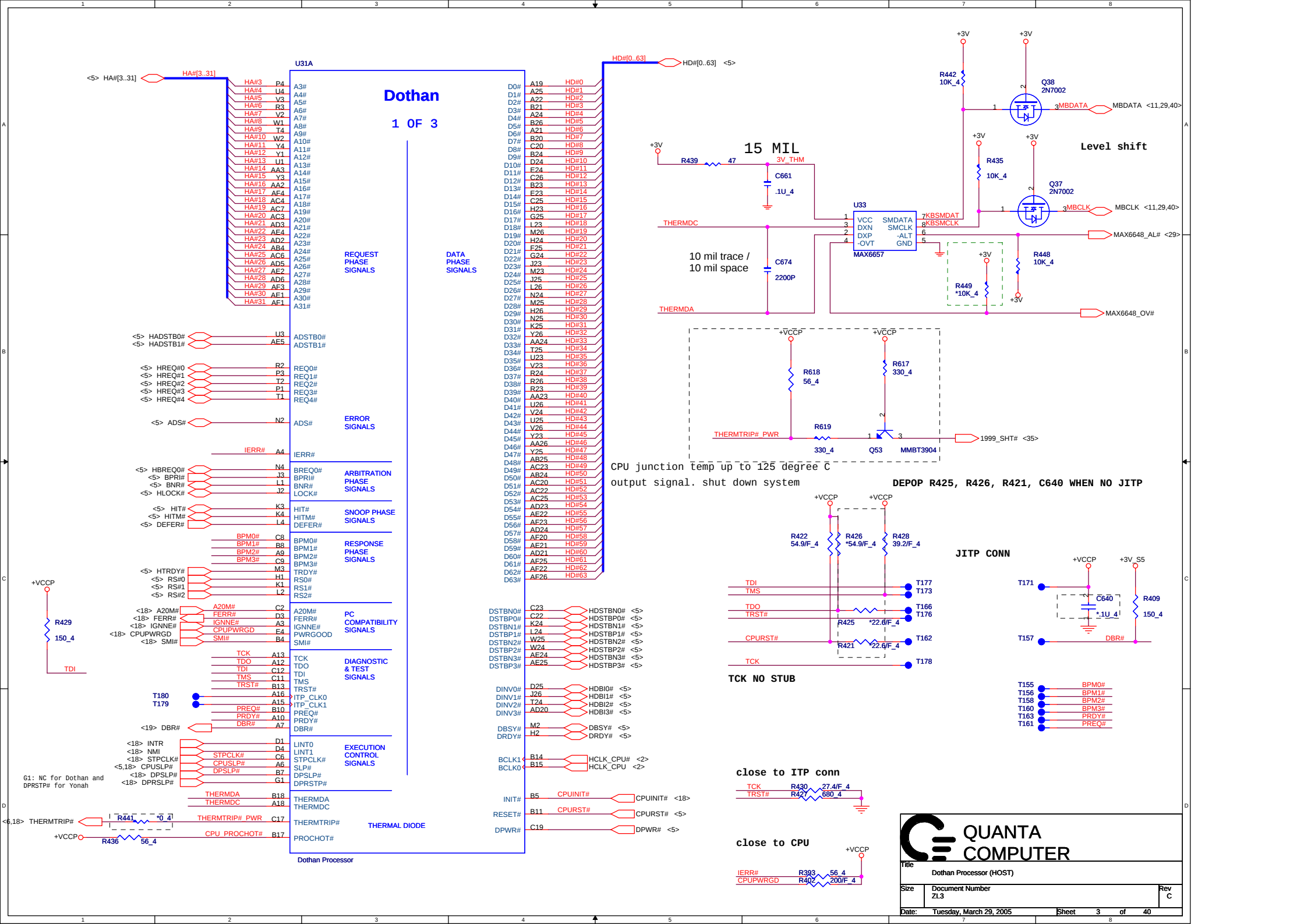
Size	Document Number	Rev
	BLOCK DIAGRAM	C
Date:	Tuesday, March 29, 2005	Sheet 1 of 40

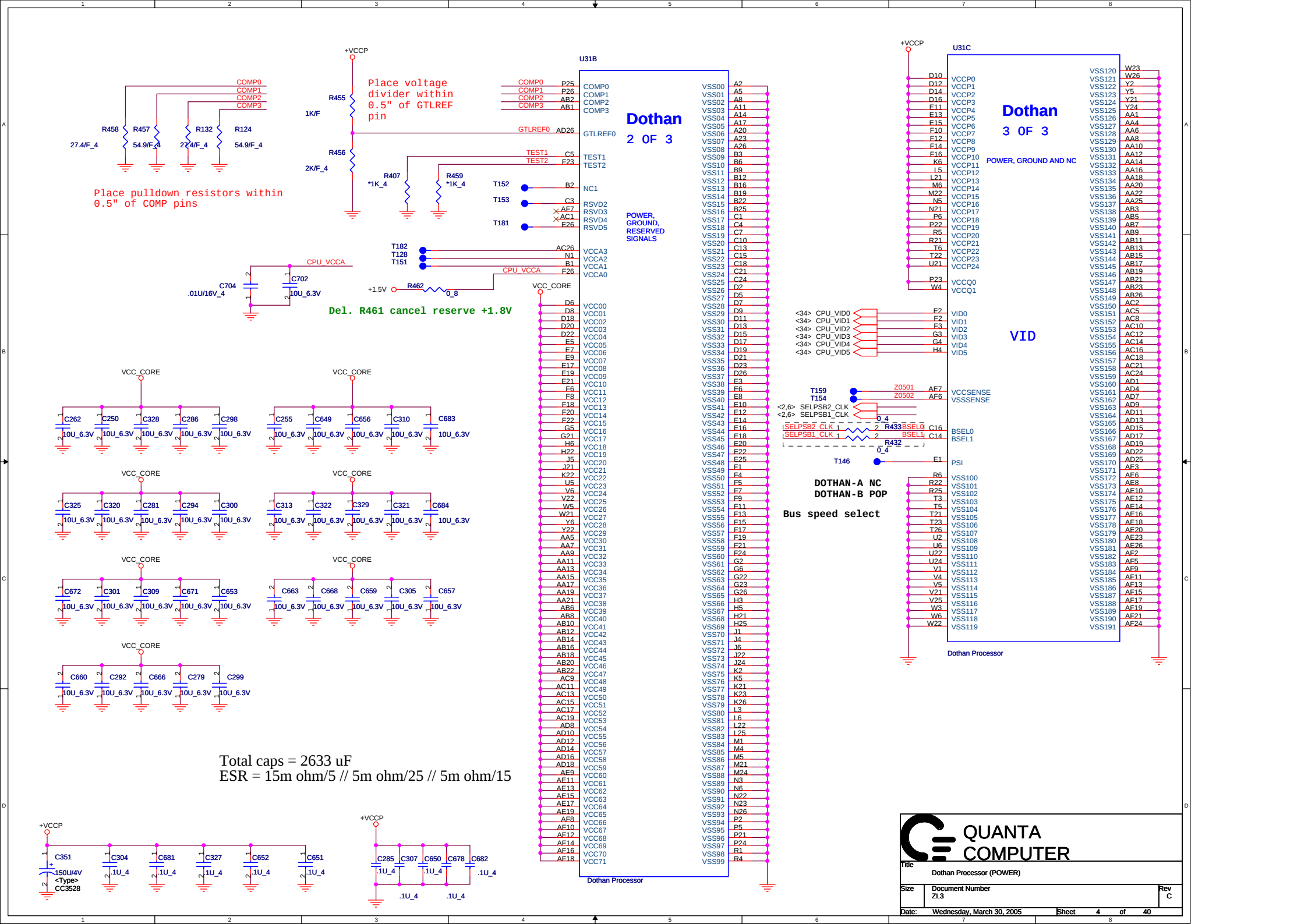
Place these termination
to close CK410M.

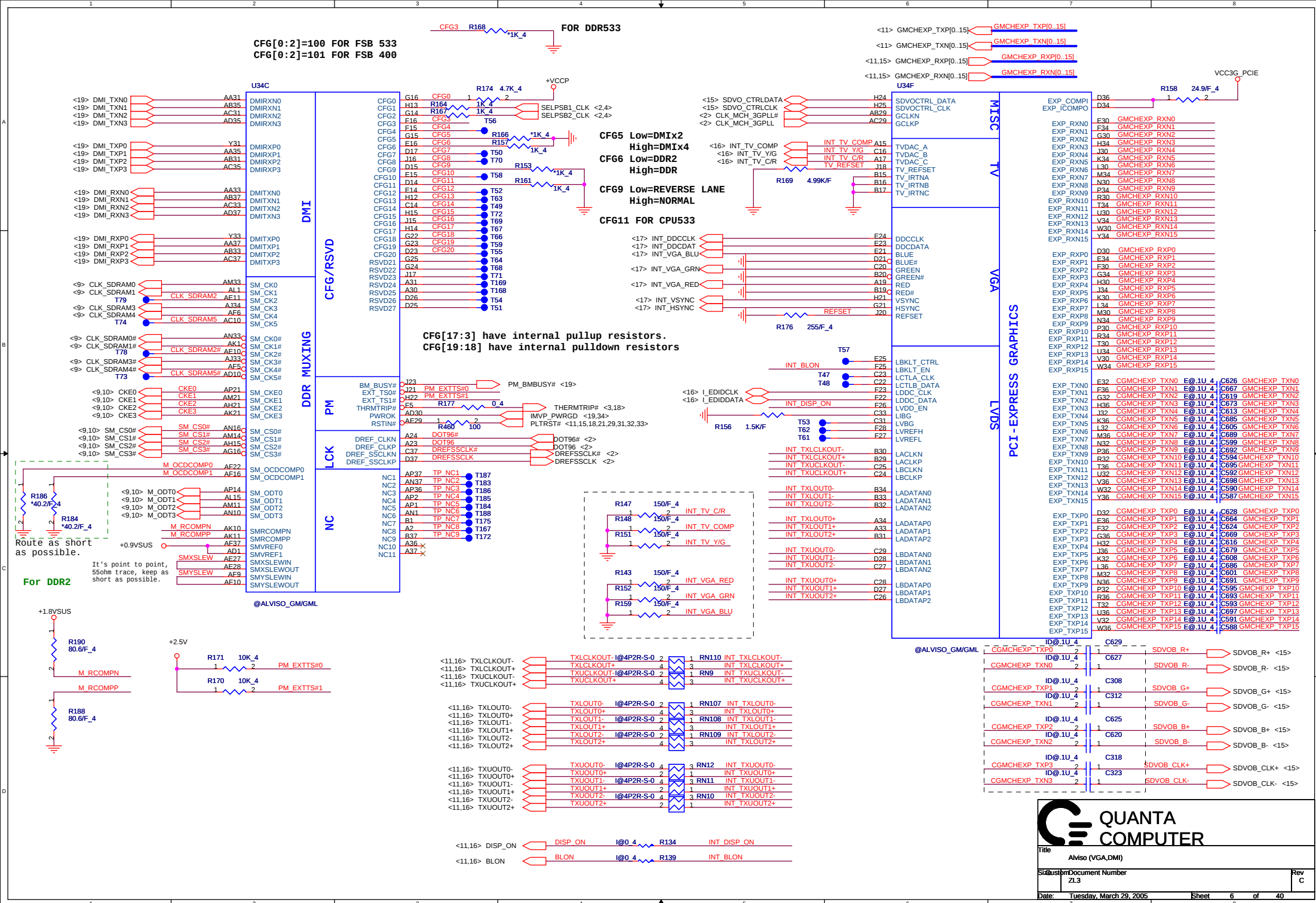


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination
to close CK410M.





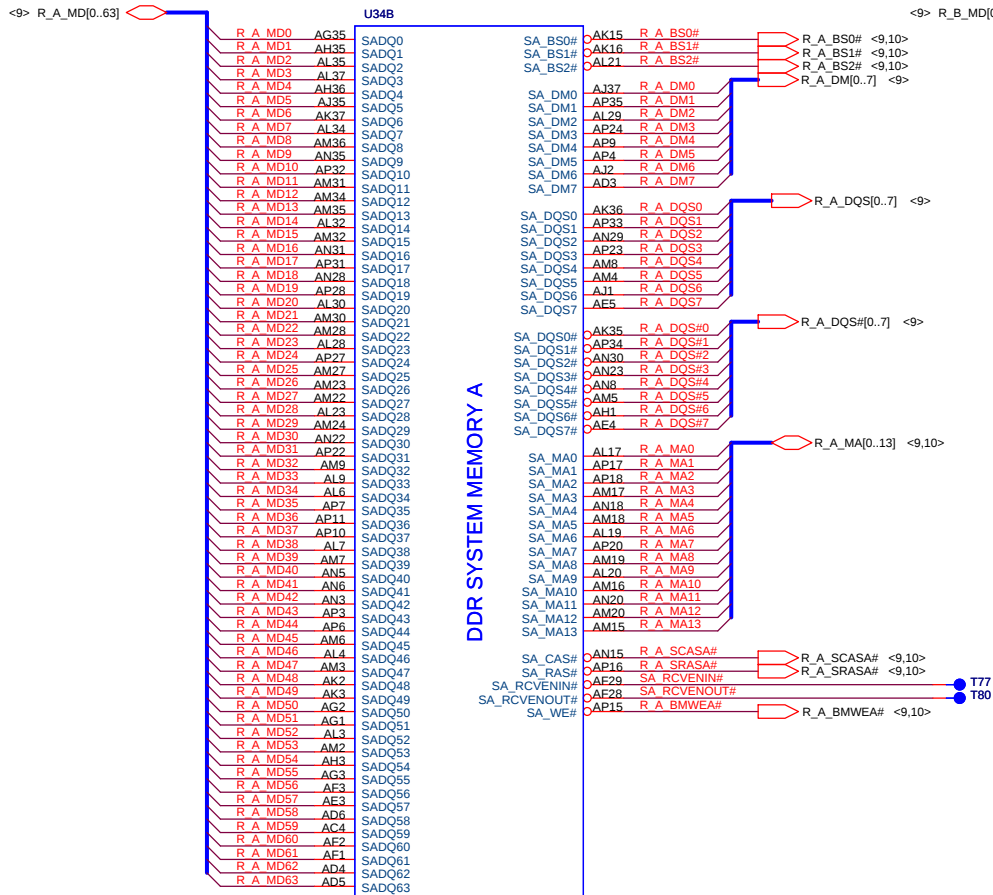


Title Alviso (VGA.DMI)

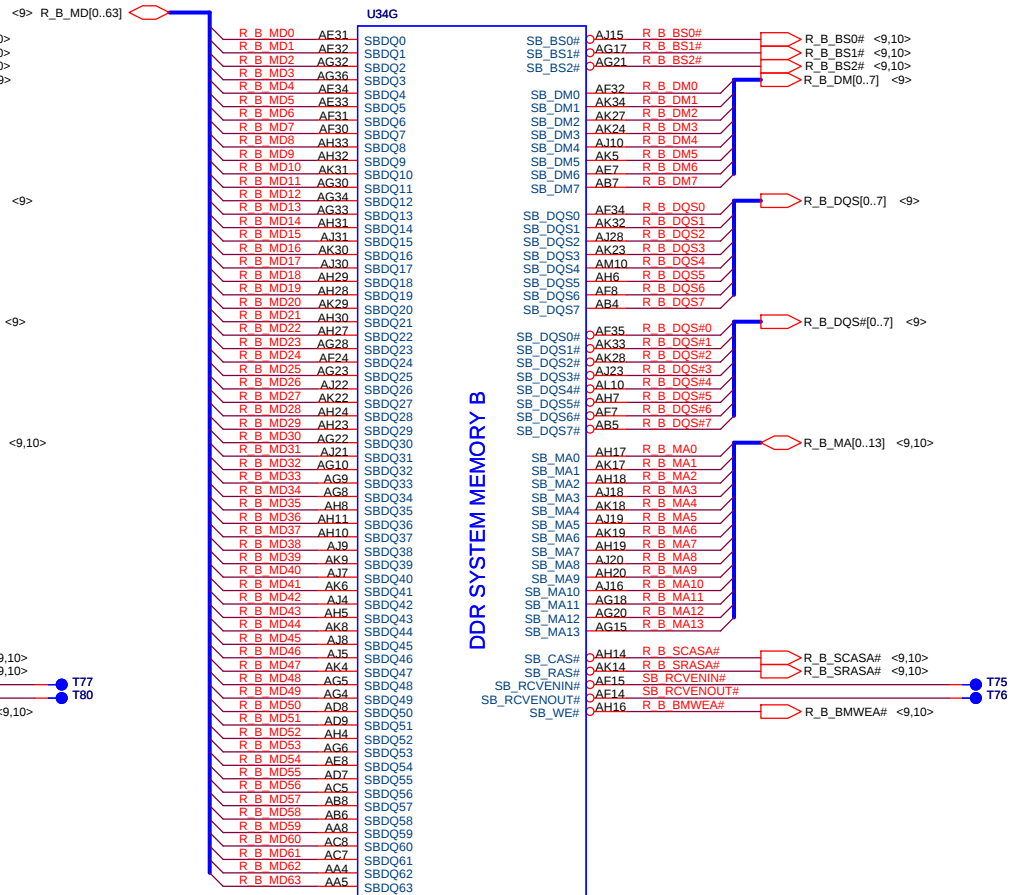
Size	Custom Document Number
	713

Date: Tuesday, March 29, 2005

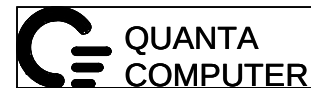
Rev
C



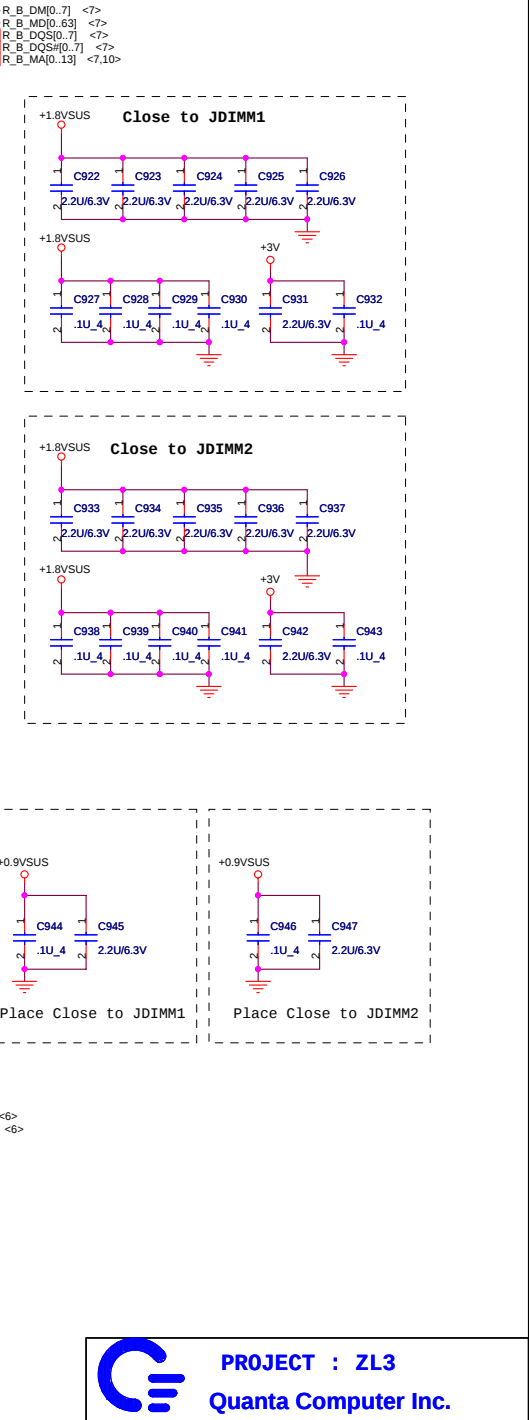
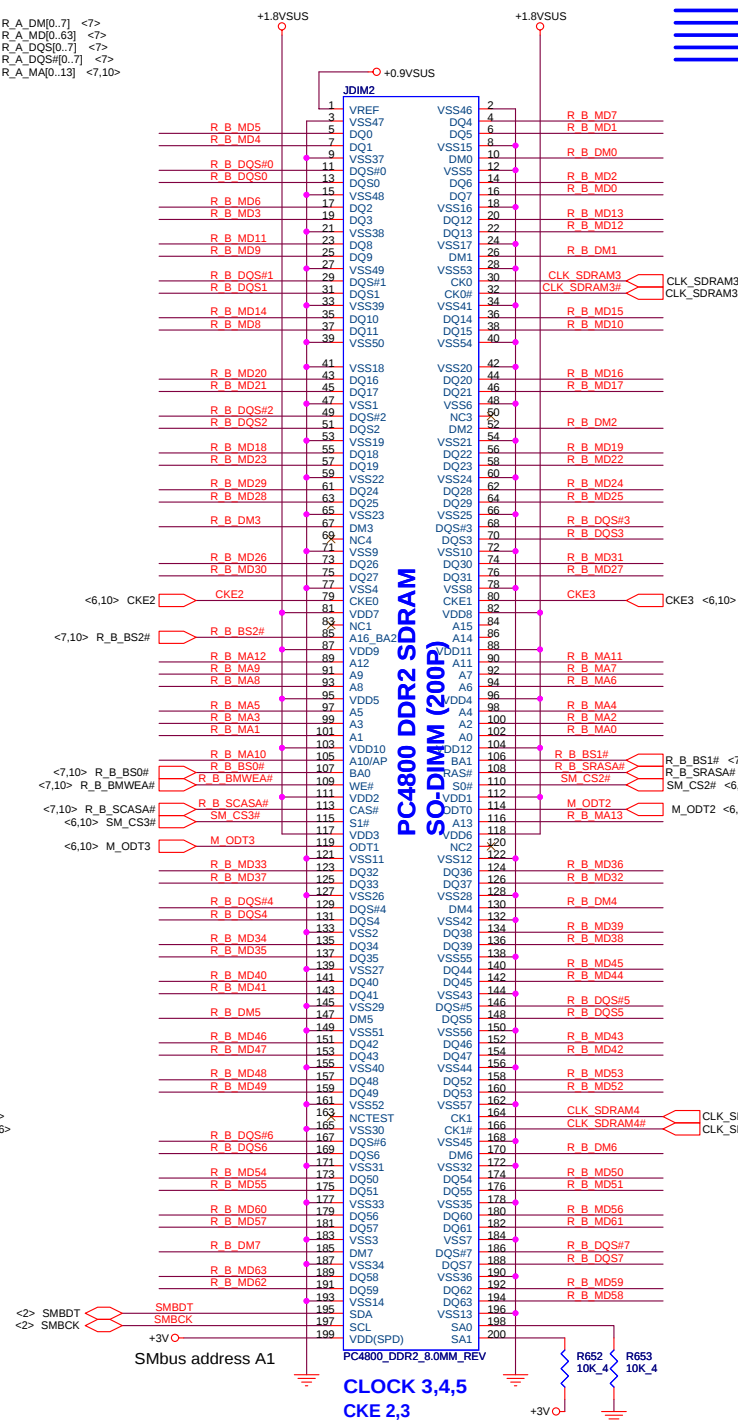
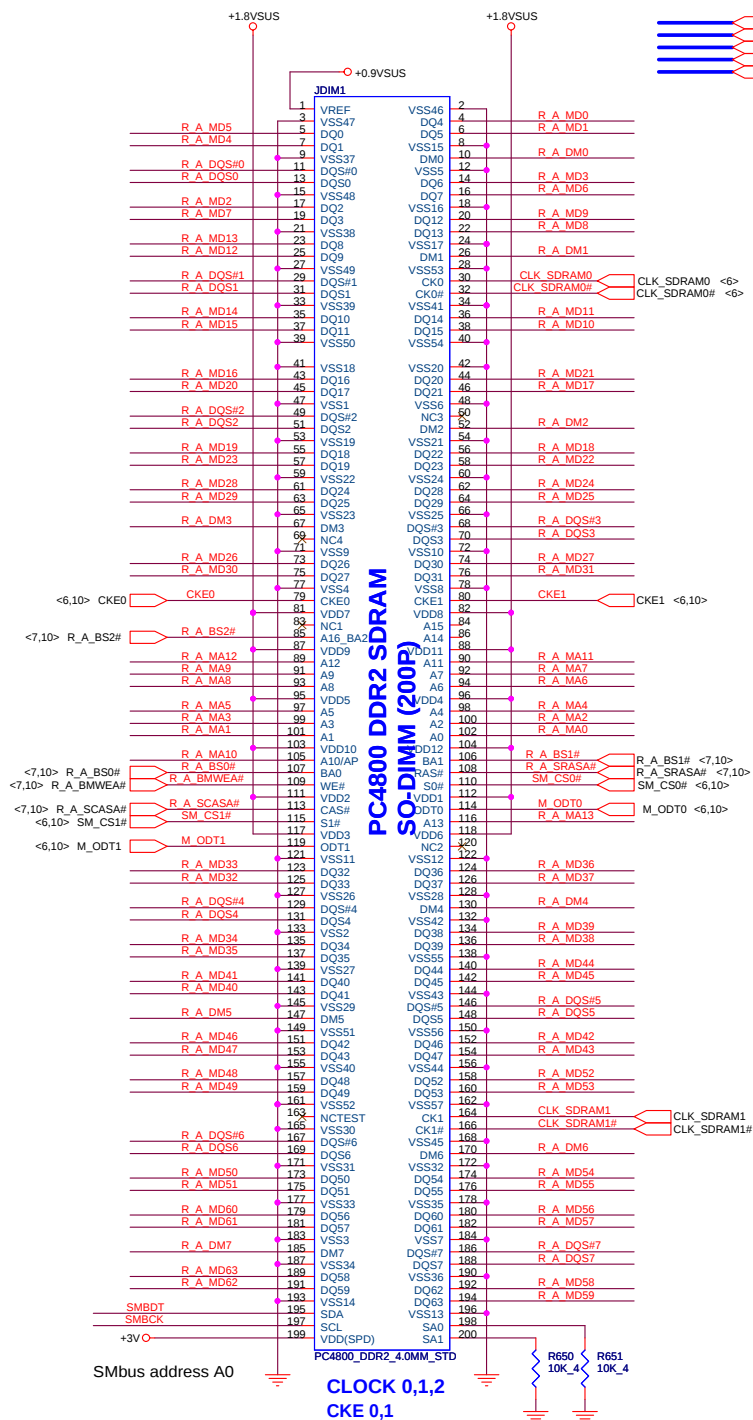
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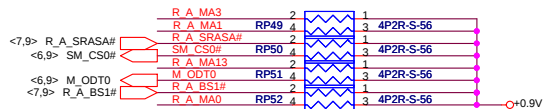
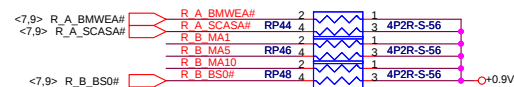
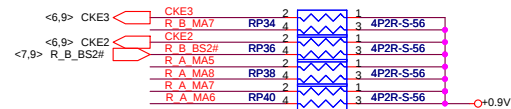
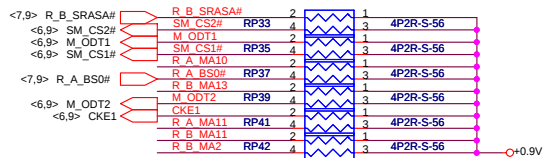
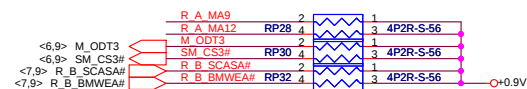
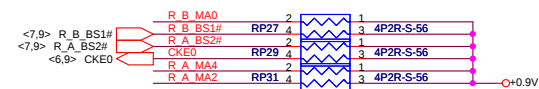
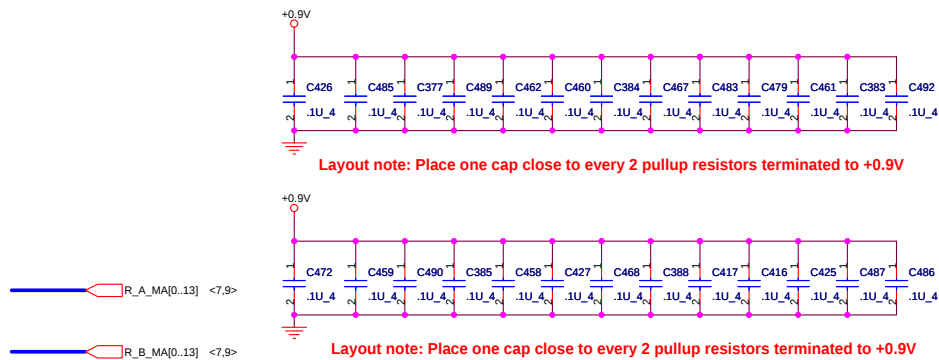


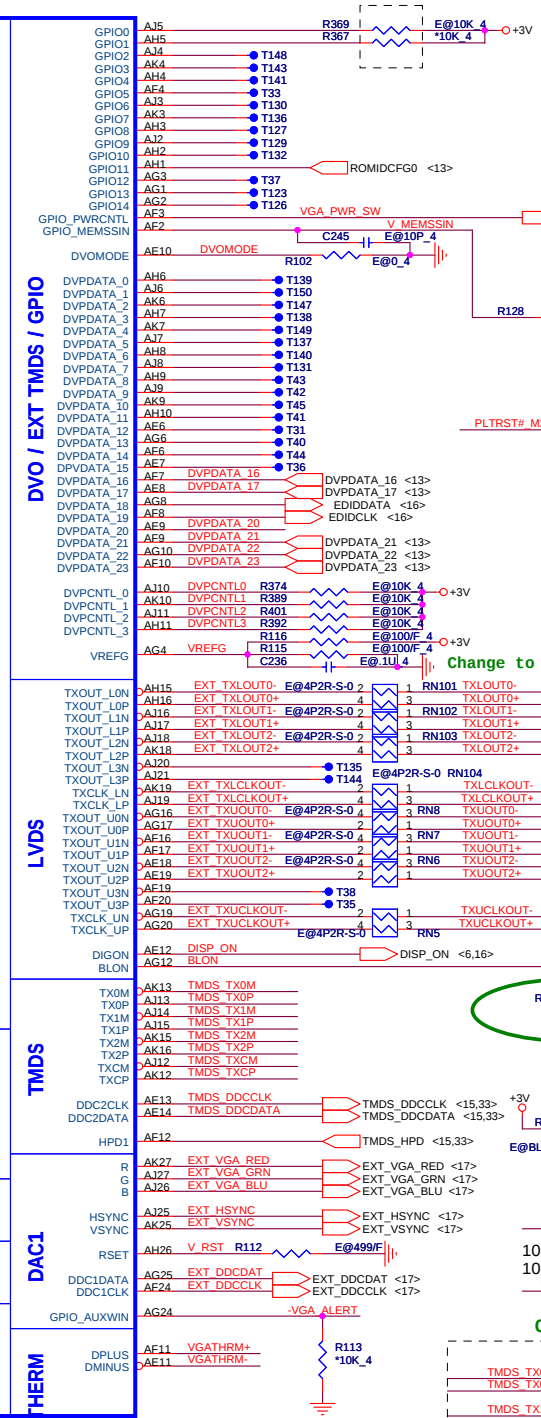
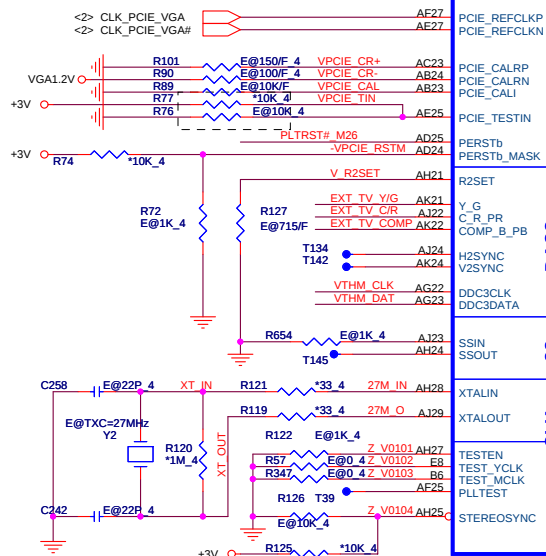
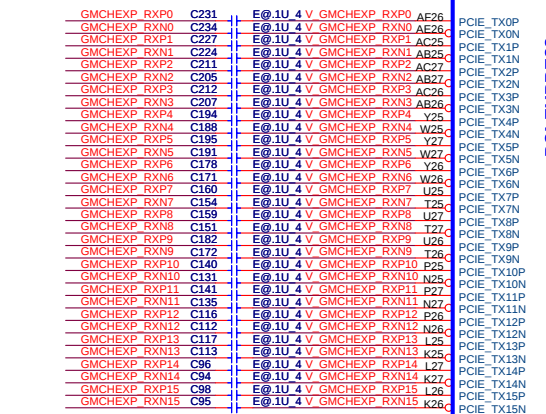
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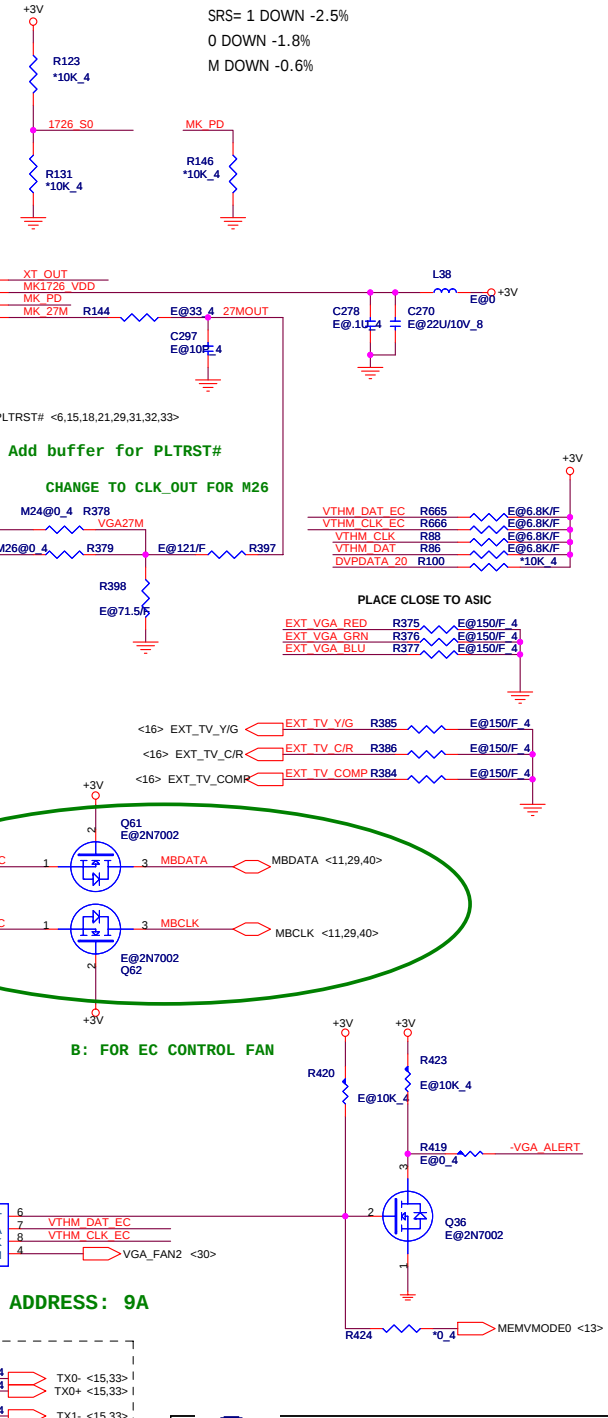


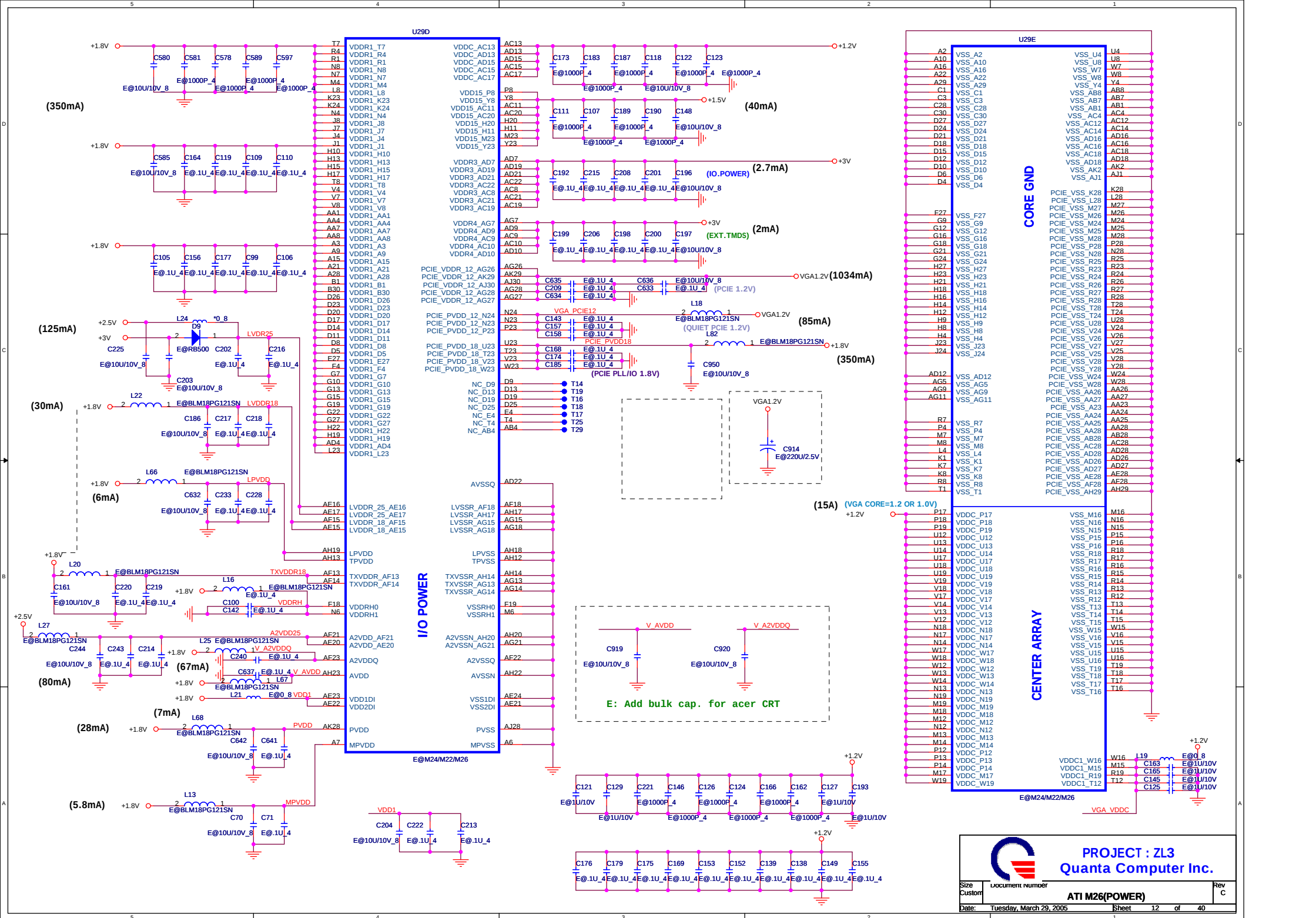


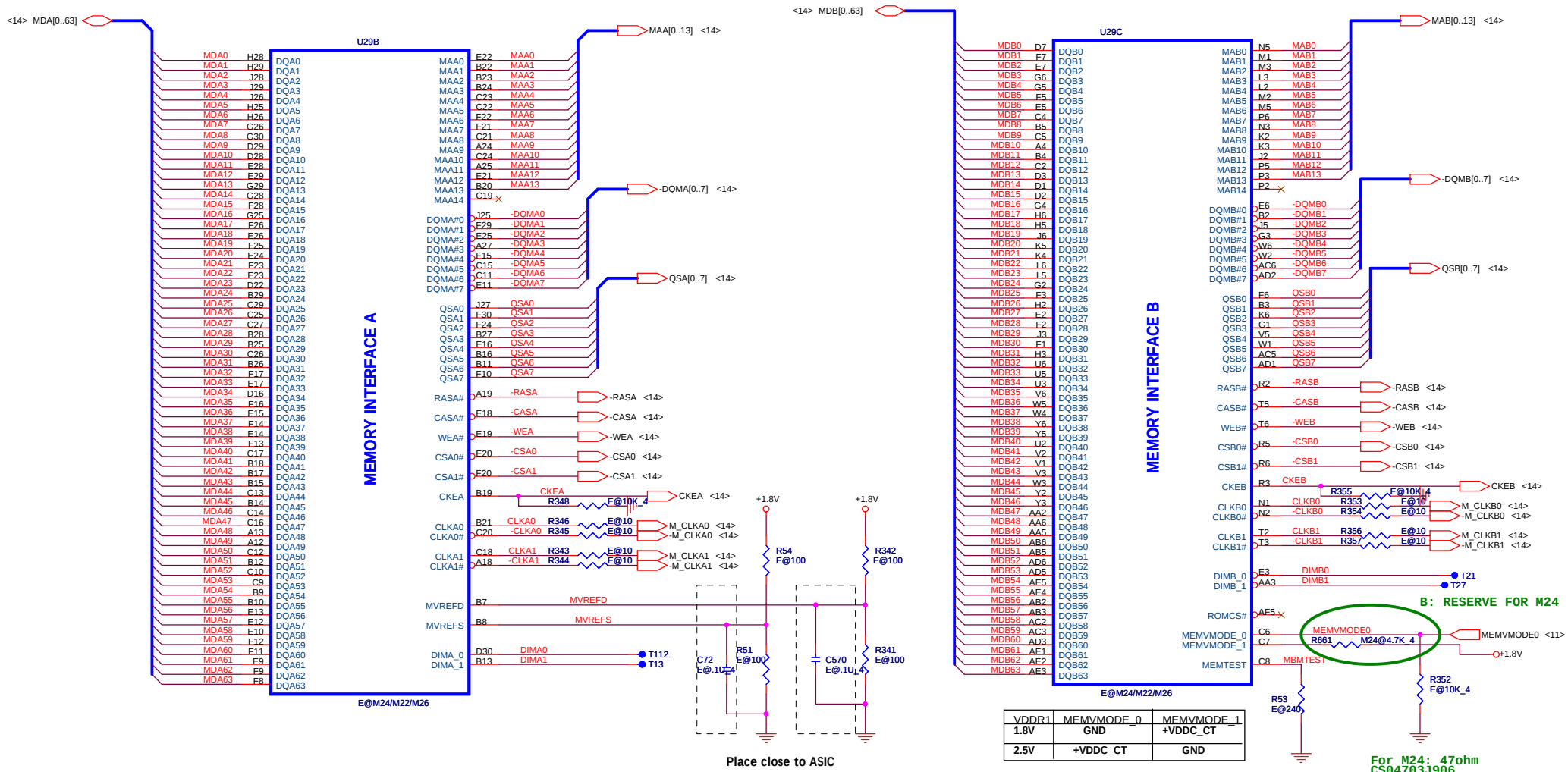


MEMORY CLOCK SPREAD SPECTRUM

Hi: 1.0V
Lo: 1.2V







GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL

GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching
GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung

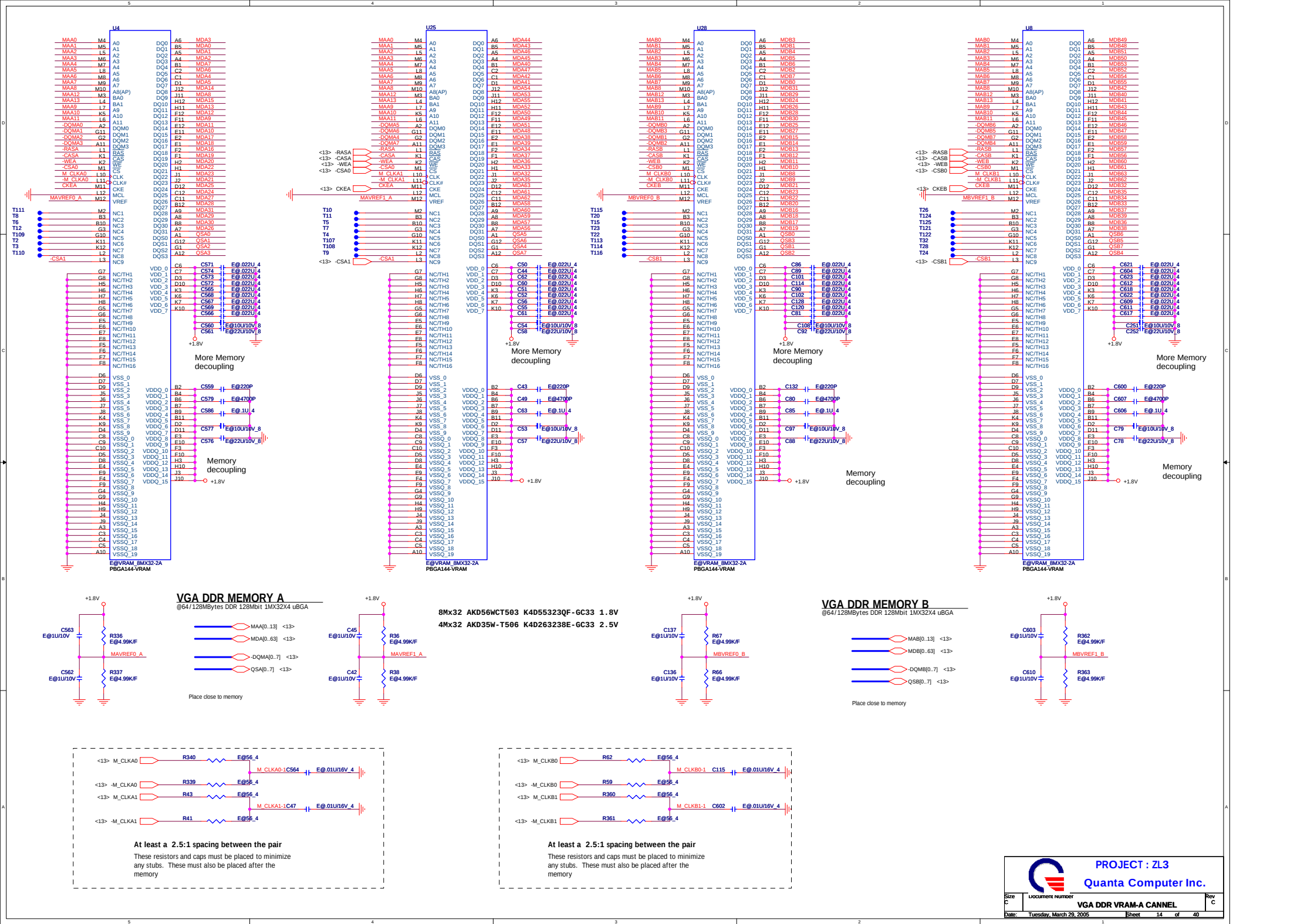
FOR M26P ONLY
0: 128M
1: 256M

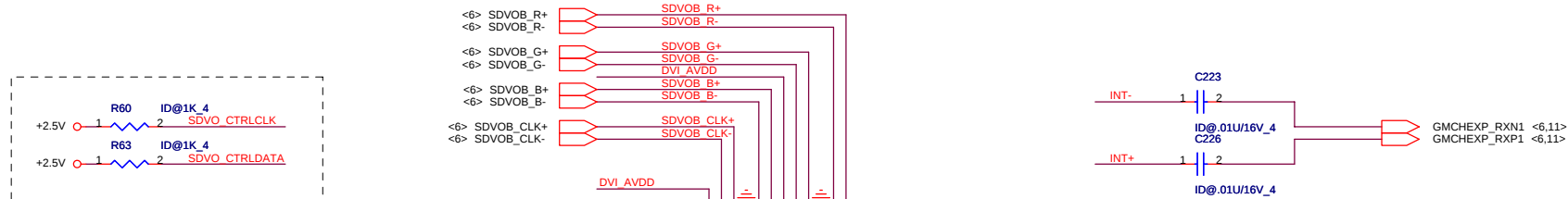
C: FOR HYNIX MEMORY

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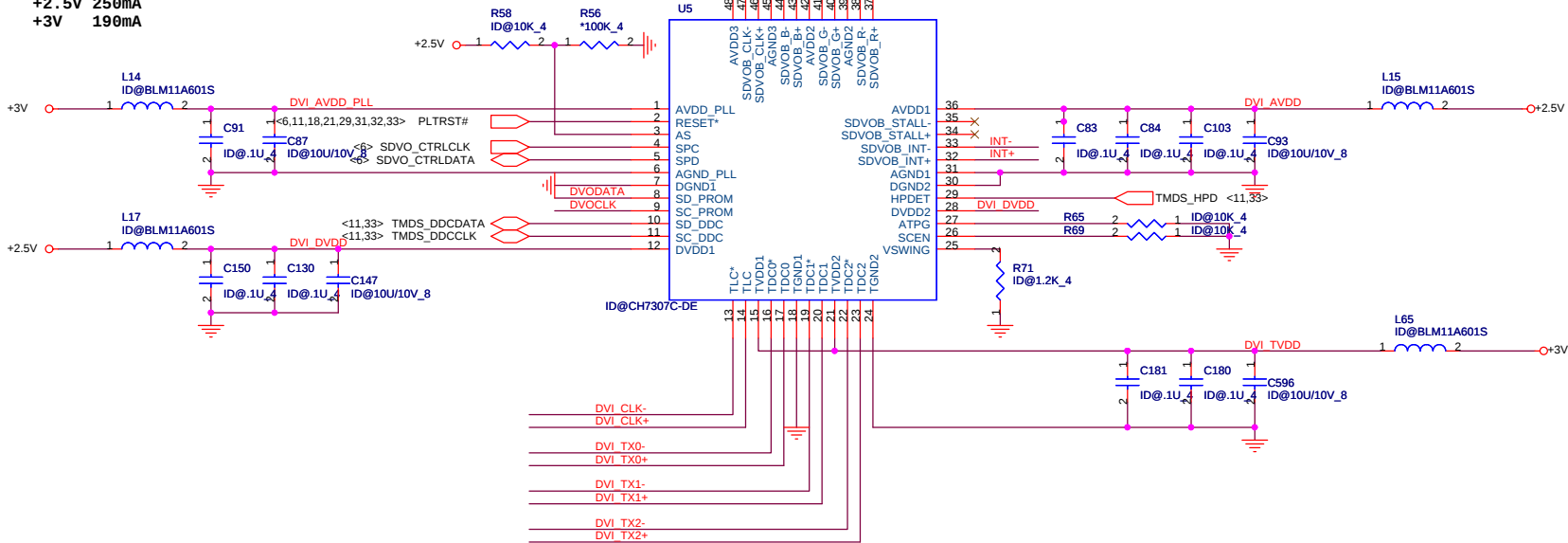
ATI M26 MEM/STRAPS PIN

Size Custom
Document number
Date: Tuesday, March 29, 2005
Sheet 13 of 40
Rev C

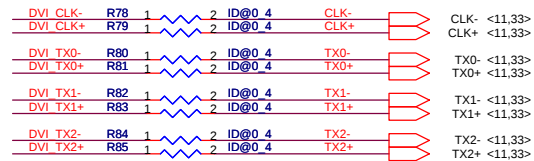
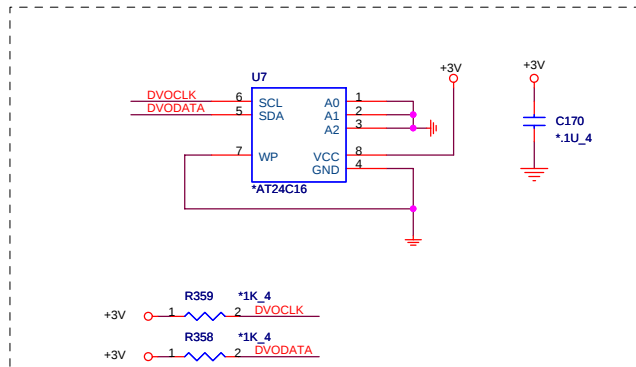


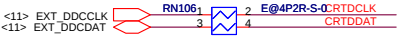
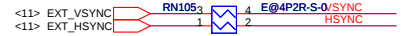
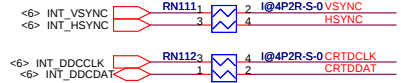


+2.5V 250mA
+3V 190mA

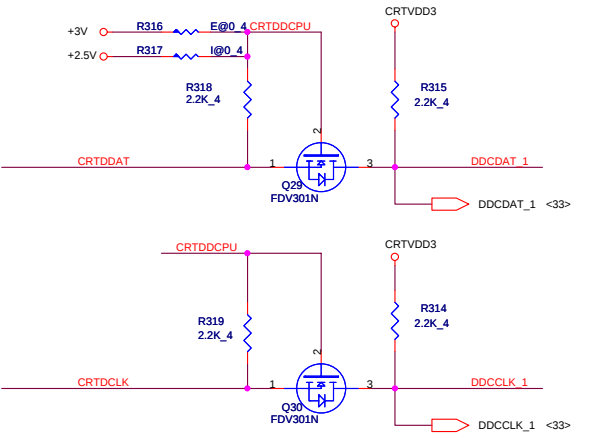
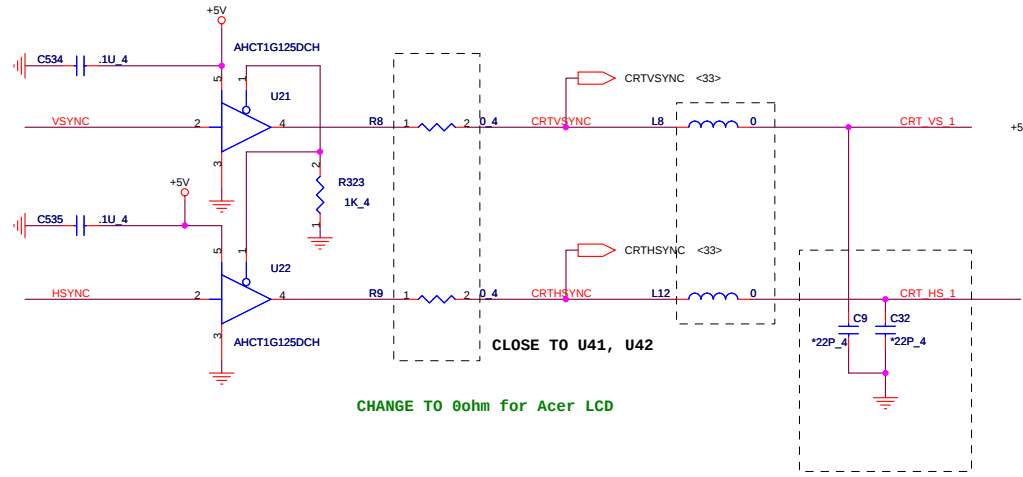
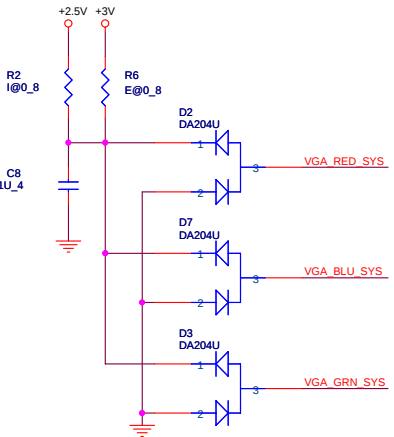
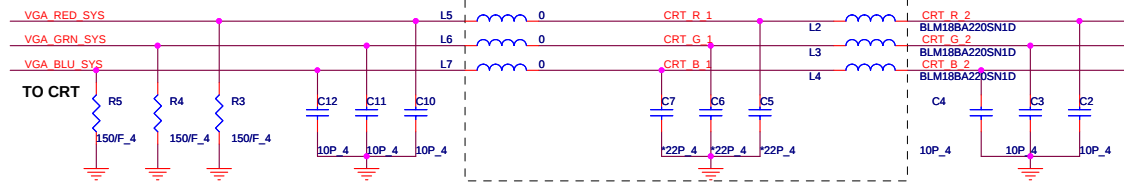
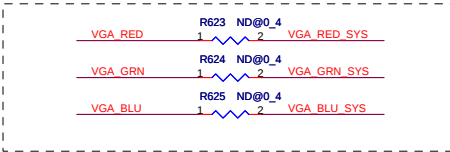
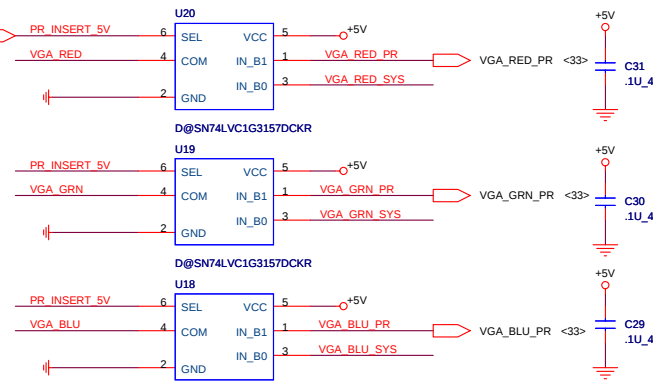


ALWAYS NOT ON, TEST ONLY

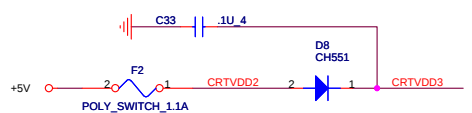
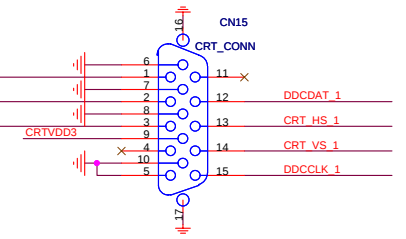




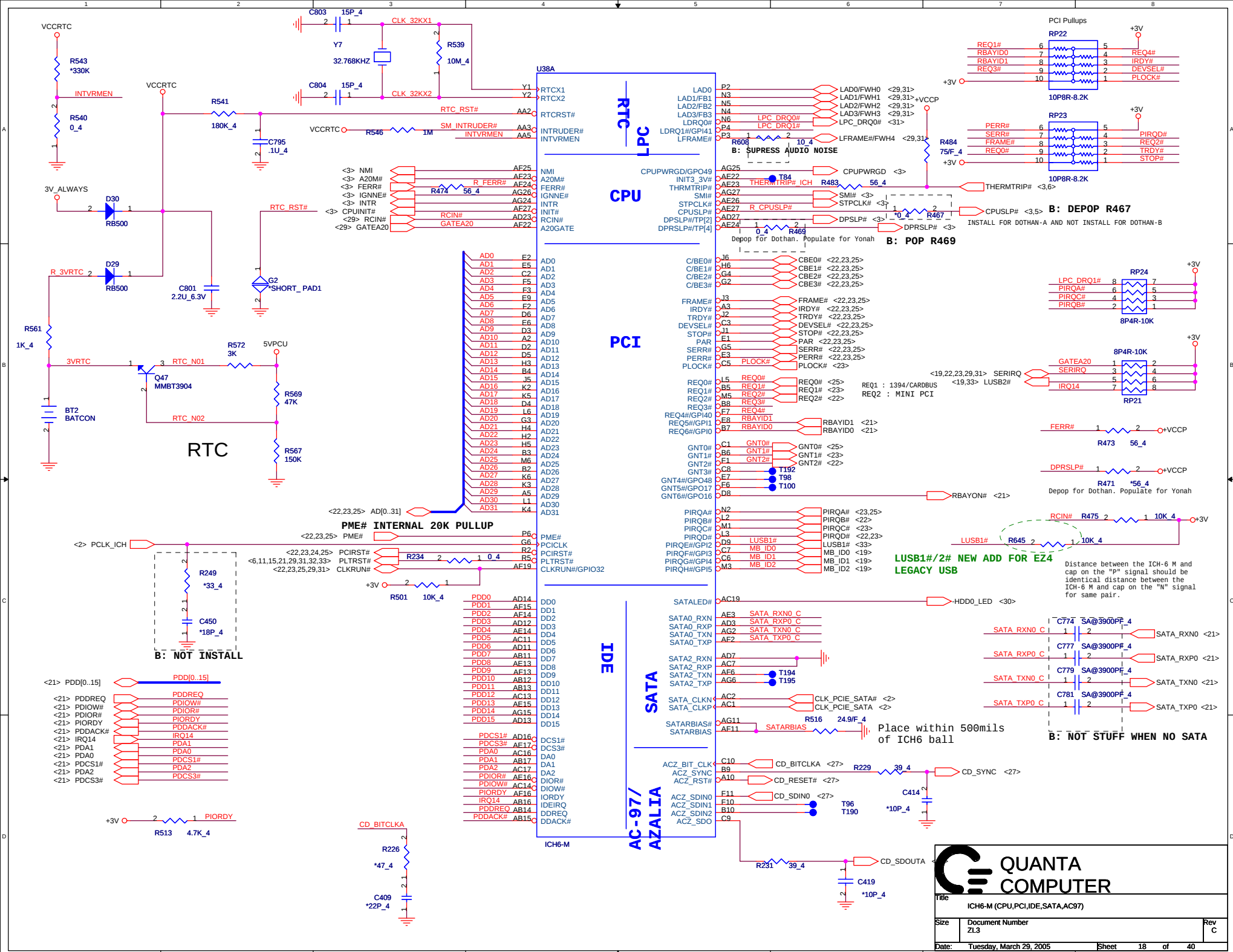
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

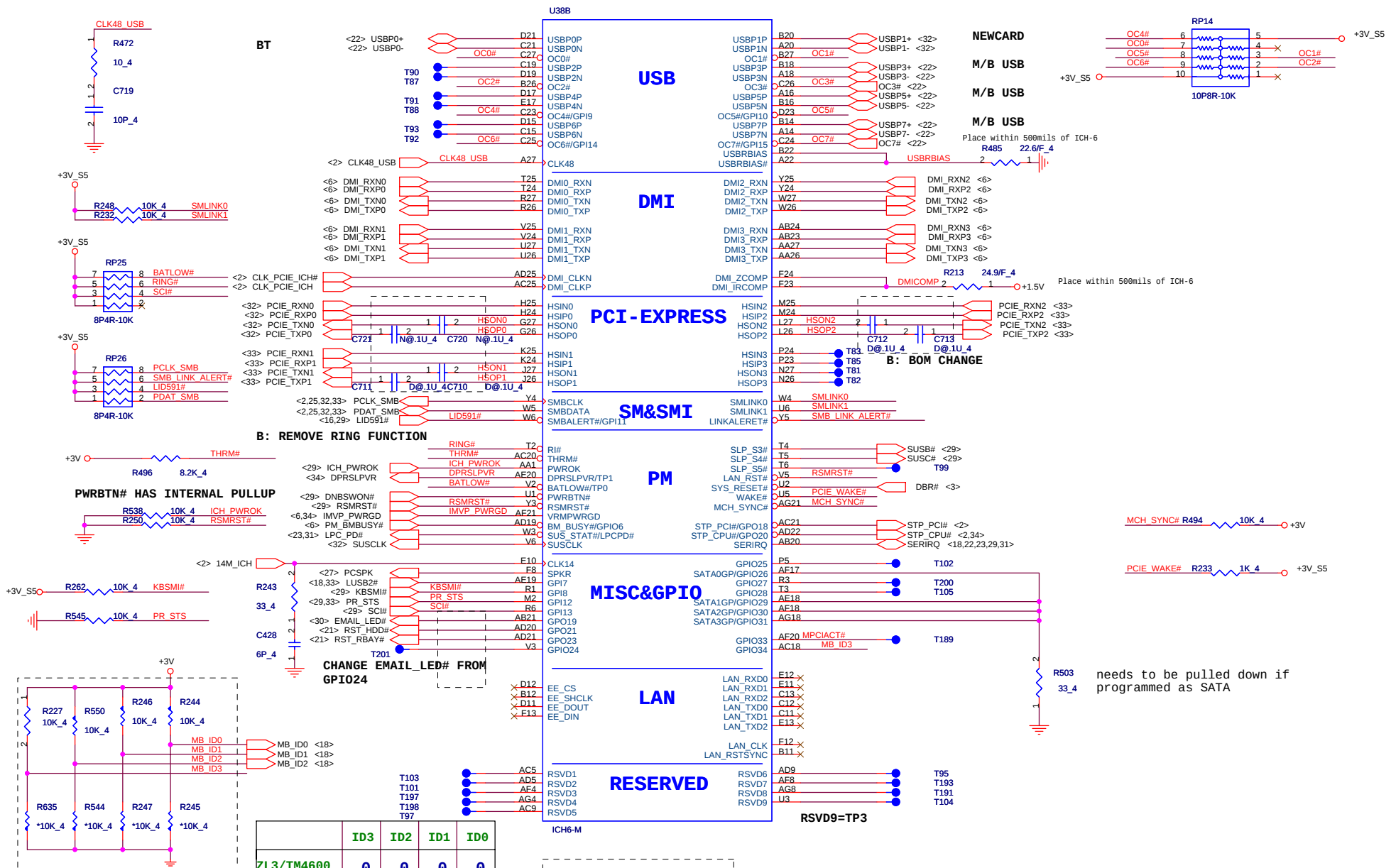


C: Change to FDV301N for Vgs issue.

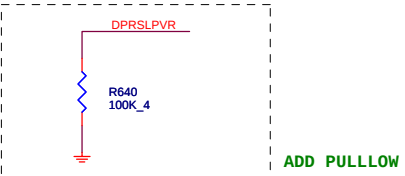


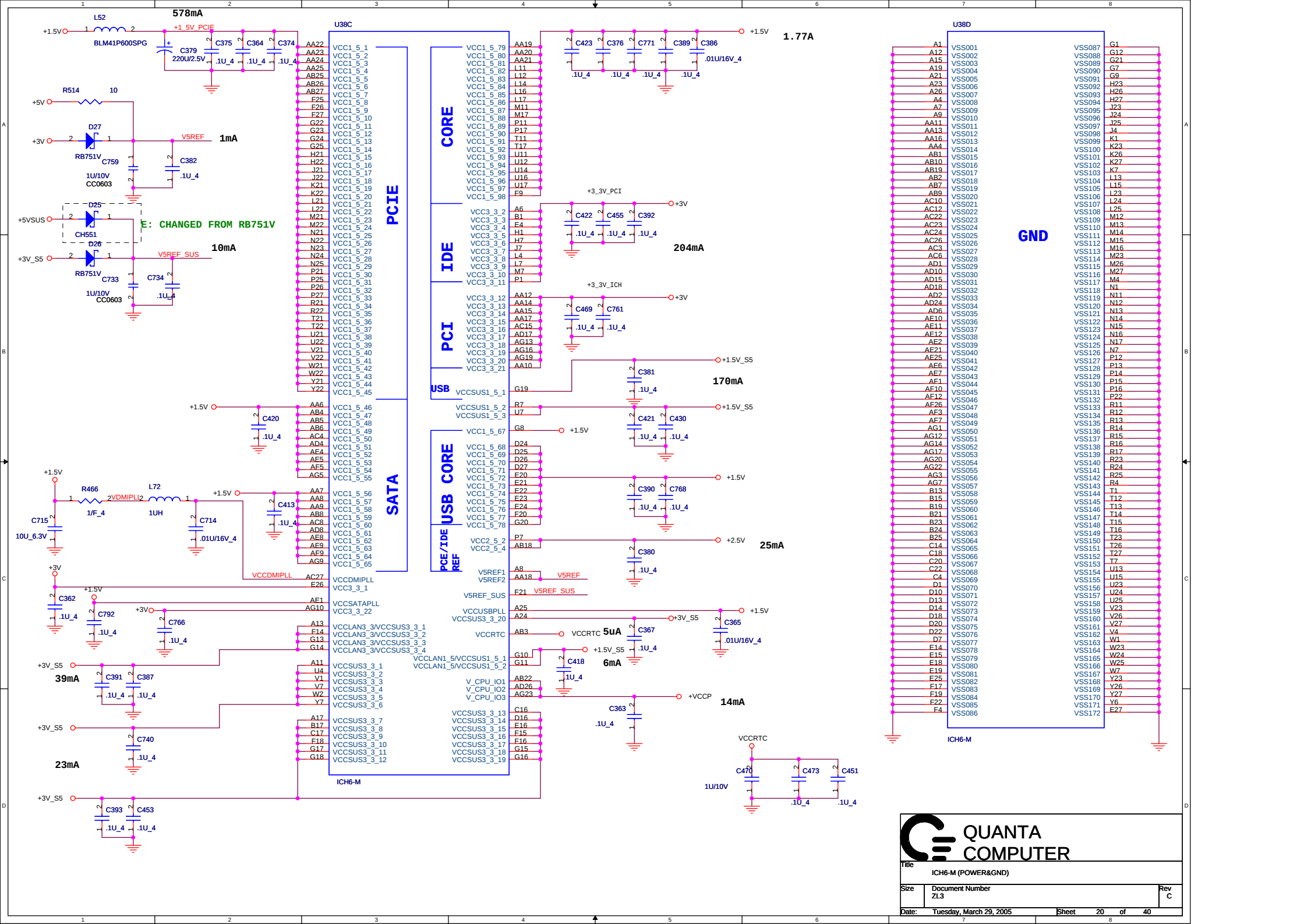
PROJECT : ZL3
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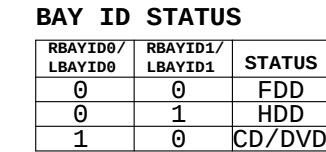
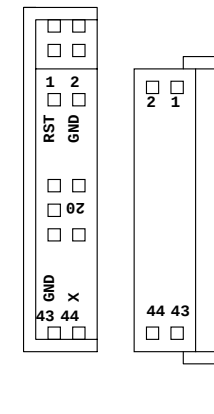


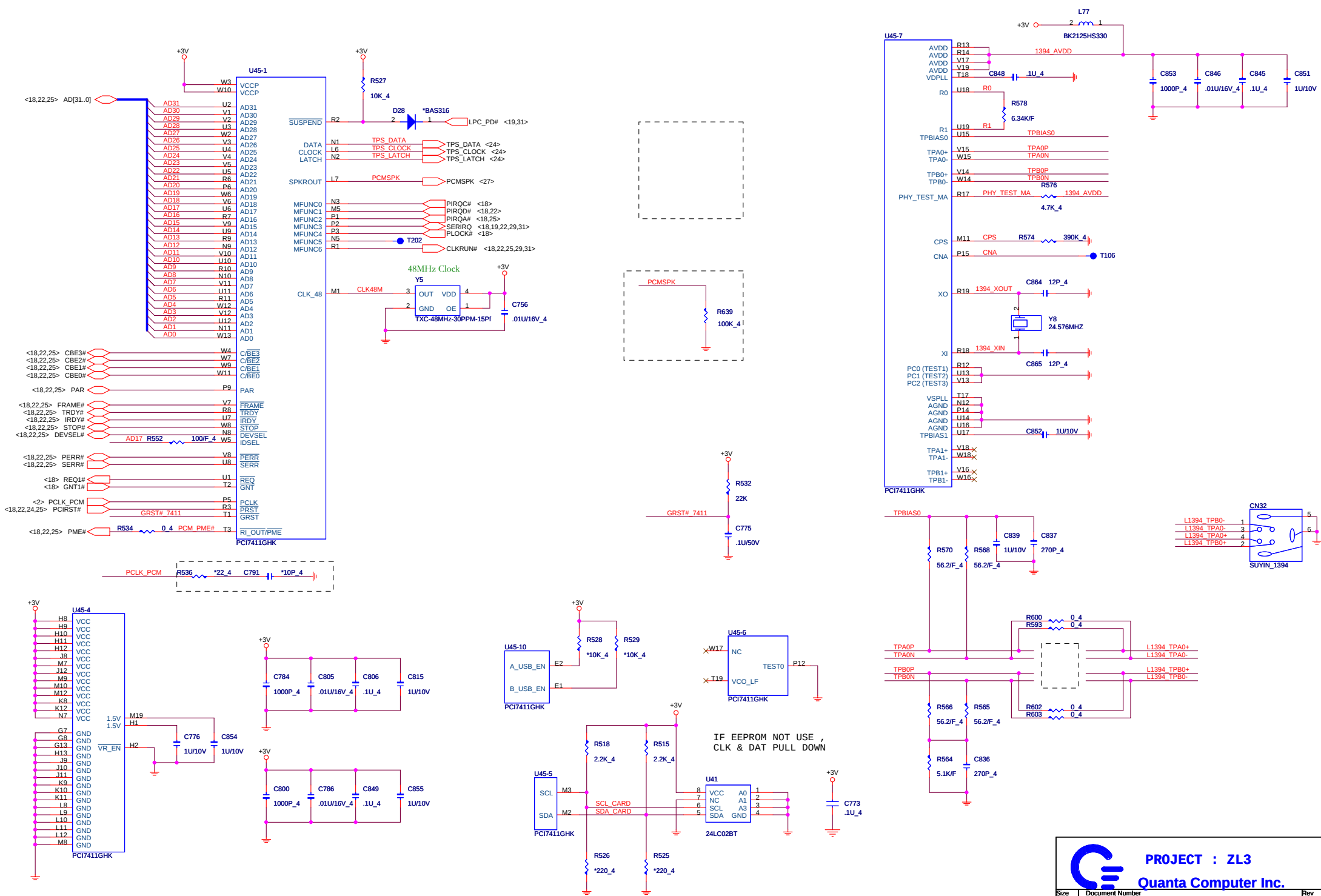


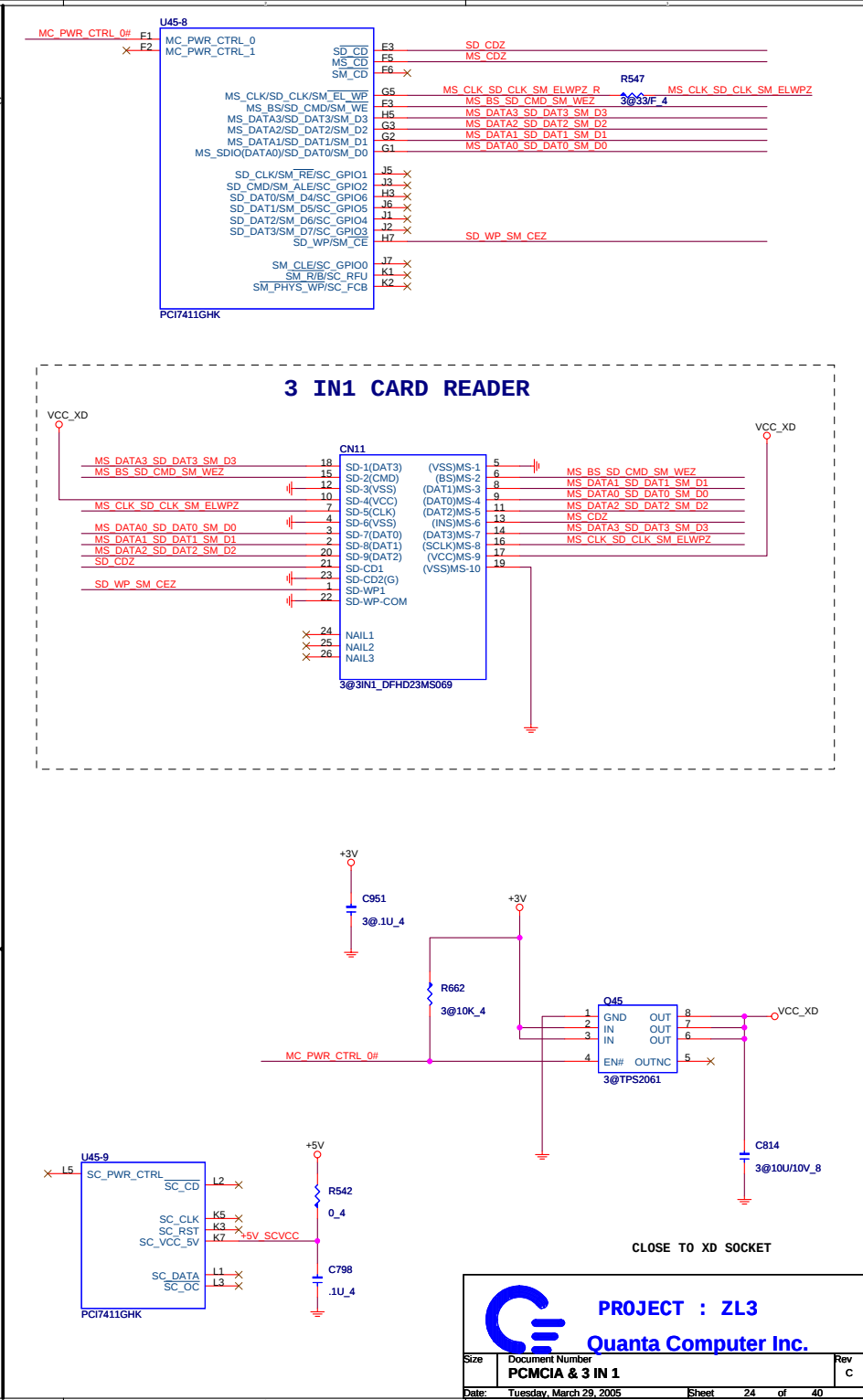
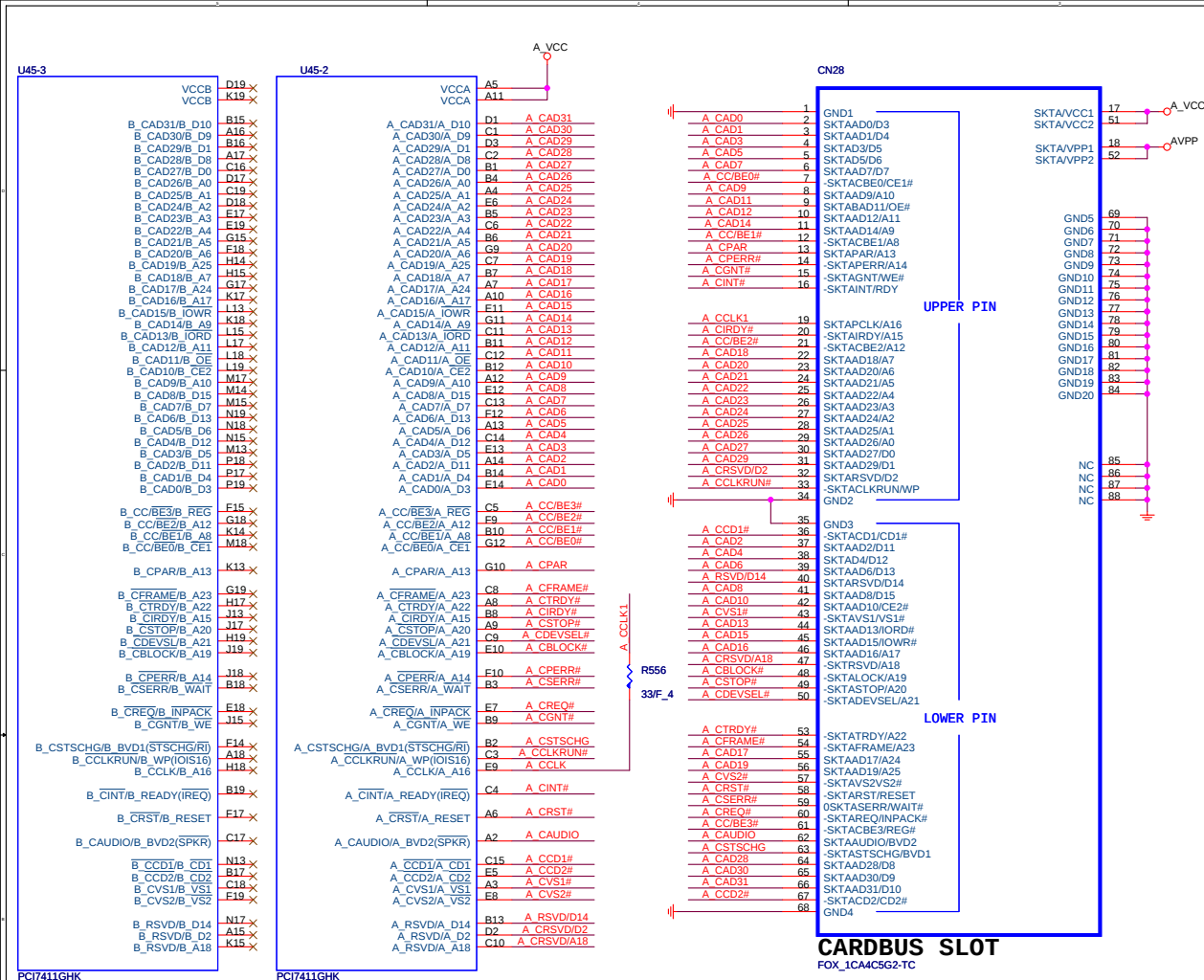
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ZL3/TM4600	0	0	0	0
ZL3B/TM4100	0	0	1	0
ZL3D/AS1690	0	1	0	0
ZL3F/AS3510	0	1	1	0
ZL3C/EX4100	1	0	1	1

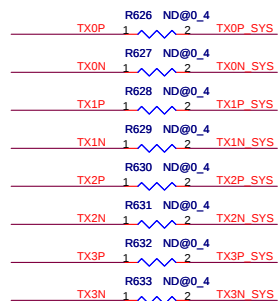
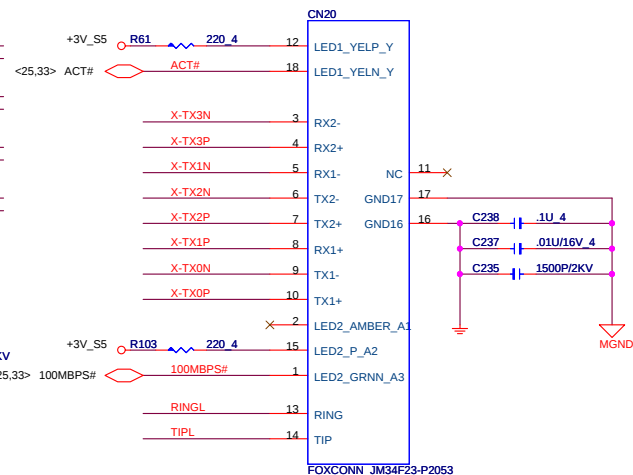
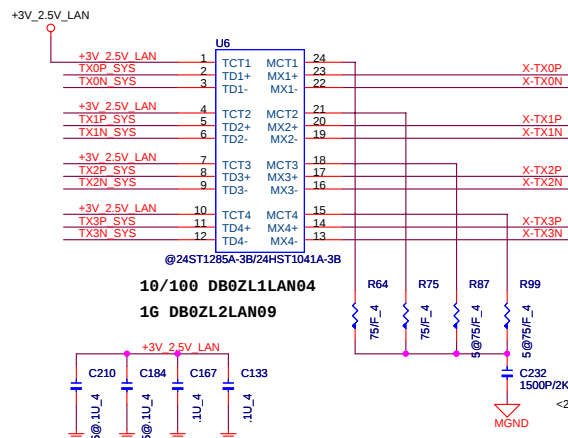
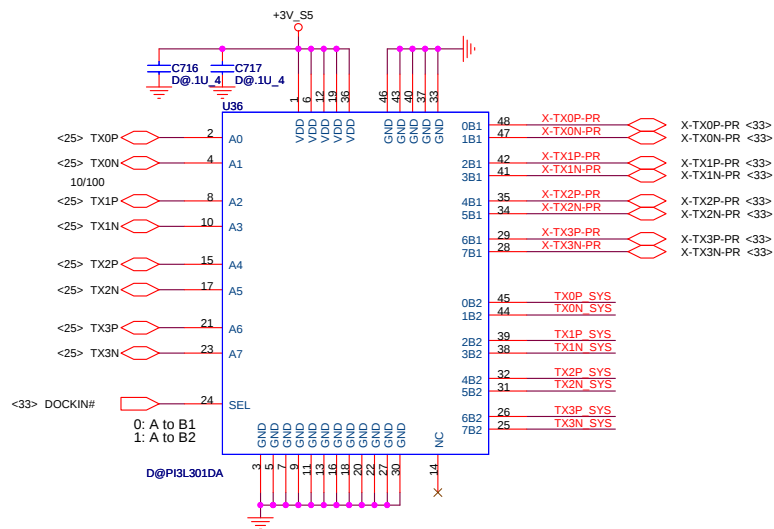




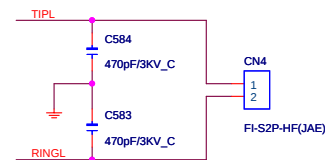




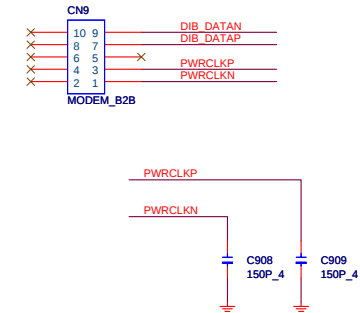
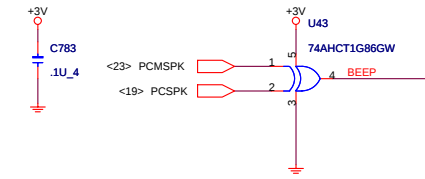
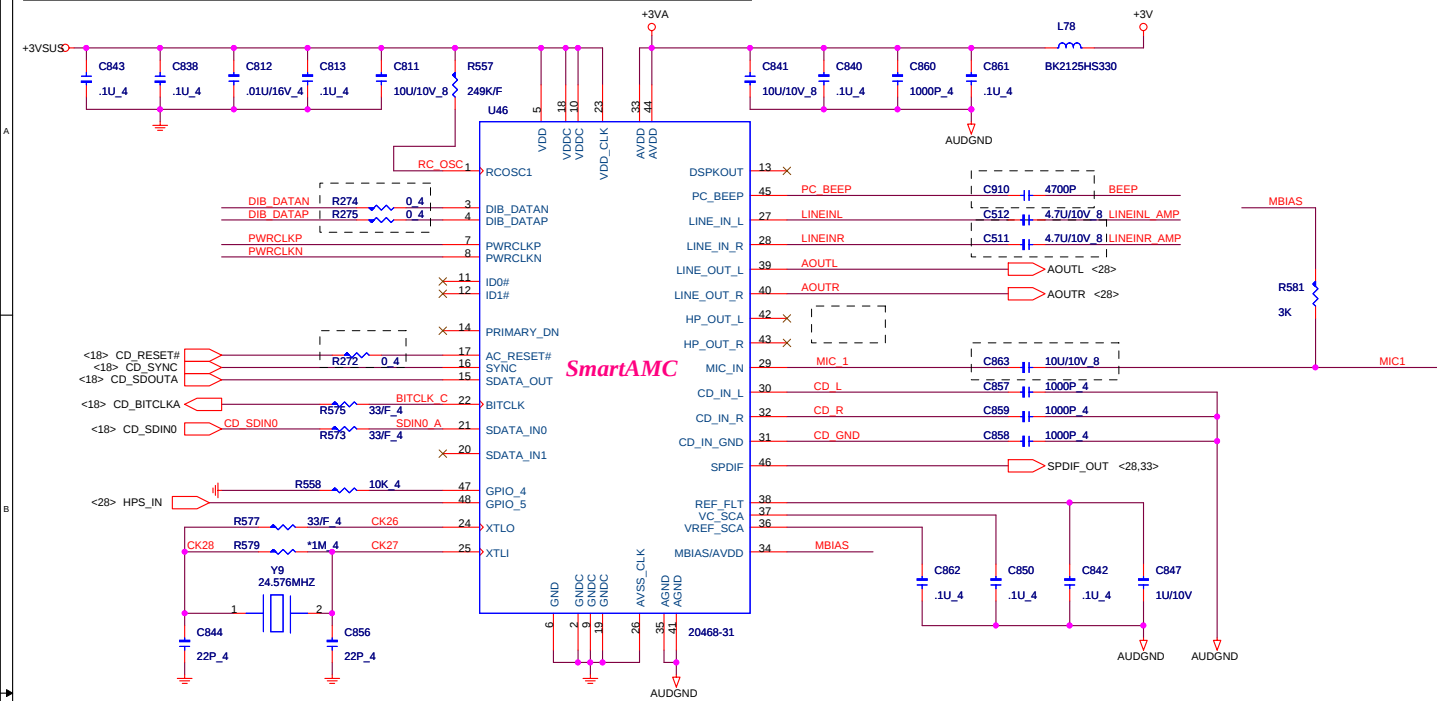




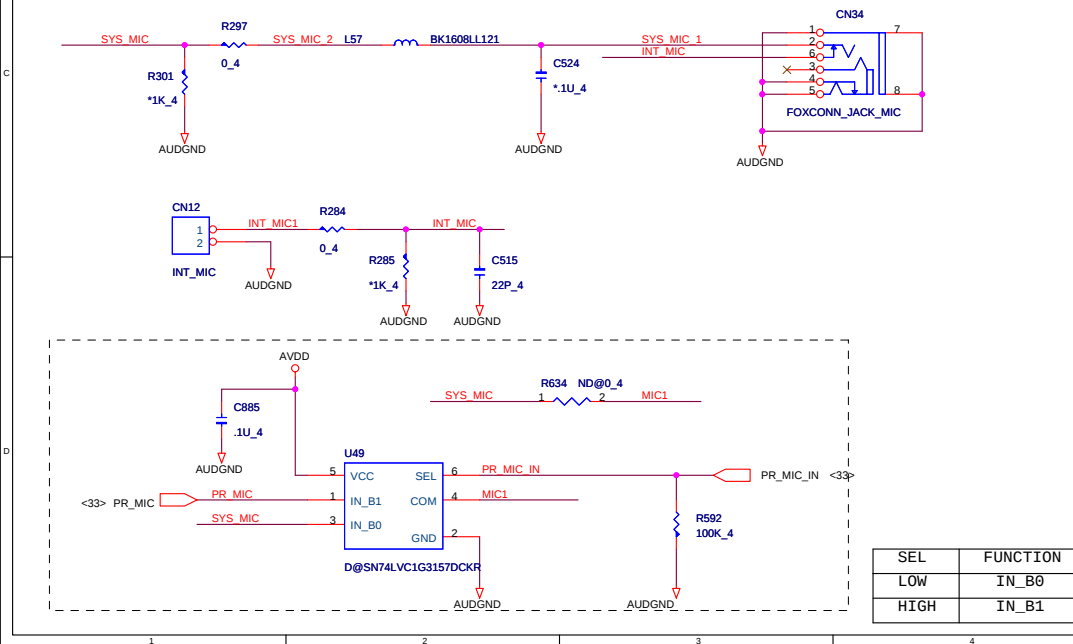
ADD CIRCUITS WHEN NO DOCKING



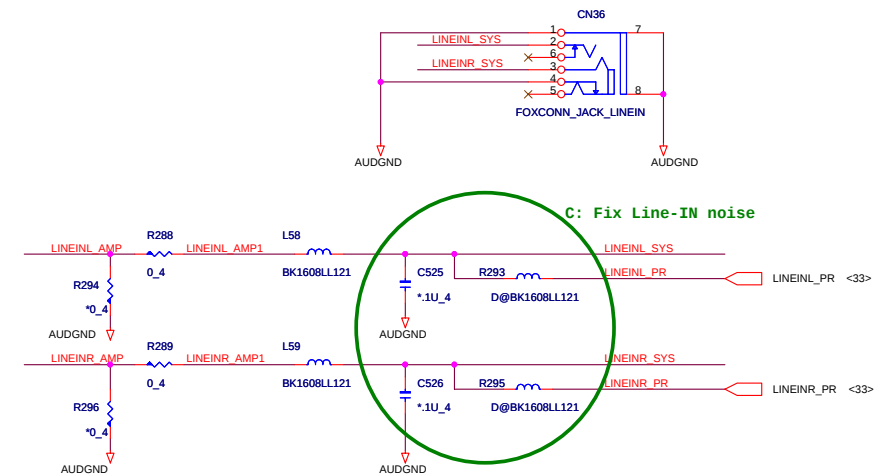
The AMC20463-004 modem is used for mother board family MBAMC20463-004.



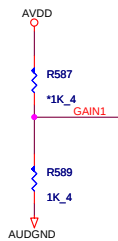
MIC



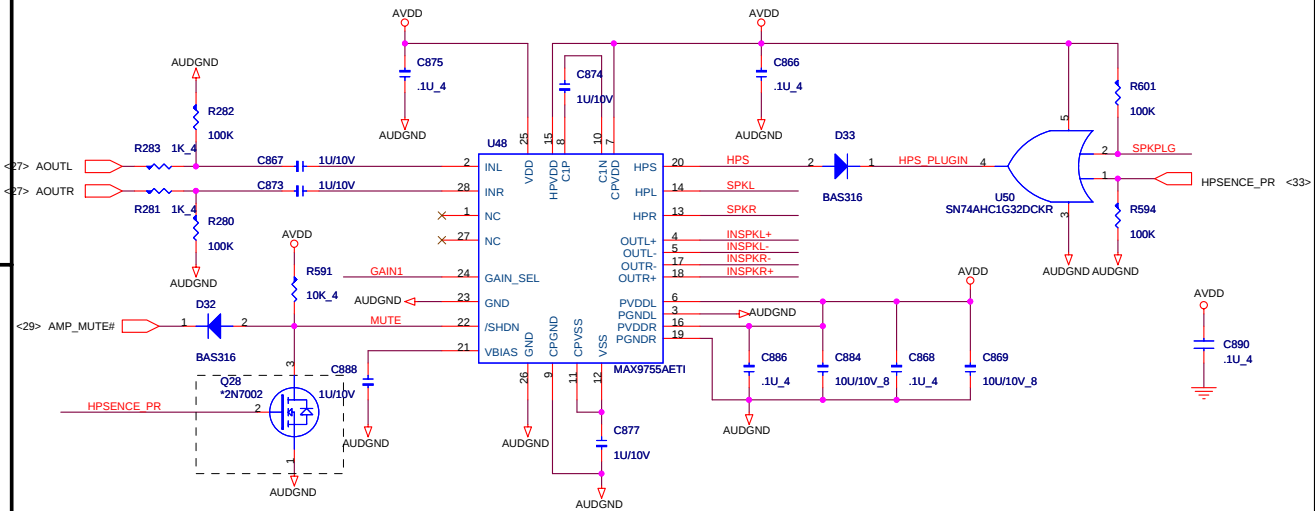
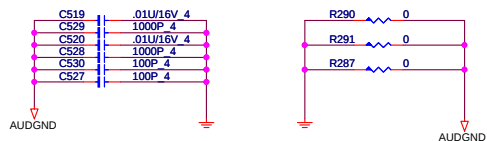
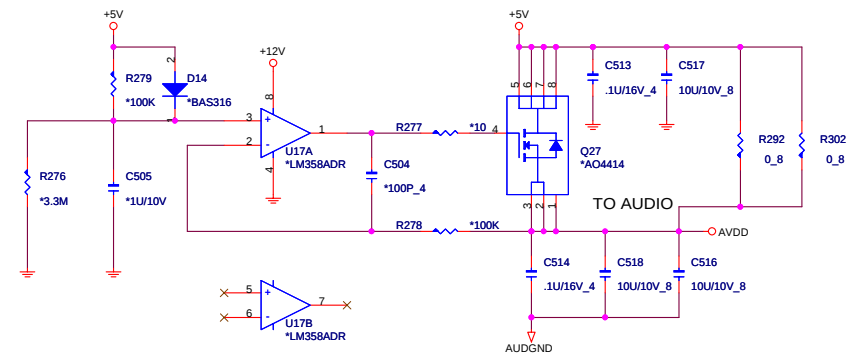
LINE IN



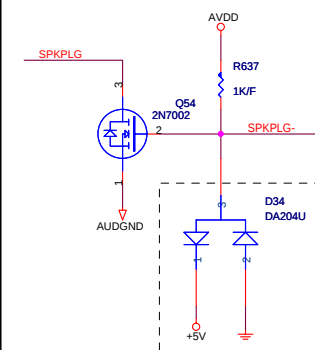
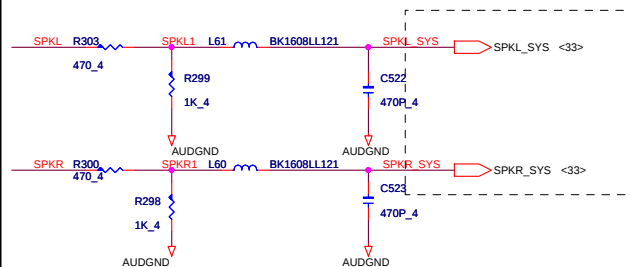
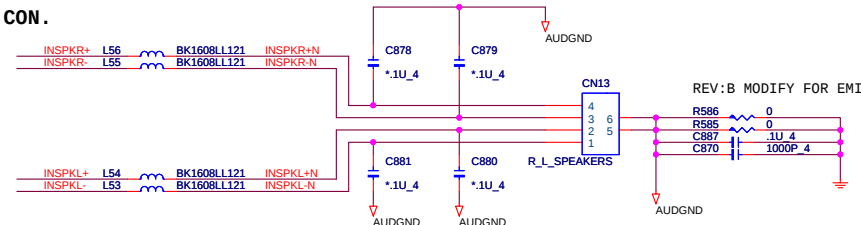
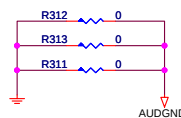
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



AMP POWER

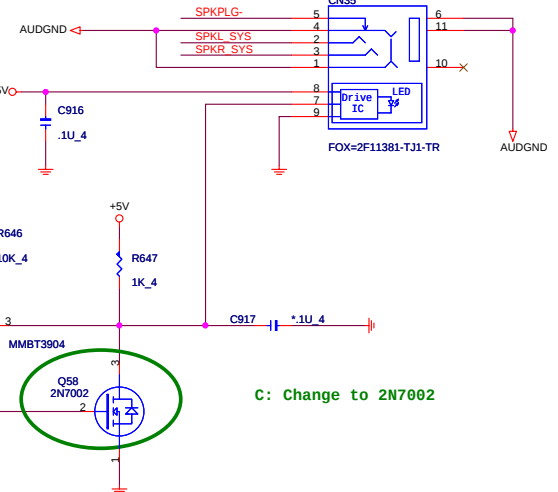


SPEAKER CON.

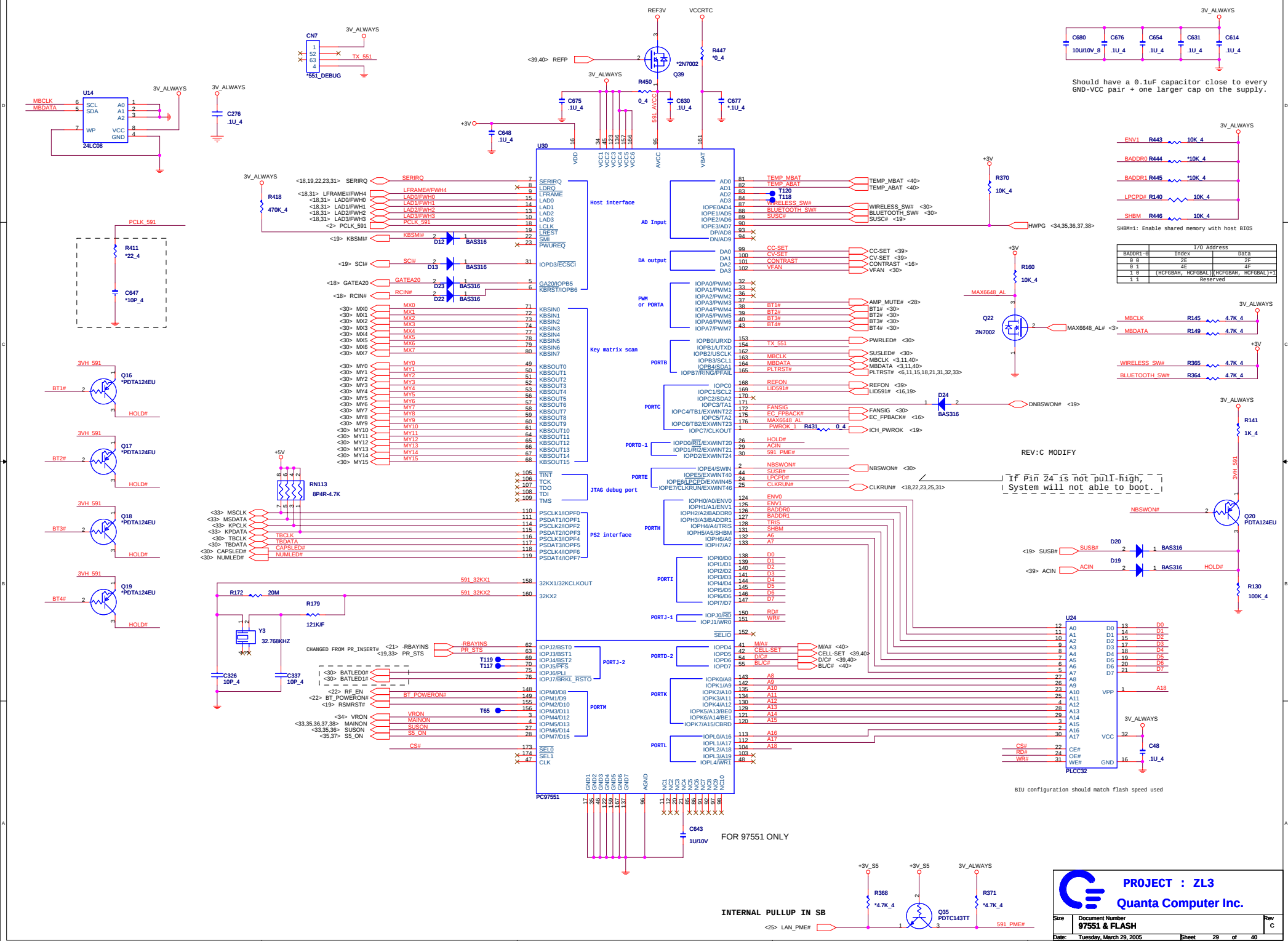


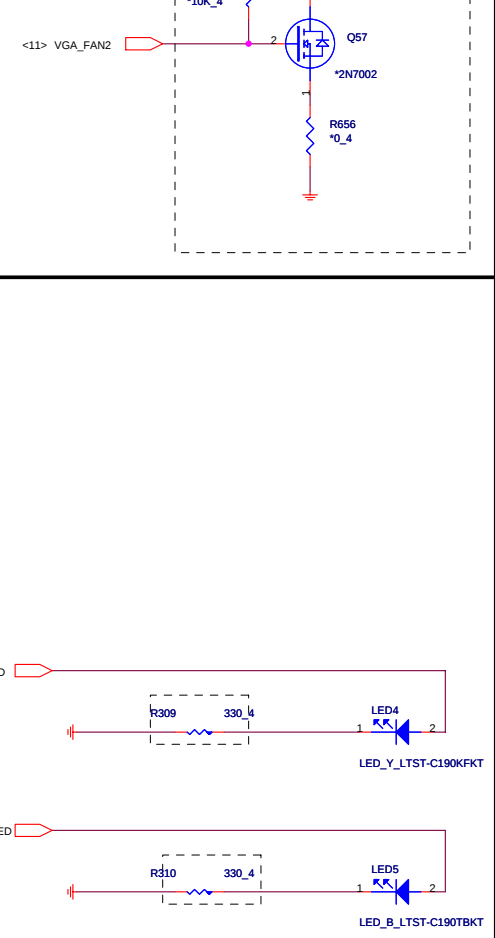
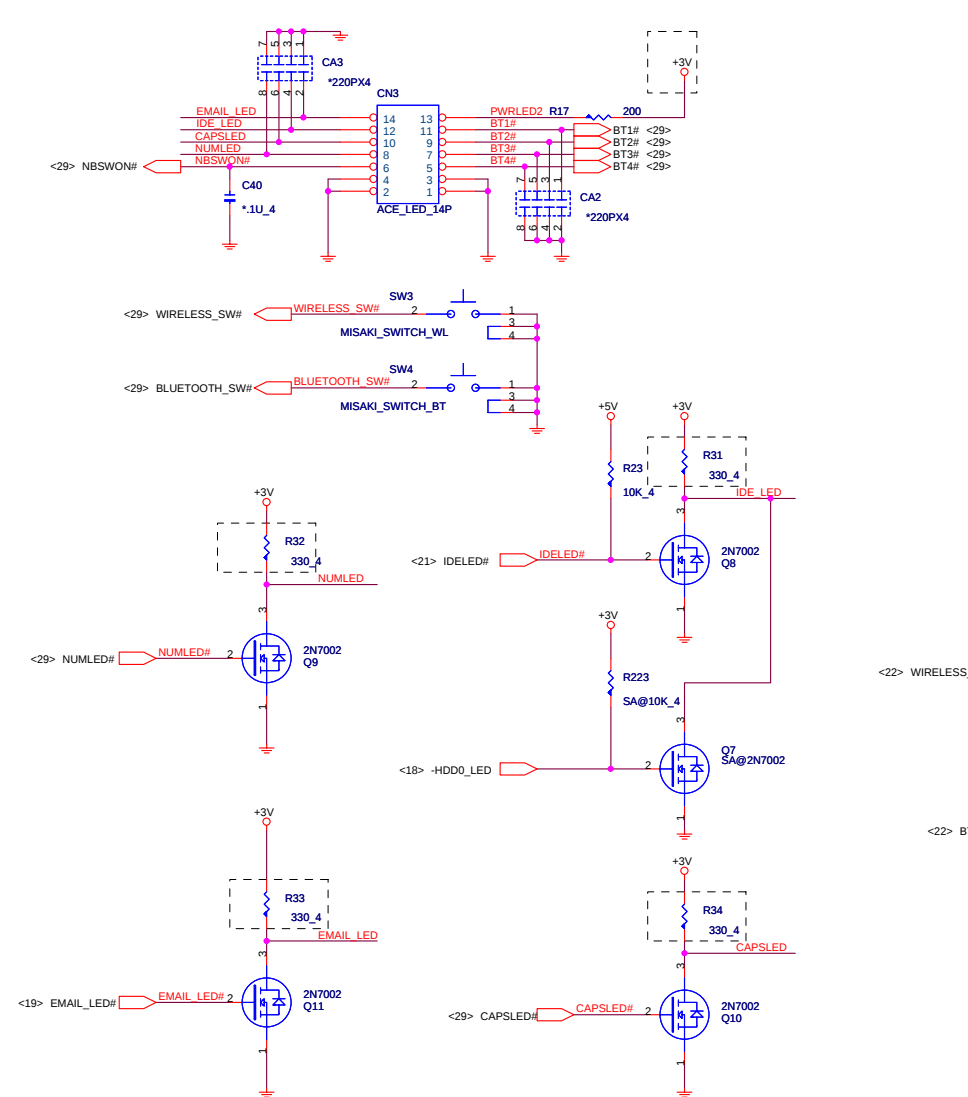
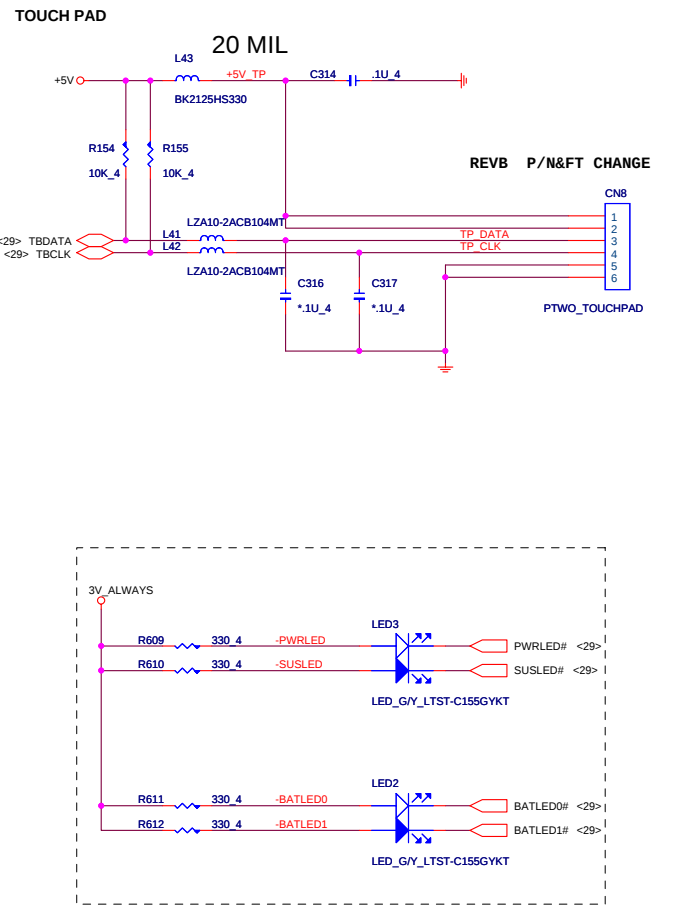
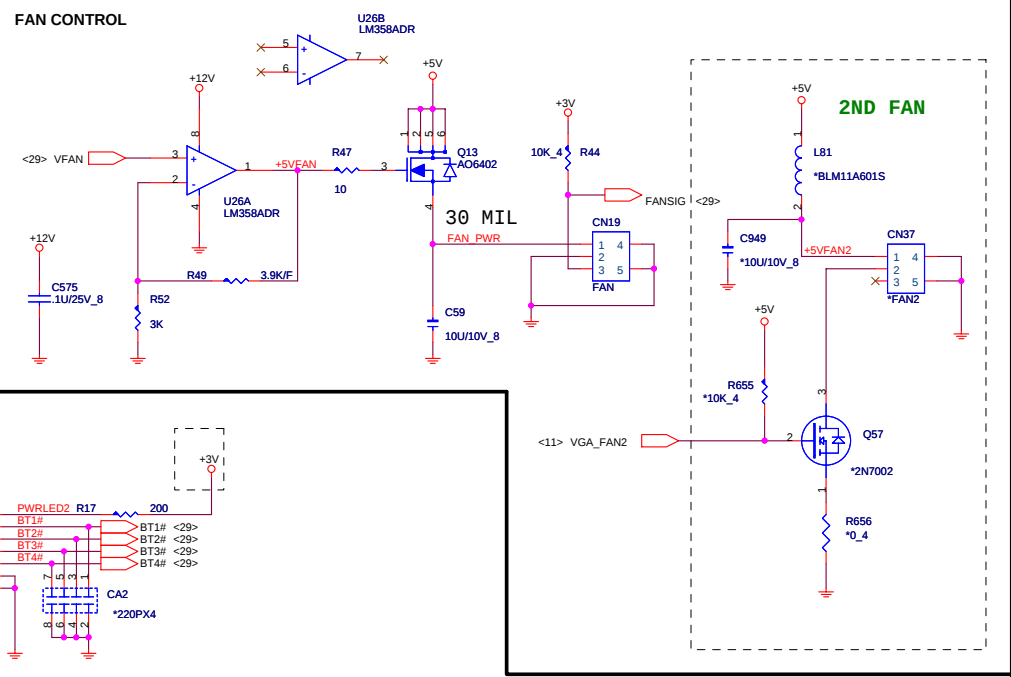
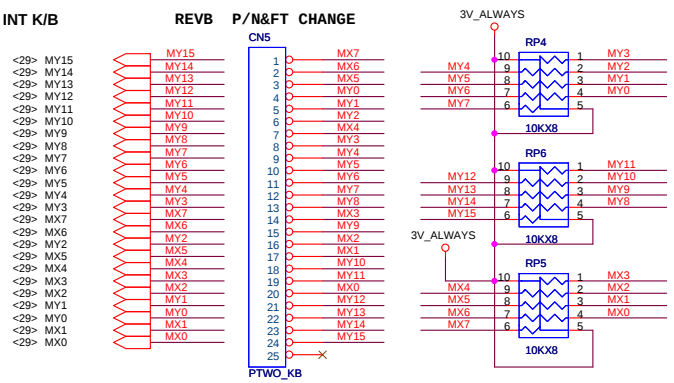
F: NEW ADD FOR ESD
CLOSE TO CN35

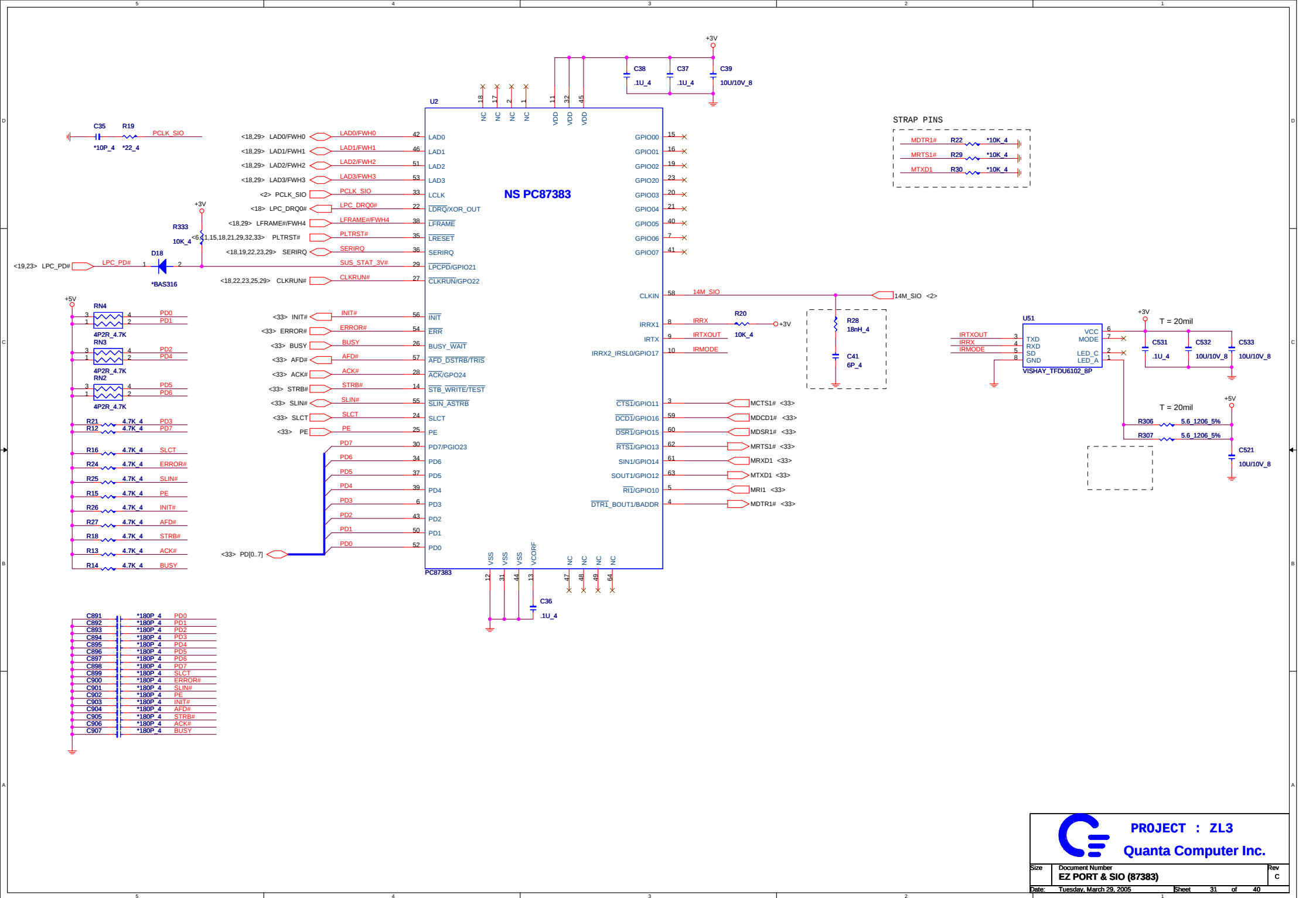
LINE OUT&SPDIF



PROJECT : ZL3
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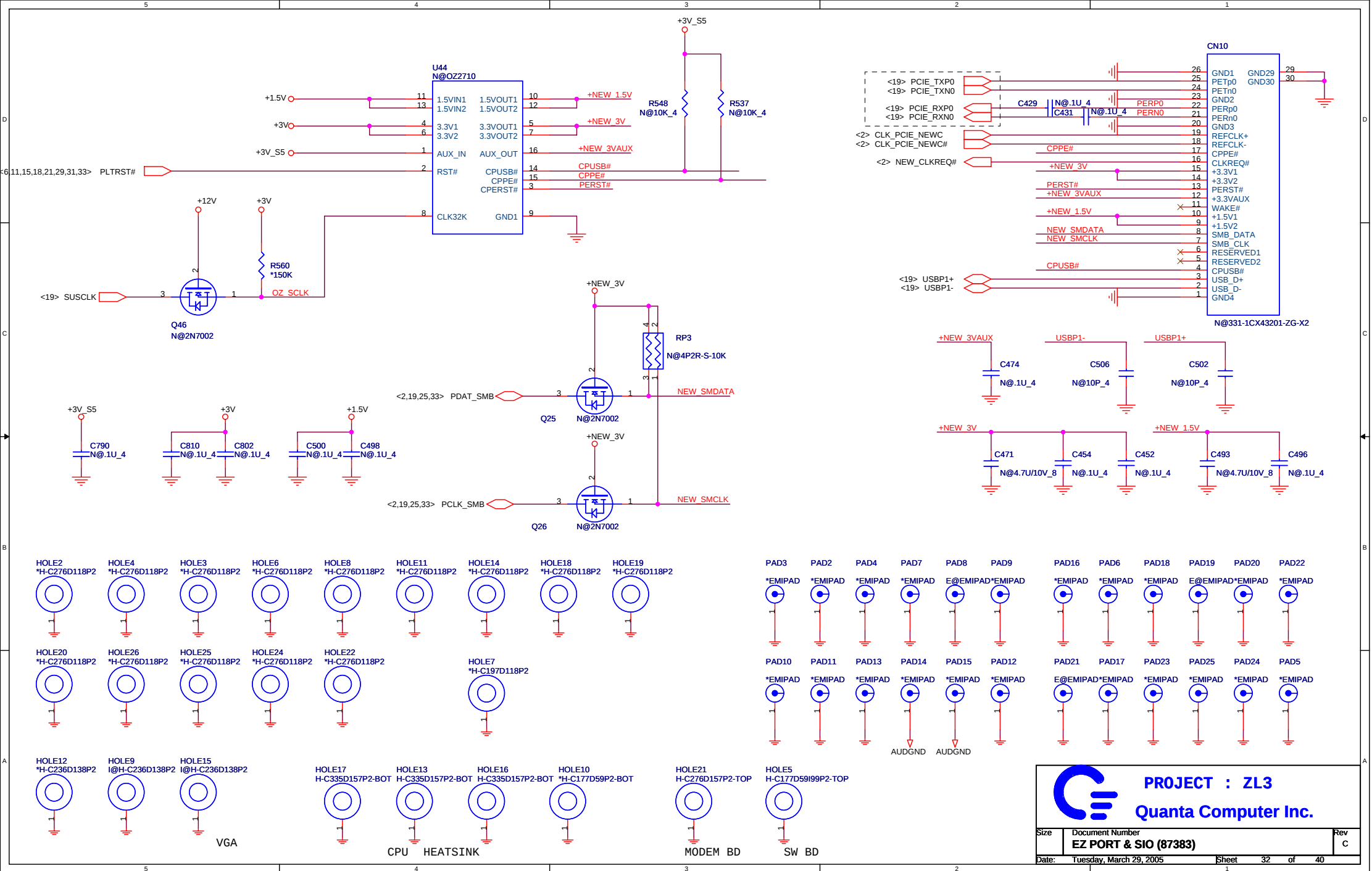


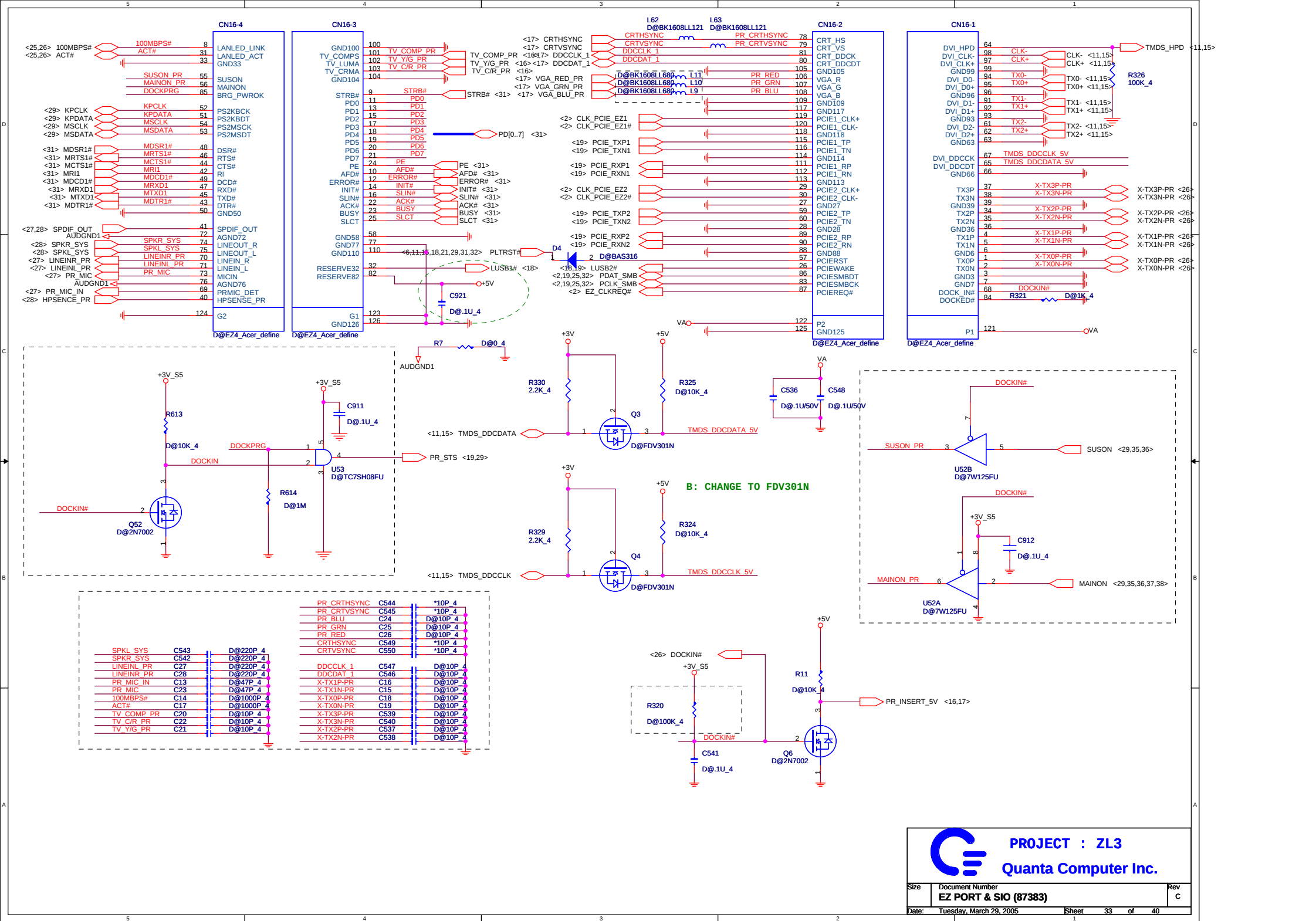


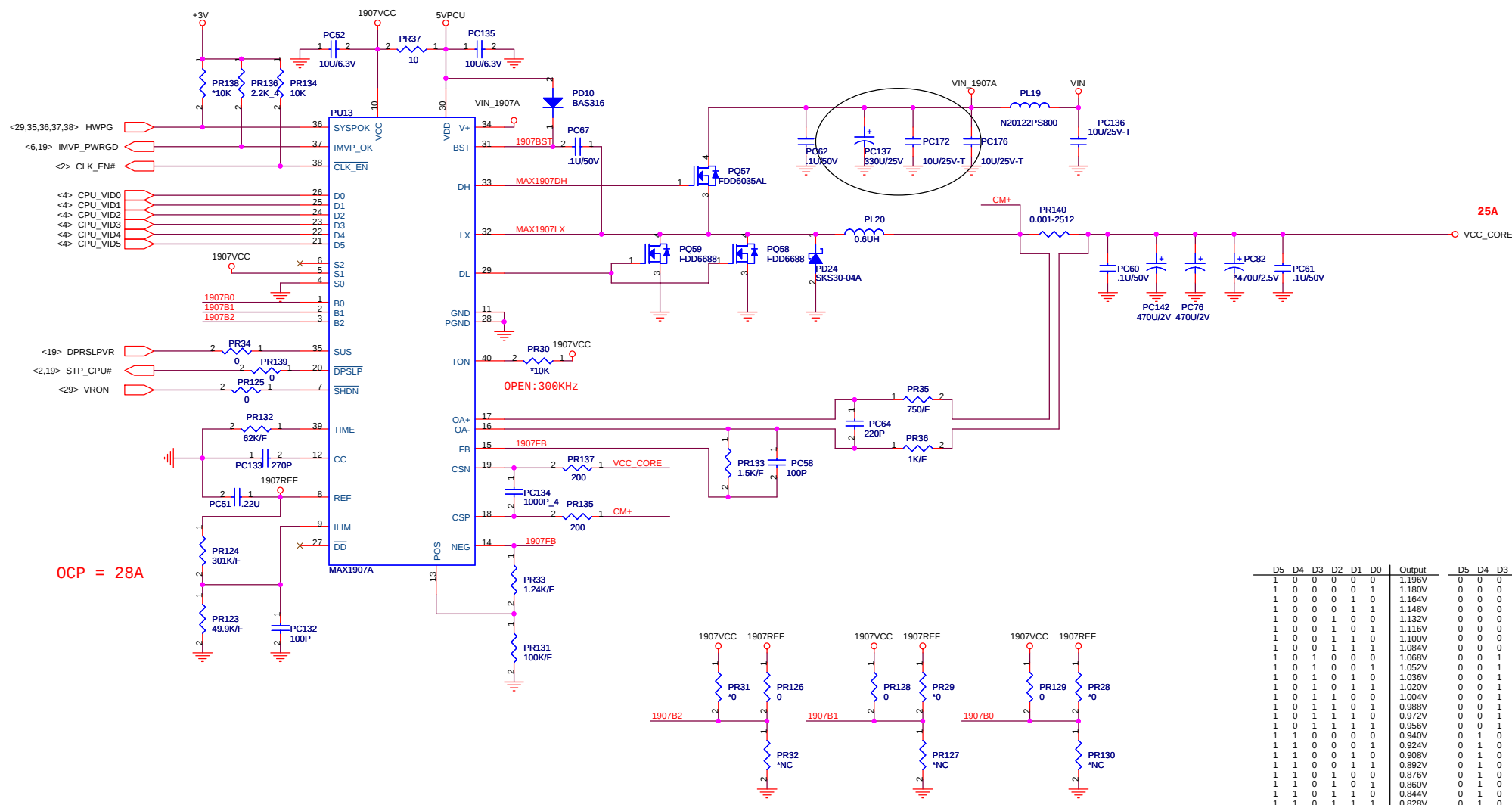


PROJECT : ZL3
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Size	Document Number	Rev
	EZ PORT & SIO (87383)	C
Date:	Tuesday, March 29, 2005	Sheet 31 of 40







OCP = 28A

OPEN: 300KHZ

SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
✓ OPEN	VCC	GND	0.748V

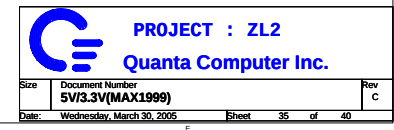
VCC_BOOT

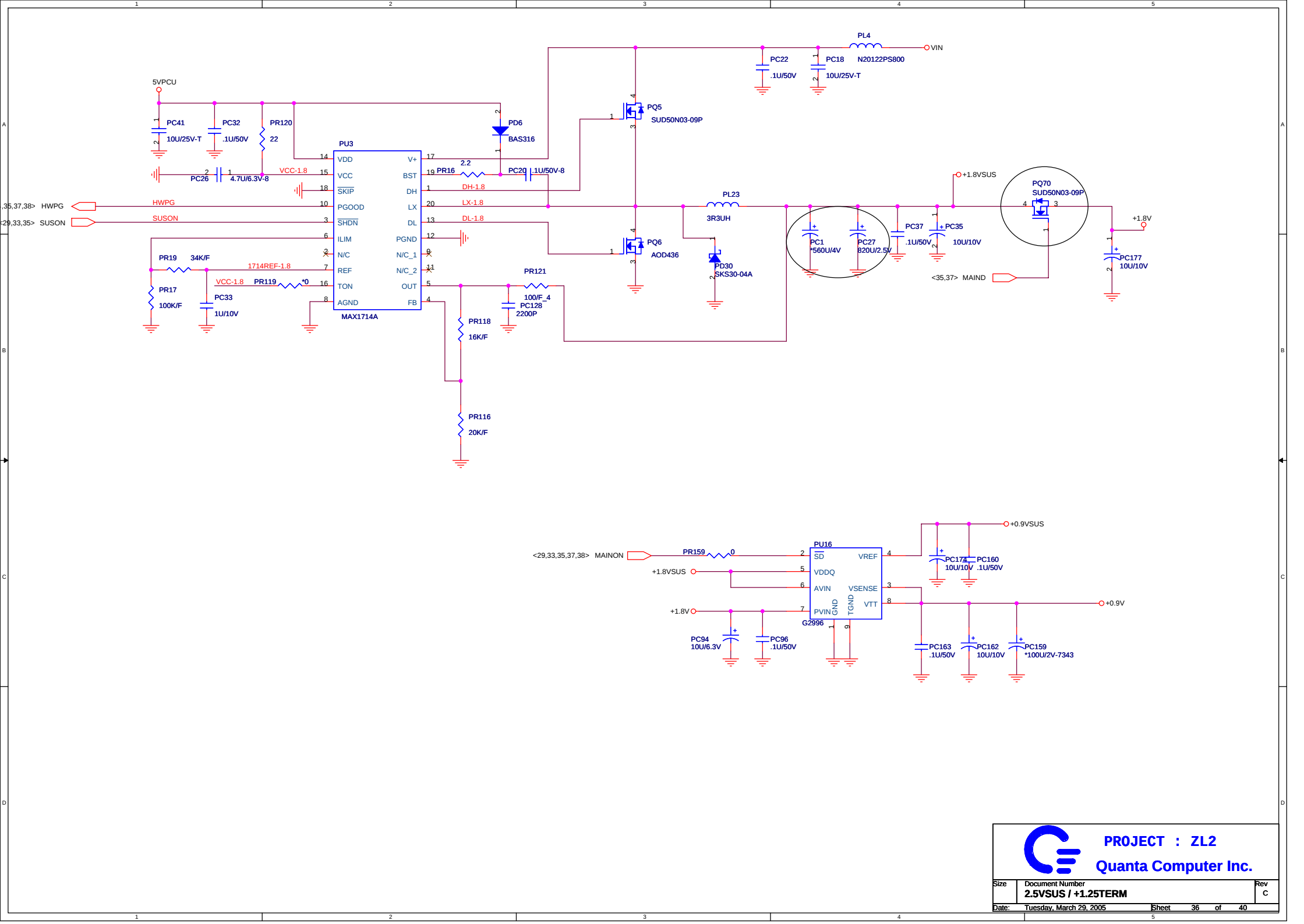
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
✓ VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

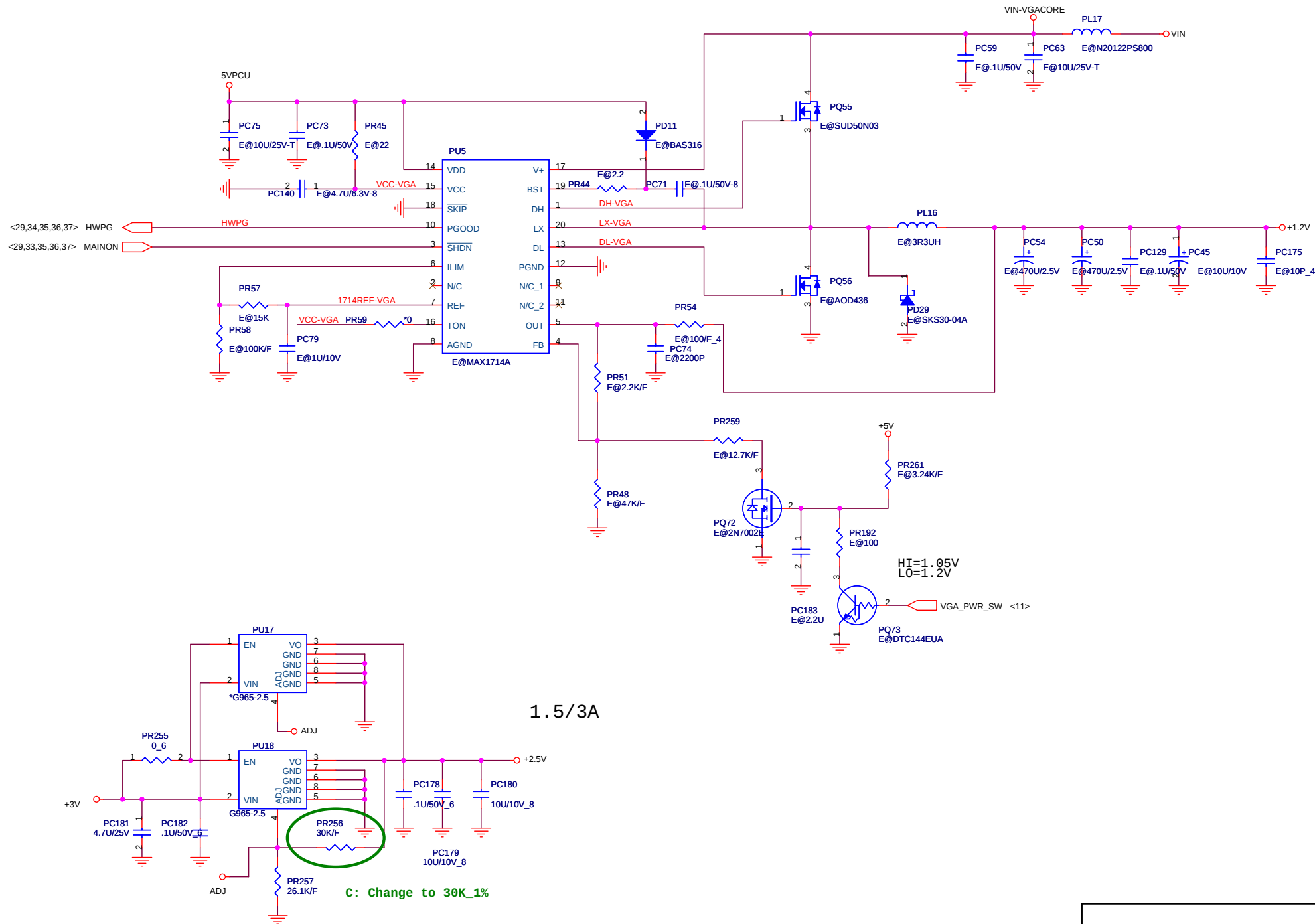
D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	1	0	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

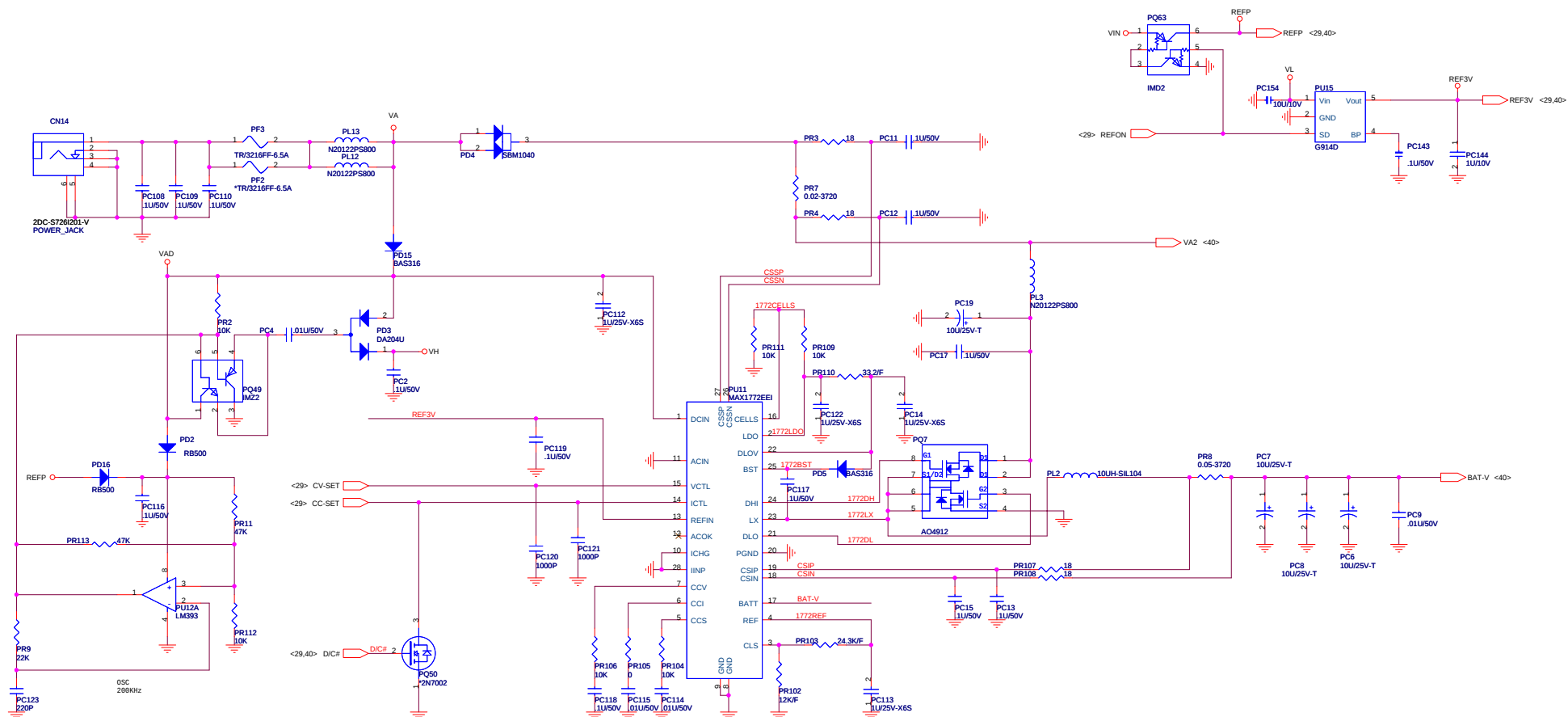
PROJECT : ZL2
Quanta Computer Inc.

Size	Document Number	Rev
	CPU CORE (MAX1907)	C
Date:	Wednesday, March 30, 2005	Sheet 34 of 40





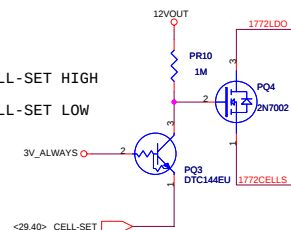




FOR 120W 6.2A



FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET LOW





 PROJECT : ZL2 Quanta Computer Inc.		
Size	Document Number BATTERY SELECT	Rev C
Date:	Tuesday, March 29, 2005	Sheet 40 of 40