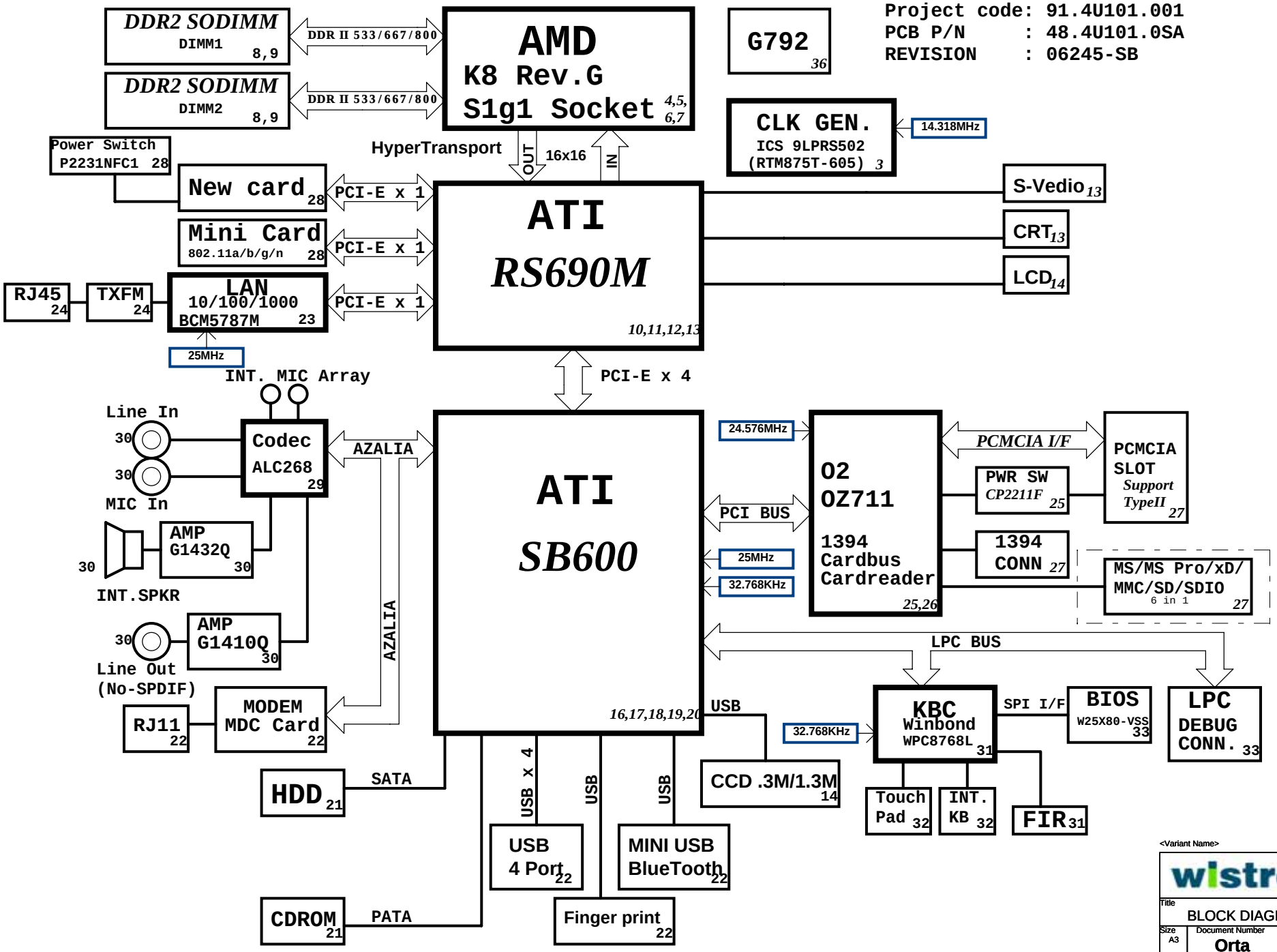
Orta Block Diagram



PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 1 of 46

SA: 07/31/06 Start

SB change
power team
1.change L7, L9 to 68.1R510.10D
2.changge U12 to 84.04706.037
3.change R66 to 10K ohm

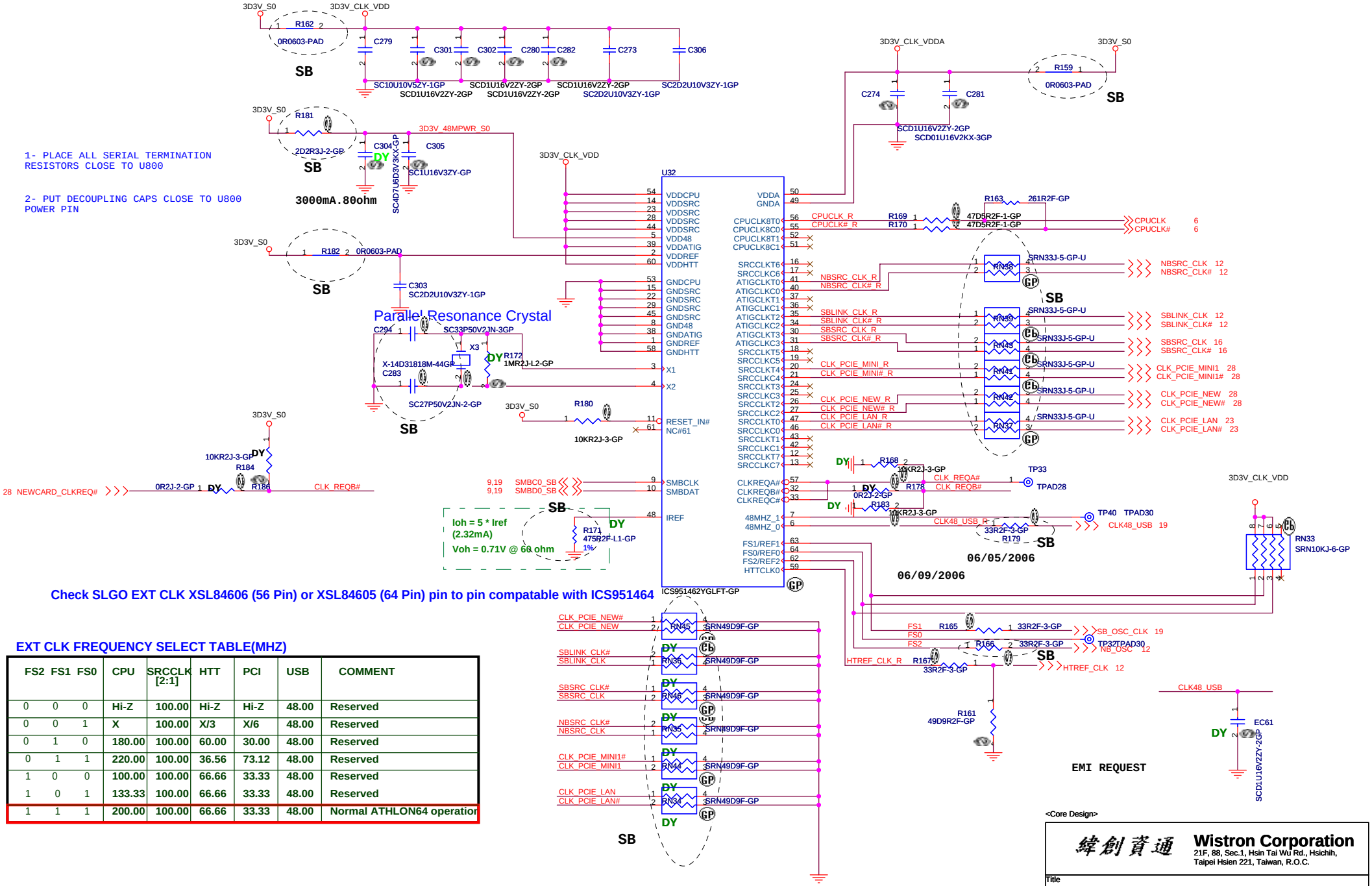
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 2 of 46



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

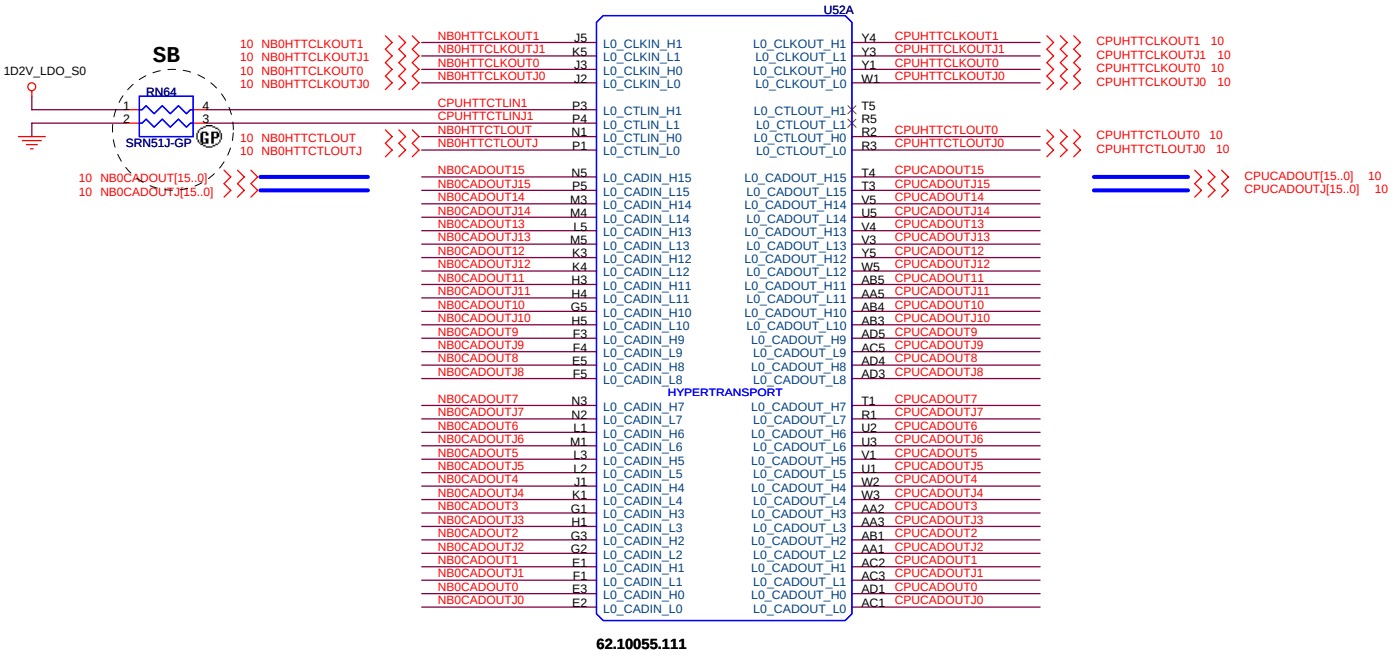
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951412

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 3 of 46



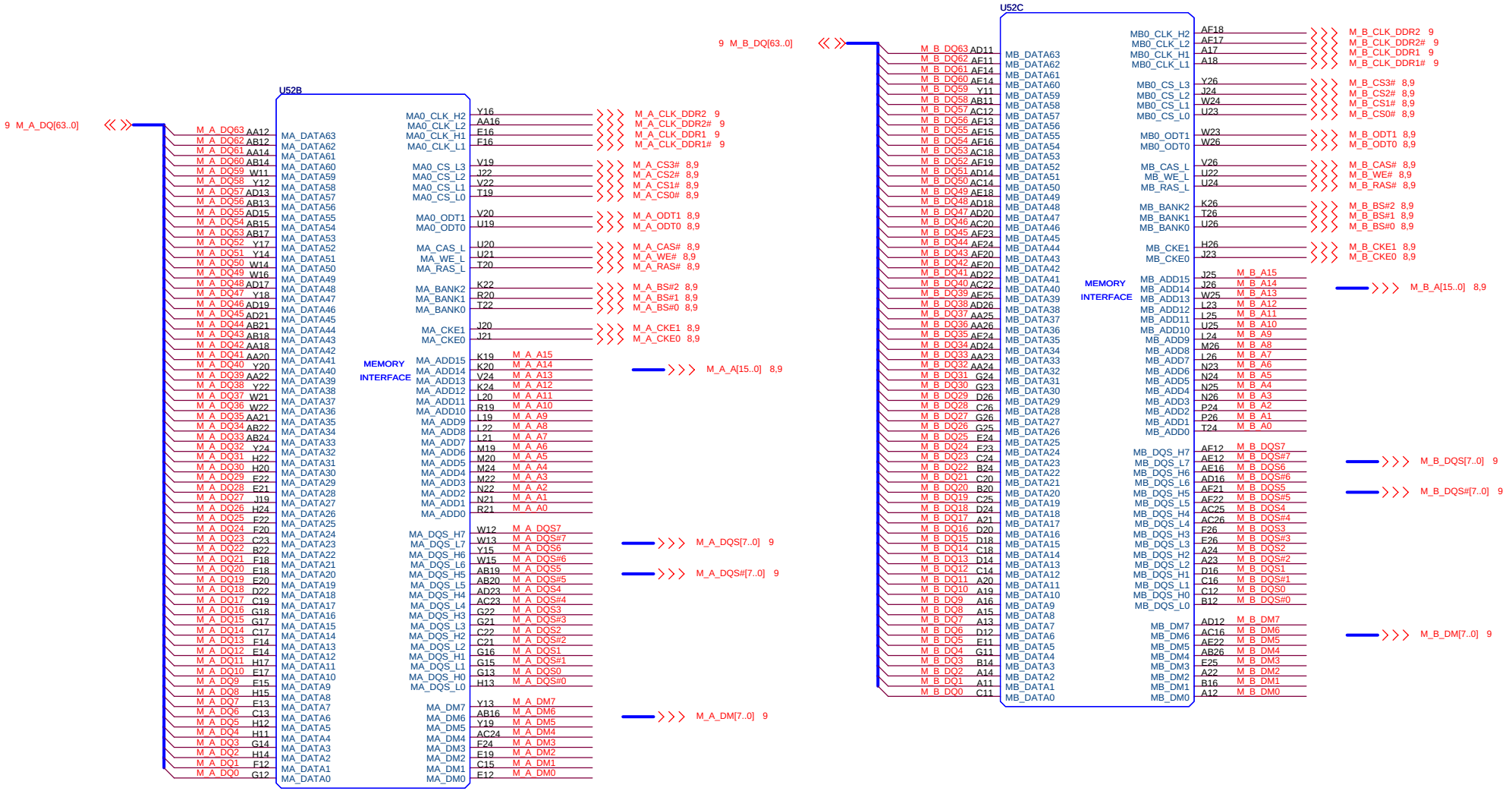
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(1/4)_HyperTransport I/F

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 4 of 46



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(2/4)_DDR**

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 5 of 46

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS_NOT_GOOD ENOUGH, TRY 68.00082.491

Near To CPU

20061031 for Power Test

Remove these resistor when using EVT CPU

Change;Add

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

VREF_DDR_CLAW

LAYOUT: Locate close to CPU.

HDT Connectors

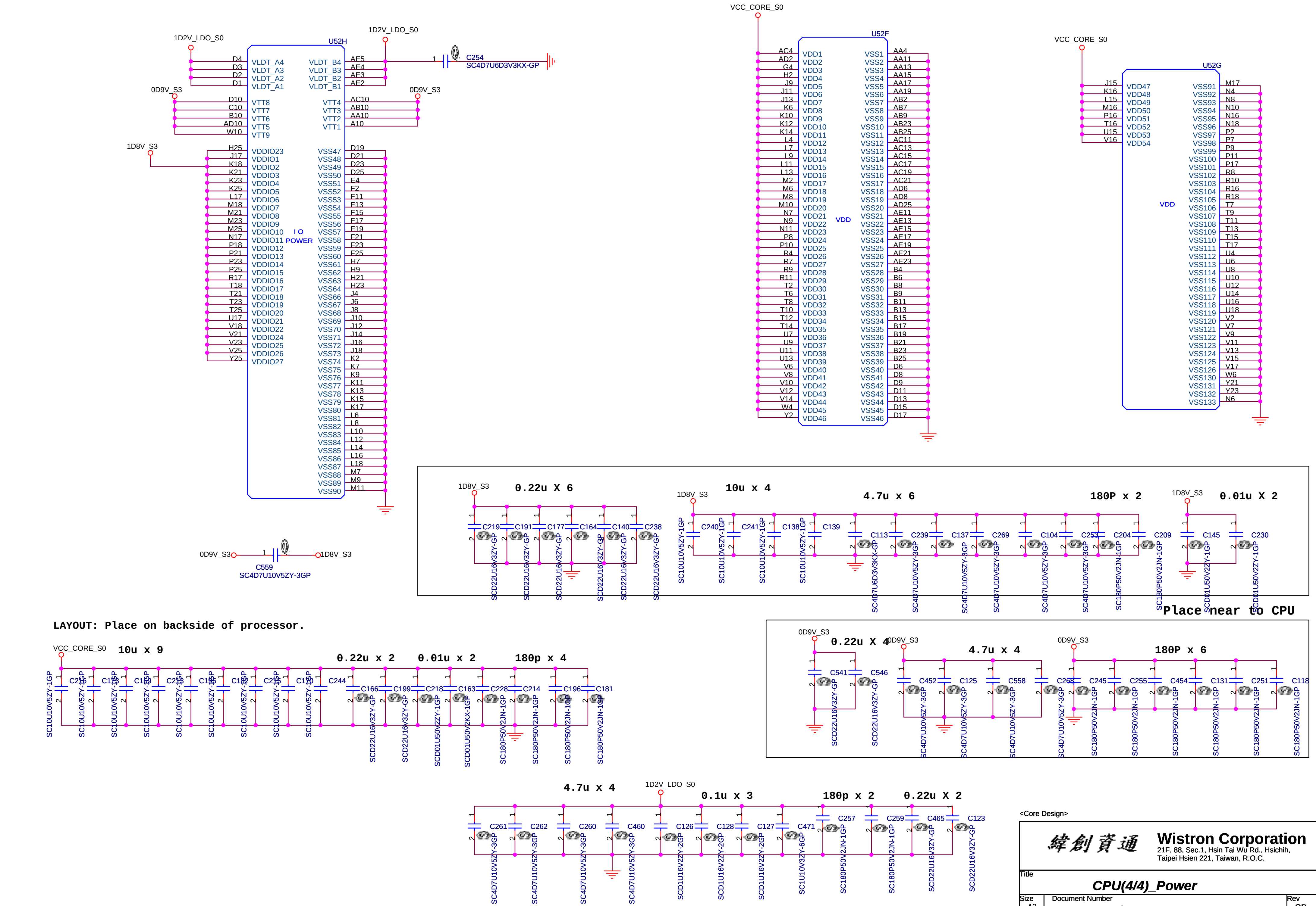
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 6 of 46



<Core Design>

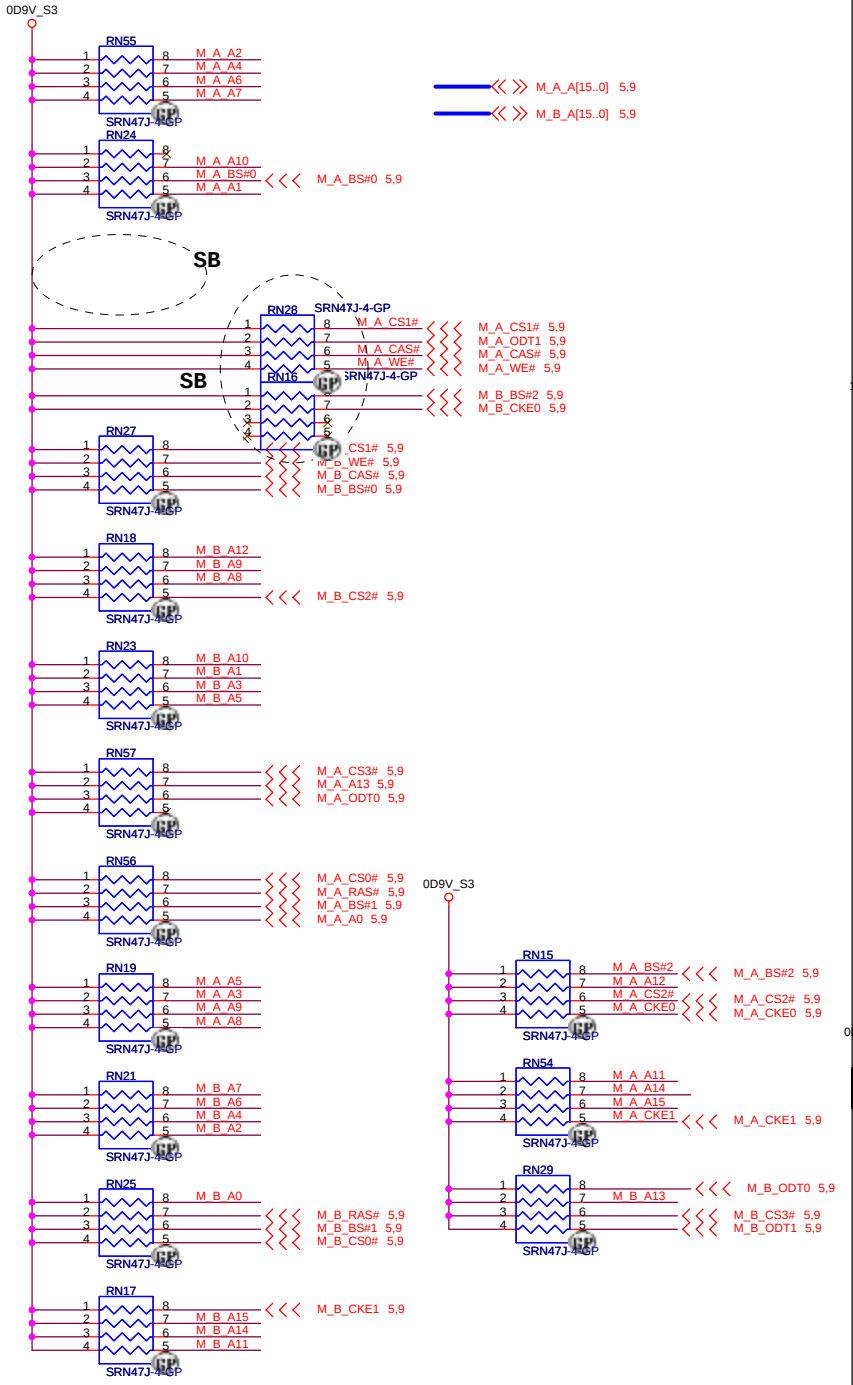
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU(4/4)_Power			
Size: A3	Document Number: Orta		Rev: SB
Date: Friday, January 12, 2007	Sheet 7 of 46		

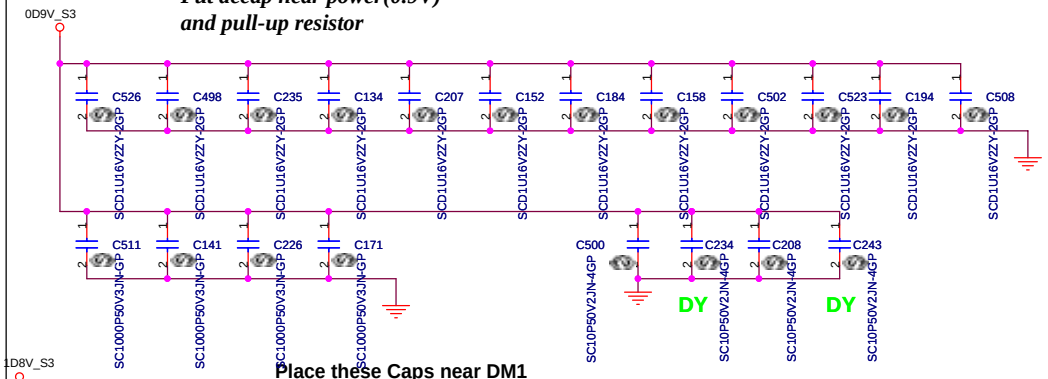
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

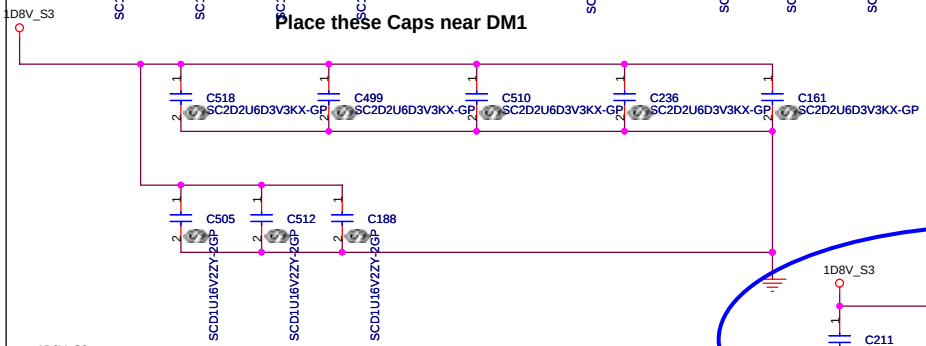


Decoupling Capacitor

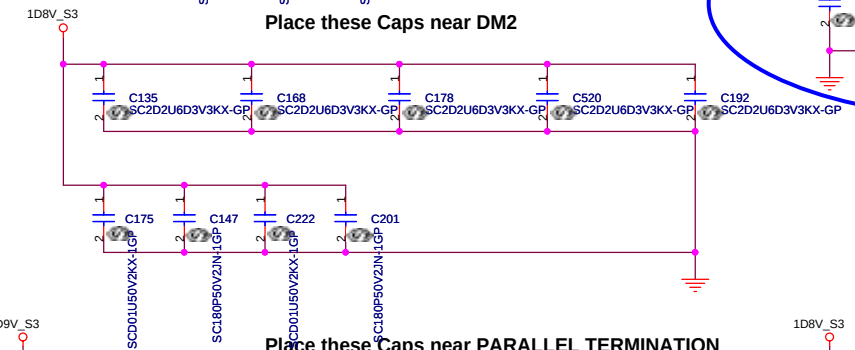
Put decap near power(0.9V) and pull-up resistor



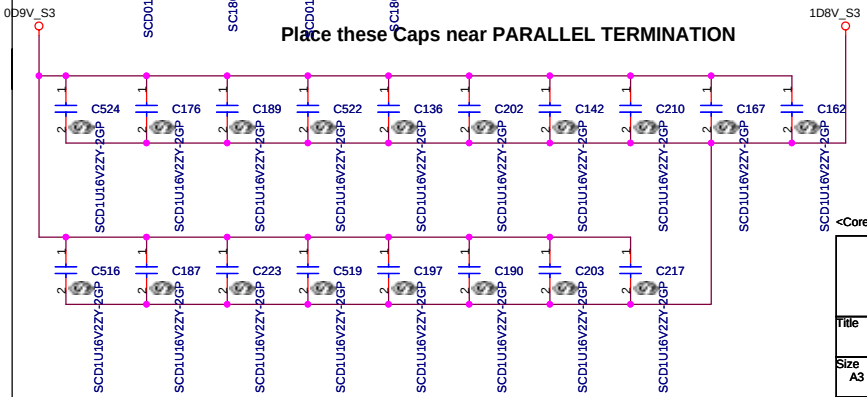
Place these Caps near DM1

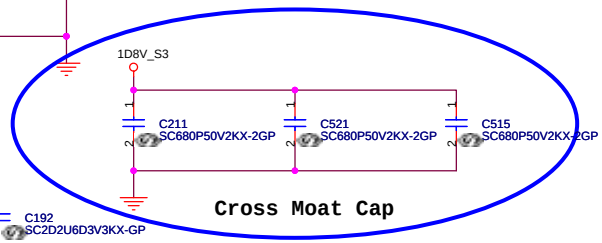


Place these Caps near DM2



Place these Caps near PARALLEL TERMINATION





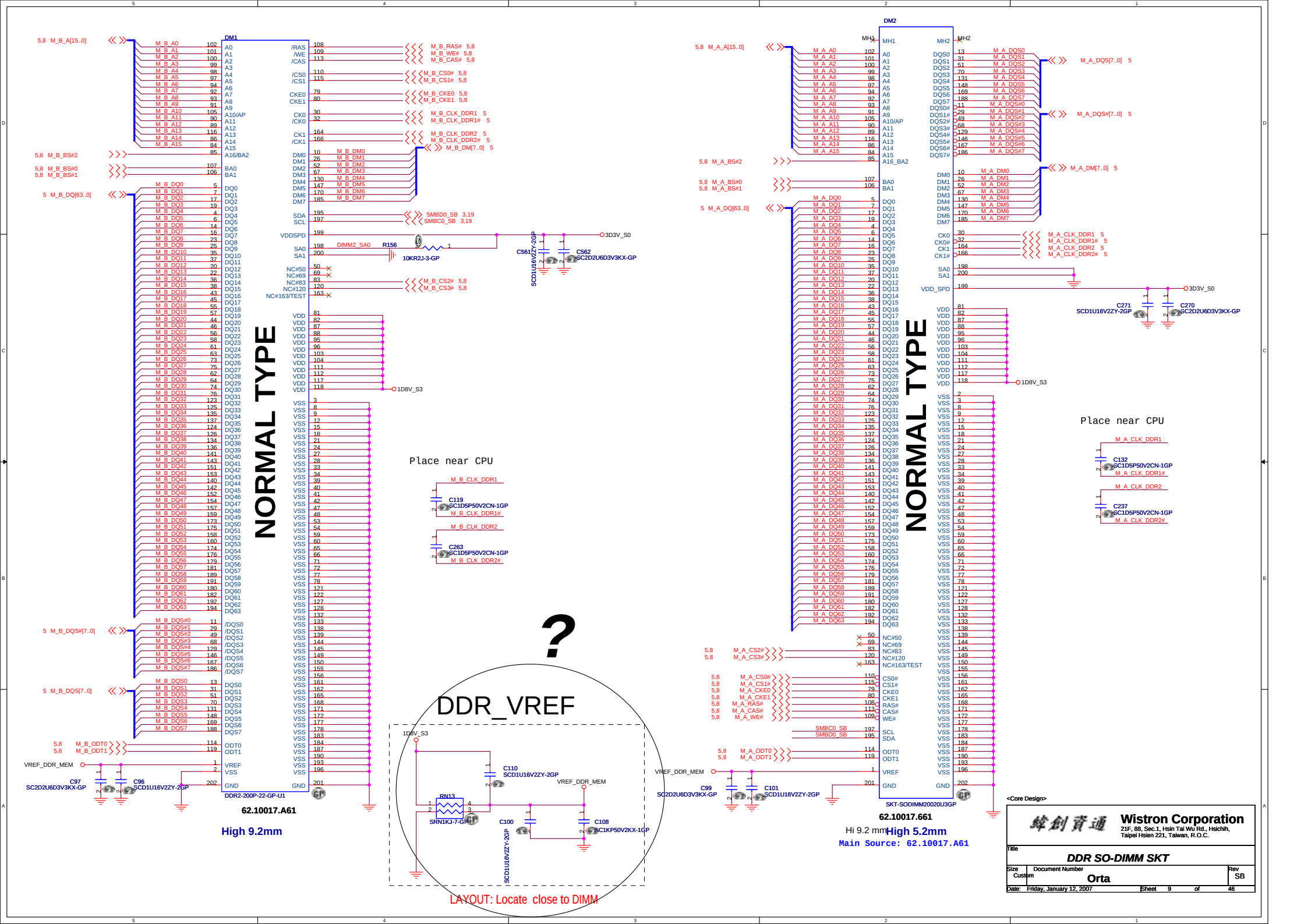
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DAMPING & TERMINATION

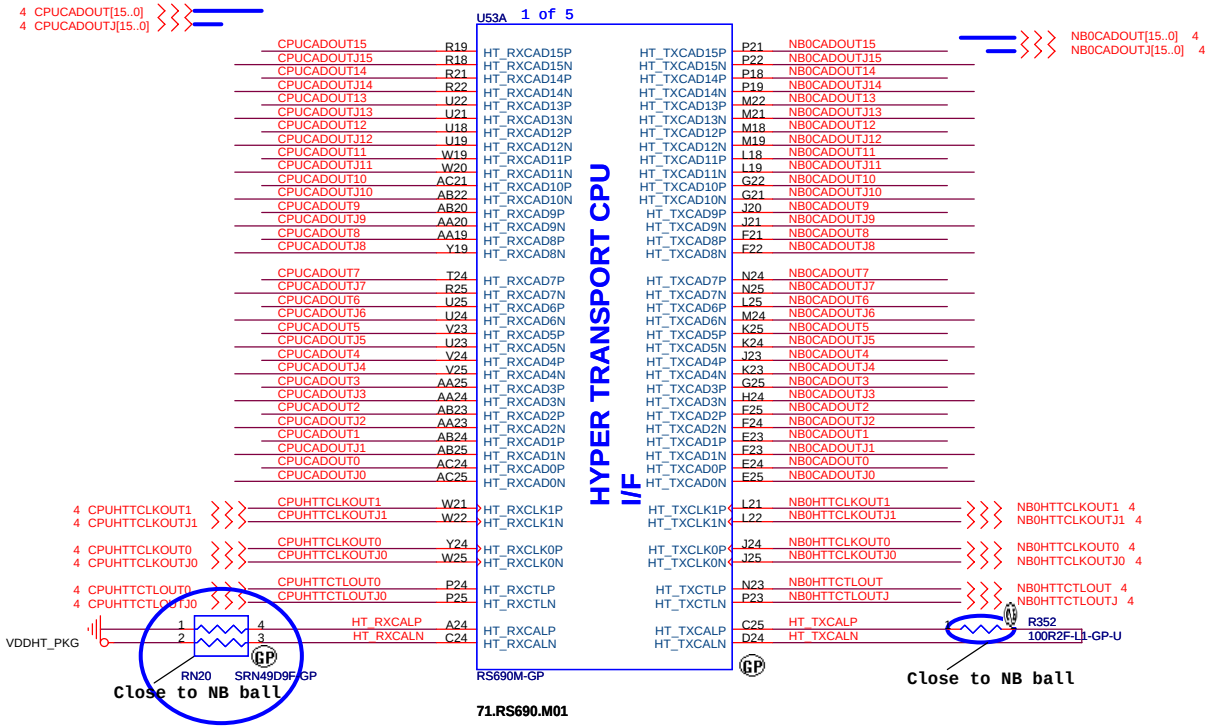
Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 8 of 46


DM1
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
Place near CPU
DDR_VREF
LAYOUT: Locate close to DIMM
DM2
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
Hi 9.2 mm
High 5.2mm
Main Source: 62.10017.A61
Place near CPU
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size
Custom
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 9 of 46

CLAW HAMMER TO NB

NB TO CLAW HAMMER



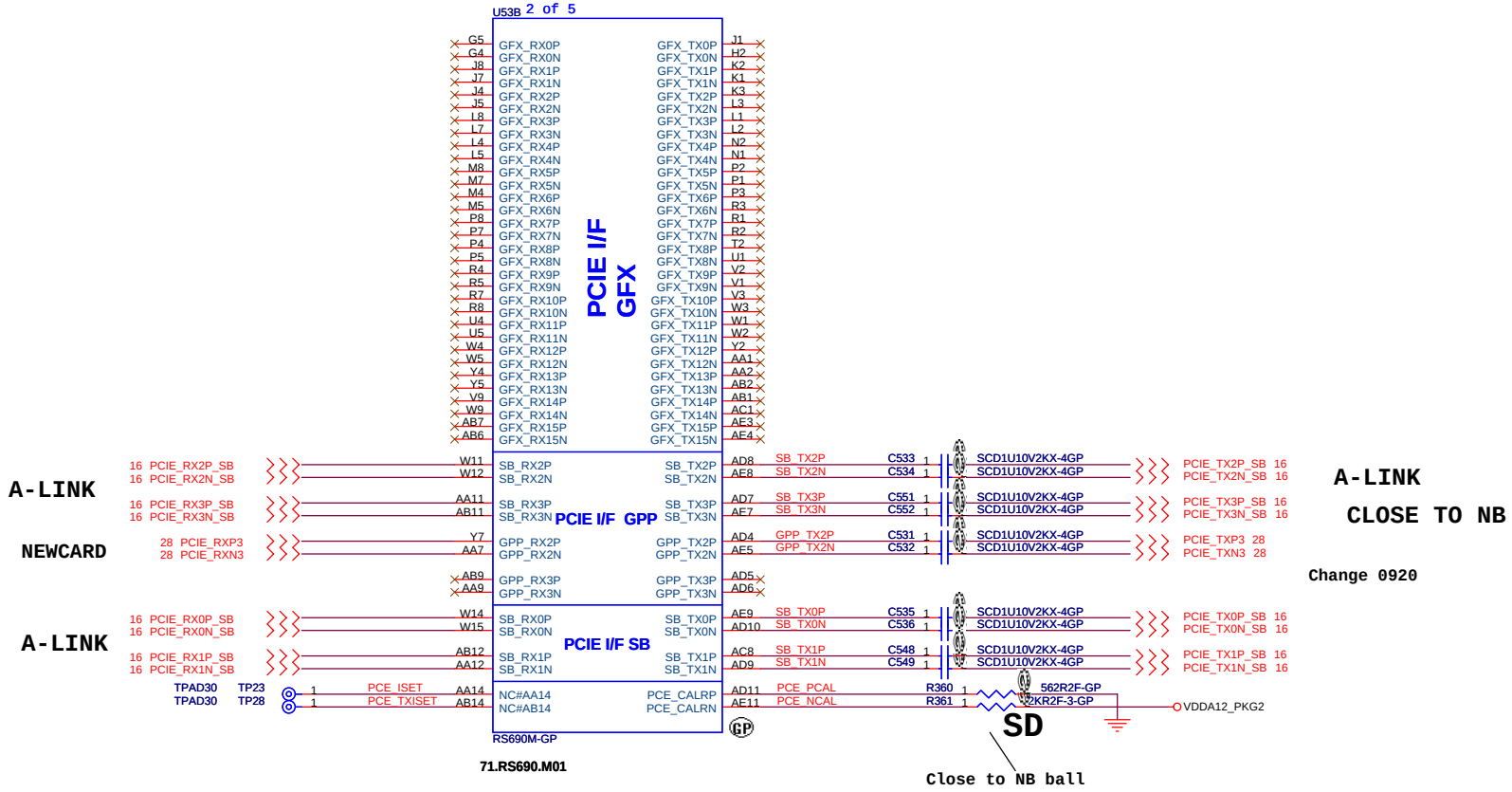
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_HT

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 10 of 46

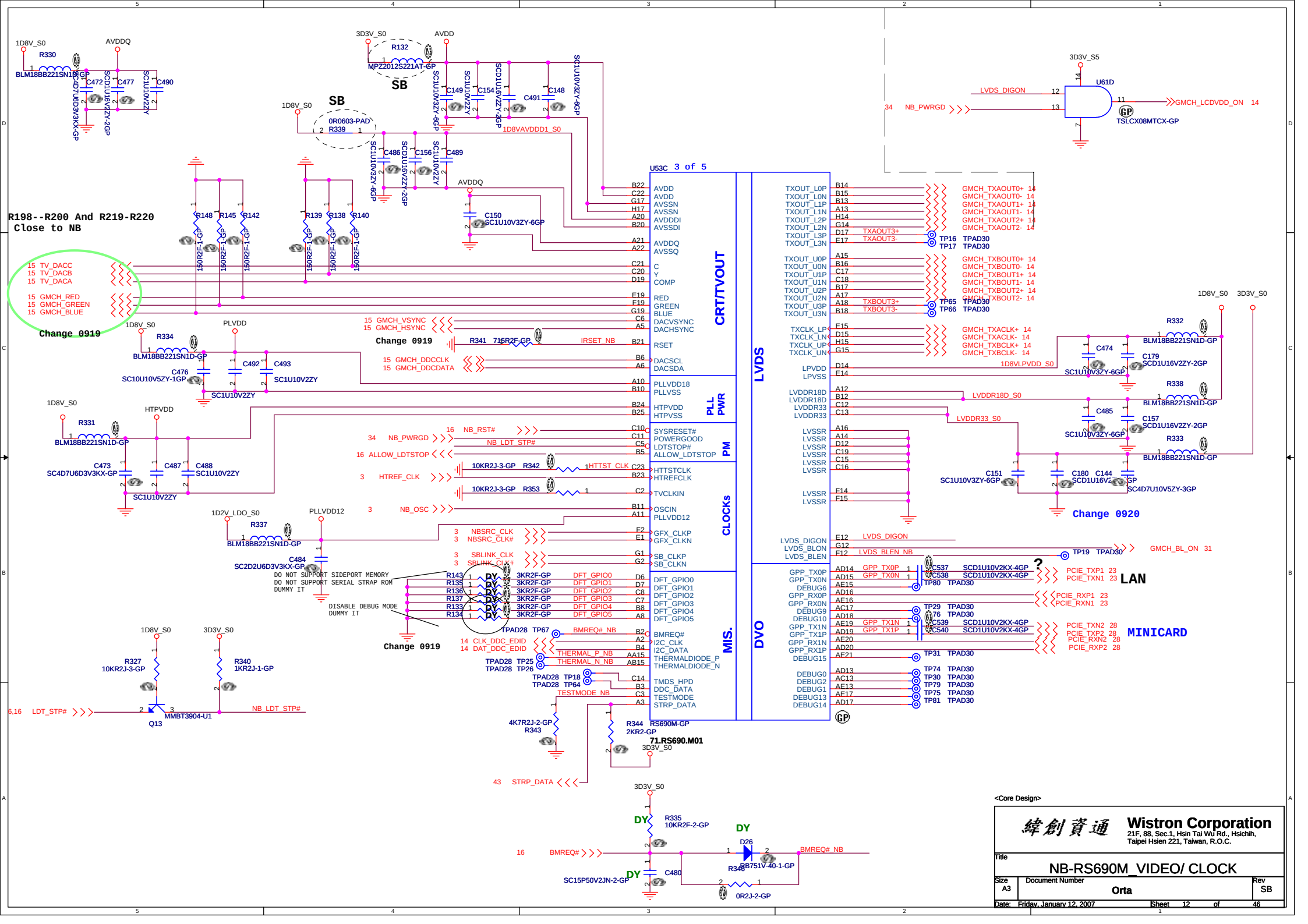


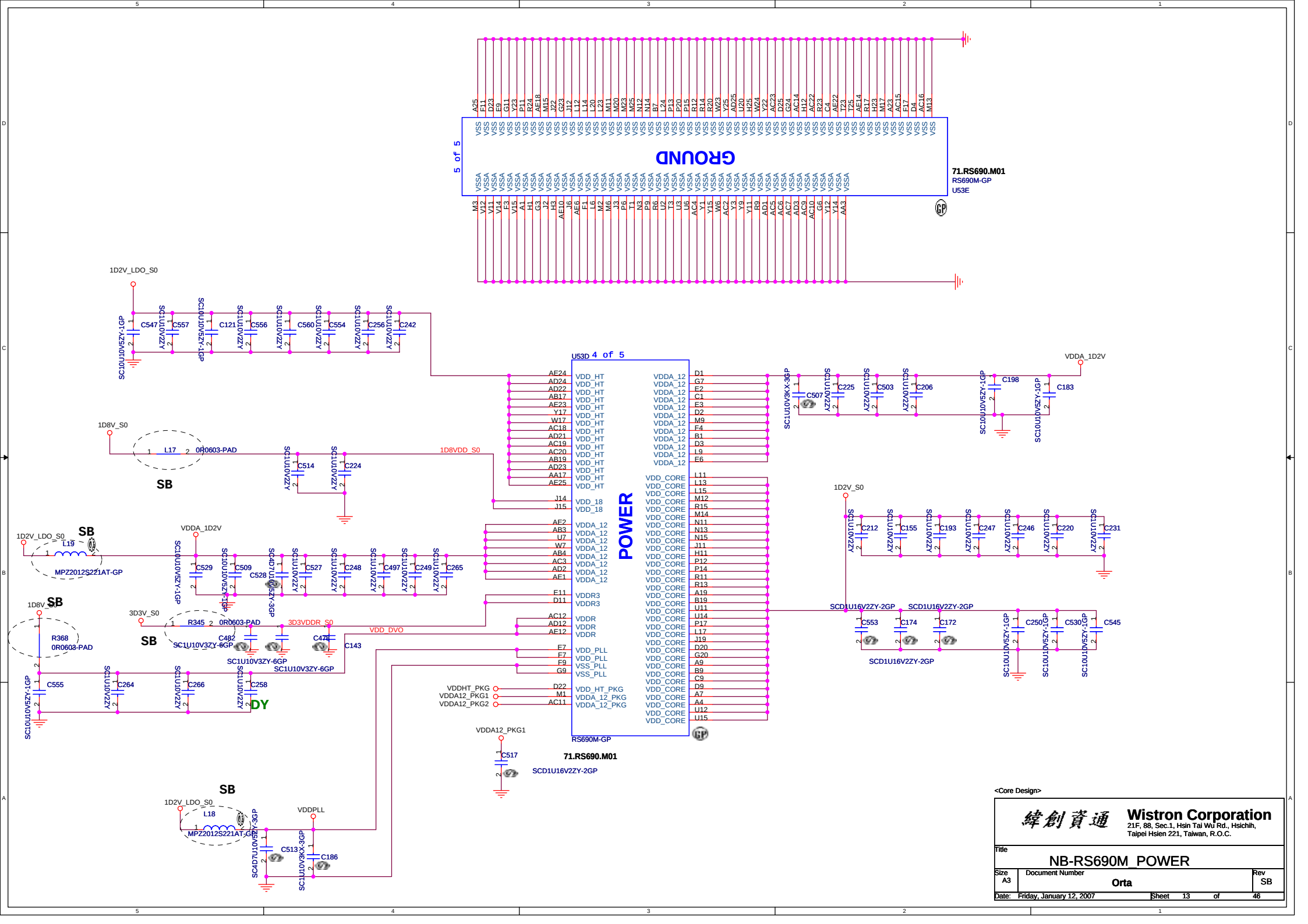
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

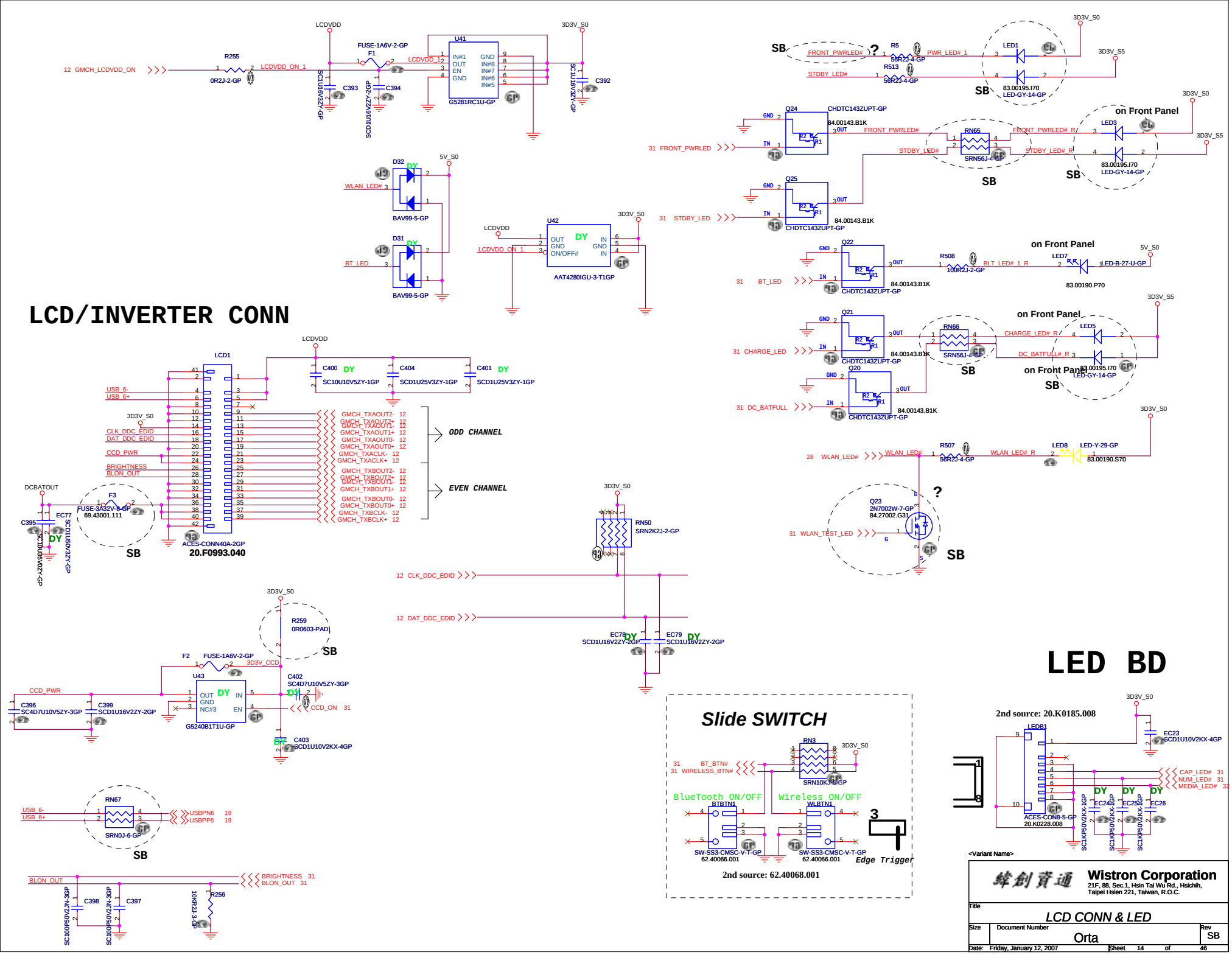
Title: NB-RS690M_MEM/PCIE_LINK I/F

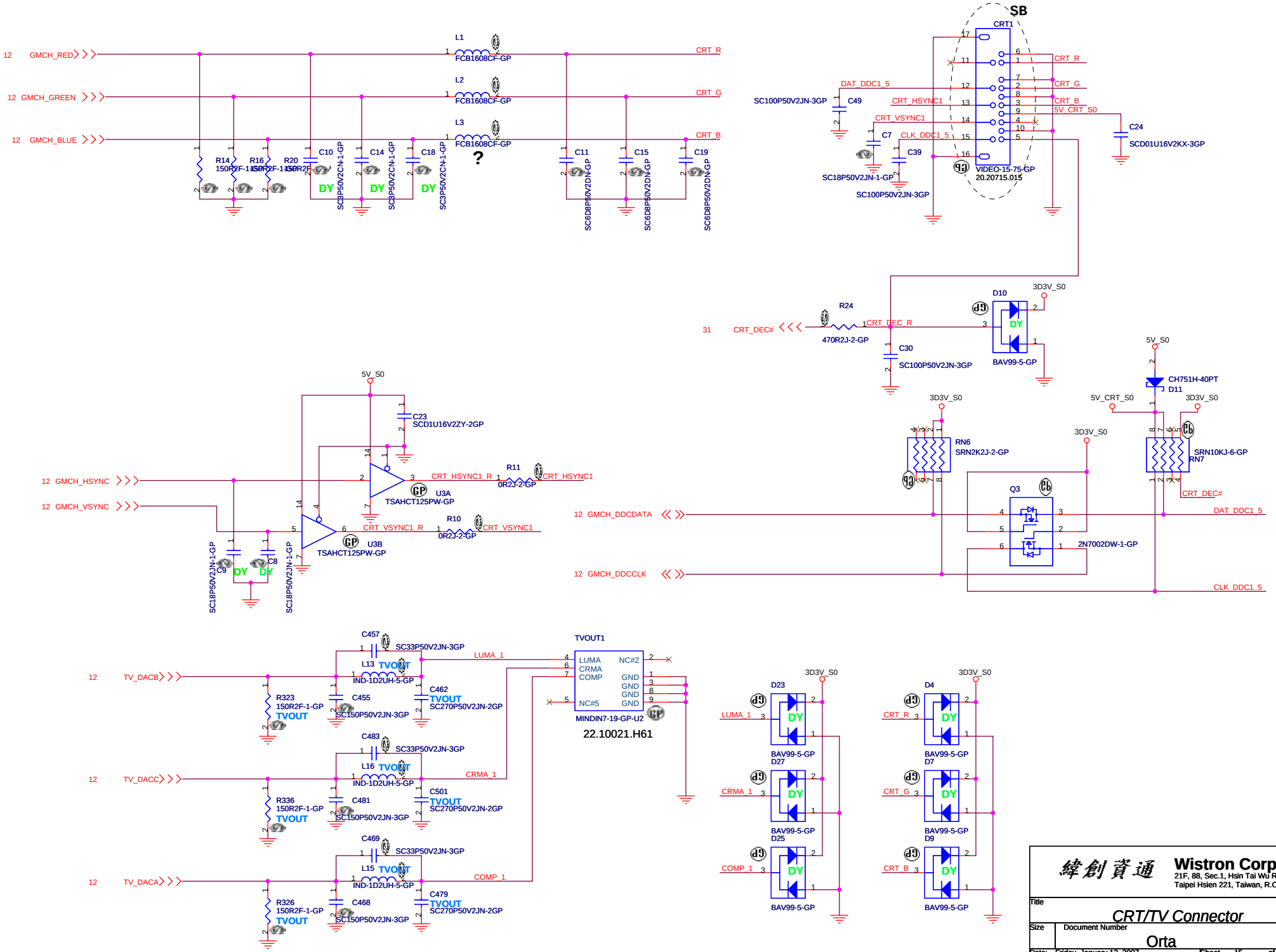
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 11 of 46


R198--R200 And R219-R220
Close to NB
Change 0919
Change 0920
SB
U53C 3 of 5
CRT/TVOUT
PLL PWR
PM
CLOCKs
MIS.
LVDS
DVO
71.RS690.M01
LAN
MINICARD
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_VIDEO/ CLOCK
Size A3
Document Number Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 12 of 46


GROUND
5 of 5
71.RS690.M01
RS690M-GP
U53E
POWER
U53D 4 of 5
RS690M-GP
71.RS690.M01
1D2V_LDO_S0
1D8V_S0
3D3V_S0
VDDA_1D2V
1D2V_S0
VDDPLL
VDDA12_PKG1
1D8VDD_S0
VDD_DVO
3D3VDDR_S0
SB
DY
MPZ2012S221AT-GP
MPZ2012S221AT-GP
0R0603-PAD
SC1U10V5ZY-1GP
SC1U10V2ZY
SC10U10V5ZY-1GP
SC4D7U10V5ZY-3GP
SC1U10V3KX-3GP
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
SC1U10V3KX-3GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_POWER
Size A3
Document Number
Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 13 of 46


LCD/INVERTER CONN
LED BD
Slide SWITCH
ODD CHANNEL
EVEN CHANNEL
BlueTooth ON/OFF
Wireless ON/OFF
Edge Trigger
2nd source: 62.40068.001
2nd source: 20.K0185.008
on Front Panel
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD CONN & LED
Orta
Friday, January 12, 2007
Sheet 14 of 46


SB
12 GMCH_RED
12 GMCH_GREEN
12 GMCH_BLUE
L1 FCB1608CF-GP
L2 FCB1608CF-GP
L3 FCB1608CF-GP
?
CRT_R
CRT_G
CRT_B
R14 150R2F-1-GP
R16 150R2F-1-GP
R20 150R2F-1-GP
C10 SC3P50V2CN-1-GP
C14 SC3P50V2CN-1-GP
C18 SC3P50V2CN-1-GP
C11 SC6D8P50V2DN-GP
C15 SC6D8P50V2DN-GP
C19 SC6D8P50V2DN-GP
DY
CRT1
VIDEO-15-75-GP
20.20715.015
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
5V_CRT_S0
C49 SC100P50V2JN-3GP
C7 SC18P50V2JN-1-GP
C39 SC100P50V2JN-3GP
C24 SCD01U16V2KX-3GP
31 CRT_DEC#
R24 470R2J-2-GP
C30 SC100P50V2JN-3GP
D10 BAV99-5-GP
3D3V_S0
5V_S0
C23 SCD1U16V2ZY-2GP
12 GMCH_HSYNC
12 GMCH_VSYNC
CRT_HSYNC1_R
CRT_VSYNC1_R
R11 0R2J-2-GP
R10 0R2J-2-GP
U3A TSAHCT125PW-GP
U3B TSAHCT125PW-GP
C9 SC18P50V2JN-1-GP
C8 SC18P50V2JN-1-GP
CH751H-40PT
D11
RN6 SRN2K2J-2-GP
SRN10KJ-6-GP
RN7
Q3 2N7002DW-1-GP
12 GMCH_DDCDATA
12 GMCH_DDCCLK
DAT_DDC1_5
CLK_DDC1_5
C457 SC33P50V2JN-3GP
C483 SC33P50V2JN-3GP
C469 SC33P50V2JN-3GP
L13 TVOUT IND-1D2UH-5-GP
L16 TVOUT IND-1D2UH-5-GP
L15 TVOUT IND-1D2UH-5-GP
12 TV_DACB
12 TV_DACC
12 TV_DACA
R323 150R2F-1-GP TVOUT
R336 150R2F-1-GP TVOUT
R326 150R2F-1-GP TVOUT
C455 SC150P50V2JN-3GP
C481 SC150P50V2JN-3GP
C468 SC150P50V2JN-3GP
C462 TVOUT SC270P50V2JN-2GP
C501 TVOUT SC270P50V2JN-2GP
C479 TVOUT SC270P50V2JN-2GP
LUMA_1
CRMA_1
COMP_1
TVOUT1
LUMA
CRMA
COMP
NC#2
GND
NC#5
MINDIN7-19-GP-U2
22.10021.H61
D23 BAV99-5-GP D27
D25 BAV99-5-GP
D4 BAV99-5-GP D7
D9 BAV99-5-GP
CRT_R
CRT_G
CRT_B
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT/TV Connector
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 15 of 46

Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

SB600 asserts PLTRST# to reset
devices on the platform.

PCIRST

Change 0921

SB

DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 PCI/CPU/LPC/RTC (1 of 5)

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 16 of 46

71.SB600.00U

62.70001.011

2nd source: 20.D0198.103

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP

U57B 2 of 4

SATA_TXP0 SATA_TXN0 SATA_RXN0 SATA_RXP0

SATA_TXP0_SB SATA_TXN0_SB SATA_RXN0_SB SATA_RXP0_SB

SATA_TX0+ SATA_TX0- SATA_RX0- SATA_RX0+ SATA_TX1+ SATA_TX1- SATA_RX1- SATA_RX1+ SATA_TX2+ SATA_TX2- SATA_RX2- SATA_RX2+ SATA_TX3+ SATA_TX3- SATA_RX3- SATA_RX3+ SATA_CAL SATA_X1 SATA_X2 SATA_ACT#/GPIO67

SERIAL ATA

SATA

SATA_X1 SATA_X2 R381 1MR2J-L2-GP XTAL-25MHZ-67GP C582 SC12P50V2JN-3GP C576 SC10P50V2JN-4GP

According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.

R397 1KR2F-3-GP R191 10KR2J-3-GP 3D3V_S0

PLLVDD_ATA XTLVDD_ATA AVDD_SATA

PLLVDD_SATA XTLVDD_SATA AVDD_SATA AVSS_SATA

IDE_IORDY IDE_IRQ IDE_A0 IDE_A1 IDE_A2 IDE_DACK# IDE_DRQ IDE_IOR# IDE_IOW# IDE_CS1# IDE_CS3#

IDE_PDIORDY INT_IRQ14 IDE_PDA0 IDE_PDA1 IDE_PDA2 IDE_PDDACK# IDE_PDDREQ IDE_PDIOR# IDE_PDIOW# IDE_PDCS1# IDE_PDCS3#

IDE_D0/GPIO15 IDE_D1/GPIO16 IDE_D2/GPIO17 IDE_D3/GPIO18 IDE_D4/GPIO19 IDE_D5/GPIO20 IDE_D6/GPIO21 IDE_D7/GPIO22 IDE_D8/GPIO23 IDE_D9/GPIO24 IDE_D10/GPIO25 IDE_D11/GPIO26 IDE_D12/GPIO27 IDE_D13/GPIO28 IDE_D14/GPIO29 IDE_D15/GPIO30

IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15

ATA 66/100

SPI_DI/GPIO12 SPI_DO/GPIO11 SPI_CLK/GPIO47 SPI_HOLD#/GPIO31 SPI_CS#/GPIO32 LAN_RST#/GPIO13 ROM_RST#/GPIO14

TP54 TP45 TP50 TP101 TP46 TP41 TP47 TPAD30

SPI ROM

FANOUT0/GPIO3 FANOUT1/GPIO48 FANOUT2/GPIO49 FANIN0/GPIO50 FANIN1/GPIO51 FANIN2/GPIO52 TEMP_COMM TEMPIN0/GPIO61 TEMPIN1/GPIO62 TEMPIN2/GPIO63 TEMPIN3/TALERT#/GPIO64 VIN0/GPIO53 VIN1/GPIO54 VIN2/GPIO55 VIN3/GPIO56 VIN4/GPIO57 VIN5/GPIO58 VIN6/GPIO59 VIN7/GPIO60

ALERT# 6,35 PSW_CLR# UMA_DIS CLK_ID FP_ID FP_ID 32 FP_DETECT# 32

HW MONITOR

AVDD AVSS

SERIAL ATA POWER

SB600-GP

SB

3D3V_S0 R149 10KR2J-3-GP R519 10KR2J-3-GP

FP_DETECT# PSW_CLR#

G41 GAP-OPEN

0 => DIS
1 => UMA

R214 10KR2J-3-GP R197 RTL R198 DY

UMA_DIS CLK_ID FP_ID

R217 DY R206 ICS R207 DY

AVDD_HWM R432 0R3-0-U-GP C613 SCD1U16V2ZY-2GP C614 SC2D2U6D3V3KX-GP DY

71.SB600.00U

SB XTLVDD_ATA R187 0R0603-PAD EC117 C318 SC2D2U6D3V3KX-GP

SB PLLVDD_ATA R193 0R0603-PAD EC118 C320 SC2D2U6D3V3KX-GP

SB AVDD_SATA R177 0R0603-PAD EC114 C311 C307 EC63 EC65 EC62 EC60 EC64

SATA

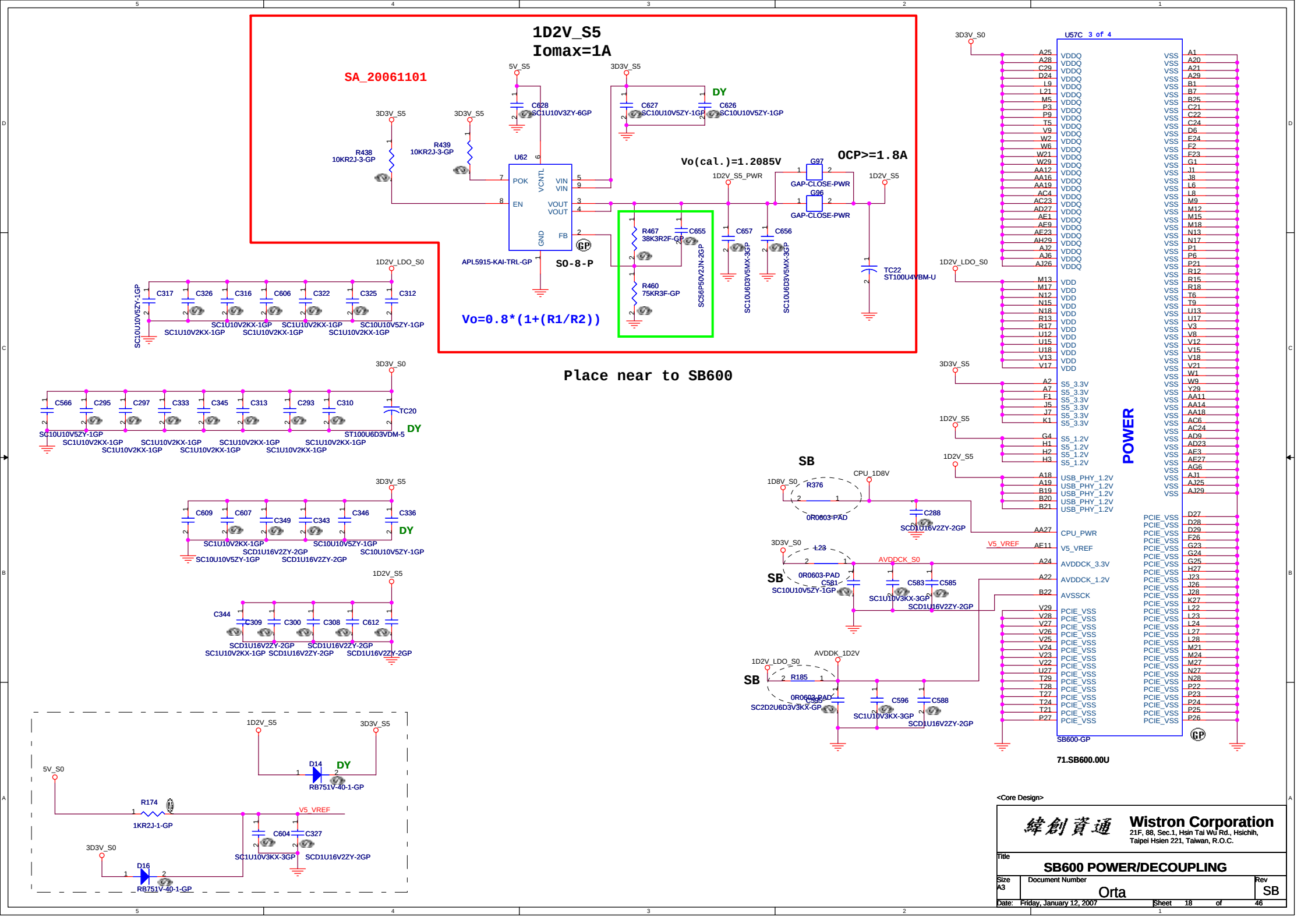
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)

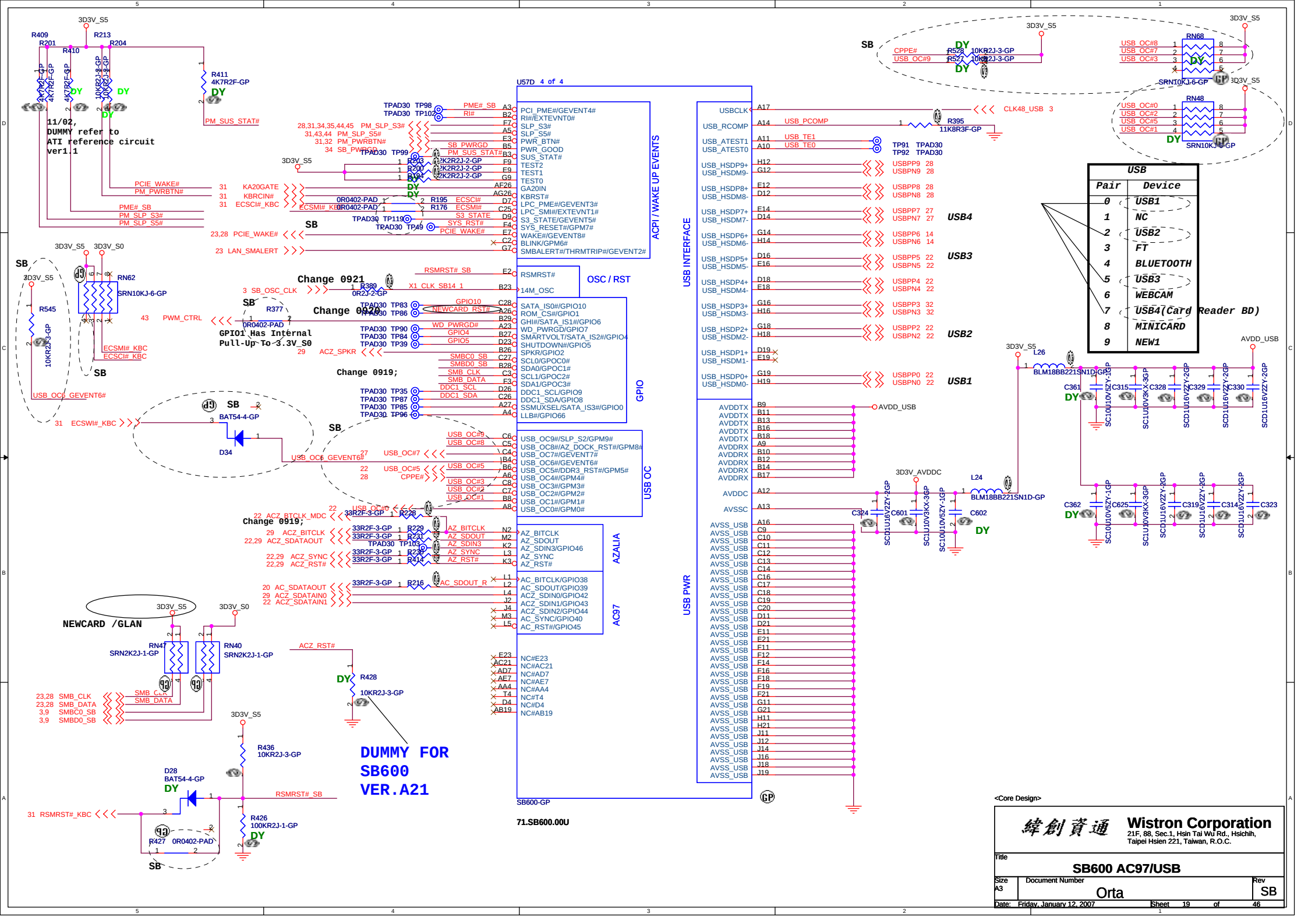
Size: A3 | Document Number: Orta | Rev: SB

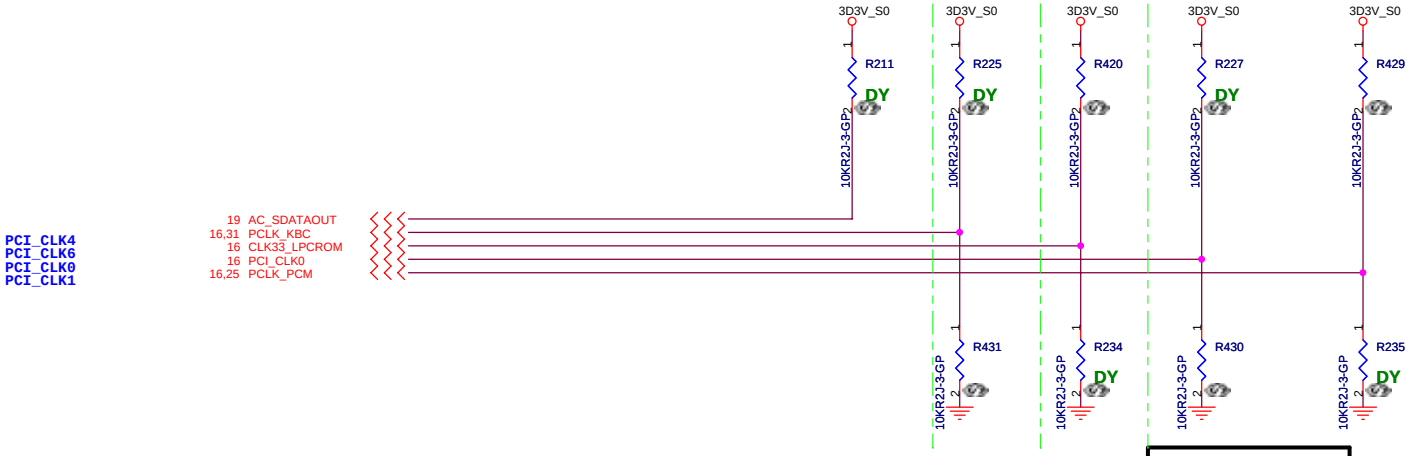
Date: Friday, January 12, 2007 | Sheet 17 of 46



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB600 POWER/DECOUPLING	
Size A3	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 18 of 46	

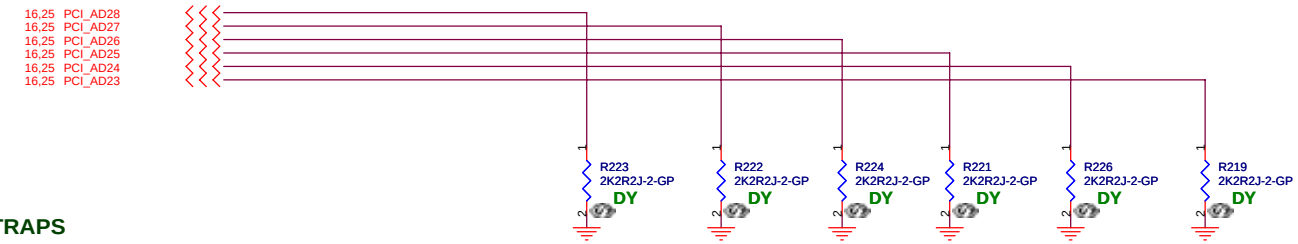

11/02,
DUMMY refer to
ATI reference circuit
ver1.1
Change 0921
Change 0920
Change 0919;
Change 0919;
GPIO1 Has Internal
Pull-Up To 3.3V_S0
NEWCARD /GLAN
DUMMY FOR
SB600
VER.A21
U57D 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
SB600-GP
71.SB600.00U
USB
Pair Device
0 USB1
1 NC
2 USB2
3 FT
4 BLUETOOTH
5 USB3
6 WEBCAM
7 USB4(Card Reader BD)
8 MINICARD
9 NEW1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 AC97/USB
Size A3
Document Number Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 19 of 46



REQUIRED SYSTEM STRAPS

				SB600	
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

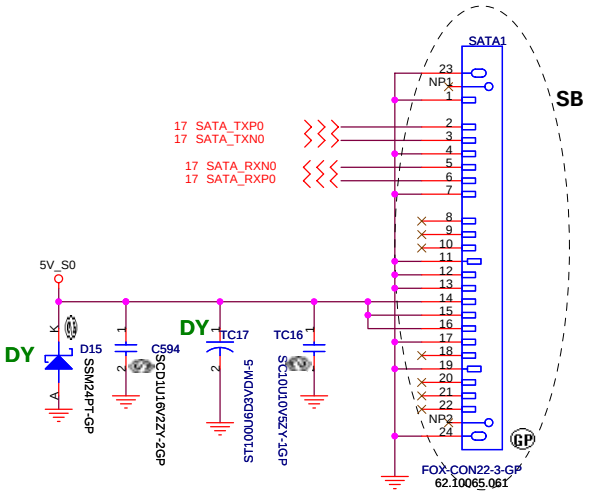
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

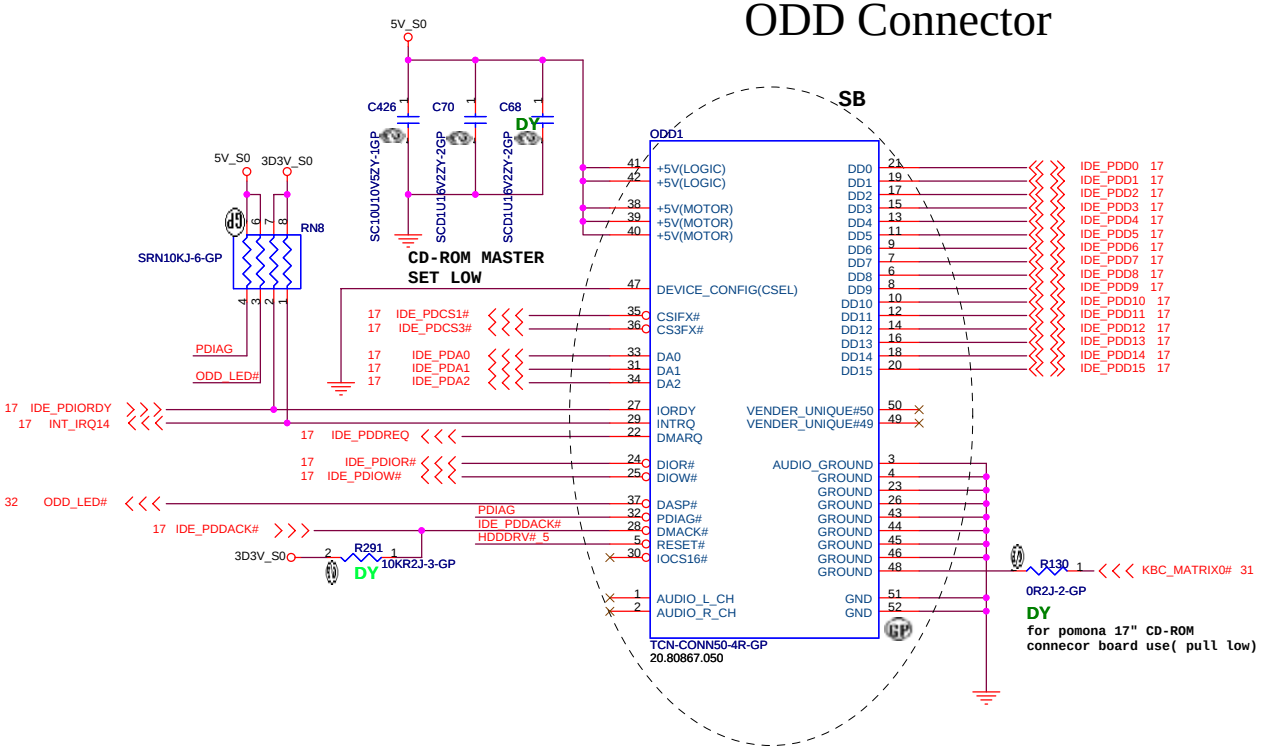
Size: A3 | Document Number: Orta | Rev: SB

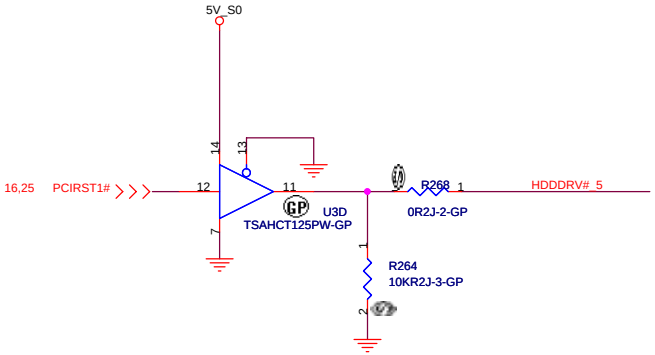
Date: Friday, January 12, 2007 | Sheet 20 of 46

SATA HD Connector



ODD Connector

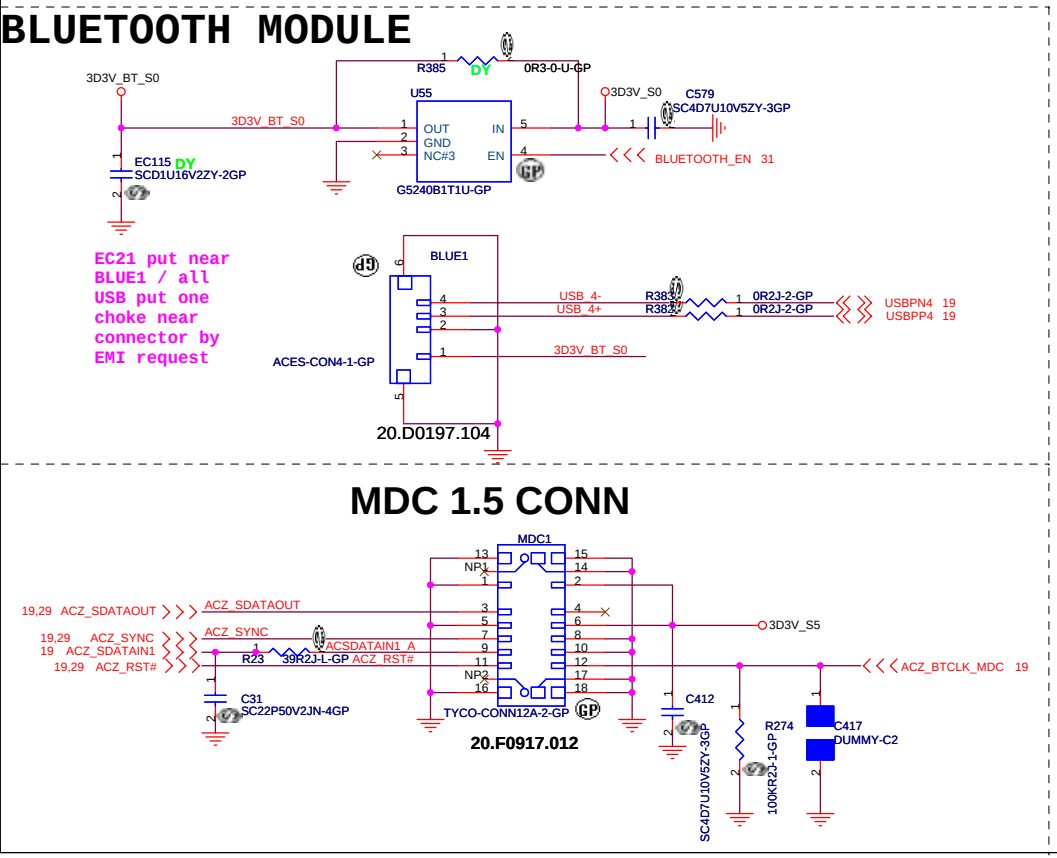


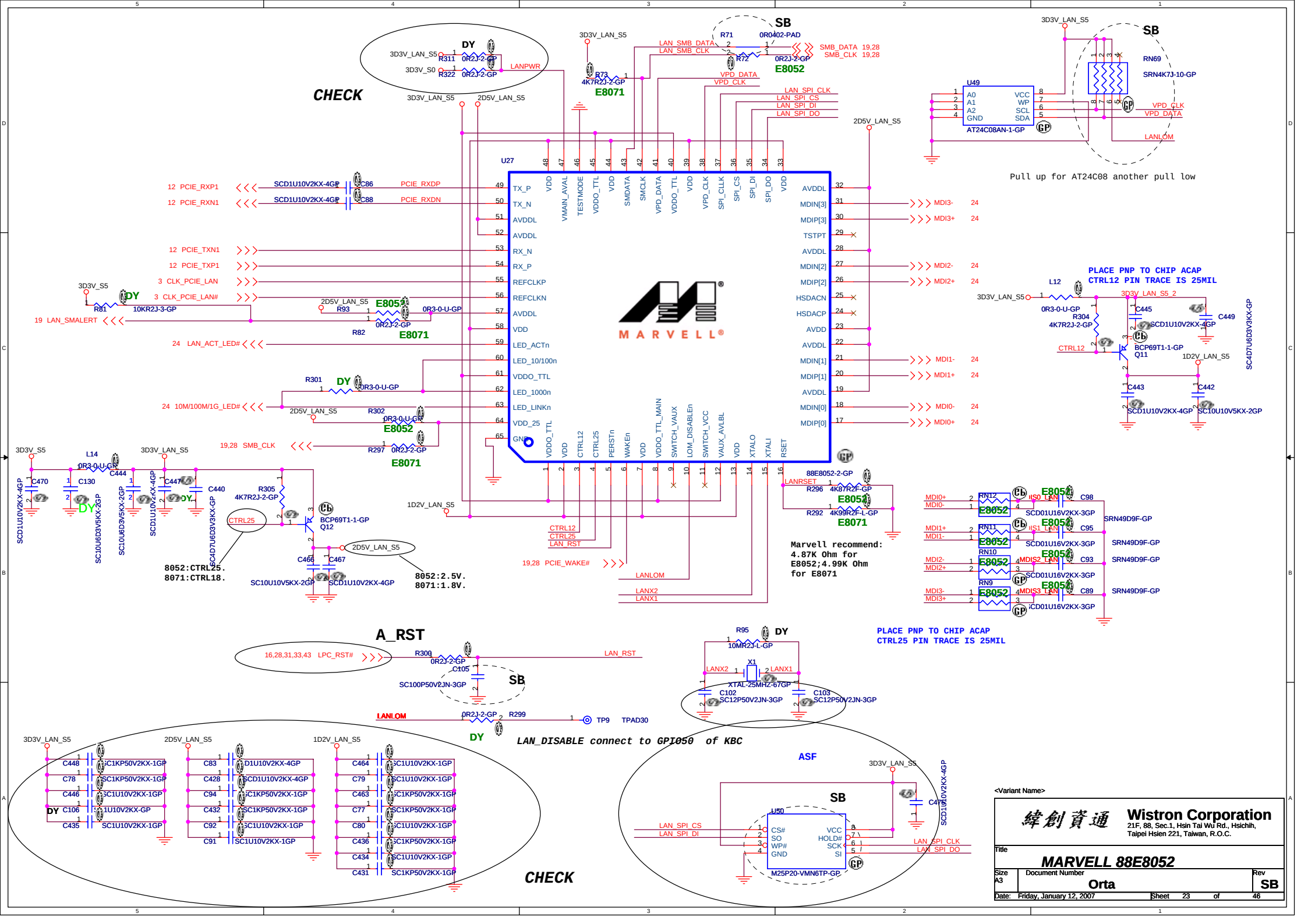


bom1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD and CDROM		
Size	Document Number	Rev
	Orta	SB
Date: Friday, January 12, 2007	Sheet 21 of 46	


BLUETOOTH MODULE
3D3V_BT_S0
R385
DY
0R3-0-U-GP
U55
OUT
GND
NC#3
IN
EN
G5240B1T1U-GP
3D3V_S0
C579
SC4D7U10V5ZY-3GP
BLUETOOTH_EN 31
EC115 DY
SCD1U16V2ZY-2GP
EC21 put near BLUE1 / all USB put one choke near connector by EMI request
BLUE1
ACES-CON4-1-GP
USB_4-
USB_4+
R383
R382
0R2J-2-GP
USBPN4 19
USBPP4 19
20.D0197.104
MDC 1.5 CONN
MDC1
TYCO-CONN12A-2-GP
20.F0917.012
19,29 ACZ_SDATAOUT
ACZ_SDATAOUT
19,29 ACZ_SYNC
19 ACZ_SDATAIN1
19,29 ACZ_RST#
ACZ_SYNC
ACSDATAIN1_A
R23
39R2J-L-GP
ACZ_RST#
C31
SC22P50V2JN-4GP
3D3V_S5
ACZ_BTCLK_MDC 19
C412
SC4D7U10V5ZY-3GP
R274
100KR2J-1-GP
C417
DUMMY-C2
5V_S5
U65
GND
IN
EN1/EN1#
EN2/EN2#
GND
OC1#
OUT1
OUT2
OC2#
5V_USB1_S5
5V_USB2_S5
USB_OC#0 19
USB_OC#5 19
SB
27,31 USB_PWR_EN#
C649
SCD1U16V2ZY-2GP
G546B2RD1UF-GP
74.00546.A73
EC125
DY
SCD1U16V2ZY-2GP
EC124
DY
SCD1U16V2ZY-2GP
100 mil
TC23
SE100U10VM-4-GP
79.10111.40L
EC127 DY
SCD1U16V2ZY-2GP
EC129 DY
SC1000P50V3JN-GP
TC13
SE150U10VM-2GP
79.15711.30L
EC126 DY
SCD1U16V2ZY-2GP
EC128 DY
SC1000P50V3JN-GP
EC51 DY
SCD1U16V2ZY-2GP
EC44 DY
SCD1U16V2ZY-2GP
USB1
SRN0J-6-GP
RN31
USBPN0 19
USBPP0 19
USB_0-
USB_0+
TR1
DY
T-63UH-GP
68.03216.20B
SKT-USB-97-UGP
22.10218.H01
2nd source: 22.10218.P01
USB2
SRN0J-6-GP
RN32
USBPN2 19
USBPP2 19
USB_1-
USB_1+
TR2
DY
T-63UH-GP
68.03216.20B
SKT-USB-97-UGP
2nd source: 22.10218.P01
22.10218.H01
USB3
RN60
SRN0J-6-GP
USBPN5 19
USBPP5 19
USB_2-
USB_2+
TR3
DY
T-63UH-GP
68.03216.20B
SKT-USB-168-GP
2nd source: 22.10218.P01
bom1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB / MDC / BLUETOOTH
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 22 of 46



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

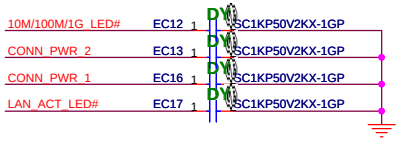
<Variant Name>

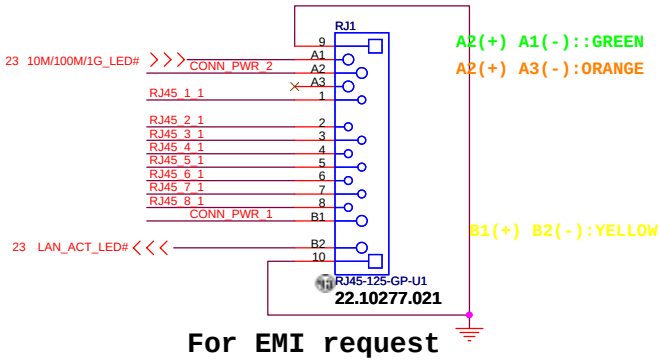
Title: MARVELL 88E8052

Size	Document Number	Rev
A3	Orta	SB

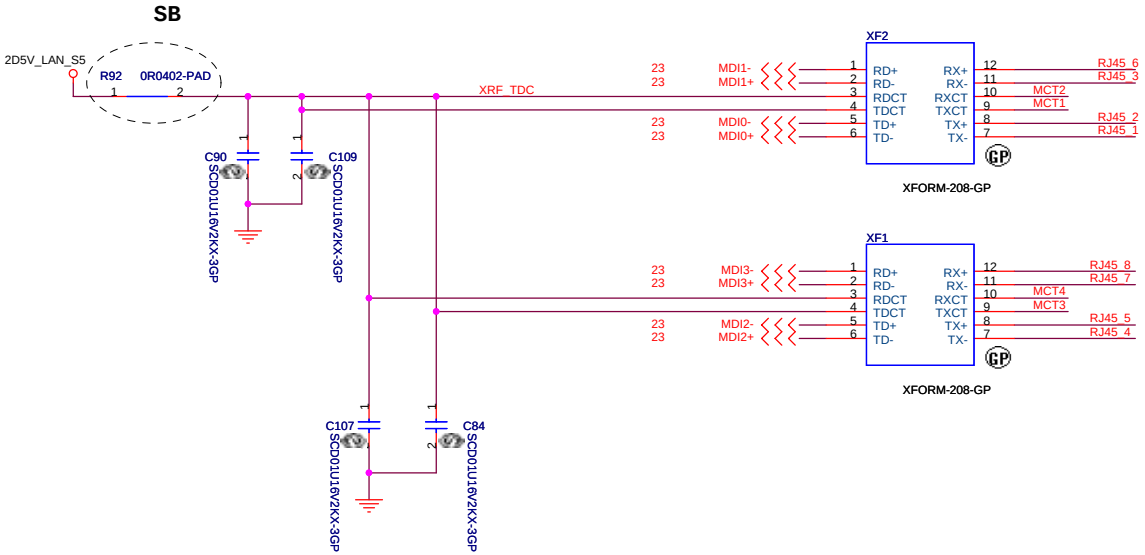
Date: Friday, January 12, 2007 Sheet 23 of 46

LAN Connector

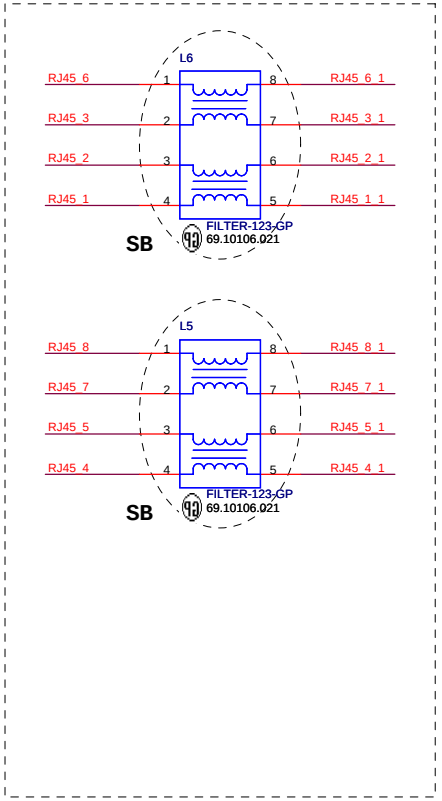




GIGA Lan Transformer



For EMI request

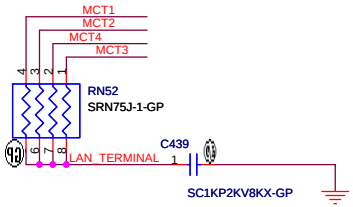


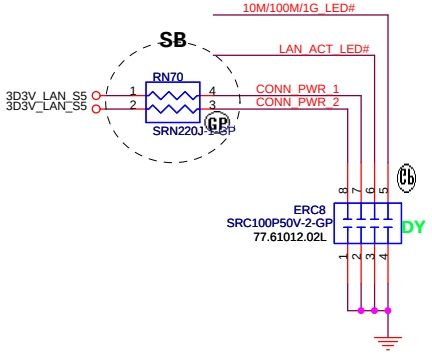
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

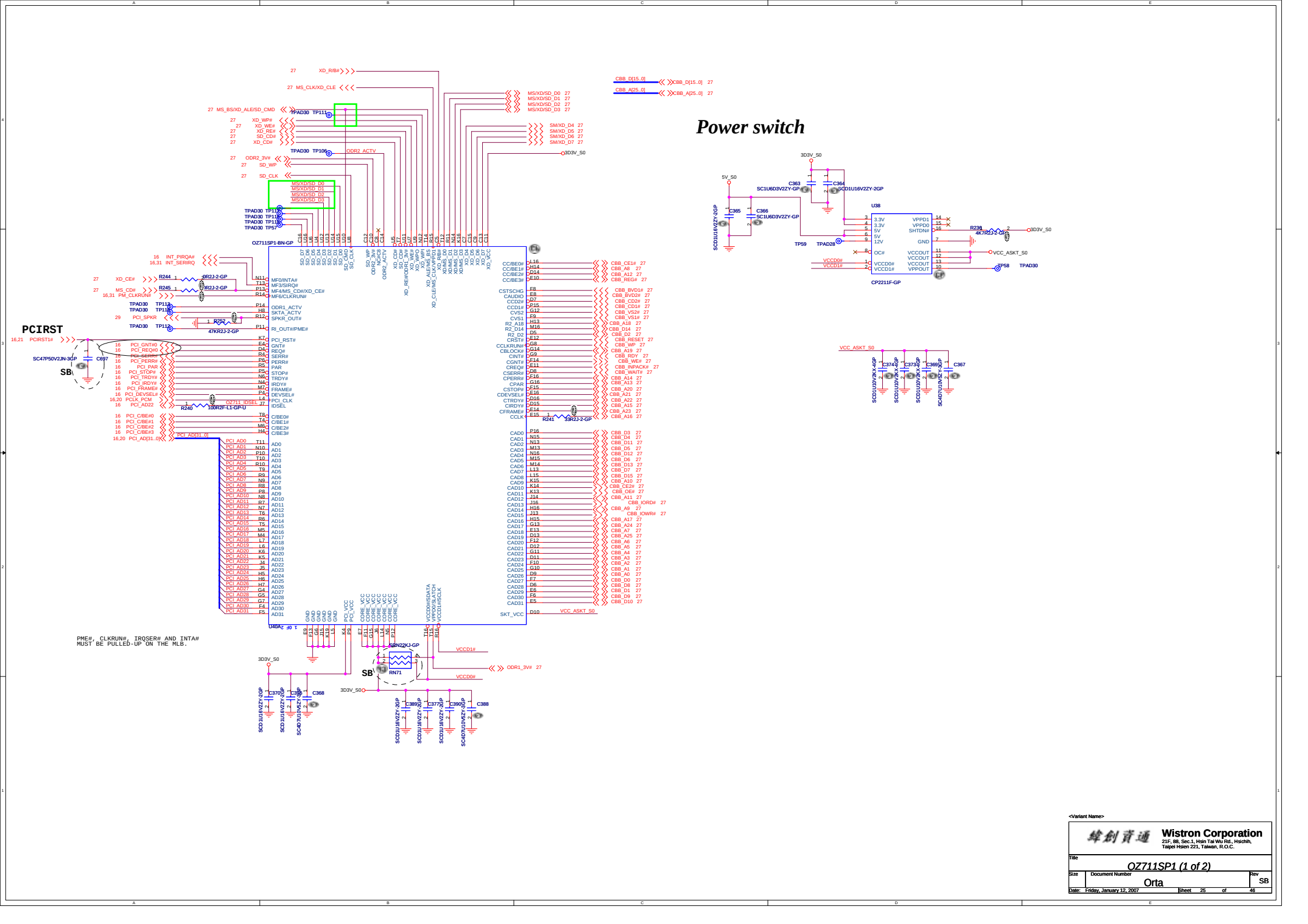


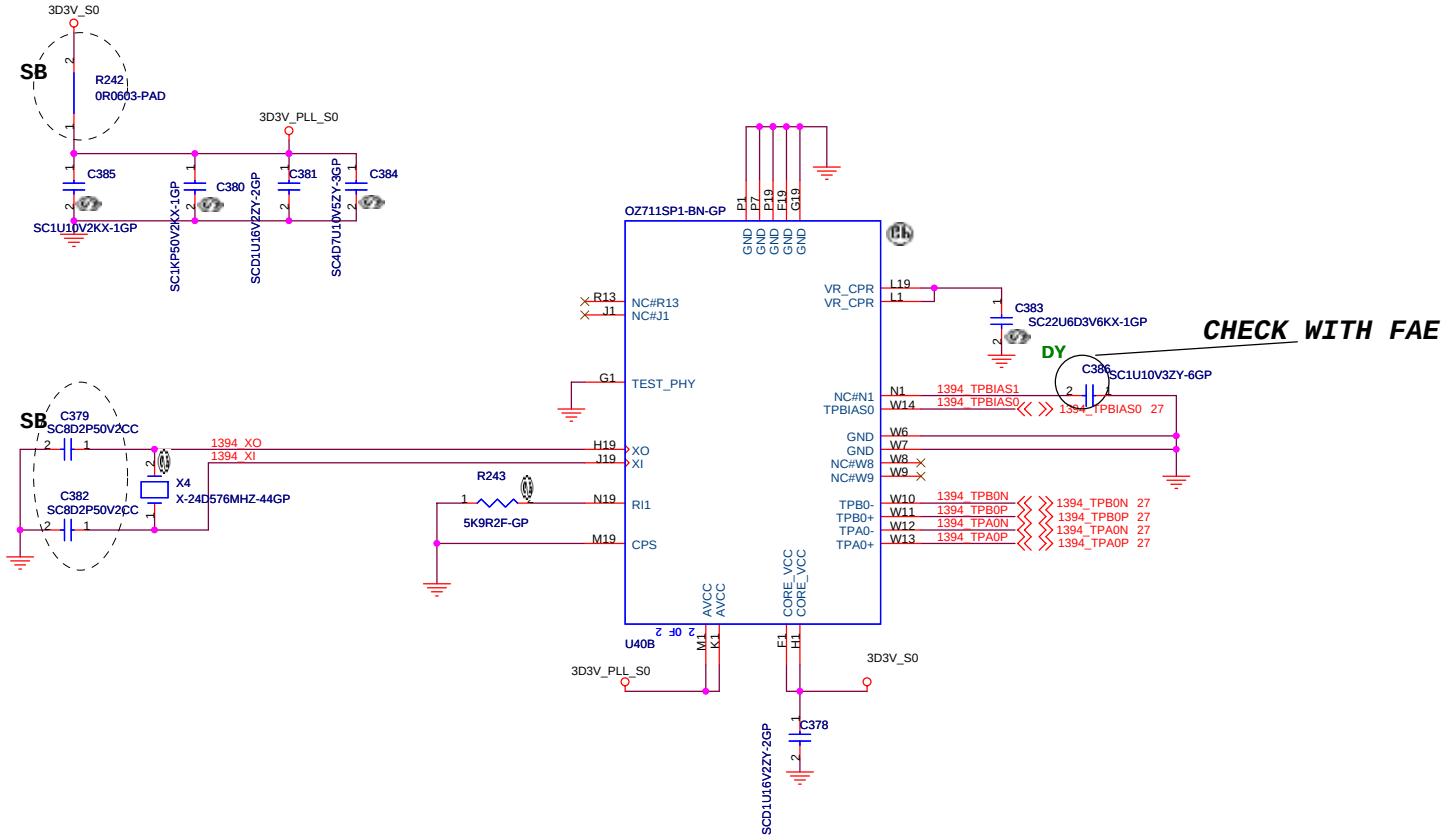


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector		
Size: A3	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 24 of 46	


Power switch
PCIRST
PME#, CLKRUN#, IRQSER# AND INTA#
MUST BE PULLED-UP ON THE MLB.
OZ711SP1-BN-GP
U40A
SB
3D3V_S0
5V_S0
VCC_ASKT_S0
CP2211F-GP
U38
Variant Name
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
OZ711SP1 (1 of 2)
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 25 of 46



<Variant Name>

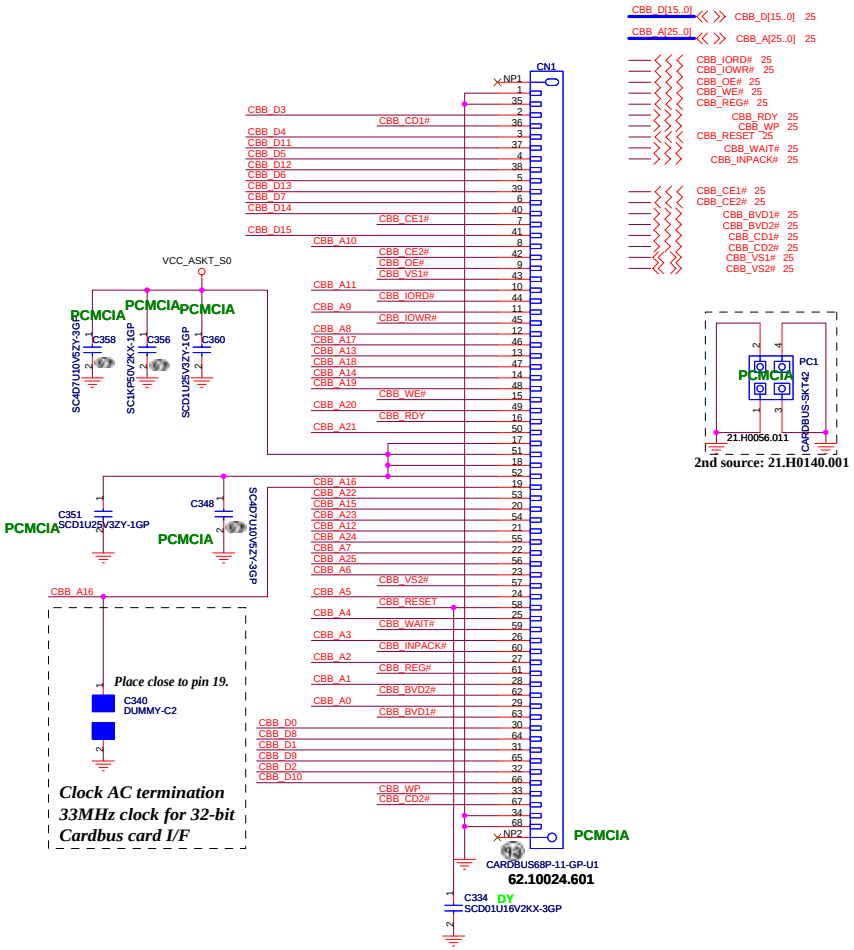
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *OZ711SP1 (2 of 2)*

Size	Document Number	Rev
	Orta	SB

Date: Friday, January 12, 2007 Sheet 26 of 46

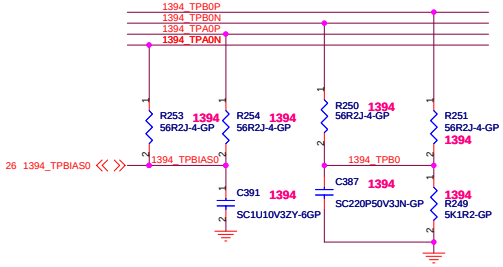
PCMCIA Socket

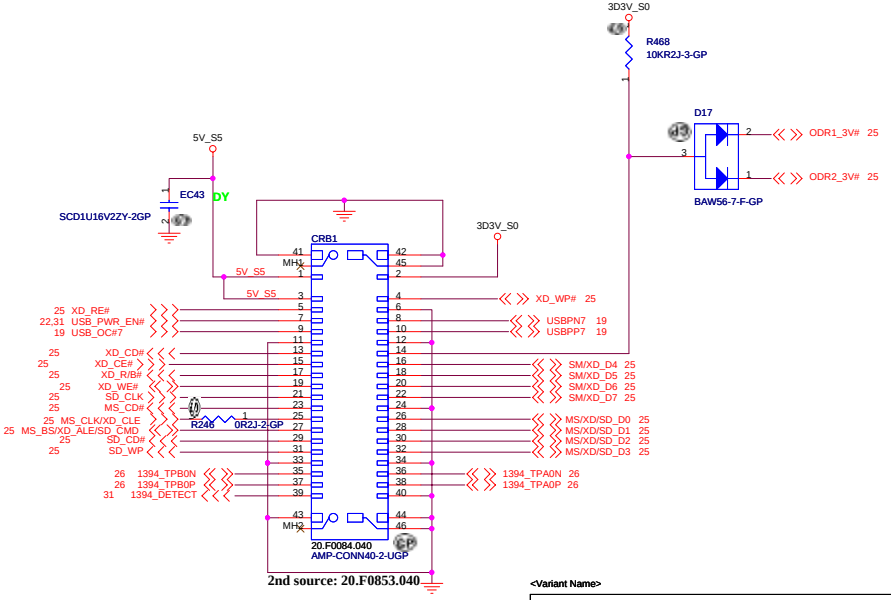


Cardbus I/F

2nd source: 21.H0140.001

CLOSE TO CHIP





2nd source: 20.F0853.040

XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

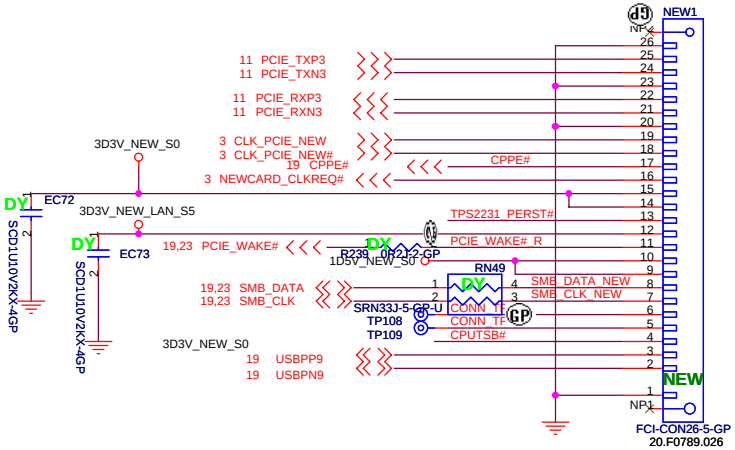
Size	Document Number	Rev
	Orta	SB

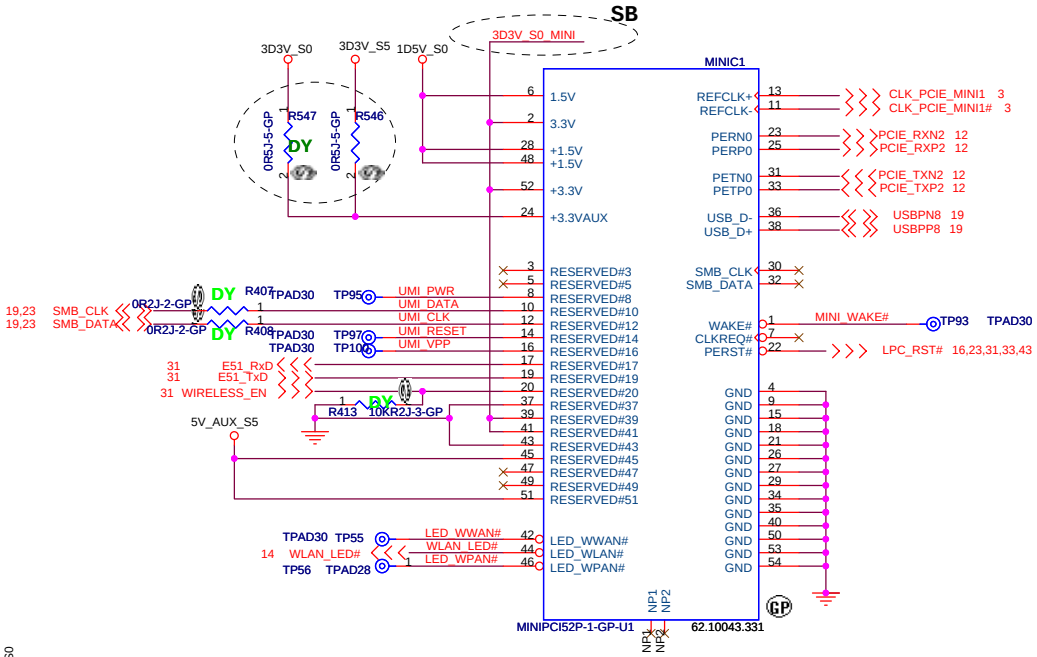
Date: Friday, January 12, 2007 Sheet 27 of 46

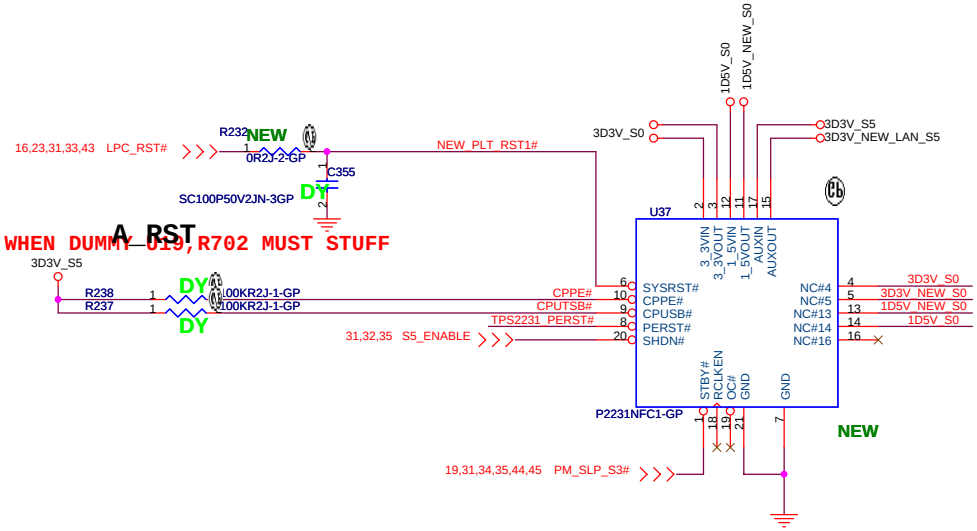
Mini Card Connector

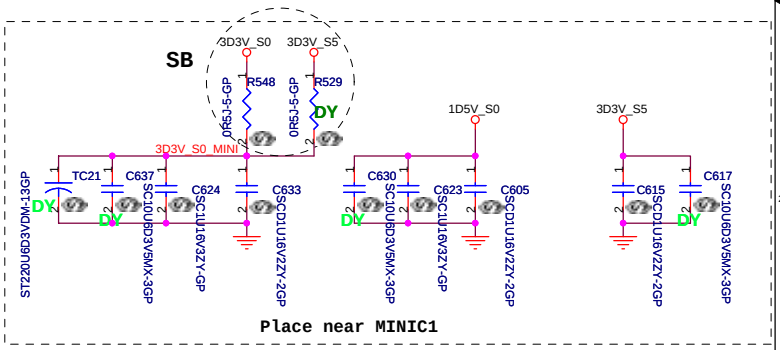
NEWCARD Connector

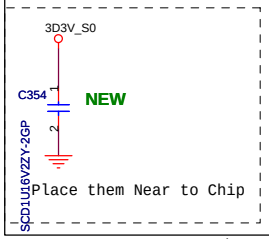
Reserve the symbol for bottom side connector

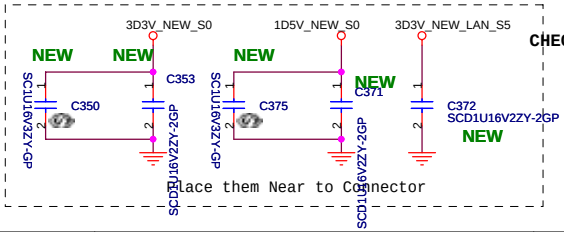










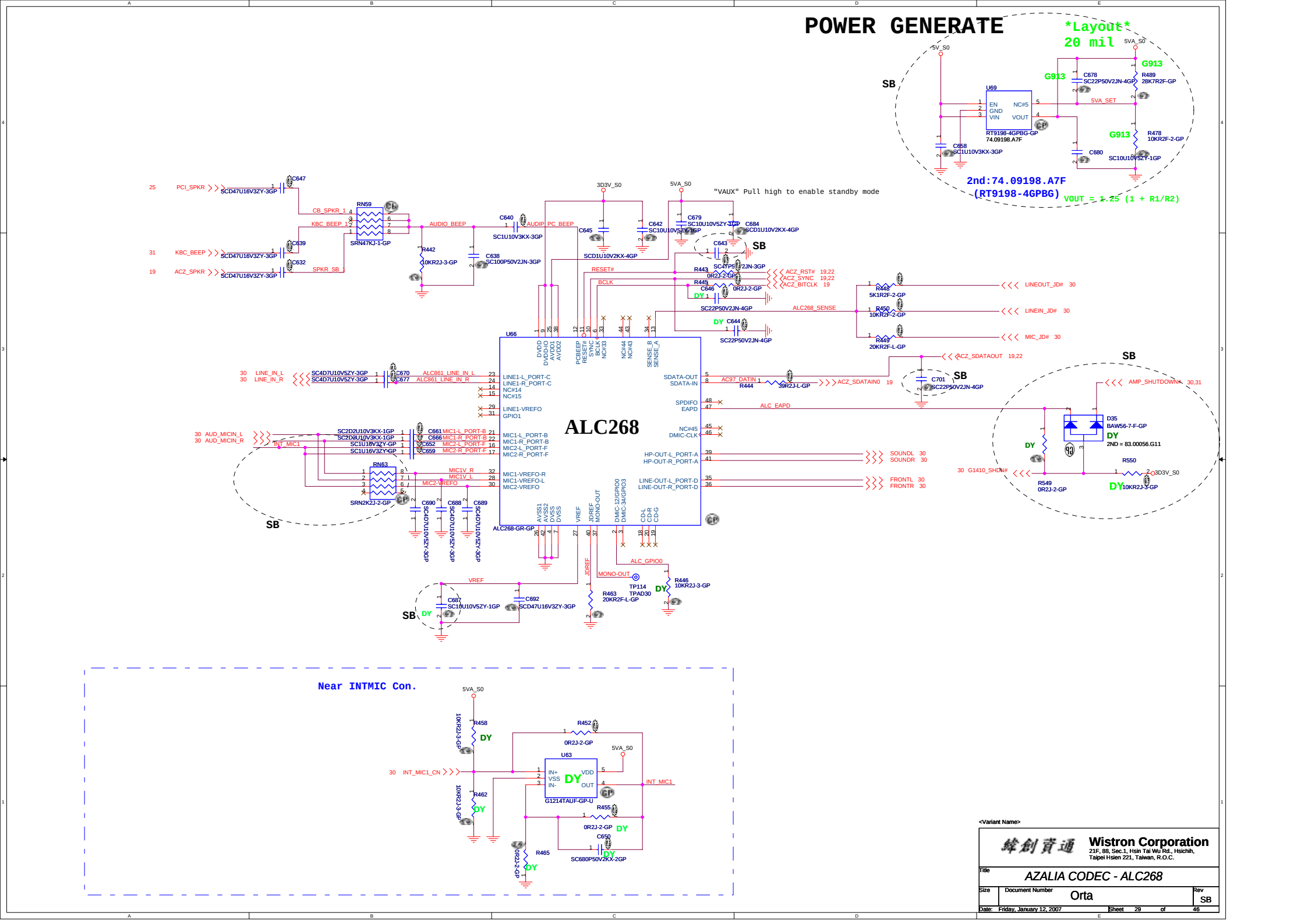


CHECK WITH COLUMBIA

bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / NEW CARD***	
Size	Document Number **Orta**	Rev SB
Date: Friday, January 12, 2007	Sheet 28 of 46	

POWER GENERATE

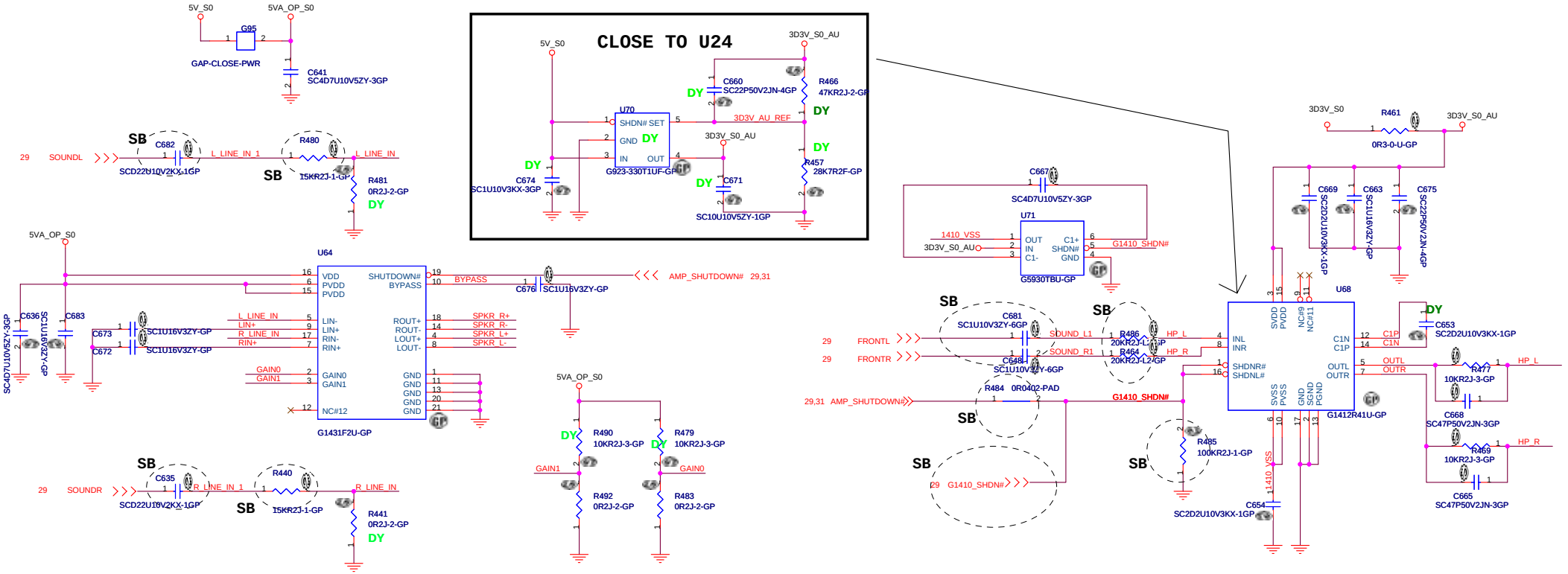


<Variant Name>

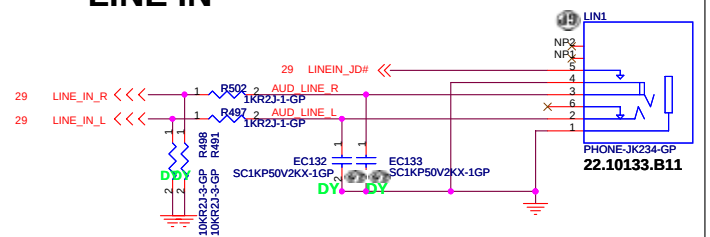
鋒創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AZALIA CODEC - ALC268	
Size	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 29 of 46	

AUDIO OP AMPLIFIER

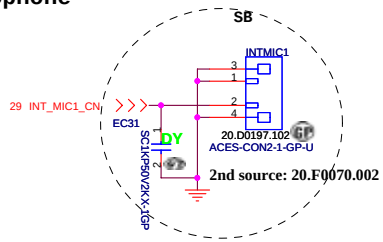
KBC_MUTE_GPIO8



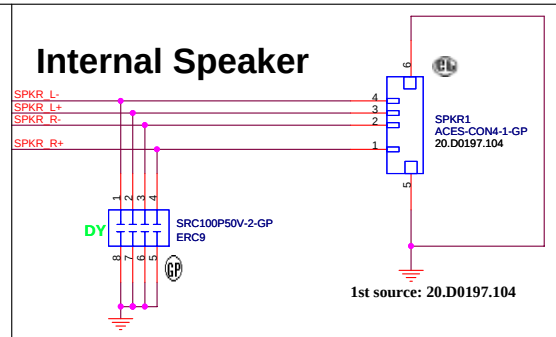
LINE IN



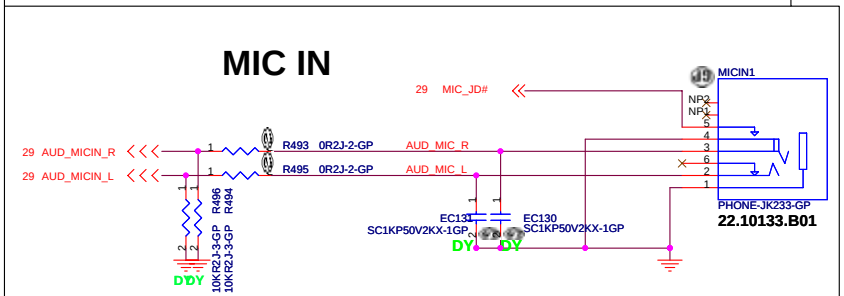
Internal Microphone



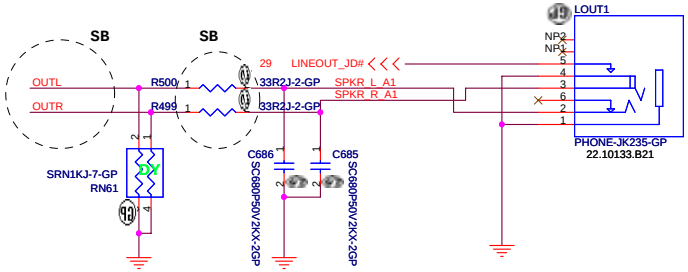
Internal Speaker



MIC IN



LINE OUT



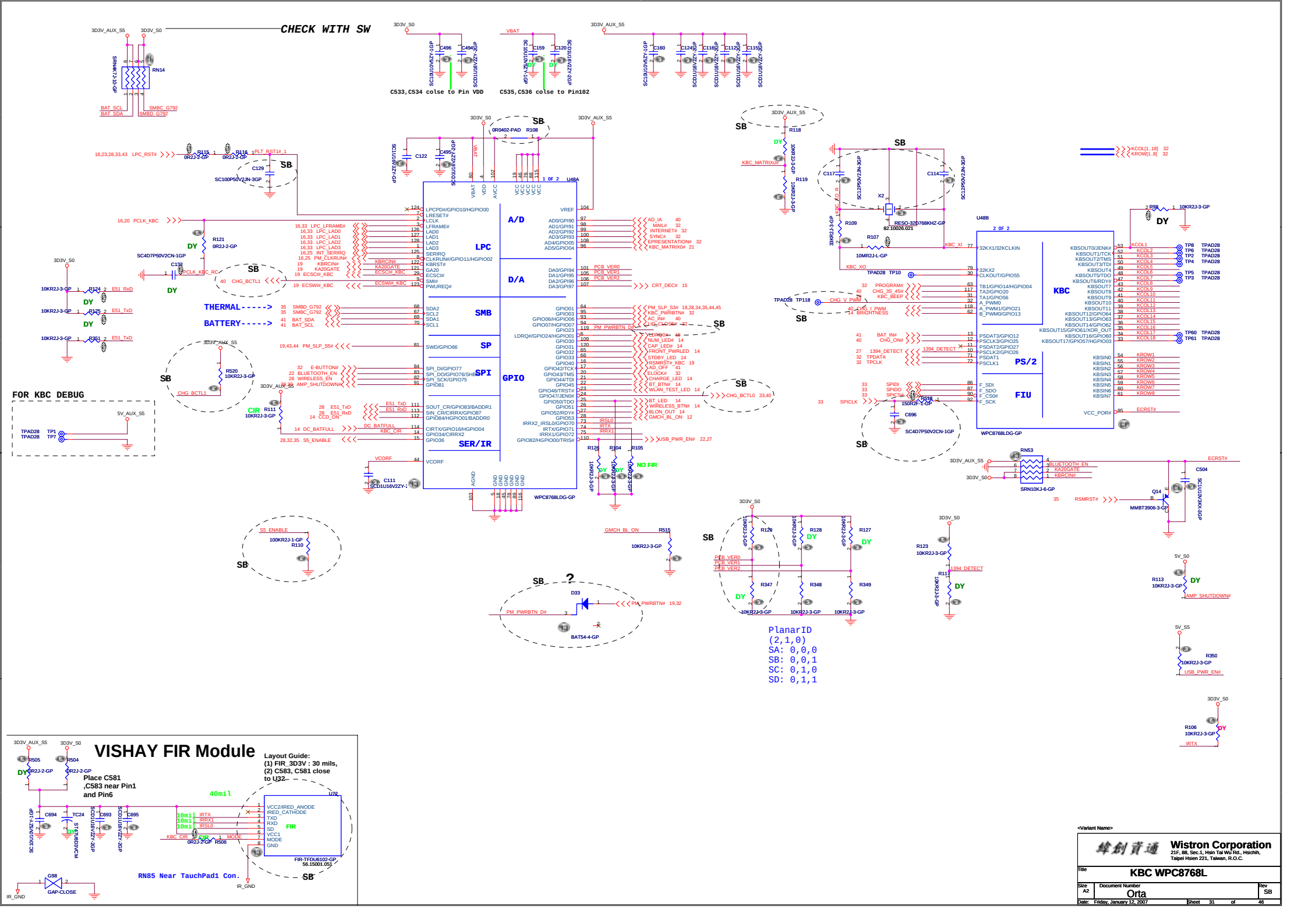
<Variant Name>

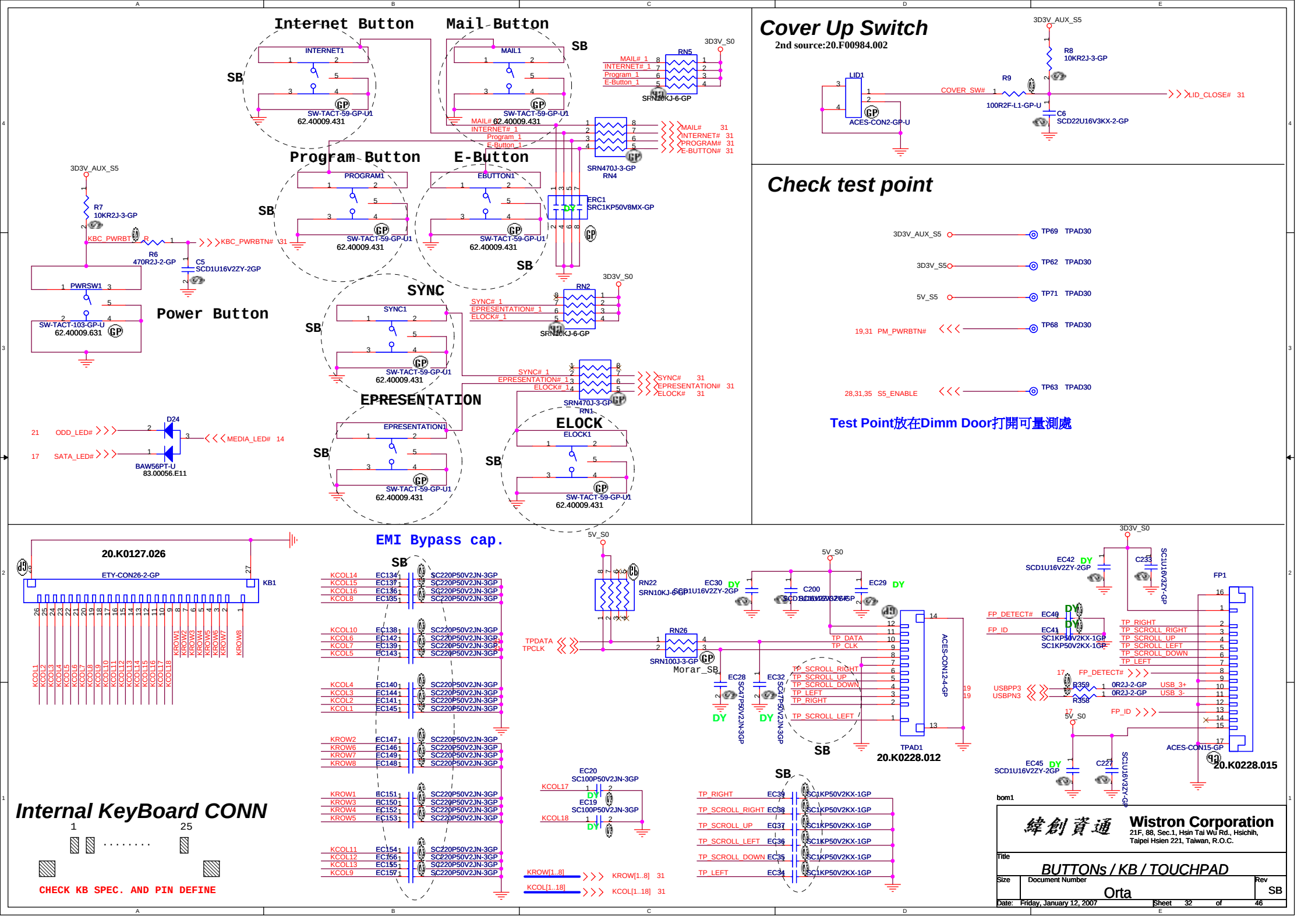
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

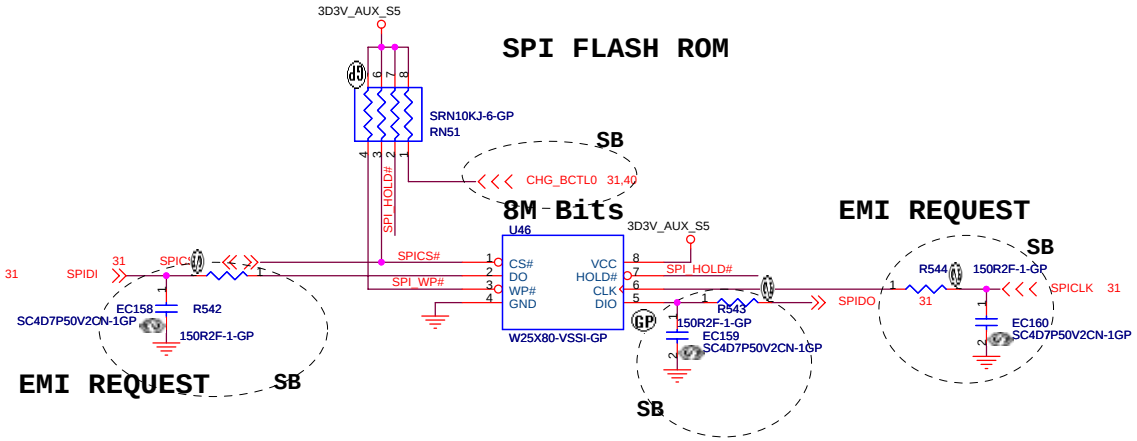
Title: AUDIO AMP AND JACK

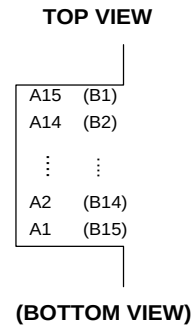
Size	Document Number	Rev
	Orta	SB

Date: Friday, January 12, 2007 Sheet 30 of 46

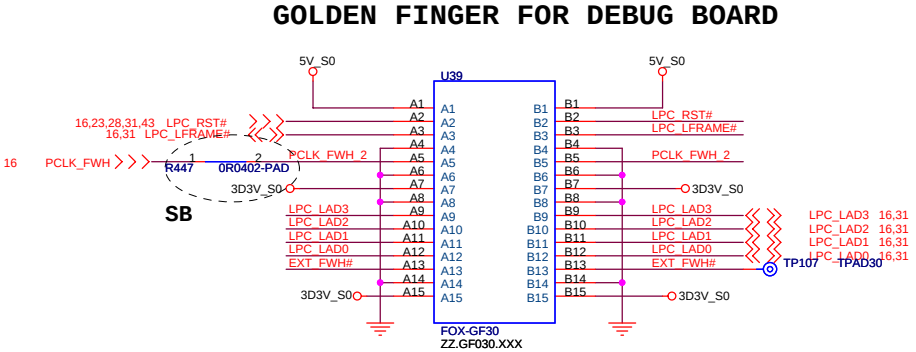

CHECK WITH SW
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
FOR KBC DEBUG
THERMAL----->
BATTERY----->
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
VISHAY FIR Module
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
Place C581 ,C583 near Pin1 and Pin6
40mil
RN85 Near TauchPad1 Con.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Orta
Friday, January 12, 2007


Internet Button
Mail Button
Program Button
E-Button
SYNC
EPRESENTATION
ELOCK
Power Button
SB
INTERNET1
MAIL1
PROGRAM1
EBUTTON1
SYNC1
EPRESENTATION1
ELOCK1
PWRSW1
SW-TACT-59-GP-U1
62.40009.431
SW-TACT-103-GP-U
62.40009.631
RN5
SRN10KJ-6-GP
RN4
SRN470J-3-GP
RN2
RN1
ERC1
SRC1KP50V8MX-GP
R7
10KR2J-3-GP
R6
470R2J-2-GP
C5
SCD1U16V2ZY-2GP
D24
BAW56PT-U
83.00056.E11
3D3V_AUX_S5
3D3V_S0
KBC_PWRBTN#
KBC_PWRBTN# 31
ODD_LED#
SATA_LED#
MEDIA_LED# 14
MAIL# 31
INTERNET# 31
PROGRAM# 31
E-BUTTON# 31
SYNC# 31
EPRESENTATION# 31
ELOCK# 31
Cover Up Switch
2nd source:20.F00984.002
LID1
ACES-CON2-GP-U
COVER_SW#
R8
10KR2J-3-GP
R9
100R2F-L1-GP-U
C6
SCD22U16V3KX-2-GP
LID_CLOSE# 31
Check test point
TP69 TPAD30
TP62 TPAD30
TP71 TPAD30
TP68 TPAD30
TP63 TPAD30
19,31 PM_PWRBTN#
28,31,35 S5_ENABLE
Test Point放在Dimm Door打開可量測處
20.K0127.026
ETY-CON26-2-GP
KB1
KCOL1
KCOL2
KCOL3
KCOL4
KCOL5
KCOL6
KCOL7
KCOL8
KCOL9
KCOL10
KCOL11
KCOL12
KCOL13
KCOL14
KCOL15
KCOL16
KCOL17
KCOL18
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
EMI Bypass cap.
SC220P50V2JN-3GP
SC100P50V2JN-3GP
SC47P50V2JN-3GP
SC1KP50V2KX-1GP
RN22
SRN10KJ-6-GP
RN26
SRN100J-3-GP
Morar_SB
TPDATA
TPCLK
TP_DATA
TP_CLK
TP_SCROLL_RIGHT
TP_SCROLL_UP
TP_SCROLL_DOWN
TP_LEFT
TP_SCROLL_LEFT
TP_RIGHT
TPAD1
20.K0228.012
ACES-CON24-GP
FP1
20.K0228.015
ACES-CON15-GP
FP_DETECT#
FP_ID
USBPP3
USBPN3
USB 3+
USB 3-
R359
R358
0R2J-2-GP
KROW[1..8] 31
KCOL[1..18] 31
Internal KeyBoard CONN
1
25
CHECK KB SPEC. AND PIN DEFINE
bom1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 32 of 46

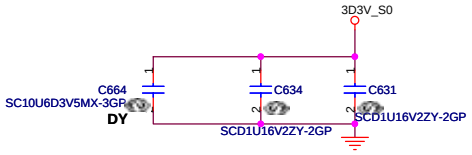




EMI REQUEST



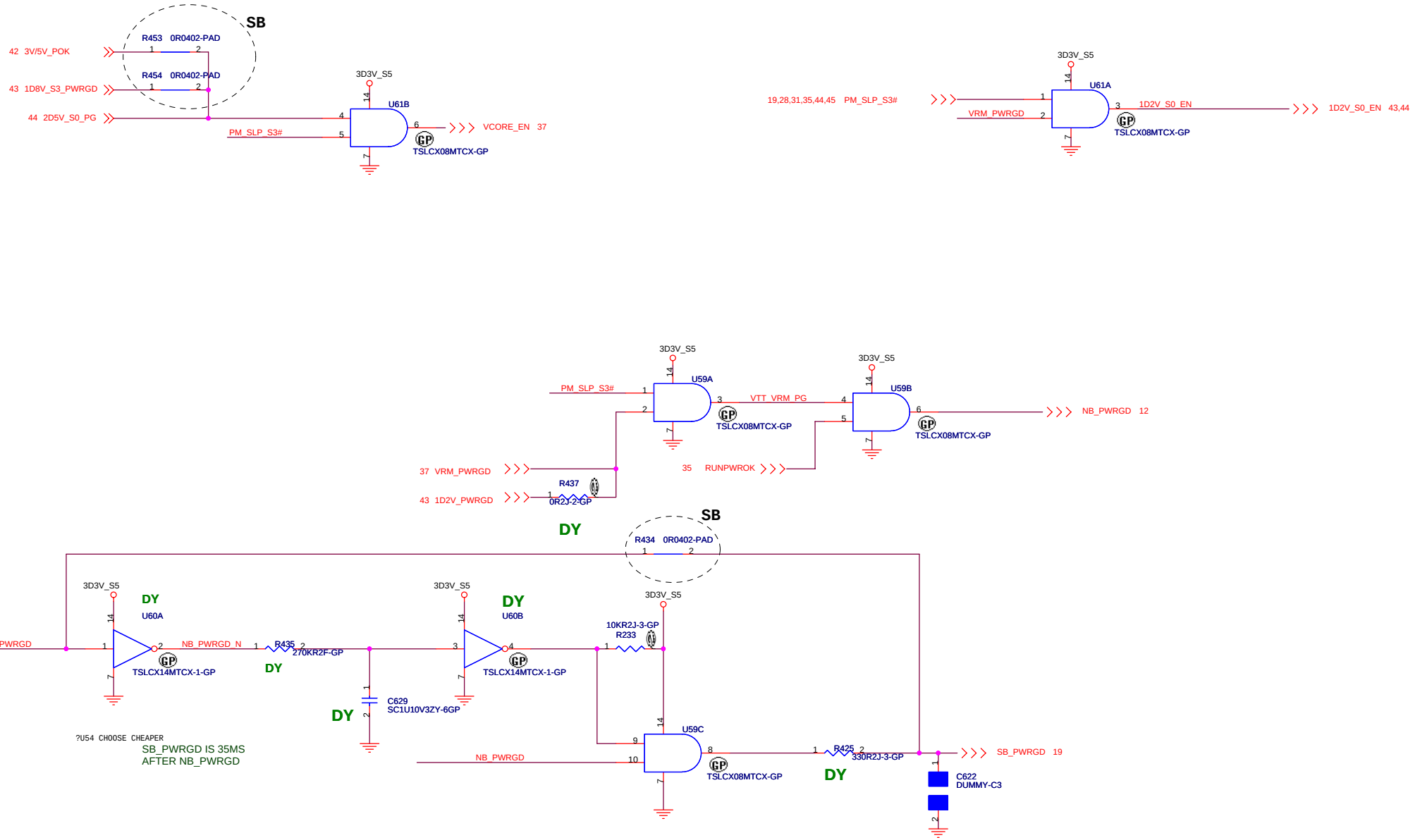
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
BIOS			
Size: A3	Document Number: Orta		Rev: SB
Date: Friday, January 12, 2007	Sheet 33 of 46		



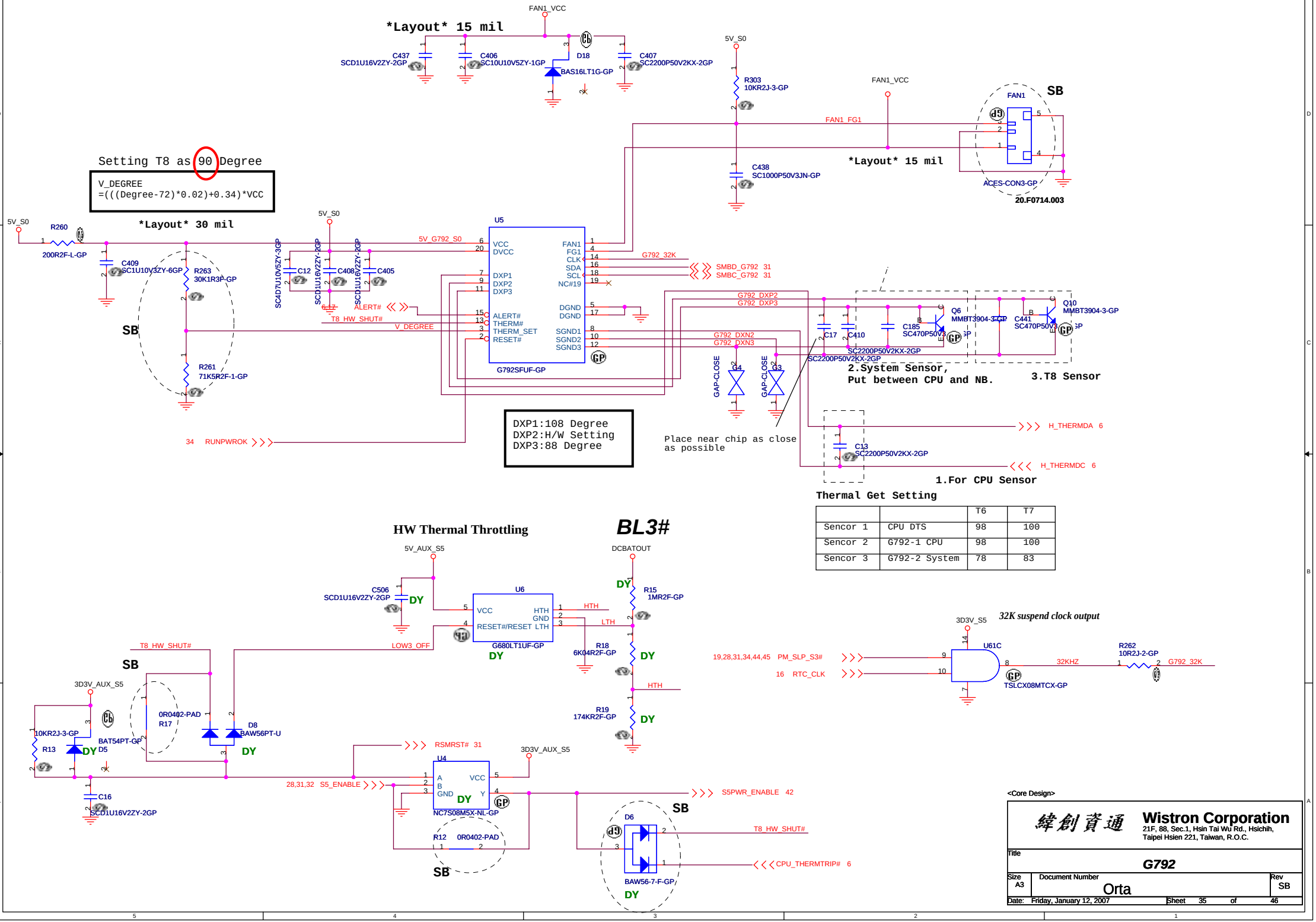
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 34 of 46



		T6	T7
Sencor 1	CPU DTS	98	100
Sencor 2	G792-1 CPU	98	100
Sencor 3	G792-2 System	78	83

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 35 of 46

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

COREFB
COREFB#

Input Power
VCC(I)
VCC(I)
VCC(I)

DCBATOUT
5V_S0
3D3V_S0

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

DCBATOUT_51120

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

Input Signal
(I)

Output Signal
(O)

AD_OFF
AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD_JK
5V_AUX_S5
AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

1D2V (6.5A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

ISL6268_VGA_CORE

VGA_CORE_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

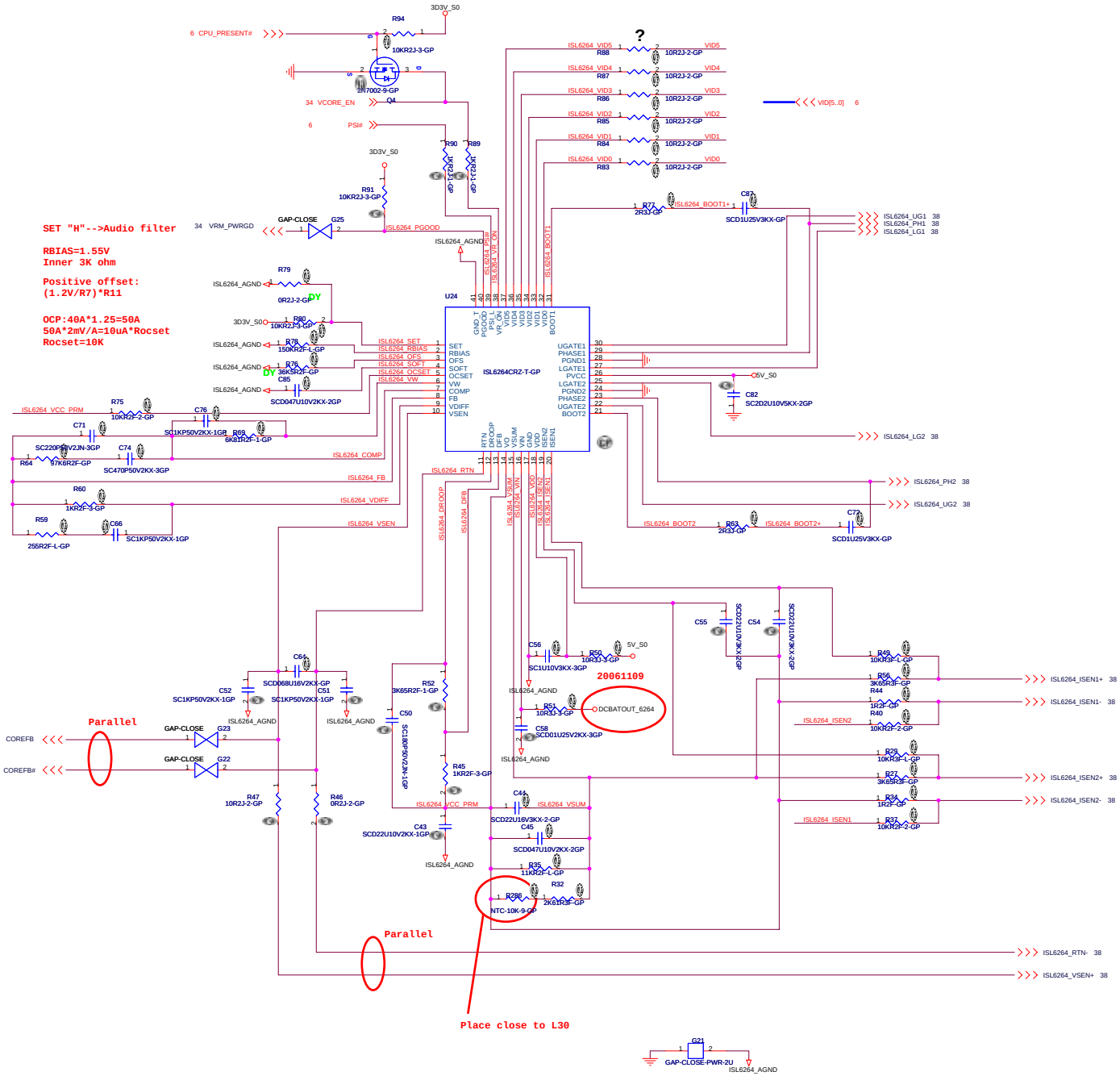
Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 36 of 46

CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



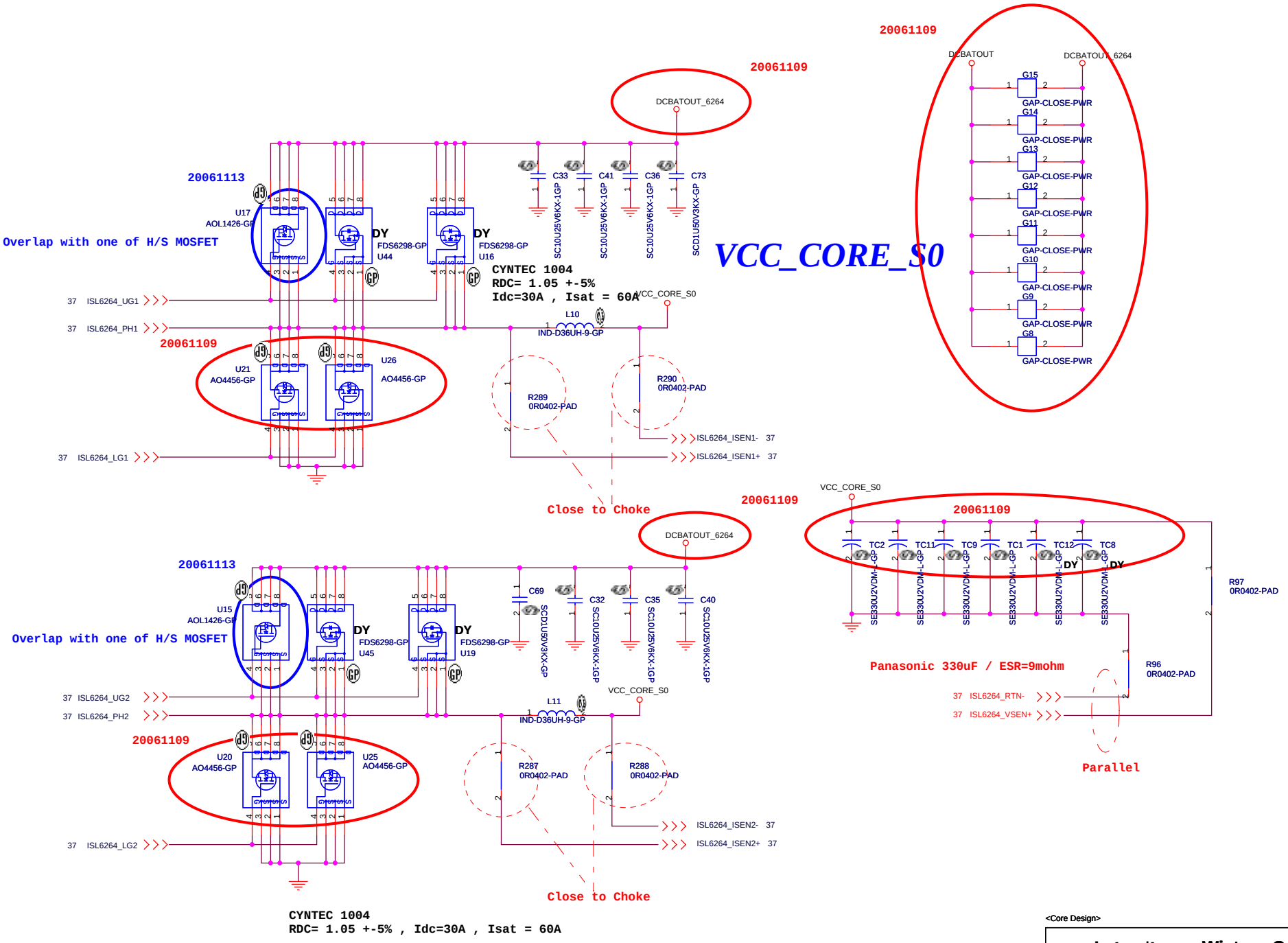
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A2 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 37 of 46



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

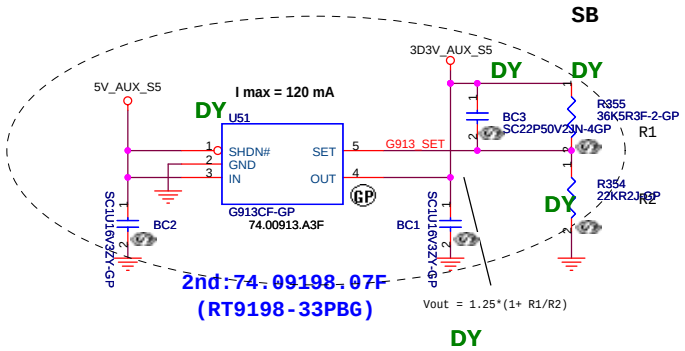
Title: *CPU Vcore Power_2*

Size	Document Number	Rev
A3	Orta	SB

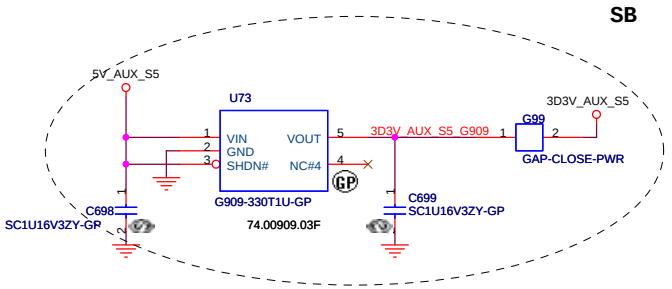
Date: Friday, January 12, 2007 Sheet 38 of 46

Aux Power

3D3V_AUX_S5



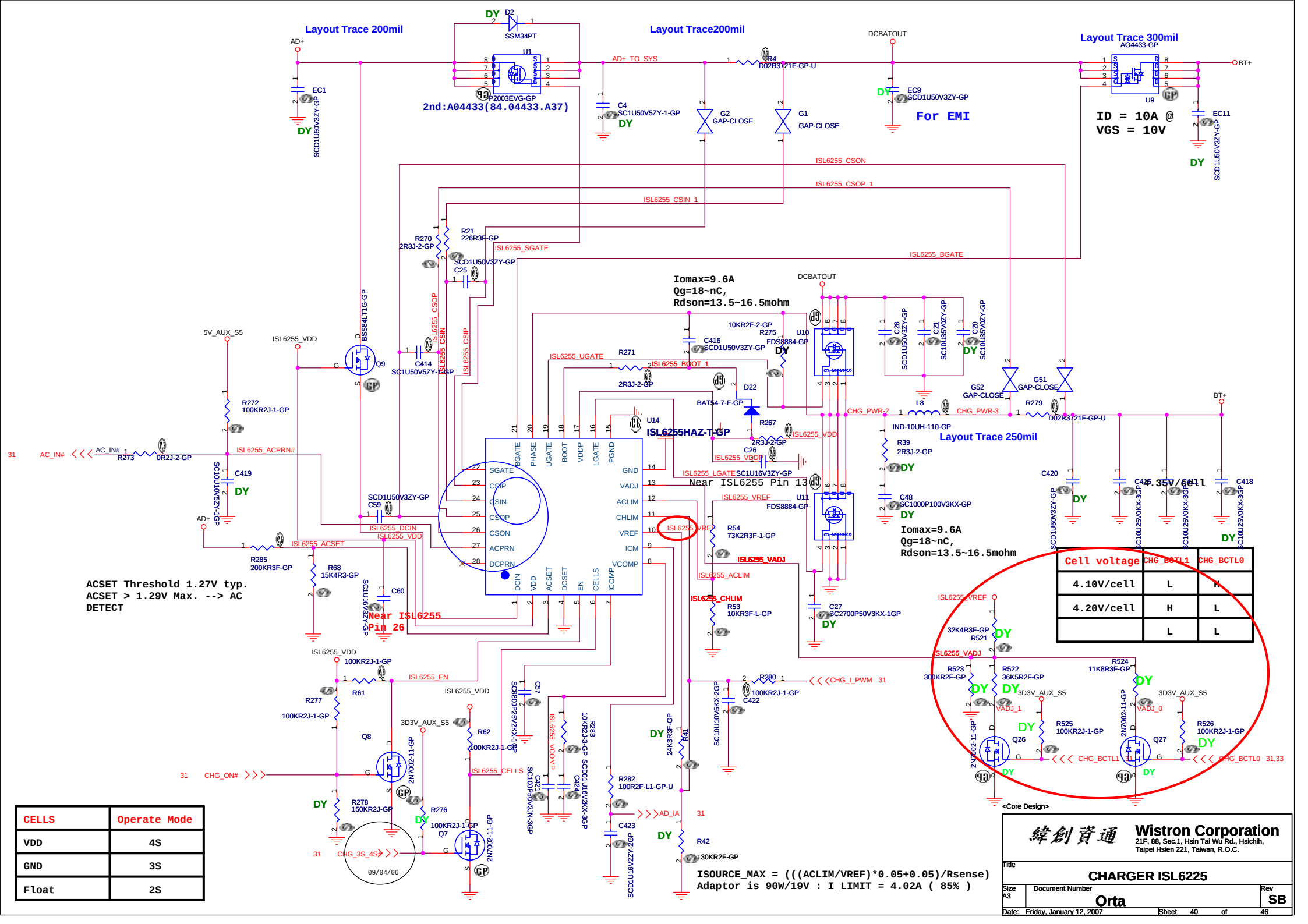
Aux Power 3D3V_AUX_S5



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3D3V_AUX		
Size: A3	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 39 of 46	



Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

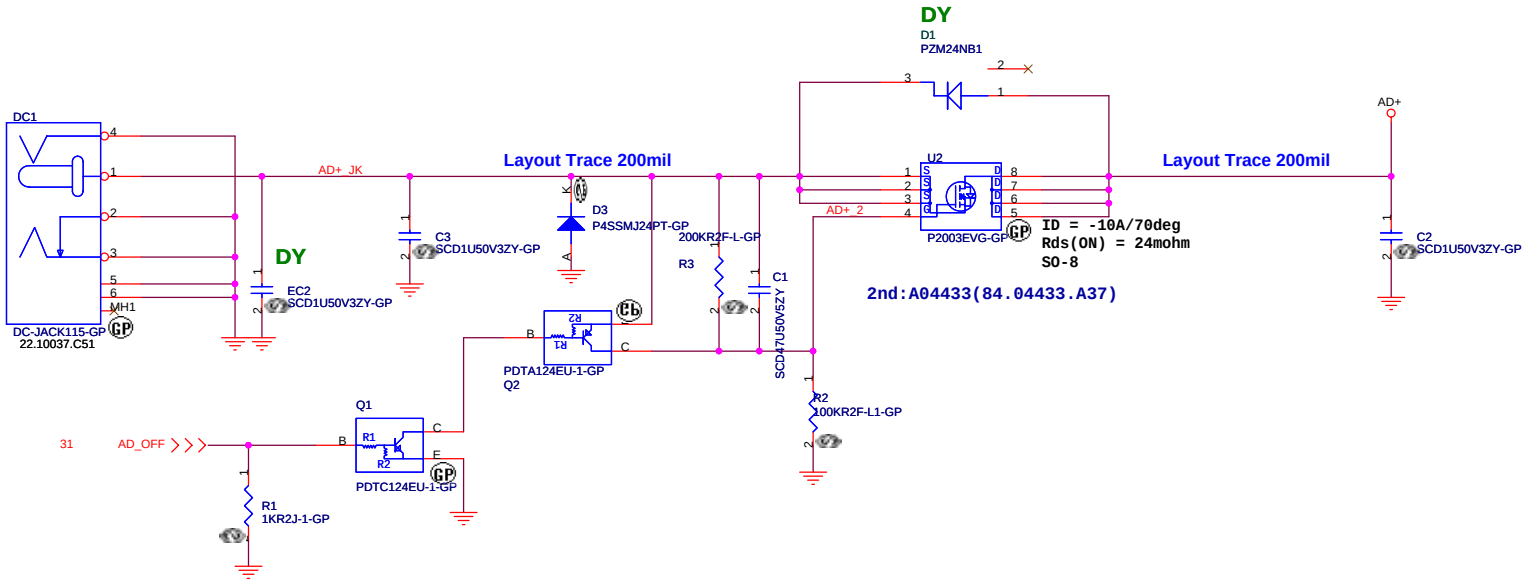
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

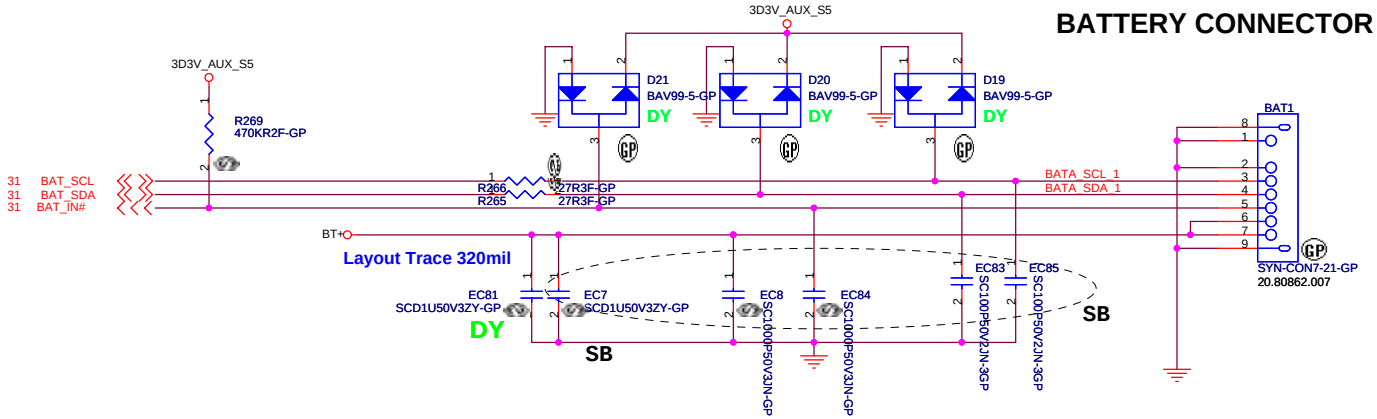
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 40 of 46

Adaptor in to generate DCBATOUT



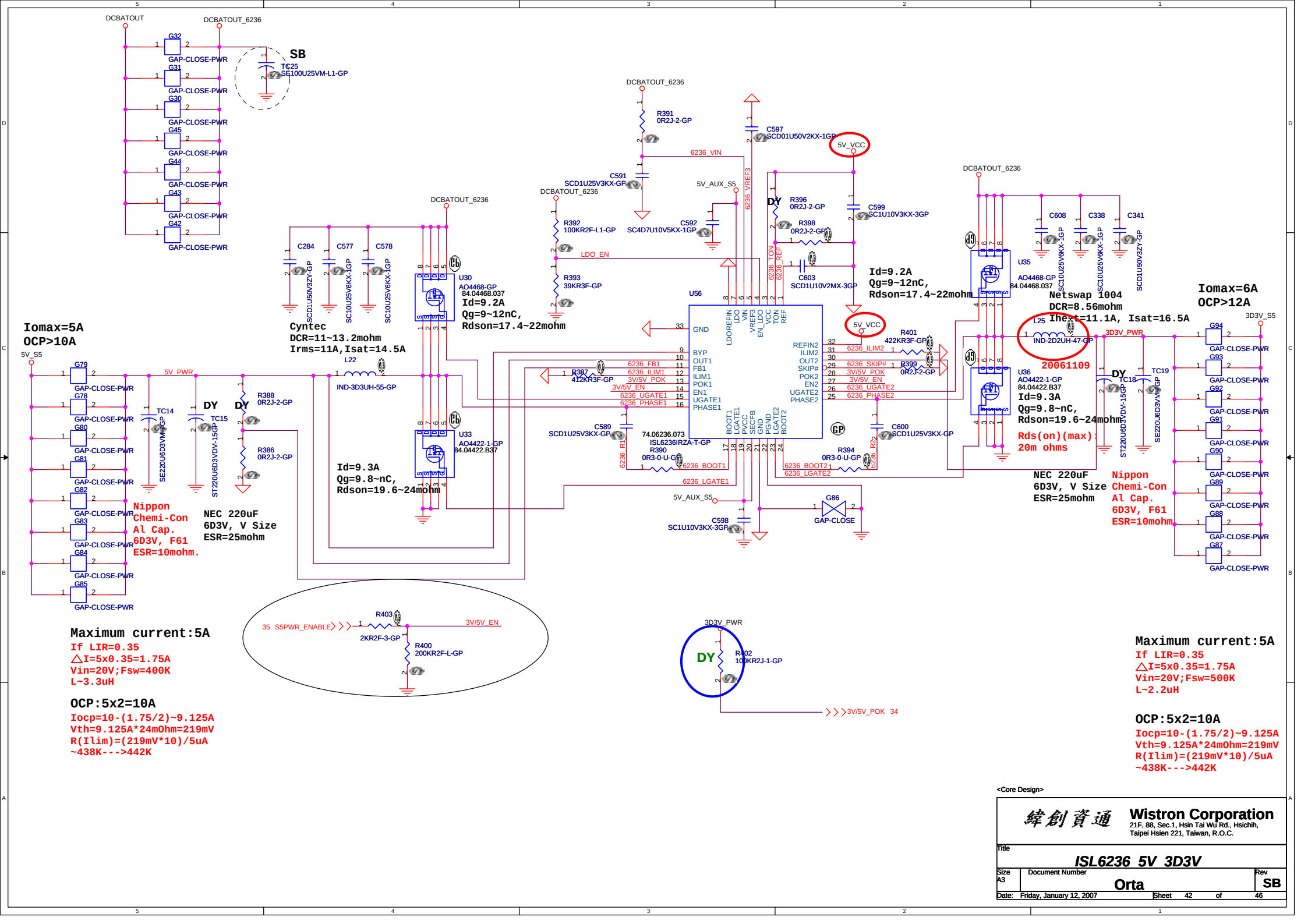
BATTERY CONNECTOR



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

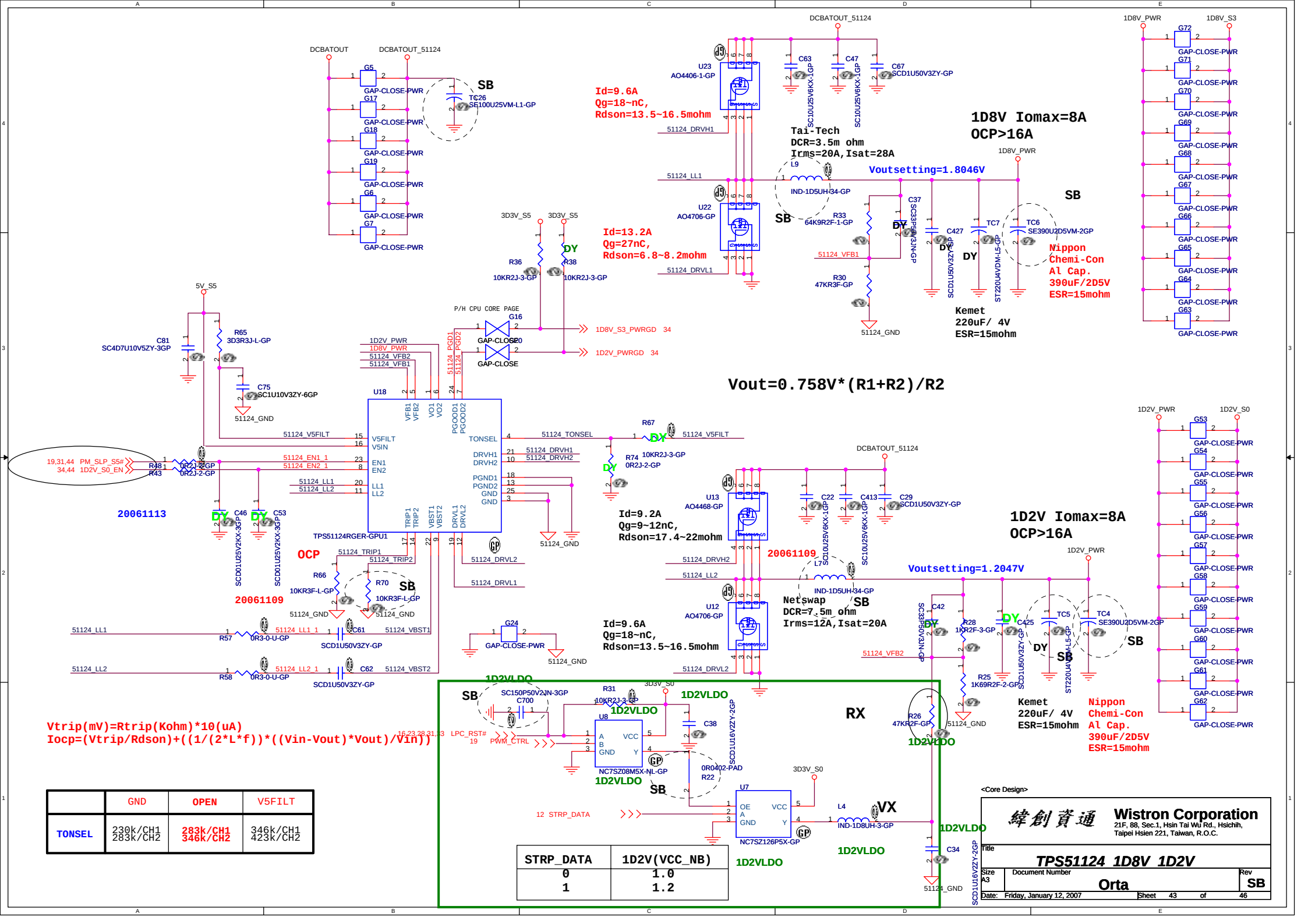
Title	AD/BATT CONN	
Size A3	Document Number Orta	Rev SB
Date: Friday, January 12, 2007	Sheet 41 of 46	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*ISL6236 5V 3D3V*	
Size A3	Document Number **Orta**	Rev **SB**
Date: Friday, January 12, 2007	Sheet 42 of 46	



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

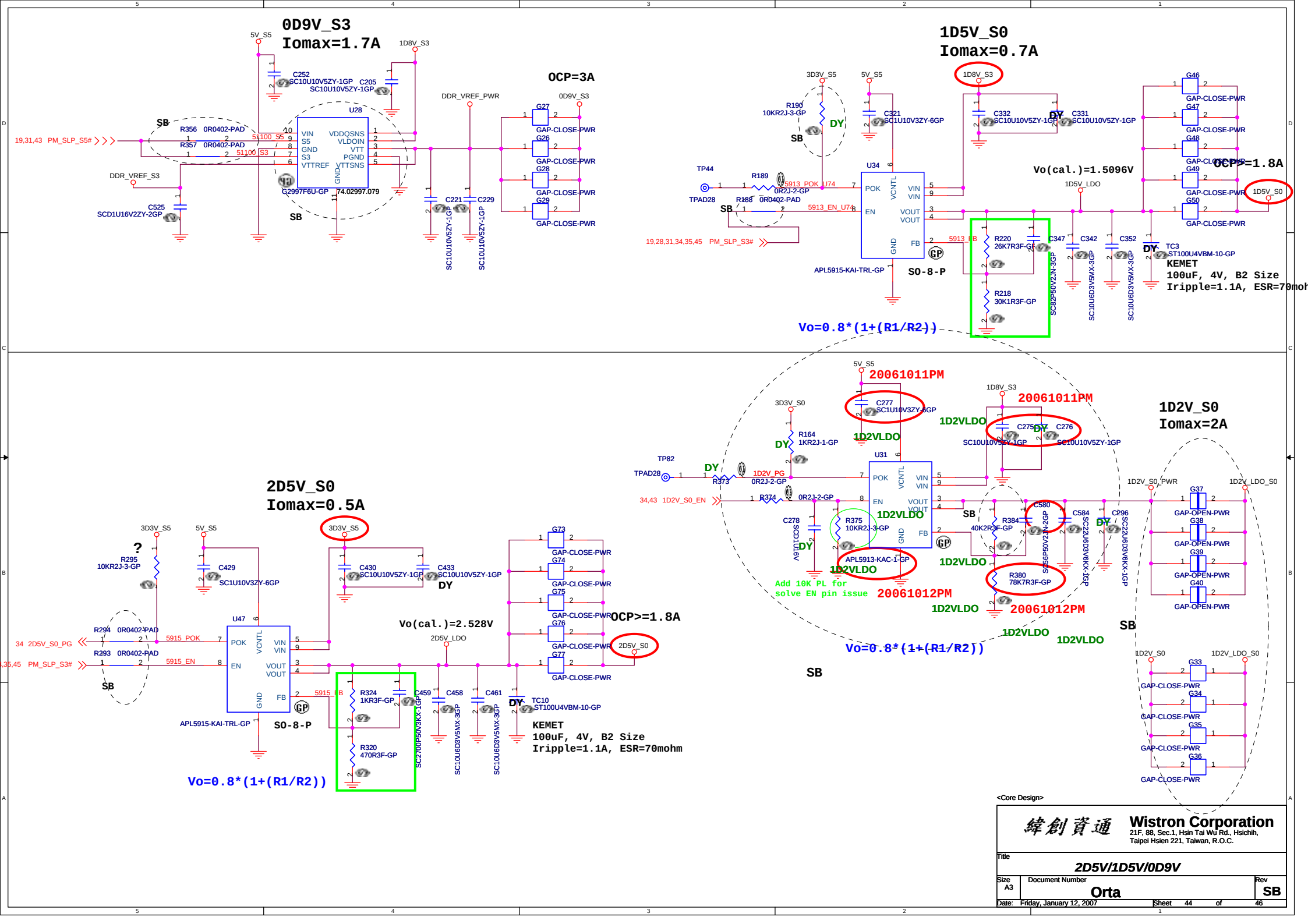
<Core Design>

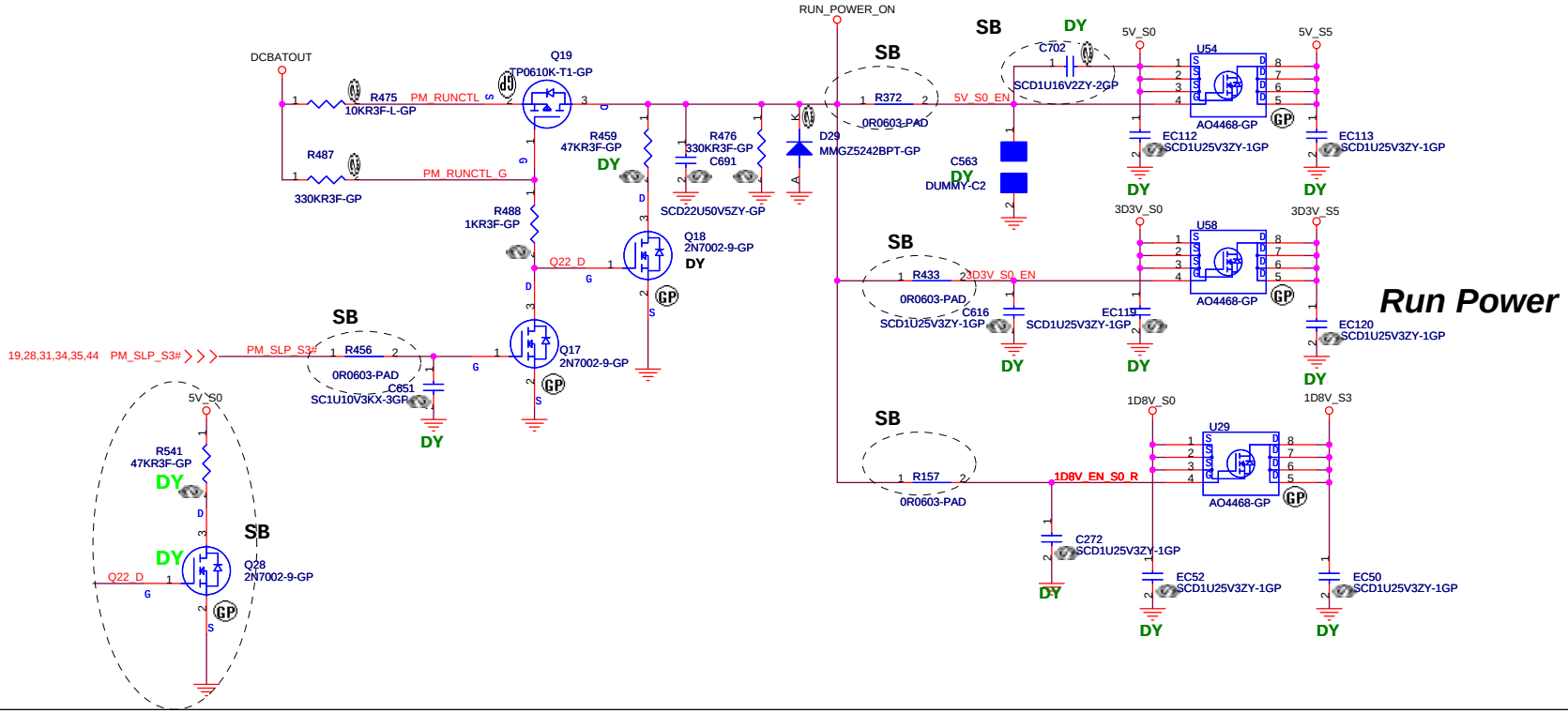
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D2V

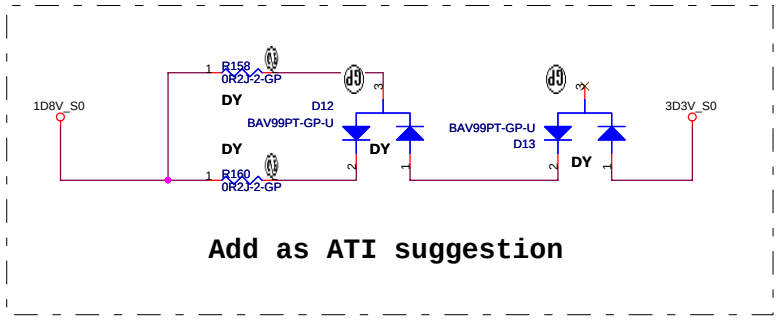
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 43 of 46


0D9V_S3
Iomax=1.7A
OCP=3A
1D5V_S0
Iomax=0.7A
Vo(cal.)=1.5096V
OCP>=1.8A
Vo=0.8*(1+(R1/R2))
2D5V_S0
Iomax=0.5A
Vo(cal.)=2.528V
OCP>=1.8A
Vo=0.8*(1+(R1/R2))
1D2V_S0
Iomax=2A
Vo=0.8*(1+(R1/R2))
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Add 10K PL for
solve EN pin issue
20061011PM
20061012PM
SO-8-P
APL5915-KAI-TRL-GP
APL5913-KAC-1-GP
G2997F6U-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
2D5V/1D5V/0D9V
Orta
Friday, January 12, 2007



Run Power



Add as ATI suggestion

Power On Logic

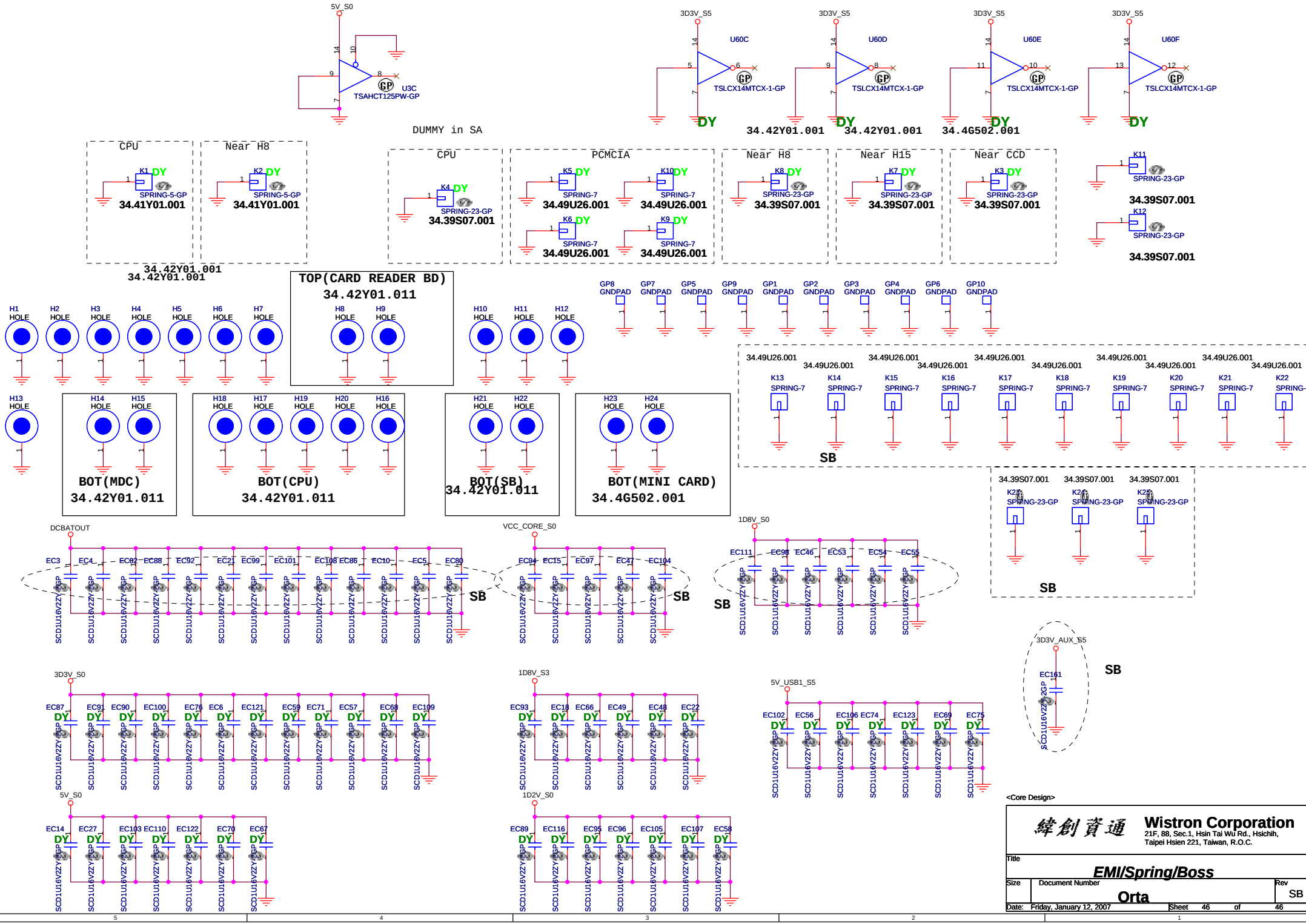
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWR CTL LOGIC / PWR PLANE

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 45 of 46


5V_S0
U3C
TSAHCT125PW-GP
DUMMY in SA
3D3V_S5
U60C
U60D
U60E
U60F
TSLCX14MTCX-1-GP
DY
34.42Y01.001
34.42Y01.001
34.4G502.001
CPU
Near H8
K1 DY
K2 DY
SPRING-5-GP
34.41Y01.001
34.41Y01.001
34.42Y01.001
34.42Y01.001
CPU
PCMCIA
Near H8
Near H15
Near CCD
K4 DY
SPRING-23-GP
34.39S07.001
K5 DY
K10 DY
K6 DY
K9 DY
SPRING-7
34.49U26.001
K8 DY
K7 DY
K3 DY
34.39S07.001
K11
K12
TOP(CARD READER BD)
34.42Y01.011
H1 HOLE
H2 HOLE
H3 HOLE
H4 HOLE
H5 HOLE
H6 HOLE
H7 HOLE
H8 HOLE
H9 HOLE
H10 HOLE
H11 HOLE
H12 HOLE
GP8 GNDPAD
GP7 GNDPAD
GP5 GNDPAD
GP9 GNDPAD
GP1 GNDPAD
GP2 GNDPAD
GP3 GNDPAD
GP4 GNDPAD
GP6 GNDPAD
GP10 GNDPAD
K13
K14
K15
K16
K17
K18
K19
K20
K21
K22
SB
H13 HOLE
H14 HOLE
H15 HOLE
H18 HOLE
H17 HOLE
H19 HOLE
H20 HOLE
H16 HOLE
H21 HOLE
H22 HOLE
H23 HOLE
H24 HOLE
BOT(MDC)
34.42Y01.011
BOT(CPU)
34.42Y01.011
BOT(SB)
34.42Y01.011
BOT(MINI CARD)
34.4G502.001
DCBATOUT
VCC_CORE_S0
1D8V_S0
3D3V_AUX_S5
EC161
3D3V_S0
1D8V_S3
5V_USB1_S5
5V_S0
1D2V_S0
SCD1U16V2ZY-2GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 46 of 46