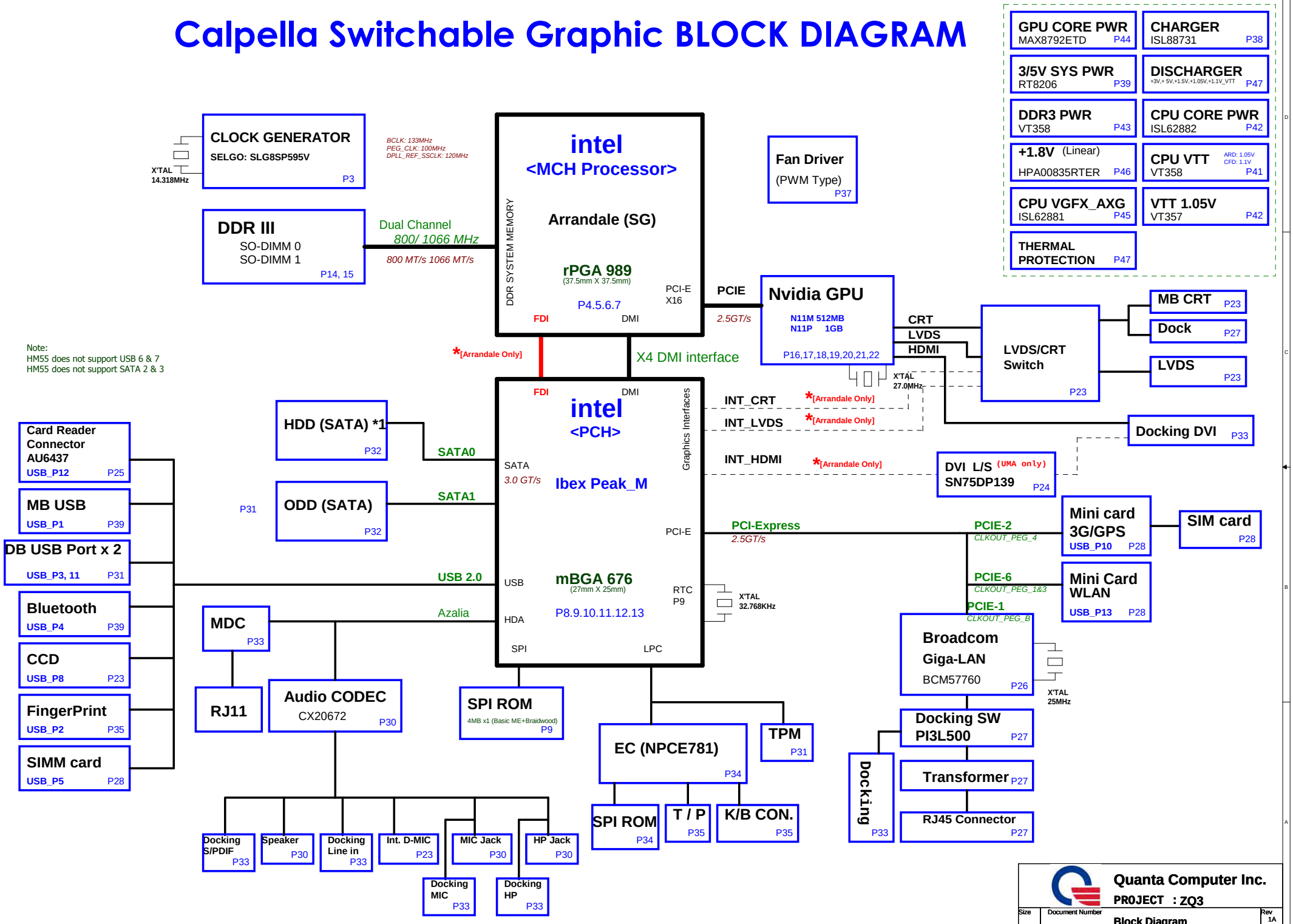
Calpella Switchable Graphic BLOCK DIAGRAM



Quanta Computer Inc.
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Size | Document Number: Block Diagram | Rev 1A
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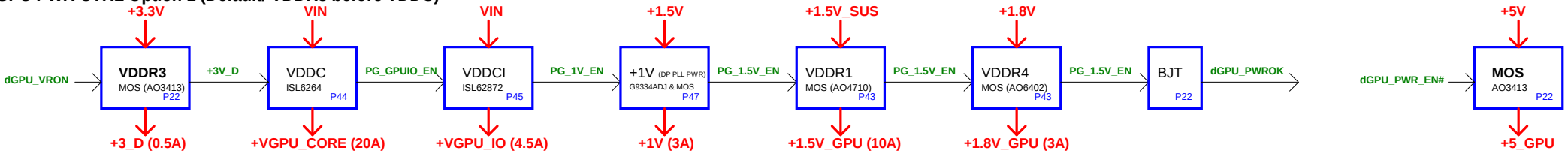
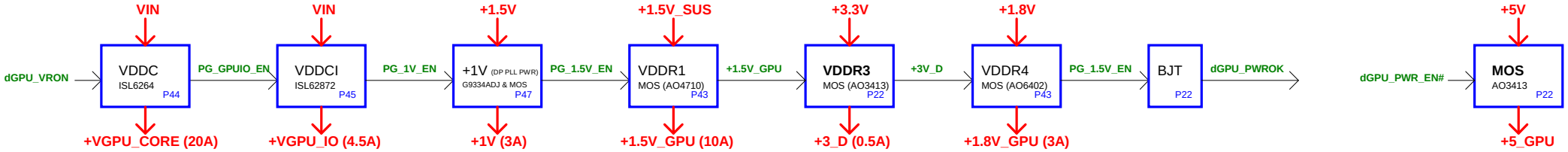
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



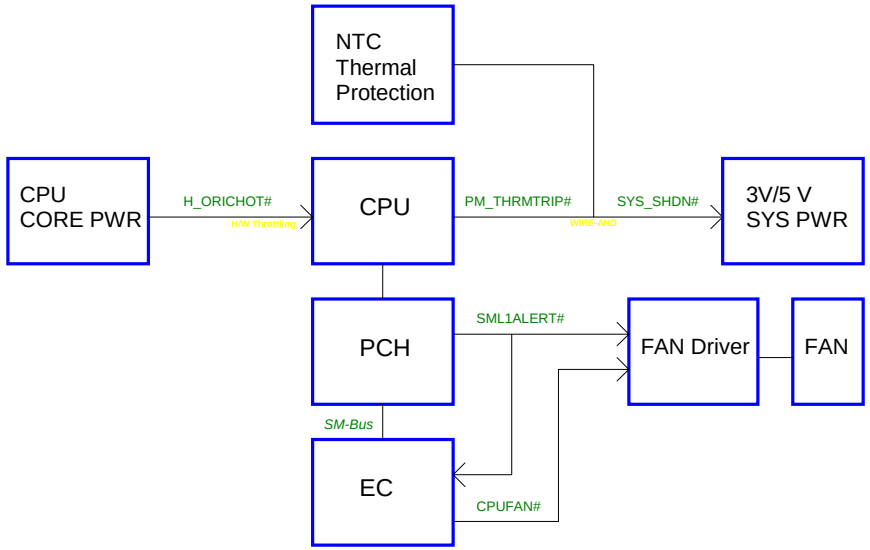
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

Thermal Follow Chart



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Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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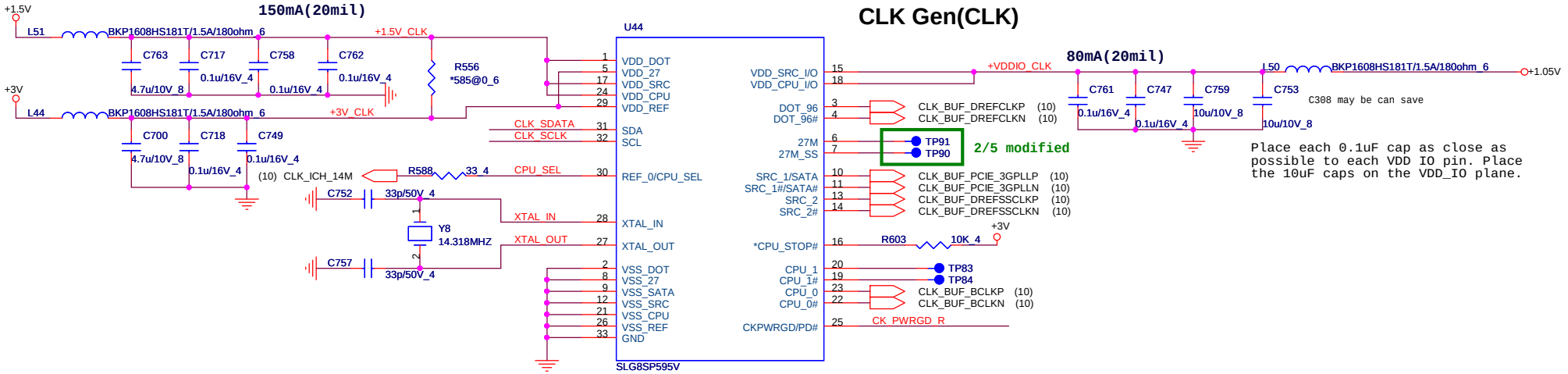
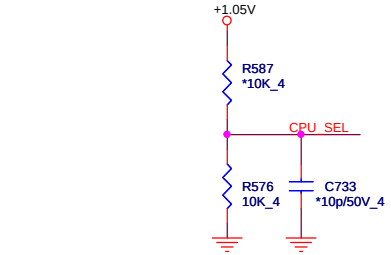
CLK Gen(CLK)

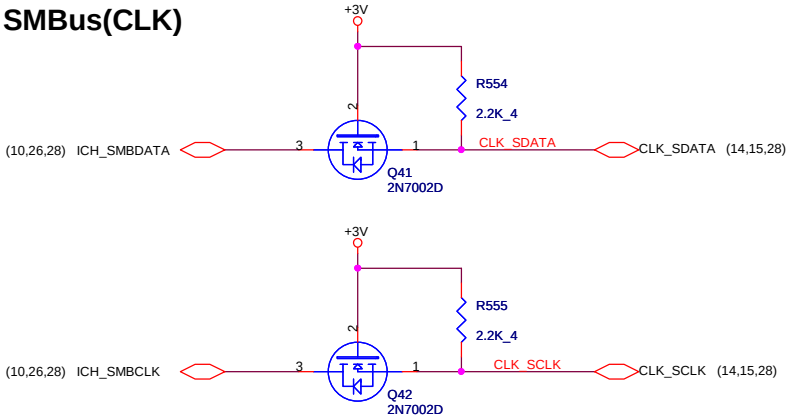


CPU_CLK select(CLK)

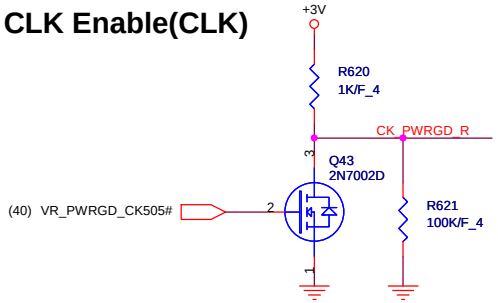


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



CLK Enable(CLK)



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	Clock Generator	1A
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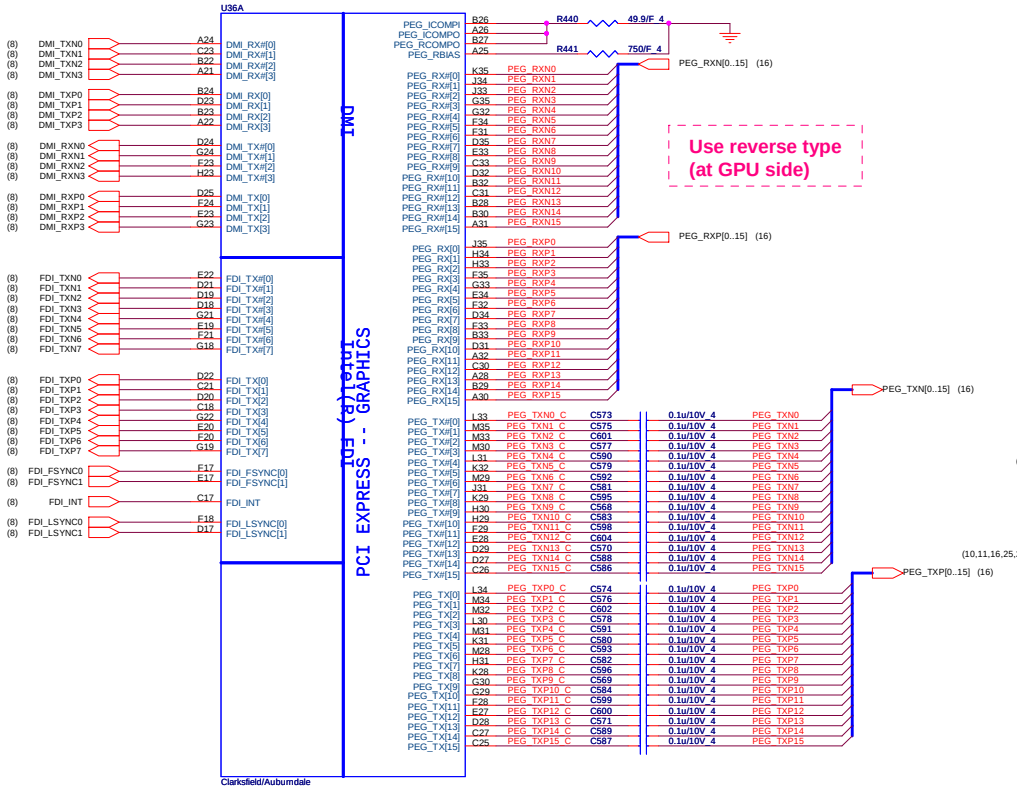
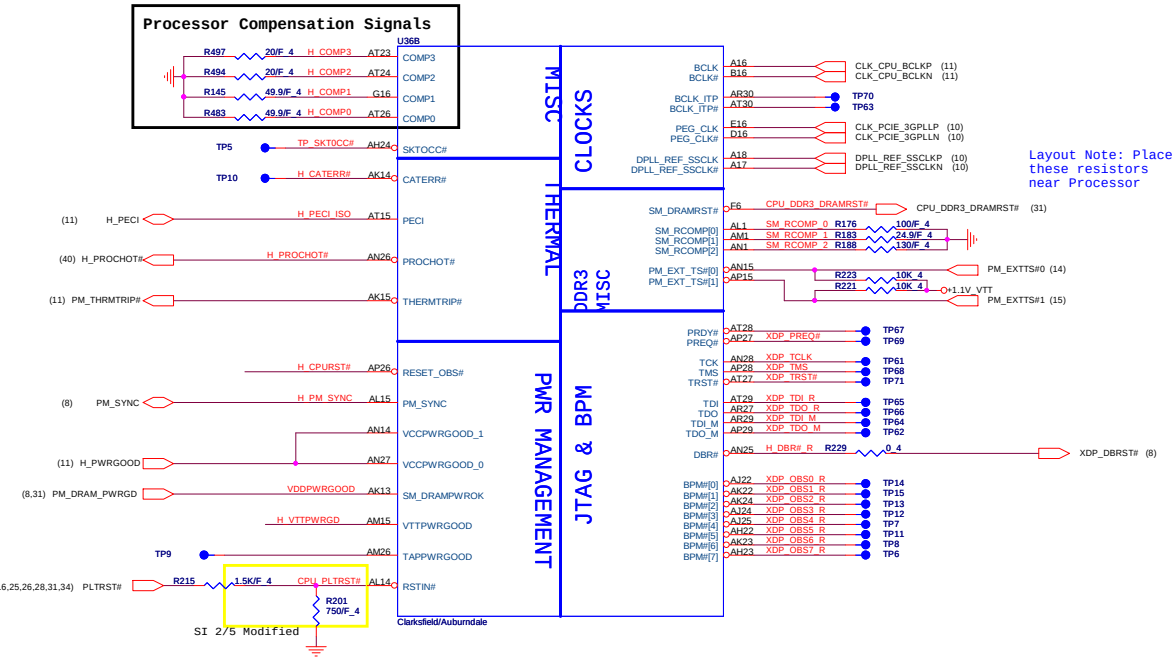
Arrandale_1(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



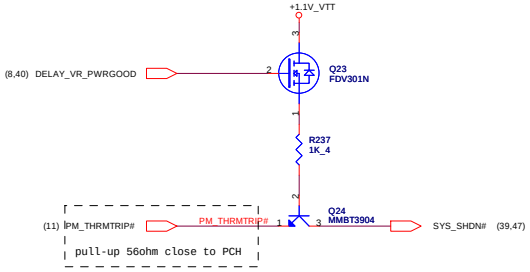
Use reverse type (at GPU side)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

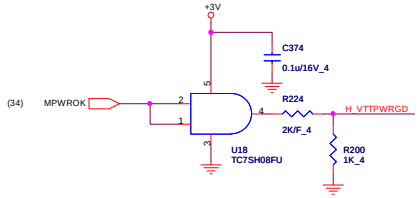


Layout Note: Place these resistors near Processor

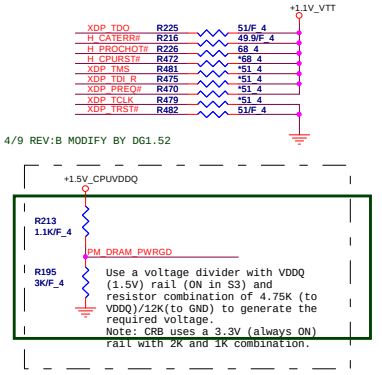
Thermaltrip protect



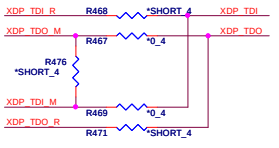
VTT PWR_Good



Processor pull-up



JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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	AUBURNDA 1/4	1A

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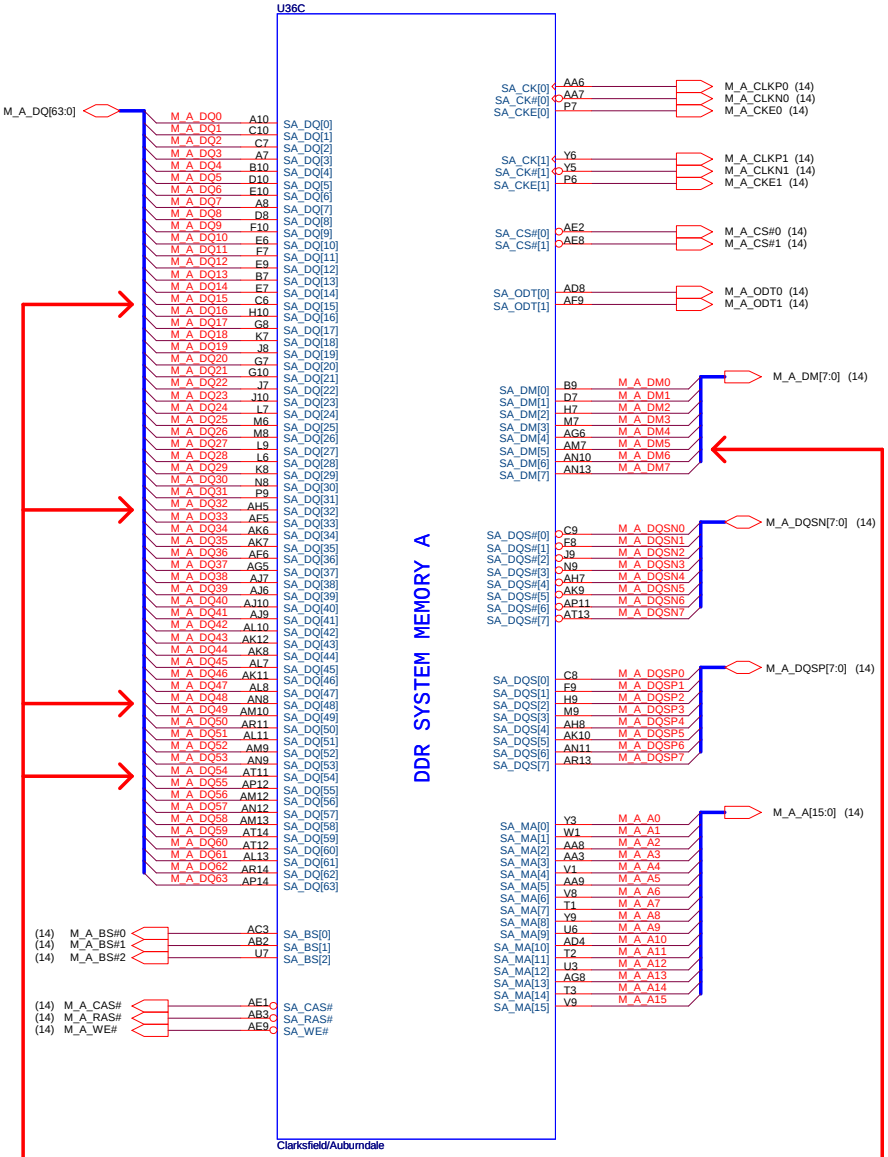
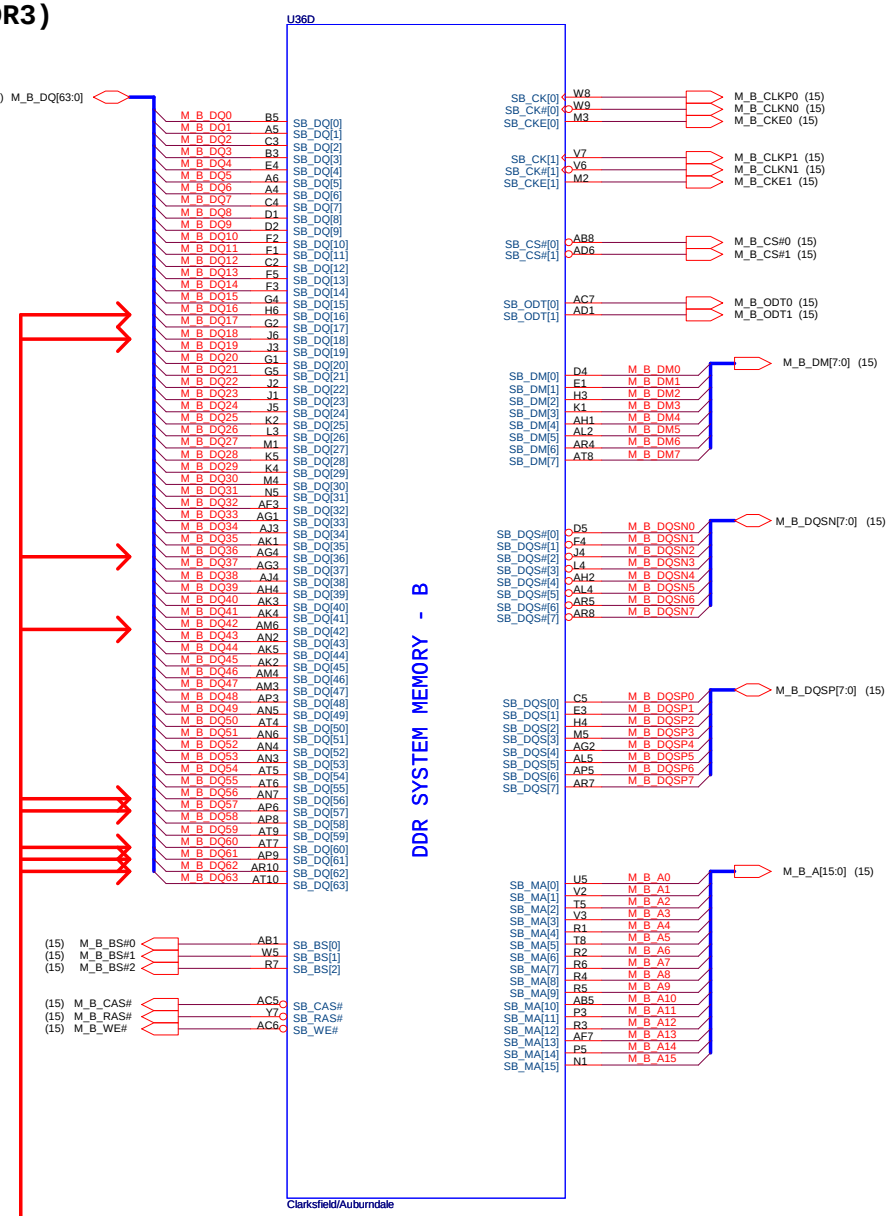
Arrandale_2(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





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Arrandale_3(CPU)

CPU Core Power

ARD:48A
CFD:52A

+VCC_CORE

U36F

C264 *330u/2V_7343
C295 330u/2V_7343
C281 *330u/2V_7343
C296 330u/2V_7343

C621 C633 C274 C304 C330 C334 C333 C628 — 22u/6.3V_8

C627 C332 C632 C310 C311 C331 C635 C634 — 22u/6.3V_8

C625 C327 C325 C320 C626 C285 C278 C623 — 10u/6.3V_6

C329 C324 C276 C323 C277 C328 C275 C631 — 10u/6.3V_6

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER / CPU CORE SUPPLY

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

18A

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

C309 C303 22u/6.3V_8
C618 22u/6.3V_8
C284 330u/2V_7343
+1.1V_VTT

C271 C629 C622 C636 — 10u/6.3V_8
C630 C615 C272 — 10u/6.3V_8

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 V10 W10 U10 T10 J12 J11 J16 J15

C282 C611 22u/6.3V_8
+1.1V_VTT
+VTT_43
+VTT_44
R143 R144 0_4
(15mils)
C251 1u/10V_4

POWER — CPU VIDS

PSI# — AN33 H_PSI# — H_PSI# (40)

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6] PROC_DPRSLPVR

AK35 H_VID0
AK33 H_VID1
AK34 H_VID2
AL35 H_VID3
AL33 H_VID4
AM33 H_VID5
AM35 H_VID6
AM34 H_DPRSLPVR

H_VID0 (40)
H_VID1 (40)
H_VID2 (40)
H_VID3 (40)
H_VID4 (40)
H_VID5 (40)
H_VID6 (40)
H_DPRSLPVR (40)

VTT_SELECT — G15 H_VTTVID1 — TP1

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE — AN35 — I_MON (40)

VCC_SENSE — AJ34 — R162 100_4 — +VCC_CORE — VCCSENSE (40)
VSS_SENSE — AJ35 — R167 100_4 — VSSSENSE (40)

VTT_SENSE — B15 VTT_SENSE — TP56
VSS_SENSE_VTT — A15 VSS_SENSE_VTT — TP57

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

U36G

+VGFX_AXG — 22A

C653 330u/2V_7343
C650 330u/2V_7343

C385 C375 C639 — 22u/6.3V_8
C535 and C1005 may be can save
C637 C381 C384 — 10u/6.3V_8

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

GRAPHICS POWER

+1.1V_VTT
C268 22u/6.3V_8
C612 22u/6.3V_8
J24 J23 H25 — VTT1_45 VTT1_46 VTT1_47

+1.1V_VTT
C620 C294 C288 C335 — 22u/6.3V_8
K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25 — VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

PDL

PEG & DMI

Clarksfield/Auburndale

SENSE LINES

VAXG_SENSE — AR22 — VCC_AXG_SENSE (45)
VSSAXG_SENSE — AT22 — VSS_AXG_SENSE (45)

GRAPHICS VIDs

GFX_VID[0] GFX_VID[1] GFX_VID[2] GFX_VID[3] GFX_VID[4] GFX_VID[5] GFX_VID[6]

AM22 AP22 AN22 AP23 AM23 AP24 AN24

GFX_VID0 (45)
GFX_VID1 (45)
GFX_VID2 (45)
GFX_VID3 (45)
GFX_VID4 (45)
GFX_VID5 (45)
GFX_VID6 (45)

R496 4.7K_4
R492 *10K_4

GFX_VR_EN — AR25 — GFX_ON (45)
GFX_DPRSLPVR — AT25 — GFX_DPRSLPVR (45)
GFX_IMON — AM24 — GFX_IMON (45)

DDR3 - 1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_CPUVDDQ
C353 C292 C315 C286 C308 — 1u/10V_4
C266 22u/6.3V_8
C265 22u/6.3V_8
C261 330u/2V_7343

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62

P10 N10 L10 K10

+1.1V_VTT
C616 10u/6.3V_6
C610 10u/6.3V_6

VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

J22 J20 J18 H21 H20 H19

C614 22u/6.3V_8
C613 22u/6.3V_8

1.8V

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

0.6A
+1.8V
C273 1u/10V_4
C280 1u/10V_4
C619 2.2u/10V_6
C617 4.7u/10V_6
C270 22u/6.3V_8

+1.1V_VTT

R191 R186 R194 R197 R203 R228 R218 R181 R174 — 1K_4 *1K_4

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
H_DPRSLPVR
H_PSI#

R190 R185 R193 R196 R202 R227 R217 R180 R173 — 1K_4 *1K_4

Note:
For Validating IMVP VR R6451 should be STUFF and R2N1 NO_STUFF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
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	AUBURNDA 3/4 (PWR)	1A

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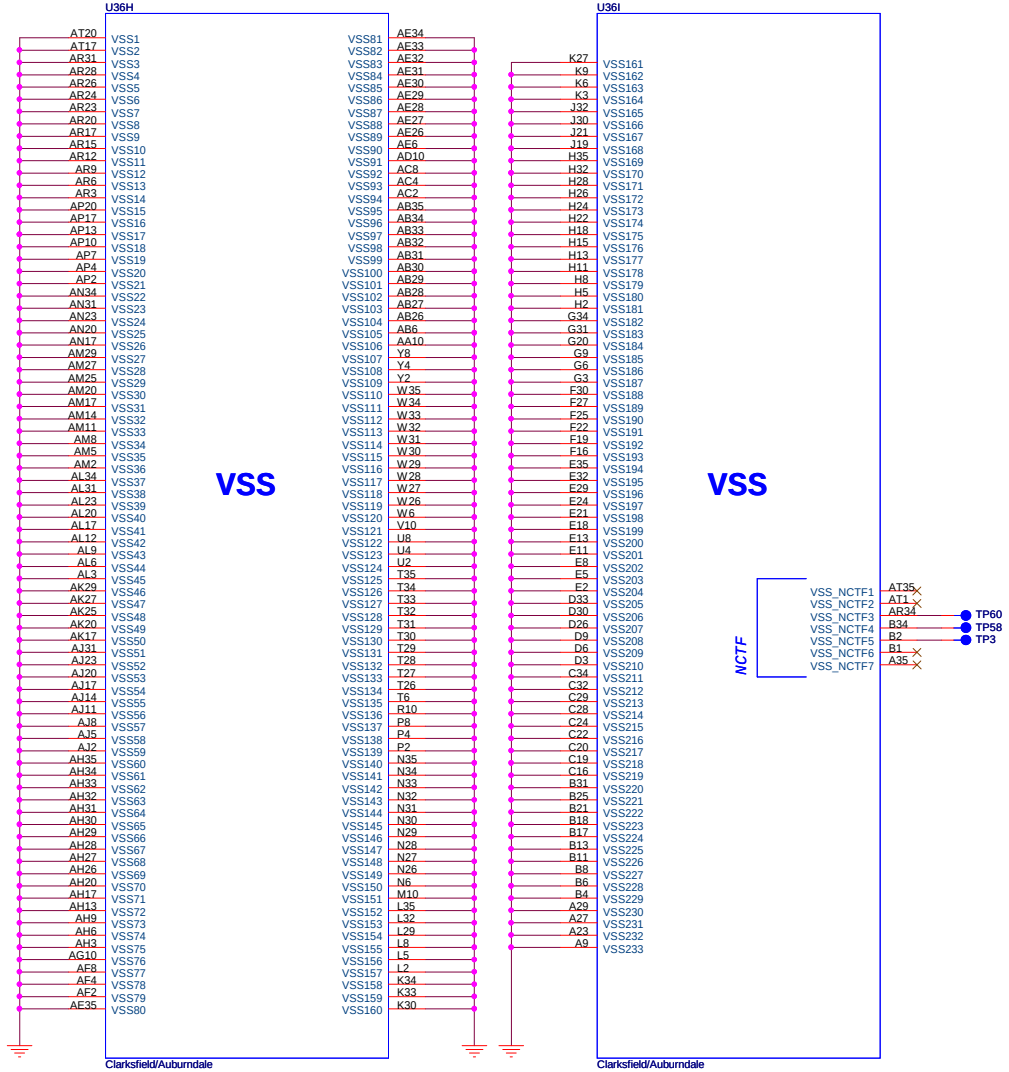
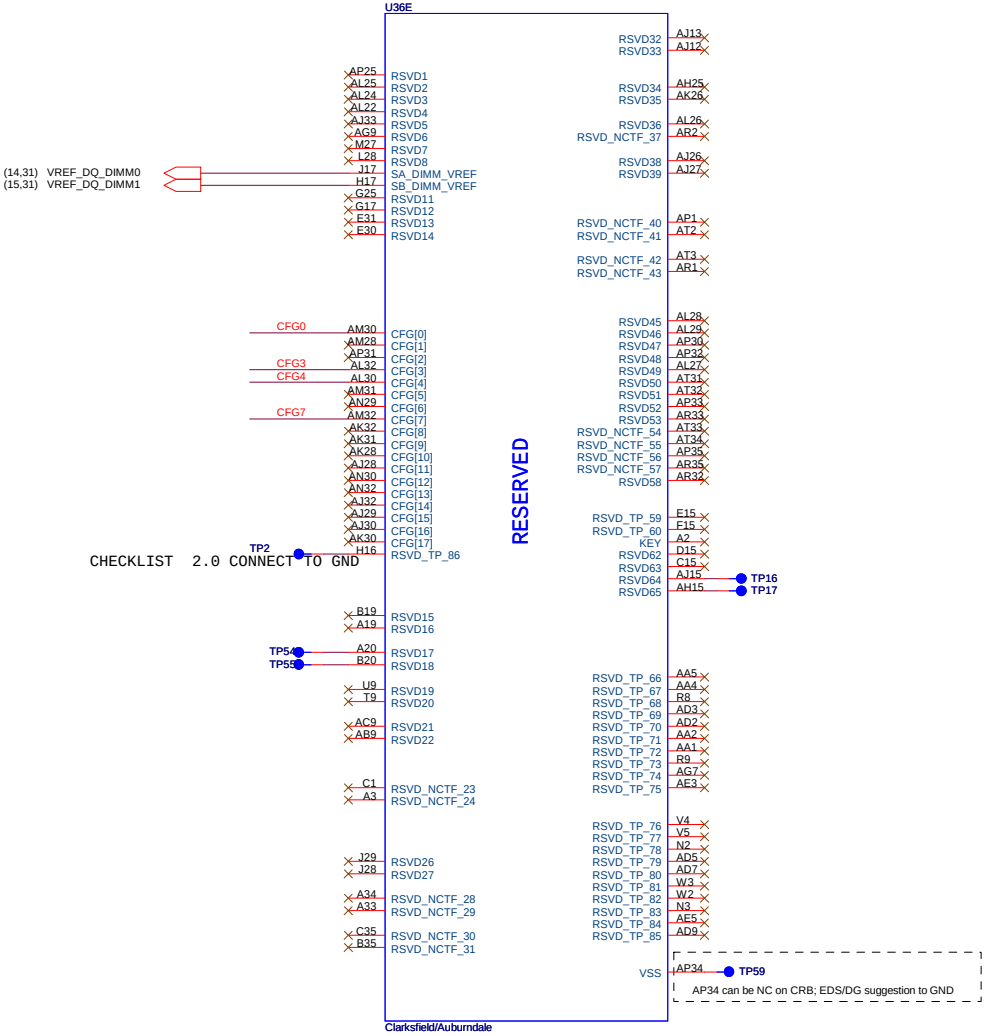
Arrandale_4(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

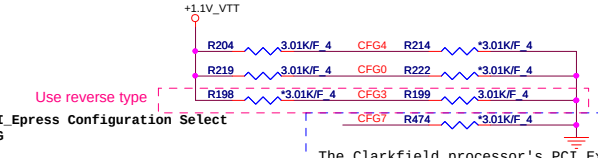


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

Quanta Computer Inc.
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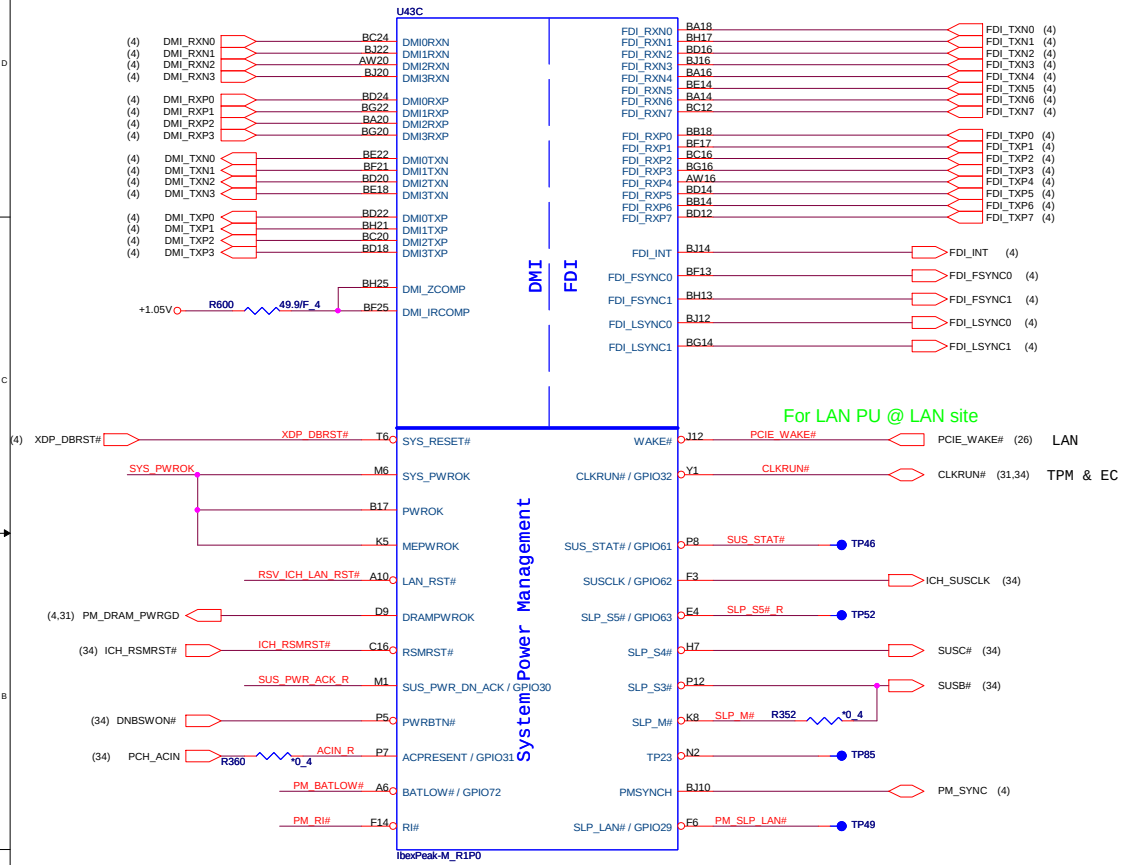
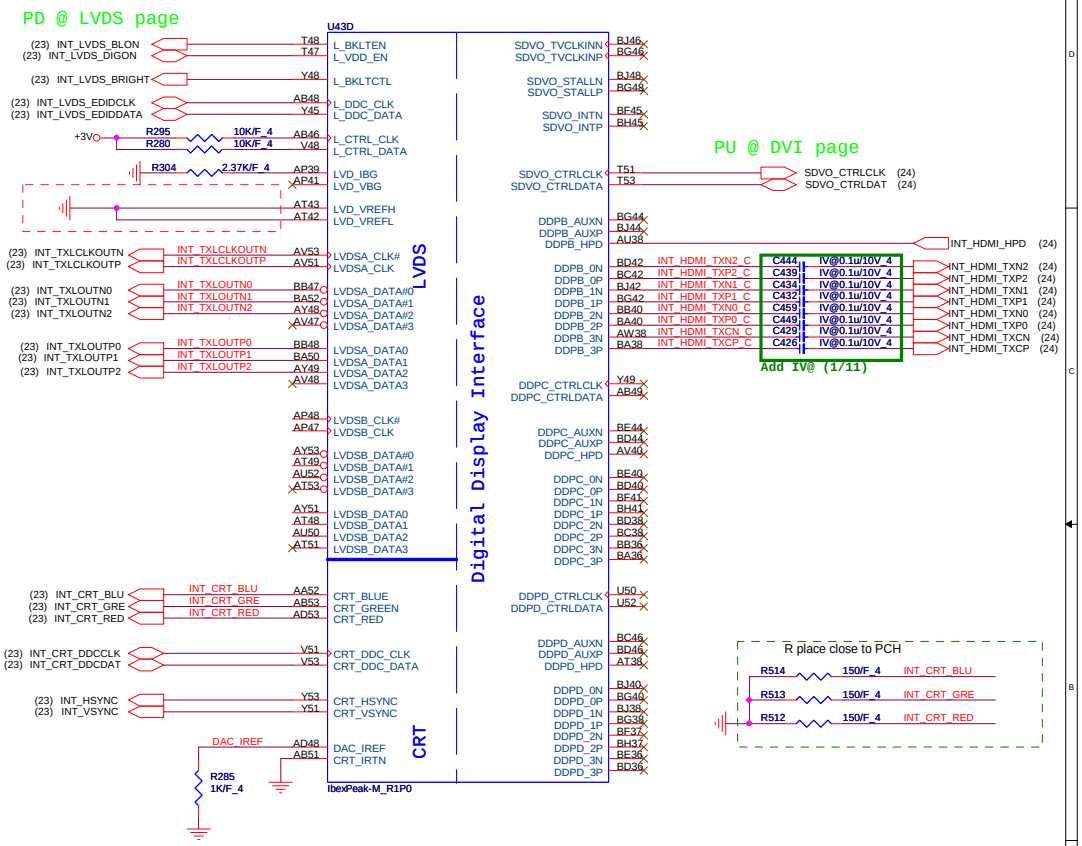
PCH1(CLG)

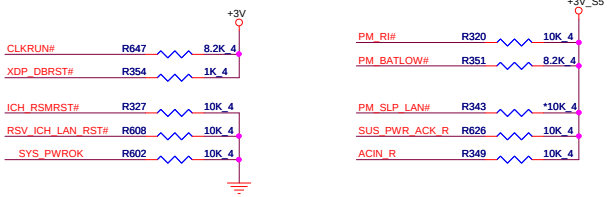
IBEX PEAK-M (DMI,FDI,GPIO)



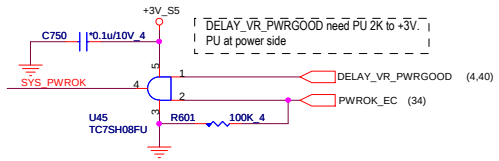
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low(CLG)



System PWR_OK(CLG)



Quanta Computer Inc.

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	IBEX PEAK-M 1/6	1A

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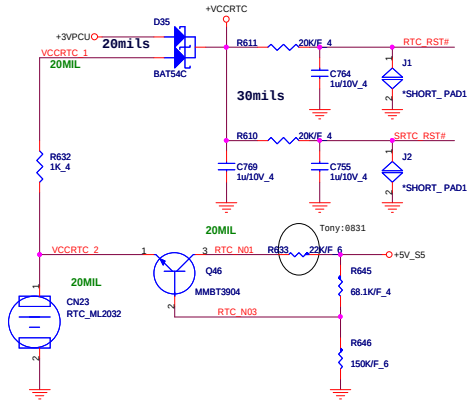
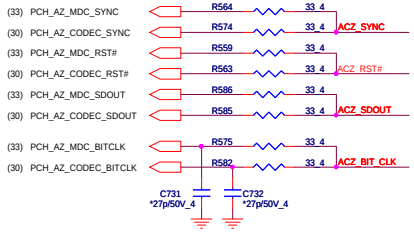
RTC Circuitry(RTC)

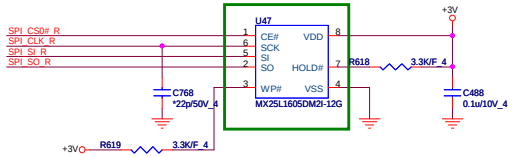


HDA Bus(CLG)



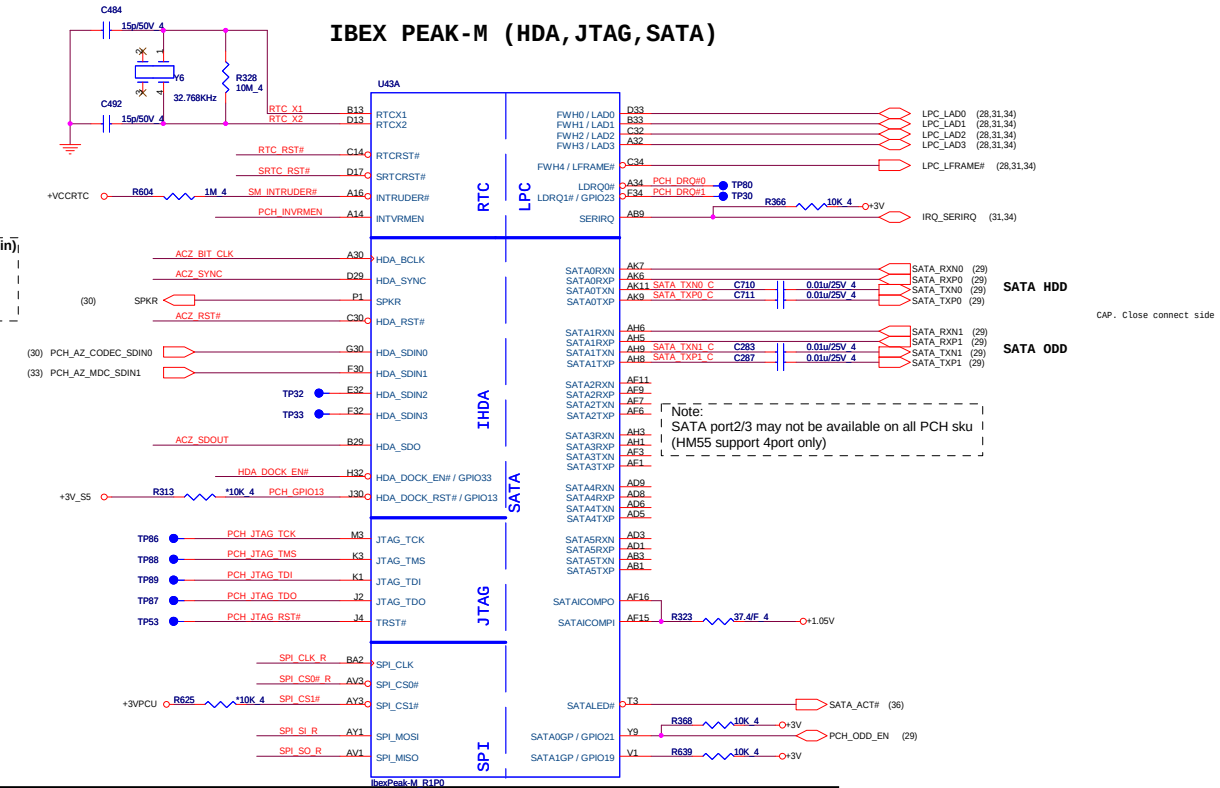
Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)



PCH2(CLG)

IBEX PEAK-M (HDA,JTAG,SATA)



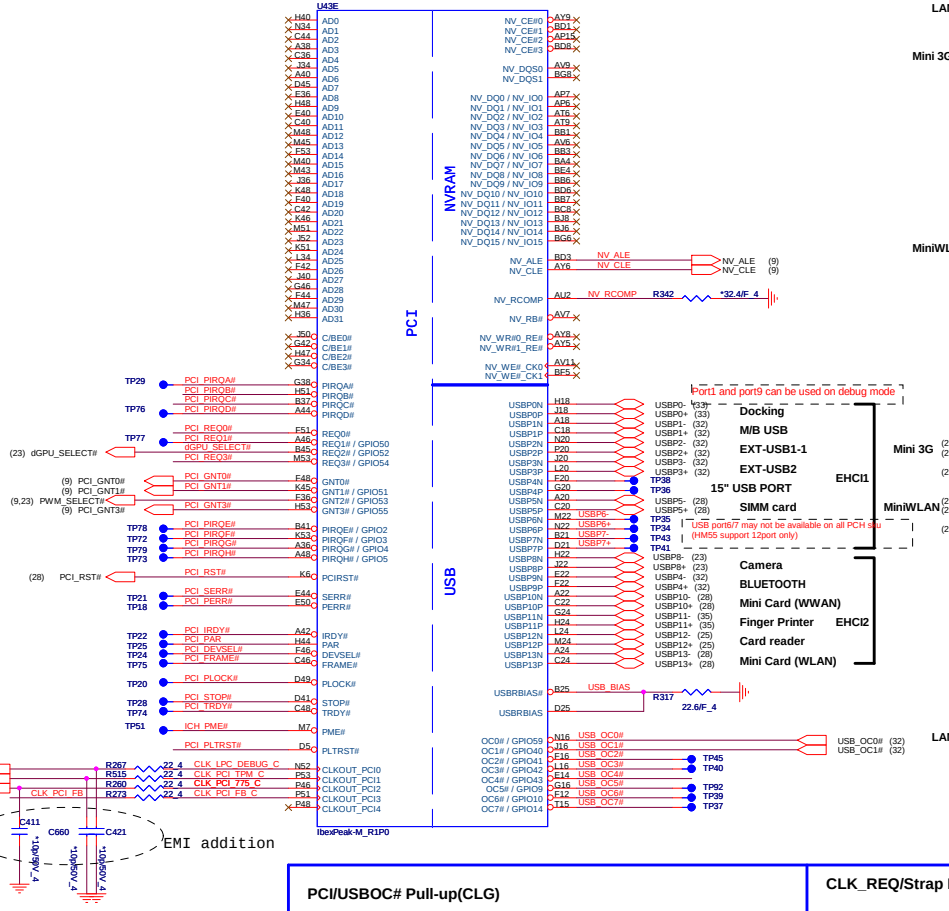
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R642 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R519 *4.7K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R606 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** +3V R284 *1K_4 R269 *1K_4 R292 1K_4 R268 1K_4 PCI_GNT0# (10) PCI_GNT1# (10) 1/11 modified
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	R303 *4.7K_4 PWM_SELECT# (10,23)
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R624 *1K_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R341 *1K_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R592 *1K_4 R594 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R623 *8.2K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R336 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R324 *10K_4 RSV_GPIO27 (11)
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R346 1K_4 CR_WAKE# (11)

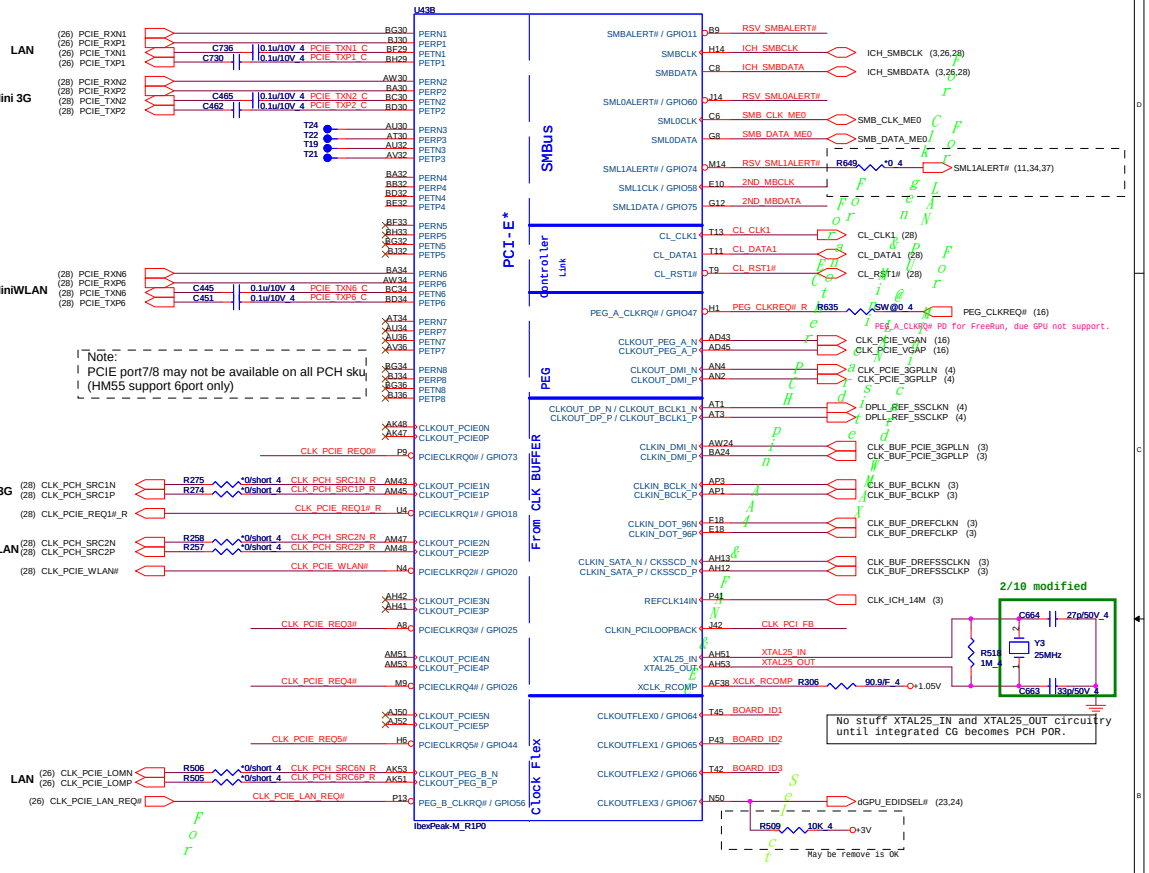
from PCH and to control SW (EC or PCH control Brightness switch)

PCH3(CLG)

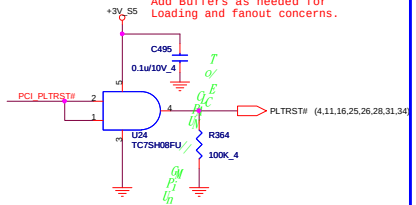
IBEX PEAK-M (PCI,USB,NVRAM)



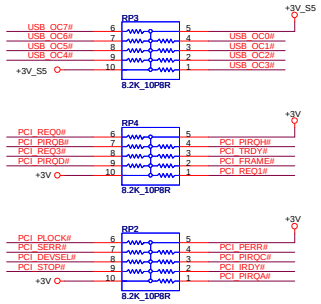
IBEX PEAK-M (PCI-E,SMBUS,CLK)



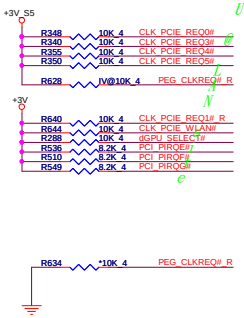
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



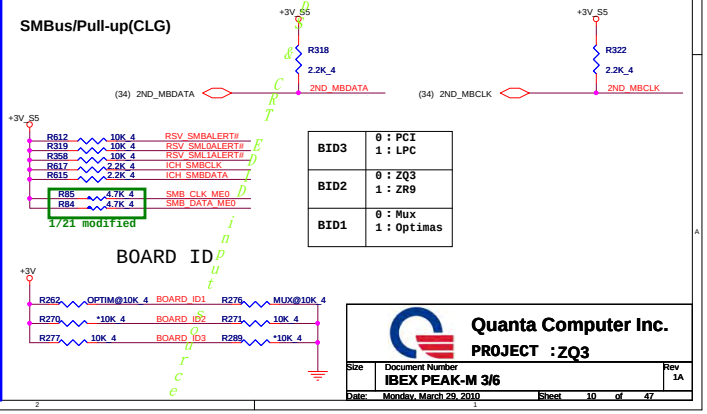
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up(CLG)



BID3	0 : PCI 1 : LPC
BID2	0 : ZQ3 1 : ZR9
BID1	0 : Mux 1 : Optimas

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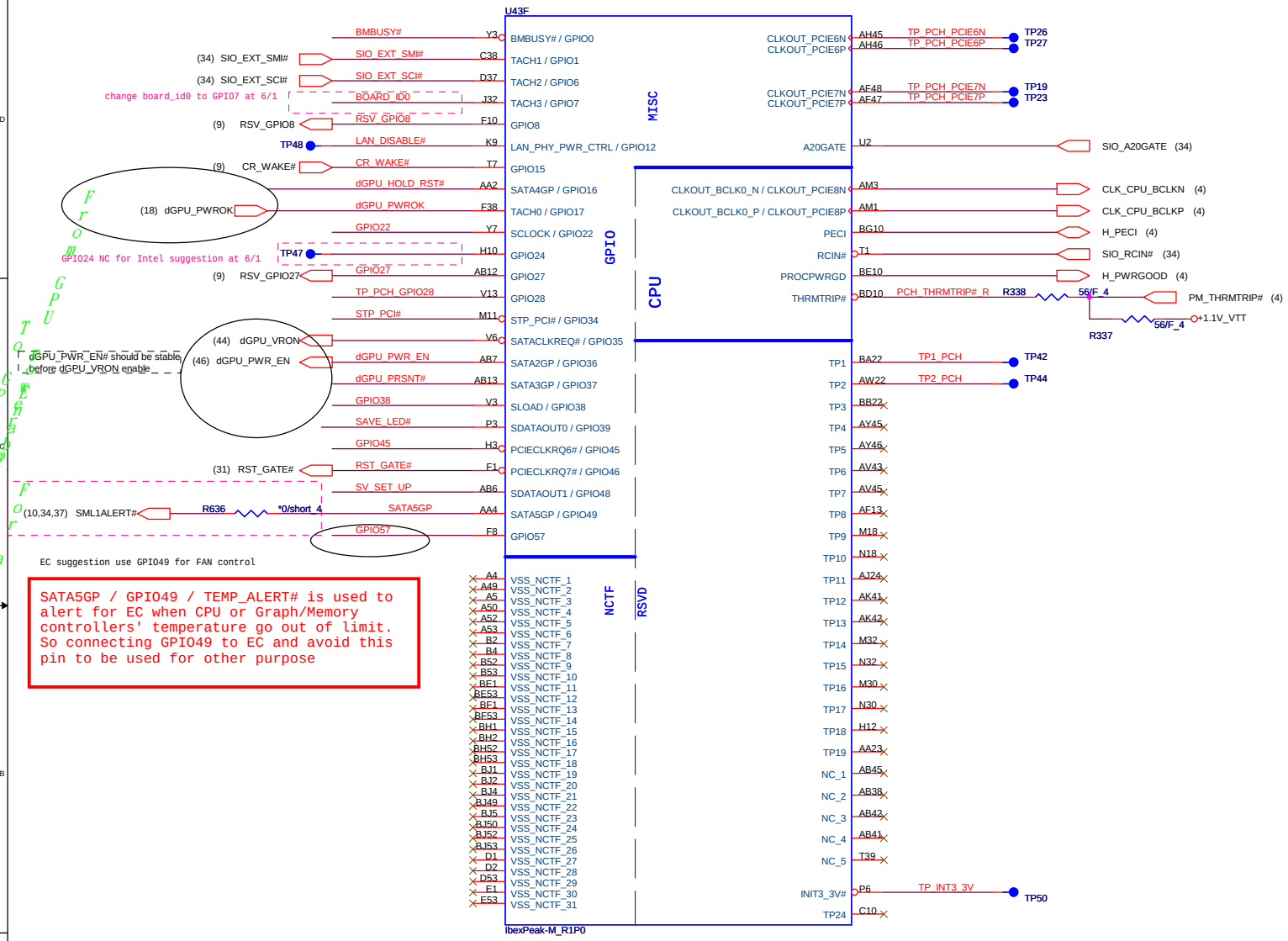
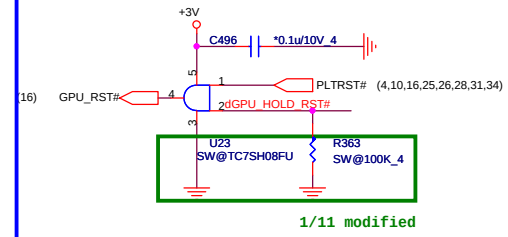
PCH4(CLG)

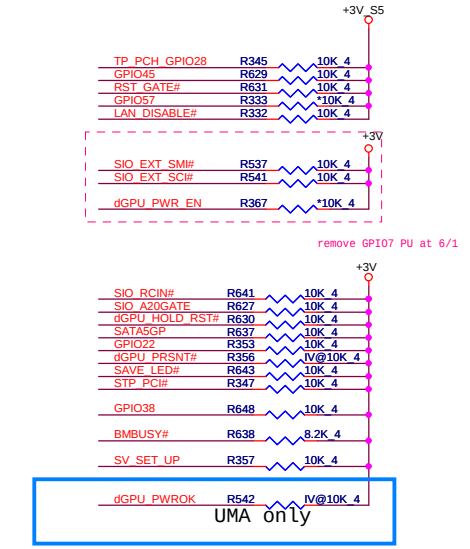
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



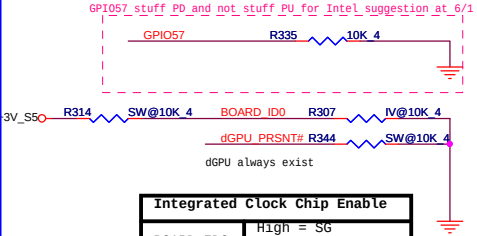
GPU RST#(CLG)



GPIO Pull-up/Pull-down(CLG)



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = SG Low = UMA
RSV_GPIO8	High = Disable Low = Enable

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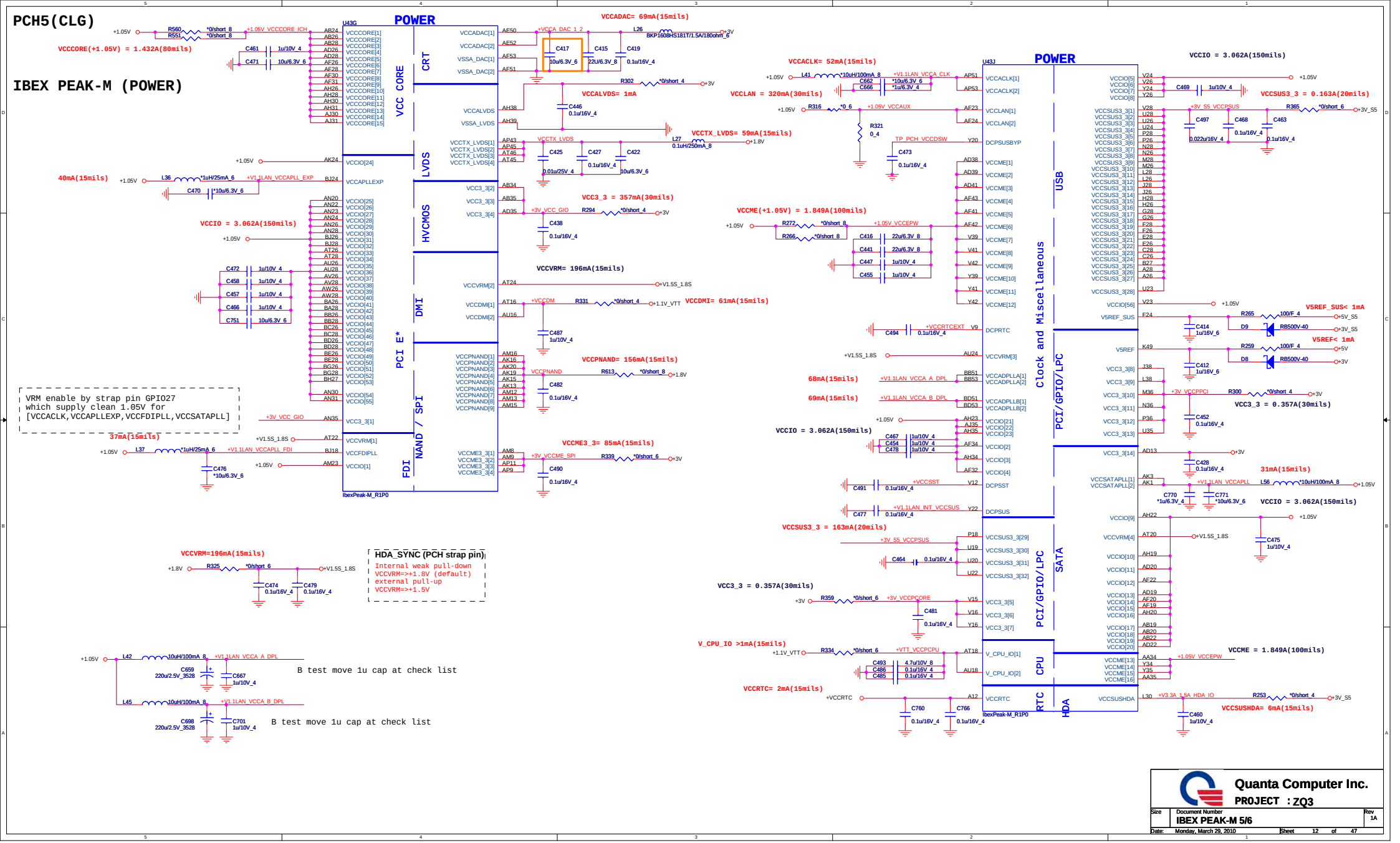
PCH5(CLG)

IBEX PEAK-M (POWER)



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IBEX PEAK-M (GND)

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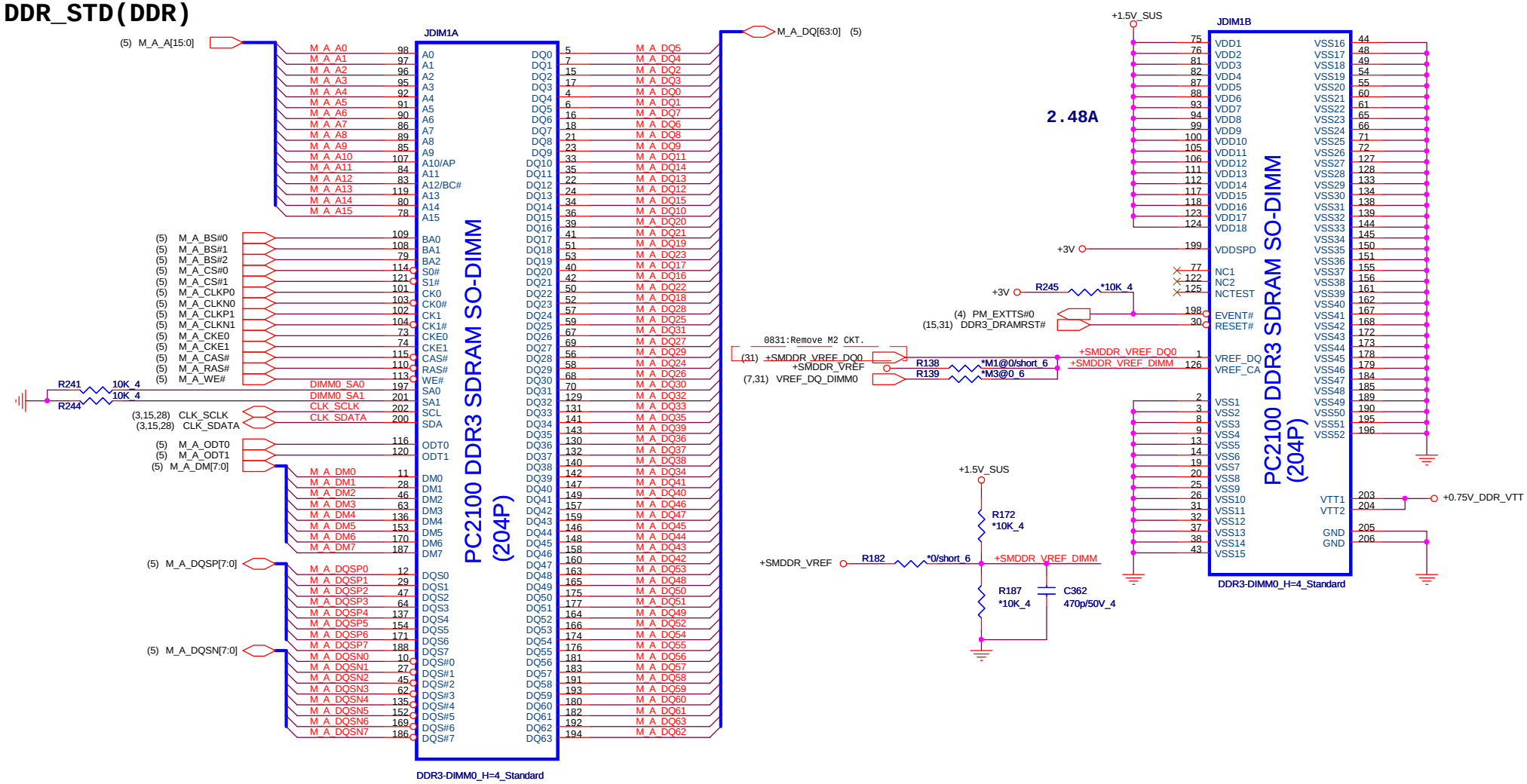
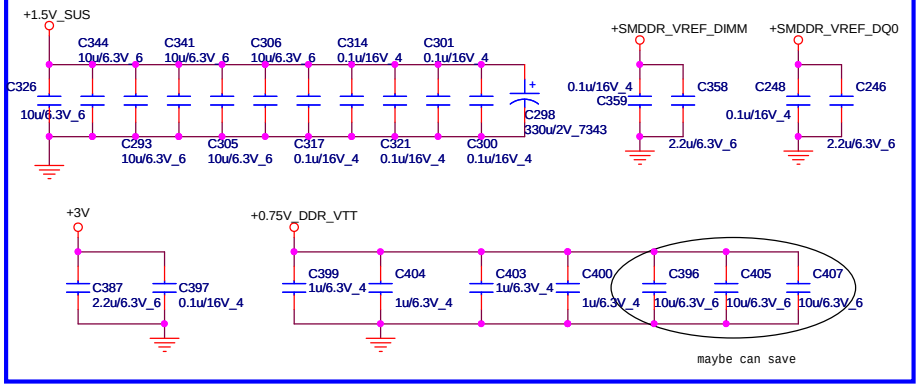
DDR_STD(DDR)



Place these Caps near So-Dimm0.



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	DDRIII SO-DIMM-0	1A
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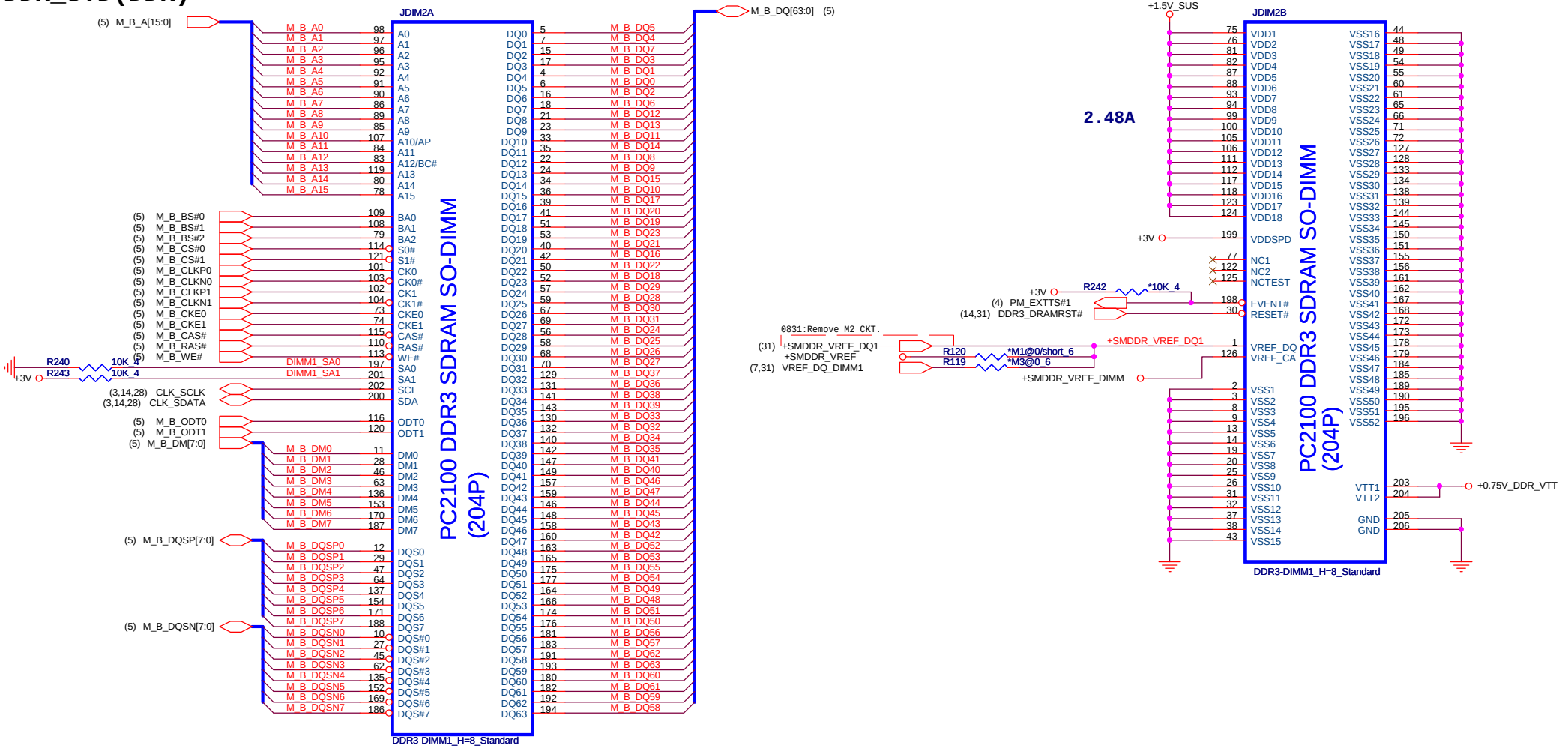
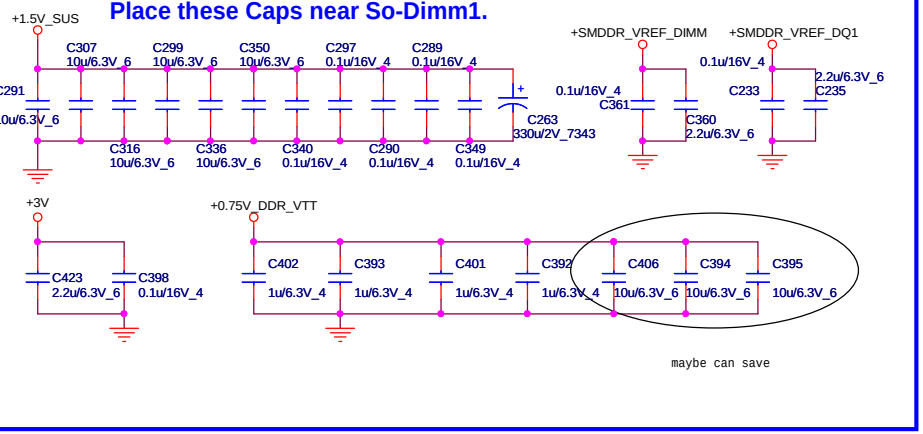
DDR_STD(DDR)





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	DDRIII SO-DIMM-1	1A
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GPU_1(VGA)

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

N11P GPU : AJ0N11P0T05

N11M GPU : AJ0N11M0T07

N11P_A2 GPU : AJ0N11P0T20

N11M_B1 GPU : AJ0N11M0T22

~ 500mA

1600mA

Near BGA

12~16 mils width 110mA

10/20 del C3553,C3554

12~16 mils width

10/20 Modify to 1uF

1211 for Nvidia request add transition cap

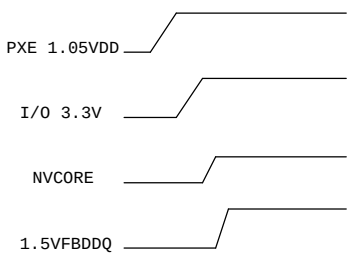
PCI EXPRESS

CSP@N11P-GE1-A3

R450 un-mount for switchable function

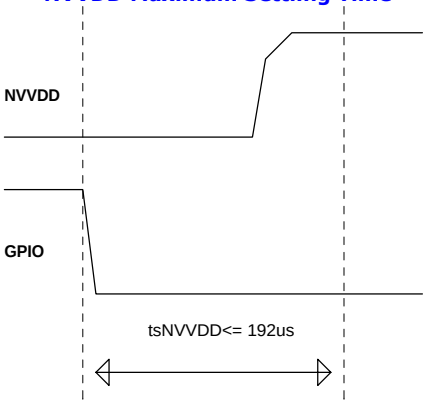
Only for Hybrid

power up sequence

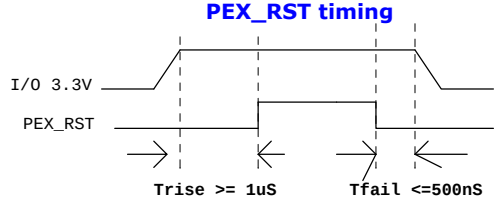


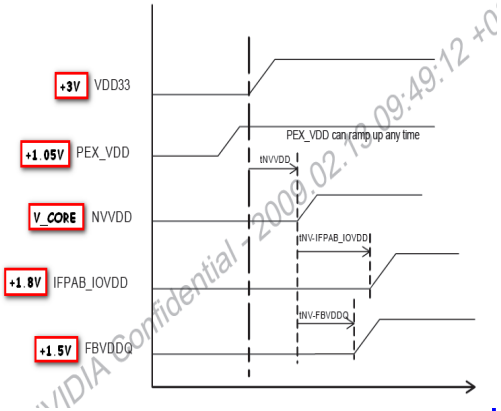
NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing





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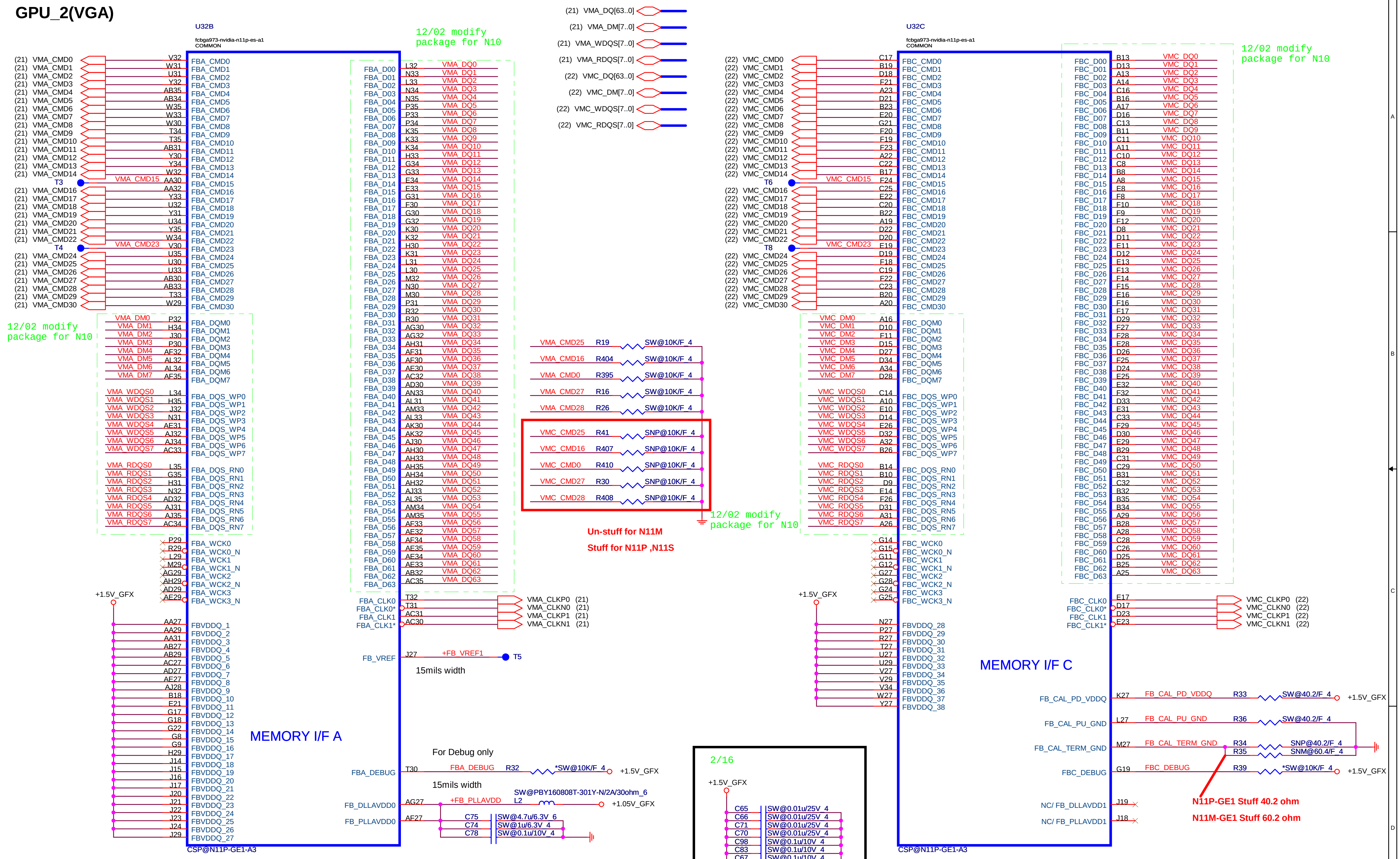
GPU_2(VGA)


U32B
fcbga973-nvidia-n11p-es-a1
COMMON
12/02 modify
package for N10
(21) VMA_CMD0 V32 FBA_CMD0
(21) VMA_CMD1 W31 FBA_CMD1
(21) VMA_CMD2 U31 FBA_CMD2
(21) VMA_CMD3 Y32 FBA_CMD3
(21) VMA_CMD4 AB35 FBA_CMD4
(21) VMA_CMD5 AB34 FBA_CMD5
(21) VMA_CMD6 W35 FBA_CMD6
(21) VMA_CMD7 W33 FBA_CMD7
(21) VMA_CMD8 W30 FBA_CMD8
(21) VMA_CMD9 T34 FBA_CMD9
(21) VMA_CMD10 T35 FBA_CMD10
(21) VMA_CMD11 AB31 FBA_CMD11
(21) VMA_CMD12 Y30 FBA_CMD12
(21) VMA_CMD13 Y34 FBA_CMD13
(21) VMA_CMD14 W32 FBA_CMD14
T3 VMA_CMD15 AA30 FBA_CMD15
(21) VMA_CMD16 AA32 FBA_CMD16
(21) VMA_CMD17 Y33 FBA_CMD17
(21) VMA_CMD18 U32 FBA_CMD18
(21) VMA_CMD19 Y31 FBA_CMD19
(21) VMA_CMD20 U34 FBA_CMD20
(21) VMA_CMD21 Y35 FBA_CMD21
(21) VMA_CMD22 W34 FBA_CMD22
T4 VMA_CMD23 V30 FBA_CMD23
(21) VMA_CMD24 U35 FBA_CMD24
(21) VMA_CMD25 U30 FBA_CMD25
(21) VMA_CMD26 U33 FBA_CMD26
(21) VMA_CMD27 AB30 FBA_CMD27
(21) VMA_CMD28 AB33 FBA_CMD28
(21) VMA_CMD29 T33 FBA_CMD29
(21) VMA_CMD30 W29 FBA_CMD30
VMA_DM0 P32 FBA_DQM0
VMA_DM1 H34 FBA_DQM1
VMA_DM2 J30 FBA_DQM2
VMA_DM3 P30 FBA_DQM3
VMA_DM4 AF32 FBA_DQM4
VMA_DM5 AL32 FBA_DQM5
VMA_DM6 AL34 FBA_DQM6
VMA_DM7 AF35 FBA_DQM7
VMA_WDQS0 L34 FBA_DQS_WP0
VMA_WDQS1 H35 FBA_DQS_WP1
VMA_WDQS2 J32 FBA_DQS_WP2
VMA_WDQS3 N31 FBA_DQS_WP3
VMA_WDQS4 AE31 FBA_DQS_WP4
VMA_WDQS5 AJ32 FBA_DQS_WP5
VMA_WDQS6 AJ34 FBA_DQS_WP6
VMA_WDQS7 AC33 FBA_DQS_WP7
VMA_RDQS0 L35 FBA_DQS_RN0
VMA_RDQS1 G35 FBA_DQS_RN1
VMA_RDQS2 H31 FBA_DQS_RN2
VMA_RDQS3 N32 FBA_DQS_RN3
VMA_RDQS4 AD32 FBA_DQS_RN4
VMA_RDQS5 AJ31 FBA_DQS_RN5
VMA_RDQS6 AJ35 FBA_DQS_RN6
VMA_RDQS7 AC34 FBA_DQS_RN7
P29 FBA_WCK0
R29 FBA_WCK0_N
L29 FBA_WCK1
M29 FBA_WCK1_N
AG29 FBA_WCK2
AH29 FBA_WCK2_N
AD29 FBA_WCK3
AE29 FBA_WCK3_N
+1.5V_GFX
AA27 FBVDDQ_1
AA29 FBVDDQ_2
AA31 FBVDDQ_3
AB27 FBVDDQ_4
AB29 FBVDDQ_5
AC27 FBVDDQ_6
AD27 FBVDDQ_7
AE27 FBVDDQ_8
AJ28 FBVDDQ_9
B18 FBVDDQ_10
E21 FBVDDQ_11
G17 FBVDDQ_12
G18 FBVDDQ_13
G22 FBVDDQ_14
G8 FBVDDQ_15
G9 FBVDDQ_16
H29 FBVDDQ_17
J14 FBVDDQ_18
J15 FBVDDQ_19
J16 FBVDDQ_20
J17 FBVDDQ_21
J20 FBVDDQ_22
J21 FBVDDQ_23
J22 FBVDDQ_24
J23 FBVDDQ_25
J24 FBVDDQ_26
J29 FBVDDQ_27
MEMORY I/F A
CSP@N11P-GE1-A3
FBA_D00 L32 VMA_DQ0
FBA_D01 N33 VMA_DQ1
FBA_D02 L33 VMA_DQ2
FBA_D03 N34 VMA_DQ3
FBA_D04 N35 VMA_DQ4
FBA_D05 P35 VMA_DQ5
FBA_D06 P33 VMA_DQ6
FBA_D07 P34 VMA_DQ7
FBA_D08 K35 VMA_DQ8
FBA_D09 K33 VMA_DQ9
FBA_D10 K34 VMA_DQ10
FBA_D11 H33 VMA_DQ11
FBA_D12 G34 VMA_DQ12
FBA_D13 G33 VMA_DQ13
FBA_D14 E34 VMA_DQ14
FBA_D15 E33 VMA_DQ15
FBA_D16 G31 VMA_DQ16
FBA_D17 F30 VMA_DQ17
FBA_D18 G30 VMA_DQ18
FBA_D19 G32 VMA_DQ19
FBA_D20 K30 VMA_DQ20
FBA_D21 K32 VMA_DQ21
FBA_D22 H30 VMA_DQ22
FBA_D23 K31 VMA_DQ23
FBA_D24 L31 VMA_DQ24
FBA_D25 L30 VMA_DQ25
FBA_D26 M32 VMA_DQ26
FBA_D27 N30 VMA_DQ27
FBA_D28 M30 VMA_DQ28
FBA_D29 P31 VMA_DQ29
FBA_D30 R32 VMA_DQ30
FBA_D31 R30 VMA_DQ31
FBA_D32 AG30 VMA_DQ32
FBA_D33 AG32 VMA_DQ33
FBA_D34 AH31 VMA_DQ34
FBA_D35 AF31 VMA_DQ35
FBA_D36 AF30 VMA_DQ36
FBA_D37 AE30 VMA_DQ37
FBA_D38 AC32 VMA_DQ38
FBA_D39 AD30 VMA_DQ39
FBA_D40 AN33 VMA_DQ40
FBA_D41 AL31 VMA_DQ41
FBA_D42 AM33 VMA_DQ42
FBA_D43 AL33 VMA_DQ43
FBA_D44 AK30 VMA_DQ44
FBA_D45 AK32 VMA_DQ45
FBA_D46 AJ30 VMA_DQ46
FBA_D47 AH30 VMA_DQ47
FBA_D48 AH33 VMA_DQ48
FBA_D49 AH35 VMA_DQ49
FBA_D50 AH34 VMA_DQ50
FBA_D51 AH32 VMA_DQ51
FBA_D52 AJ33 VMA_DQ52
FBA_D53 AL35 VMA_DQ53
FBA_D54 AM34 VMA_DQ54
FBA_D55 AM35 VMA_DQ55
FBA_D56 AF33 VMA_DQ56
FBA_D57 AE32 VMA_DQ57
FBA_D58 AF34 VMA_DQ58
FBA_D59 AE35 VMA_DQ59
FBA_D60 AE34 VMA_DQ60
FBA_D61 AE33 VMA_DQ61
FBA_D62 AB32 VMA_DQ62
FBA_D63 AC35 VMA_DQ63
FBA_CLK0 T32 VMA_CLKP0 (21)
FBA_CLK0* T31 VMA_CLKN0 (21)
FBA_CLK1 AC31 VMA_CLKP1 (21)
FBA_CLK1* AC30 VMA_CLKN1 (21)
FB_VREF J27 +FB_VREF1 T5
15mils width
For Debug only
FBA_DEBUG T30 FBA_DEBUG R32 *SW@10K/F_4 +1.5V_GFX
15mils width
FB_DLLAVDD0 AG27 +FB_PLLAVDD L2 SW@PBY160808T-301Y-N/2A/30ohm_6 +1.05V_GFX
FB_PLLAVDD0 AF27
C75 SW@4.7u/6.3V_6
C74 SW@1u/6.3V_4
C78 SW@0.1u/10V_4
(21) VMA_DQ[63..0]
(21) VMA_DM[7..0]
(21) VMA_WDQS[7..0]
(21) VMA_RDQS[7..0]
(22) VMC_DQ[63..0]
(22) VMC_DM[7..0]
(22) VMC_WDQS[7..0]
(22) VMC_RDQS[7..0]
VMA_CMD25 R19 SW@10K/F_4
VMA_CMD16 R404 SW@10K/F_4
VMA_CMD0 R395 SW@10K/F_4
VMA_CMD27 R16 SW@10K/F_4
VMA_CMD28 R26 SW@10K/F_4
VMC_CMD25 R41 SNP@10K/F_4
VMC_CMD16 R407 SNP@10K/F_4
VMC_CMD0 R410 SNP@10K/F_4
VMC_CMD27 R30 SNP@10K/F_4
VMC_CMD28 R408 SNP@10K/F_4
12/02 modify
package for N10
Un-stuff for N11M
Stuff for N11P ,N11S
2/16
+1.5V_GFX
C65 SW@0.01u/25V_4
C66 SW@0.01u/25V_4
C71 SW@0.01u/25V_4
C70 SW@0.01u/25V_4
C98 SW@0.1u/10V_4
C83 SW@0.1u/10V_4
C67 SW@0.1u/10V_4
C62 SW@0.047u/10V_4
C61 SW@0.047u/10V_4
C72 SW@0.047u/10V_4
C121 SW@4.7u/6.3V_6
C49 SW@4.7u/6.3V_6
All need stuff for N10P
U32C
fcbga973-nvidia-n11p-es-a1
COMMON
(22) VMC_CMD0 C17 FBC_CMD0
(22) VMC_CMD1 B19 FBC_CMD1
(22) VMC_CMD2 D18 FBC_CMD2
(22) VMC_CMD3 F21 FBC_CMD3
(22) VMC_CMD4 A23 FBC_CMD4
(22) VMC_CMD5 D21 FBC_CMD5
(22) VMC_CMD6 B23 FBC_CMD6
(22) VMC_CMD7 E20 FBC_CMD7
(22) VMC_CMD8 G21 FBC_CMD8
(22) VMC_CMD9 F20 FBC_CMD9
(22) VMC_CMD10 F19 FBC_CMD10
(22) VMC_CMD11 F23 FBC_CMD11
(22) VMC_CMD12 A22 FBC_CMD12
(22) VMC_CMD13 C22 FBC_CMD13
(22) VMC_CMD14 B17 FBC_CMD14
T6 VMC_CMD15 F24 FBC_CMD15
(22) VMC_CMD16 C25 FBC_CMD16
(22) VMC_CMD17 E22 FBC_CMD17
(22) VMC_CMD18 C20 FBC_CMD18
(22) VMC_CMD19 B22 FBC_CMD19
(22) VMC_CMD20 A19 FBC_CMD20
(22) VMC_CMD21 D22 FBC_CMD21
(22) VMC_CMD22 D20 FBC_CMD22
T8 VMC_CMD23 E19 FBC_CMD23
(22) VMC_CMD24 D19 FBC_CMD24
(22) VMC_CMD25 F18 FBC_CMD25
(22) VMC_CMD26 C19 FBC_CMD26
(22) VMC_CMD27 F22 FBC_CMD27
(22) VMC_CMD28 C23 FBC_CMD28
(22) VMC_CMD29 B20 FBC_CMD29
(22) VMC_CMD30 A20 FBC_CMD30
VMC_DM0 A16 FBC_DQM0
VMC_DM1 D10 FBC_DQM1
VMC_DM2 F11 FBC_DQM2
VMC_DM3 D15 FBC_DQM3
VMC_DM4 D27 FBC_DQM4
VMC_DM5 D34 FBC_DQM5
VMC_DM6 A34 FBC_DQM6
VMC_DM7 D28 FBC_DQM7
VMC_WDQS0 C14 FBC_DQS_WP0
VMC_WDQS1 A10 FBC_DQS_WP1
VMC_WDQS2 E10 FBC_DQS_WP2
VMC_WDQS3 D14 FBC_DQS_WP3
VMC_WDQS4 E26 FBC_DQS_WP4
VMC_WDQS5 D32 FBC_DQS_WP5
VMC_WDQS6 A32 FBC_DQS_WP6
VMC_WDQS7 B26 FBC_DQS_WP7
VMC_RDQS0 B14 FBC_DQS_RN0
VMC_RDQS1 B10 FBC_DQS_RN1
VMC_RDQS2 D9 FBC_DQS_RN2
VMC_RDQS3 E14 FBC_DQS_RN3
VMC_RDQS4 F26 FBC_DQS_RN4
VMC_RDQS5 D31 FBC_DQS_RN5
VMC_RDQS6 A31 FBC_DQS_RN6
VMC_RDQS7 A26 FBC_DQS_RN7
G14 FBC_WCK0
G15 FBC_WCK0_N
G11 FBC_WCK1
G12 FBC_WCK1_N
G27 FBC_WCK2
G28 FBC_WCK2_N
G24 FBC_WCK3
G25 FBC_WCK3_N
+1.5V_GFX
N27 FBVDDQ_28
P27 FBVDDQ_29
R27 FBVDDQ_30
T27 FBVDDQ_31
U27 FBVDDQ_32
U29 FBVDDQ_33
V27 FBVDDQ_34
V29 FBVDDQ_35
V34 FBVDDQ_36
W27 FBVDDQ_37
Y27 FBVDDQ_38
MEMORY I/F C
CSP@N11P-GE1-A3
12/02 modify
package for N10
FBC_D00 B13 VMC_DQ0
FBC_D01 D13 VMC_DQ1
FBC_D02 A13 VMC_DQ2
FBC_D03 A14 VMC_DQ3
FBC_D04 C16 VMC_DQ4
FBC_D05 B16 VMC_DQ5
FBC_D06 A17 VMC_DQ6
FBC_D07 D16 VMC_DQ7
FBC_D08 C13 VMC_DQ8
FBC_D09 B11 VMC_DQ9
FBC_D10 C11 VMC_DQ10
FBC_D11 A11 VMC_DQ11
FBC_D12 C10 VMC_DQ12
FBC_D13 C8 VMC_DQ13
FBC_D14 B8 VMC_DQ14
FBC_D15 A8 VMC_DQ15
FBC_D16 E8 VMC_DQ16
FBC_D17 F8 VMC_DQ17
FBC_D18 F10 VMC_DQ18
FBC_D19 F9 VMC_DQ19
FBC_D20 F12 VMC_DQ20
FBC_D21 D8 VMC_DQ21
FBC_D22 D11 VMC_DQ22
FBC_D23 E11 VMC_DQ23
FBC_D24 D12 VMC_DQ24
FBC_D25 E13 VMC_DQ25
FBC_D26 F13 VMC_DQ26
FBC_D27 F14 VMC_DQ27
FBC_D28 F15 VMC_DQ28
FBC_D29 E16 VMC_DQ29
FBC_D30 F16 VMC_DQ30
FBC_D31 F17 VMC_DQ31
FBC_D32 D29 VMC_DQ32
FBC_D33 F27 VMC_DQ33
FBC_D34 F28 VMC_DQ34
FBC_D35 E28 VMC_DQ35
FBC_D36 D26 VMC_DQ36
FBC_D37 F25 VMC_DQ37
FBC_D38 D24 VMC_DQ38
FBC_D39 E25 VMC_DQ39
FBC_D40 E32 VMC_DQ40
FBC_D41 F32 VMC_DQ41
FBC_D42 D33 VMC_DQ42
FBC_D43 E31 VMC_DQ43
FBC_D44 C33 VMC_DQ44
FBC_D45 F29 VMC_DQ45
FBC_D46 D30 VMC_DQ46
FBC_D47 E29 VMC_DQ47
FBC_D48 B29 VMC_DQ48
FBC_D49 C31 VMC_DQ49
FBC_D50 C29 VMC_DQ50
FBC_D51 B31 VMC_DQ51
FBC_D52 C32 VMC_DQ52
FBC_D53 B32 VMC_DQ53
FBC_D54 B35 VMC_DQ54
FBC_D55 B34 VMC_DQ55
FBC_D56 A29 VMC_DQ56
FBC_D57 B28 VMC_DQ57
FBC_D58 A28 VMC_DQ58
FBC_D59 C28 VMC_DQ59
FBC_D60 C26 VMC_DQ60
FBC_D61 D25 VMC_DQ61
FBC_D62 B25 VMC_DQ62
FBC_D63 A25 VMC_DQ63
FBC_CLK0 E17 VMC_CLKP0 (22)
FBC_CLK0* D17 VMC_CLKN0 (22)
FBC_CLK1 D23 VMC_CLKP1 (22)
FBC_CLK1* E23 VMC_CLKN1 (22)
FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R33 SW@40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND L27 FB_CAL_PU_GND R36 SW@40.2/F_4
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R34 SNP@40.2/F_4
R35 SNM@60.4/F_4
FBC_DEBUG G19 FBC_DEBUG R39 *SW@10K/F_4 +1.5V_GFX
NC/ FB_DLLAVDD1 J19
NC/ FB_PLLAVDD1 J18
N11P-GE1 Stuff 40.2 ohm
N11M-GE1 Stuff 60.2 ohm

Quanta Computer Inc.

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	N11P-GE (MEMORY I/F) 2/5	1A

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GPU_3(VGA)

U32D COMMON — fcbga973-nvidia-n11p-es-a1

IFPAB(LVDS)

+1.05V_GFX — SW@FBMA-10-160808-300T/300mA/30ohm_6 L8 — +IFPAB_PLLVDD — 220 mA — AK9 IFPAB_PLLVDD
C173 SW@1u/6.3V_4
C179 SW@4.7u/6.3V_6
10/20 Del C3647

R49 *SW@1K/F_4 IFPAB_RSET — AJ11 IFPAB_RSET

+1.8V_GFX — SW@FBMA-10-160808-300T/300mA/30ohm_6 L17 — +IFPAB_IOVDD — 200 mA — AG9 IFPA_IOVDD, AG10 IFPB_IOVDD
C165 SW@0.1u/10V_4
C216 SW@0.1u/10V_4
C217 SW@1u/6.3V_4
C219 SW@4.7u/6.3V_6

IFPA_TXC	AM11	EV_TXLCLKOUTP (23)
IFPA_TXC*	AM12	EV_TXLCLKOUTN (23)
IFPA_TXD0	AM8	EV_TXLOUTP0 (23)
IFPA_TXD0*	AL8	EV_TXLOUTN0 (23)
IFPA_TXD1	AM10	EV_TXLOUTP1 (23)
IFPA_TXD1*	AM9	EV_TXLOUTN1 (23)
IFPA_TXD2	AK10	EV_TXLOUTP2 (23)
IFPA_TXD2*	AL10	EV_TXLOUTN2 (23)
IFPA_TXD3	AK11	
IFPA_TXD3*	AL11	
IFPB_TXC	AP13	
IFPB_TXC*	AN13	
IFPB_TXD4	AN8	
IFPB_TXD4*	AP8	
IFPB_TXD5	AP10	
IFPB_TXD5*	AN10	
IFPB_TXD6	AR11	
IFPB_TXD6*	AR10	
IFPB_TXD7	AN11	
IFPB_TXD7*	AP11	

LVDS clk spread : Center
+/-0.5% (30~33KHZ)

IFPC / IFPD / IFPCD

R59 SW@10K/F_4 +IFPCD_PLLVDD — 220 mA — AJ9 IFPCD_PLLVDD/ IFPC_PLLVDD, AC6 DACB_VDD/ IFPD_PLLVDD

R58 *SW@1K/F_4 IFPC_RSET — AK7 IFPCD_RSET/ IFPC_RSET
R61 *SW@1K/F_4 IFPD_RSET — AB6 DACB_RSET/ IFPD_RSET

R51 SW@10K/F_4 +IFPCD_IOVDD — 285 mA — AJ8 IFPC_IOVDD, AK8 IFPD_IOVDD

I2CW_SDA/ IFPC_AUX_N	AN3	
I2CW_SCL/ IFPC_AUX	AP2	
IFPC_L3_N	AR2	
IFPC_L3	AP1	
IFPC_L2_N	AM4	
IFPC_L2	AM3	
IFPC_L1_N	AM5	
IFPC_L1	AL5	
IFPC_L0_N	AM6	
IFPC_L0	AM7	
I2CX_SDA/ IFPD_AUX_N	AN4	
I2CX_SCL/ IFPD_AUX	AP4	
IFPD_L3_N	AR4	
IFPD_L3	AR5	
IFPD_L2_N	AP5	
IFPD_L2	AN5	
IFPD_L1_N	AN7	
IFPD_L1	AP7	
IFPD_L0_N	AR7	
IFPD_L0	AR8	

TMDS channel two

IFPEF

R424 SW@1K/F_4 IFPE_RSET — AL1 IFPEF_RSET

C188 SW@0.1u/10V_4
C200 SW@1u/6.3V_4
C214 SW@0.1u/10V_4
C215 SW@0.1u/10V_4
C218 SW@4.7u/6.3V_6

SW@FBMA-10-160808-300T/300mA/30ohm_6
+3V_GFX — L16 — IFPEF_PLLVDD — AJ6 IFPEF_PLLVDD
(1.05V +/- 3%) +1.05V_GFX — L15 — IFPEF_IOVDD — AE7 IFPE_IOVDD, AD7 IFPF_IOVDD
SW@MLB-201209-0030P-N1-RU/6A/30ohm_8

C197 SW@0.1u/10V_4
C206 SW@0.1u/10V_4
C202 SW@1u/6.3V_4
C212 SW@4.7u/6.3V_6

SW@PBY160808T-301Y-N/2A/30ohm_6
+3V_GFX — L7
C157 SW@0.1u/10V_4
C163 SW@0.1u/10V_4
C146 SW@0.1u/10V_4

I2CY_SCL/ IFPE_AUX	AE4	MXM_DDCCK_C → MXM_DDCCK_C (24)
I2CY_SDA/ IFPE_AUX*	AD4	MXM_DDCDAT_C → MXM_DDCDAT_C (24)
IFPE_L0	AH6	HDMITXP2 (24)
IFPE_L0*	AH5	HDMITXN2 (24)
IFPE_L1	AH4	HDMITXP1 (24)
IFPE_L1*	AG4	HDMITXN1 (24)
IFPE_L2	AF4	HDMITXP0 (24)
IFPE_L2*	AF5	HDMITXN0 (24)
IFPE_L3	AE6	HDMICLKP (24)
IFPE_L3*	AE5	HDMICLKN (24)
I2CZ_SCL/ IFPF_AUX	AF3	
I2CZ_SDA/ IFPF_AUX*	AF2	
IFPF_L0	AL2	
IFPF_L0*	AL3	
IFPF_L1	AJ3	
IFPF_L1*	AJ2	
IFPF_L2	AJ1	
IFPF_L2*	AH1	
IFPF_L3	AH2	
IFPF_L3*	AH3	

DVI

Display port output

DACA(CRT)

+DACA_VDD — 120 mA — AJ12 DACA_VDD
C167 SW@1u/6.3V_4
C172 SW@4.7u/6.3V_6
C175 SW@4700p/25V_4
C154 SW@470p/50V_4

C144 SW@0.1u/10V_4 DACA_VREF — AK12
R45 SW@124/F_4 DACA_RSET — AK13 DACA_VREF, DACA_RSET

DACA_RED	AM15	EV_CRT_RED → EV_CRT_RED (23)
DACA_GREEN	AM14	EV_CRT_GRE → EV_CRT_GRE (23)
DACA_BLUE	AL14	EV_CRT_BLU → EV_CRT_BLU (23)
DACA_HSYNC	AM13	EV_HSYNC_R — R63 SW@33_4 — EV_HSYNC (23)
DACA_VSYNC	AL13	EV_VSYNC_R — R57 SW@33_4 — EV_VSYNC (23)
I2CA_SCL	G1	EV_CRTDCLK → EV_CRTDCLK (23)
I2CA_SDA	G4	EV_CRTDDAT → EV_CRTDDAT (23)

DACC(CRT2)

R62 SW@10K/F_4 +DACB_VDD — AG7 DACC_VDD/ DACB_VDD
AK6 DACC_VREF/ DACB_VREF
AH7 DACC_RSET/ DACB_RSET

/DACC_RED DACB_RED	AK4	
/DACC_GREEN DACB_GREEN	AL4	
/DACC_BLUE DACB_BLUE	AJ4	
DACB_HSYNC/ DACC_HSYNC	AM1	
DACB_VSYNC/ DACC_VSYNC	AM2	
I2CB_SCL	G3	I2CB_SCL — R79 SW@2.2K_4 — +3V_GFX
I2CB_SDA	G2	I2CB_SDA — R93 SW@2.2K_4 — +3V_GFX

PLACE CLOSE TO GPU

DACB(TV)

AC5 DACB_VREF/ NC

NC/ DACB_RED	AA4	
NC/ DACB_GREEN	AB4	
NC/ DACB_BLUE	Y4	
CEC/ DACB_CSYNC	AB5	DACB_CSYNC — R67 SW@10K/F_4

XTAL_PLL

+1.05V_GFX — SW@100nH/400mA_6 L14 — +NV_PLLVDD — 60mA — AF9 PLLVDD, AD9 VID_PLLVDD
C171 SW@0.1u/10V_4
C180 SW@0.1u/10V_4
C189 SW@1u/6.3V_4
C199 SW@4.7u/6.3V_6

+1.05V_GFX — SW@100nH/400mA_6 L13 — +NV_SPPLLVDD — 45mA — AF9 SP_PLLVDD
C195 SW@1u/6.3V_4
C198 SW@4.7u/6.3V_6
10/20 Del C3515

CSP@N11P-GE1-A3

XTAL_SSIN	D2	XTAL_SSIN
XTAL_OUTBUFF	D1	BXTALOUT
XTAL_IN	B1	XTALI_27M
XTAL_OUT	B2	XTALO_27M — 2 — Y2 — 1

C566 SW@18p/50V_4 — Y2 SW@27MHZ — C564 SW@18p/50V_4

2/5 modified

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

GPU all PWROK

10/20
+3V_GFX
+3V_S5
R109 SW@10K_4
R108 SW@10K_4
dGPU_PWROK (11)
Q4 SW@2N7002D
+1.8V_GFX
Q3 SW@PDTC143TT

10/20 STUFF

+3V_GFX
R80 SW@4.7K_4 EV_CRTDCLK
R81 SW@4.7K_4 EV_CRTDDAT
R425 SW@4.7K_4 MXM_DDCCK_C
R426 SW@4.7K_4 MXM_DDCDAT_C

EV_CRT_RED R50 SW@150/F_4
EV_CRT_GRE R54 SW@150/F_4
EV_CRT_BLU R47 SW@150/F_4

XTAL_SSIN R420 SW@10K/F_4
BXTALOUT R433 SW@10K/F_4

10 kΩ pull-down only if no spread chip used.

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PIN STRAPS(VGA)

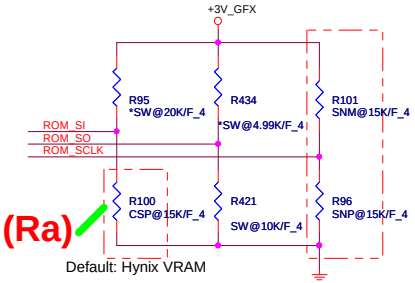
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

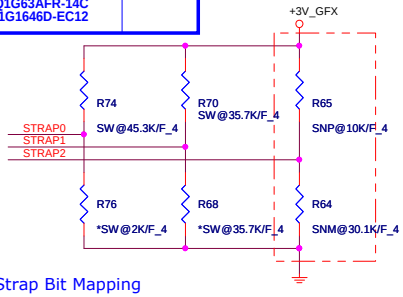
AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502



(Ra)

Default: Hynix VRAM

Hynix =15K pull down(64Mx16)
Samsung =20k pull down(64Mx16)

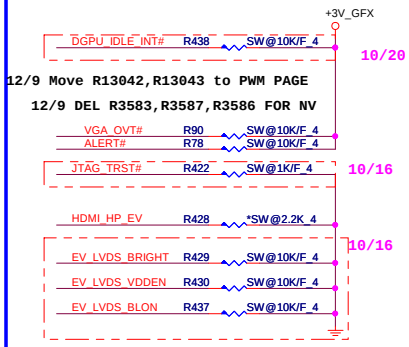


CHIP	ROM_SCLK	STRAP2	PCI_DEVID
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PD 15K	PU 10K	0x0A29

Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

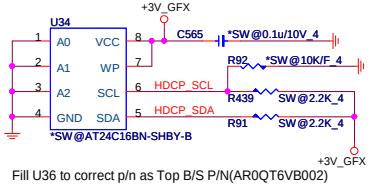
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDCP ROM (VGA)

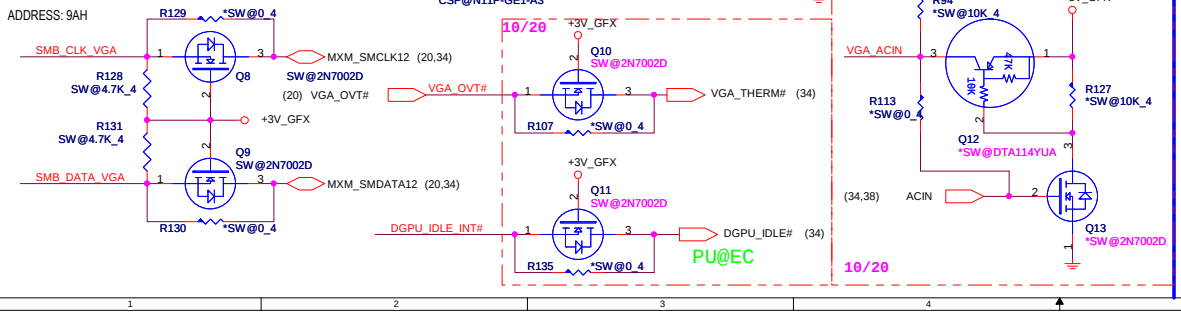


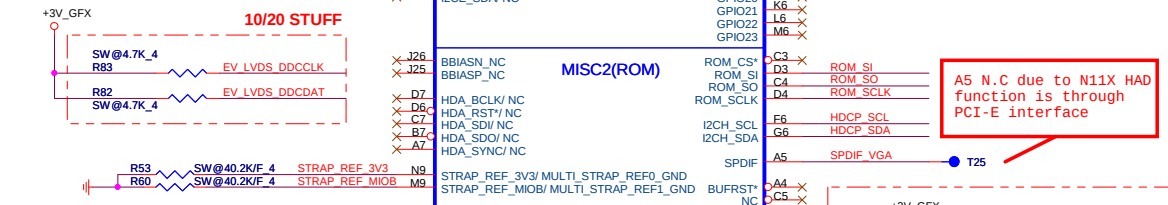
Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

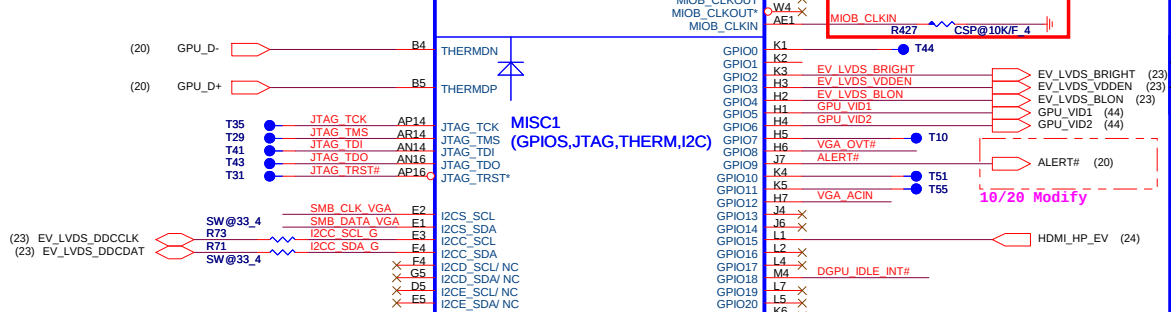
DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

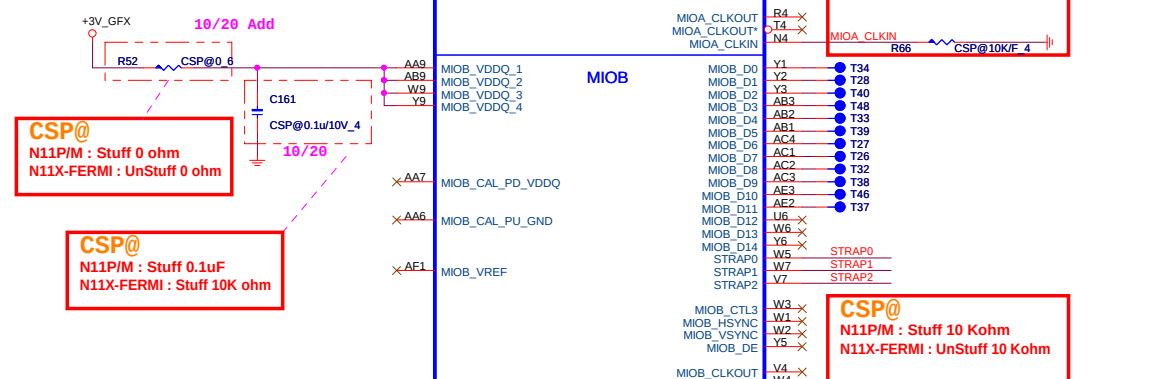
HDCP ROM reserve , Due to N11x had support internal HDCP function.

VGA Thermal(VGA)









GPU_4(VGA)

U32F

+VGPU_CORE

fcbga973-nvidia-n11p-es-a1

COMMON

+VGPU_CORE

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

CSP@N11P-GE1-A3

U32G

fcbga973-nvidia-n11p-es-a1

COMMON

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

CSP@N11P-GE1-A3

NVVDD Decoupling

+VGPU_CORE

2/16

PLACE UNDER BALLS

C133	SW@0.01u/25V_4
C90	SW@0.01u/25V_4
C116	SW@0.01u/25V_4
C115	SW@0.01u/25V_4
C134	SW@0.01u/25V_4
C151	SW@0.01u/25V_4
C91	SW@0.022u/16V_4
C105	SW@0.022u/16V_4
C122	SW@0.022u/16V_4
C152	SW@0.022u/16V_4
C92	SW@0.047u/25V_4
C117	SW@0.047u/25V_4
C135	SW@0.047u/25V_4
C106	SW@0.22u/6.3V_4
C150	SW@0.22u/6.3V_4
C104	SW@1u/6.3V_4
C96	SW@4700p/25V_4
C86	SW@4700p/25V_4

PLACE NEAR BALLS

C93	SW@4.7u/6.3V_6
C82	SW@10u/6.3V_8
C80	SW@10u/6.3V_8
C126	SW@150u/6.3V_3528
C778*	SW@150u/6.3V_3528

1/27 modified
(change to 3258)

12/9 ADD TWO 4700PF

Thermal Sensor(VGA)

+3V_GFX

R88 *SW@10K_4

(19,34) MXM_SMCLK12

Q5 *SW@2N7002D

1/12 modified

+3V_GFX

*SW@10K_4 R89

(19,34) MXM_SMDATA12

Q6 *SW@2N7002D

GPU_SMCLK

GPU_SMDATA

(19) ALERT#

(19) VGA_OVT#

10/20 Modify

U8

SCLK	8	VCC	1
SDA	7	DXP	2
ALERT#	6	DXN	3
OVERT#	4	GND	5

*SW@G780-1P81U(MSOP)

ADDRESS: 9AH

+3V_GFX

*SW@0.1u/10V_4 C229

C196 *SW@2200p/50V_4

GPU_D+ (19)

GPU_D- (19)

NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

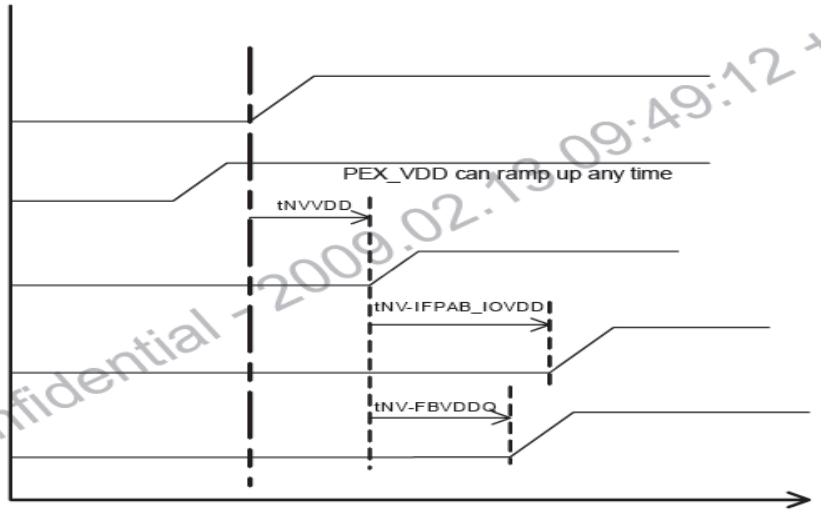
+3V VDD33

+1.05V PEX_VDD

V_CORE NVVDD

+1.8V IFPAB_IOVDD

+1.5V FBVDDQ



Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE (POWER & GND&THM) 5/5	1A

Date: Monday, March 29, 2010 Sheet 20 of 47

VRAM_A(VGA)

CHANNEL A: 256MB/512MB DDR3

(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]

(17,22,46) +1.5V_GFX

U4 / U30 / U29 / U3 — 96-BALL SDRAM DDR3 — CSP@VRAM _DDR3

Should be 240 Ohms +-1%

R24 SW@243/F_4
R394 SW@243/F_4
R403 SW@243/F_4
R17 SW@243/F_4

VMA_ZQ1
VMA_ZQ2
VMA_ZQ3
VMA_ZQ4

Samsung 1Gb : AKD5LGGT506
Hynix 1Gb : AKD5LZGTW04

R398 SW@243/F_4 (VMA_CLKP0 / VMA_CLKN0)
R21 SW@243/F_4 (VMA_CLKP1 / VMA_CLKN1)

R397 SW@1.33K/F_4
R23 SW@1.33K/F_4
R22 SW@1.33K/F_4
R396 SW@1.33K/F_4

R393 SW@1.33K/F_4 — C526 SW@0.1u/10V_4
R20 SW@1.33K/F_4 — C29 SW@0.1u/10V_4
R18 SW@1.33K/F_4 — C20 SW@0.1u/10V_4
R392 SW@1.33K/F_4 — C516 SW@0.1u/10V_4

12/9 NV recommend 0.1uf x 5, 1uf x 4 per DDR3

DEL C3627,C3684,C3681,C3662 ,C3678,C3692
C3690,C3695,C3685 FOR NV suggestion

10/21 Add for NV Request

+1.5V_GFX
C514 SW@4.7u/6.3V_6
C26 SW@0.1u/10V_4
C519 SW@0.1u/10V_4
C545 SW@0.1u/10V_4
C28 SW@0.1u/10V_4

+1.5V_GFX
C520 SW@0.1u/10V_4
C521 SW@0.1u/10V_4
C548 SW@0.1u/10V_4
C517 SW@0.1u/10V_4
C549 SW@0.1u/10V_4
C546 SW@0.1u/10V_4
C37 SW@0.1u/10V_4
C527 SW@0.1u/10V_4

+1.5V_GFX
C515 SW@0.1u/10V_4
C518 SW@0.1u/10V_4
C550 SW@0.1u/10V_4
C523 SW@0.1u/10V_4
C25 SW@0.1u/10V_4
C40 SW@0.1u/10V_4
C35 SW@0.1u/10V_4
C522 SW@0.1u/10V_4

10/21 Add for NV Request

+1.5V_GFX
C24 SW@1u/6.3V_4
C31 SW@1u/6.3V_4
C38 SW@1u/6.3V_4
C27 SW@1u/6.3V_4
C19 SW@1u/6.3V_4
C39 SW@1u/6.3V_4
C547 SW@1u/6.3V_4
C17 SW@1u/6.3V_4

10/21 Add for NV Request

+1.5V_GFX
C524 SW@1u/6.3V_4
C16 SW@1u/6.3V_4
C18 SW@1u/6.3V_4
C77 SW@1u/6.3V_4
C22 SW@1u/6.3V_4
C41 SW@1u/6.3V_4
C23 SW@1u/6.3V_4
C21 SW@1u/6.3V_4

Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE VRAM-1(DDR3 BGA96)	1A
Date: Monday, March 29, 2010	Sheet 21 of 47	

VRAM_C(VGA)

CHANNEL B: 256MB/512MB DDR3

(17) VMC_DQ[63..0]
(17) VMC_DM[7..0]
(17) VMC_WDQS[7..0]
(17) VMC_RDQS[7..0]

(17,21,46) +1.5V_GFX

U33 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

U7 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

U5 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

U31 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

Should be 240 Ohms +-1%

R413 SNP@243/F_4
R48 SNP@243/F_4
R37 SNP@243/F_4
R409 SNP@243/F_4

R414 SNP@243/F_4
R411 SNP@1.33K/F_4
R412 SNP@1.33K/F_4
C558 SNP@0.1u/10V_4
R42 SNP@1.33K/F_4
R46 SNP@1.33K/F_4
C153 SNP@0.1u/10V_4
R31 SNP@243/F_4
R405 SNP@1.33K/F_4
R406 SNP@1.33K/F_4
C555 SNP@0.1u/10V_4
R27 SNP@1.33K/F_4
R29 SNP@1.33K/F_4
C45 SNP@0.1u/10V_4

12/9 NV recommend 0.1uf x 5, 1uf x 4 per DDR3
DEL C3585,C3637,C3653,C3655,C3665 FOR NV recommend

10/21 Add for NV Request

C537	SNP@4.7u/6.3V_6
C32	SNP@0.1u/10V_4
C46	SNP@0.1u/10V_4
C557	SNP@0.1u/10V_4
C554	SNP@0.1u/10V_4

C544	SNP@0.1u/10V_4
C561	SNP@0.1u/10V_4
C541	SNP@0.1u/10V_4
C36	SNP@0.1u/10V_4
C553	SNP@0.1u/10V_4
C540	SNP@0.1u/10V_4
C107	SNP@0.1u/10V_4
C140	SNP@0.1u/10V_4

C543	SNP@0.1u/10V_4
C132	SNP@0.1u/10V_4
C169	SNP@0.1u/10V_4
C556	SNP@0.1u/10V_4
C34	SNP@0.1u/10V_4
C539	SNP@0.1u/10V_4
C542	SNP@0.1u/10V_4
C538	SNP@0.1u/10V_4

C69	SNP@1u/6.3V_4
C158	SNP@1u/6.3V_4
C51	SNP@1u/6.3V_4
C525	SNP@1u/6.3V_4
C166	SNP@1u/6.3V_4
C164	SNP@1u/6.3V_4
C128	SNP@1u/6.3V_4
C33	SNP@1u/6.3V_4

C552	SNP@1u/6.3V_4
C97	SNP@1u/6.3V_4
C42	SNP@1u/6.3V_4
C63	SNP@1u/6.3V_4
C551	SNP@1u/6.3V_4
C30	SNP@1u/6.3V_4
C60	SNP@1u/6.3V_4
C112	SNP@1u/6.3V_4

Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE VRAM-2(DDR3 BGA96)	1A
Date: Monday, March 29, 2010	Sheet 22 of 47	

CRT Switch(CRT)

IV@

SW@

S	Yn
0	EV
1	IV

dGPU_SELECT# dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT

U12 SW@SN74CBT3257CPWR

U10 SW@SN74CBT3257CPWR

3.3V or 5V level?

U9 SW@SN74CBT3257CPWR

10/20 Del

10/20 Modify

10/16

1/22 add for EMI

UMA only

CRT SWITCH (DOK)

U35 SN74CBT3257CPWR

(CRT)

1/27 change R443 to fuse

2/03 modify footprint

CM2009-02QR

LVDS Switch (LDS)

U13 SW@TS3DV421DGVR

S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

10/16

UMA only

For EMI (12/22)

LVDS

0.8A

1/22 add for EMI

LCD Power(LDS)

10/20 Modify

AAT4280-4

10/16

Backlight Control (LDS)

10/20 Modify

LID591#,EC intrnal PU

10/16

CAMERA Module(CCD)

CCD&MIC CONN

EMI addition

For EMI. (3/26)

10/18

1/22 add for EMI

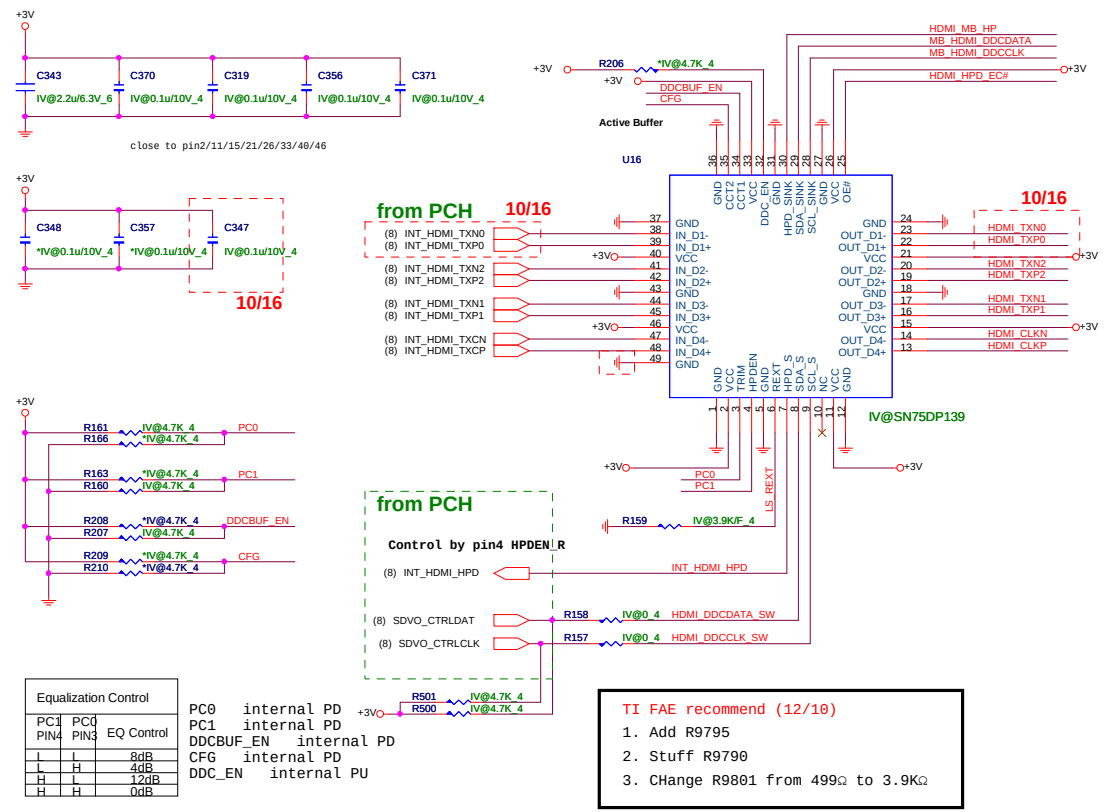
Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

Date: Monday, March 29, 2010 Sheet 23 of 47

I@ HDMI LEVEL SHIFTER(DOK)

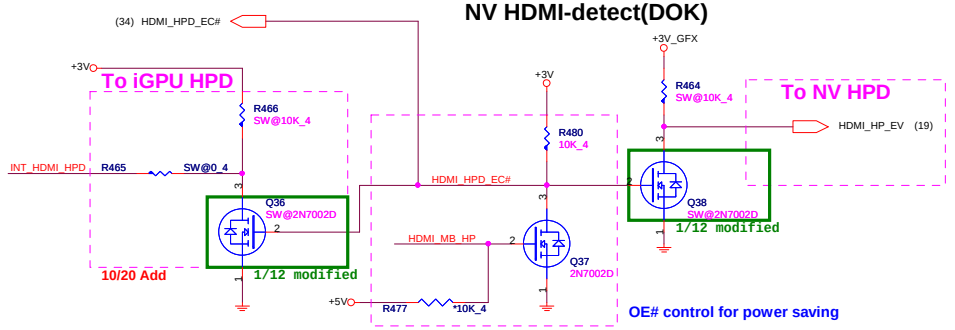


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

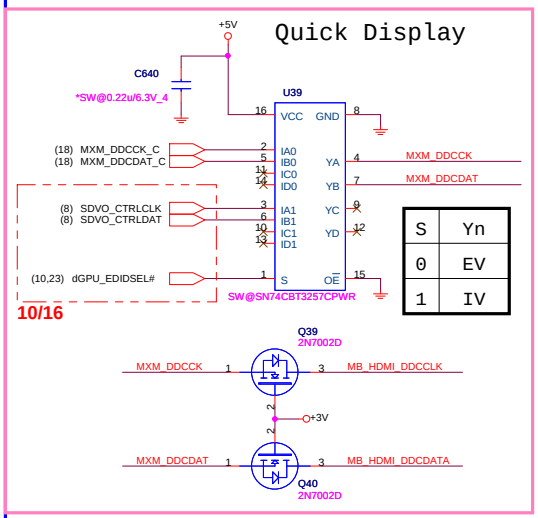
PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

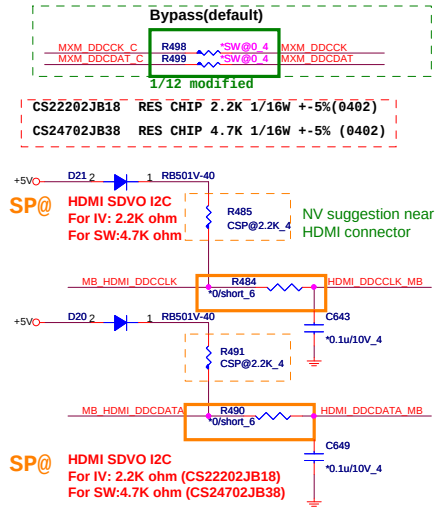
TI FAE recommend (12/10)
1. Add R9795
2. Stuff R9790
3. CHange R9801 from 499Ω to 3.9KΩ

NV HDMI-detect(DOK)

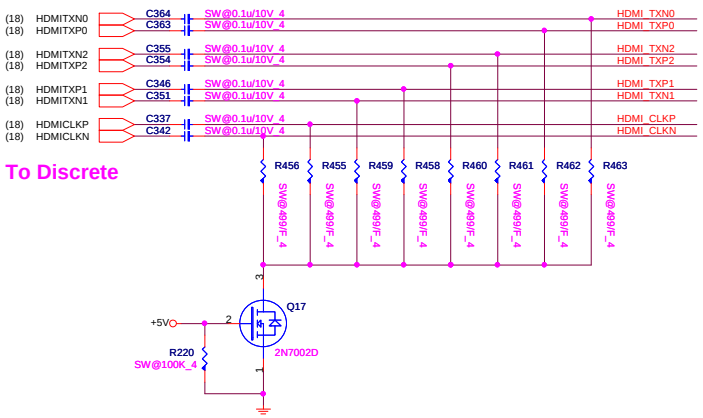


SDVO I2C Control(DOK)

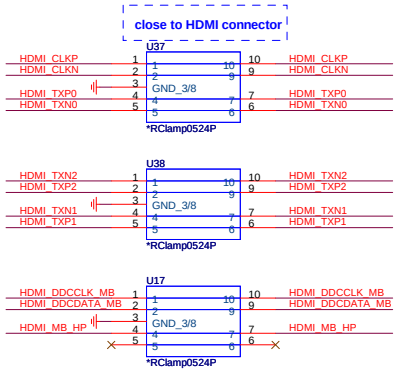


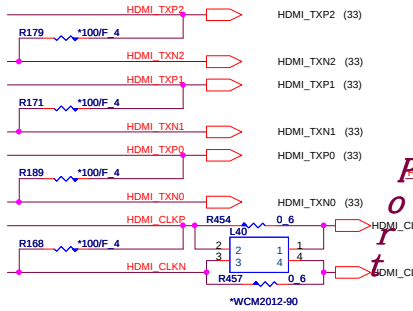


Switchable Graphic HDMI source(DOK)



ESD Protect(DOK)





Replicat

Quanta Computer Inc.			
PROJECT : ZQ3			
Size	Document Number		Rev
	DVI (PS8101)		1A
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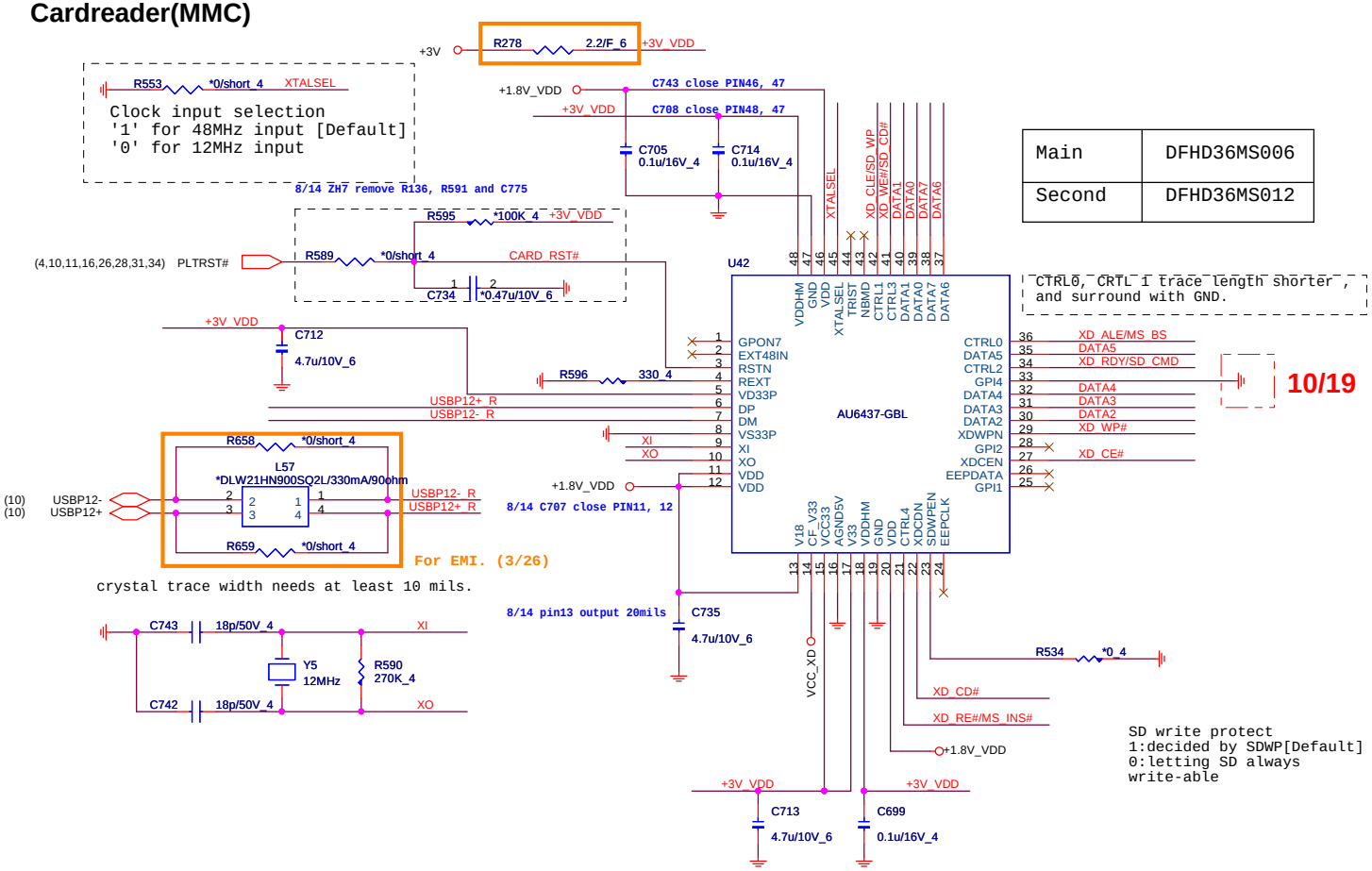
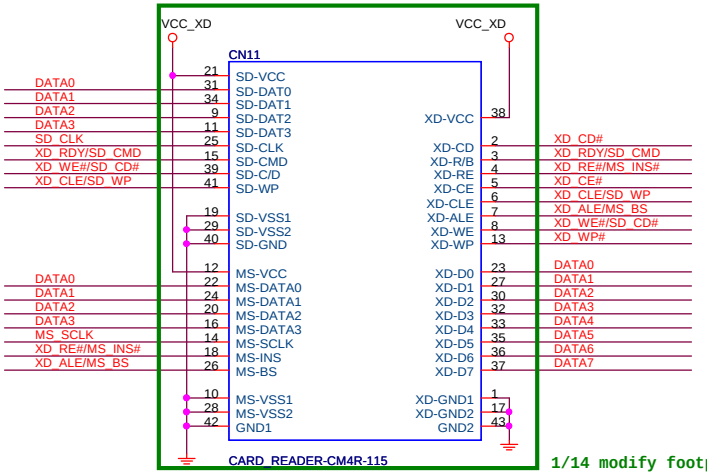
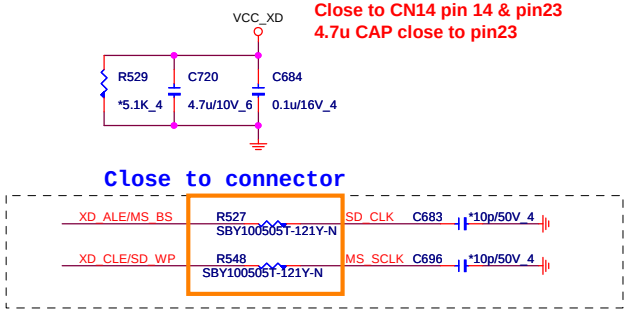
Cardreader(MMC)



Main	DFHD36MS006
Second	DFHD36MS012

4 IN 1 CARD READER (MMC)





Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	AU6437 CardReader	1A

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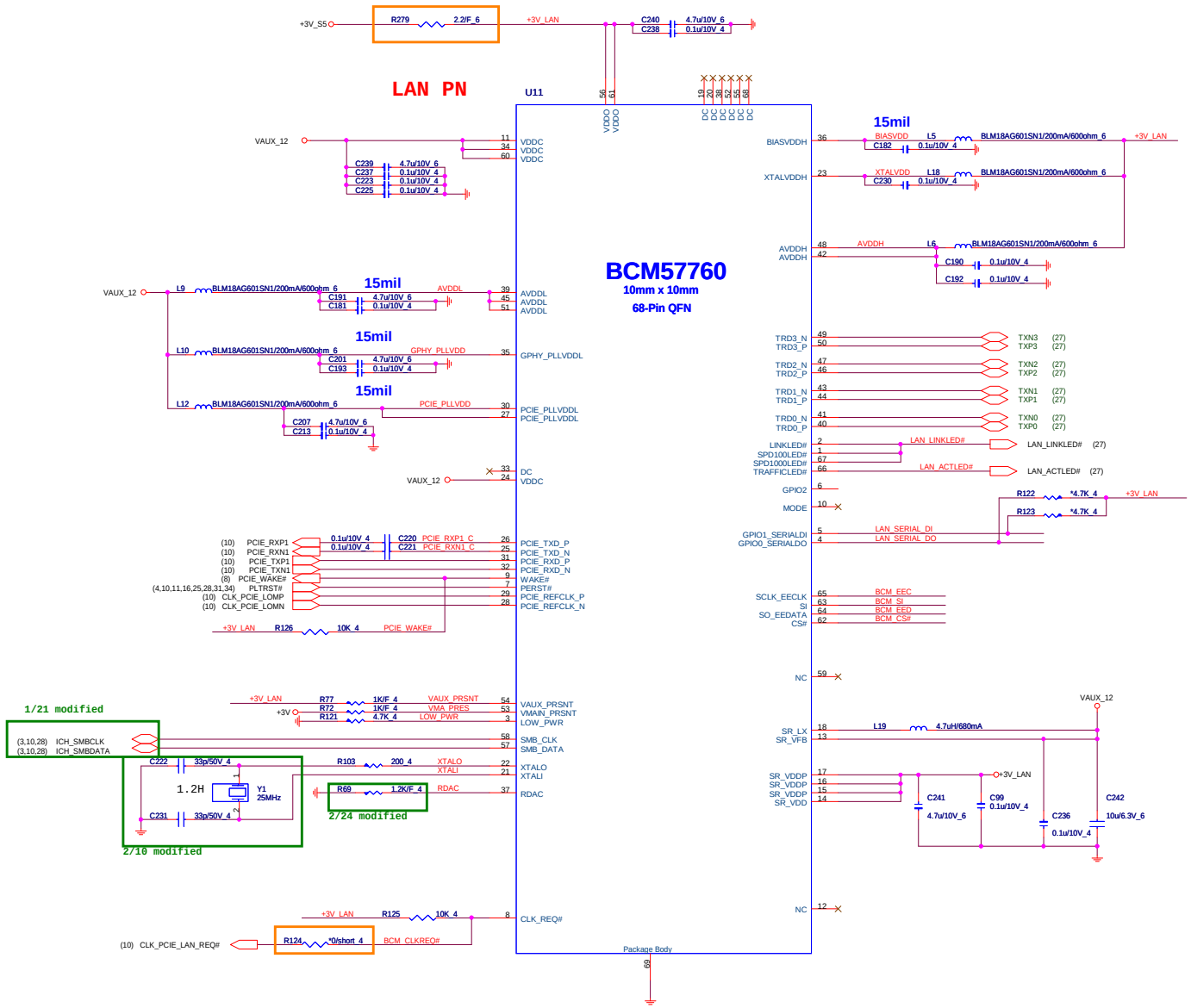
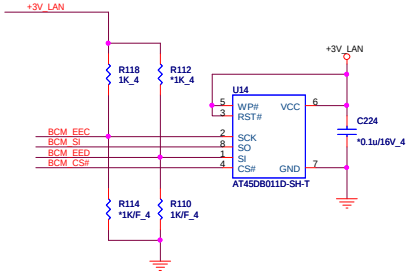
Giga-LAN BCM57760(LAN)



Flash (1M) for ASF2.0



Quanta Computer Inc.			
PROJECT : ZQ3			
Size	Document Number		Rev
	LAN (AR8151)		1A
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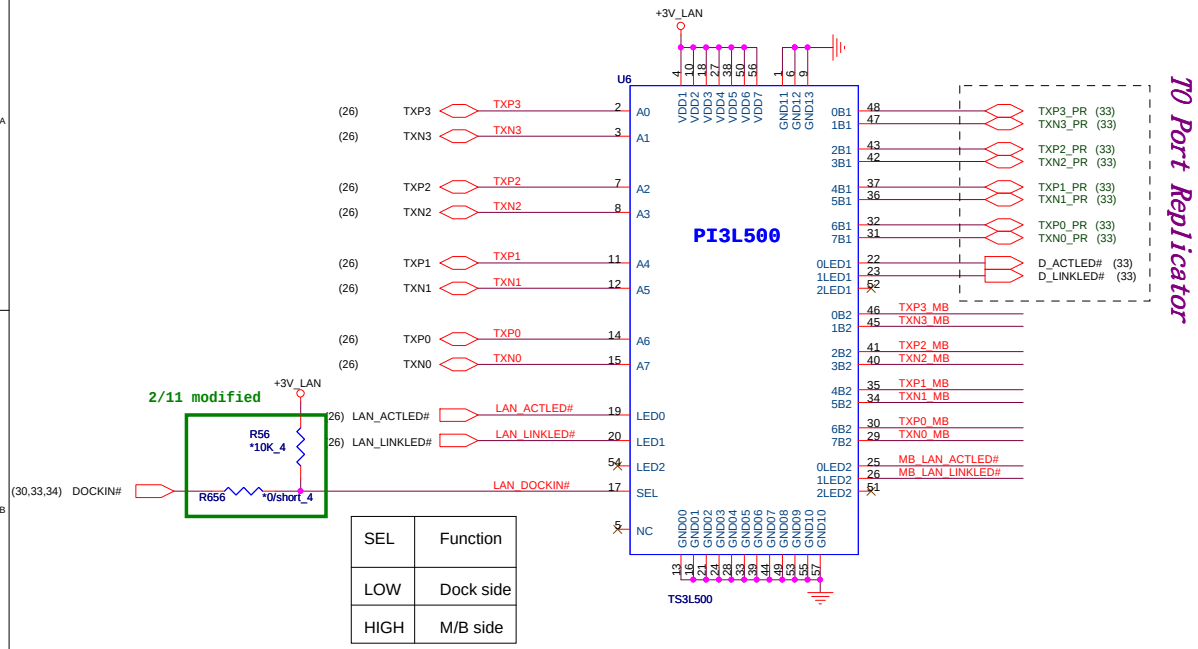
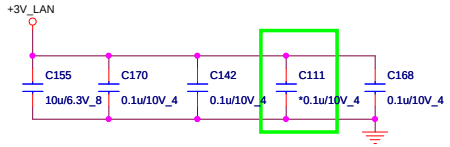
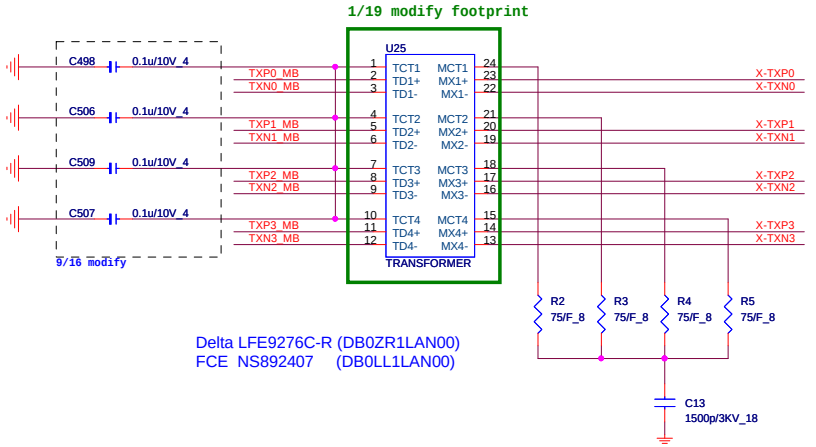
LAN SWITCH (DOK)



SEL	Function
LOW	Dock side
HIGH	M/B side

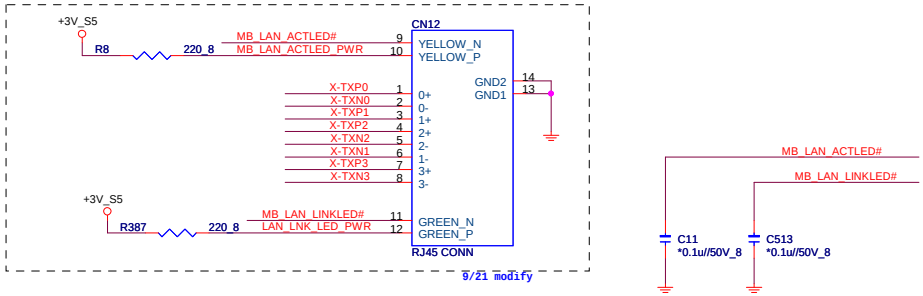


TRANSFORMER (LAN)



Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

RJ45(LAN)



Quanta Computer Inc. PROJECT : ZQ3			
Size	Document Number: LAN SWITCH/TRANSFORMER/RJ45/BT		Rev 1A
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+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

MINI-CARD WLAN/WMAX(MPC)

1/21 modify (R281,R291 no stuff)

H=5.6mm

CN20

MINI-CARD 5.6H CONN

1/21 modify to NMOS

Active Low

9/10 modify

9/2 modify

9/4 modify

9/22 modify

8/12 modify

MINI-CARD 3G(MNC)Reserve for JV41-CP

H=7.0mm

CN17

MINI-CARD 7.0H CONN

Active Low

1/13 modified

9/10 modify

9/4 modify

9/22 modify

A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

SIM CARD FFC connector(RFM)

CN4

3G@SIM_CARD FFC CONN

U20
*3G@SN74AHC1G32DCKR

Quanta Computer Inc.			
PROJECT : ZQ3			
Size	Document Number		Rev
	Mini-Card/WL/3G/SIM		1A
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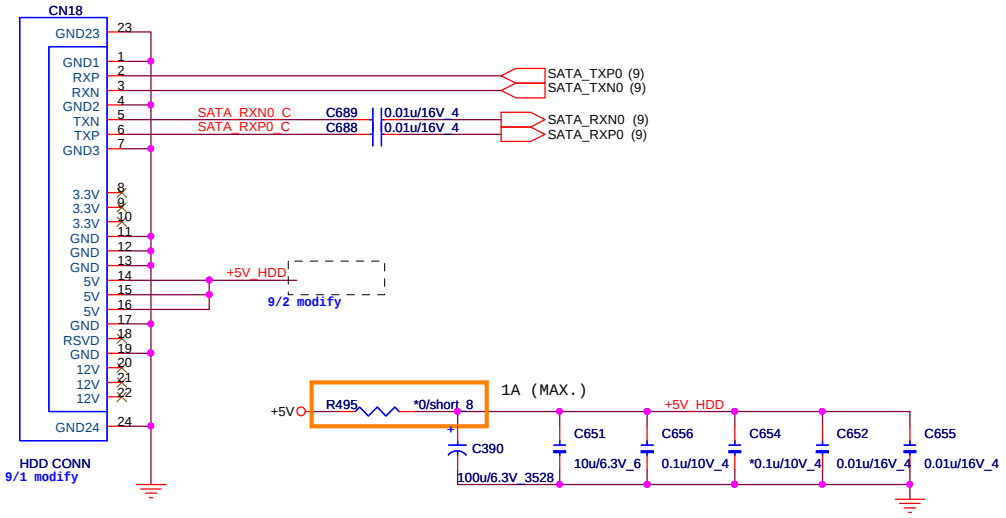
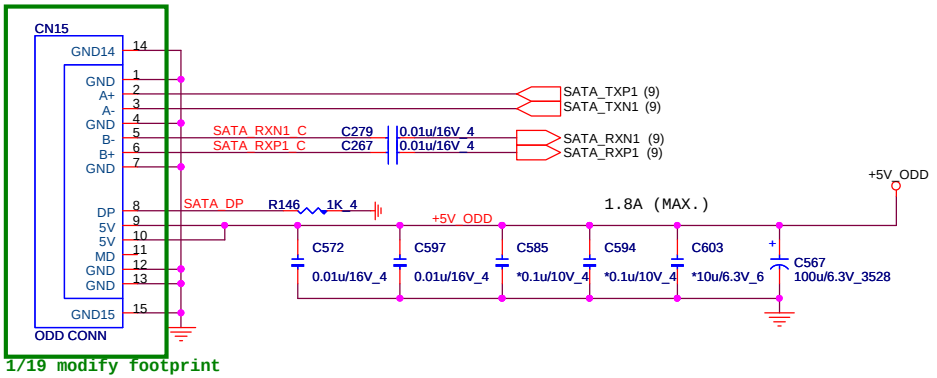
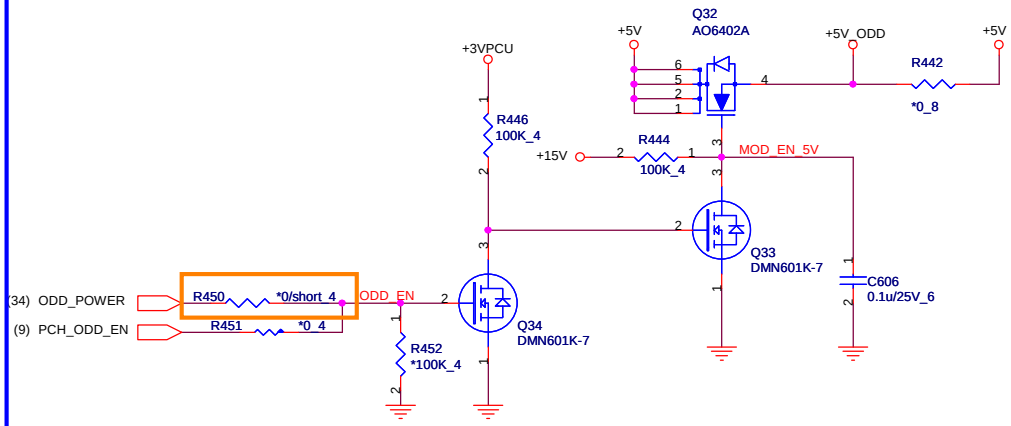
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: SATA-HDD/ODD/HOLE	Rev: 1A
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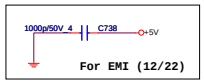
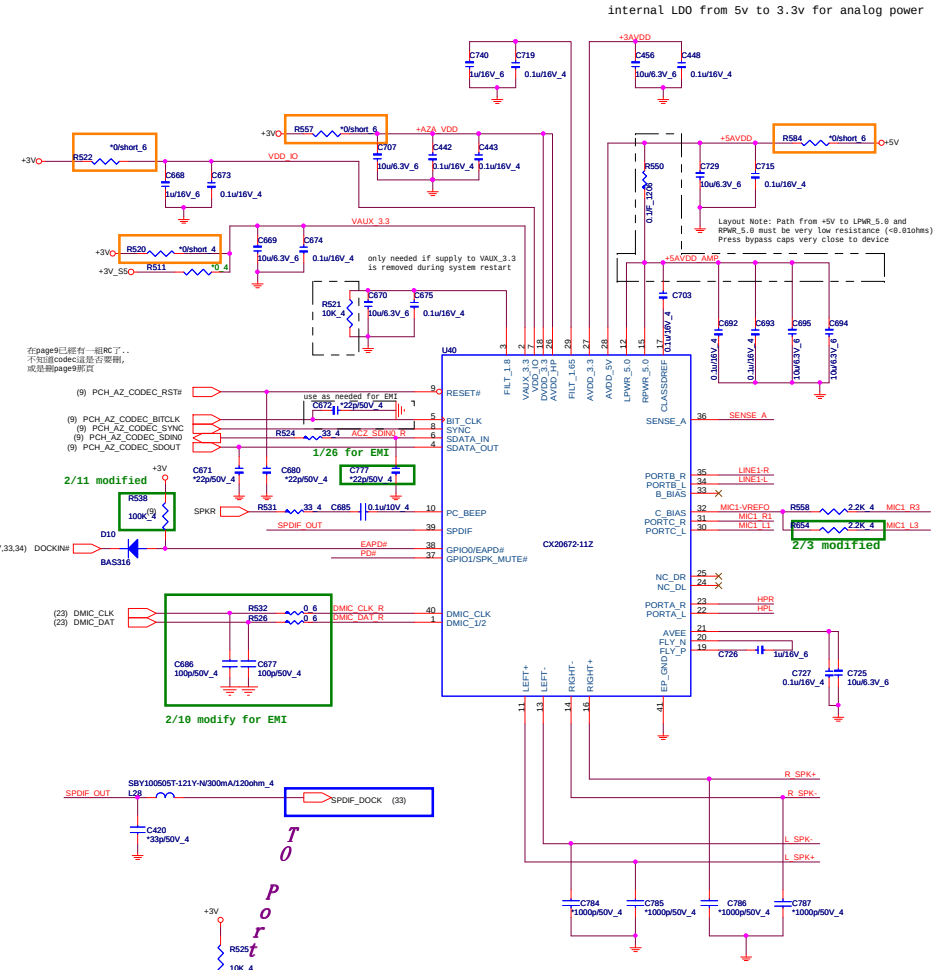
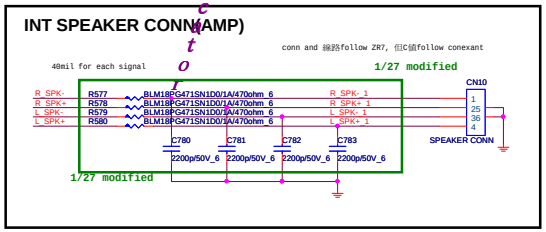
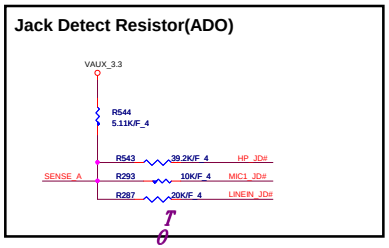
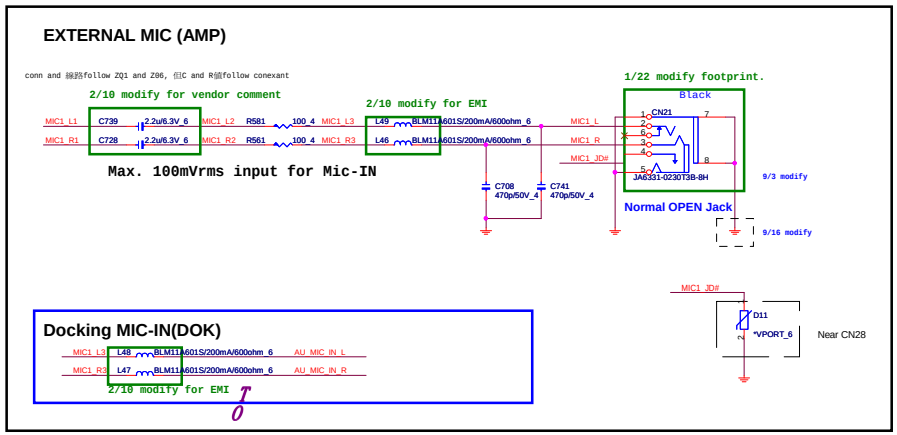
Codec(ADO)

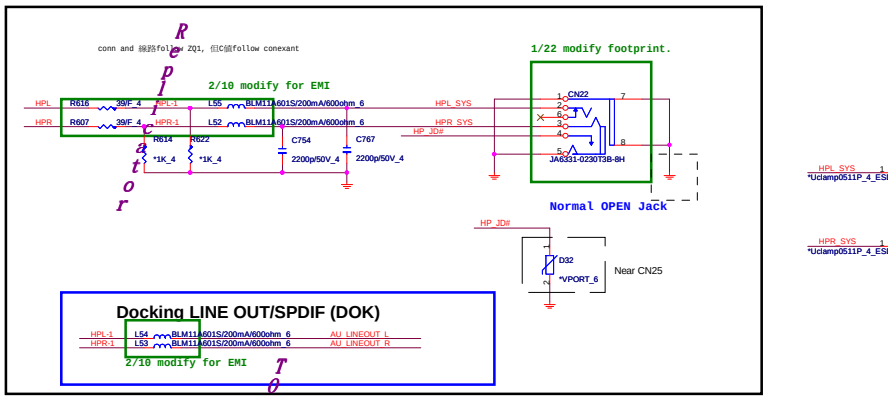


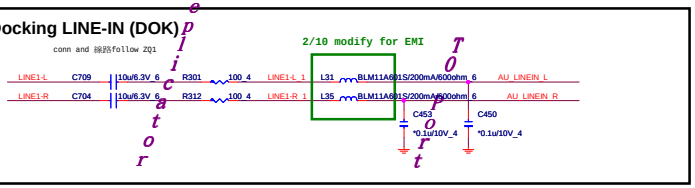


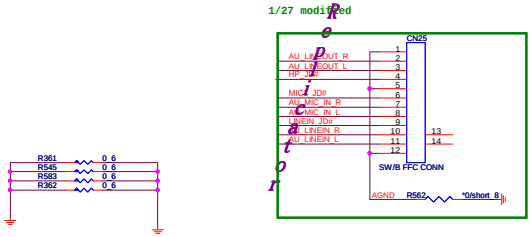


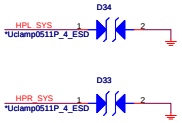












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PROJECT : ZQ3			
Size	Document Number		Rev
	CX20672-11Z/ AMP / SPK		1A
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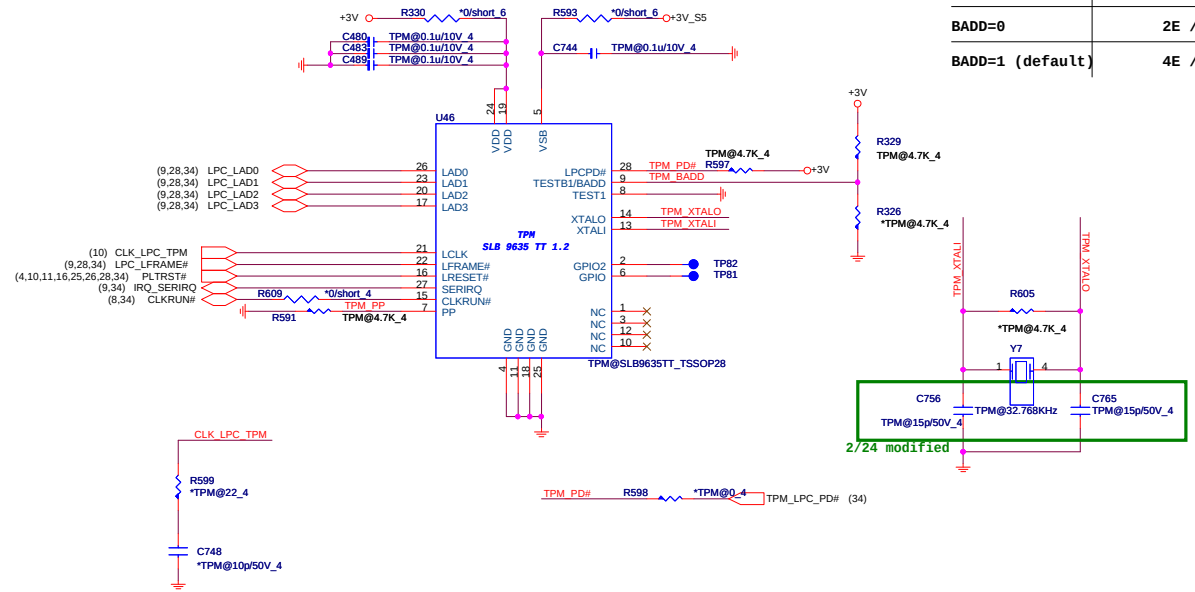
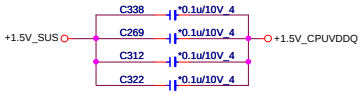
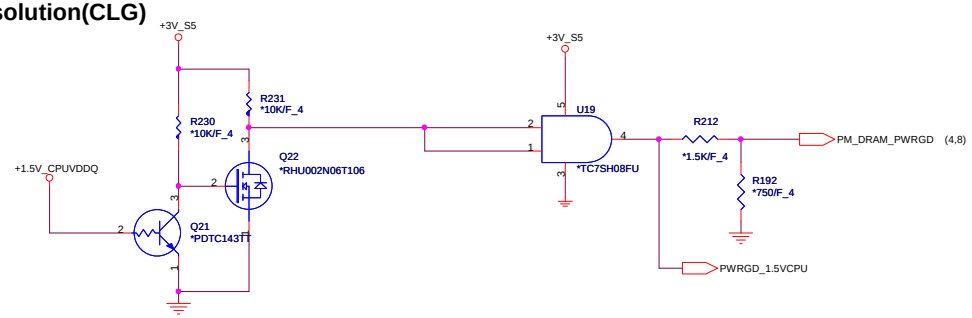
(TPM)

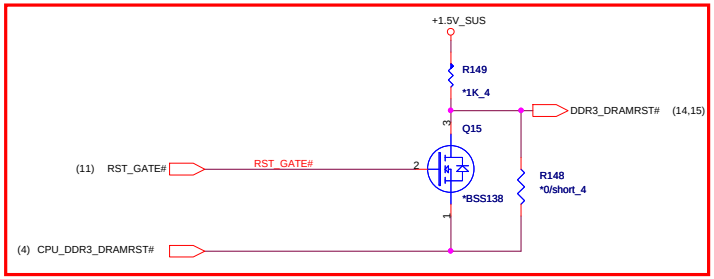
	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

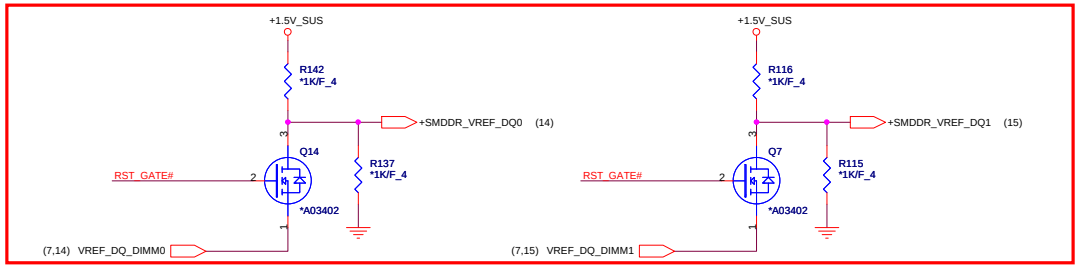




S3 leakage solution(CLG)







Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
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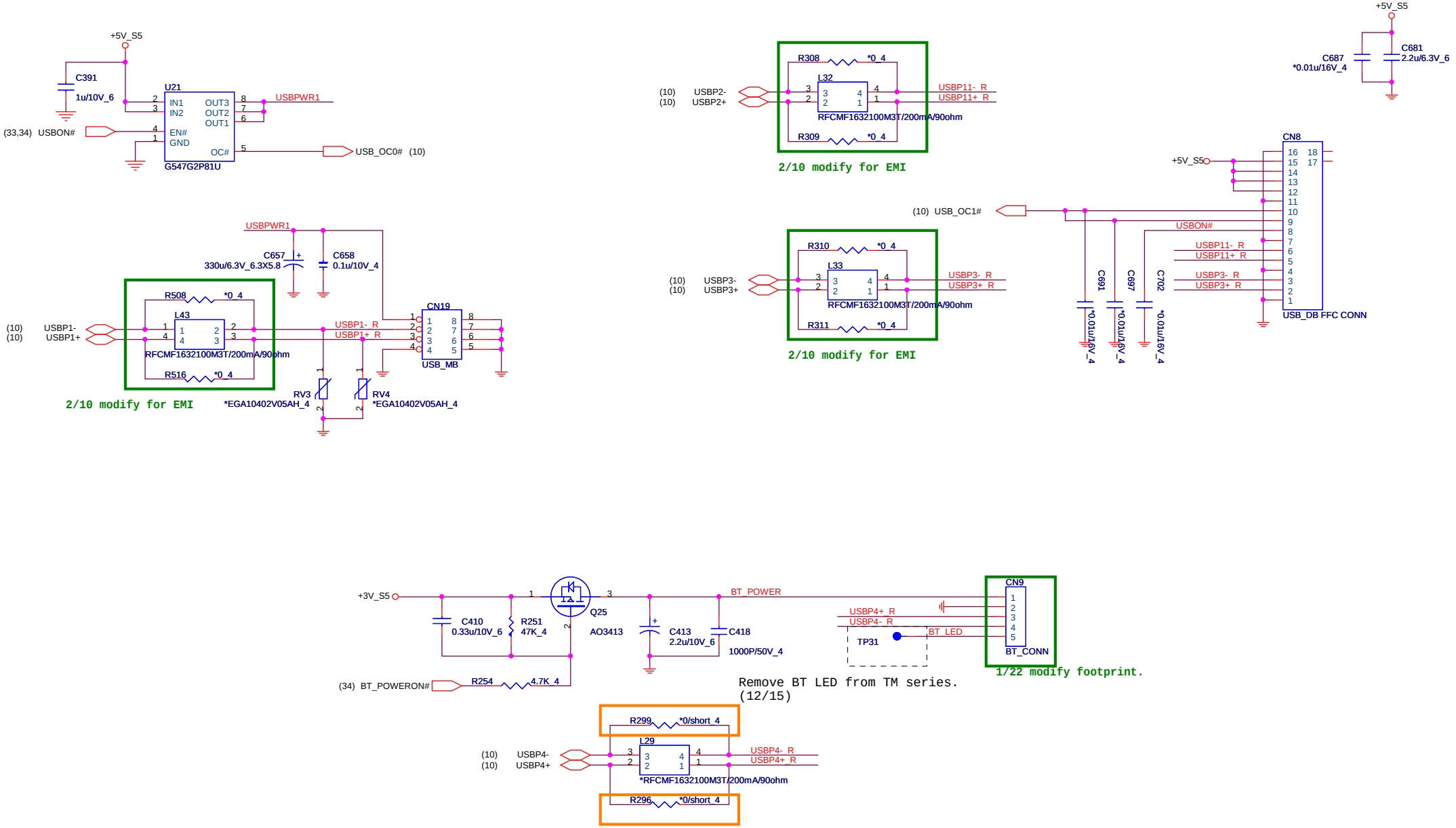

Quanta Computer Inc.

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Size	Document Number	Rev
	eSATA/USB	1A

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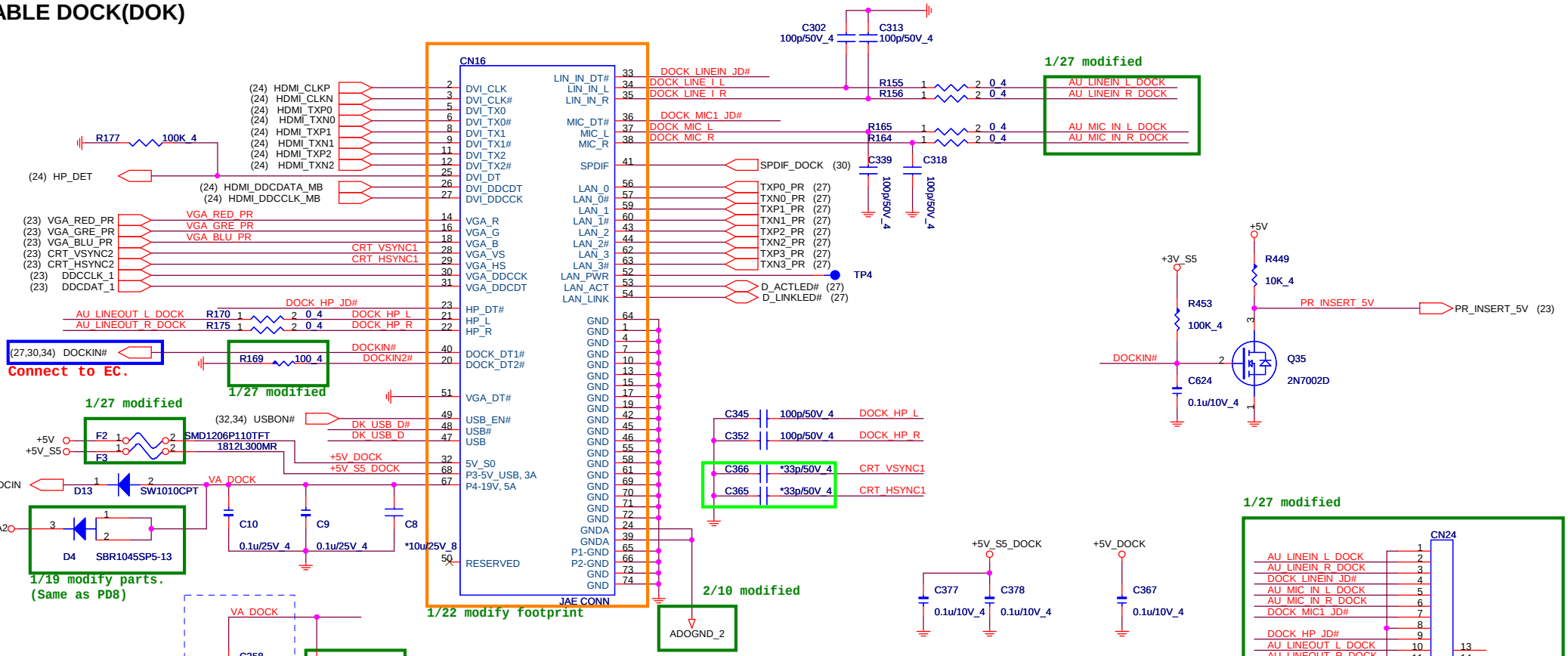
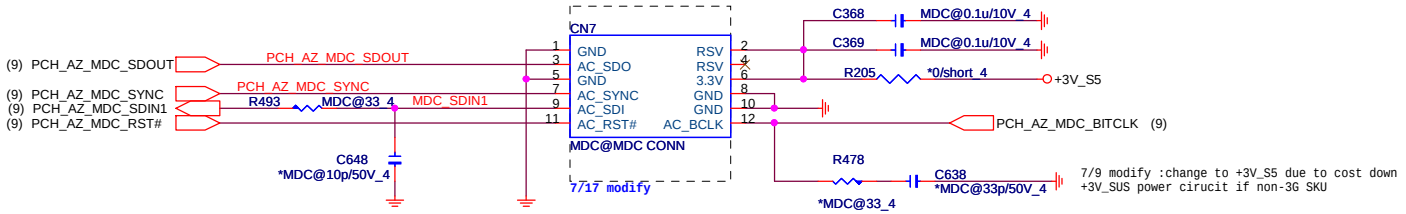
CABLE DOCK(DOK)



MDC(MDM)



Quanta Computer Inc.		
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	Docking	1A
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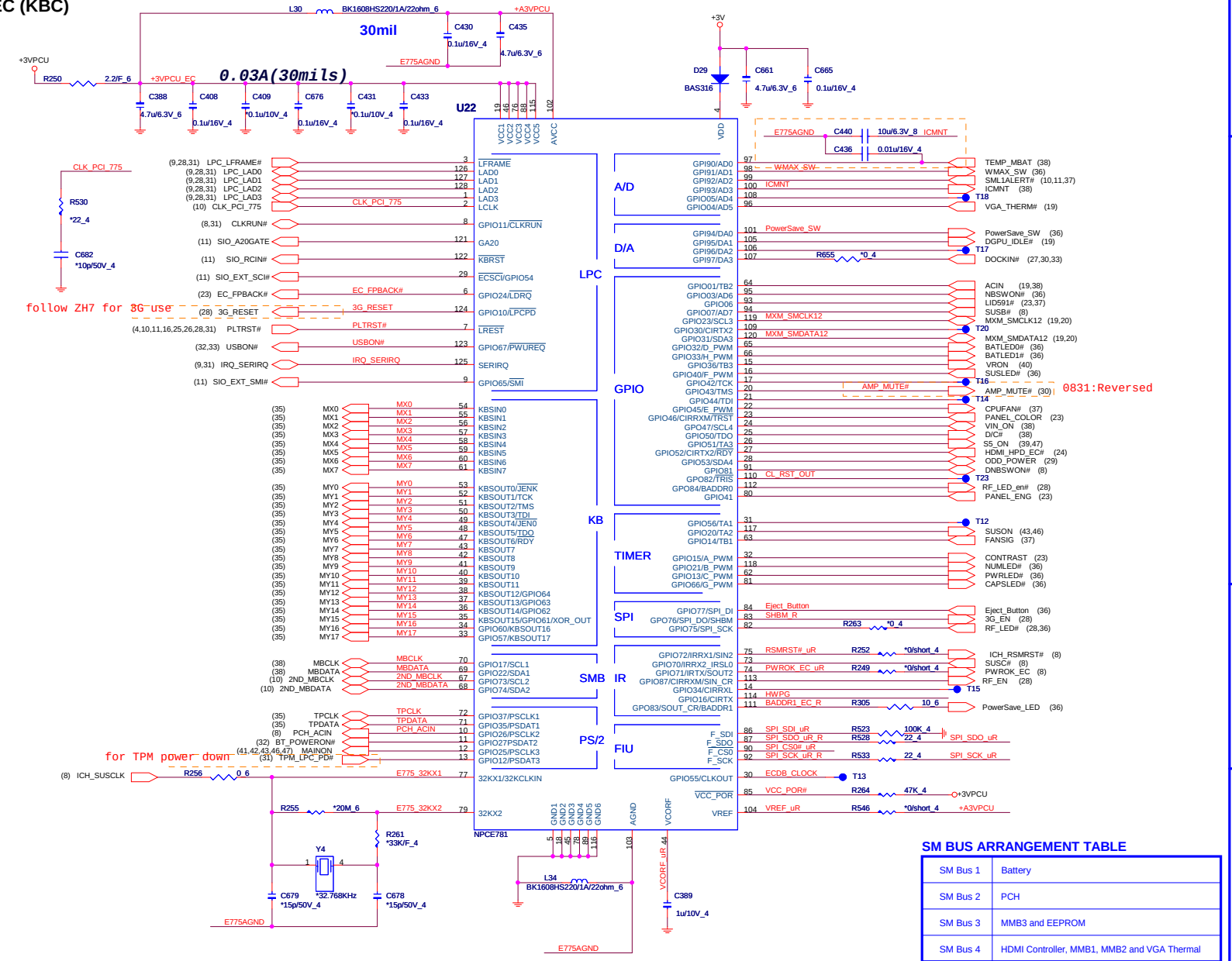
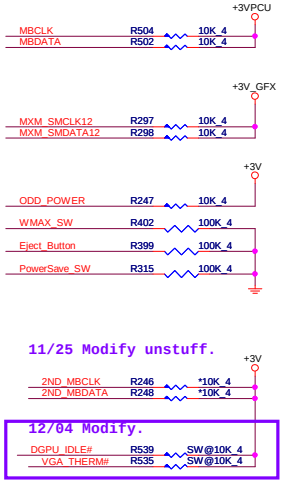
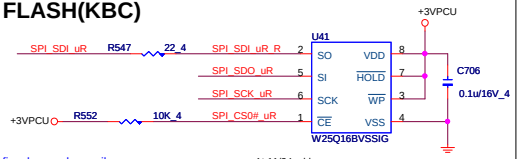
EC (KBC)



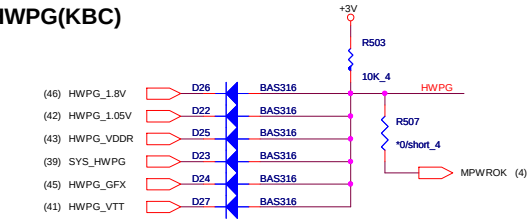
SM BUS PU(KBC)



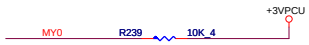
SPI FLASH(KBC)



HWPG(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)



Quanta Computer Inc.	PROJECT : ZQ3
Size	Document Number: WPCE775C_0DG & FLASH — Rev: 1A
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INT K/B (KBC)

CP2 *100p/8P4C: MX3 MX2 MX1 MX0
CP1 *100p/8P4C: MX7 MX6 MX5 MX4
CP3 *100p/8P4C: MY3 MY2 MY1 MY0
CP4 *100p/8P4C: MY7 MY6 MY5 MY4
CP5 *100p/8P4C: MY11 MY10 MY9 MY8
CP6 *100p/8P4C: MY15 MY14 MY13 MY12
C559 *100p/50V_4 MY16
C560 *100p/50V_4 MY17

(34) MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15 MY16 MY17 MX7 MX6 MX5 MX4 MX3 MX2 MX1 MX0

CN5 KB CONN

+3VPCU

RP1 10K/10P8R: MX4 MX5 MX6 MX7 / MX3 MX2 MX1 MX0

1/22 modify footprint.

TOUCHPAD & Finger-Printer CONN.(TPD)

+5V
R418 10K_4
R419 10K_4
(34) TPDATA
(34) TPCLK
L38 LZA10-2ACB104MT/100mA
L39 LZA10-2ACB104MT/100mA
C563 0.01u/25V_4
C562 0.01u/25V_4

For EMI. (3/26)

+5V
L3 BLM21P300S/3A/30ohm_8
C145 0.1u/16V_4
20mil
+TPVDD
TPDATA_R
TPCLK_R
(10)USBP11+
(10)USBP11-
USBP11+
USBP11-
CN6 TP+FP FFC CONN
RV1 *EGA10402V05AH_
RV2 *EGA10402V05AH_
USBP11-
USBP11+

HOLE1 *HG-C276D118P2
HOLE2 *HG-C315D118P2
HOLE28 *HG-C276D118P2
HOLE7 *HG-C276D118P2
HOLE5 *HG-TC276BC315D118P2
HOLE12 *HG-C197D118P2
HOLE10 *HG-TC315BC276D118P2
HOLE16 *HG-C276D118P2
HOLE23 *HG-C276D118P2
HOLE21 *HG-C236D118P2
HOLE24 *HG-C236D118P2
HOLE22 *HG-C315D118P2
HOLE14 *HG-C315D118P2
HOLE3 *H-C276D142P2
HOLE4 *H-C217D146P2
HOLE9 *H-C217D146P2
HOLE11 *H-TC276BC256D146P2
HOLE15 * H-C197D59P2
HOLE18 * H-C197D59P2
HOLE17 *H-TC276BC217D146P2
HOLE20 *H-TC276BC217D146P2
HOLE25 *H-C197D87P2
HOLE26 *H-C197D87P2
HOLE27 * H-C197D51P1
HOLE6 *H-C94D94N
HOLE8 *O-ZQ3-2
HOLE19 *O-ZQ3-1

ZQ3_BKT
*Intel_CPU_BKT

+3V
EC4 *0.1u/10V_4
EC5 *0.1u/10V_4
EC6 *0.1u/10V_4
+5V_S5
EC7 *0.1u/10V_4
EC8 *0.1u/10V_4
EC9 *0.1u/10V_4

2/8 modified for EMI

Quanta Computer Inc.
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Size	Document Number	Rev
	KB/TP+FP/CIR/BT/TPScreen	1A

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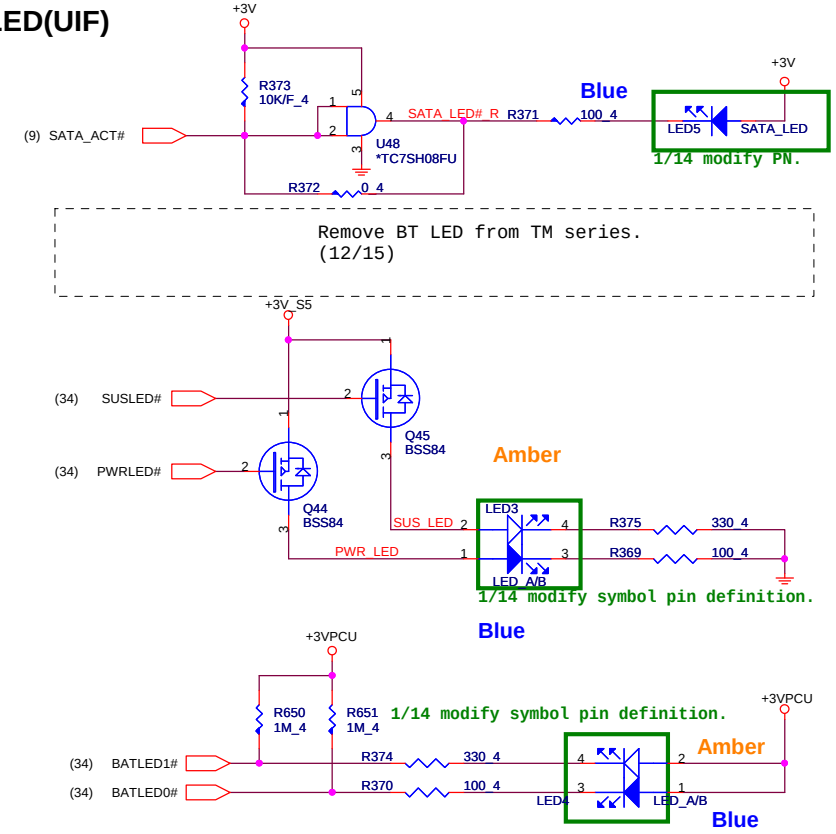
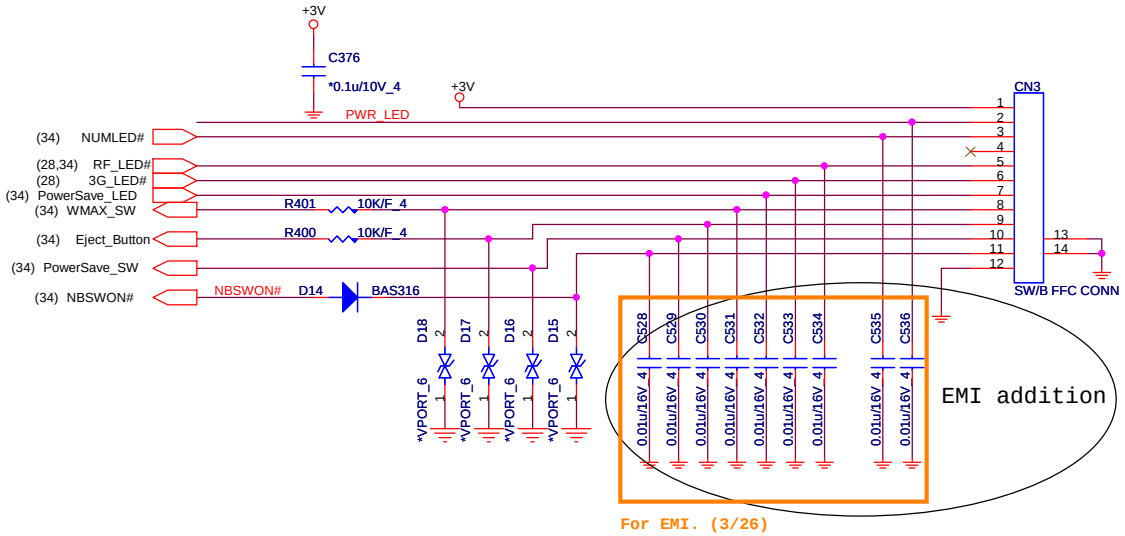
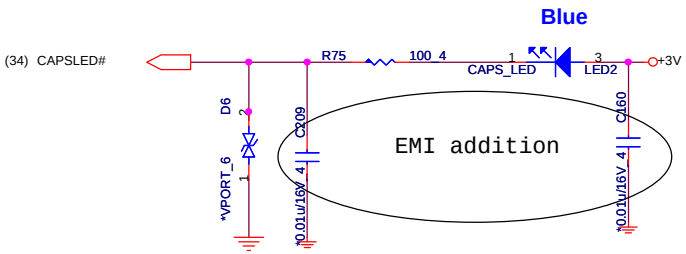
M/B LED(UIF)

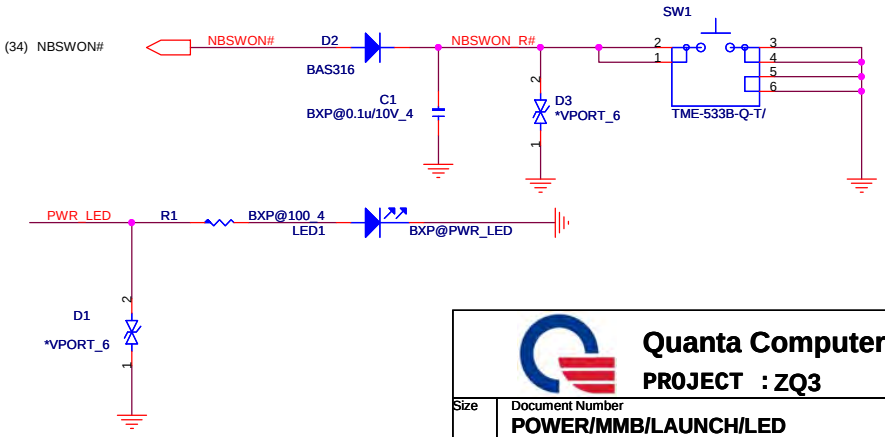


SW BOARD CONNECTOR(UIF)



M/B LED(UIF)





Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A

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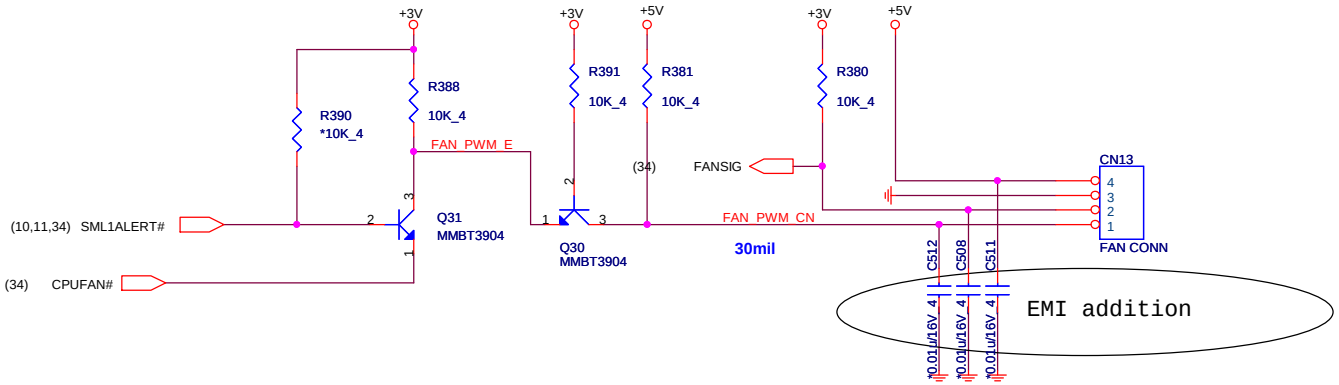
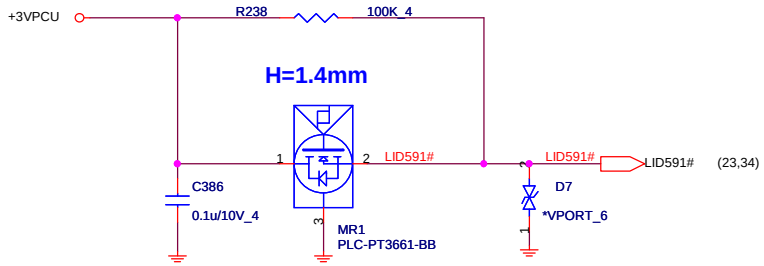
CPU FAN(THM)



HALL SENSOR(HSR)



Quanta Computer Inc. PROJECT : ZQ3		
Size	Document Number: FAN/Thermal Protection	Rev: 1A
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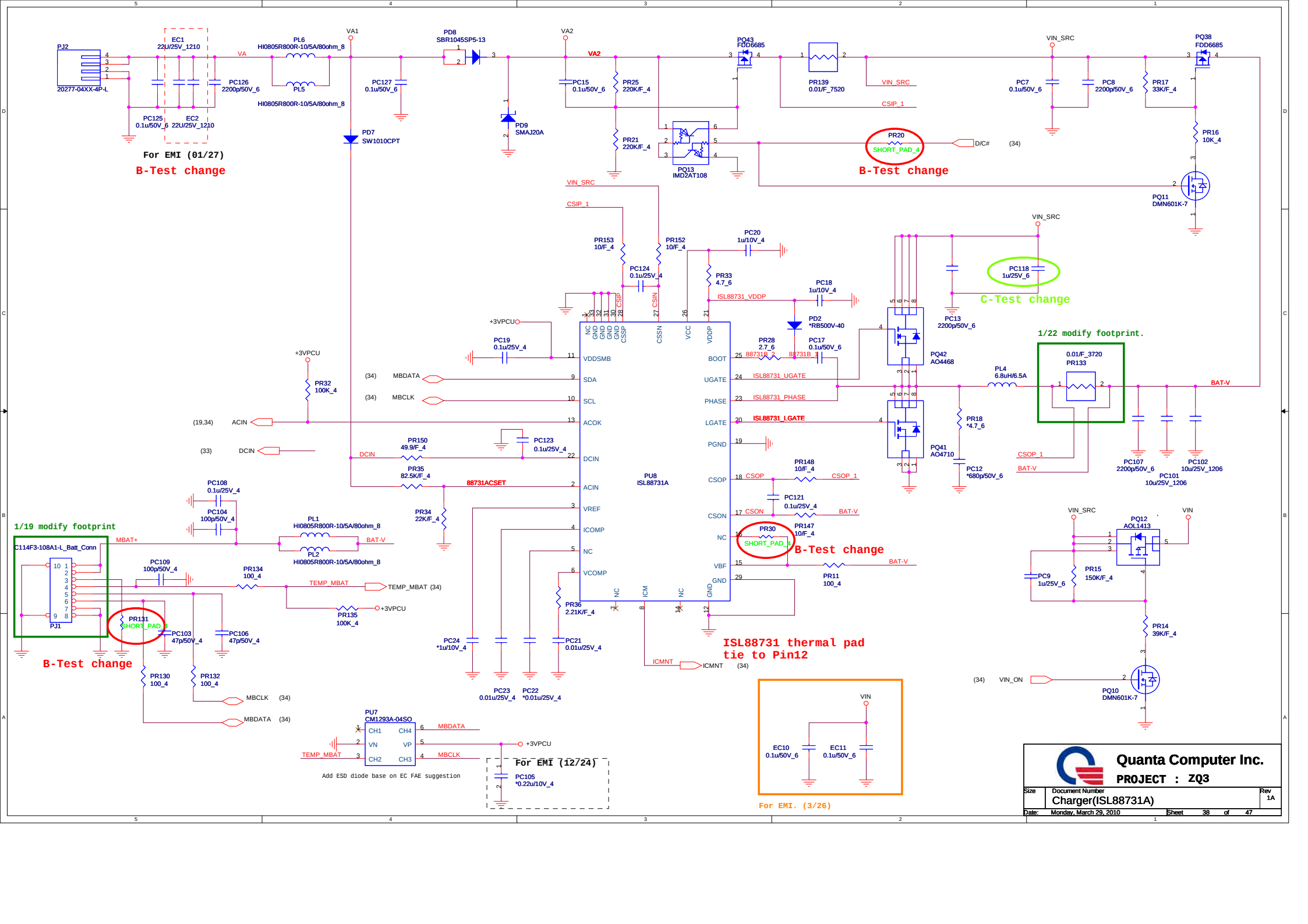
PJ2
20277-04XX-4P-L
EC1
22U/25V_1210
EC2
22U/25V_1210
PC125
0.1u/50V_6
PC126
2200p/50V_6
VA
PL6
HI0805R800R-10/5A/80ohm_8
PL5
HI0805R800R-10/5A/80ohm_8
VA1
PC127
0.1u/50V_6
PD7
SW1010CPT
For EMI (01/27)
B-Test change
PD8
SBR1045SP5-13
PD9
SMAJ20A
VA2
PC15
0.1u/50V_6
PR25
220K/F_4
PR21
220K/F_4
PQ43
FDD6685
PQ13
IMD2AT108
PR139
0.01/F_7520
VIN_SRC
CSIP_1
PR20
SHORT_PAD_4
D/C#
(34)
B-Test change
PC7
0.1u/50V_6
PC8
2200p/50V_6
PR17
33K/F_4
PQ38
FDD6685
PR16
10K_4
PQ11
DMN601K-7
PR153
10/F_4
PR152
10/F_4
PC124
0.1u/25V_4
PC20
1u/10V_4
PR33
4.7_6
ISL88731_VDDP
PC18
1u/10V_4
PD2
*RB500V-40
PC17
0.1u/50V_6
PC118
1u/25V_6
C-Test change
PC13
2200p/50V_6
+3VPCU
PC19
0.1u/25V_4
PR32
100K_4
(34) MBDATA
(34) MBCLK
(19,34) ACIN
(33) DCIN
PR150
49.9/F_4
PC123
0.1u/25V_4
PR35
82.5K/F_4
88731ACSET
PR34
22K/F_4
PU8
ISL88731A
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
88731B_2
88731B_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PR28
2.7_6
PC121
0.1u/25V_4
PR148
10/F_4
PR147
10/F_4
PR30
SHORT_PAD_4
PR11
100_4
PR36
2.21K/F_4
PC24
*1u/10V_4
PC23
0.01u/25V_4
PC22
*0.01u/25V_4
PC21
0.01u/25V_4
ICMNT
(34)
ISL88731 thermal pad
tie to Pin12
PQ42
AO4468
PQ41
AO4710
PR18
*4.7_6
PC12
*680p/50V_6
PL4
6.8uH/6.5A
1/22 modify footprint.
0.01/F_3720
PR133
BAT-V
CSOP_1
PC107
2200p/50V_6
PC102
10u/25V_1206
PC101
10u/25V_1206
1/19 modify footprint
C114F3-108A1-L_Batt_Conn
MBAT+
PC108
0.1u/25V_4
PC104
100p/50V_4
PL1
HI0805R800R-10/5A/80ohm_8
PL2
HI0805R800R-10/5A/80ohm_8
BAT-V
PC109
100p/50V_4
PR134
100_4
TEMP_MBAT
TEMP_MBAT (34)
PR135
100K_4
+3VPCU
PR131
SHORT_PAD_4
PC103
47p/50V_4
PC106
47p/50V_4
PJ1
B-Test change
PR130
100_4
PR132
100_4
MBCLK (34)
MBDATA (34)
PU7
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
MBCLK
TEMP_MBAT
+3VPCU
Add ESD diode base on EC FAE suggestion
For EMI (12/24)
PC105
*0.22u/10V_4
VIN
EC10
0.1u/50V_6
EC11
0.1u/50V_6
For EMI. (3/26)
PQ12
AOL1413
PC9
1u/25V_6
PR15
150K/F_4
PR14
39K/F_4
(34) VIN_ON
PQ10
DMN601K-7
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
Charger(ISL88731A)
Rev
1A
Date: Monday, March 29, 2010
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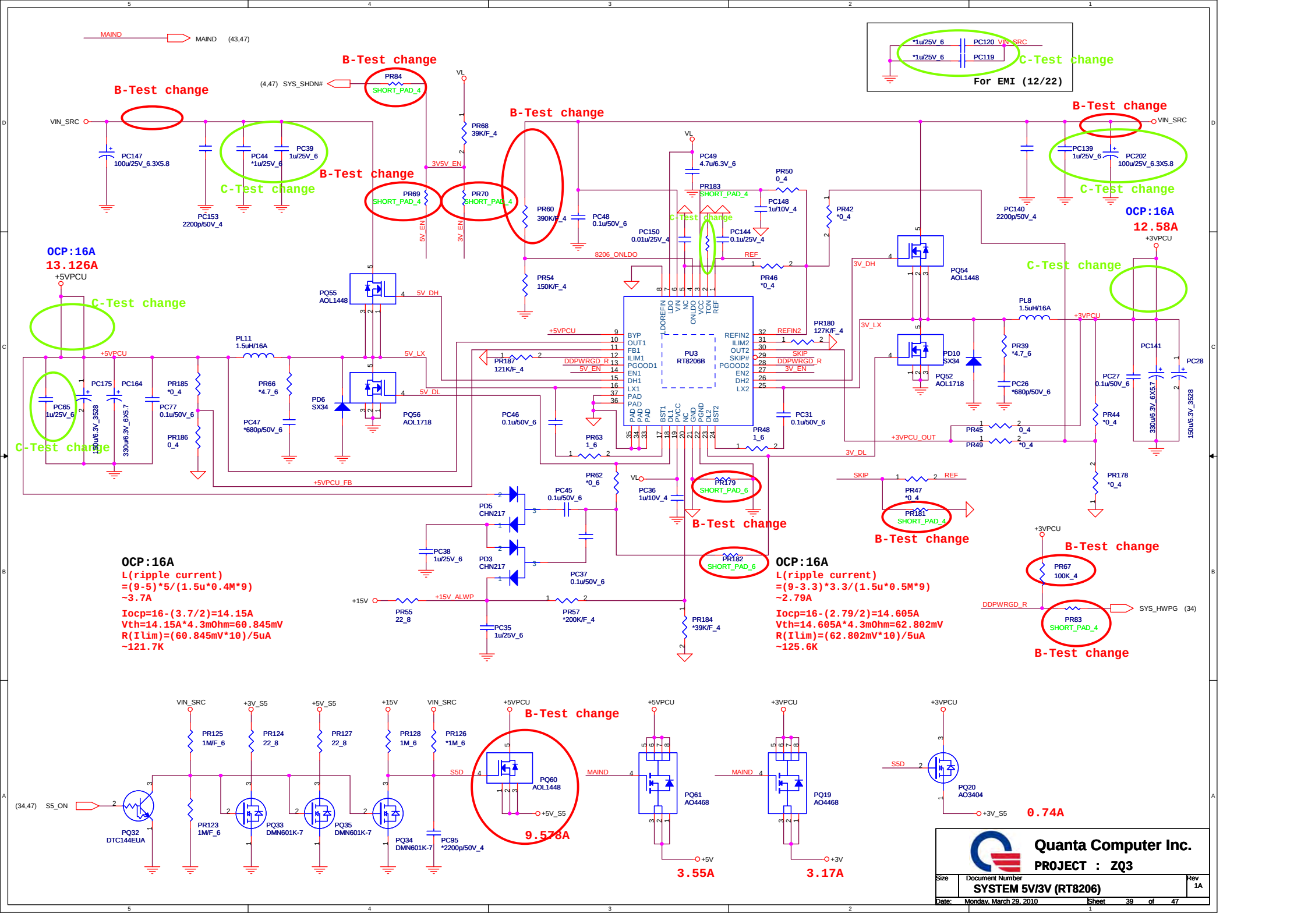
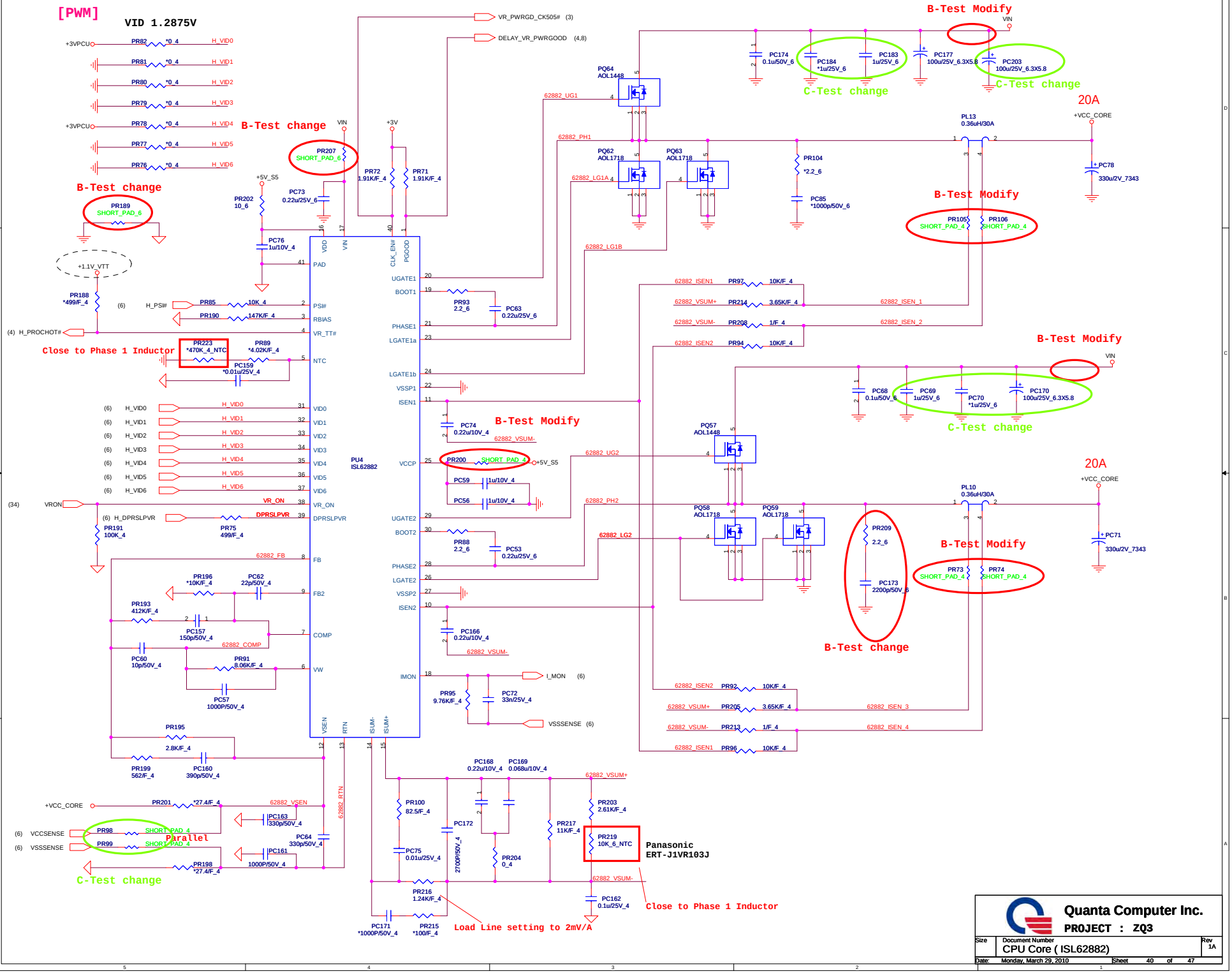
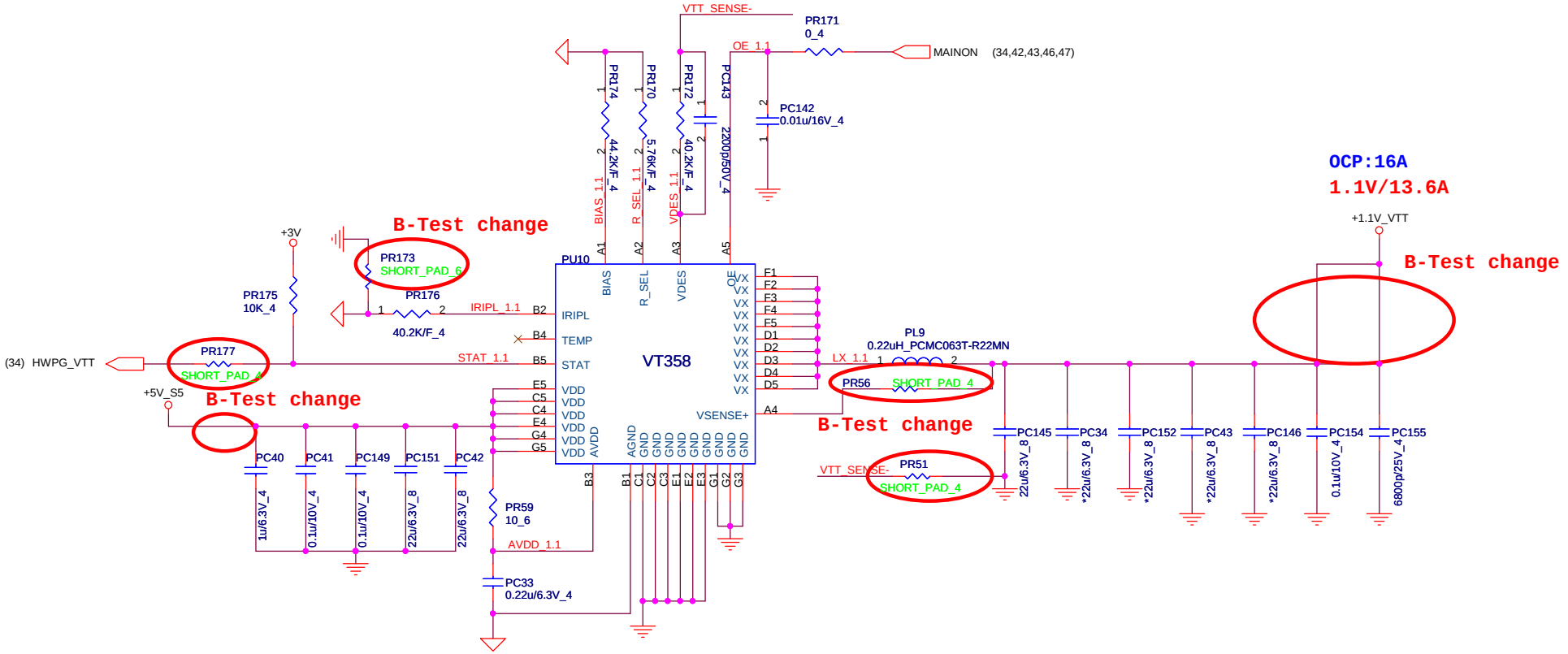

MAIND
MAIND (43,47)
B-Test change
(4,47) SYS_SHDN#
PR84
SHORT_PAD_4
VL
PR68
39K/F_4
3V5V_EN
5V_EN
3V_EN
PR69
SHORT_PAD_4
PR70
SHORT_PAD_4
PR60
390K/F_4
PC48
0.1u/50V_6
PC150
0.01u/25V_4
PC49
4.7u/6.3V_6
PR183
SHORT_PAD_4
PR50
0_4
PC148
1u/10V_4
PC144
0.1u/25V_4
PR42
*0_4
PR46
*0_4
8206_ONLDO
REF
PR54
150K/F_4
VIN_SRC
PC147
100u/25V_6.3X5.8
PC153
2200p/50V_4
PC44
*1u/25V_6
PC39
1u/25V_6
C-Test change
PC120 VIN_SRC
PC119
*1u/25V_6
*1u/25V_6
For EMI (12/22)
PC139
1u/25V_6
PC202
100u/25V_6.3X5.8
PC140
2200p/50V_4
OCP:16A
12.58A
OCP:16A
13.126A
+5VPCU
+3VPCU
PQ55
AOL1448
5V_DH
3V_DH
PQ54
AOL1448
PL11
1.5uH/16A
PL8
1.5uH/16A
5V_LX
3V_LX
PU3
RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
PR187
121K/F_4
DDPWRGD_R
5V_EN
SKIP
3V_EN
PR180
127K/F_4
REFIN2
PD6
SX34
PD10
SX34
PQ56
AOL1718
PQ52
AOL1718
PR185
*0_4
PR186
0_4
PR66
*4.7_6
PC47
*680p/50V_6
PR39
*4.7_6
PC26
*680p/50V_6
PC65
1u/25V_6
PC175
150u/6.3V_3528
PC164
330u/6.3V_6X5.7
PC77
0.1u/50V_6
PC46
0.1u/50V_6
PC31
0.1u/50V_6
PR63
1_6
PR48
1_6
PR45
0_4
PR49
*0_4
PC27
0.1u/50V_6
PC141
330u/6.3V_6X5.7
PC28
150u/6.3V_3528
PR44
*0_4
PR178
*0_4
+5VPCU_FB
+3VPCU_OUT
3V_DL
PR62
*0_6
PC45
0.1u/50V_6
PC36
1u/10V_4
PR179
SHORT_PAD_6
PR47
*0_4
PR181
SHORT_PAD_4
SKIP
REF
PD5
CHN217
PD3
CHN217
PC38
1u/25V_6
PC37
0.1u/50V_6
PR182
SHORT_PAD_6
+15V
+15V_ALWP
PR55
22_8
PR57
*200K/F_4
PC35
1u/25V_6
PR184
*39K/F_4
OCP:16A
L(ripple current)
=(9-5)*5/(1.5u*0.4M*9)
~3.7A
Iocp=16-(3.7/2)=14.15A
Vth=14.15A*4.3mOhm=60.845mV
R(Ilim)=(60.845mV*10)/5uA
~121.7K
OCP:16A
L(ripple current)
=(9-3.3)*3.3/(1.5u*0.5M*9)
~2.79A
Iocp=16-(2.79/2)=14.605A
Vth=14.605A*4.3mOhm=62.802mV
R(Ilim)=(62.802mV*10)/5uA
~125.6K
+3VPCU
PR67
100K_4
DDPWRGD_R
SYS_HWPG (34)
PR83
SHORT_PAD_4
B-Test change
VIN_SRC
+3V_S5
+5V_S5
+15V
PR125
1M/F_6
PR124
22_8
PR127
22_8
PR128
1M_6
PR126
*1M_6
S5D
(34,47) S5_ON
PQ32
DTC144EUA
PR123
1M/F_6
PQ33
DMN601K-7
PQ35
DMN601K-7
PQ34
DMN601K-7
PC95
*2200p/50V_4
PQ60
AOL1448
9.578A
MAIND
PQ61
AO4468
3.55A
PQ19
AO4468
3.17A
PQ20
AO3404
0.74A
+5V
+3V
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
1A
Date: Monday, March 29, 2010
Sheet 39 of 47


[PWM]
VID 1.2875V
B-Test Modify
B-Test change
C-Test change
20A
Close to Phase 1 Inductor
Parallel
Panasonic
ERT-J1VR103J
Load Line setting to 2mV/A
PU4
ISL62882
Quanta Computer Inc.
PROJECT : ZQ3
CPU Core (ISL62882)
Monday, March 29, 2010

[PWM]

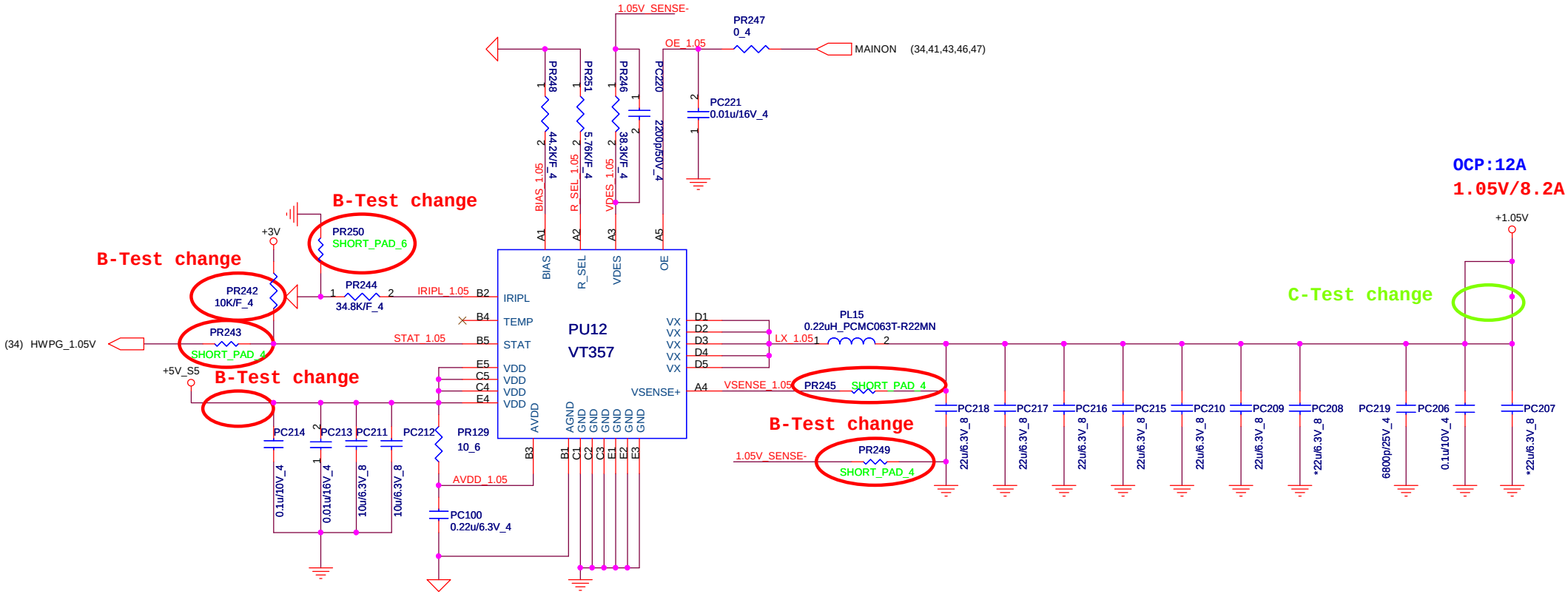


Quanta Computer Inc.

PROJECT : ZQ3

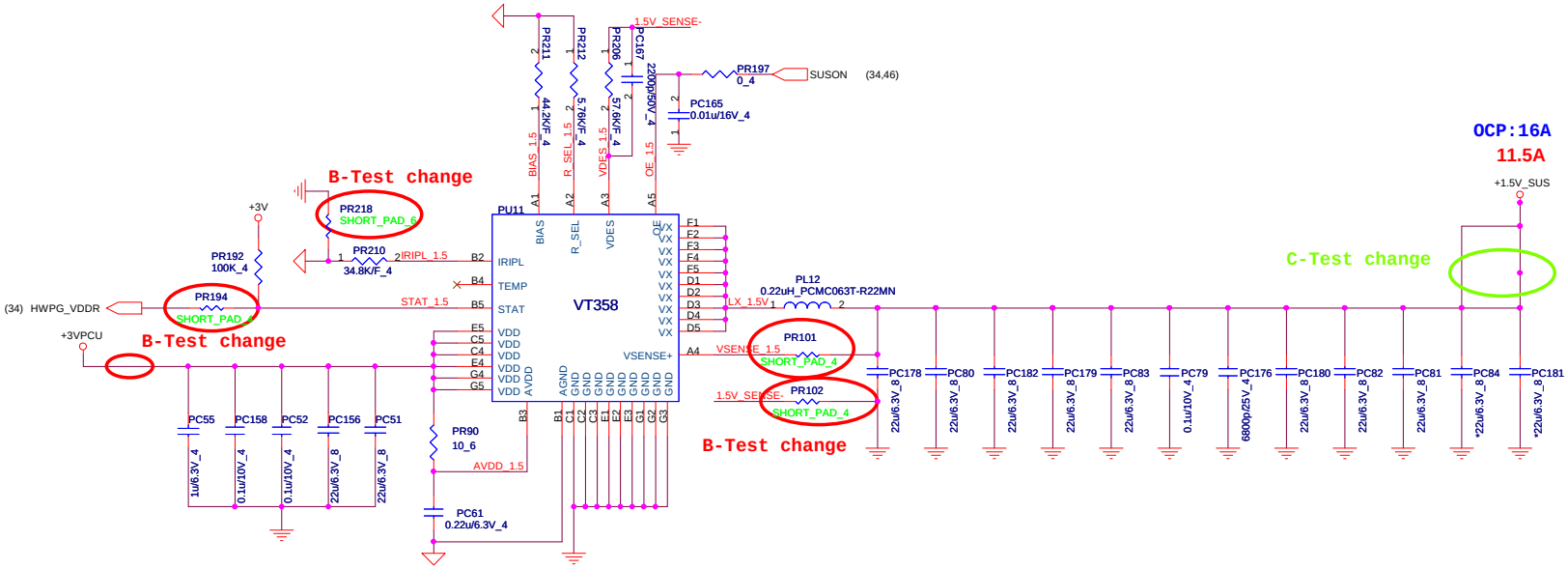
Size	Document Number	Rev
	+VTT (UP6111A)	1A

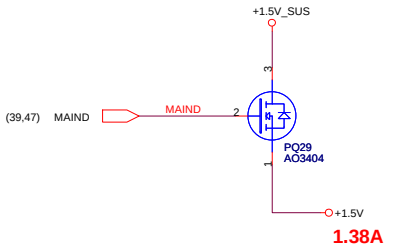
Date: Monday, March 29, 2010 Sheet 41 of 47

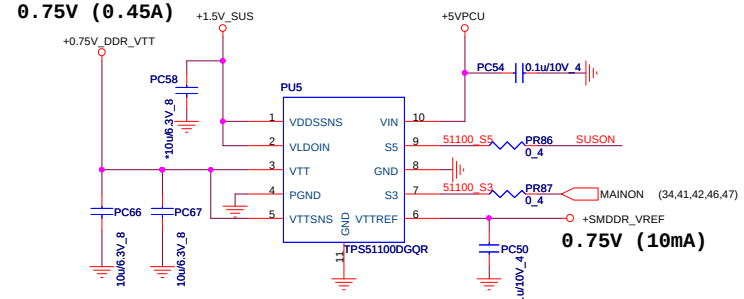


Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Monday, March 29, 2010	Sheet 42 of 47	

[PWM]







	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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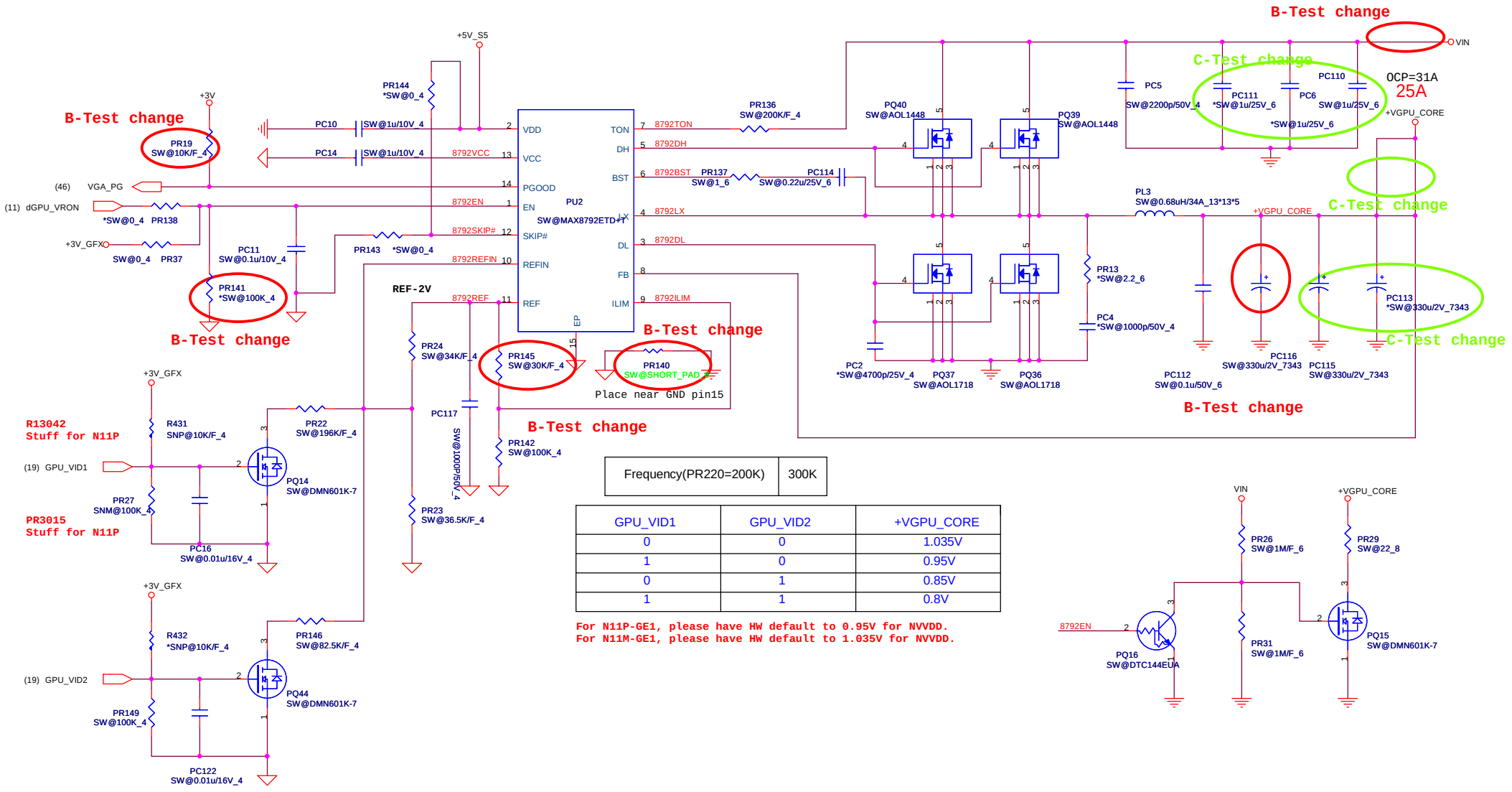

Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
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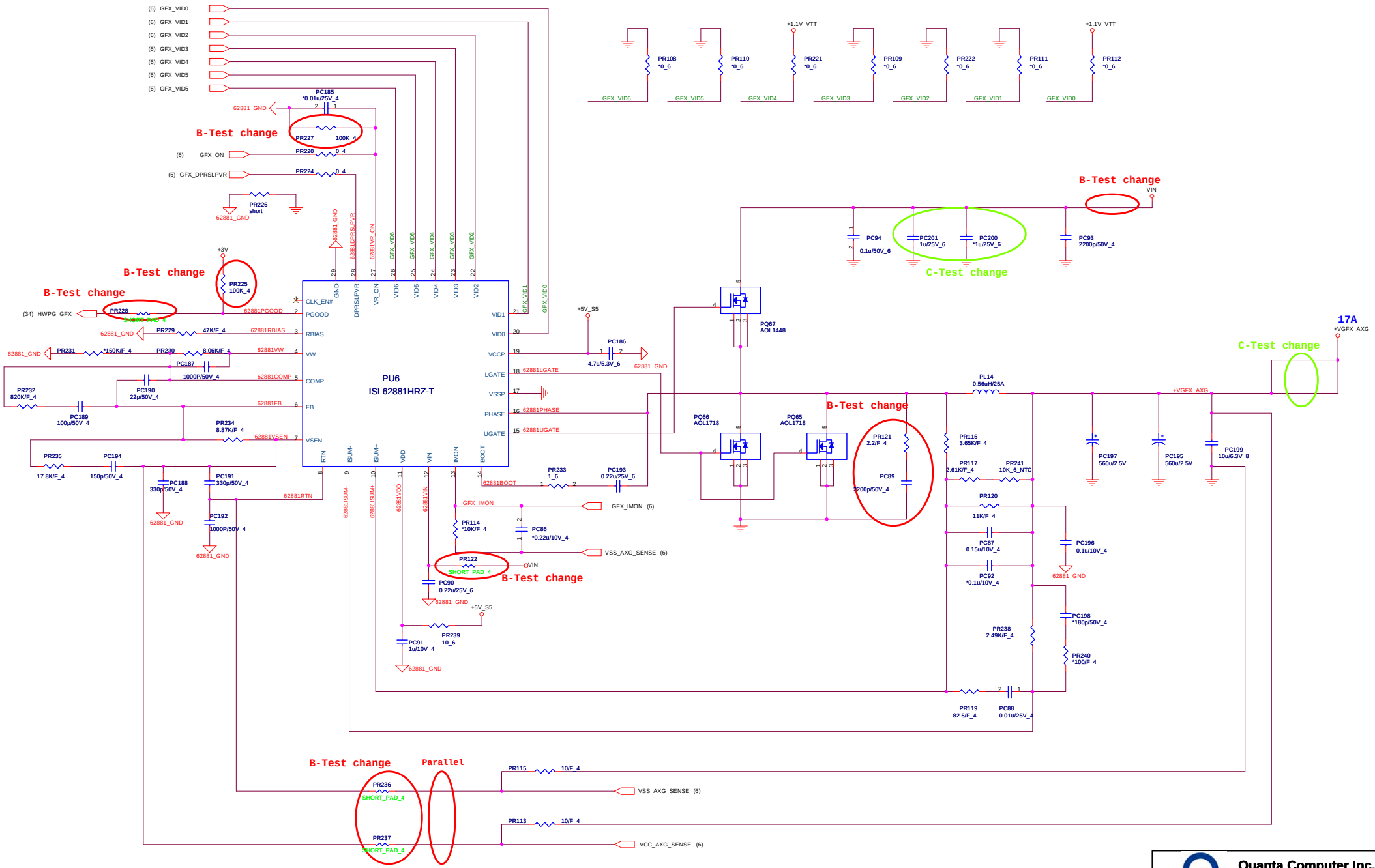
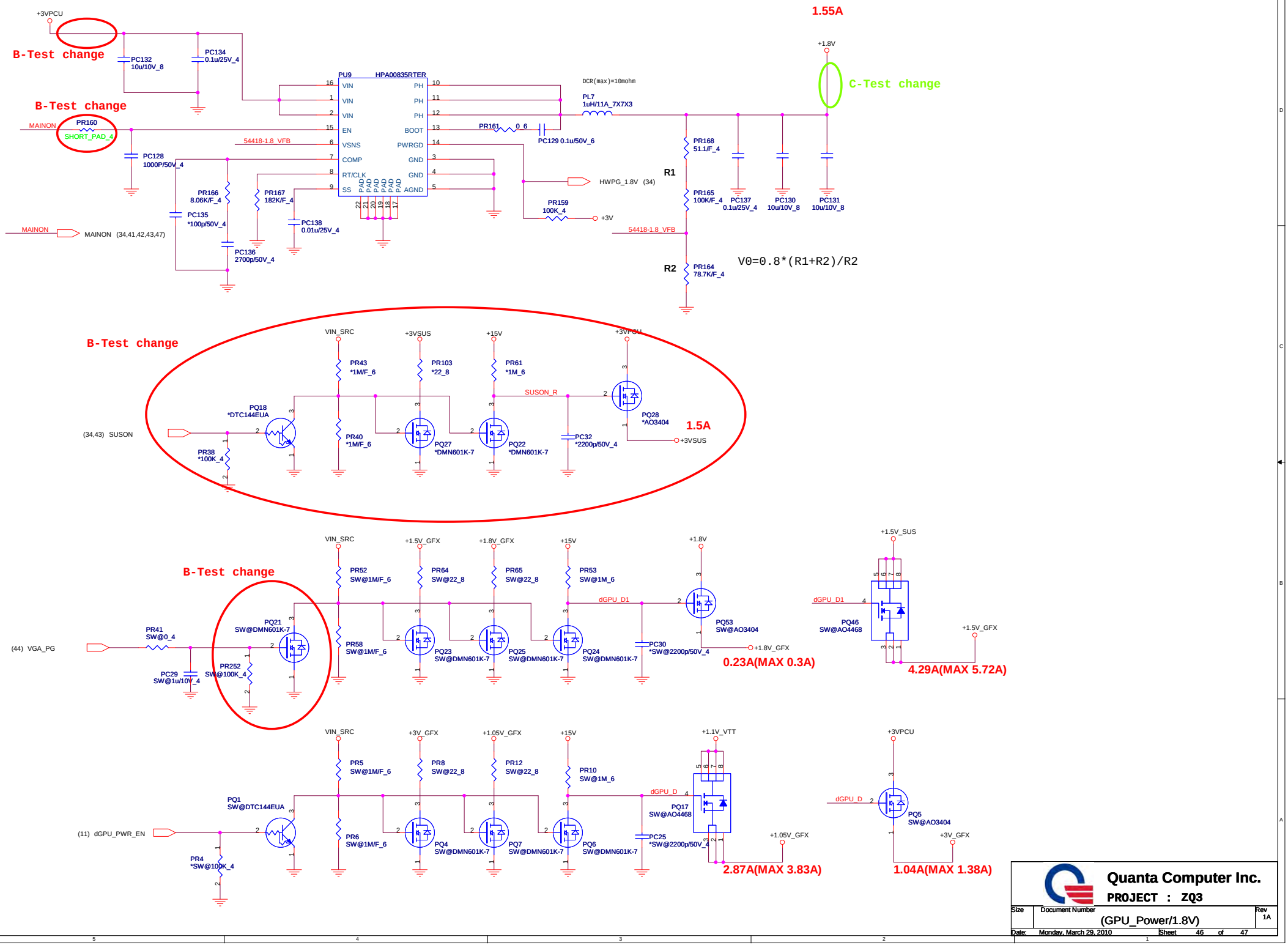
Int_VGA [PWM]


PU6
ISL62881HRZ-T
B-Test change
C-Test change
Parallel
17A
+VGFX_AXG
PQ67 AOL1448
PQ66 AOL1718
PQ65 AOL1718
PL14 0.56uH/25A
PR225 100K_4
PR226 short
PR227 100K_4
PR220 0_4
PR224 0_4
PR228 SHORT_PAD_4
PR229 47K/F_4
PR231 *150K/F_4
PR230 8.06K/F_4
PR232 820K/F_4
PR234 8.87K/F_4
PR235 17.8K/F_4
PR233 1_6
PR114 *10K/F_4
PR122 SHORT_PAD_4
PR239 10_6
PR121 2.2/F_4
PR116 3.65K/F_4
PR117 2.61K/F_4
PR241 10K_6_NTC
PR120 11K/F_4
PR238 2.49K/F_4
PR240 *100/F_4
PR119 82.5/F_4
PR236 SHORT_PAD_4
PR237 SHORT_PAD_4
PR115 10/F_4
PR113 10/F_4
PC185 *0.01u/25V_4
PC187 1000P/50V_4
PC190 22p/50V_4
PC189 100p/50V_4
PC194 150p/50V_4
PC188 330p/50V_4
PC191 330p/50V_4
PC192 1000P/50V_4
PC186 4.7u/6.3V_6
PC193 0.22u/25V_6
PC86 *0.22u/10V_4
PC90 0.22u/25V_6
PC91 1u/10V_4
PC94 0.1u/50V_6
PC201 1u/25V_6
PC200 *1u/25V_6
PC93 2200p/50V_4
PC89 2200p/50V_4
PC87 0.15u/10V_4
PC92 *0.1u/10V_4
PC196 0.1u/10V_4
PC198 *180p/50V_4
PC88 0.01u/25V_4
PC197 560u/2.5V
PC195 560u/2.5V
PC199 10u/6.3V_8
PR108 *0_6
PR110 *0_6
PR221 *0_6
PR109 *0_6
PR222 *0_6
PR111 *0_6
PR112 *0_6
+1.1V_VTT
+5V_S5
+3V
VIN
62881_GND
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6
GFX_ON
GFX_DPRSLPVR
GFX_IMON
VSS_AXG_SENSE
VCC_AXG_SENSE
HWPG_GFX
62881PGOOD
62881RBIAS
62881VW
62881COMP
62881FB
62881VSEN
62881RTN
62881LGATE
62881PHASE
62881UGATE
62881BOOT
62881VR_ON
62881DPRSLPVR
CLK_EN#
PGOOD
RBIAS
VW
COMP
FB
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT
VID1
VID0
VCCP
LGATE
VSSP
PHASE
UGATE
GND
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
Quanta Computer Inc.
PROJECT : ZQ3
+VGFX_AXG (ISL62881)
Size
Document Number
Rev
1A
Date: Monday, March 29, 2010
Sheet 45 of 47
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.


1.55A
B-Test change
C-Test change
+3VPCU
+1.8V
PC132 10u/10V_8
PC134 0.1u/25V_4
PU9 HPA00835RTER
VIN
PH
BOOT
PWRGD
GND
AGND
EN
VSNS
COMP
RT/CLK
SS
PAD
DCR(max)=10mohm
PL7 1uH/11A_7X7X3
PR160 SHORT_PAD_4
MAINON
PR161 0_6
PC129 0.1u/50V_6
54418-1.8_VFB
PC128 1000P/50V_4
PR166 8.06K/F_4
PR167 182K/F_4
PC135 *100p/50V_4
PC136 2700p/50V_4
PC138 0.01u/25V_4
HWPG_1.8V (34)
PR159 100K_4
+3V
MAINON (34,41,42,43,47)
R1
R2
PR168 51.1/F_4
PR165 100K/F_4
PR164 78.7K/F_4
PC137 0.1u/25V_4
PC130 10u/10V_8
PC131 10u/10V_8
V0=0.8*(R1+R2)/R2
B-Test change
VIN_SRC
+3VSUS
+15V
+3VPCU
PR43 *1M/F_6
PR103 *22_8
PR61 *1M_6
SUSON_R
PQ18 *DTC144EUA
(34,43) SUSON
PR38 *100K_4
PR40 *1M/F_6
PQ27 *DMN601K-7
PQ22 *DMN601K-7
PC32 *2200p/50V_4
PQ28 *AO3404
1.5A
+3VSUS
B-Test change
VIN_SRC
+1.5V_GFX
+1.8V_GFX
+15V
+1.8V
PR52 SW@1M/F_6
PR64 SW@22_8
PR65 SW@22_8
PR53 SW@1M_6
dGPU_D1
PQ21 SW@DMN601K-7
(44) VGA_PG
PR41 SW@0_4
PC29 SW@1u/10V_4
PR252 SW@100K_4
PR58 SW@1M/F_6
PQ23 SW@DMN601K-7
PQ25 SW@DMN601K-7
PQ24 SW@DMN601K-7
PC30 *SW@2200p/50V_4
PQ53 SW@AO3404
+1.8V_GFX
0.23A(MAX 0.3A)
+1.5V_SUS
dGPU_D1
PQ46 SW@AO4468
+1.5V_GFX
4.29A(MAX 5.72A)
VIN_SRC
+3V_GFX
+1.05V_GFX
+15V
+1.1V_VTT
PR5 SW@1M/F_6
PR8 SW@22_8
PR12 SW@22_8
PR10 SW@1M_6
dGPU_D
PQ1 SW@DTC144EUA
(11) dGPU_PWR_EN
PR4 *SW@100K_4
PR6 SW@1M/F_6
PQ4 SW@DMN601K-7
PQ7 SW@DMN601K-7
PQ6 SW@DMN601K-7
PC25 *SW@2200p/50V_4
PQ17 SW@AO4468
+1.05V_GFX
2.87A(MAX 3.83A)
+3VPCU
dGPU_D
PQ5 SW@AO3404
+3V_GFX
1.04A(MAX 1.38A)
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
(GPU_Power/1.8V)
Rev 1A
Date: Monday, March 29, 2010
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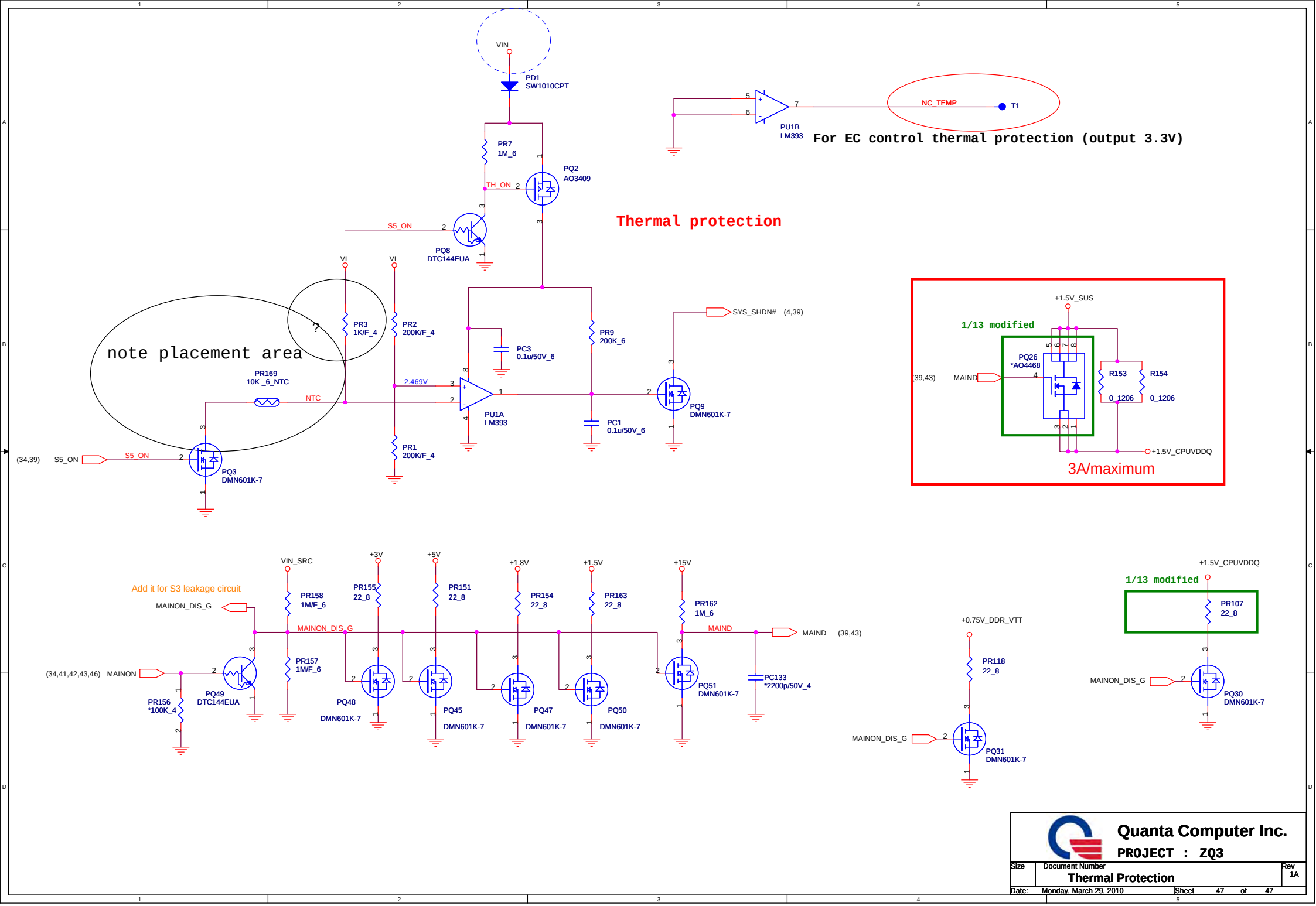

Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: Thermal Protection	Rev: 1A
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