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HSF Property:ROHS

ACER

JM31/SJM31/BAP31

Discrete

MAIN BOARD

2009.05.26

Tuesday, May 26, 2009		A03
DATE	CHANGE NO.	REV

DRAWER		EE	DATE	POWER	DATE	INVENTEC TITLE BAP31G SFF							
DESIGN													
CHECK													
RESPONSIBLE													
SIZE=						VER:		SIZE		CODE	DOC NUMBER		REV
FILE NAME: XXXXX.XXXXXX.XXX								C	CS	D-CS-1310A2264501-ALG		47	
PIN XXXXXXX000000								SHEET		1 of		47	

1. Schematic Page Description :

Montevina Schematic Ver : A03

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD CNN/SATA/3G/WLAN

32. KBC ITE8512F

33. IO CN

34. IO CN

35. IO CN

36. Audio Codec

37. BLANK

38. M92-S2(1/5)

39. M92-S2(2/5)

40. M92-S2(3/5)

41. M92-S2(4/5)

42. M92-S2(5/5)

43. DDR3 VRAM

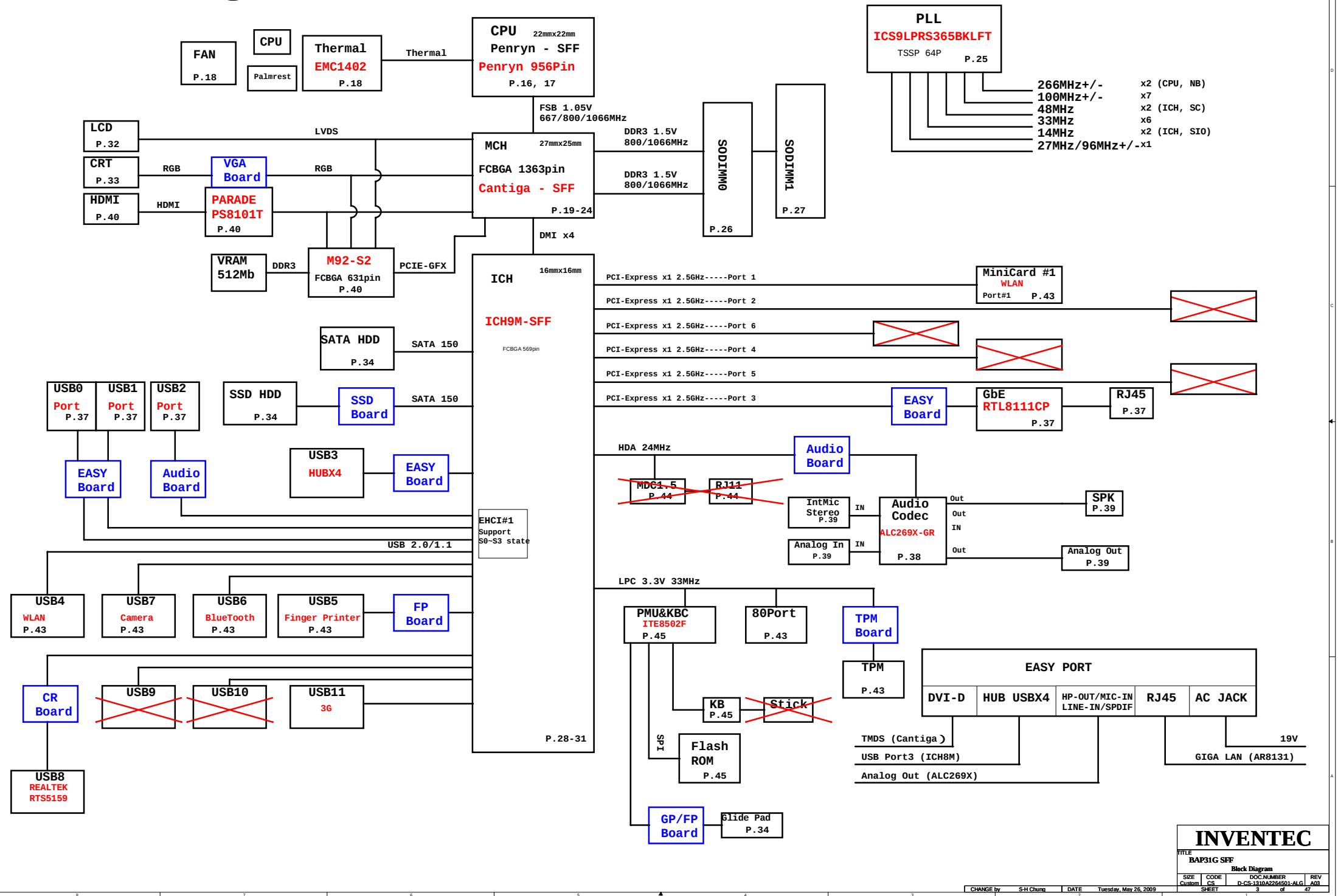
44. HyBrid Switch

45. dGPU Power

46. dGPU Power

47. dGPU Power

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V~1.4375V~1.4591V 0.9221V~0.9625V~0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+HIMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V~1.05V~1.10V 0.997V~1.05V~1.102V 0.9975V~1.05V~1.1025V 0.9975V~1.05V~1.1025V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.71V~1.8V~1.89V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TVDAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLF Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V 3.0V~3.3V~3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V~3.3V~3.6V 3.0V~3.3V~3.6V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

INVENTEC

TITLE

BAP31G SFF

ANNOTATIONS

SIZE

Custom

CODE

CS

DOCNUMBER

D-CS-1310A2264501-ALG_A03

REV

A03

SHEET

4

of

47

CHANGE byS-H ChungDATETuesday, May 26, 2009

6.Schematic modify Item and History :

- 2009.0108
- 1. ADD USB P3 for Docking, USB P5 for Finger printer, Modify CN5 -----P28
 - 2. Modify CN20 to 50pin-----P33
 - 3. Move PWR_SWIN# from CN14 to CN20
 - 4. ADD TPM module-----P34

- 2009.0109
- 1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33

- 2009.0112
- 1. Change power item: R490,R291,BAT CNN TH PIN

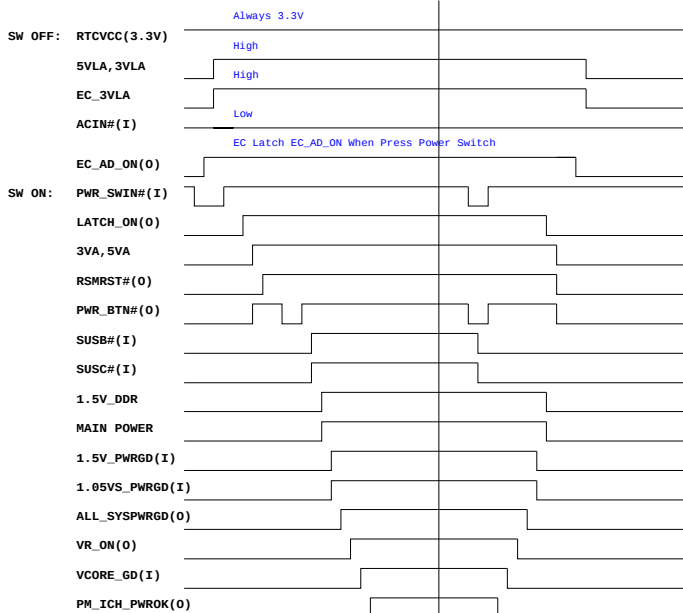
INVENTEC			
TITLE BAP31G SFF			
Schematic Modify			
SIZE Custom	CODE CS	DOCNUMBER D-CS-1310A2264501-ALG	REV A03
CHANGE by S-H Chung		DATE Tuesday, May 26, 2009	SHEET 5 of 47

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

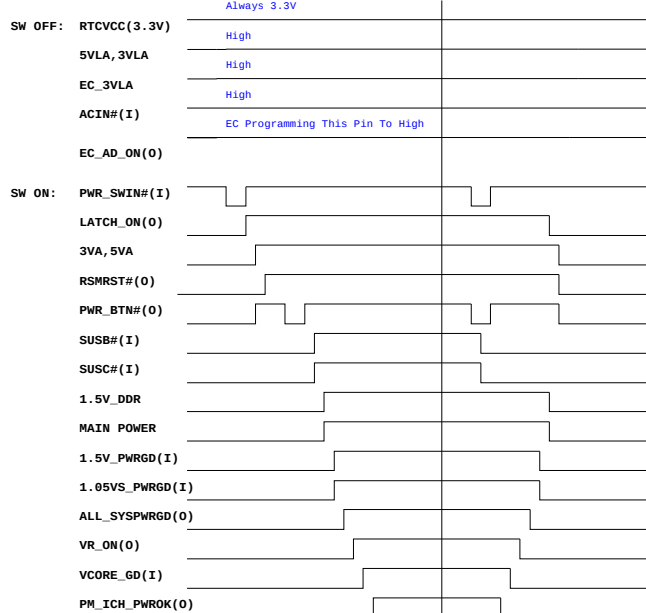
Power on/off sequence AC insert (without Battery Pack)

Power on sequence Power off sequence



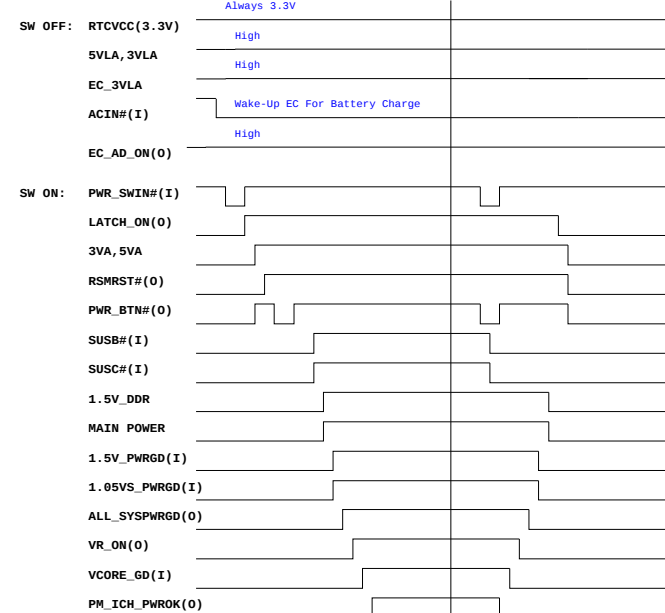
Power on/off sequence Battery insert (without AC adapter)

Power on sequence Power off sequence



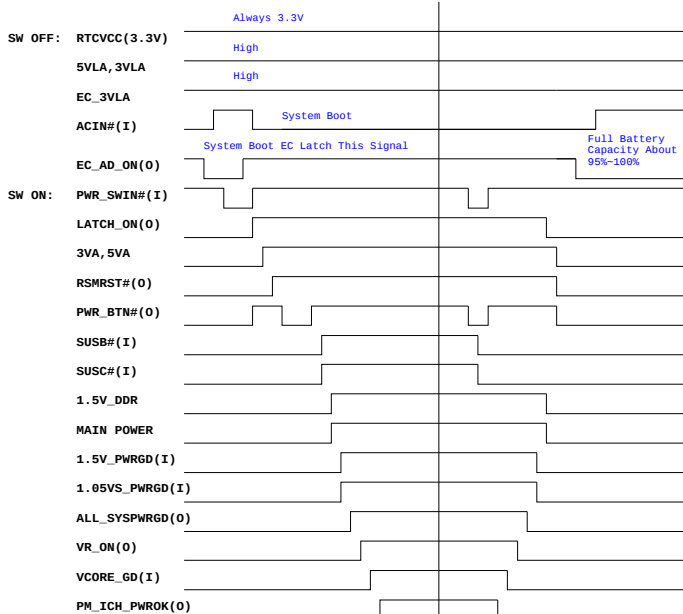
Power on/off sequence AC insert(with charge over 95%)

Power on sequence Power off sequence



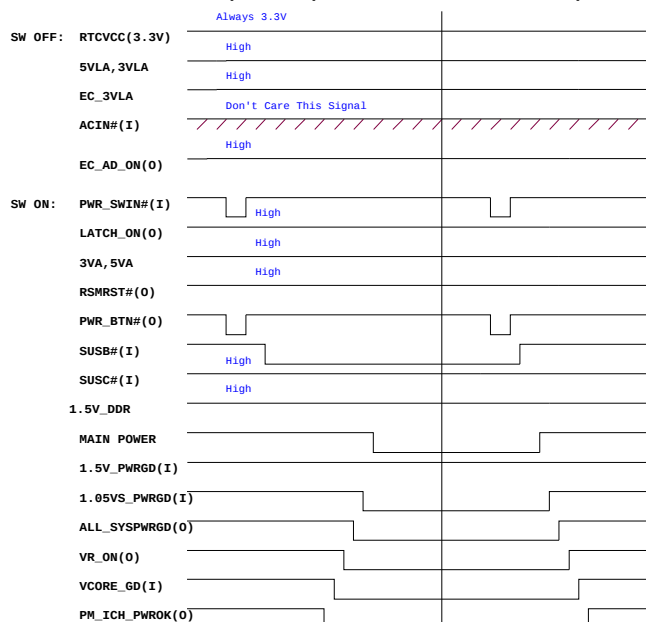
Power on/off sequence AC insert(without charge over 95%)

Power on sequence Power off sequence



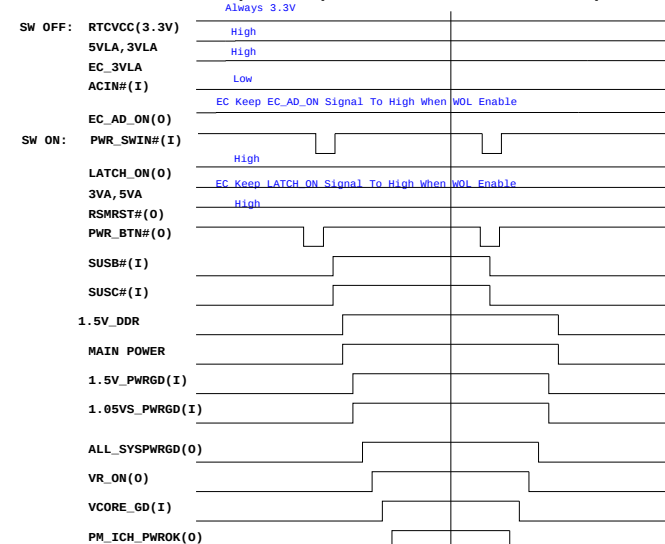
Suspend And Resume Sequence (S3)

Suspend sequence Resume sequence



Power on/off sequence after windows shoutdown (WOL enable)

Suspend sequence Resume sequence



INVENTEC

TITLE
BAP31G SFF

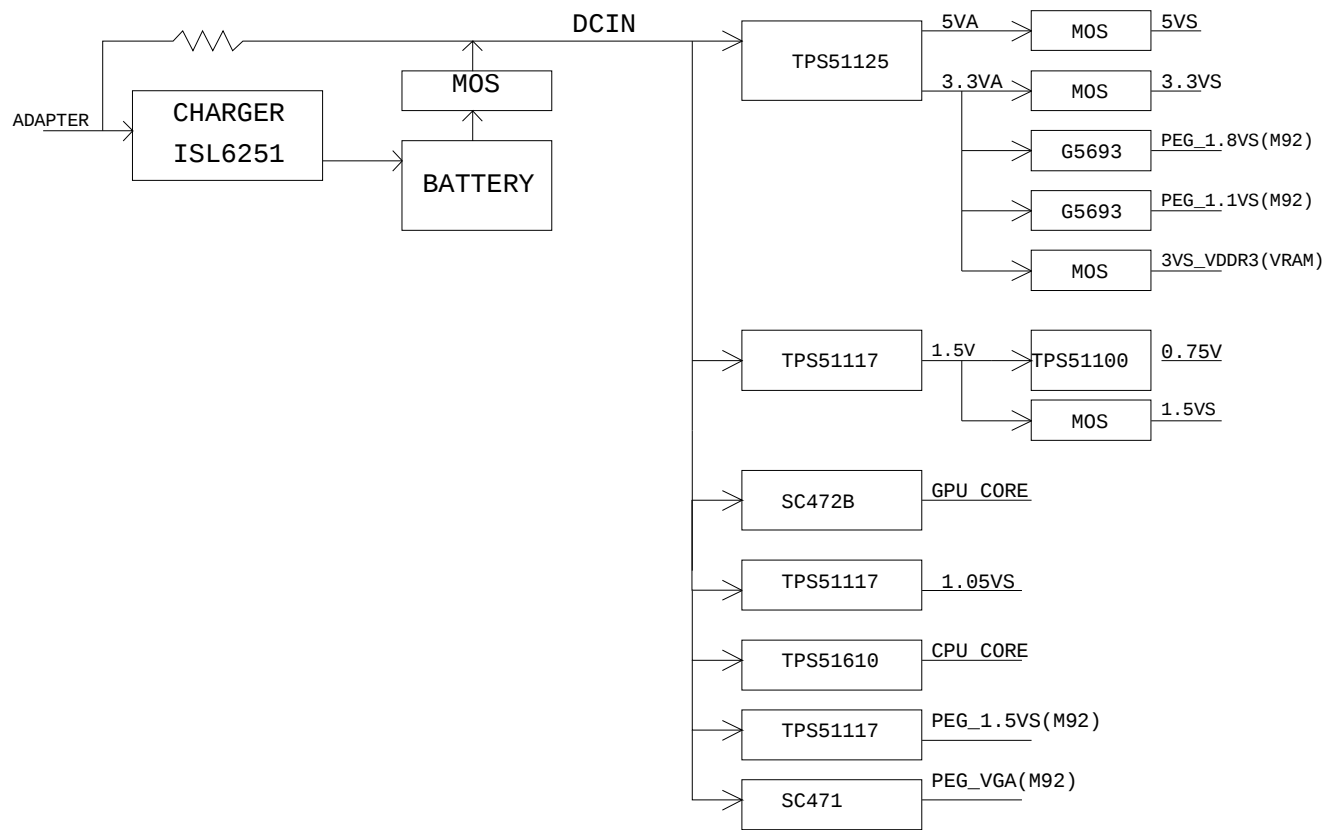
Time Diagram

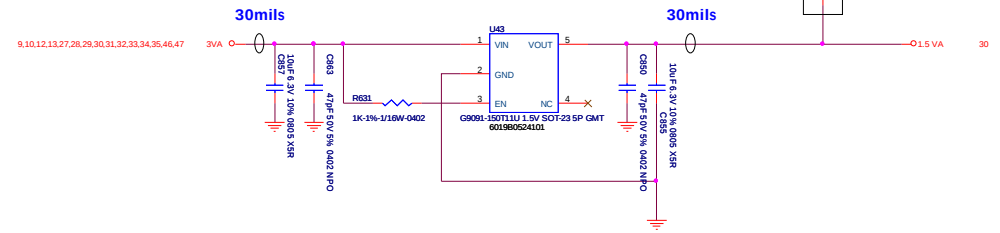
SIDE CODE DOC NUMBER REV

Custom CS D-CS-1310A226501-ALG 47

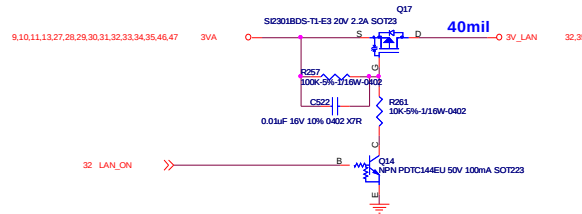
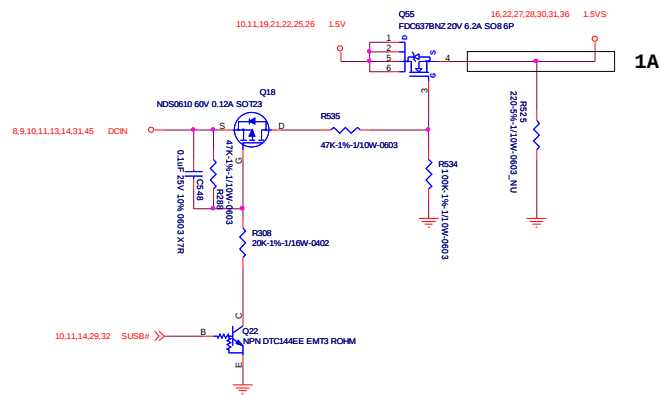
CHANGE by S-H Chung DATE Tuesday, May 26, 2009 SHEET 6 of 47

Power Block Diagram :

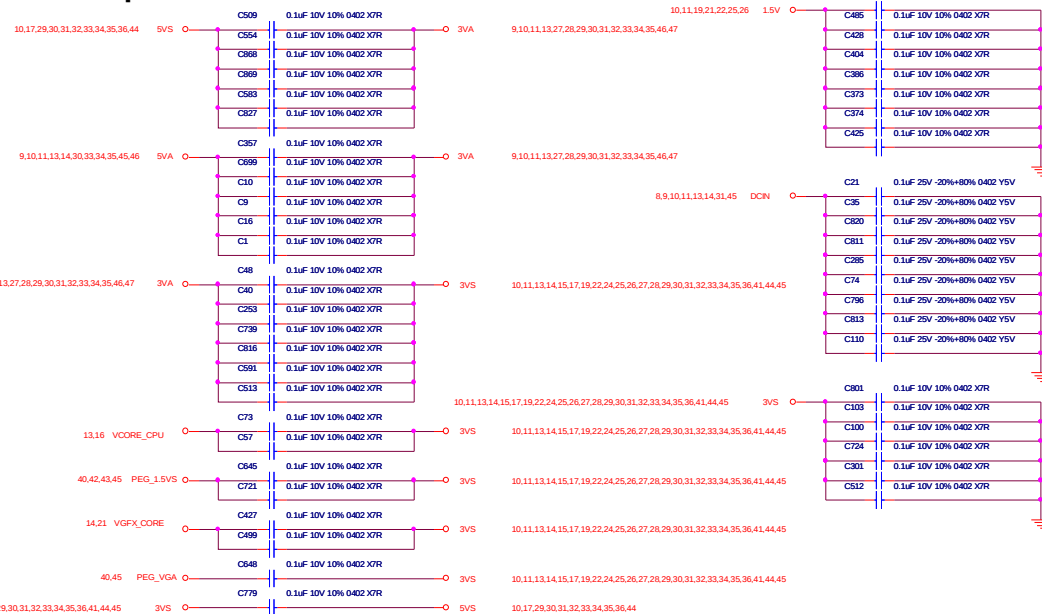




1.5VS

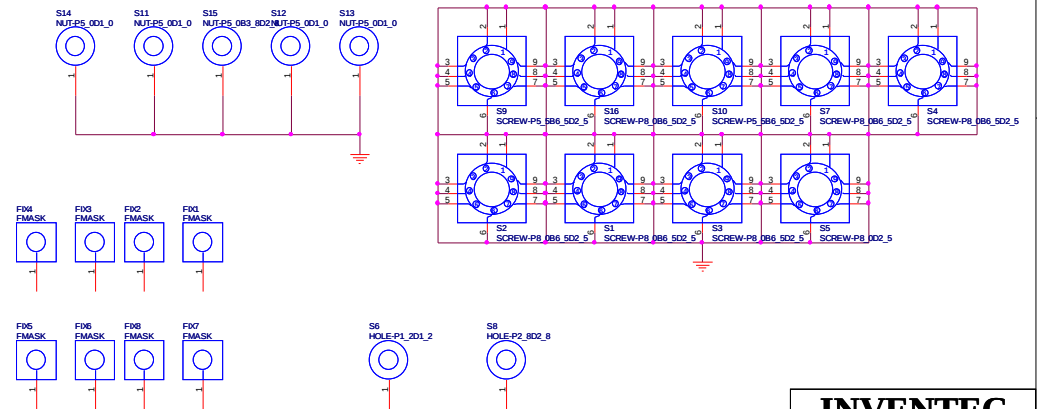
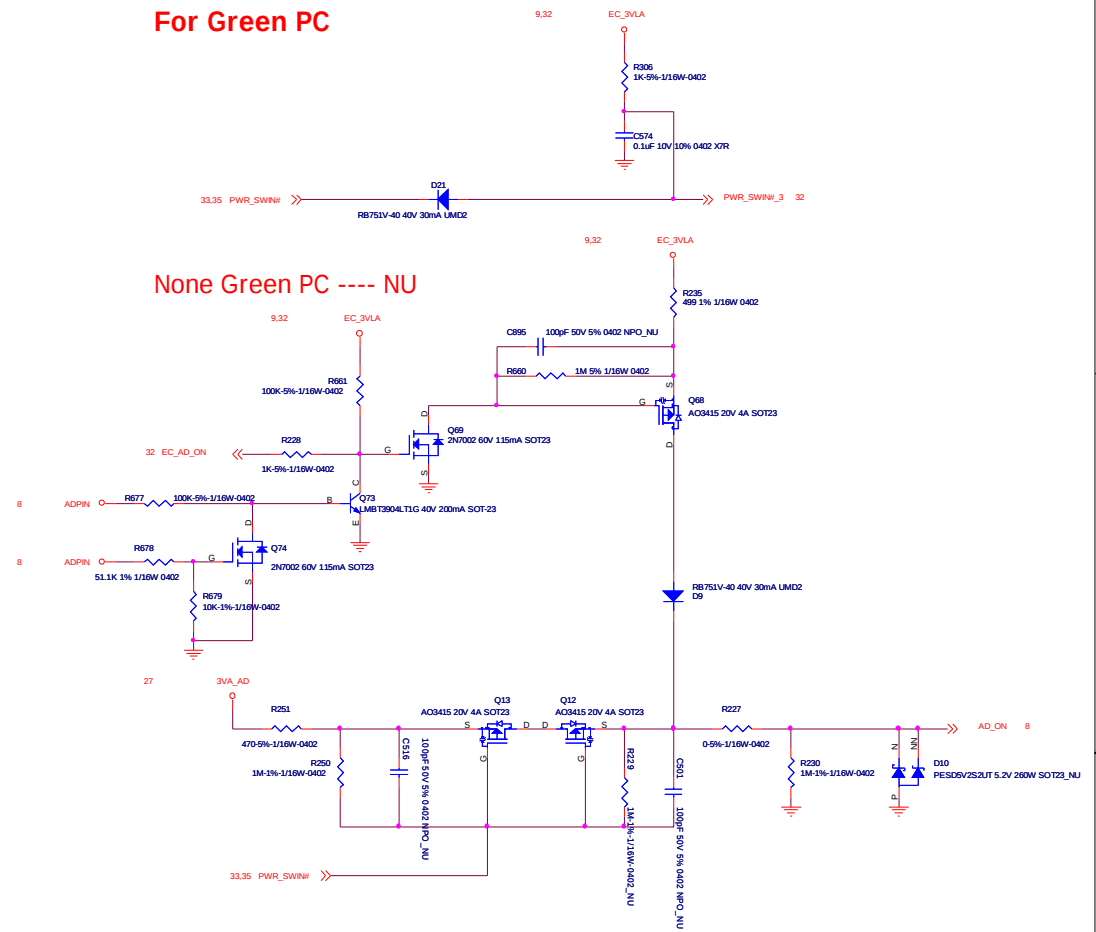


EMI Cap

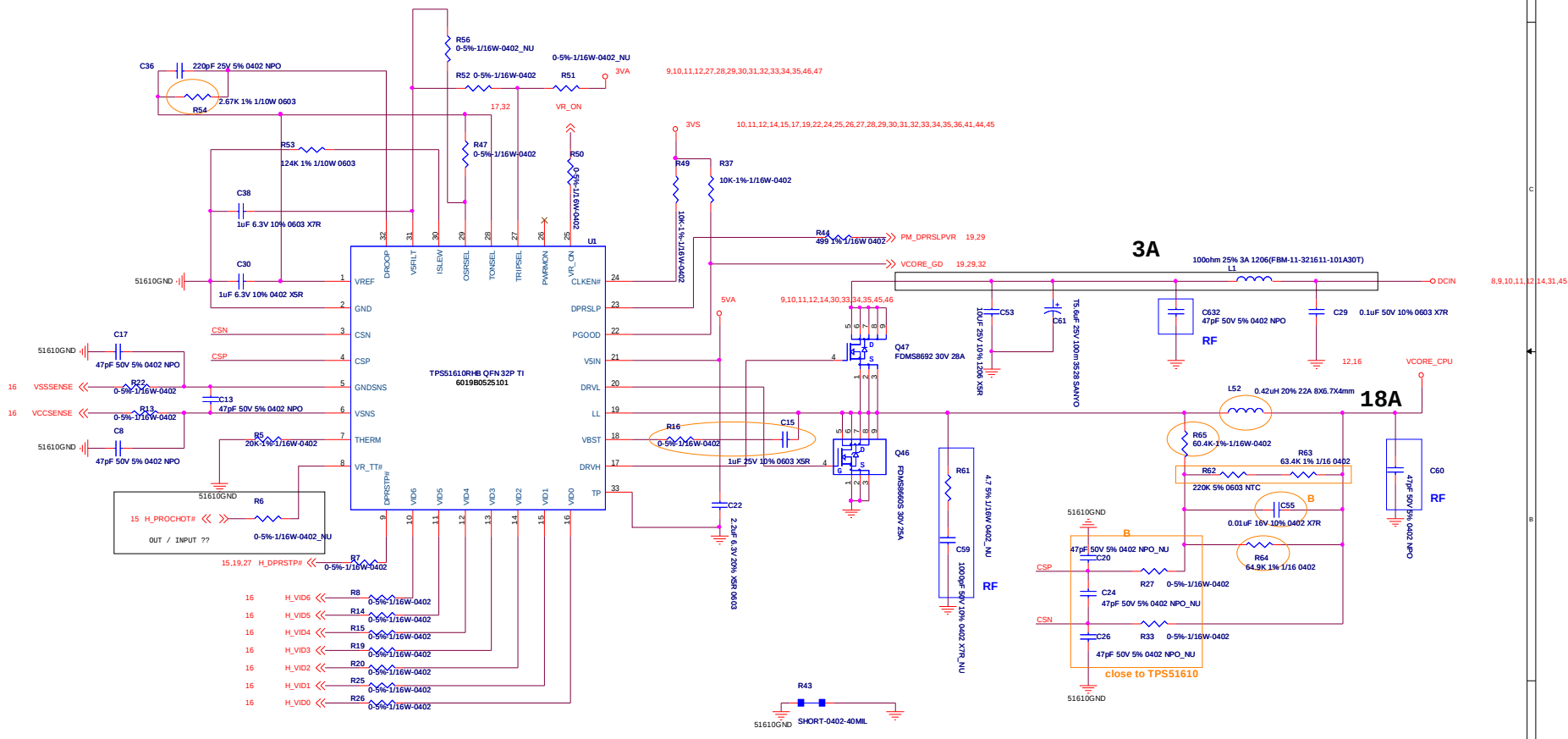


For Green PC

None Green PC ---- NU



INVENTEC				
TITLE: BAP31G SFF				
Power on latch				
SDE: Custom	CODE: CS	DOC:NUMBER: D-CS-1310A226-S01-ALG	REV: A00	
CHANGE by: S-H Chung		DATE: Tuesday, May 26, 2009		SHEET: 12 of 47



INVENTEC

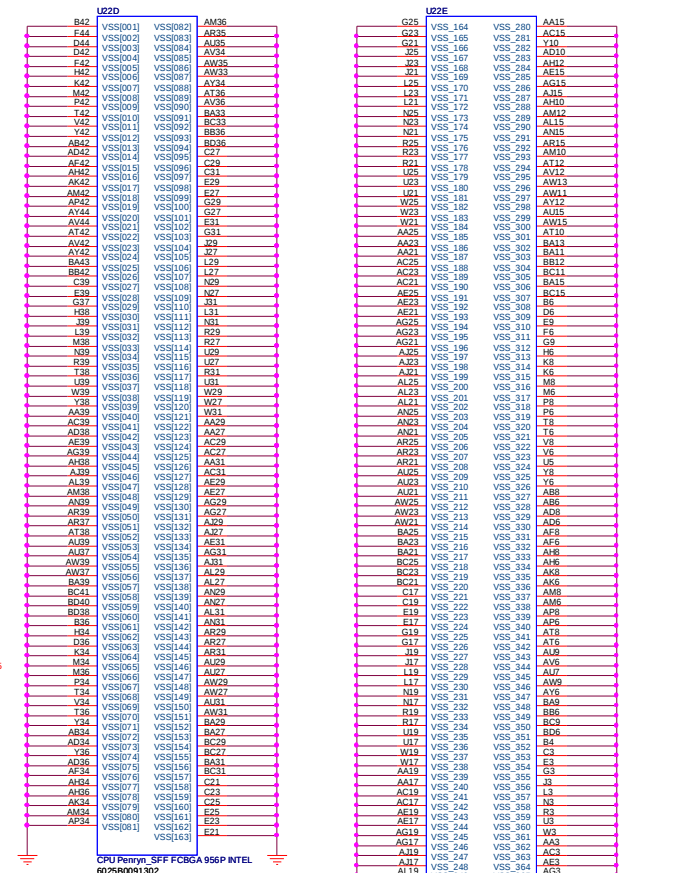
FILE
BAP31G SFF

CPU Core Power

SHEET	CODE	DOC NUMBER	REV
C	CS	D-CS-1310A2264501-ALG	A03

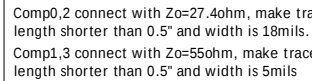
CHANGE by S-H Chung DATE Tuesday, May 26, 2009

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XDP P/U & P/D

Signal	Pin	Function	Supply
XDP_DBRESET#	R88	1K-5% 1/16W-0402	3VS
XDP_TDO	R418	54.9-1% 1/16W-0402, NJ	1.05VS_CPU
XDP_TMS	R89	54.9-1% 1/16W-0402	
XDP_TCK	R374	54.9-1% 1/16W-0402	
XDP_BPMIS	R419	54.9-1% 1/16W-0402	
XDP_TRST#	R373	54.9-1% 1/16W-0402	
XDP_TCK	R405	54.9-1% 1/16W-0402	



H_PWRGD rise time :
Max : 15ns

Power-up peak current : 4.5A (max)
Steady-state current : 2.5A (max)



10mil

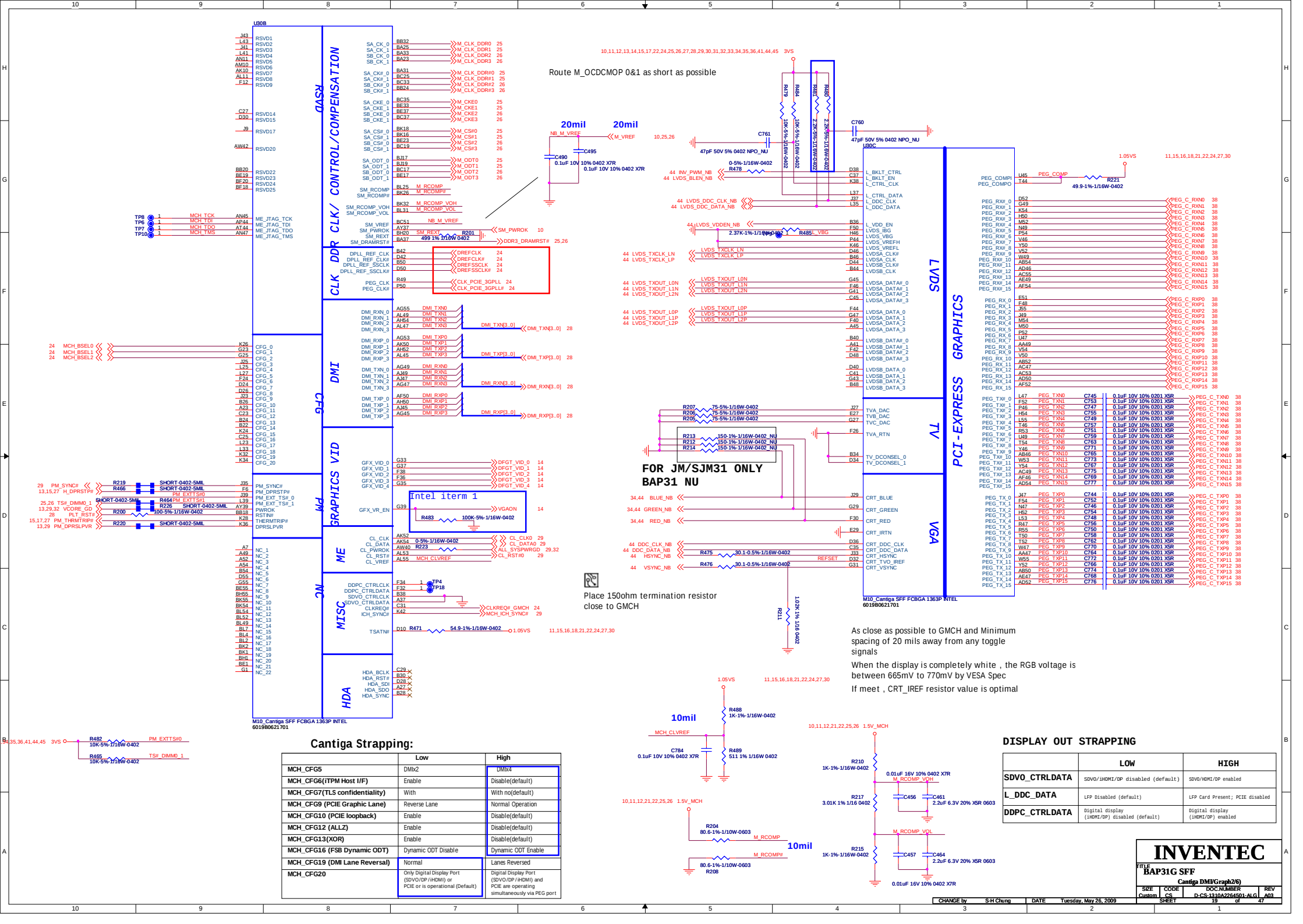
10 mil

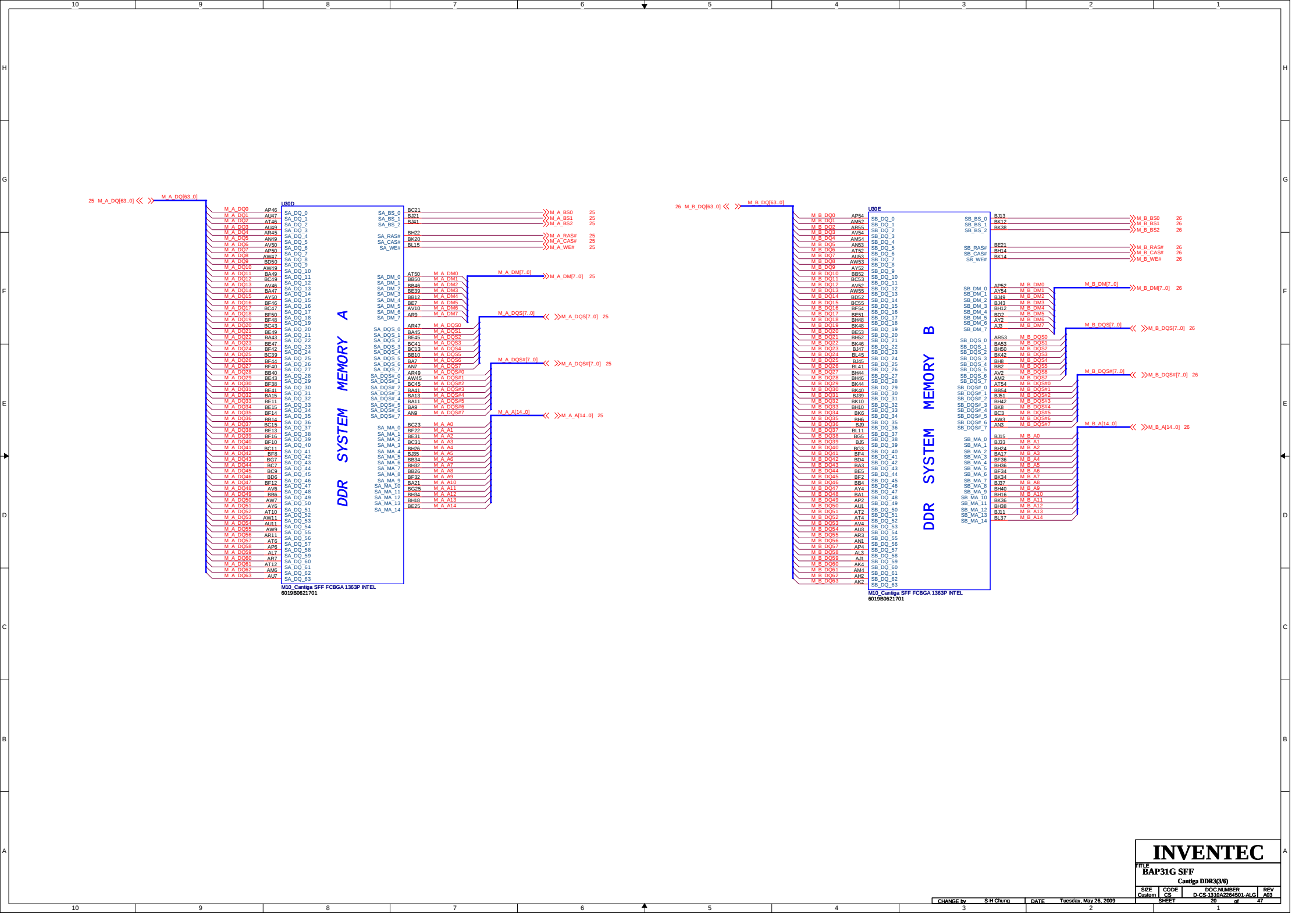
10 mil

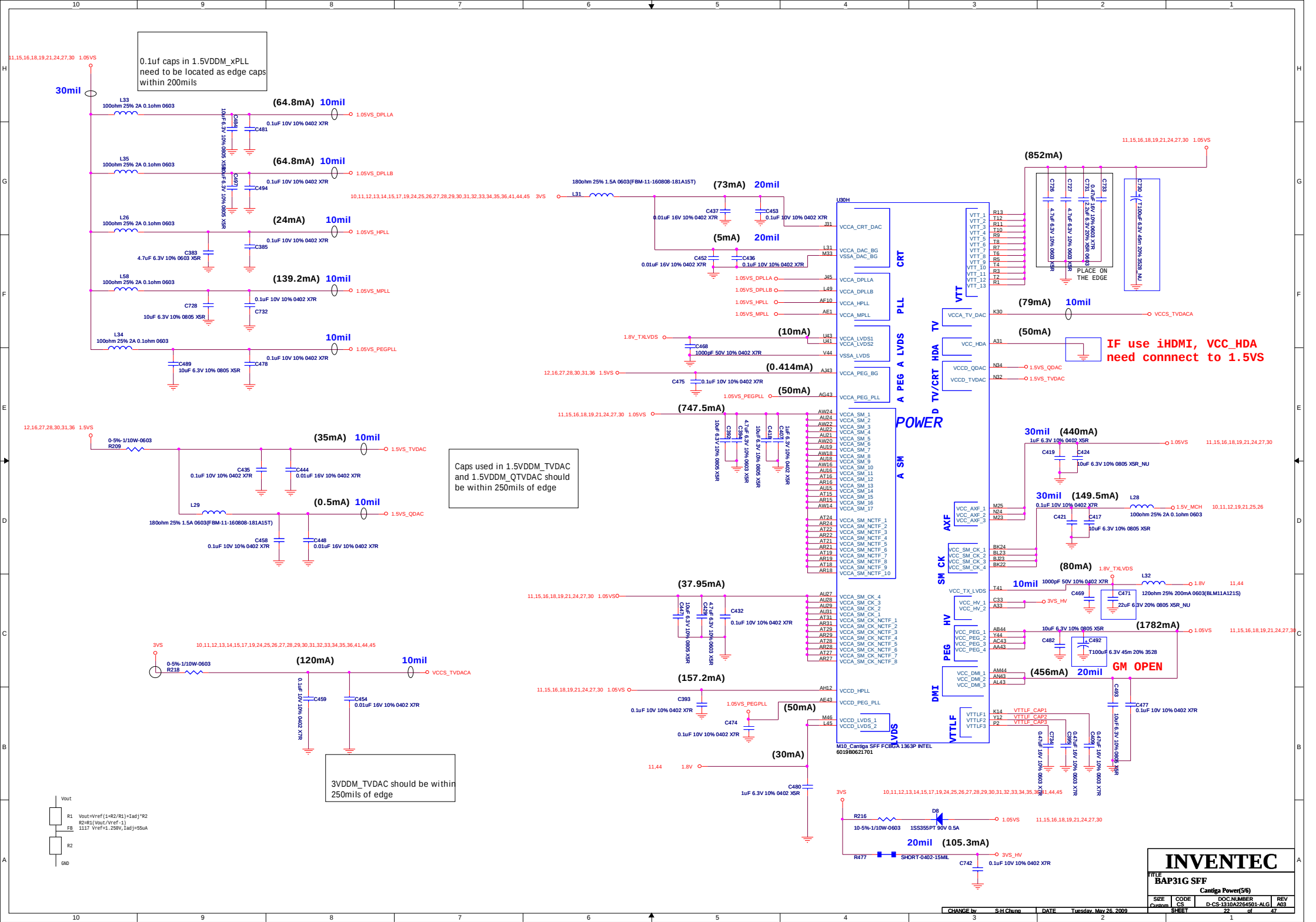
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CPU Thermal			
SIZE	CODE	DOC. NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET		17	of 47

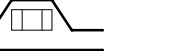
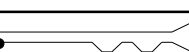
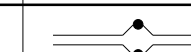
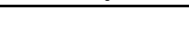
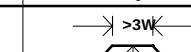
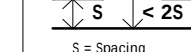
CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009
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Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Diferential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

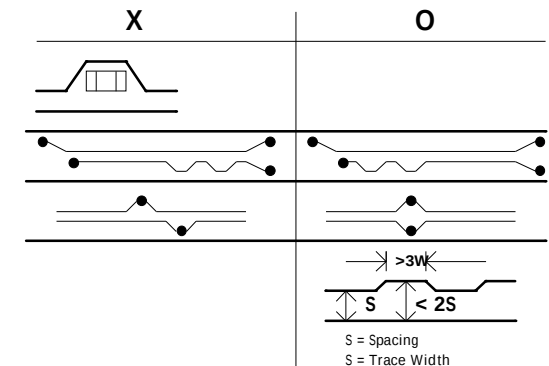
X	O
	
	
	
	
	 $\text{S} = \text{Spacing}$ $\text{S} = \text{Trace Width}$

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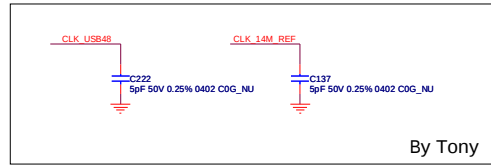
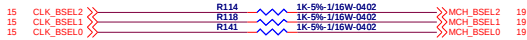
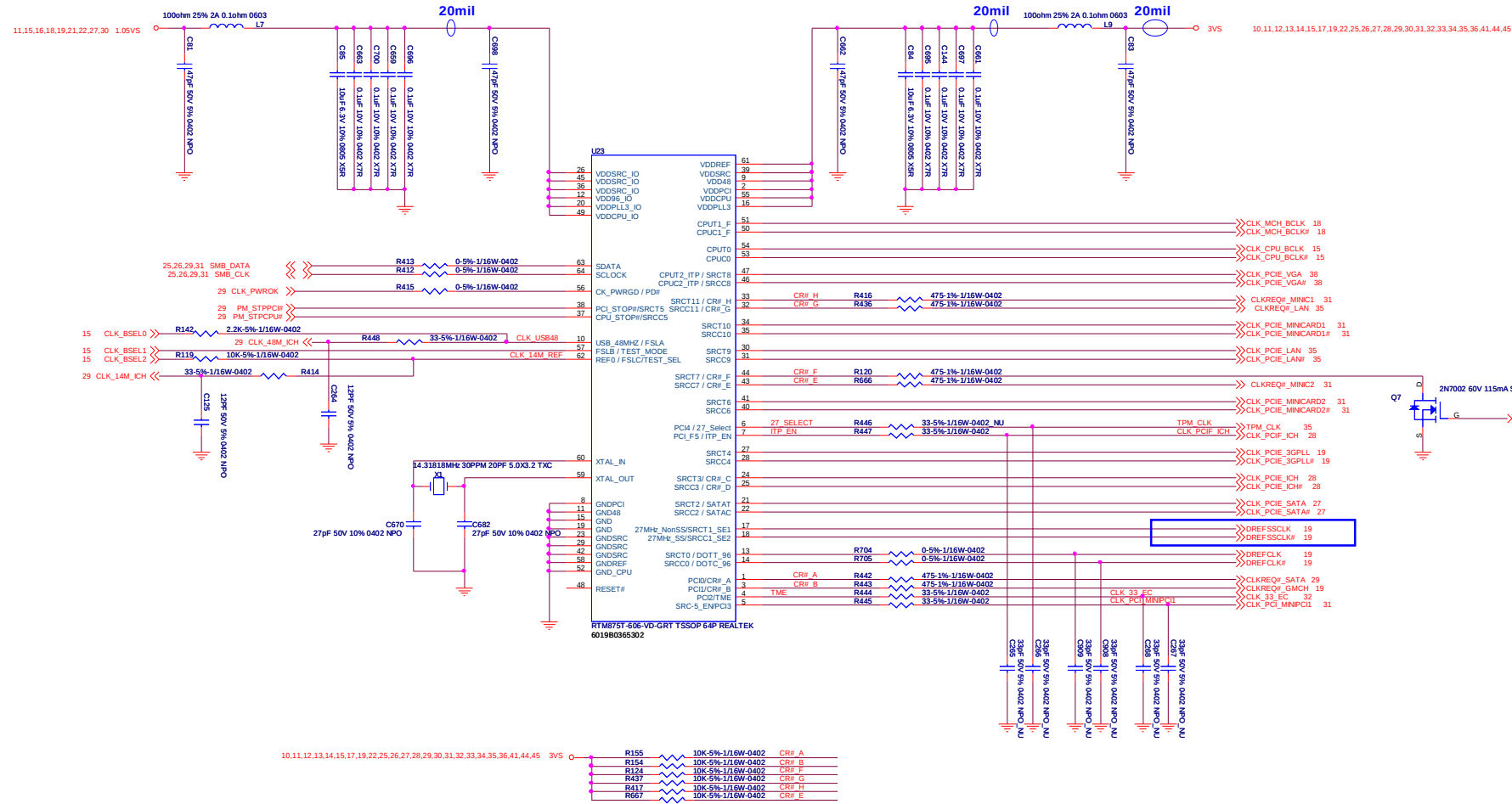
graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ExpressMiniCard [Express/Mini Card]
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA[LA]
    LA --- LB[LB]
    LB --- LC[LC]
    LC --- Rx2
    Rx1 --- LZ[LZ]
    LZ --- LY[LY]
    LY --- Tx2
    style LB stroke-dasharray: 5 5
    style LC stroke-dasharray: 5 5
  
```

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane

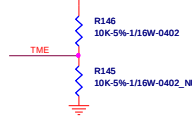
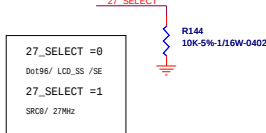
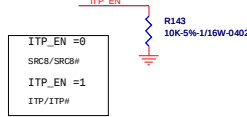
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



TITLE			
BAP31G SFF			
Contiga Ground(6/6)			
SIZE	CODE	DOC. NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET		23	of 47



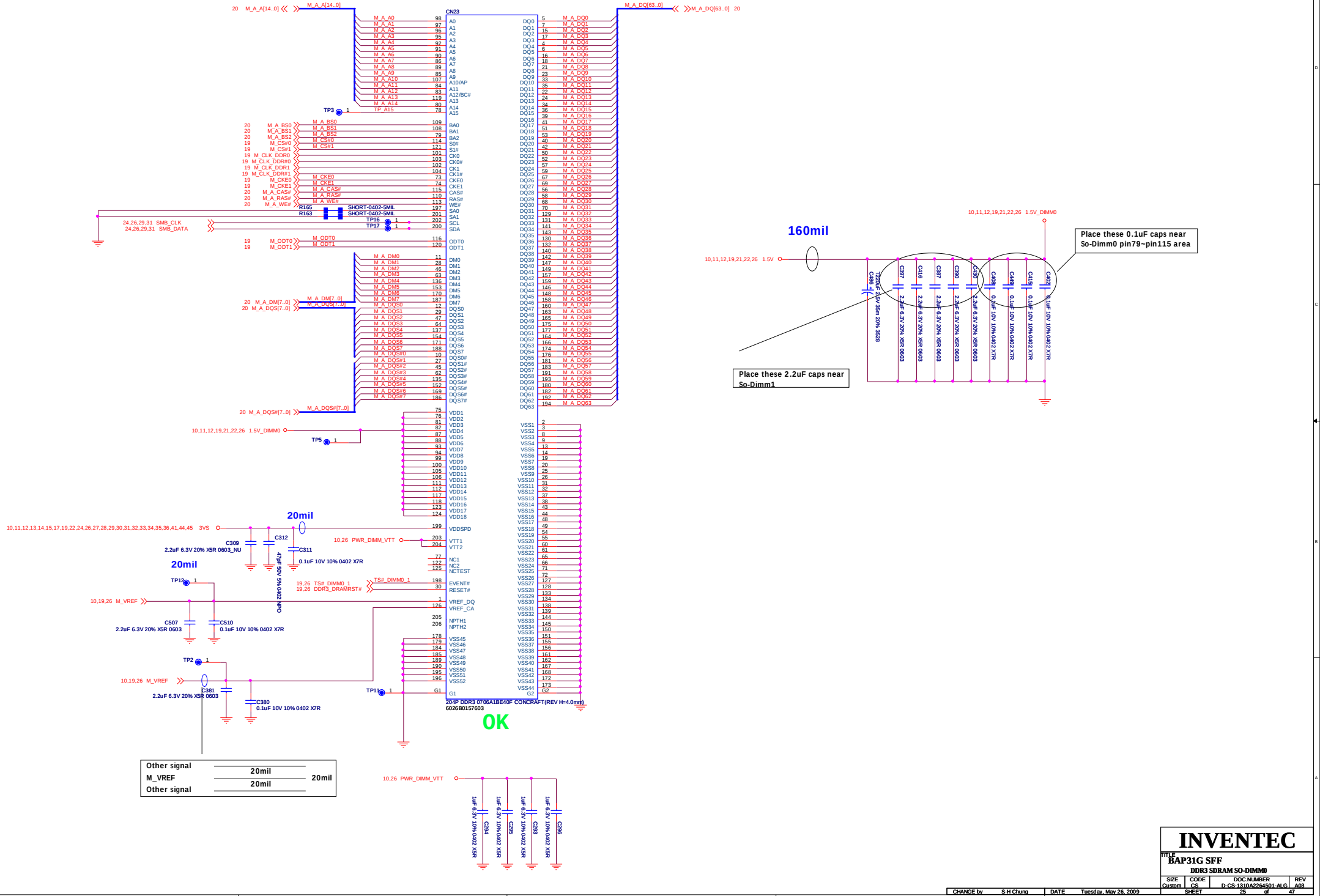
FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200
0	0	0	1067	266 *



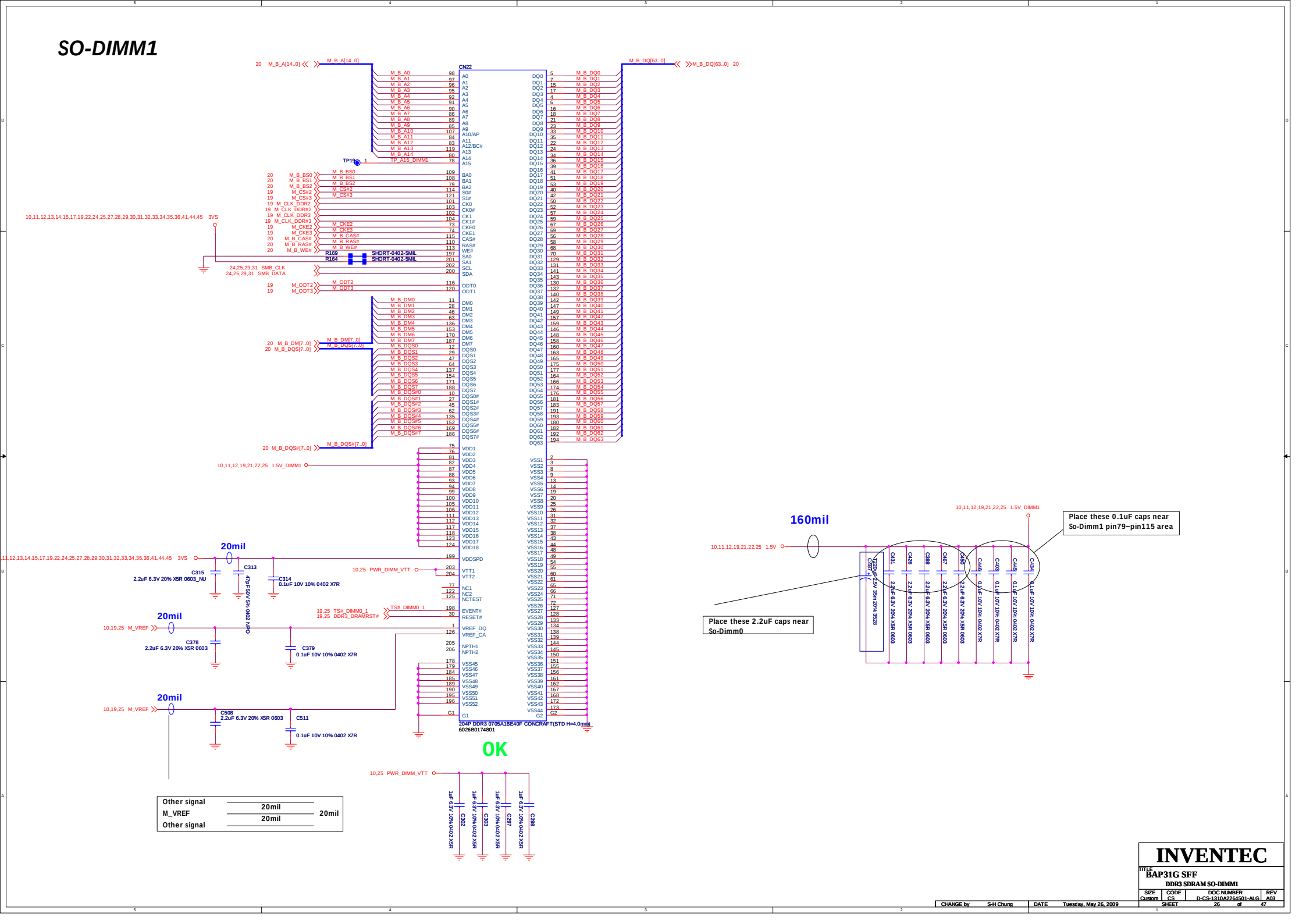
CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

INVENTEC			
BAP31G SFF			
Clock Generator			
SIZE	CODE	DOCNUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG_A03	01
SHEET		24 of 47	

SO-DIMMO



SO-DIMM1



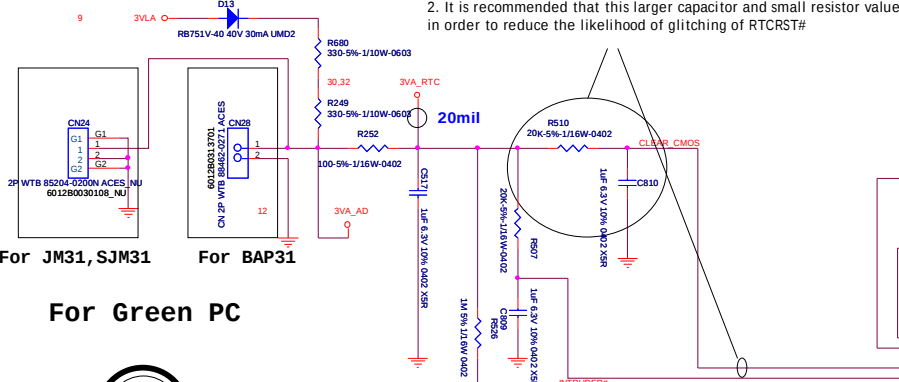
INVENTEC

BAP31G SFF

DDR3 SDRAM SO-DIMM1

RTC Circuit

- 1. RC delay time should be in the range of 18-25ms
- 2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#



For JM31, SJM31

For Green PC

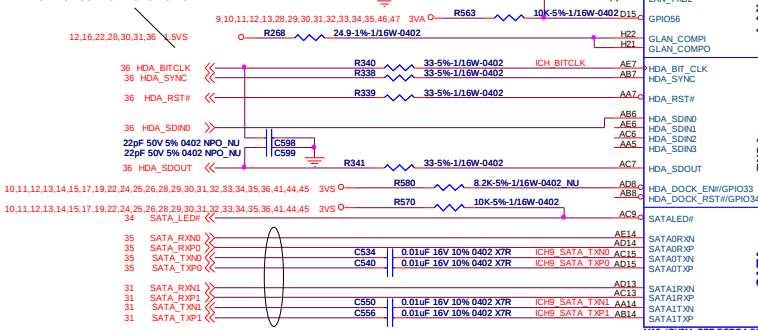


CABLE, ROUND, 3POS, 75mm, I, RTC_NU
6027B0066801

RTC Battery Life :
220mAh (220000uAh) / 6uA = 4.2 year

- 1. The ICHm requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
- 2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
- 3. On FR-4, a 5-mils trace has approximately 2pF per inch
- 4. Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
- 5. Ground coupling plane is highly recommended

Place all series resistors 0.6 to 2.6 inches from the ICH9



Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

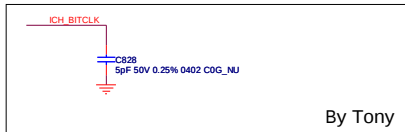
Internal VRM enabled for
VccSus1_05, VccSus1_5,
VccCL1_5, VccLAN1_05 and
VccCL1_05

ACZ_SDATAOUT strap functionality base on RSV09 strap
XOR chain entrance (RSV09 pulled low)
PCIe port config bit 1(RSV09 not pulled low)

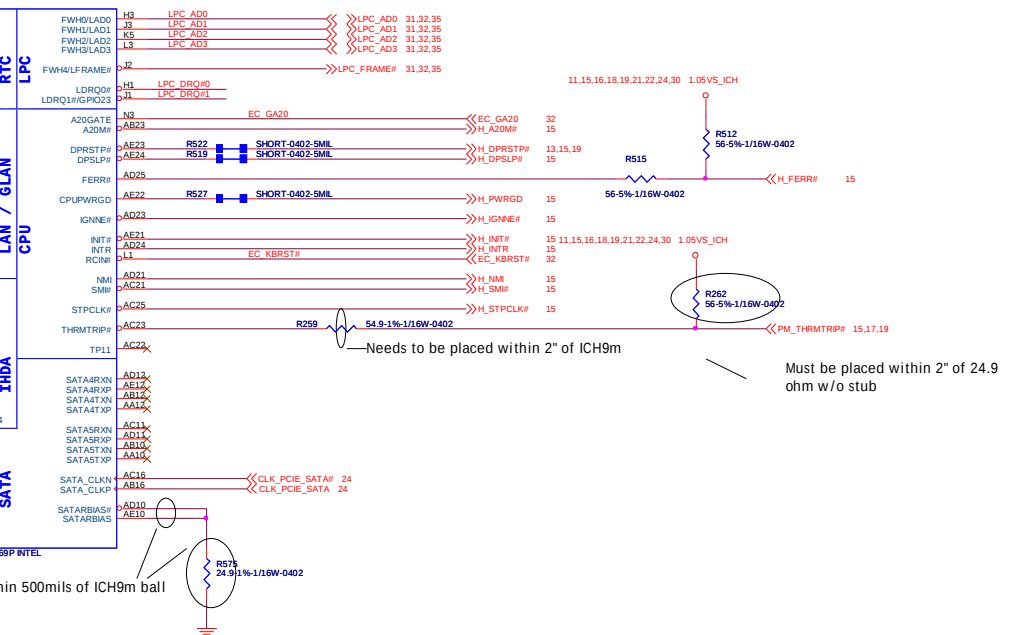
Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated	
ICH_TP3	RSV0
0	1
1	0
2	0
3	1

Short pins AG1 and AG2 at the package



By Tony



Must be placed within 2" of 24.9 ohm w/o stub

INVENTEC

BAP31G SFF

ICH9M CPU/IDE/SATA(I/O)

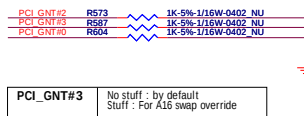
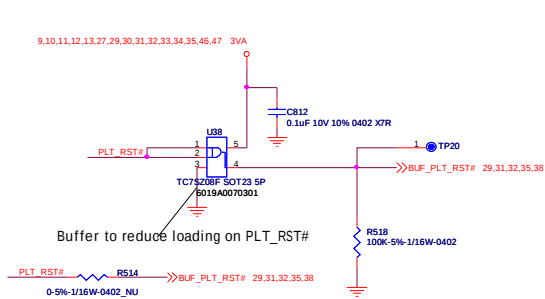
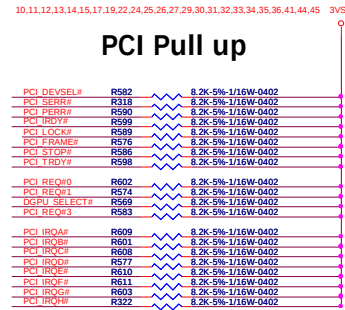
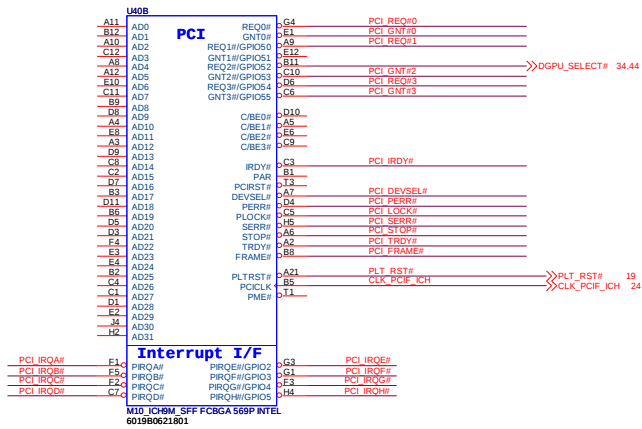
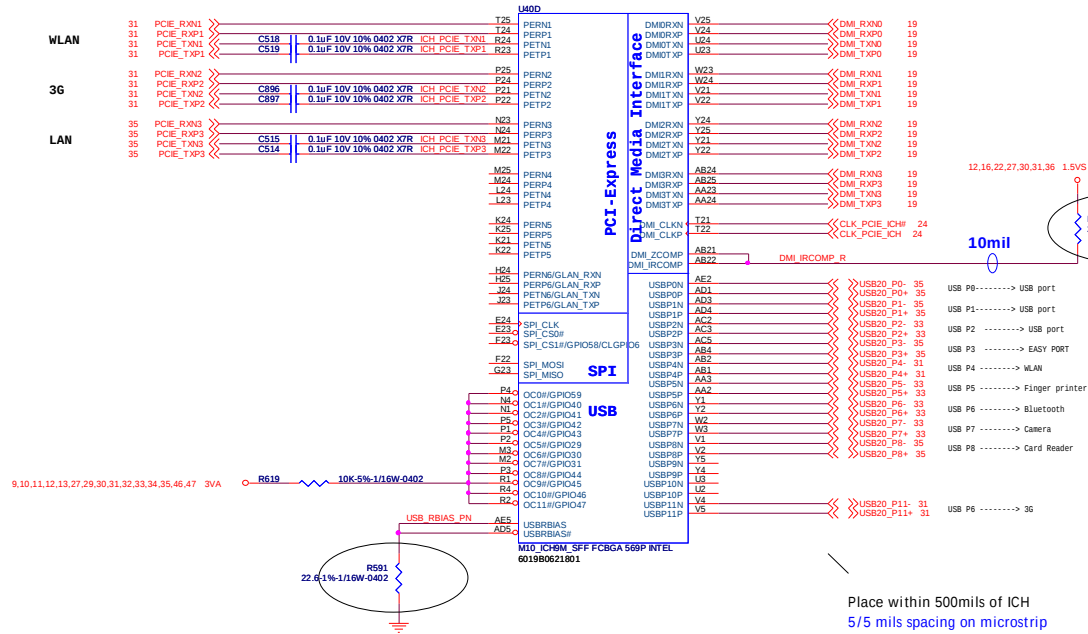
SIZE CODE DOC NUMBER REV

Custom CS D-CS-1310A2264501-ALG A03

CHANGE by S.H.Chung DATE Tuesday, May 26, 2009

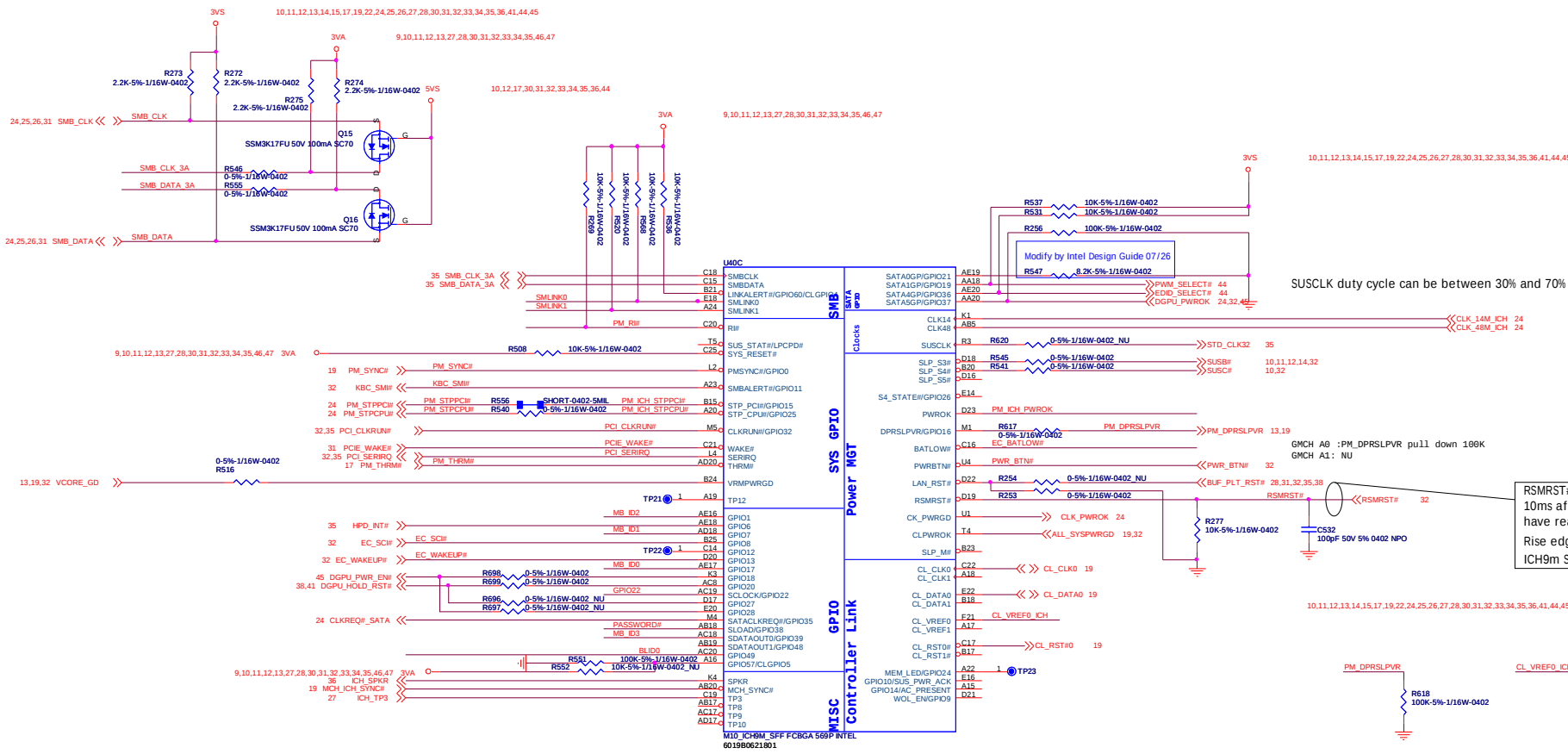
SHEET 27 of 47

PCIE AC coupling caps need to be within 250mils of the driver

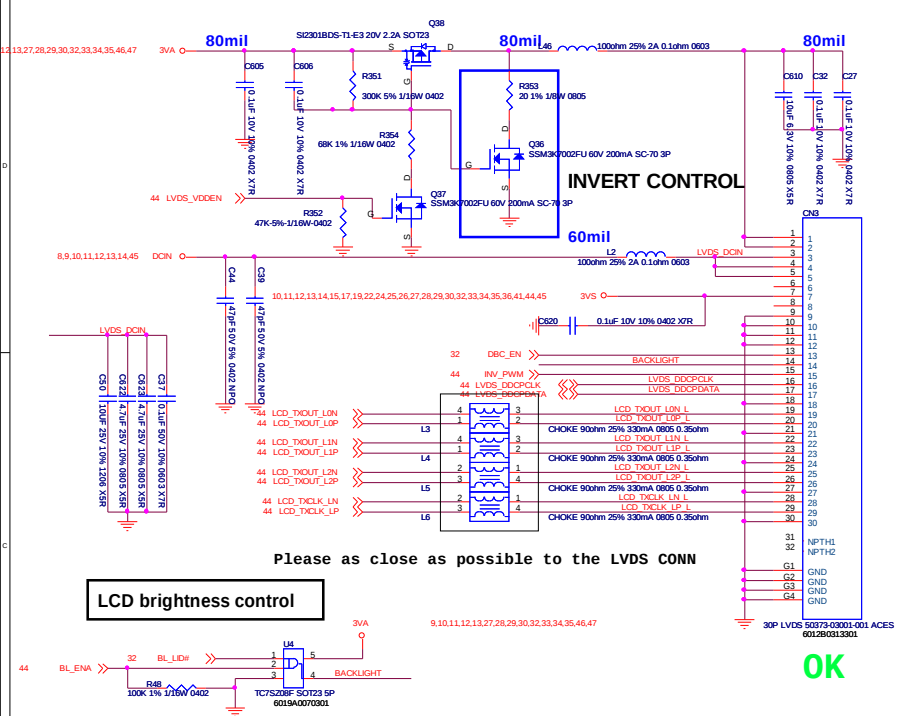


PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type



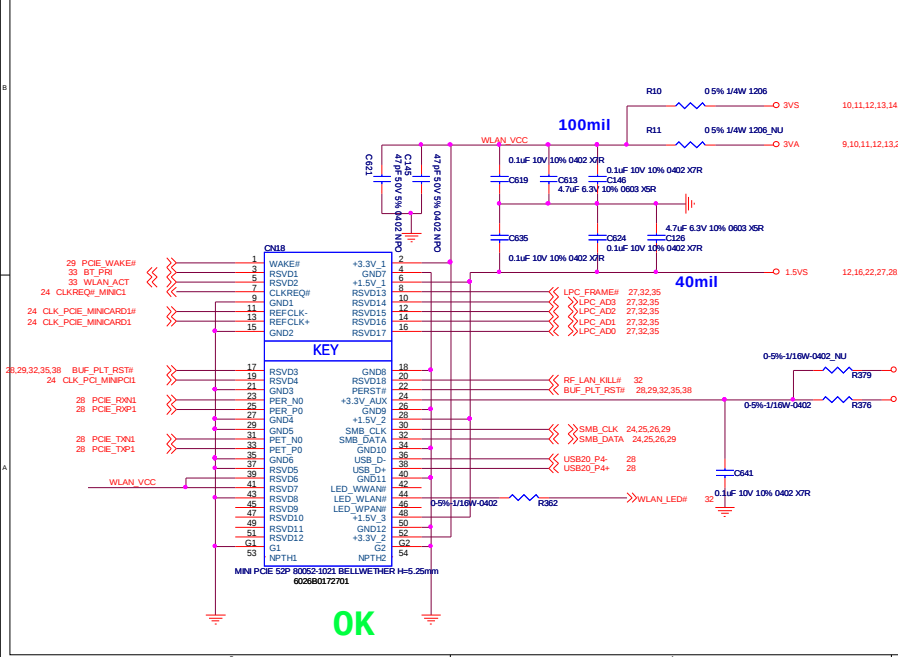
LVDS Interface



Please as close as possible to the LVDS CONN

LCD brightness control

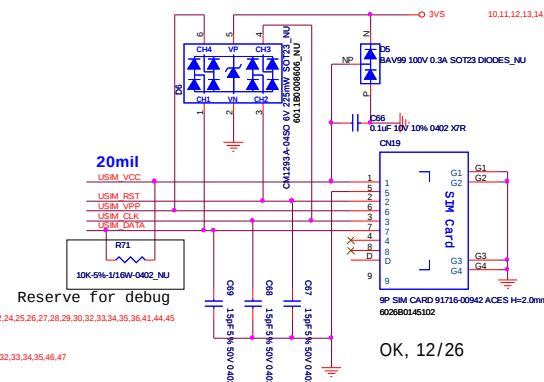
PCIE Mini Card(WLAN)



OK

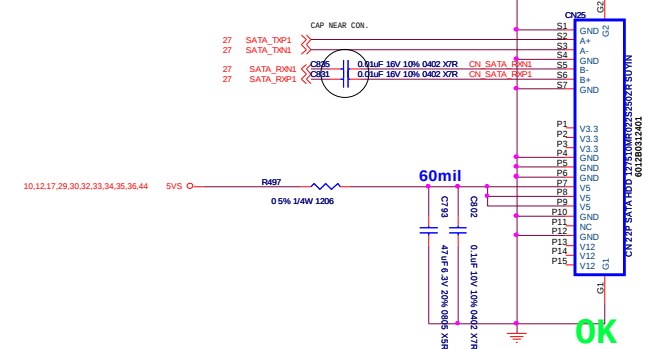
SIM CARD slot

On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.



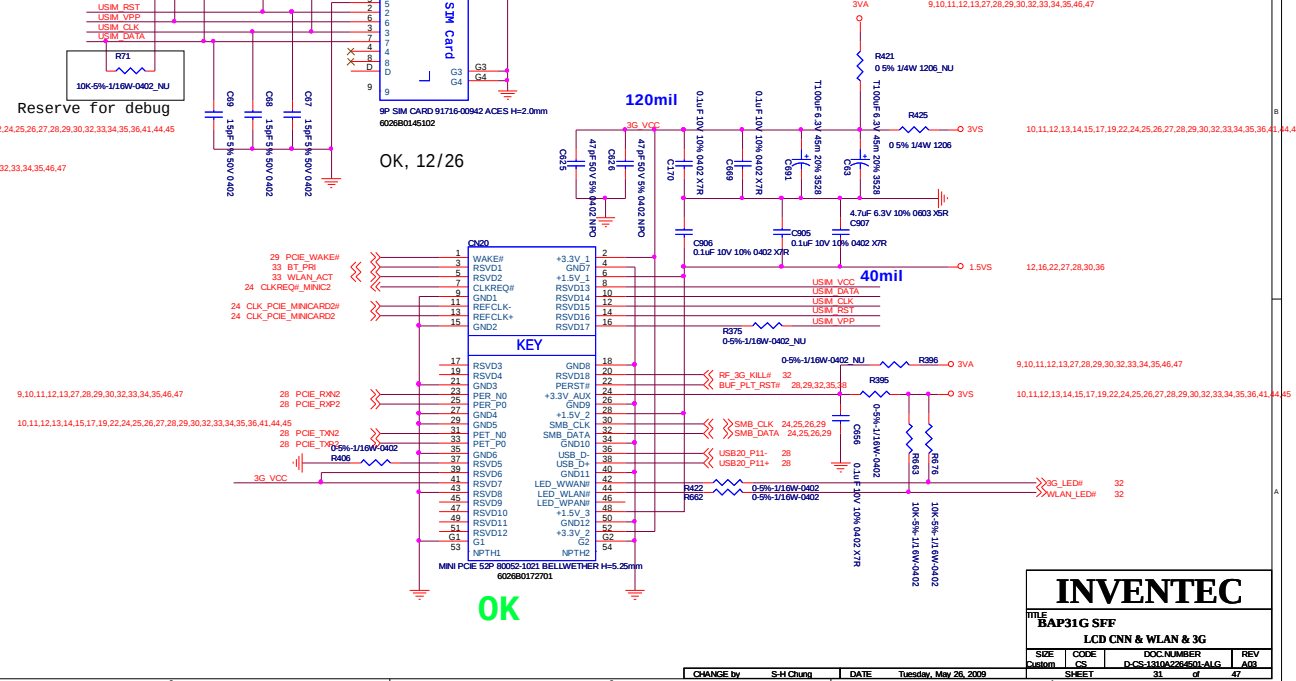
OK, 12/26

HDD I/F



OK

PCIE Mini Card for 3G

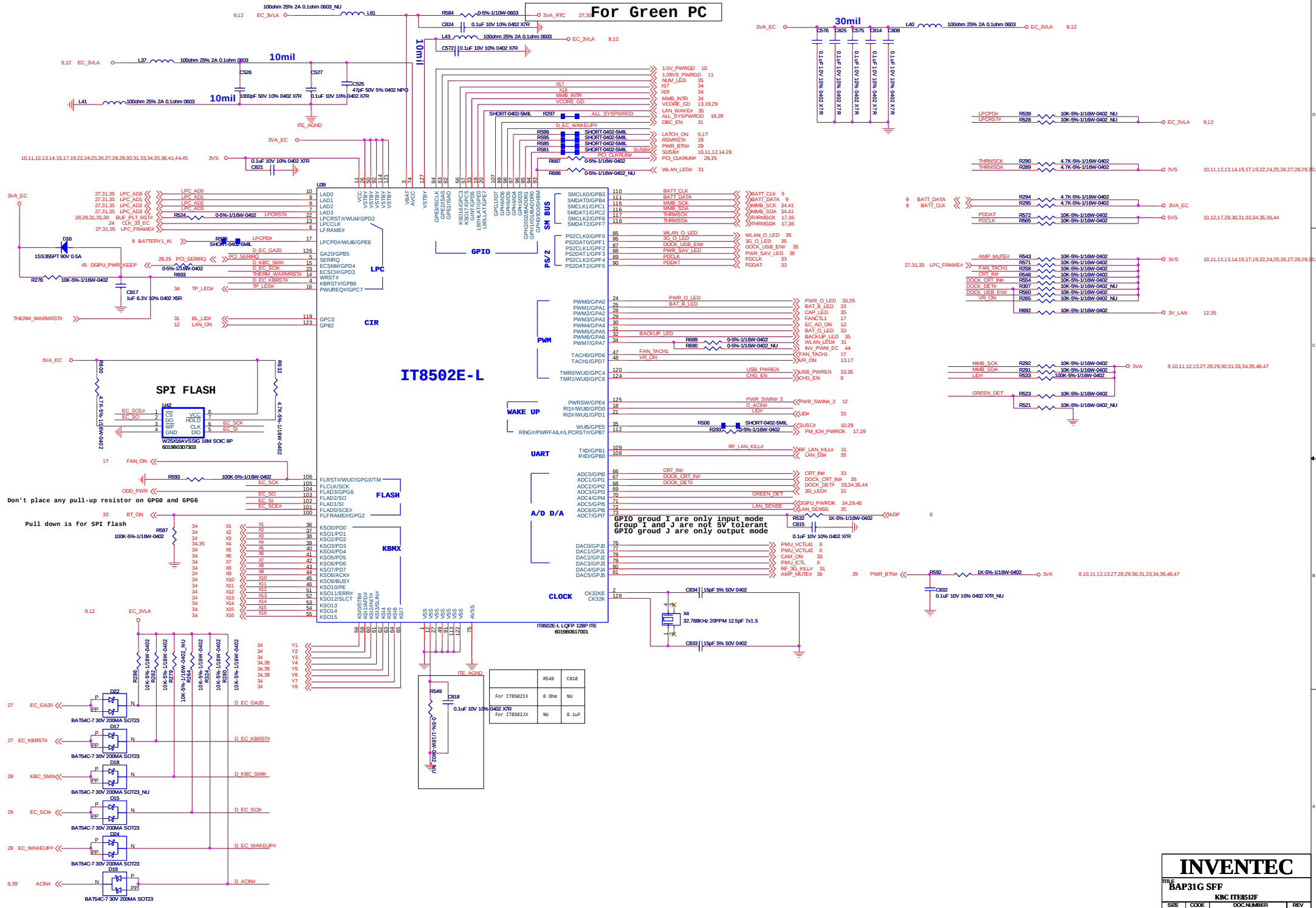


OK

INVENTEC

TITLE			
BAP31G SFF			
LCD CNN & WLAN & 3G			
SIZE	CODE	DOC. NUMBER	REV
Custom	CS	D-CS-1310A226-501-ALG	A03
SHEET		31	of 47

For Green PC



INVENTEC

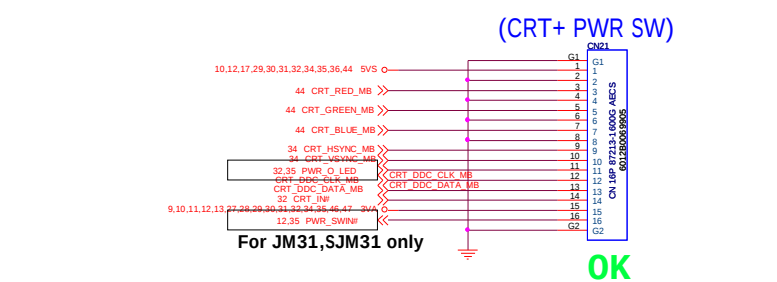
TITLE: BAP31G SFF
KBC IT8502F

SIDE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-3310A228501-ALG	A00

CHANGE by: S-H Chung DATE: Tuesday, May 26, 2009 SHEET: 32 of 47

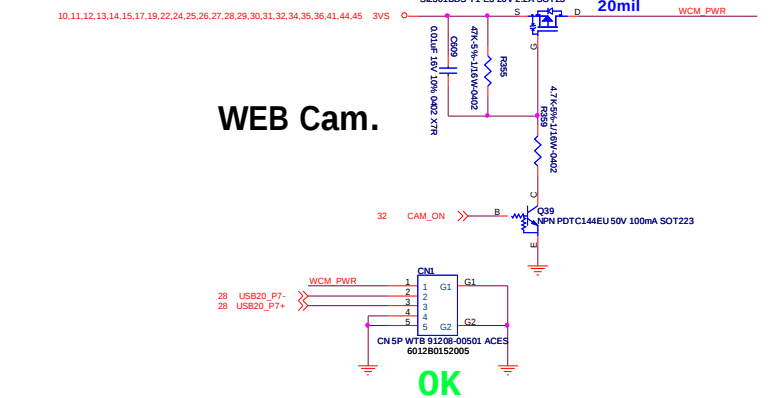
For All Model

VGA Board CN



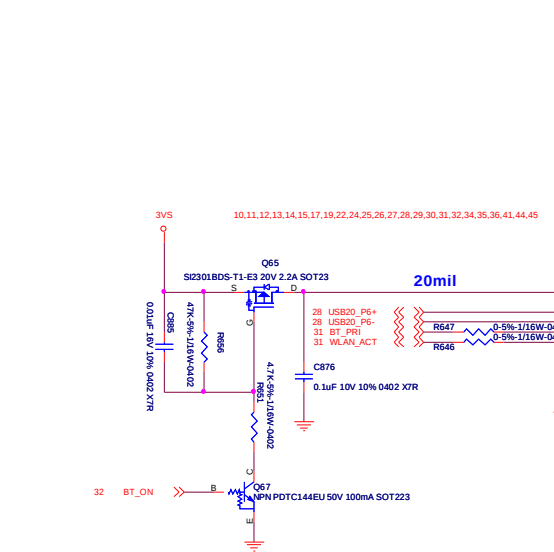
For All Model

WEB Cam.



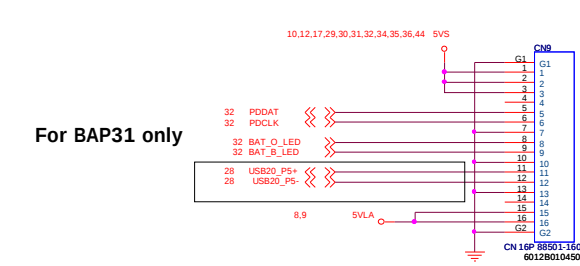
For All Model

Bluetooth CON.



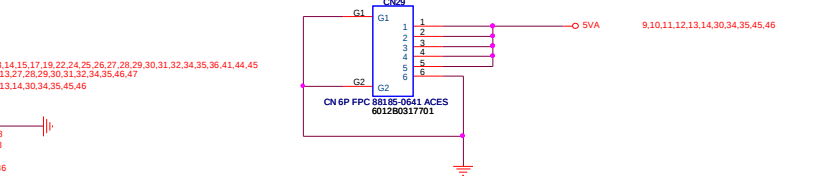
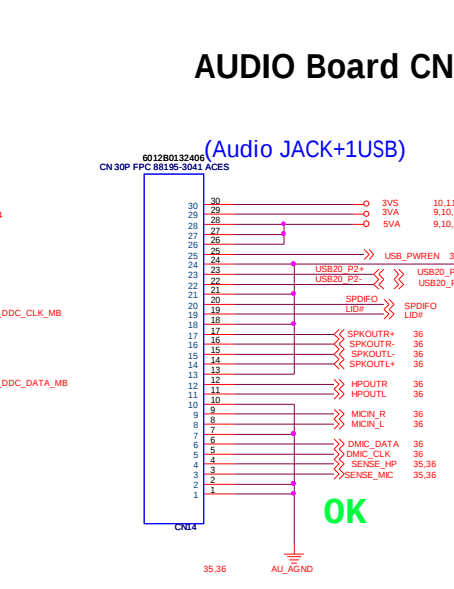
For All Model

GLIDE PAD Board

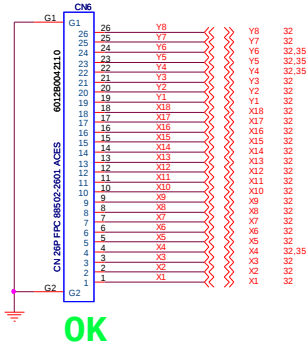


For All Model

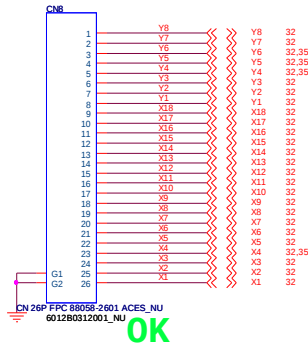
AUDIO Board CN



To K/B(For All Model)



To K/B(No Use)



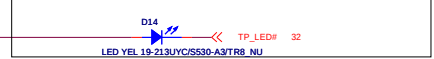
GP lock Button / LED(FOR SJM31)



GP lock Button / LED(FOR BAP31)

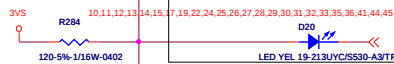


GP lock Button / LED(FOR JM31)

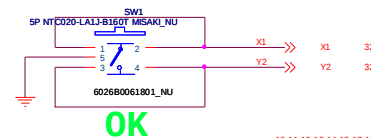


R284

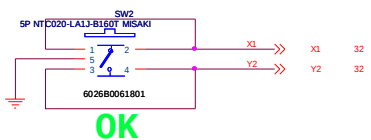
120 ohm for JM31, BAP31
470 ohm for SJM31



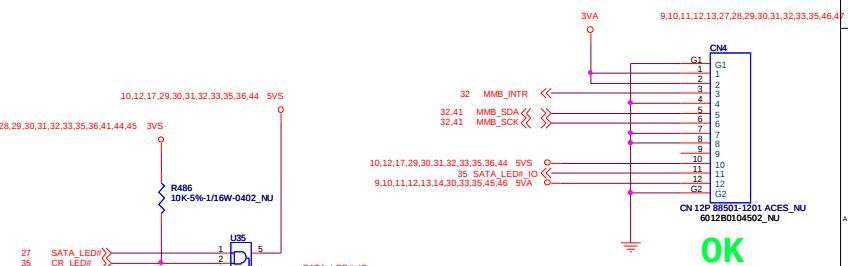
SW (No Use)



SW (FOR All Model)



SW Sensor BOARD(For JM31,SJM31)



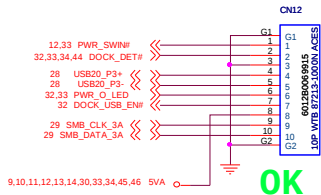
INVENTEC

TITLE			
BAP31G SEF			
BAP			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-13/A02268501-ALG	A03
SHEET			
34	09	47	

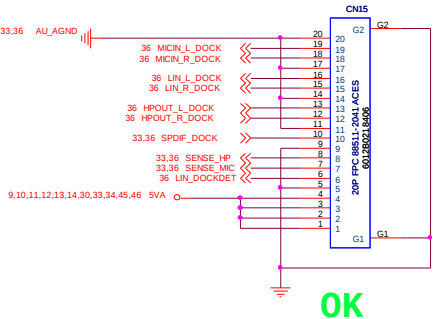
CHANGE by S.H.Chung DATE Tuesday, May 26, 2009

For BAP31(EASY/B)

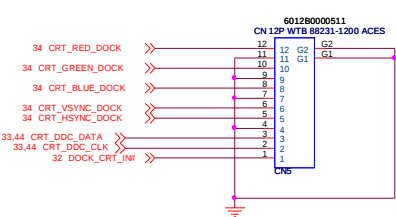
MB(USB) TO EASY/B
For BAP31



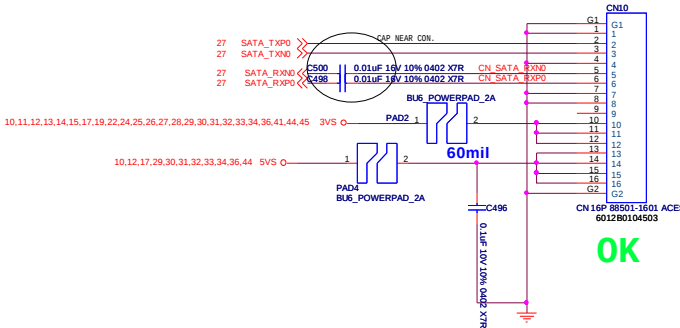
MB(AUDIO) TO EASY/B
For BAP31



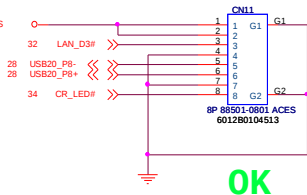
MB(RGB) TO EASY/B
For BAP31



SSD I/F
For All Model

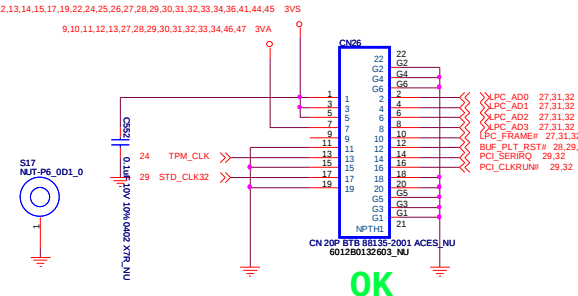


Card Reader BOARD CN
For All Model



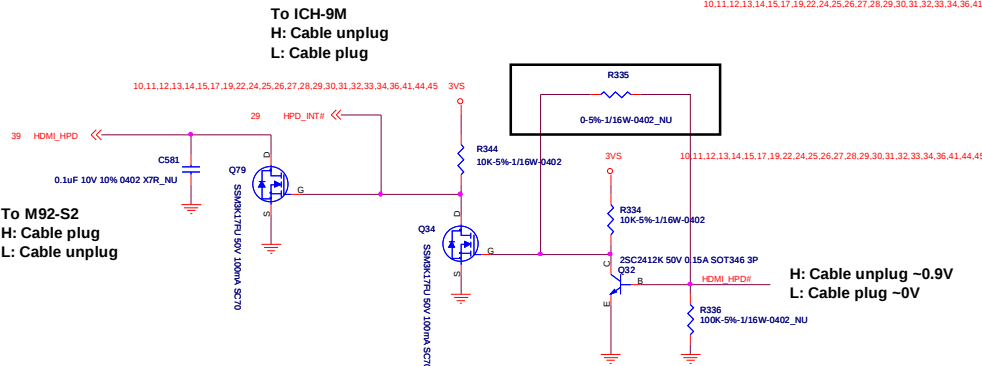
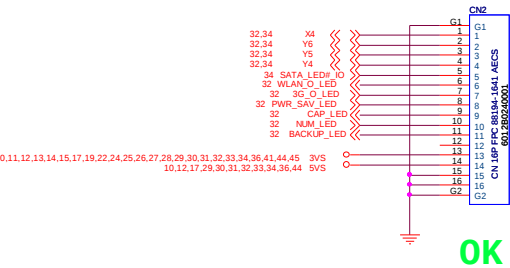
NO NEED

TPM CN

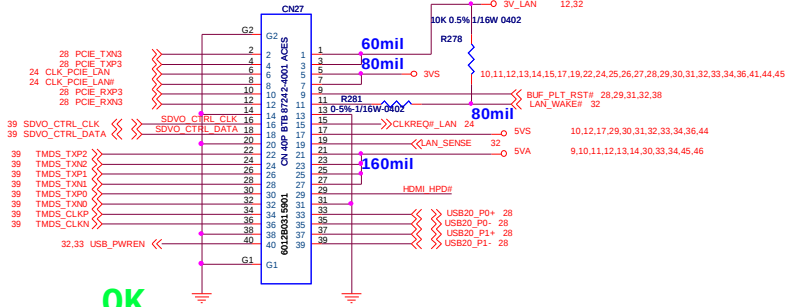


For BAP31

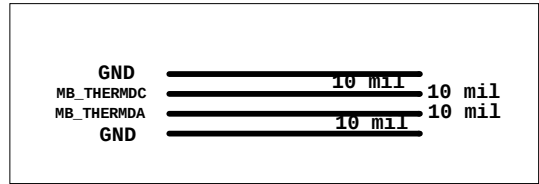
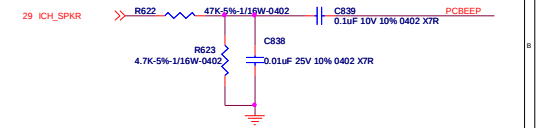
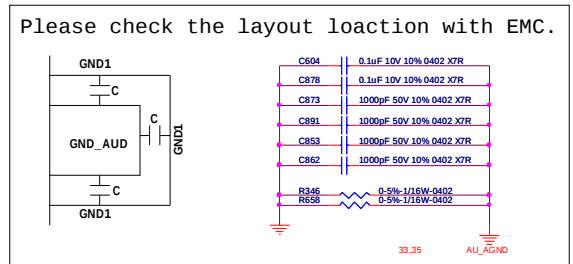
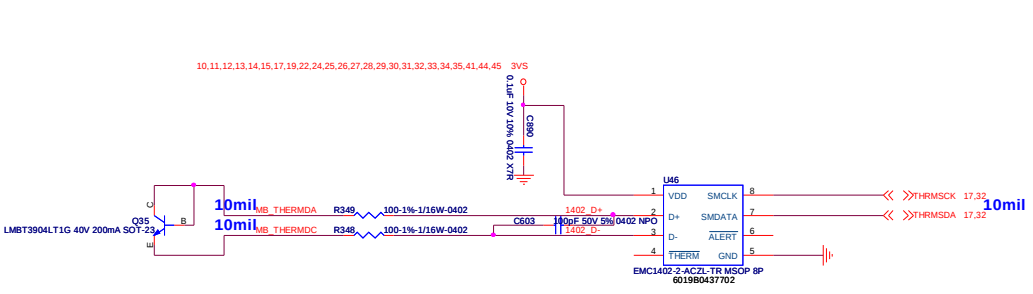
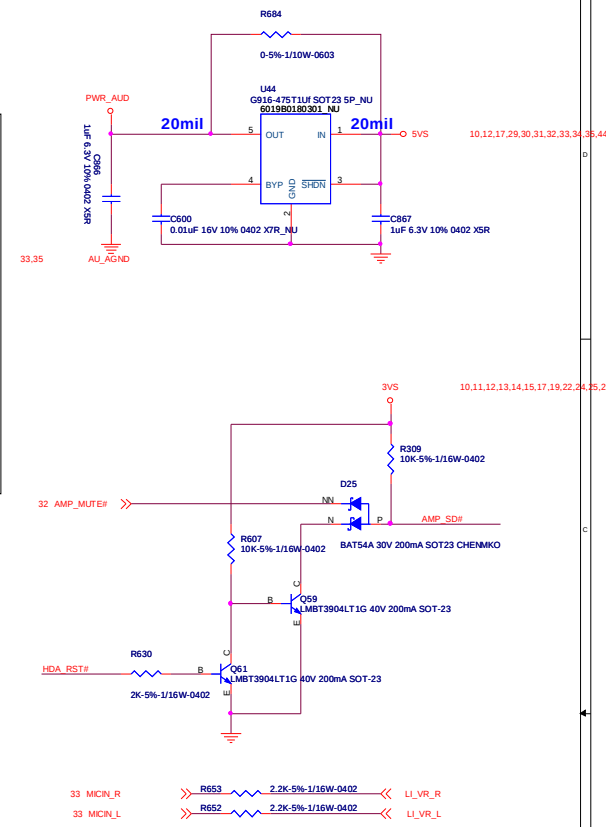
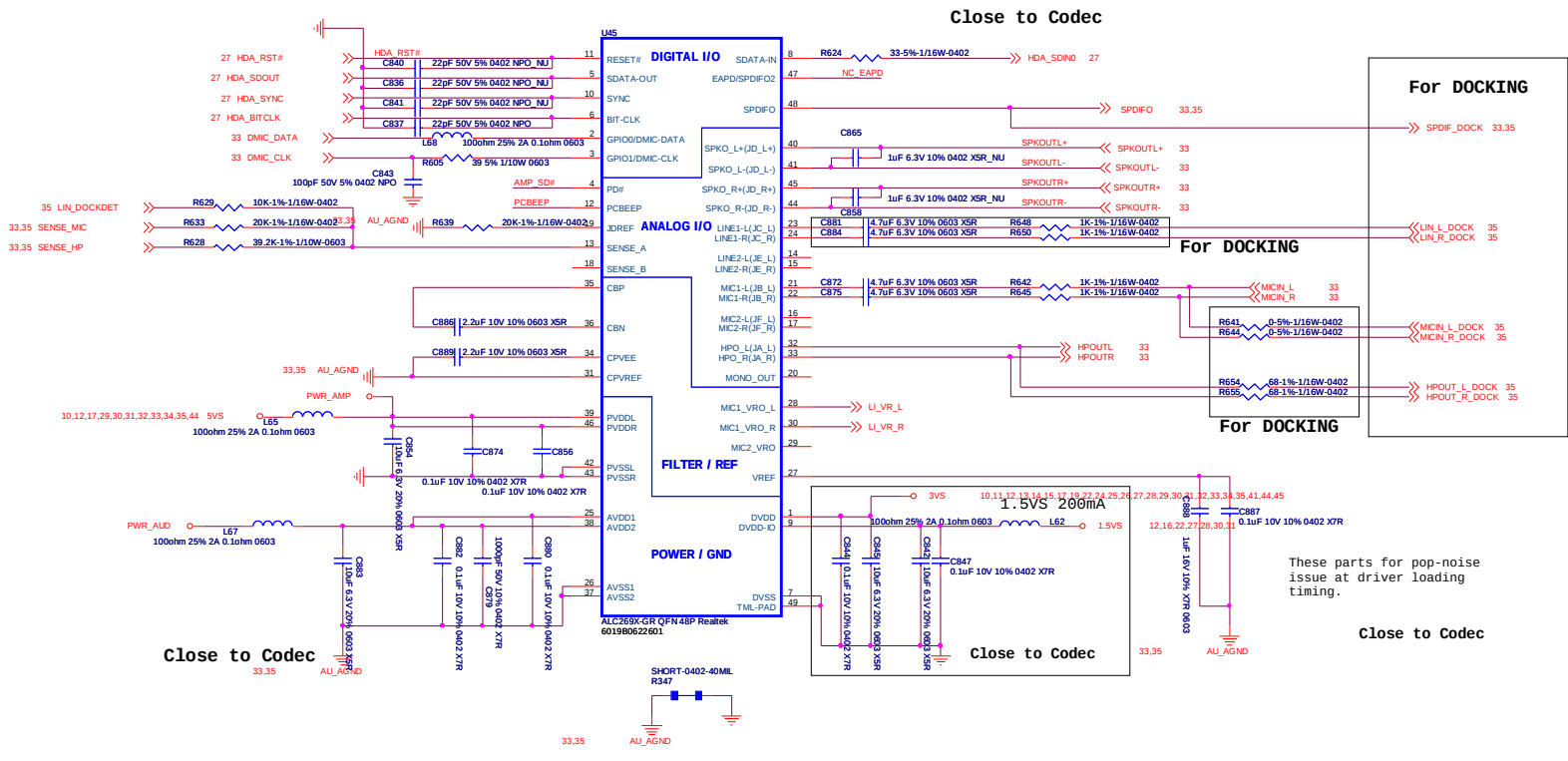
SW/B CN



USB Board CN (LAN+HDMI+2USB)
For All Model



INVENTEC			
BAP31G SFF			
BAP			
SIZE	CODE	DOC NUMBER	REV
Custom	C3	D-CS-13-002268501-ALG	A03
SHEET 35 OF 47			



INVENTEC			
BAP31G SFF			
Audio Codec			
TITLE	DOC NUMBER	REV	
Custom	D-CS-1310A2268501-ALG	A03	
SIZE	CODE	REV	
Sheet	CS	36	47

BLANK

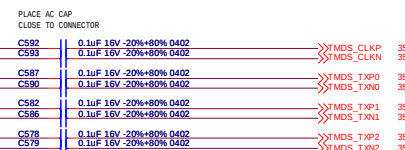
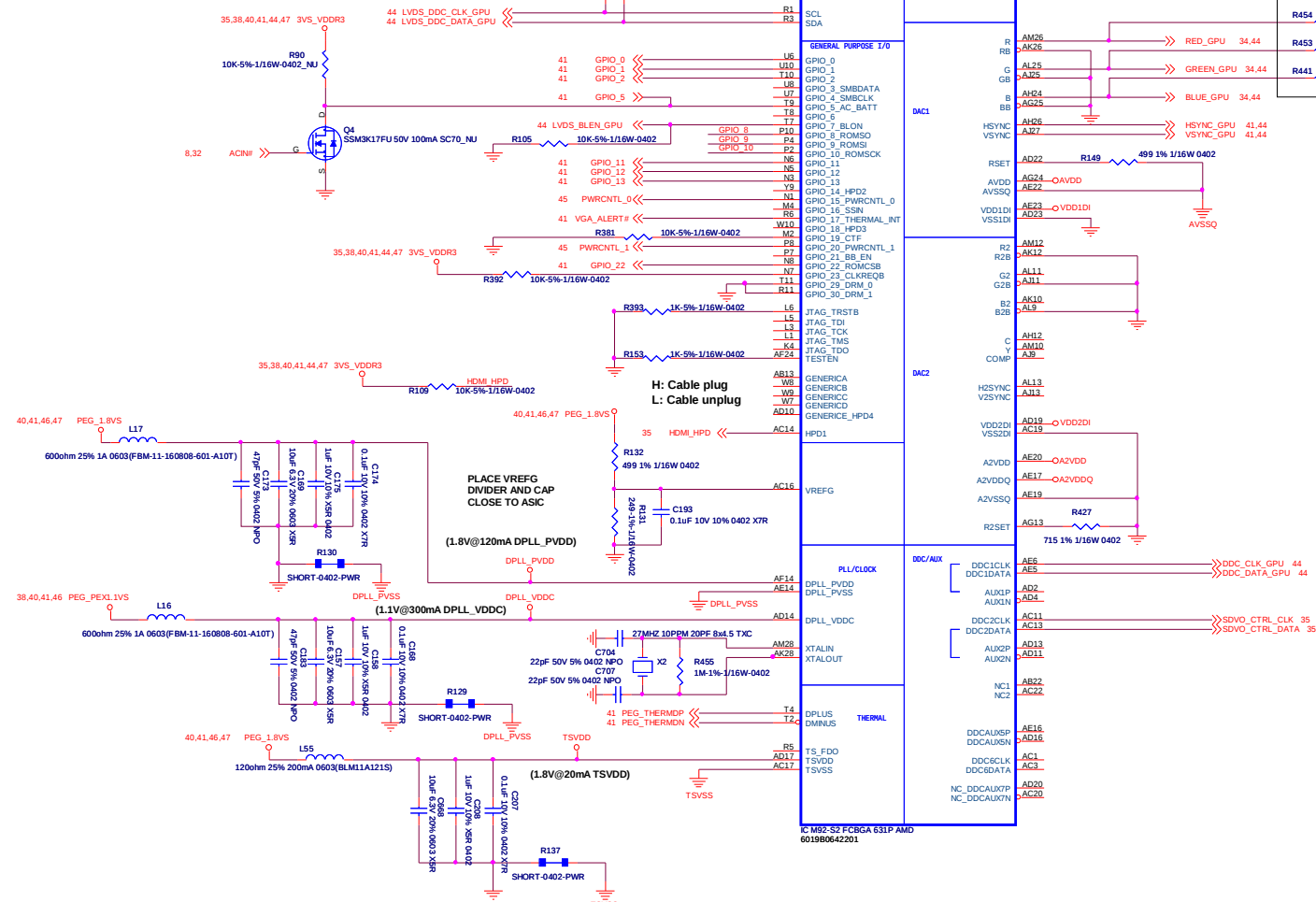
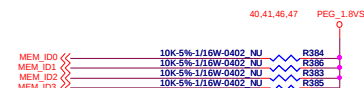
INVENTEC

TITLE
BAP31G SFF BLANK

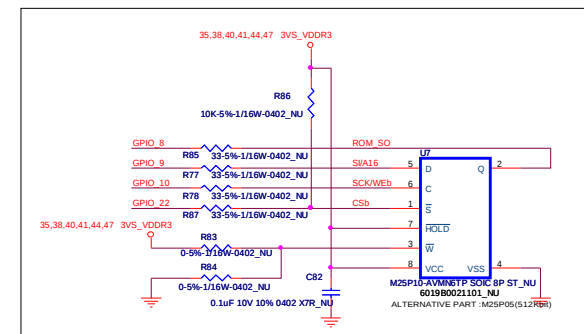
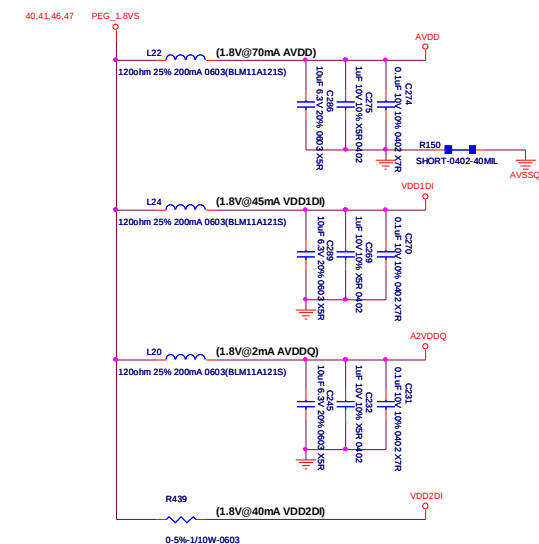
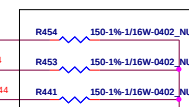
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A226-S01-ALG	A00

MEM ID3	MEM ID2	MEM ID1	MEM ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V



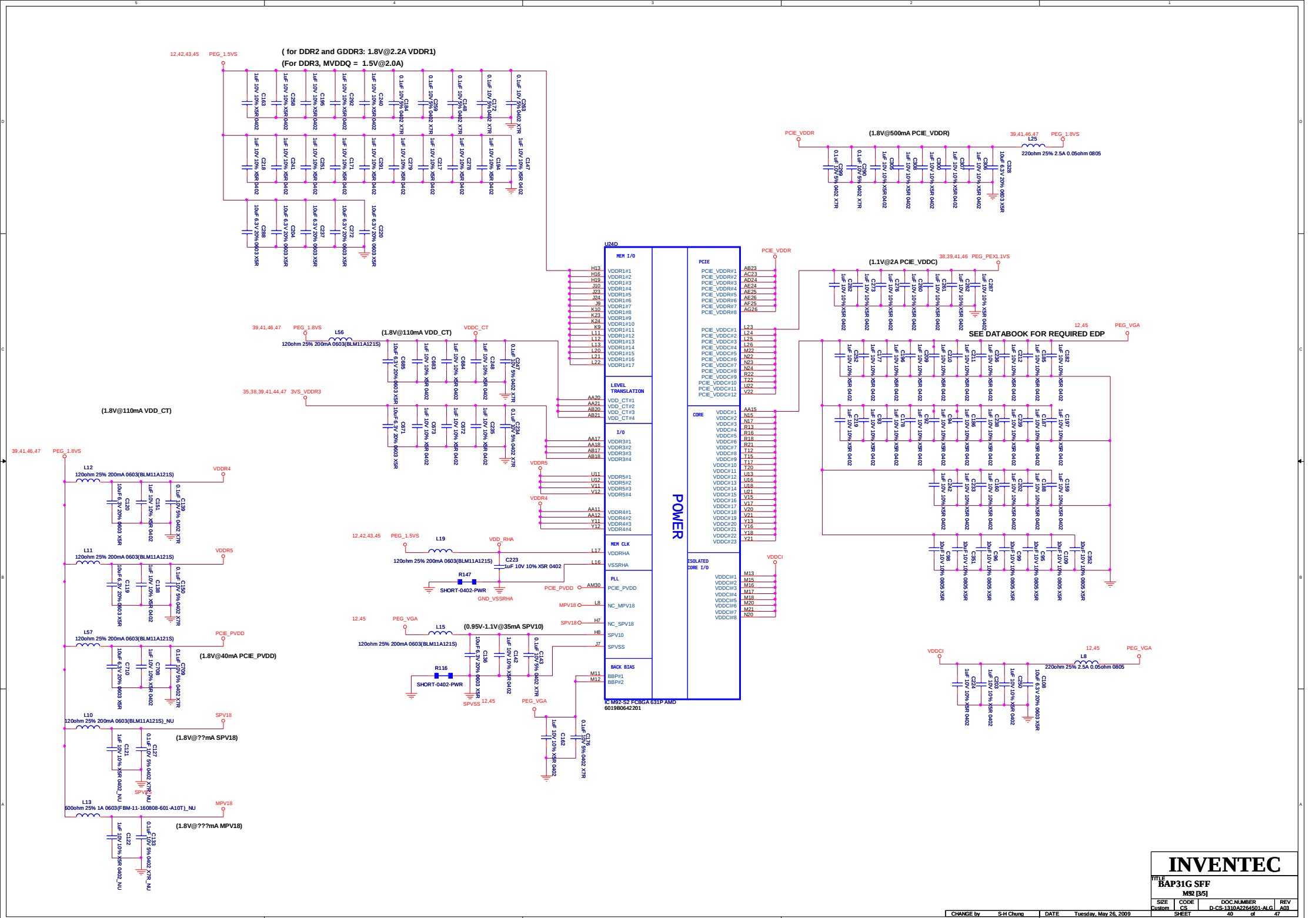
FOR JM/SJM31 ONLY
BAP31 NU



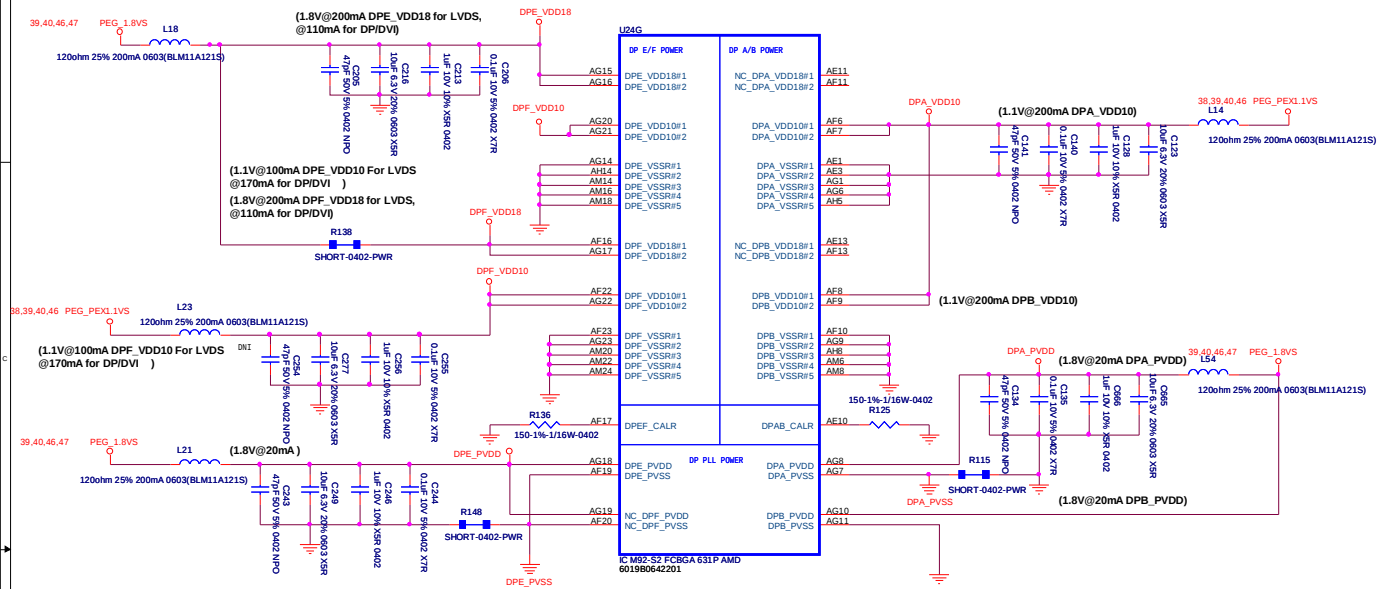
RESERVE SERIAL EEPROM 512K/1M

INVENTEC

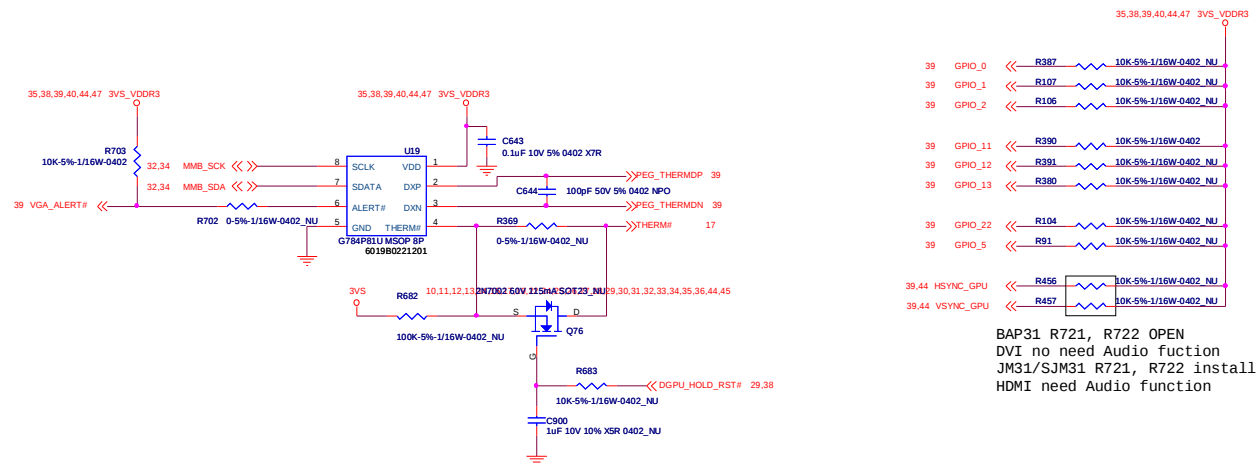
TITLE BAP31G SFF			
M92 [2/5]			
SIZE Custom	CODE CS	DOC NUMBER D-CS-1310A2264501-ALG	REV A03



For 92, DPx_VDD10 = 1.1V
For Future ASIC, DPx_VDD10 = 1.0V



PIN STRAPS



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERIC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function	X X
		0 1 Audio for DisplayPort and HDMI if dongle is detected	
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERIC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

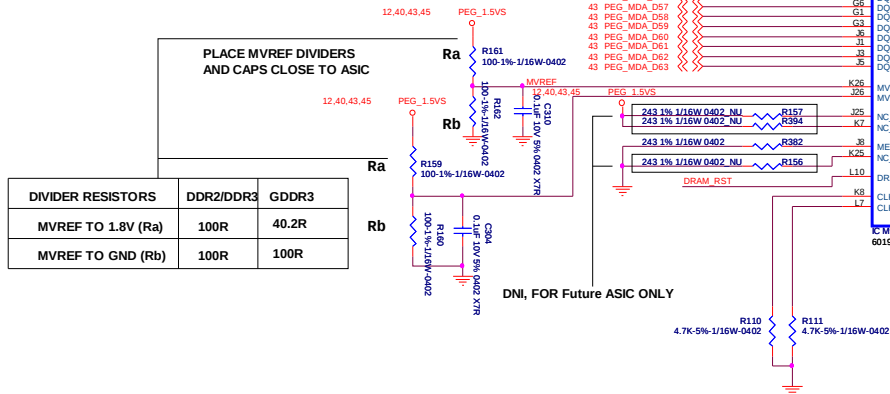
BAP31 R721, R722 OPEN
DVI no need Audio fuction
JM31/SJM31 R721, R722 install
HDMI need Audio function

INVENTEC

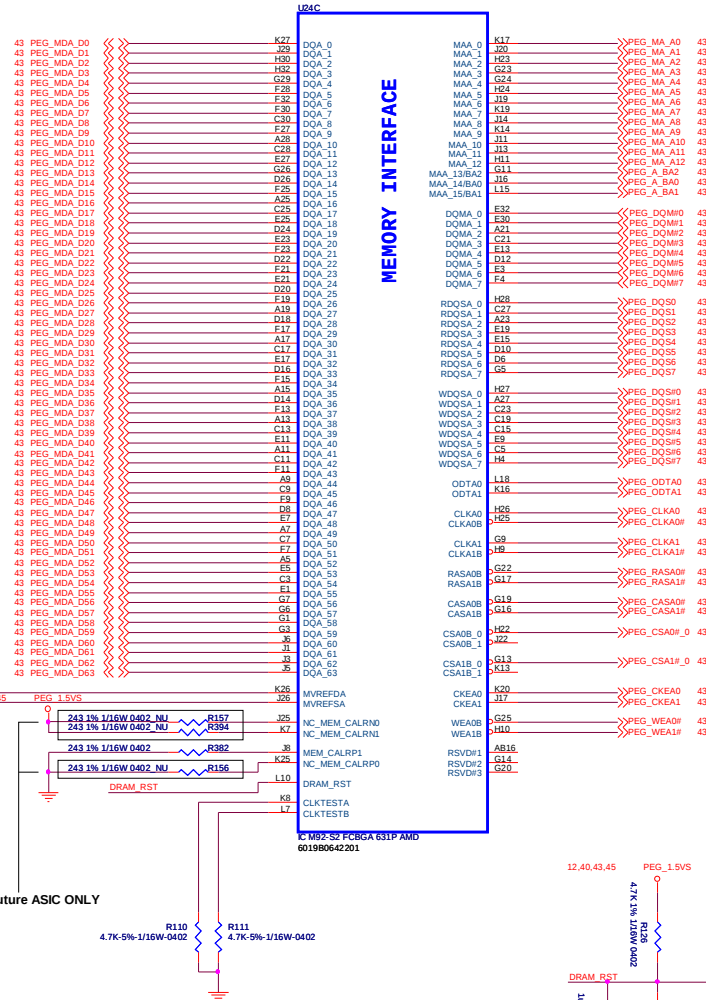
TITLE
BAP31G SFF
M92 [4/5]

SIZE	CODE	DOC. NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET		41 of	47

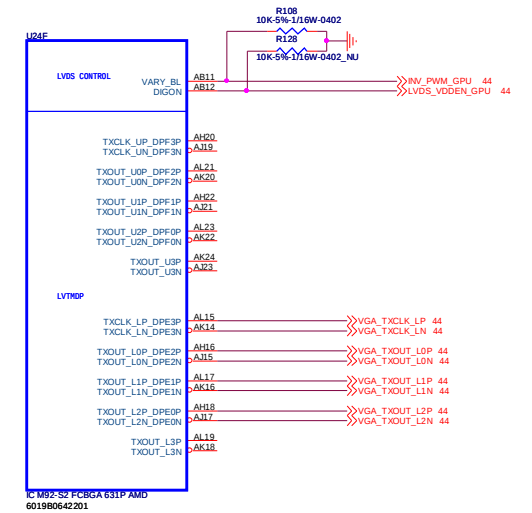
**MVDDQ = 1.5V FOR
DDR3 Memory**



DDR3 Memory Interface



LVDS Interface



INVENTEC

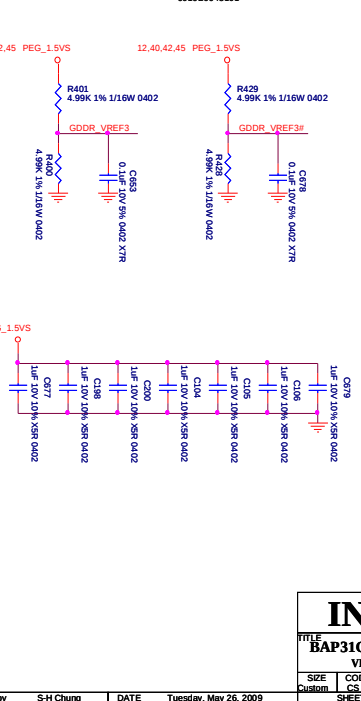
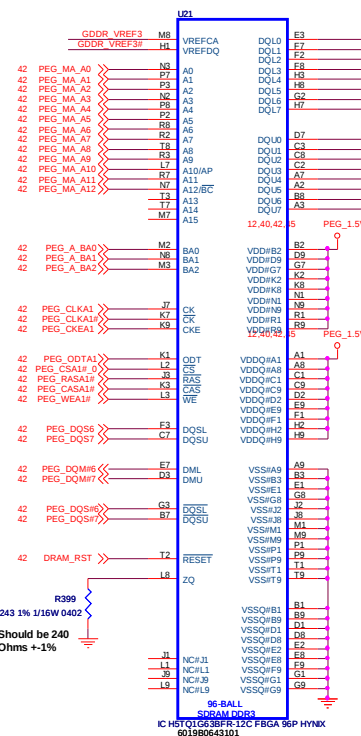
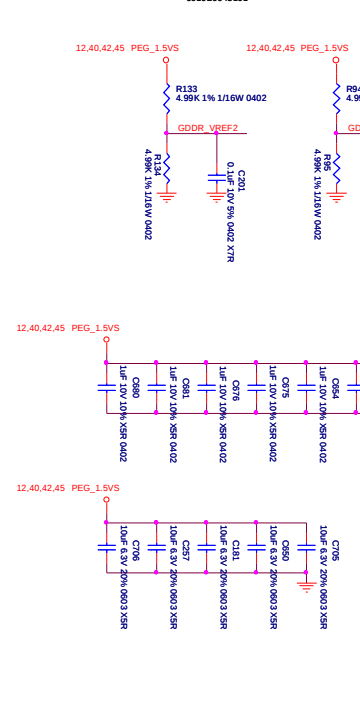
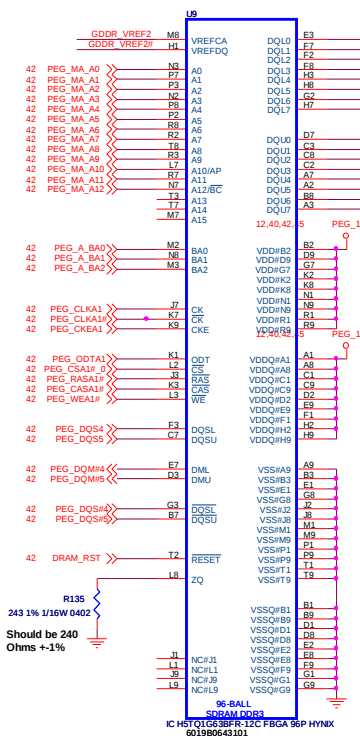
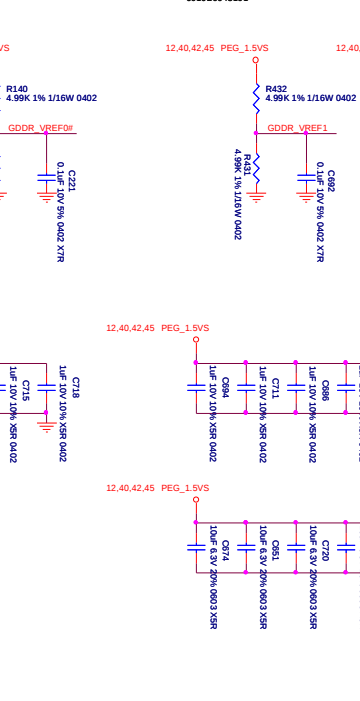
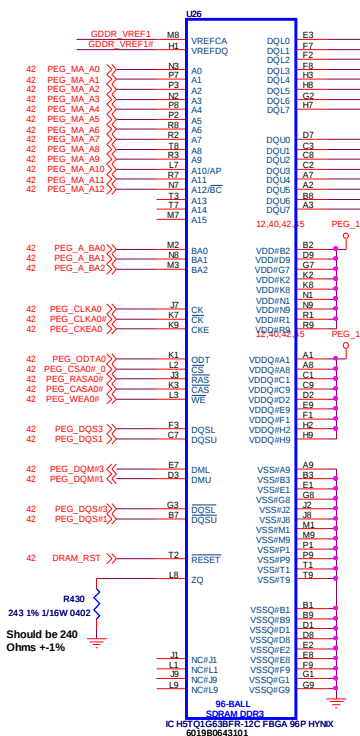
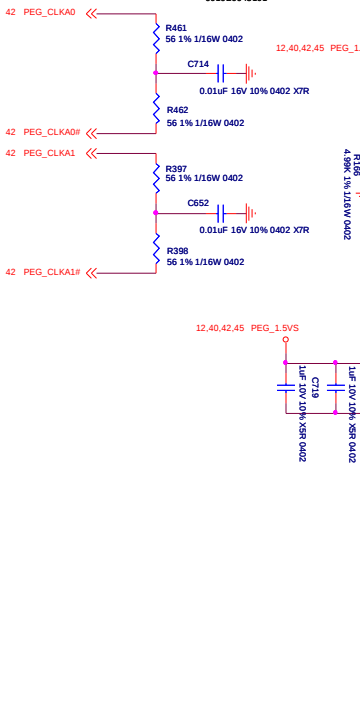
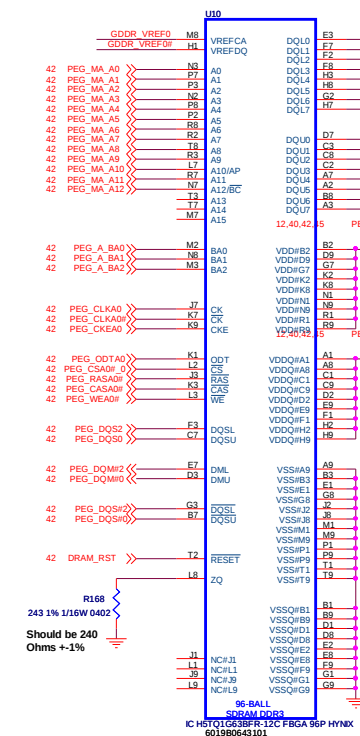
FILE: BAP31G SFF

M92 [5/5]

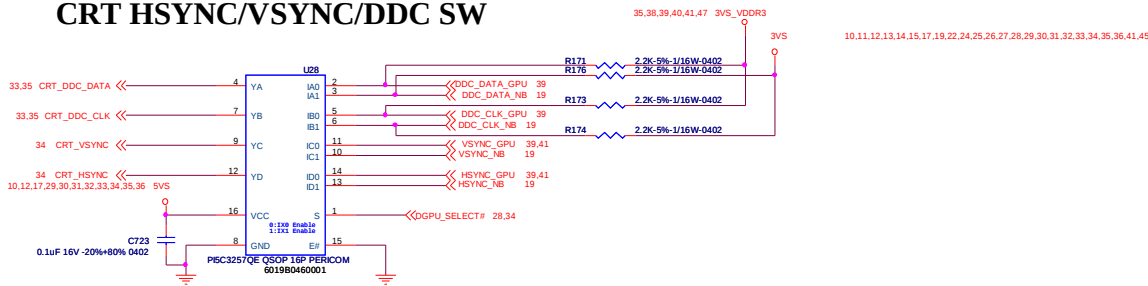
SIZE: Custom CODE: CS DOCNUMBER: D-CS-1310A2264591-ALG_A03

SHEET: 42 of 47

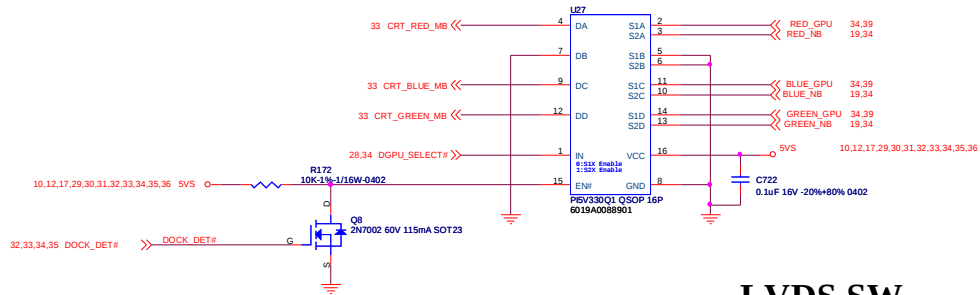
CHANGE by: S-H Chung DATE: Tuesday, May 26, 2009



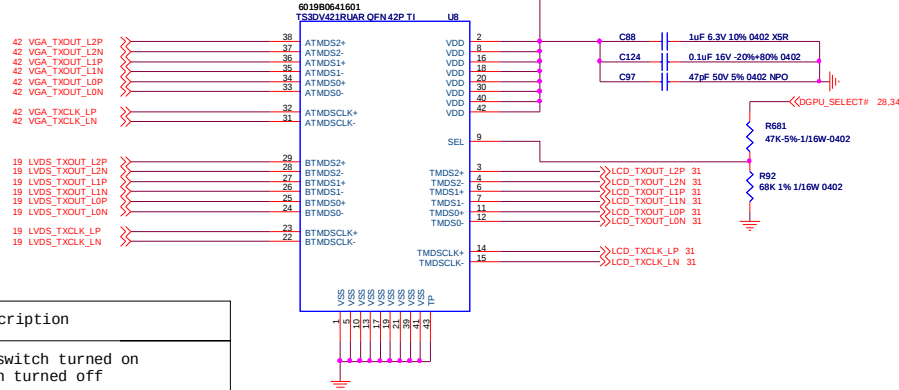
CRT HSYNC/VSYNC/DDC SW



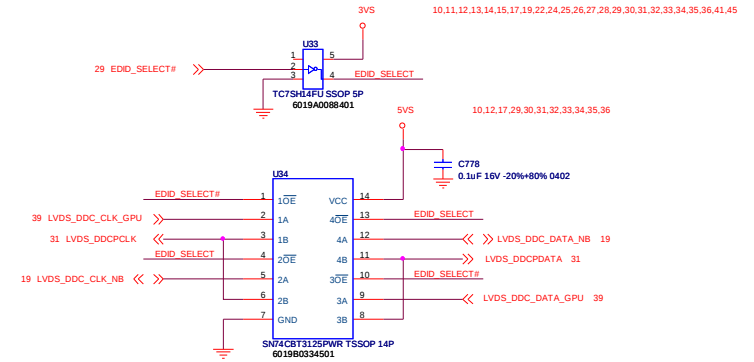
CRT R/G/B SW



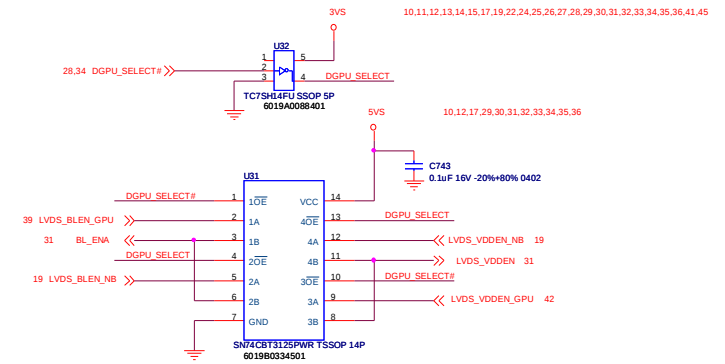
LVDS SW



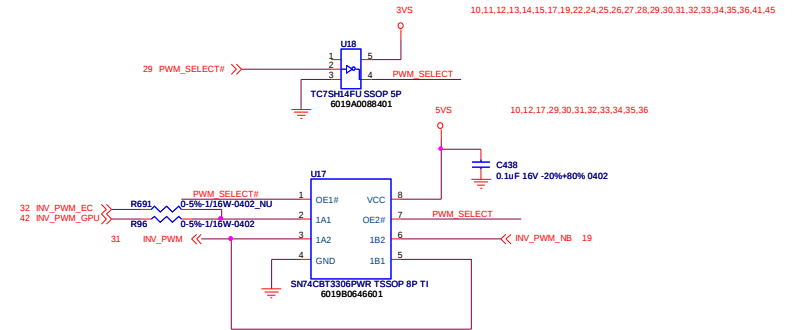
LCD DDC SW



LVDS BKL and Vcc Enable SW



LCD PWM SW



Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

INVENTEC

TITLE BAP31G SFF			
Hybrid Switch			
SIZE Custom	CODE CS	DOCNUMBER D-CS-1310A2264501-ALG	REV A03
SHEET 44		REV 47	

