BAP/BXP30

A02 Build

2010.05.22

INVENTEC			
TITLE: BAP/BXP30			
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01
CHANGE by: IEC	DATE: Saturday, May 22, 2010	SHEET: 1 of 41	

1. Schematic Page Description :

BAP30/BXP30 Schematic Ver : X01

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
None	

PCIINT	CHIP	Interface
None		

REQ	CHIP
None	

3. USB & PCI-Express & SATA Description :

USB Port	DEVICE	USB Port	DEVICE
Port 0	System (ESATA)	Port 7	Bluetooth
Port 1	System	Port 8	
Port 2	System	Port 9	Web Cam
Port 3	System	Port 10	
Port 4	CardReader	Port 11	FingerPrint
Port 5		Port 12	
Port 6		Port 13	3G

PCI-E	DEVICE
Port 1	New Card
Port 2	Docking
Port 3	Mini Card(WLAN)
Port 4	Mini Card(3G)
Port 5	Mini Card(ROBSON)
Port 6	Giga-LAN

SATA	DEVICE
Port 1	HDD
Port 2	E-SATA
Port 4	BAY
Port 5	None

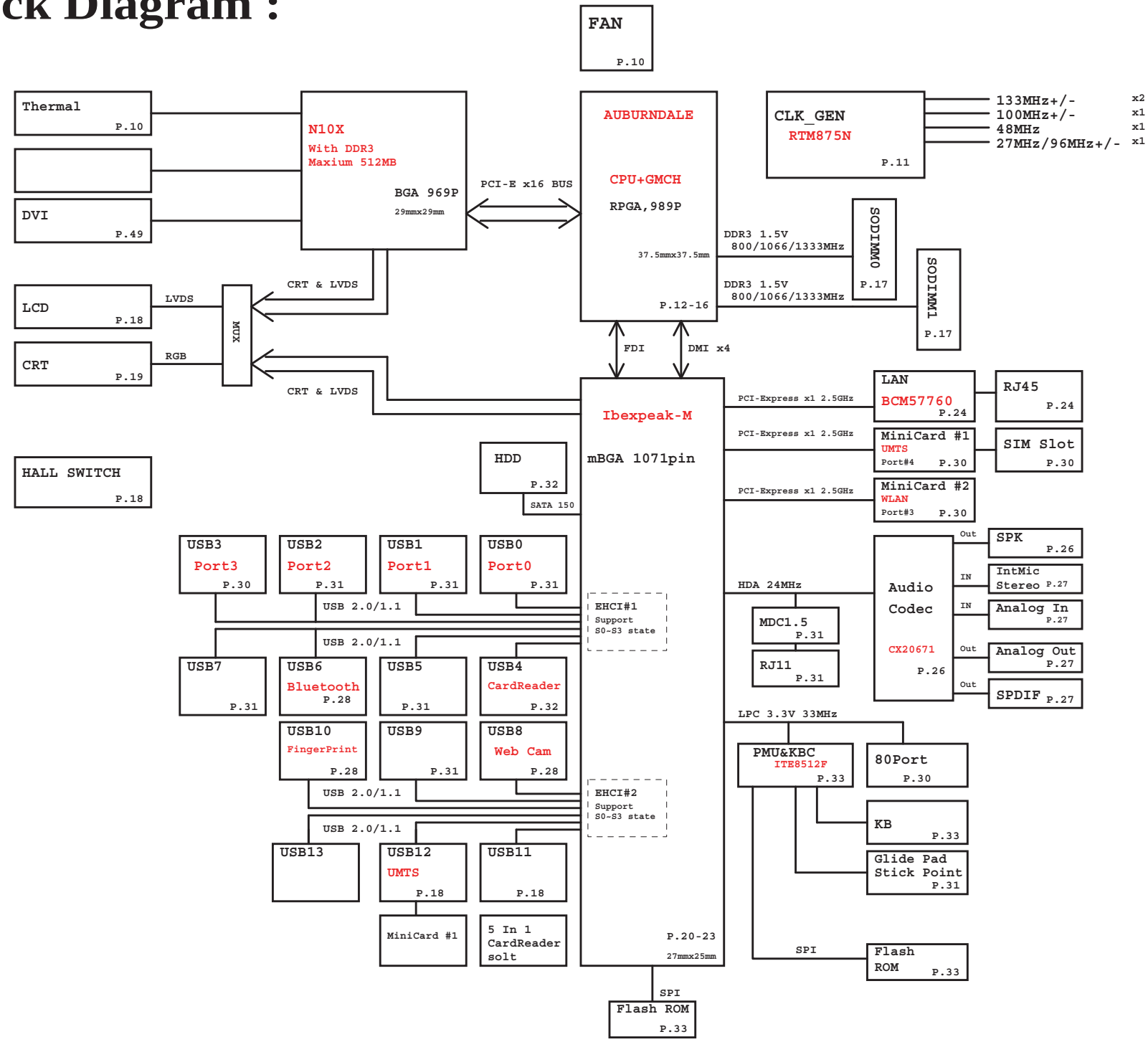
INVENTEC

TITLE: BAP/BXP30
schematics page DESCR

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Friday, May 21, 2010 | SHEET 2 of 41

3. Block Diagram :



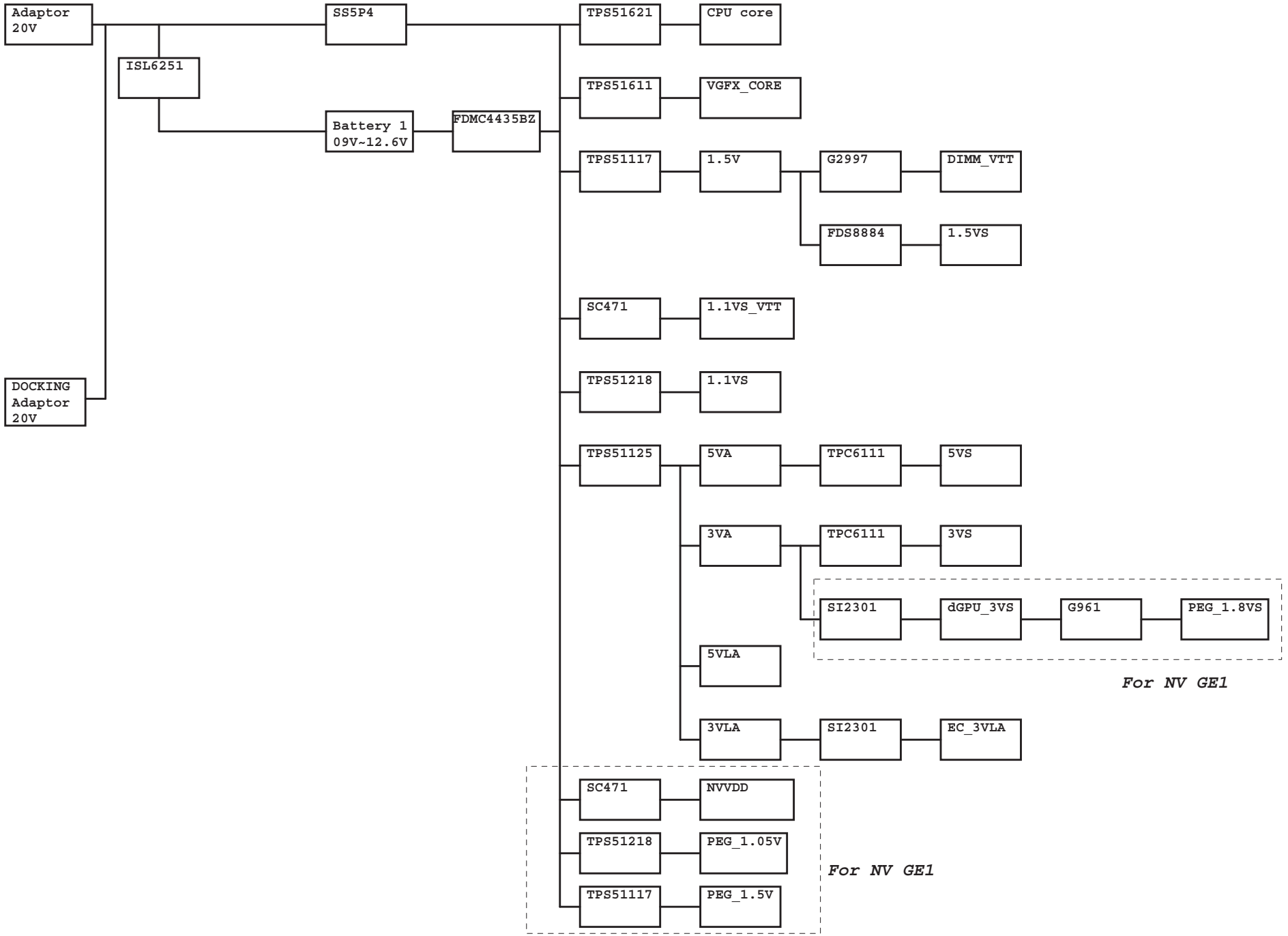
INVENTEC

TITLE: BAP/BXP30
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Friday, May 21, 2010 | SHEET 3 of 41

Power Block Diagram :



INVENTEC

TITLE: BAP/BXP30 Power Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02

CHANGE by IEC | DATE Friday, May 21, 2010 | SHEET 4 of 41

4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
EC_3VLA	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
3VM	3.3V power rail by SUSM#
1.05VM	1.05V switched power rail by SUSM#
1.5V	1.5V switched power rail by SUSC#
1.8V	1.8V power rail by SUSC#
3VS	3.3V power rail by SUSB#
5VS	5.0V power rail by SUSB#
1.5VS	1.5V power rail by SUSB#
1.05VS	1.05V power rail by SUSB#
PWR_DIMM_VTT	0.75V DDR Termination Voltage by SUSB#
VGFX_CORE	1.05V power rail for UMA by SUSB#
PEG_1.8VS	1.8V switched power rail for NB9x by SUSB#
PEG_PEX_1.1VS	1.1V switched power rail for NB9x by SUSB#
PEG_NVDD	Variable switched power rail for NB9x by SUSB#
Vcore_CPU	Core switched power rail for CPU

Part Naming Conventions

C	=	Capacitor	Q	=	Transistor
CN	=	Connector	R	=	Resistor
D	=	Diode	RP	=	Resistor Pack
F	=	Fuse	U	=	Arbitrary Logic Device
L	=	Inductor	Y	=	Crystal and Osc

Name Suffix

#	=	Active Low signal
NU	=	No Stuff

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn HFM:	1.3319V~1.4375V~1.4591V	36A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn: AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GM: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GM: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GM:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GM:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GM:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GM:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GM:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GM:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GM: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GM: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GM: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GM: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GM: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GM: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GM: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GM: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GM: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS397BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:	3.0V~3.3V~3.6V	
	Super I/O: IT8305E		
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:82567LM	1.0V and 1.8V	Each 1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: GL827	3.0V~3.3V~3.6V	
	Azalia Codec: ALC262	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	ODD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
	Audio AMP: G1432		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	1.5A
	USB and ESATA	5VA	2A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

INVENTEC

TITLE: BAP/BXP30
Annotations

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Friday, May 21, 2010 | SHEET 5 of 41

6.Schematic modify Item and History :

CHANGE by	IEC		
DATE	Friday, May 21, 2010		

INVENTEC

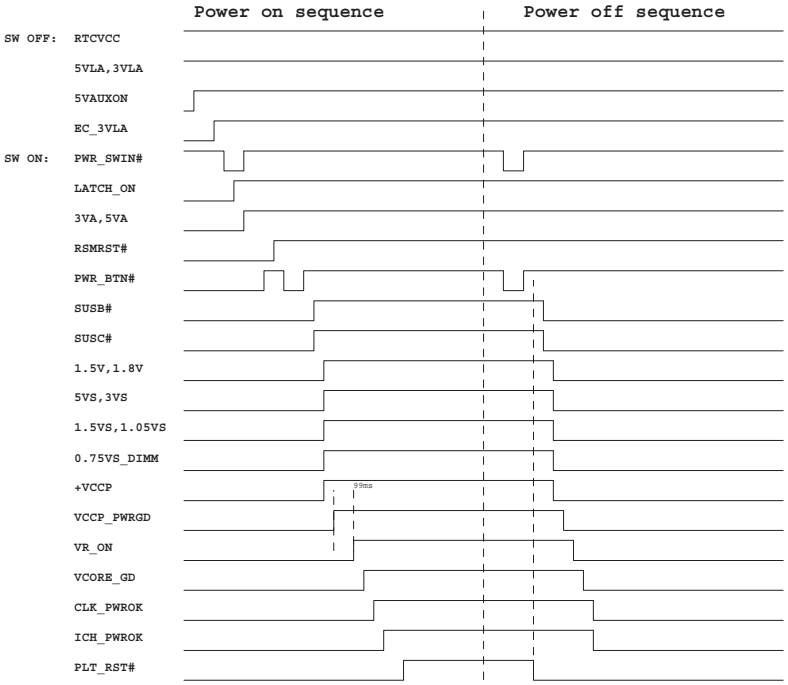
TITLE: BAP/BXP30
schematics modify

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

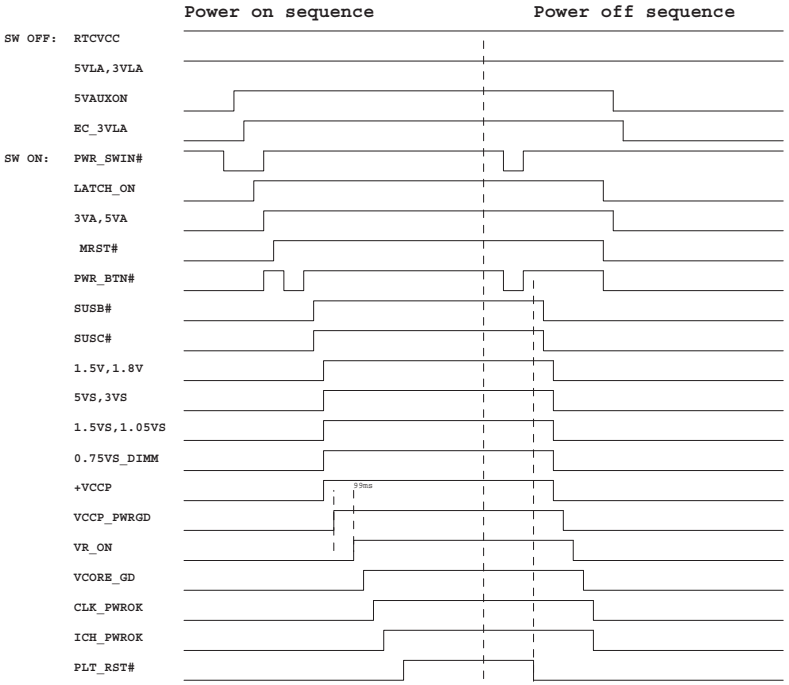
SHEET 6 of 41

8.SYSTEM POWER SEQUENCE :

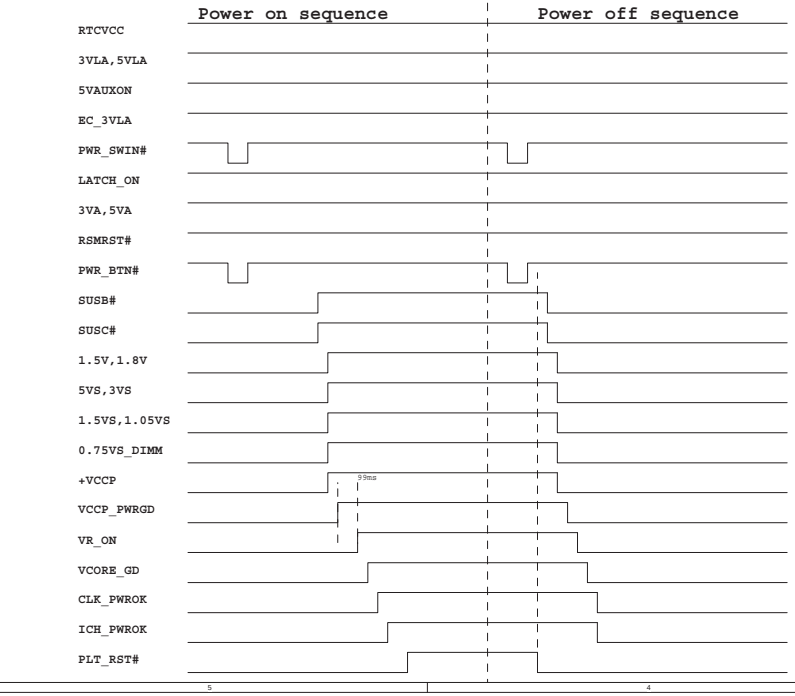
Power on/off sequence AC insert(First)



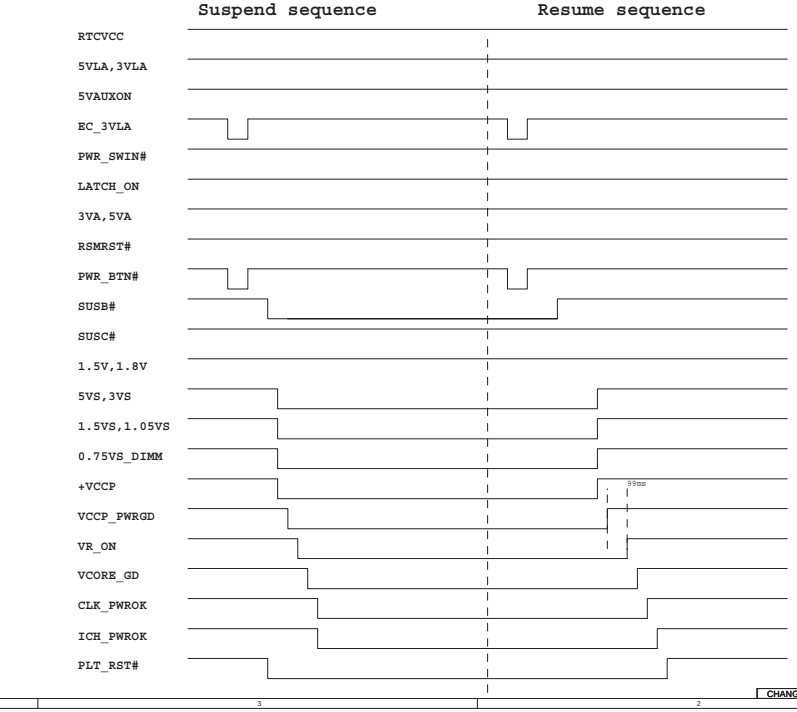
Battery only Power on/off sequence



Power on/off sequence AC insert(S4)



Suspend resume sequence(S3)

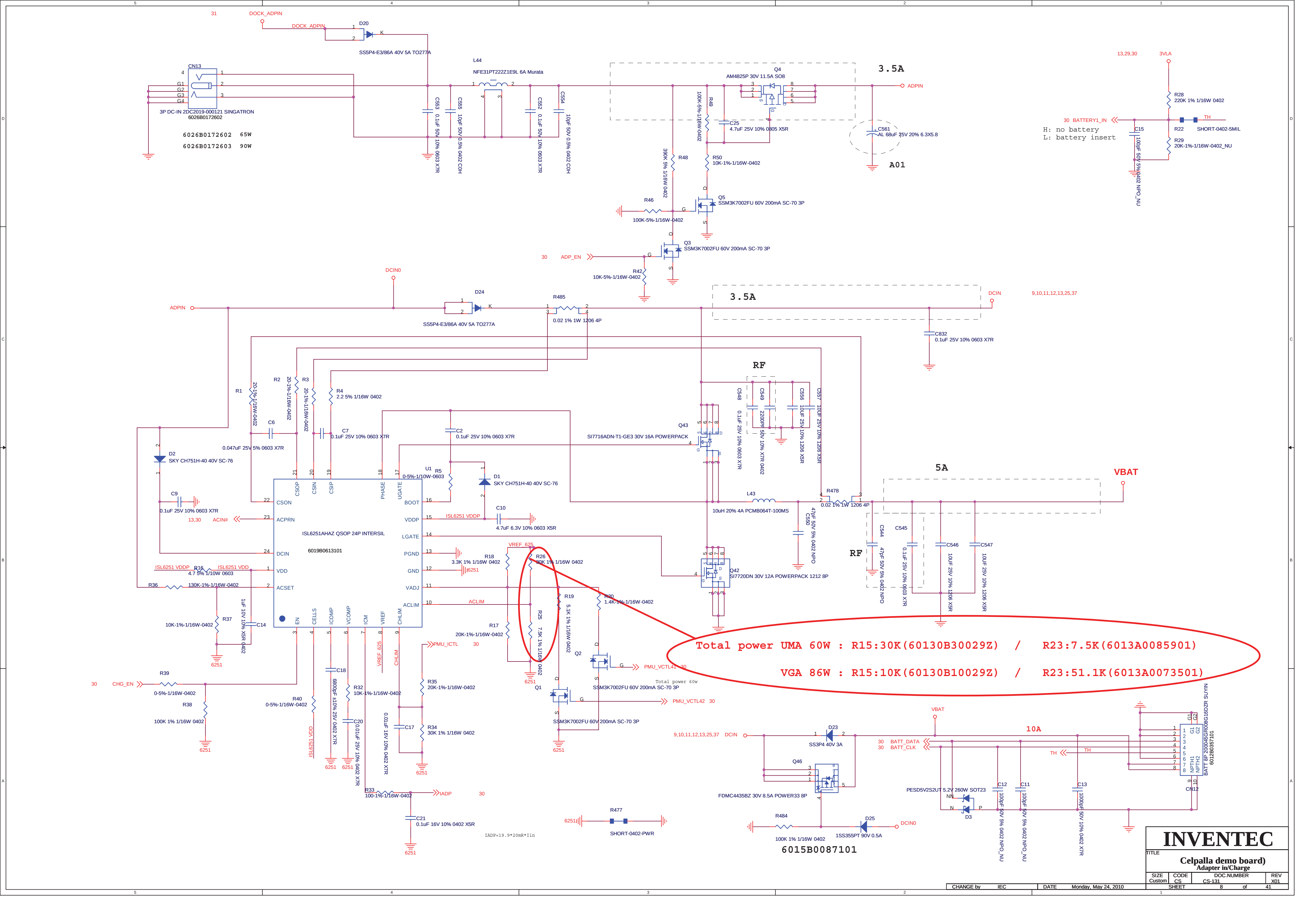


INVENTEC

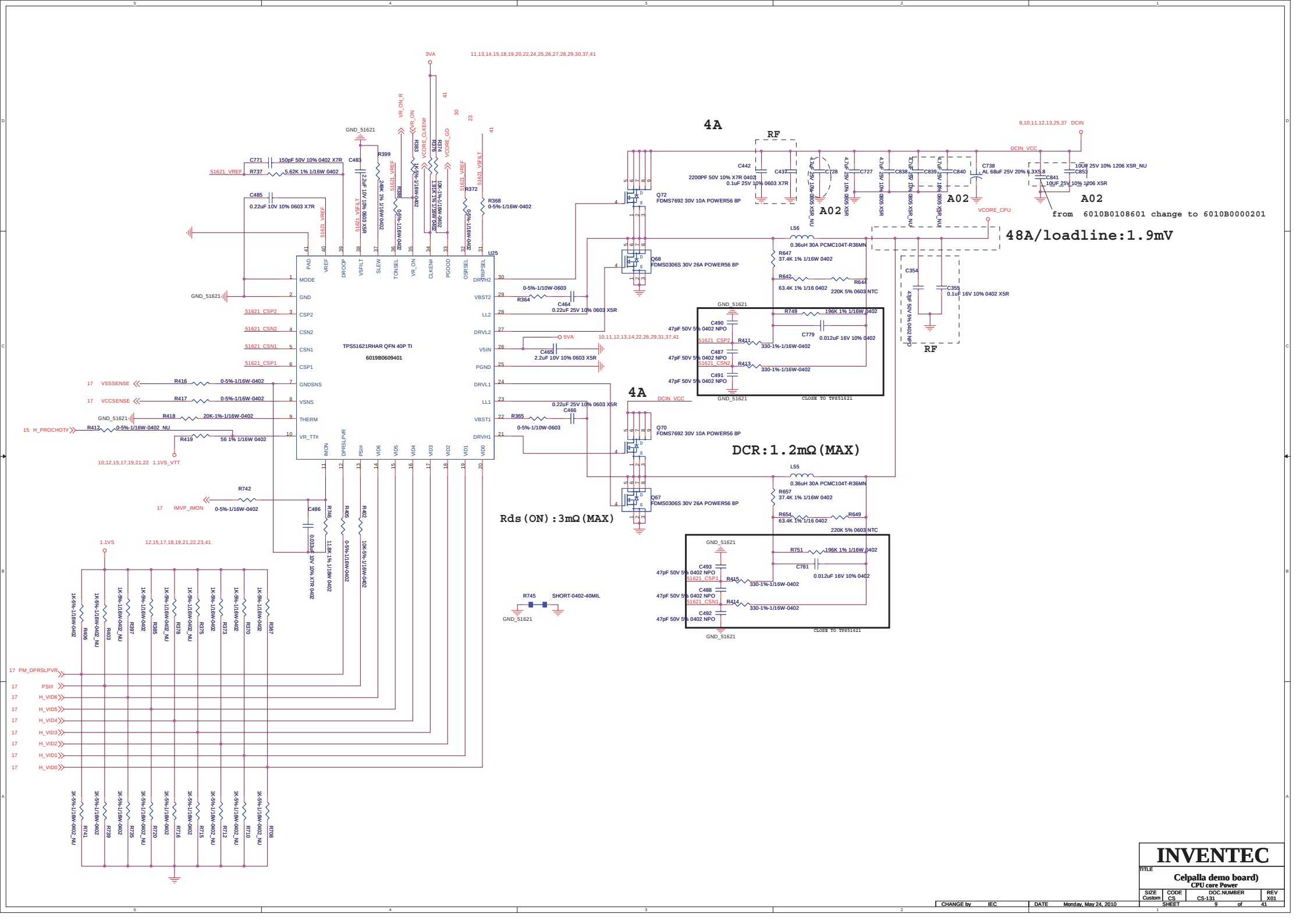
TITLE: BAP/BXP30
Timing Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Friday, May 21, 2010 | SHEET 7 of 41



DOCK_ADPIN
D20
SS5P4-E3/86A 40V 5A TO277A
L44
NFE31PT222Z1E9L 6A Murata
CN13
3P DC-IN 2DC2019-000121 SINGATRON
6026B0172602
6026B0172602 65W
6026B0172603 90W
C553 0.1uF 50V 10% 0603 X7R
C555 10pF 50V 0.5% 0402 COH
C552 0.1uF 50V 10% 0603 X7R
C554 10pF 50V 0.5% 0402 COH
3.5A
Q4
AM4825P 30V 11.5A SO8
ADPIN
C25 4.7uF 25V 10% 0805 X5R
R49 100K-5%-1/16W-0402
C561 AL 68uF 25V 20% 6.3X5.8
A01
R48 390K 5% 1/16W 0402
R50 10K-1%-1/16W-0402
Q5 SSM3K7002FU 60V 200mA SC-70 3P
R46 100K-5%-1/16W-0402
Q3 SSM3K7002FU 60V 200mA SC-70 3P
ADP_EN
R42 10K-5%-1/16W-0402
3VLA
R28 220K 1% 1/16W 0402
BATTERY1_IN
TH
R22 SHORT-0402-5MIL
H: no battery
L: battery insert
C15 100pF 50V 5% 0402 NPO_NU
R29 20K-1%-1/16W-0402_NU
DCIN0
D24
SS5P4-E3/86A 40V 5A TO277A
R485
0.02 1% 1W 1206 4P
3.5A
DCIN
C832 0.1uF 25V 10% 0603 X7R
RF
R1 20-1%-1/16W-0402
R2 20-1%-1/16W-0402
R3 20-1%-1/16W-0402
R4 2.2 5% 1/16W 0402
C6 0.047uF 25V 5% 0603 X7R
C7 0.1uF 25V 10% 0603 X7R
C2 0.1uF 25V 10% 0603 X7R
C548 0.1uF 25V 10% 0603 X7R
C549 2200PF 50V 10% X7R 0402
C556 10UF 25V 10% 1206 X5R
C557 10UF 25V 10% 1206 X5R
Q43 SI7716ADN-T1-GE3 30V 16A POWERPACK
D2 SKY CH751H-40 40V SC-76
D1 SKY CH751H-40 40V SC-76
U1
R5 0-5%-1/10W-0603
ISL6251AHAZ QSOP 24P INTERSIL
6019B0613101
CSON ACPRN DCIN VDD ACSET EN CELLS ICOMP VCOMP ICM VREF CHLIM ACLIM VADJ GND PGND LGATE VDDP BOOT UGATE PHASE CSIP CSIN CSOP
C9 0.1uF 25V 10% 0603 X7R
ACIN#
ISL6251 VDDP
C10 4.7uF 6.3V 10% 0603 X5R
VREF_625
R18 3.3K 1% 1/16W 0402
R26 30K 1% 1/16W 0402
R16 4.7 5% 1/10W 0603
ISL6251 VDD
R36 130K-1%-1/16W-0402
R37 10K-1%-1/16W-0402
C14 1uF 10V 10% X5R 0402
L43 10uH 20% 4A PCMB064T-100MS
R478 0.02 1% 1W 1206 4P
5A
VBAT
C550 47pF 50V 5% 0402 NPO
C544 47pF 50V 5% 0402 NPO
C545 0.1uF 25V 10% 0603 X7R
C546 10UF 25V 10% 1206 X5R
C547 10UF 25V 10% 1206 X5R
RF
Q42 SI7720DN 30V 12A POWERPACK 1212 8P
R19 5.1K 1% 1/16W 0402
R20 1.4K-1%-1/16W-0402
R25 7.5K 1% 1/16W 0402
R17 20K-1%-1/16W-0402
Total power UMA 60W : R15:30K(60130B30029Z) / R23:7.5K(6013A0085901)
VGA 86W : R15:10K(60130B10029Z) / R23:51.1K(6013A0073501)
Q2
PMU_VCTL41
SSM3K7002FU 60V 200mA SC-70 3P
Total power 60w
Q1
SSM3K7002FU 60V 200mA SC-70 3P
PMU_VCTL42
PMU_ICTL
CHG_EN
R39 0-5%-1/16W-0402
R38 100K 1% 1/16W 0402
R40 0-5%-1/16W-0402
C18 6800pF ±10% 25V 0402 X7R
R32 10K-1%-1/16W-0402
C20 0.01uF 25V 10% 0402 X7R
C17 0.01uF 16V 10% 0402 X7R
R35 20K-1%-1/16W-0402
R34 30K 1% 1/16W 0402
R33 100-1%-1/16W-0402
IADP
C21 0.1uF 16V 10% 0402 X5R
IADP=19.9*20mR*Iin
R477 SHORT-0402-PWR
DCIN
D23 SS3P4 40V 3A
Q46 FDMC4435BZ 30V 8.5A POWER33 8P
R484 100K 1% 1/16W 0402
D25 1SS355PT 90V 0.5A
DCIN0
6015B0087101
10A
BATT_DATA
BATT_CLK
PESD5V2S2UT 5.2V 260W SOT23
D3
C12 100pF 50V 5% 0402 NPO_NU
C11 100pF 50V 5% 0402 NPO_NU
C13 1000pF 50V 10% 0402 X7R
CN12
BATT 8P 200045GR008G16DZR SUYIN
6012B0357101
INVENTEC
TITLE Celpalla demo board)
Adapter in/Charge
SIZE Custom CODE CS DOC.NUMBER CS-131 REV X01
CHANGE by IEC DATE Monday, May 24, 2010 SHEET 8 of 41



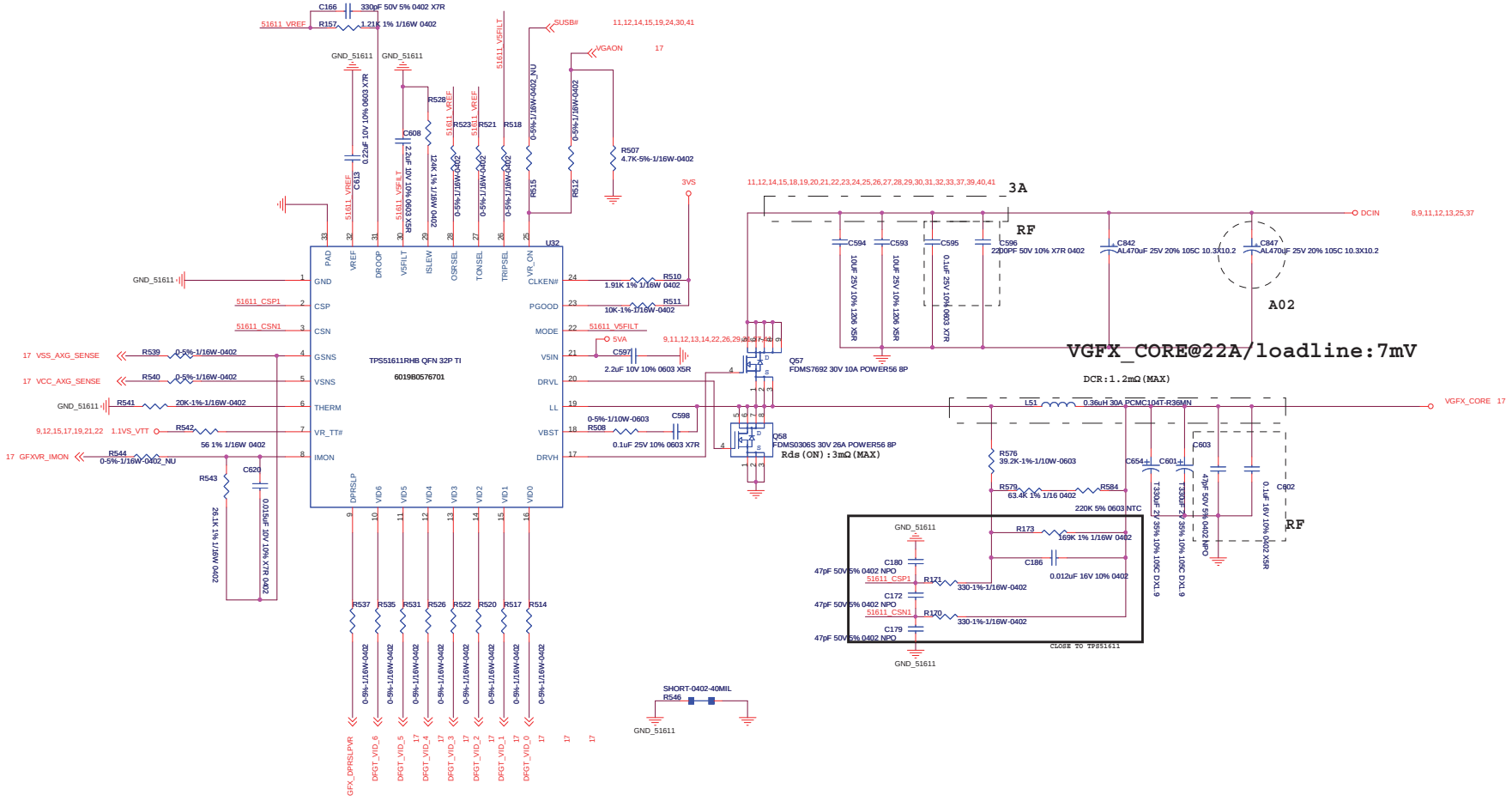
CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

TITLE: Celpalla demo board)
CPU core Power

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 9 of 41



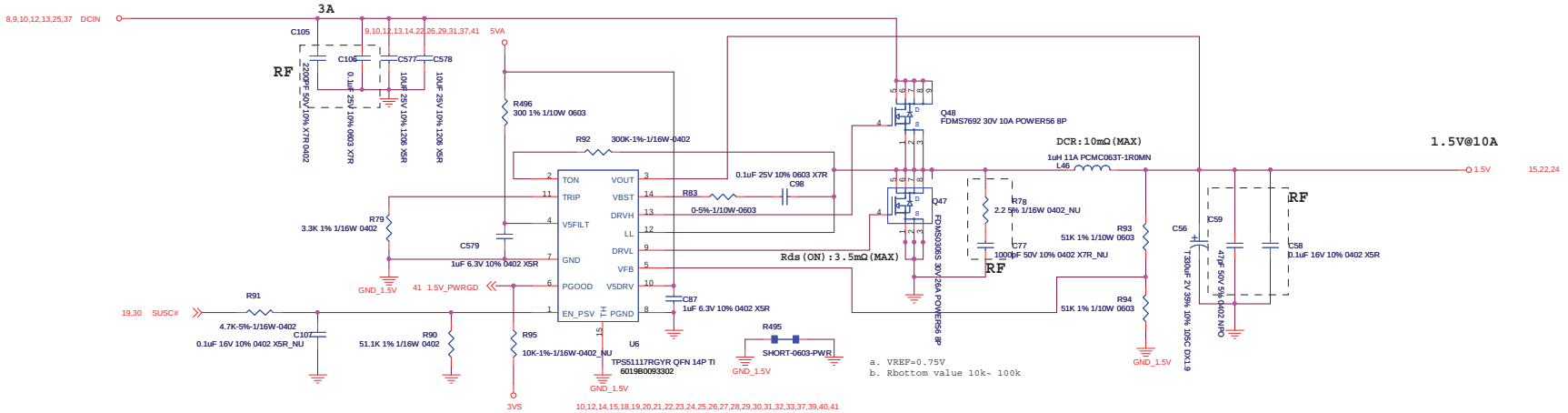
CHANGE by	IEC	DATE	Monday, May 24, 2010	SHEET	10 of 41

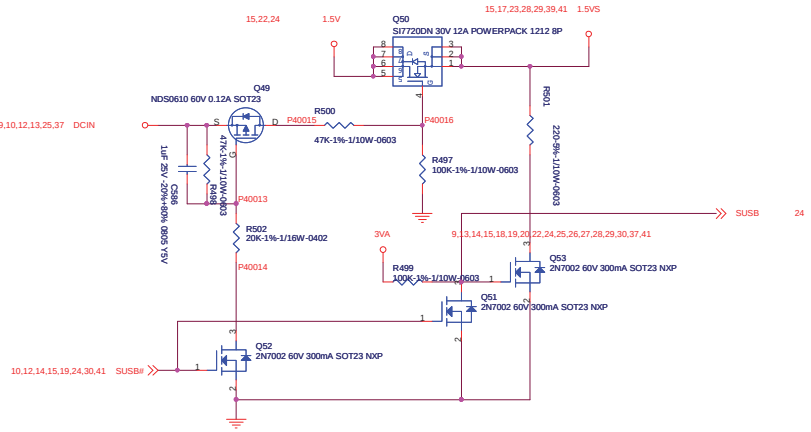
INVENTEC

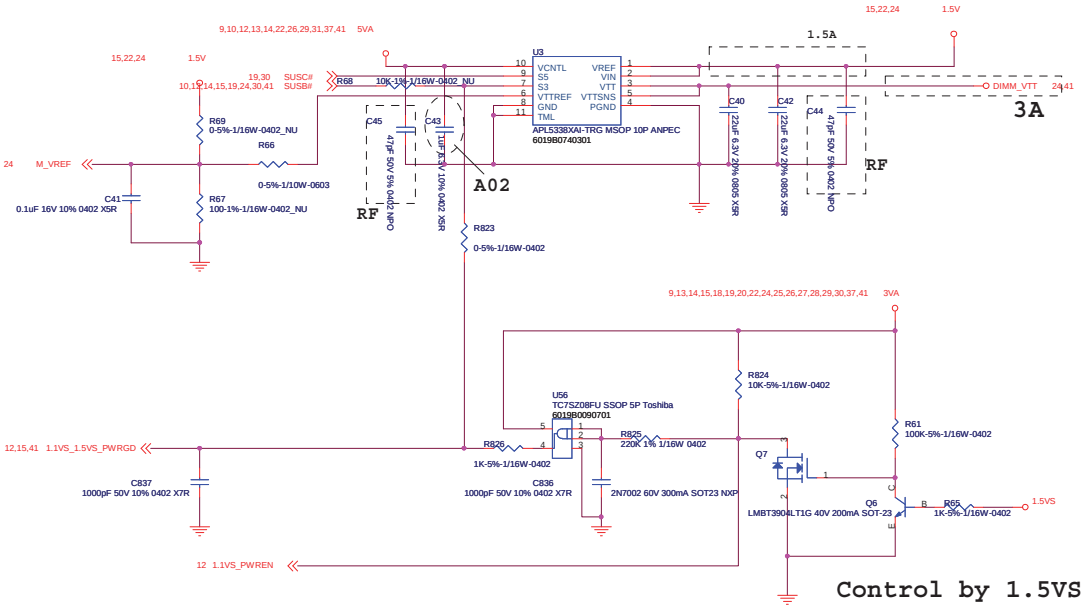
TITLE: Celpalla demo board) VGFX

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

DDR POWER







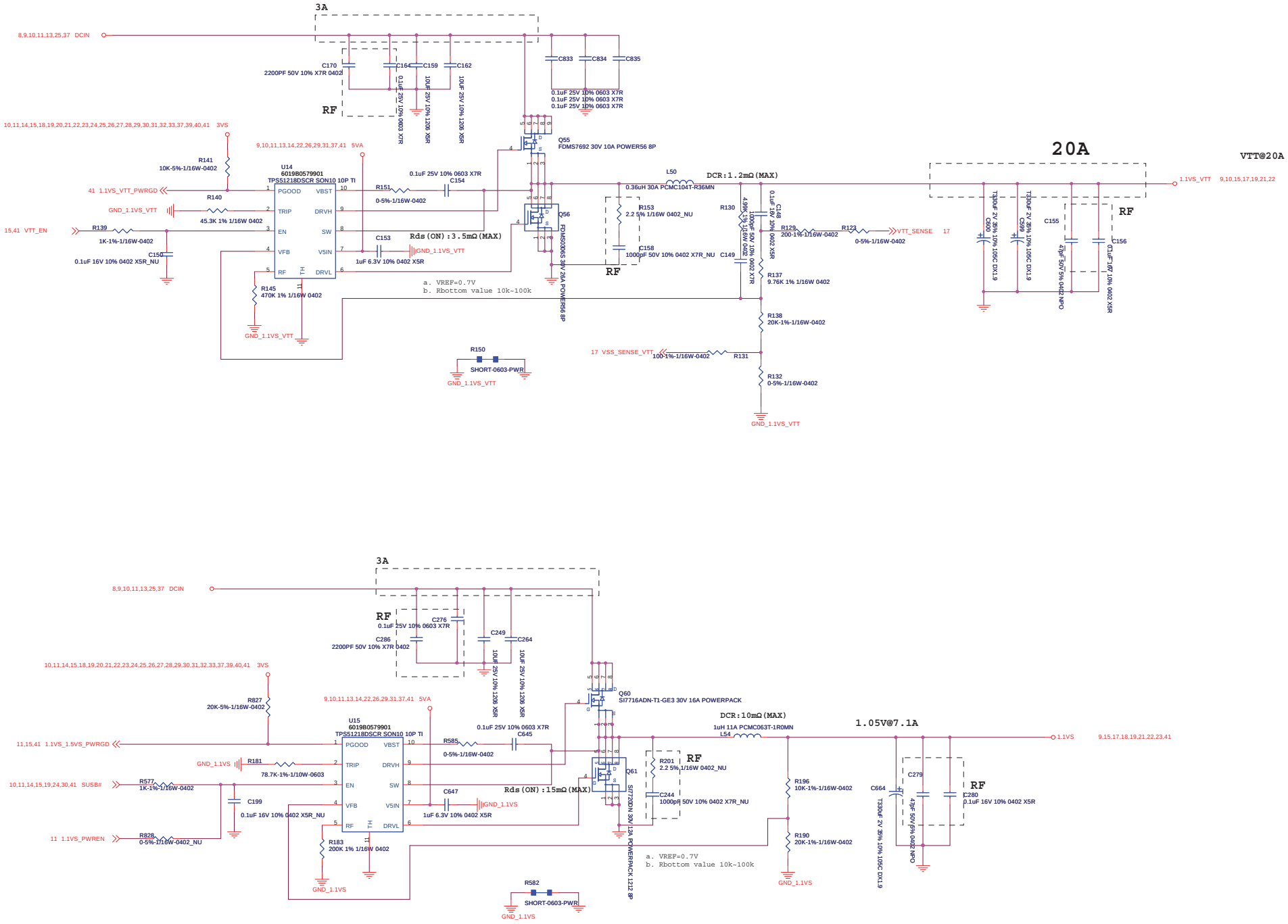
CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

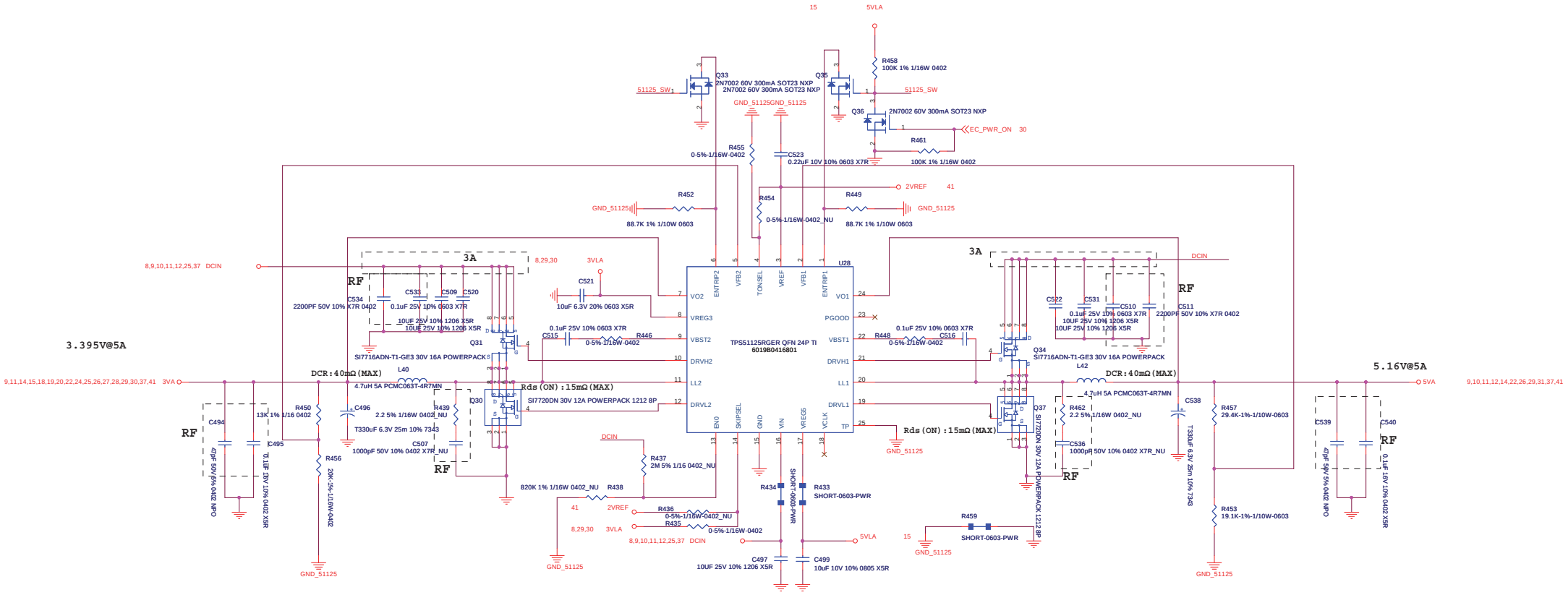
TITLE: Celpalla demo board)
DDR PWR

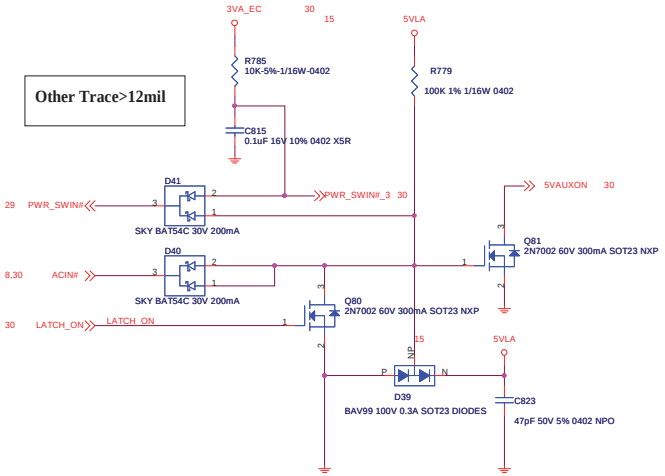
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 11 of 41

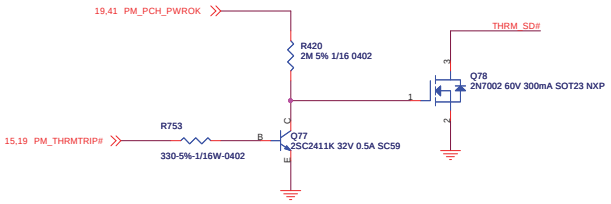


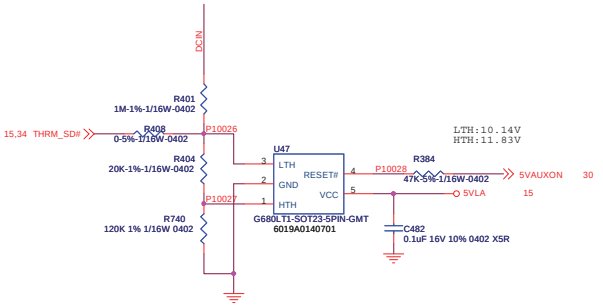
INVENTEC			
TITLE: Celpalla demo board)			
1.1VS_VTT/1.1VS			
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01
CHANGE by: IEC	DATE: Monday, May 24, 2010	SHEET: 12 of 41	





Temperature Security



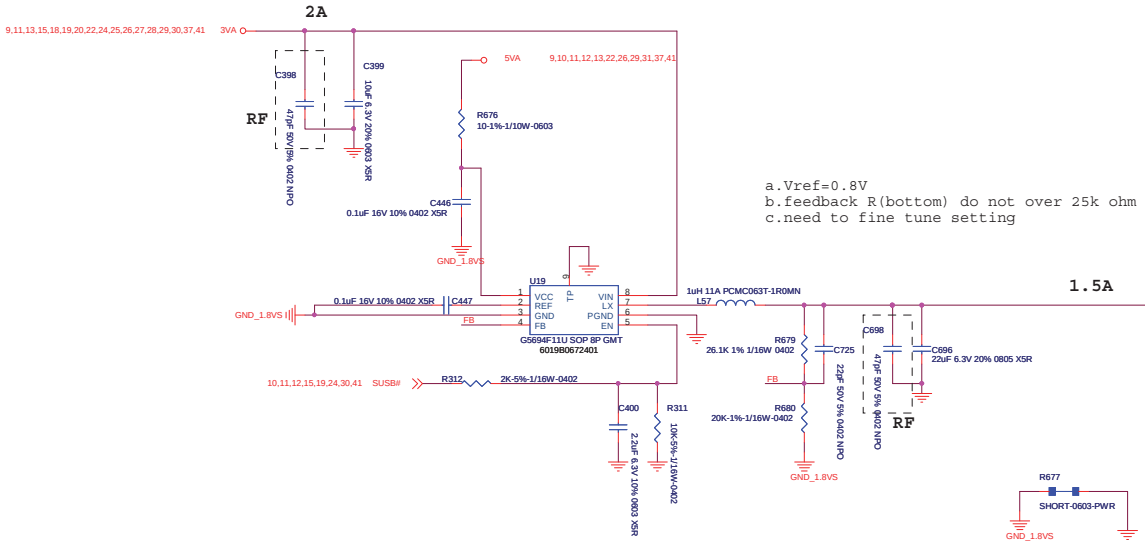


CHANGE by	IEC	DATE	Monday, May 24, 2010	
			SHEET	13 of 41

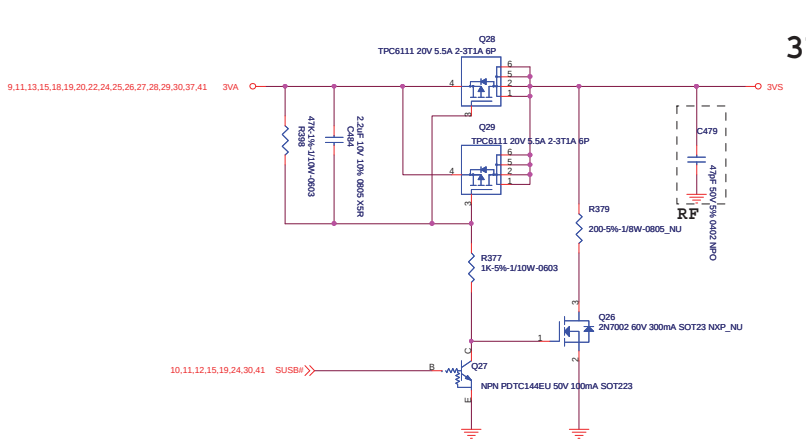
INVENTEC

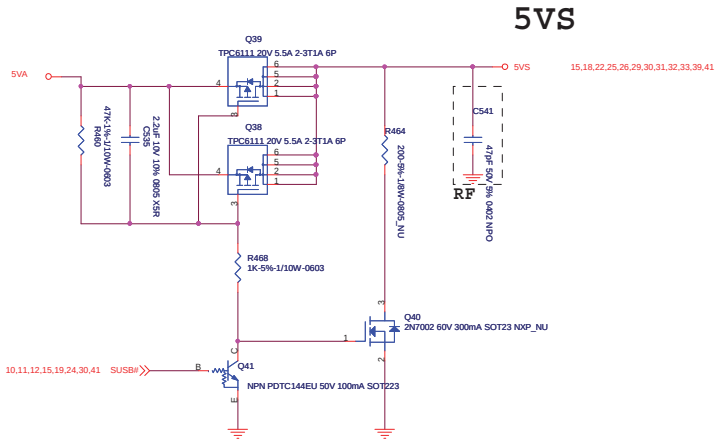
TITLE: Celpalla demo board)
5VA/5VLA/3VA/3VLA

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01



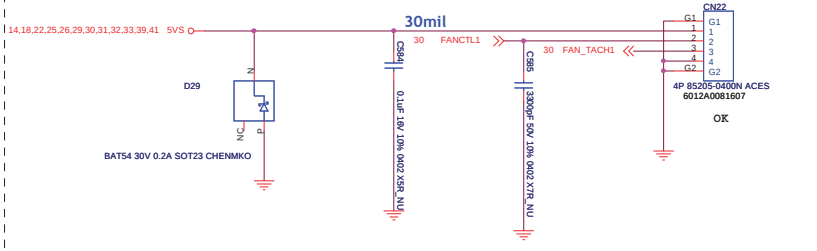
a.Vref=0.8V
b.feedback R(bottom) do not over 25k ohm
c.need to fine tune setting





INVENTEC					
TITLE: Celpalla demo board) '3VS/5VS/1.8VS/3VM					
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131		REV: X01	
CHANGE by: IEC	DATE: Monday, May 24, 2010	SHEET: 14	of	41	

Fan control



CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

TITLE: **BAP/BXP30**
Processor(1/4)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 15 of 41

6026B0154901-005

CN24C CN 989P CPU SKT 47989-0142 MOLEX

DDR SYSTEM MEMORY A

6026B0154901-005

CN24D CN 989P CPU SKT 47989-0142 MOLEX

DDR SYSTEM MEMORY - B

CN24H
CN 989P CPU SKT 47989-0142 MOLEX
6026B0154903

VSS

CN24I
CN 989P CPU SKT 47989-0142 MOLEX
6026B0154903

VSS

NCTF

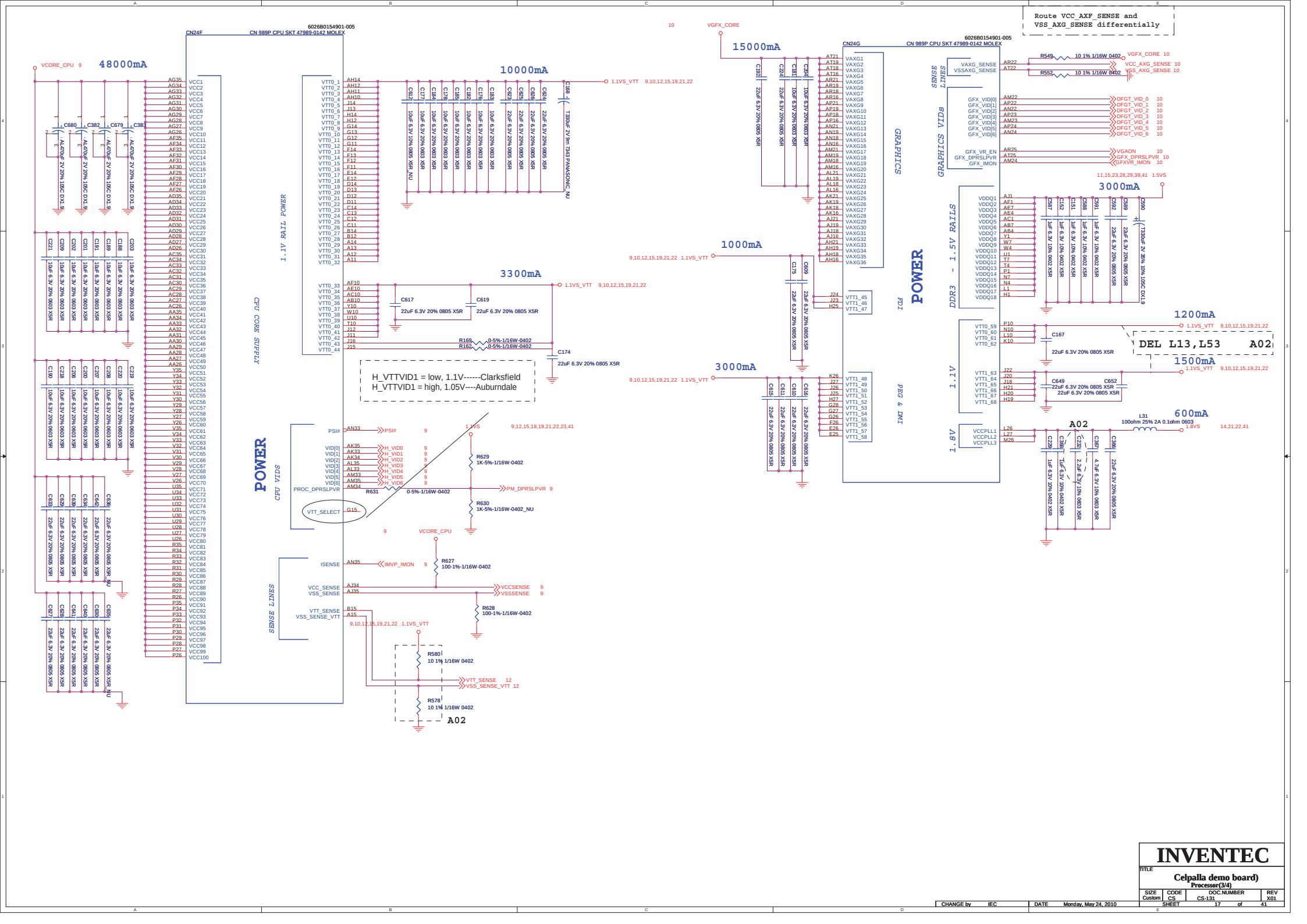
INVENTEC

TITLE

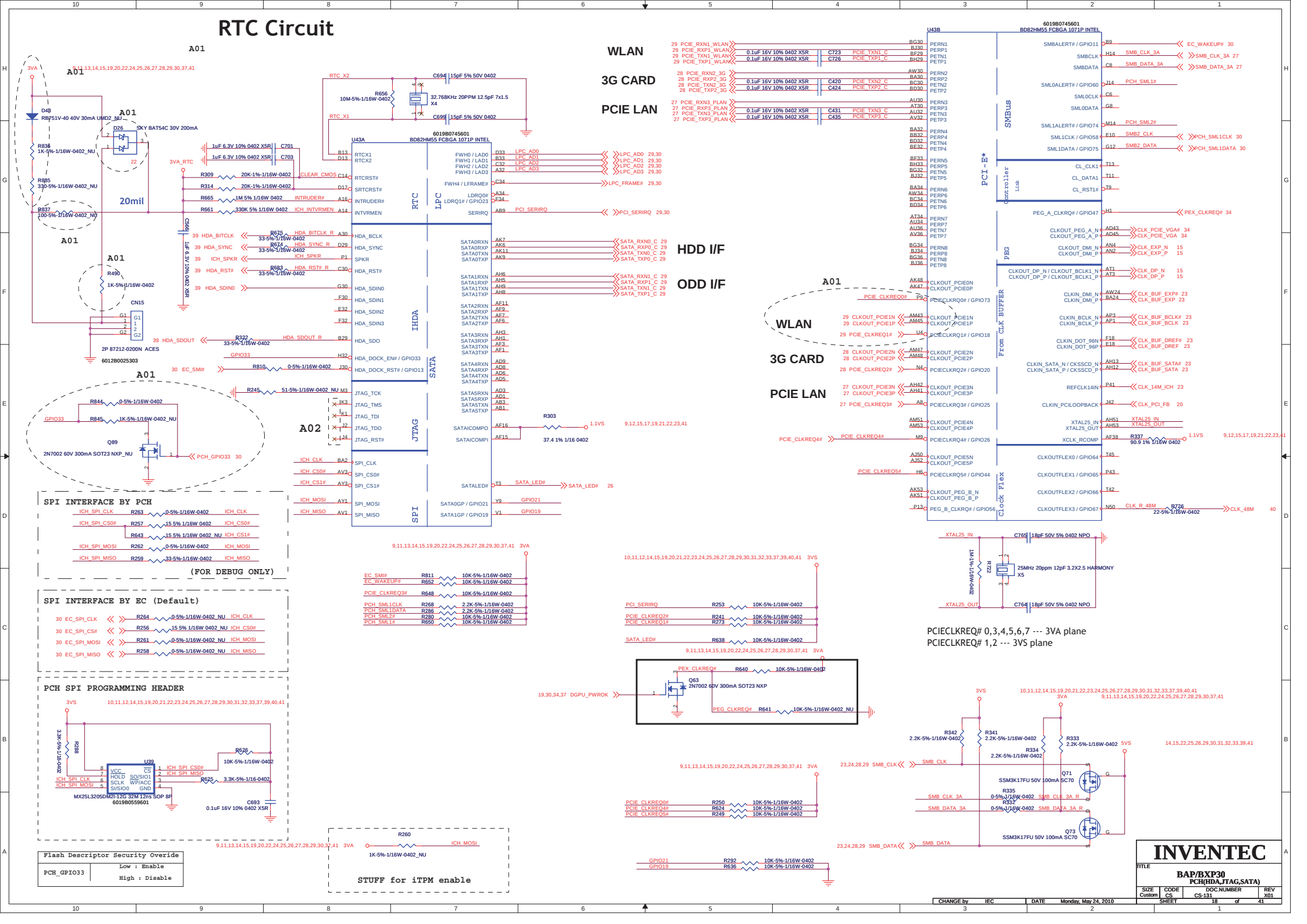
BAP/BXP30
Processor(2/4)

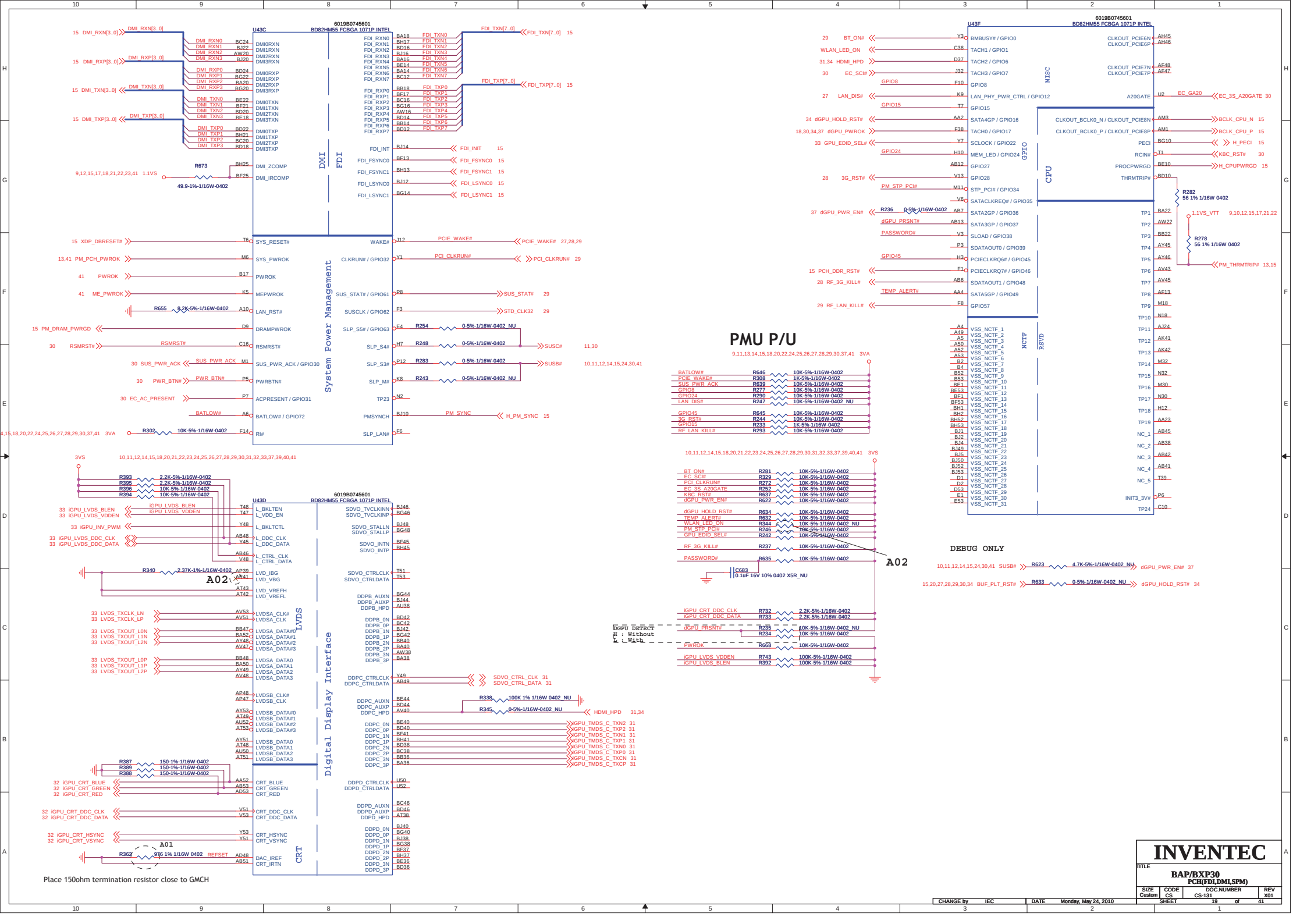
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

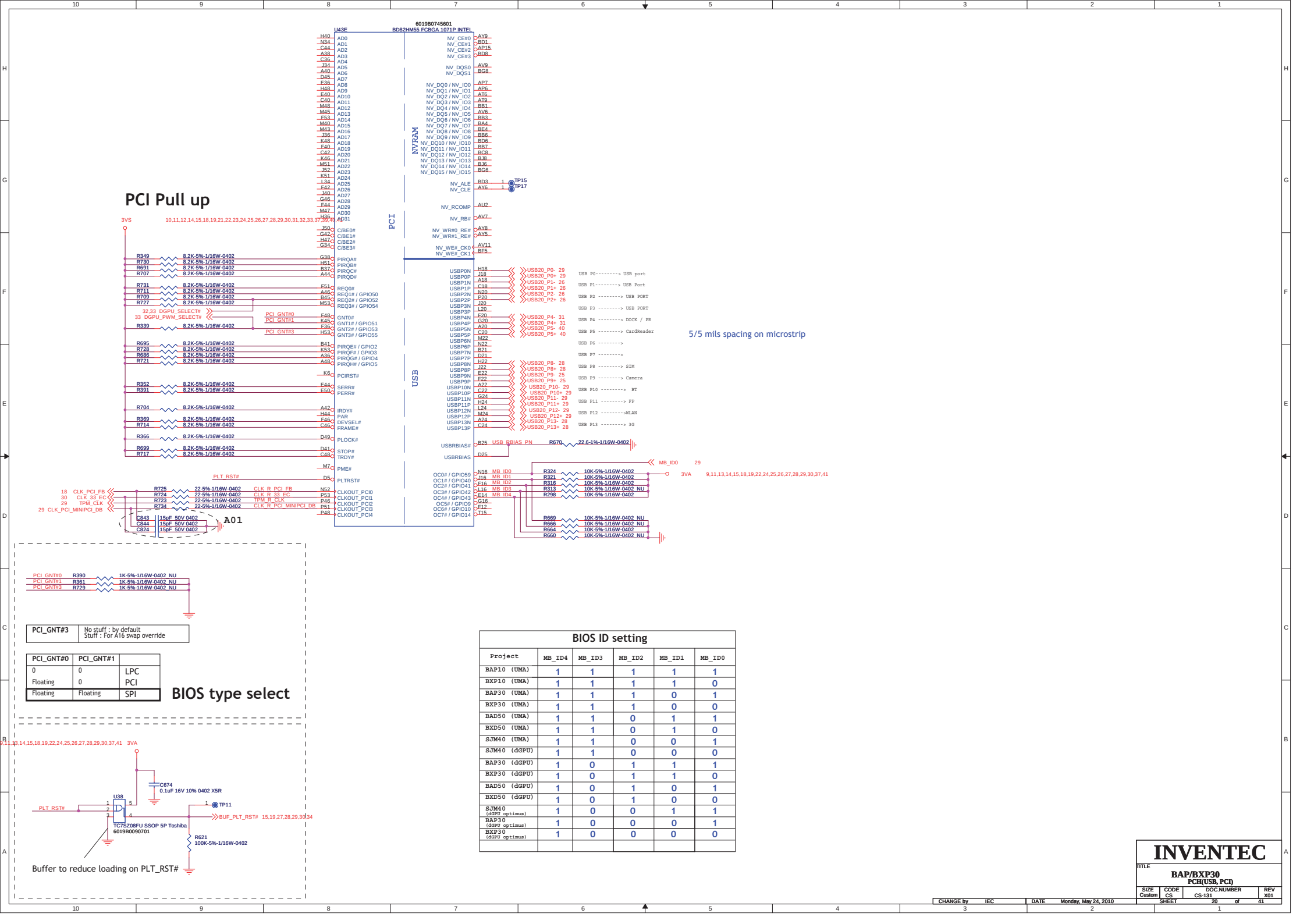
CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 16 of 41


Route VCC_AXF_SENSE and VSS_AXG_SENSE differentially
CN24F
6026B0154901-005
CN 989P CPU SKT 47989-0142 MOLEX
CN24G
6026B0154901-005
CN 989P CPU SKT 47989-0142 MOLEX
VCORE_CPU 9
48000mA
10000mA
3300mA
15000mA
1000mA
3000mA
1200mA
1500mA
600mA
1.1VS_VTT 9,10,12,15,19,21,22
VGFX_CORE 10
H_VTTVID1 = low, 1.1V------Clarksfield
H_VTTVID1 = high, 1.05V----Auburndale
DEL L13,L53 A02
A02
POWER
CPU VIDS
CPU CORE SUPPLY
1.1V RAIL POWER
GRAPHICS
FDI
PEG & DMI
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
INVENTEC
Celpalla demo board)
Processor(3/4)
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
CHANGE by IEC
DATE Monday, May 24, 2010
SHEET 17 of 41

RTC Circuit


A01
3VA
D4B
RB751V-40 40V 30mA UMD2_NU
D26
SKY BAT54C 30V 200mA
R836
1K-5%-1/16W-0402_NU
R885
330-5%-1/16W-0402_NU
R837
100-5%-1/16W-0402_NU
20mil
R490
1K-5%-1/16W-0402
CN15
2P 87212-0200N ACES
6012B0025303
R844
0-5%-1/16W-0402
R845
1K-5%-1/16W-0402_NU
Q89
2N7002 60V 300mA SOT23 NXP_NU
PCH_GPIO33 30
A02
SPI INTERFACE BY PCH
ICH_SPI_CLK R263 0-5%-1/16W-0402 ICH_CLK
ICH_SPI_CS0# R257 15 5% 1/16W 0402 ICH_CS0#
R643 15 5% 1/16W 0402_NU ICH_CS1#
ICH_SPI_MOSI R262 0-5%-1/16W-0402 ICH_MOSI
ICH_SPI_MISO R259 33-5%-1/16W-0402 ICH_MISO
(FOR DEBUG ONLY)
SPI INTERFACE BY EC (Default)
30 EC_SPI_CLK R264 0-5%-1/16W-0402_NU ICH_CLK
30 EC_SPI_CS# R256 15 5% 1/16W 0402_NU ICH_CS0#
30 EC_SPI_MOSI R261 0-5%-1/16W-0402_NU ICH_MOSI
30 EC_SPI_MISO R258 0-5%-1/16W-0402_NU ICH_MISO
PCH SPI PROGRAMMING HEADER
3VS
R28
3K-5%-1/16W-0402
U39
MX25L3205DM2I-12G 32M 12ns SOP 8P
6019B0559601
R626
10K-5%-1/16W-0402
R625
3.3K-5%-1/16-0402
C693
0.1uF 16V 10% 0402 X5R
Flash Descriptor Security Overide
PCH_GPIO33
Low : Enable
High : Disable
R260
1K-5%-1/16W-0402_NU
ICH_MOSI
STUFF for iTPM enable
RTC_X2
RTC_X1
C694 15pF 5% 50V 0402
C699 15pF 5% 50V 0402
R656
10M-5%-1/16W-0402
32.768KHz 20PPM 12.5pF 7x1.5
X4
1uF 6.3V 10% 0402 X5R C701
1uF 6.3V 10% 0402 X5R C703
3VA_RTC
R309 20K-1%-1/16W-0402 CLEAR_CMOS
R314 20K-1%-1/16W-0402
R665 1M 5% 1/16W 0402 INTRUDER#
R661 330K 5% 1/16W 0402 ICH_INTVRMEN
C686 1uF 6.3V 10% 0402 X5R
6019B0745601
BD82HM55 FCBGA 1071P INTEL
U43A
RTC
LPC
IHDA
SATA
JTAG
SPI
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
LDRQ1# / GPIO23
SERIRQ
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_RST#
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
SATA0GP / GPIO21
SATA1GP / GPIO19
R303
37.4 1% 1/16 0402
1.1VS
SATA_LED#
GPIO21
GPIO19
WLAN
3G CARD
PCIE LAN
HDD I/F
ODD I/F
U43B
BD82HM55 FCBGA 1071P INTEL
SMBus
PCI-E*
Controller
Link
PEG
From CLK BUFFER
Clock Flex
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67
PCIECLKRQ0# / GPIO73
PCIECLKRQ1# / GPIO18
PCIECLKRQ2# / GPIO20
PCIECLKRQ3# / GPIO25
PCIECLKRQ4# / GPIO26
PCIECLKRQ5# / GPIO44
PEG_B_CLKRQ# / GPIO56
PCIE_CLKREQ0#
PCIE_CLKREQ1#
PCIE_CLKREQ2#
PCIE_CLKREQ3#
PCIE_CLKREQ4#
PCIE_CLKREQ5#
WLAN
3G CARD
PCIE LAN
C765 18pF 50V 5% 0402 NPO
C764 18pF 50V 5% 0402 NPO
R722 20K-1%-1/16W-0402
25MHz 20ppm 12pF 3.2X2.5 HARMONY
X5
PCIECLKREQ# 0,3,4,5,6,7 --- 3VA plane
PCIECLKREQ# 1,2 --- 3VS plane
PEX_CLKREQ#
Q63
2N7002 60V 300mA SOT23 NXP
PEG_CLKREQ#
19,30,34,37 DGPU_PWROK
R342 2.2K-5%-1/16W-0402
R341 2.2K-5%-1/16W-0402
R333 2.2K-5%-1/16W-0402
R334 2.2K-5%-1/16W-0402
SMB_CLK
SMB_CLK_3A
SMB_DATA_3A
SMB_CLK_3A_R
SMB_DATA_3A_R
R335 0-5%-1/16W-0402
R332 0-5%-1/16W-0402
Q71
SSM3K17FU 50V 100mA SC70
Q73
SSM3K17FU 50V 100mA SC70
23,24,28,29 SMB_CLK
23,24,28,29 SMB_DATA
5VS
3VS
3VA
INVENTEC
TITLE
BAP/BXP30
PCH(HDA,JTAG,SATA)
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
SHEET 18 of 41
CHANGE by IEC
DATE Monday, May 24, 2010


U43C
6019B0745601
BD82HM55 FCBGA 1071P INTEL
DMI
FDI
System Power Management
U43D
LVDS
Digital Display Interface
CRT
U43F
GPIO
CPU
MISC
NCTF
RSVD
PMU P/U
A02
A01
DEBUG ONLY
Place 150ohm termination resistor close to GMCH
INVENTEC
BAP/BXP30
PCH(FDI,DMI,SPM)
CHANGE by IEC
DATE Monday, May 24, 2010
SHEET 19 of 41



BIOS ID setting

Project	MB_ID4	MB_ID3	MB_ID2	MB_ID1	MB_ID0
BAP10 (UMA)	1	1	1	1	1
BXP10 (UMA)	1	1	1	1	0
BAP30 (UMA)	1	1	1	0	1
BXP30 (UMA)	1	1	1	0	0
BAD50 (UMA)	1	1	0	1	1
BXD50 (UMA)	1	1	0	1	0
SJM40 (UMA)	1	1	0	0	1
SJM40 (dGPU)	1	1	0	0	0
BAP30 (dGPU)	1	0	1	1	1
BXP30 (dGPU)	1	0	1	1	0
BAD50 (dGPU)	1	0	1	0	1
BXD50 (dGPU)	1	0	1	0	0
SJM40 (dGPU optimus)	1	0	0	1	1
BAP30 (dGPU optimus)	1	0	0	0	1
BXP30 (dGPU optimus)	1	0	0	0	0

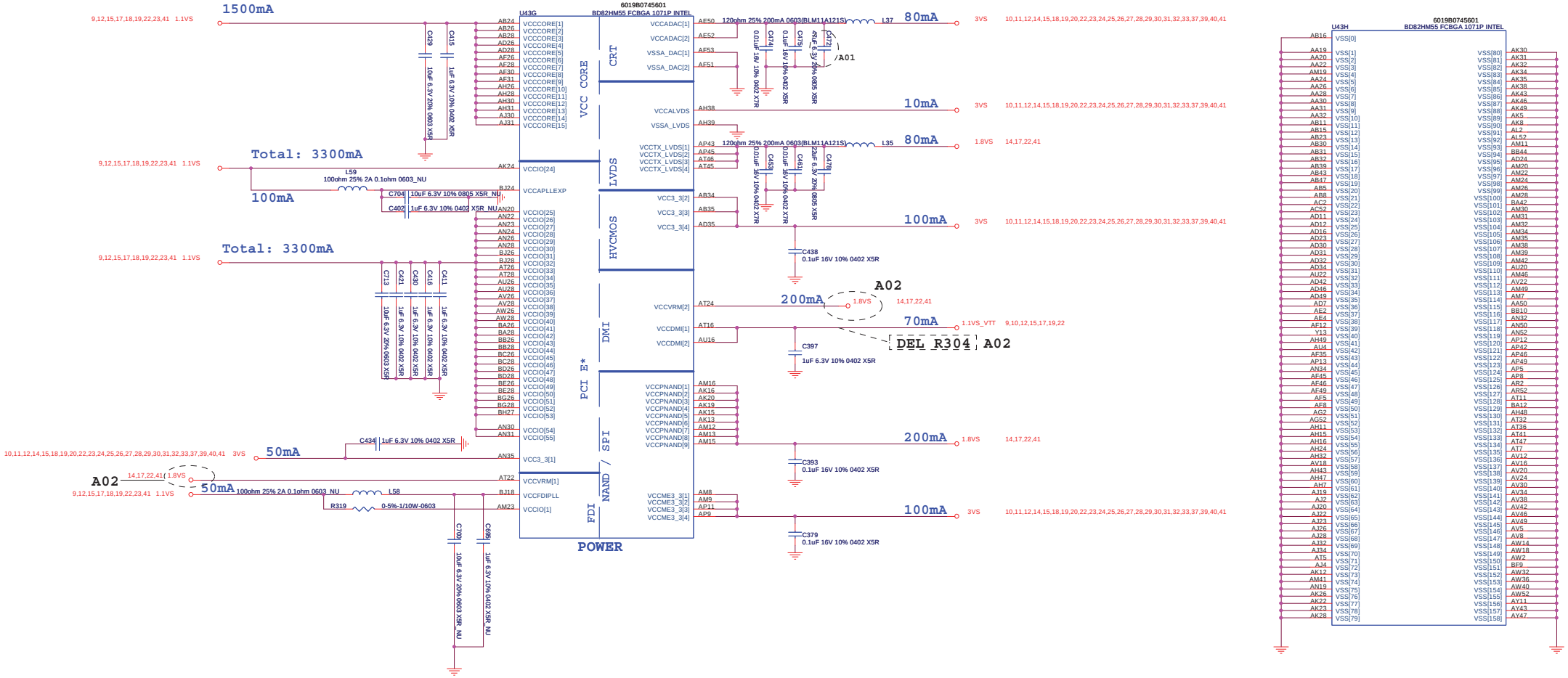
INVENTEC

TITLE: BAP/BXP30 PCH(USB, PCI)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 20 of 41

CHANGE by IEC DATE Monday, May 24, 2010



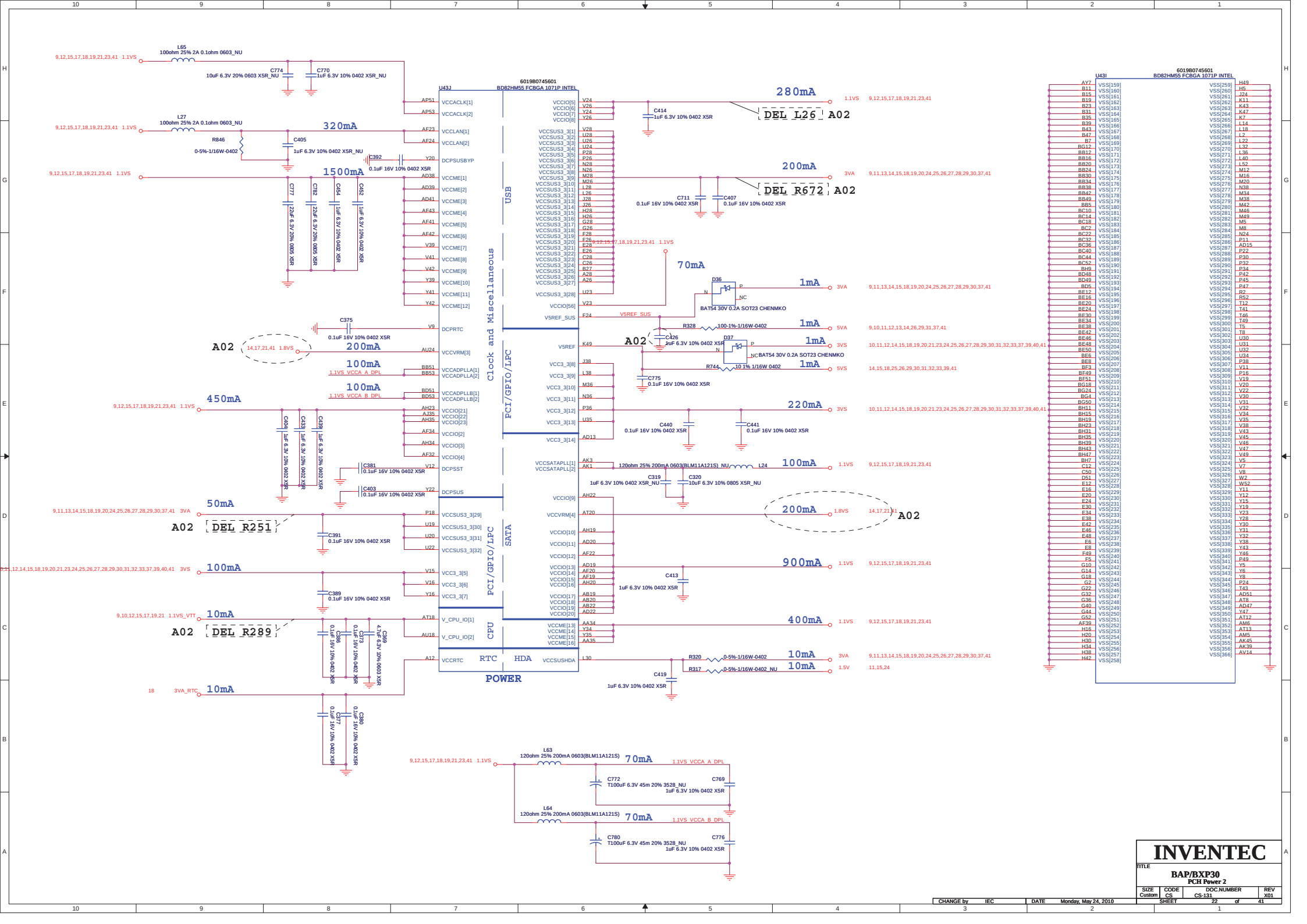
CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

TITLE: BAP/BXP30
PCH Power 1

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 21 of 41



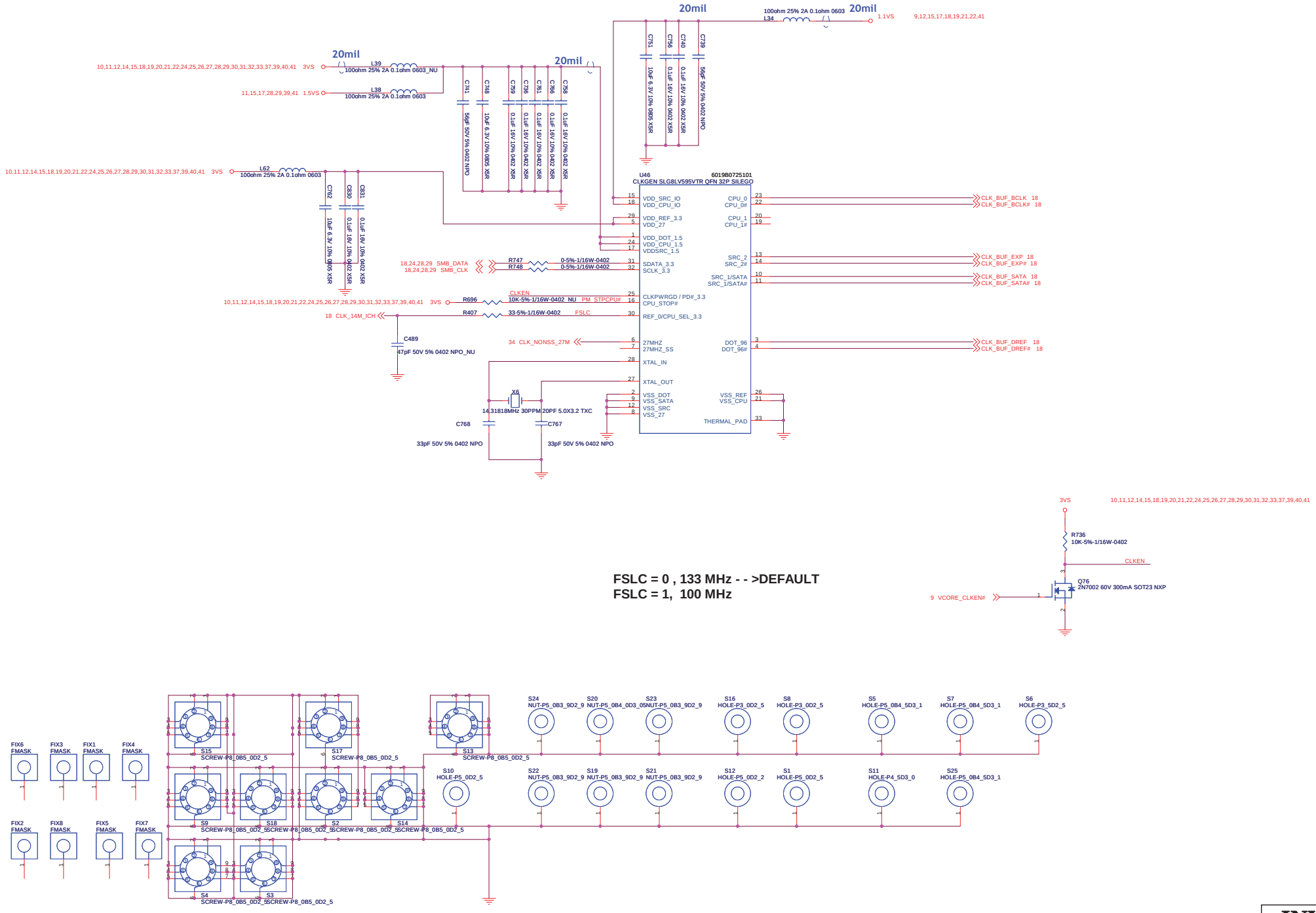
CHANGE by	IEC	DATE	Monday, May 24, 2010

INVENTEC

TITLE: BAP/BXP30
PCH Power 2

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 22 of 41



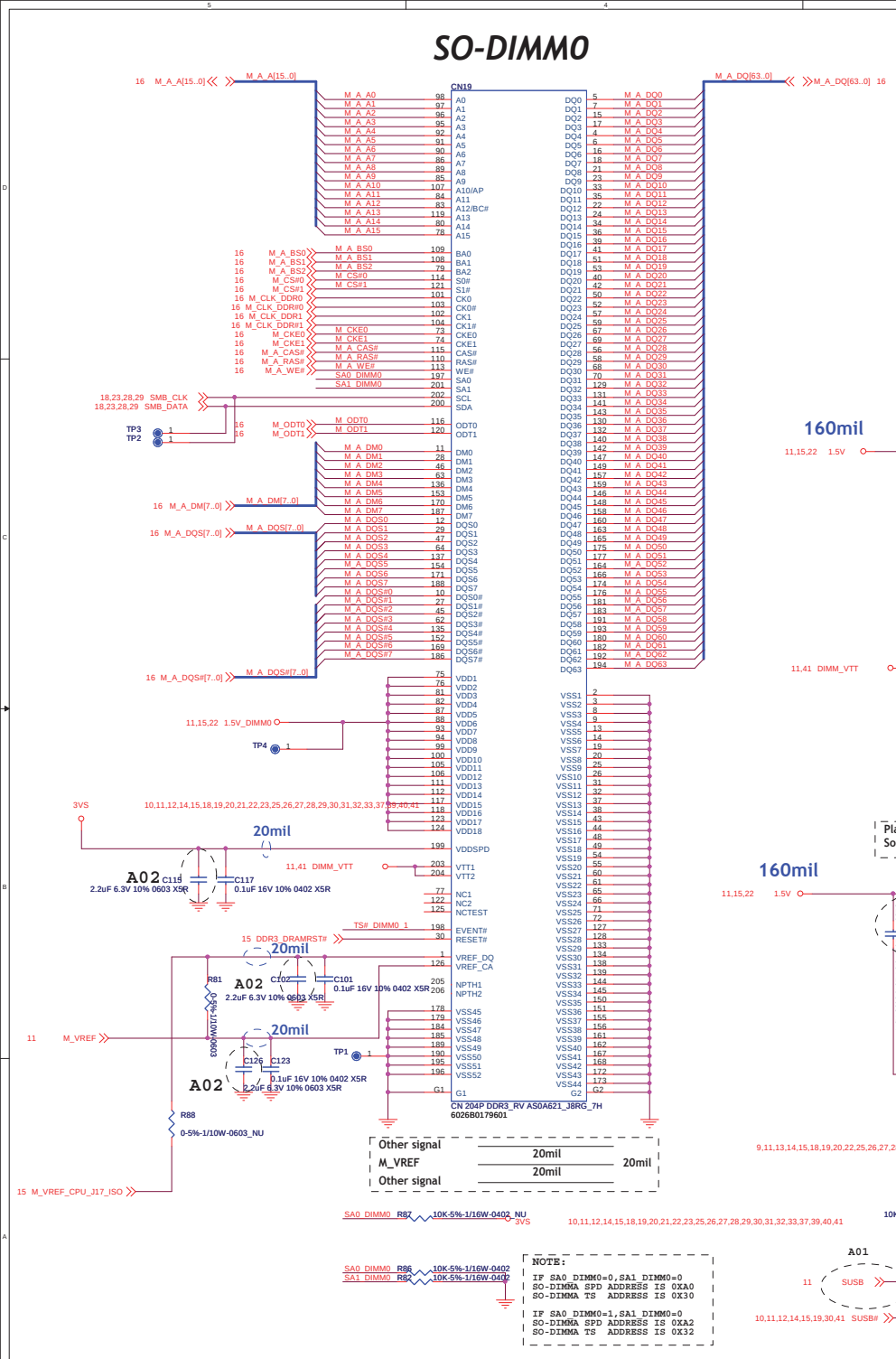
INVENTEC

TITLE: BAP/BXP30
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 23 of 41

SO-DIMM0



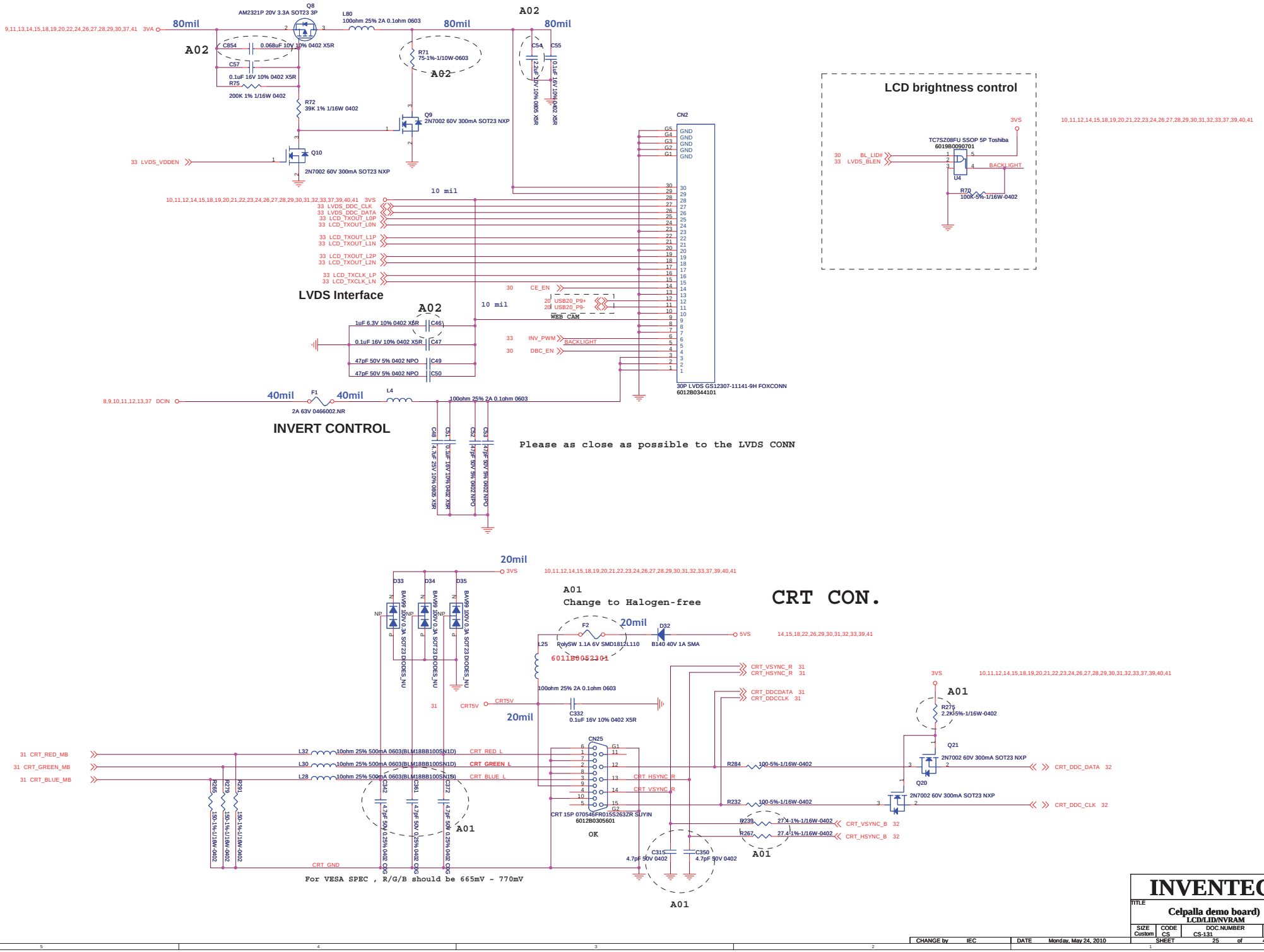
SO-DIMM1

CHANGE by	IEC	DATE	Monday, May 24, 2010	
			SHEET	24 of 41

INVENTEC

TITLE: BAP/BXP30
DDR3 SDRAM SO-DIMM 0/1

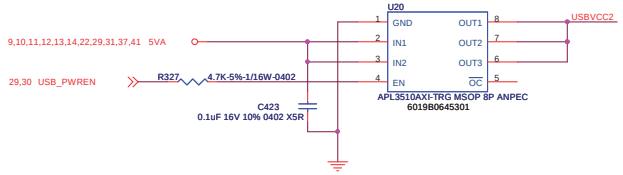
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

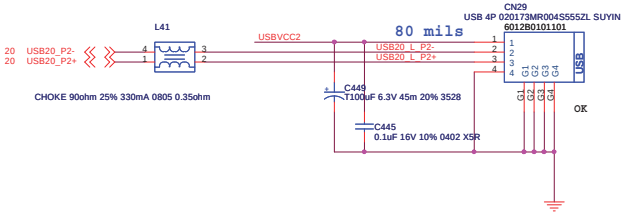


TITLE	Celpalla demo board) LCD/LID/NVRAM		
SIZE Custom	CODE CS	DOC.NUMBER CS-131	REV X01
CHANGE by IEC	DATE Monday, May 24, 2010	SHEET 25 of 41	

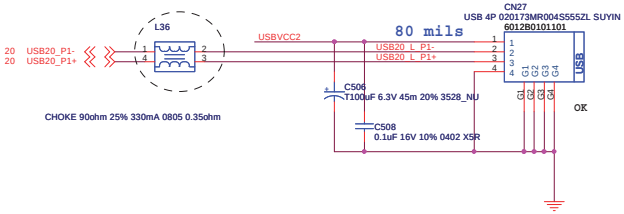
INVENTEC

USB

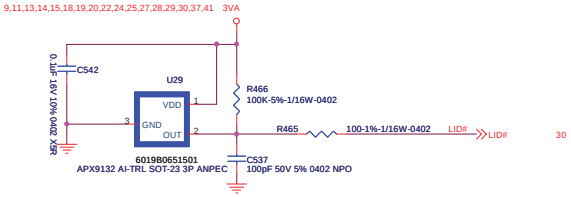


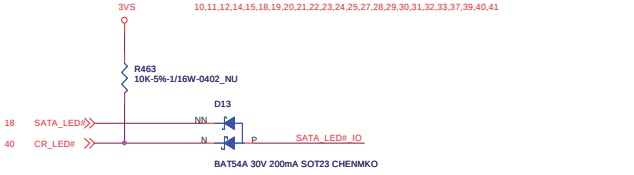


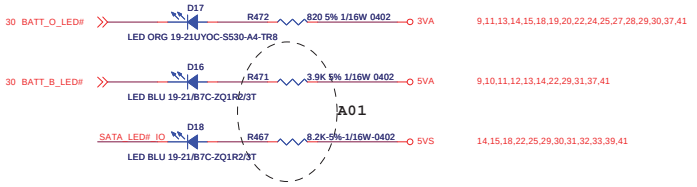
move to bottom side

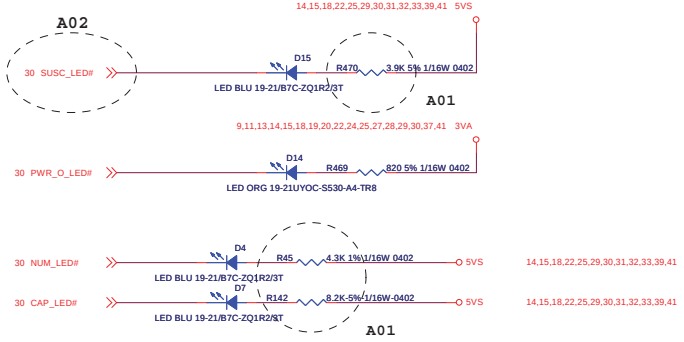


HALL Switch

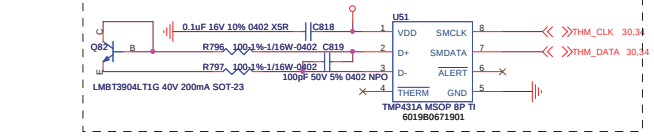




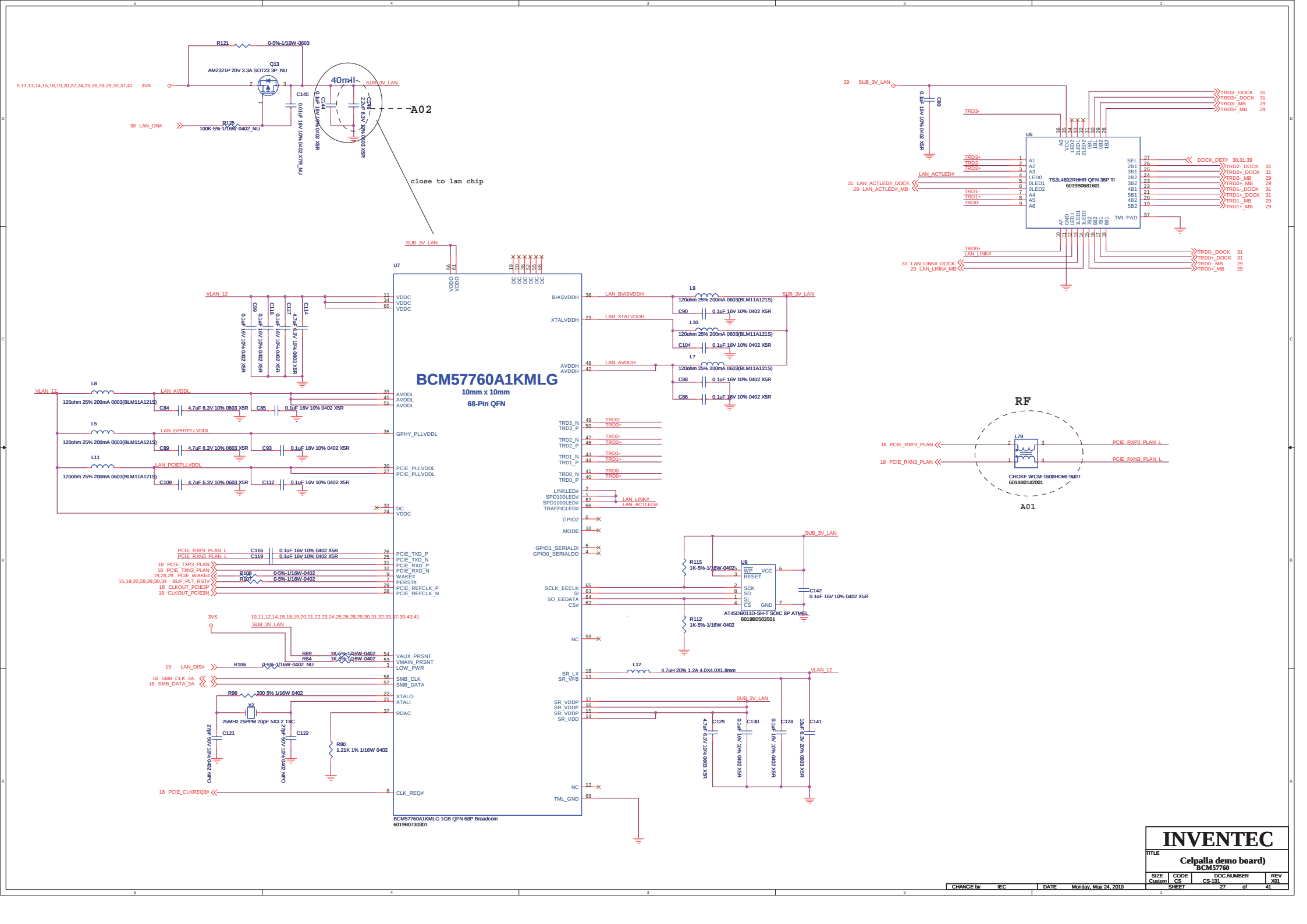




REMOTE thermal sensor
Place near the hottest spot area under Palm-rest



CHANGE by	IEC	DATE	Monday, May 24, 2010	
INVENTEC				
TITLE	BAP/BXP30			
	HDD/DAUGHTER CONNECTOR			
SIZE	CODE	DOC.NUMBER		REV
Custom	CS	CS-131		X01
		SHEET	26 of 41	



CHANGE by	IEC	DATE	Monday, May 24, 2010

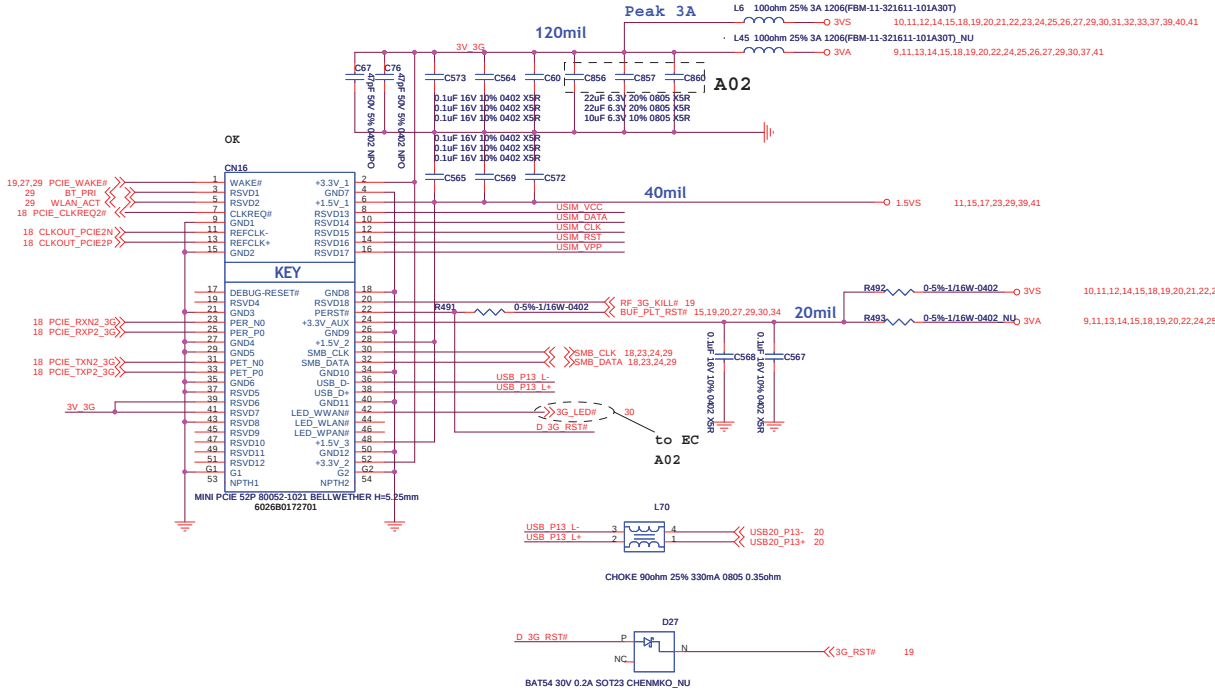
INVENTEC

TITLE: Celpalla demo board)
BCM57760

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

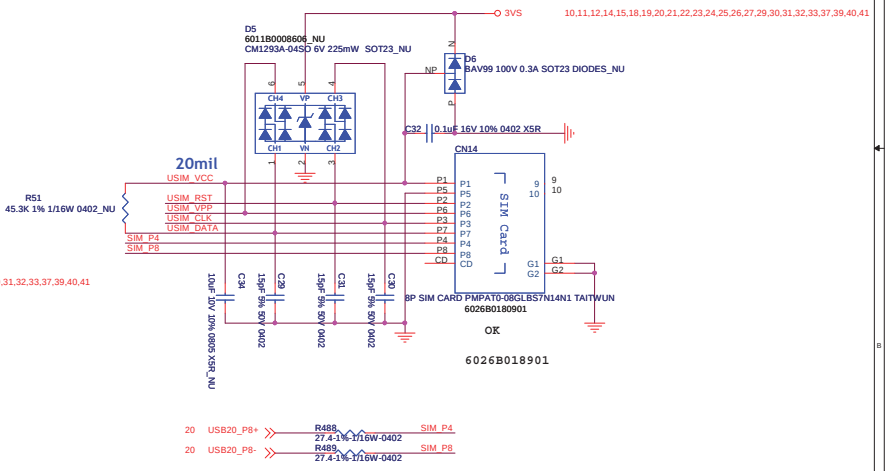
SHEET 27 of 41

PCIE Mini Card for 3G



On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.

SIM CARD slot



CHANGE by	IEC	DATE	Monday, May 24, 2010	

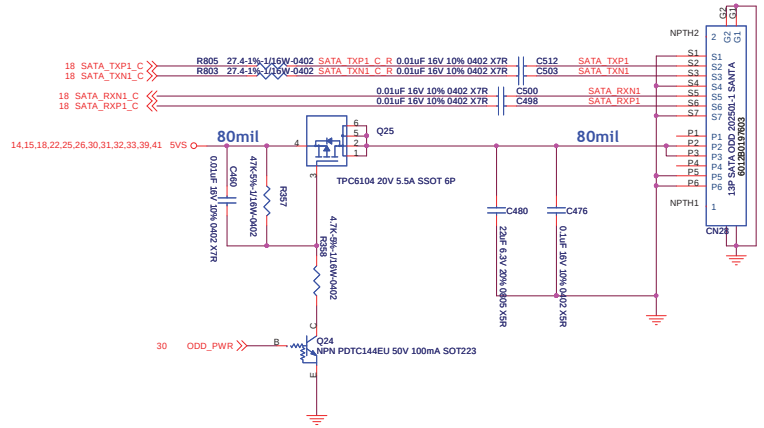
INVENTEC

TITLE: BAP/BXP30 WLAN/3G

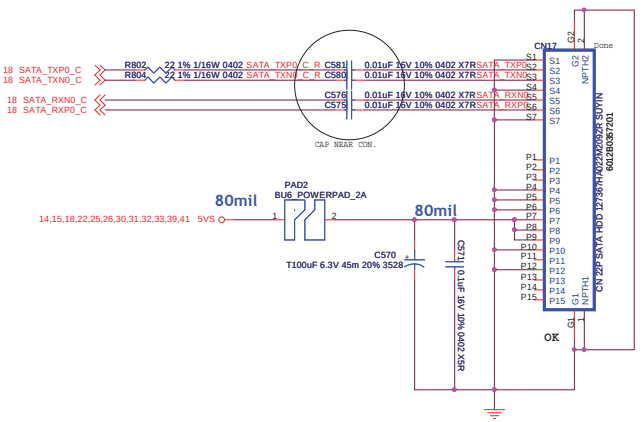
SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

SHEET 28 of 41

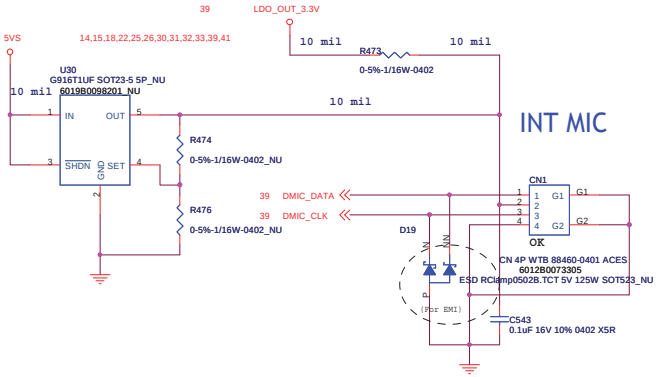
ODD I/F



HDD I/F

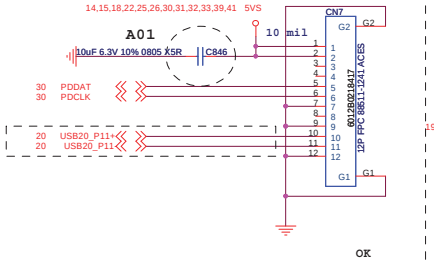


DMIC CNN

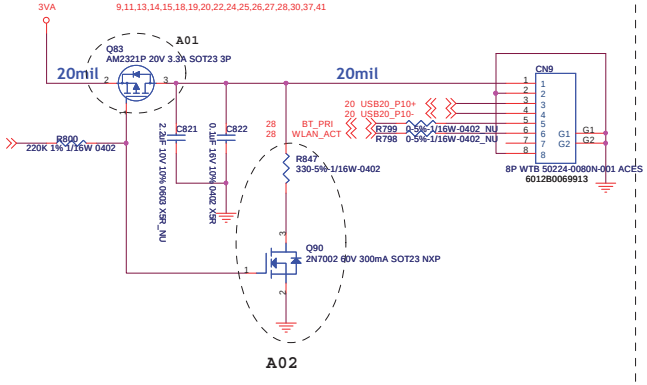


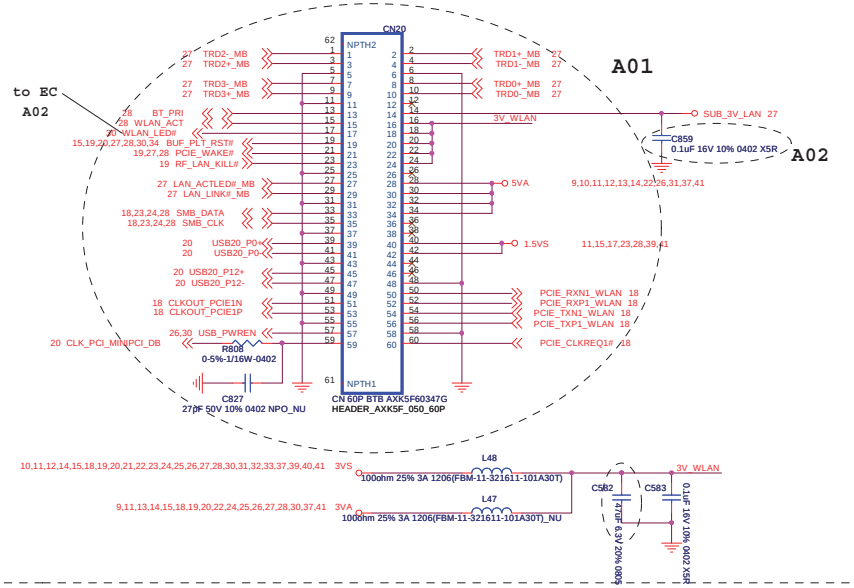
TO USB/WLAN BOARD

GP + FP CNN.

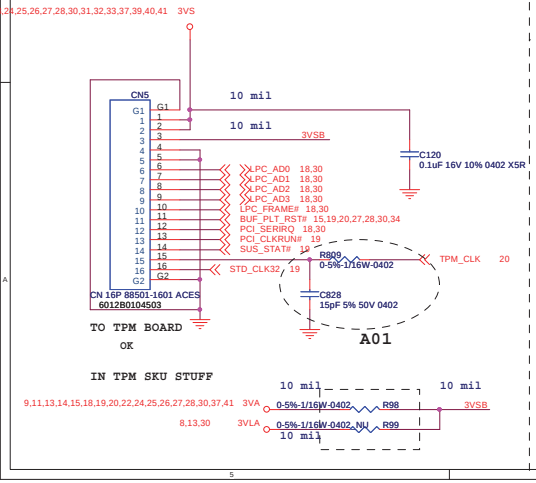


Bluetooth CNN.

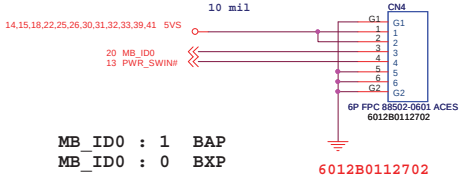




TPM CNN



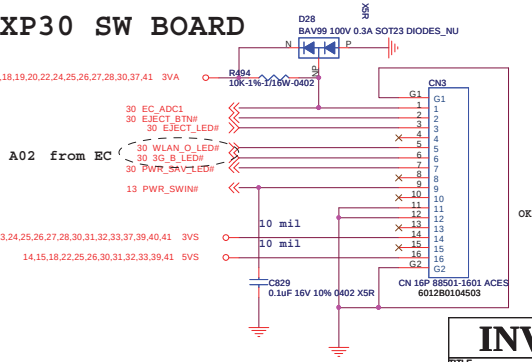
FOR BXP30 POWER BUTTON BOARD



MB_ID0 : 1 BAP
MB_ID0 : 0 BXP

6012B0112702

FOR BAP/BXP30 SW BOARD

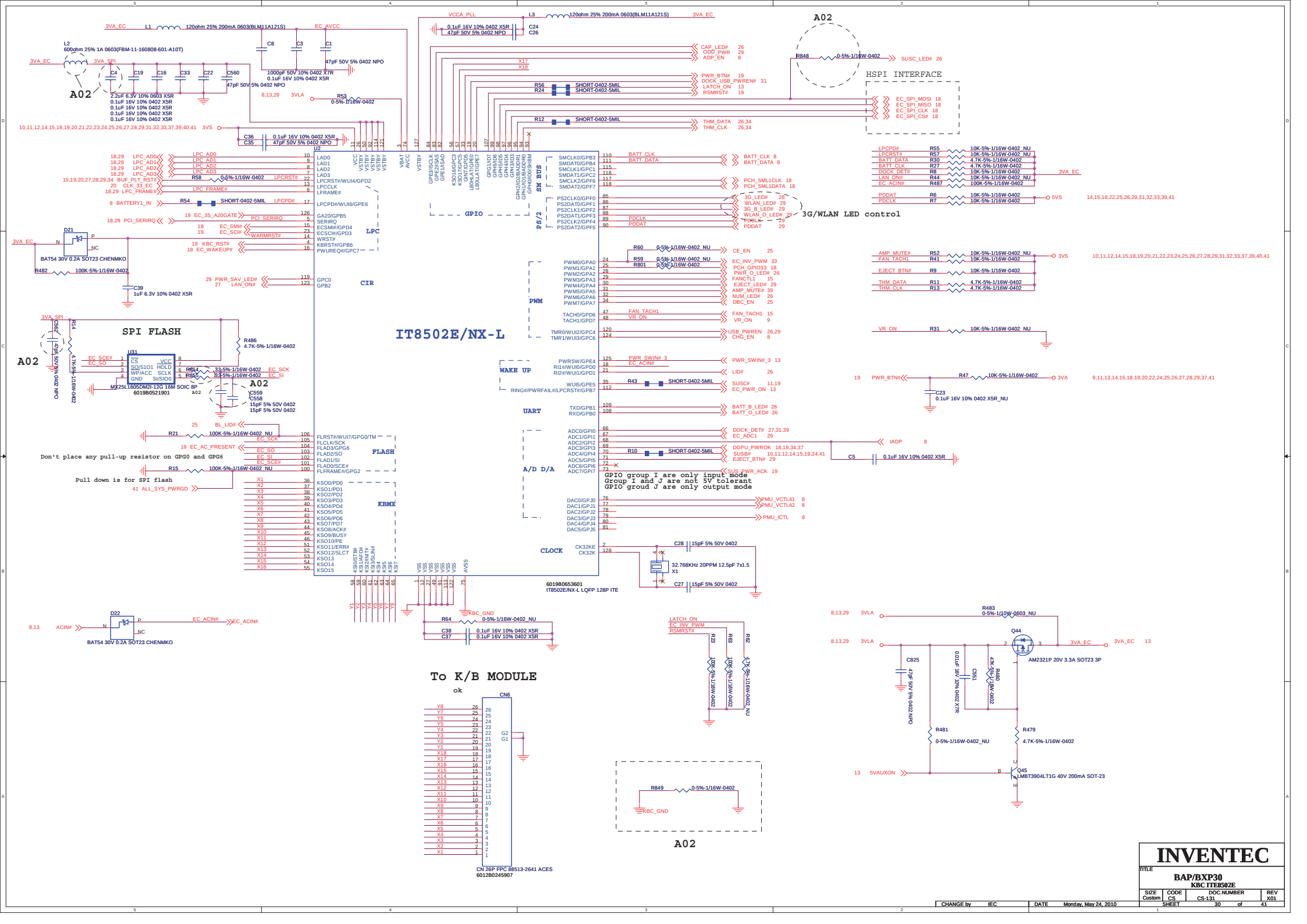


INVENTEC

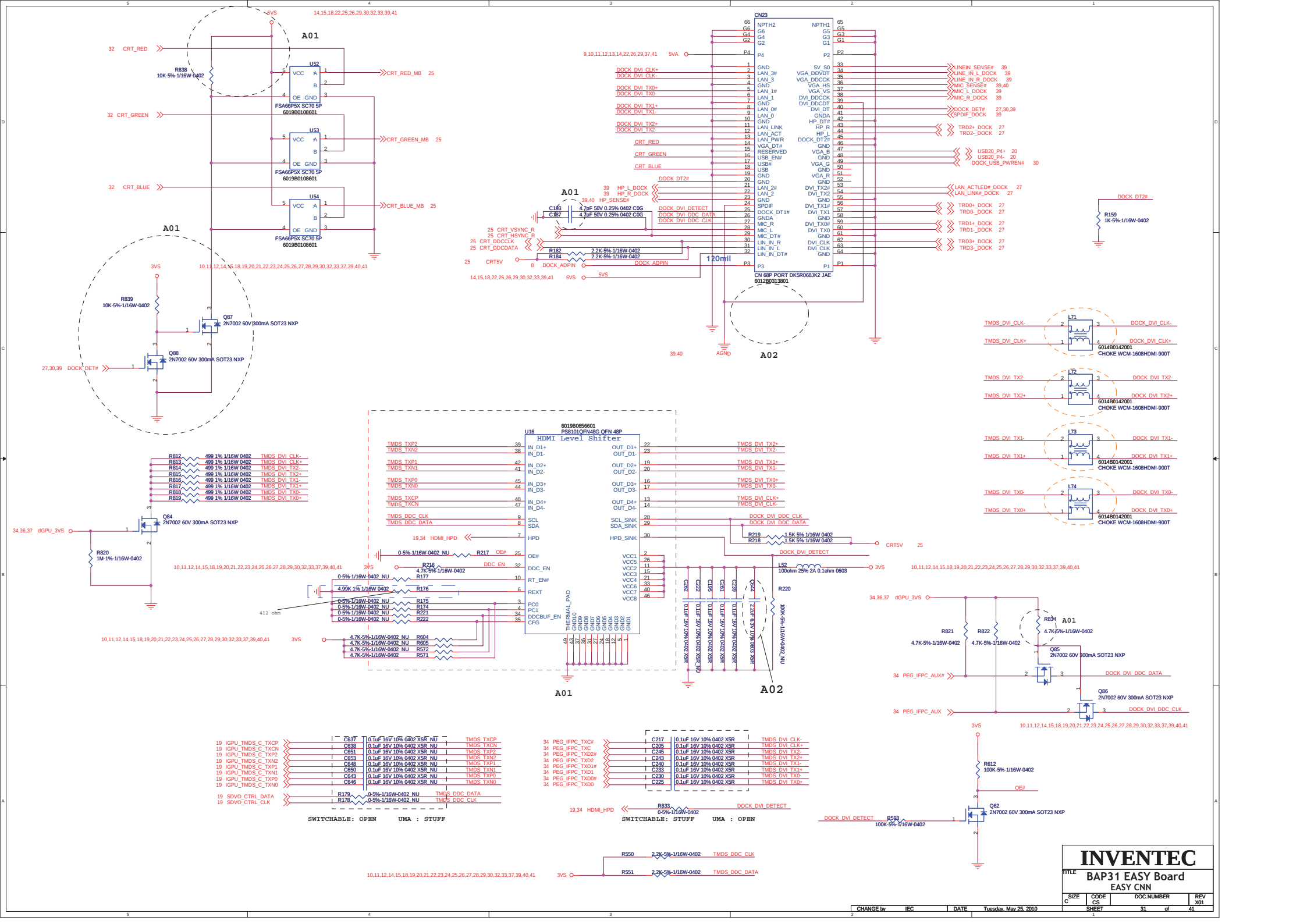
TITLE: Celpalla demo board)
USB/eSATA/G-sensor/CON

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

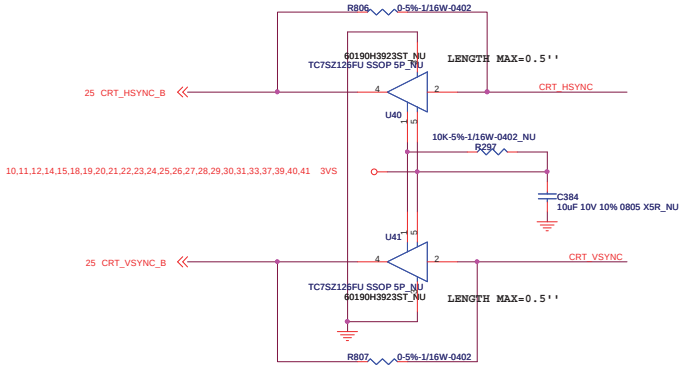
CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 29 of 41

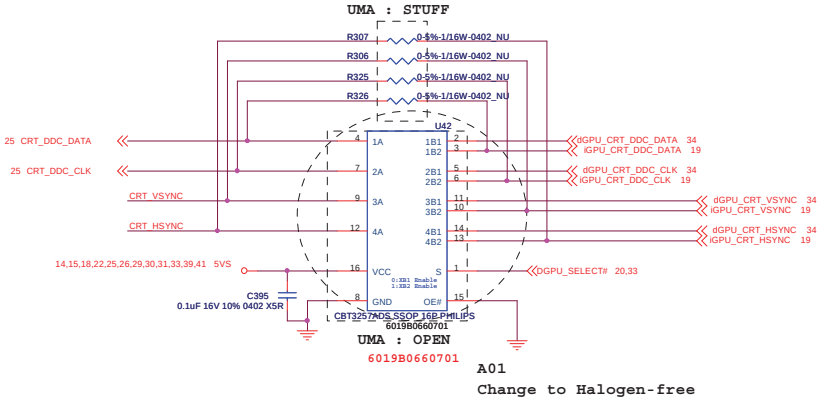


CHANGE by	IEC	DATE	Monday, May 24, 2010
SIZE: Custom	CODE: CS	DOC.NUMBER: CS-131	REV: X01
		SHEET 30 of 41	

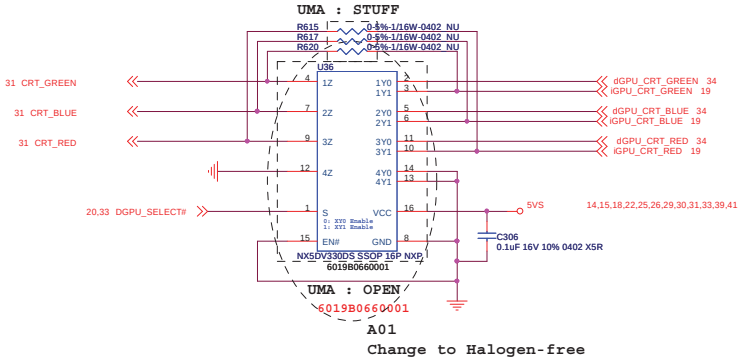

A01
A02
CN23
CN 68P PORT DK5R068JK2 JAE
6012B0313801
U52
U53
U54
FSA66P5X SC70 5P
6019B0108601
U16
6019B0656601
PS8101QFN48G QFN 48P
HDMI Level Shifter
SWITCHABLE: OPEN UMA : STUFF
SWITCHABLE: STUFF UMA : OPEN
INVENTEC
BAP31 EASY Board
EASY CNN
SIZE C
CODE CS
DOC.NUMBER
REV X01
SHEET 31 of 41
CHANGE by IEC
DATE Tuesday, May 25, 2010

CRT HSYNC/VSYNC SW For Dock





CRT HSYNC/VSYNC/DDC SW



CRT R/G/B SW

Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
DGPU_PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
GPU_EDID_SEL#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

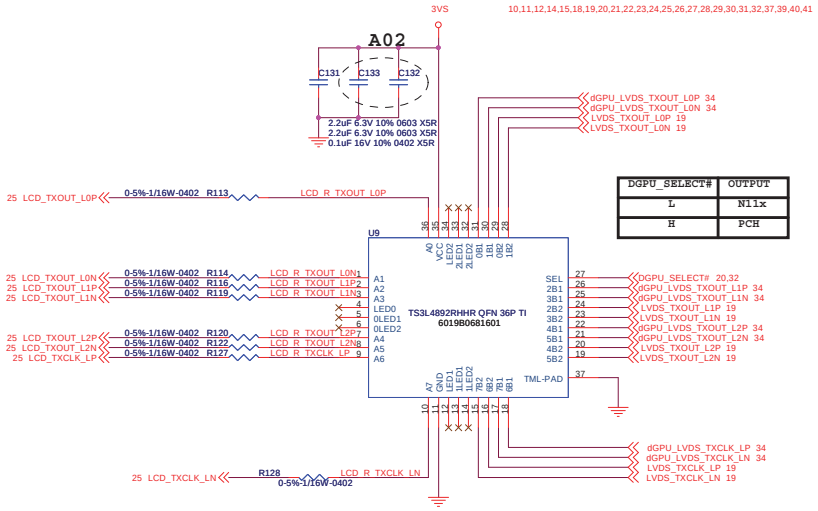
INVENTEC

TITLE: BAP/BXP30
Hybird Switch (1/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

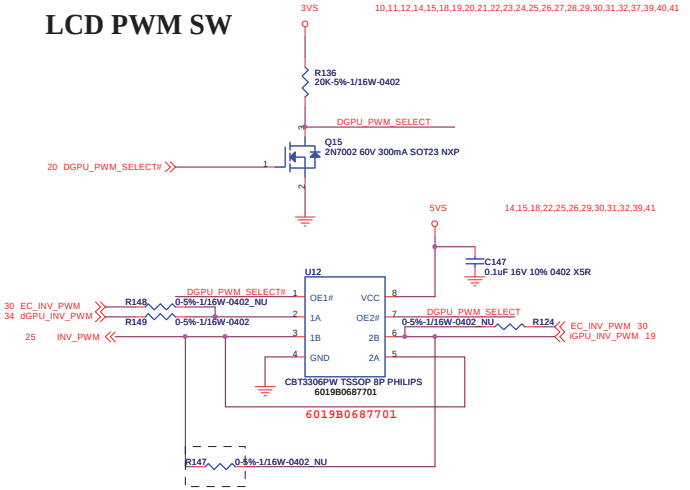
CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 32 of 41

LVDS SW



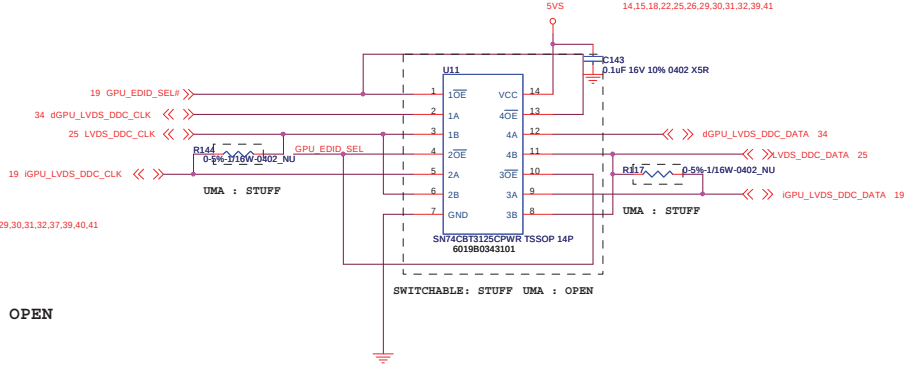
DGPU_SELECT#	OUTPUT
L	N11x
H	PCH

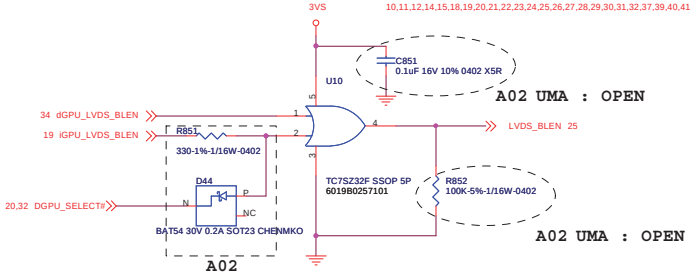
LCD PWM SW

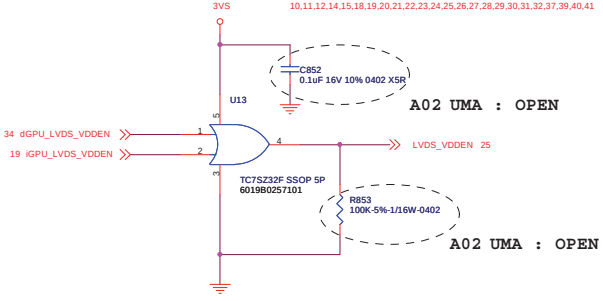


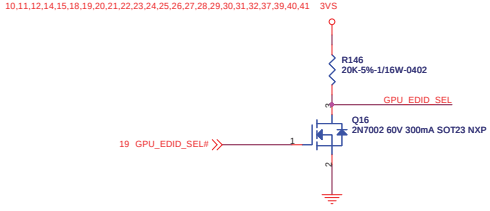
SW Gfx:OPEN
UMA:Stuff

LCD DDC SW









INVENTEC

TITLE: BAP/BXP30
Hybird Switch (2/2)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X01

CHANGE by IEC | DATE Monday, May 24, 2010 | SHEET 33 of 41

GPU Thermal Sensor
Please close GPU side

Physical Ttrapping Pin	N11M-GE 1 Hynix H5TQ1G63BFR-12C	N11M-GE 1 SAMSUNG K4W1G1646E-HC12	N11M-GE 2 Hynix H5TQ1G63BFR-12C	N11M-GE 2 SAMSUNG K4W1G1646E-HC12
PEG_ROM_SO	10K:pull-down	10K:pull-down	10K:pull-down	10K:pull-down
PEG_ROM_SI	15K:pull-down	20K ohm Pull-Down	15K:pull-down	20K ohm Pull-Down
PEG_ROM_SCLK	15K:pull-Up	15K:pull-Up	15K:pull-Up	15K:pull-Up
PEG_MIOB_STRAP2	30K:pull-down	30K:pull-down	5K:pull-down	5K:pull-down
PEG_MIOB_STRAP1	35K:pull-up	35K:pull-up	35K:pull-up	35K:pull-up
PEG_MIOB_STRAP0	45K:pull-up	45K:pull-up	45K:pull-up	45K:pull-up

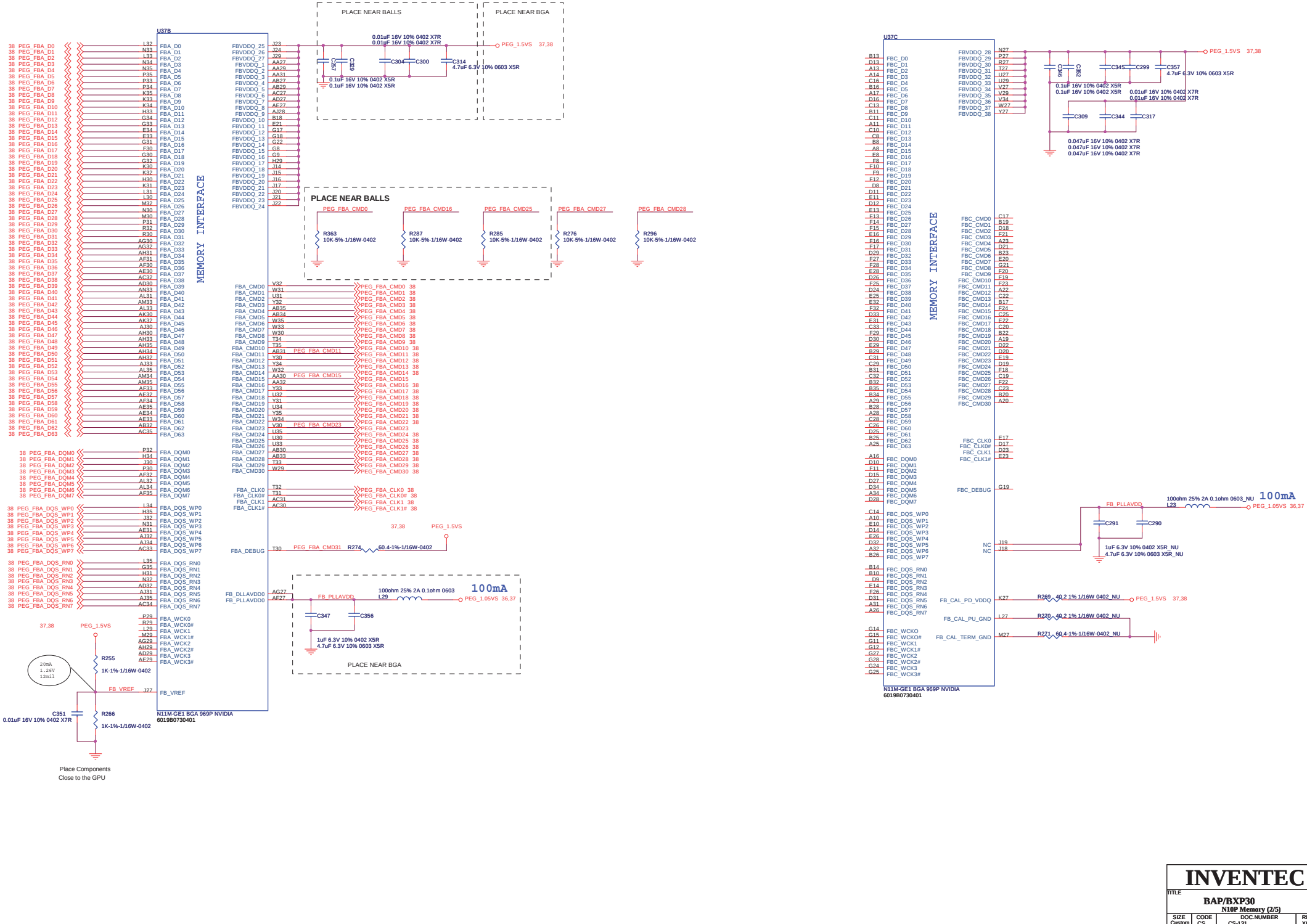
Device	Interface	I2C Bus
CRT	DAC A	I2C A
LVDS	LVDS	I2C C
DVI	IFP C	IFPC_AUX

INVENTEC

TITLE: BAP/BXP30
N10P PCIE I/O (1/5)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02

CHANGE by: IEC | DATE: Monday, May 24, 2010 | SHEET 34 of 41

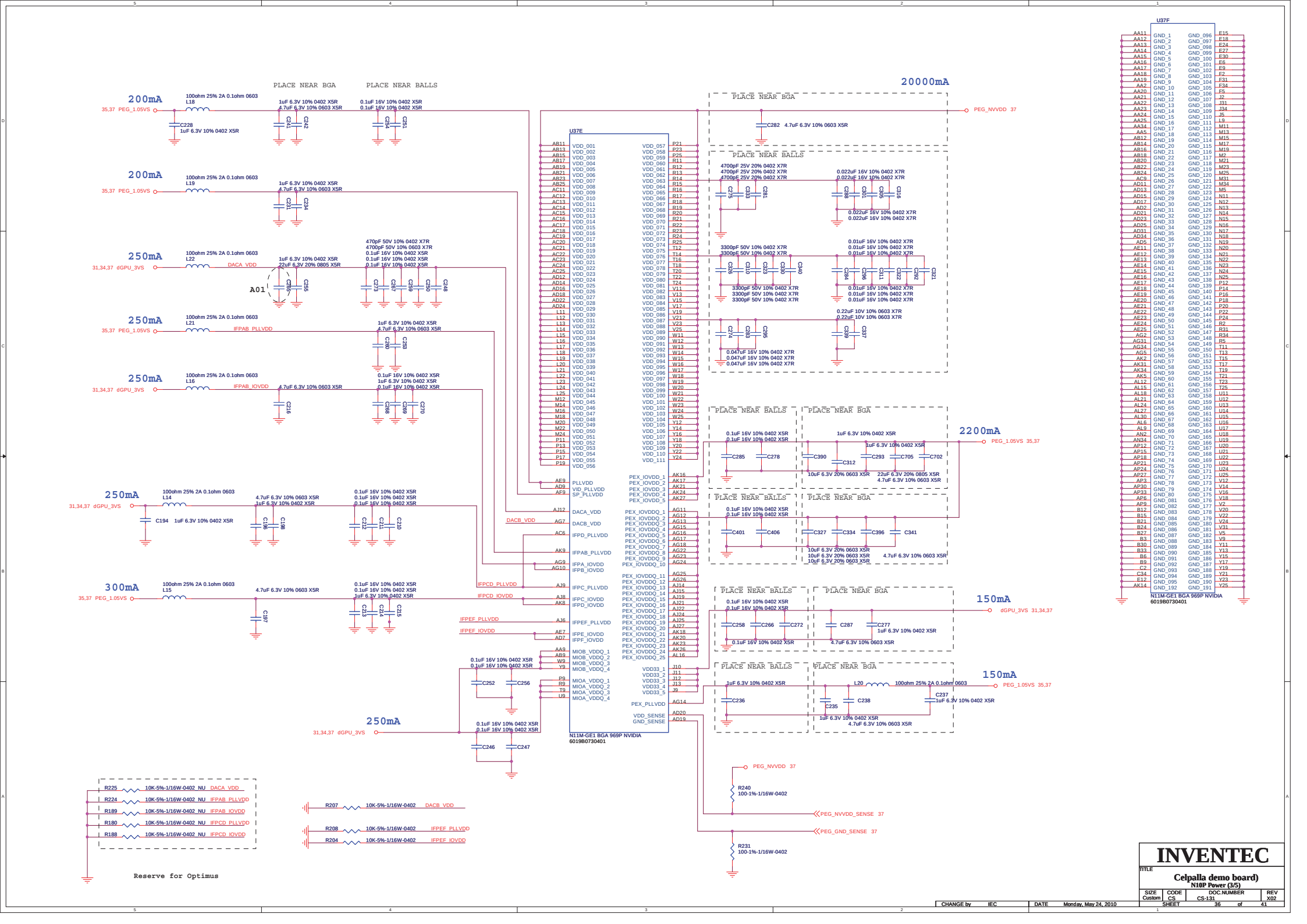


CHANGE by	IEC	DATE	Monday, May 24, 2010	
		SHEET	35 of 41	

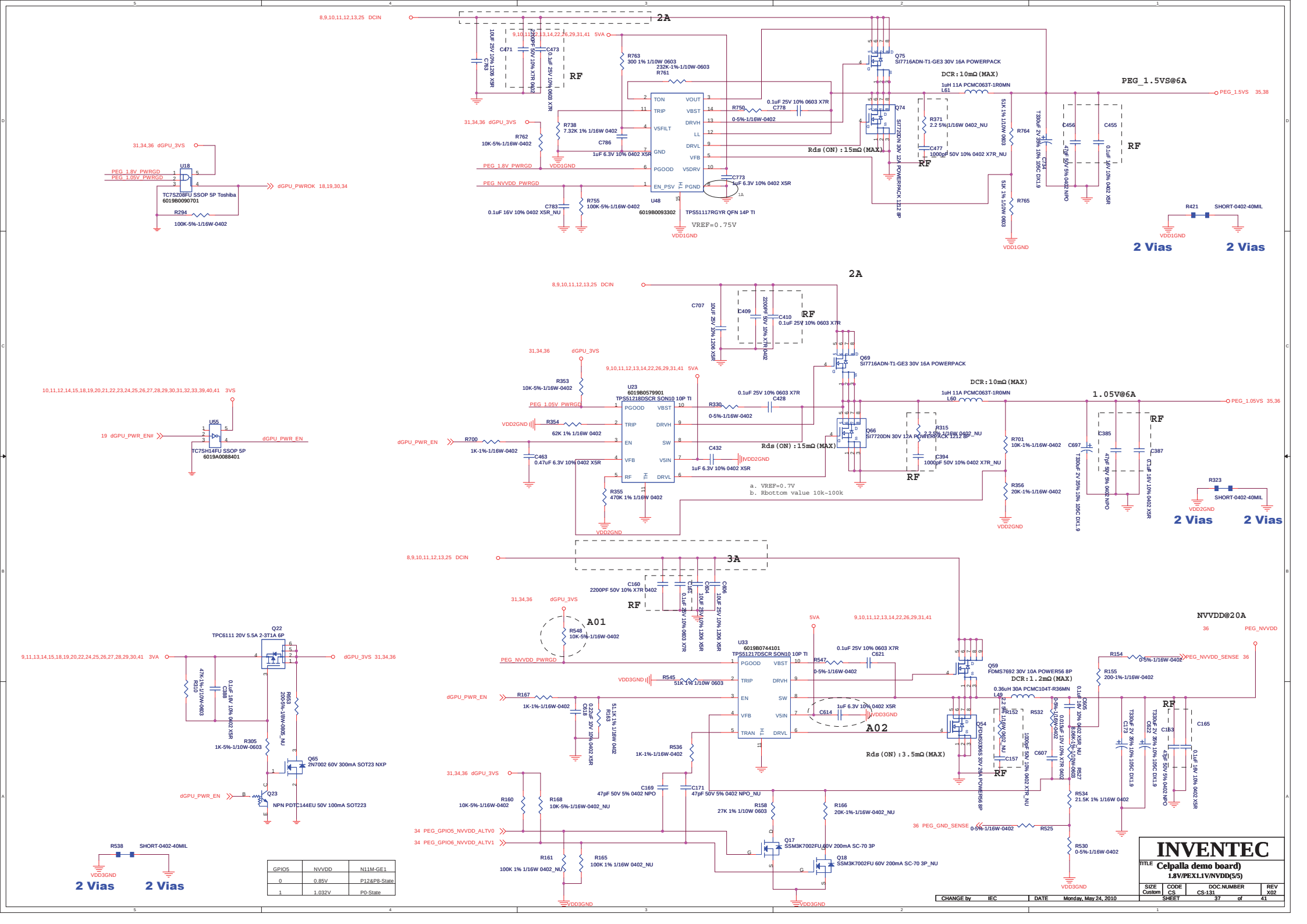
INVENTEC

TITLE: **BAP/BXP30**
N10P Memory (2/5)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02



INVENTEC			
TITLE	Celpalla demo board) N10P Power (3/5)		
SIZE Custom	CODE CS	DOC.NUMBER CS-131	REV X02
CHANGE by IEC	DATE Monday, May 24, 2010	SHEET 36 of 41	



GPIO5	NVVDD	N11M-GE1
0	0.85V	P12&P8-State
1	1.032V	P0-State

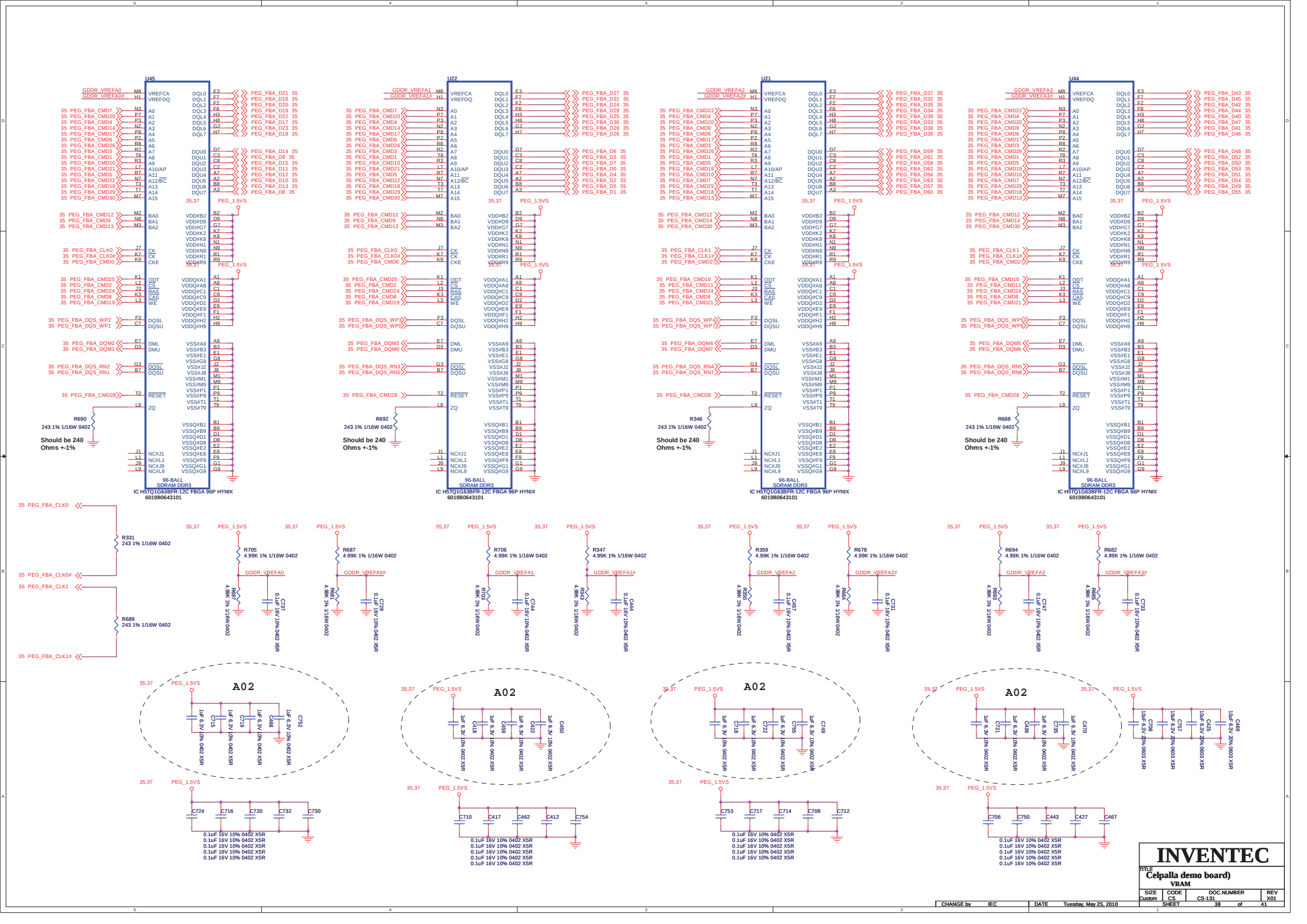
INVENTEC

TITLE: Celpalla demo board)
1.8V/PEX1.1V/NVDD(5/5)

SIZE	CODE	DOC.NUMBER	REV
Custom	CS	CS-131	X02

SHEET 37 of 41

CHANGE by IEC | DATE Monday, May 24, 2010


U45
U22
U21
U44
96-BALL SDRAM DDR3
IC H5TQ1G63BFR-12C FBGA 96P HYNIX
6019B0643101
R690
R692
R346
R688
243 1% 1/16W 0402
Should be 240 Ohms +-1%
R331
R689
R705
R687
R706
R347
R359
R678
R694
R682
4.99K 1% 1/16W 0402
A02
0.1uF 16V 10% 0402 X5R
1uF 6.3V 10% 0402 X5R
10uF 6.3V 20% 0603 X5R
INVENTEC
Celpalla demo board)
VRAM
CHANGE by IEC
DATE Tuesday, May 25, 2010
SIZE Custom
CODE CS
DOC.NUMBER CS-131
REV X01
SHEET 38 of 41

AUDIO CODEC

Note:

To support Wake-on-Jack, the CODEC VAUX_3.3 pins must be powered by a Standby supply.

VDD_IO set signaling level for HDA bus

R1137 only needed if supply to VAUX_3.3 is removed during system re-start.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

30mA@MAX

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

CX20672-11Z QFN 40P Conexant
6019B0730901

BAT54 30V 0.2A SOT23 CHENMKO

BAT54A 30V 200mA SOT23 CHENMKO

LMBT3904LT1G 40V 200mA SOT-23

FOR DOCK

Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono mic (stereo option)
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)

SPEAKER

30mil

CN 4P 88266-04001 ACES
6012B0096202

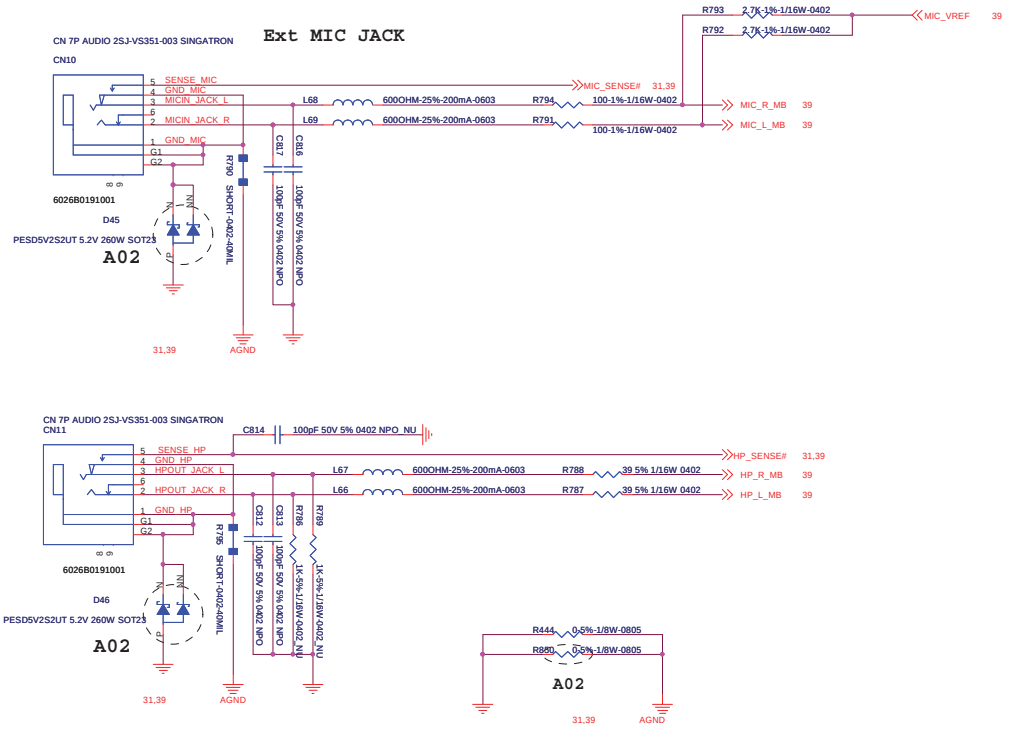
OK

For EMC

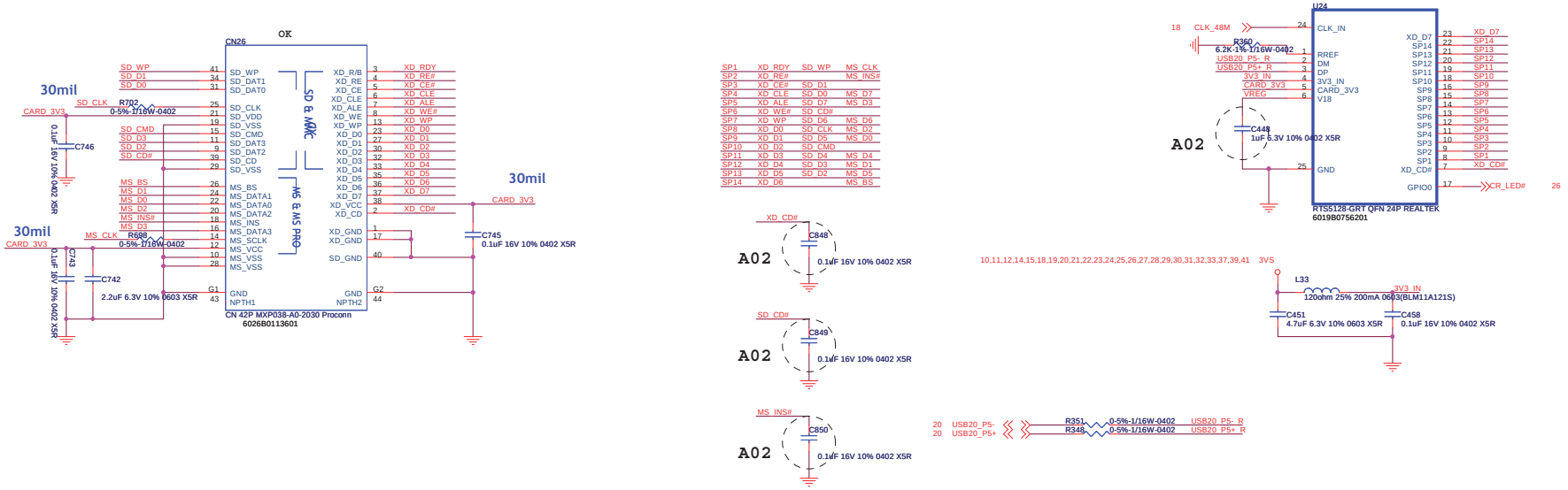
GND1
GND_AUD

Project	Celpalla demo board)
Title	Audio Codec /AMP
Size	Custom
Code	CS
Doc.Number	CS-131
Rev	X01
Change by	IEC
Date	Monday, May 24, 2010
Sheet	39 of 41

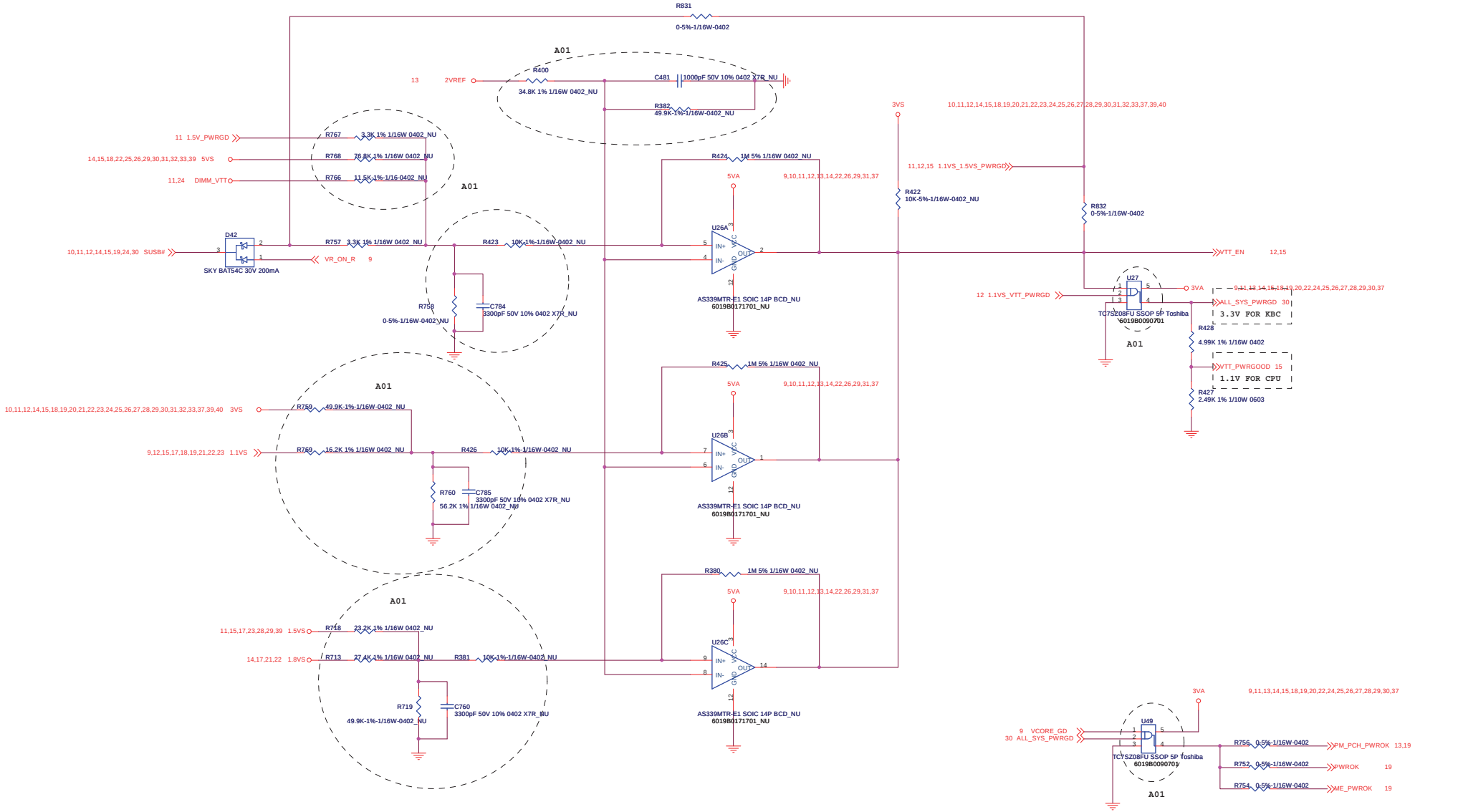
INVENTEC



5 in 1 CARDREADER



INVENTEC			
TITLE: BAP/BXP30 CARD READER/AUDIO BOARD			
SIZE: Custom	CODE: A03	DOC.NUMBER: D-CS-1310A2271201-ALG	REV: A03
CHANGE by: <CHANGE by>	DATE: Monday, May 24, 2010	SHEET: 40 of 41	



INVENTEC

TITLE: BAP/BXP30
POWER SEQUENCE

SIZE	CODE	DOC.NUMBER	REV
Custom	A03		A03

CHANGE by <CHANGE by> | DATE Monday, May 24, 2010 | SHEET 41 of 41