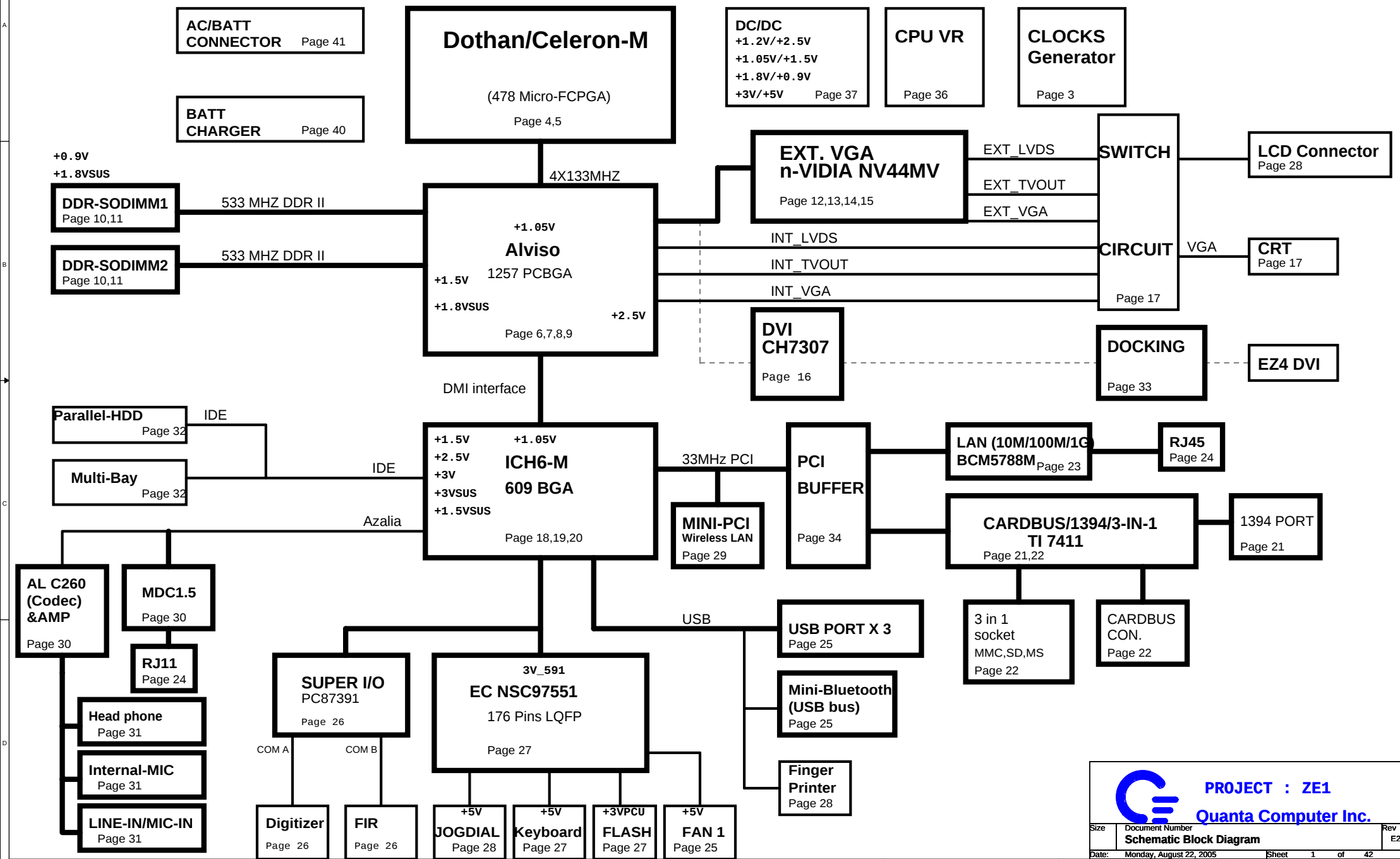


ZE1

REV : E2C



PROJECT : ZE1
Quanta Computer Inc.

06/22 MODIFY LIST

1. Remove all no-use
2. Page 12 Change R

- 06/23 MODIFY LIST

- 06/28 MODIFY LIST

- 06/28 MODIFY LIST

07/19 MODIFY LIST

07/19 MODIFY LIST

- 07/26 MODIFY LIST

- 07/29 MODIFY LIST

14. Page 85, Right:

- ### C TEST CHANGE ITEMS:

08/9 MODIFY LIST

49. Page 26. Add GNI

- FBI - Page 06 - CPU 00

- 08/12 MODIFY LIST

- 08/13 MODIFY LIST

08/18 MODIFY LIST

- 08/19 MODIFY LIST

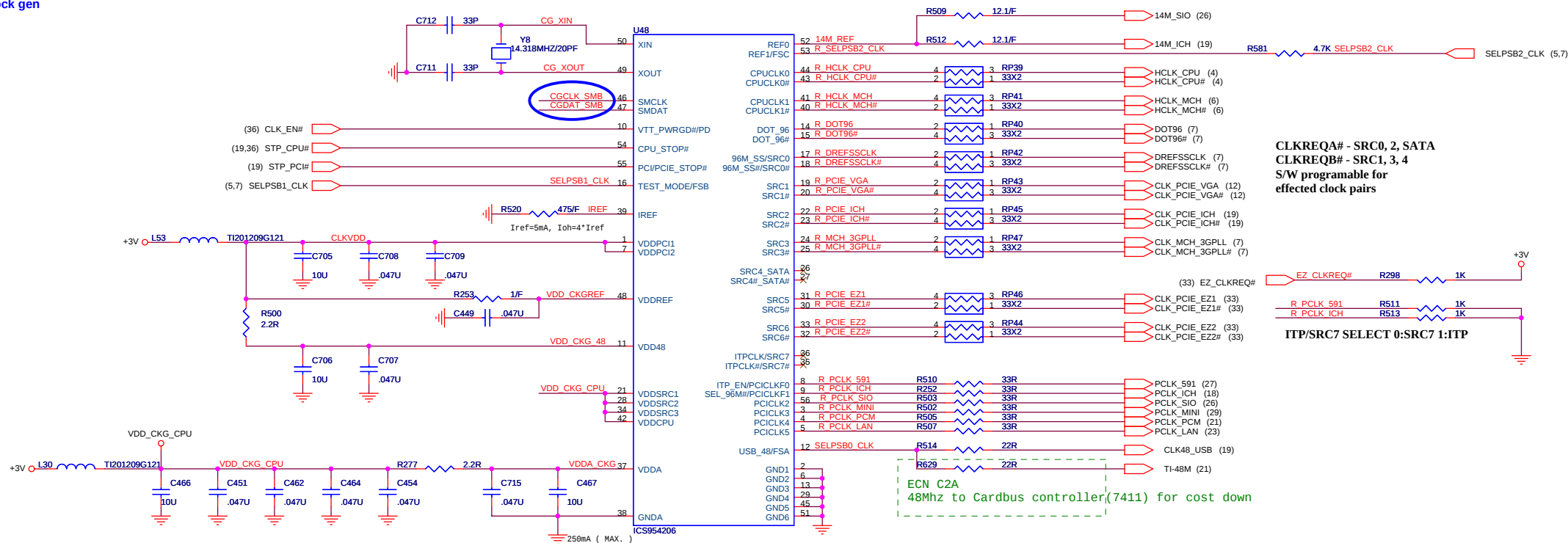
- 06/27 LAYOUT SWAP

Pin 'JDIM2.153' moved to net 'R_A_MD46'

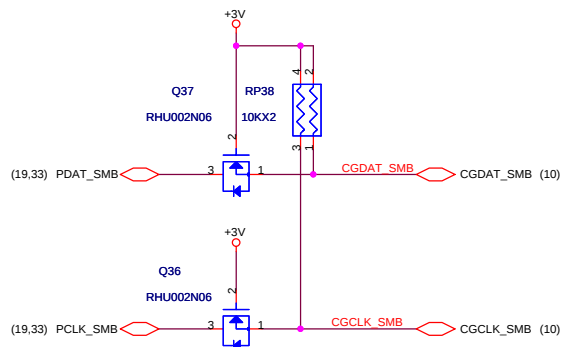
- [illegible]



Clock gen



SM Bus



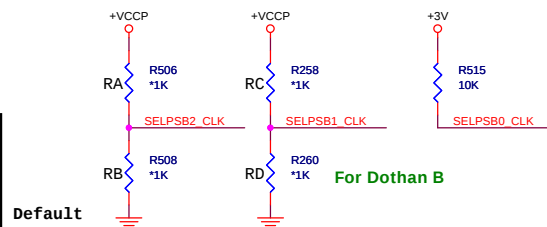
Speed setting

Resistor Stuff Table

	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X

Clock Gen. Frequency Selection Table

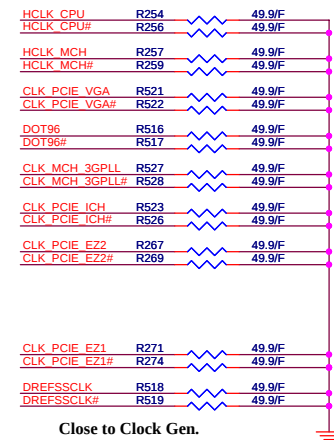
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



DOTHAN BSEL Output Value

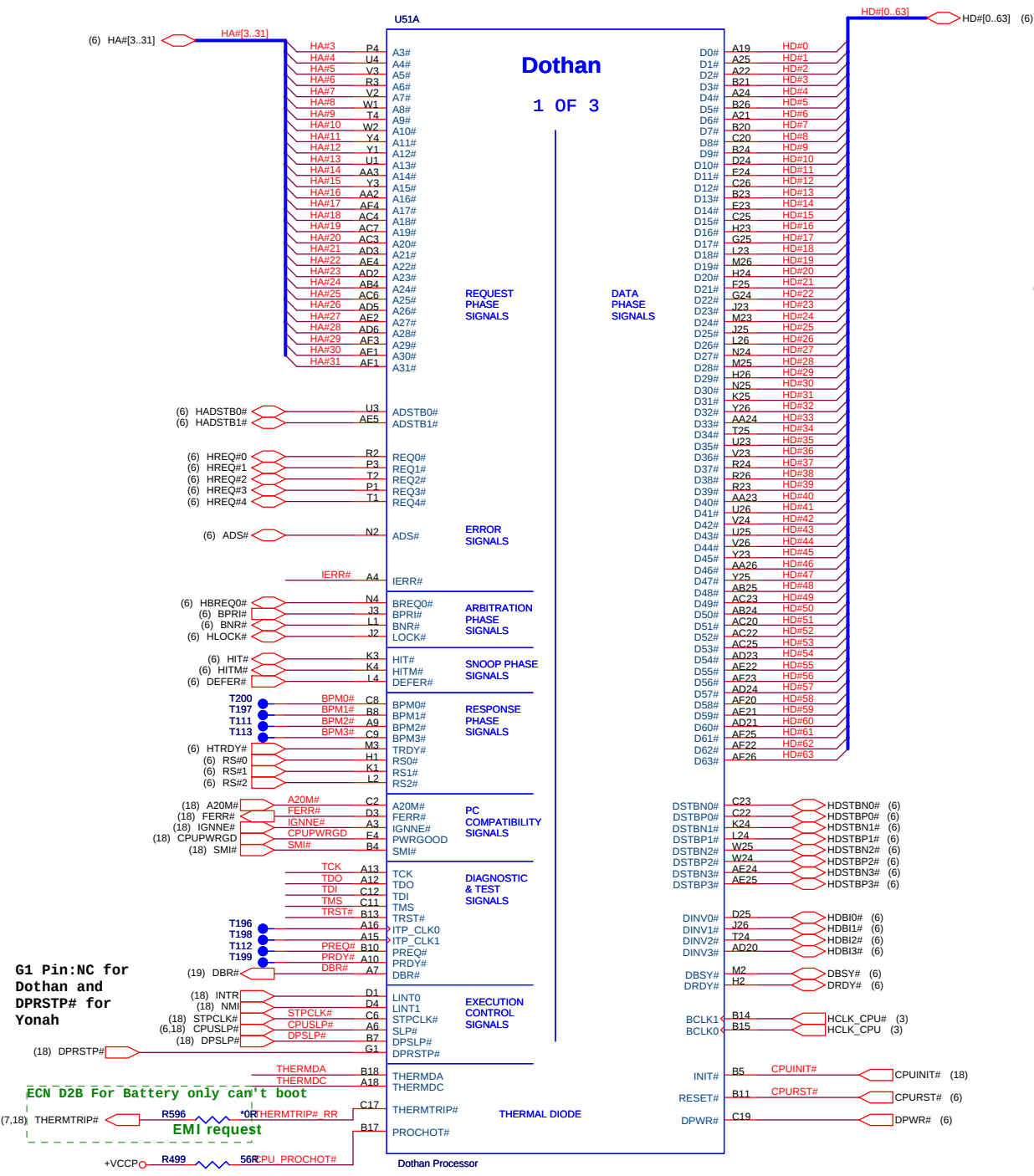
FSB Frequency	DOTHAN A-Step		DOTHAN B-Step	
	BSEL1	BSEL0	BSEL1	BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0

Clock terminator

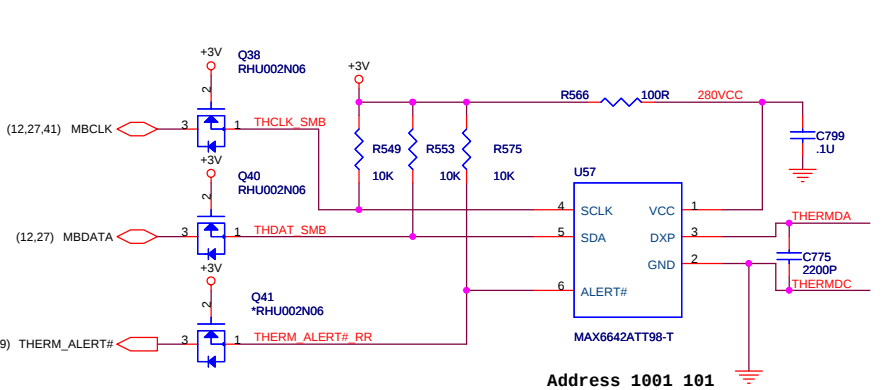


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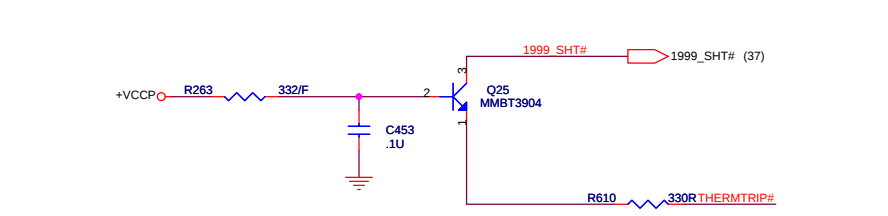
Size	Document Number Clock Gen.	Rev B2A
Date:	Monday, August 22, 2005	Sheet 3 of 42



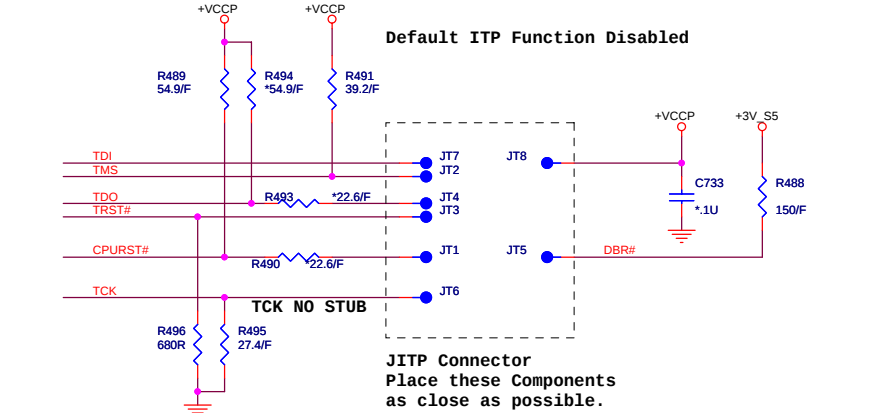
Thermal monitor



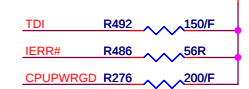
Power reset circuit



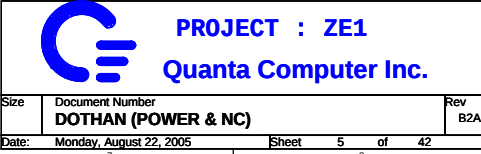
ITP debug

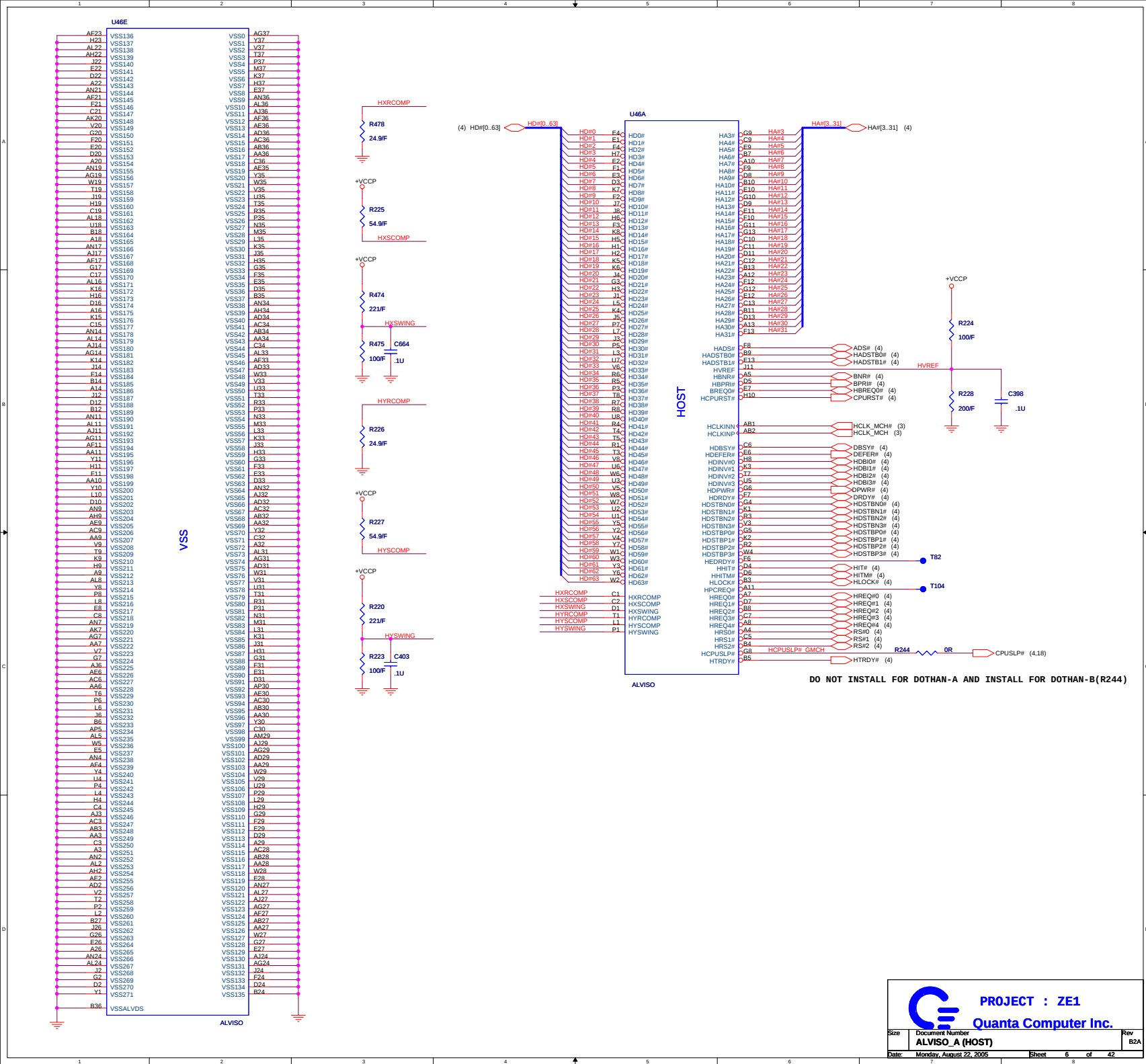


Close to CPU



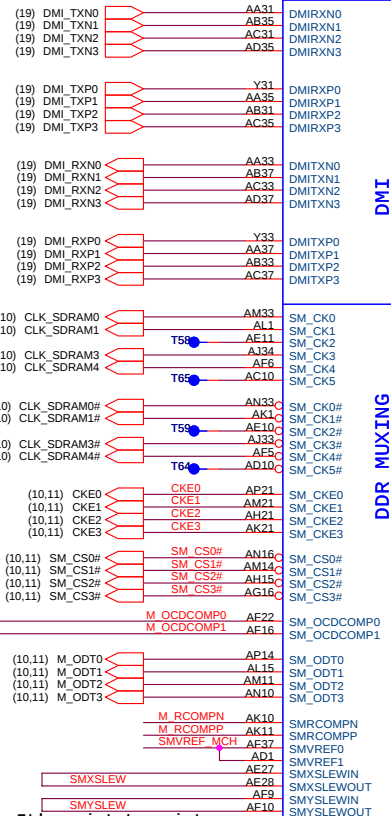
PROJECT : ZE1
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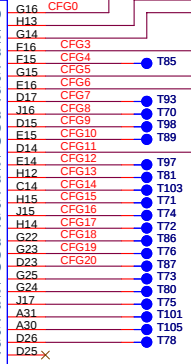
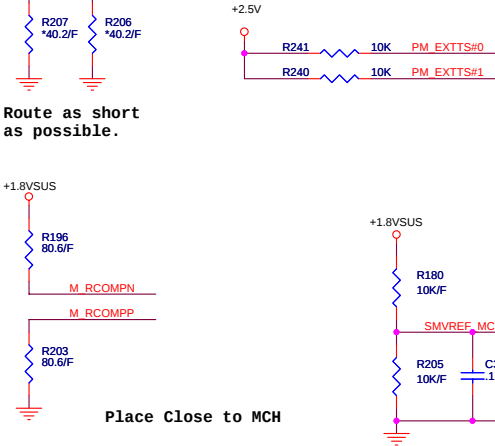


CFG[0:2]=100 FOR FSB 533
CFG[0:2]=101 FOR FSB 400

U46C



ALVISO



FOR DDR533
Low=DMiX2
High=DMiX4

FOR CPU533

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

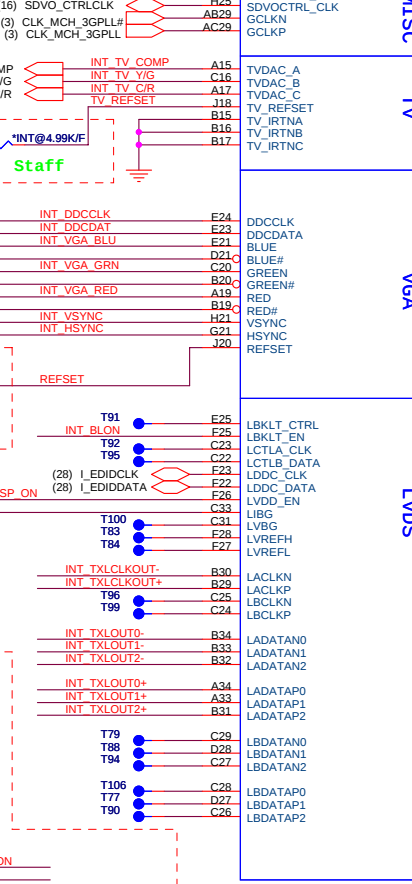
INT VGA Staff

INT VGA Staff

INT VGA Staff

INT VGA Staff

U46F



PCI-EXPRESS GRAPHICS

LVDS

EXT VGA Staff

EXT VGA Staff

EXT VGA Staff

EXT VGA Staff

EXT VGA Staff

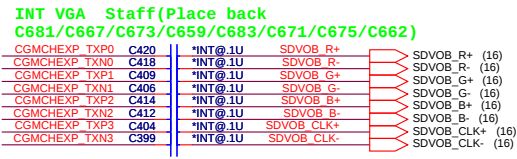
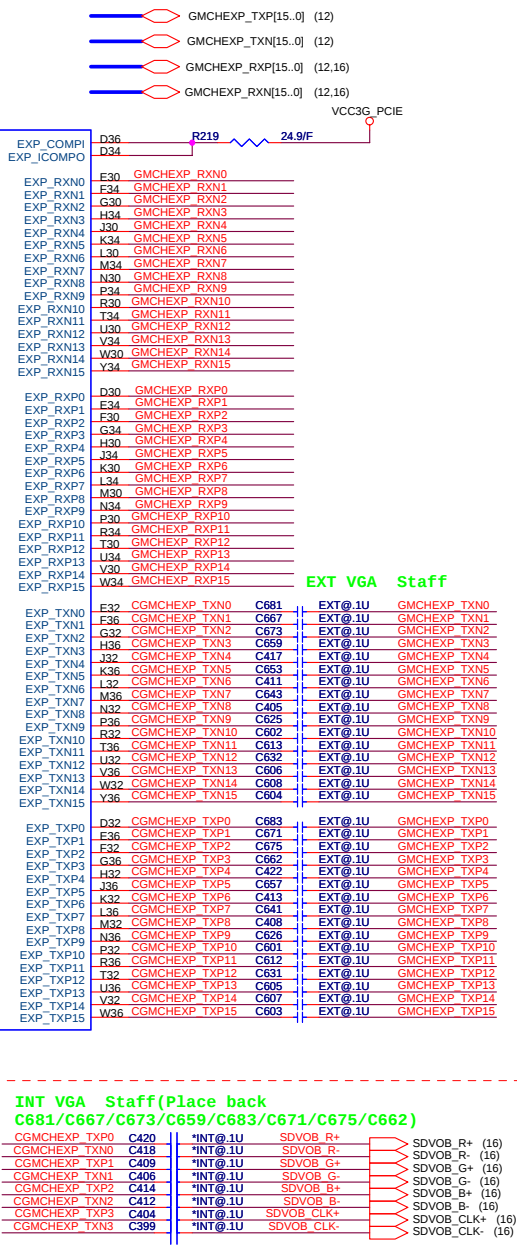
EXT VGA Staff

EXT VGA Staff

EXT VGA Staff

EXT VGA Staff

EXT VGA Staff



(10) R_A_MD[0..63]



DDR SYSTEM MEMORY A

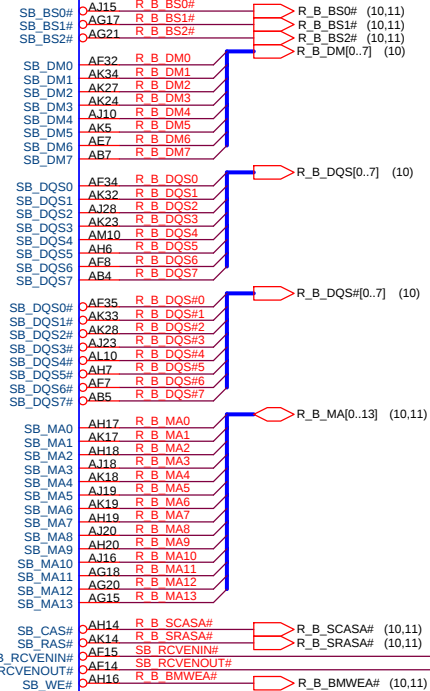


ALVISO

(10) R_B_MD[0..63]



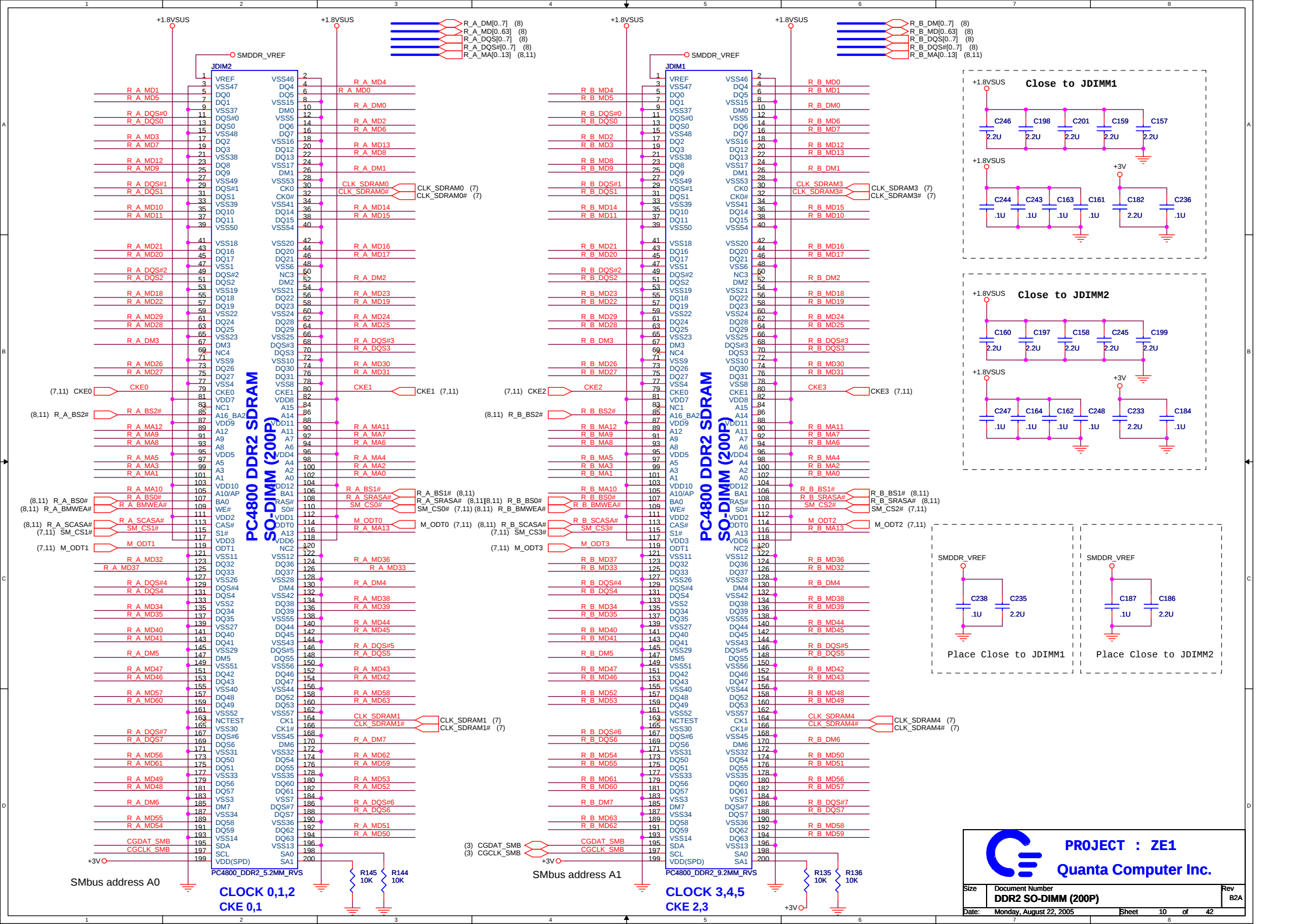
DDR SYSTEM MEMORY B

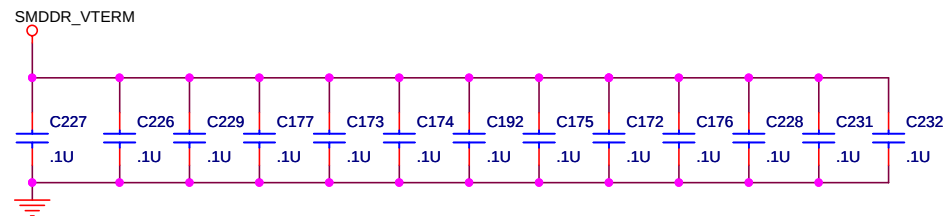


ALVISO

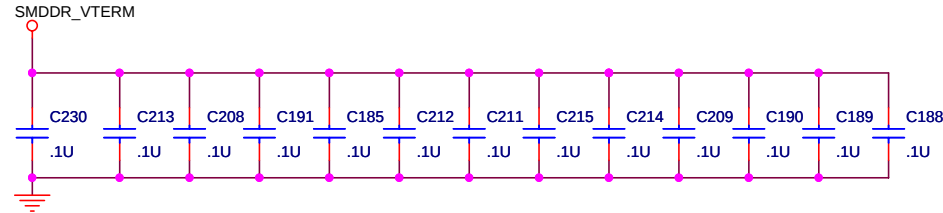


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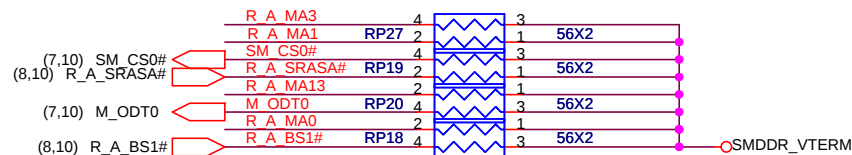
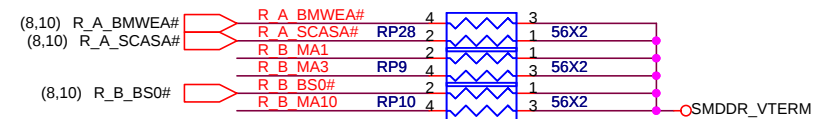
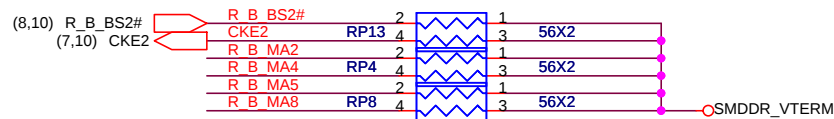
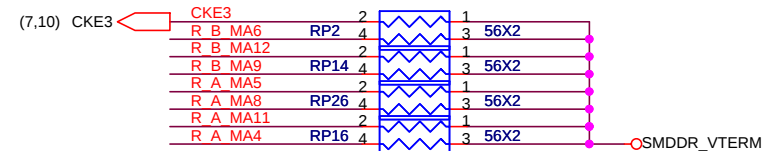
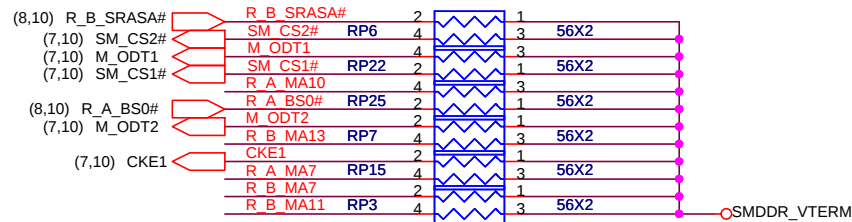
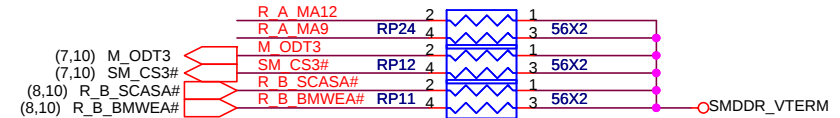
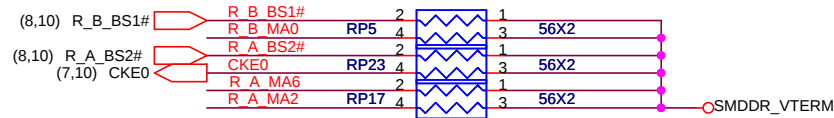
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

R_A_MA[0..13] (8,10)

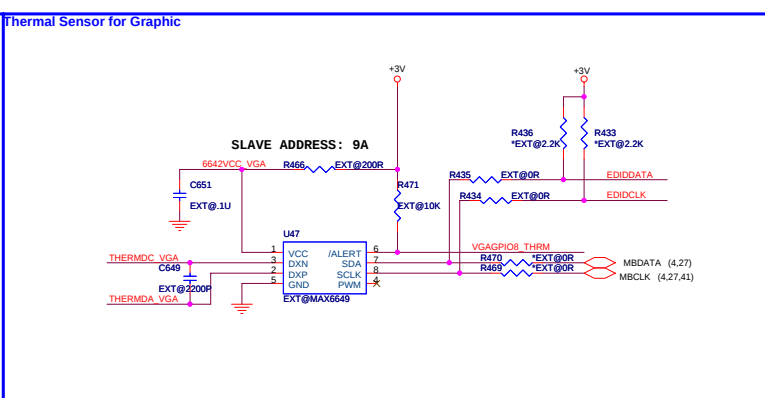
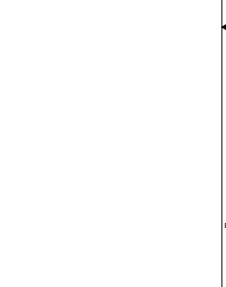
R_B_MA[0..13] (8,10)

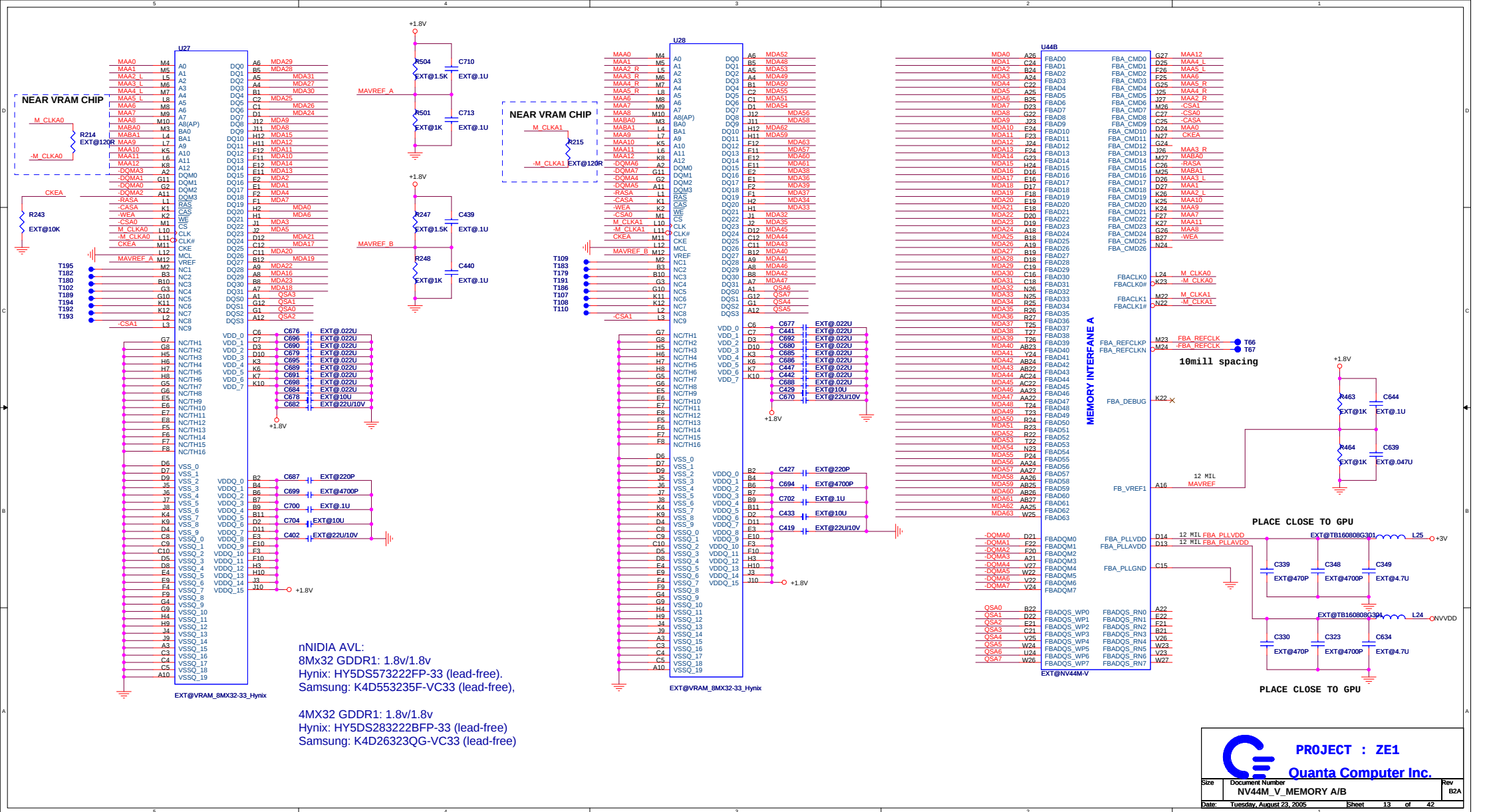


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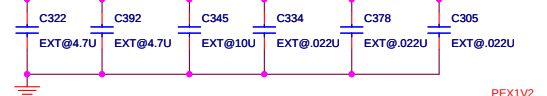


AD23-PEX_IOVDD
280mA
AC16-PEX_IOVDDQ
1580mA

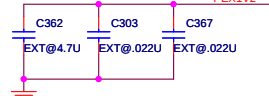
PLACE NEAR BALLS

1580mA

PEX1V2



MEP43=1.05V/11.03A
MEP44(400/350)1.25V/9.02A

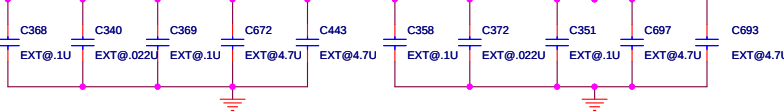


U44C
W17 PEX_IOVDD0
W18 PEX_IOVDD1
AB10 PEX_IOVDD2
AB11 PEX_IOVDD3
AB14 PEX_IOVDD4
AB15 PEX_IOVDD5
AB20 PEX_IOVDD6
AB21 PEX_IOVDD7
AA4 PEX_IOVDDQ0
AB5 PEX_IOVDDQ1
AB6 PEX_IOVDDQ2
AB7 PEX_IOVDDQ3
AB8 PEX_IOVDDQ4
AB9 PEX_IOVDDQ5
AB12 PEX_IOVDDQ6
AB13 PEX_IOVDDQ7
AB16 PEX_IOVDDQ8
AB17 PEX_IOVDDQ9
AB18 PEX_IOVDDQ10
AB19 PEX_IOVDDQ11
AC9 PEX_IOVDDQ12
AC11 PEX_IOVDDQ13
AC12 PEX_IOVDDQ14
AC16 PEX_IOVDDQ15
AC17 PEX_IOVDDQ16
AC19 PEX_IOVDDQ17
AC20 PEX_IOVDDQ18

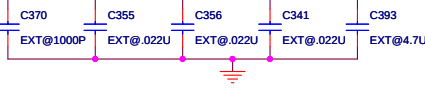
FBVDDQ0 F17
FBVDDQ1 F19
FBVDDQ2 J22
FBVDDQ3 J22
FBVDDQ4 M19
FBVDDQ5 L22
FBVDDQ6 T19
FBVDDQ7 U22
FBVDDQ8 Y22
FBVDDQ9

FBVTT0 E15
FBVTT1 F15
FBVTT2 J17
FBVTT3 J18
FBVTT4 J18
FBVTT5 N19
FBVTT6 R19
FBVTT7 U19
FBVTT8 W19
FBVTT9

PLACE NEAR BALLS



PLACE NEAR BALLS



POWER

J9 VDD0
J10 VDD1
J11 VDD2
L12 VDD3
L13 VDD4
L15 VDD5
L16 VDD6
M9 VDD7
M11 VDD8
M12 VDD9
M13 VDD10
M14 VDD11
M15 VDD12
M16 VDD13
M17 VDD14
M9 VDD15
N11 VDD16
N17 VDD17
R9 VDD18
R11 VDD19
R17 VDD20
T9 VDD21
T11 VDD22
T12 VDD23
T14 VDD24
T15 VDD25
T16 VDD26
U12 VDD28
U13 VDD29
U15 VDD30
U16 VDD32
W13 VDD33
W15 VDD34
W16 VDD35

W8 VDD_LP0
W10 VDD_LP1
W11 VDD_LP2
W12 VDD_LP3

F13 VDD33_0
F14 VDD33_1
J12 VDD33_2
J13 VDD33_3
J15 VDD33_4
J16 VDD33_5

Y6 PEX_PLL_AVDD
AA5 PEX_PLL_DVDD

EXT@NV44M-V

MIOA_VDDQ0 F6
MIOA_VDDQ1 G6
MIOA_VDDQ2 J6

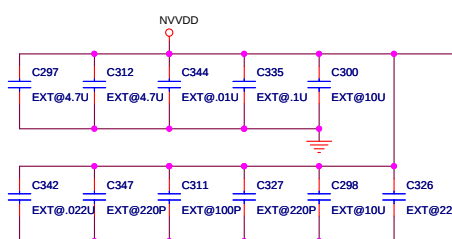
MIOB_VDDQ0 K5
MIOB_VDDQ1 K6
MIOB_VDDQ2 L6

FBVDDQ0 D15
FBVDDQ1 R457
FBVDDQ2 EXT@37.4/F

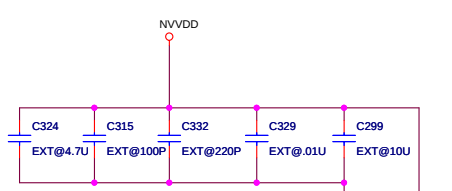
MIOB_VDDQ0 J5
MIOB_VDDQ1 R181
MIOB_VDDQ2 *EXT@49.9/F

MIOB_VREF J4

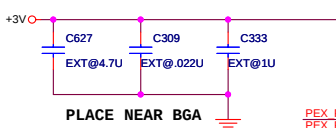
PLACE NEAR BALLS



PLACE NEAR BALLS



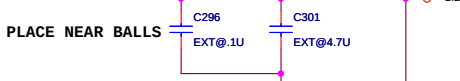
PLACE NEAR BGA



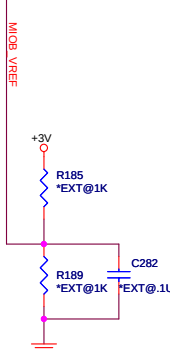
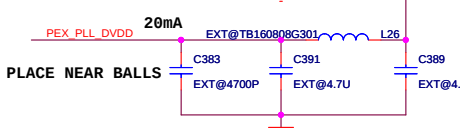
PLACE NEAR BGA



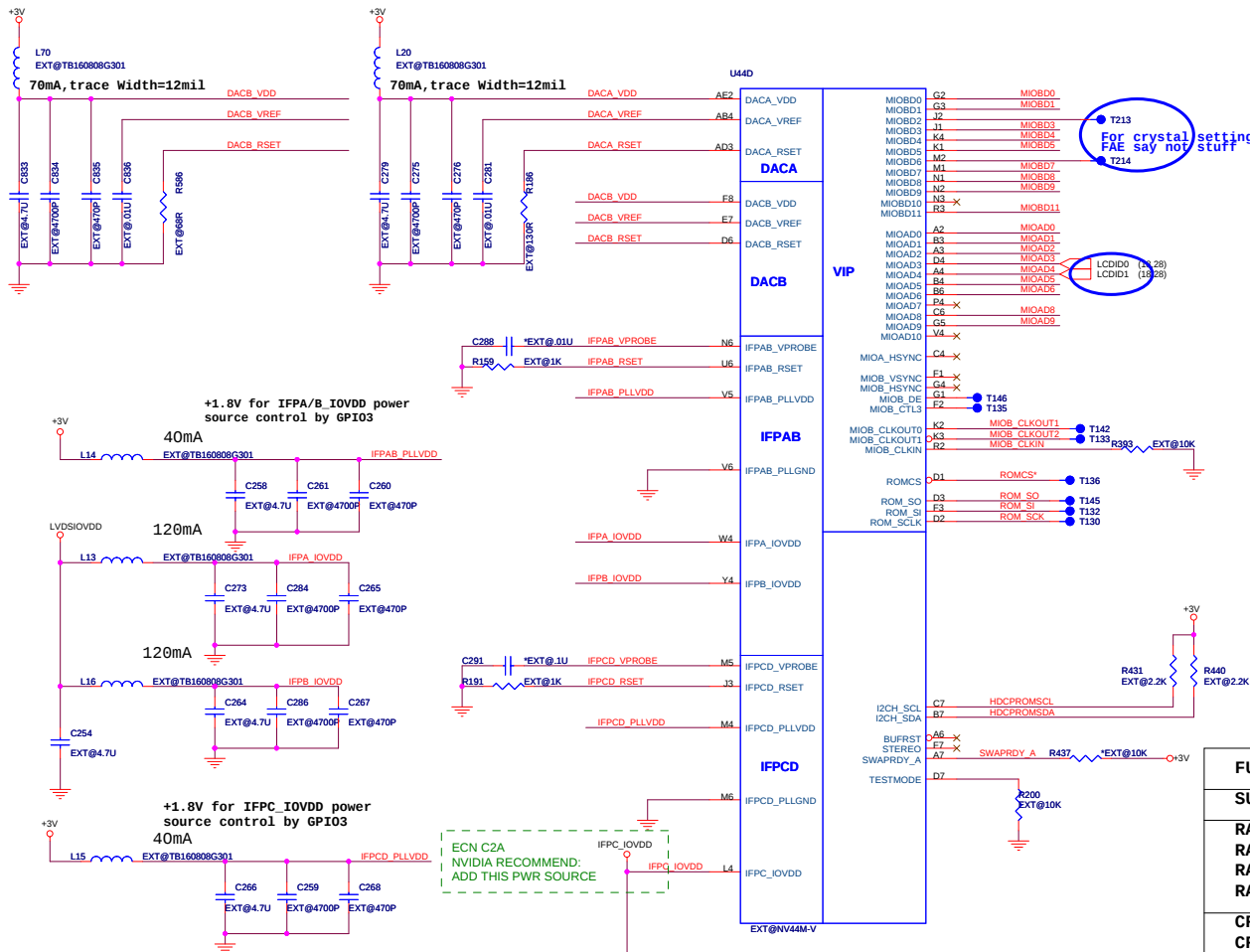
PLACE NEAR BALLS



PLACE NEAR BALLS



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SUB_VENDOR: 0:SYSTEM BIOS 1:ADAPTER BIOS	
CRYSTAL[1:0]: MS_00:13.5MHz MS_10:27MHz	MS_01:14.318MHz MS_11:RESERVED
PCI_DEVID[3:0]: MS_0110:NV18M MS_0111:NV18MPRO MS_1010:NV31M MS_1011:NV31MPRO MS_1100:NV31GLM MS_1110:NV31GLMPRO MS_0100:NV34M	
ROM_TYPE[1:0]: MS_00:PARALLEL MS_01:SERIAL AT25F MS_10:SERIAL SST45VF MS_11:RESERVED	

FUNCTION	NV4x and MEP4x	SETTING
SUB_VENDOR	MIOAD1	L0
RAMCFG0	MIOBD0	HI
RAMCFG1	MIOBD1	L0
RAMCFG2	MIOBD8	L0
RAMCFG3	MIOBD9	L0
CRYSTAL0	MIOBD2	L0
CRYSTAL1	MIOBD6	HI
PCI_DEVID0	MIOBD4	HI
PCI_DEVID1	MIOBD5	HI
PCI_DEVID2	MIOBD3	HI
PCI_DEVID3	MIOBD11	L0
USER0	MIOAD2	HI
USER1	MIOAD3	HI
USER2	MIOAD4	HI
USER3	MIOAD5	HI
ROMTYPE0	MIOBD10	L0
ROMTYPE1	MIOB_VSYNC	L0
36IO_PADC6G_LUT_ADR0	MIOAD6	HI
36IO_PADC6G_LUT_ADR1	MIOAD8	L0
36IO_PADC6G_LUT_ADR2	MIOAD9	L0
PEX_PLL_EN_TERM	MIOAD0	L0
PEX_PADC6G0	MIOAD6	HI
PEX_PADC6G1	MIOAD8	L0
PEX_PADC6G2	MIOAD9	L0
Mobile_Mode	MIOBD7	L0

DVI control schematic(INT VGA USE)

INT VGA Staff

(7) SDVOB_R+
(7) SDVOB_R-
(7) SDVOB_G+
(7) SDVOB_G-
(7) SDVOB_B+
(7) SDVOB_B-
(7) SDVOB_CLK+
(7) SDVOB_CLK-

SDVOB_R+
SDVOB_R-
SDVOB_G+
SDVOB_G-
SDVOB_B+
SDVOB_B-
SDVOB_CLK+
SDVOB_CLK-

DVI AVDD

Always not, Reserve only

+2.5V R90 *INT@10K R91 *100K

+3V L7 *INT@BLM11A601S DVI AVDD PLL
C83 (7,12,18,19,26,27,32,33) PLTRST#
*INT@1U C111 *INT@10U
(7) SDVO_CTRLCLK
(7) SDVO_CTRLDATA

+2.5V L3 *INT@BLM11A601S DVI DVDD
C55 *INT@1U C58 *INT@1U C46 *INT@10U
(12,33) TMDS_DDCDATA
(12,33) TMDS_DDCCLK

Always not, Test only

U6
SCL A0
SDA A1
WP A2
VCC
GND
*AT24C16
+3V R80 *1K DVOCCLK
+3V R84 *1K DVODATA

*EXT@CH7307C-DE

DVI CLK-
DVI CLK+
DVI TX0-
DVI TX0+
DVI TX1-
DVI TX1+
DVI TX2-
DVI TX2+

AVDD1
SDVOB_STALL-
SDVOB_STALL+
SDVOB_INT-
SDVOB_INT+
AGND1
DGND2
HPDET
DVDD2
ATPG
SCEN
VSWING
R66 *INT@1.2K
R72 R69 *INT@10K *INT@10K

ECN C2A
N-vidia suggestio
De1 R584/R585

INT- C65 *INT@.01U/16V R584 *EXT@0R
INT+ C61 *INT@.01U/16V R585 *EXT@0R
GMCHEXP_RXN1 (7,12)
GMCHEXP_RXP1 (7,12)

+2.5V R89 *INT@1K SDVO_CTRLCLK

+2.5V R88 *INT@1K SDVO_CTRLDATA

PULL Low For DVO Not
Present(Internal PULL LOW In 915GM)

+2.5V 250mA
+3V 190mA

DVI Output select

INT VGA Staff

ECN C2A
CAHGE FROM R TO RN

DVI CLK+ RN16 4 3 *INT@0X2
DVI CLK- RN16 2 1
DVI TX0+ RN17 4 3 *INT@0X2
DVI TX0- RN17 2 1
DVI TX1+ RN18 4 3 *INT@0X2
DVI TX1- RN18 2 1
DVI TX2+ RN19 4 3 *INT@0X2
DVI TX2- RN19 2 1
TMDS_TXCP_PR (33)
TMDS_TXCM_PR (33)
TMDS_TX0P_PR (33)
TMDS_TX0M_PR (33)
TMDS_TX1P_PR (33)
TMDS_TX1M_PR (33)
TMDS_TX2P_PR (33)
TMDS_TX2M_PR (33)

EXT VGA Staff(Default)

(12) EXT_TMDS_TXCP_PR RN5 2 1 EXT@0X2
(12) EXT_TMDS_TXCM_PR RN5 4 3
(12) EXT_TMDS_TX0P_PR RN8 2 1 EXT@0X2
(12) EXT_TMDS_TX0M_PR RN8 4 3
(12) EXT_TMDS_TX1P_PR RN7 2 1 EXT@0X2
(12) EXT_TMDS_TX1M_PR RN7 4 3
(12) EXT_TMDS_TX2P_PR RN6 2 1 EXT@0X2
(12) EXT_TMDS_TX2M_PR RN6 4 3

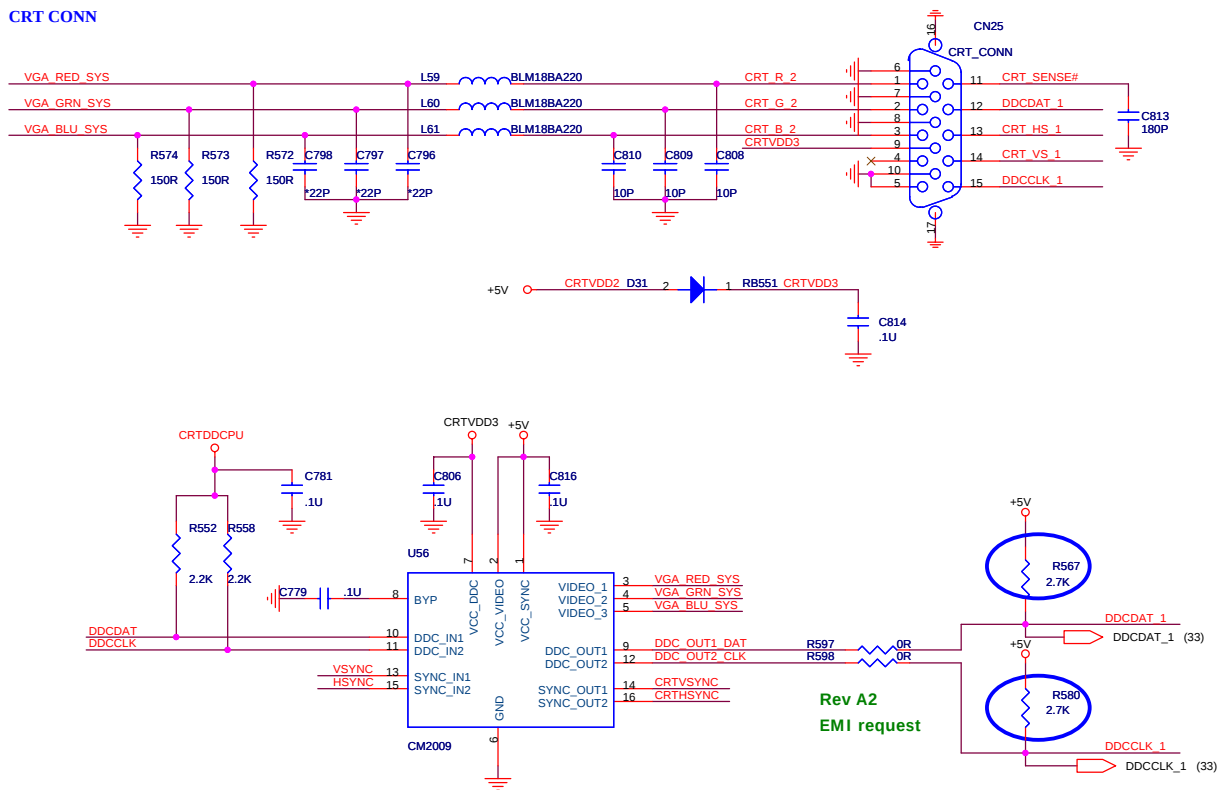


PROJECT : ZE1

Quanta Computer Inc.

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CRT CONN



CRT Select

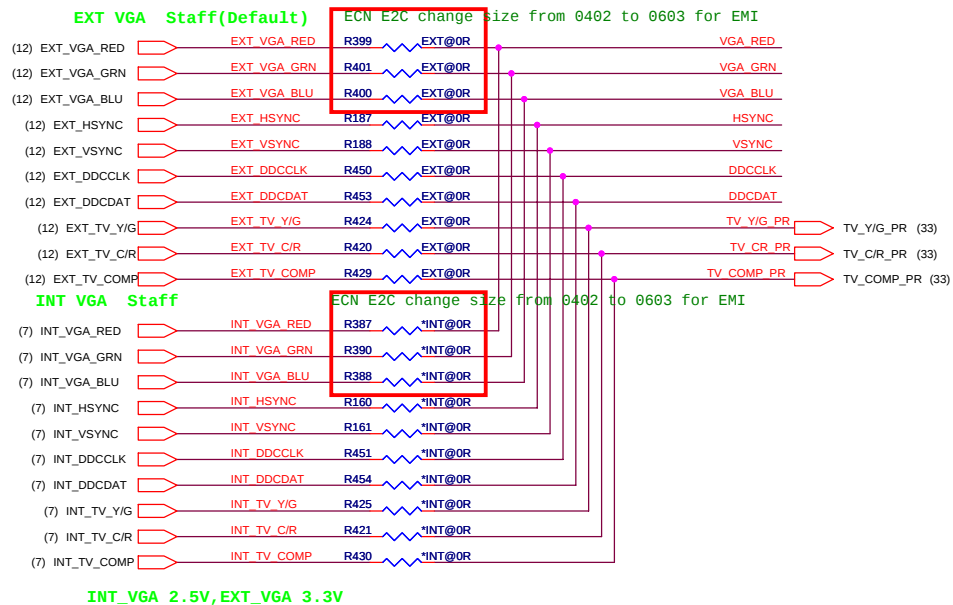
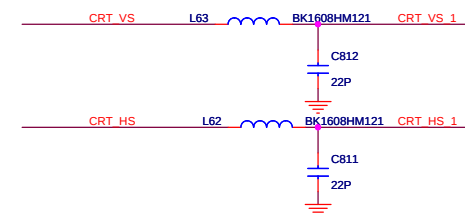
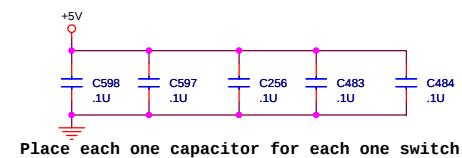
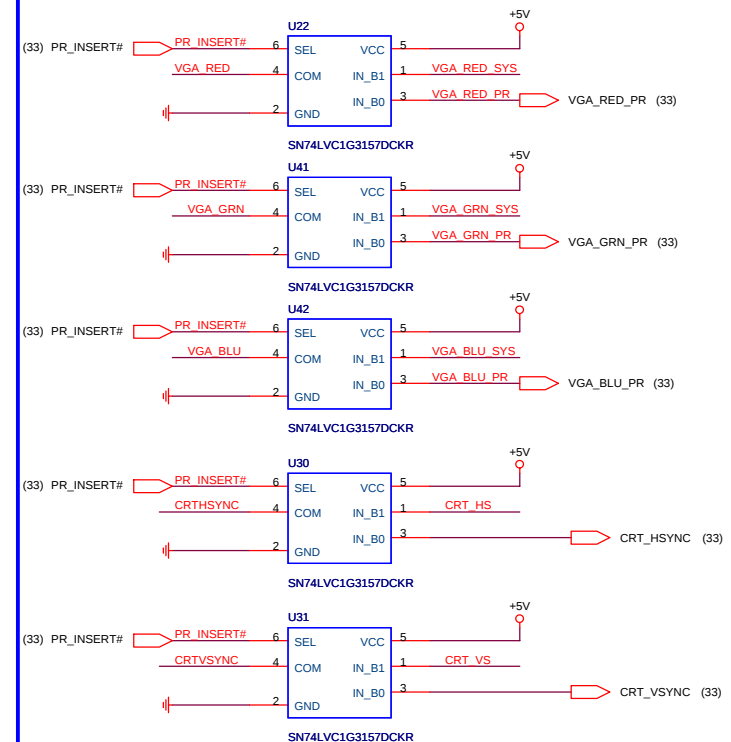
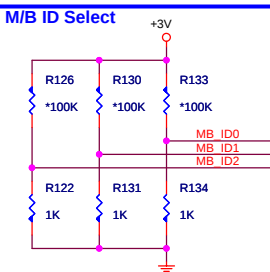
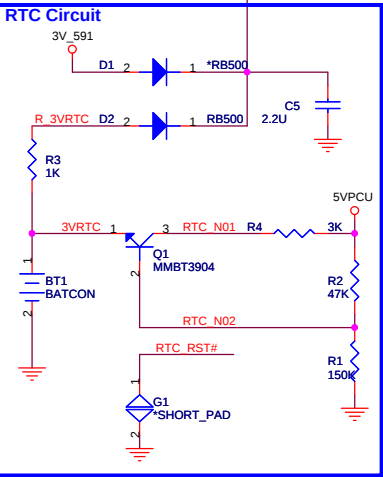


Diagram illustrating the power supply connections for the CRTDCPU:

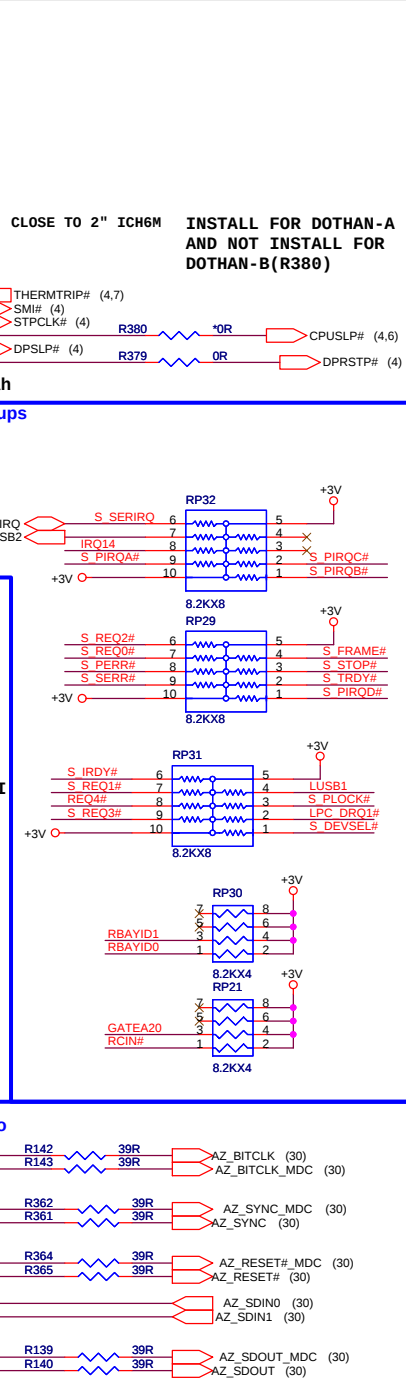
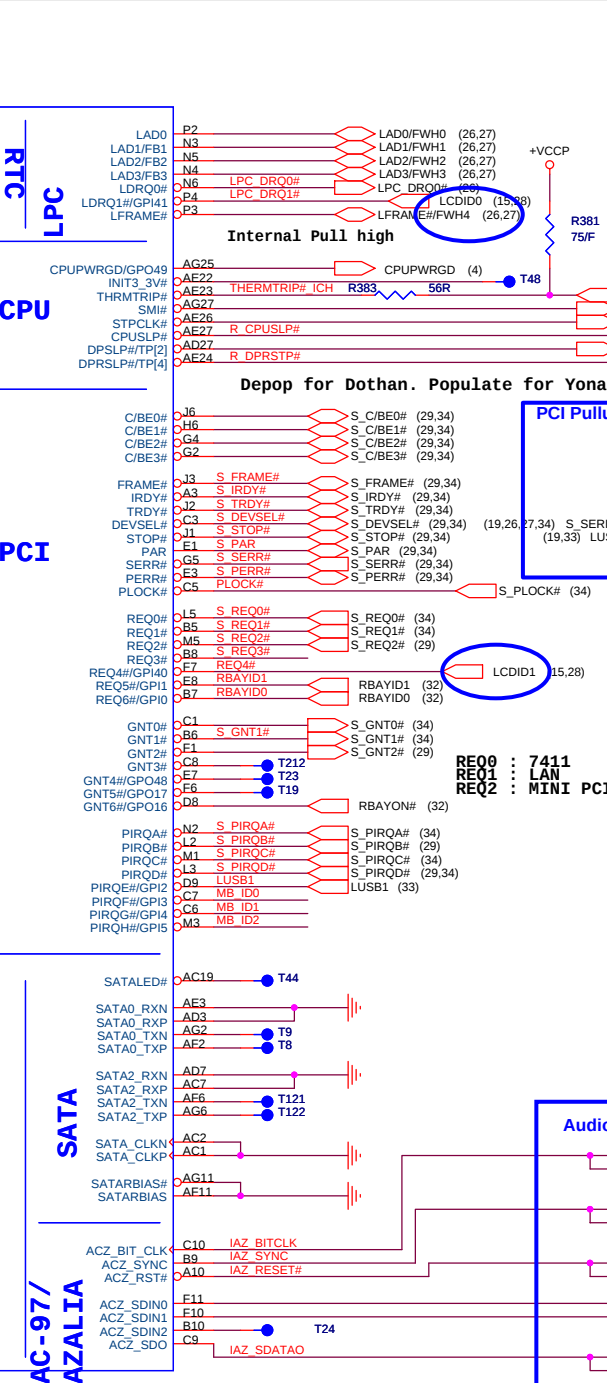
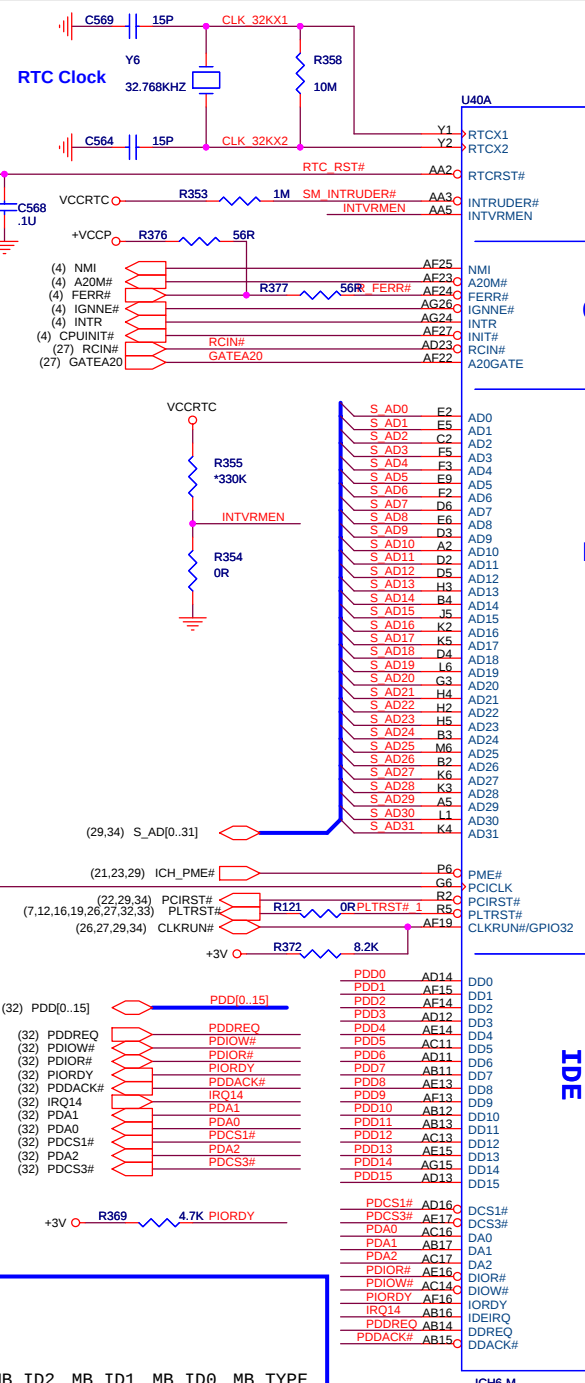
- +3V** input is connected through resistor **R559** to the **EXT@0R** pin.
- +2.5V** input is connected through resistor **R557** to the ***INT@0R** pin.
- Both **EXT@0R** and ***INT@0R** pins are connected to the **CRTDCPU** output.

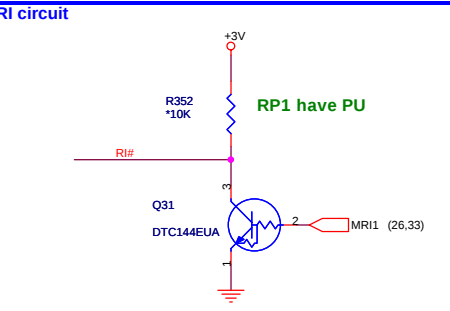
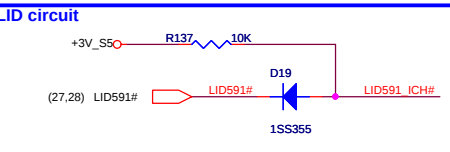
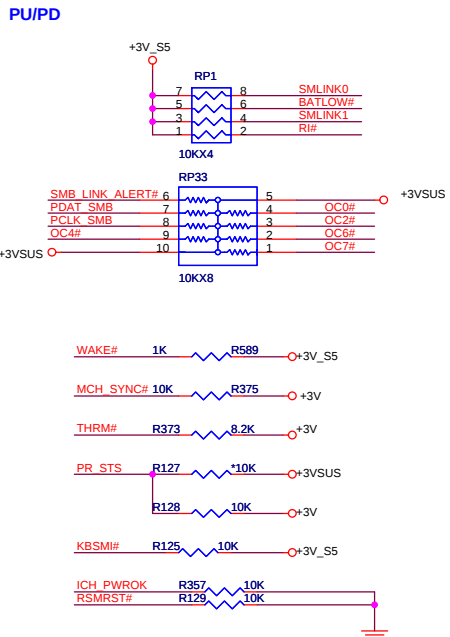
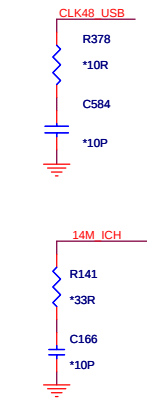
SWITCH CIRCUIT



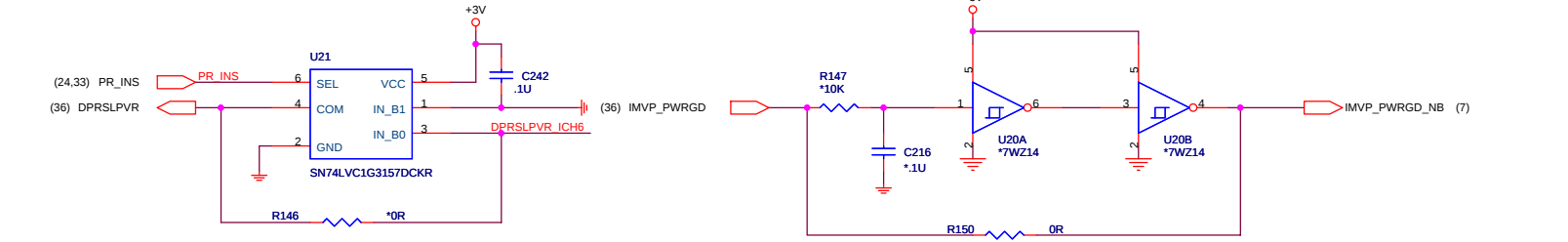


MB_ID2	MB_ID1	MB_ID0	MB TYPE
0	0	0	TYPE 1
0	0	1	TYPE 2
0	1	0	TYPE 3
0	1	1	TYPE 4
1	0	0	TYPE 5





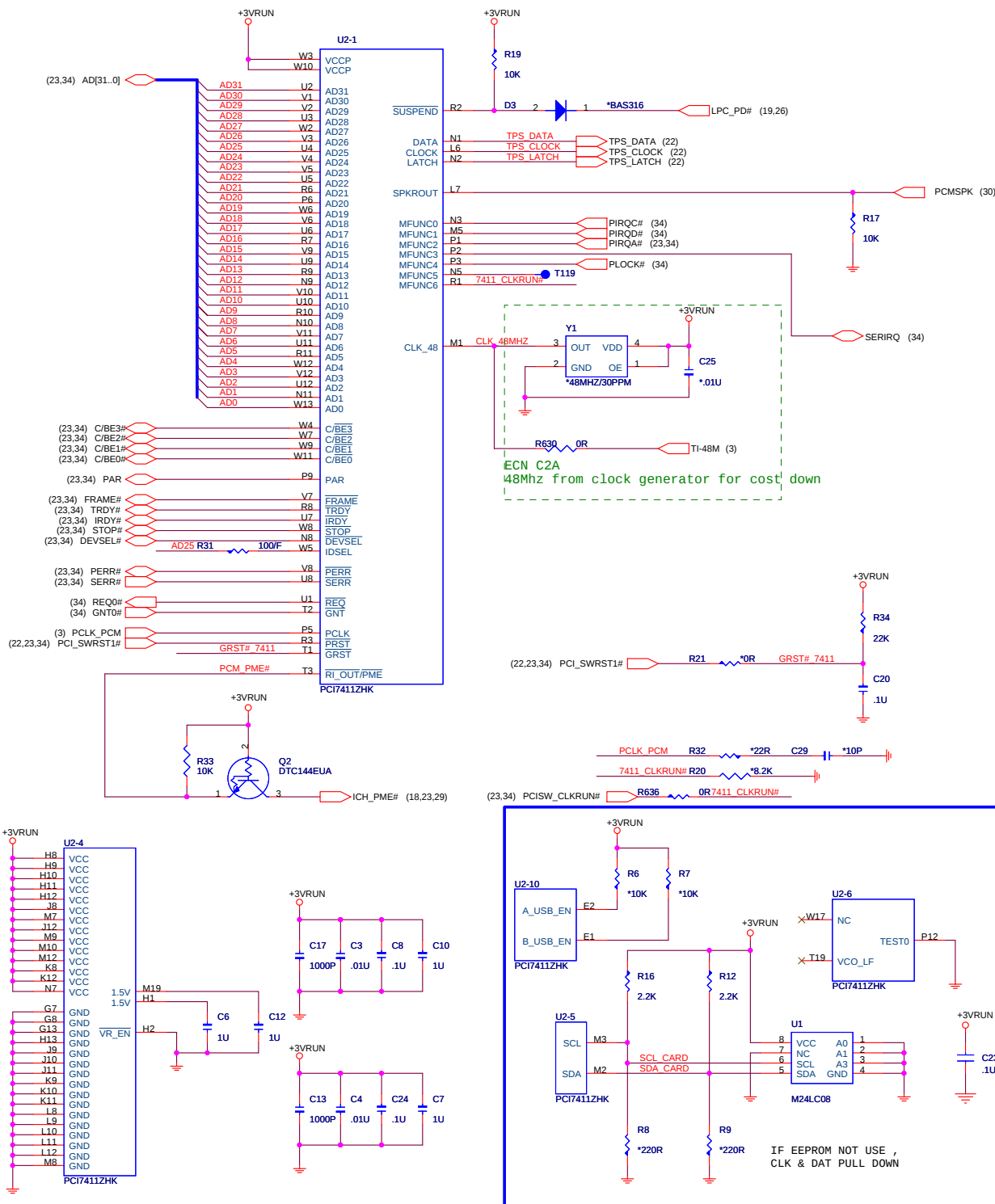
Power good to SB and NB/Deeper Sleep Voltage control for C4



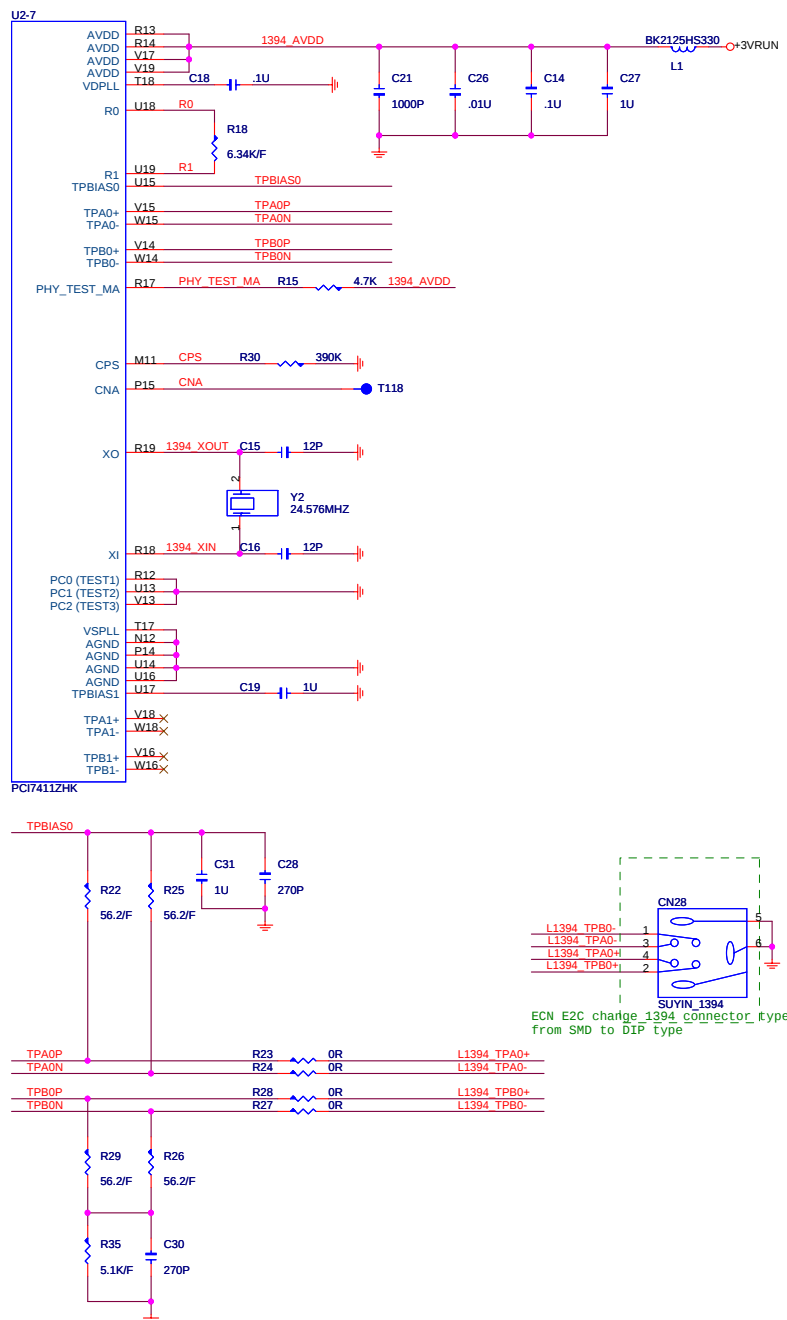


Size	Document Number ICH6-M (POWER & GND)	Rev B2A
Date:	Monday, August 22, 2005	Sheet 20 of 42

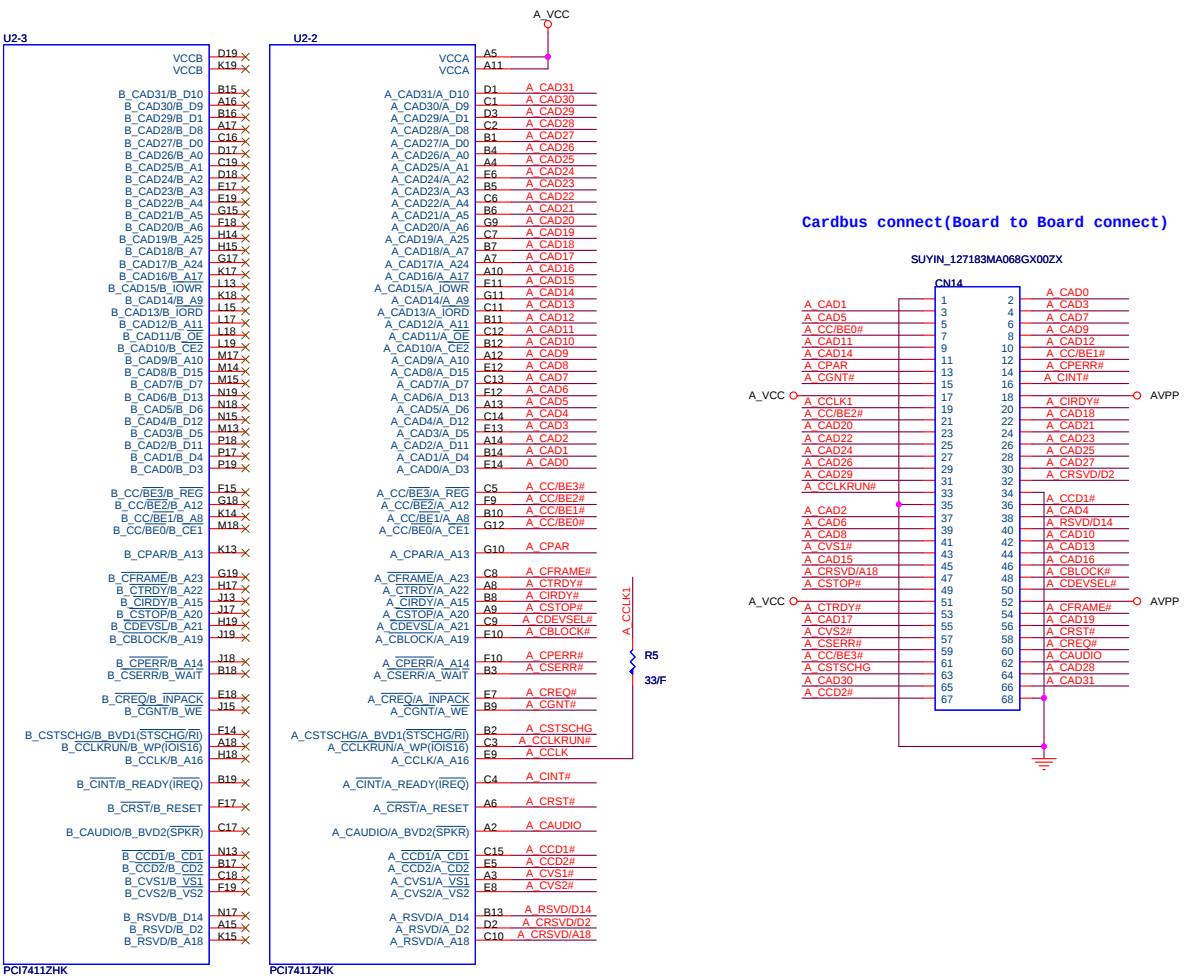
7411 PCI Interface



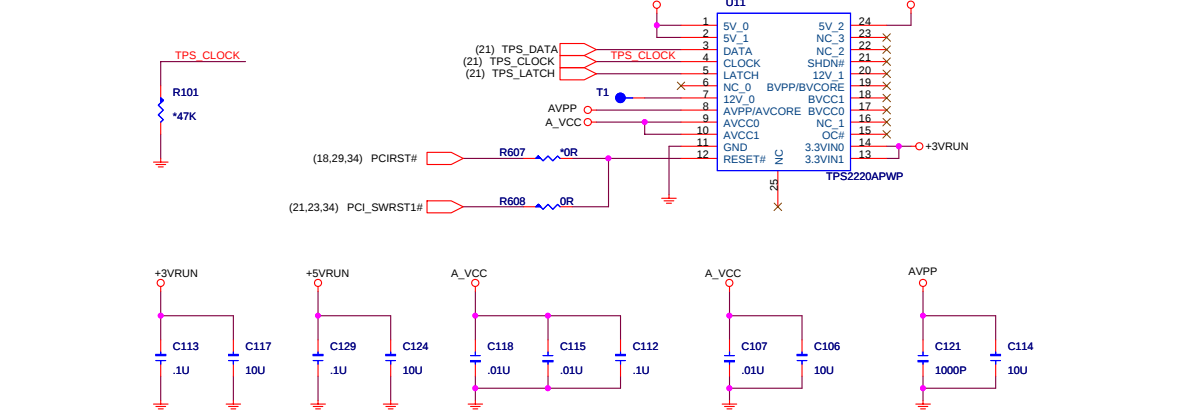
1394 Interface(CONN/EEPROM)



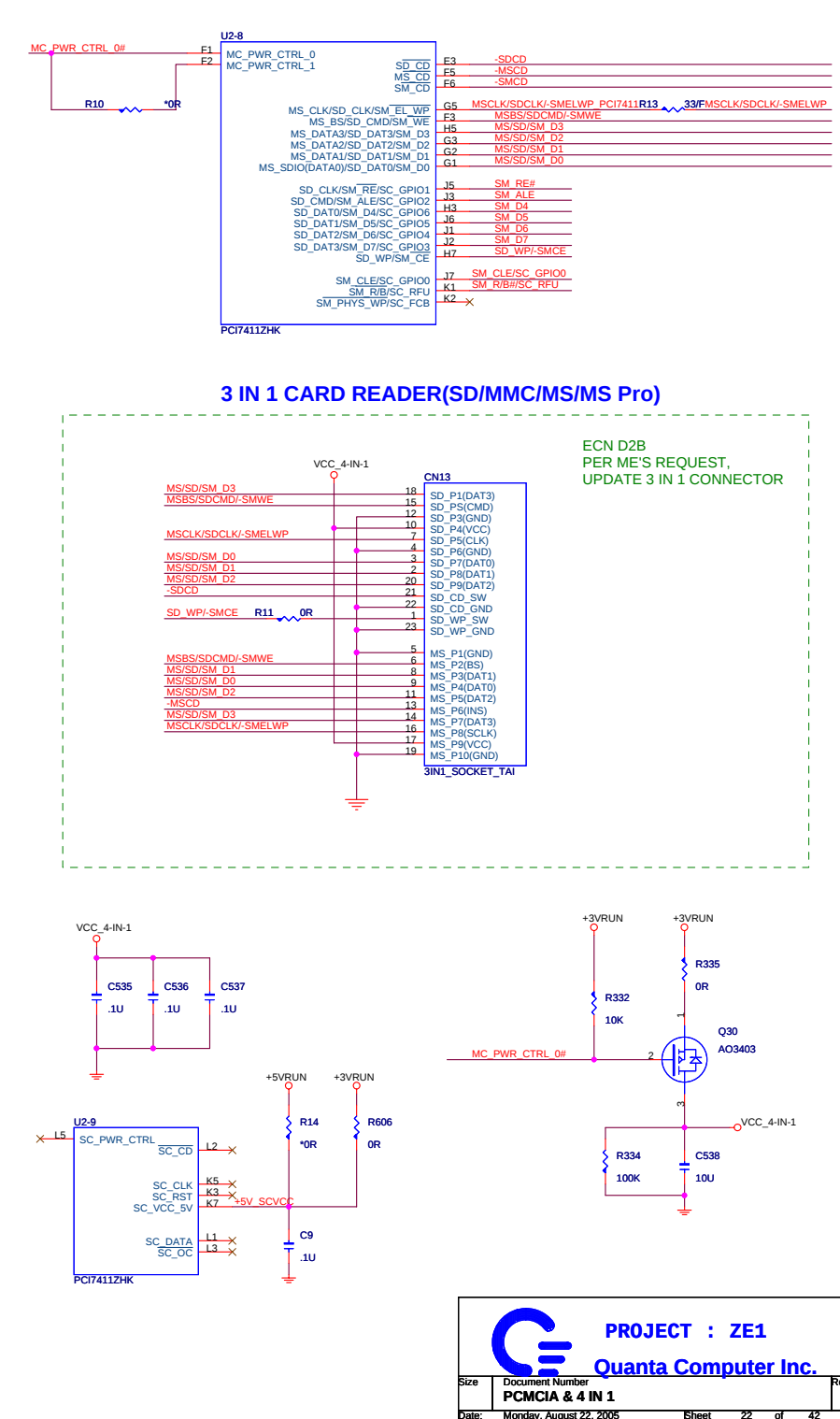
Cardbus Interface



Cardbus Power

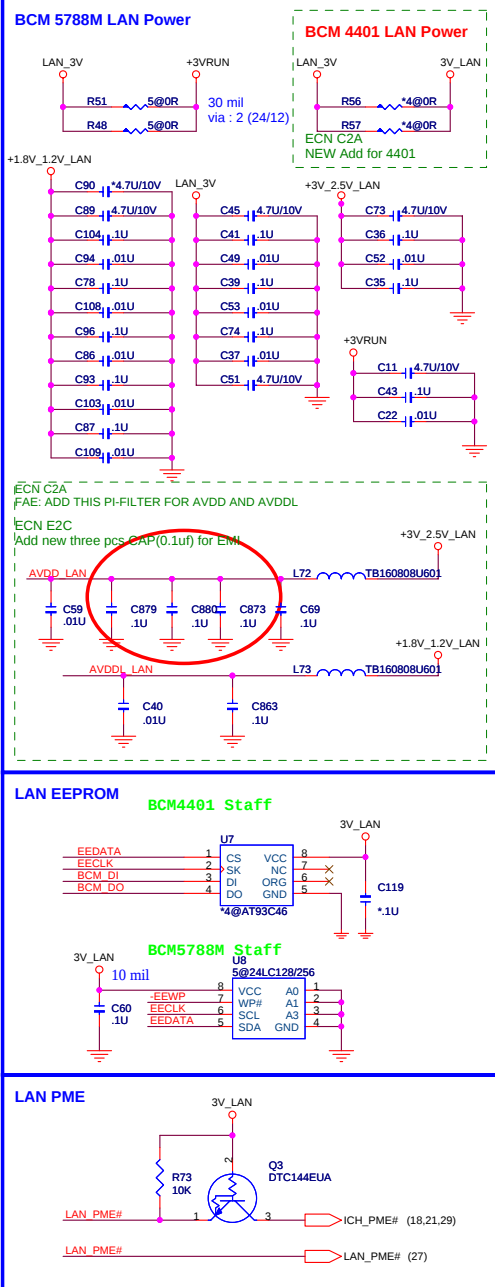
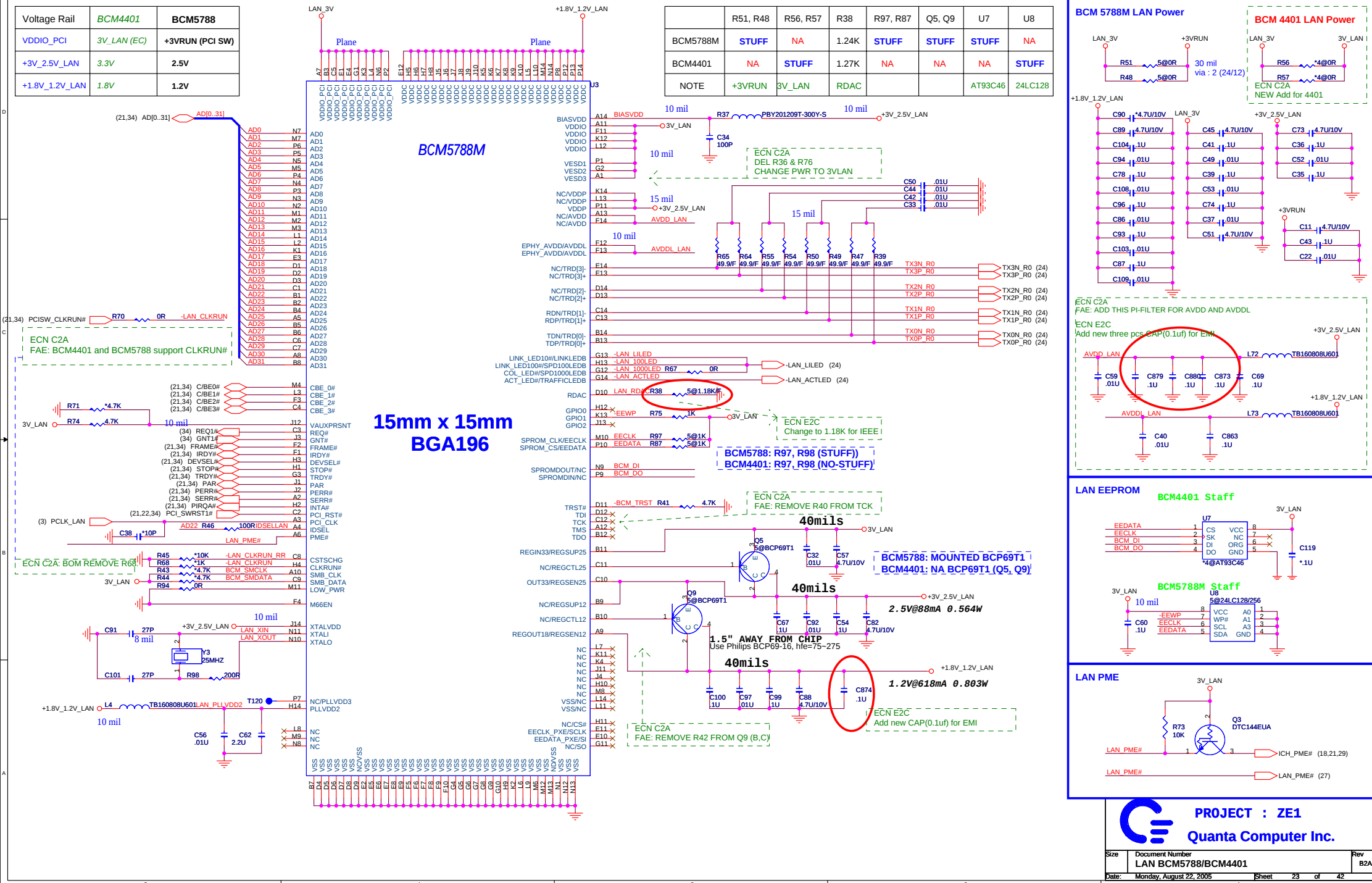


Card Reader Interface

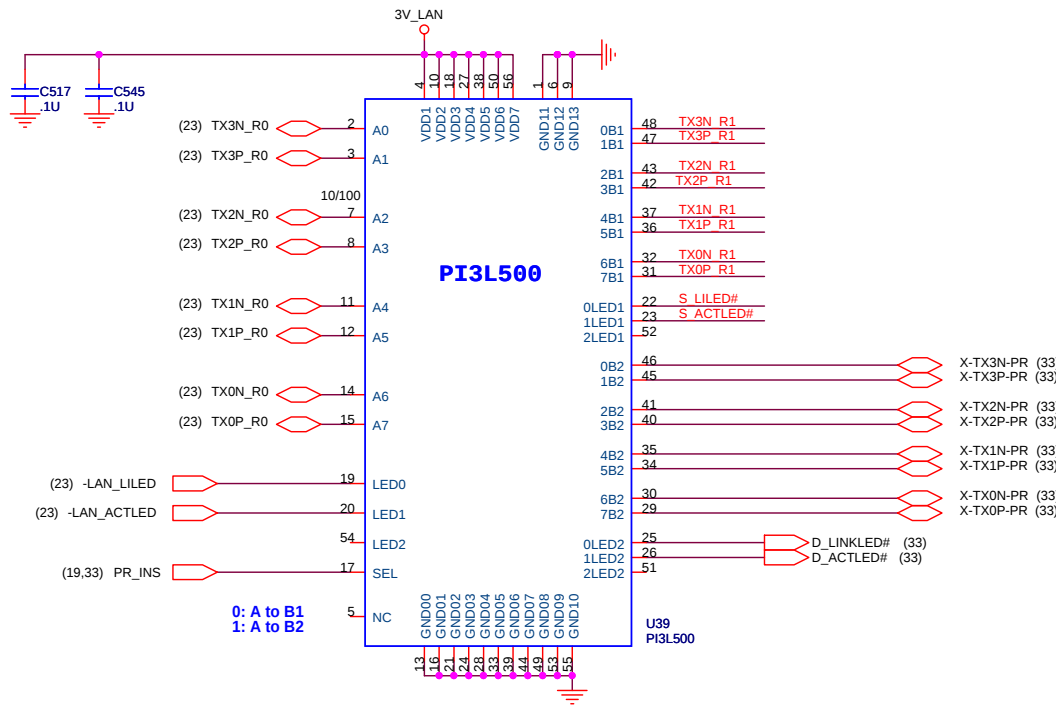


Voltage Rail	BCM4401	BCM5788
VDDIO_PCI	3V_LAN (EC)	+3VRUN (PCI SW)
+3V_2.5V_LAN	3.3V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V

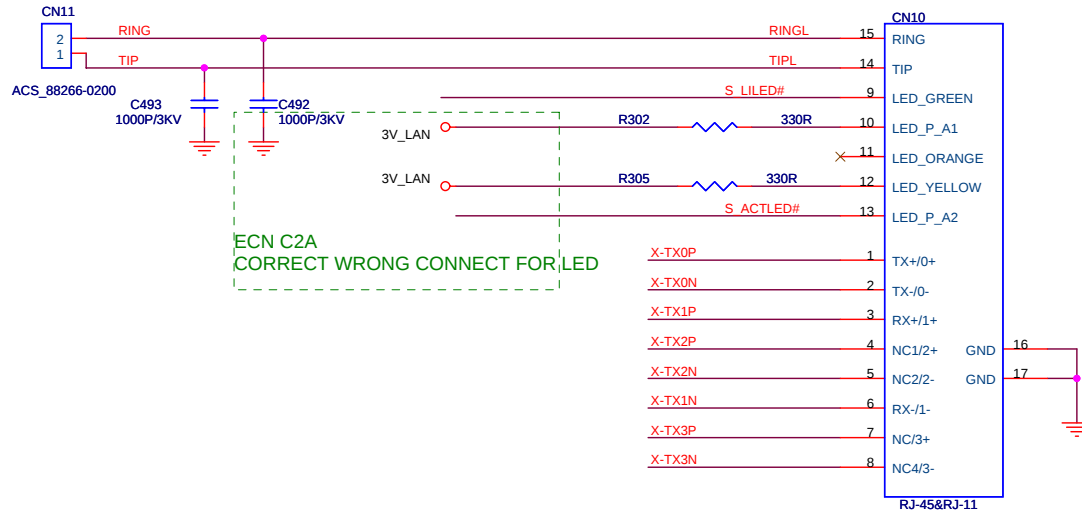
	R51, R48	R56, R57	R38	R97, R87	Q5, Q9	U7	U8
BCM5788M	STUFF	NA	1.24K	STUFF	STUFF	STUFF	NA
BCM4401	NA	STUFF	1.27K	NA	NA	NA	STUFF
NOTE	+3VRUN	3V_LAN	RDAC			AT93C46	24LC128



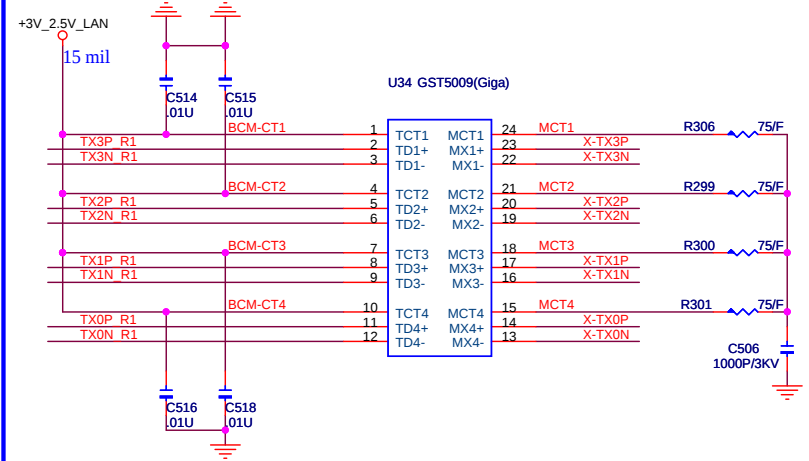
LAN Switch



Modem conn and LAN connect

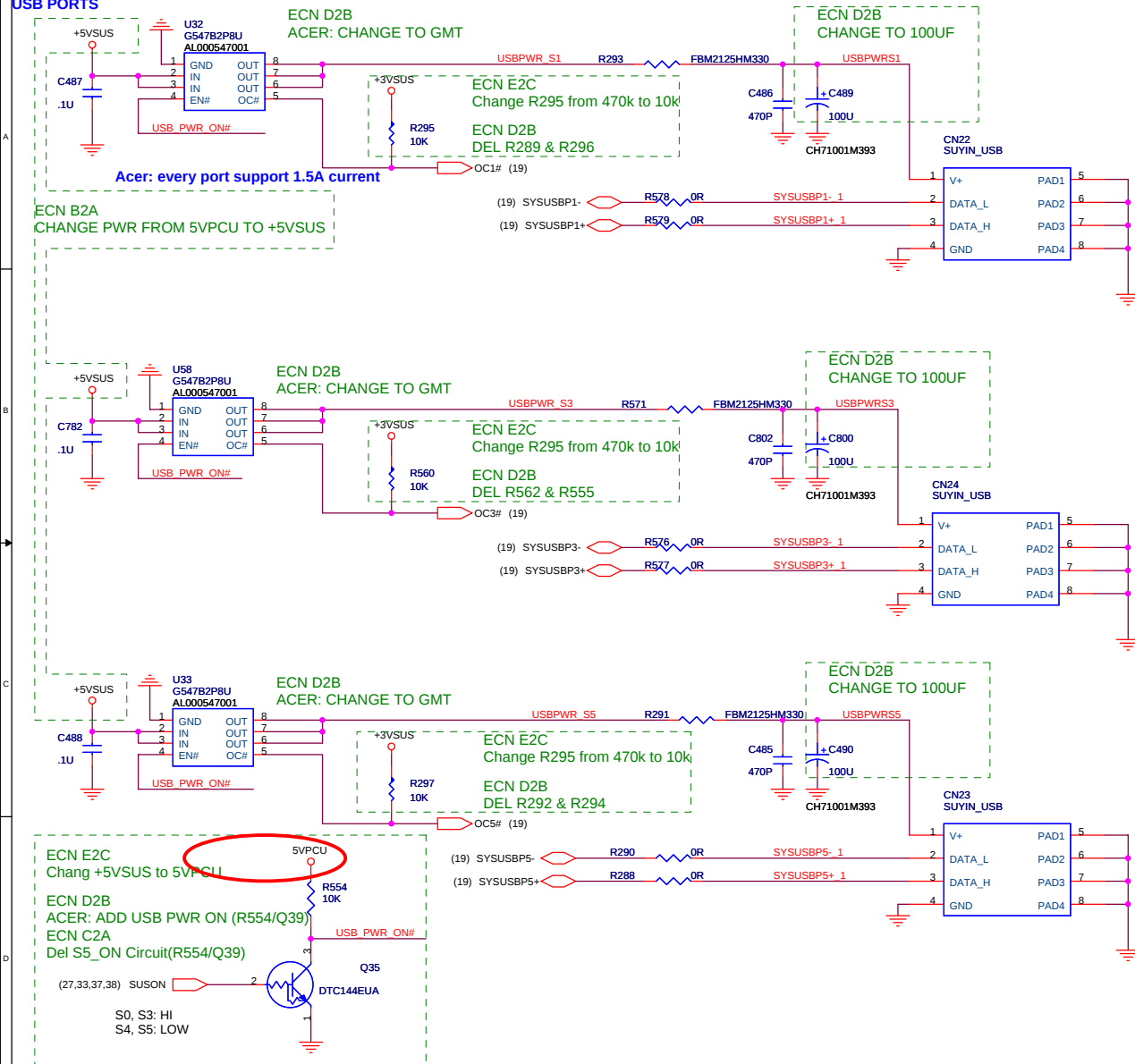


LAN transformer

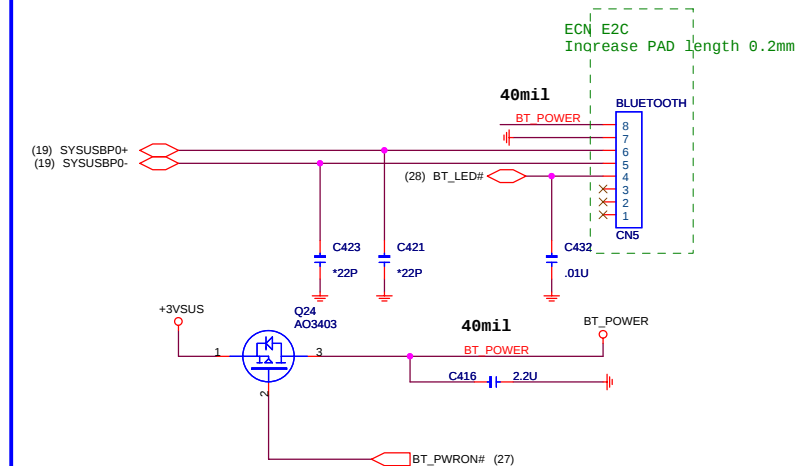


PROJECT : ZE1
Quanta Computer Inc.

USB PORTS

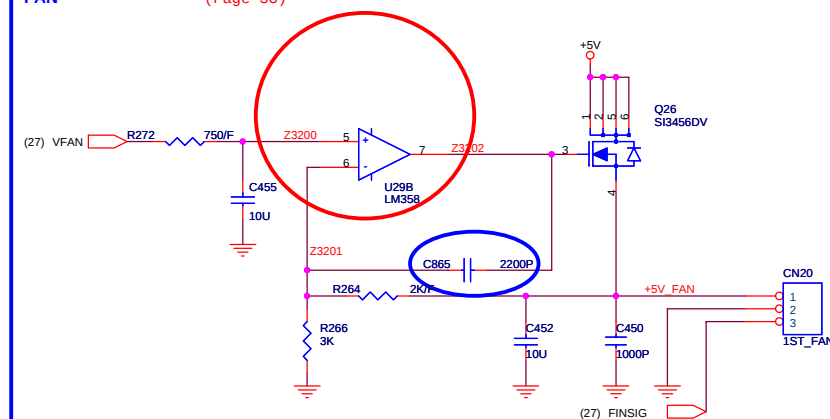


Bluetooth



FAN

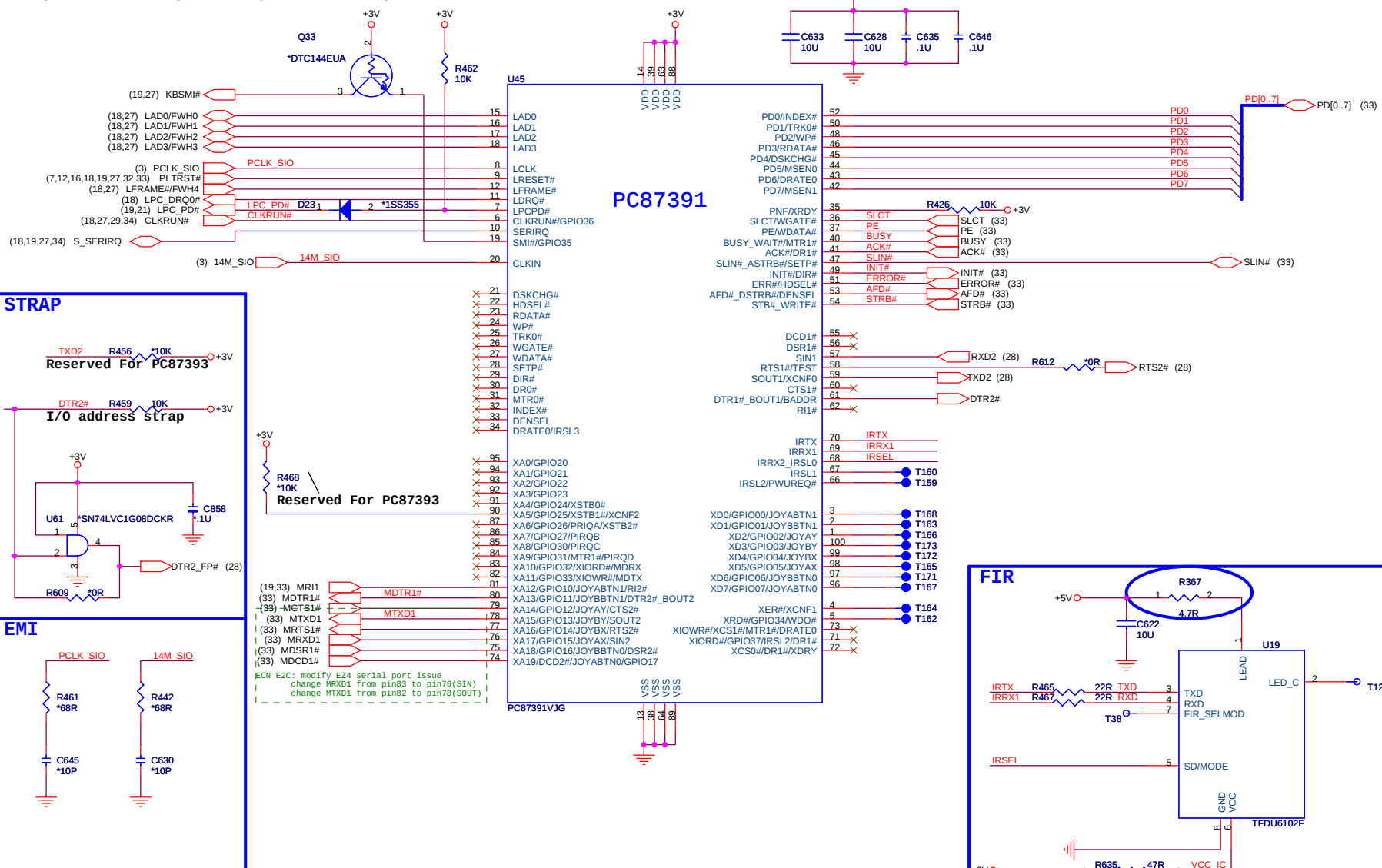
U29 use together with Transfer 2.5V circuit
(Page 38)



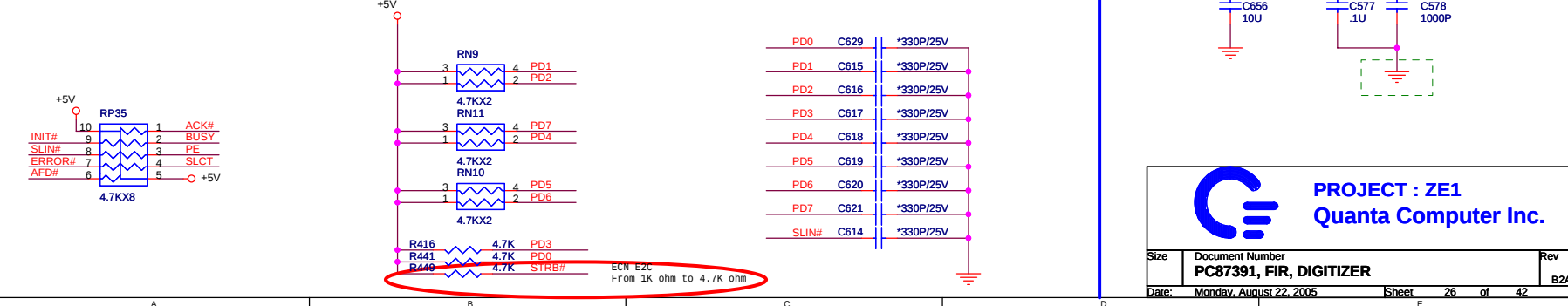
PROJECT : ZE1
Quanta Computer Inc.

Size	Document Number	Rev
USB PORTS & BLUETOOTH & FAN		D2E
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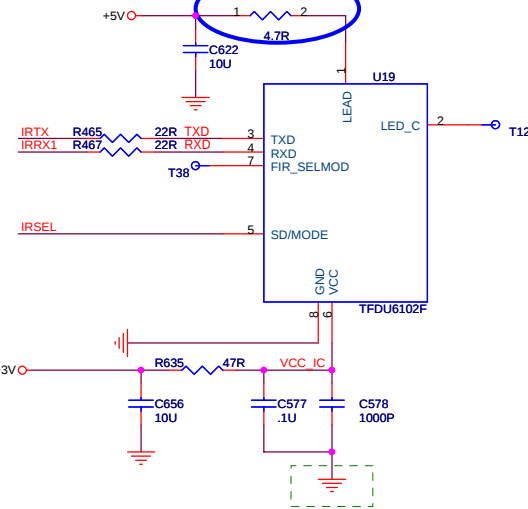
SIO(LPT/Serial port/Digitizer/FIR)



LPT PU



FIR



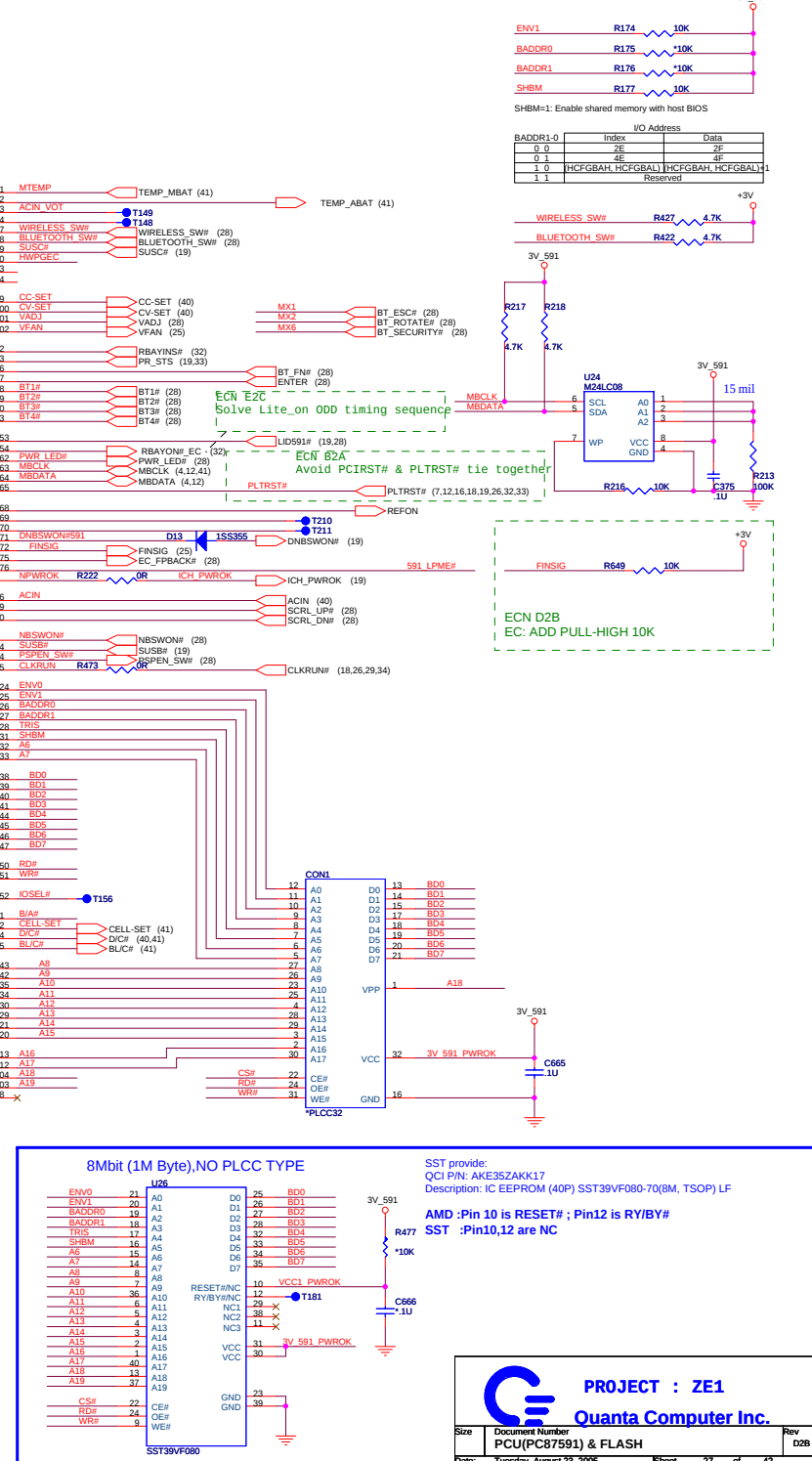
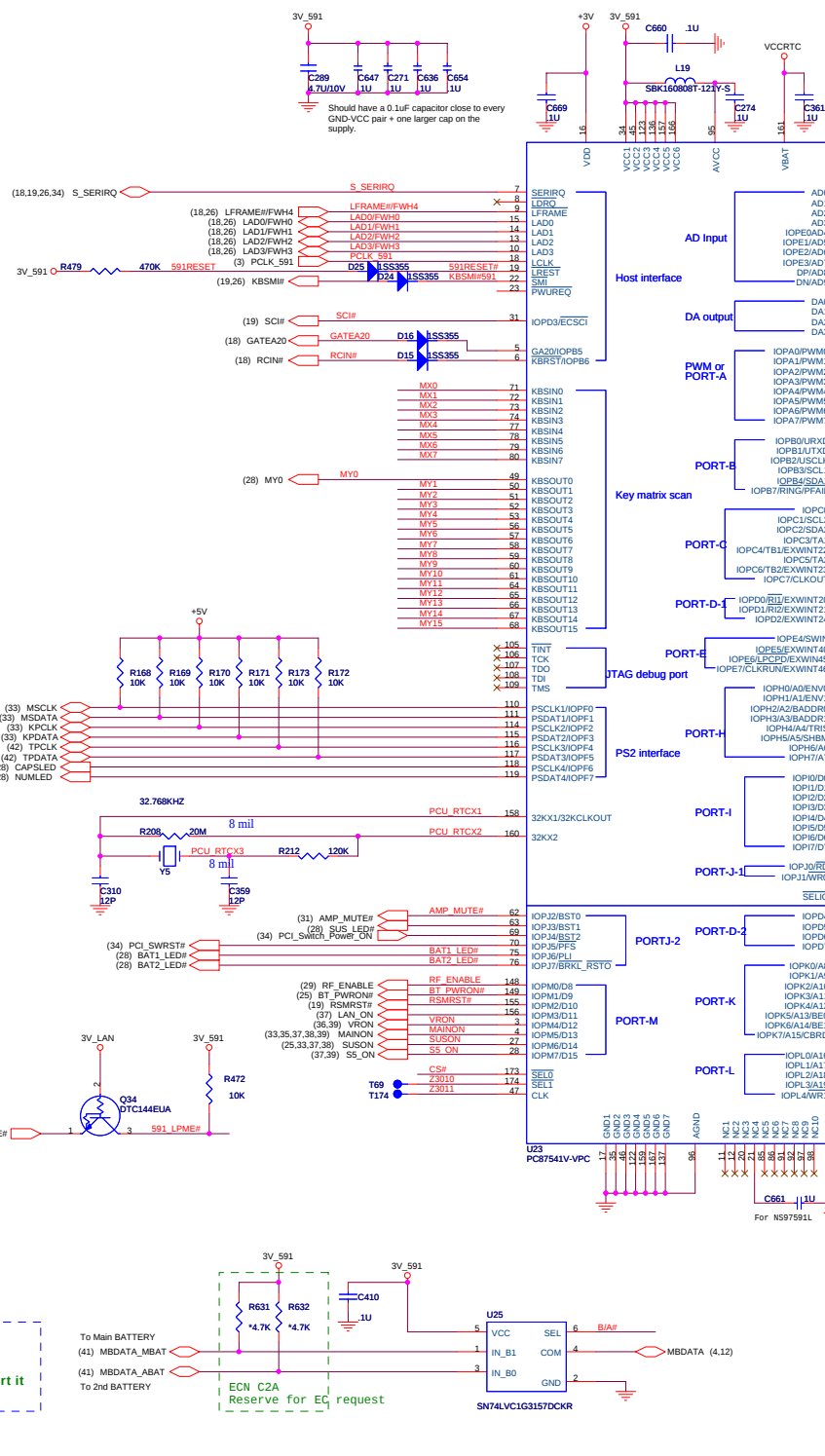
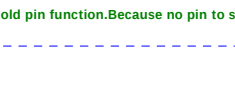
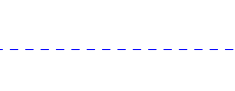
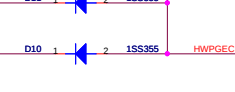
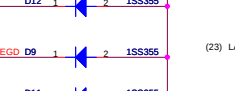
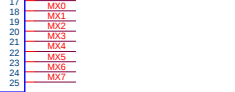
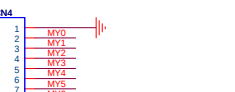
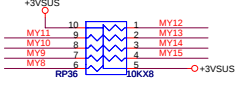
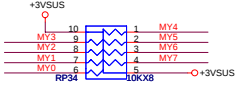
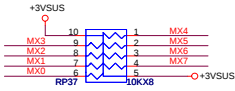


PROJECT : ZE1
Quanta Computer Inc.

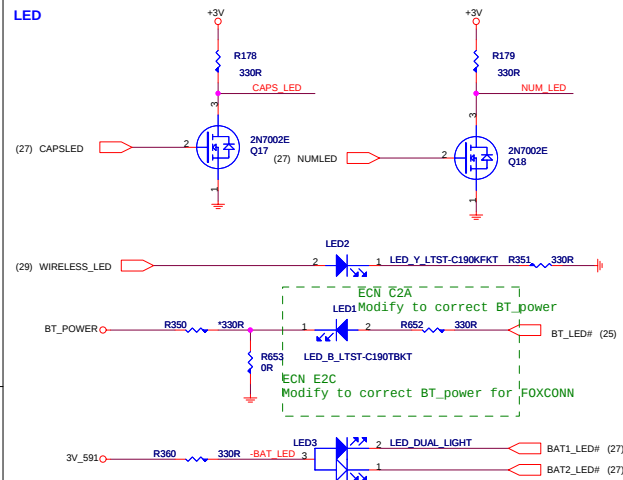
Size	Document Number	Rev
	PC87391, FIR, DIGITIZER	B2A
Date:	Monday, August 22, 2005	Sheet 26 of 42

EC suggestion for S3 wake-up change power from 5VPCU to +3VSUS

KEYBOARD

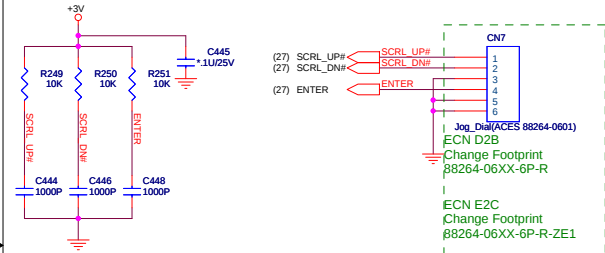


LED

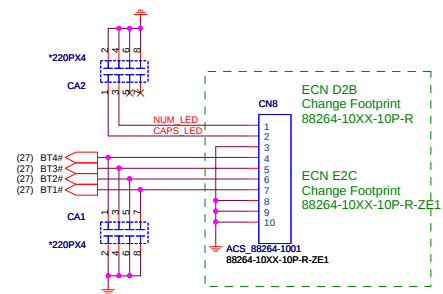


**TRACK POINT CIRCUITS
MOVE TO PAGE 42**

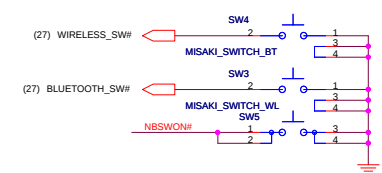
Jogdial & CONN.



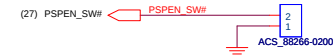
Quick Button Board



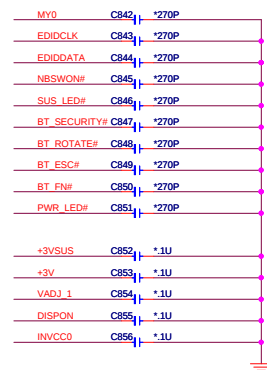
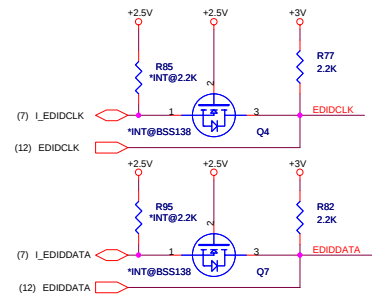
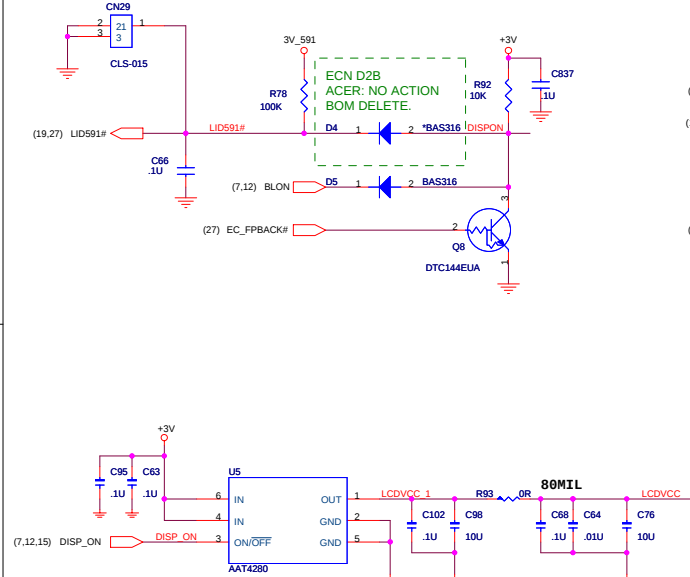
Switch



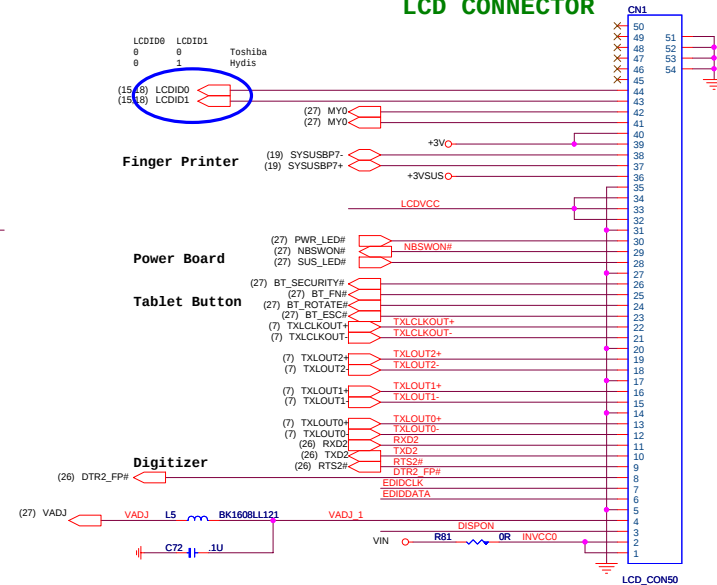
Pressure Sensitive Pen Detect



LID/Display on



LCD CONNECTOR

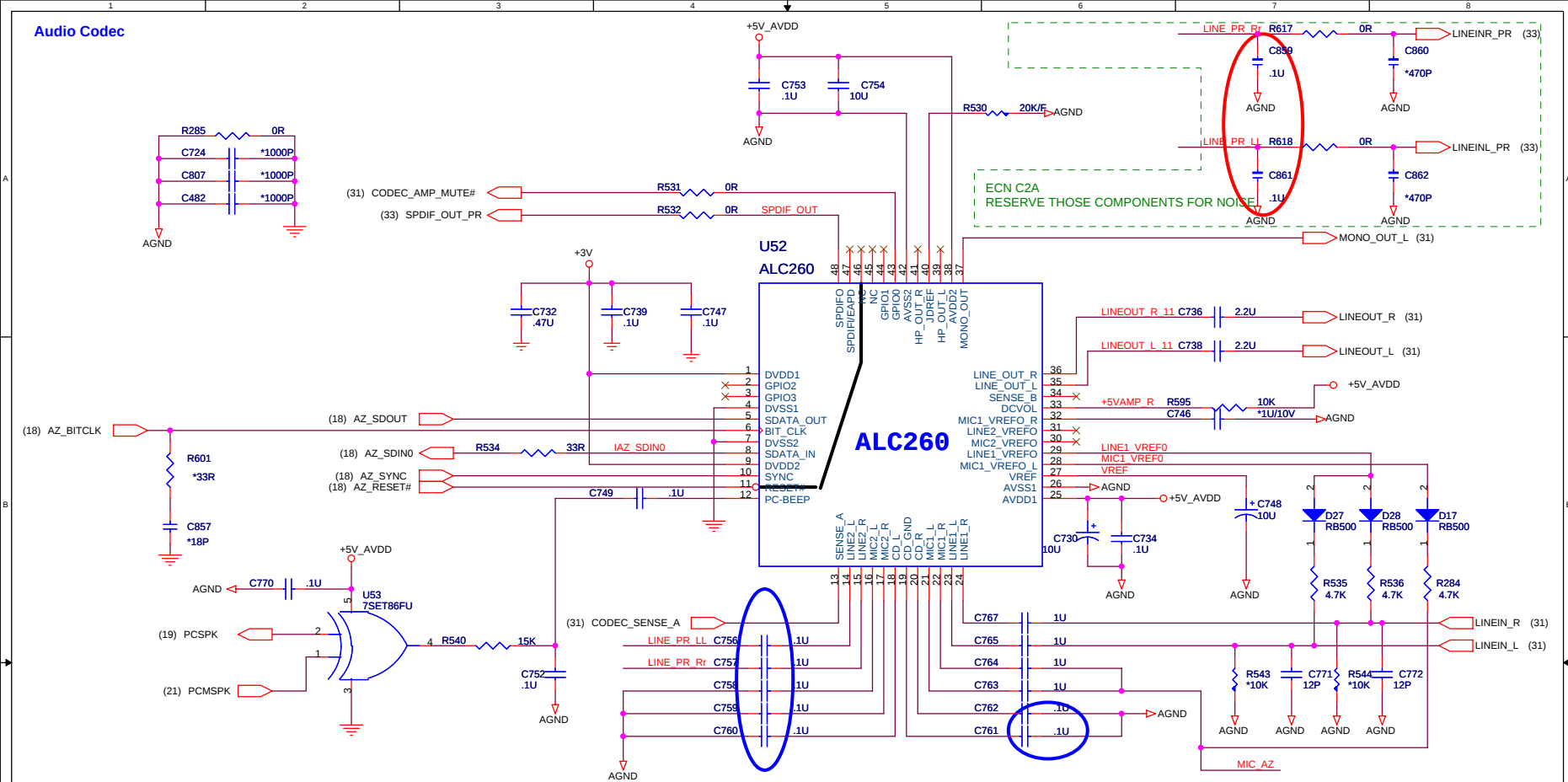


PROJECT : ZE1
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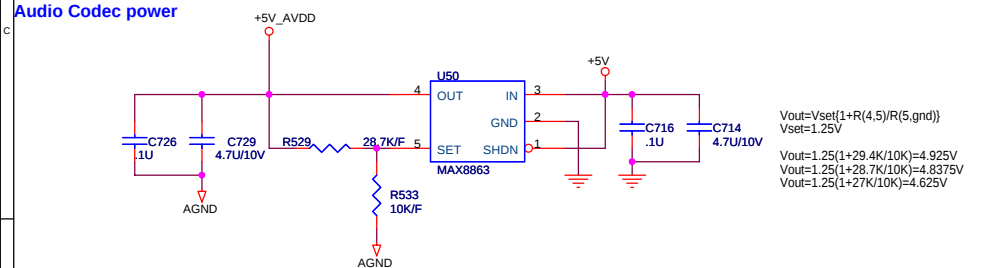
Size	Document Number LED, T/P, FAN, Q-BUTTON, LCD CONN.	Rev D2B
Date:	Monday, August 22, 2005	Sheet 28 of 42

Rev
B2A

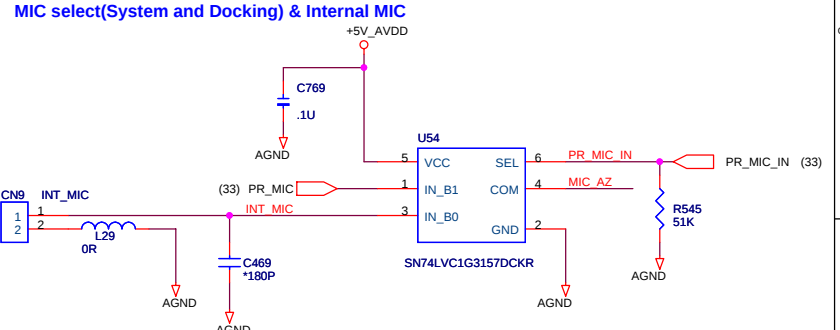
Audio Codec



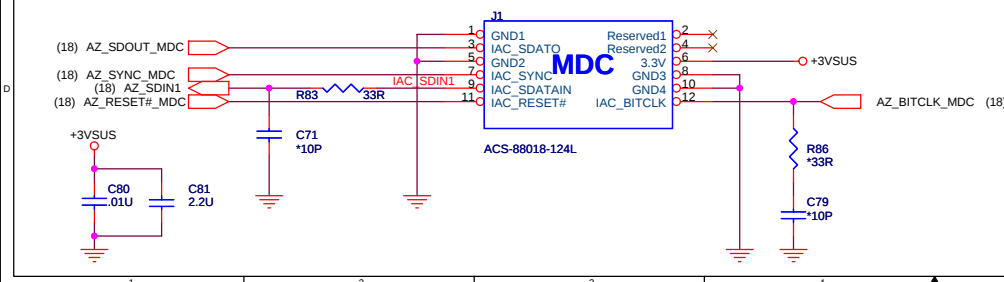
Audio Codec power



MIC select(System and Docking) & Internal MIC



Azalia Modem



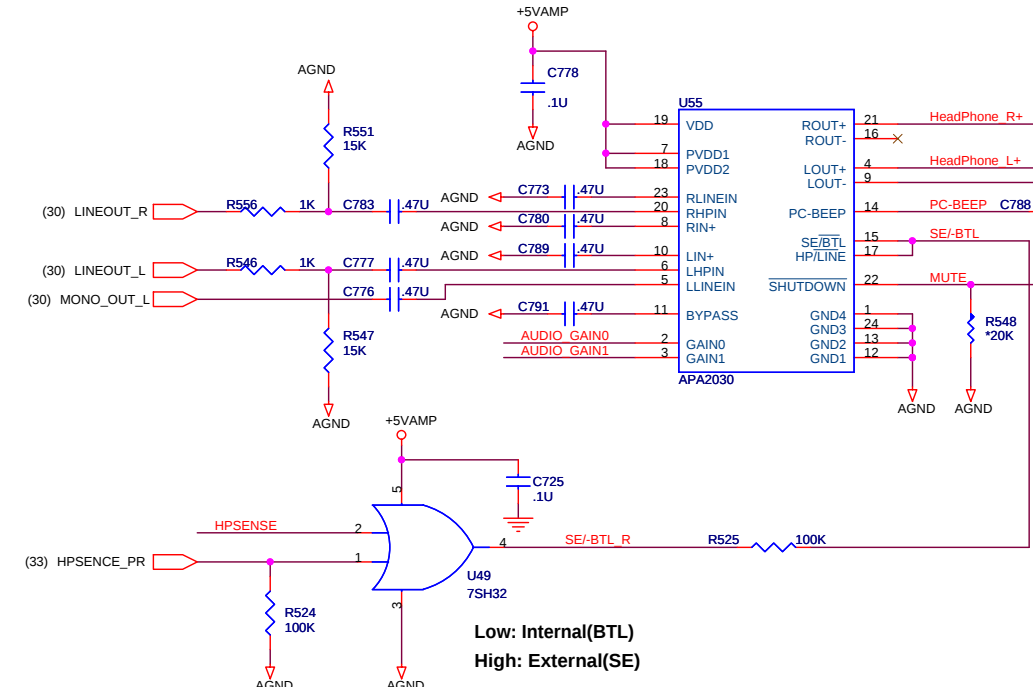
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

PROJECT : ZE1

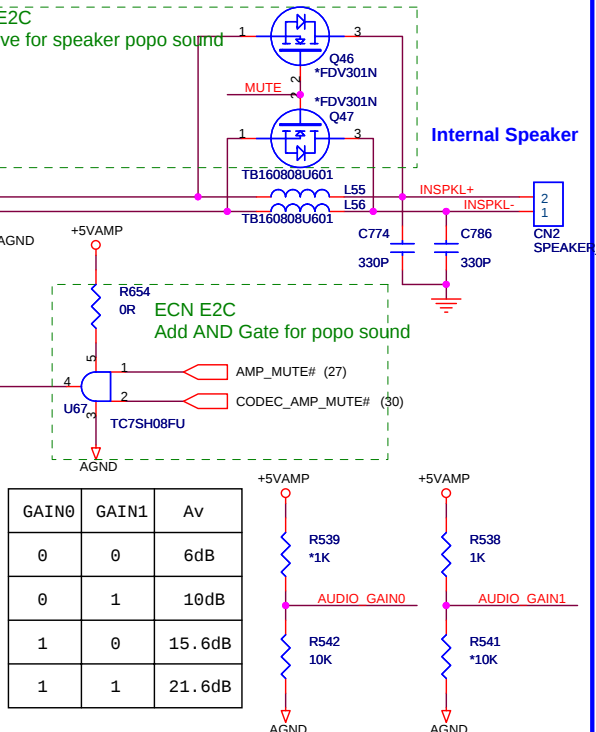
Quanta Computer Inc.

Size	Document Number	Rev
	ALC260 CODEC/MDC 1.5	B2A
Date:	Tuesday, August 23, 2005	Sheet 30 of 42

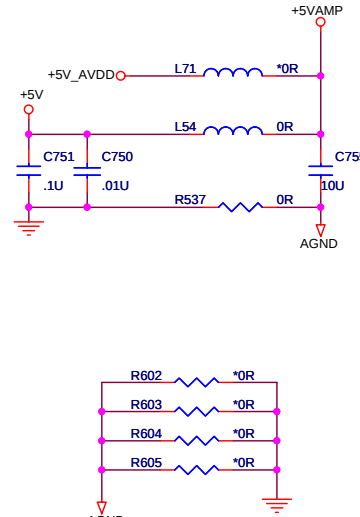
Audio Amplifier



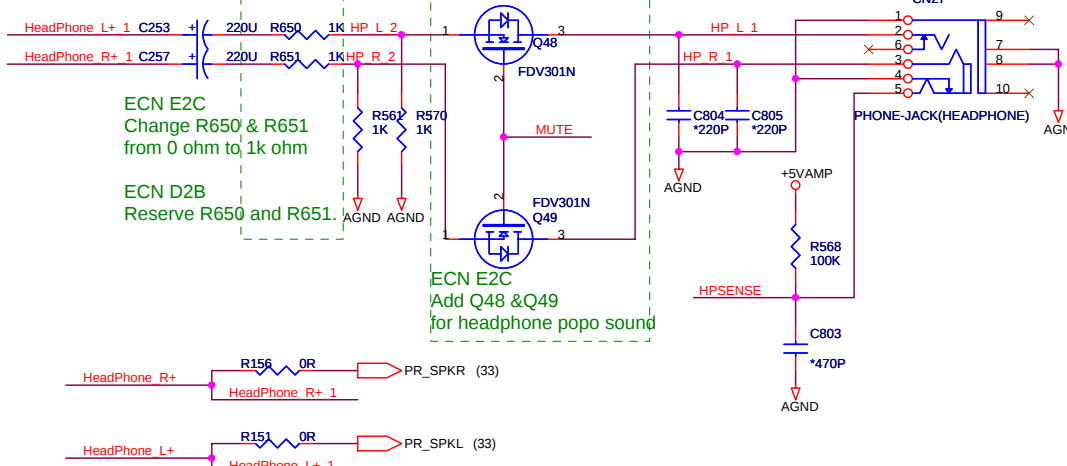
ECN E2C
Reserve for speaker popo sound



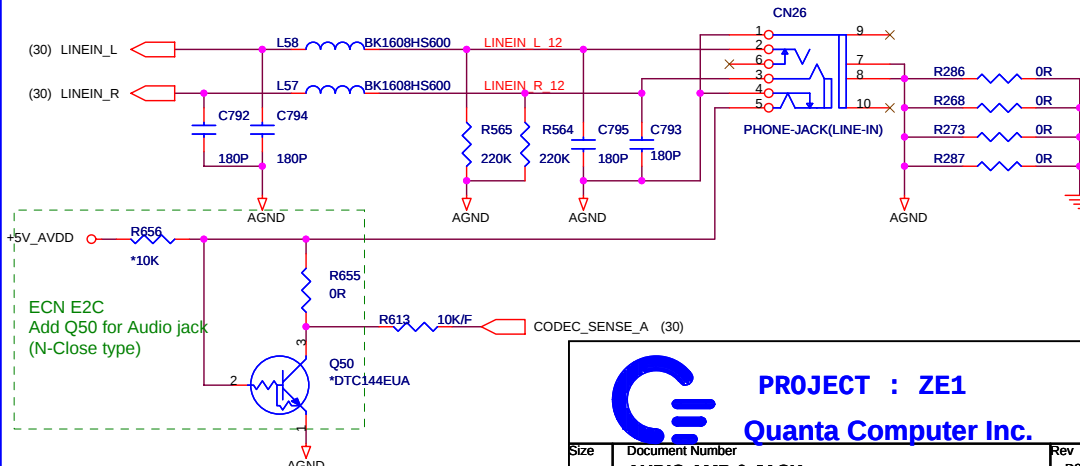
AMP power



Head phone/Line out

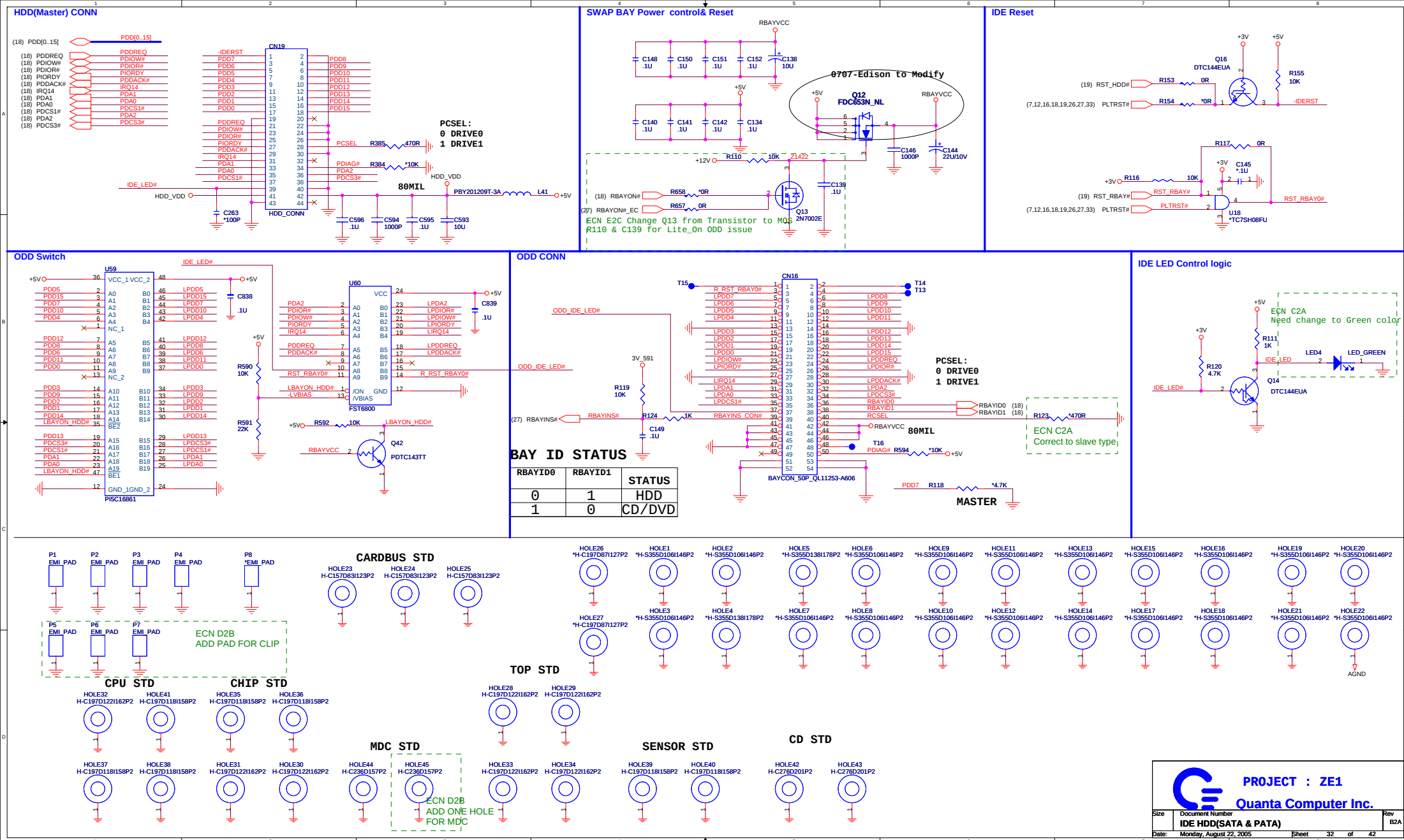


Mic in/Line in

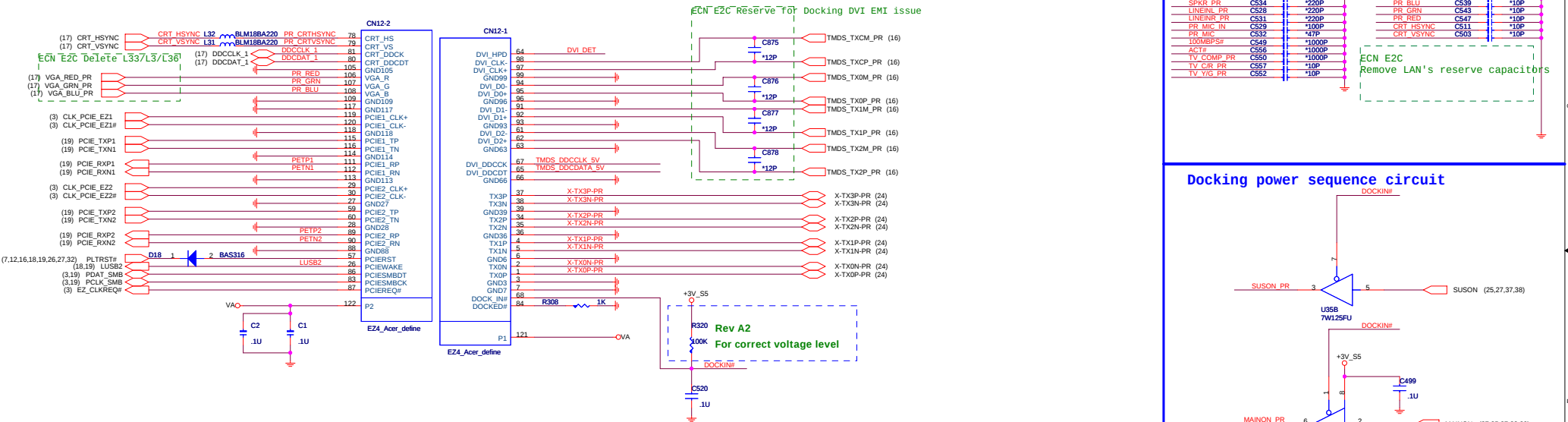
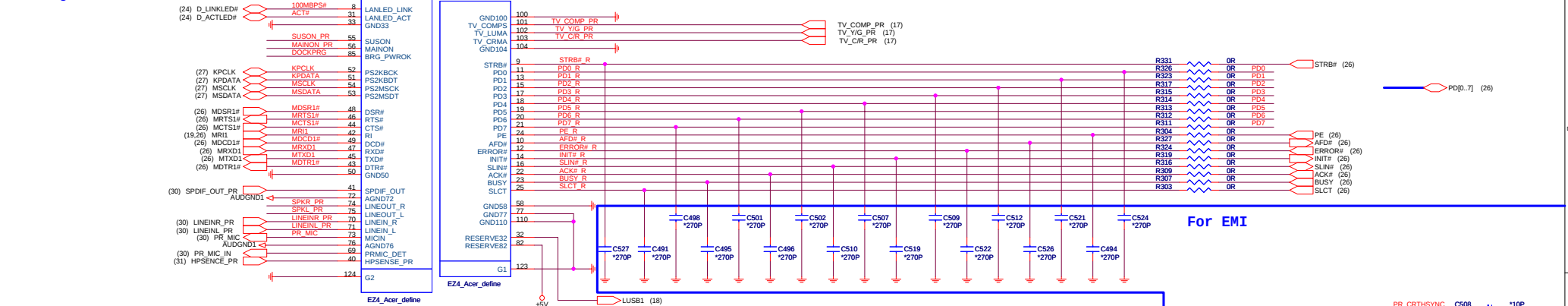


PROJECT : ZE1
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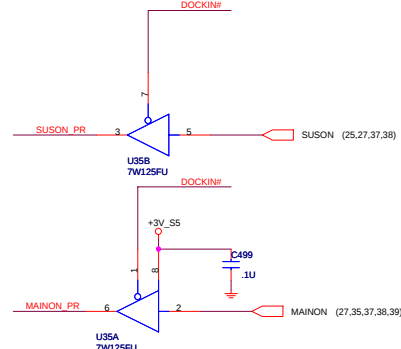
Size	Document Number AUDIO AMP & JACK	Rev D2
Date	Monday, August 22, 2005	Sheet 31 of 42



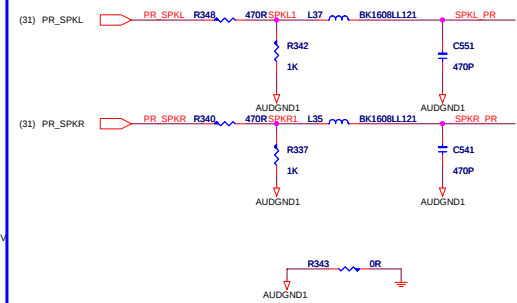
Docking Interface



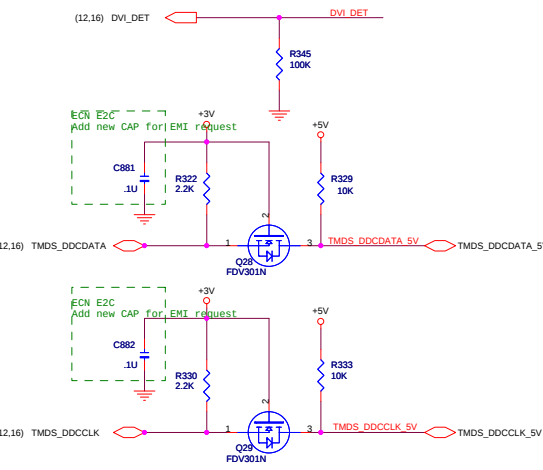
Docking power sequence circuit



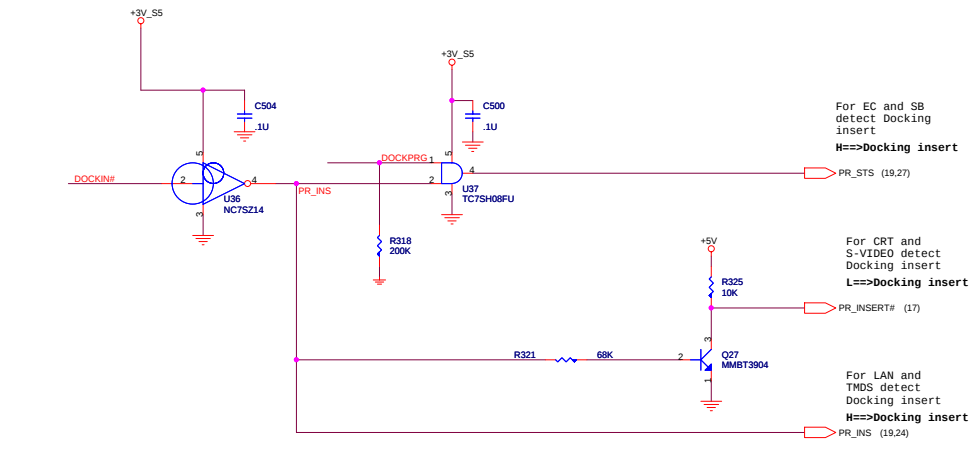
Docking Audio circuit



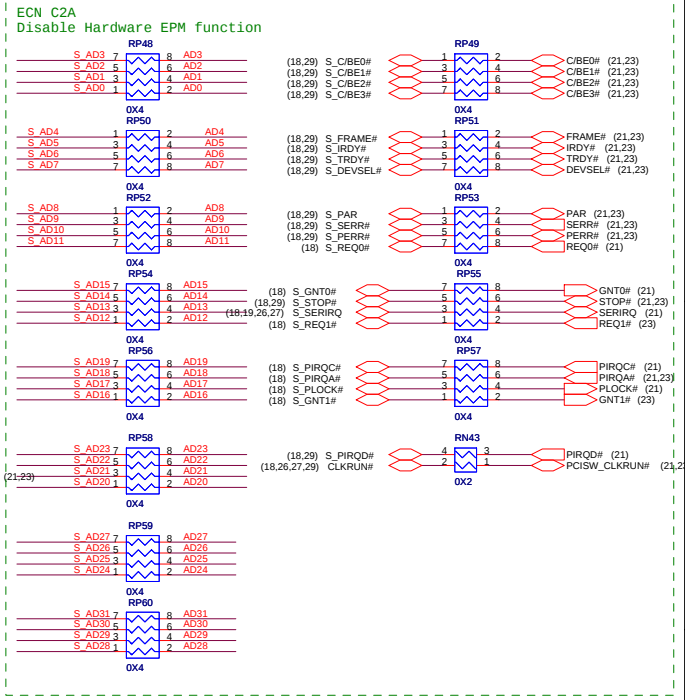
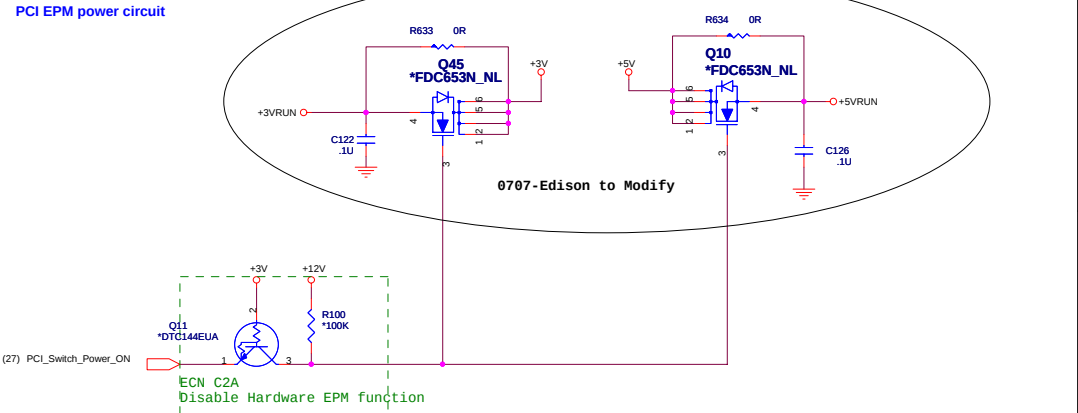
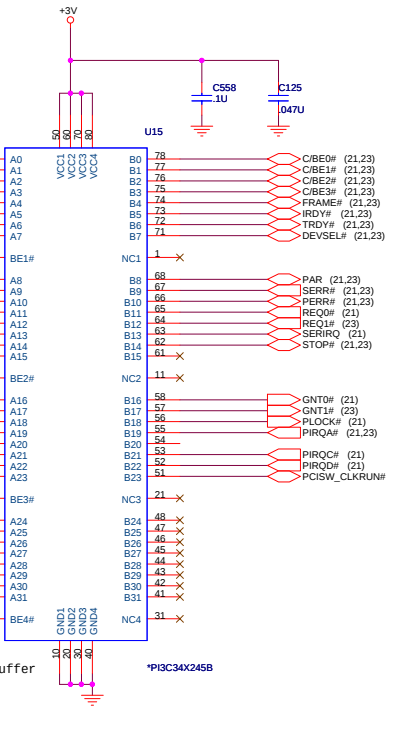
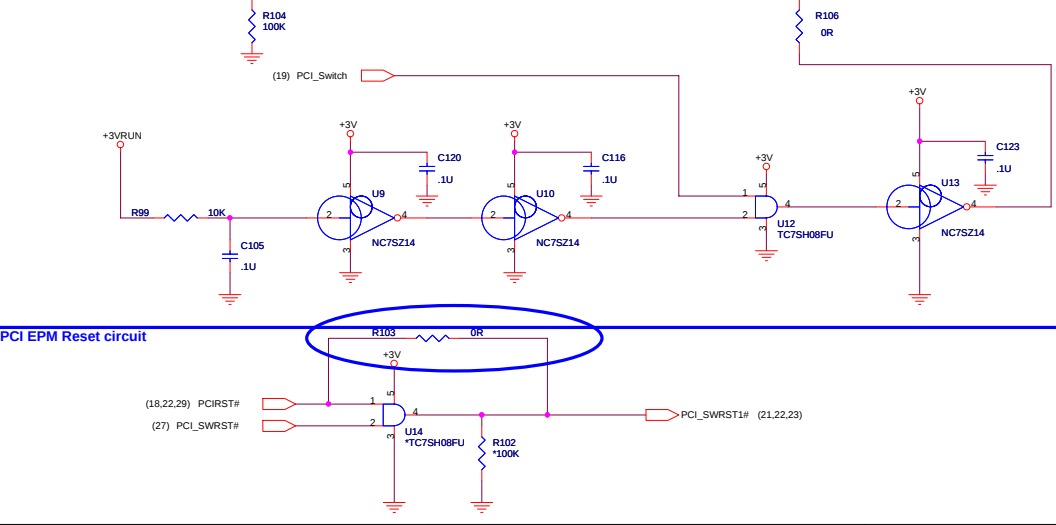
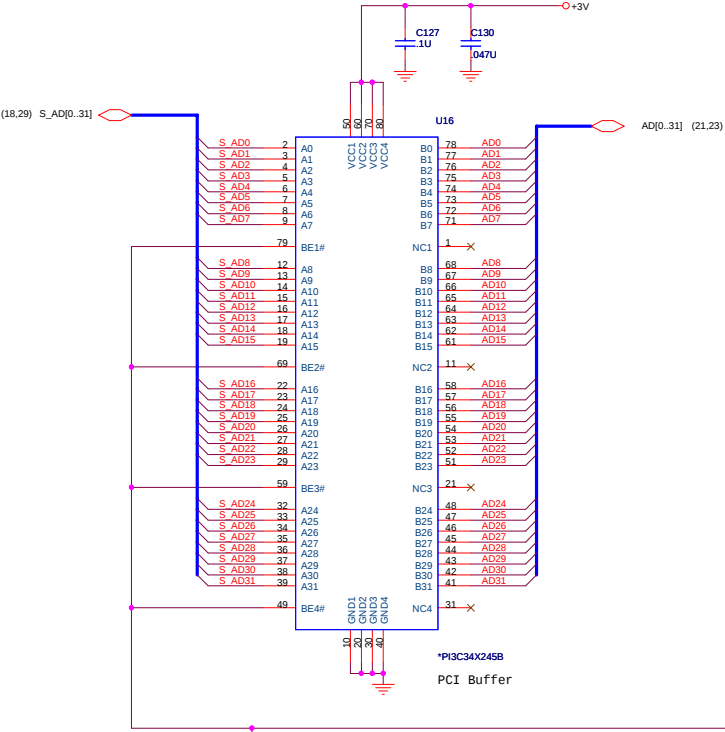
Docking TMDS circuit

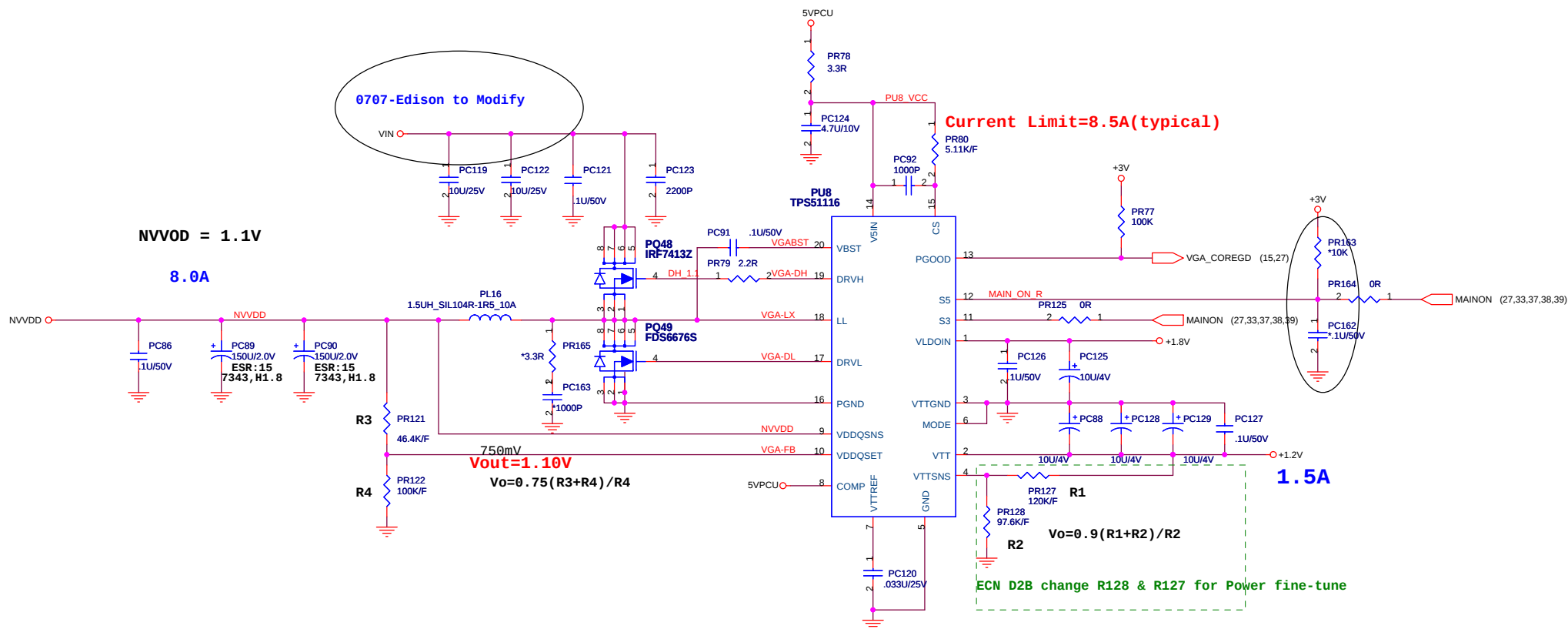


Docking Insert circuit

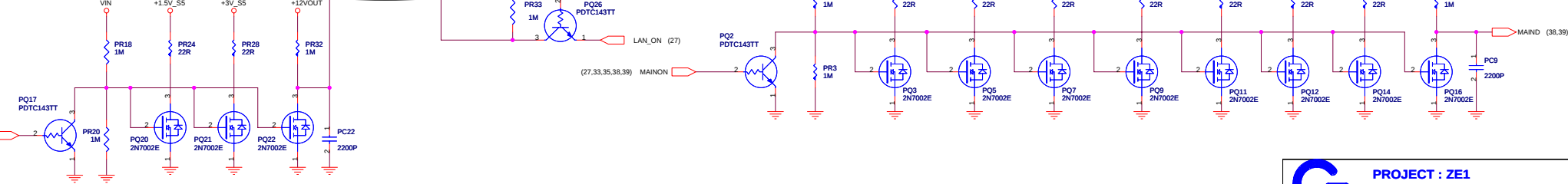
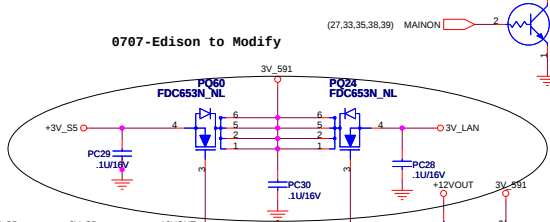
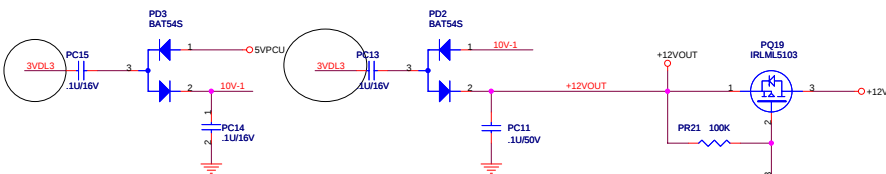
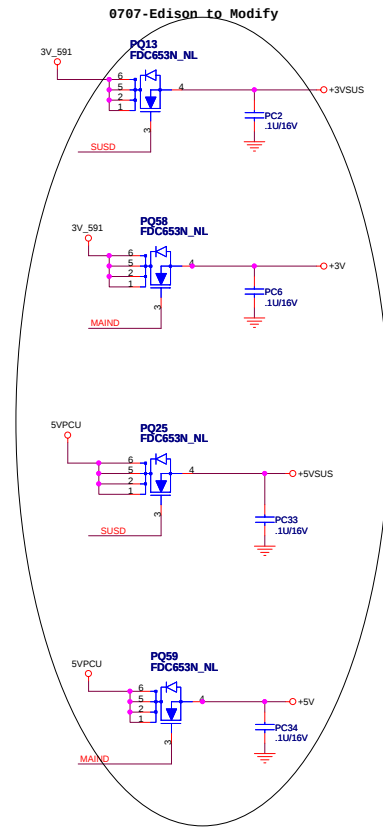
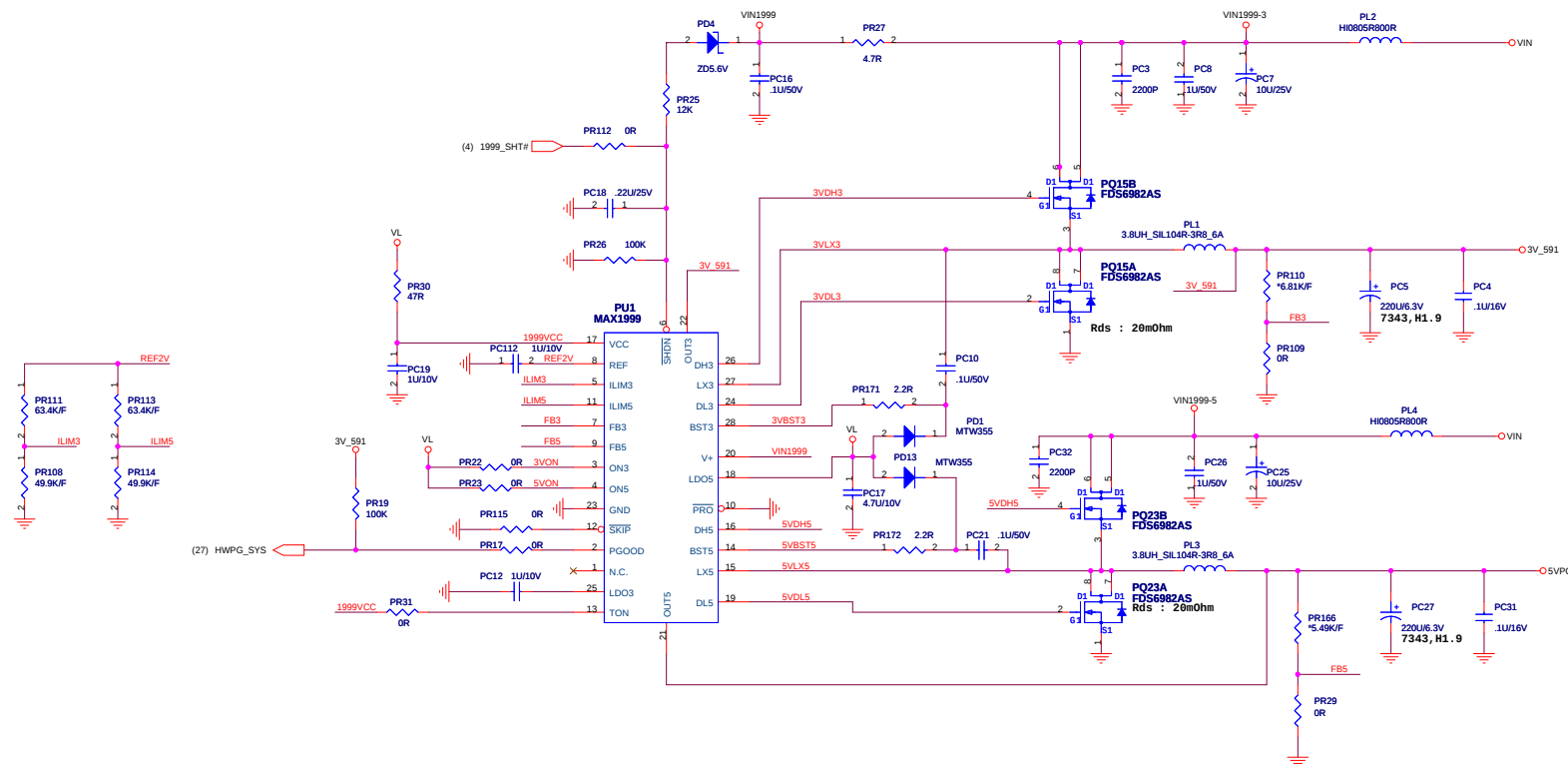


PCI EPM Buffer





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1ST_BATT_CONN

