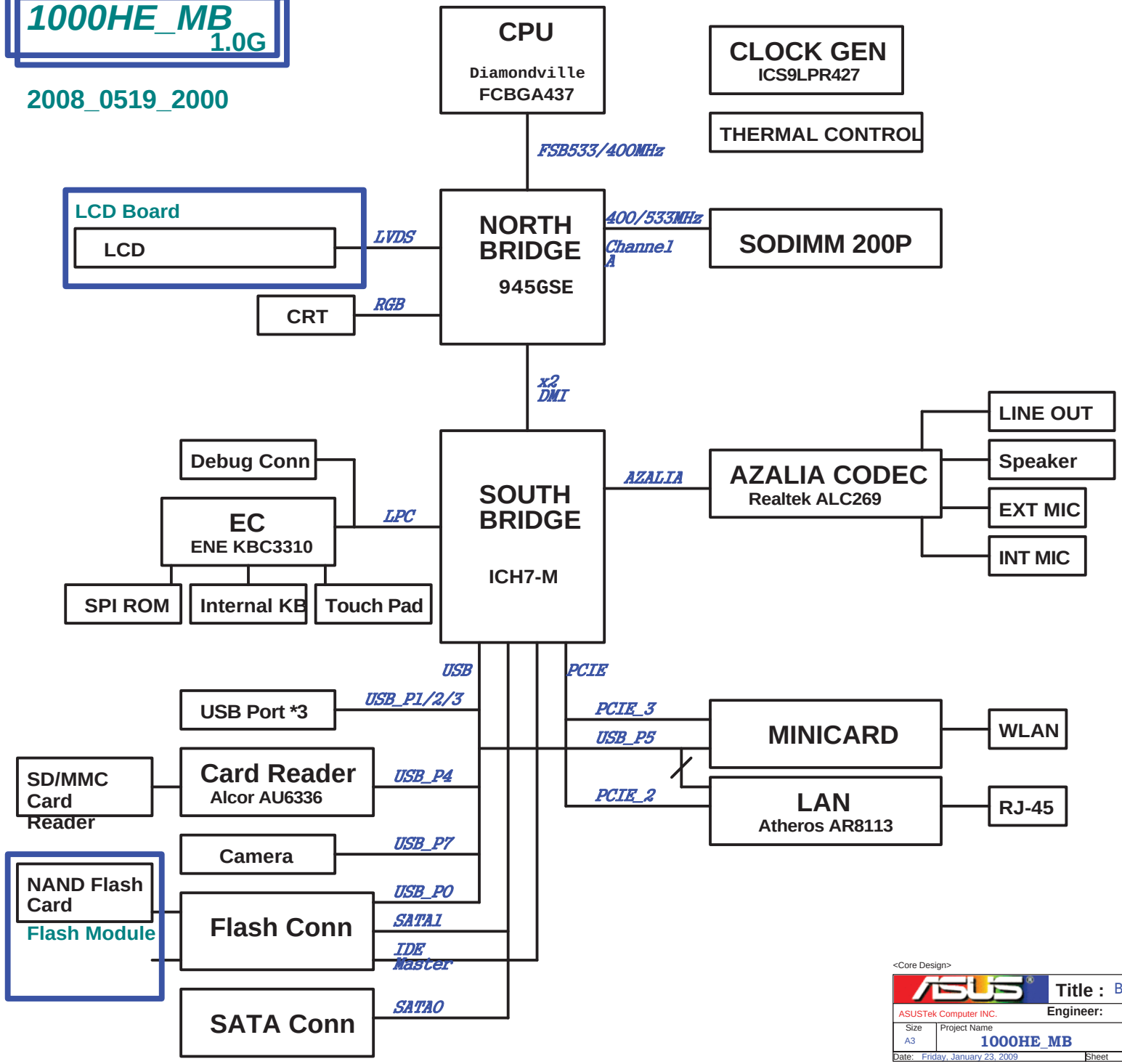
1000HE_MB 1.0G

2008_0519_2000

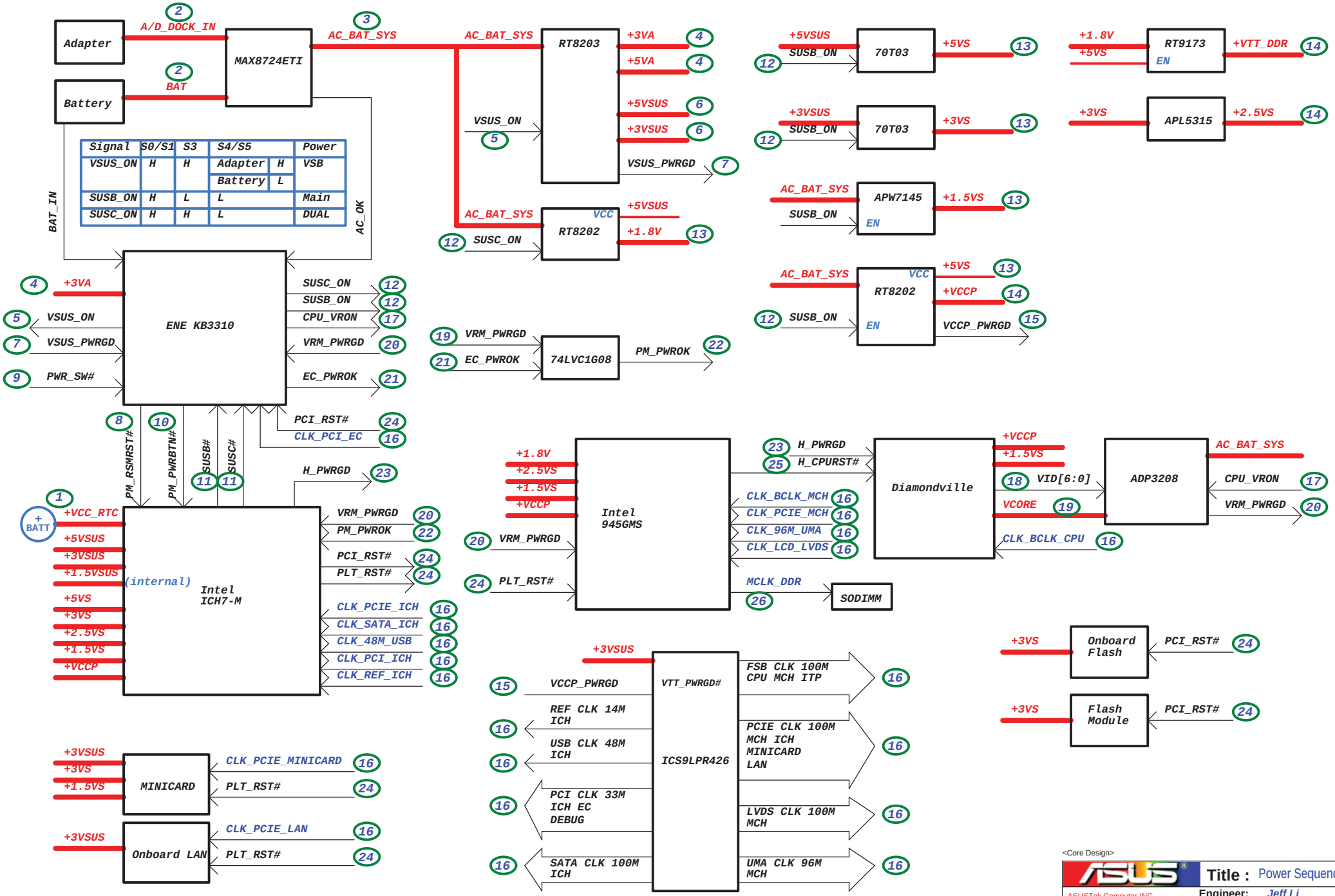


<Core Design>

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Echo_Huang	
Size: A3	Project Name: 1000HE_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 1 of 47	

<Core Design>

ASUSTek Computer INC.	Title : History	
	Engineer: *KingCa_Jin*	
Size: A3	Project Name: **1000HE_MB**	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 2 of 47	



<Core Design>

Title : Power Sequence

ASUSTek Computer INC.

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 3 of 47

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SCI#	EXT_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configureation
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSAVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Core Design>

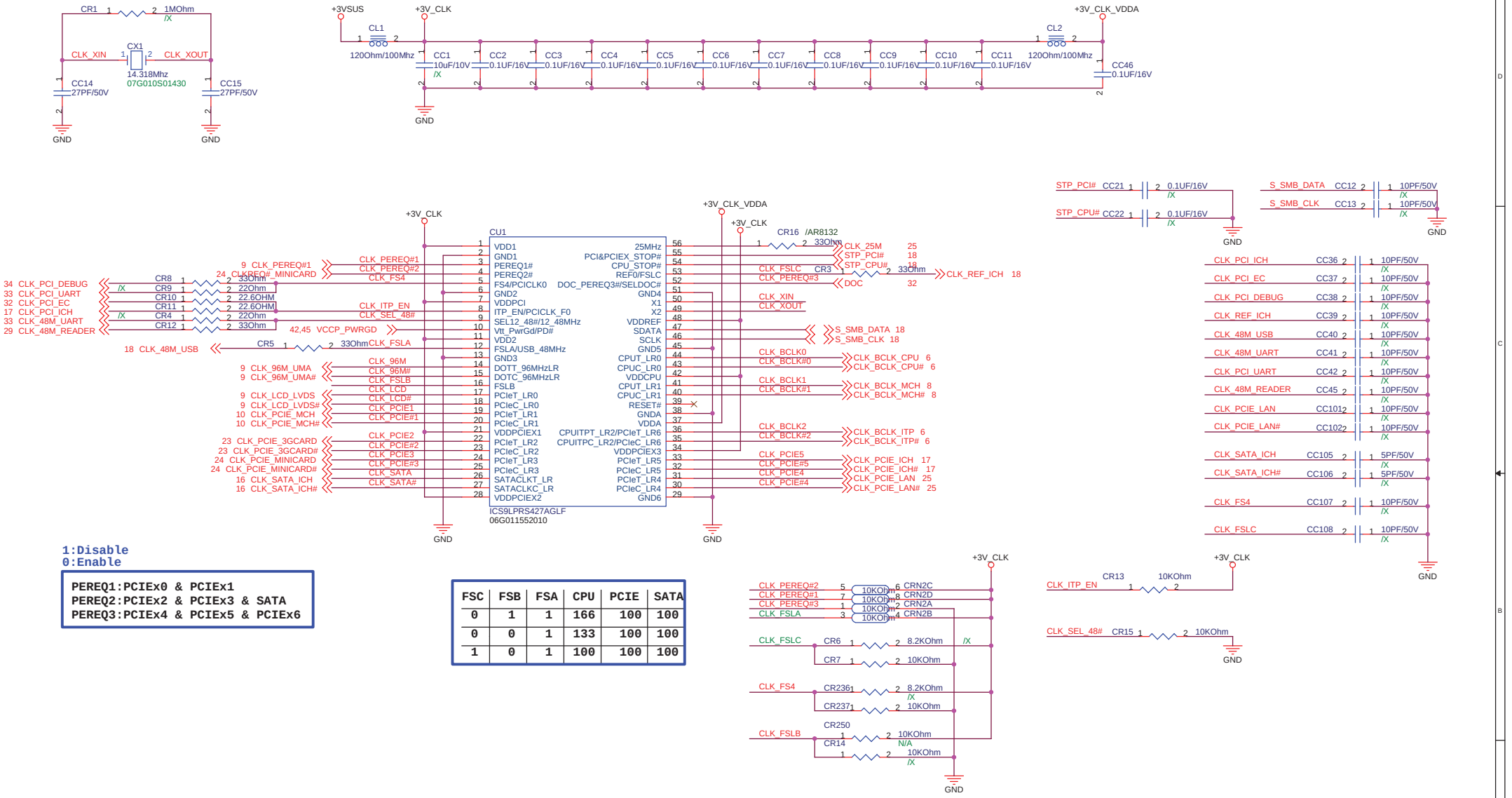
ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 4 of 47



1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	1	1	166	100	100
0	0	1	133	100	100
1	0	1	100	100	100

<Core Design>

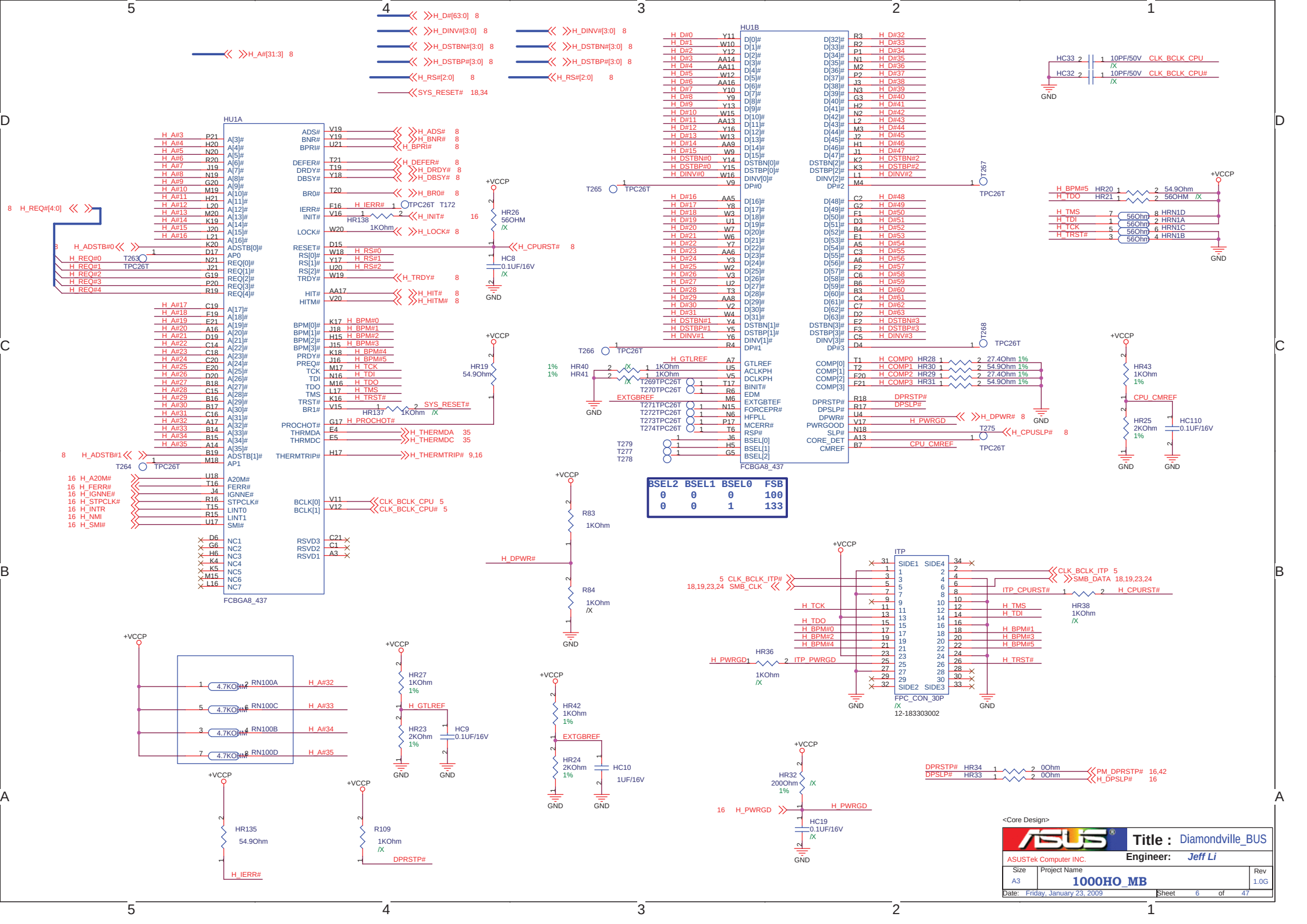
ASUSTek Computer INC.

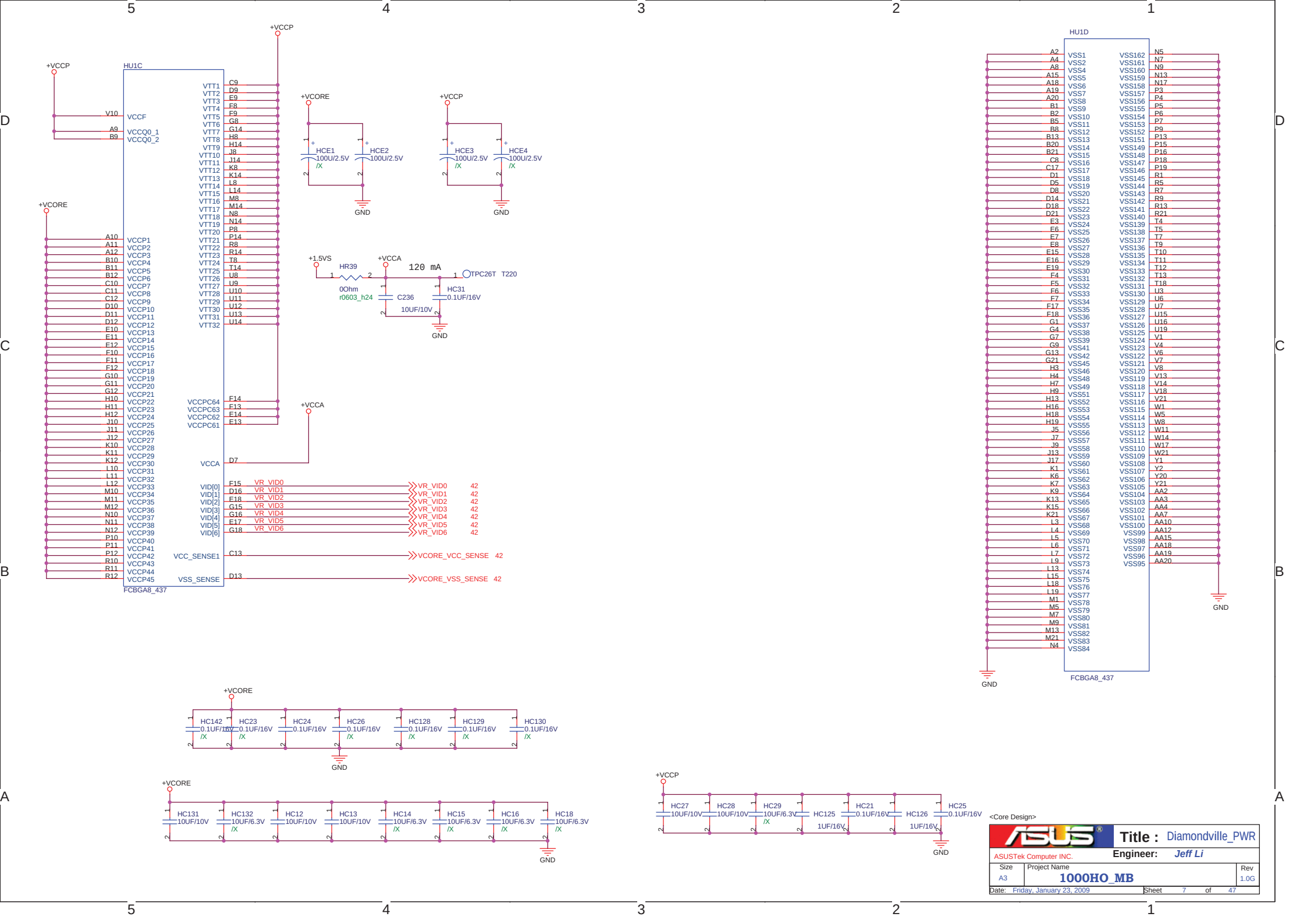
Title : Clock Gen_ICS9LPRS427

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 5 of 47

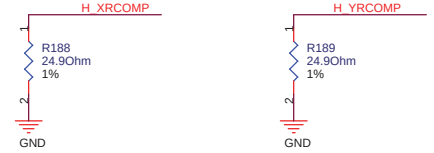

HU1A
HU1B
FCBGA8_437
FCBGA8_437
H_A#[31:3] 8
H_D#[63:0] 8
H_DINV#[3:0] 8
H_DSTBN#[3:0] 8
H_DSTBP#[3:0] 8
H_RS#[2:0] 8
SYS_RESET# 18,34
H_REQ#[4:0] 8
H_ADSTB#0 8
H_ADSTB#1 8
H_A20M# 16
H_FERR# 16
H_IGNNE# 16
H_STPCLK# 16
H_INTR 16
H_NMI 16
H_SMI# 16
H_ADS# 8
H_BNR# 8
H_BPRI# 8
H_DEFER# 8
H_DRDY# 8
H_DBSY# 8
H_BR0# 8
H_IERR# 1
H_INIT# 16
H_LOCK# 8
H_CPURST# 8
H_TRDY# 8
H_HIT# 8
H_HITM# 8
H_BPM#0
H_BPM#1
H_BPM#2
H_BPM#3
H_BPM#4
H_BPM#5
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#
H_PROCHOT# 35
H_THERMDA 35
H_THERMDC 35
H_THERMTRIP# 9,16
CLK_BCLK_CPU 5
CLK_BCLK_CPU# 5
H_GTLREF
EXTGBREF
H_PWRGD
H_DPWR# 8
H_CPUSLP# 8
CPU_CMREF
DPRSTP#
DPSLP#
PM_DPRSTP# 16,42
H_DPSLP# 16
BSEL2 BSEL1 BSEL0 FSB
0 0 0 100
0 0 1 133
ITP
FPC_CON_30P
12-183303002
CLK_BCLK_ITP 5
SMB_DATA 18,19,23,24
CLK_BCLK_ITP# 5
SMB_CLK 18,19,23,24
ITP_CPURST#
ITP_PWRGD
+VCCP
GND
HC33 10PF/50V CLK_BCLK_CPU /X
HC32 10PF/50V CLK_BCLK_CPU# /X
HR26 56OHM /X
HC8 0.1UF/16V /X
HR19 54.9Ohm
HR137 1KOhm /X
HR138 1KOhm
HR40 1KOhm /X
HR41 1KOhm /X
HR83 1KOhm
HR84 1KOhm /X
HR36 1KOhm /X
HR38 1KOhm /X
HR42 1KOhm 1%
HR24 2KOhm 1%
HC10 1UF/16V
HR27 1KOhm 1%
HR23 2KOhm 1%
HC9 0.1UF/16V
HR32 200Ohm 1% /X
HC19 0.1UF/16V /X
HR135 54.9Ohm
R109 1KOhm /X
DPRSTP#
HR34 0Ohm
HR33 0Ohm
HR20 54.9Ohm
HR21 56OHM /X
HR43 1KOhm 1%
HR25 2KOhm 1%
HC110 0.1UF/16V
HR28 27.4Ohm 1%
HR29 27.4Ohm 1%
HR30 54.9Ohm 1%
HR31 54.9Ohm 1%
HRN1D 56Ohm
HRN1A 56Ohm
HRN1C 56Ohm
HRN1B 56Ohm
RN100A 4.7KOHM
RN100C 4.7KOHM
RN100B 4.7KOHM
RN100D 4.7KOHM
T263 TPC26T
T264 TPC26T
T265 TPC26T
T266 TPC26T
T267 TPC26T
T268 TPC26T
T269TPC26T
T270TPC26T
T271TPC26T
T272TPC26T
T273TPC26T
T274TPC26T
T275 TPC26T
T279
T277
T278
<Core Design>
ASUSTek Computer INC.
Title : Diamondville_BUS
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 6 of 47


HU1C
FCBGA8_437
+VCCP
+VCORE
+VCCA
+1.5VS
GND
HCE1 100U/2.5V /X
HCE2 100U/2.5V /X
HCE3 100U/2.5V /X
HCE4 100U/2.5V /X
HR39 0Ohm r0603_h24
C236 10UF/10V
HC31 0.1UF/16V
120 mA
TPC26T T220
VCCF
VCCQ0_1
VCCQ0_2
VCCP1 VCCP2 VCCP3 VCCP4 VCCP5 VCCP6 VCCP7 VCCP8 VCCP9 VCCP10 VCCP11 VCCP12 VCCP13 VCCP14 VCCP15 VCCP16 VCCP17 VCCP18 VCCP19 VCCP20 VCCP21 VCCP22 VCCP23 VCCP24 VCCP25 VCCP26 VCCP27 VCCP28 VCCP29 VCCP30 VCCP31 VCCP32 VCCP33 VCCP34 VCCP35 VCCP36 VCCP37 VCCP38 VCCP39 VCCP40 VCCP41 VCCP42 VCCP43 VCCP44 VCCP45
VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9 VTT10 VTT11 VTT12 VTT13 VTT14 VTT15 VTT16 VTT17 VTT18 VTT19 VTT20 VTT21 VTT22 VTT23 VTT24 VTT25 VTT26 VTT27 VTT28 VTT29 VTT30 VTT31 VTT32
VCCPC64 VCCPC63 VCCPC62 VCCPC61
VCCA
VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]
VR_VID0 VR_VID1 VR_VID2 VR_VID3 VR_VID4 VR_VID5 VR_VID6
VCC_SENSE1
VSS_SENSE
VCORE_VCC_SENSE
VCORE_VSS_SENSE
HU1D
HC142 HC23 HC24 HC26 HC128 HC129 HC130 0.1UF/16V /X
HC131 HC132 HC12 HC13 HC14 HC15 HC16 HC18 10UF/10V 10UF/6.3V /X
HC27 HC28 10UF/10V
HC29 10UF/6.3V /X
HC125 1UF/16V
HC21 HC126 0.1UF/16V
HC25 0.1UF/16V
<Core Design>
Title : Diamondville_PWR
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 7 of 47

Power : +VCCP

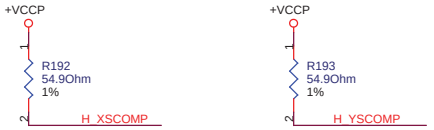
RCOMP

For Calibrating the FSB I/O Buffer



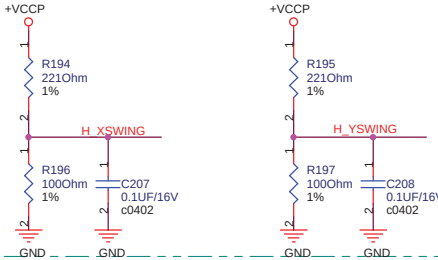
SCOMP

For Slew Rate Compenssation on the FSB

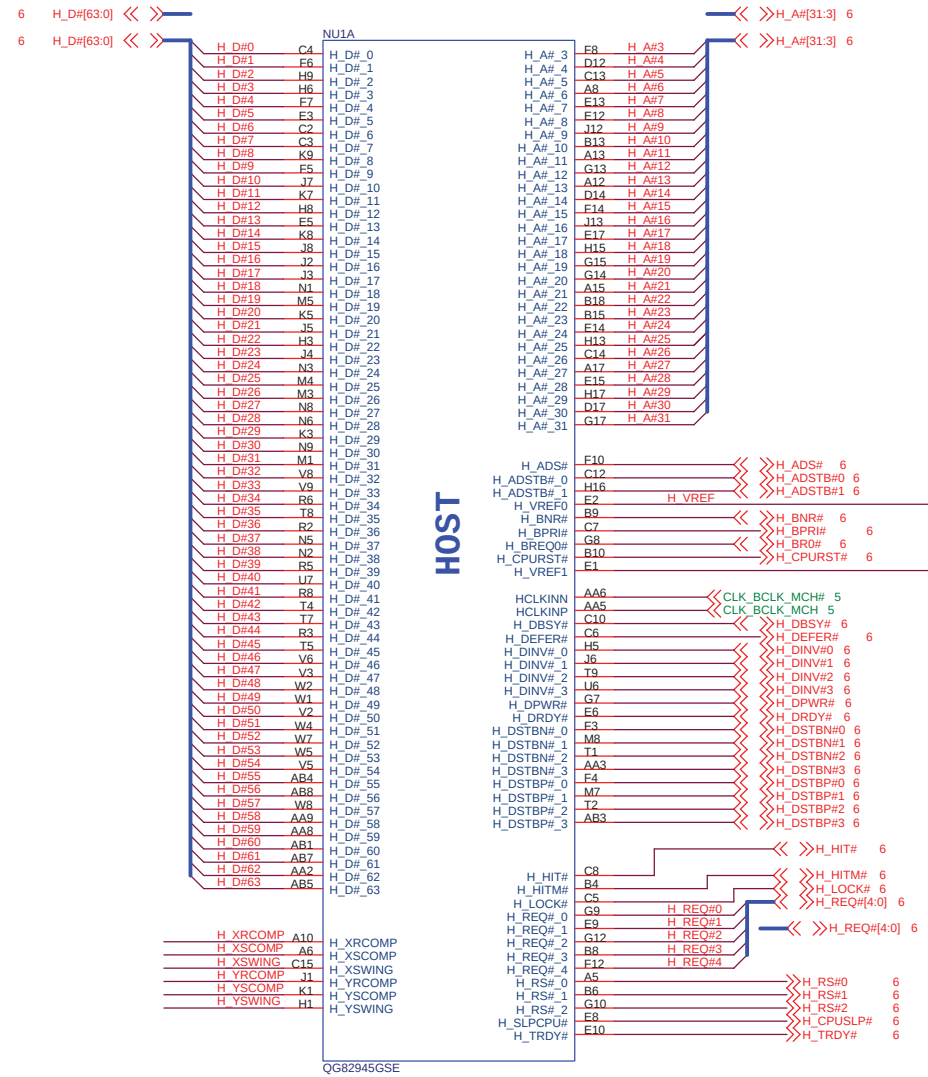


Voltage Swing

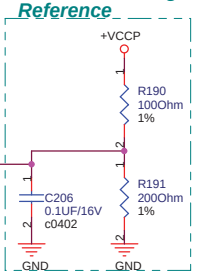
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing



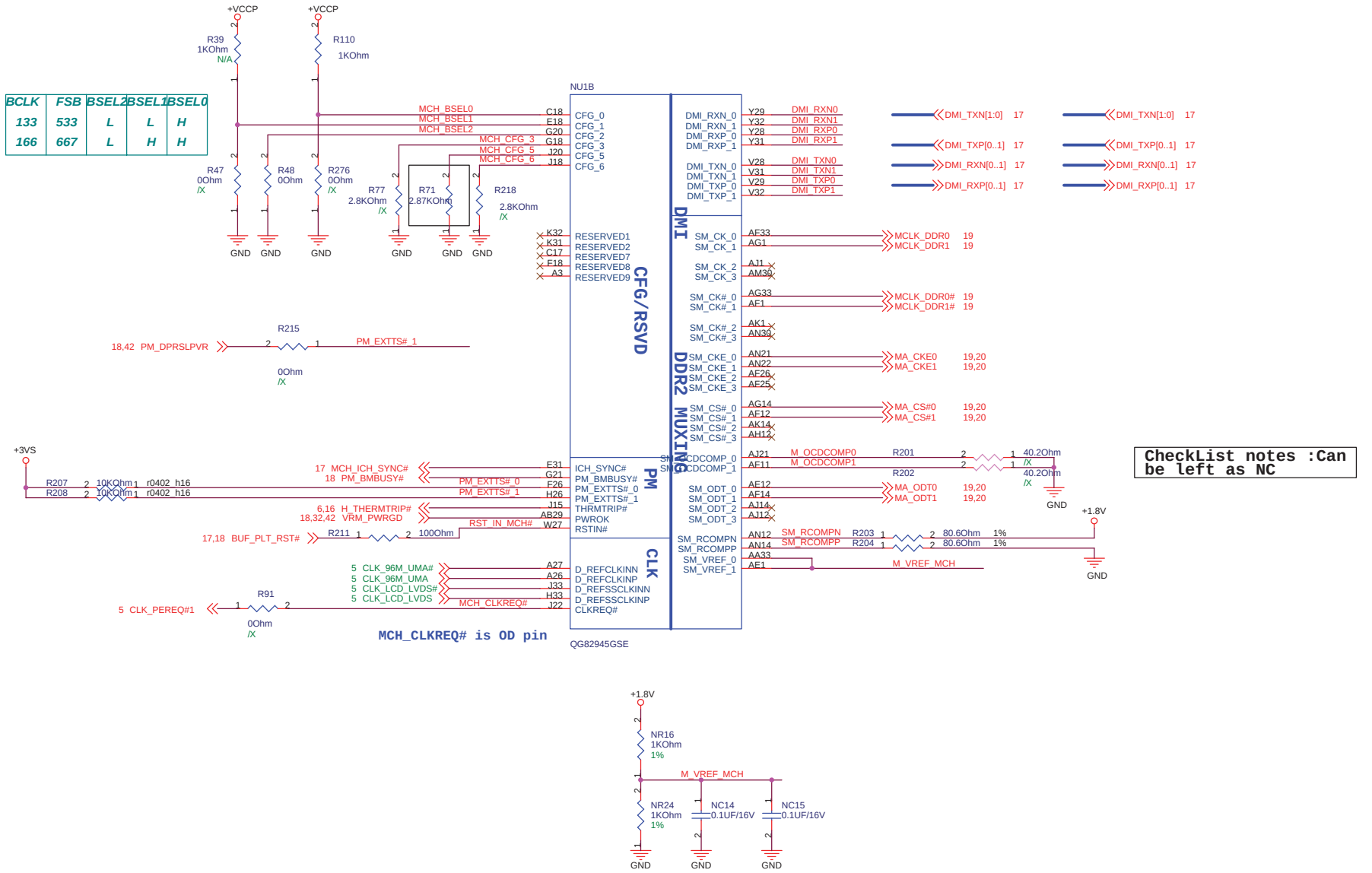
AGTL+ I/O Voltage Reference



Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

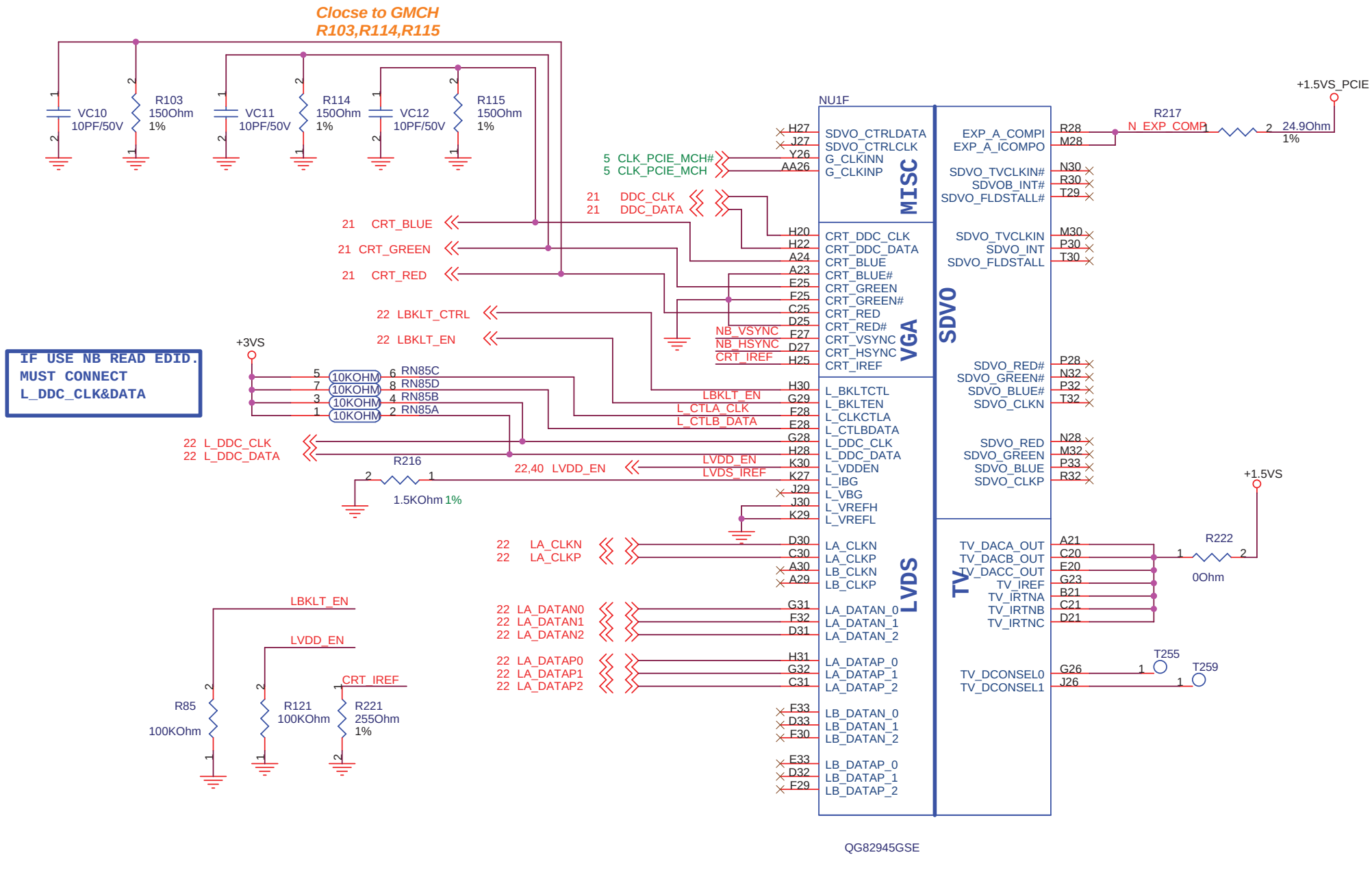
<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(HOST)	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 8 of 47	



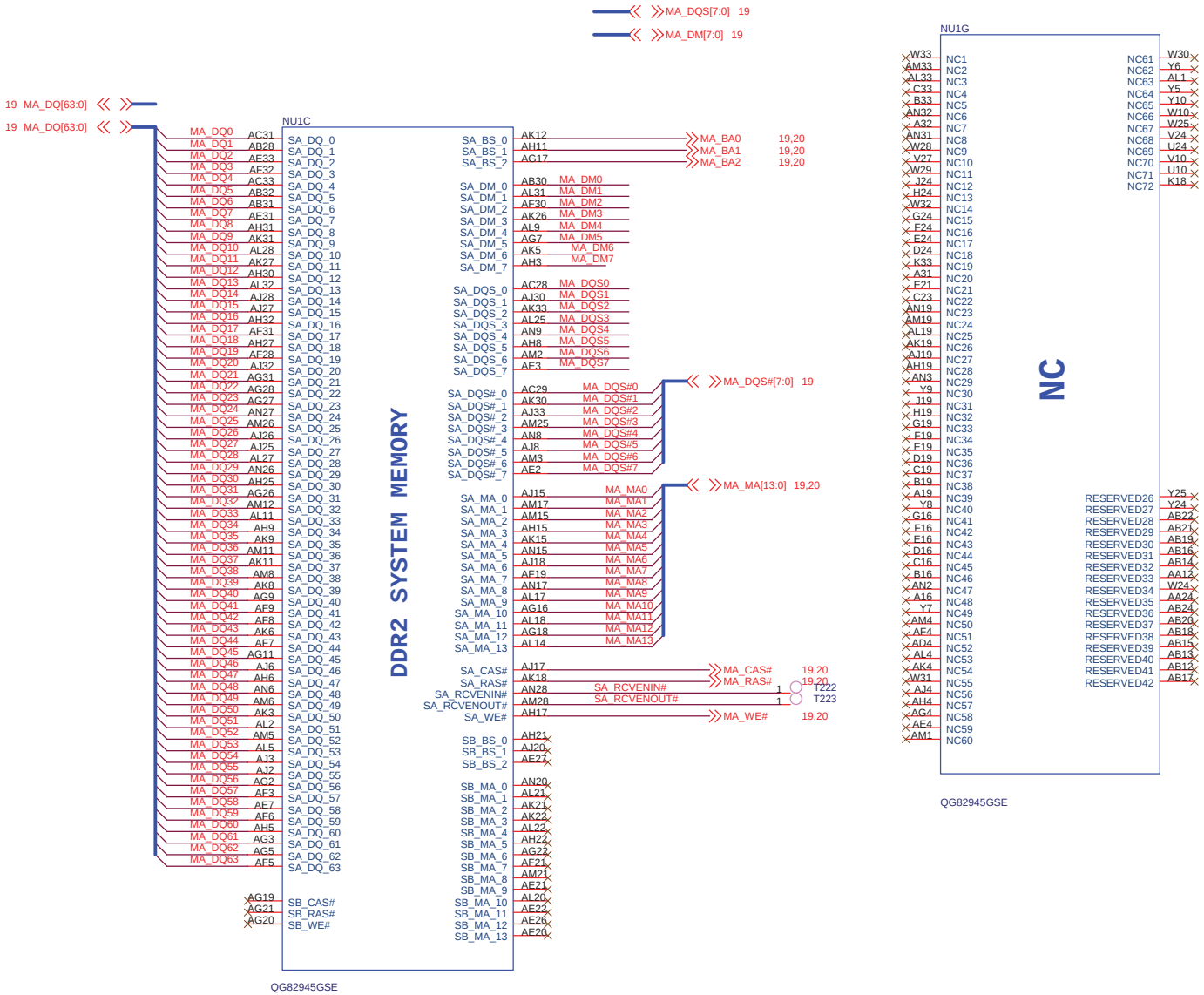
<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(DMI & CFG)	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 9 of 47	



<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(GRAPHIC)	
	Engineer: Jeff Li	
Size: A4	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 10 of 47	



<Core Design>

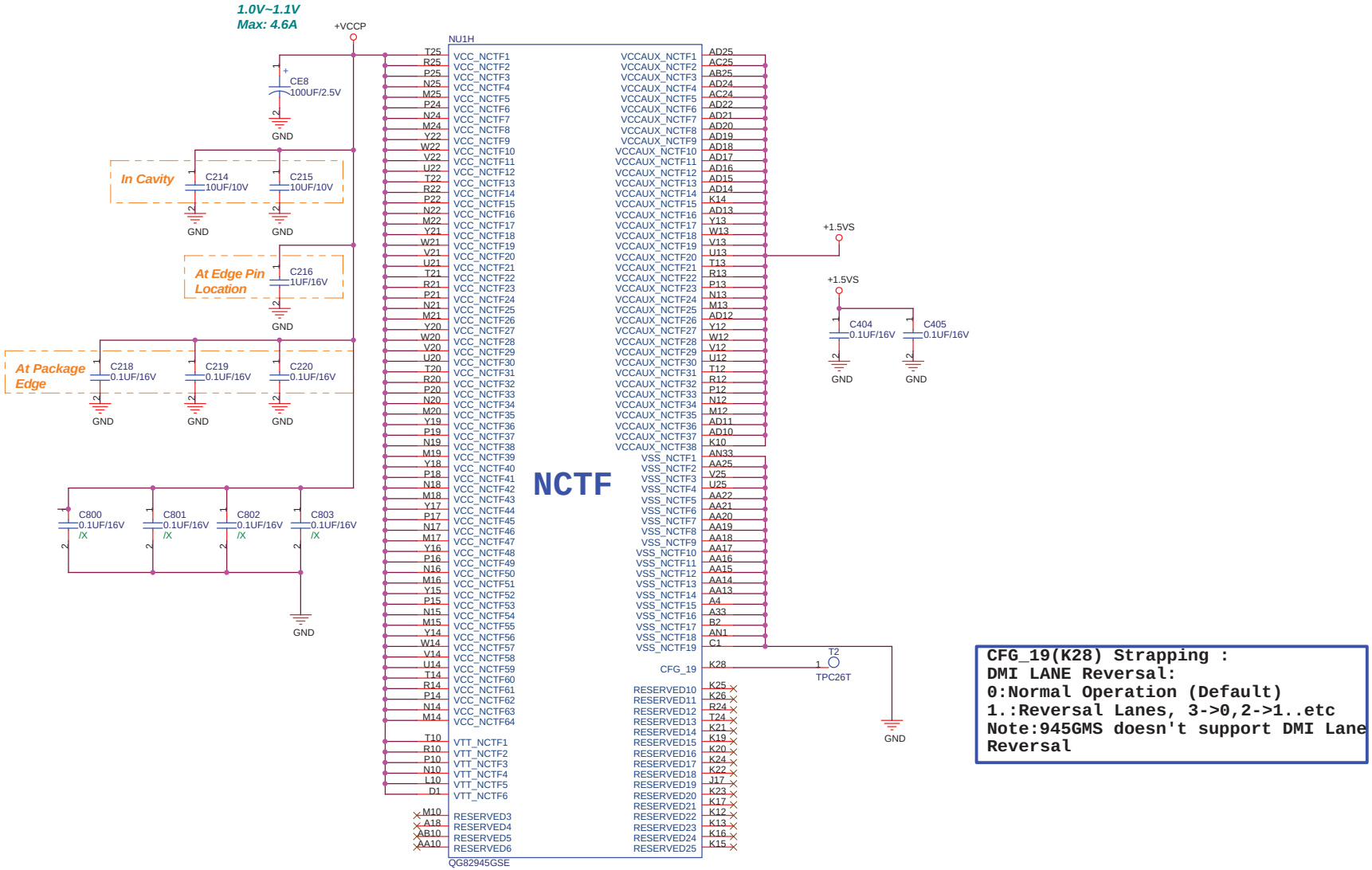
ASUSTeK COMPUTER INC.

Title : NB-945GMS(DDR2)

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 11 of 47



<Core Design>

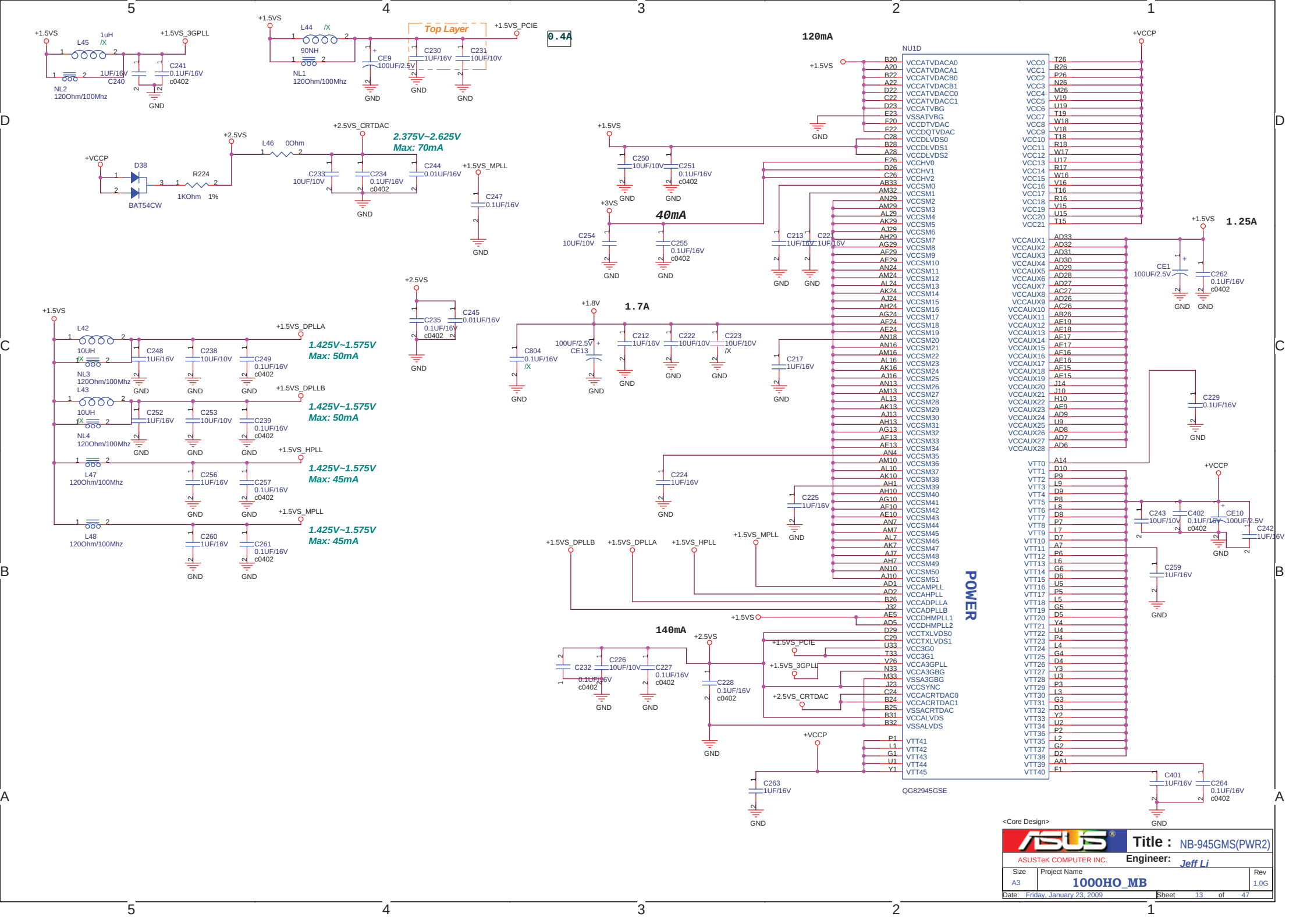
Title : NB-945GMs(PWR)

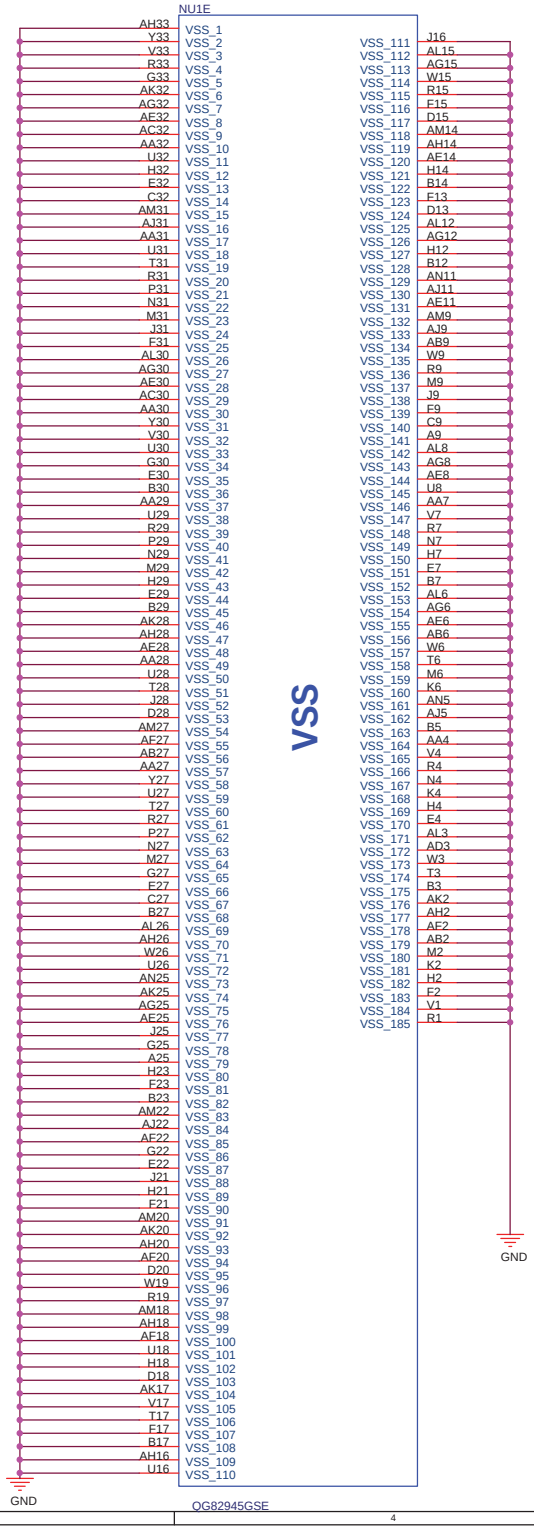
ASUSTeK COMPUTER INC.

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

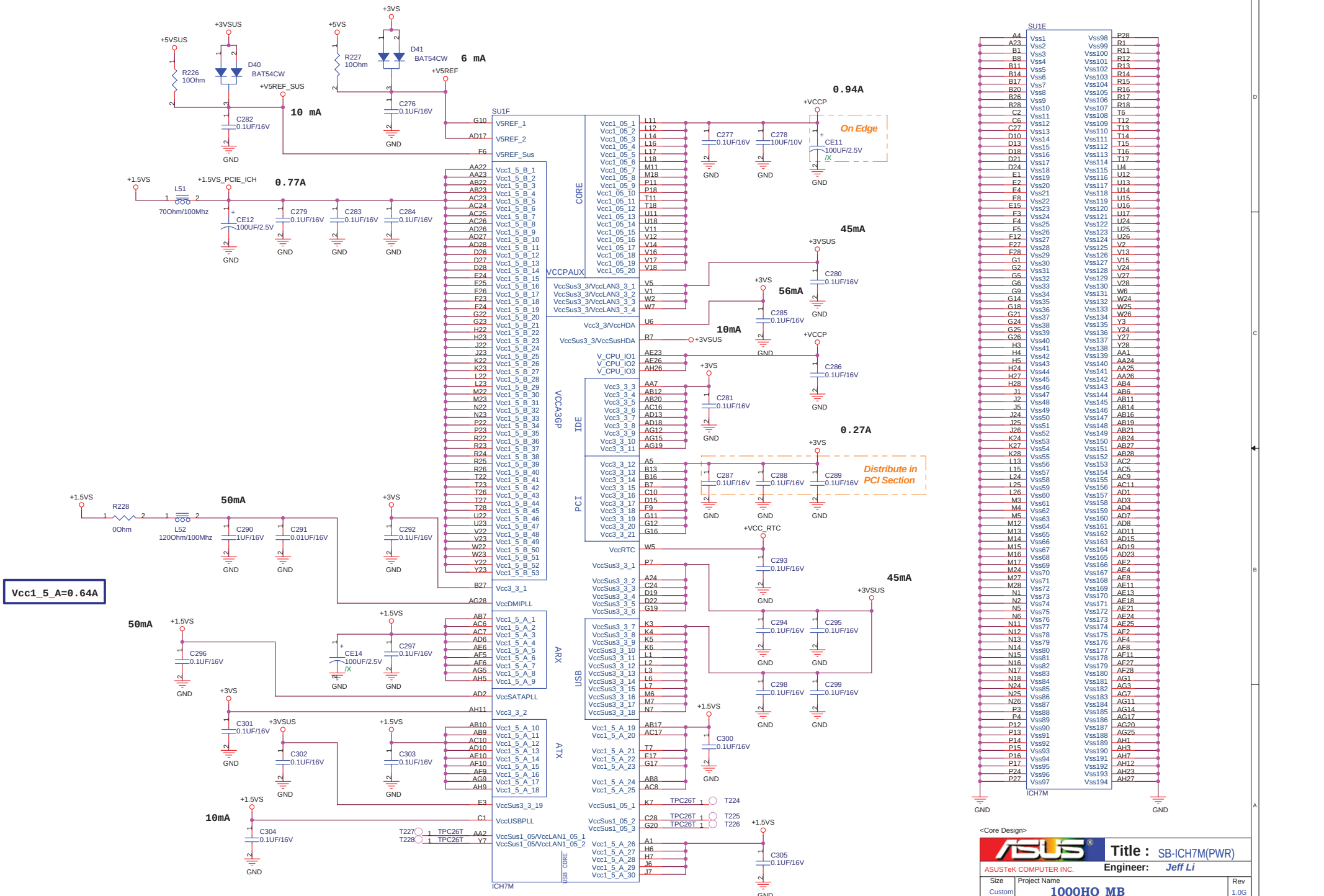
Date: Friday, January 23, 2009 Sheet 12 of 47

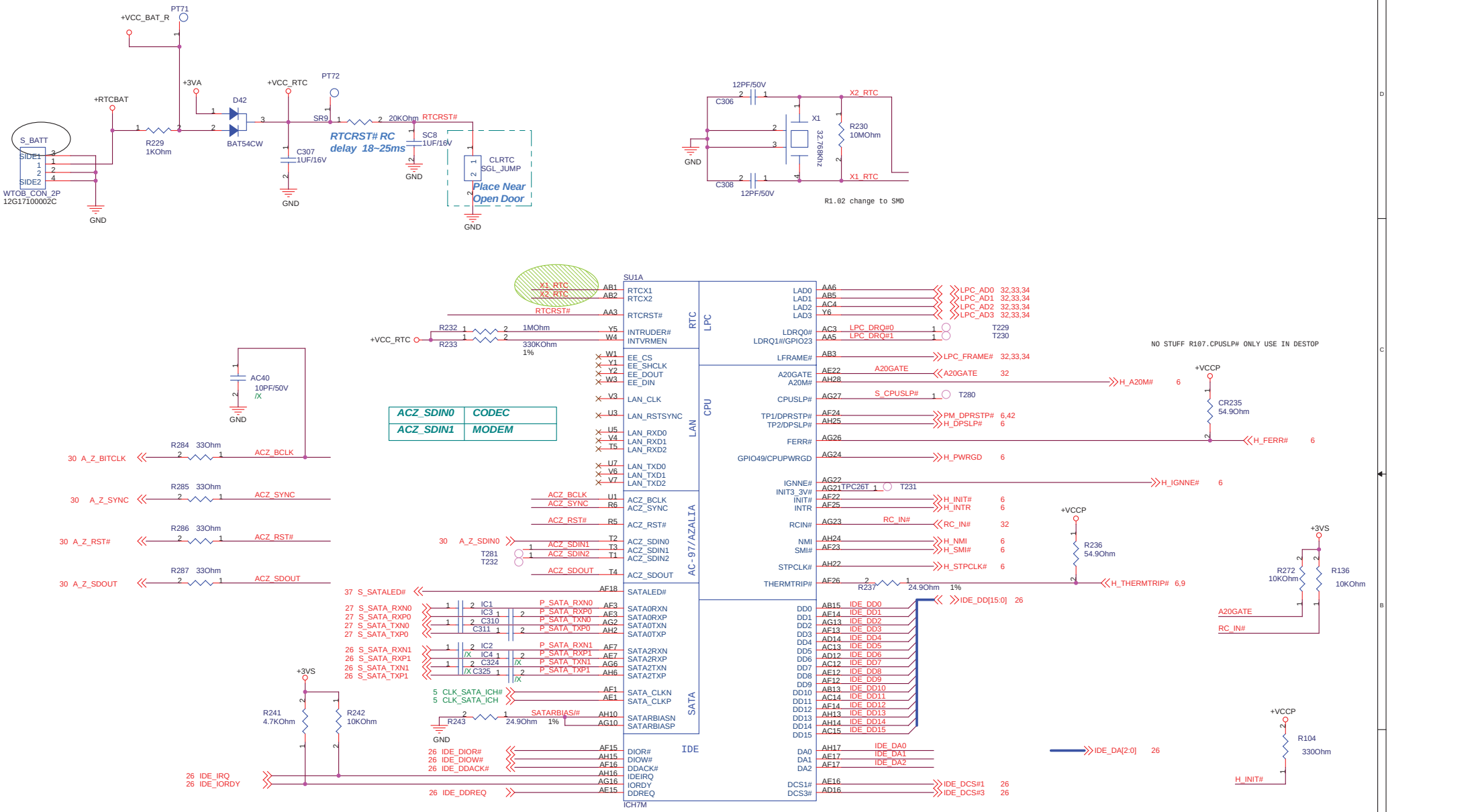

Top Layer
0.4A
120mA
1.25A
1.7A
40mA
140mA
NU1D
POWER
QG82945GSE
+1.5VS
+1.5VS_3GPLL
+1.5VS_PCIE
+2.5VS
+2.5VS_CRTDAC
+3VS
+VCCP
+1.8V
+1.5VS_MPLL
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
GND
L45 1uH /X
L44 /X
90NH
NL1 120Ohm/100Mhz
NL2 120Ohm/100Mhz
L46 0Ohm
D38
BAT54CW
R224 1KOhm 1%
L42 10UH /X
L43 10UH /X
L47 120Ohm/100Mhz
L48 120Ohm/100Mhz
NL3 120Ohm/100Mhz
NL4 120Ohm/100Mhz
2.375V~2.625V
Max: 70mA
1.425V~1.575V
Max: 50mA
1.425V~1.575V
Max: 50mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
<Core Design>
Title : NB-945GMS(PWR2)
ASUSTeK COMPUTER INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 13 of 47



<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945PMS(GND)		
	Engineer: Jeff Li		
Size: A3	Project Name: 1000HO_MB		Rev: 1.0G
Date: Friday, January 23, 2009		Sheet 14 of 47	


+3VS
+3VSUS
+5VS
+5VSUS
+V5REF
+V5REF_SUS
D40
BAT54CW
D41
BAT54CW
6 mA
10 mA
R226
10Ohm
R227
10Ohm
C276
0.1UF/16V
C282
0.1UF/16V
GND
SU1F
V5REF_1
V5REF_2
V5REF_Sus
+1.5VS
+1.5VS_PCIE_ICH
0.77A
L51
70Ohm/100Mhz
CE12
100UF/2.5V
C279
0.1UF/16V
C283
0.1UF/16V
C284
0.1UF/16V
CORE
VCCPAUX
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
VCCA3GP
IDE
PCI
VccRTC
VccSus3_3_1
USB
ARX
ATX
VccSATAPLL
Vcc3_3_2
VccUSBPLL
VccSus3_3_19
VccSus1_05_1
VccSus1_05_2
VccSus1_05_3
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
Vcc1_5_A_26
Vcc1_5_A_27
Vcc1_5_A_28
Vcc1_5_A_29
Vcc1_5_A_30
ICH7M
0.94A
On Edge
CE11
100UF/2.5V
C277
0.1UF/16V
C278
10UF/10V
45mA
56mA
C280
0.1UF/16V
C285
0.1UF/16V
10mA
C286
0.1UF/16V
C281
0.1UF/16V
0.27A
Distribute in PCI Section
C287
0.1UF/16V
C288
0.1UF/16V
C289
0.1UF/16V
+VCC_RTC
C293
0.1UF/16V
45mA
C294
0.1UF/16V
C295
0.1UF/16V
C298
0.1UF/16V
C299
0.1UF/16V
C300
0.1UF/16V
C305
0.1UF/16V
TPC26T
T224
T225
T226
T227
T228
R228
0Ohm
L52
120Ohm/100Mhz
50mA
C290
1UF/16V
C291
0.01UF/16V
C292
0.1UF/16V
Vcc1_5_A=0.64A
C296
0.1UF/16V
CE14
100UF/2.5V
C297
0.1UF/16V
C301
0.1UF/16V
C302
0.1UF/16V
C303
0.1UF/16V
10mA
C304
0.1UF/16V
SU1E
ICH7M
<Core Design>
ASUSTeK COMPUTER INC.
Title : SB-ICH7M(PWR)
Engineer: Jeff Li
Size Custom
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 15 of 47



<Core Design>

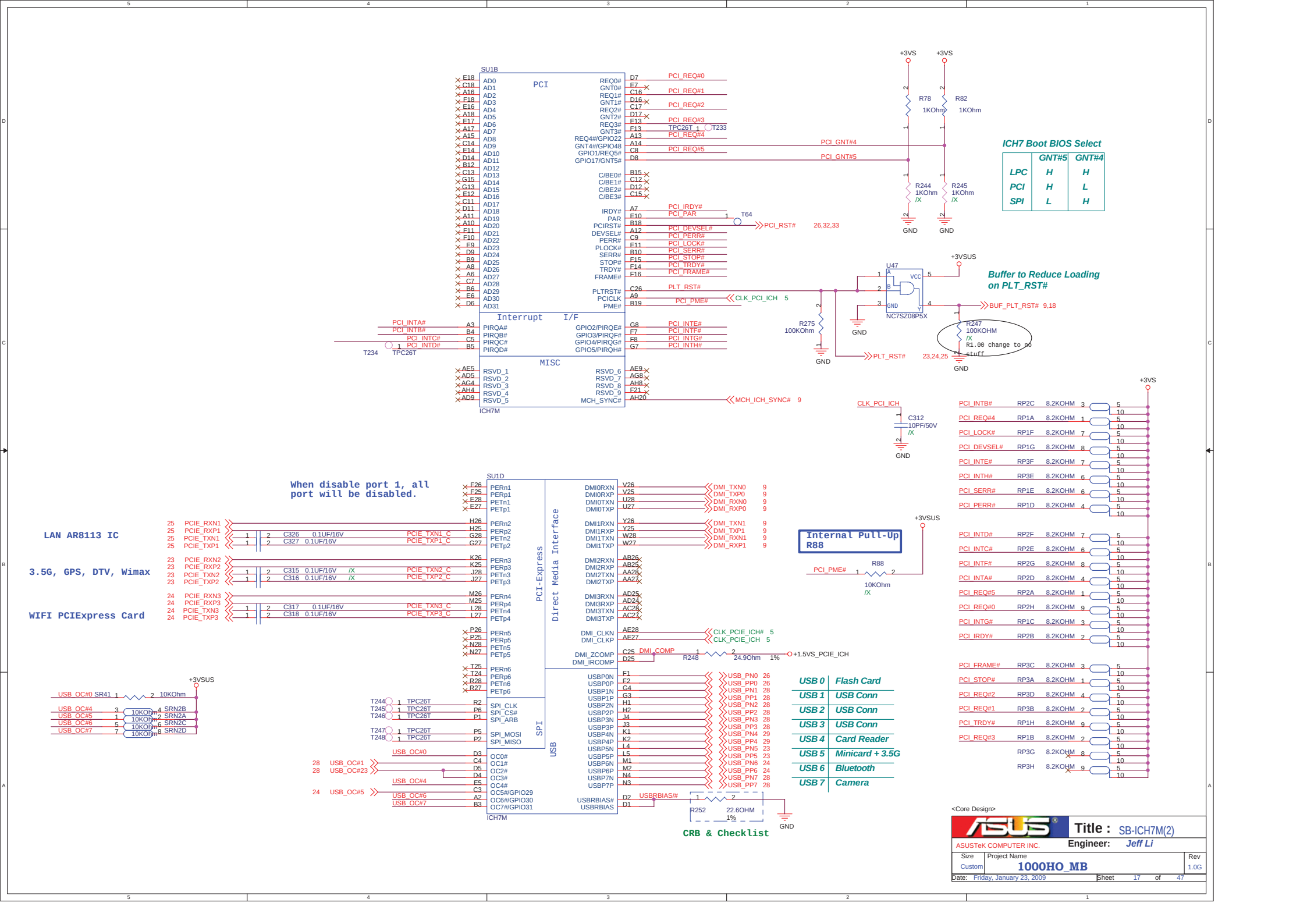
ASUSTeK COMPUTER INC.

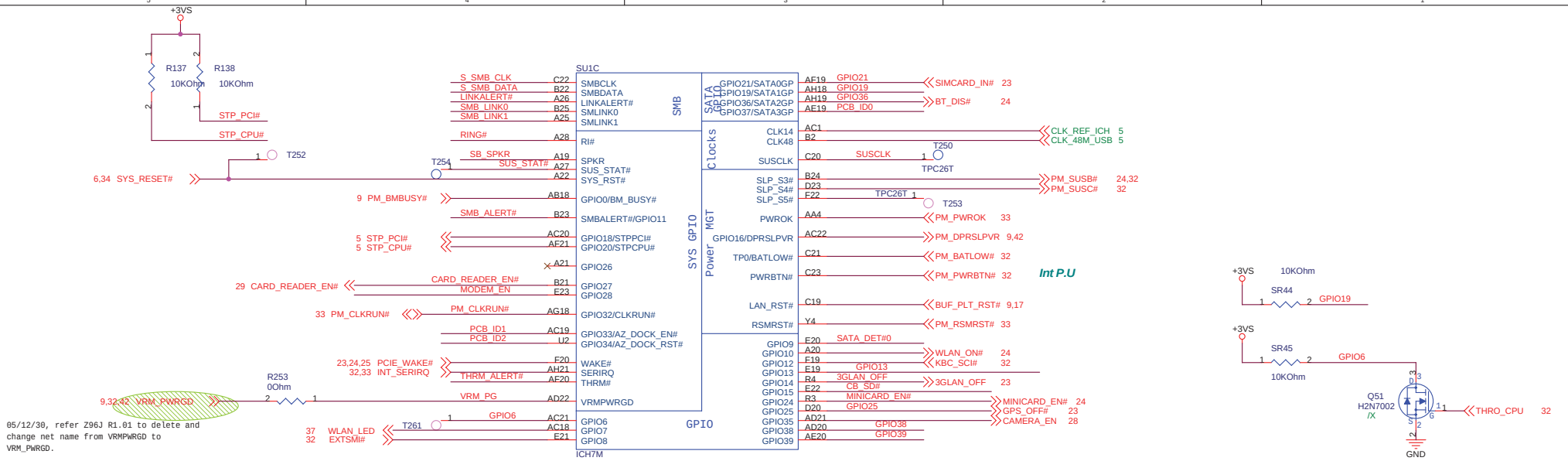
Title : SB-ICH7-M(1)

Engineer: Jeff Li

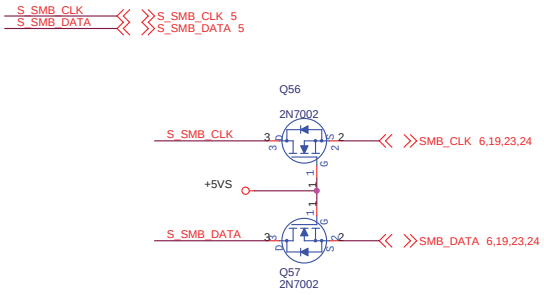
Size	Project Name	Rev
Custom	1000HO_MB	1.0G

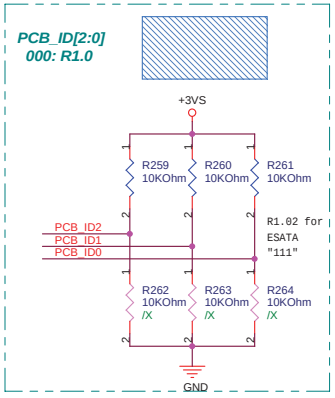
Date: Friday, January 23, 2009 Sheet 16 of 47


SU1B
PCI
Interrupt I/F
MISC
ICH7M
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_REQ#5
PCI_GNT#4
PCI_GNT#5
PCI_IRDY#
PCI_PAR
PCI_RST#
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
PLT_RST#
CLK_PCI_ICH
PCI_PME#
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_INTE#
PCI_INTF#
PCI_INTG#
PCI_INTH#
MCH_ICH_SYNC#
+3VS
+3VSUS
GND
R78 1KOhm
R82 1KOhm
R244 1KOhm /X
R245 1KOhm /X
R275 100KOhm
R247 100KOHM /X
R1.00 change to no stuff
U47 NC7SZ08P5X
BUF_PLT_RST# 9,18
ICH7 Boot BIOS Select
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
When disable port 1, all port will be disabled.
LAN AR8113 IC
3.5G, GPS, DTV, Wimax
WIFI PCIExpress Card
PCI-Express
Direct Media Interface
SPI
USB
C326 0.1UF/16V
C327 0.1UF/16V
C315 0.1UF/16V /X
C316 0.1UF/16V /X
C317 0.1UF/16V
C318 0.1UF/16V
PCIE_TXN1_C
PCIE_TXP1_C
PCIE_TXN2_C
PCIE_TXP2_C
PCIE_TXN3_C
PCIE_TXP3_C
C312 10PF/50V /X
Internal Pull-Up R88
R88 10KOhm /X
R248 24.9Ohm 1%
R252 22.6OHM 1%
CLK_PCIE_ICH#
CLK_PCIE_ICH
DMI_COMP
+1.5VS_PCIE_ICH
USB_OC#0 SR41 10KOhm
USB_OC#4 SRN2B
USB_OC#5 SRN2A
USB_OC#6 SRN2C
USB_OC#7 SRN2D
USB 0 Flash Card
USB 1 USB Conn
USB 2 USB Conn
USB 3 USB Conn
USB 4 Card Reader
USB 5 Minicard + 3.5G
USB 6 Bluetooth
USB 7 Camera
CRB & Checklist
RP2C 8.2KOHM
RP1A 8.2KOHM
RP1F 8.2KOHM
RP1G 8.2KOHM
RP3F 8.2KOHM
RP3E 8.2KOHM
RP1E 8.2KOHM
RP1D 8.2KOHM
RP2F 8.2KOHM
RP2E 8.2KOHM
RP2G 8.2KOHM
RP2D 8.2KOHM
RP2A 8.2KOHM
RP2H 8.2KOHM
RP1C 8.2KOHM
RP2B 8.2KOHM
RP3C 8.2KOHM
RP3A 8.2KOHM
RP3D 8.2KOHM
RP3B 8.2KOHM
RP1H 8.2KOHM
RP1B 8.2KOHM
RP3G 8.2KOHM
RP3H 8.2KOHM
<Core Design>
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Jeff Li
Size Custom
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 17 of 47

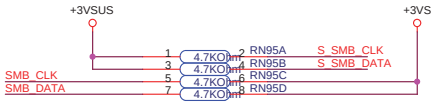


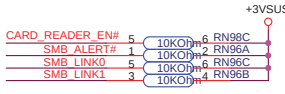
WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x

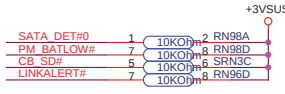


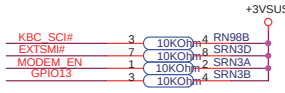


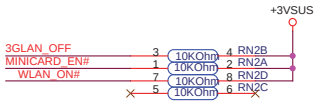
PCB_VID3 : PROJECT CODE

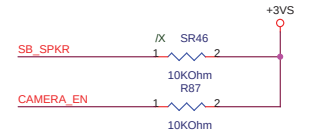


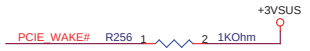


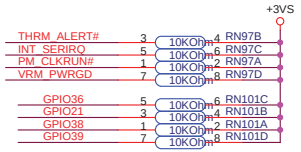












<Core Design>

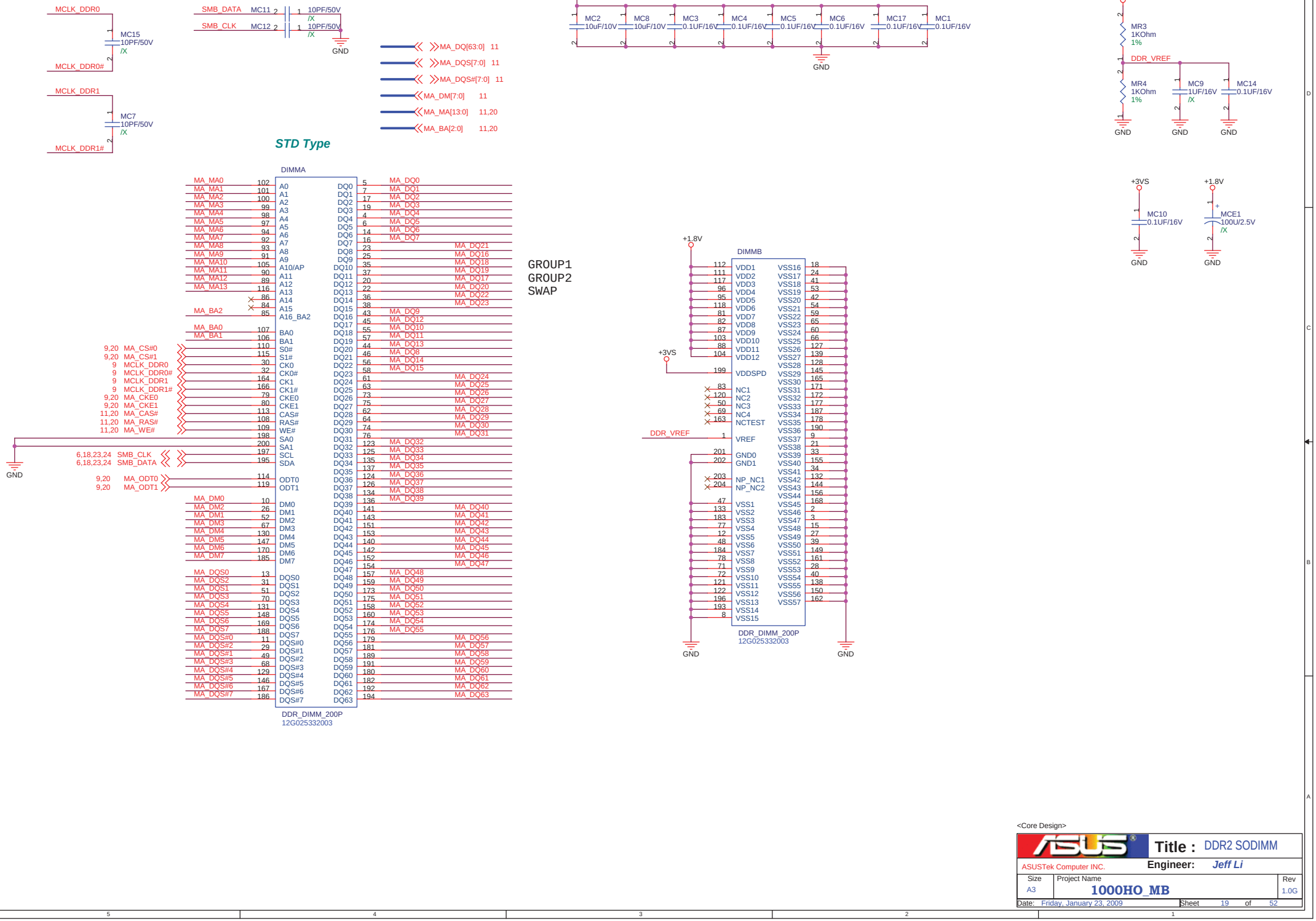
ASUSTeK COMPUTER INC

Title : SB-ICH7M(3)

Engineer: Jeff Li

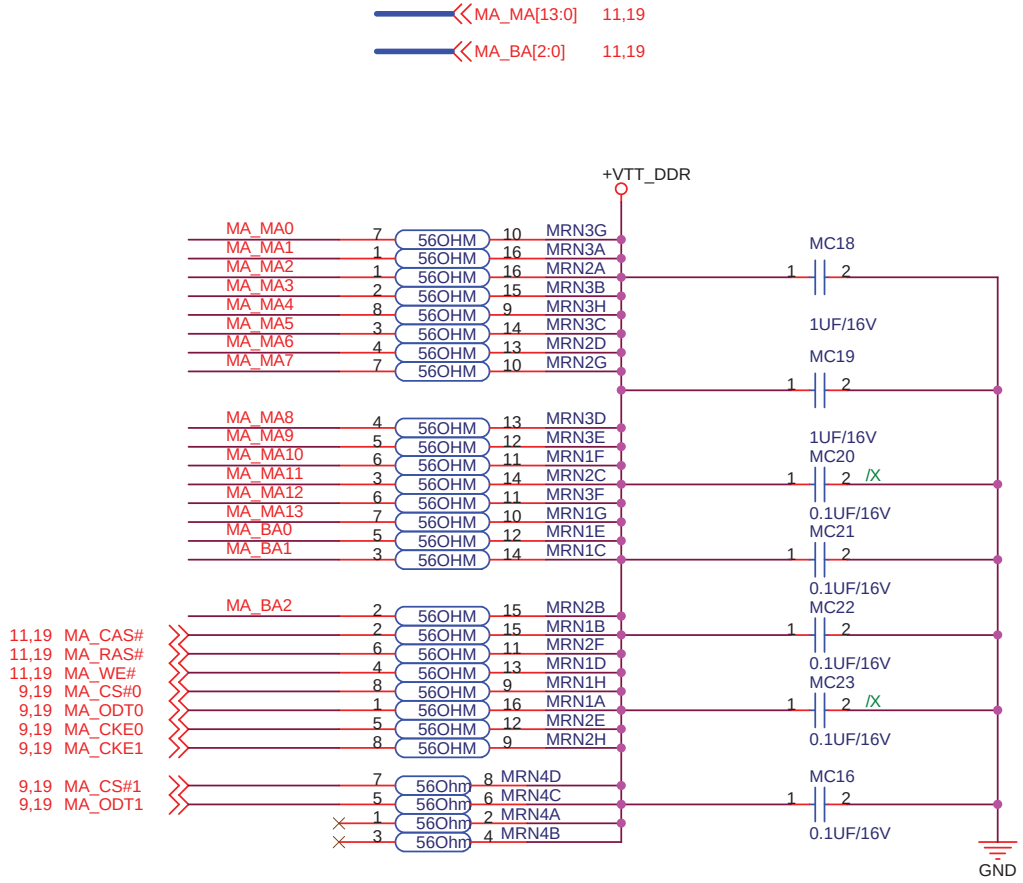
Size	Project Name	Rev
Custom	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 18 of 47



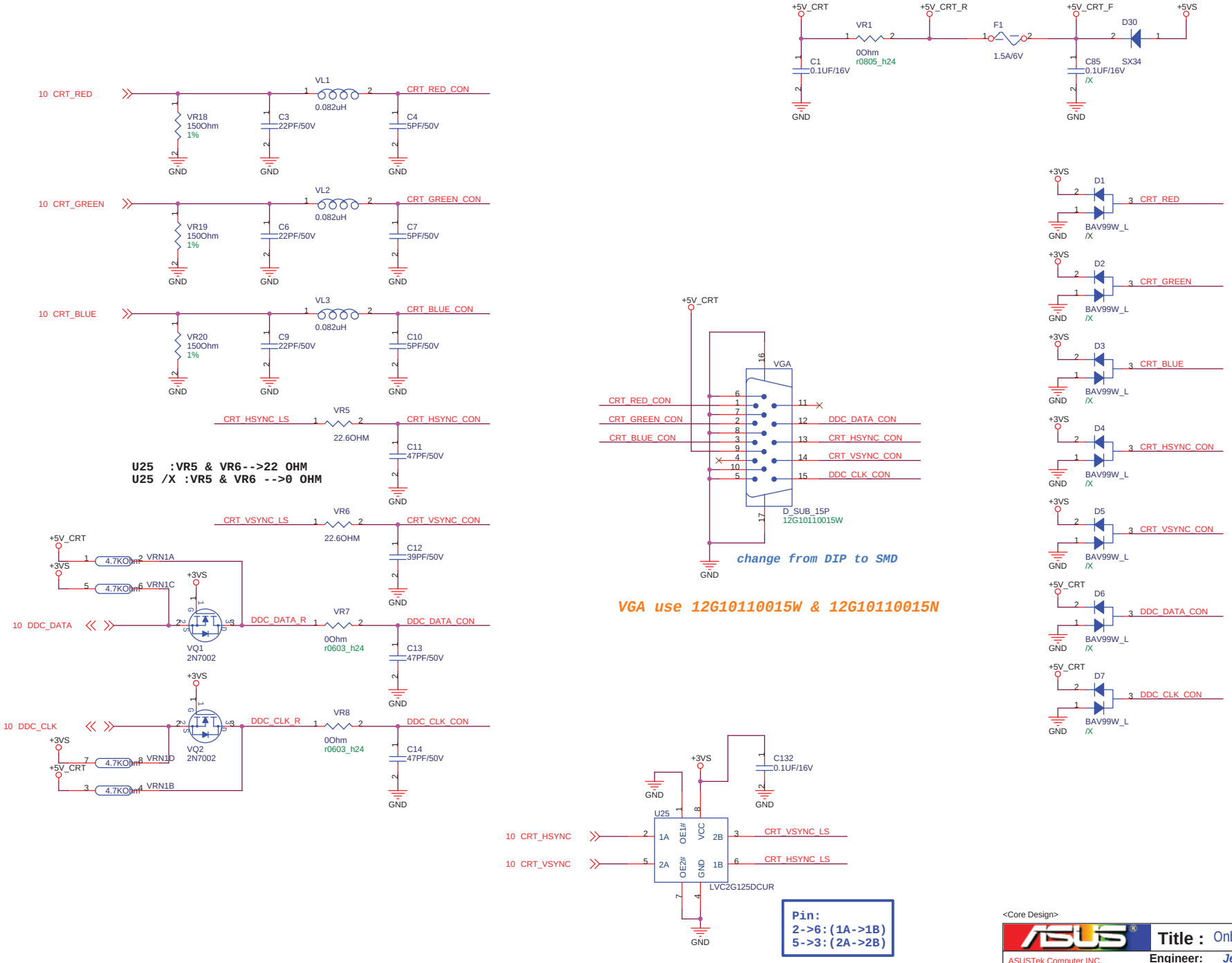
<Core Design>

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 19 of 52	



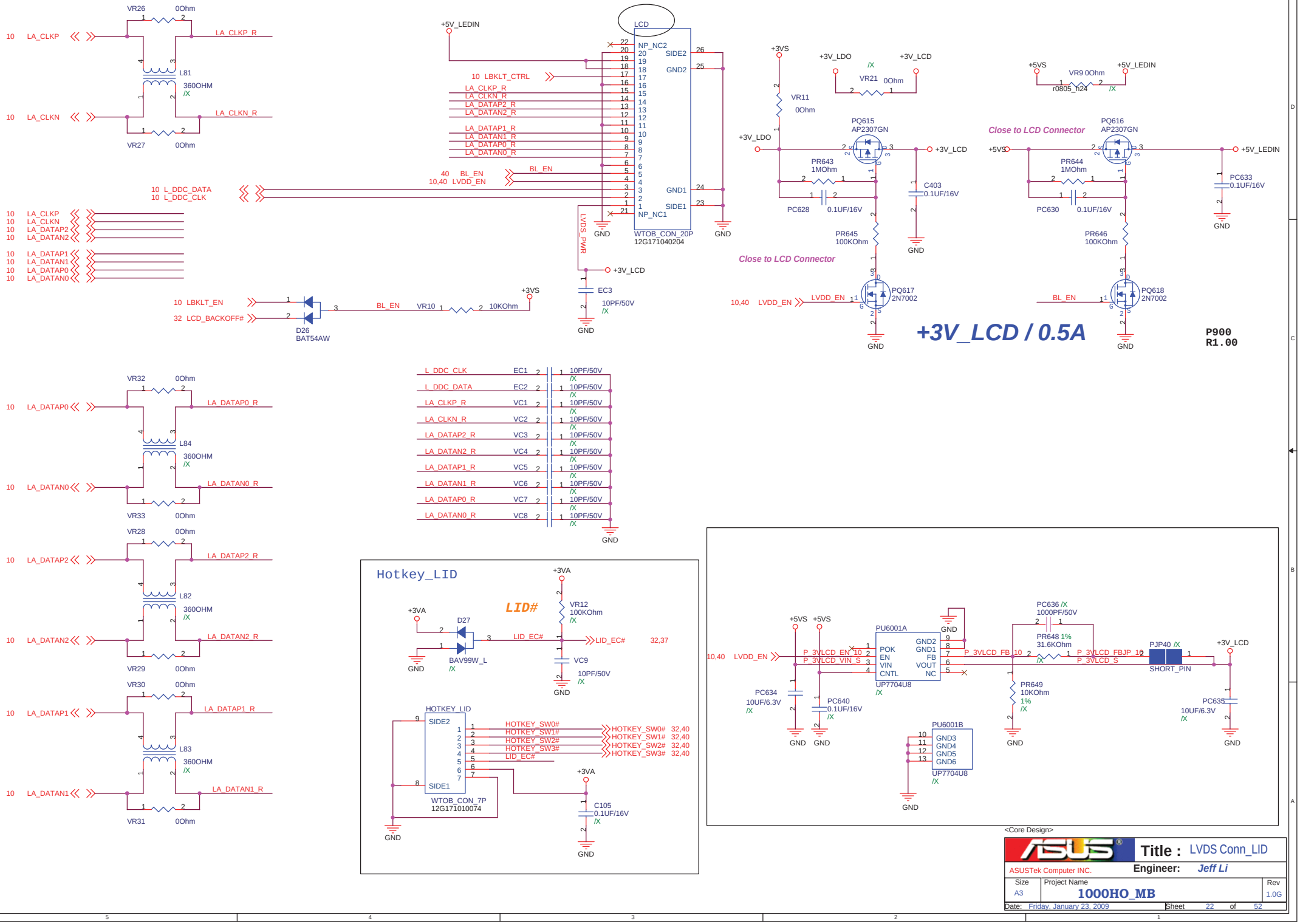
<Core Design>

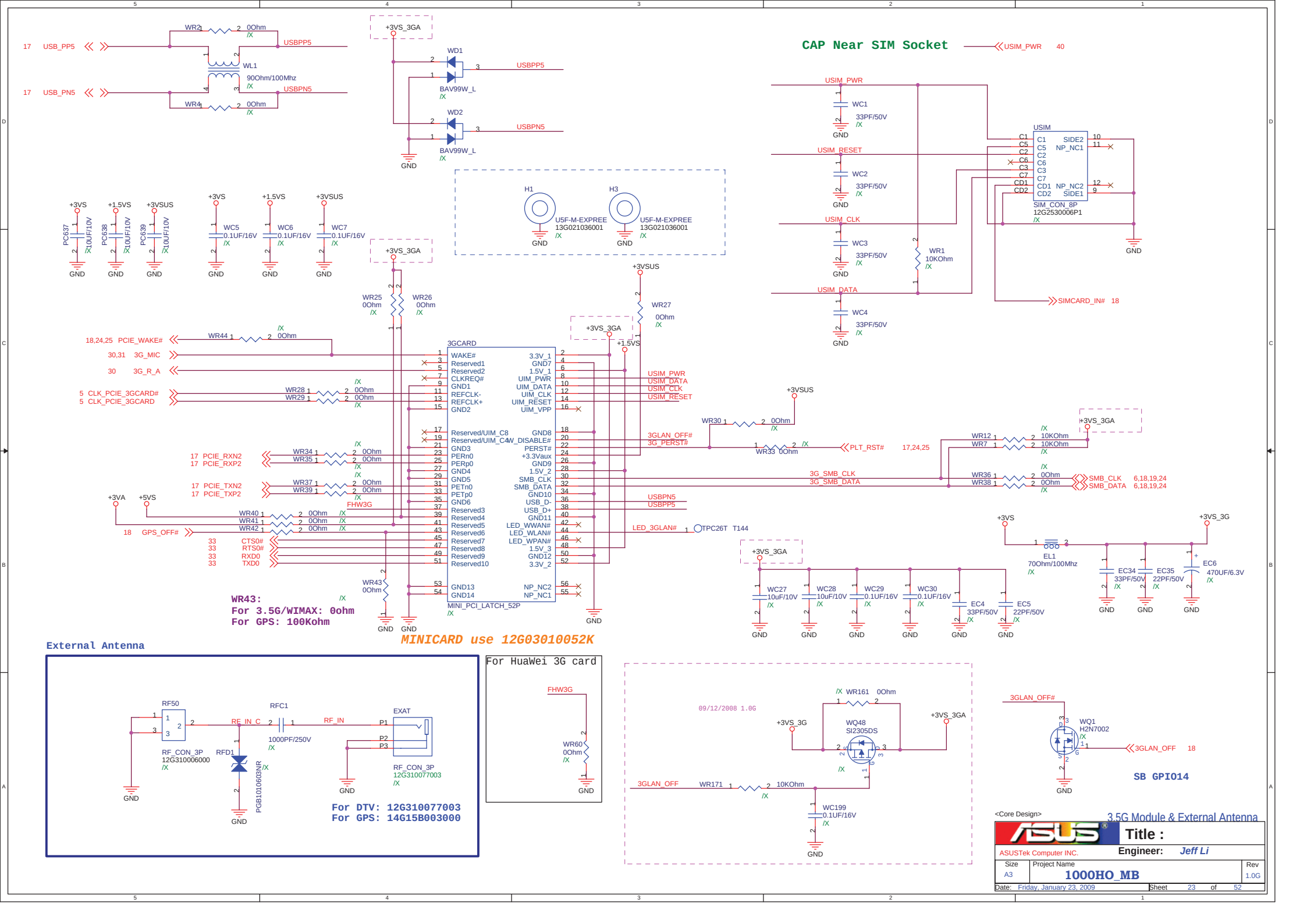
ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Jeff Li*	
Size: A4	Project Name: **1000HO_MB**	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 20 of 52	

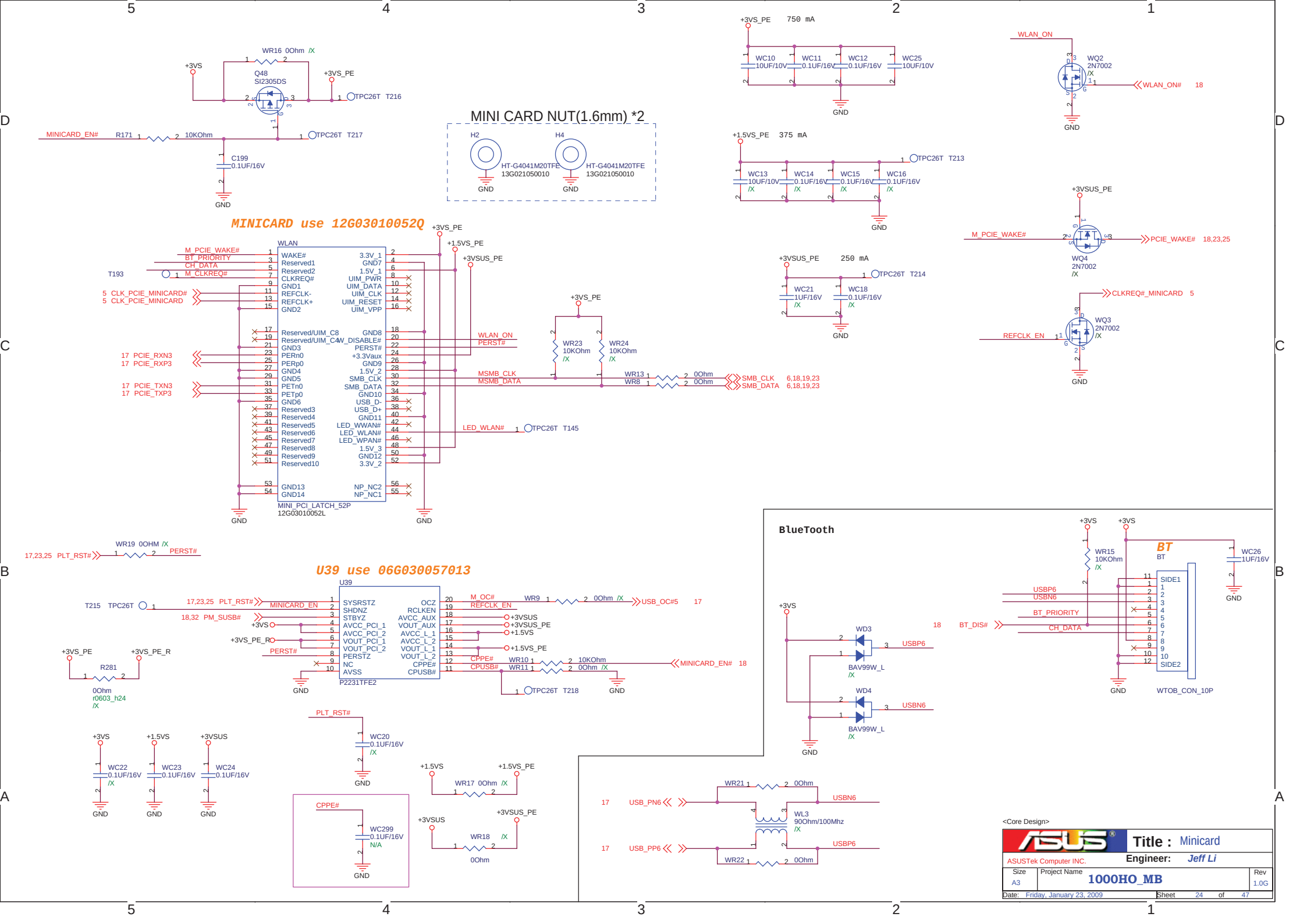


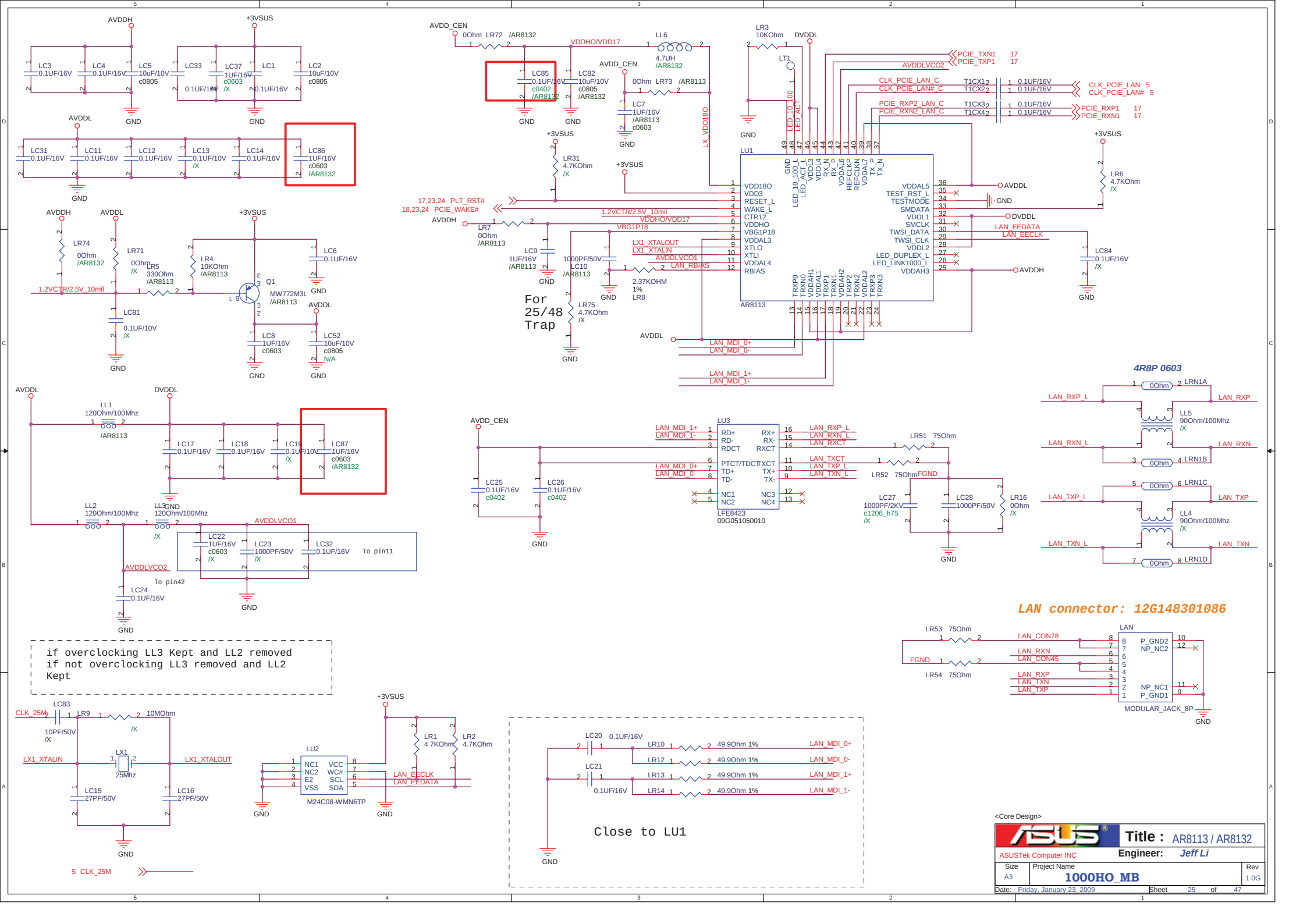
<Core Design>

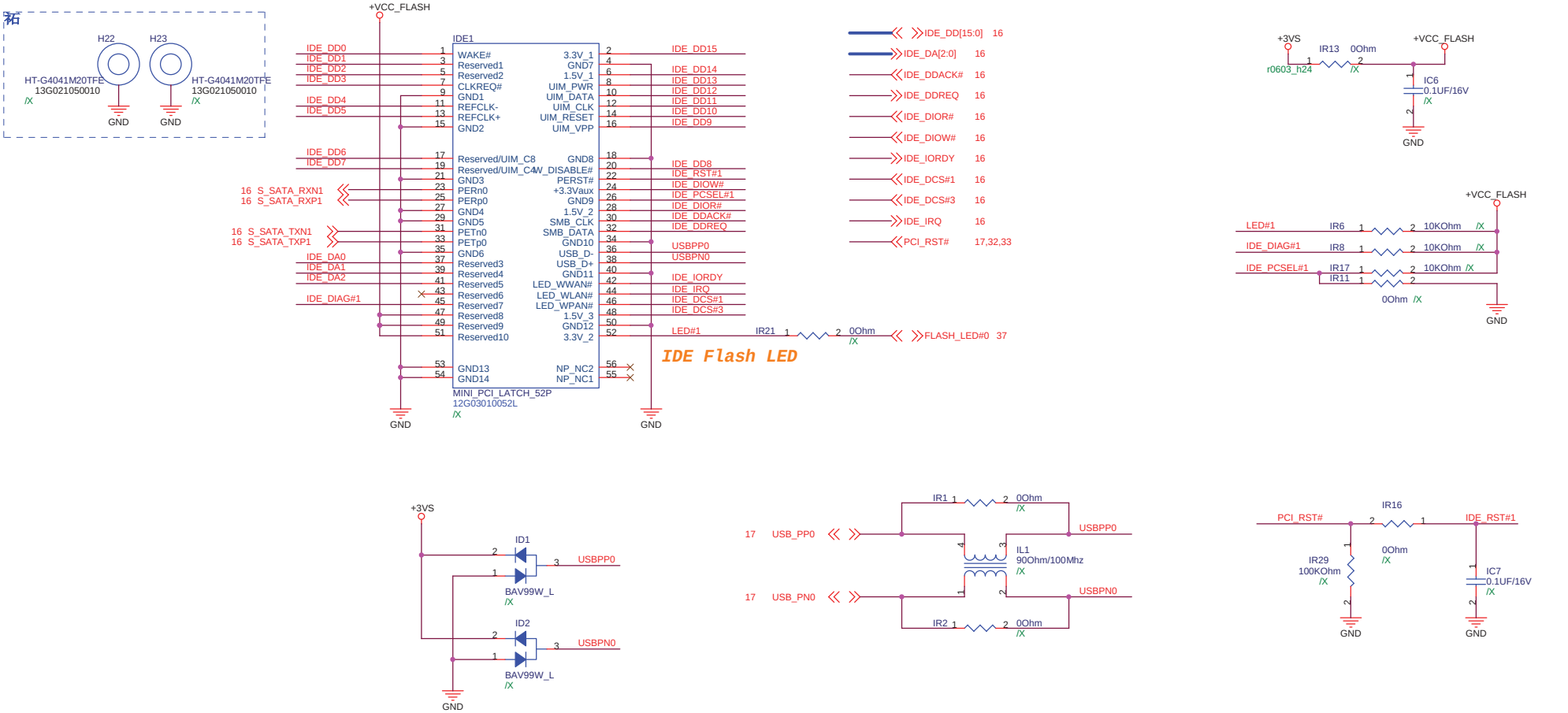
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 21 of 52	


VR26 0Ohm
10 LA_CLKP
LA_CLKP_R
L81
360OHM
/X
10 LA_CLKN
LA_CLKN_R
VR27 0Ohm
LCD
+5V_LEDIN
10 LBKLT_CTRL
LA_CLKP_R
LA_CLKN_R
LA_DATAP2_R
LA_DATAN2_R
LA_DATAP1_R
LA_DATAN1_R
LA_DATAP0_R
LA_DATAN0_R
40 BL_EN
10,40 LVDD_EN
BL_EN
10 L_DDC_DATA
10 L_DDC_CLK
NP_NC2
SIDE2
GND2
GND1
SIDE1
NP_NC1
WTOB_CON_20P
12G171040204
LVDS_PWR
+3V_LCD
EC3
10PF/50V
/X
GND
10 LBKLT_EN
32 LCD_BACKOFF#
D26
BAT54AW
BL_EN
VR10 10KOhm
+3VS
+3VS
+3V_LDO
/X
+3V_LCD
VR21 0Ohm
VR11
0Ohm
PQ615
AP2307GN
PR643
1MOhm
PC628 0.1UF/16V
C403
0.1UF/16V
PR645
100KOhm
Close to LCD Connector
10,40 LVDD_EN
LVDD_EN
PQ617
2N7002
+5VS
VR9 0Ohm
r0805_n24
+5V_LEDIN
/X
Close to LCD Connector
PQ616
AP2307GN
PR644
1MOhm
PC630 0.1UF/16V
PC633
0.1UF/16V
PR646
100KOhm
BL_EN
PQ618
2N7002
+3V_LCD / 0.5A
P900
R1.00
VR32 0Ohm
10 LA_DATAP0
LA_DATAP0_R
L84
360OHM
/X
10 LA_DATAN0
LA_DATAN0_R
VR33 0Ohm
VR28 0Ohm
10 LA_DATAP2
LA_DATAP2_R
L82
360OHM
/X
10 LA_DATAN2
LA_DATAN2_R
VR29 0Ohm
VR30 0Ohm
10 LA_DATAP1
LA_DATAP1_R
L83
360OHM
/X
10 LA_DATAN1
LA_DATAN1_R
VR31 0Ohm
L_DDC_CLK EC1 10PF/50V /X
L_DDC_DATA EC2 10PF/50V /X
LA_CLKP_R VC1 10PF/50V /X
LA_CLKN_R VC2 10PF/50V /X
LA_DATAP2_R VC3 10PF/50V /X
LA_DATAN2_R VC4 10PF/50V /X
LA_DATAP1_R VC5 10PF/50V /X
LA_DATAN1_R VC6 10PF/50V /X
LA_DATAP0_R VC7 10PF/50V /X
LA_DATAN0_R VC8 10PF/50V /X
GND
Hotkey_LID
+3VA
LID#
D27
BAV99W_L
/X
LID_EC#
32,37
VR12
100KOhm
/X
VC9
10PF/50V
/X
HOTKEY_LID
SIDE2
SIDE1
WTOB_CON_7P
12G171010074
HOTKEY_SW0#
HOTKEY_SW1#
HOTKEY_SW2#
HOTKEY_SW3#
LID_EC#
HOTKEY_SW0# 32,40
HOTKEY_SW1# 32,40
HOTKEY_SW2# 32,40
HOTKEY_SW3# 32,40
C105
0.1UF/16V
/X
+5VS
+5VS
10,40 LVDD_EN
P_3VLCD_EN_10
P_3VLCD_VIN_S
PU6001A
POK
EN
VIN
CNTL
GND2
GND1
FB
VOUT
NC
UP7704U8
/X
P_3VLCD_FB_10
PC636 /X
1000PF/50V
PR648 1%
31.6KOhm
/X
P_3VLCD_FBJP_10
P_3VLCD_S
PJP40 /X
SHORT_PIN
+3V_LCD
PC634
10UF/6.3V
/X
PC640
0.1UF/16V
/X
PR649
10KOhm
1%
/X
PC635
10UF/6.3V
/X
PU6001B
GND3
GND4
GND5
GND6
UP7704U8
/X
<Core Design>
Title : LVDS Conn_LID
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 22 of 52

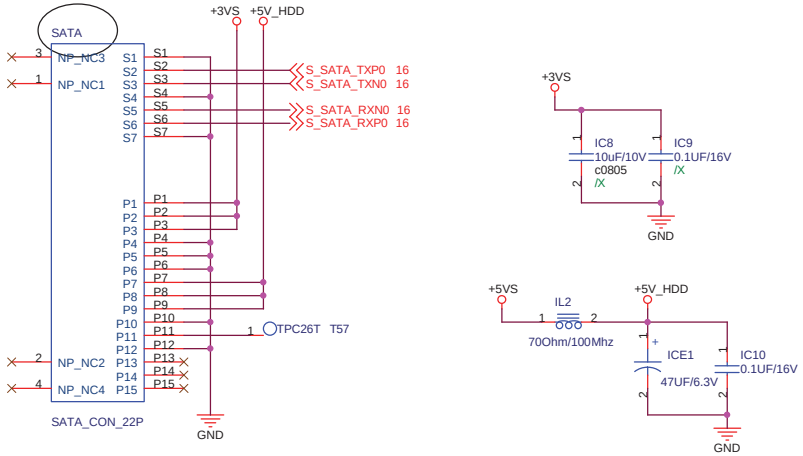

CAP Near SIM Socket
USIM_PWR 40
WR2 0Ohm /X
USB_PP5 17
USBPP5
WL1
90Ohm/100Mhz /X
USB_PN5 17
USBPN5
WR4 0Ohm /X
+3VS_3GA
WD1
BAV99W_L /X
WD2
BAV99W_L /X
GND
USIM_PWR
WC1 33PF/50V /X
USIM_RESET
WC2 33PF/50V /X
USIM_CLK
WC3 33PF/50V /X
USIM_DATA
WC4 33PF/50V /X
WR1 10KOhm /X
USIM
C1 SIDE2 10
C5 NP_NC1 11
C2
C6
C3
C7
CD1 NP_NC2 12
CD2 SIDE1 9
SIM_CON_8P
12G2530006P1 /X
SIMCARD_IN# 18
+3VS
+1.5VS
+3VSUS
PC637 10UF/10V /X
PC638 10UF/10V /X
PC639 10UF/10V /X
WC5 0.1UF/16V /X
WC6 0.1UF/16V /X
WC7 0.1UF/16V /X
H1
H3
U5F-M-EXPREE
13G021036001 /X
WR25 0Ohm /X
WR26 0Ohm /X
WR27 0Ohm /X
18,24,25 PCIE_WAKE#
30,31 3G_MIC
30 3G_R_A
5 CLK_PCIE_3GCARD#
5 CLK_PCIE_3GCARD
WR44 0Ohm /X
WR28 0Ohm /X
WR29 0Ohm /X
3GCARD
WAKE# 3.3V_1
Reserved1 GND7
Reserved2 1.5V_1
CLKREQ# UIM_PWR
GND1 UIM_DATA
REFCLK- UIM_CLK
REFCLK+ UIM_RESET
GND2 UIM_VPP
Reserved/UIM_C8 GND8
Reserved/UIM_C4 W_DISABLE#
GND3 PERST#
PERn0 +3.3Vaux
PERp0 GND9
GND4 1.5V_2
GND5 SMB_CLK
PETn0 SMB_DATA
PETp0 GND10
GND6 USB_D-
Reserved3 USB_D+
Reserved4 GND11
Reserved5 LED_WWAN#
Reserved6 LED_WLAN#
Reserved7 LED_WPAN#
Reserved8 1.5V_3
Reserved9 GND12
Reserved10 3.3V_2
GND13 NP_NC2
GND14 NP_NC1
MINI_PCI_LATCH_52P /X
USIM_PWR
USIM_DATA
USIM_CLK
USIM_RESET
3GLAN_OFF#
3G_PERST#
USBPN5
USBPP5
LED_3GLAN# 1
TPC26T T144
17 PCIE_RXN2
17 PCIE_RXP2
17 PCIE_TXN2
17 PCIE_TXP2
WR34 0Ohm /X
WR35 0Ohm /X
WR37 0Ohm /X
WR39 0Ohm /X
+3VA
+5VS
FHW3G
WR40 0Ohm /X
WR41 0Ohm /X
WR42 0Ohm /X
18 GPS_OFF#
33 CTS0#
33 RTS0#
33 RXD0
33 TXD0
WR43 0Ohm /X
WR30 0Ohm /X
WR33 0Ohm /X
PLT_RST# 17,24,25
WR12 10KOhm /X
WR7 10KOhm /X
WR36 0Ohm /X
WR38 0Ohm /X
3G_SMB_CLK
3G_SMB_DATA
SMB_CLK 6,18,19,24
SMB_DATA 6,18,19,24
WC27 10uF/10V /X
WC28 10uF/10V /X
WC29 0.1UF/16V /X
WC30 0.1UF/16V /X
EC4 33PF/50V /X
EC5 22PF/50V /X
EL1 70Ohm/100Mhz /X
EC34 33PF/50V /X
EC35 22PF/50V /X
EC6 470UF/6.3V /X
WR161 0Ohm /X
09/12/2008 1.0G
WQ48 SI2305DS
3GLAN_OFF
WR171 10KOhm /X
WC199 0.1UF/16V /X
WQ1 H2N7002 /X
3GLAN_OFF 18
SB GPIO14
WR43:
For 3.5G/WIMAX: 0ohm
For GPS: 100Kohm
MINICARD use 12G03010052K
External Antenna
RF50
RF_CON_3P
12G310006000 /X
RFC1
RF_IN_C
1000PF/250V /X
RF_IN
RFD1
PGB1010603NR /X
EXAT
P1
P2
P3
RF_CON_3P
12G310077003 /X
For DTV: 12G310077003
For GPS: 14G15B003000
For HuaWei 3G card
FHW3G
WR60 0Ohm /X
<Core Design>
3.5G Module & External Antenna
Title :
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 23 of 52


MINI CARD NUT(1.6mm) *2
MINICARD use 12G030010052Q
U39 use 06G030057013
BlueTooth
WLAN
MINI_PCI_LATCH_52P
12G03010052L
P2231TFE2
WTOB_CON_10P
<Core Design>
Title : Minicard
ASUSTek Computer INC.
Engineer: Jeff Li
1000HO_MB
Date: Friday, January 23, 2009
Sheet 24 of 47


AVDDH
+3VSUS
AVDDL
GND
LC3 0.1UF/16V
LC4 0.1UF/16V
LC5 10uF/10V c0805
LC33 0.1UF/16V
LC37 1UF/16V c0603 /X
LC1 0.1UF/16V
LC2 10uF/10V c0805
LC31 0.1UF/16V
LC11 0.1UF/16V
LC12 0.1UF/16V
LC13 0.1UF/16V /X
LC14 0.1UF/16V
LC86 1UF/16V c0603 /AR8132
LR74 0Ohm /AR8132
LR71 0Ohm /X
LR5 330Ohm /AR8113
LR4 10KOhm /AR8113
1.2VCTR/2.5V_10mil
Q1
MW772M3L /AR8113
LC6 0.1UF/16V
LC81 0.1UF/10V /X
LC8 1UF/16V c0603
LC52 10uF/10V c0805 N/A
AVDD_CEN
0Ohm LR72 /AR8132
VDDHO/VDD17
LL6 4.7UH /AR8132
LC85 0.1UF/16V c0402 /AR8132
LC82 10uF/10V c0805 /AR8132
0Ohm LR73 /AR8113
LC7 1UF/16V /AR8113 c0603
LX_VDD18O
LR31 4.7KOhm /X
17,23,24 PLT_RST#
18,23,24 PCIE_WAKE#
LR7 0Ohm /AR8113
VBG1P18
LC9 1UF/16V /AR8113
1000PF/50V
LC10 /AR8113
LX1_XTALOUT
LX1_XTALIN
AVDDLVCO1
LAN_RBIAS
2.37KOHM 1% LR8
LR75 4.7KOhm /X
For 25/48 Trap
LR3 10KOhm
DVDDL
LT1
LED_10_100
LED_ACT
LU1
VDD18O
VDD3
RESET_L
WAKE_L
CTR12
VDDHO
VBG1P18
VDDAL3
XTLO
XTLI
VDDAL4
RBIAS
AR8113
PCIE_TXN1 17
PCIE_TXP1 17
AVDDLVCO2
CLK_PCIE_LAN_C
CLK_PCIE_LAN#_C
T1CX12
T1CX22
0.1UF/16V
CLK_PCIE_LAN 5
CLK_PCIE_LAN# 5
PCIE_RXP2_LAN_C
PCIE_RXN2_LAN_C
T1CX32
T1CX42
PCIE_RXP1 17
PCIE_RXN1 17
VDDAL5
TEST_RST_L
TESTMODE
SMDATA
VDDL1
SMCLK
TWSI_DATA
TWSI_CLK
VDDL2
LED_DUPLEX_L
LED_LINK1000_L
VDDAH3
LAN_EEDATA
LAN_EECLK
LR6 4.7KOhm /X
LC84 0.1UF/16V /X
LAN_MDI_0+
LAN_MDI_0-
LAN_MDI_1+
LAN_MDI_1-
LL1 120Ohm/100Mhz /AR8113
LC17 0.1UF/16V
LC18 0.1UF/16V
LC19 0.1UF/10V /X
LC87 1UF/16V c0603 /AR8132
LL2 120Ohm/100Mhz
LL3 120Ohm/100Mhz /X
AVDDLVCO1
LC22 1UF/16V c0603 /X
LC23 1000PF/50V /X
LC32 0.1UF/16V
To pin11
AVDDLVCO2
To pin42
LC24 0.1UF/16V
LU3
RD+
RD-
RDCT
PTCT/TDCT
TD+
TD-
RX+
RX-
RXCT
TXCT
TX+
TX-
NC1
NC2
NC3
NC4
LFE8423
09G051050010
LAN_RXP_L
LAN_RXN_L
LAN_RXCT
LAN_TXCT
LAN_TXP_L
LAN_TXN_L
LC25 0.1UF/16V c0402
LC26 0.1UF/16V c0402
LR51 75Ohm
LR52 75Ohm FGND
LC27 1000PF/2KV c1206_h75 /X
LC28 1000PF/50V
LR16 0Ohm /X
4R8P 0603
LRN1A
LRN1B
LRN1C
LRN1D
LL5 90Ohm/100Mhz /X
LL4 90Ohm/100Mhz /X
LAN connector: 12G148301086
LR53 75Ohm
LR54 75Ohm
LAN_CON78
LAN_CON45
LAN
P_GND2
NP_NC2
NP_NC1
P_GND1
MODULAR_JACK_8P
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept
CLK_25M
LC83 10PF/50V /X
LR9 10MOhm /X
LX1
25Mhz
LC15 27PF/50V
LC16 27PF/50V
5 CLK_25M
LU2
NC1
NC2
E2
VSS
VCC
WC#
SCL
SDA
M24C08-WMN6TP
LR1 4.7KOhm
LR2 4.7KOhm
LAN_EECLK
LAN_EEDATA
LC20 0.1UF/16V
LC21 0.1UF/16V
LR10 49.9Ohm 1%
LR12 49.9Ohm 1%
LR13 49.9Ohm 1%
LR14 49.9Ohm 1%
Close to LU1
<Core Design>
Title : AR8113 / AR8132
ASUSTek Computer INC
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 25 of 47


H22
H23
HT-G4041M20TFE
13G021050010
/X
GND
+VCC_FLASH
IDE1
WAKE#
Reserved1
Reserved2
CLKREQ#
GND1
REFCLK-
REFCLK+
GND2
3.3V_1
GND7
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
Reserved/UIM_C8
Reserved/UIM_C4
GND3
PERn0
PERp0
GND4
GND5
PETn0
PETp0
GND6
Reserved3
Reserved4
Reserved5
Reserved6
Reserved7
Reserved8
Reserved9
Reserved10
GND8
W_DISABLE#
PERST#
+3.3Vaux
GND9
1.5V_2
SMB_CLK
SMB_DATA
GND10
USB_D-
USB_D+
GND11
LED_WWAN#
LED_WLAN#
LED_WPAN#
1.5V_3
GND12
3.3V_2
GND13
GND14
NP_NC2
NP_NC1
MINI_PCI_LATCH_52P
12G03010052L
IDE_DD0
IDE_DD1
IDE_DD2
IDE_DD3
IDE_DD4
IDE_DD5
IDE_DD6
IDE_DD7
IDE_DA0
IDE_DA1
IDE_DA2
IDE_DIAG#1
16 S_SATA_RXN1
16 S_SATA_RXP1
16 S_SATA_TXN1
16 S_SATA_TXP1
IDE_DD15
IDE_DD14
IDE_DD13
IDE_DD12
IDE_DD11
IDE_DD10
IDE_DD9
IDE_DD8
IDE_RST#1
IDE_DIOW#
IDE_PCSEL#1
IDE_DIOR#
IDE_DDACK#
IDE_DDREQ
USBPP0
USBPN0
IDE_IORDY
IDE_IRQ
IDE_DCS#1
IDE_DCS#3
LED#1
IR21 1 2 0Ohm /X
FLASH_LED#0 37
IDE_DD[15:0] 16
IDE_DA[2:0] 16
IDE_DDACK# 16
IDE_DDREQ 16
IDE_DIOR# 16
IDE_DIOW# 16
IDE_IORDY 16
IDE_DCS#1 16
IDE_DCS#3 16
IDE_IRQ 16
PCI_RST# 17,32,33
IDE Flash LED
+3VS
IR13 0Ohm
r0603_h24
IC6
0.1UF/16V
LED#1
IDE_DIAG#1
IDE_PCSEL#1
IR6 10KOhm
IR8 10KOhm
IR17 10KOhm
IR11 0Ohm
ID1
ID2
BAV99W_L
IR1 0Ohm
IR2 0Ohm
17 USB_PP0
17 USB_PN0
IL1
90Ohm/100Mhz
IR16
IR29
100KOhm
IC7
PCI_RST#
IDE_RST#1
Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?
<Core Design>
Title : HD + Flash Conn
ASUSTek Computer INC.
Engineer: Kell_Huang
Size A3
Project Name 1000H_MB
Rev 1.1G
Date: Friday, January 23, 2009
Sheet 26 of 47

SATA HDD Connector



<Core Design>

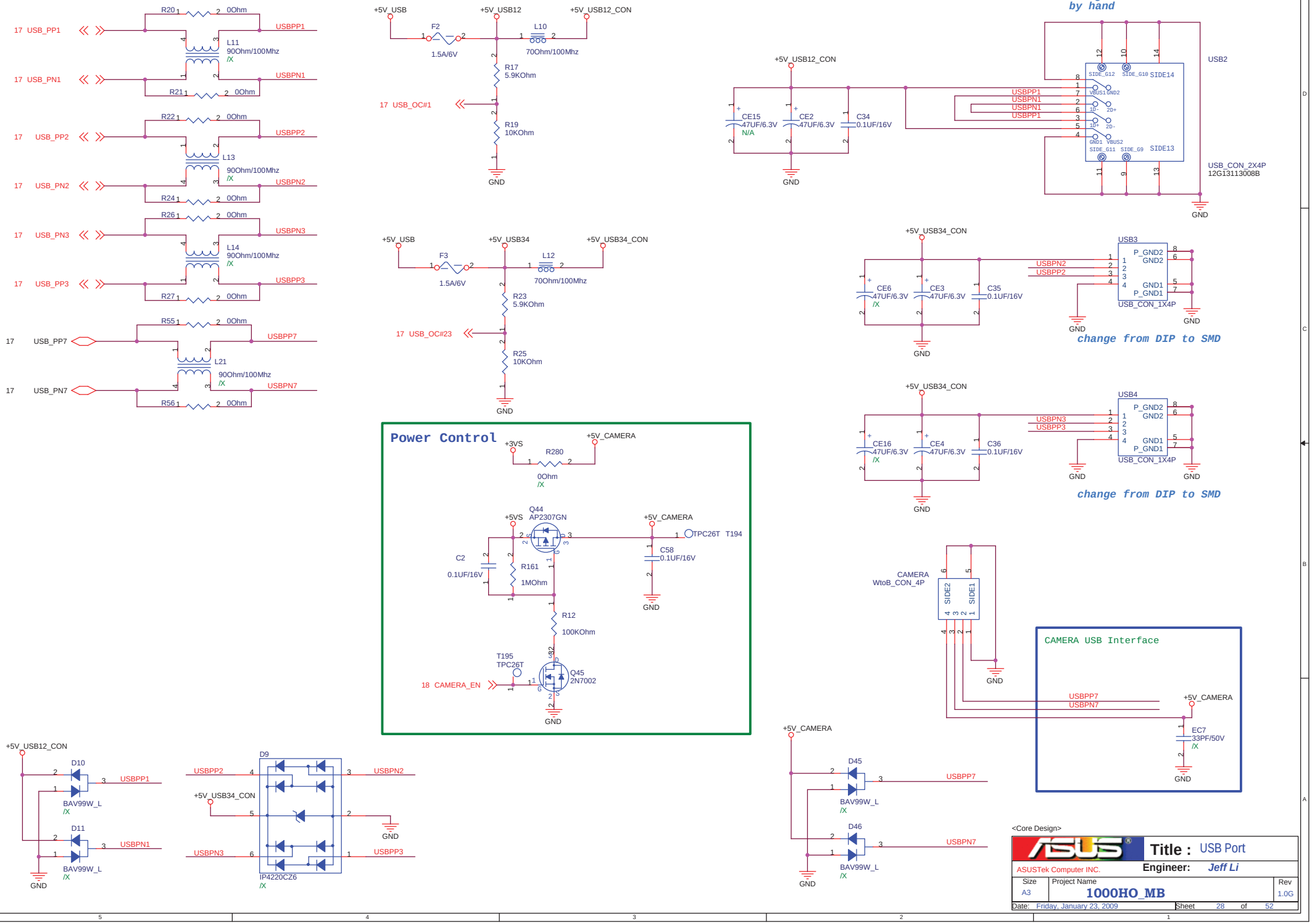
ASUSTek Computer INC.

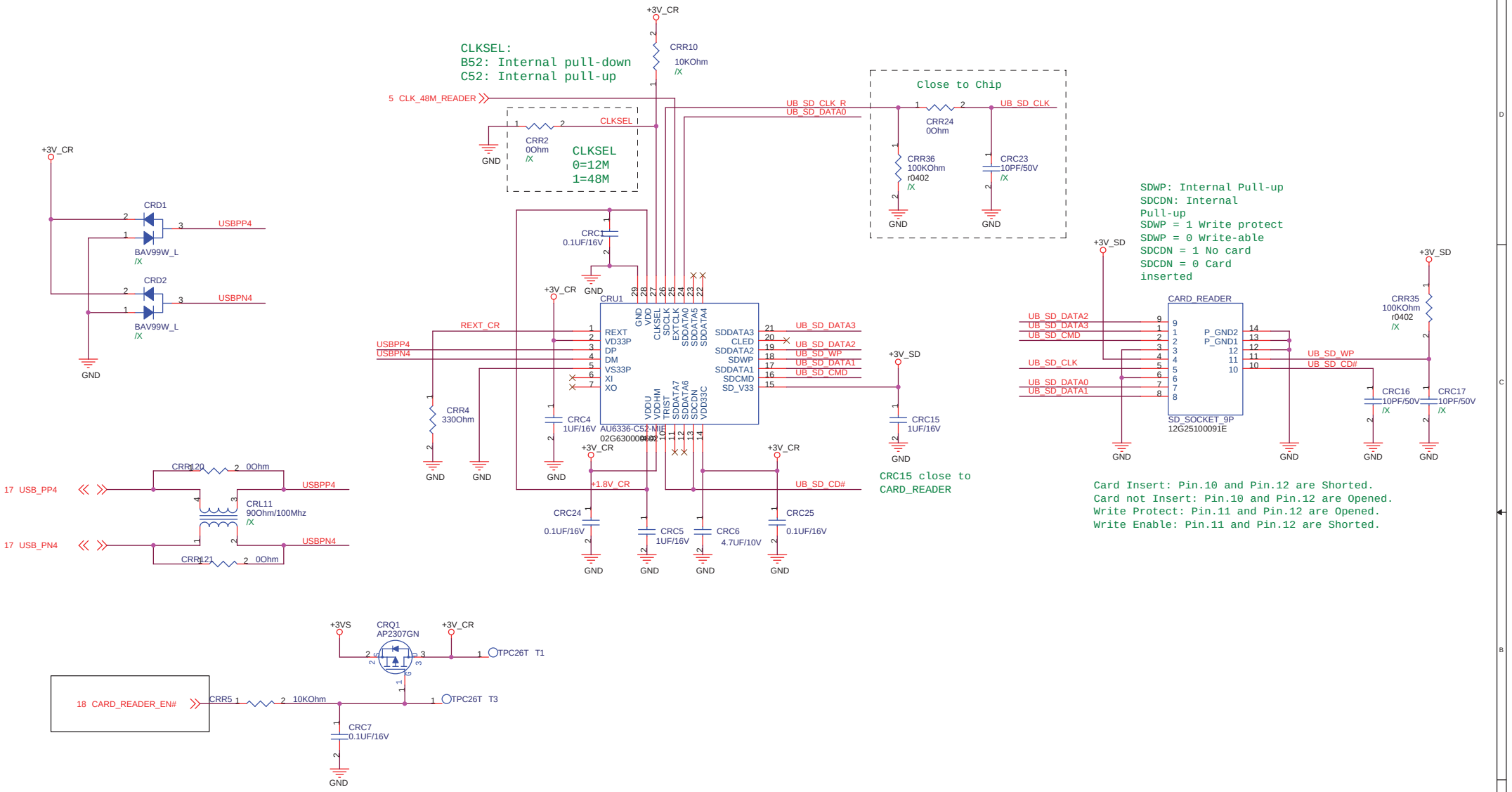
Title : HDD

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

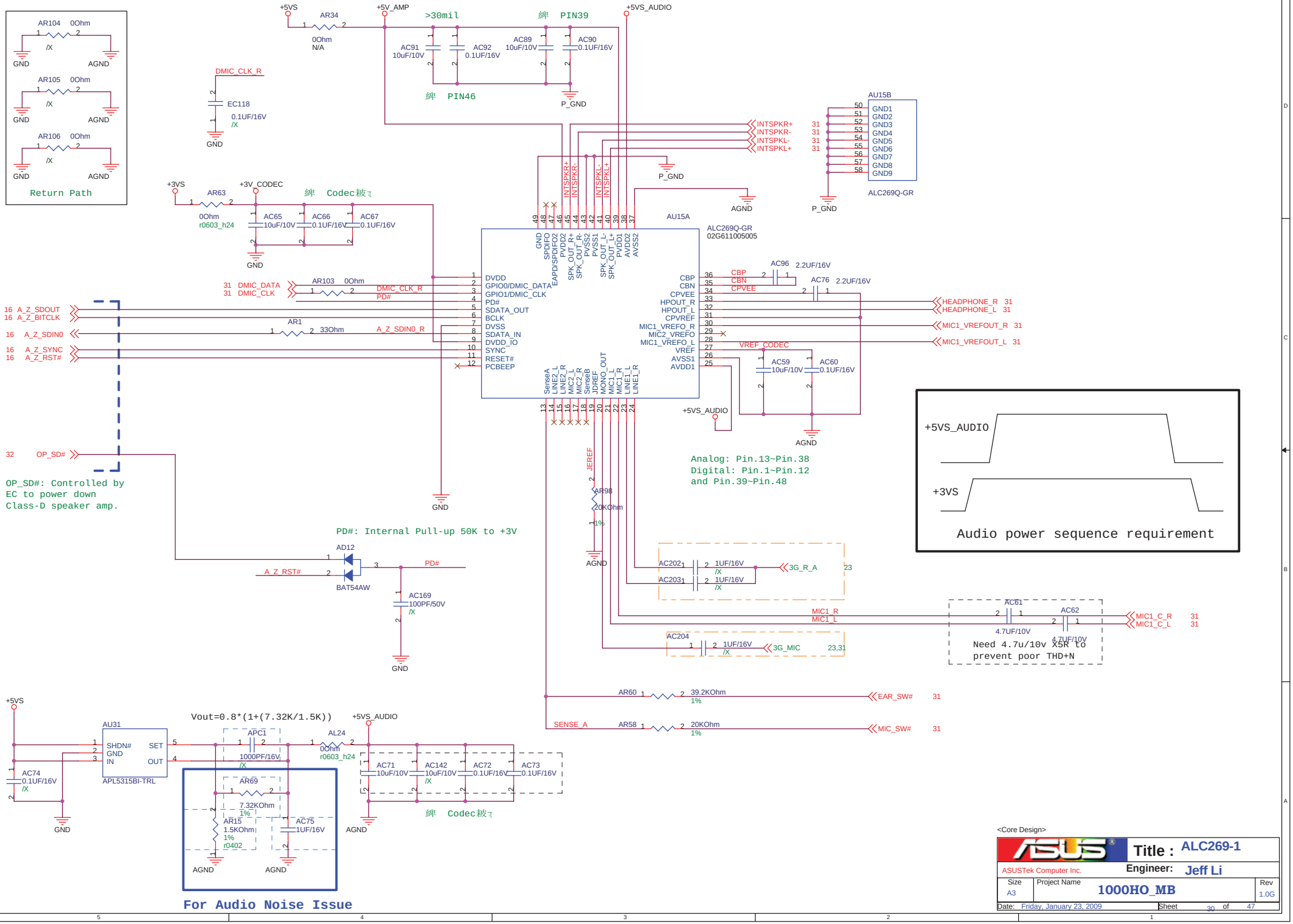
Date: Friday, January 23, 2009 Sheet 27 of 47


change from DIP to SMD by hand
USB_PP1
USB_PN1
USB_PP2
USB_PN2
USB_PN3
USB_PP3
USB_PP7
USB_PN7
R20 0Ohm
R21 0Ohm
R22 0Ohm
R24 0Ohm
R26 0Ohm
R27 0Ohm
R55 0Ohm
R56 0Ohm
L11 90Ohm/100Mhz /X
L13 90Ohm/100Mhz /X
L14 90Ohm/100Mhz /X
L21 90Ohm/100Mhz /X
USBPP1
USBPN1
USBPP2
USBPN2
USBPN3
USBPP3
USBPP7
USBPN7
+5V_USB
+5V_USB12
+5V_USB12_CON
F2 1.5A/6V
L10 70Ohm/100Mhz
R17 5.9KOhm
R19 10KOhm
USB_OC#1
GND
CE15 47UF/6.3V N/A
CE2 47UF/6.3V
C34 0.1UF/16V
USB2
SIDE_G12
SIDE_G10
SIDE14
SIDE_G11
SIDE_G9
SIDE13
VBUS1
GND2
1D-
2D+
1D+
2D-
GND1
VBUS2
USB_CON_2X4P
12G13113008B
+5V_USB34
+5V_USB34_CON
F3 1.5A/6V
L12 70Ohm/100Mhz
R23 5.9KOhm
R25 10KOhm
USB_OC#23
CE6 47UF/6.3V /X
CE3 47UF/6.3V
C35 0.1UF/16V
USB3
P_GND2
GND2
GND1
P_GND1
USB_CON_1X4P
CE16 47UF/6.3V /X
CE4 47UF/6.3V
C36 0.1UF/16V
USB4
Power Control
+3VS
+5V_CAMERA
R280 0Ohm /X
Q44 AP2307GN
C2 0.1UF/16V
R161 1MOhm
C58 0.1UF/16V
TPC26T T194
R12 100KOhm
T195 TPC26T
Q45 2N7002
CAMERA_EN
CAMERA WtoB_CON_4P
SIDE2
SIDE1
CAMERA USB Interface
EC7 33PF/50V /X
D10
D11
BAV99W_L /X
D9
IP4220CZ6 /X
D45
D46
<Core Design>
Title : USB Port
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 28 of 52



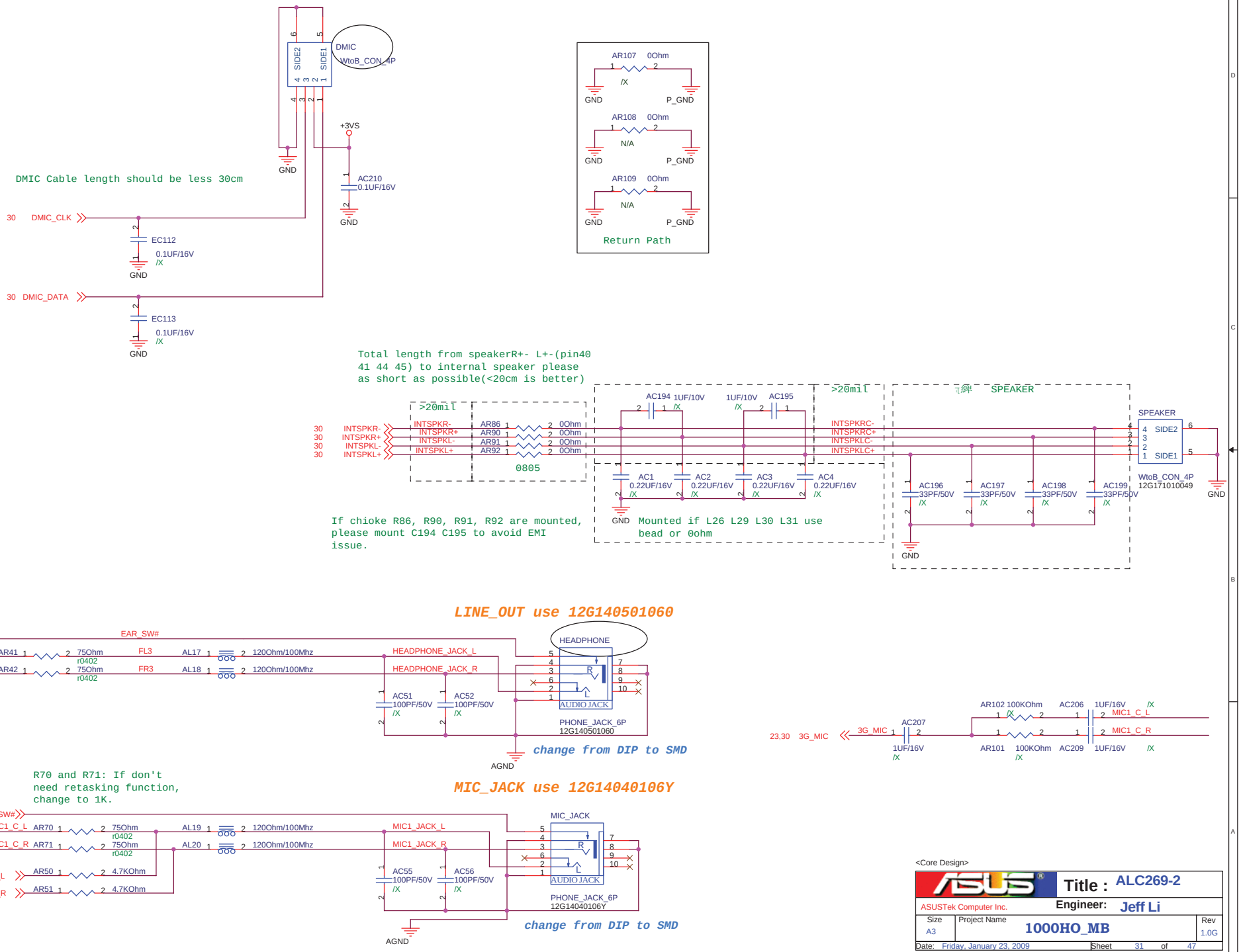
<Core Design>

ASUSTek Computer Inc.	Title : AU6336-C52	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 29 of 47	



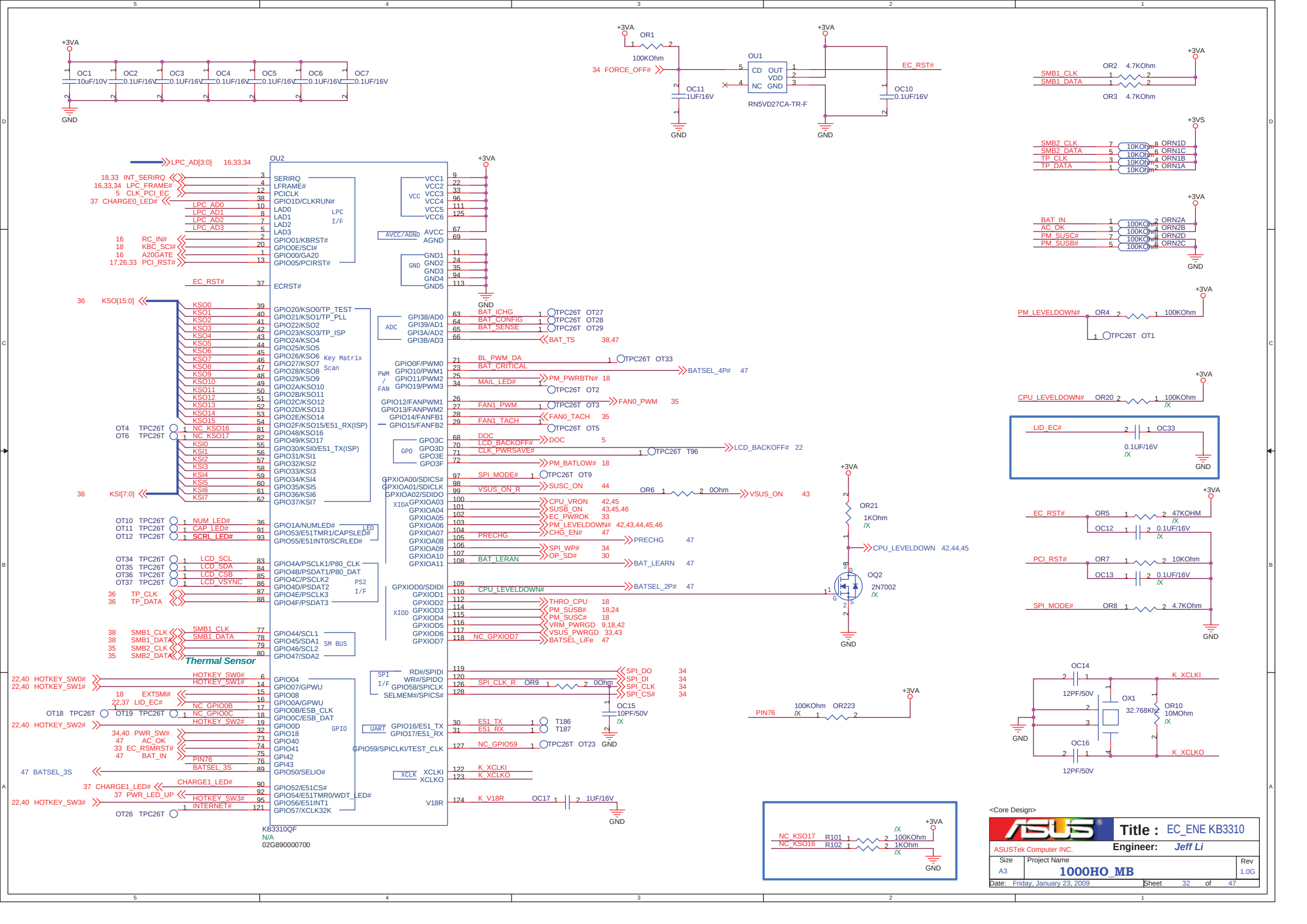
<Core Design>

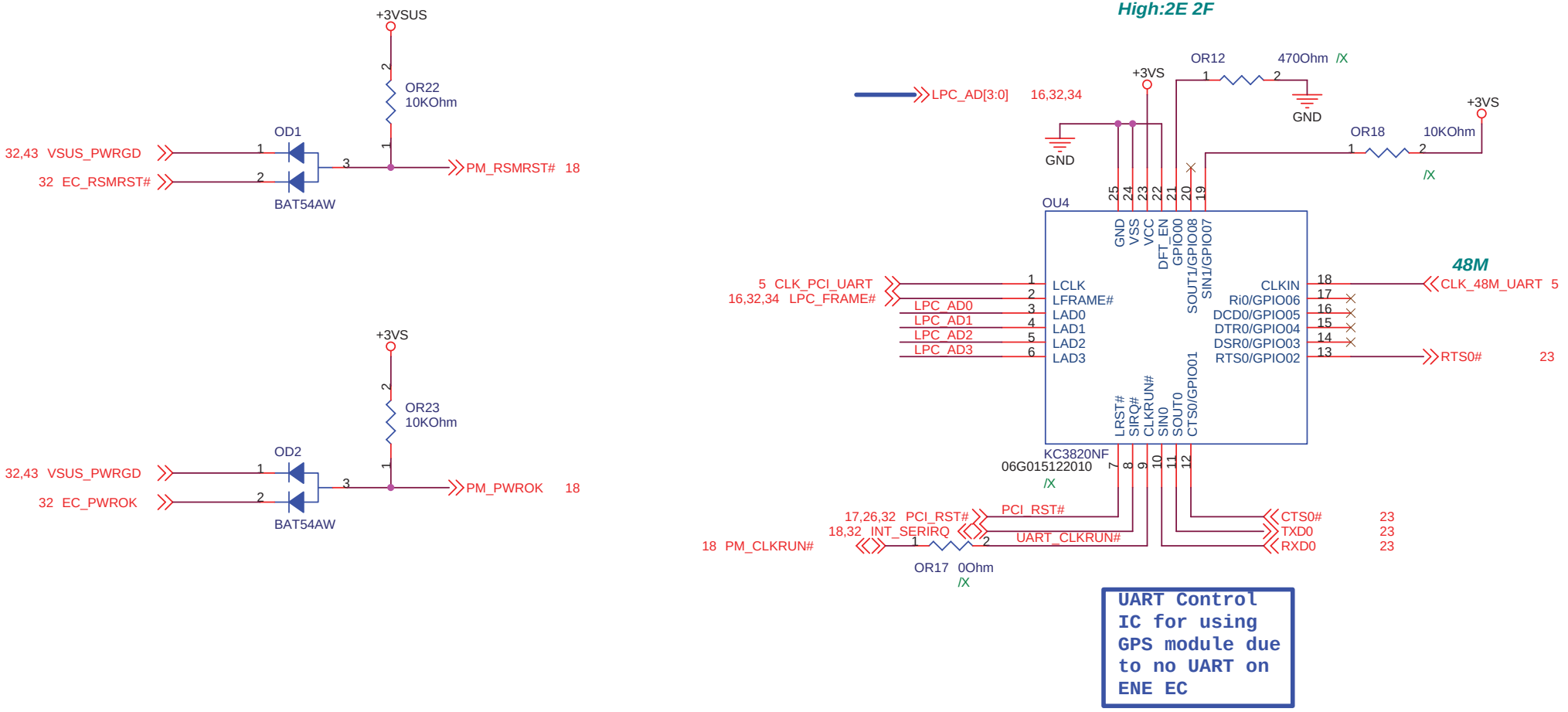
ASUSTek Computer Inc.	Title : ALC269-1	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 30 of 47	



<Core Design>

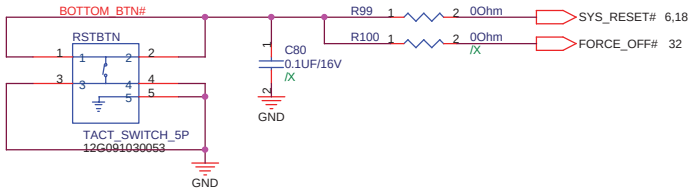
ASUSTek Computer Inc.	Title : ALC269-2	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 31 of 47	

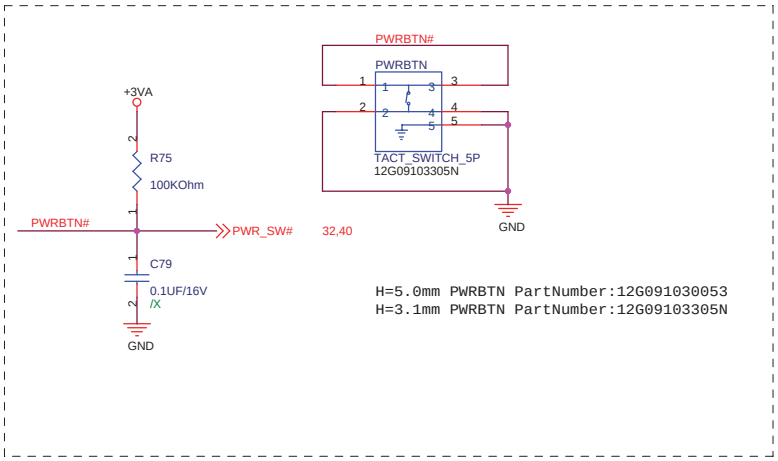

OU2
KB3310QF
N/A
02G890000700
Thermal Sensor
Key Matrix Scan
LPC I/F
PS2 I/F
SM BUS
LED
GPIO
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 32 of 47
<Core Design>

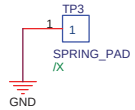


<Core Design>

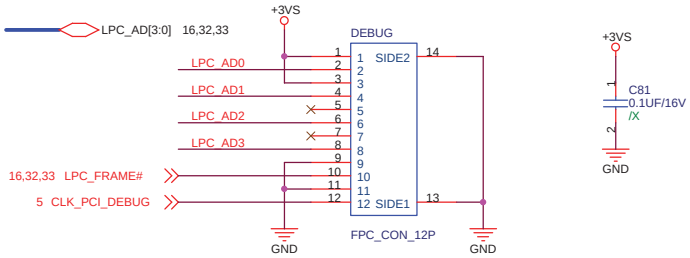
ASUSTek Computer INC.	Title : EC_UART_KC3820	
	Engineer: Jeff Li	
Size: A4	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 33 of 47	



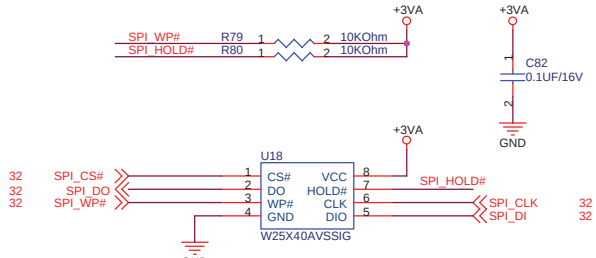




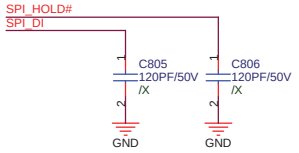
For Debug



Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125

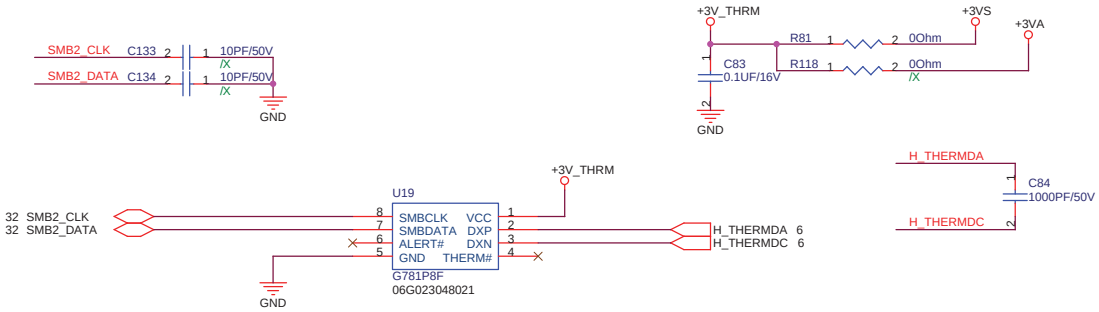


U18 use 05G001002900 & 05G00100F130

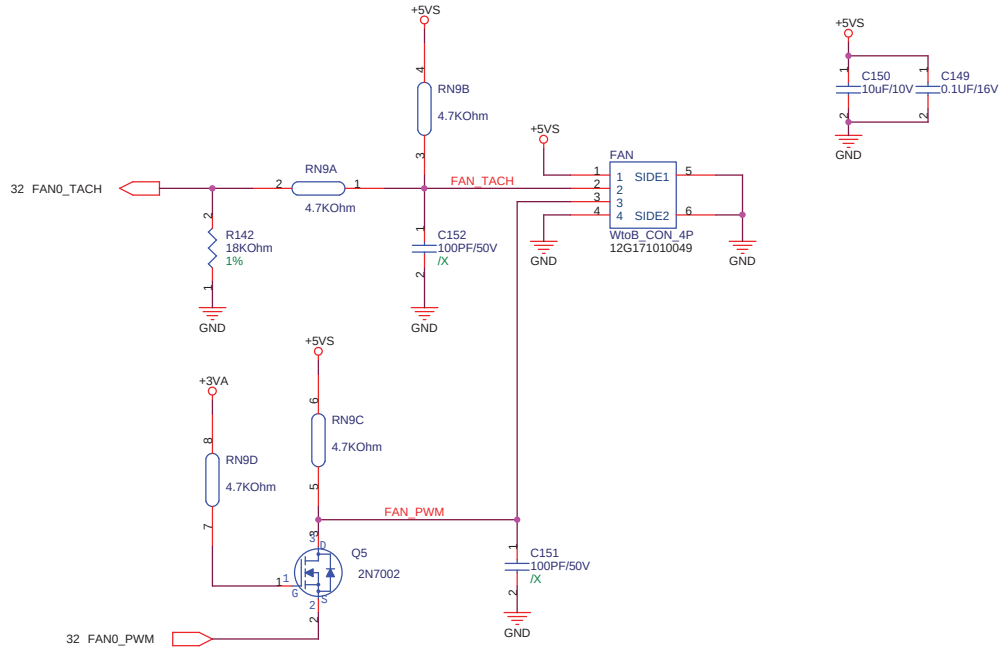


<Core Design>

ASUSTek Computer INC.	Title : Switch_SPI ROM_Debug	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 34 of 52	



U19 use 06G023048021

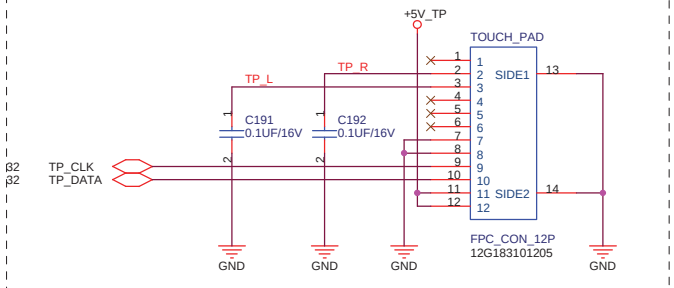


<Core Design>

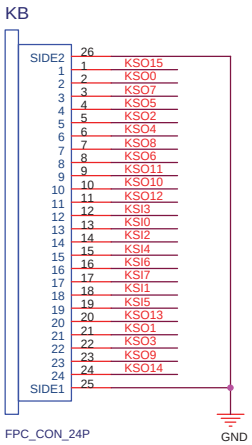
ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 35 of 52	

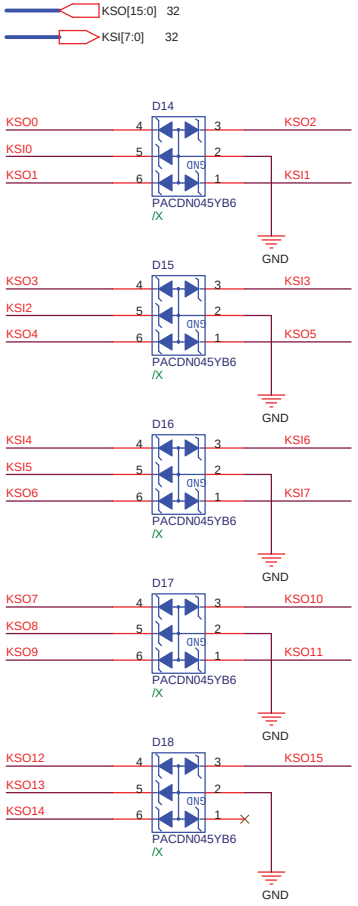
For Touch-Pad

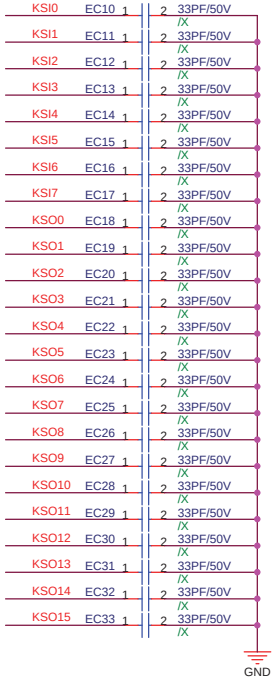
P900 R1.0G



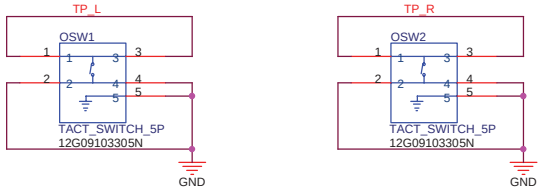
For Keyboard Connector

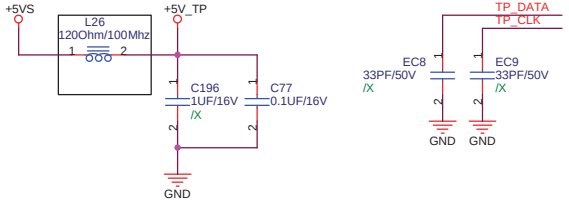


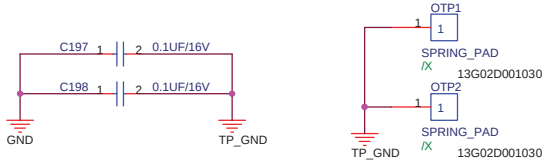




SW2, SW3 use 12G09103305N



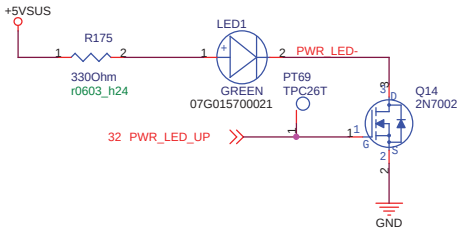




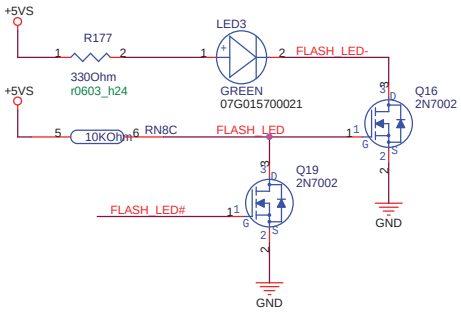
<Core Design>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 36 of 52	

for POWER LED

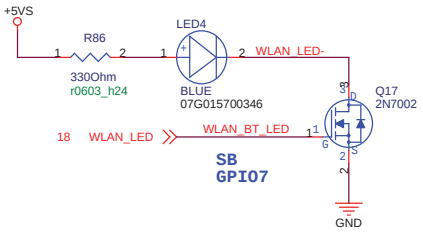


for FLASH LED

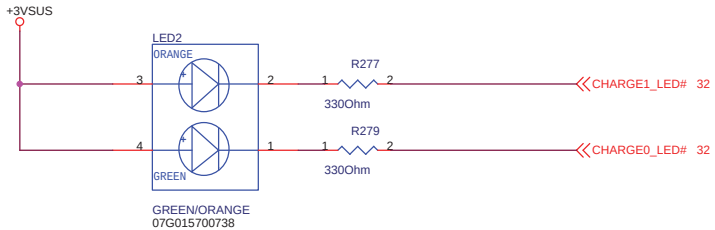


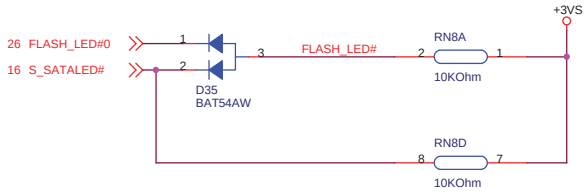
for WLAN/BlueTooth LED

R86 use 4.7K OHm 10G213472003030

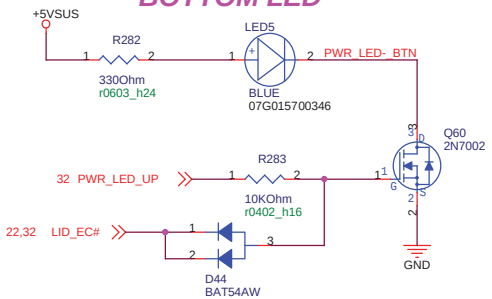


for CHARGE LED





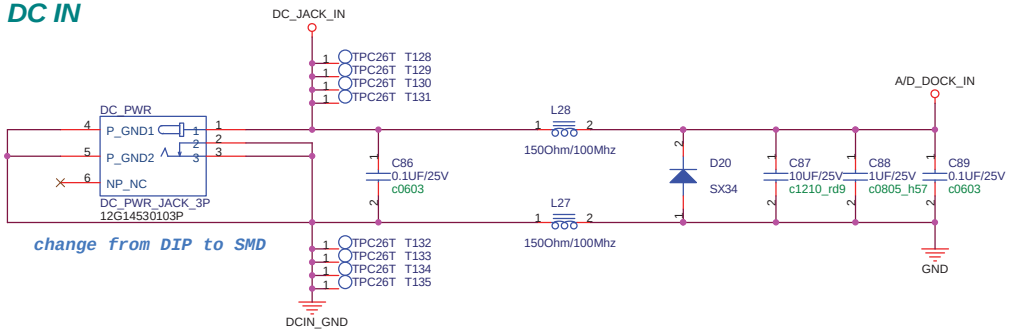
for POWER BOTTOM LED



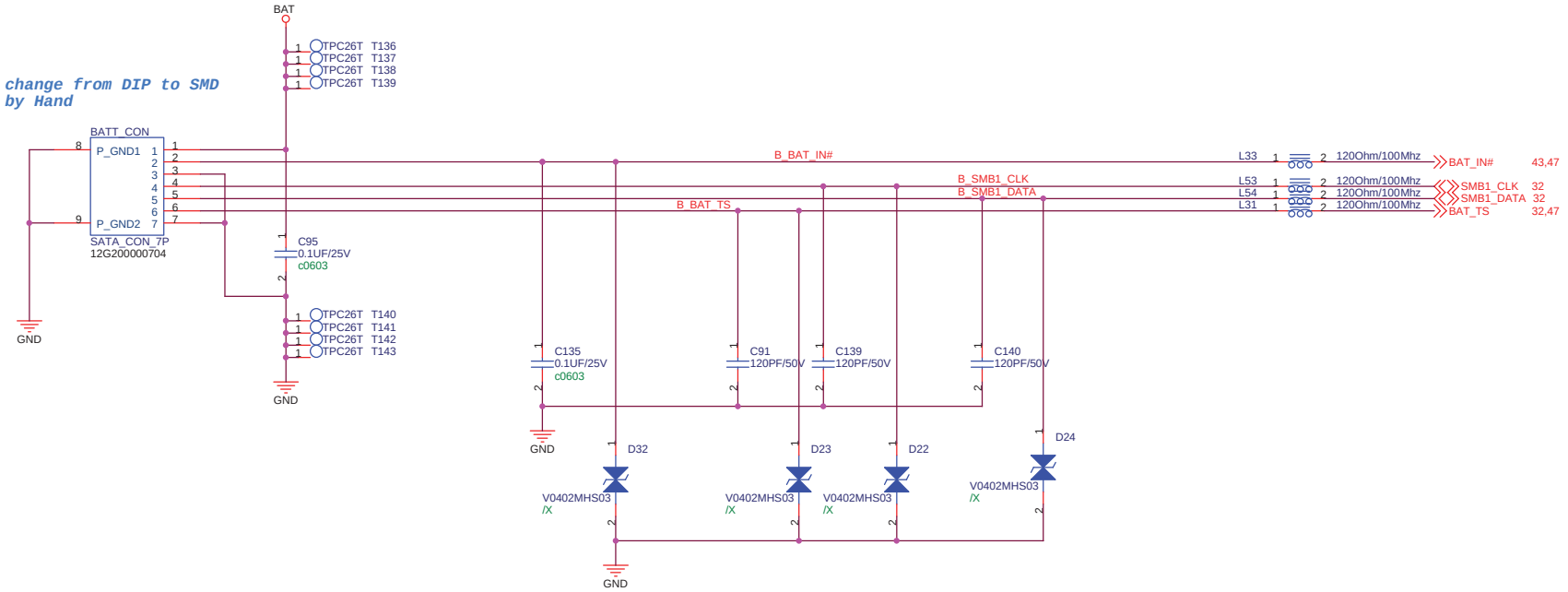
<Core Design>

ASUSTek Computer INC.	Title : LED	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 37 of 47	

DC IN

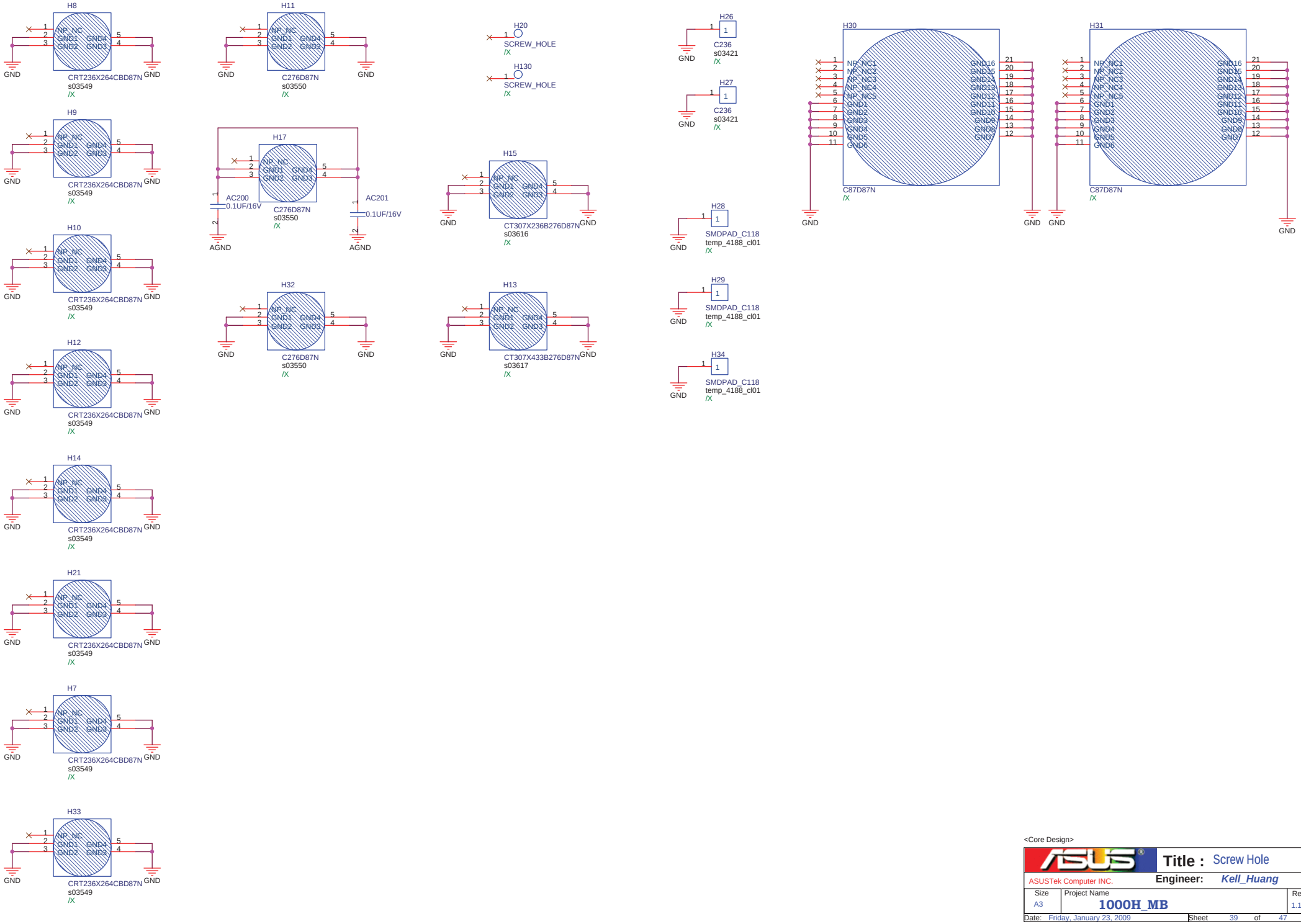


BAT IN



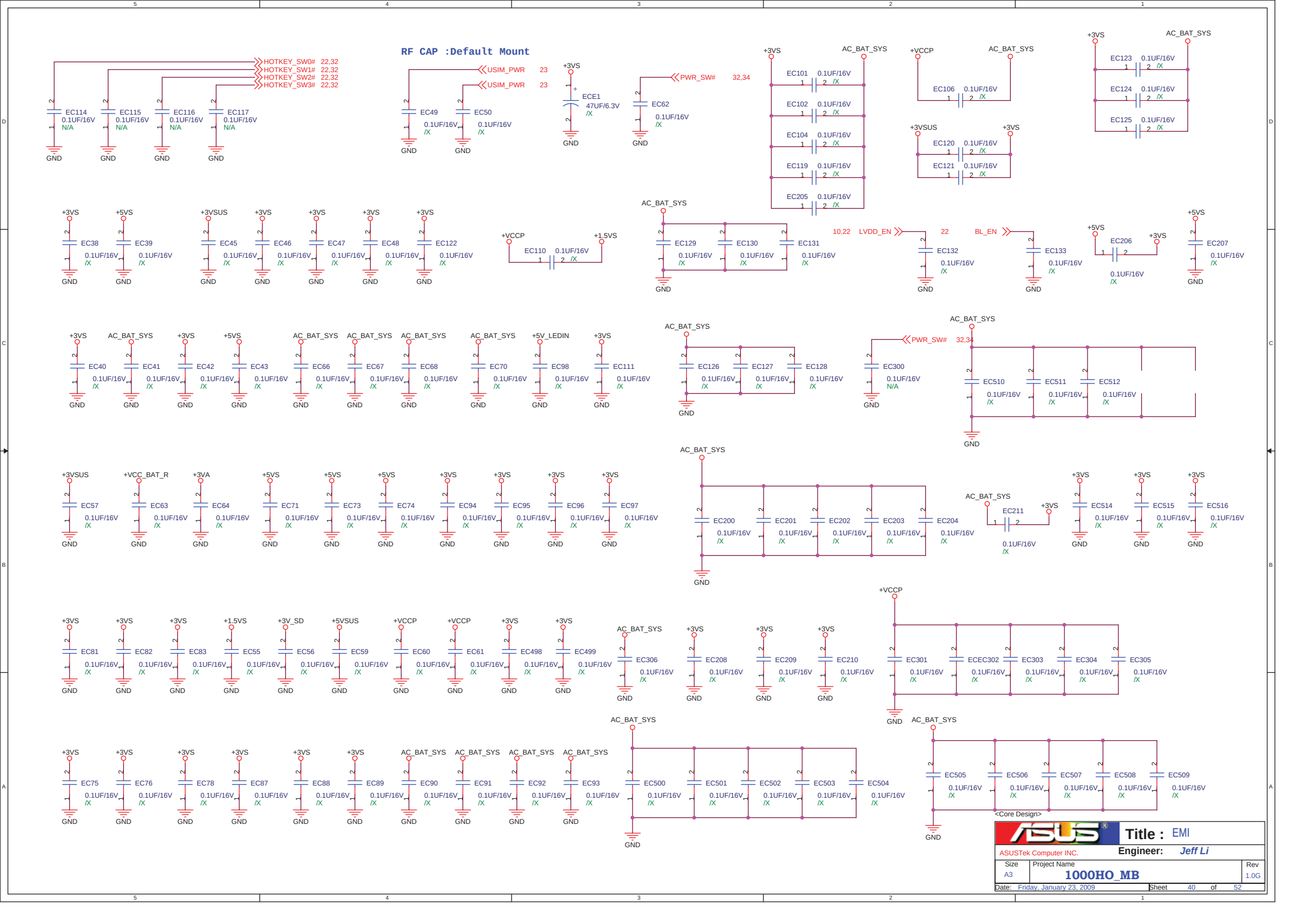
<Core Design>

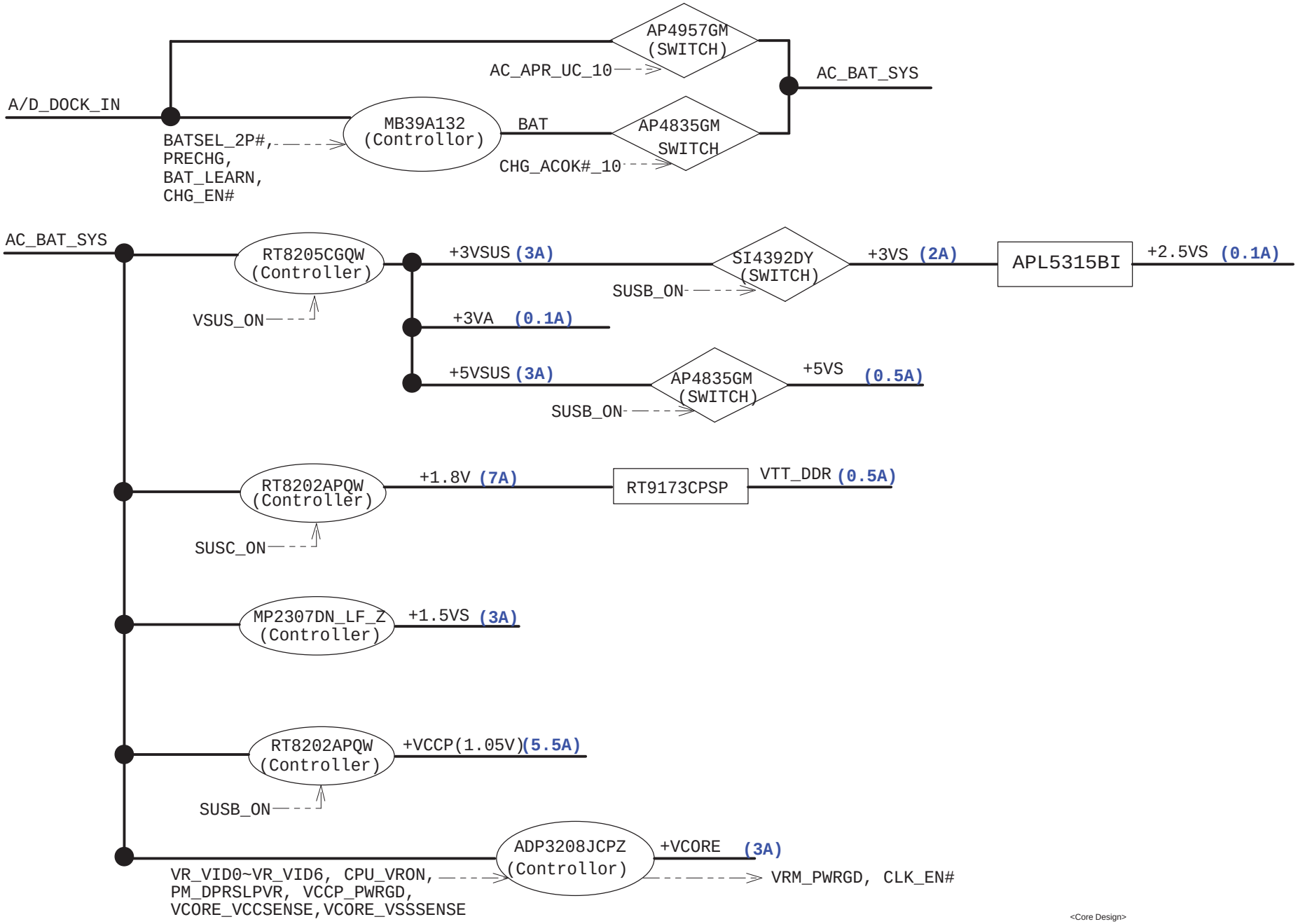
ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 38 of 52	



<Core Design>

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 39 of 47	


RF CAP :Default Mount
HOTKEY_SW0# 22,32
HOTKEY_SW1# 22,32
HOTKEY_SW2# 22,32
HOTKEY_SW3# 22,32
EC114 0.1UF/16V N/A
EC115 0.1UF/16V N/A
EC116 0.1UF/16V N/A
EC117 0.1UF/16V N/A
USIM_PWR 23
USIM_PWR 23
EC49 0.1UF/16V /X
EC50 0.1UF/16V /X
+3VS
ECE1 47UF/6.3V /X
PWR_SW# 32,34
EC62 0.1UF/16V /X
AC_BAT_SYS
EC101 0.1UF/16V /X
EC102 0.1UF/16V /X
EC104 0.1UF/16V /X
EC119 0.1UF/16V /X
EC205 0.1UF/16V /X
+VCCP
EC106 0.1UF/16V /X
+3VSUS
EC120 0.1UF/16V /X
EC121 0.1UF/16V /X
EC123 0.1UF/16V /X
EC124 0.1UF/16V /X
EC125 0.1UF/16V /X
+5VS
EC38 EC39 EC40 EC41 EC42 EC43 EC45 EC46 EC47 EC48 EC122
EC110 0.1UF/16V /X
+1.5VS
EC129 EC130 EC131
10,22 LVDD_EN
22 BL_EN
EC132 EC133
EC206
EC207
EC66 EC67 EC68 EC70 EC98 EC111
+5V_LEDIN
EC126 EC127 EC128
EC300 0.1UF/16V N/A
EC510 EC511 EC512
+VCC_BAT_R
+3VA
EC57 EC63 EC64 EC71 EC73 EC74 EC94 EC95 EC96 EC97
EC200 EC201 EC202 EC203 EC204
EC211
EC514 EC515 EC516
EC81 EC82 EC83 EC55 EC56 EC59 EC60 EC61 EC498 EC499
+1.5VS
+3V_SD
+5VSUS
EC306 EC208 EC209 EC210
EC301 ECEC302 EC303 EC304 EC305
EC75 EC76 EC78 EC87 EC88 EC89 EC90 EC91 EC92 EC93
EC500 EC501 EC502 EC503 EC504
EC505 EC506 EC507 EC508 EC509
GND
0.1UF/16V
/X
N/A
<Core Design>
Title : EMI
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 40 of 52



<Core Design>

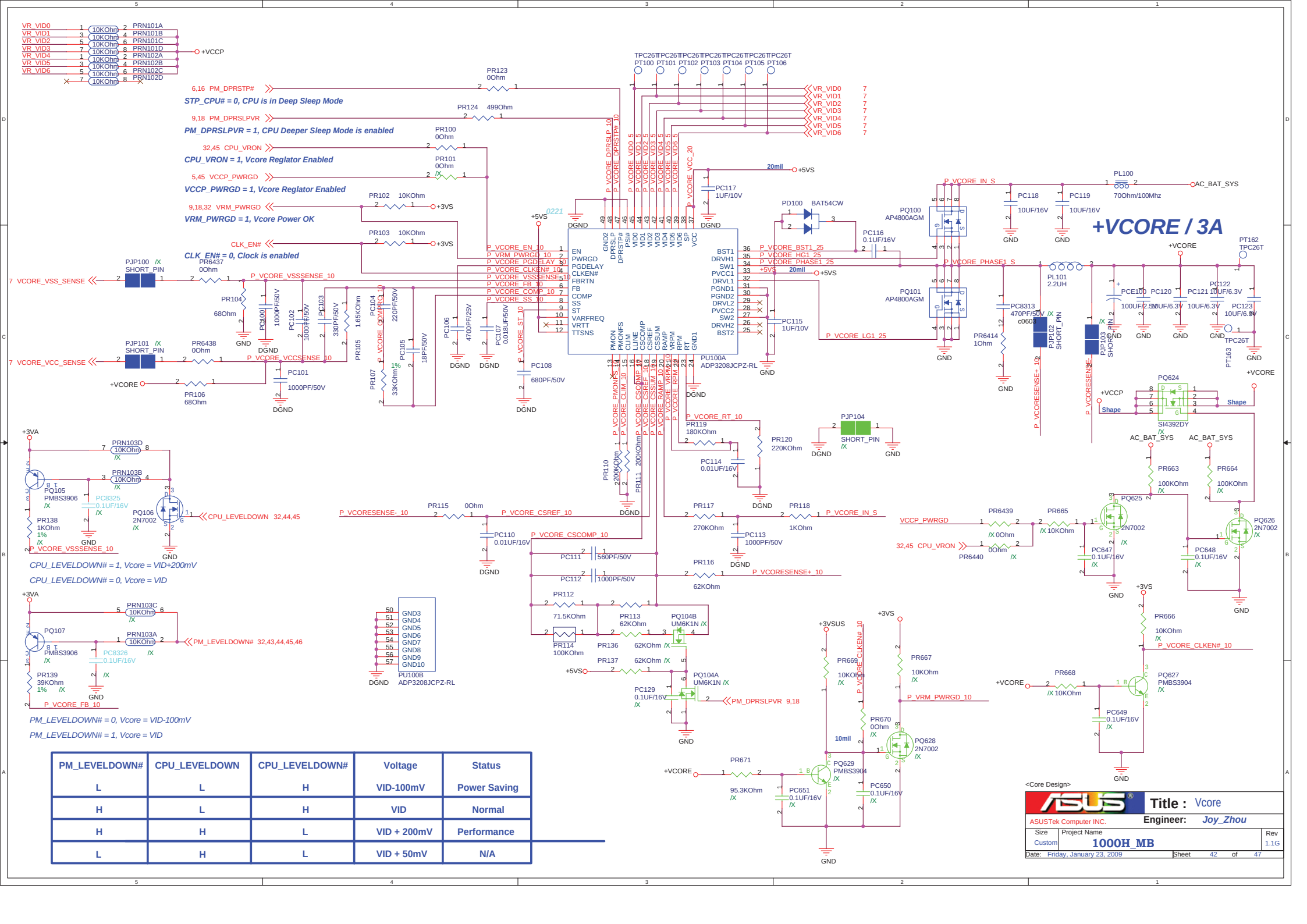
ASUSTek Computer INC.

Title : Power Flow

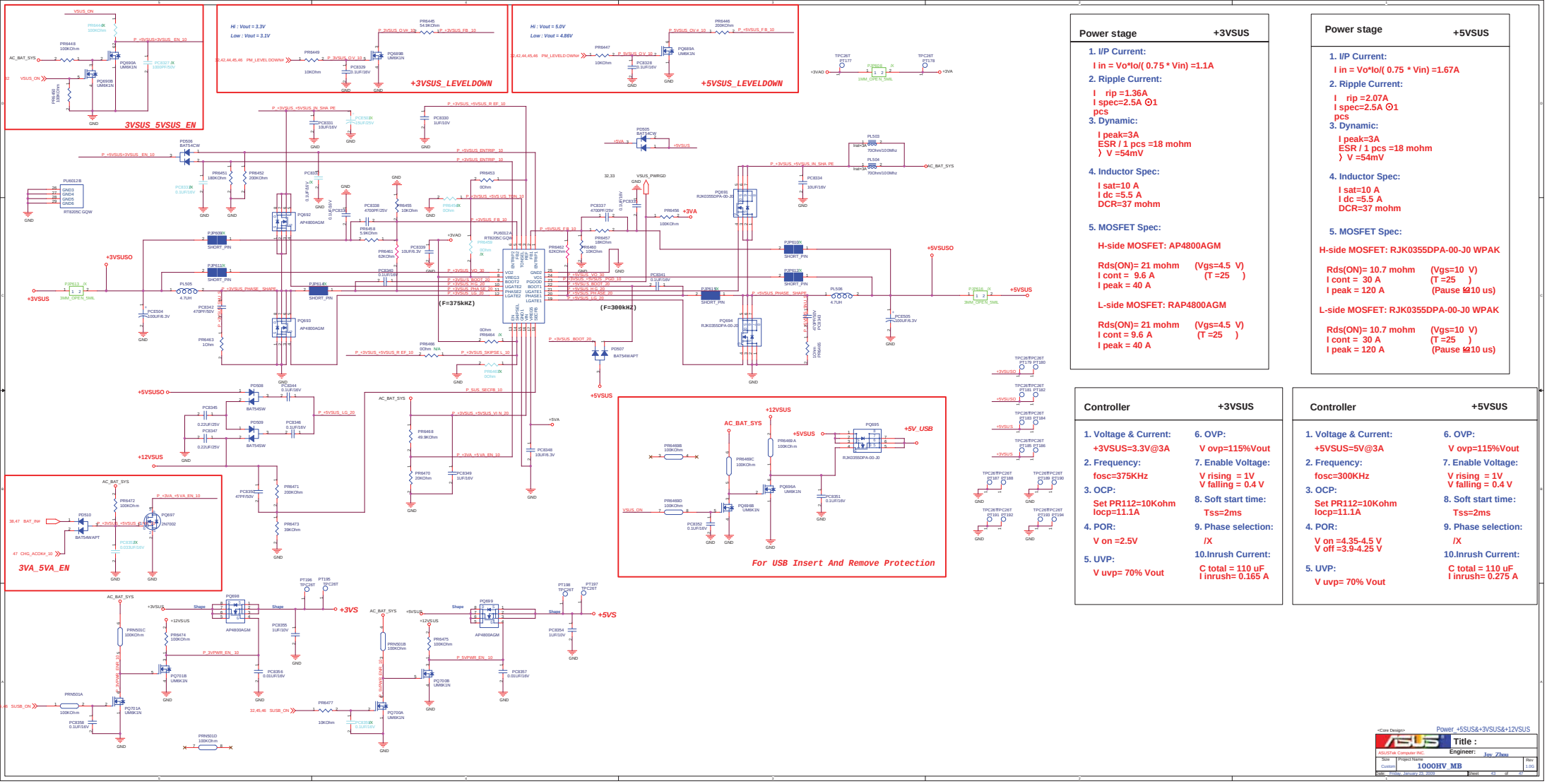
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 41 of 47



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A



Power stage +3VSUS

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.1A
2. Ripple Current:
   I rip =1.36A
   I spec=2.5A ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   〉V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:
   H-side MOSFET: AP4800AGM
   Rds(ON)= 21 mohm (Vgs=4.5 V)
   I cont = 9.6 A (T =25)
   I peak = 40 A
   L-side MOSFET: RAP4800AGM
   Rds(ON)= 21 mohm (Vgs=4.5 V)
   I cont = 9.6 A (T =25)
   I peak = 40 A

Power stage +5VSUS

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.67A
2. Ripple Current:
   I rip =2.07A
   I spec=2.5A ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   〉V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA-00-J0 WPAK
   Rds(ON)= 10.7 mohm (Vgs=10 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)
   L-side MOSFET: RJK0355DPA-00-J0 WPAK
   Rds(ON)= 10.7 mohm (Vgs=10 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

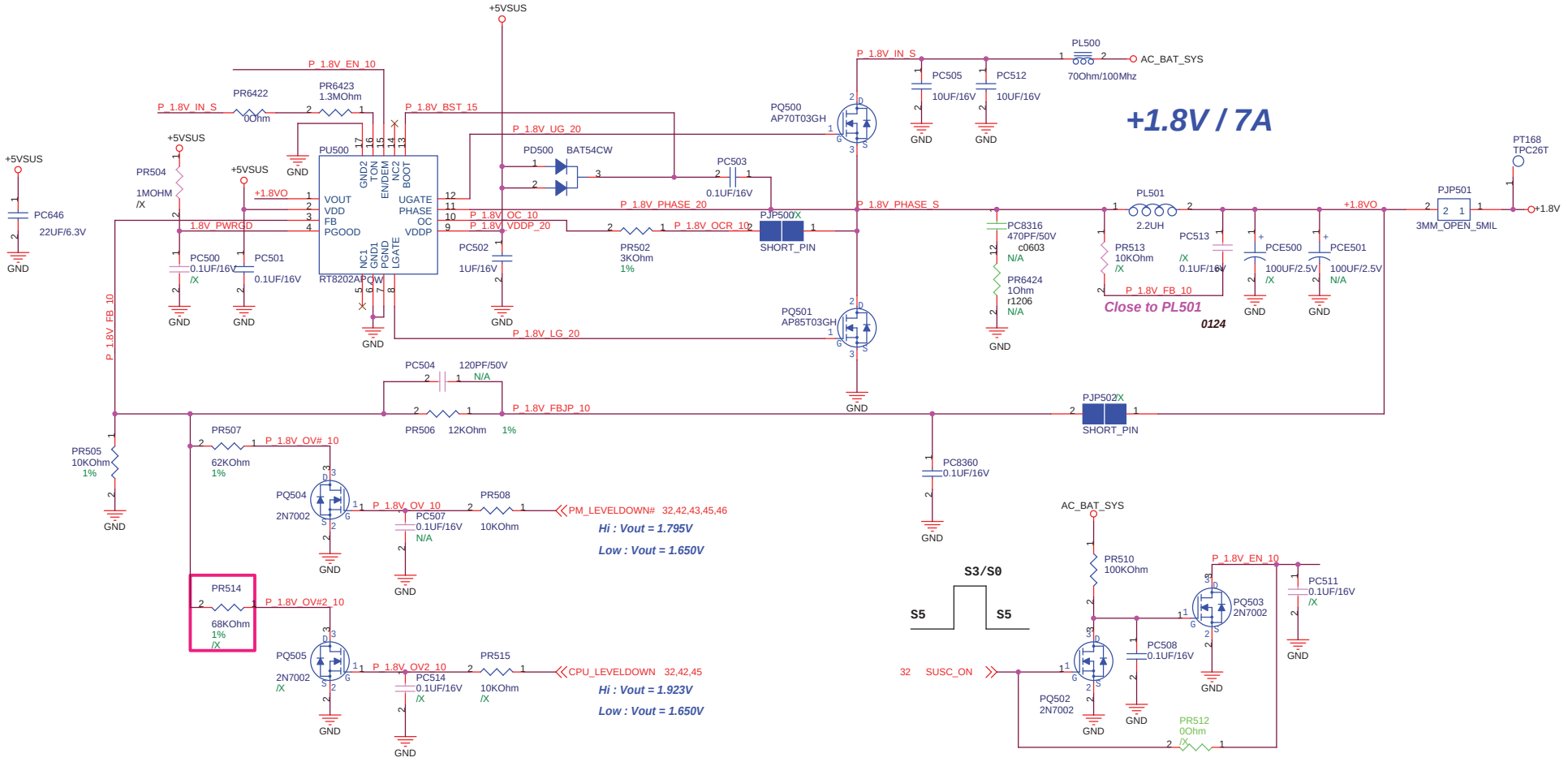
Controller +3VSUS

1. Voltage & Current:
   +3VSUS=3.3V@3A
2. Frequency:
   fosc=375KHz
3. OCP:
   Set PR112=10Kohm
   Iocp=11.1A
4. POR:
   V on =2.5V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 110 uF
    I inrush= 0.165 A

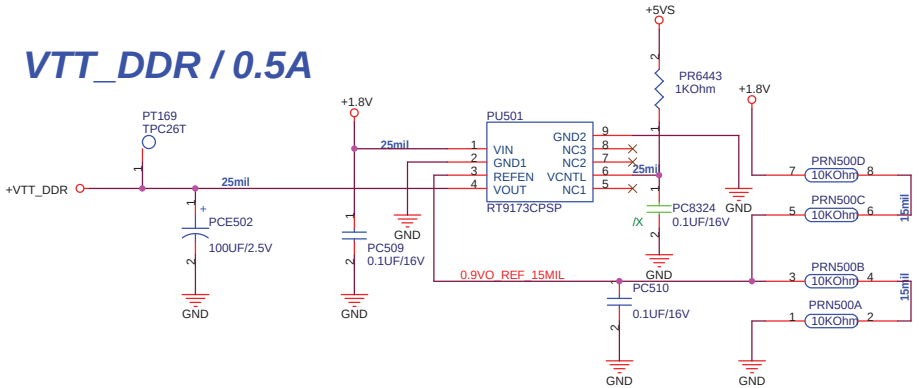
Controller +5VSUS

1. Voltage & Current:
   +5VSUS=5V@3A
2. Frequency:
   fosc=300KHz
3. OCP:
   Set PR112=10Kohm
   Iocp=11.1A
4. POR:
   V on =4.35-4.5 V
   V off =3.9-4.25 V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 110 uF
    I inrush= 0.275 A

<Core Design> Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTeK Computer INC
Engineer: Jay_Zhou
Size: Custom | Project Name: 1000HV_MB | Rev: 1.00
Date: Friday, January 22, 2010 | Sheet 33 of 47



VTT_DDR / 0.5A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

<Core Design>

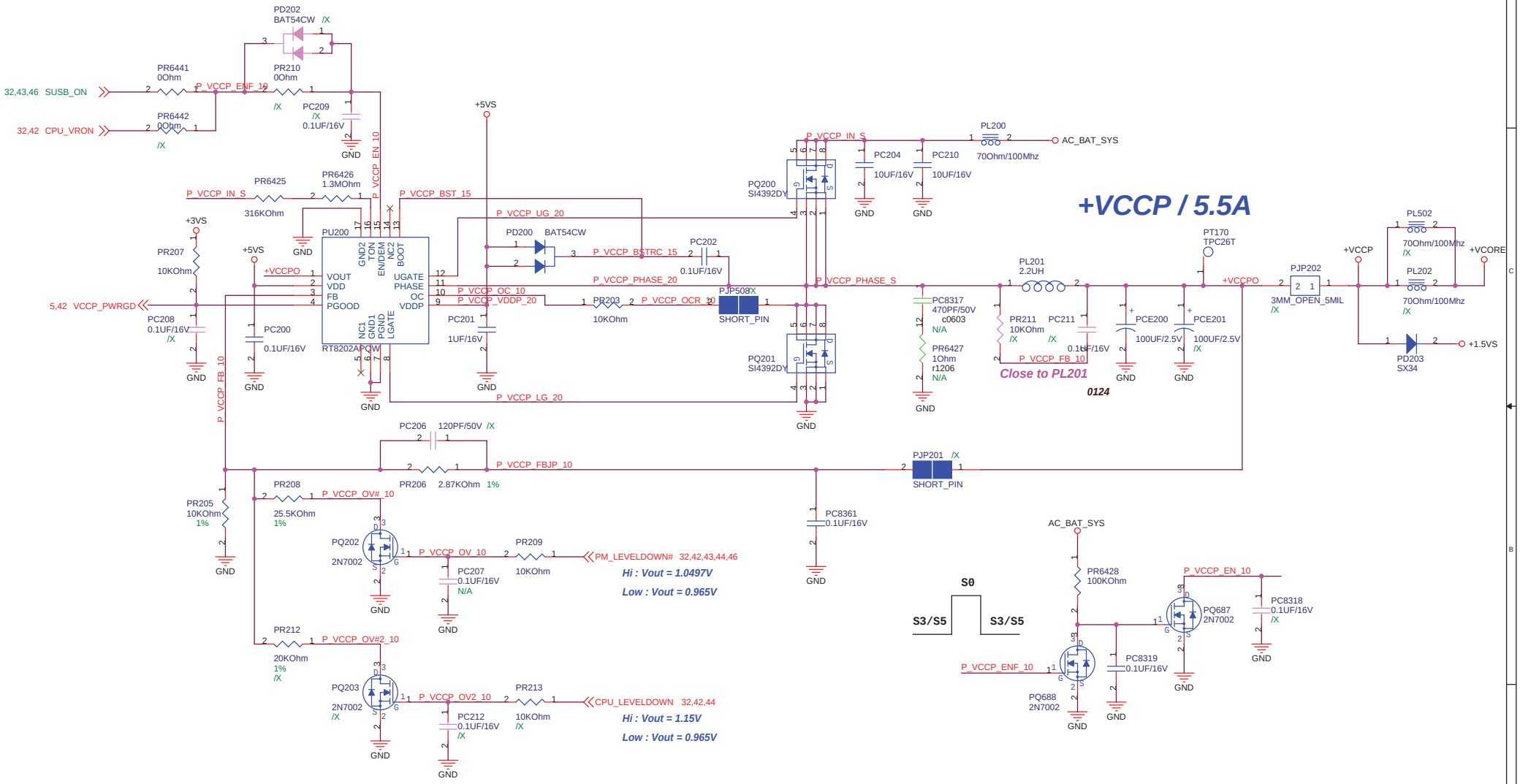
ASUSTek Computer INC.

Title : +1.8V & VTTDDR

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 44 of 47



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<Core Design>

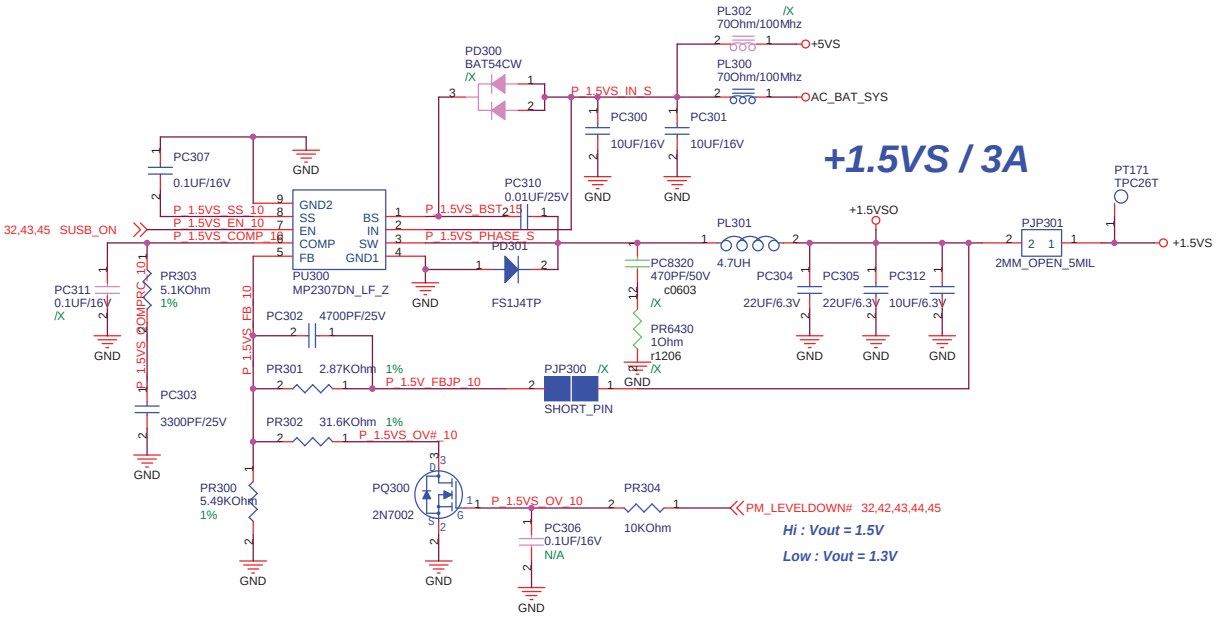
ASUSTek Computer INC.

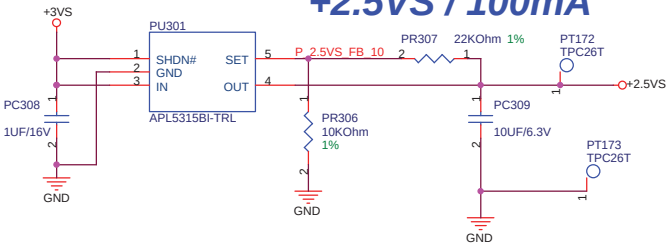
Title : VCCP

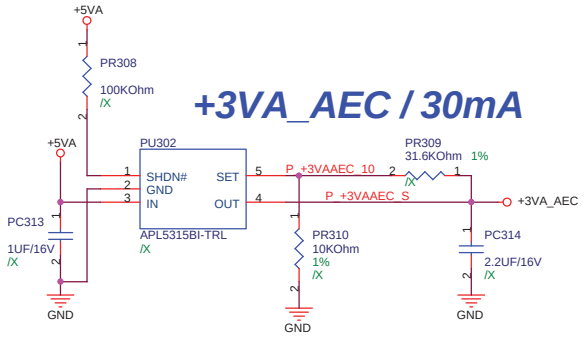
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 45 of 47

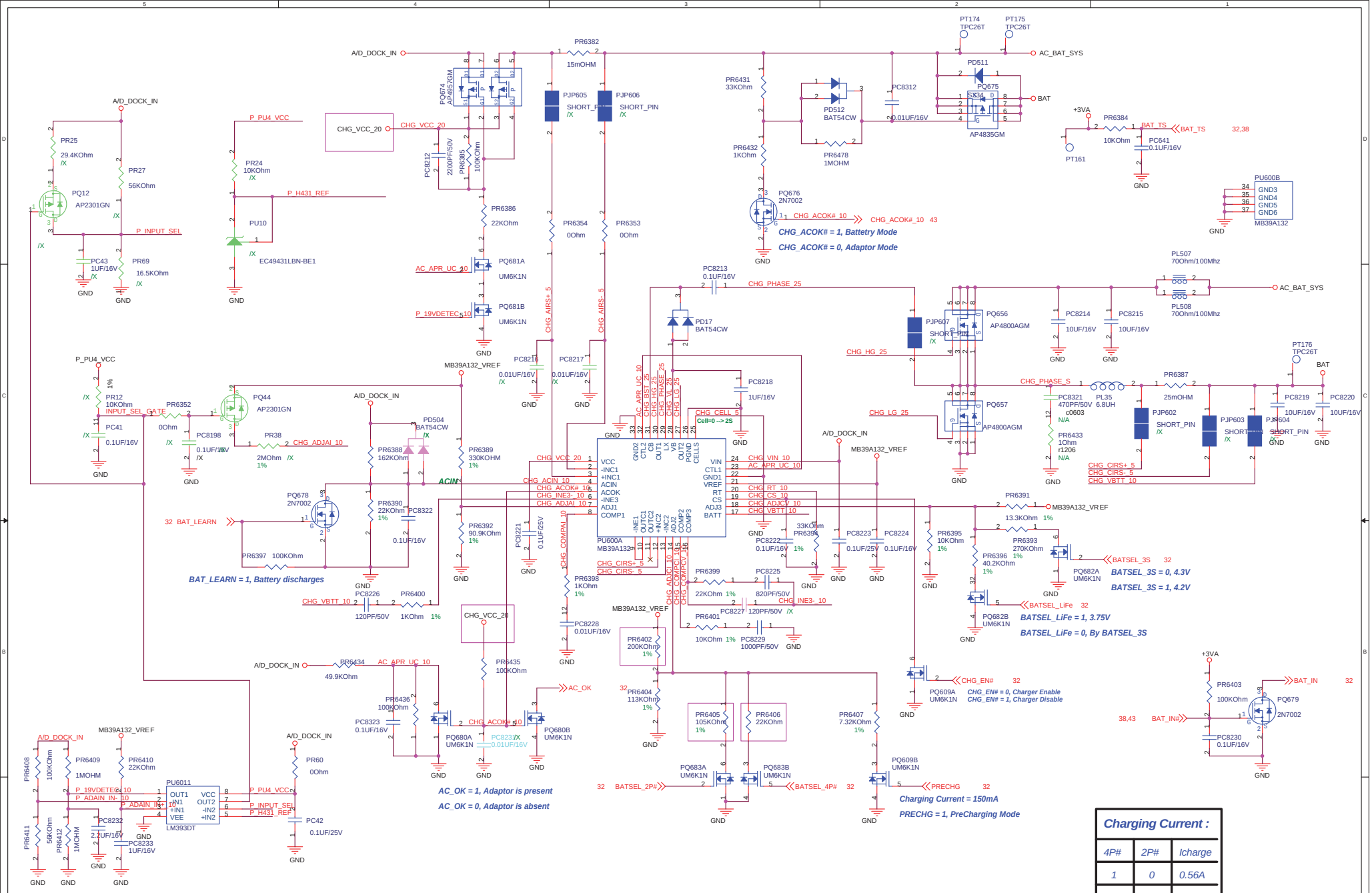






<Core Design>

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 46 of 47	



Charging Current :		
4P#	2P#	Icharge
1	0	0.56A
0	1	1.6A
0	0	2.8A

Battery Charging Voltage :
Vadj3 > 4.1V ==> Vbat = 4.2V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Charging Current :
4.4V > Vadj2 >= 0V ==>
Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)

Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV

Adaptor Max. Current :
PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)
PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)

ACIN Threshold = 1.25V
Adaptor > 8.63V, System Powered by Adaptor
Adaptor < 8.63V, System Powered by Battery

Prevent Input from 19V :
Adaptor > 13.06V, PQ603B Turn-off
Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
BAT_ID = 1, 2 Cells; Vadj2 = 0.998V
=> Icharge = 1.477A
BAT_ID = 0, 4/6 Cells; Vadj2 = 1.648V
=> Icharge = 2.517A

VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)

VTH of -IN1: 5V / 62 * (100+62) = 13.06V

VTH of ACIN: 1.25V / 25 * (185+25) = 10.5V
Change PR607 and PR608 value

<Core Design>

ASUSTek Computer INC.

Title : Charger
Engineer: Joy_Zhou
Size: Custom
Project Name: 1000H_MB
Rev: 1.1G
Date: Friday, January 23, 2009
Sheet 47 of 47

<Core Design>

ASUSTek Computer INC.	Title : Note	
	Engineer: *KingCa_Jin*	
Size: A3	Project Name: **1000HE_MB**	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 48 of 47	