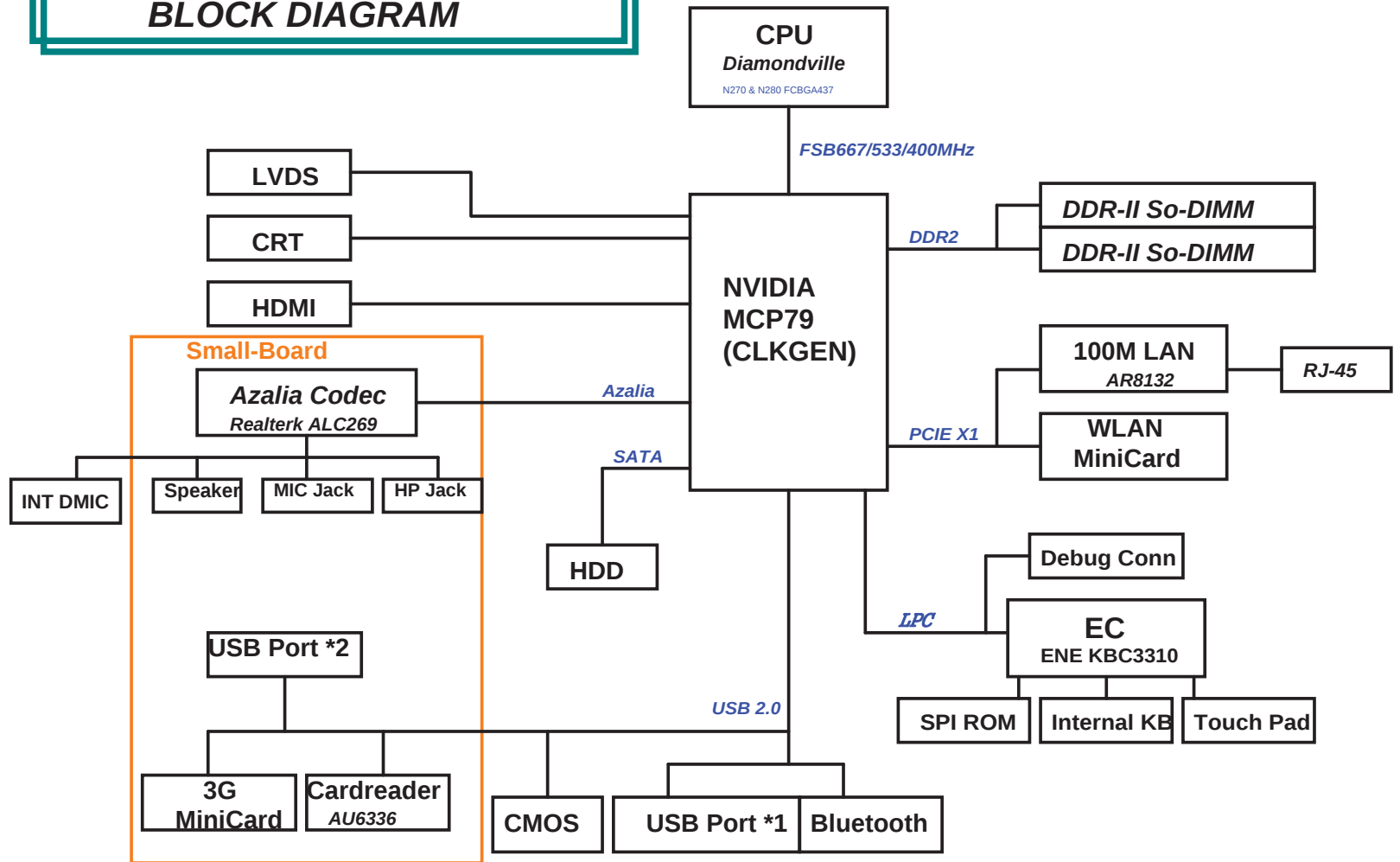


01_BLOCK DIAGRAM
02_MCP79 GPIO SETTING
03_NVIDIA MCP79--CPU (1)
04_NVIDIA MCP79--SATA&USB(9)
05_NVIDIA MCP79--MISC(10)
06_NVIDIA MCP79--HDCP&Other
07_NVIDIA MCP79--STRAP
08_CPU-Diamondville (1)
09_CPU-Diamondville (2)
10_CPU-Diamondville (3)
11_NVIDIA MCP79--DDR2 BUS (2)
12_NVIDIA MCP79--MEM CONTROL(3)
13_NVIDIA MCP79--POWER(4)
14_NVIDIA MCP79--GND(5)
15_NVIDIA MCP79--PCIE(6)
16_NVIDIA MCP79--LAN(7)
17_NVIDIA MCP79--LPC(8)
18_DDR2 SODIMM
19_DDR2 Termination
20_HDMI
21_CRT
22_LCD Conn_LID
23_3.5G
24_Mini WIFI
25_Bluetooth_BT253
26_FAN_THERMAL SENSOR
27_LAN_Atheros AR8113/AR8132
28_RJ45
29_Small brd Conn
30_EMI
31_USB Port&SATA HDD
32_EC_ENE KB3310
33_SPI ROM_Debug Conn
34_Reset Map
35_KB_Touch Pad
36_CMOS&DMIC
37_Discharge
38_PWR Jack
39_Screw Hole
40_Power Flow
41_Charger_Support JEITA
42_Power System
43_Power_1.05VSUS & VCCP
44_Power_VCORE_RT8152 Solution
45_Power_+1.8V & VTTDDR
46_Power_+1.5VS
47_Power_VDD_CORE
48_Power_Load Switch
49_Power Latch
50_BLANK
51_HISTORY
52_EC Pin Define
53_Power Sequence_DC
54_Power Sequence_AC
55_Power Sequence Description

1201I: Diamondville+MCP79 BLOCK DIAGRAM

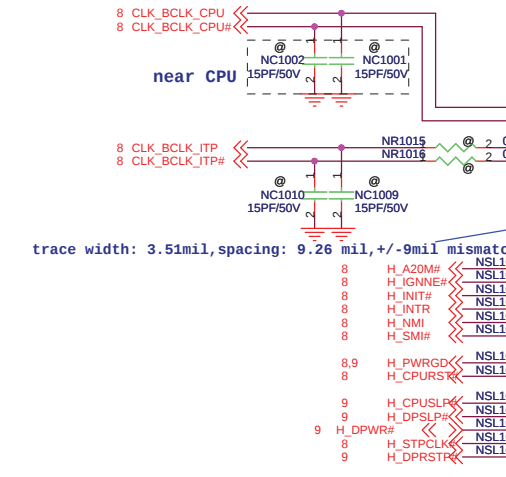
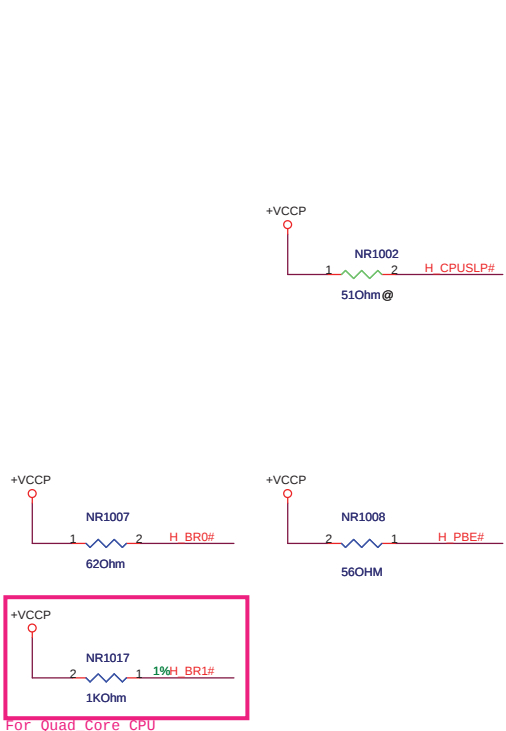


<Variant Name>

ASUS		Title : Block Diagram	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	1201I	1.0	
Date: Monday, July 20, 2009	Sheet	1	of 54

MCP79 GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N45	GPIOUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOUS3/ USBCC	+VCCP_OV0	I/O CMOS3.3	Sus	VIX-unknown	OFF	output
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	CARD_READER_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F34	GPIO2	SIMCARD_IN#	I/O CMOS3.3	Core	OFF	OFF	iutput
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

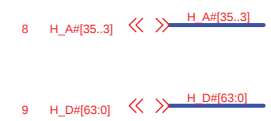


H_D#0	Y43	CPU_D0#
H_D#1	W42	CPU_D1#
H_D#2	Y40	CPU_D2#
H_D#3	W41	CPU_D3#
H_D#4	Y39	CPU_D4#
H_D#5	W42	CPU_D5#
H_D#6	Y41	CPU_D6#
H_D#7	Y42	CPU_D7#
H_D#8	P42	CPU_D8#
H_D#9	U41	CPU_D9#
H_D#10	R42	CPU_D10#
H_D#11	T39	CPU_D11#
H_D#12	T42	CPU_D12#
H_D#13	T41	CPU_D13#
H_D#14	R41	CPU_D14#
H_D#15	T43	CPU_D15#
H_D#16	W35	CPU_D16#
H_D#17	AA37	CPU_D17#
H_D#18	W33	CPU_D18#
H_D#19	W34	CPU_D19#
H_D#20	AA36	CPU_D20#
H_D#21	AA34	CPU_D21#
H_D#22	AA38	CPU_D22#
H_D#23	AA35	CPU_D23#
H_D#24	U38	CPU_D24#
H_D#25	U36	CPU_D25#
H_D#26	U35	CPU_D26#
H_D#27	U33	CPU_D27#
H_D#28	U34	CPU_D28#
H_D#29	W38	CPU_D29#
H_D#30	R33	CPU_D30#
H_D#31	U37	CPU_D31#
H_D#32	N34	CPU_D32#
H_D#33	N33	CPU_D33#
H_D#34	R34	CPU_D34#
H_D#35	R35	CPU_D35#
H_D#36	P35	CPU_D36#
H_D#37	R39	CPU_D37#
H_D#38	R37	CPU_D38#
H_D#39	R38	CPU_D39#
H_D#40	L37	CPU_D40#
H_D#41	L39	CPU_D41#
H_D#42	L38	CPU_D42#
H_D#43	N36	CPU_D43#
H_D#44	N38	CPU_D44#
H_D#45	J39	CPU_D45#
H_D#46	J38	CPU_D46#
H_D#47	J37	CPU_D47#
H_D#48	L42	CPU_D48#
H_D#49	M42	CPU_D49#
H_D#50	P41	CPU_D50#
H_D#51	N41	CPU_D51#
H_D#52	N40	CPU_D52#
H_D#53	M40	CPU_D53#
H_D#54	K42	CPU_D54#
H_D#55	K42	CPU_D55#
H_D#56	H41	CPU_D56#
H_D#57	L41	CPU_D57#
H_D#58	H43	CPU_D58#
H_D#59	H42	CPU_D59#
H_D#60	K41	CPU_D60#
H_D#61	J40	CPU_D61#
H_D#62	H39	CPU_D62#
H_D#63	M43	CPU_D63#
H_BPR1#	AA41	CPU_BPR1#
H_DEFER#	AA40	CPU_DEFER#
BCLK_OUT_CPU_P	G42	BCLK_OUT_CPU_P
BCLK_OUT_CPU_N	G41	BCLK_OUT_CPU_N
BCLK_OUT_XDP_P	AL43	BCLK_OUT_XDP_P
BCLK_OUT_XDP_N	AL42	BCLK_OUT_XDP_N
BCLK_OUT_ITP_P	AL41	BCLK_OUT_ITP_P
BCLK_OUT_ITP_N	AK42	BCLK_OUT_ITP_N
BCLK_OUT_NB_P	AK41	BCLK_OUT_NB_P
BCLK_OUT_NB_N	AJ40	BCLK_OUT_NB_N
BCLK_IN_N	AJ40	BCLK_IN_N
BCLK_IN_P	AJ40	BCLK_IN_P
CPU_A20M#	AF41	CPU_A20M#
CPU_IGNNE#	AH39	CPU_IGNNE#
CPU_INIT#	AH42	CPU_INIT#
CPU_INTR#	AE42	CPU_INTR#
CPU_NMI	AG41	CPU_NMI
CPU_SMI#	AH41	CPU_SMI#
CPU_PWRGD	AH43	CPU_PWRGD
CPU_RST#	H38	CPU_RST#
CPU_SLP#	AM33	CPU_SLP#
CPU_DPSLP#	AN33	CPU_DPSLP#
CPU_DPWR#	AM32	CPU_DPWR#
CPU_STPCLK#	AG42	CPU_STPCLK#
CPU_DPRSTP#	AN32	CPU_DPRSTP#

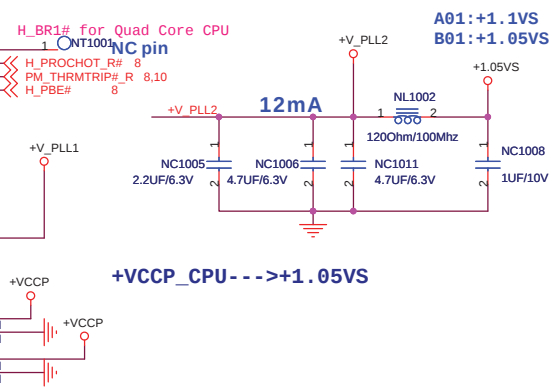
SEC
1 OF 11

FSB

CPU_D0#	T40	H_DSTBP#0	9
CPU_D1#	U40	H_DSTBN#0	9
CPU_D2#	V41	H_DIN#0	9
CPU_D3#	W39	H_DSTBP#1	9
CPU_D4#	W37	H_DSTBN#1	9
CPU_D5#	W35	H_DIN#1	9
CPU_D6#	N37	H_DSTBP#2	9
CPU_D7#	L36	H_DSTBN#2	9
CPU_D8#	N35	H_DIN#2	9
CPU_D9#	M39	H_DSTBP#3	9
CPU_D10#	M41	H_DSTBN#3	9
CPU_D11#	J41	H_DIN#3	9
CPU_D12#	AC34	H_A#3	
CPU_D13#	AE38	H_A#4	
CPU_D14#	AE34	H_A#5	
CPU_D15#	AC37	H_A#6	
CPU_D16#	AE37	H_A#7	
CPU_D17#	AE35	H_A#8	
CPU_D18#	AB35	H_A#9	
CPU_D19#	AF35	H_A#10	
CPU_D20#	AG35	H_A#11	
CPU_D21#	AG39	H_A#12	
CPU_D22#	AE33	H_A#13	
CPU_D23#	AG37	H_A#14	
CPU_D24#	AG38	H_A#15	
CPU_D25#	AG34	H_A#16	
CPU_D26#	AN38	H_A#17	
CPU_D27#	AL39	H_A#18	
CPU_D28#	AG33	H_A#19	
CPU_D29#	AL33	H_A#20	
CPU_D30#	AL33	H_A#21	
CPU_D31#	AN36	H_A#22	
CPU_D32#	AJ35	H_A#23	
CPU_D33#	AJ37	H_A#24	
CPU_D34#	AJ36	H_A#25	
CPU_D35#	AJ38	H_A#26	
CPU_D36#	AL37	H_A#27	
CPU_D37#	AL34	H_A#28	
CPU_D38#	AN37	H_A#29	
CPU_D39#	AJ34	H_A#30	
CPU_D40#	AL38	H_A#31	
CPU_D41#	AL35	H_A#32	
CPU_D42#	AN34	H_A#33	
CPU_D43#	AR39	H_A#34	
CPU_D44#	AN35	H_A#35	
CPU_ADSTB#0	AE36	H_ADSTB#0	8
CPU_ADSTB#1	AK35	H_ADSTB#1	8
CPU_REQ#0	AC38	H_REQ#0	8
CPU_REQ#1	AA33	H_REQ#1	8
CPU_REQ#2	AC39	H_REQ#2	8
CPU_REQ#3	AC33	H_REQ#3	8
CPU_REQ#4	AC35	H_REQ#4	8
CPU_ADS#	AD42	H_ADS#	8
CPU_BNR#	AD43	H_BNR#	8
CPU_BR0#	AE40	H_BR0#	8
CPU_DBSY#	AD39	H_DBSY#	8
CPU_DRDY#	AD41	H_DRDY#	8
CPU_HIT#	AD42	H_HIT#	8
CPU_HITM#	AD40	H_HITM#	8
CPU_LOCK#	AC43	H_LOCK#	8
CPU_TRDY#	AE41	H_TRDY#	8
CPU_BR1#	E41	H_BR1#	
CPU_PROCHOT#	AJ41	H_PROCHOT_R#	8
CPU_THERMTRIP#	AG43	PM_THRMTRIP#	8,10
CPU_FERR#	AH40	H_FERR#	8
CPU_BSEL2	F42	MCH_BSEL2	9
CPU_BSEL1	D42	MCH_BSEL1	9
CPU_BSEL0	F41	MCH_BSEL0	9
CPU_RS#0	AC41	H_RS#0	8
CPU_RS#1	AB41	H_RS#1	8
CPU_RS#2	AC42	H_RS#2	8
V_PLL_CPU	AH28	+V_PLL2	
V_PLL_DP	U28	+V_PLL2	
BCLK_VML_COMP_VDD	AM39	BCLK_VML_COMP_VDD	1
BCLK_VML_COMP_GND	AM40	BCLK_VML_COMP_GND	1
CPU_COMP_VCC	AM43	CPU_COMP_VCC	1
CPU_COMP_GND	AM42	CPU_COMP_GND	1



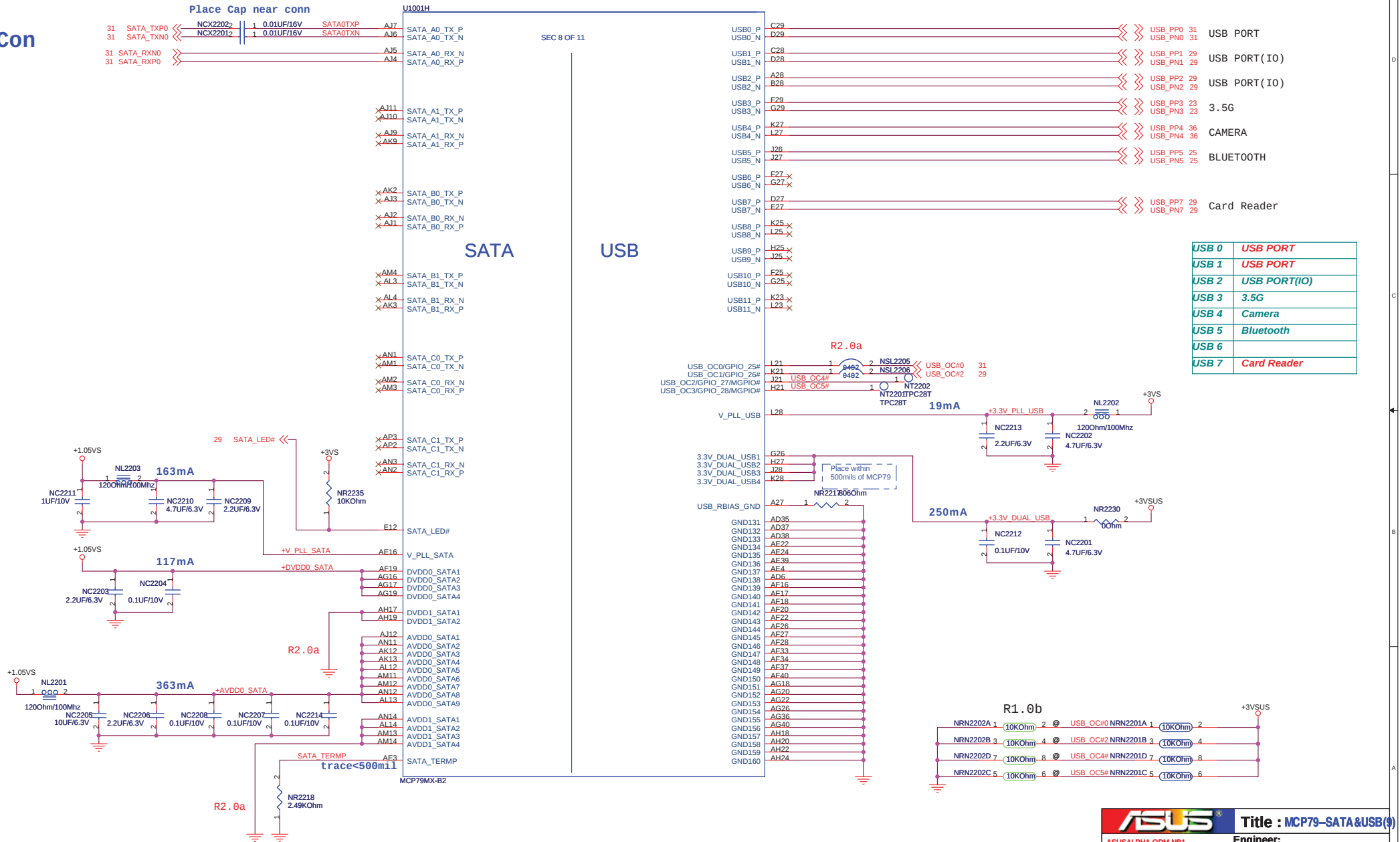
REF:DA-03658-001_V01
A01:+1.1VS
B01:+1.05VS



R2.0a

MCP79MX-B2
026190014901

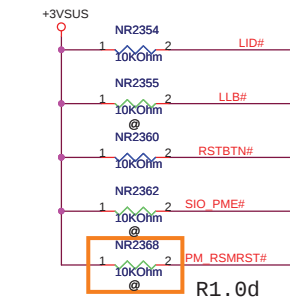
HDD Con



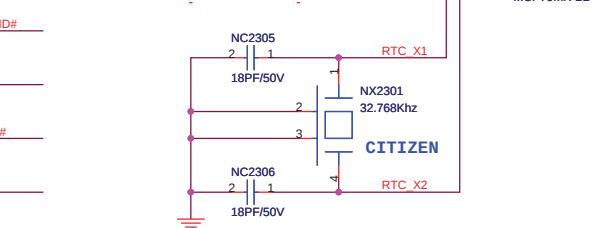
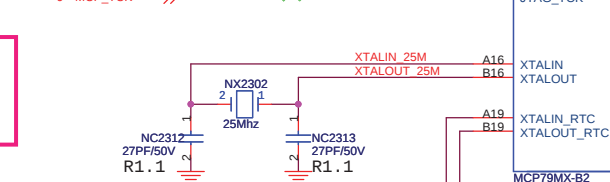
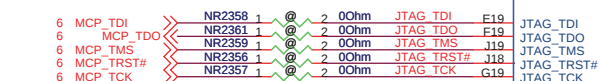
USB 0	USB PORT
USB 1	USB PORT
USB 2	USB PORT(IO)
USB 3	3.5G
USB 4	Camera
USB 5	Bluetooth
USB 6	
USB 7	Card Reader

FROM PWR PWM PG

DEL JTAG_TDI/JTAG_TMS
for MCP79 internal
pull up to +3VS.



R1.0d



M90 0925 FROM F80S
Check OK

WT0B_CON_2P
N/A
SMD
12G17100002C

HDA



SEC 9 OF 11

GPIO_1/PWRDN_OK/SPI_CS1

GPIO_12/SUS_STAT/ACCLMTR_EXT_RIG#

A20GATE

KBRDRSTIN#

SIO_PME#

EXT_SMI/GPIO_32#

INTRUDER#

LID#

LLB#

CPU_DPRSLPVR

PWRBTN#

RSTBTN#

RTCRST#

PWRGD_SB

PS_PWRGD

CPU_VLD

CPUVDD_EN

SUS_CLK

SUS_CLK/GPIO_34

BUF_SIO_CLK

TEST_MODE_EN

PKG_TEST

MCP79MX-B2

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

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1: 24MHz

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0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

MISC

GPIO_1/PWRDN_OK/SPI_CS1

GPIO_12/SUS_STAT/ACCLMTR_EXT_RIG#

A20GATE

KBRDRSTIN#

SIO_PME#

EXT_SMI/GPIO_32#

INTRUDER#

LID#

LLB#

CPU_DPRSLPVR

PWRBTN#

RSTBTN#

RTCRST#

PWRGD_SB

PS_PWRGD

CPU_VLD

CPUVDD_EN

SUS_CLK

SUS_CLK/GPIO_34

BUF_SIO_CLK

TEST_MODE_EN

PKG_TEST

MCP79MX-B2

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

V_DUAL_HDA1

V_DUAL_HDA2

HDA_SYNC

HDA_DOCK_EN/GPIO_4/PS2_MS_CLK#

HDA_DOCK_RST/GPIO_5/PS2_MS_DATA#

SMB_CLK0

SMB_DATA0

SMB_CLK1/MSMB_CLK

SMB_DATA1/MSMB_DATA

SMB_ALERT/GPIO_64#

FANRPM0/GPIO_60

FANCTLO/GPIO_61

FANRPM1/GPIO_63

FANCTLI/GPIO_62

CPUVDD_EN

SUS_CLK

SUS_CLK/GPIO_34

BUF_SIO_CLK

TEST_MODE_EN

PKG_TEST

MCP79MX-B2

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

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1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

V_DUAL_HDA1

V_DUAL_HDA2

HDA_SYNC

HDA_DOCK_EN/GPIO_4/PS2_MS_CLK#

HDA_DOCK_RST/GPIO_5/PS2_MS_DATA#

SMB_CLK0

SMB_DATA0

SMB_CLK1/MSMB_CLK

SMB_DATA1/MSMB_DATA

SMB_ALERT/GPIO_64#

FANRPM0/GPIO_60

FANCTLO/GPIO_61

FANRPM1/GPIO_63

FANCTLI/GPIO_62

CPUVDD_EN

SUS_CLK

SUS_CLK/GPIO_34

BUF_SIO_CLK

TEST_MODE_EN

PKG_TEST

MCP79MX-B2

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

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0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

V_DUAL_HDA1

V_DUAL_HDA2

HDA_SYNC

HDA_DOCK_EN/GPIO_4/PS2_MS_CLK#

HDA_DOCK_RST/GPIO_5/PS2_MS_DATA#

SMB_CLK0

SMB_DATA0

SMB_CLK1/MSMB_CLK

SMB_DATA1/MSMB_DATA

SMB_ALERT/GPIO_64#

FANRPM0/GPIO_60

FANCTLO/GPIO_61

FANRPM1/GPIO_63

FANCTLI/GPIO_62

CPUVDD_EN

SUS_CLK

SUS_CLK/GPIO_34

BUF_SIO_CLK

TEST_MODE_EN

PKG_TEST

MCP79MX-B2

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

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0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

0: 14.318MHz

1: 24MHz

V_DUAL_HDA1

V_DUAL_HDA2

HDA_SYNC

HDA_DOCK_EN/GPIO_4/PS2_MS_CLK#

HDA_DOCK_RST/GPIO_5/PS2_MS_DATA#

SMB_CLK0

SMB_DATA0

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

MCP79

MEMORY

SYSTEM

R1.15

JTAG INTERFACE

R1.0d

HDCP ROM

WP=1 Write Protect
WP=0 Normal

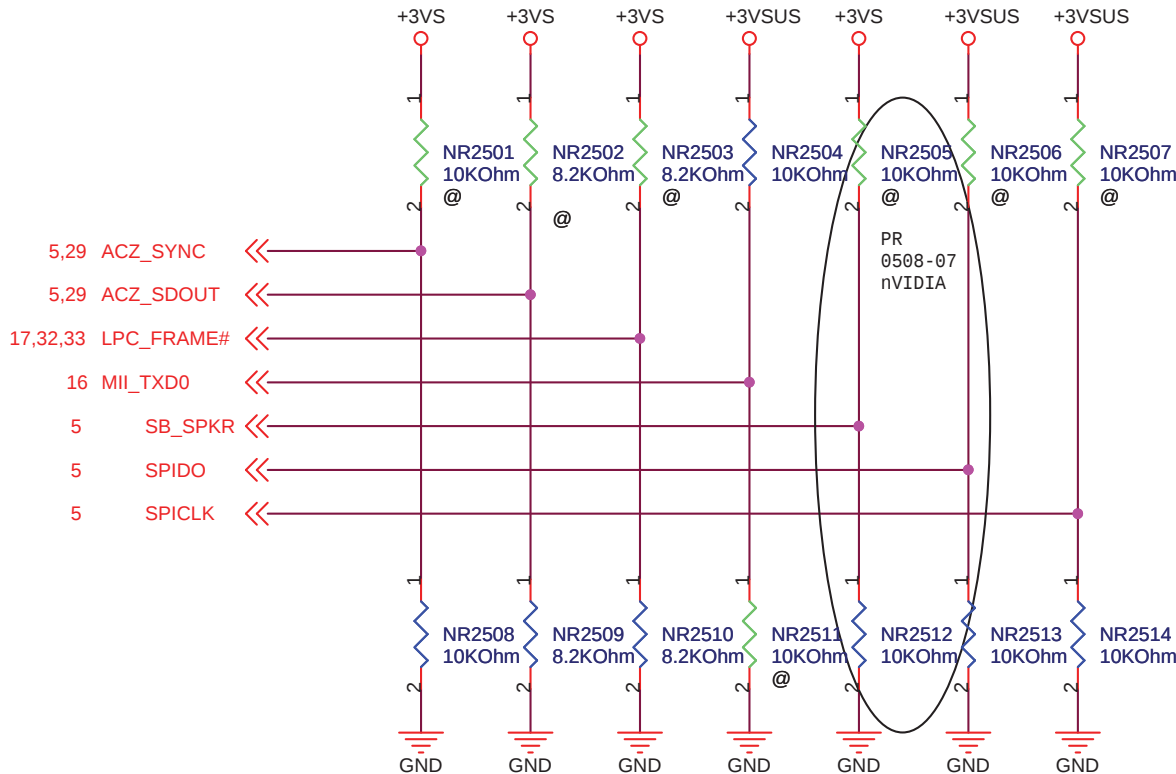
HDA_SYNC STRAP (BUF_SIO_CLK)	
0	14.318MHz (default)
1	24MHz

RGMII_TXD0	
0	MII
1	RGMII

SPKR	
0	User mode boot Init table
1	Safe mode boot Init table

Base on EC		
HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_D0	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz

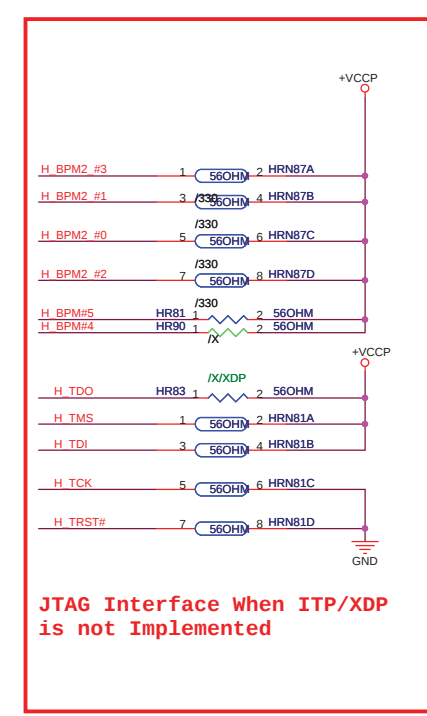
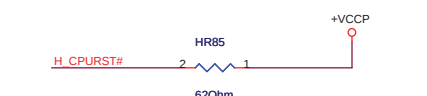
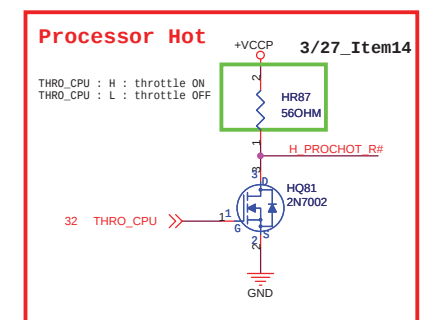
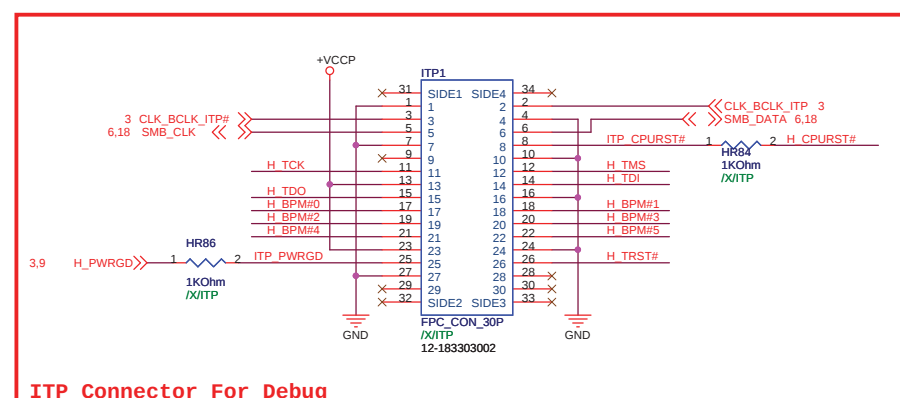
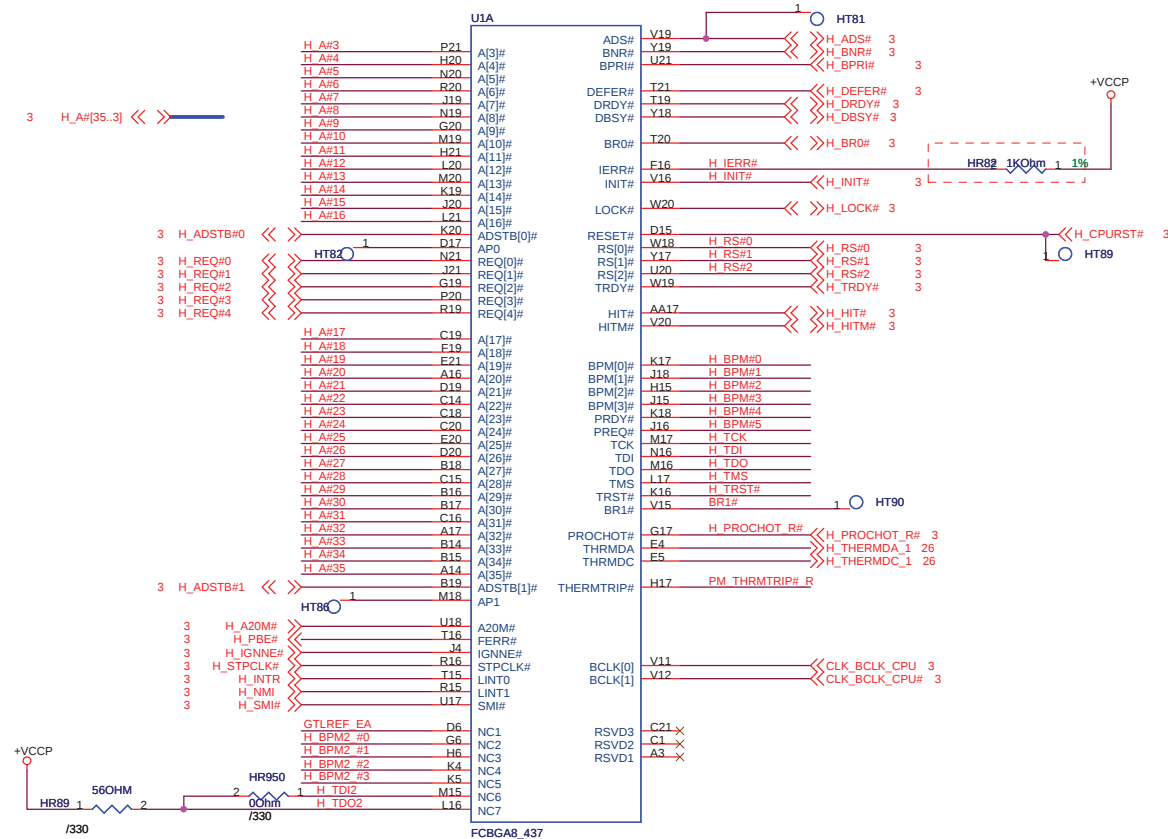
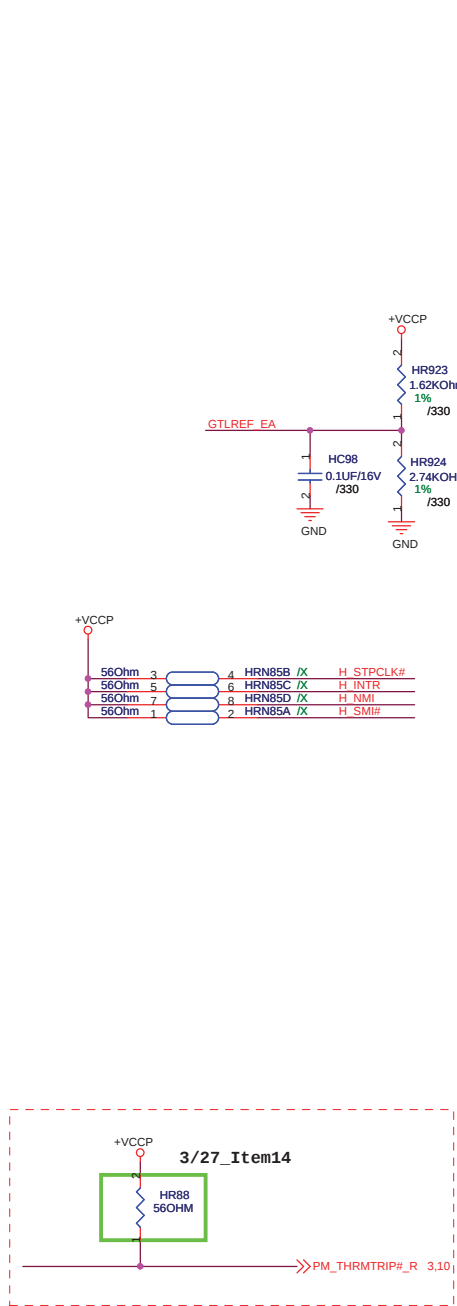


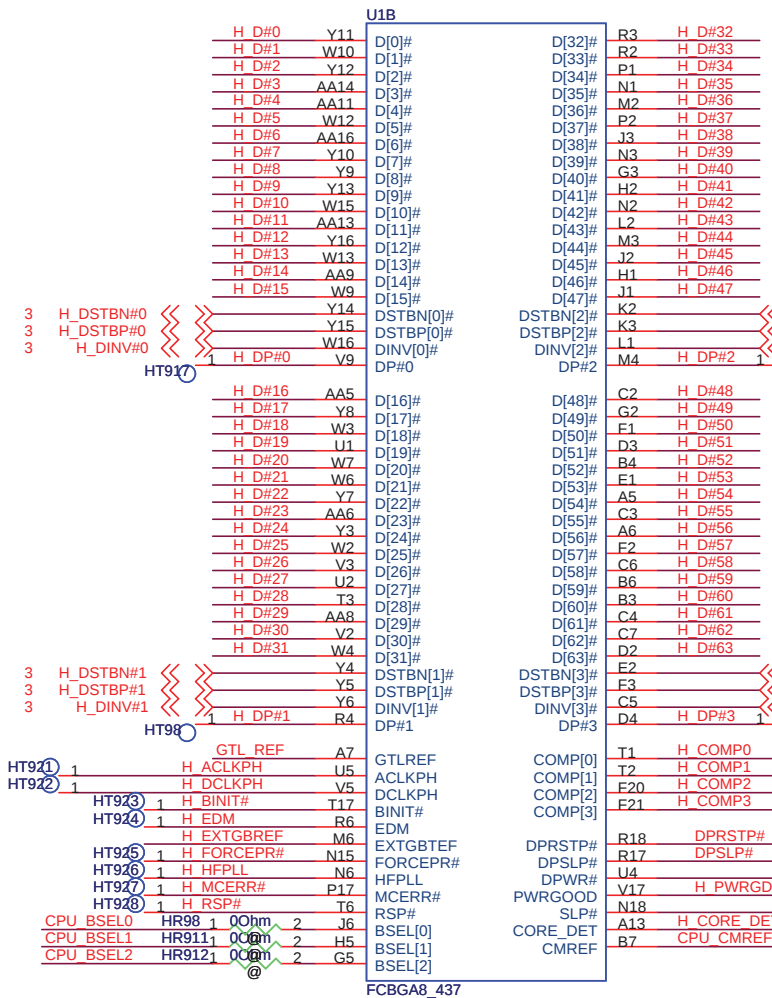
**Title : MCP79 STRAP**

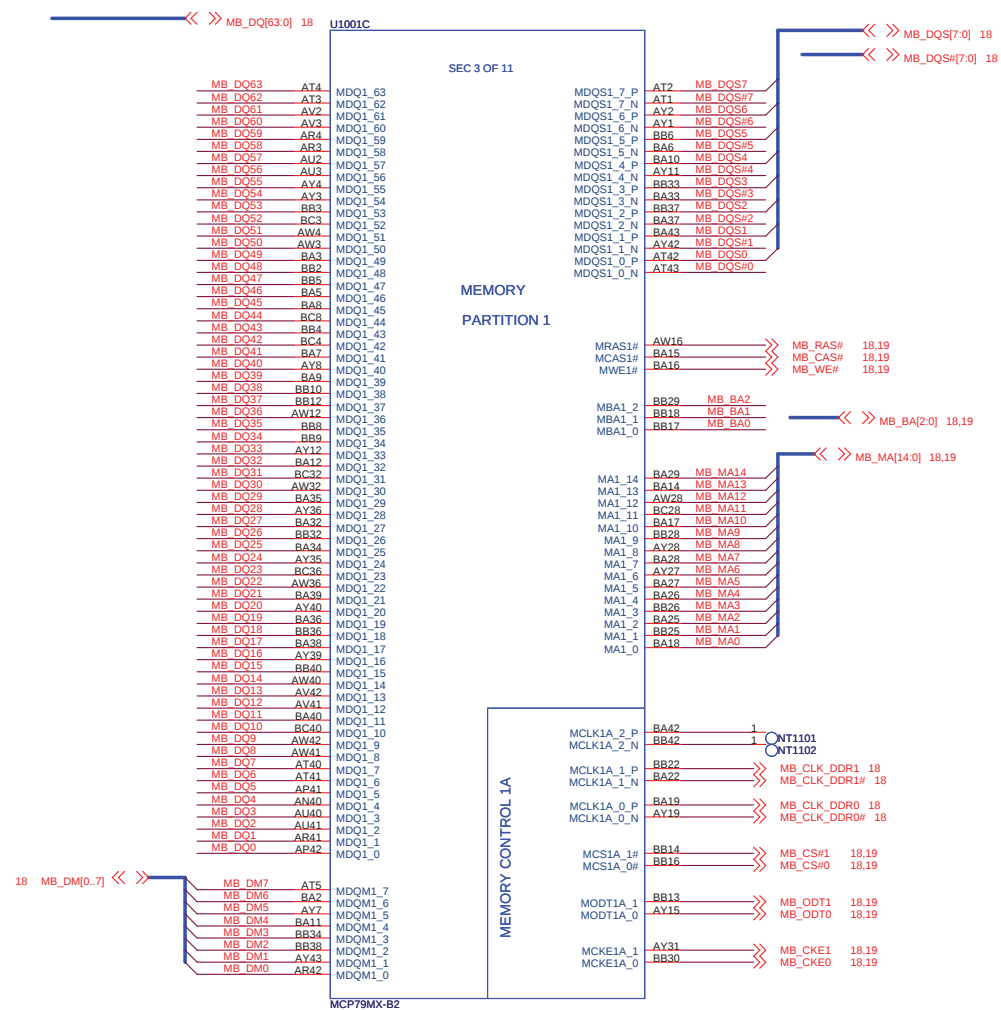
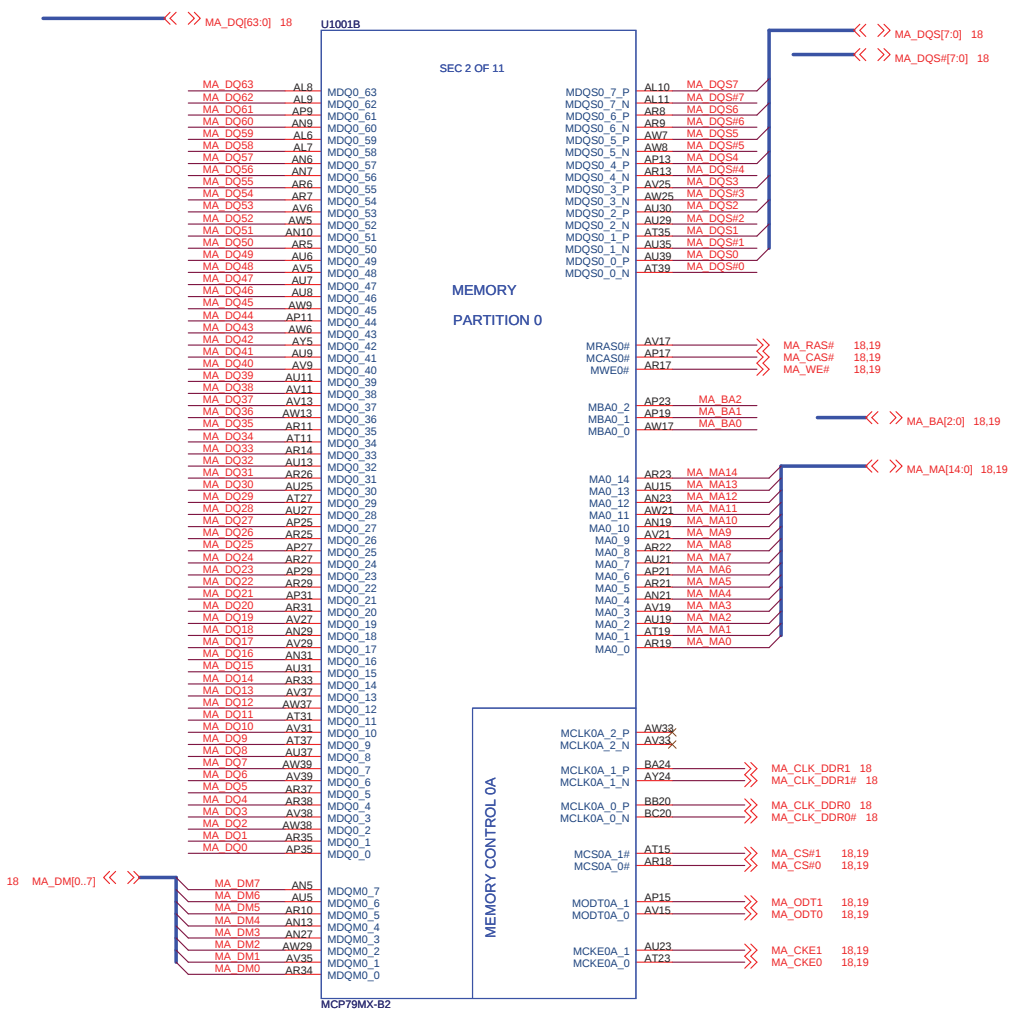
ASUSTeK COMPUTER INC. NB1**Engineer:**

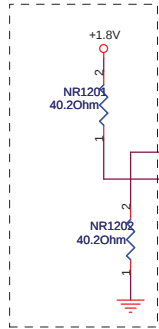
Size A	Project Name 1201I	Rev 2.0g
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Date: Friday, August 28, 2009Sheet 7 of 54

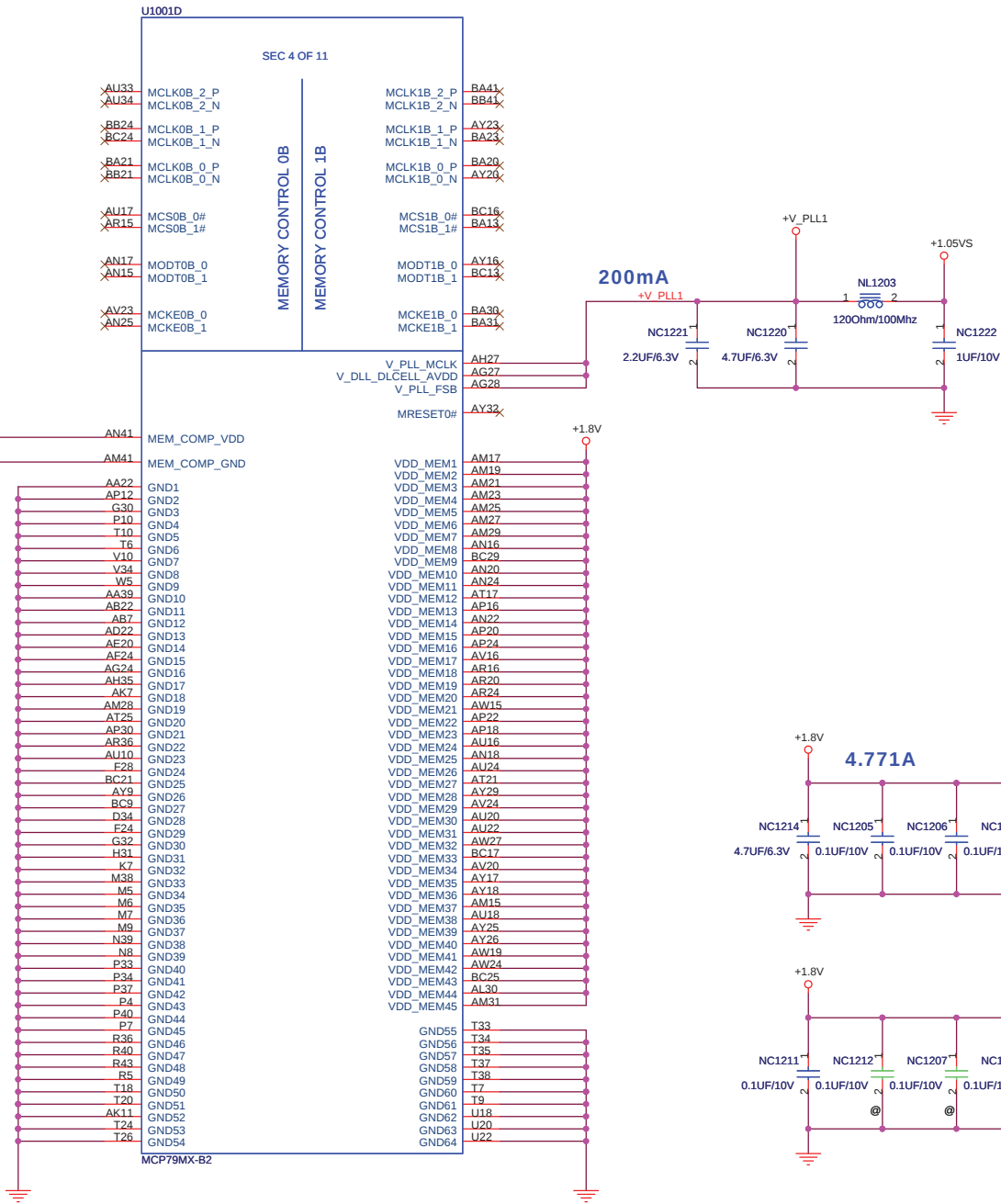


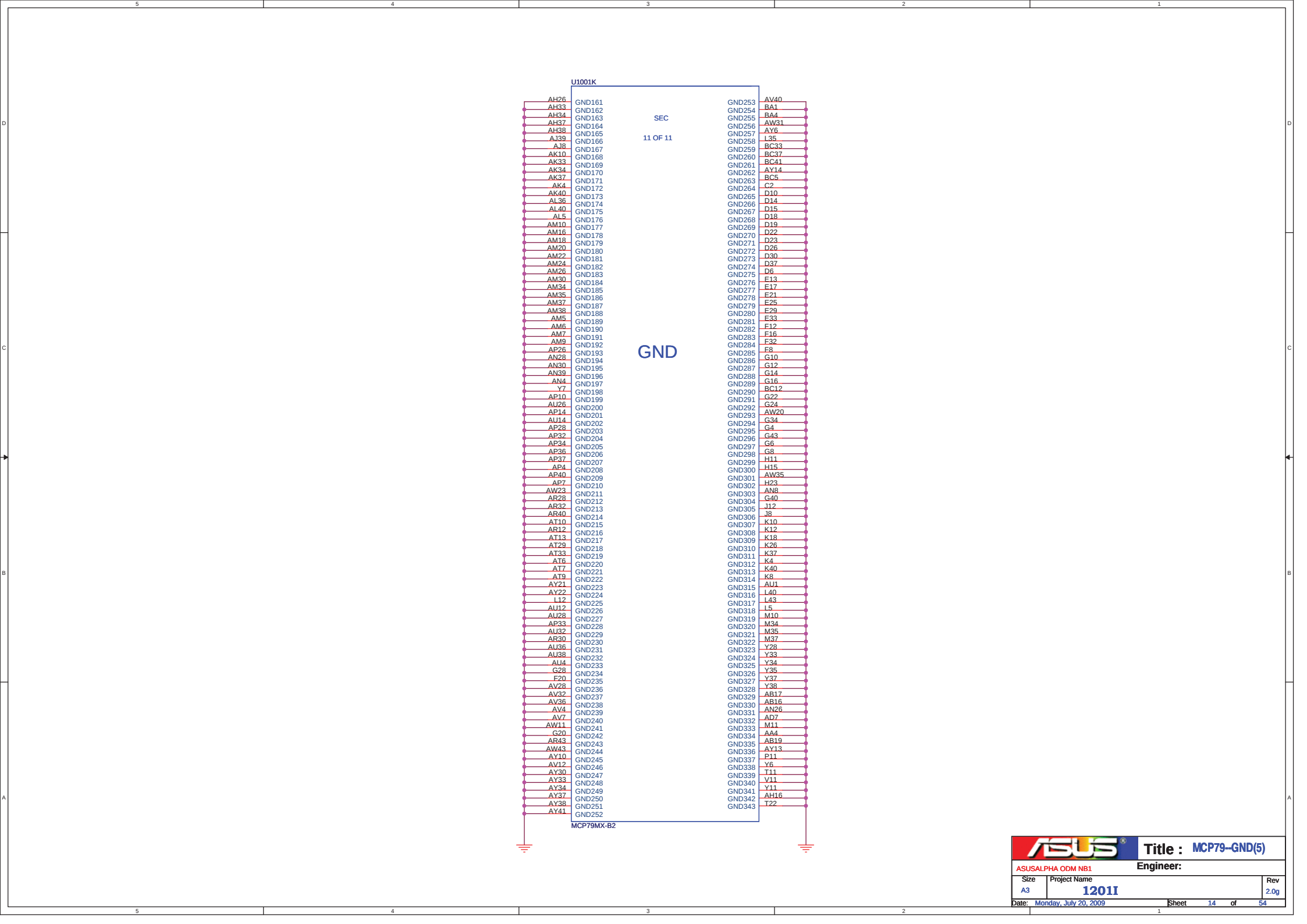


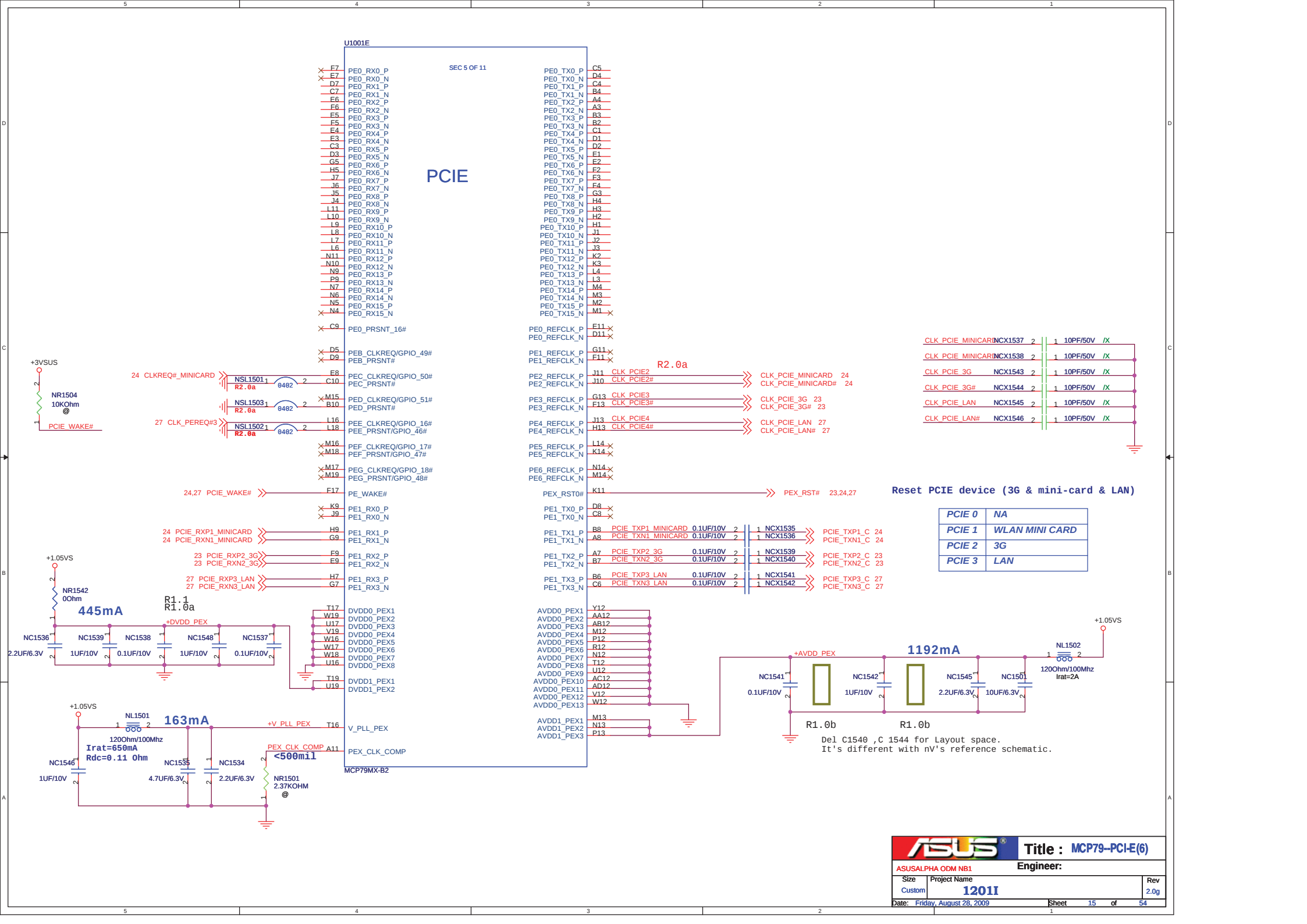


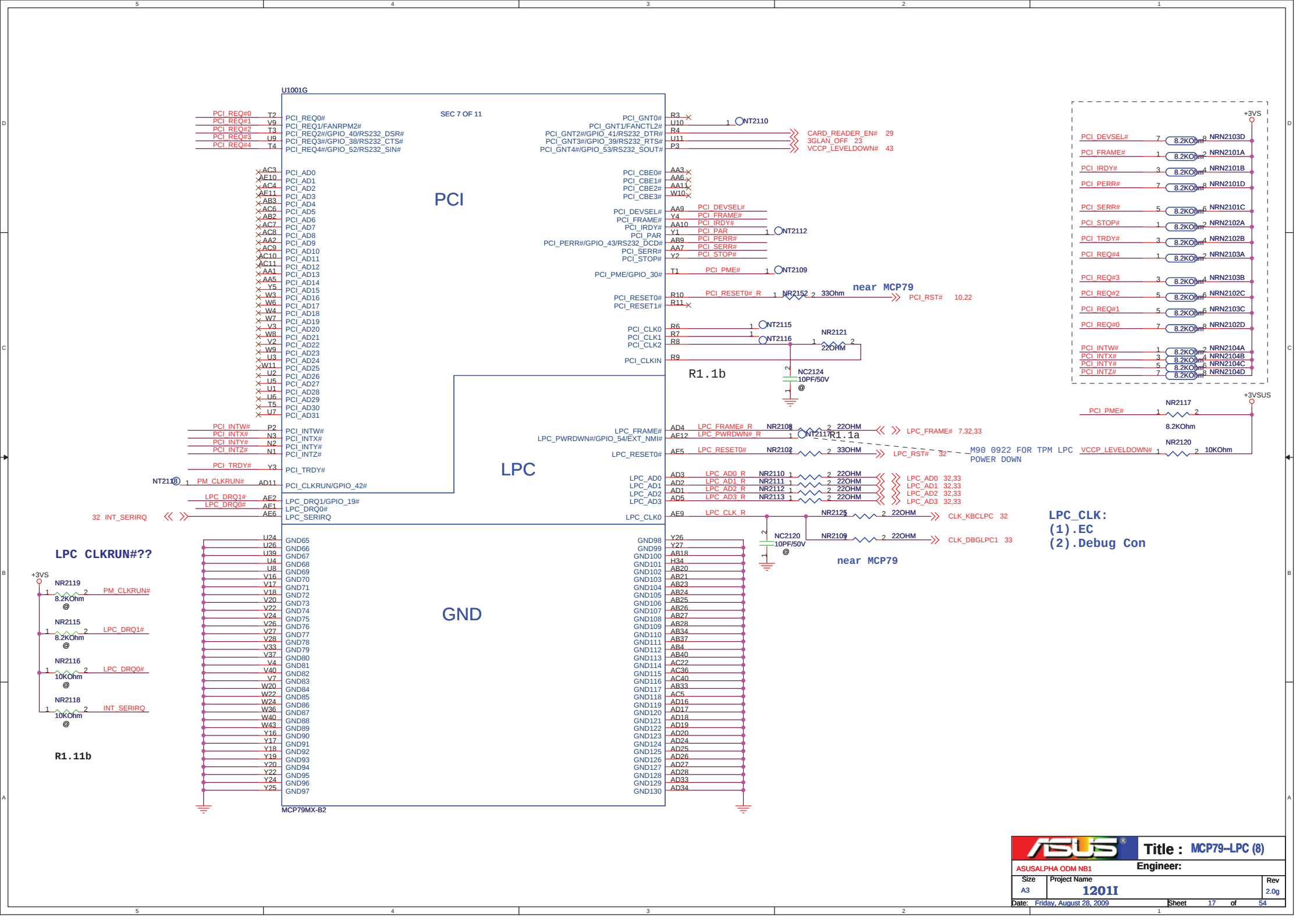


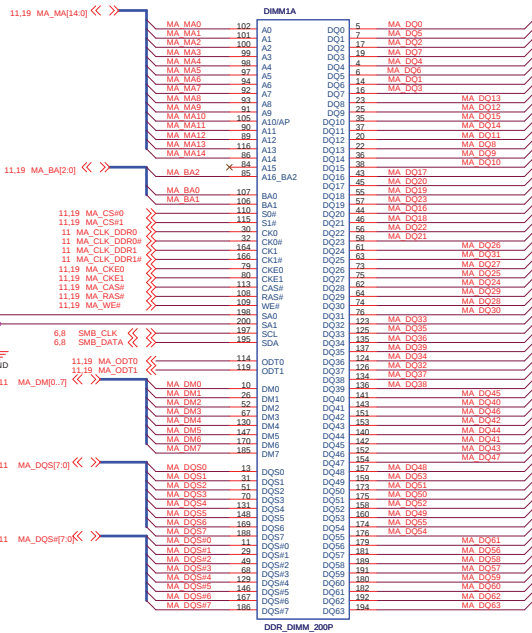
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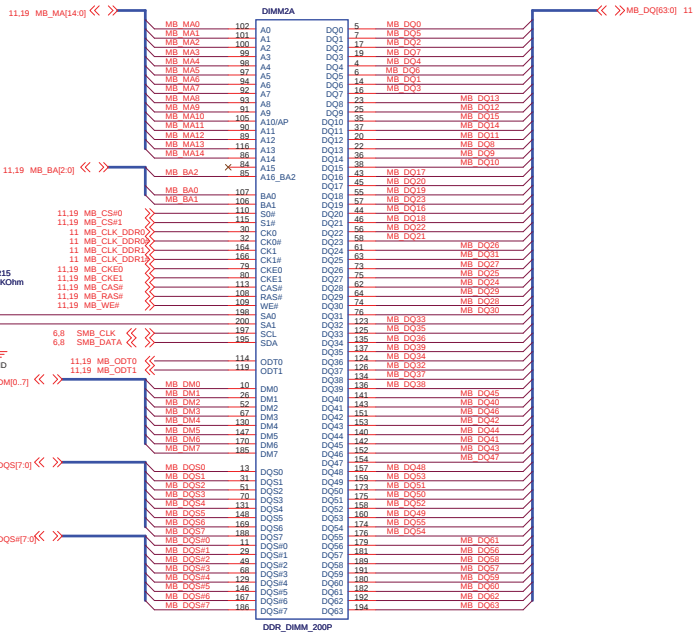




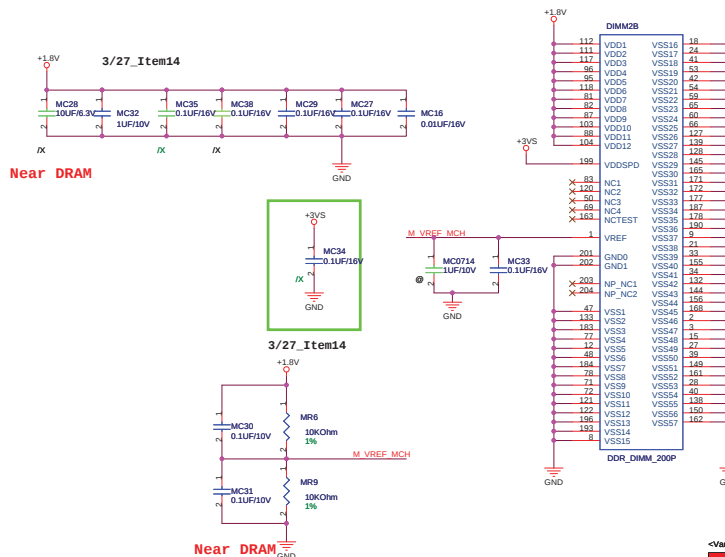
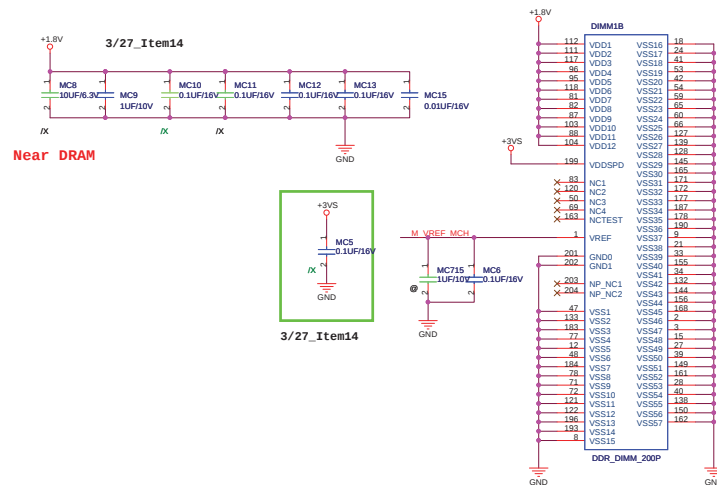




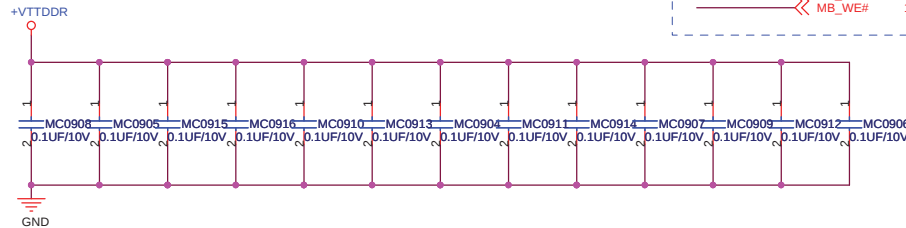
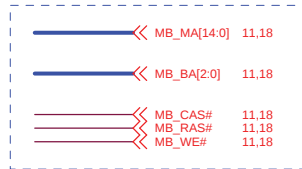
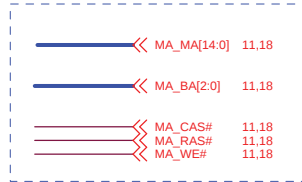
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DDR10. slot  Symbol use 12G02533200E
STD TYPE
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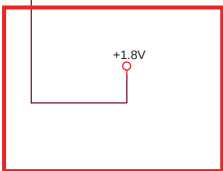
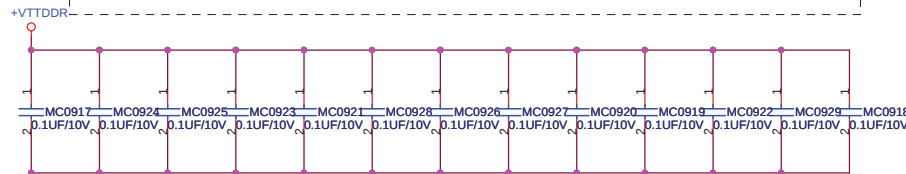
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DDR10. slot  Symbol use 12G02533200D
REV TYPE
```



+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve STR_EN# and SUSC#



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

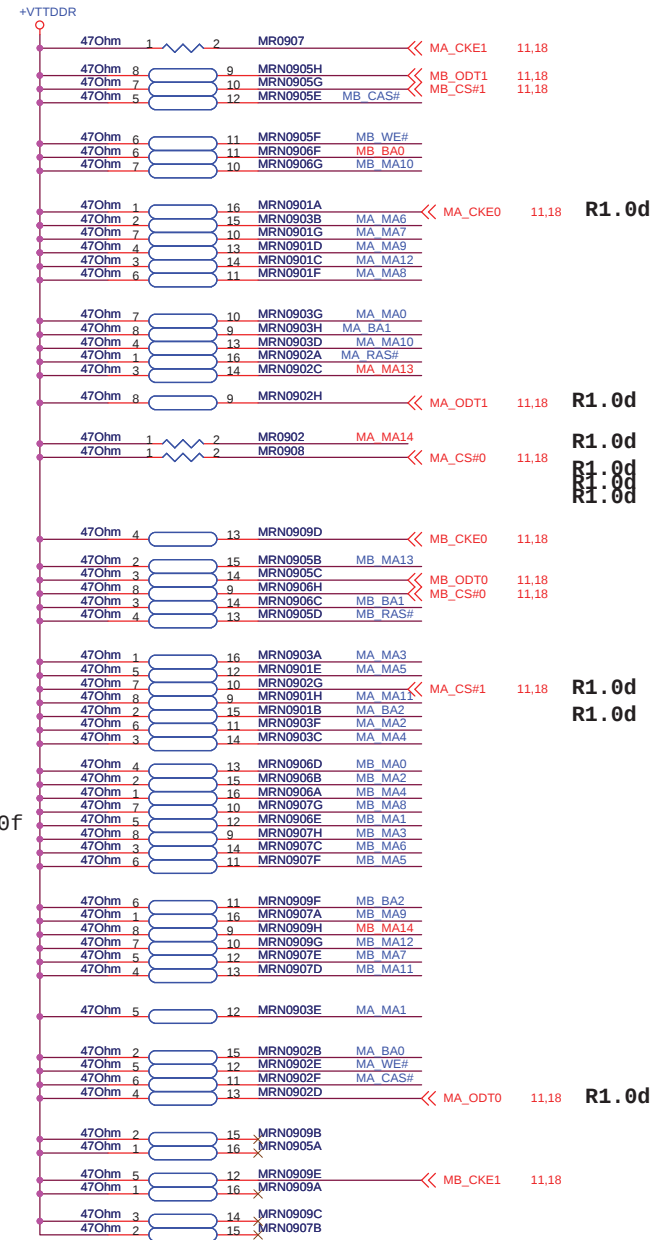


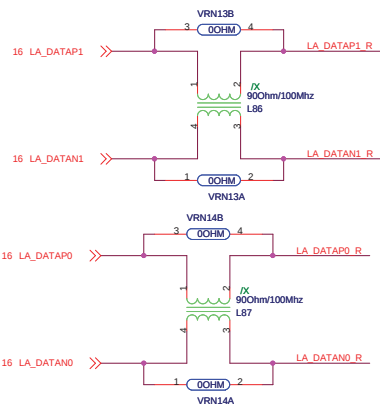
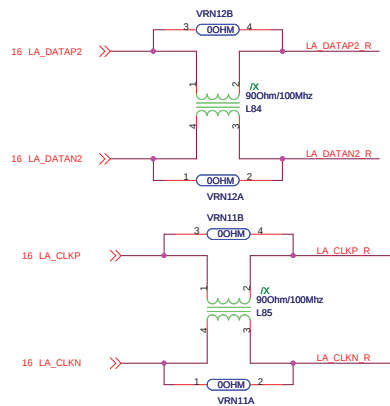
16X0.1UF to GND
16X0.1UF to 1.8V

HAS TO BE SWAPED

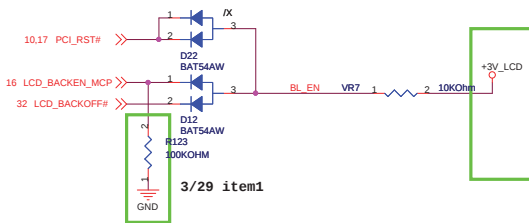
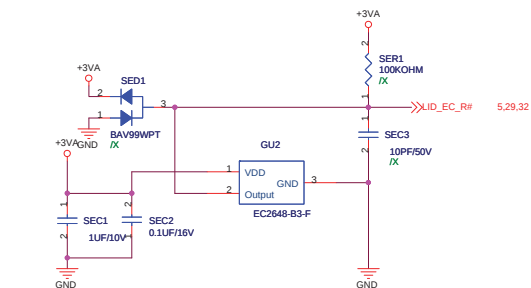
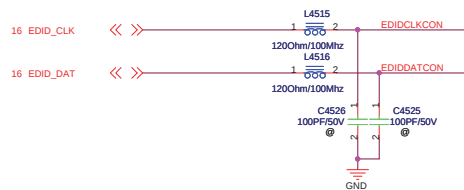
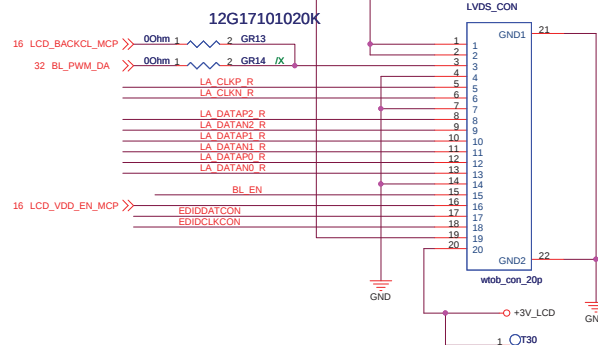
M_A_14 is reserved signal and keep R0901 separately

Don't include this page into DesignIP because of swapping



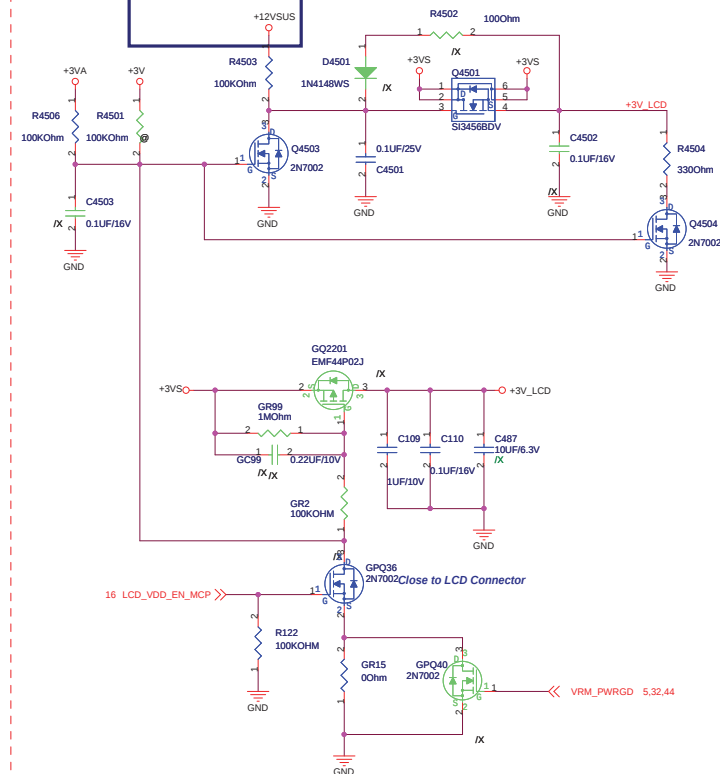


3/26_Item7 FOR RF

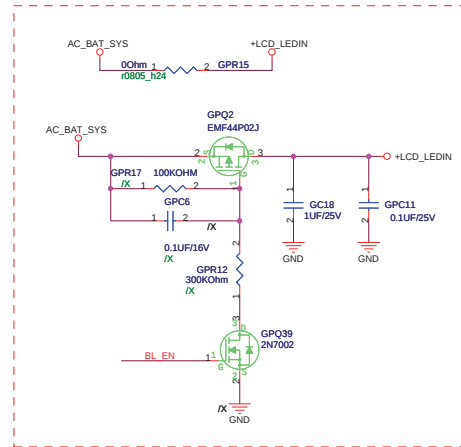


Backlight Enable Discharge

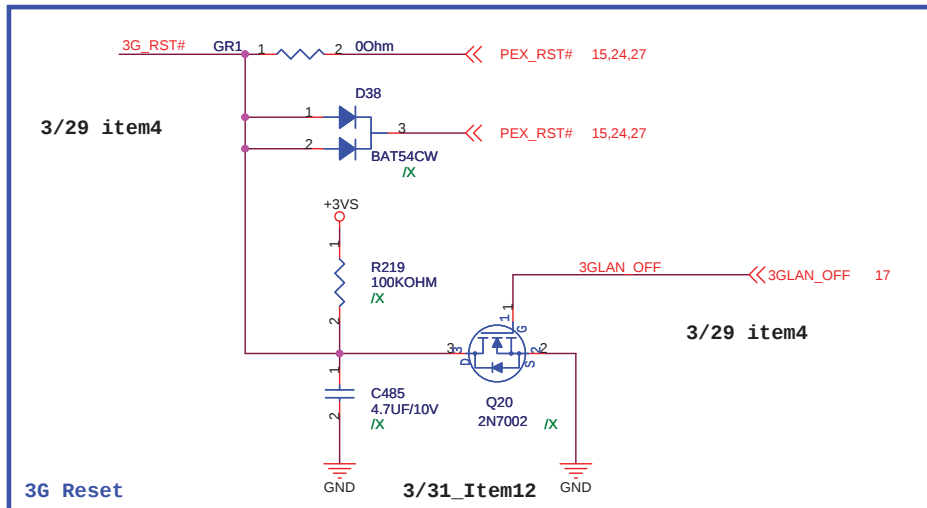
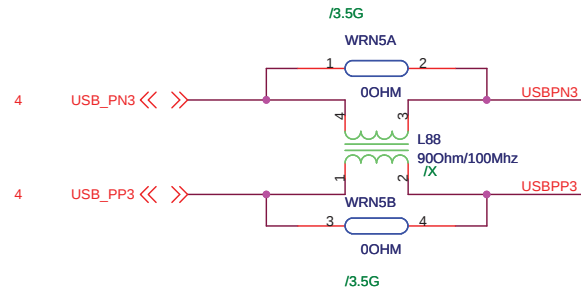
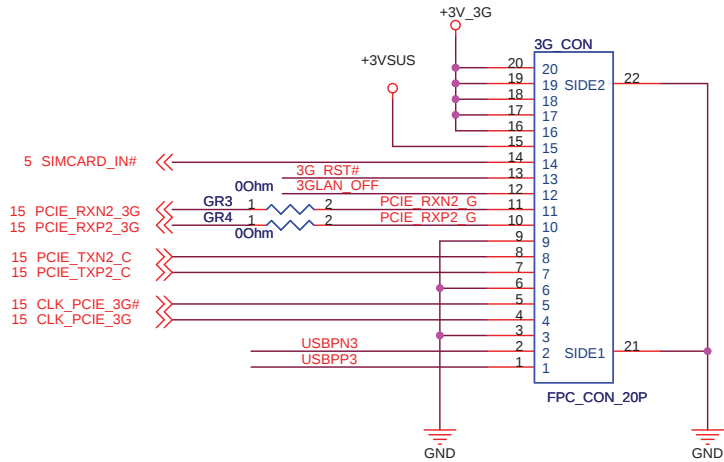
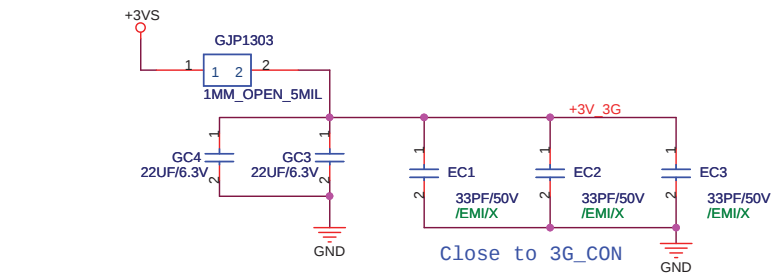
Seams OK, need check



LCD 3V Switch



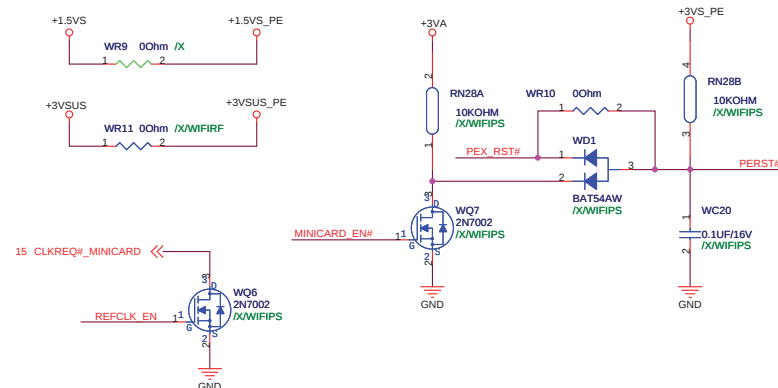
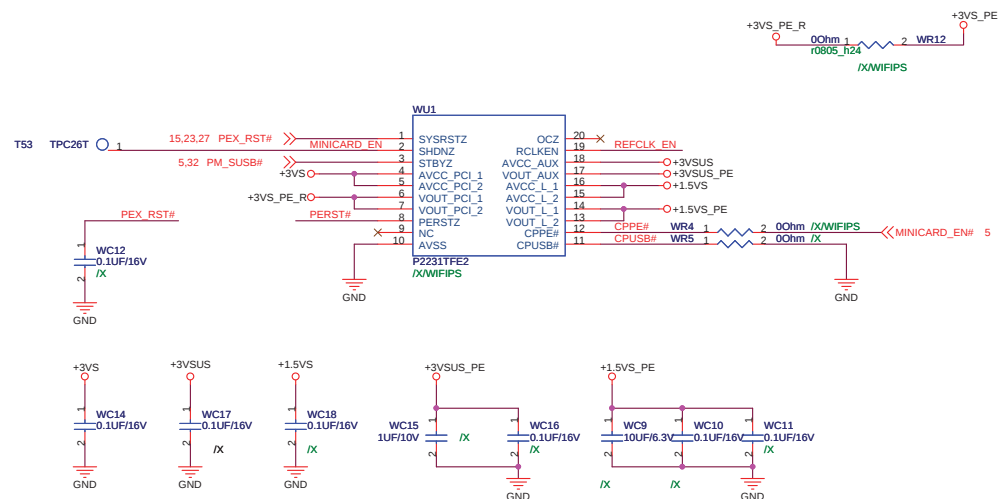
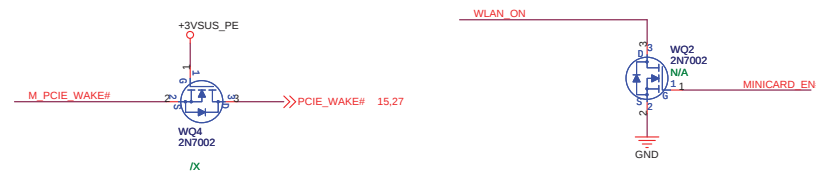
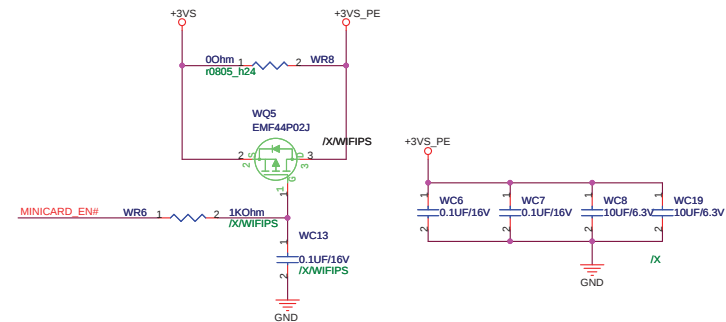
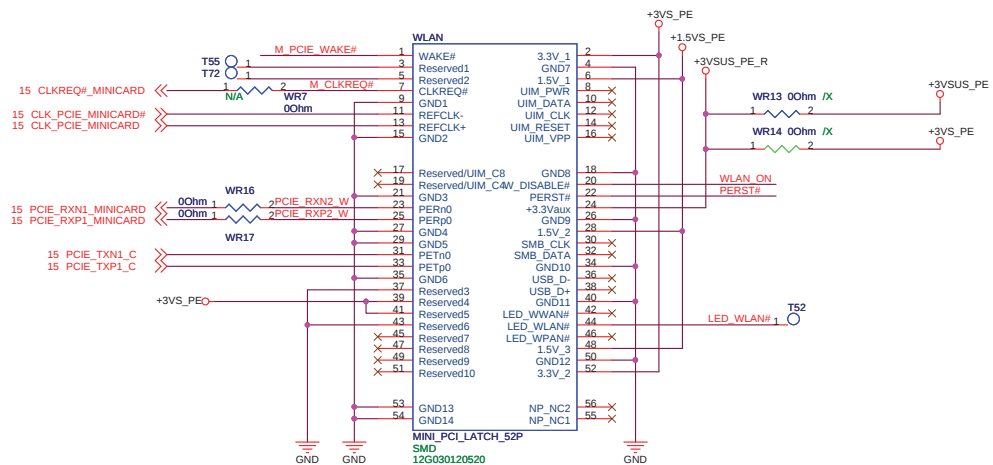
3/29 item6

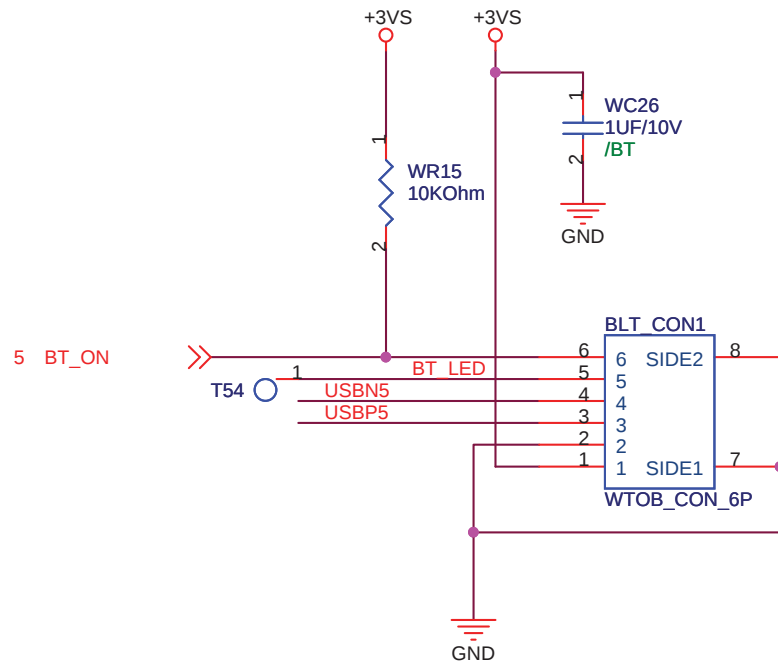


<Variant Name>

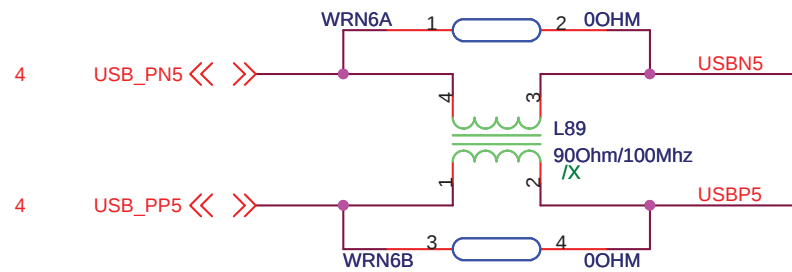
3.5G Module & External Antenna

ASUS		Title :	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
Custom	1201I	1.0	
Date: Friday, August 28, 2009		Sheet 23 of 54	



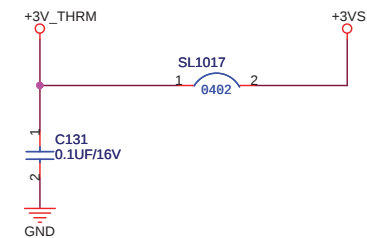
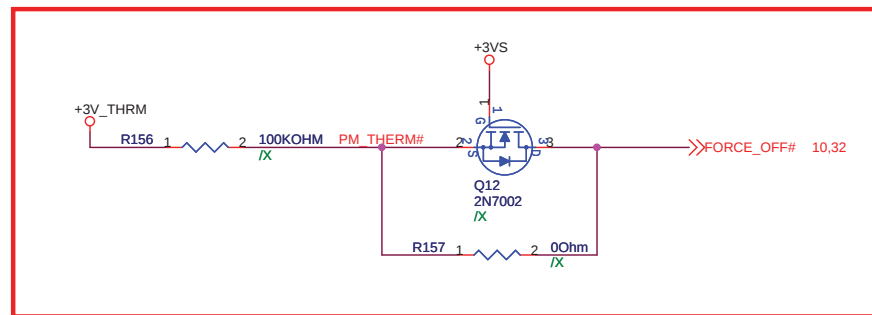
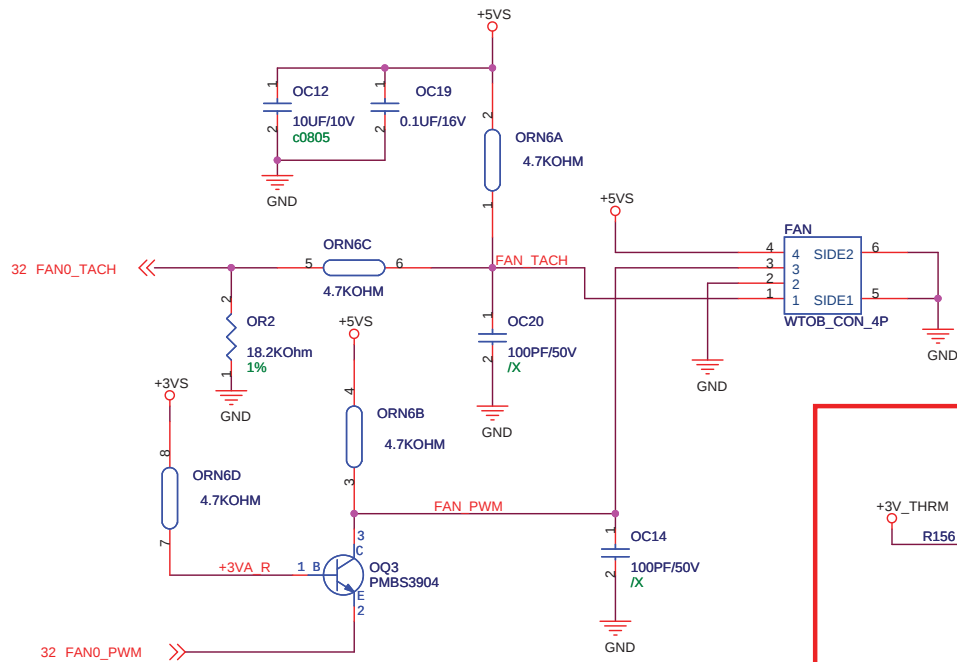


BT Conn



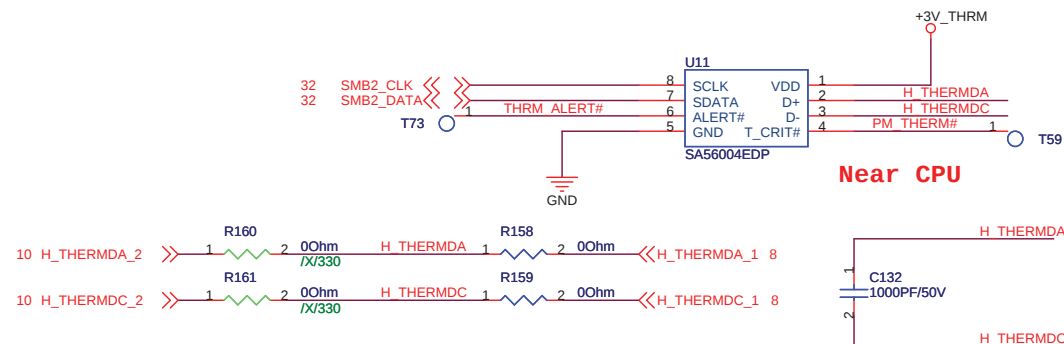
<Variant Name>

ASUS®		Title : Bluetooth	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name 1201I		Rev 1.0
Date: Friday, August 28, 2009		Sheet	25 of 54



Thermal Sensor Power Supply

Thermal Sensor



U11 use 06G023044020,
second source 06G023055010

<Variant Name>



Title : FAN_THERMAL SENSOR

ASUSTek Computer INC.

Engineer: N/A

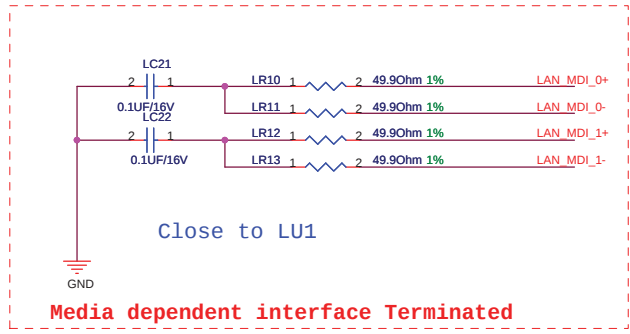
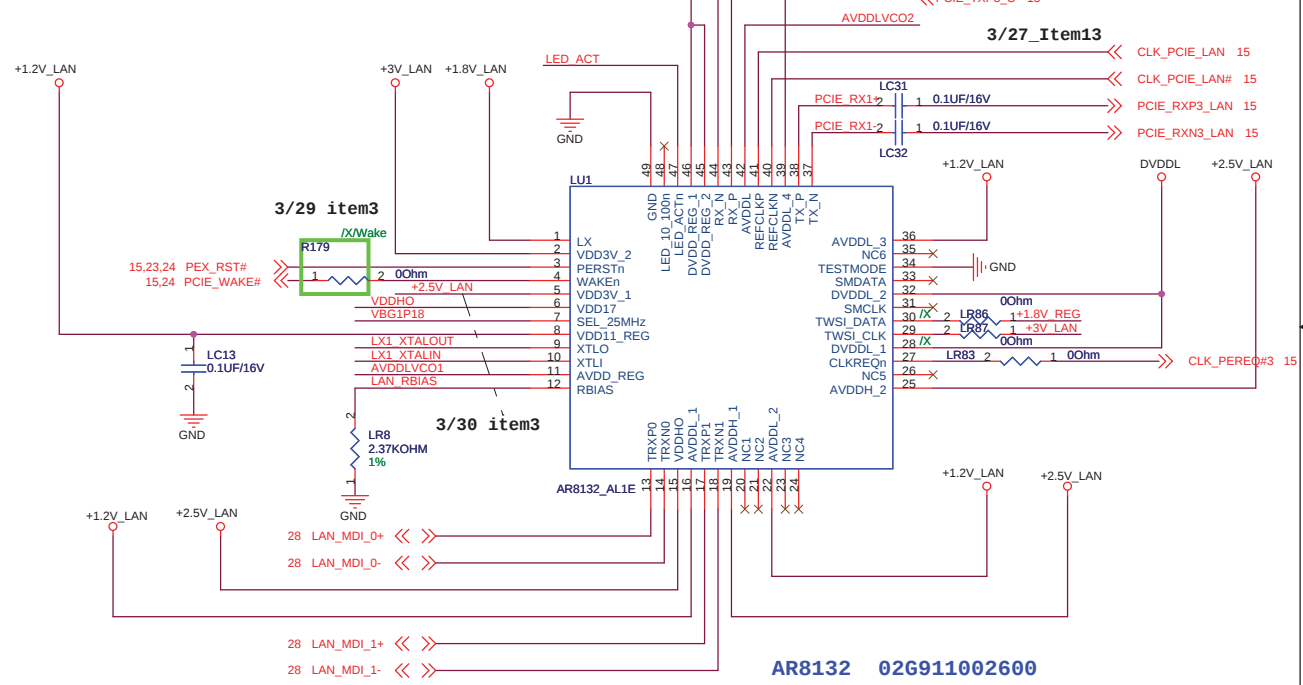
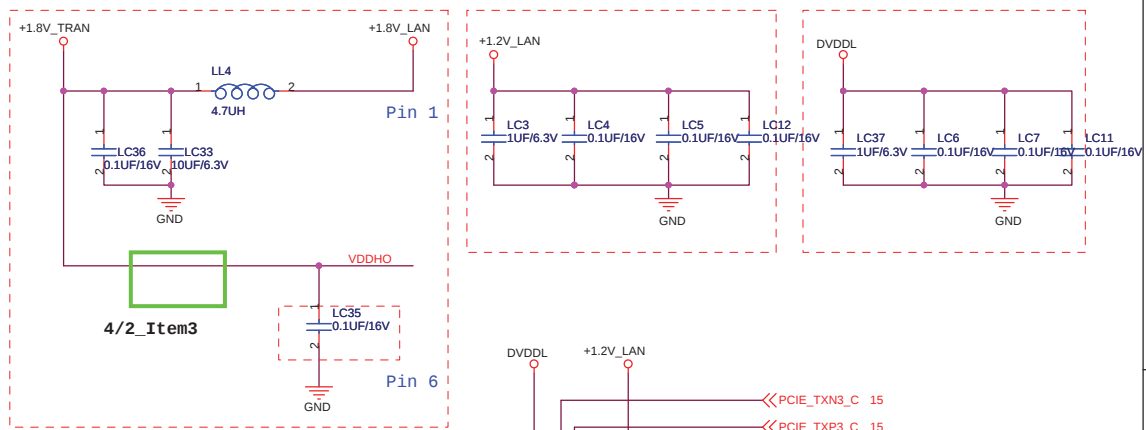
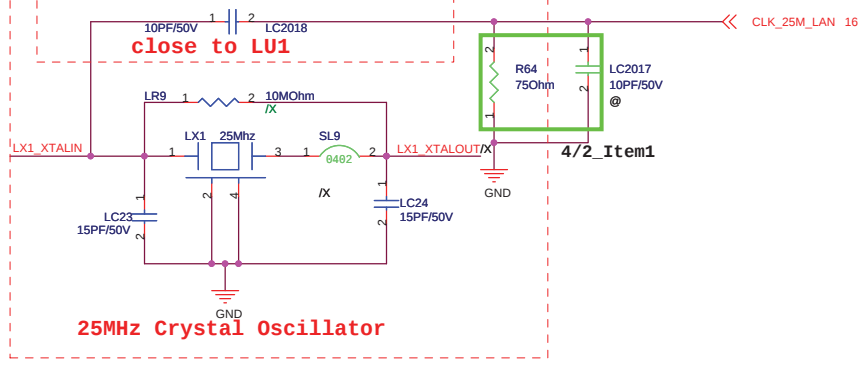
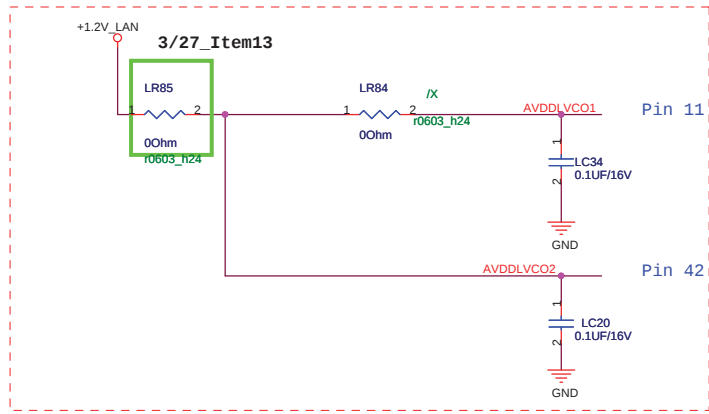
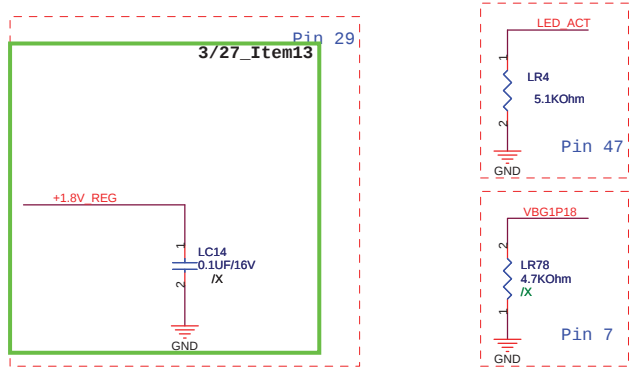
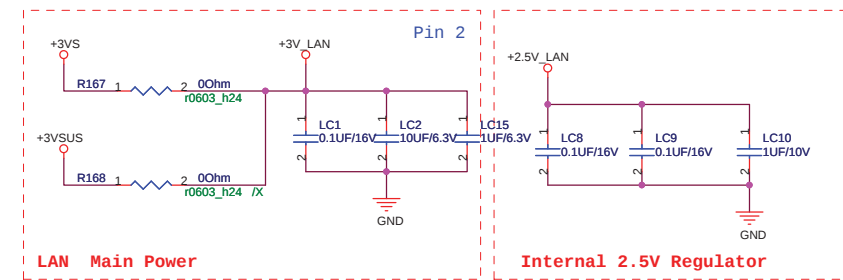
Size
Custom

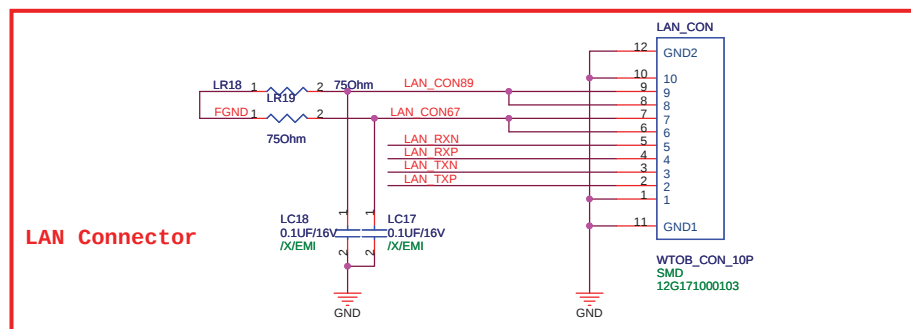
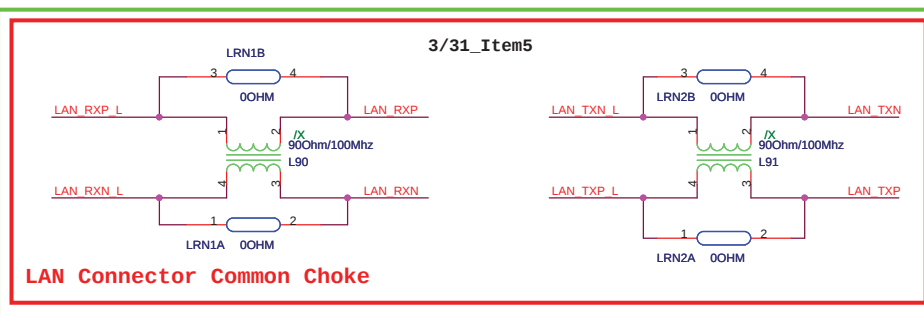
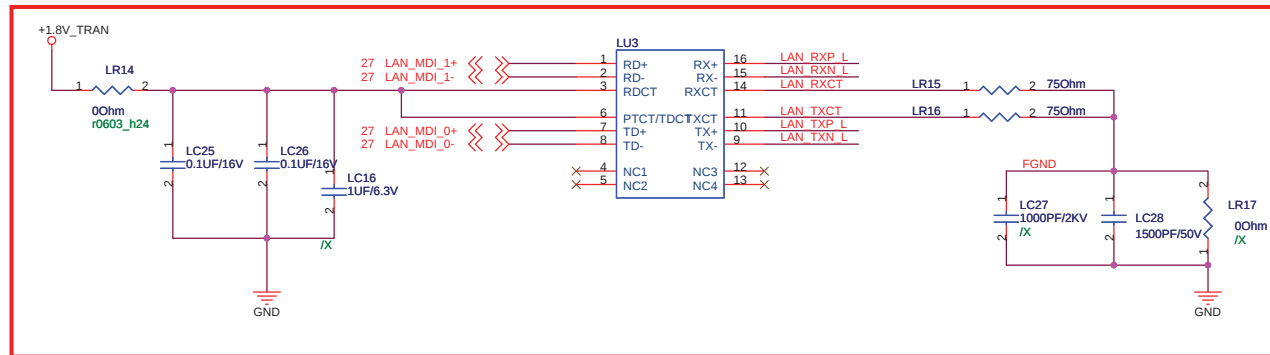
Project Name
12011

Rev
1.0

Date: Wednesday, September 02, 2009

Sheet 26 of 54

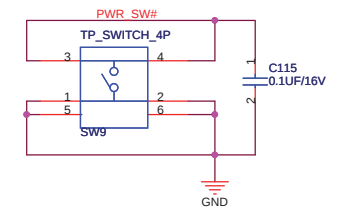
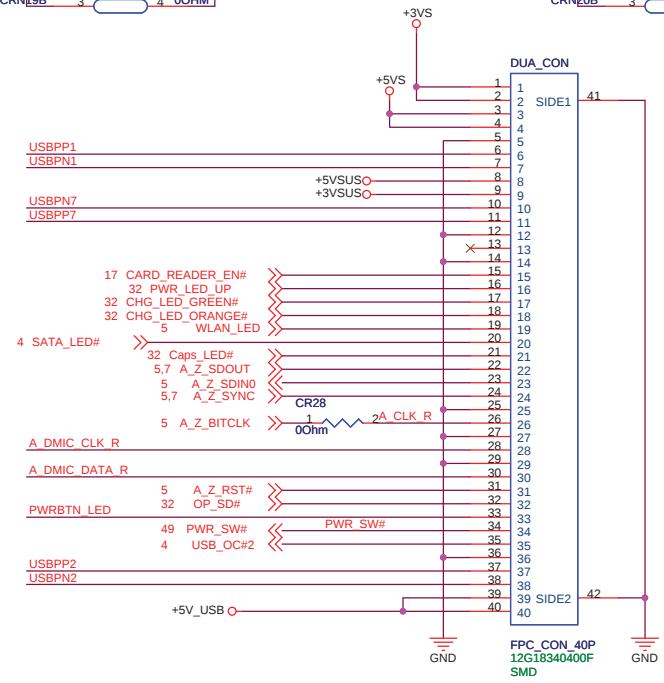
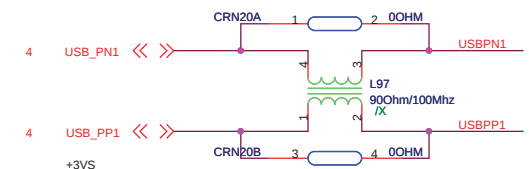
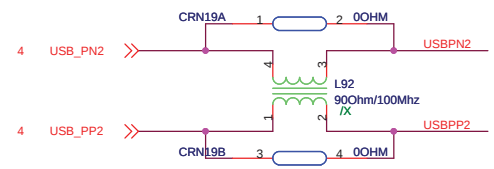
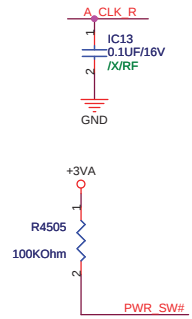




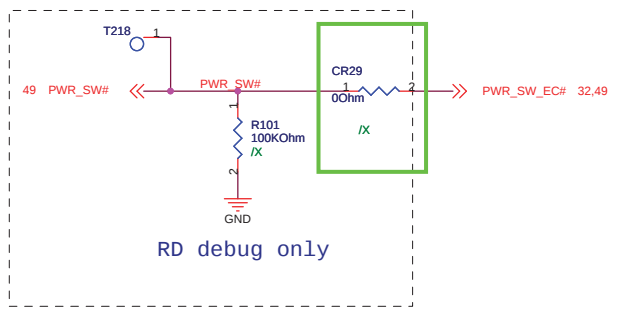
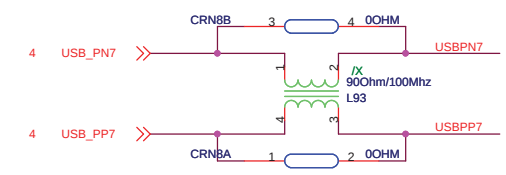
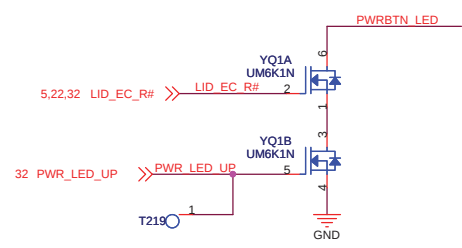
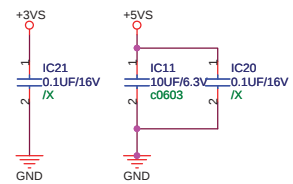
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36 A_DMIC_CLK_R << >> A_DMIC_CLK_R

36 A_DMIC_DATA_R << >> A_DMIC_DATA_R



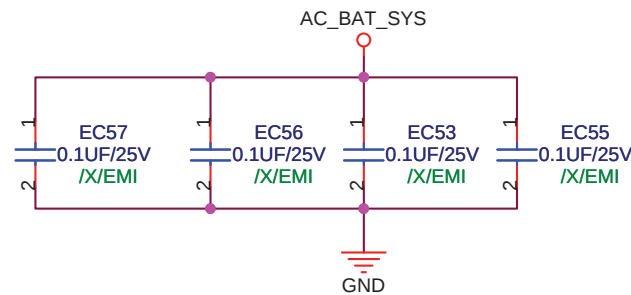
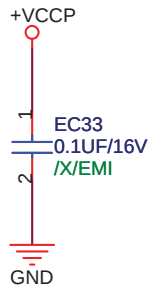
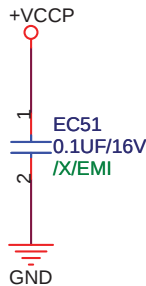
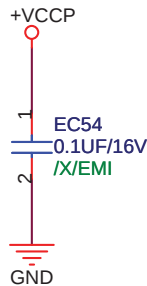
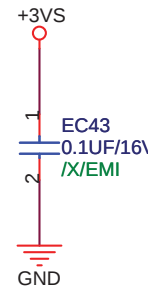
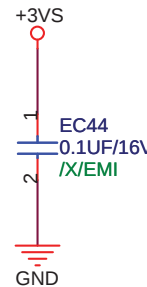
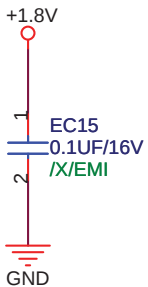
RD debug only



RD debug only

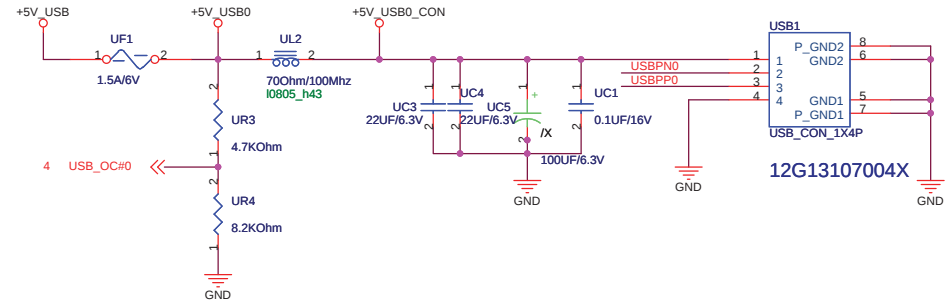
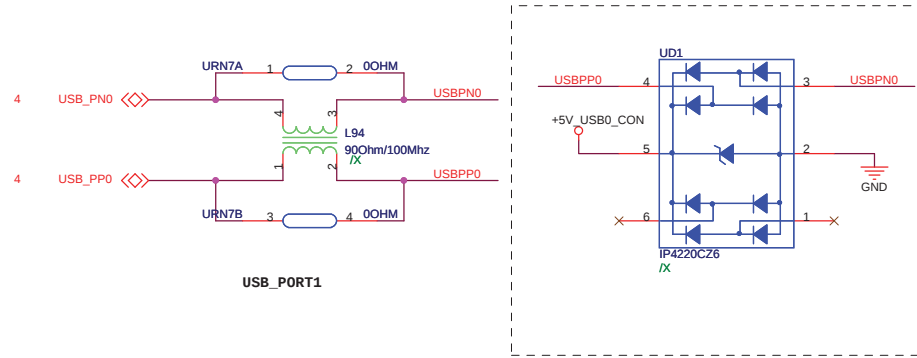
3/26 item11

3/25 item3

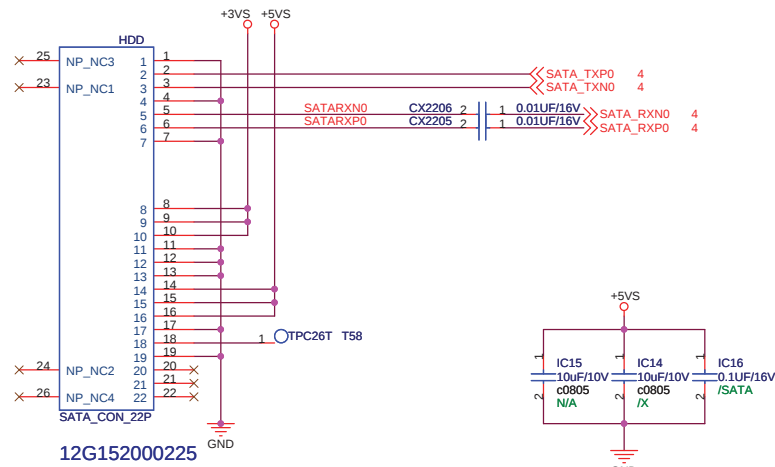


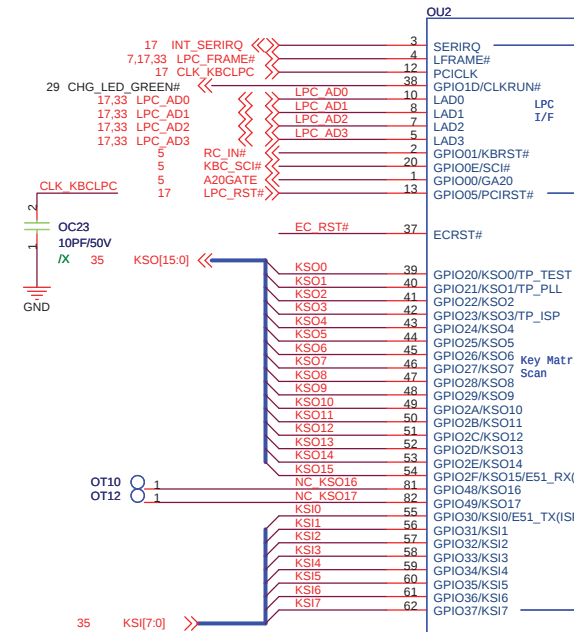
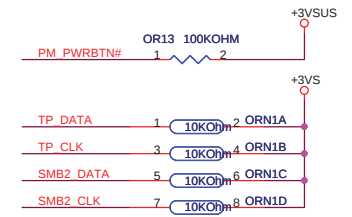
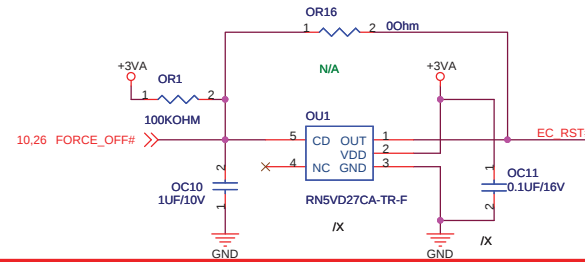
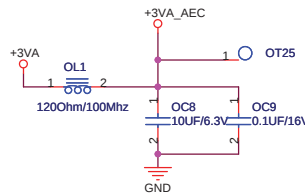
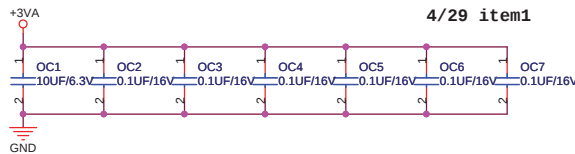
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		Title : EMI	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name 1201I		Rev 1.0
Date: Friday, August 07, 2009		Sheet	30 of 54



SATA HDD Connector





3/30 item1

3/27 item6

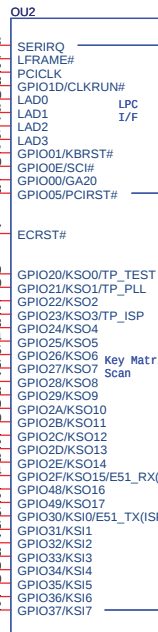
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

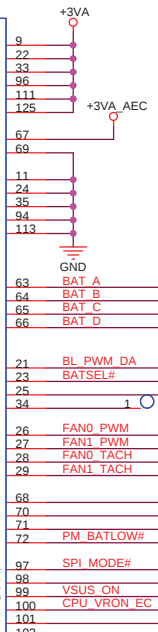
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

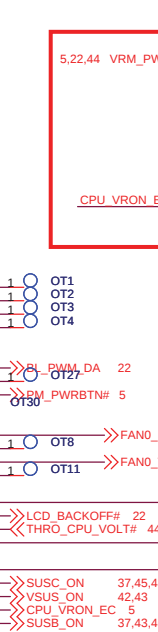
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

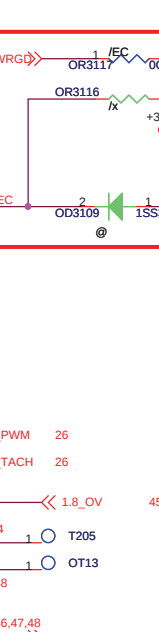
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

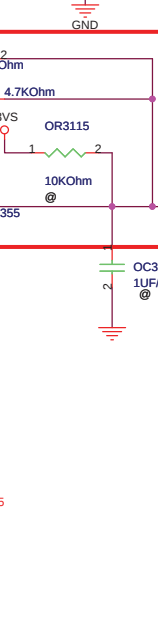
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

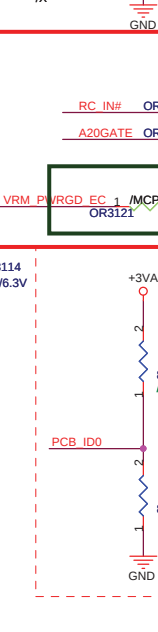
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

3/30 item9

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3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

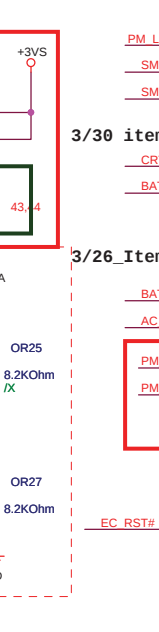
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

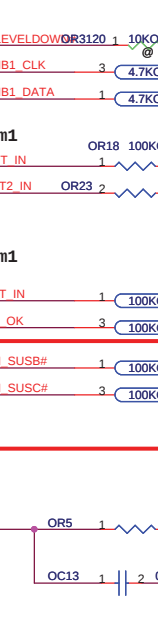
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

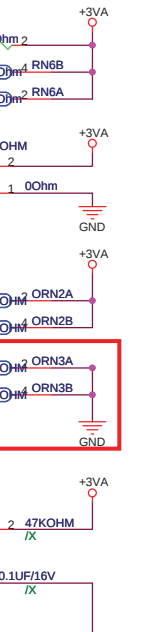
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

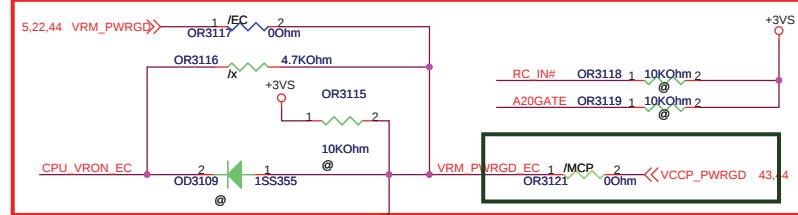
3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU



3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU

3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU

3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU

3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU

3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU

3/30 item1

3/27 item6

3/30 item9

3/25 item10

3/26 Item1

3/25 item10

HOTKEY_SW0# - HOTKEY_SW3# internal PU

3/30 item1

3/27 item6

3/30 item9

3/25 item10

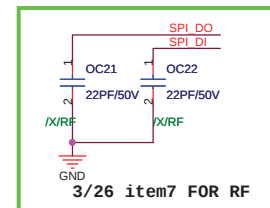
3/26 Item1

3/25 item10

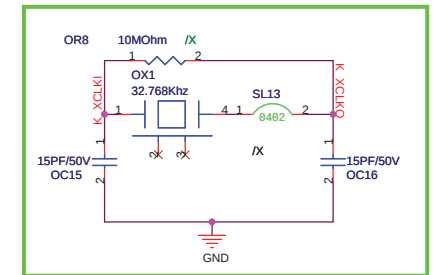
HOTKEY_SW0# - HOTKEY_SW3# internal PU

Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home



3/26 item7 FOR RF

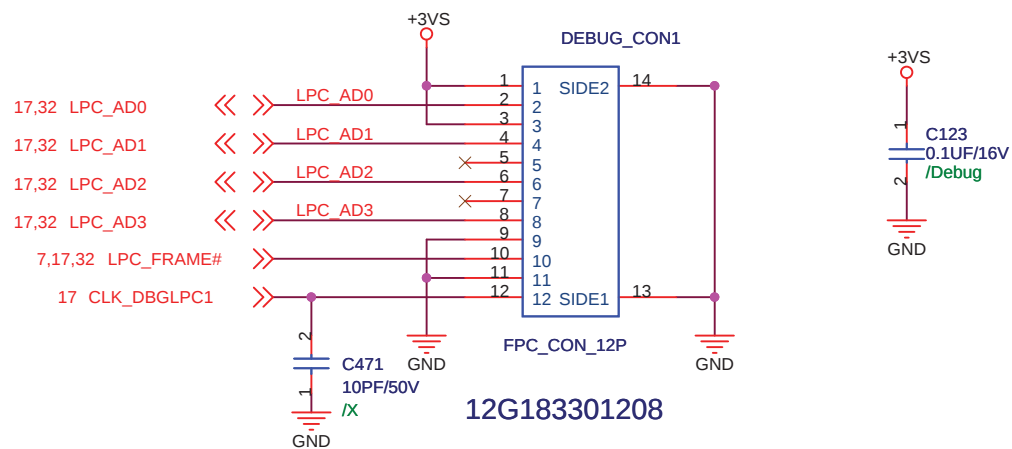


3/31 item14

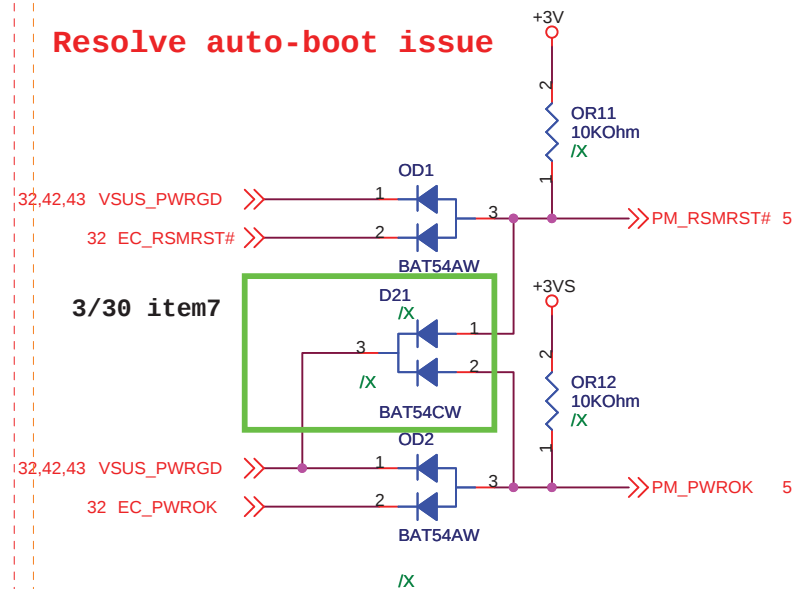
<Variant Name>

ASUS		Title : EC_ENE KB3310	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
A3	12011	1.0	
Date: Friday, August 28, 2009		Sheet 32 of 54	

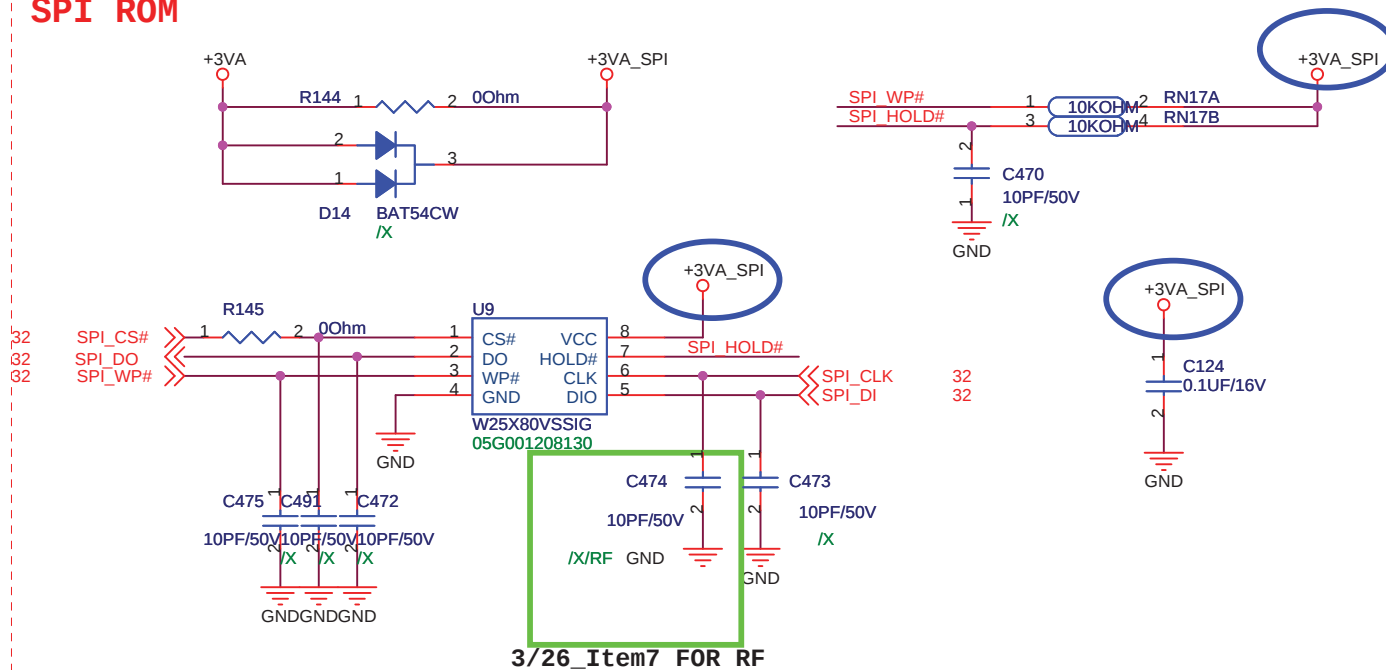
For Debug



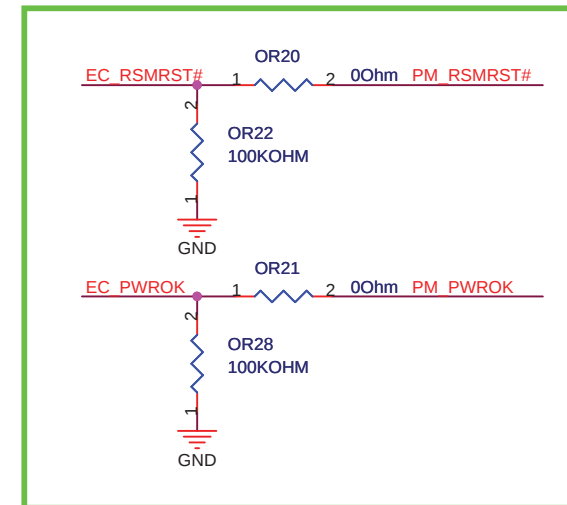
Resolve auto-boot issue



SPI ROM

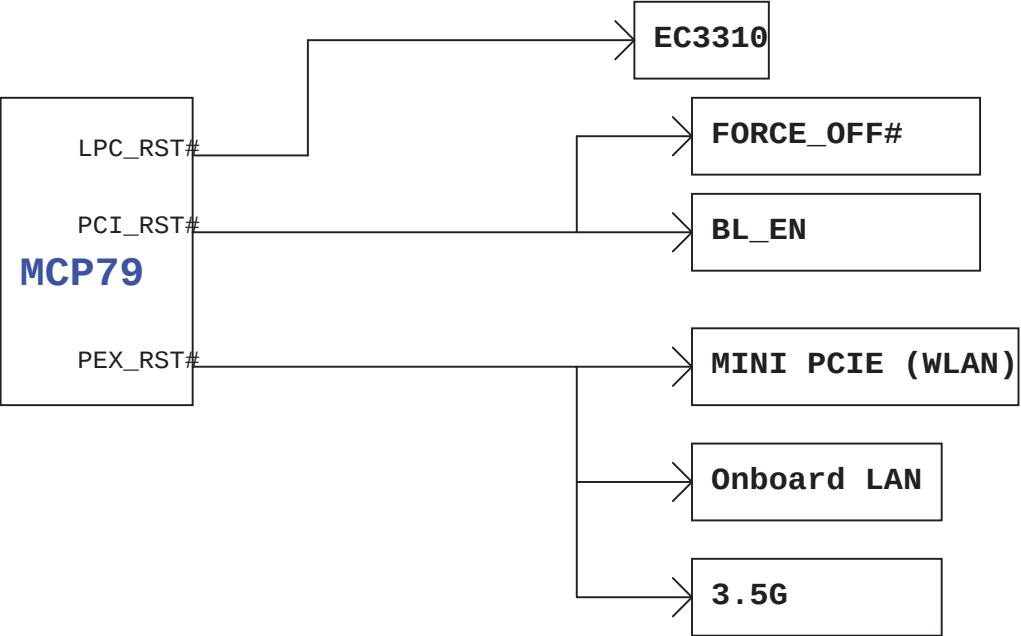


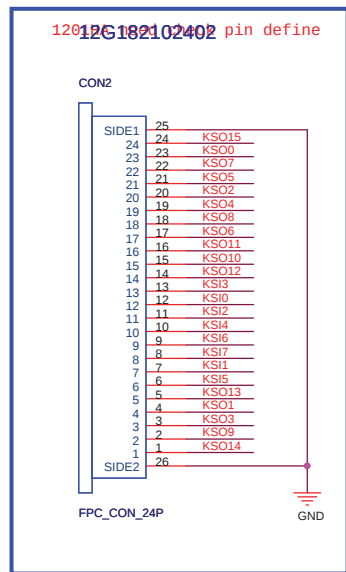
3/30 item7



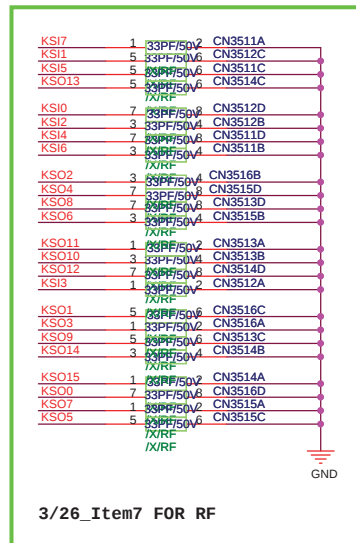
<Variant Name>

ASUS		Title : SPI ROM/ Debug	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 12011		Rev 1.0
Date: Friday, August 28, 2009	Sheet 33 of 54		

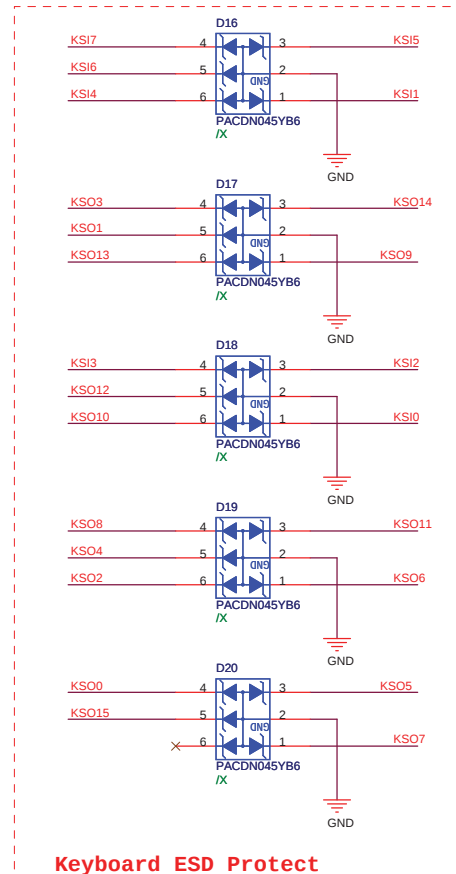




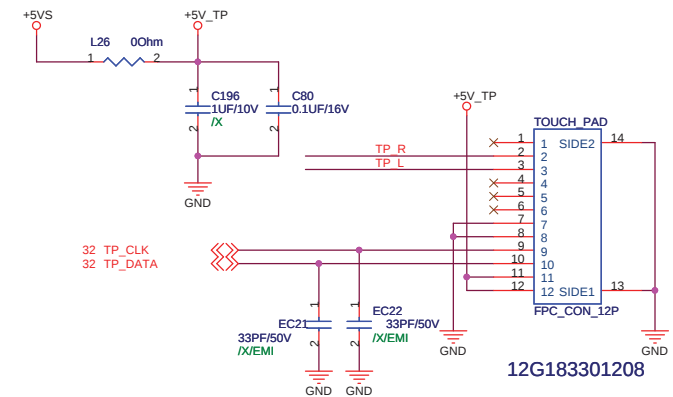
For Keyboard Connector



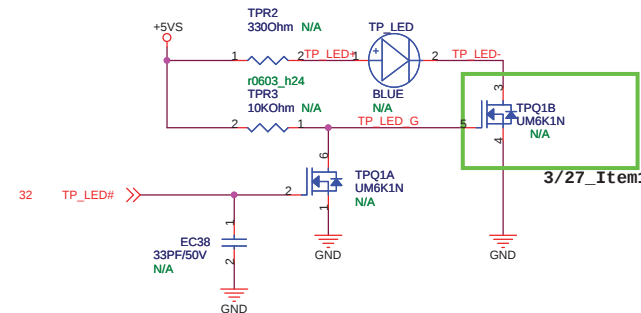
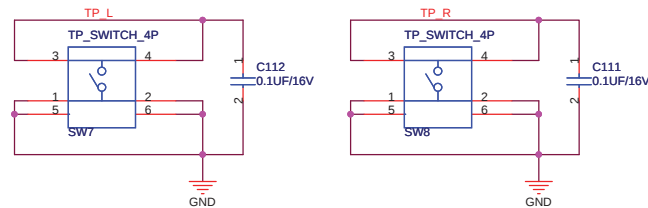
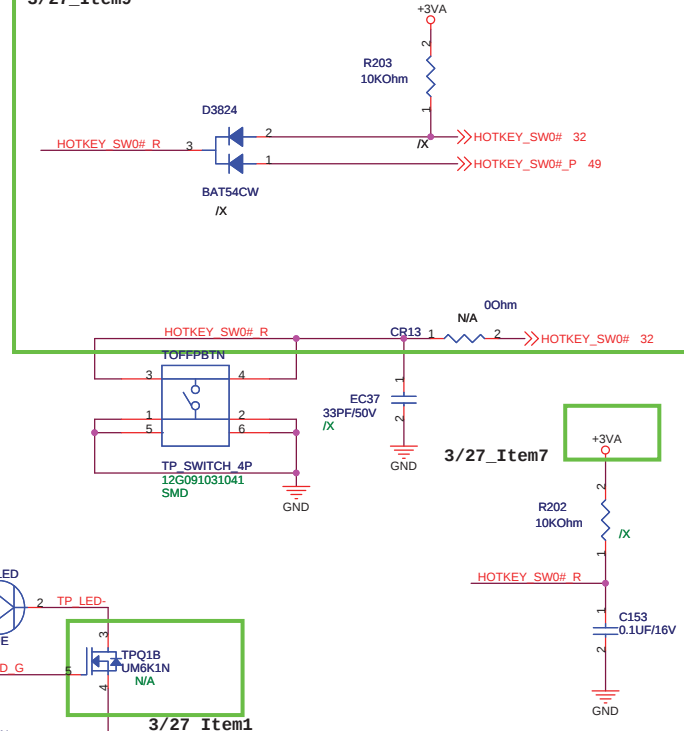
4/3_Item1



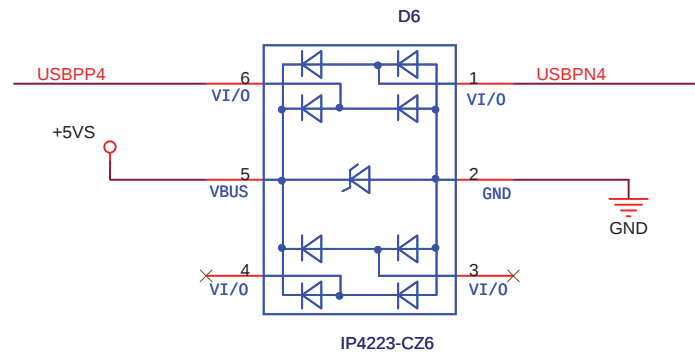
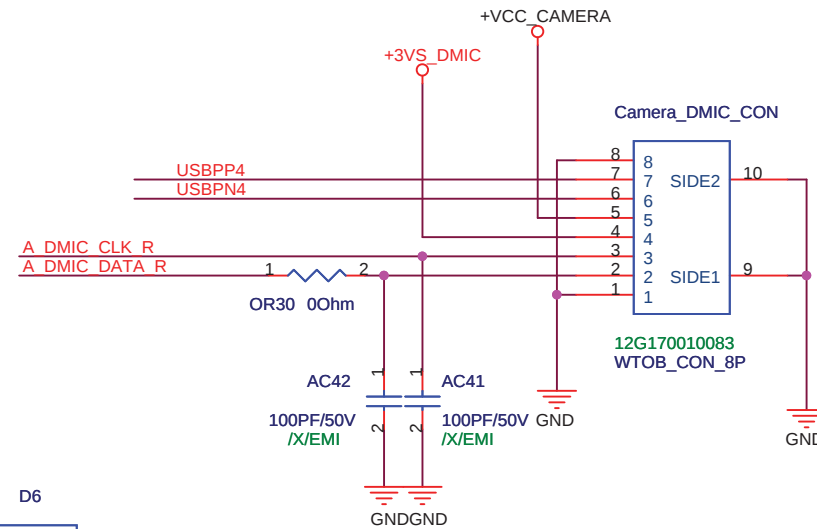
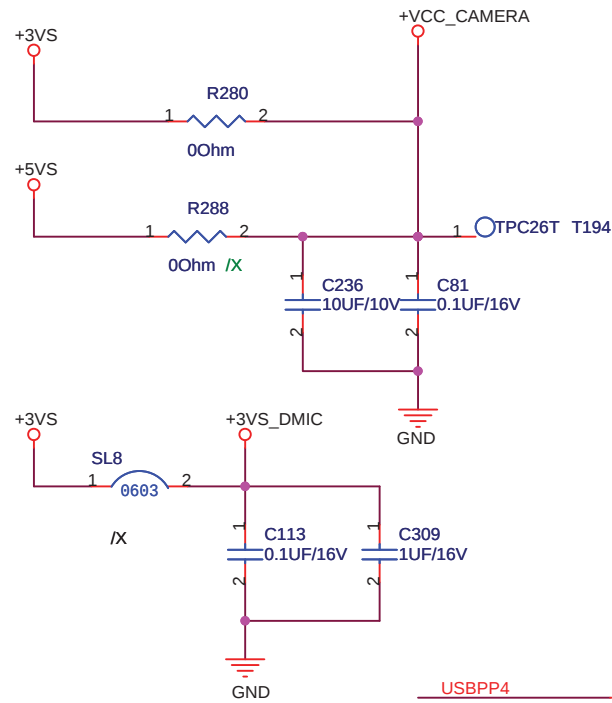
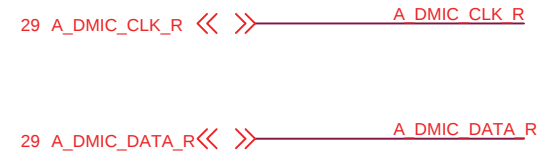
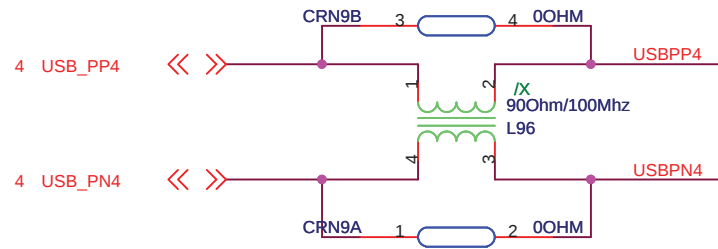
For Touch-Pad



3/27_Item9

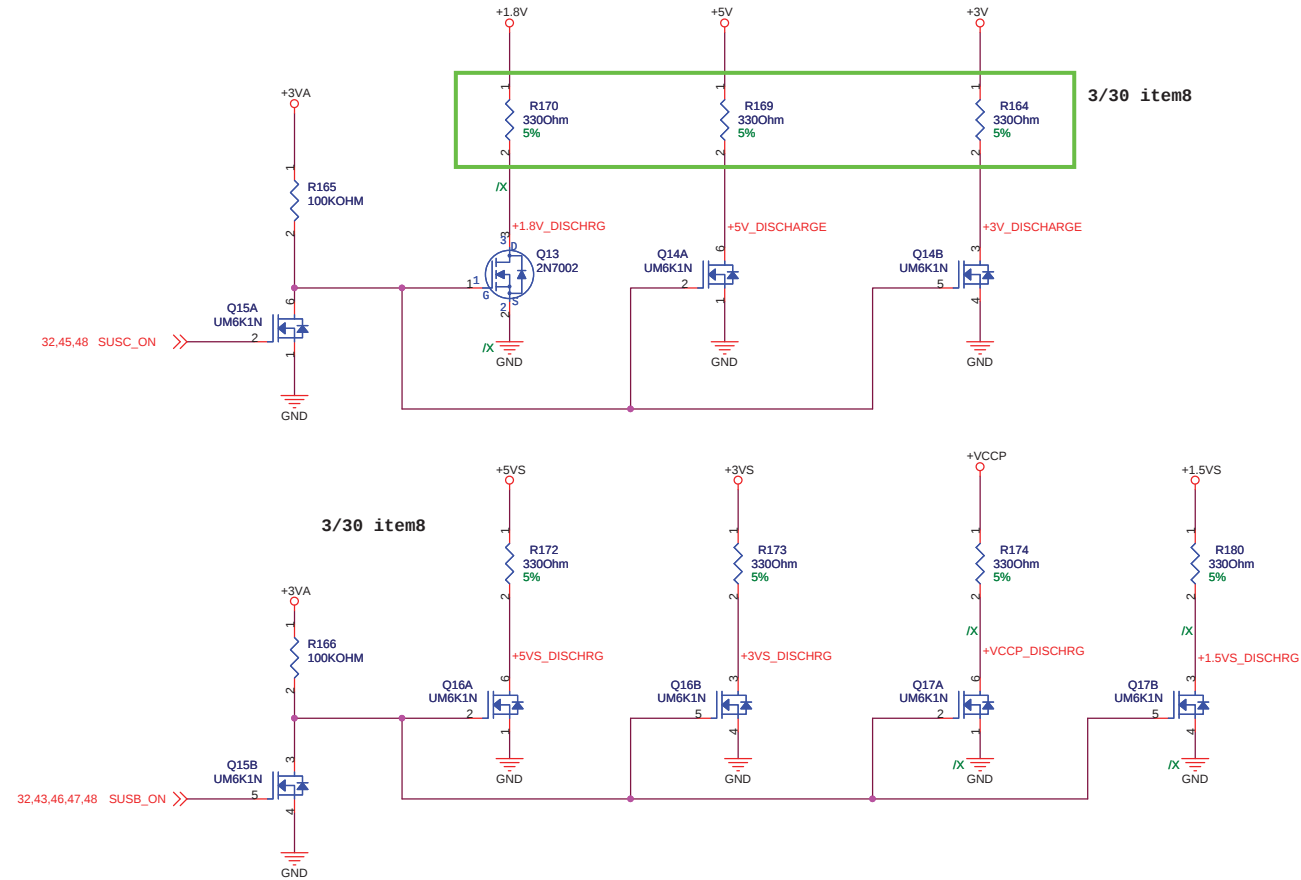


<Variant Name>



<Variant Name>

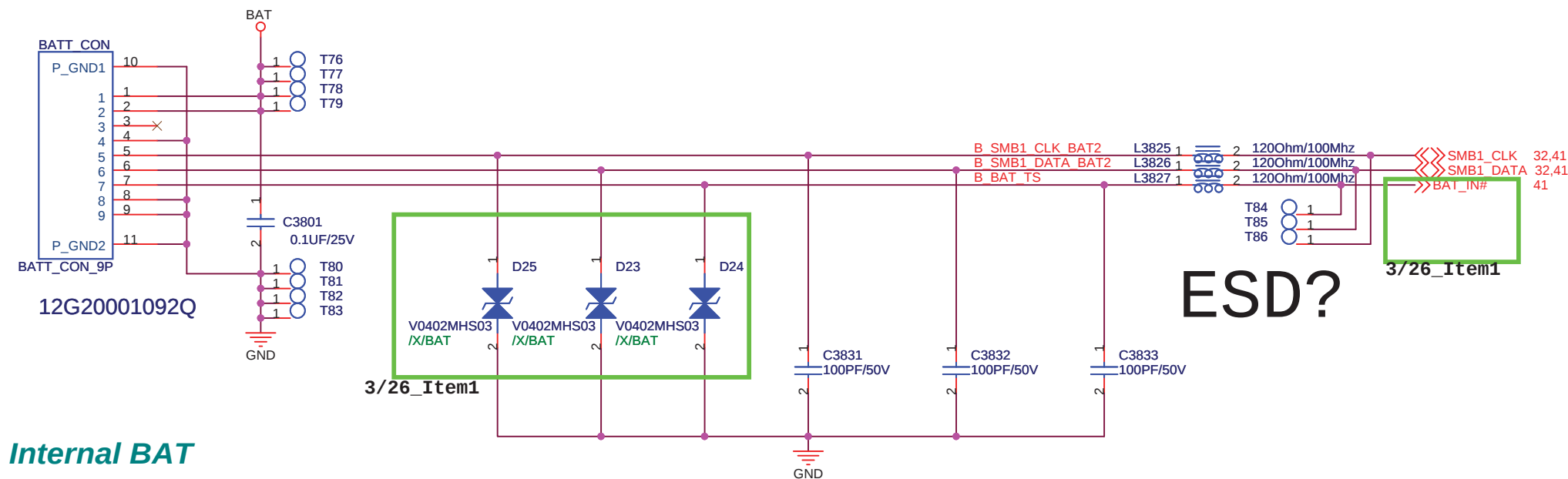
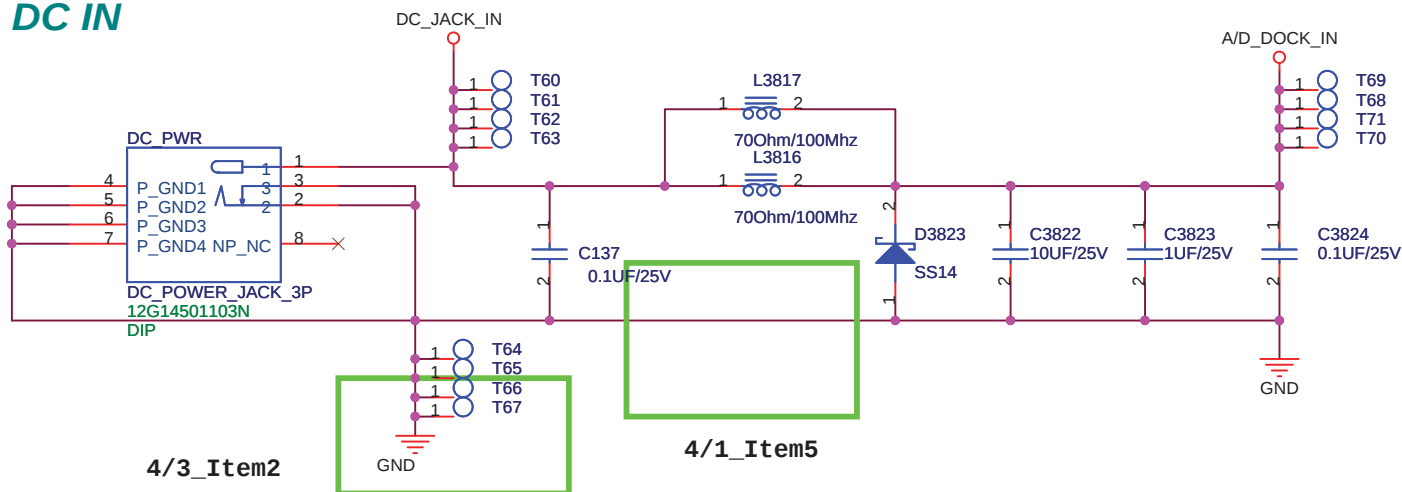
ASUS		Title : CMOS	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1201I		Rev 1.0
Date: Friday, August 28, 2009		Sheet	36 of 54



<Variant Name>

		Title : Discharge	
ASUSTek Computer INC.		Engineer: N/A	
Size A3	Project Name 1201I	Rev 1.0	
Date: Friday, August 28, 2009		Sheet 37 of 54	

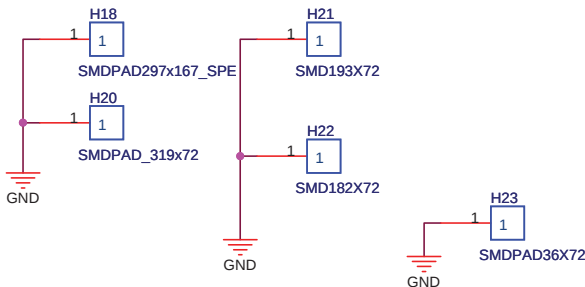
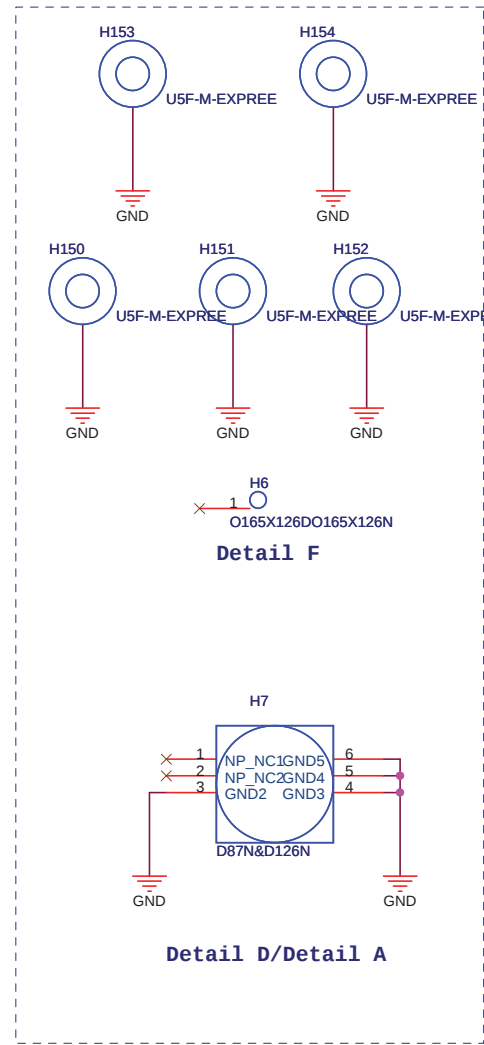
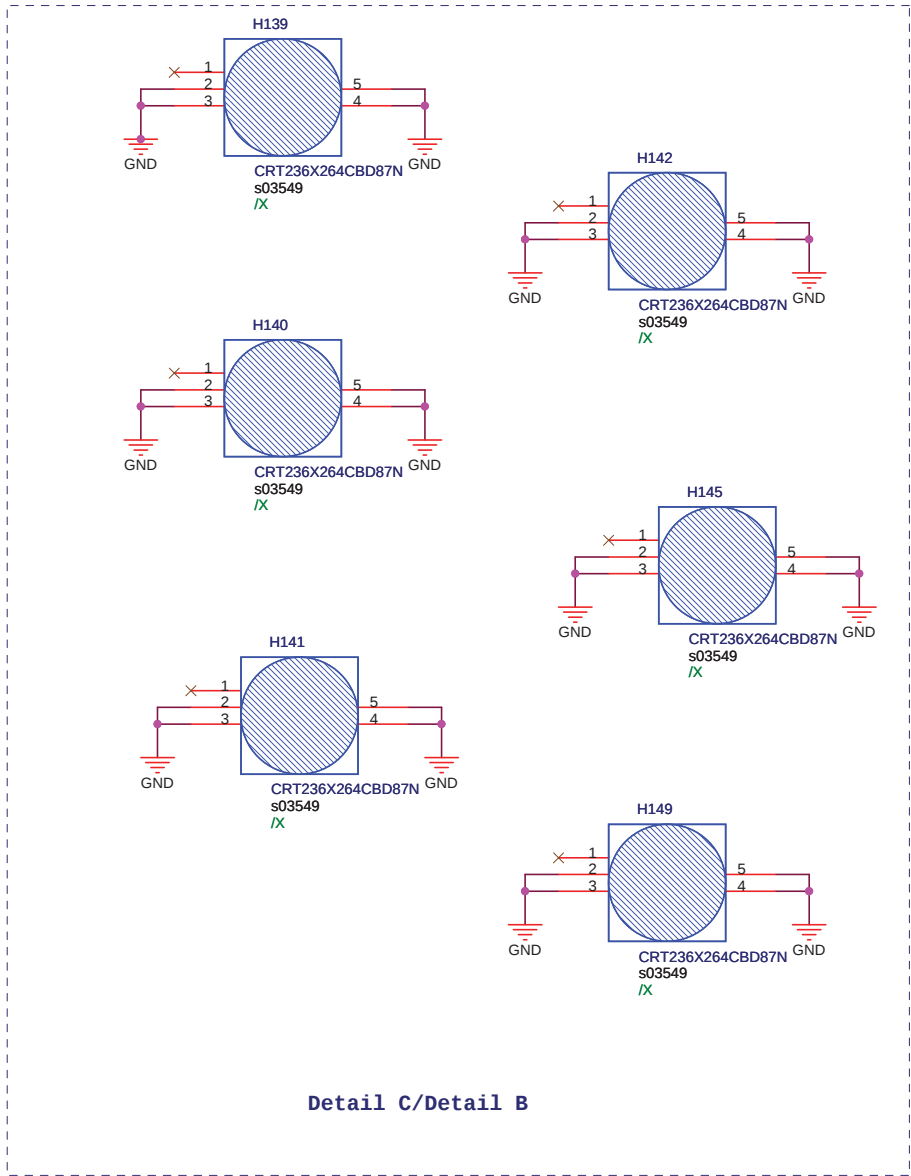
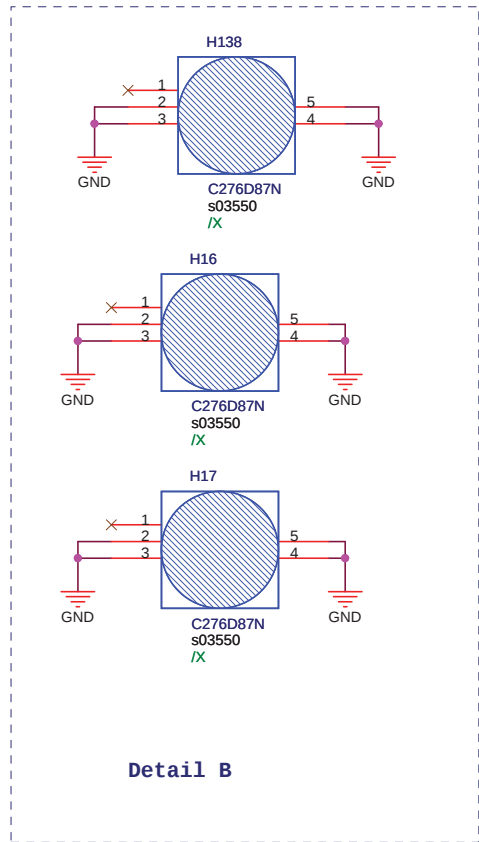
DC IN



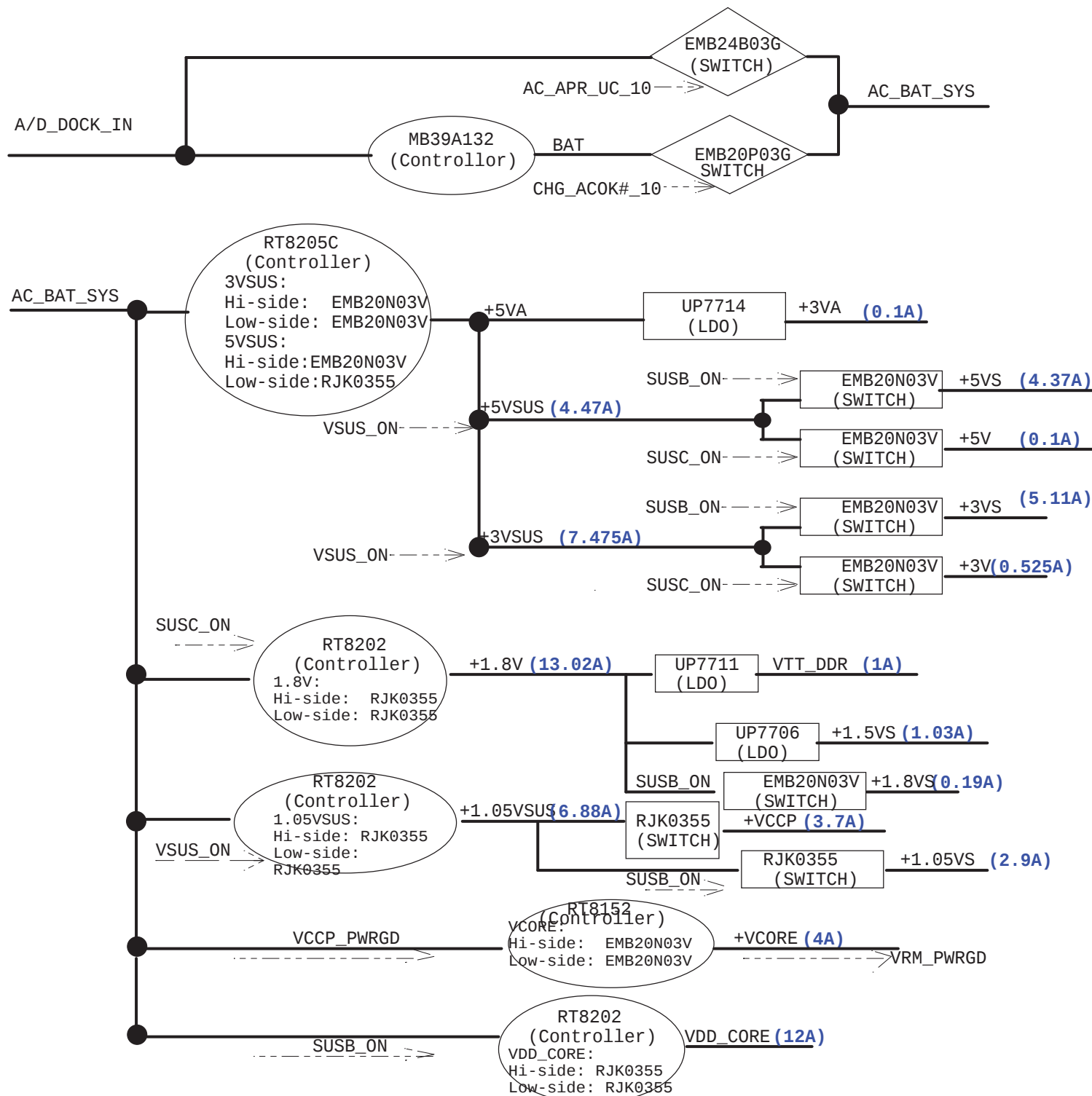
Internal BAT

<Variant Name>

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1201I		Rev 1.0
Date: Friday, August 28, 2009		Sheet	38 of 54

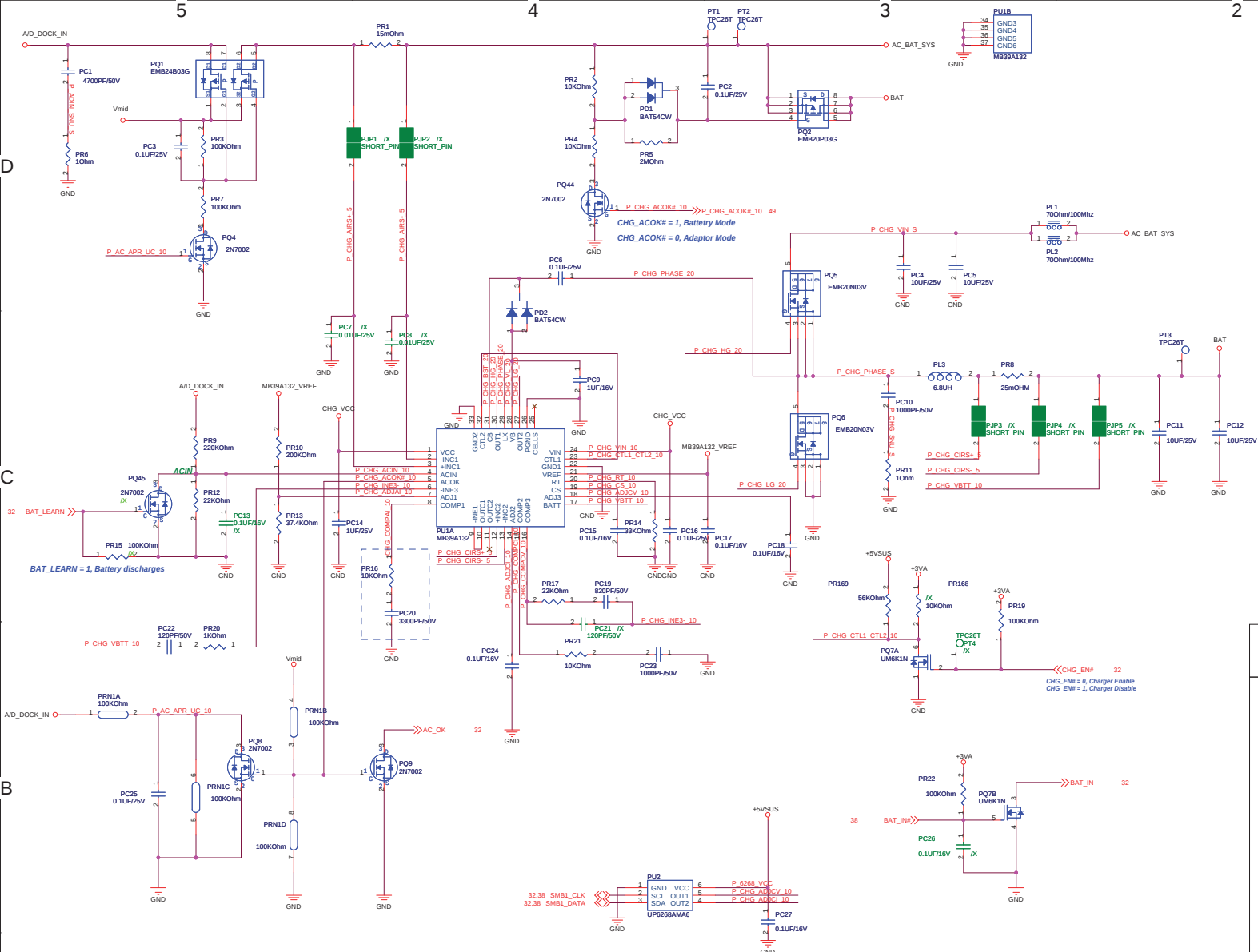


<Variant Name>		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
Custom	12011	1.0	
Date: Thursday, September 03, 2009		Sheet	39 of 54



<Variant Name>

ASUS		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Jerry Liu	
Size A3	Project Name 12011	Rev 1.2	
Date: Wednesday, August 26, 2009		Sheet 40 of 54	

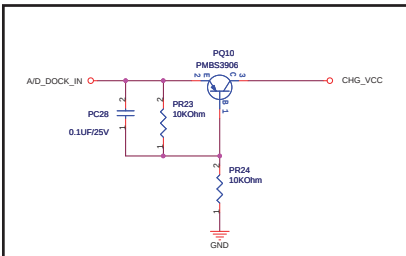


Power stage

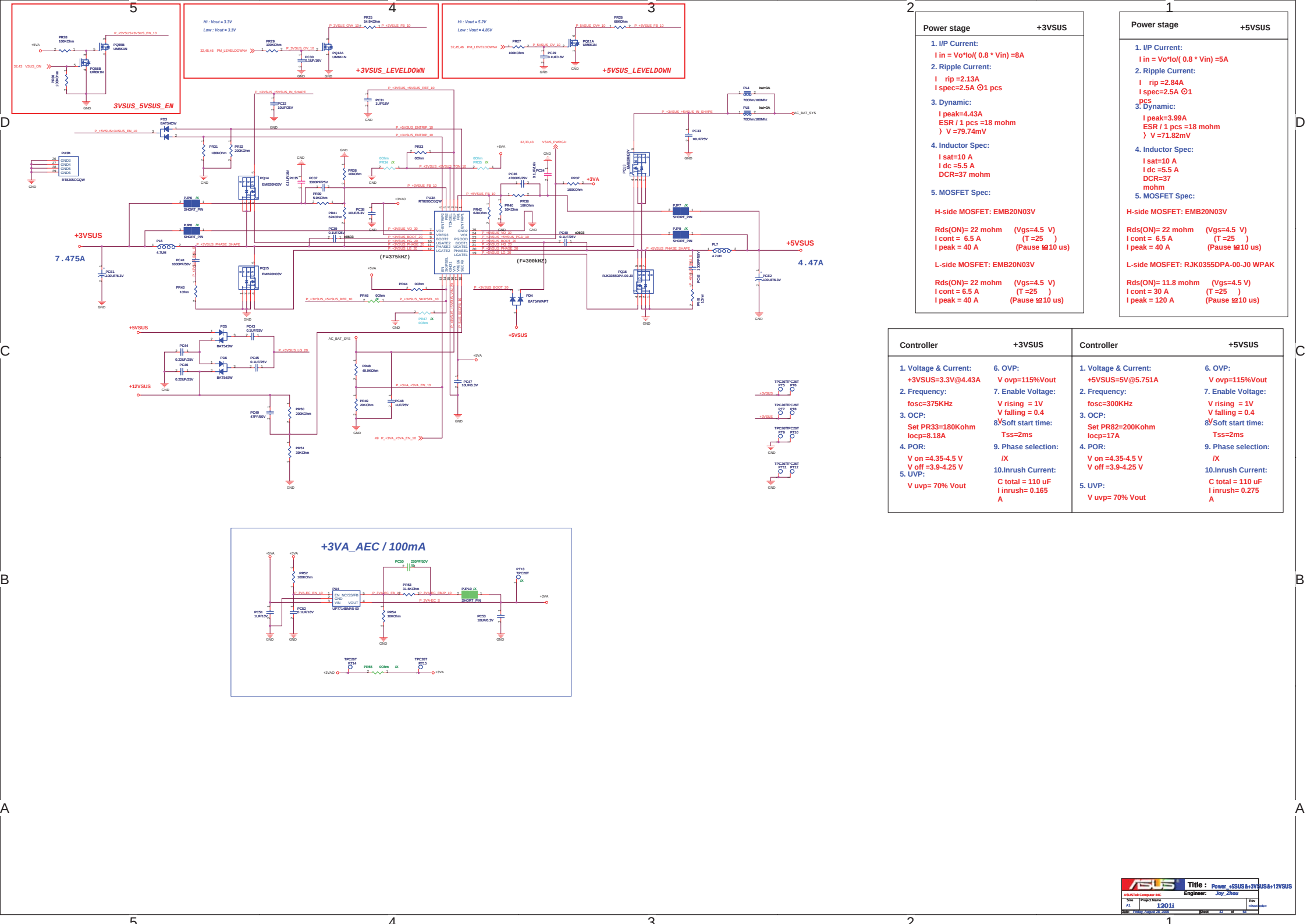
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$
- Ripple Current:**
 $I_{ripple} = 0.875A$
 $I_{spec} = 2A \text{ } \phi 1 \text{ pcs}$
- Inductor Spec:**
 $I_{sat} = 8A$
 $I_{dc} = 4.5A$
 $DCR = 60m\Omega$
- MOSFET Spec:**
H-side MOSFET: EMB20N03V
 $R_{ds(ON)} = 22m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10us$)
L-side MOSFET: EMB20N03V
 $R_{ds(ON)} = 22m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\geq 10us$)

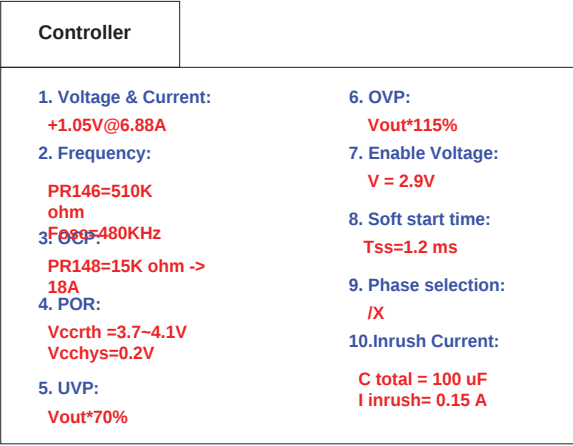
Controller

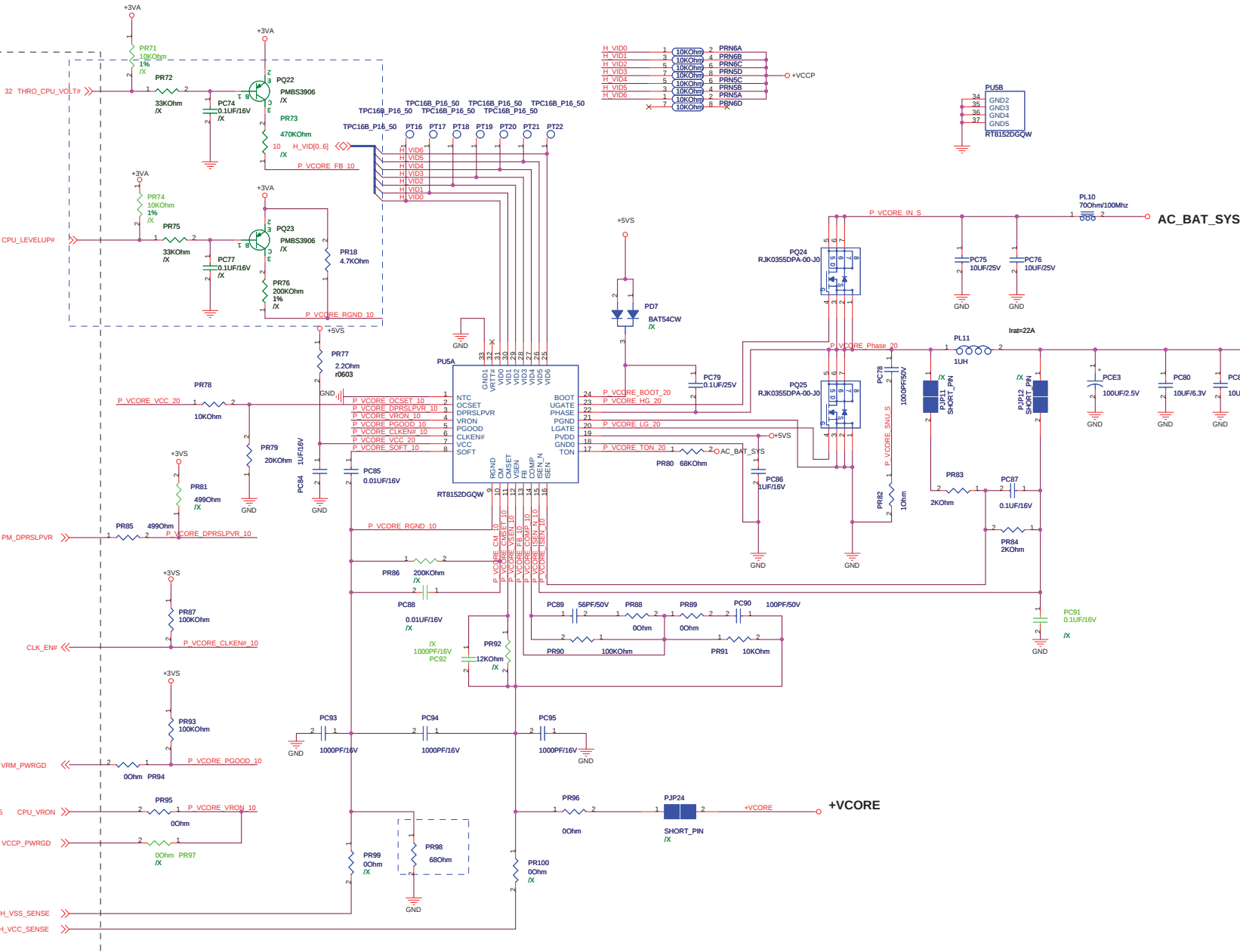
- Voltage & Current:**
 $+12.6V @ 2.5A$
- Frequency:**
 $PR122 = 33K\Omega$,
 $F_{osc} = 17000 / RT(K\Omega) = 515KHz$
- OC:**
 $POR \text{ Hysteresis} = 0.1V$
 $V_{on} = 7.5V$
- Enable Voltage:**
 $V = 2.9V$
- Soft start time:**
 $T_{ss} = 23ms$
- Phase selection:**
 N/A
- Inrush Current:**
 $C_{total} = 20\mu F$
 $I_{inrush} = 0.01A$



Battery Charging Current : $I_{chg} = (V_{adj} - 0.075) / (25 \cdot R_s)$ Input Adaptor Max. Current Limit : $I_{limit_current} = (V_{adj} - 0.075) / (25 \cdot R_s) = 1.90A$	ACIN Threshold = 1.25V Adaptor > 13.75V, System Powered by Adaptor Adaptor < 13.75V, System Powered by Battery	Battery Charging Voltage : $V_{adj3} : V_{REF} \Rightarrow V_{bat} = 4.2V / cell$ $3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} = 4.35V / cell$ $V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / cell$ $2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 \cdot V_{adj3} / cell$ Battery Cell Selection : $CELLS : V_{REF} \Rightarrow 4 \text{ Cells;}$ $CELLS : OPEN \Rightarrow 3 \text{ Cells;}$ $CELLS : GND \Rightarrow 2 \text{ Cells;}$	VREF = 5.0V $f_{osc}(KHz) = 17000 / RT(K\Omega)$ $Soft \ start : ts(s) = 0.23 \cdot CS(\mu F)$
---	---	--	---







Power stage

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.89 \text{ A}$
2. Ripple Current:
Ripple=3A
3. Ripple Voltage:
 $V_{ripple} = \text{Ripple} \cdot \text{ESR} = 54 \text{ mV}$
4. Dynamic:
 $I_{peak} = 8.5 \text{ A}$
 $\text{ESR} = 18 \text{ m}\Omega$
 $V = 153 \text{ mV}$
5. Inductor Spec:
 $I_{sat} = 15 \text{ A}$
 $I_{dc} = 8 \text{ A}$
 $\text{DCR} = 18 \text{ m}\Omega (\text{type}) / 20 \text{ m}\Omega (\text{max})$
6. MOSFET Spec:
H-side and L-side
MOSFET: RJK0355DPA-00-J0 WPAK

$R_{ds(ON)} = 11.8 \text{ m}\Omega$ ($V_{gs} = 4.5 \text{ V}$)
 $I_{cont} = 30 \text{ A}$ ($T = 25^\circ \text{C}$)
 $I_{peak} = 120 \text{ A}$ (Pause $\geq 10 \text{ us}$)

Controller

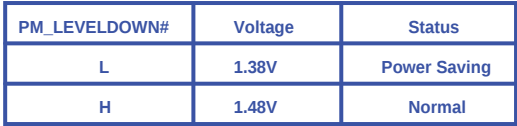
1. Voltage & Current:
+Vcore: 1.1V/8.5A
2. Frequency:
 $R_{ton} = 68 \text{ k}\Omega$
 $F_{sw} = 480 \text{ KHz}$ $V_{in} = 6 \text{ V}$
3. OCP:
 $\text{DCR} \cdot I_{max} \cdot (PR235 / (PR232 + PR235)) = 83.3 \text{ mV}$
 $I_{max} = 16.6 \text{ A}$
4. On time:
 $T_{on} = 265 - 580 \text{ ns}$
5. Load Line:
 $R_{cs} = PR84 / (PR83 + PR84) \cdot R_{dcr} = 5 \text{ m}\Omega$

THRO_CPU_VOLT#	CPU_LEVELUP#	Voltage	Status
L	H	VID-50mV	Power Saving
H	H	VID	Normal
H	L	VID+50mV	Performance

<Variant Name>

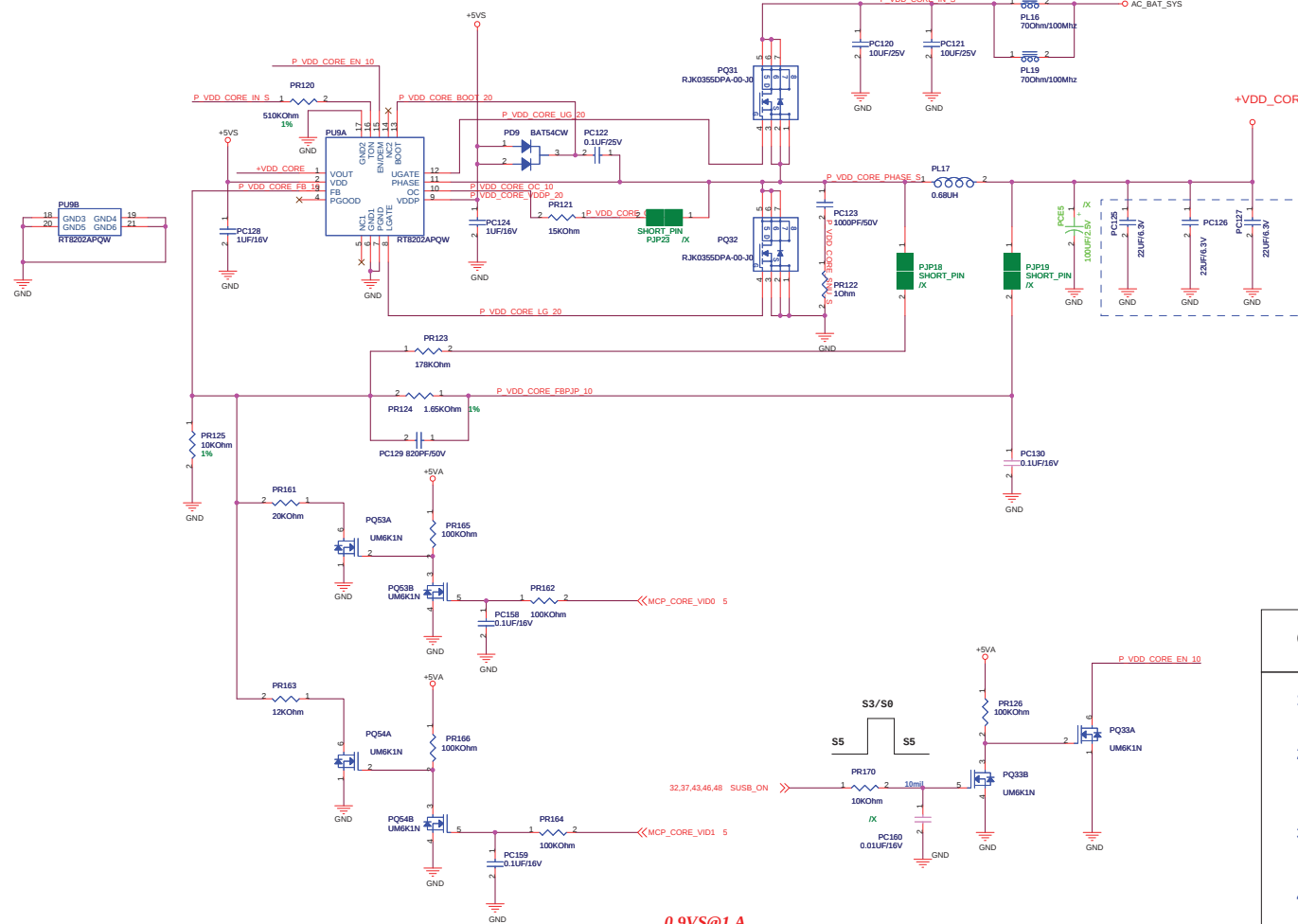
ASUS® Title: POWER_VCORE_RT8152
ASUSTek COMPUTER INC. NB Engineer: Joy_zhou

Size C Project Name 12011 Rev 1.0
Date: Friday, August 28, 2009 Sheet 44 of 54



PM_LEVELDOWN#	Voltage	Status
L	1.38V	Power Saving
H	1.48V	Normal

1. Dropout Voltage:
 $V = 300 \text{ mV}$ ($I_o = 2 \text{ A}$)
2. Current Limit:
 $I_{\text{limit}} = 2.8 \text{ A}$
3. Continue Current:
 $I_{\text{cont}} = 1 \text{ A}$
4. Pd:
 $R_{\text{thjc}} = 5 \text{ C/W}$
 $P_d = 1.9 \text{ W}$
5. EN Voltage:
 $V_{\text{rising}} = 1.4 \text{ V}$
 $V_{\text{falling}} = 0.4 \text{ V}$
6. Supply Voltage:
 $V_{\text{cc}} = 5 \text{ V}$
7. Inrush current:
 $T_{\text{ss}} = 4 \text{ ms}$
 $C_{\text{total}} = 20 \text{ uF}$
 $I_{\text{inrush}} = 7.5 \text{ mA}$



Power stage

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.7A$$

2. Ripple Current:

$$I_{rip} = 2.72A$$

$$I_{spec} = 2.5A$$

3. Dynamic:

$$I_{peak} = 6.8A$$

$$ESR / 1 \text{ pcs} = 18 \text{ mohm}$$

$$V = 122.4mV$$

4. Inductor Spec:

$$I_{SAC} = 25.5A$$

$$IDC = 15.5A$$

$$DCR = 5mohm$$

5. MOSFET Spec:

H-side MOSFET: RJK0355DPA-00-J0

$$R_{ds(ON)} = 16.5 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 30A \quad (T = 25^\circ C)$$

$$I_{peak} = 120A \quad (\text{Pause} \geq 10 \mu s)$$

L-side MOSFET: RJK0355DPA-00-J0

$$R_{ds(ON)} = 16.5 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 30A \quad (T = 25^\circ C)$$

$$I_{peak} = 120A \quad (\text{Pause} \geq 10 \mu s)$$

Controller

1. Voltage & Current:

$$+1.8V @ 6.8A$$

2. Frequency:

$$PR120 = 510K \text{ ohm}$$

$$F_{osc} = 480KHz$$

$$PR121 = 18K \text{ ohm} \rightarrow 13.6A$$

3. POR:

$$V_{ccrth} = 3.7 \sim 4.1V$$

$$V_{cclys} = 0.2V$$

4. UVP:

$$V_{out} * 70\%$$

6. OVP:

$$V_{out} * 115\%$$

7. Enable Voltage:

$$V = 2.9V$$

8. Soft start time:

$$T_{ss} = 1.2 \text{ ms}$$

9. Phase selection:

$$/X$$

10. Inrush Current:

$$C_{total} = 100 \mu F$$

$$I_{inrush} = 0.15A$$

0.9VS@1 A

1. Dropout Voltage:

$$V = 0.3V \quad (I_o = 2A)$$

2. Current Limit:

$$I_{limit} = 4A$$

3. Continue Current:

$$I_{cont} = 3A$$

4. Power Dissipation:

$$R_{thjc} = 52$$

$$/W$$

$$P_d = 1.9W$$

5. EN Voltage:

$$V_{en} = 1.4V$$

$$V_{sd} = 0.8V$$

6. Supply Voltage:

$$V_{cc} = 5V$$

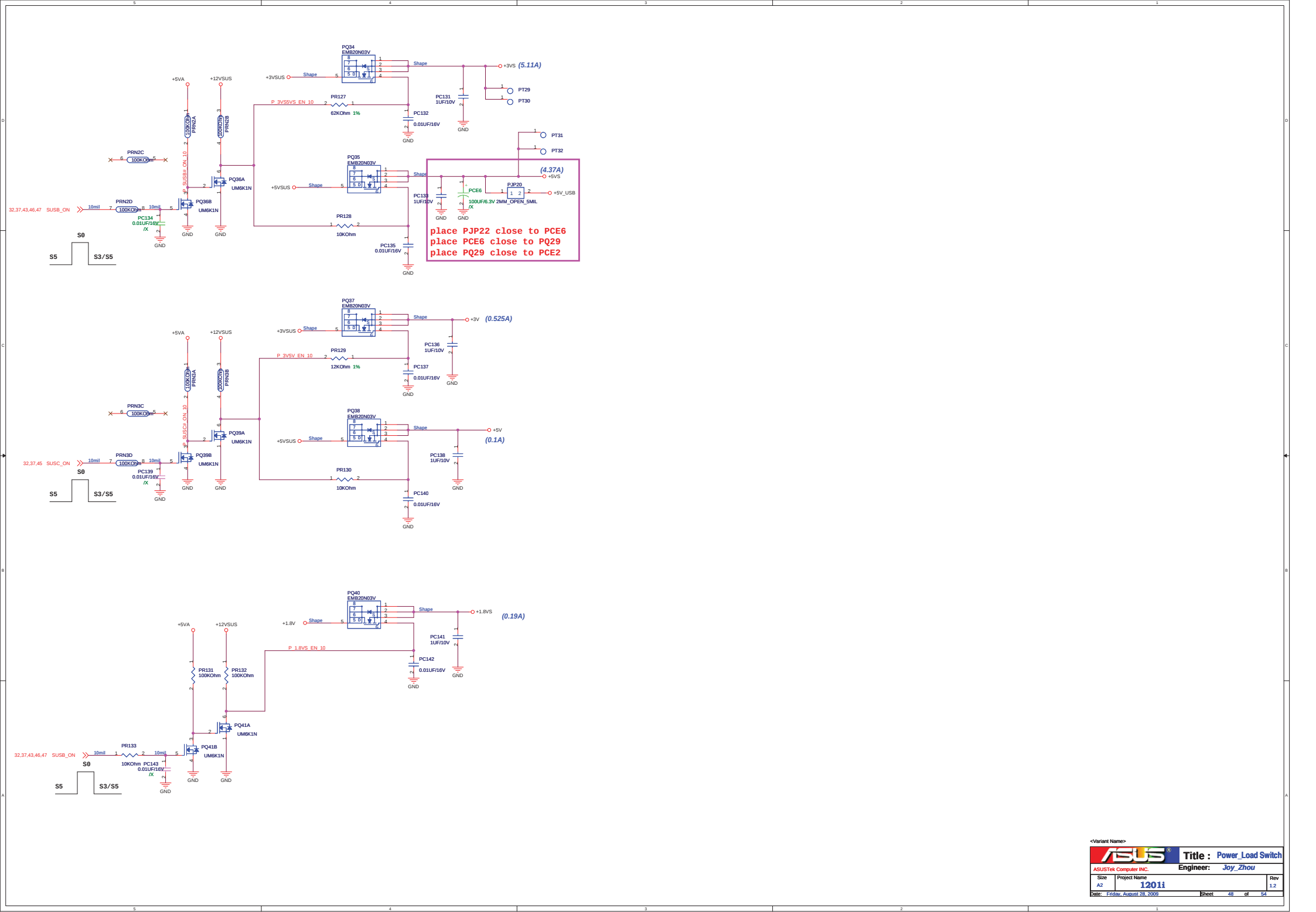
7. Inrush current:

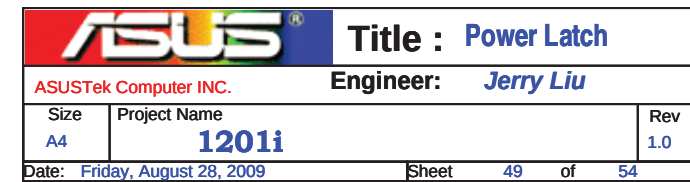
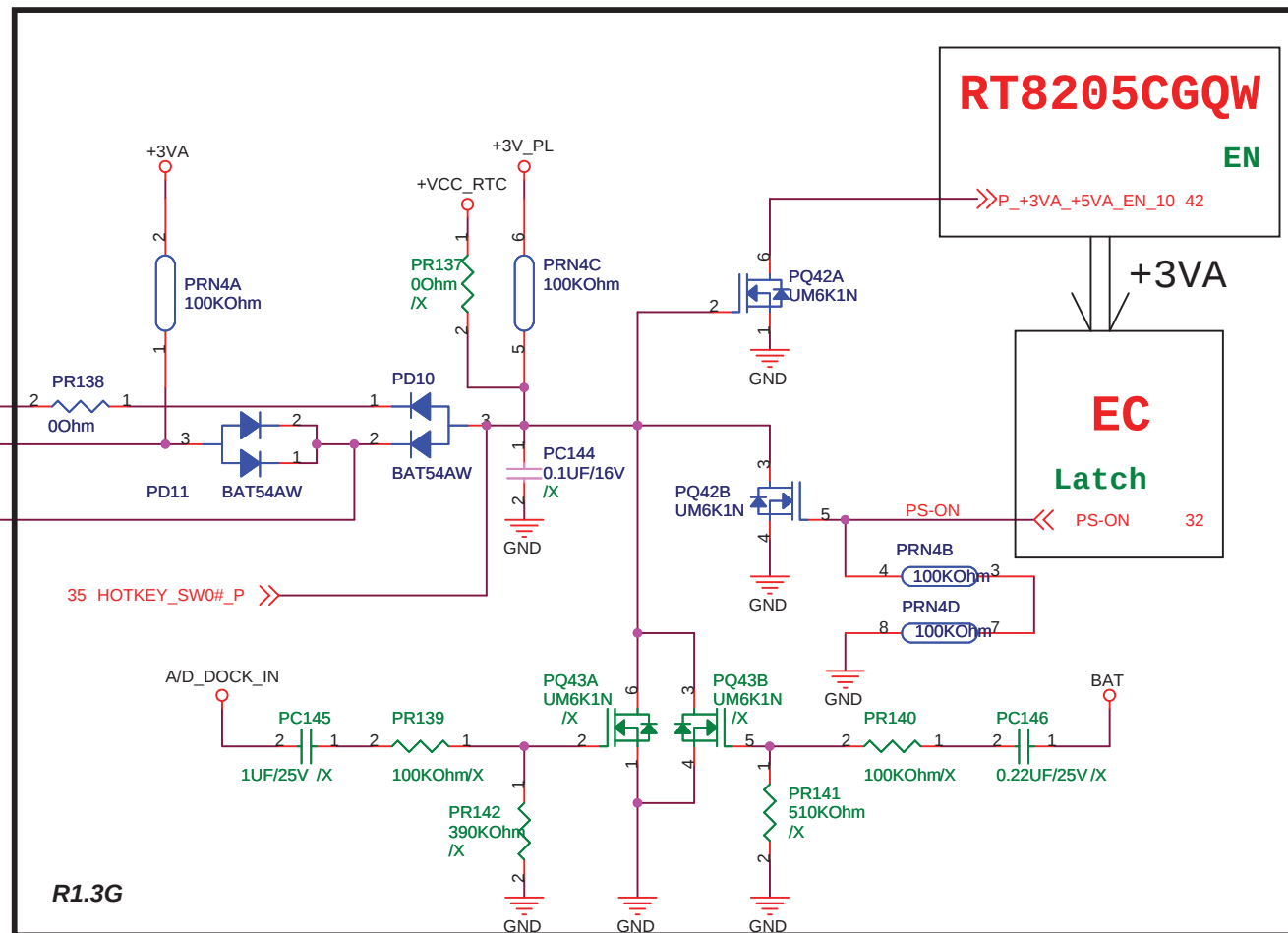
$$T_{ss} = 5ms$$

$$C_{total} = 10 \mu F$$

$$I_{inrush} = 3mA$$

VID2	VID1	VID0	Voltage	Status
L	L	L	0.88V	N/A
L	L	H	1V	Normal
L	H	L	0.95V	Performance
L	H	H	0.9V	Power Saving





5	4	3	2	1
D				D
C				C
B				B
A				A

DATE 0706

- 1. P40,Delete some EMI CAP,add RF CAP EC58
- 2. P23,3G_RST# PU POWER change from +3VS to +3V_3G
- 3. P15,SCH_GPIO_0 PD R93 change from 10k to 1K
- 4. P16,+5VS_REF ADD serial R109
- 5. P22,+3V_LCD ADD GR15/PQ40
- 6. P23,+3V_3G GR21/GR22 change to 0805
- 7. P35,L26 change to 0 OHM
- 7. P7,CLK_PCIE_3G/CLK_PCIE_3G# add reserved CAP C476/C477

DATE 0707

- 1. P13,SDVO BUS/PCIE add net name before capacitor
- 2. P22,LVDS CON change part number to 12G17101020K
- 3. P40, add EMI CAP EC52/EC54
- 3. P29, add power switch for debug

DATE 0708

- 1.Delete test point T27/T28
- 2.ADD D6/OR30
- 3.Add net name for PCIE BUS

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	LPC_RST#	I	
14	GPIO07	CRT_IN	I	100K pull high to +3VA
15	GPIO08	EXT_SMI#	O	
16	GPIO0A	LID_EC_R#	I	Internal pull high
17	GPIO0B/ESB_CLK	PCB_ID0	I	8.2K pull down to GND
18	GPIO0C/ESB_DAT	PCB_ID1	I	8.2K pull down to GND
19	GPIO0D	LID_EC_L#(no use)	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	O	10K pull high to +3VSUS
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#(no use)	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	100K pull high to +3VSUS
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM(no use)	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH(no use)	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX(no use)	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX(no use)	I	RS232 debug port
32	GPIO18	PWR_SW_EC#	I	100K pull high to +3VA
34	GPIO19/PWM3	PS-ON	O	latch power, 200K pull down to GND
36	GPIO1A/NUMLED	NUM_LED#(no use)	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#(no use)	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A(no use)	I	
64	GPI39/AD1	BAT_B(no use)	I	
65	GPIO3A/AD2	BAT_C(no use)	I	
66	GPIO3B/AD3	BAT_D(no use)	I	
68	GPO3C/DA0	CHG_EN#	O	100K pull high to +3VA

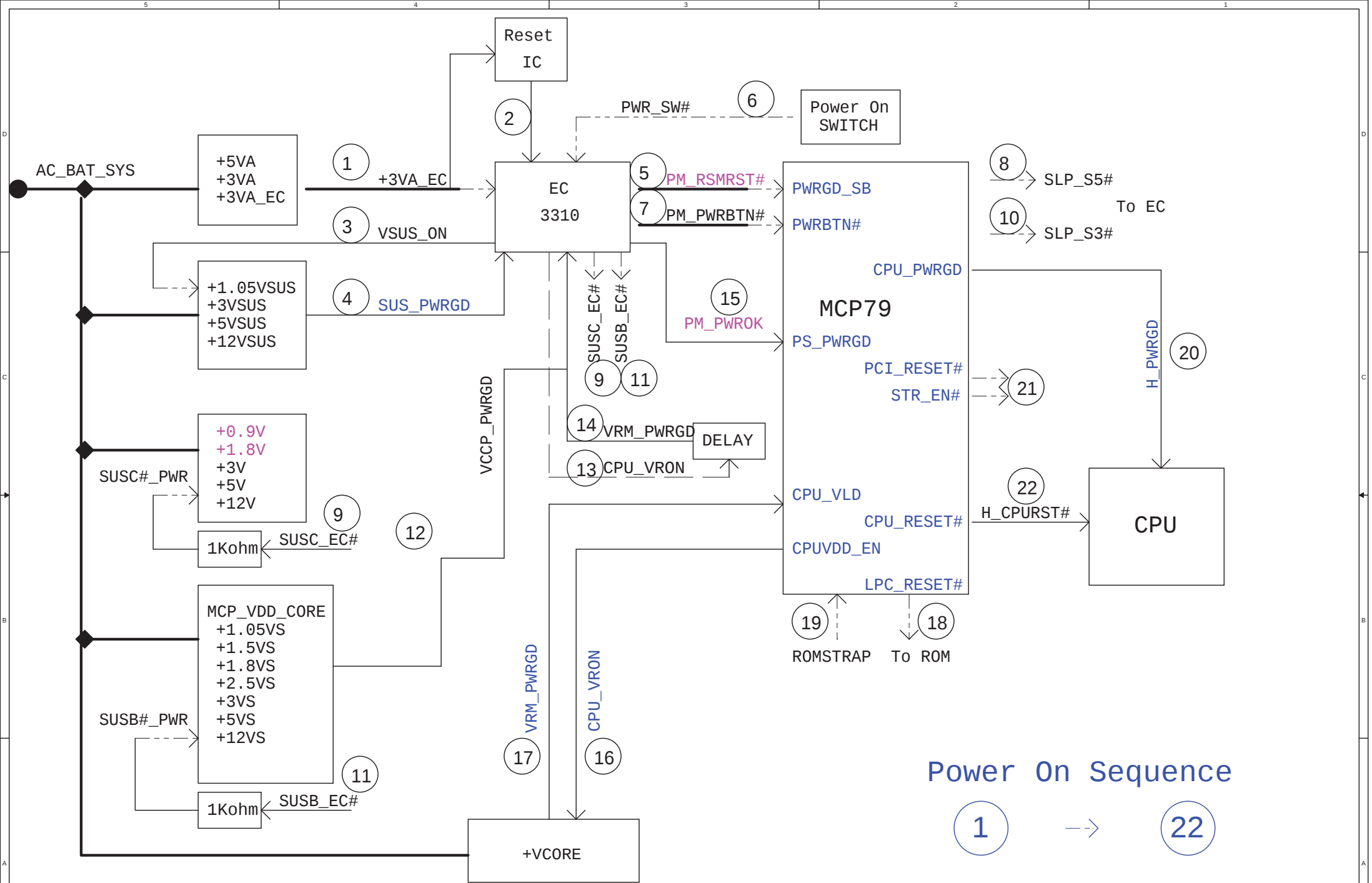
EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_KBCLPC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
67	ECRST#	EC_RST#	I	100K pull high to +3VA
69	AVCC	+3VA_AEC	P	
94	AGND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_DO	I	
120	WR#/SPIDO	SPI_DI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	K_V18R	P	Reserved 4.7uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	Default High
72	GPO3F/DA3	BAT_LL#(NO USE)	O	Battery Low Low
73	GPIO40	AC_OK	I	100K pull high to +3VA
74	GPIO41	EC_RSMRST#	O	100K pull down to GND
75	GPI42	BAT_IN	I	100K pull high to +3VA
76	GPI43	BAT2_IN(no use)	I	Batt1 (Small/Internal): 1-present, 0-absent (to GND)
77	GPIO44/SC1	SMB1_CLK	I/OD	4.7K pull high to +3VA
78	GPIO45/SDA1	SMB1_DATA	I/OD	4.7K pull high to +3VA
79	GPIO46/SC2	SMB2_CLK	I/OD	10K pull high to +3VS
80	GPIO47/SDA2	SMB2_DATA	I/OD	10K pull high to +3VS
81	GPIO48/KSO16	KB_ID0(no use)	I	for KB type detection
82	GPIO49/KSO17	KB_ID1(no use)	I	for KB type detection
83	GPIO4A/PSCLK1	1.8_OV	O	10K pull down to GND; default low
84	GPIO4B/PSDAT1	NC	I	
85	GPIO4C/PSCLK2	NC	O	
86	GPIO4D/PSDAT2	NC	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3VS
88	GPIO4F/PSDAT3	TP_DATA	I/OD	10K pull high to +3VS
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_ORANGE#	O	Orange charger LED
91	GPIO53/CAPLED	CAPS_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLLED	SCRL_LED#(no use)	O	
95	GPIO56	GS1_INT1(no use)	I	Internal pull high
97	GPIOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON_EC	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#(no use)	O	
103	GPXOA06	PM_LEVELDOWN#	O	Default High
104	GPXOA07	CNT2_CHG#(no use)	O	
105	GPXOA08	CNT2_CHG#(no use)	O	
106	GPXOA09	SPI_WP#	O	10K pull high to +3VA
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	100K pull down to GND
109	GPXID0/SDIDI	EC_PWROK	O	100K pull down to GND
110	GPXID1	CPU_LEVELUP#	O	Default High
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SUSB#	I	100K pull down to GND
115	GPXID4	PM_SUSC#	I	100K pull down to GND
116	GPXID5	VRM_PWRGD_EC	I	100K Pull high to +3VS
117	GPXID6	VSUS_PWRGD	I	100K Pull high to +3VA
118	GPXID7	NC	O	
121	GPIO57	GS1_INT2(no use)	I	Internal pull high
126	GPIO58/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

<Variant Name>

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S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for AC_OK until adaptor power is good, then
- 2.At least 5mS after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.
- 3.At least 20mS after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)
- 4.EC asserts RSTWARN.
- 5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 6.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.
- 7.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 8.CPU_VRON is deasserted at least 100mS after SUSB power is stable.
- 9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 10.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 11.Waiting for RSTRDY# until deasserted by SCH.
- 12.RESET# can be deasserted at lease 100uS after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for BAT_IN until battery power is good, then
- 2.Waiting for PWR_SW# until user is pressed.
- 3.EC asserts VSUS_ON to enable VSUS power.
- 4.At least 20mS after VSUS power is stable.
- 5.EC asserts RSTWARN.
- 6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.
- 8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.
- 10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 12.Waiting for RSTRDY# until deasserted by SCH.
- 13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

- 1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).

2.At least 20mS after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.

- 3.Waiting for SLPRDY# until has been asserted.

- 4.EC asserts RSTWARN to SCH to begin internal sequence.

- 5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.

- 6.EC asserts RESET# after detecting RSTRDY# asserted.

- 7.EC deasserts ICH_PWROK.

- 8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

- 9.EC asserts PM_RSMRST#.
- 10.EC deasserts SUSC_ON to turn off the other power planes.
- 11.EC deasserts VSUS_ON if in battery mode.
- 12.EC deasserts RSTWARN to save more power.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

- 1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.
- 2.For external wake event (PWR_SW#, keyboard wake up), then
- 3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.
- 4.EC asserts SUSB_ON to enable SUSB power.
- 5.CPU_VRON is deasserted at least 100mS after SUSB power is stable.
- 6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 7.At least 5mS after receiving CPUPWR_GD, ICH_PWROK is asserted.
- 8.Deasserts RSTWARN after ICH_PWROK is asserted.
- 9.RESET# can be deasserted 100uS after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# for 1200uS to SCH after asserts RSTWARN.
- 4.EC deasserts RSTWARN.
- 5.EC deasserts RESET# after at least 100uS delay from RSTWARN.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# to SCH after asserts RSTWARN.
- 4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.
- 5.EC asserts PM_RSMRST# after CPU_VRON power is off.
- 6.EC disables SUSC_ON power for 3~5 seconds.
- 7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.