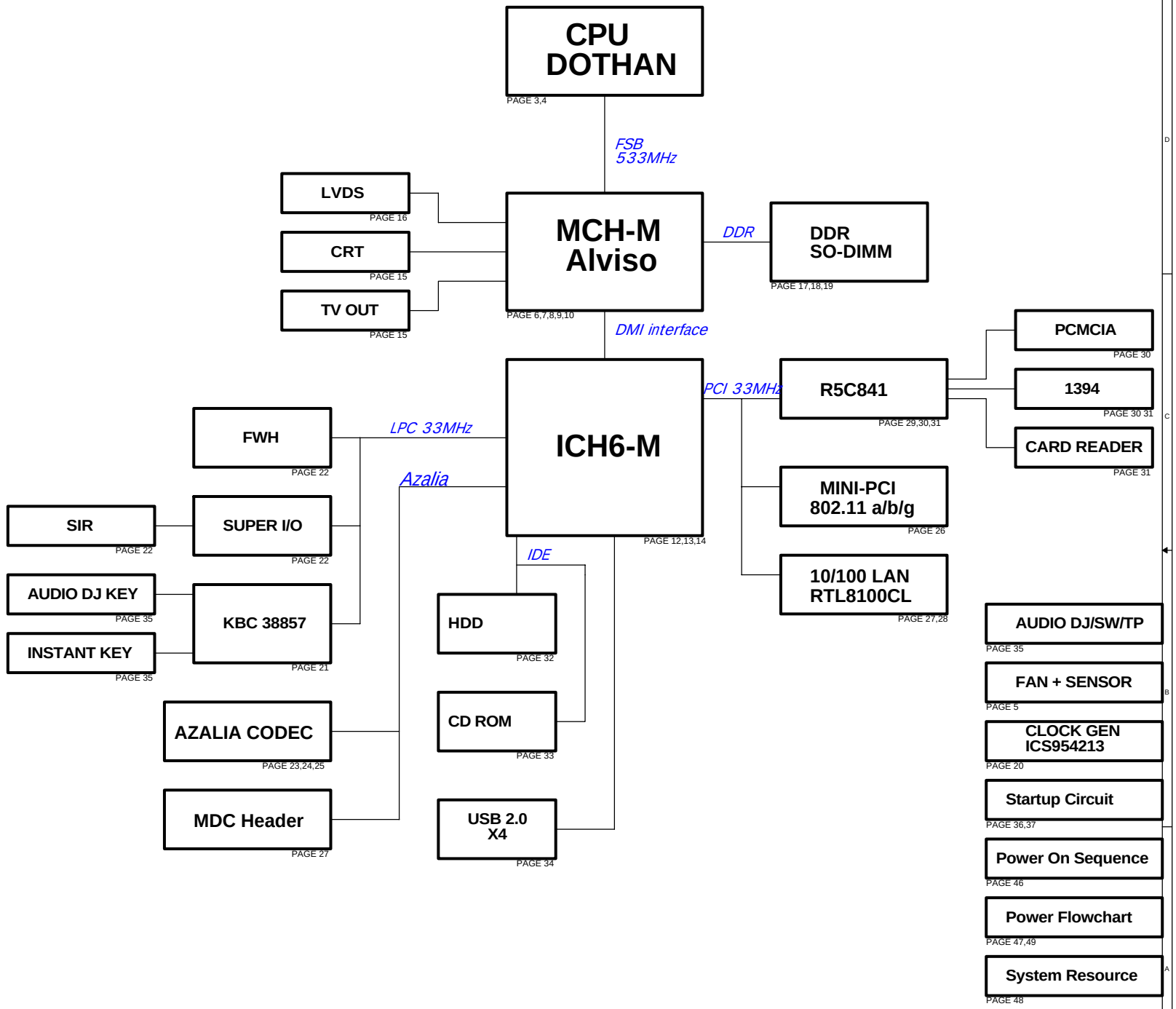
A3A CONTEXT



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 1 of 50	

REVISION LIST

R1.0 2005/01/10

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
~~+1.5VSUS~~	~~1.5V~~	~~270 mA~~
+2.5V	2.5V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 18 mils

37.5 OHM WIDTH

TOP/BOT 11 mils
IN1/IN2 9.5 mils

50 OHM WIDTH

TOP/BOT 6 mils
IN1/IN2 5 mils

55 OHM WIDTH

TOP/BOT 5.5 mils
IN1/IN2 4.5 mils

75 OHM WIDTH

TOP/BOT 4 mils
IN1/IN3 3.5 mils

Differential

85 OHM WIDTH/SPACE

TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils

90 OHM WIDTH/SPACE

TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils

110 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 GND
L3 IN1
L4 IN2
L5 GND
L6 BOT

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```
SIGNAL  IN:   VR_VID[0..5]
              PM_DPRSLPVR
              STP_CPU#
              PM_PSI#
              CPU_VRON
              MCH_OK
        OUT:  DELAY_VR_PWRGD
              CLK_PWR_GD#

POWER   IN:   AC_BAT_SYS
              +5VO
              +3VO
        OUT:  +VCORE
```

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```
SIGNAL   IN:  SUSC#_PWR
              VSUS_ON

POWER    IN:  AC_BAT_SYS

         OUT: +12VO
              +3VO
              +5VO
```

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```
SIGNAL  IN: SUSB#_PWR
            SUSC#_PWR
            CPU_VRON

POWER   IN: AC_BAT_SYS
            +5VO

       OUT: +1.8V
            +1.5VS
            +2.5VS
            +VCC_GMCH_CORE
            +5VALWAYS
            +3VALWAYS
            +VCCP
```

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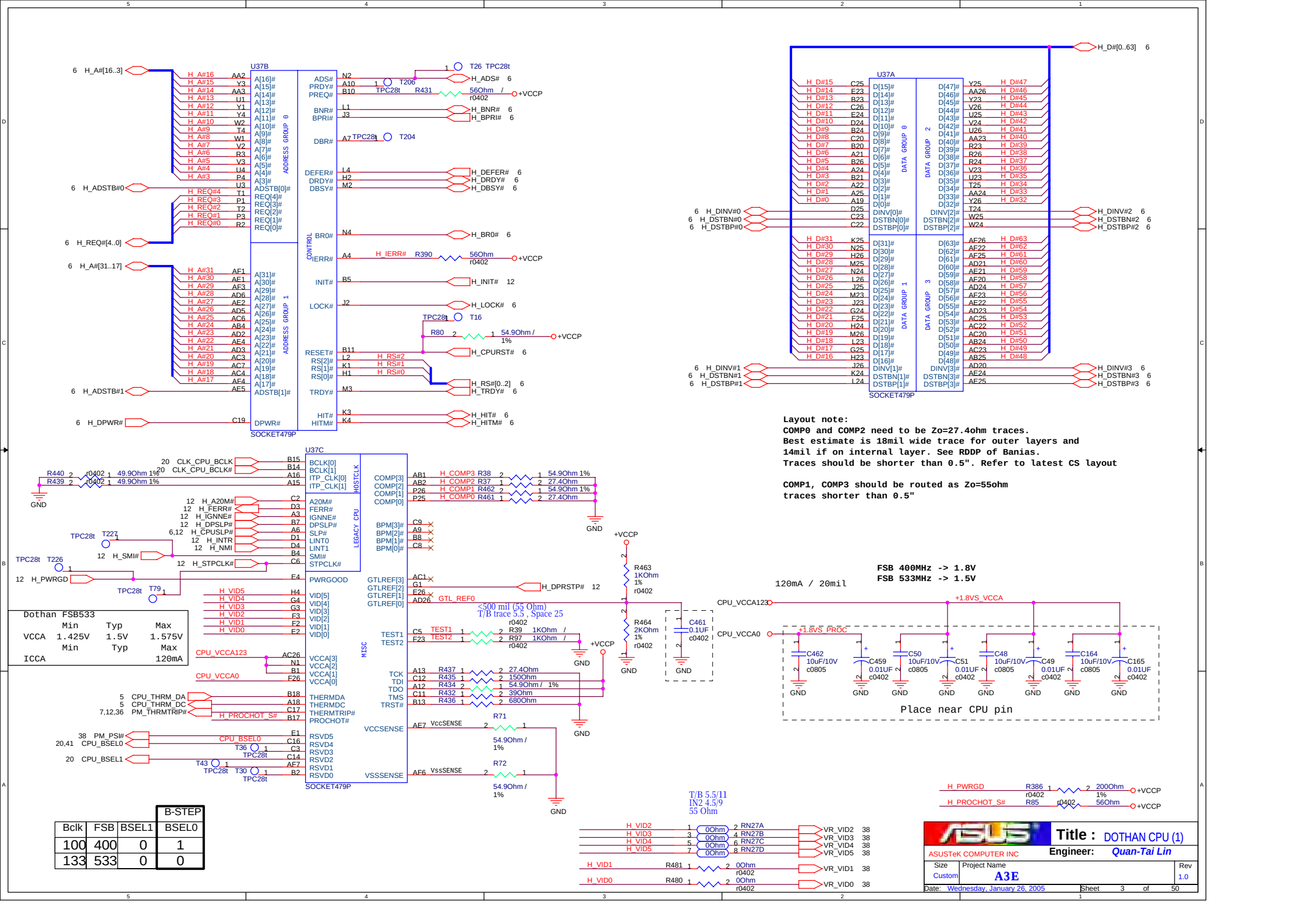
```
SIGNAL  IN: SUSB#_PWR

POWER   IN: +3V
            +1.8V

       OUT: +0.9VS
```

ASUSTeK COMPUTER INC	Title : REVISION LIST	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 2 of 50	


U37B
SOCKET479P
U37A
SOCKET479P
U37C
SOCKET479P
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
FSB 400MHz -> 1.8V
FSB 533MHz -> 1.5V
120mA / 20mil
Place near CPU pin
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
Bclk FSB BSEL1 B-STEP BSEL0
100 400 0 1
133 533 0 0
Title : DOTHAN CPU (1)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 3 of 50

Dothan FSB533	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

+VCCP

+VCORE

U37D

VCC

SOCKET479P

U37E

GND

SOCKET479P

GND

GND

MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

+VCCP

CE4 150U/4.0V
C100 0.1UF c0402
C442 0.1UF c0402
C99 0.1UF c0402
C441 0.1UF c0402
C127 0.1UF c0402
C412 0.1UF c0402
C407 0.1UF c0402
C128 0.1UF c0402
C408 0.1UF c0402
C443 0.1UF c0402
C414 10uF/10V c0805
C434 10uF/10V c0805

GND

+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

ASUSTeK COMPUTER INC	Title : DOTHAN CPU (2)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 4 of 50	

Fan Speed Control

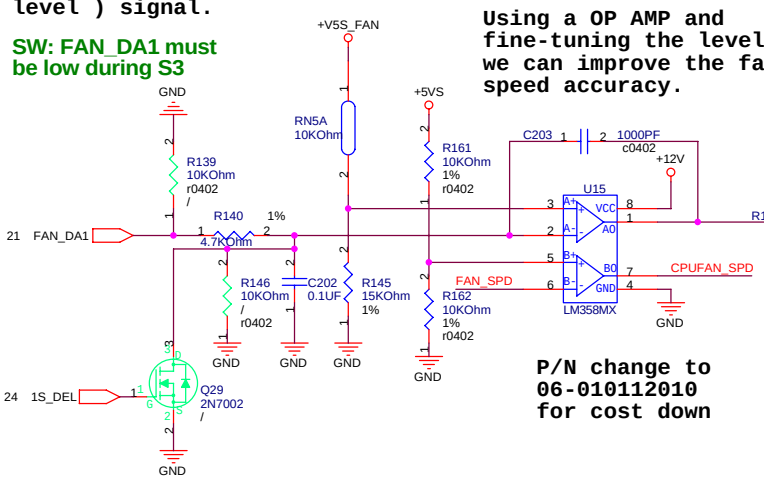
CPU FAN

KBC will issue a analog (a voltage level) signal.

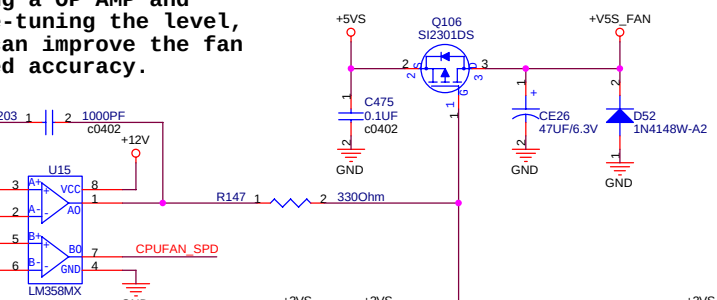
SW: FAN_DA1 must be low during S3

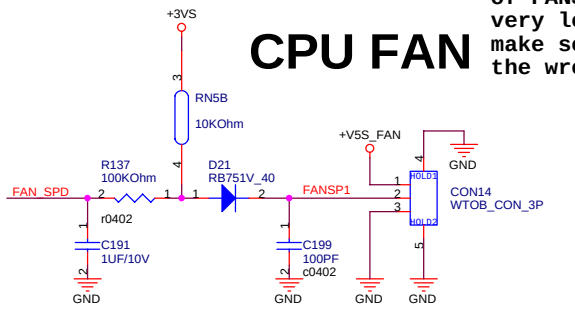
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

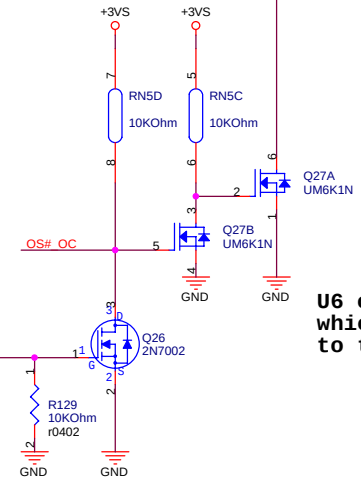
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

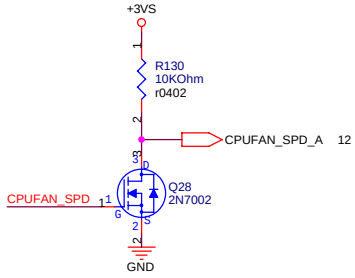


P/N change to 06-010112010 for cost down









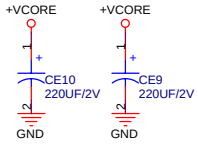
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

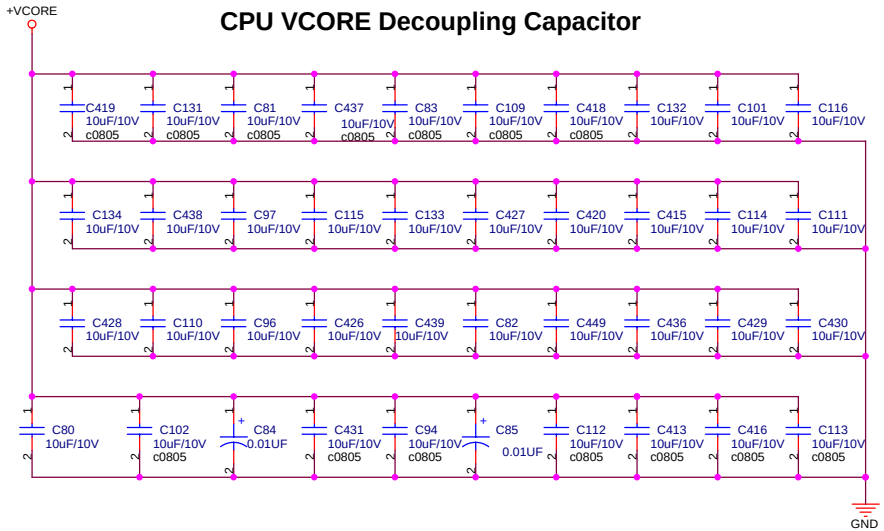
Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



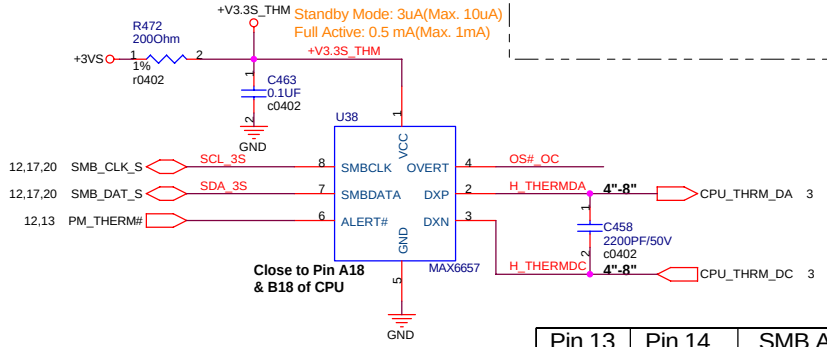
CPU VCORE Decoupling Capacitor



Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

Four 200 uF are located in IMVP4

Title : THER-SENSOR,FAN

ASUSTeK COMPUTER INC Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 5 of 50

In OrCAD circuit,ALVISO PM P/N :02-010002600

But we have to use ALVISO GM P/N : 02-010002610 in BOM list

H_XRCOMP 12/20mils

R380 24.9Ohm 1% — GND

+VCCP

R379 54.9Ohm 1%

H_XSCOMP 5.5/20 mils

+VCCP

R414 221Ohm 1% r0402

H_XSWING 12/20mils

R413 100Ohm 1% r0402 — C398 0.1UF c0402 — C399 10uF/10V c0805 — GND

H_YRCOMP 12/20mils

R433 24.9Ohm 1% — GND

+VCCP

R420 54.9Ohm 1%

H_YSCOMP 5.5/20 mils

+VCCP

R429 221Ohm 1% r0402

H_YSWING 12/20mils

R430 100Ohm 1% r0402 — C405 0.1UF c0402 — C409 10uF/10V c0805 — GND

3 H_D#[0..63]

U36D — HOST — ALVISO_BGA1257

H_D#0	E4	HD0#	
H_D#1	E1	HD1#	
H_D#2	F4	HD2#	
H_D#3	H7	HD3#	
H_D#4	F2	HD4#	
H_D#5	F1	HD5#	
H_D#6	E3	HD6#	
H_D#7	D3	HD7#	
H_D#8	K7	HD8#	
H_D#9	F2	HD9#	
H_D#10	J7	HD10#	
H_D#11	J8	HD11#	
H_D#12	H6	HD12#	
H_D#13	F3	HD13#	
H_D#14	K8	HD14#	
H_D#15	H5	HD15#	
H_D#16	H1	HD16#	
H_D#17	H2	HD17#	
H_D#18	K5	HD18#	
H_D#19	K6	HD19#	
H_D#20	J4	HD20#	
H_D#21	G3	HD21#	
H_D#22	H3	HD22#	
H_D#23	J1	HD23#	
H_D#24	L5	HD24#	
H_D#25	K4	HD25#	
H_D#26	J5	HD26#	
H_D#27	P7	HD27#	
H_D#28	L7	HD28#	
H_D#29	J3	HD29#	
H_D#30	P5	HD30#	
H_D#31	L3	HD31#	
H_D#32	U7	HD32#	
H_D#33	V6	HD33#	
H_D#34	R6	HD34#	
H_D#35	R5	HD35#	
H_D#36	P3	HD36#	
H_D#37	T8	HD37#	
H_D#38	R7	HD38#	
H_D#39	R8	HD39#	
H_D#40	U8	HD40#	
H_D#41	R4	HD41#	
H_D#42	T4	HD42#	
H_D#43	T5	HD43#	
H_D#44	R1	HD44#	
H_D#45	T3	HD45#	
H_D#46	V8	HD46#	
H_D#47	U6	HD47#	
H_D#48	W6	HD48#	
H_D#49	U3	HD49#	
H_D#50	V5	HD50#	
H_D#51	W8	HD51#	
H_D#52	W7	HD52#	
H_D#53	U2	HD53#	
H_D#54	U1	HD54#	
H_D#55	Y5	HD55#	
H_D#56	Y2	HD56#	
H_D#57	V4	HD57#	
H_D#58	Y7	HD58#	
H_D#59	W1	HD59#	
H_D#60	W3	HD60#	
H_D#61	Y3	HD61#	
H_D#62	Y6	HD62#	
H_D#63	W2	HD63#	

H_XRCOMP	C1	HXRCOMP	
H_XSCOMP	C2	HXSCOMP	
H_XSWING	D1	HXSWING	
H_YRCOMP	T1	HYRCOMP	
H_YSCOMP	L1	HYSCOMP	
H_YSWING	P1	HYSWING	

HA3#	G9	H_A#3	
HA4#	C9	H_A#4	
HA5#	F9	H_A#5	
HA6#	B7	H_A#6	
HA7#	A10	H_A#7	
HA8#	F9	H_A#8	
HA9#	D8	H_A#9	
HA10#	B10	H_A#10	
HA11#	E10	H_A#11	
HA12#	G10	H_A#12	
HA13#	D9	H_A#13	
HA14#	E11	H_A#14	
HA15#	F10	H_A#15	
HA16#	G11	H_A#16	
HA17#	G13	H_A#17	
HA18#	C10	H_A#18	
HA19#	C11	H_A#19	
HA20#	D11	H_A#20	
HA21#	C12	H_A#21	
HA22#	B13	H_A#22	
HA23#	A12	H_A#23	
HA24#	F12	H_A#24	
HA25#	G12	H_A#25	
HA26#	E12	H_A#26	
HA27#	C13	H_A#27	
HA28#	B11	H_A#28	
HA29#	D13	H_A#29	
HA30#	A13	H_A#30	
HA31#	F13	H_A#31	

H_A#[31..3] 3

HADS#	F8	H_ADS#	H_ADS# 3
HADSTB0#	B9	H_ADSTB#0	H_ADSTB#0 3
HADSTB1#	E13	H_ADSTB#1	H_ADSTB#1 3
HVREF	J11		H_VREF
HBNR#	A5	H_BNR#	H_BNR# 3
HBPR#	D5	H_BPRI#	H_BPRI# 3
HBREQ0#	E7	H_BREQ#0	H_BR0# 3
HCPURST#	H10	H_CPURST#	H_CPURST# 3

HCLKINN	AB1		CLK_MCH_BCLK# 20
HCLKINP	AB2		CLK_MCH_BCLK 20
HDBSY#	C6	H_DBSY#	H_DBSY# 3
HDEFER#	E6		H_DEFER# 3
HDINV0#	H8	H_DINV#0	H_DINV#0 3
HDINV1#	K3	H_DINV#1	H_DINV#1 3
HDINV2#	T7	H_DINV#2	H_DINV#2 3
HDINV3#	U5	H_DINV#3	H_DINV#3 3
HDPWR#	G6		H_DPWR# 3
HDRDY#	F7		H_DRDY# 3
HDSTBN0#	G4	H_DSTBN#0	H_DSTBN#0 3
HDSTBN1#	K1	H_DSTBN#1	H_DSTBN#1 3
HDSTBN2#	R3	H_DSTBN#2	H_DSTBN#2 3
HDSTBN3#	V3	H_DSTBN#3	H_DSTBN#3 3
HDSTBP0#	G5	H_DSTBP#0	H_DSTBP#0 3
HDSTBP1#	K2	H_DSTBP#1	H_DSTBP#1 3
HDSTBP2#	R2	H_DSTBP#2	H_DSTBP#2 3
HDSTBP3#	W4	H_DSTBP#3	H_DSTBP#3 3
HEDRDY#	F6	TP_H_EDRDY#	T35 TPC28t
HHIT#	D4		H_HIT# 3
HHITM#	D6		H_HITM# 3
HLOCK#	B3		H_LOCK# 3
HPCREQ#	A11	TP_H_PCREQ#	T199 TPC28t
HREQ0#	A7	H_REQ#0	H_REQ#[4..0] 3
HREQ1#	D7	H_REQ#1	
HREQ2#	B8	H_REQ#2	
HREQ3#	C7	H_REQ#3	
HREQ4#	A8	H_REQ#4	
HRS0#	A4	H_RS#0	H_RS#[0..2] 3
HRS1#	C5	H_RS#1	
HRS2#	B4	H_RS#2	
HCPUSLP#	G8	R42 1 — 2 0Ohm r0402	H_CPUSLP# 3,12
HTRDY#	B5		H_TRDY# 3

+VCCP

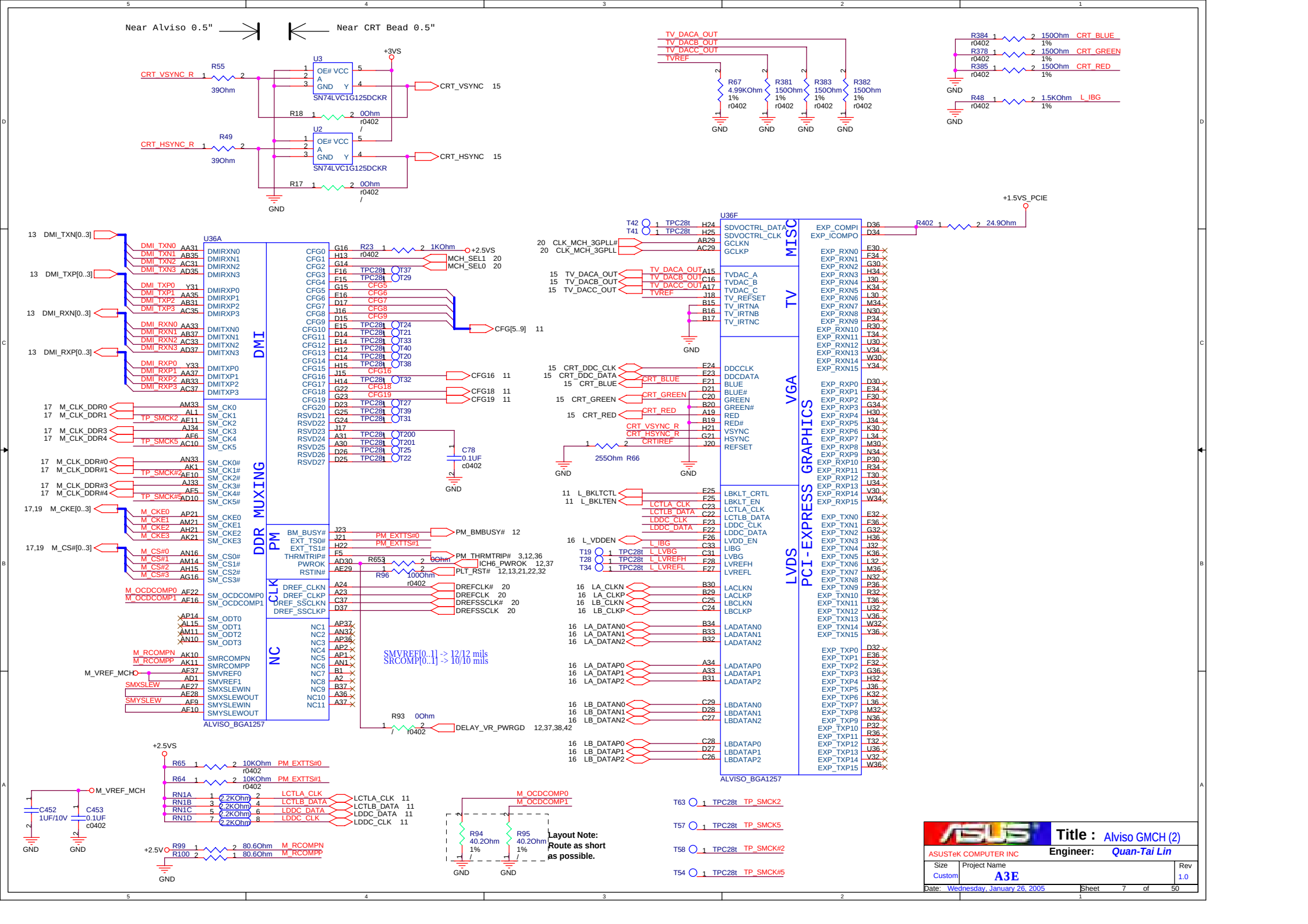
R74 100Ohm 1% r0402 — <500 mil (55 Ohm) T/B trace 5.5 , Space 25

H_VREF

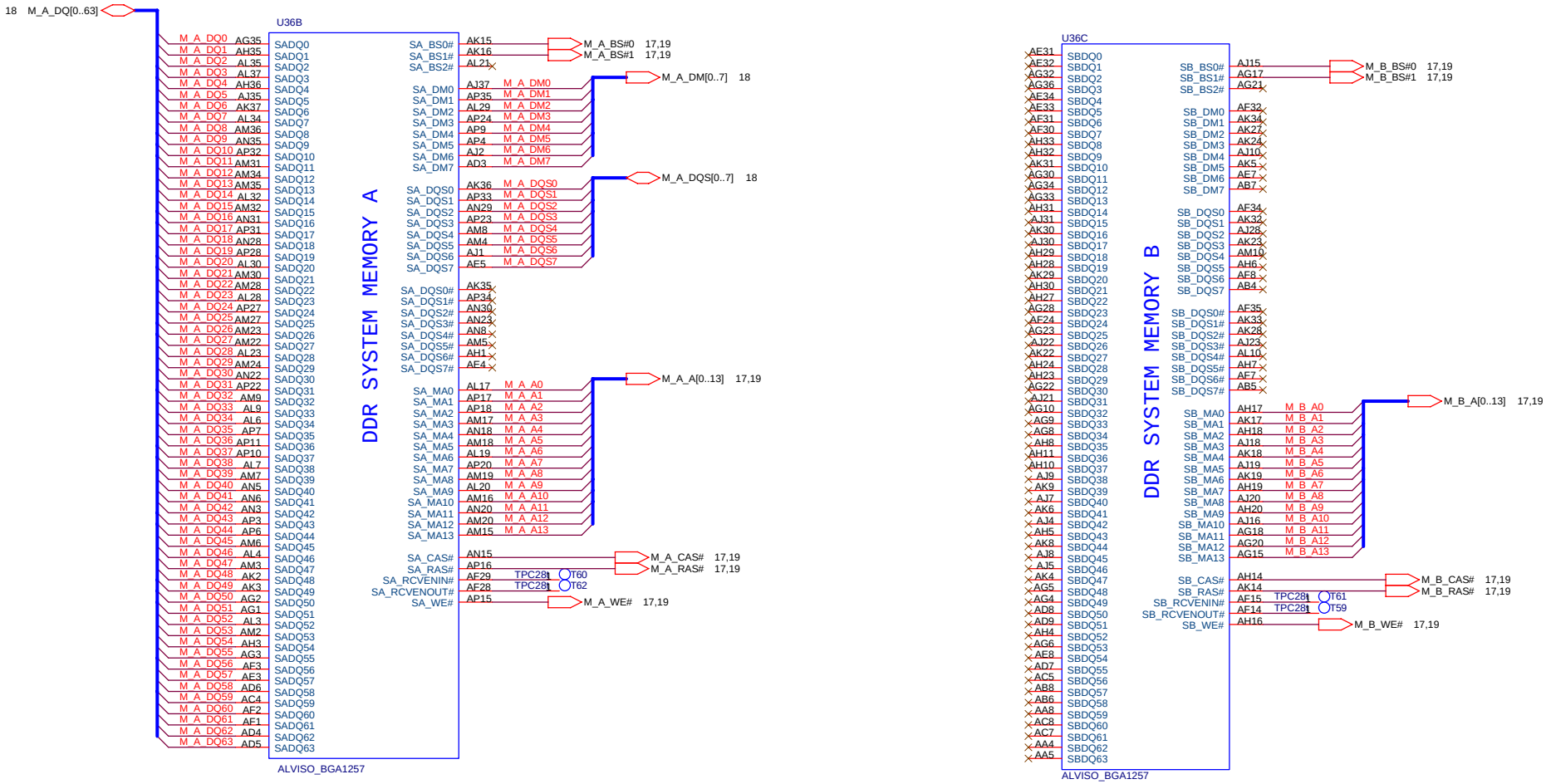
R70 200Ohm r0402 1% — C77 0.1UF c0402 — GND

Dothan A : R282 NO STUFF

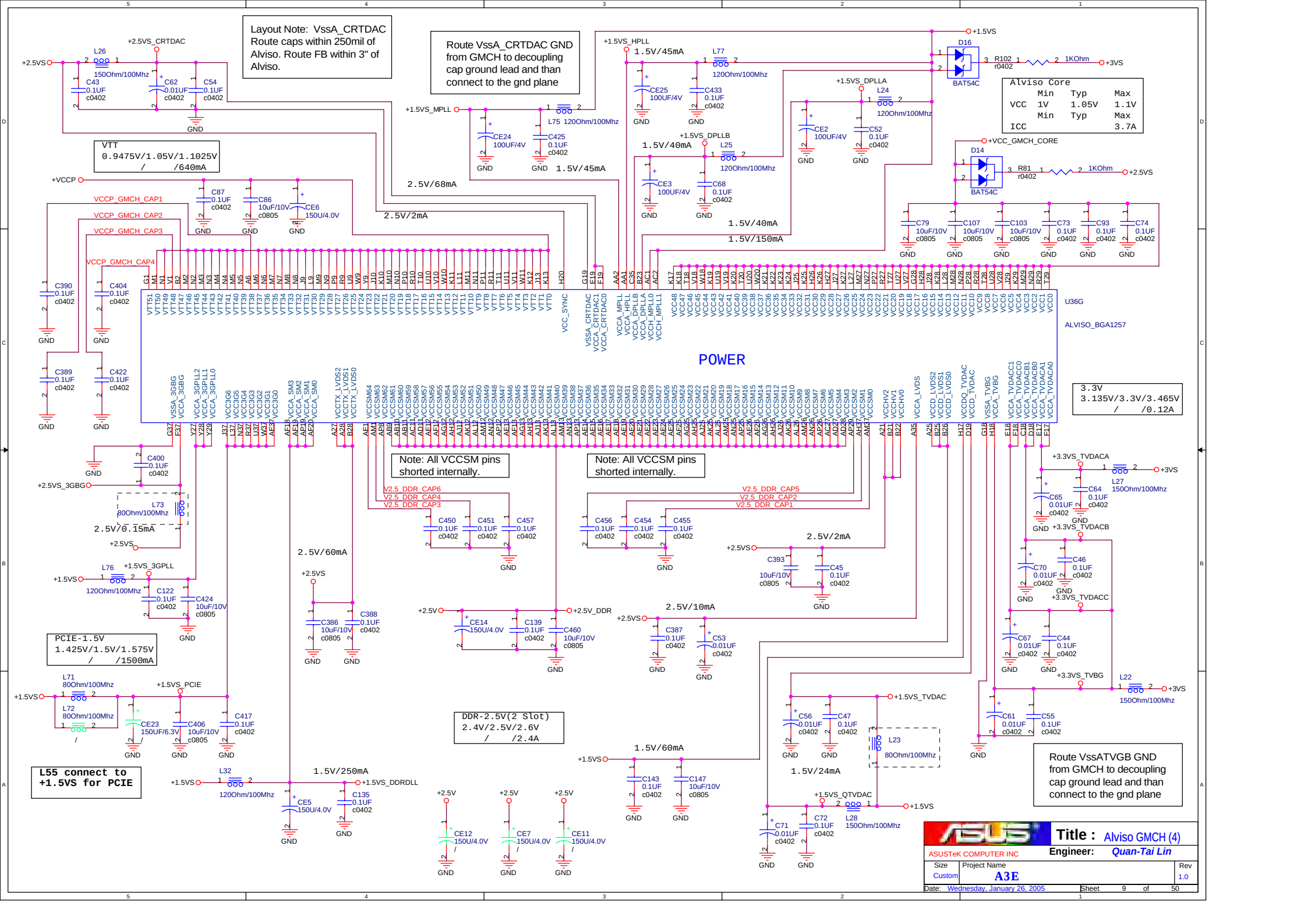
Title : Alviso GMCH (1)		
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 6 of 50	

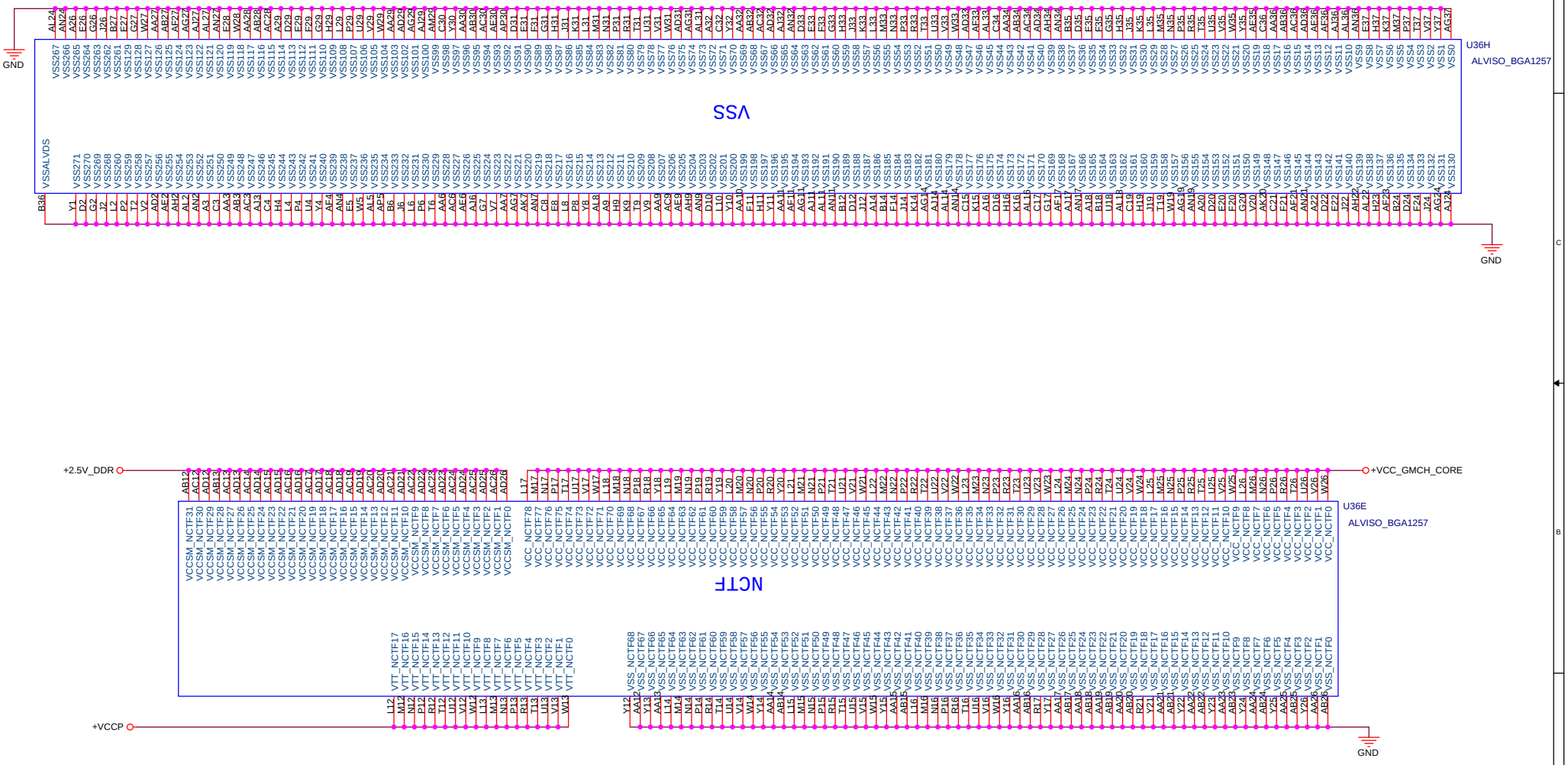


Title :	Alviso GMCH (2)
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E
Rev: 1.0	
Date: Wednesday, January 26, 2005	Sheet 7 of 50



ASUSTeK COMPUTER INC	Title : Alviso GMCH (3)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 8 of 50		


Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Alviso Core
Min Typ Max
VCC 1V 1.05V 1.1V
Min Typ Max
ICC 3.7A
VTT
0.9475V/1.05V/1.1025V
/ /640mA
POWER
U36G
ALVISO_BGA1257
3.3V
3.135V/3.3V/3.465V
/ /0.12A
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PCIE-1.5V
1.425V/1.5V/1.575V
/ /1500mA
DDR-2.5V(2 Slot)
2.4V/2.5V/2.6V
/ /2.4A
L55 connect to +1.5VS for PCIE
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Title : Alviso GMCH (4)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 9 of 50

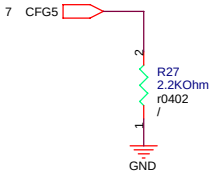


ASUSTeK COMPUTER INC	Title : Alviso GMCH (5)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 10 of 50		

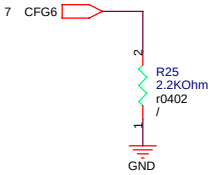
CFG[2:0] are HVCMOS (+2.5VS)
CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
CFG[19..18] have internal pulldown resistors./HVCMOS(+2.5VS)/
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

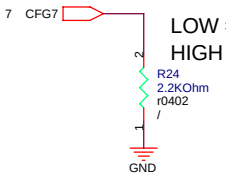
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



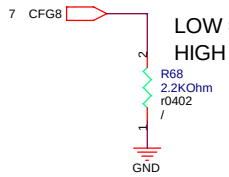
CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)



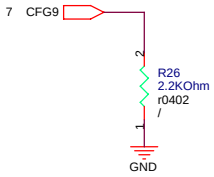
CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



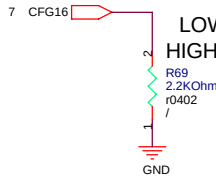
CFG8 : PCI-X POWER Saving
LOW = PCI-X POWER Saving
HIGH (Default)



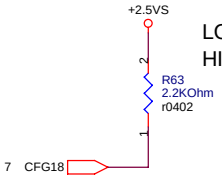
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



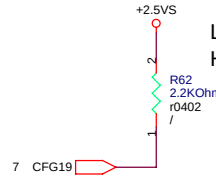
CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

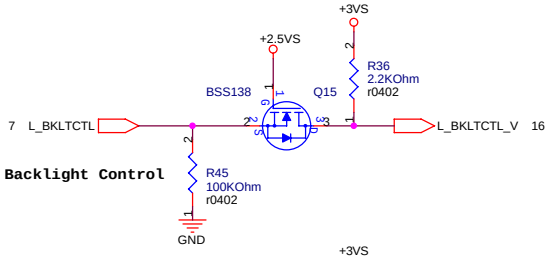


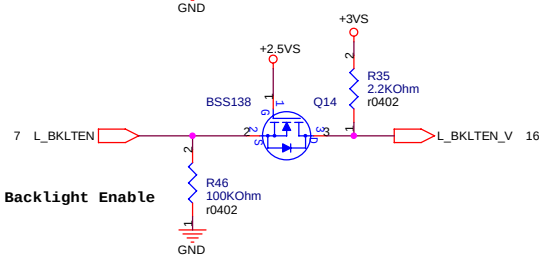
CFG18 : VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V

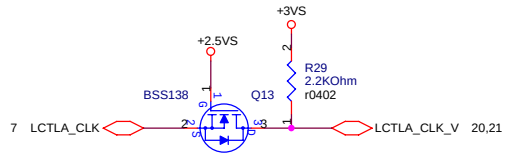


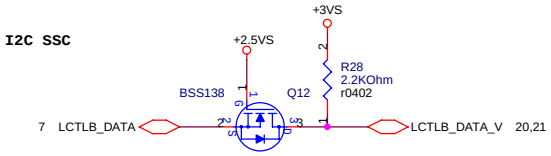
CFG19 : VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V

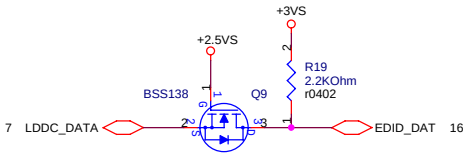


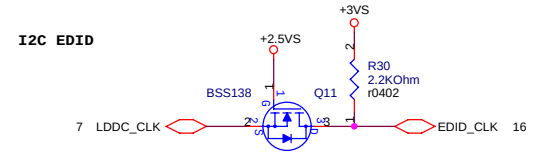












ASUSTeK COMPUTER INC	Title : GMCH Strapping	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 11 of 50	

ICH6-M from 02-010002500 change to 02-010004402
on bom list

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

U20C

U20D

PLACE WITHIN 500mils of ICH6 ball

H_CPUSLP# R193 : B STEP NO STUFF
H_DPRSTP# R231 : A STEP NO STUFF

INTERNAL PULL-DOWN
PULL-UP : NO REBOOT

INTERNAL PULL-UP
PULL-DOWN : RESERVED

TP_3 INTERNAL PULL-UP
PULL-DOWN : PCI
Express Port chain test

DELAY 18~25ms

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2"
from the series resistor

ICH6_M

Q64
2N7002

Q72
2N7002

BAT1
BATT_HOLDER_2P

D56
RB715F

D36
1N4148W-A2

ASUSTeK COMPUTER INC

Title : ICH6_M (1)

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 12 of 50

PLT_RST#
ICH6,Alviso/KBC/FWH/HDD

U20A

ICH6_M

U20B

ICH6_M

PLACE within 500 mils of ICH.

PLACE within 500 mils of ICH.
5.5mil/8mil

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK , AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , SDD[7] , PDDREQ , SDDREQ , SPKR , USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
EE_DIN , EE_DOUT , GNT[B:A]# , GNT[5]# , GPIO[17:16] , LAD[3:0]# , LDRQ[1:0] , LAN_RXD[2:0] , PME# , PWRBTN#

(USB 4 for CAMERA)
(USB 5 for WLAN)

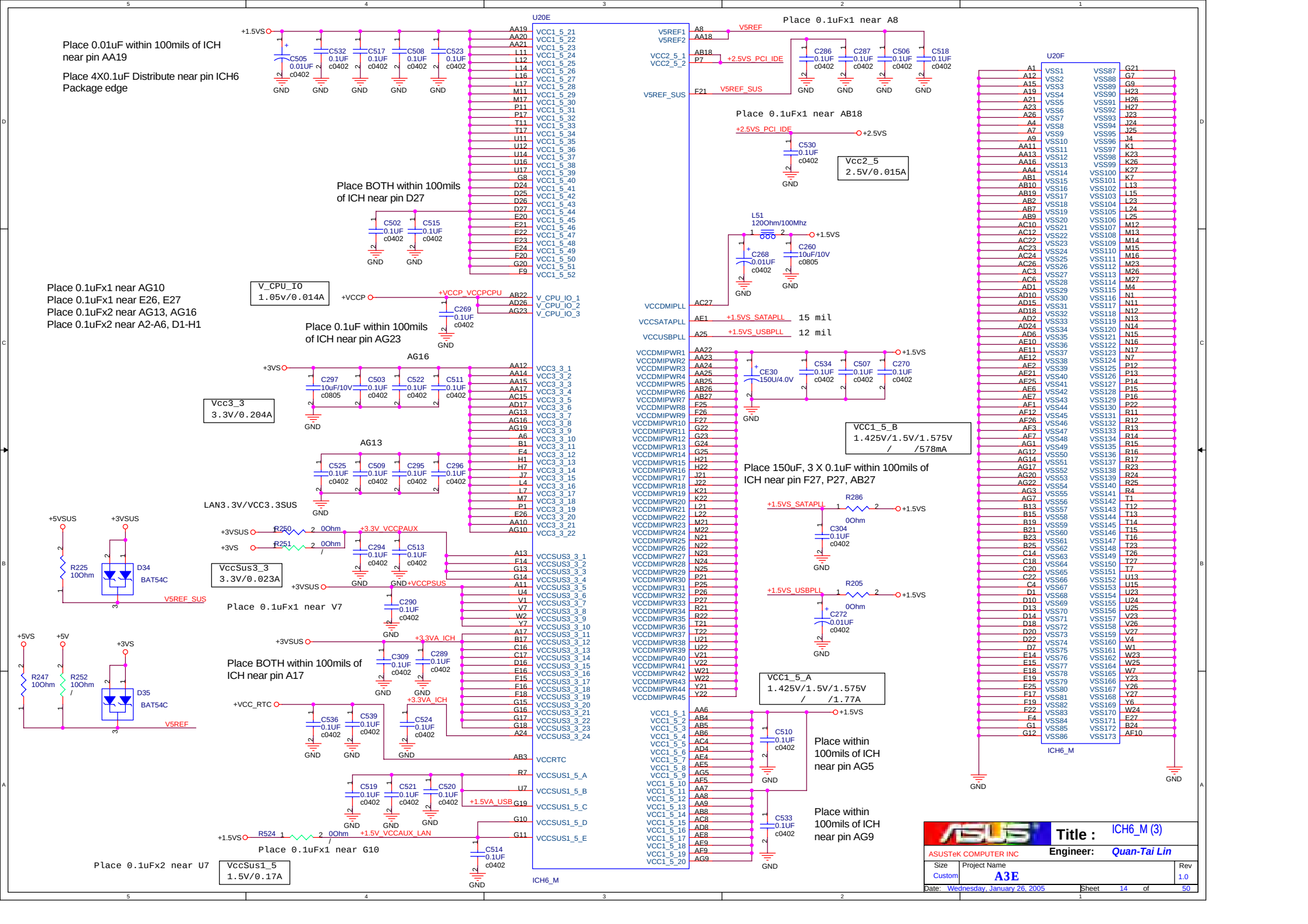
PCB_VID 0 1 2
MB V1.0 0 0 0

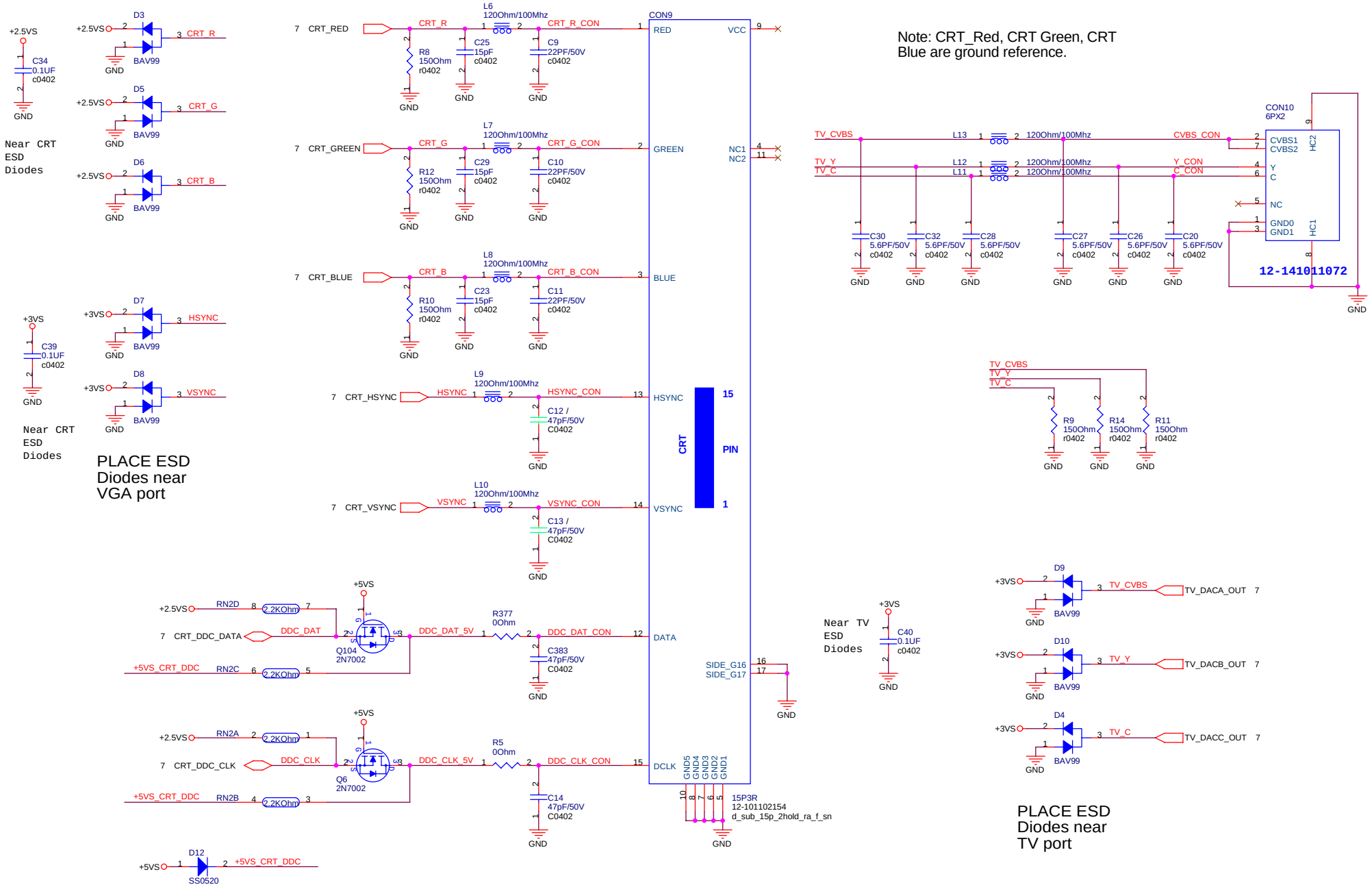
PCB_VID3 : PROJECT CODE

INTERNAL PULL-UP
PULL-DOWN : Boot BIOS destination select

INTERNAL PULL-UP
PULL-DOWN :TOP-BLOCK SWAP

Title :	ICH6_M (2)
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E
Rev: 1.0	
Date: Wednesday, January 26, 2005	Sheet 13 of 50


Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1
V_CPU_IO 1.05v/0.014A
Place 0.1uF within 100mils of ICH near pin AG23
AG16
Vcc3_3 3.3V/0.204A
AG13
LAN3.3V/VCC3.3SUS
VccSus3_3 3.3V/0.023A
Place 0.1uFx1 near V7
Place BOTH within 100mils of ICH near pin A17
Place 0.1uFx1 near G10
Place 0.1uFx2 near U7
VccSus1_5 1.5V/0.17A
Place 0.1uFx1 near A8
Place 0.1uFx1 near AB18
Vcc2_5 2.5V/0.015A
15 mil
12 mil
VCC1_5_B 1.425V/1.5V/1.575V / /578mA
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
VCC1_5_A 1.425V/1.5V/1.575V / /1.77A
Place within 100mils of ICH near pin AG5
Place within 100mils of ICH near pin AG9
U20E
U20F
ICH6_M
Title : ICH6_M (3)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 14 of 50



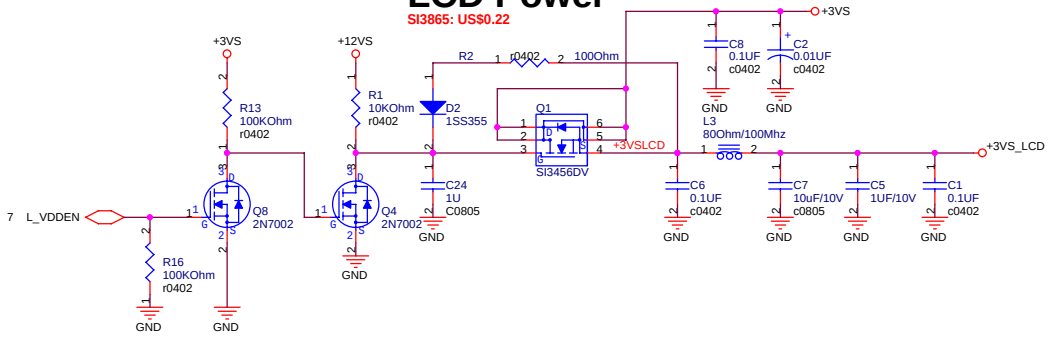
Title :	CRT & TV OUT		
ASUSTeK COMPUTER INC		Engineer:	Quan-Tai Lin
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005		Sheet 15 of 50	

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

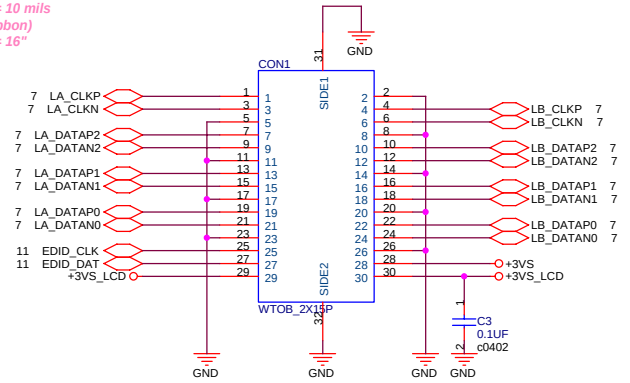
LCD Power

SI3865: US$0.22

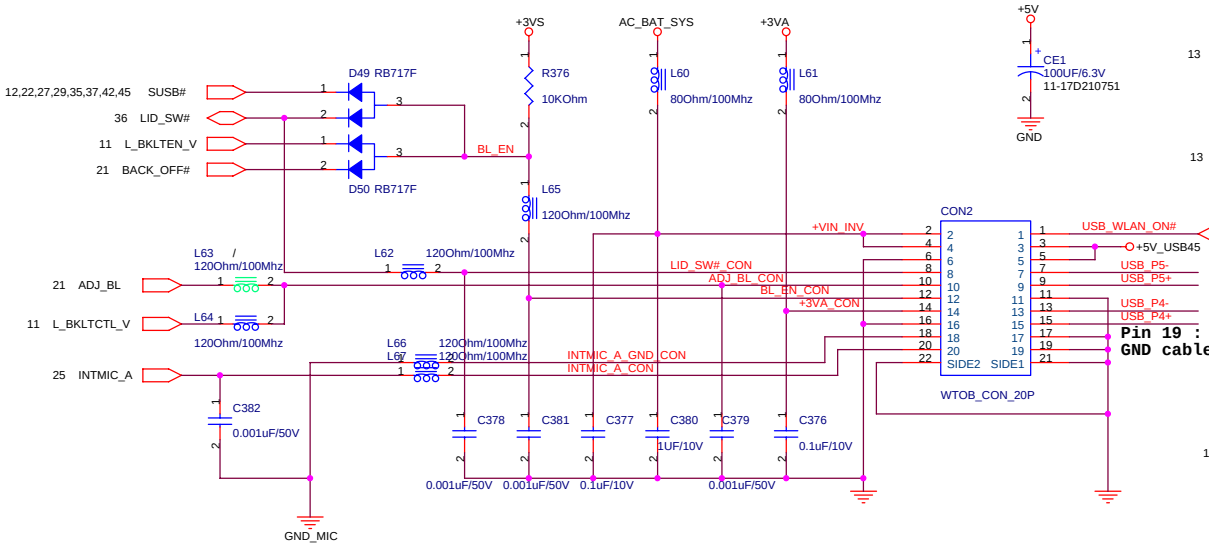


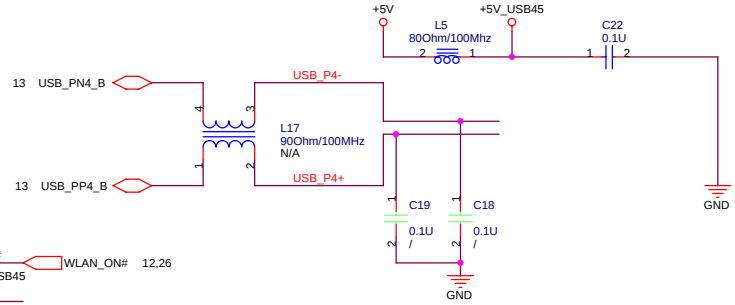
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface



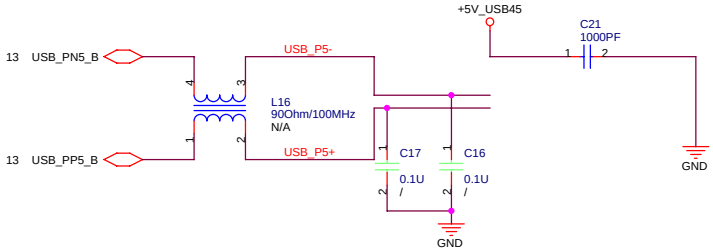
INVERTER Interface





USB PORT 4 for CAMERA

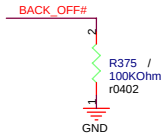
Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



USB PORT 5 for WLAN

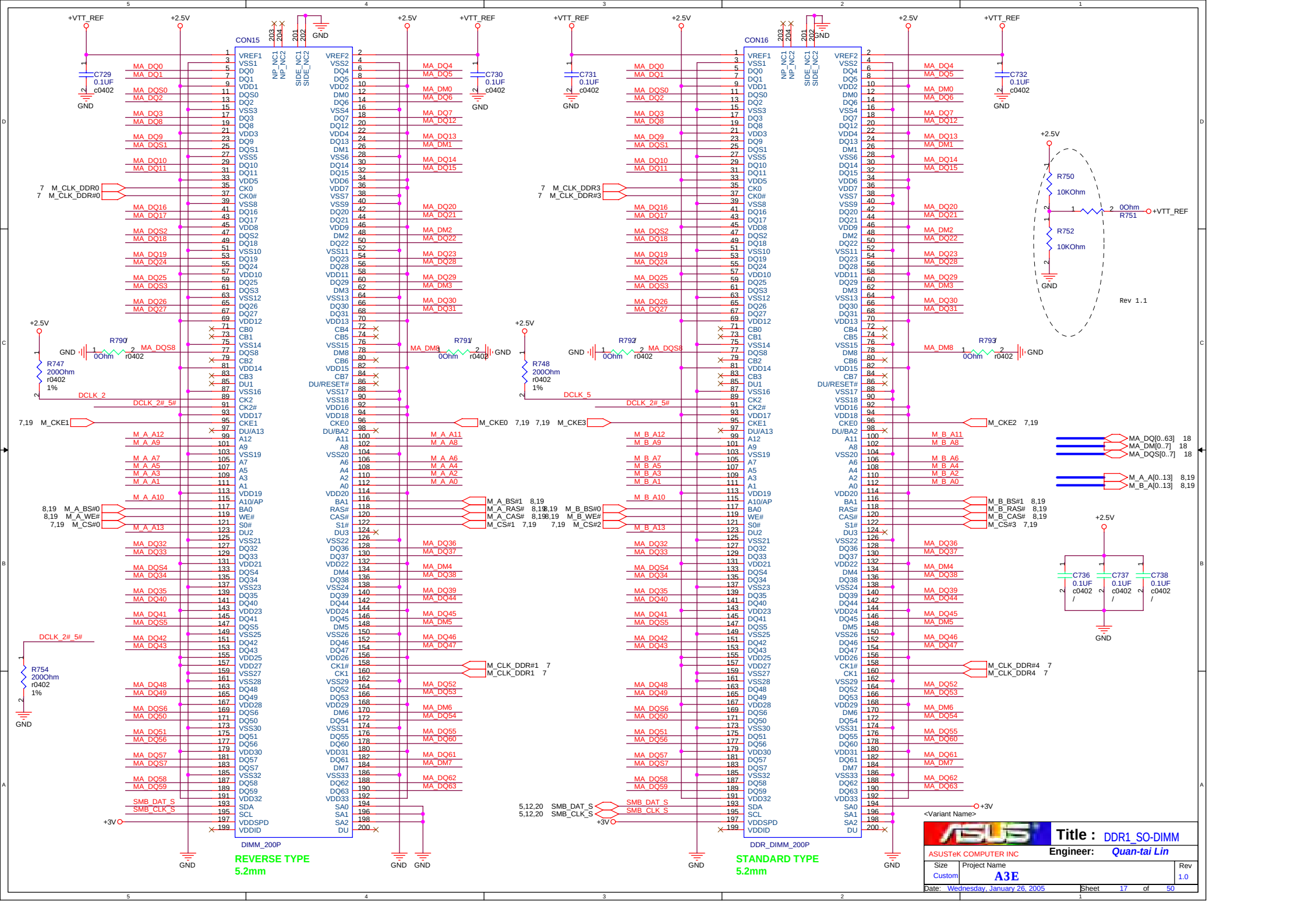
BIOS
ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

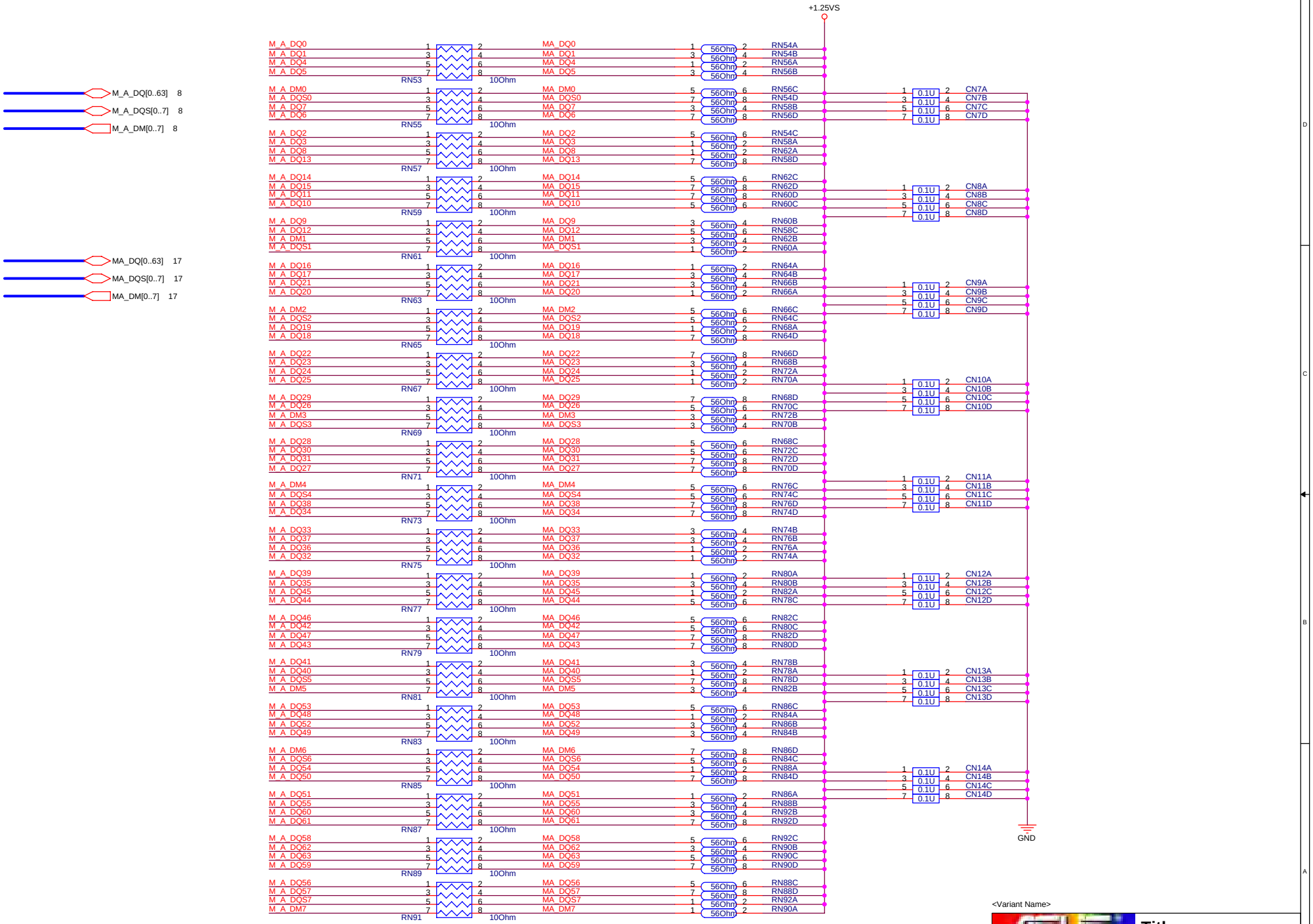
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 16 of 50	


CON15
CON16
DIMM_200P
DDR_DIMM_200P
REVERSE TYPE
5.2mm
STANDARD TYPE
5.2mm
+VTT_REF
+2.5V
+3V
GND
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR3
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
DCLK_2
DCLK_2#_5#
DCLK_5
R747 200Ohm r0402 1%
R748 200Ohm r0402 1%
R754 200Ohm r0402 1%
R750 10KOhm
R751 0Ohm
R752 10KOhm
R790 0Ohm r0402
R791 0Ohm r0402
R792 0Ohm r0402
R793 0Ohm r0402
C729 0.1UF c0402
C730 0.1UF c0402
C731 0.1UF c0402
C732 0.1UF c0402
C736 0.1UF c0402
C737 0.1UF c0402
C738 0.1UF c0402
SMB_DAT_S
SMB_CLK_S
MA_DQ[0..63] 18
MA_DM[0..7] 18
MA_DQS[0..7] 18
M_A_A[0..13] 8,19
M_B_A[0..13] 8,19
Rev 1.1
<Variant Name>
Title : DDR1_SO-DIMM
ASUSTeK COMPUTER INC
Engineer: Quan-tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 17 of 50



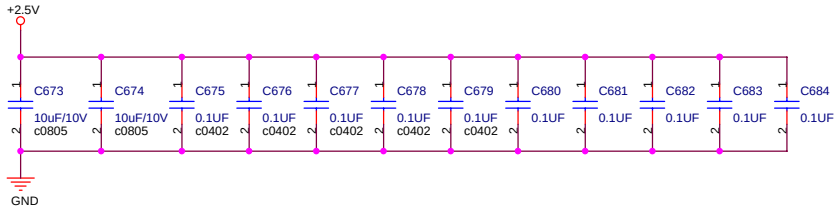
<Variant Name>

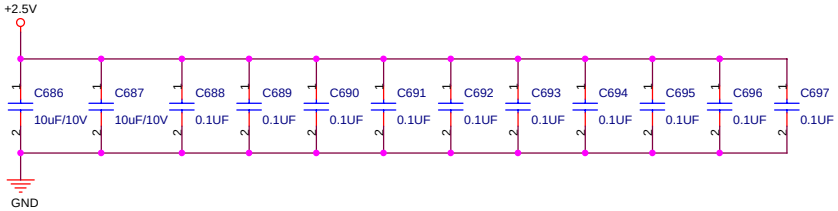
Title DDR DATA TERMINATION

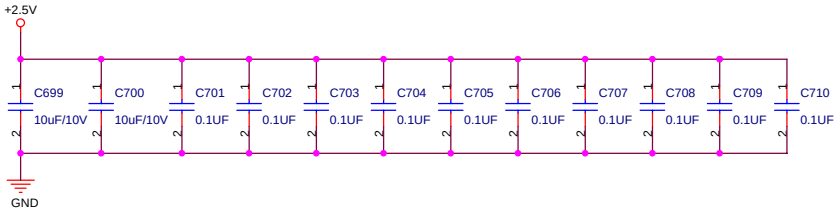
ASUSTeK COMPUTER INC Engineer: Quan-tai Lin

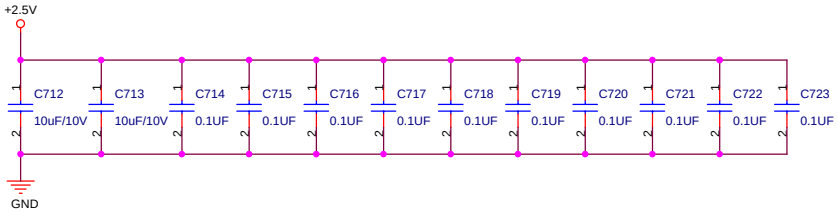
Size	Project Name	Rev
Custom	A3E	1.0

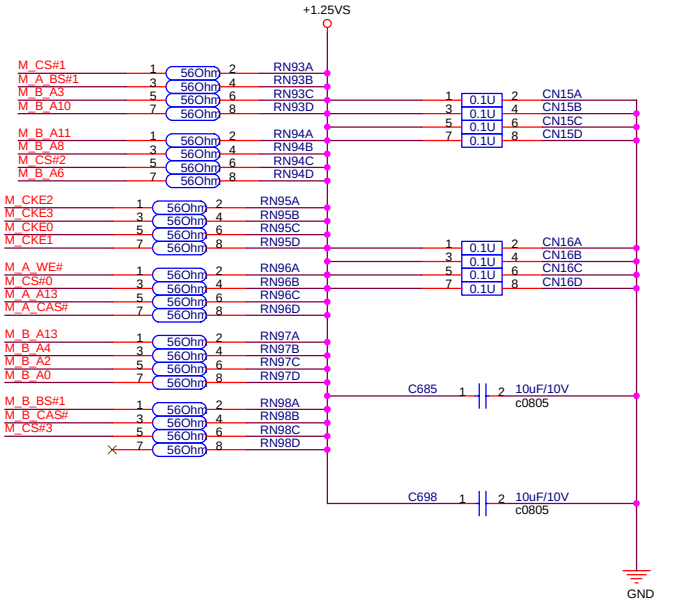
Date: Wednesday, January 26, 2005 Sheet 18 of 50

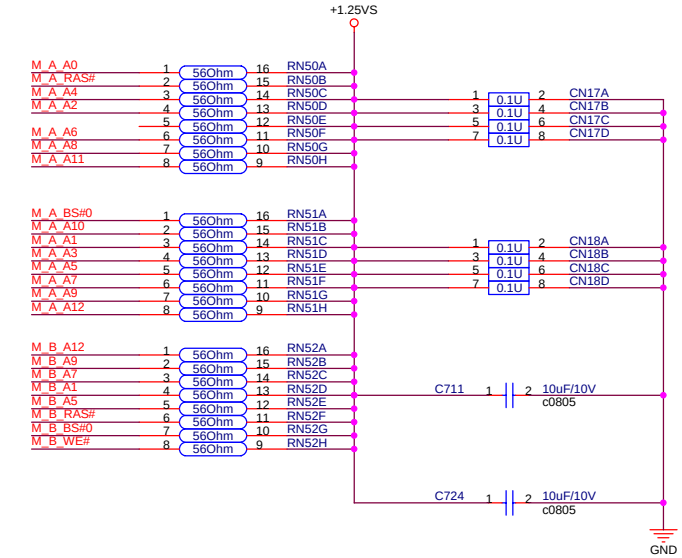












M_A_A[0..13] 8,17
M_B_A[0..13] 8,17
M_CKE[0..3] 7,17
M_CS#[0..3] 7,17

M_B_RAS# M_B_CAS# M_B_WE# — M_B_RAS# 8,17 / M_B_CAS# 8,17 / M_B_WE# 8,17

M_A_RAS# M_A_CAS# M_A_WE# — M_A_RAS# 8,17 / M_A_CAS# 8,17 / M_A_WE# 8,17

M_A_BS#0 M_A_BS#1 — M_A_BS#0 8,17 / M_A_BS#1 8,17

M_B_BS#0 M_B_BS#1 — M_B_BS#0 8,17 / M_B_BS#1 8,17

<Variant Name>

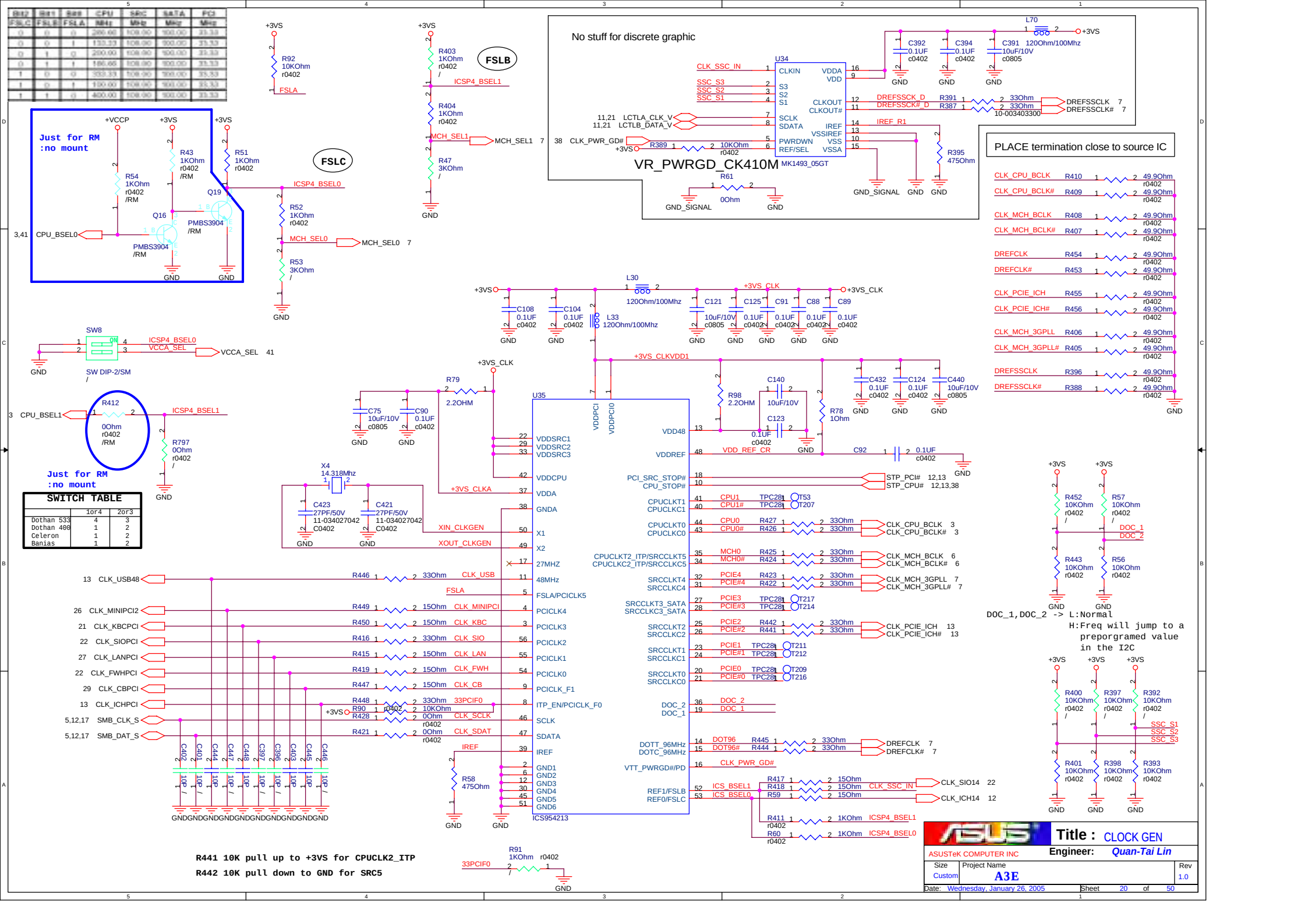
ASUSTeK COMPUTER INC

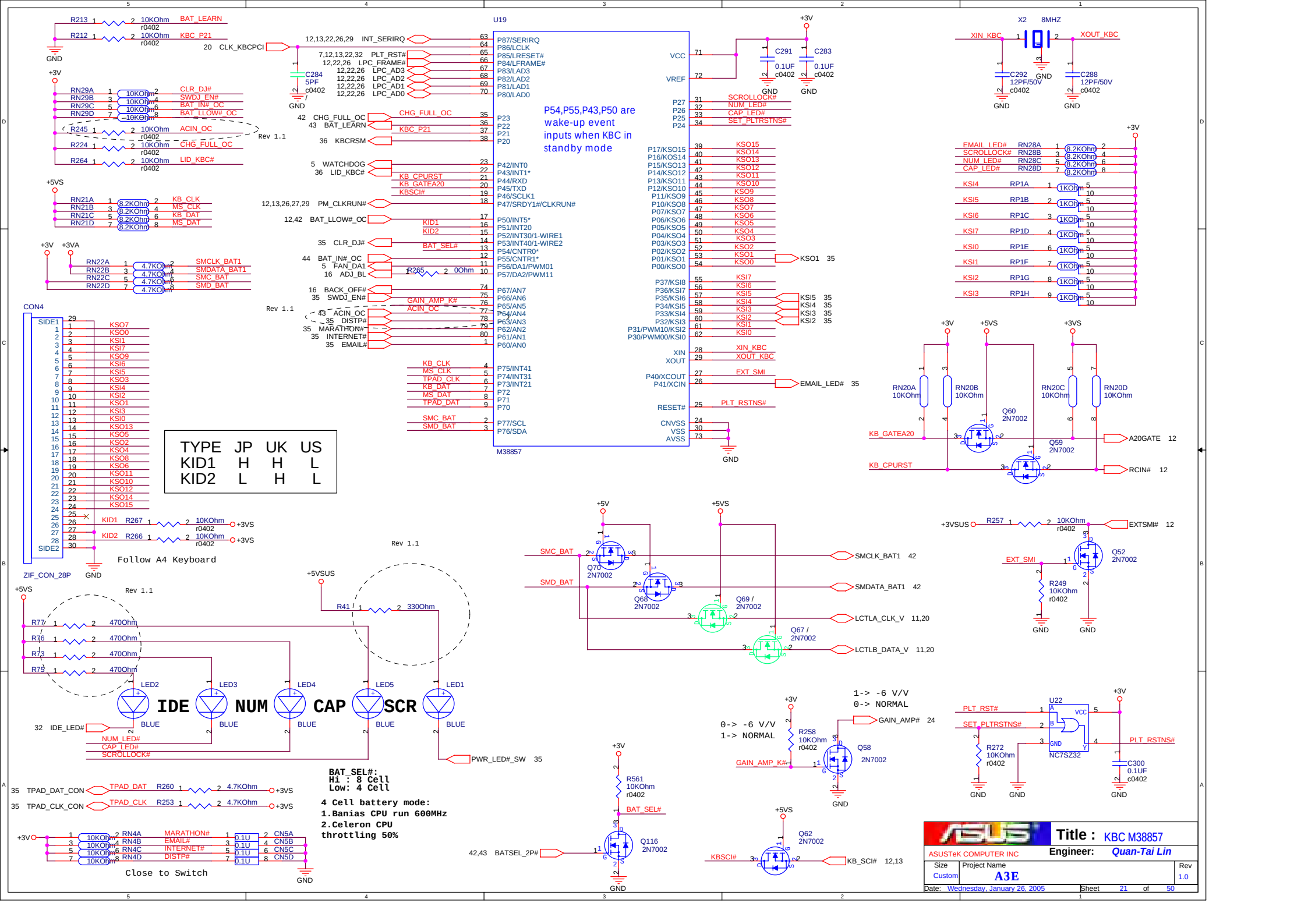
Title : DDR ADDR TERM

Engineer: Quan-tai Lin

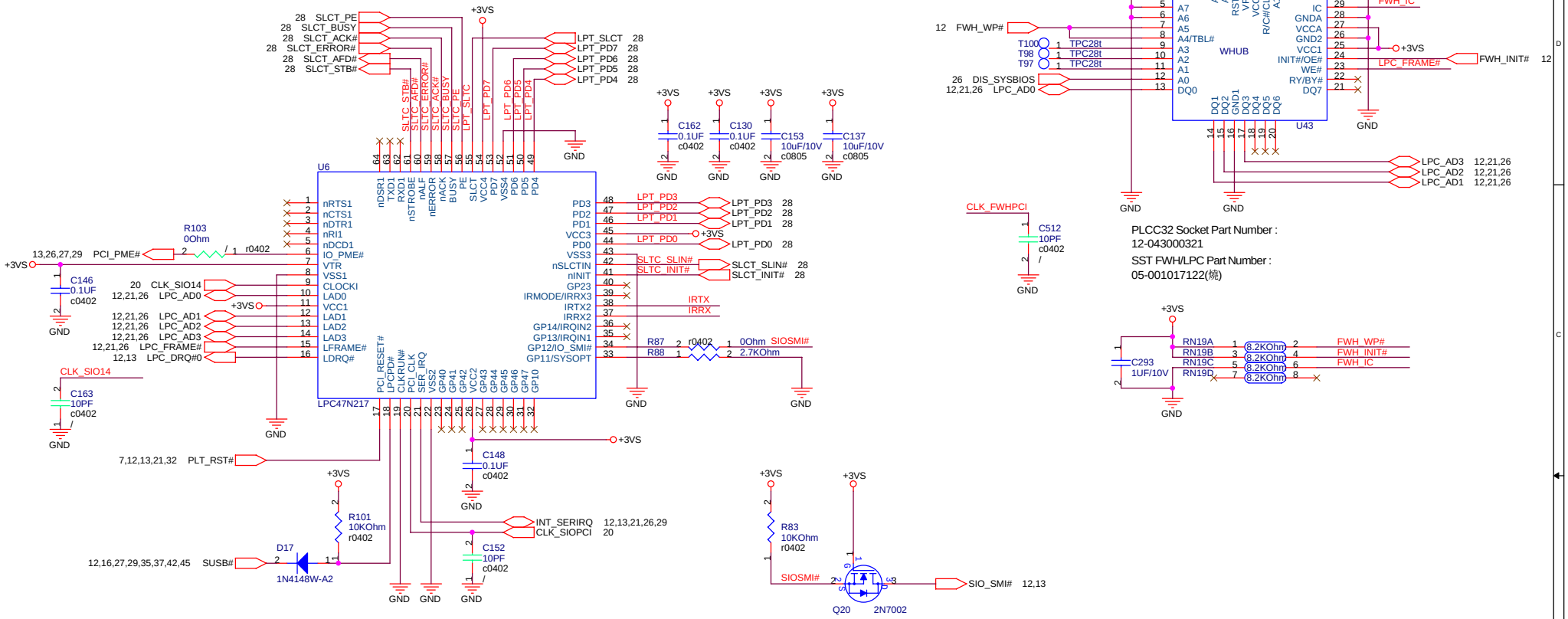
Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 19 of 50


No stuff for discrete graphic
VR_PWRGD_CK410M
MK1493_05GT
PLACE termination close to source IC
Just for RM
:no mount
SWITCH TABLE
1or4 2or3
Dothan 533 4 3
Dothan 400 1 2
Celeron 1 2
Banias 1 2
R441 10K pull up to +3VS for CPUCLK2_ITP
R442 10K pull down to GND for SRC5
DOC_1,DOC_2 -> L:Normal
H:Freq will jump to a
preporgramed value
in the I2C
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 20 of 50


U19
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
CON4
ZIF_CON_28P
Follow A4 Keyboard
TYPE JP UK US
KID1 H H L
KID2 L H L
IDE NUM CAP SCR
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
Close to Switch
Rev 1.1
X2 8MHZ
Title : KBC M38857
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 21 of 50

Super I/O

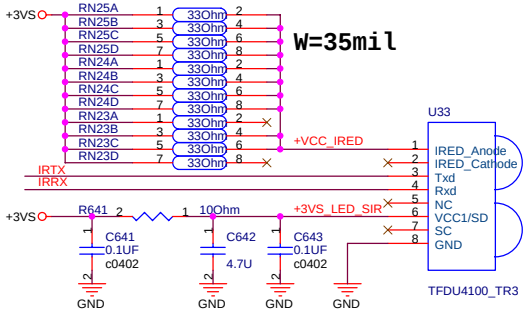


PLCC32 Socket Part Number :
12-043000321

SST FWH/LPC Part Number :
05-001017122(燒)

Keep From Leakage Current

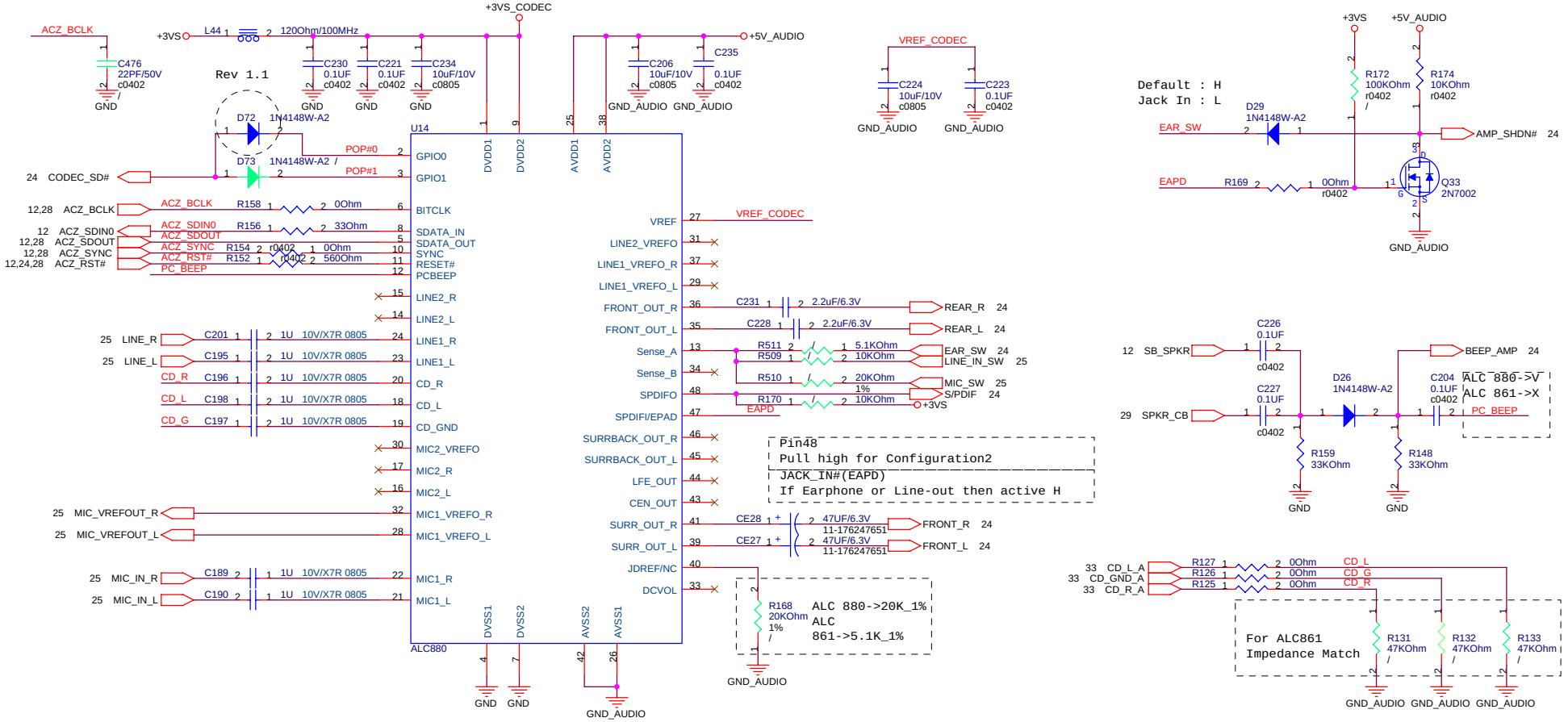
W=35mil



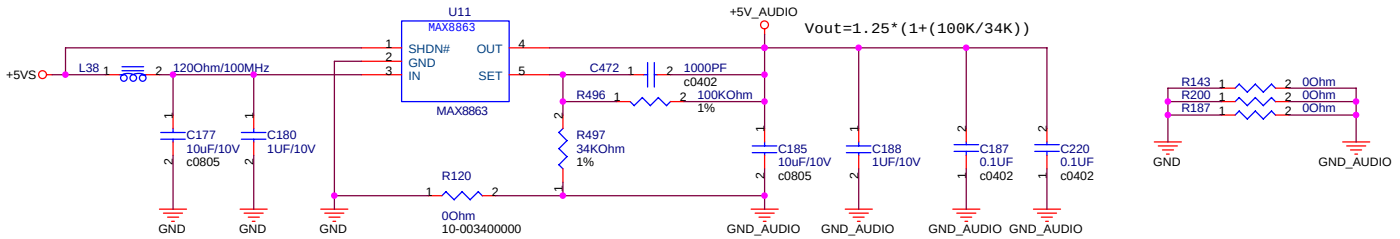
W=35mil

W=20mil

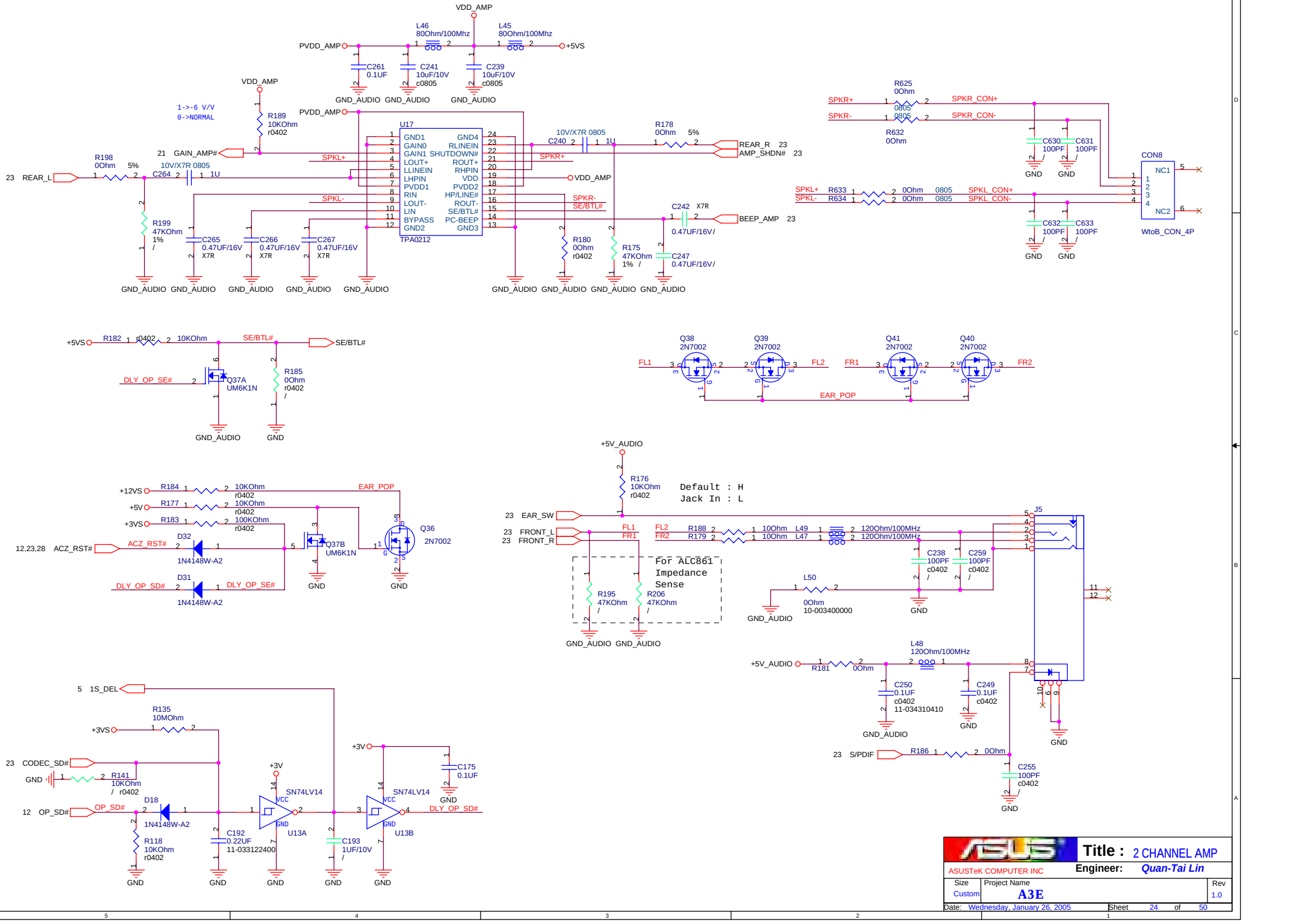
ASUSTeK COMPUTER INC	Title : FWH / SIO / SIR		
	Engineer: *Quan-Tai Lin*		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 22 of 50		



ALC880/ALC861



Title : AZALIA		
ASUSTek COMPUTER INC. NB1	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 23 of 50	



ASUSTeK COMPUTER INC

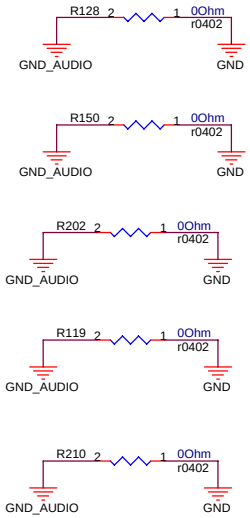
Title : 2 CHANNEL AMP

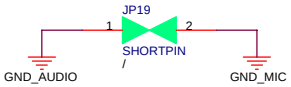
Engineer: Quan-Tai Lin

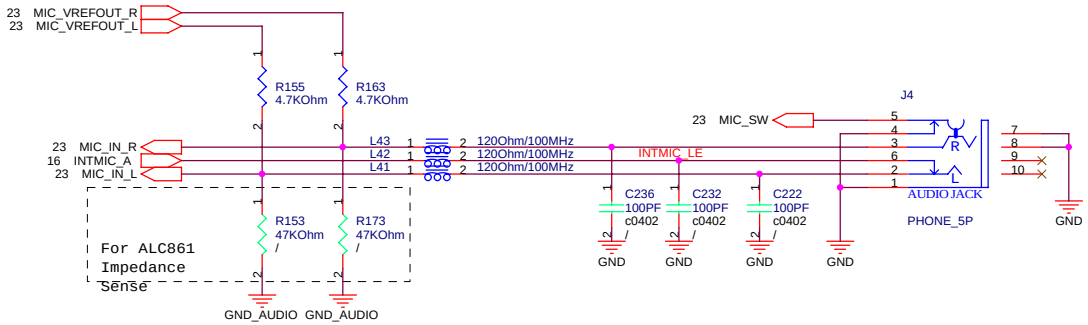
Size	Project Name	Rev
Custom	A3E	1.0

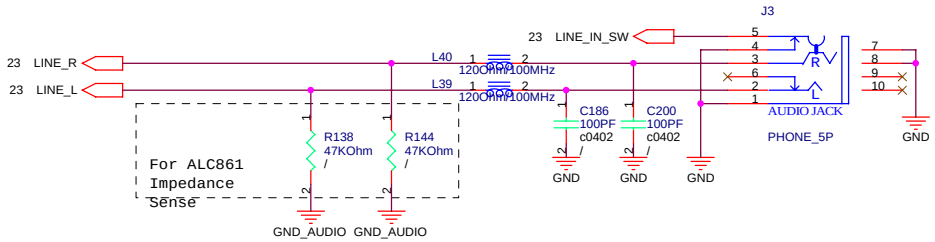
Date: Wednesday, January 26, 2005 Sheet 24 of 50

INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

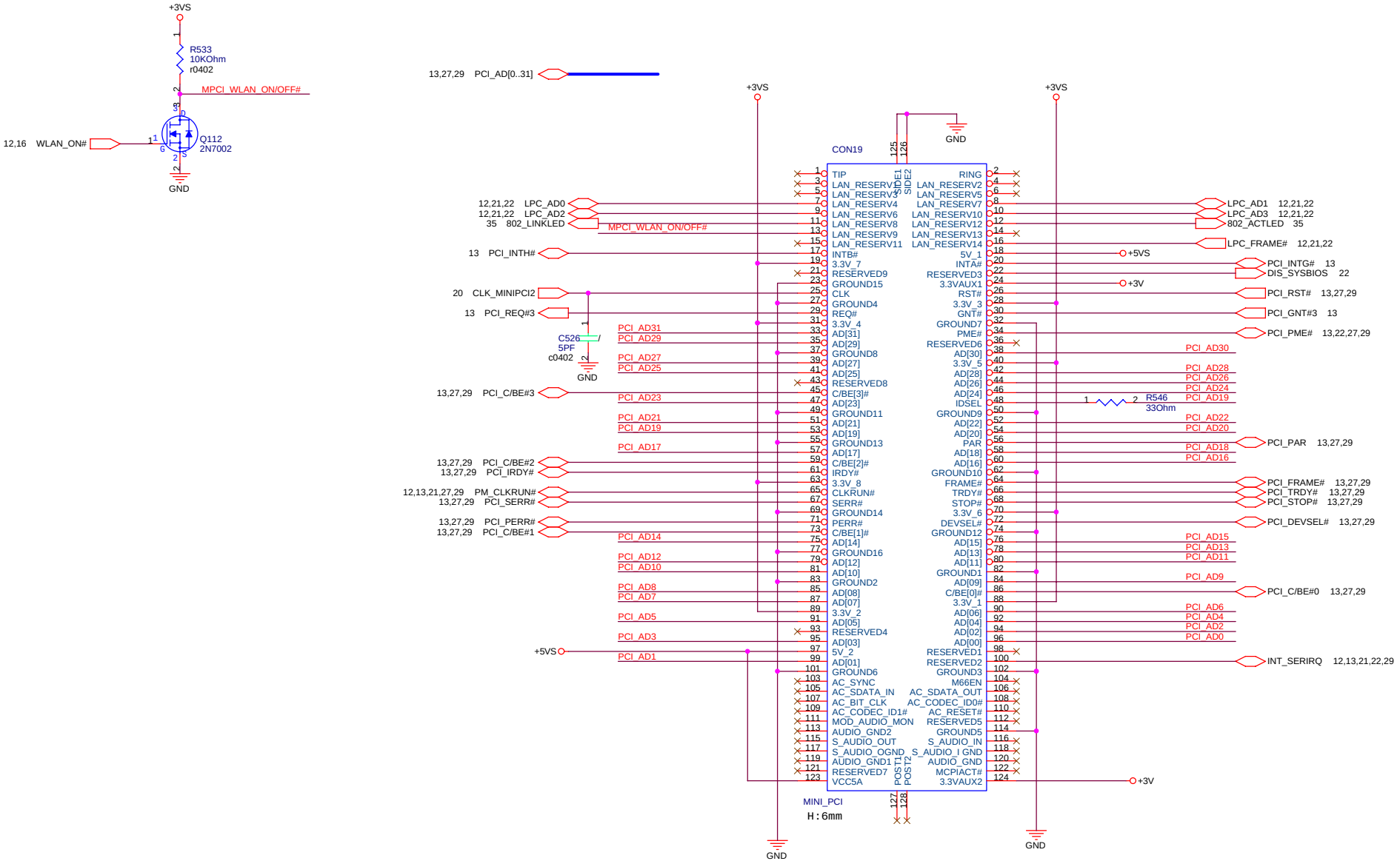








ASUSTeK COMPUTER INC	Title : MIC / Line-IN Jack	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 25 of 50	


+3VS
R533
10KOhm
r0402
MPCI_WLAN_ON/OFF#
12,16 WLAN_ON#
Q112
2N7002
GND
13,27,29 PCI_AD[0..31]
CON19
MINI_PCI
H:6mm
TIP
LAN_RESERV1
LAN_RESERV2
LAN_RESERV3
LAN_RESERV4
LAN_RESERV6
LAN_RESERV8
LAN_RESERV9
LAN_RESERV11
INTB#
3.3V_7
RESERVED9
GROUND15
CLK
GROUND4
REQ#
3.3V_4
AD[31]
AD[29]
GROUND8
AD[27]
AD[25]
RESERVED8
C/BE[3]#
AD[23]
GROUND11
AD[21]
AD[19]
GROUND13
AD[17]
C/BE[2]#
IRDY#
3.3V_8
CLKRUN#
SERR#
GROUND14
PERR#
C/BE[1]#
AD[14]
GROUND16
AD[12]
AD[10]
GROUND2
AD[08]
AD[07]
3.3V_2
AD[05]
RESERVED4
AD[03]
5V_2
AD[01]
GROUND6
AC_SYNC
AC_SDATA_IN
AC_BIT_CLK
AC_CODEC_ID1#
MOD_AUDIO_MON
AUDIO_GND2
S_AUDIO_OUT
S_AUDIO_OGND
AUDIO_GND1
RESERVED7
VCC5A
RING
LAN_RESERV2
LAN_RESERV5
LAN_RESERV7
LAN_RESERV10
LAN_RESERV12
LAN_RESERV13
LAN_RESERV14
5V_1
INTA#
RESERVED3
3.3VAUX1
RST#
3.3V_3
GNT#
GROUND7
PME#
RESERVED6
AD[30]
3.3V_5
AD[28]
AD[26]
AD[24]
IDSEL
GROUND9
AD[22]
AD[20]
PAR
AD[18]
AD[16]
GROUND10
FRAME#
TRDY#
STOP#
3.3V_6
DEVSEL#
GROUND12
AD[15]
AD[13]
AD[11]
GROUND1
AD[09]
C/BE[0]#
3.3V_1
AD[06]
AD[04]
AD[02]
AD[00]
RESERVED1
RESERVED2
GROUND3
M66EN
AC_SDATA_OUT
AC_CODEC_ID0#
AC_RESET#
RESERVED5
GROUND5
S_AUDIO_IN
S_AUDIO_I GND
AUDIO_GND
MCPIACT#
3.3VAUX2
12,21,22 LPC_AD0
12,21,22 LPC_AD2
35 802_LINKLED
MPCI_WLAN_ON/OFF#
13 PCI_INTH#
20 CLK_MINIPCI2
13 PCI_REQ#3
C526
5PF
c0402
13,27,29 PCI_C/BE#3
13,27,29 PCI_C/BE#2
13,27,29 PCI_IRDY#
12,13,21,27,29 PM_CLKRUN#
13,27,29 PCI_SERR#
13,27,29 PCI_PERR#
13,27,29 PCI_C/BE#1
+5VS
PCI_AD31
PCI_AD29
PCI_AD27
PCI_AD25
PCI_AD23
PCI_AD21
PCI_AD19
PCI_AD17
PCI_AD14
PCI_AD12
PCI_AD10
PCI_AD8
PCI_AD7
PCI_AD5
PCI_AD3
PCI_AD1
LPC_AD1 12,21,22
LPC_AD3 12,21,22
802_ACTLED 35
LPC_FRAME# 12,21,22
+5VS
PCI_INTG# 13
DIS_SYSBIOS 22
+3V
PCI_RST# 13,27,29
PCI_GNT#3 13
PCI_PME# 13,22,27,29
PCI_AD30
PCI_AD28
PCI_AD26
PCI_AD24
R546
33Ohm
PCI_AD19
PCI_AD22
PCI_AD20
PCI_PAR 13,27,29
PCI_AD18
PCI_AD16
PCI_FRAME# 13,27,29
PCI_TRDY# 13,27,29
PCI_STOP# 13,27,29
PCI_DEVSEL# 13,27,29
PCI_AD15
PCI_AD13
PCI_AD11
PCI_AD9
PCI_C/BE#0 13,27,29
PCI_AD6
PCI_AD4
PCI_AD2
PCI_AD0
INT_SERIRQ 12,13,21,22,29
+3V
C531
10uF/10V
c0805
C538
0.1UF
c0402
C529
0.1UF
c0402
C541
0.01UF
c0402
C540
0.01UF
c0402
C542
0.01UF
c0402
C528
0.01UF
c0402
C527
0.01UF
c0402
CE31
150U/4.0V
Title : MINIPCI (802.11)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size
Custom
Project Name
A3E
Rev
1.0
Date: Wednesday, January 26, 2005
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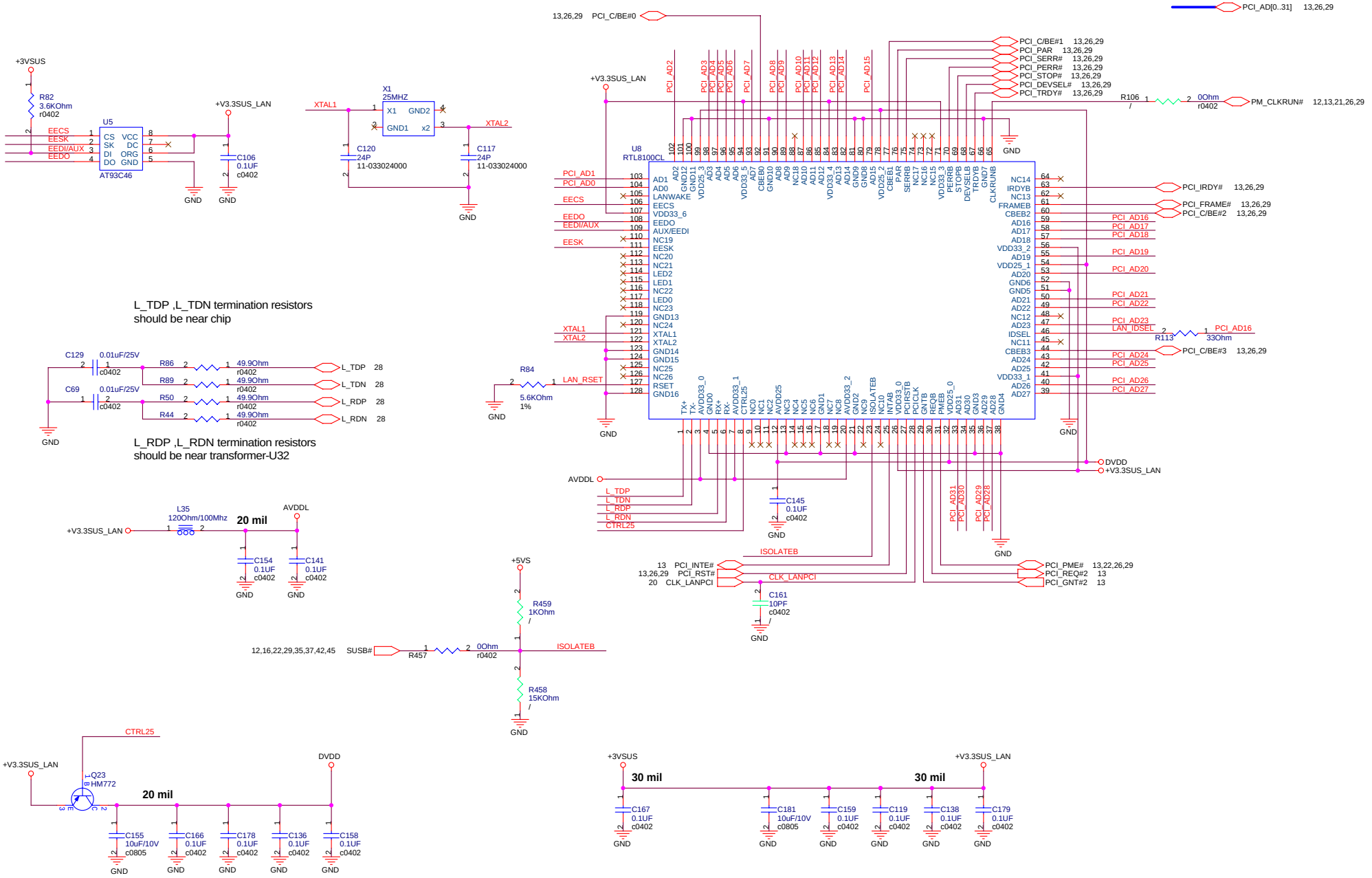
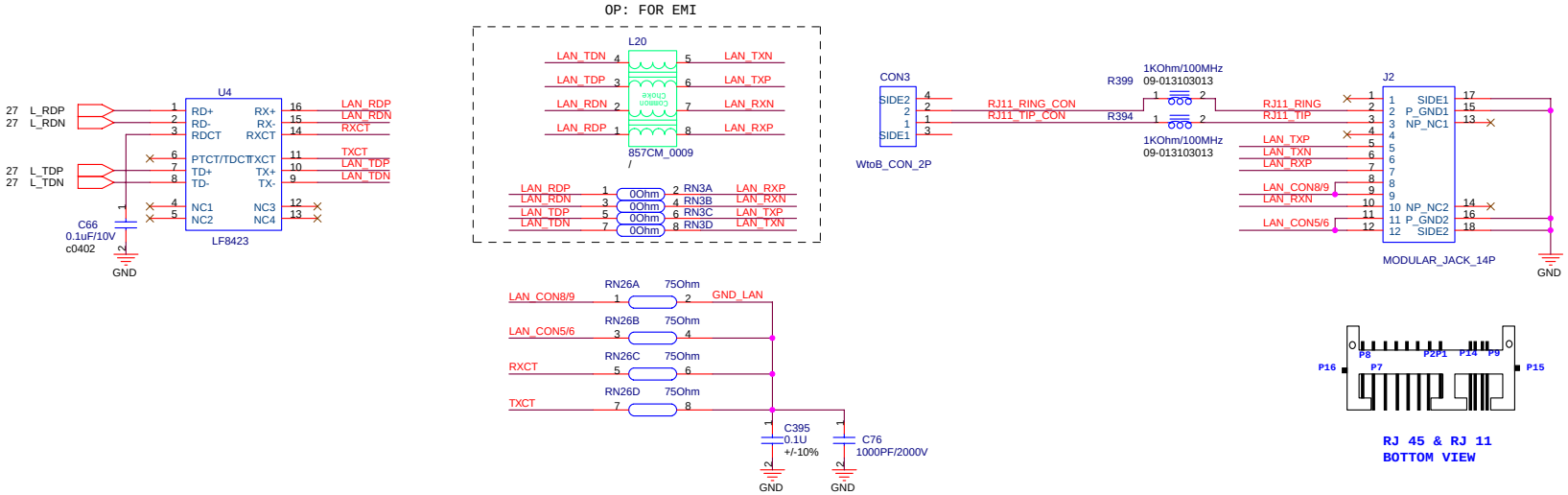


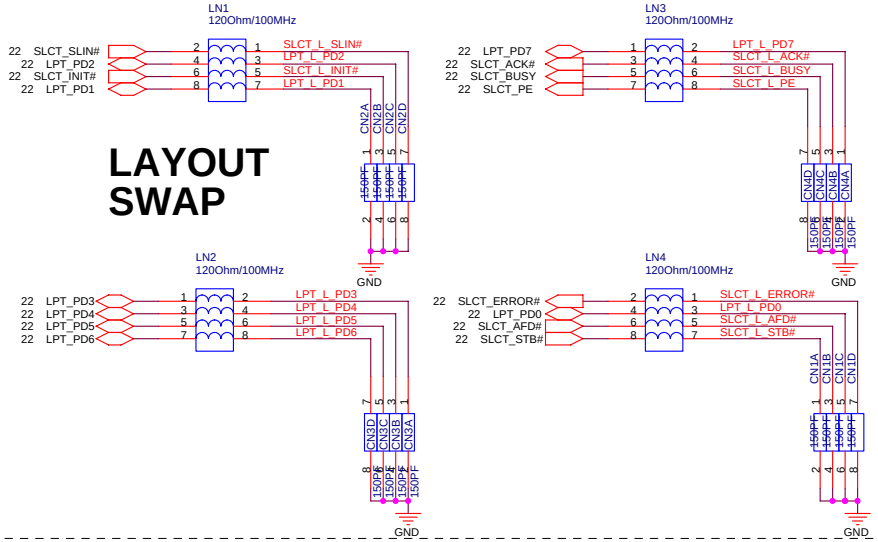
ASUSTeK COMPUTER INC	Title : 10/100 LAN RTL8100CL		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 27 of 50		

LAN PORT

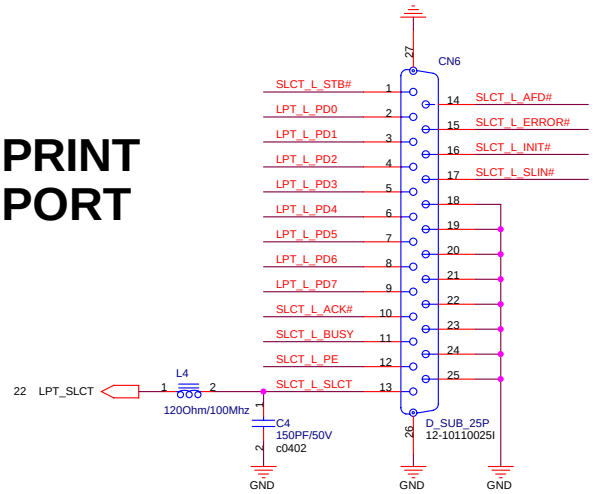


RJ 45 & RJ 11
BOTTOM VIEW

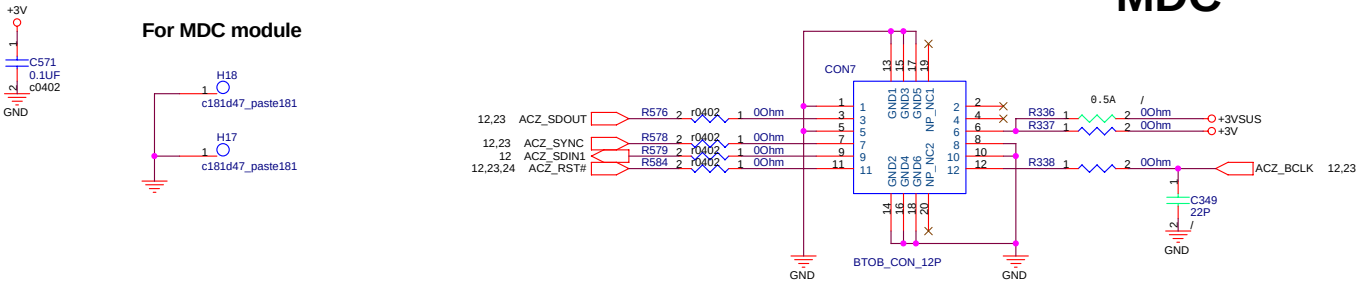
LAYOUT SWAP



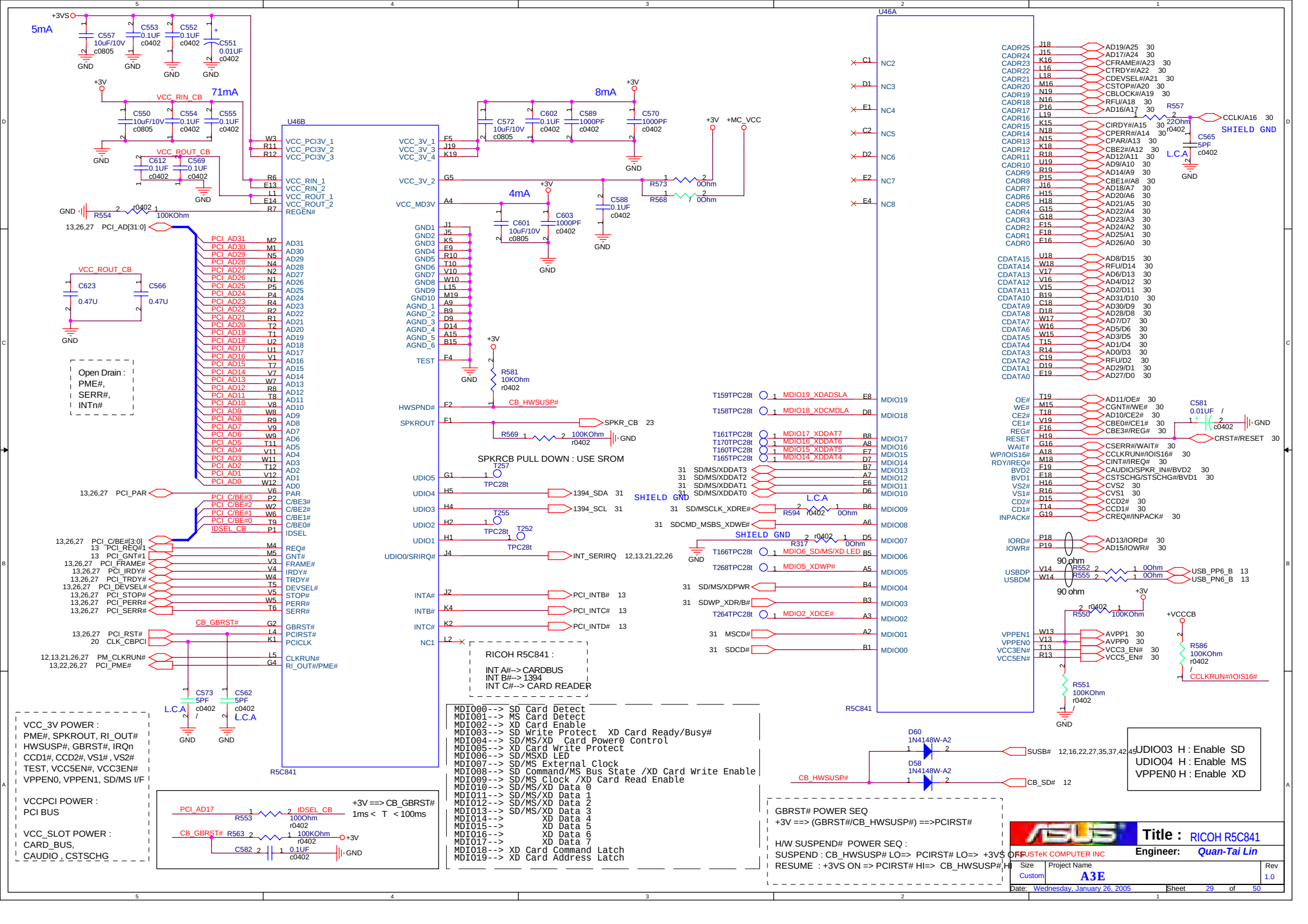
PRINT PORT



MDC



ASUSTeK COMPUTER INC	Title : RJ11+45,MDC,PRN	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 28 of 50	


5mA
71mA
8mA
4mA
U46B
U46A
R5C841
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
SHIELD GND
L.C.A
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP#_HI
Title : RICOH R5C841
Engineer: Quan-Tai Lin
ASUSTeK COMPUTER INC
Size: Custom
Project Name: A3E
Rev: 1.0
Date: Wednesday, January 26, 2005
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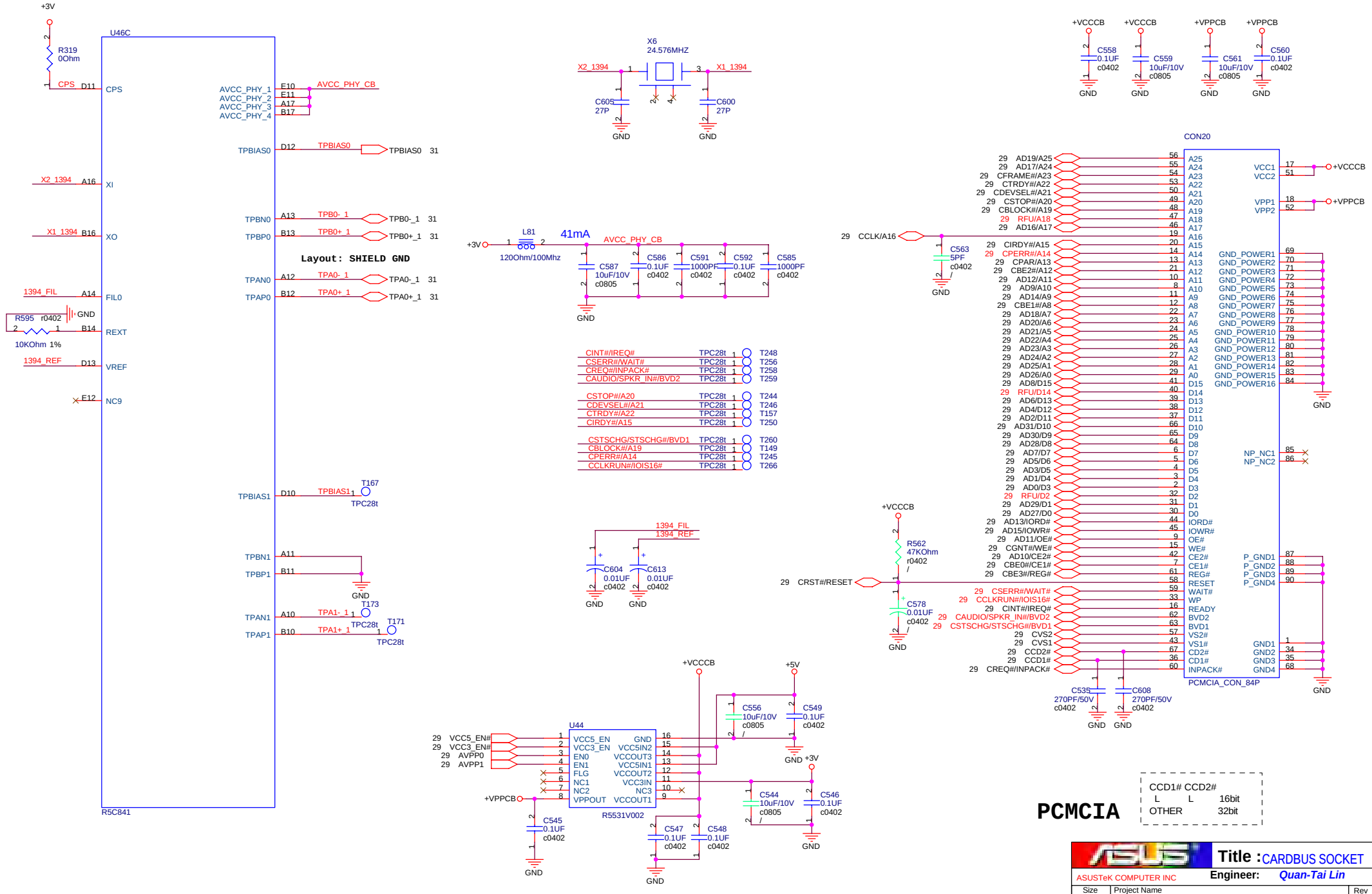
+3V
R319
0Ohm
CPS D11
U46C
CPS
XI
XO
FIL0
REXT
VREF
NC9
R5C841
X2_1394 A16
X1_1394 B16
1394_FIL A14
R595 r0402
10KOhm 1%
B14
1394_REF D13
E12
AVCC_PHY_1 E10
AVCC_PHY_2 E11
AVCC_PHY_3 A17
AVCC_PHY_4 B17
AVCC_PHY_CB
TPBIAS0 D12
TPBIAS0 31
TPBN0 A13
TPBP0 B13
TPB0- 1
TPB0+ 1
TPB0-_1 31
TPB0+_1 31
Layout: SHIELD GND
TPAN0 A12
TPAP0 B12
TPA0- 1
TPA0+ 1
TPA0-_1 31
TPA0+_1 31
TPBIAS1 D10
TPBIAS1 1
T167
TPC28t
TPBN1 A11
TPBP1 B11
TPAN1 A10
TPAP1 B10
TPA1- 1
TPA1+ 1
T173
T171
X6
24.576MHZ
X2_1394 1
X1_1394 3
C605 27P
C600 27P
GND
L81
120Ohm/100Mhz
41mA
C586 0.1UF c0402
C591 1000PF c0402
C592 0.1UF c0402
C585 1000PF c0402
C587 10uF/10V c0805
CINT#/IREQ# T248
CSERR#/WAIT# T256
CREQ#/INPACK# T258
CAUDIO/SPKR_IN#/BVD2 T259
CSTOP#/A20 T244
CDEVSEL#/A21 T246
CTRDY#/A22 T157
CIRDY#/A15 T250
CSTSCHG/STSCHG#/BVD1 T260
CBLOCK#/A19 T149
CPERR#/A14 T245
CCLKRUN#/IOIS16# T266
TPC28t
1394_FIL
1394_REF
C604 0.01UF c0402
C613 0.01UF c0402
U44
VCC5_EN
VCC3_EN
EN0
EN1
FLG
NC1
NC2
VPPOUT
GND
VCC5IN2
VCCOUT3
VCC5IN1
VCCOUT2
VCC3IN
NC3
VCCOUT1
R5531V002
29 VCC5_EN#
29 VCC3_EN#
29 AVPP0
29 AVPP1
+VPPCB
+VCCCB
+5V
+3V
C556 10uF/10V c0805
C549 0.1UF c0402
C544 10uF/10V c0805
C546 0.1UF c0402
C545 0.1UF c0402
C547 0.1UF c0402
C548 0.1UF c0402
+VCCCB
+VCCCB
+VPPCB
+VPPCB
C558 0.1UF c0402
C559 10uF/10V c0805
C561 10uF/10V c0805
C560 0.1UF c0402
CON20
29 AD19/A25
29 AD17/A24
29 CFRAME#/A23
29 CTRDY#/A22
29 CDEVSEL#/A21
29 CSTOP#/A20
29 CBLOCK#/A19
29 RFU/A18
29 AD16/A17
29 CCLK/A16
C563 5PF c0402
29 CIRDY#/A15
29 CPERR#/A14
29 CPAR/A13
29 CBE2#/A12
29 AD12/A11
29 AD9/A10
29 AD14/A9
29 CBE1#/A8
29 AD18/A7
29 AD20/A6
29 AD21/A5
29 AD22/A4
29 AD23/A3
29 AD24/A2
29 AD25/A1
29 AD26/A0
29 AD8/D15
29 RFU/D14
29 AD6/D13
29 AD4/D12
29 AD2/D11
29 AD31/D10
29 AD30/D9
29 AD28/D8
29 AD7/D7
29 AD5/D6
29 AD3/D5
29 AD1/D4
29 AD0/D3
29 RFU/D2
29 AD29/D1
29 AD27/D0
29 AD13/IORD#
29 AD15/IOWR#
29 AD11/OE#
29 CGNT#/WE#
29 AD10/CE2#
29 CBE0#/CE1#
29 CBE3#/REG#
29 CRST#/RESET
R562 47KOhm r0402
C578 0.01UF c0402
29 CSERR#/WAIT#
29 CCLKRUN#/IOIS16#
29 CINT#/IREQ#
29 CAUDIO/SPKR_IN#/BVD2
29 CSTSCHG/STSCHG#/BVD1
29 CVS2
29 CVS1
29 CCD2#
29 CCD1#
29 CREQ#/INPACK#
C535 270PF/50V c0402
C608 270PF/50V c0402
A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
IORD# IOWR# OE# WE# CE2# CE1# REG# RESET WAIT# WP READY BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
VCC1 VCC2 VPP1 VPP2
GND_POWER1 GND_POWER2 GND_POWER3 GND_POWER4 GND_POWER5 GND_POWER6 GND_POWER7 GND_POWER8 GND_POWER9 GND_POWER10 GND_POWER11 GND_POWER12 GND_POWER13 GND_POWER14 GND_POWER15 GND_POWER16
NP_NC1 NP_NC2
P_GND1 P_GND2 P_GND3 P_GND4
GND1 GND2 GND3 GND4
PCMCIA_CON_84P
+VCCCB
+VPPCB
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
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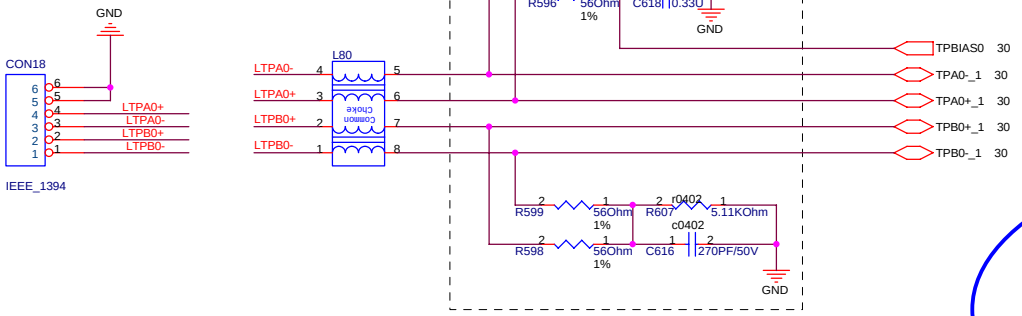
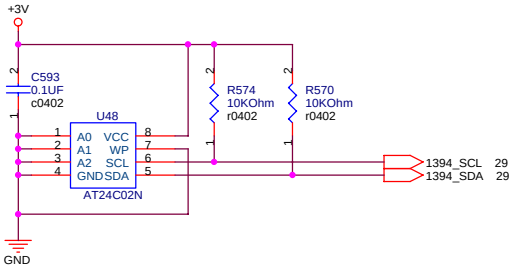
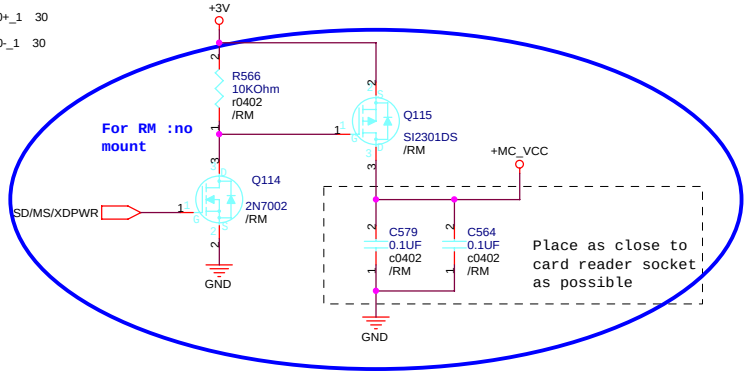
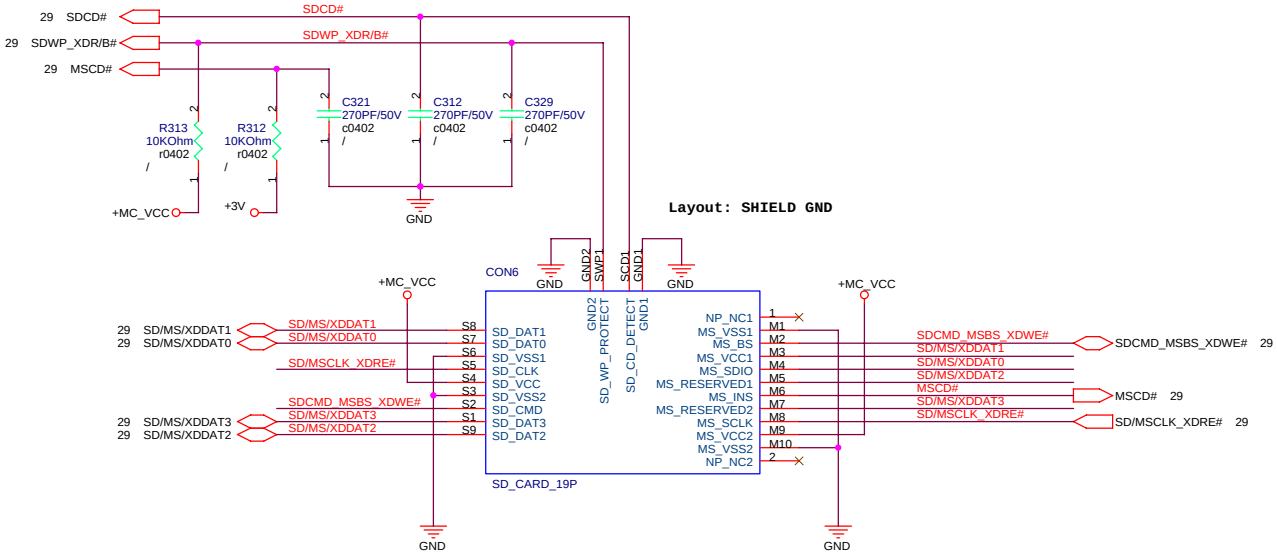


1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm







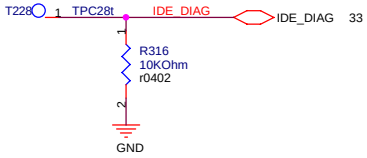
ASUSTeK COMPUTER INC

Title : 1394 & 3 IN 1 CON

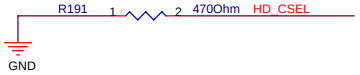
Engineer: Quan-Tai Lin

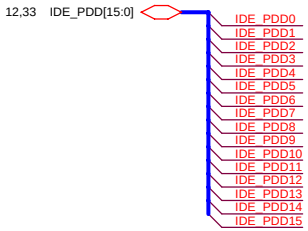
Size	Project Name	Rev
Custom	A3E	1.0

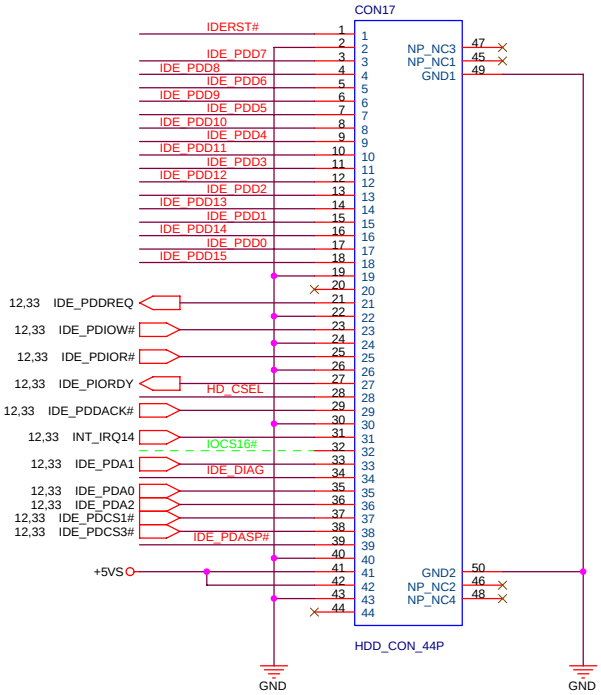
Date: Wednesday, January 26, 2005 Sheet 31 of 50

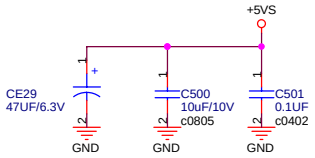


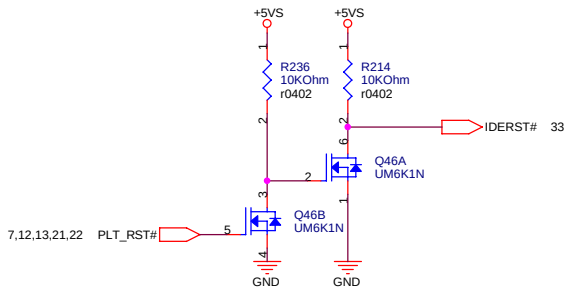
HD_CSEL : Pull-Down, HDD as Master



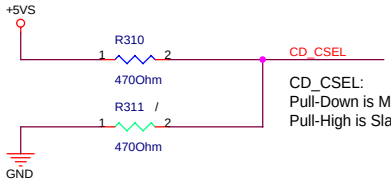




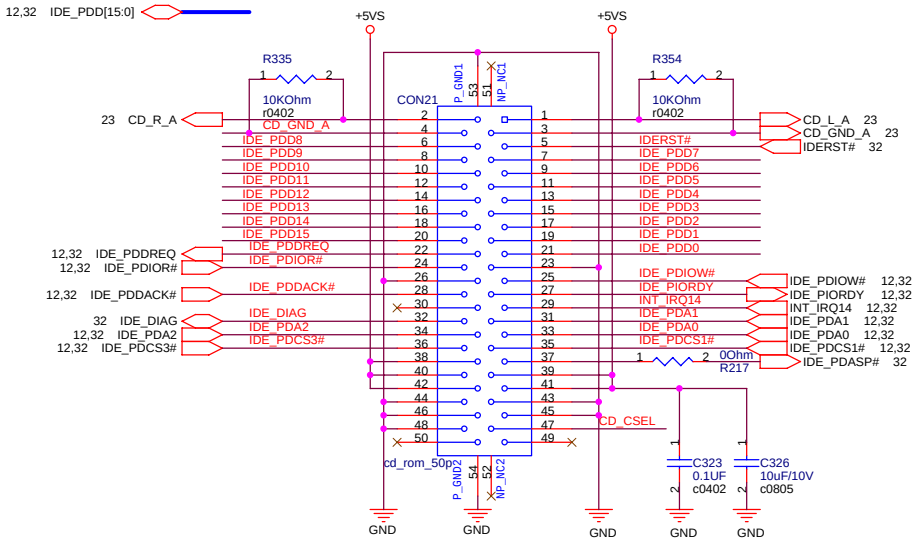


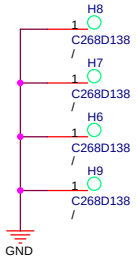


ASUSTeK COMPUTER INC	Title : HDD CONNECTOR	
	Engineer: *Quan-Tai Lin*	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 32 of 50	

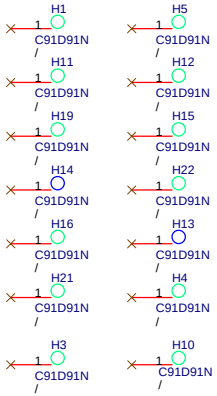


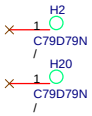
CD_CSEL:
Pull-Down is Master
Pull-High is Slave

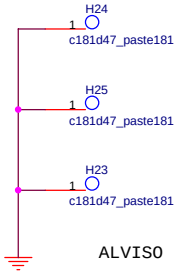




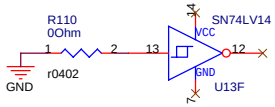
CPU

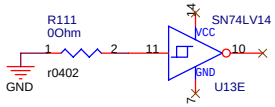






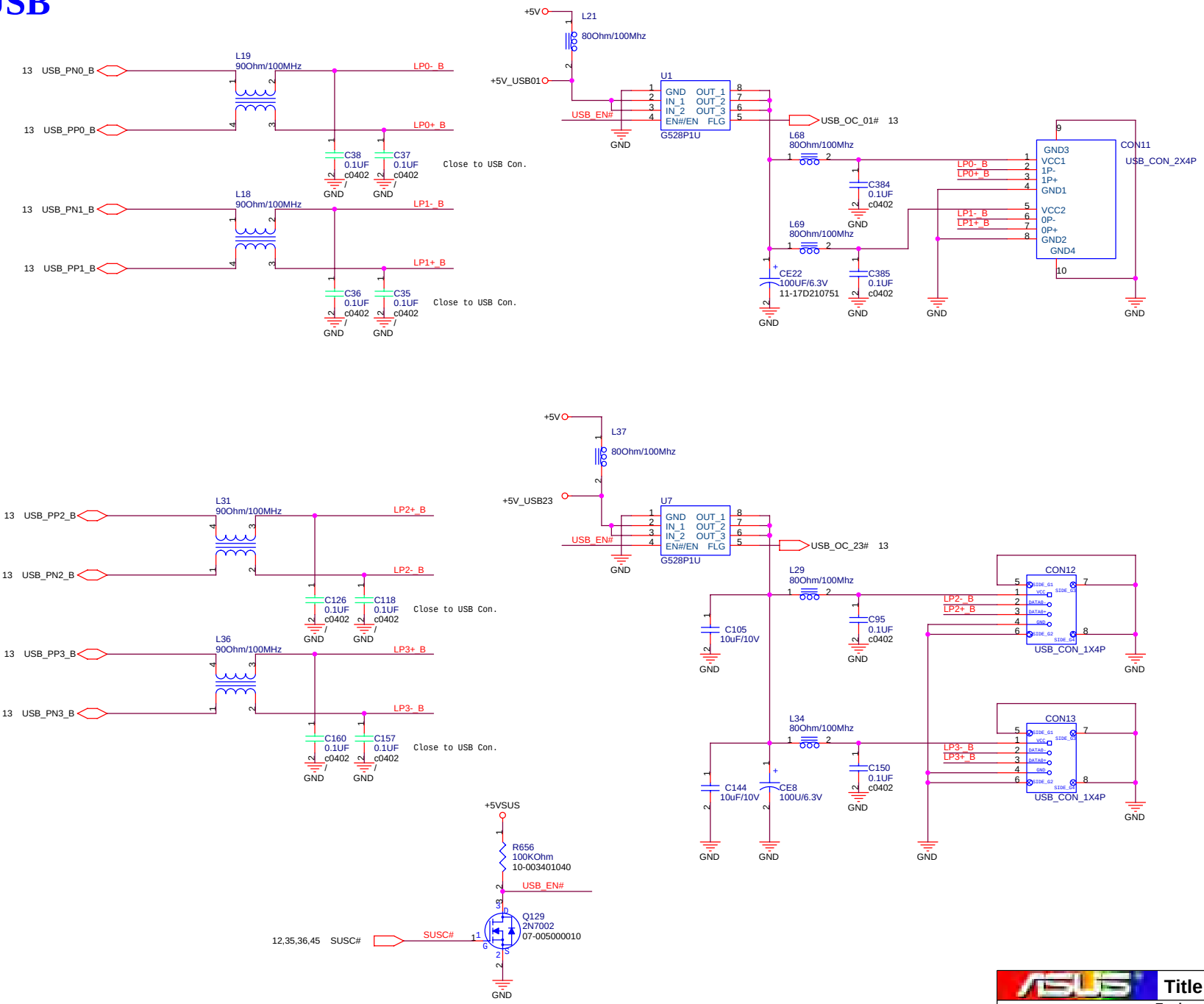
ALVISO



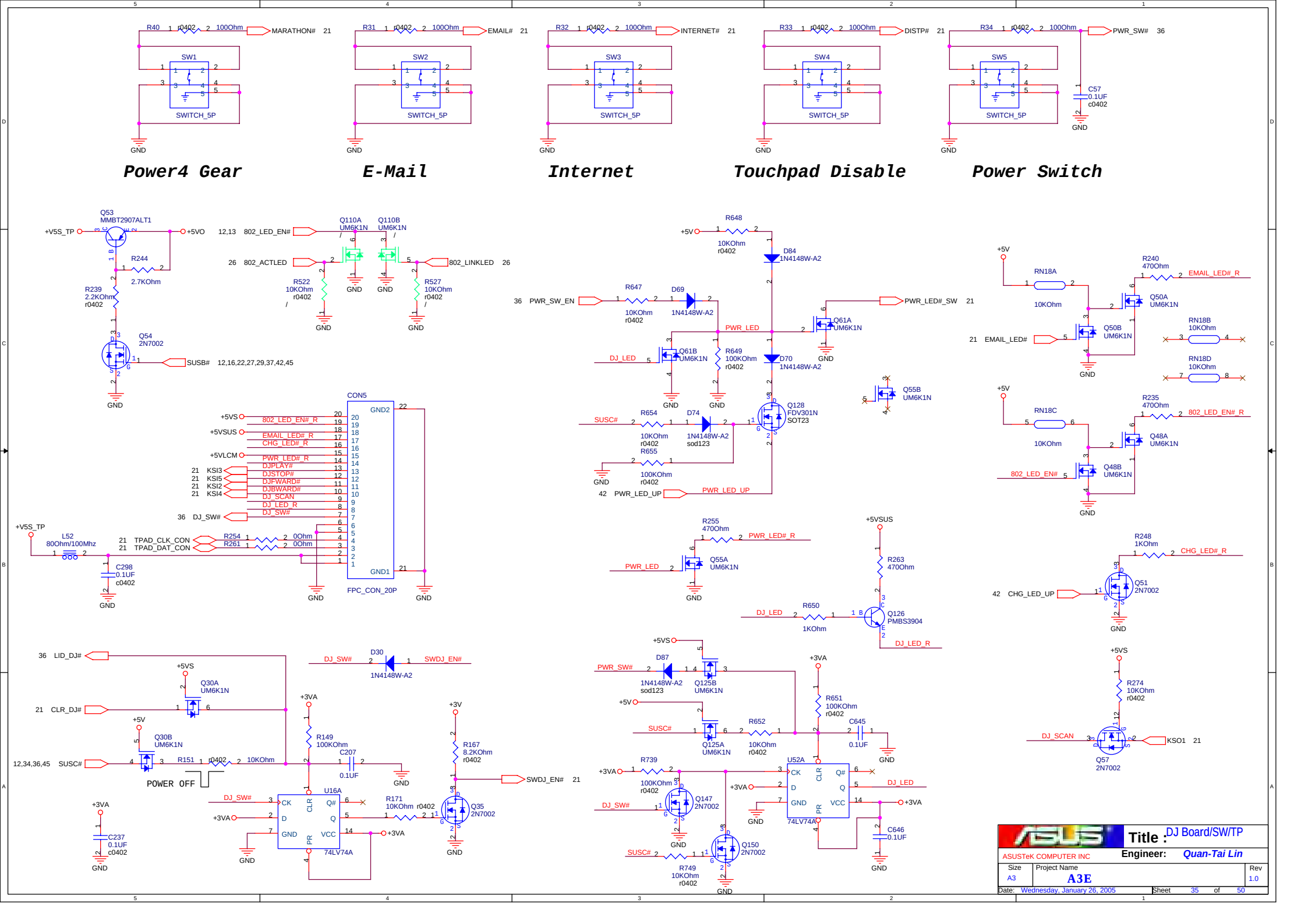


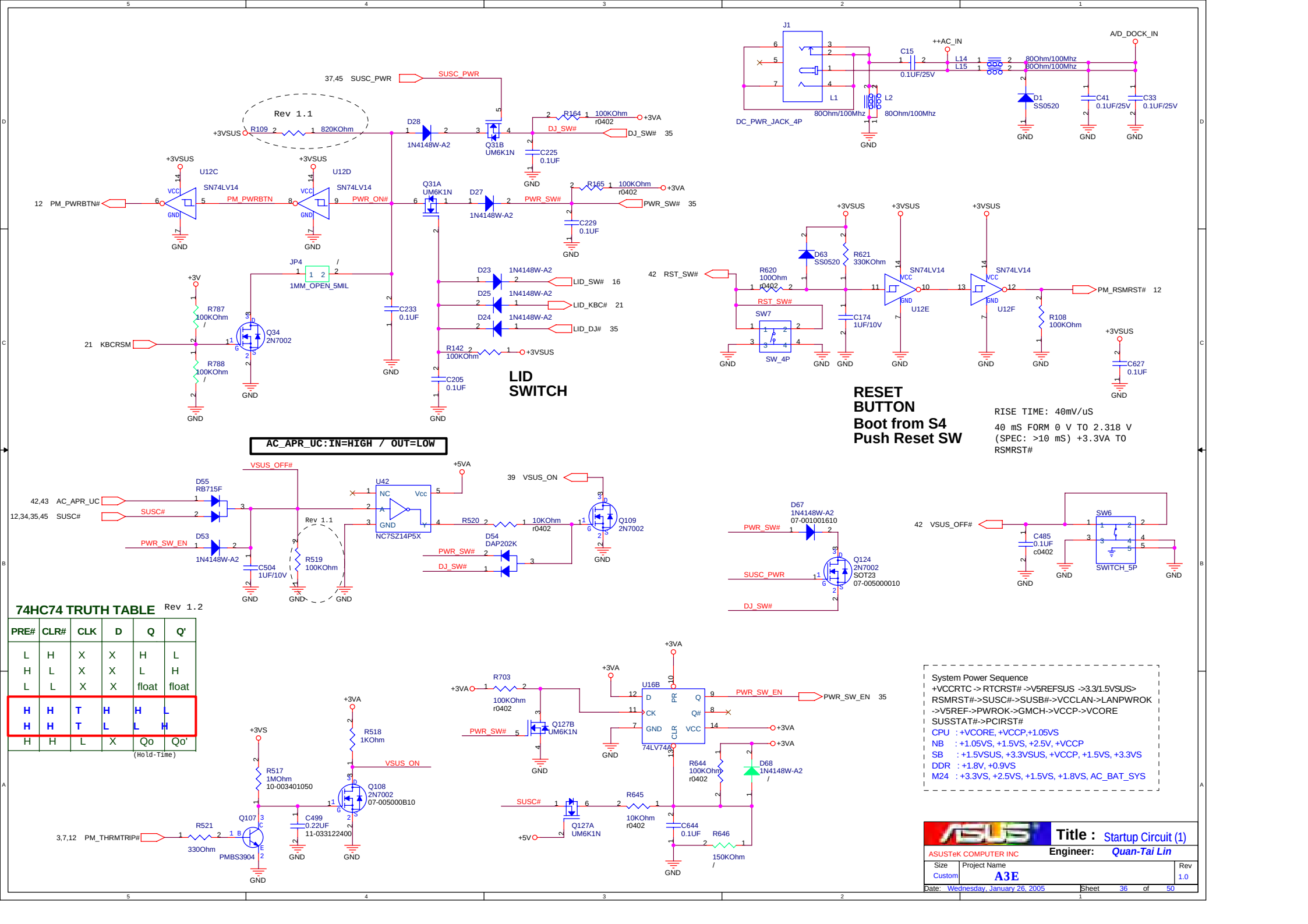
ASUSTeK COMPUTER INC	Title : CDROM	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 33 of 50	

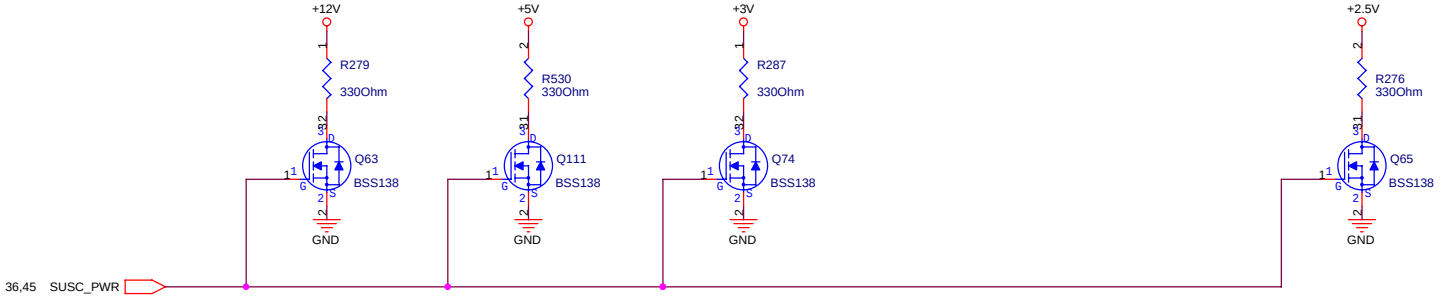
USB

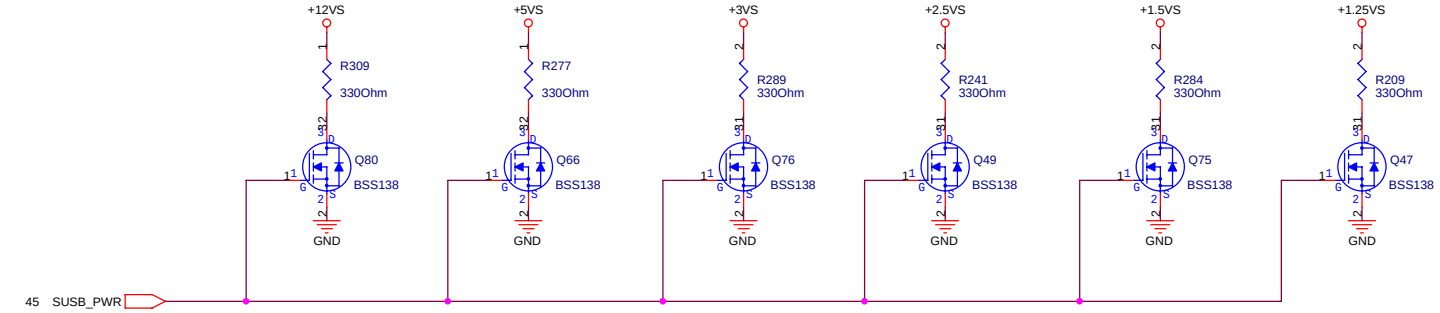


ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 34 of 50	


R40 r0402 100Ohm MARATHON# 21
SW1 SWITCH_5P
GND
Power4 Gear
R31 r0402 100Ohm EMAIL# 21
SW2 SWITCH_5P
GND
E-Mail
R32 r0402 100Ohm INTERNET# 21
SW3 SWITCH_5P
GND
Internet
R33 r0402 100Ohm DISTP# 21
SW4 SWITCH_5P
GND
Touchpad Disable
R34 r0402 100Ohm PWR_SW# 36
SW5 SWITCH_5P
C57 0.1UF c0402
GND
Power Switch
Q53 MMBT2907ALT1
+V5S_TP
+5VO
R244 2.7KOhm
R239 2.2KOhm r0402
Q54 2N7002
SUSB# 12,16,22,27,29,37,42,45
GND
12,13 802_LED_EN#
26 802_ACTLED
Q110A UM6K1N
Q110B UM6K1N
R522 10KOhm r0402
R527 10KOhm r0402
802_LINKLED 26
CON5
FPC_CON_20P
+5VS
+5VSUS
+5VLCM
802_LED_EN#_R
EMAIL_LED#_R
CHG_LED#_R
PWR_LED#_R
DJPLAY#
DJSTOP#
DJFWARD#
DJBWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
21 KSI3
21 KSI5
21 KSI2
21 KSI4
36 DJ_SW#
21 TPAD_CLK_CON
21 TPAD_DAT_CON
R254 0Ohm
R261 0Ohm
L52 80Ohm/100Mhz
C298 0.1UF c0402
R648 10KOhm r0402
D84 1N4148W-A2
36 PWR_SW_EN
R647 10KOhm r0402
D69 1N4148W-A2
PWR_LED
PWR_LED#_SW 21
Q61A UM6K1N
Q61B UM6K1N
DJ_LED
R649 100KOhm r0402
D70 1N4148W-A2
Q55B UM6K1N
SUSC#
R654 10KOhm r0402
D74 1N4148W-A2 sod123
Q128 FDV301N SOT23
R655 100KOhm r0402
42 PWR_LED_UP
RN18A 10KOhm
R240 470Ohm
EMAIL_LED#_R
Q50A UM6K1N
Q50B UM6K1N
21 EMAIL_LED#
RN18B 10KOhm
RN18D 10KOhm
RN18C 10KOhm
R235 470Ohm
802_LED_EN#_R
Q48A UM6K1N
Q48B UM6K1N
802_LED_EN#
R255 470Ohm
PWR_LED#_R
Q55A UM6K1N
R263 470Ohm
R650 1KOhm
Q126 PMBS3904
DJ_LED_R
R248 1KOhm
CHG_LED#_R
Q51 2N7002
42 CHG_LED_UP
36 LID_DJ#
21 CLR_DJ#
12,34,36,45 SUSC#
Q30A UM6K1N
Q30B UM6K1N
R151 r0402 10KOhm
POWER OFF
D30 1N4148W-A2
DJ_SW#
SWDJ_EN#
R149 100KOhm
C207 0.1UF
U16A 74LV74A
R171 10KOhm r0402
R167 8.2KOhm r0402
Q35 2N7002
SWDJ_EN# 21
C237 0.1UF c0402
D87 1N4148W-A2 sod123
Q125B UM6K1N
Q125A UM6K1N
R651 100KOhm r0402
R652 10KOhm r0402
C645 0.1UF
R739 100KOhm r0402
Q147 2N7002
U52A 74LV74A
C646 0.1UF
Q150 2N7002
R749 10KOhm r0402
R274 10KOhm r0402
DJ_SCAN
KSO1 21
Q57 2N7002
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size A3
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 35 of 50

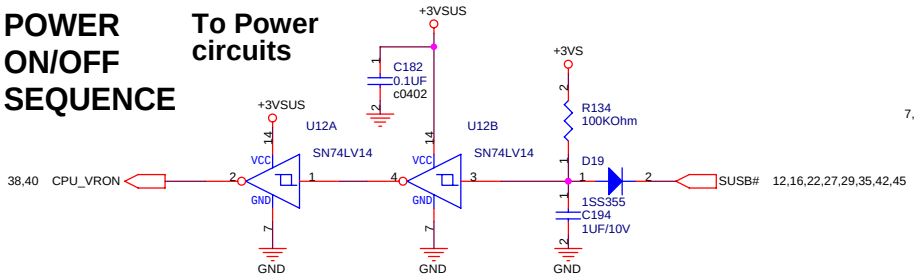

Rev 1.1
37,45 SUSC_PWR
SUSC_PWR
+3VSUS
R109 820KOhm
D28 1N4148W-A2
Q31B UM6K1N
C225 0.1UF
R164 100KOhm r0402
+3VA
DJ_SW# 35
+3VSUS
U12C SN74LV14
+3VSUS
U12D SN74LV14
12 PM_PWRBTN#
PM_PWRBTN
PWR_ON#
Q31A UM6K1N
D27 1N4148W-A2
PWR_SW#
R165 100KOhm r0402
PWR_SW# 35
C229 0.1UF
JP4
1MM_OPEN_5MIL
+3V
R787 100KOhm
R788 100KOhm
Q34 2N7002
21 KBCRSM
C233 0.1UF
D23 1N4148W-A2
D25 1N4148W-A2
D24 1N4148W-A2
LID_SW# 16
LID_KBC# 21
LID_DJ# 35
R142 100KOhm
+3VSUS
C205 0.1UF
GND
LID SWITCH
J1
DC_PWR_JACK_4P
L1 80Ohm/100Mhz
L2 80Ohm/100Mhz
C15 0.1UF/25V
++AC_IN
L14 L15
80Ohm/100Mhz
80Ohm/100Mhz
A/D_DOCK_IN
D1 SS0520
C41 0.1UF/25V
C33 0.1UF/25V
42 RST_SW#
R620 100Ohm r0402
RST_SW#
SW7
SW_4P
D63 SS0520
R621 330KOhm
C174 1UF/10V
U12E
U12F
R108 100KOhm
PM_RSMRST# 12
C627 0.1UF
RESET BUTTON
Boot from S4
Push Reset SW
RISE TIME: 40mV/uS
40 mS FORM 0 V TO 2.318 V (SPEC: >10 mS) +3.3VA TO RSMRST#
AC_APR_UC:IN=HIGH / OUT=LOW
42,43 AC_APR_UC
12,34,35,45 SUSC#
SUSC#
PWR_SW_EN
D55 RB715F
D53 1N4148W-A2
C504 1UF/10V
R519 100KOhm
VSUS_OFF#
U42 NC7SZ14P5X
+5VA
R520 10KOhm r0402
39 VSUS_ON
Q109 2N7002
D54 DAP202K
PWR_SW#
DJ_SW#
D67 1N4148W-A2 07-001001610
Q124 2N7002 SOT23 07-005000010
42 VSUS_OFF#
C485 0.1UF c0402
SW6 SWITCH_5P
74HC74 TRUTH TABLE Rev 1.2
PRE# CLR# CLK D Q Q'
L H X X H L
H L X X L H
L L X X float float
H H T H H L
H H T L L H
H H L X Qo Qo'
(Hold-Time)
3,7,12 PM_THRMTRIP#
R521 330Ohm
Q107 PMBS3904
+3VS
R517 1MOhm 10-003401050
C499 0.22UF 11-033122400
+3VA
R518 1KOhm
VSUS_ON
Q108 2N7002 07-005000B10
R703 100KOhm r0402
Q127B UM6K1N
U16B 74LV74A
PWR_SW_EN
PWR_SW_EN 35
+3VA
R644 100KOhm r0402
D68 1N4148W-A2
SUSC#
Q127A UM6K1N
R645 10KOhm r0402
C644 0.1UF
R646 150KOhm
+5V
System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.5VS, +2.5V, +VCCP
SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS
M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS
Title : Startup Circuit (1)
ASUSTeK COMPUTER INC
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 36 of 50

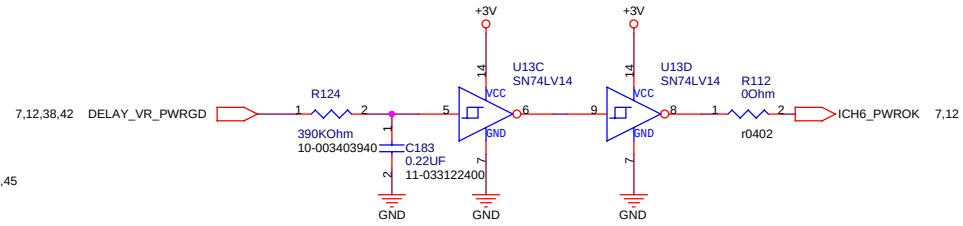




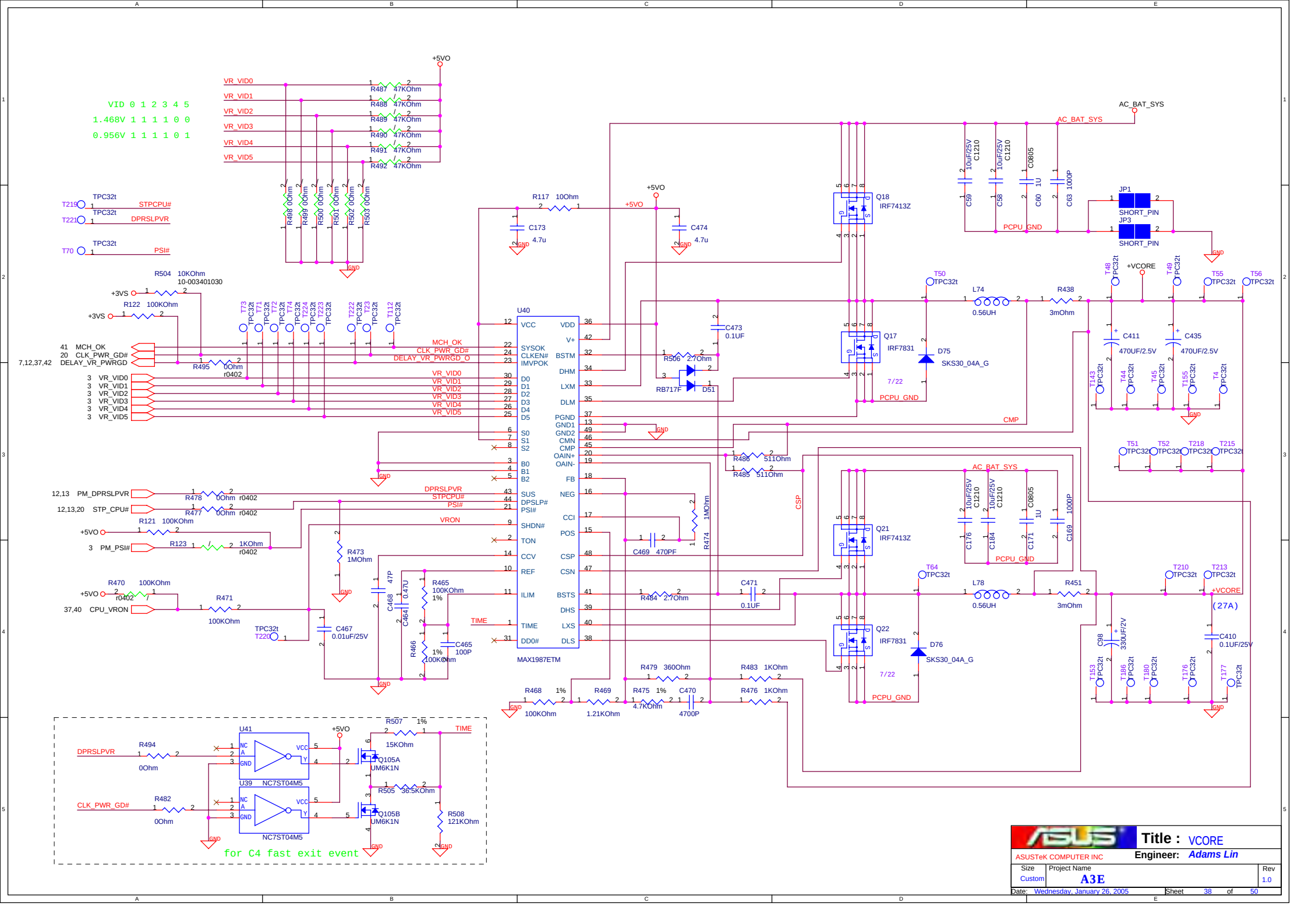
POWER ON/OFF SEQUENCE

To Power circuits

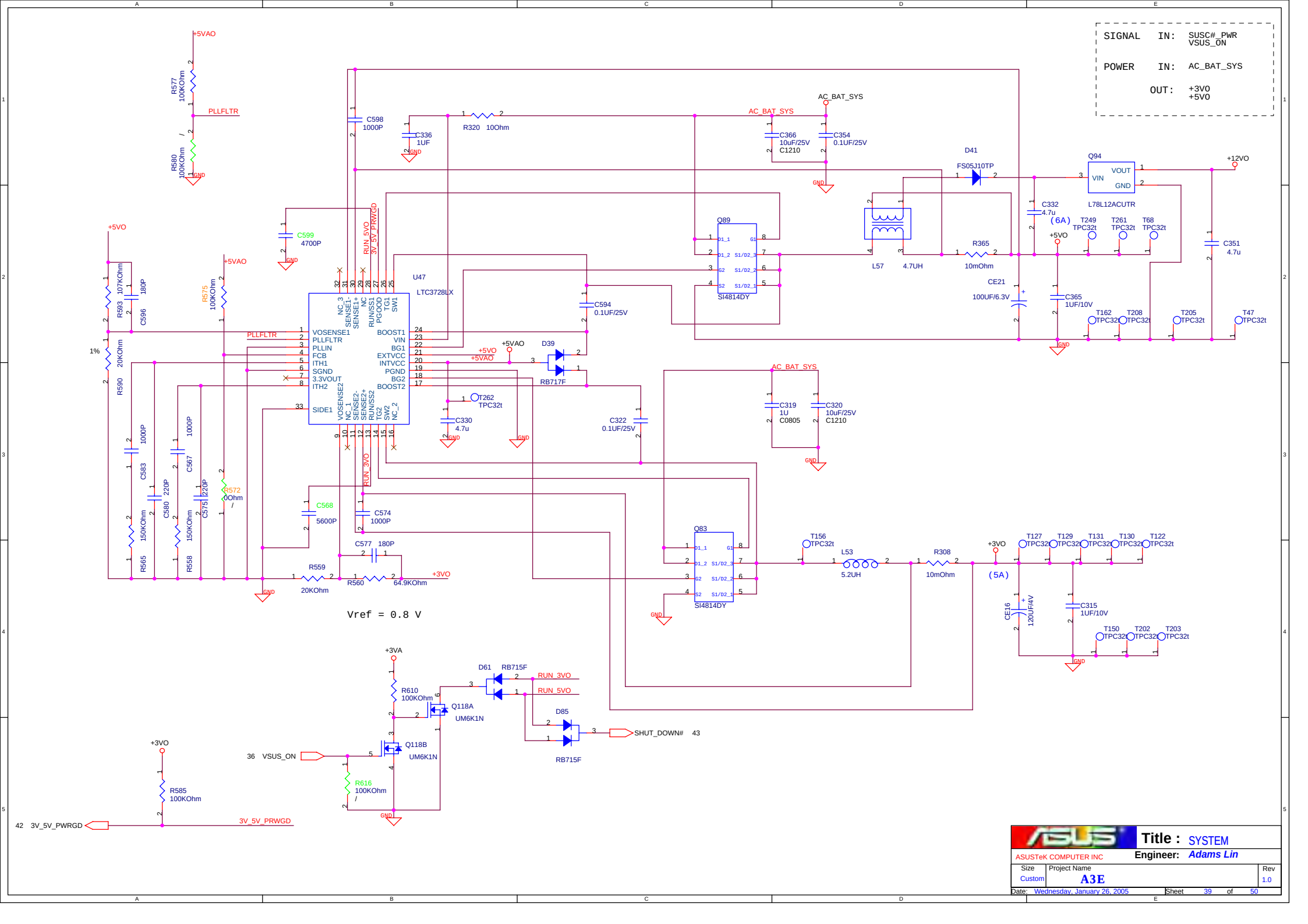


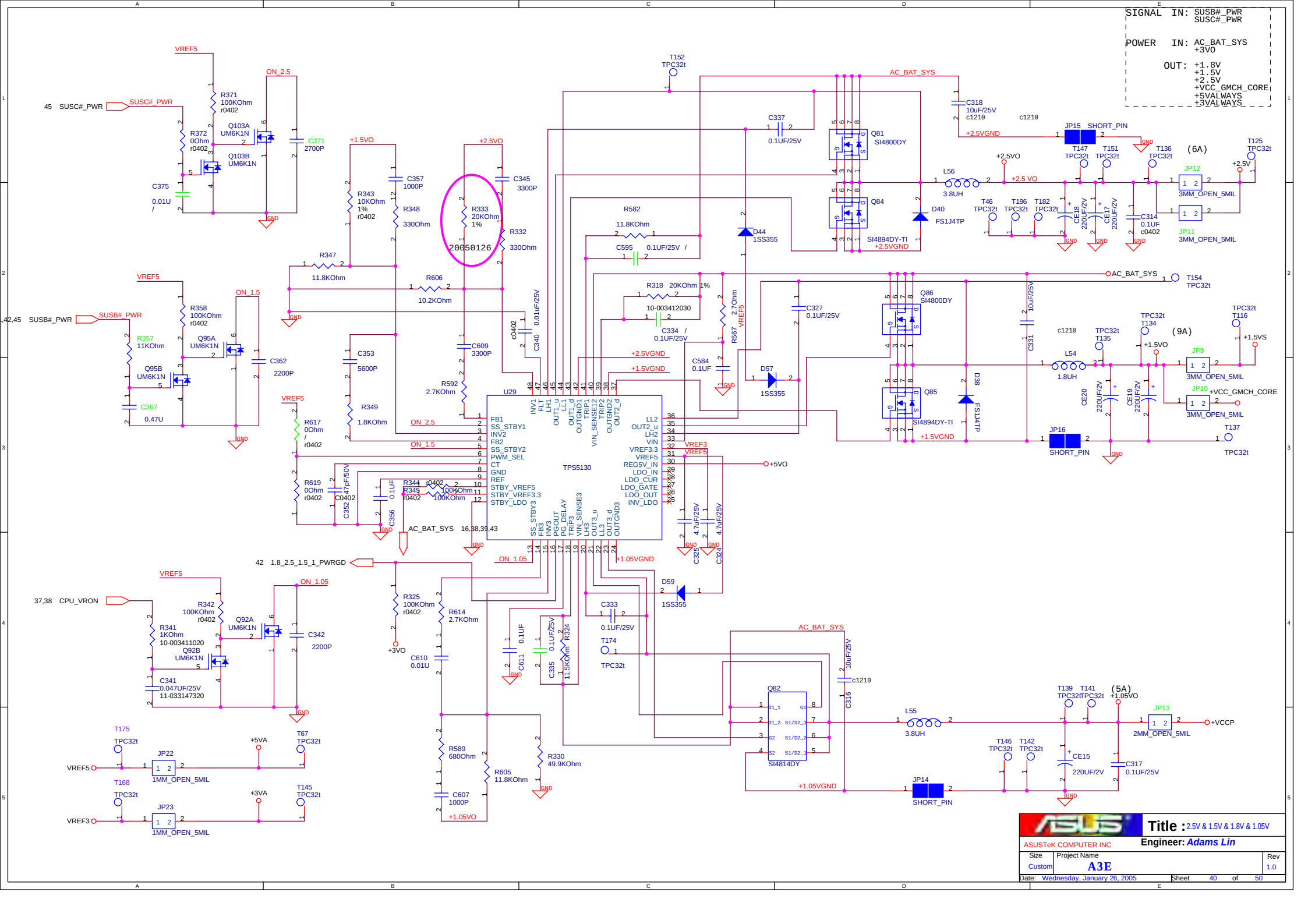


ASUSTeK COMPUTER INC	Title : Startup Circuit (2)	
	Engineer: *Quan-Tai Lin*	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 37 of 50	



Title :	VCORE
ASUSTeK COMPUTER INC	Engineer: Adams Lin
Size: Custom	Project Name: A3E
Rev	1.0
Date: Wednesday, January 26, 2005	Sheet 38 of 50


SIGNAL IN: SUSC#_PWR
VSUS_ON
POWER IN: AC_BAT_SYS
OUT: +3VO
+5VO
U47
LTC3728LX
Q89
SI4814DY
Q83
SI4814DY
Q94
L78L12ACUTR
D41
FS05J10TP
D39
RB717F
D61
RB715F
D85
RB715F
Q118A
UM6K1N
Q118B
UM6K1N
L57 4.7UH
L53 5.2UH
R320 10Ohm
R365 10mOhm
R308 10mOhm
R559 20KOhm
R560 64.9KOhm
Vref = 0.8 V
36 VSUS_ON
42 3V_5V_PWRGD
SHUT_DOWN# 43
Title : SYSTEM
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 39 of 50


SIGNAL IN: SUSB#_PWR
SUSC#_PWR
POWER IN: AC_BAT_SYS
+3VO
OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS
TPS5130
20050126
Title : 2.5V & 1.5V & 1.8V & 1.05V
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3E
Rev 1.0
Date: Wednesday, January 26, 2005
Sheet 40 of 50

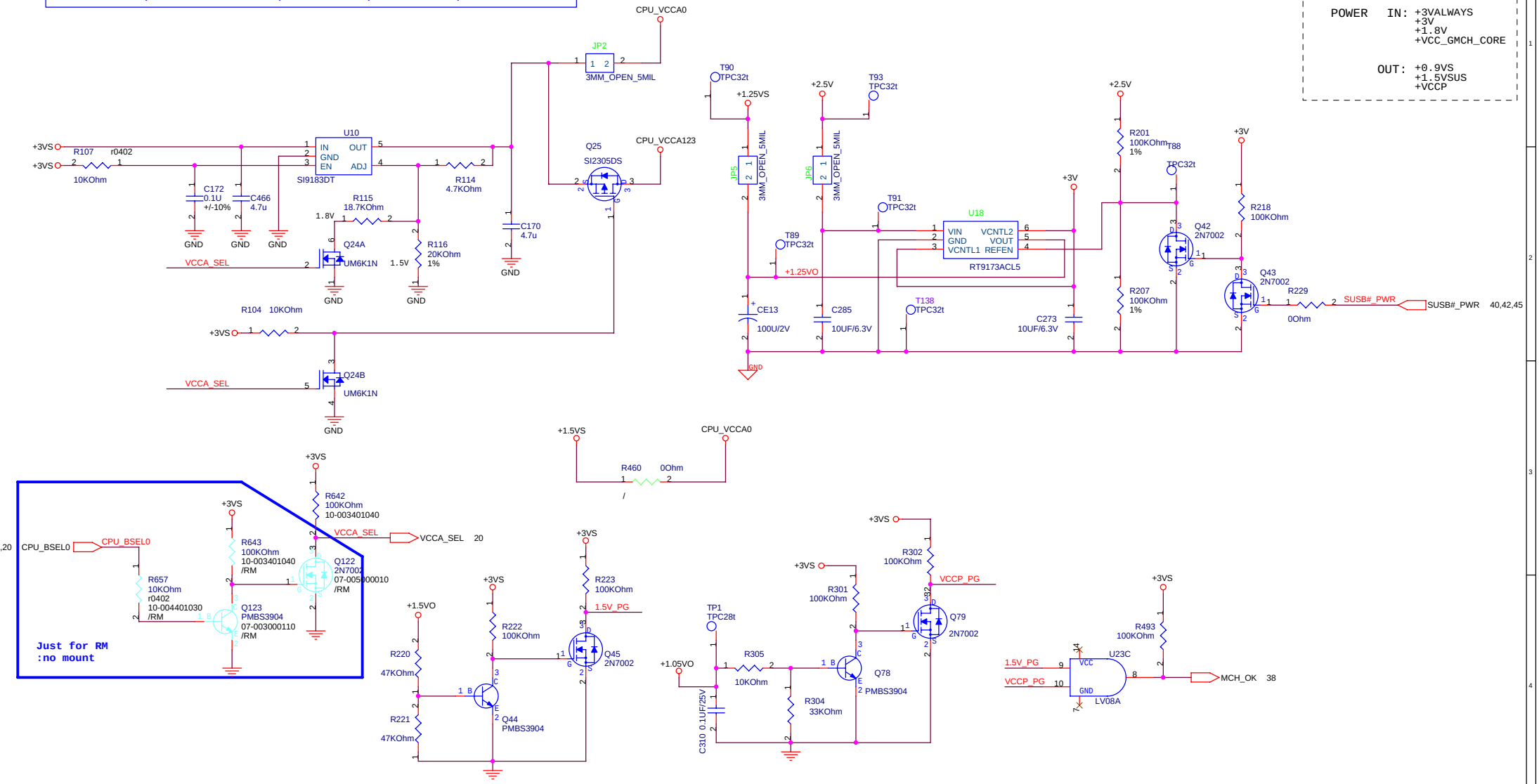
For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V

For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

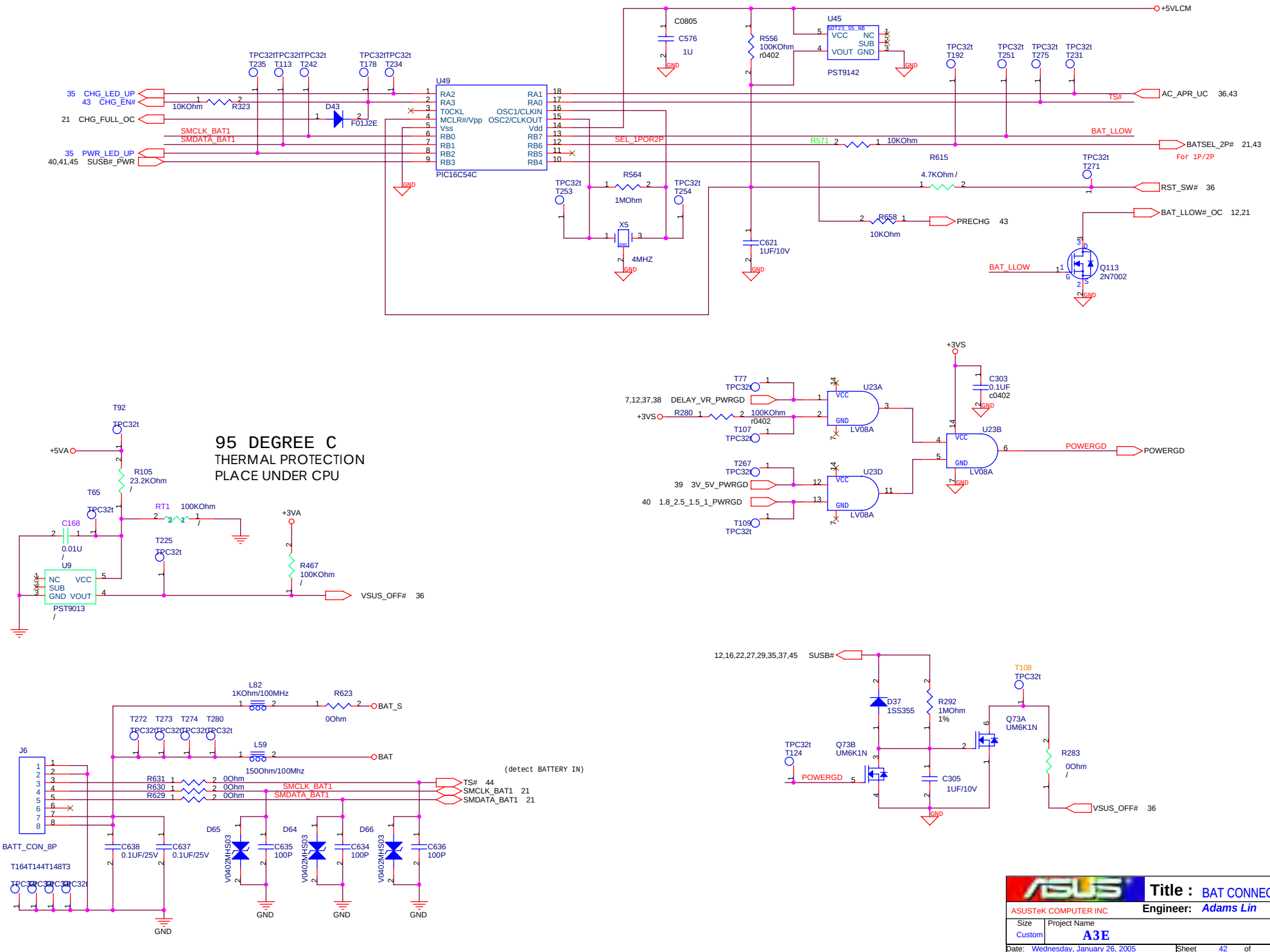
SIGNAL IN: SUSB#_PWR
CPU_VRON

POWER IN: +3VALWAYS
+3V
+1.8V
+VCC_GMCH_CORE

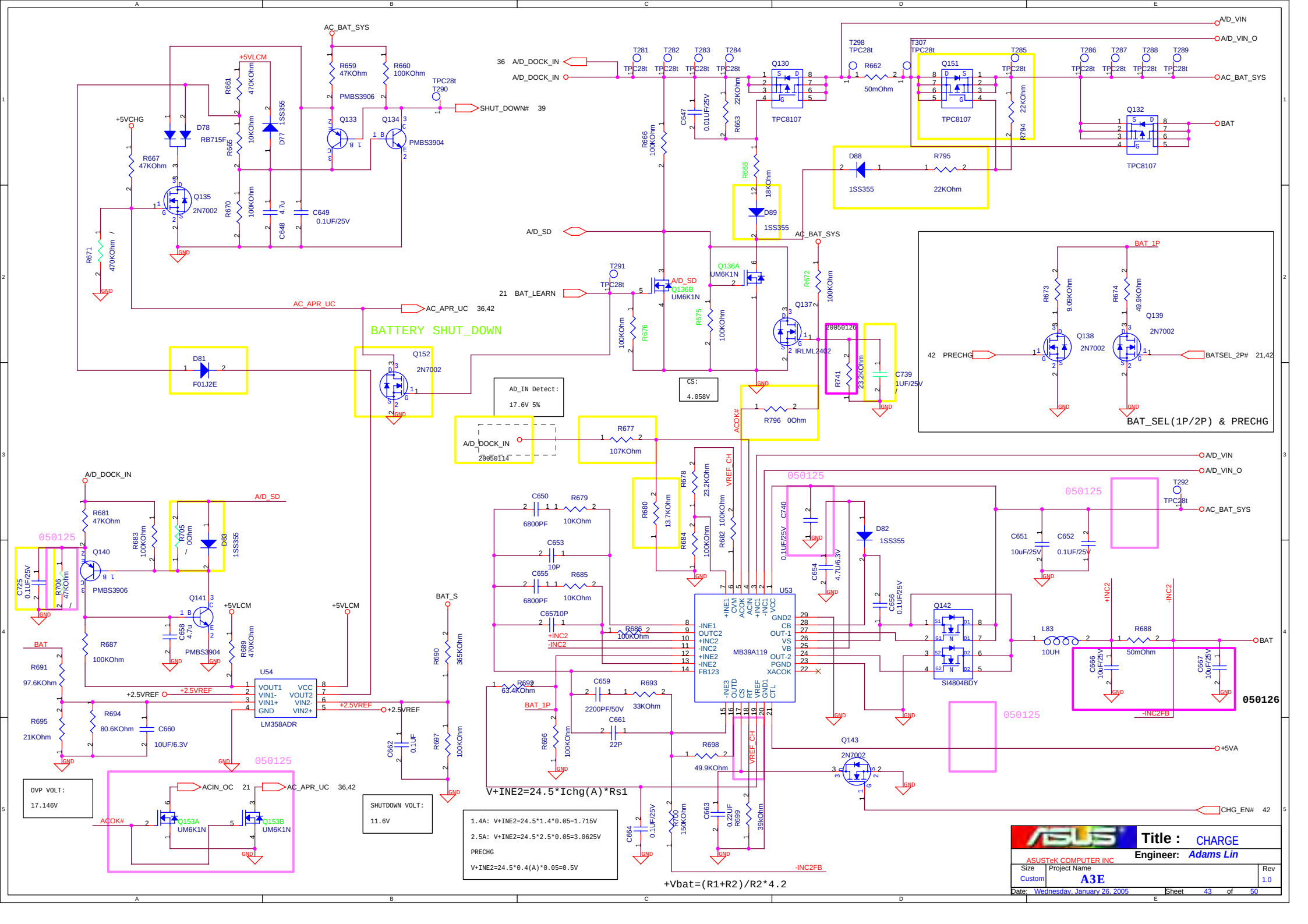
OUT: +0.9VS
+1.5VSUS
+VCCP

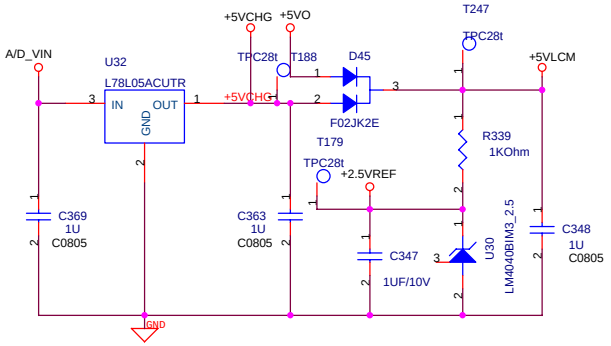


ASUSTeK COMPUTER INC	Title : 1.5VA & DDR2	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 41 of 50	

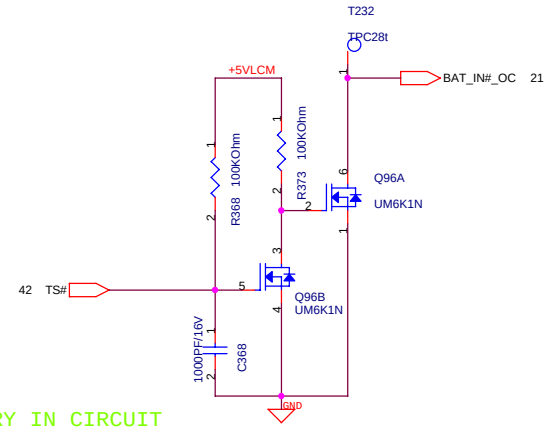


ASUSTeK COMPUTER INC	Title : BAT CONNECT	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 42 of 50	


AC_BAT_SYS
+5VLCM
+5VCHG
D78
RB715F
D77
1SS355
R659
47KOhm
R660
100KOhm
PMBS3906
TPC28t
T290
SHUT_DOWN#
39
Q133
Q134
PMBS3904
R661
470KOhm
R665
10KOhm
R667
47KOhm
Q135
2N7002
R670
100KOhm
C648
4.7u
C649
0.1UF/25V
R671
470KOhm
GND
AC_APR_UC
AC_APR_UC
36,42
BATTERY SHUT_DOWN
D81
F01J2E
Q152
2N7002
36
A/D_DOCK_IN
A/D_DOCK_IN
T281
T282
T283
T284
TPC28t
Q130
TPC8107
C647
0.01UF/25V
R663
22KOhm
R666
100KOhm
R668
18KOhm
D89
1SS355
T298
TPC28t
R662
50mOhm
T307
TPC28t
Q151
TPC8107
T285
R794
22KOhm
D88
1SS355
R795
22KOhm
T286
T287
T288
T289
Q132
TPC8107
A/D_VIN
A/D_VIN_O
AC_BAT_SYS
BAT
A/D_SD
21
BAT_LEARN
T291
Q136A
UM6K1N
Q136B
UM6K1N
R672
100KOhm
R675
100KOhm
R676
100KOhm
Q137
IRLML2402
20050126
R741
23.2KOhm
C739
1UF/25V
R796
0Ohm
ACOK#
AD_IN Detect:
17.6V 5%
CS:
4.058V
A/D_DOCK_IN
20050114
R677
107KOhm
BAT_1P
R673
9.09KOhm
R674
49.9KOhm
Q139
2N7002
Q138
2N7002
42
PRECHG
BATSEL_2P#
21,42
BAT_SEL(1P/2P) & PRECHG
A/D_DOCK_IN
R681
47KOhm
R683
100KOhm
R705
0Ohm
D83
1SS355
A/D_SD
050125
Q140
PMBS3906
C725
0.1UF/25V
R706
47KOhm
Q141
PMBS3904
C658
4.7u
R687
100KOhm
R689
470KOhm
+5VLCM
+5VLCM
BAT
R691
97.6KOhm
R695
21KOhm
R694
80.6KOhm
C660
10UF/6.3V
+2.5VREF
+2.5VREF
U54
VOUT1
VIN1-
VIN1+
GND
VCC
VOUT2
VIN2-
VIN2+
LM358ADR
+2.5VREF
+2.5VREF
BAT_S
R690
365KOhm
R697
100KOhm
C662
0.1UF
GND
050125
ACIN_OC
21
AC_APR_UC
36,42
ACOK#
Q153A
UM6K1N
Q153B
UM6K1N
OVP VOLT:
17.146V
SHUTDOWN VOLT:
11.6V
C650
6800PF
R679
10KOhm
C653
10P
C655
6800PF
R685
10KOhm
C657
10P
+INC2
-INC2
R686
100KOhm
R692
63.4KOhm
BAT_1P
R696
100KOhm
C659
2200PF/50V
R693
33KOhm
C661
22P
R698
49.9KOhm
VREF_CH
R678
23.2KOhm
R680
13.7KOhm
R682
100KOhm
R684
100KOhm
VREF_CH
U53
MB39A119
-INE1
OUTC2
+INC2
-INC2
+INE2
-INE2
FB123
+INE1
CVM
ACOK
ACIN
+INC1
-INC1
VCC
GND2
CB
OUT-1
VS
VB
OUT-2
PGND
XACOK
-INE3
OUTD
CS
RT
VREF
GND1
CTL
C740
0.1UF/25V
C654
4.7U/6.3V
D82
1SS355
C656
0.1UF/25V
Q142
SI4804BDY
C651
10uF/25V
C652
0.1UF/25V
T292
TPC28t
AC_BAT_SYS
L83
10UH
+INC2
-INC2
R688
50mOhm
BAT
C666
10uF/25V
C667
10uF/25V
-INC2FB
050126
050125
+5VA
Q143
2N7002
CHG_EN#
42
V+INE2=24.5*Ichg(A)*Rs1
1.4A: V+INE2=24.5*1.4*0.05=1.715V
2.5A: V+INE2=24.5*2.5*0.05=3.0625V
PRECHG
V+INE2=24.5*0.4(A)*0.05=0.5V
C664
0.1UF/25V
R700
150KOhm
C663
0.22UF
R699
39KOhm
-INC2FB
+Vbat=(R1+R2)/R2*4.2
Title : CHARGE
Engineer: Adams Lin
ASUSTeK COMPUTER INC
Size
Custom
Project Name
A3E
Rev
1.0
Date: Wednesday, January 26, 2005
Sheet 43 of 50

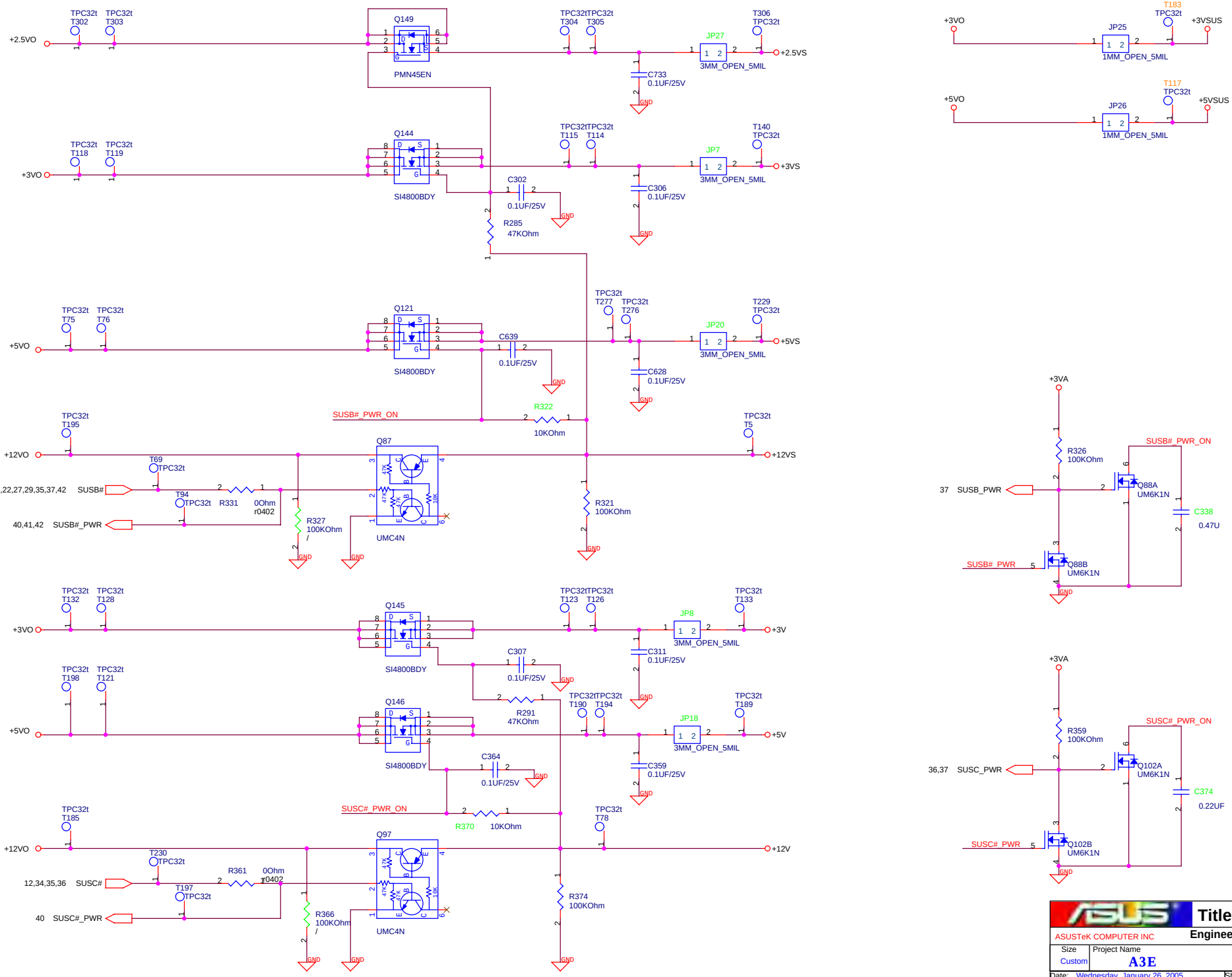


+5VCHG, +5VLCM, +2.5VREF



BATTERY IN CIRCUIT

ASUSTeK COMPUTER INC	Title : BATLOW/SD#	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 44 of 50	



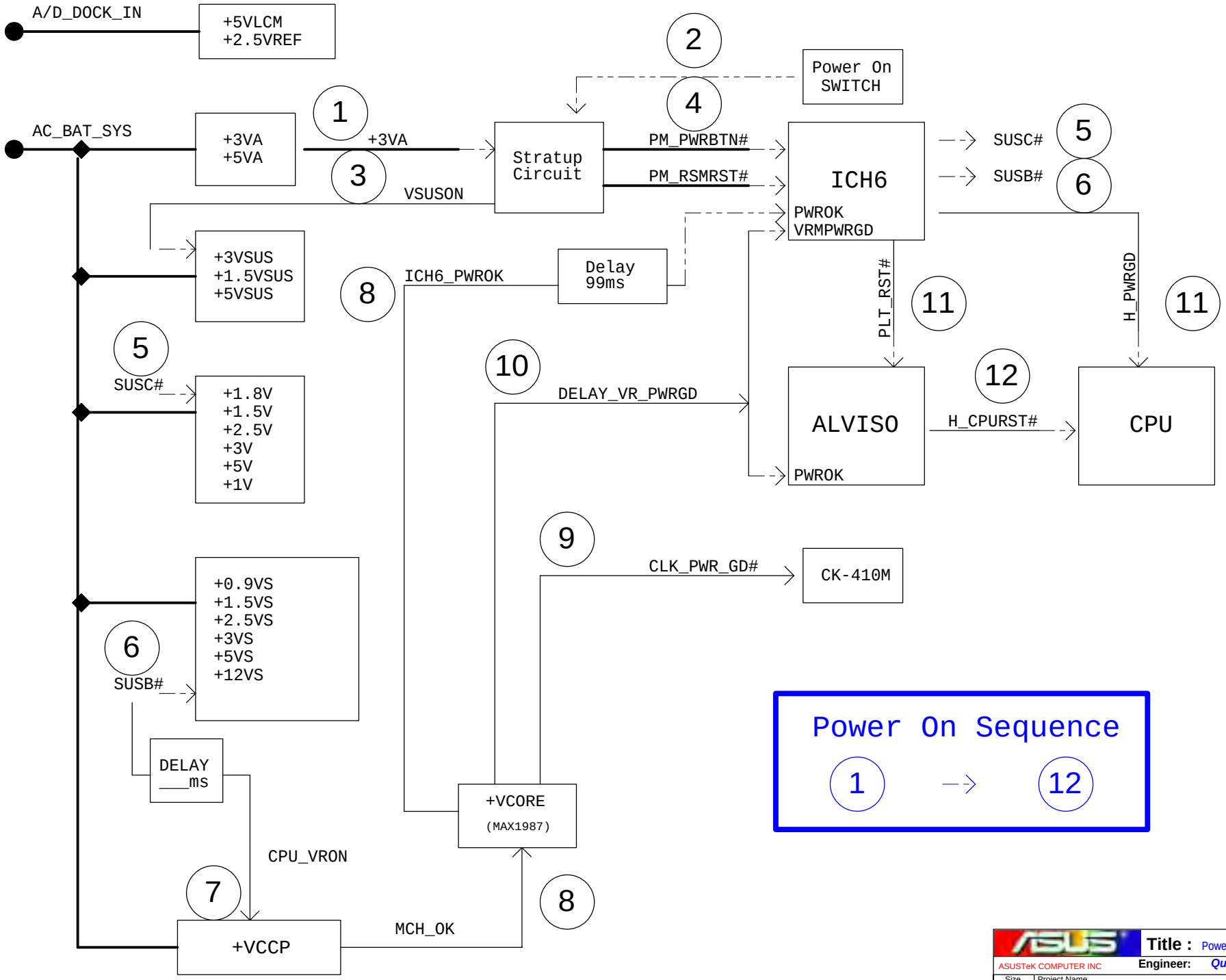
Title : LOAD SWITCH

ASUSTeK COMPUTER INC

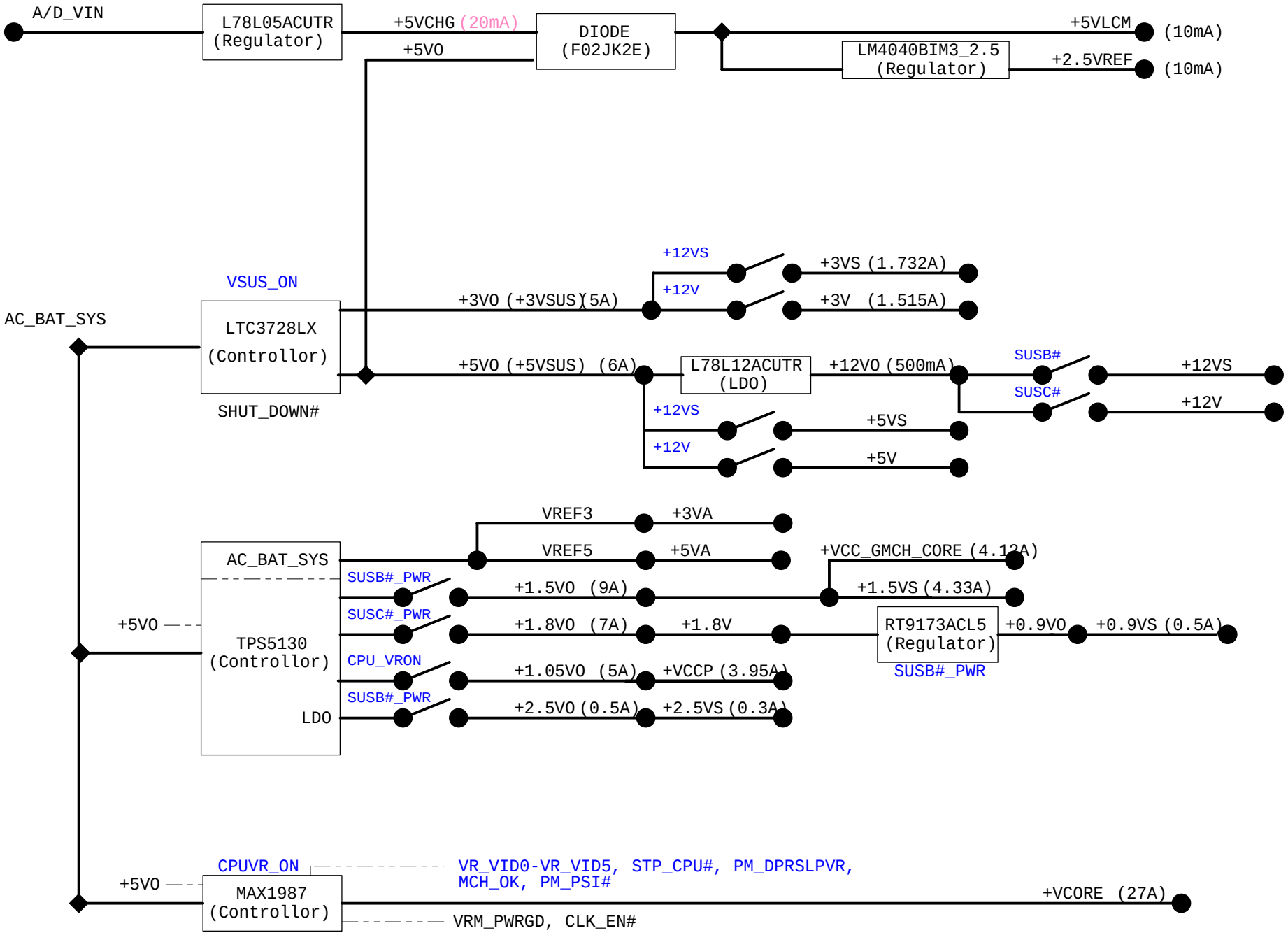
Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 45 of 50



ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 46 of 50		



ASUSTeK COMPUTER INC	Title : POWER FLOWCHART	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 1.0
Date: Wednesday, January 26, 2005	Sheet 47 of 50	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Title : System Resource

ASUSTeK COMPUTER INC Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 48 of 50

Rev.	Data	Description
1.0	05' 01/06	Initial release
2005/01/21-1140		R735.R736.R750.R752 footprint change to 0603
2005/01/21-1140		JP28 for CMOS clear renames to JRST1 and no mount
2005/01/21-1140		U19.77 signal changes to ACIN_OC and R245 still mount
2005/01/21-1140		R73.R75.R76.R77 value change to 470ohm and R41 is 330ohm
2005/01/21-1140		R519 value changes to 100Kohm
2005/01/24-1035		Add SW8 ,R797 but no mount
2005/01/26-0945		R109 value changes to 820Kohm
2005/01/26-0945		D72 mount

Rev.	Data	Description
For RM:		
2005/01/24-1035		Page 31 no mount : R566,Q114,Q115,C579,C564 Page 20 no mount : R54,R43,Q16,Q19,R412 Page 41 no mount : R657,R643,Q122,Q123 Mount SW8 ,R797 Add SWITCH TABLE for CPU frequency select

ASUSTeK COMPUTER INC

Title : History-EE

Engineer: *Quan-Tai Lin*

Size	Project Name	Rev
A3	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 49 of 50

Rev.	Data	Description
1.0	05' 01/06	Initial release
	2005/01/21-1200	Add 22Kohm R794.R795 , P-MOS Q151 , diode D88.D89
	2005/01/21-1200	Add capacitor C739,resistor R796,N-MOS Q152,diode D90
	2005/01/21-1200	R677 value is from 110Kohm to 107Kohm and R677.1 connect to A/D_DOCK_IN
	2005/01/21-1200	R680 value is from 14Kohm to 13.7Kohm and D81 changes to F01J2E
	2005/01/21-1200	D83 mount and R705 no mount and R725 mount
	2005/01/26-0945	R333 value changes to 20Kohm
	2005/01/26-0945	Add Q153 for ACIN_OC and AC_APR_UC signals and delete D90
	2005/01/26-0945	Change U53.18 and U53.19 for signal VREF_CH
	2005/01/26-0945	Delete JP24 and add a cap C740 0.1UF
	2005/01/26-0945	C725 still mount and R706 no mount
	2005/01/26-0945	R741 value changes to 23.2K ohm
	2005/01/26-1250	C666 changes to connect to L83.2

Rev.	Data	Description

ASUSTeK COMPUTER INC

Title : History-PWR

Engineer: *Quan-Tai Lin*

Size	Project Name	Rev
Custom	A3E	1.0

Date: Wednesday, January 26, 2005 Sheet 50 of 50