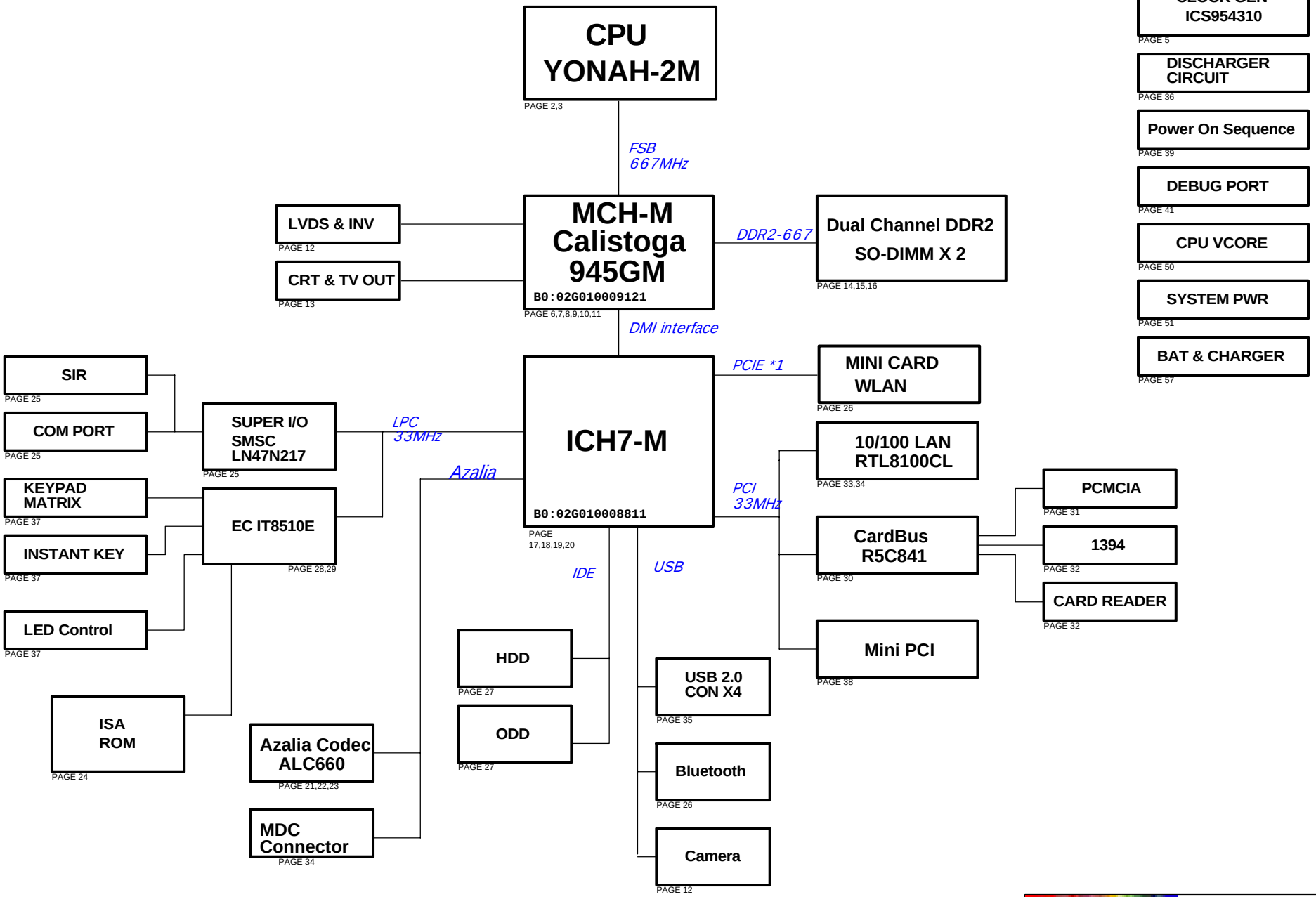
A3F Block Diagram



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Ping-Yen Tsai	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 1 of 63	

6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]

U200A

ADDR GROUP 0

H_A#3 J4 A[3]#
H_A#4 L4 A[4]#
H_A#5 M3 A[5]#
H_A#6 K5 A[6]#
H_A#7 M1 A[7]#
H_A#8 N2 A[8]#
H_A#9 J1 A[9]#
H_A#10 N3 A[10]#
H_A#11 P5 A[11]#
H_A#12 P2 A[12]#
H_A#13 L1 A[13]#
H_A#14 P4 A[14]#
H_A#15 P1 A[15]#
H_A#16 R1 A[16]#
6 H_ADSTB#0 L2 ADSTB[0]#

H_REQ#0 K3 REQ[0]#
H_REQ#1 H2 REQ[1]#
H_REQ#2 K2 REQ[2]#
H_REQ#3 J3 REQ[3]#
H_REQ#4 L5 REQ[4]#

ADDR GROUP 1

H_A#17 Y2 A[17]#
H_A#18 U5 A[18]#
H_A#19 R3 A[19]#
H_A#20 W6 A[20]#
H_A#21 U4 A[21]#
H_A#22 Y5 A[22]#
H_A#23 U2 A[23]#
H_A#24 R4 A[24]#
H_A#25 T5 A[25]#
H_A#26 T3 A[26]#
H_A#27 W3 A[27]#
H_A#28 W5 A[28]#
H_A#29 Y4 A[29]#
H_A#30 W2 A[30]#
H_A#31 Y1 A[31]#
6 H_ADSTB#1 V4 ADSTB[1]#

CONTROL

ADS# H1 H_ADS# → H_ADS# 6
BNR# E2 H_BNR# → H_BNR# 6
BPRI# G5 H_BPRI# → H_BPRI# 6
DEFER# H5 H_DEFER# → H_DEFER# 6
DRDY# F21 H_DRDY# → H_DRDY# 6
DBSY# E1 H_DBSY# → H_DBSY# 6
BR0# F1 H_BR0# → H_BR0# 6
IERR# D20
INIT# B3 H_INIT# → H_INIT# 17
LOCK# H4 H_LOCK# → H_LOCK# 6
RESET# B1 H_CPURST# → H_CPURST# 6
RS[0]# F3 H_RS#0 → H_RS#0 6
RS[1]# F4 H_RS#1 → H_RS#1 6
RS[2]# G3 H_RS#2 → H_RS#2 6
TRDY# G2 H_TRDY# → H_TRDY# 6
HIT# G6 H_HIT# → H_HIT# 6
HITM# E4 H_HITM# → H_HITM# 6

R201 56Ohm: H_IERR# D20 → +VCCP_AGTL+
R202 54.9Ohm /: H_CPURST# → +VCCP_AGTL+
T200, T201

XDP/ITP SIGNALS

BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2 PRDY# → T202
PREQ# AC1 PREQ# → R203 56Ohm / → +VCCP_AGTL+
TCK AC5 TCK → R204 56Ohm → +VCCP_AGTL+
TDI AA6 TDI → R205 56Ohm → +VCCP_AGTL+
TDO AB3 TDO → R217 56Ohm / → +VCCP_AGTL+
TMS AB5 TMS → R206 56Ohm → +VCCP_AGTL+
TRST# AB6 TRST# → R207 56Ohm → +VCCP_AGTL+
DBR# C20 CPU_DBR# → T204 TPC28T
GND

THERM

PROCHOT# D21 H_PROCHOT_S#
THERMDA A24 CPU_THRM_DA → CPU_THRM_DA 4
THERMDC A25 CPU_THRM_DC → CPU_THRM_DC 4
THERMTRIP# C7 PM_THRMTRIP# → PM_THRMTRIP# 4,7,17

HCLK

17 H_A20M# A6 A20M#
17 H_FERR# A5 FERR#
17 H_IGNNE# C4 IGNNE#
17 H_STPCLK# D5 STPCLK#
17 H_INTR C6 LINT0
17 H_NMI B4 LINT1
17 H_SMI# A3 SMI#
BCLK[0] A22 CLK_CPU_BCLK → CLK_CPU_BCLK 5
BCLK[1] A21 CLK_CPU_BCLK# → CLK_CPU_BCLK# 5

RESERVED

RSVD[1] AA1
RSVD[2] AA4
RSVD[3] AB2
RSVD[4] AA3
RSVD[5] M4
RSVD[6] N5
RSVD[7] T2
RSVD[8] V3
RSVD[9] B2
RSVD[10] C3
RSVD[11] B25
RSVD[12] T22
RSVD[A2] A2
RSVD[13] D2
RSVD[14] F6
RSVD[15] D3
RSVD[16] C1
RSVD[17] AF1
RSVD[18] D22
RSVD[19] C23
RSVD[20] C24

SOCKET479P

12G04600479A

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

+VCCP_AGTL+ → R200 1KOhm 1% → H_GTLREF
C200 0.1UF/10V / → GND
R211 2KOhm 1% → GND
<500 mil (55 Ohm) T/B trace 5.5 Space 25
R212 1KOhm, R214 51Ohm → GND
H_GTLREF AD26
H_TEST1 C26
H_TEST2 D25
H_BSEL0 B22
H_BSEL1 B23
H_BSEL2 C21

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

U200B

6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0

DATA GRP 0

H_D#0 E22 D[0]#
H_D#1 F24 D[1]#
H_D#2 E26 D[2]#
H_D#3 H22 D[3]#
H_D#4 F23 D[4]#
H_D#5 G25 D[5]#
H_D#6 E25 D[6]#
H_D#7 E23 D[7]#
H_D#8 K24 D[8]#
H_D#9 G24 D[9]#
H_D#10 J24 D[10]#
H_D#11 J23 D[11]#
H_D#12 H26 D[12]#
H_D#13 F26 D[13]#
H_D#14 K22 D[14]#
H_D#15 H25 D[15]#
H_DSTBN#0 H23 DSTBN[0]#
H_DSTBP#0 G22 DSTBP[0]#
H_DINV#0 J26 DINV[0]#

DATA GRP 2

D[32]# AA23 H_D#32
D[33]# AB24 H_D#33
D[34]# V24 H_D#34
D[35]# V26 H_D#35
D[36]# W25 H_D#36
D[37]# U23 H_D#37
D[38]# U25 H_D#38
D[39]# U22 H_D#39
D[40]# AB25 H_D#40
D[41]# W22 H_D#41
D[42]# Y23 H_D#42
D[43]# AA26 H_D#43
D[44]# Y26 H_D#44
D[45]# Y22 H_D#45
D[46]# AC26 H_D#46
D[47]# AA24 H_D#47
DSTBN[2]# W24 H_DSTBN#2 → H_DSTBN#2 6
DSTBP[2]# Y25 H_DSTBP#2 → H_DSTBP#2 6
DINV[2]# V23 H_DINV#2 → H_DINV#2 6

6 H_DSTBN#1
6 H_DSTBP#1
6 H_DINV#1

DATA GRP 1

H_D#16 N22 D[16]#
H_D#17 K25 D[17]#
H_D#18 P26 D[18]#
H_D#19 R23 D[19]#
H_D#20 L25 D[20]#
H_D#21 L22 D[21]#
H_D#22 L23 D[22]#
H_D#23 M23 D[23]#
H_D#24 P25 D[24]#
H_D#25 P22 D[25]#
H_D#26 P23 D[26]#
H_D#27 T24 D[27]#
H_D#28 R24 D[28]#
H_D#29 L26 D[29]#
H_D#30 T25 D[30]#
H_D#31 N24 D[31]#
H_DSTBN#1 M24 DSTBN[1]#
H_DSTBP#1 N25 DSTBP[1]#
H_DINV#1 M26 DINV[1]#

DATA GRP 3

D[48]# AC22 H_D#48
D[49]# AC23 H_D#49
D[50]# AB22 H_D#50
D[51]# AA21 H_D#51
D[52]# AB21 H_D#52
D[53]# AC25 H_D#53
D[54]# AD20 H_D#54
D[55]# AE22 H_D#55
D[56]# AF23 H_D#56
D[57]# AD24 H_D#57
D[58]# AE21 H_D#58
D[59]# AD21 H_D#59
D[60]# AE25 H_D#60
D[61]# AF25 H_D#61
D[62]# AF22 H_D#62
D[63]# AF26 H_D#63
DSTBN[3]# AD23 H_DSTBN#3 → H_DSTBN#3 6
DSTBP[3]# AE24 H_DSTBP#3 → H_DSTBP#3 6
DINV[3]# AC20 H_DINV#3 → H_DINV#3 6

MISC

GTLREF
TEST1
TEST2
BSEL[0]
BSEL[1]
BSEL[2]
COMP[0] R26 H_COMP0 R208 1 2 27.4Ohm 1%
COMP[1] U26 H_COMP1 R209 1 2 54.9Ohm 1%
COMP[2] U1 H_COMP2 R210 1 2 27.4Ohm 1%
COMP[3] V1 H_COMP3 R213 1 2 54.9Ohm 1%
GND
DPRSTP# E5 H_DPRSTP# → H_DPRSTP# 17,50
DPSLP# B5 H_DPSLP# → H_DPSLP# 17
DPWR# D24 H_DPWR# → H_DPWR# 6
PWRGOOD D6 H_PWRGD → H_PWRGD 17
SLP# D7
PSI# AE6 H_CPUSLP# → H_CPUSLP# 6,17
T205
PM_PSI# → PM_PSI# 50

SOCKET479P
12G04600479A
12G04600479A

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

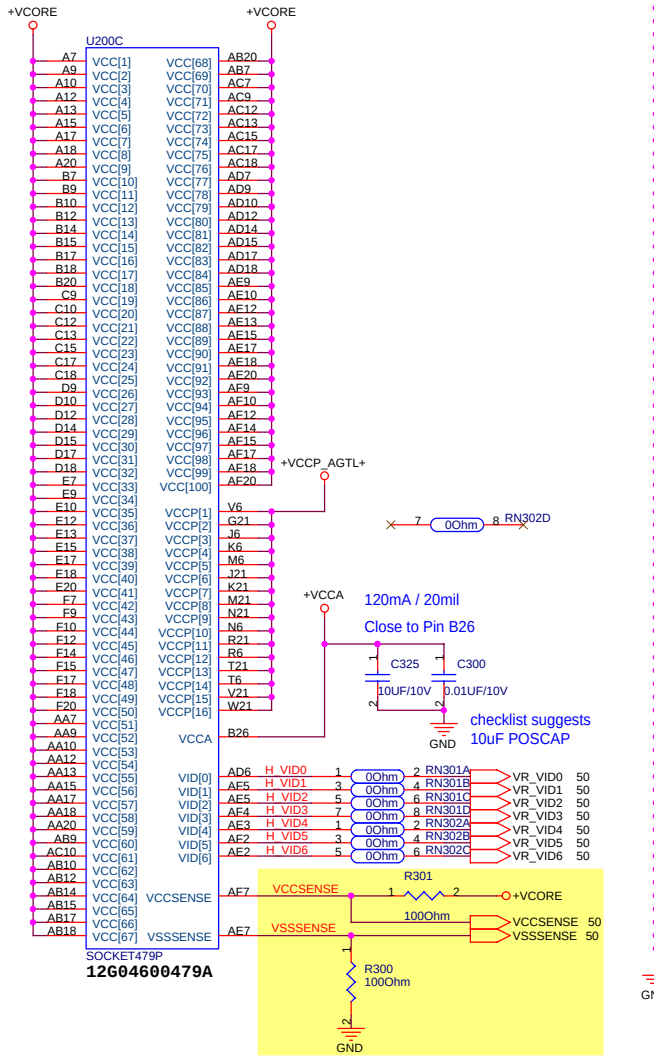
+VCCP_AGTL+ → JP200 SHORT_PIN → +VCCP
2.5A
+VCCP 6,9,20,52
+VCCP_AGTL+ 3,5,6,9

1205
28 H_PROCHOT_S# → R215 56Ohm → +VCCP_AGTL+
H_PWRGD → R216 56Ohm / → +VCCP_AGTL+

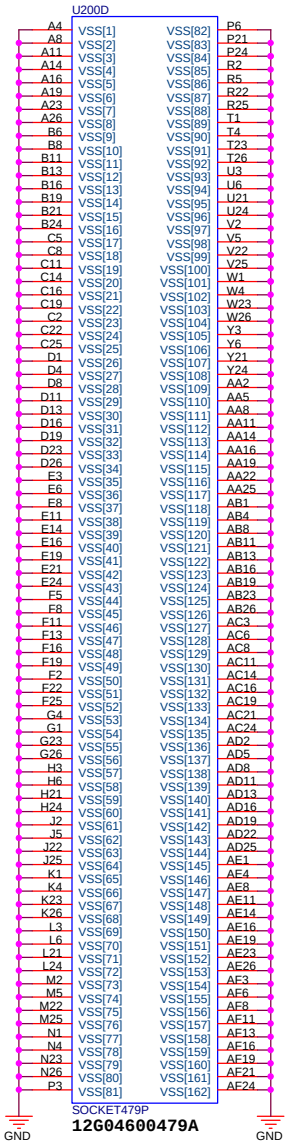
ASUSTeK COMPUTER INC	Title : YONAH CPU (1)			
	Engineer: Ping-Yen Tsai			
Size: Custom	Project Name: A3F			Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 2 of 63			

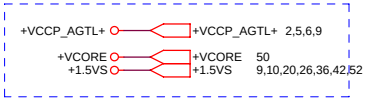
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

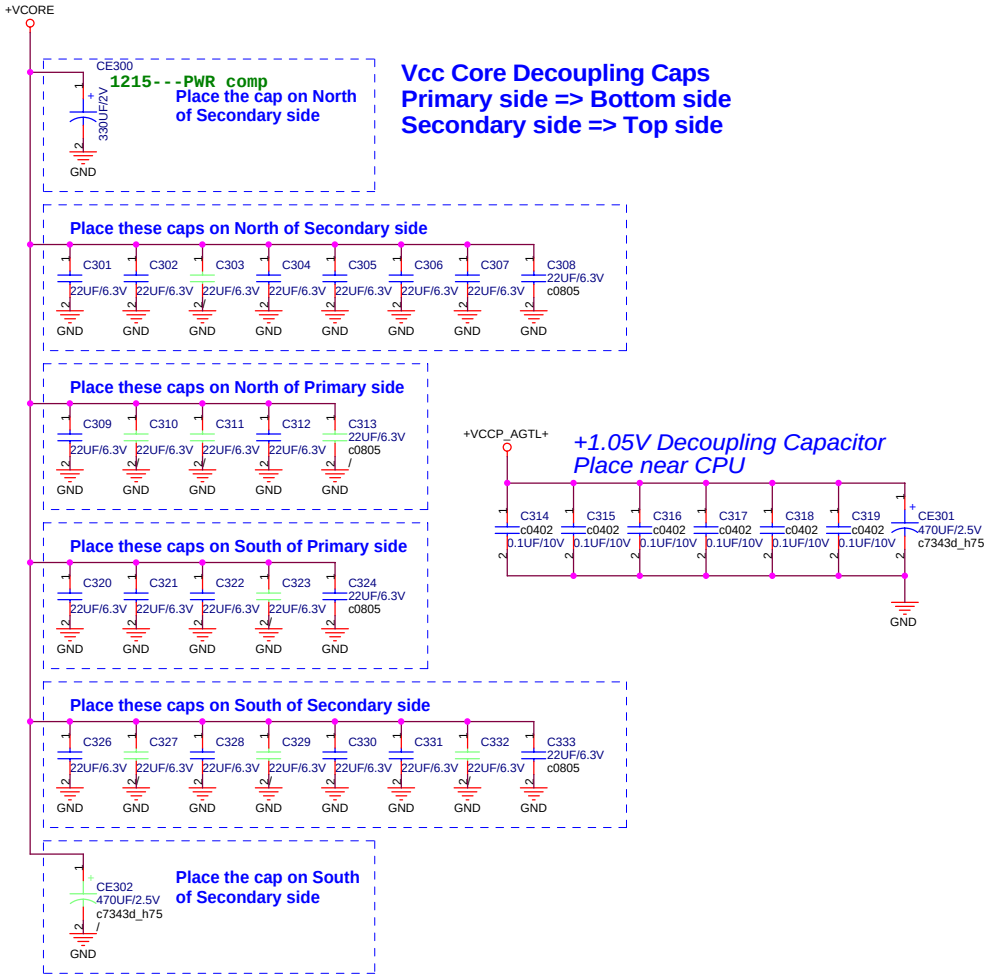
YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.







Title : Yonah CPU (2)

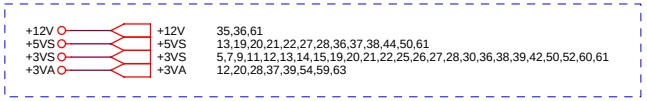
ASUSTeK COMPUTER INC

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 3 of 63

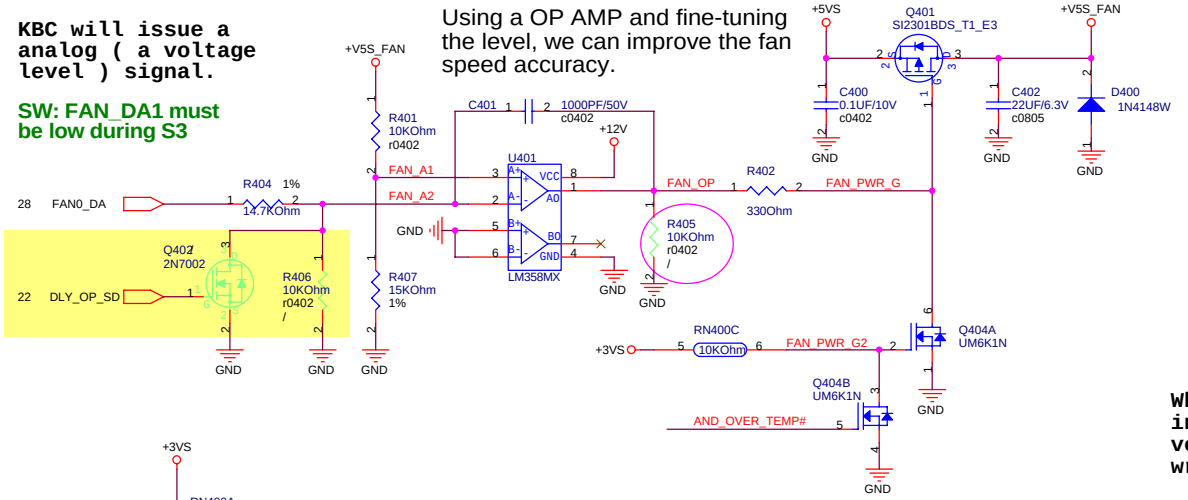
Fan Speed Control

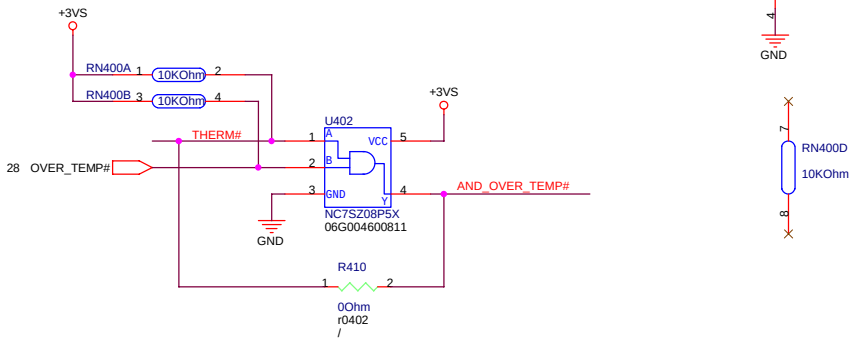


KBC will issue a analog (a voltage level) signal.

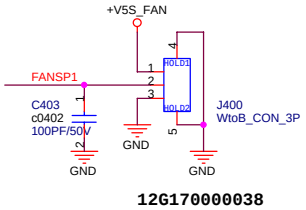
SW: FAN_DA1 must be low during S3

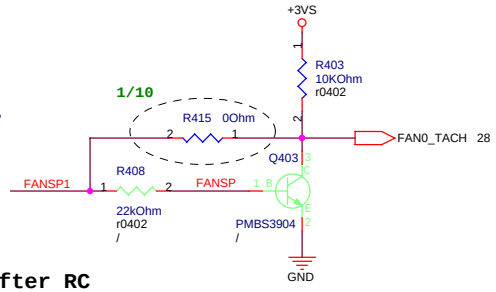
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



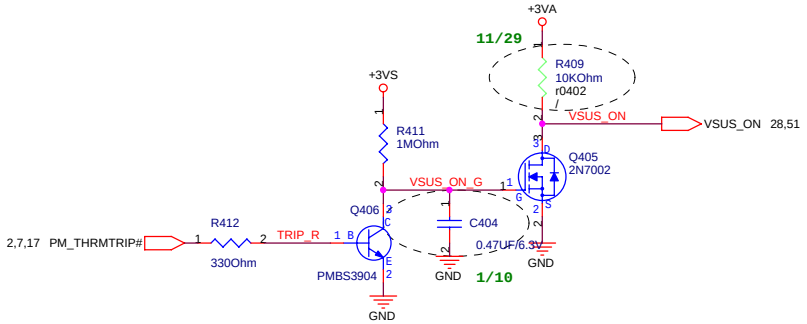


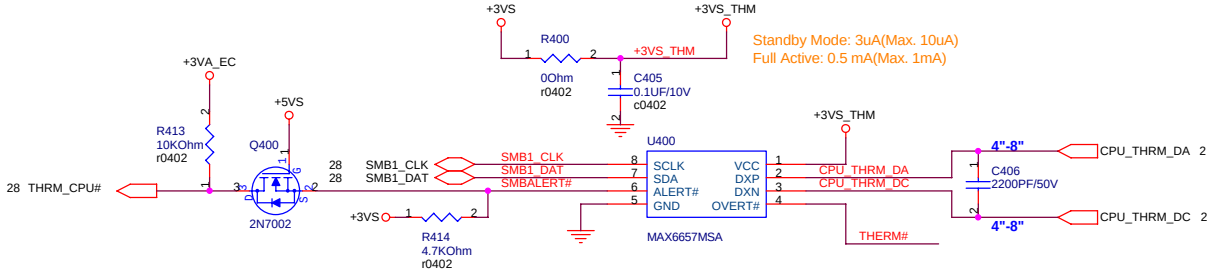
CPU FAN





When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSTeK COMPUTER INC		Title : THER-SENSOR,FAN	
		Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**		Rev: 2.0
Date: Wednesday, January 18, 2006		Sheet 4 of 63	

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

		FSLC	FSLB	FSLA
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ — +VCCP_AGTL+ 2,3,6,9

+3VS — +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

U500 ICS954310BGLFT

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519,Remove R550 R534

Internal Pull-Up Resistor

Internal Pull-Down Resistor

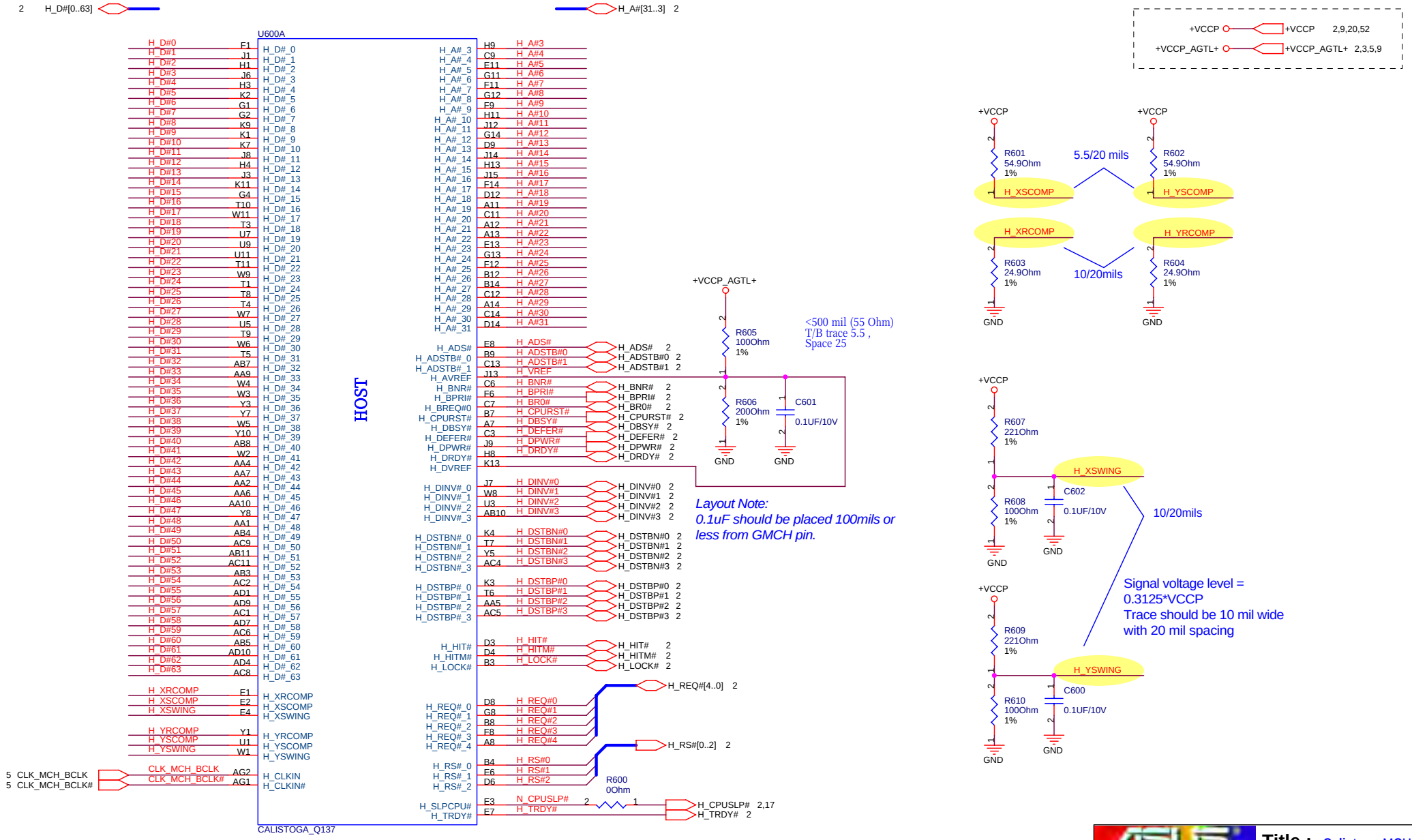
ASUSTeK COMPUTER INC

Title : CLOCK GEN

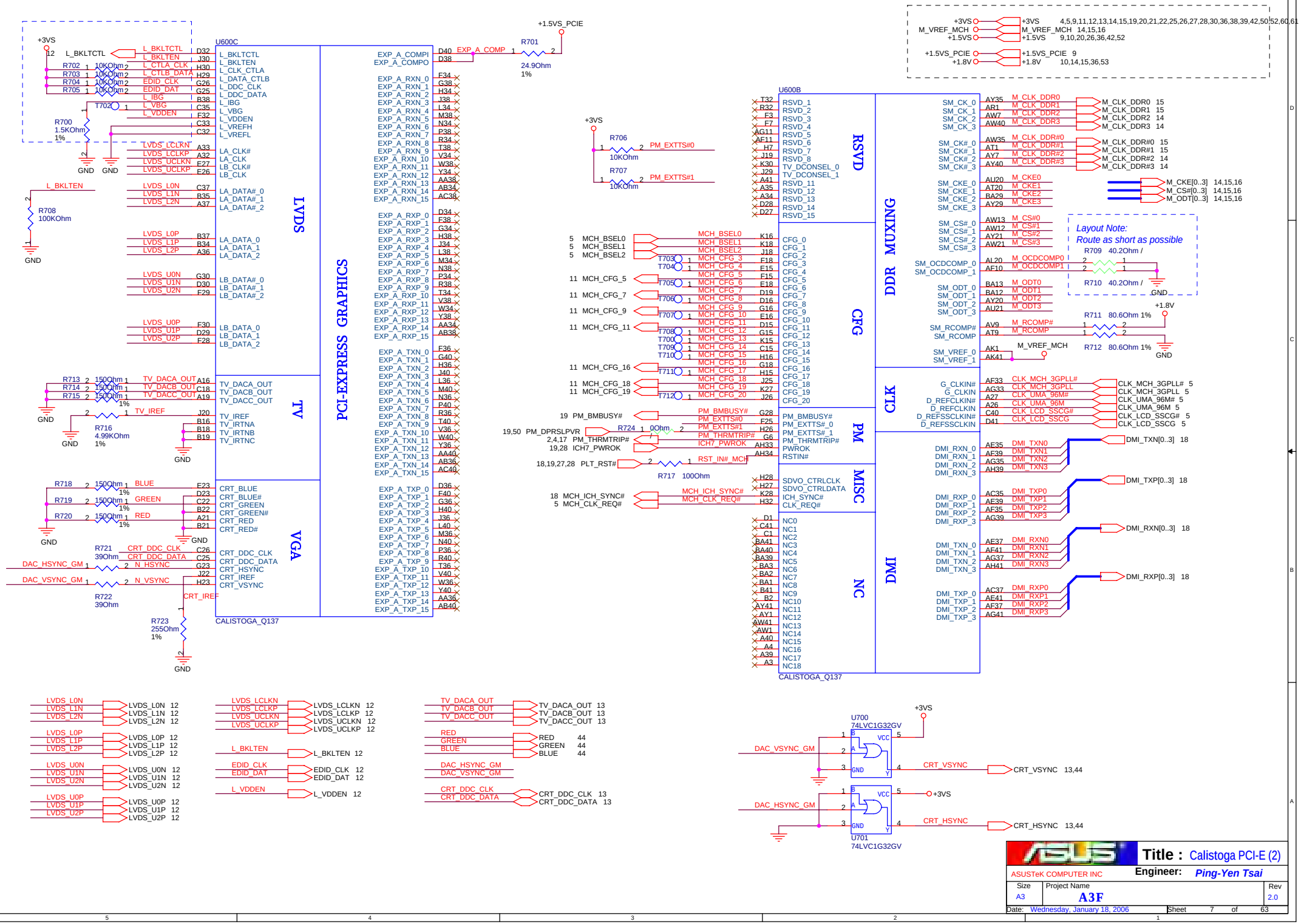
Engineer: Ping-Yen Tsai

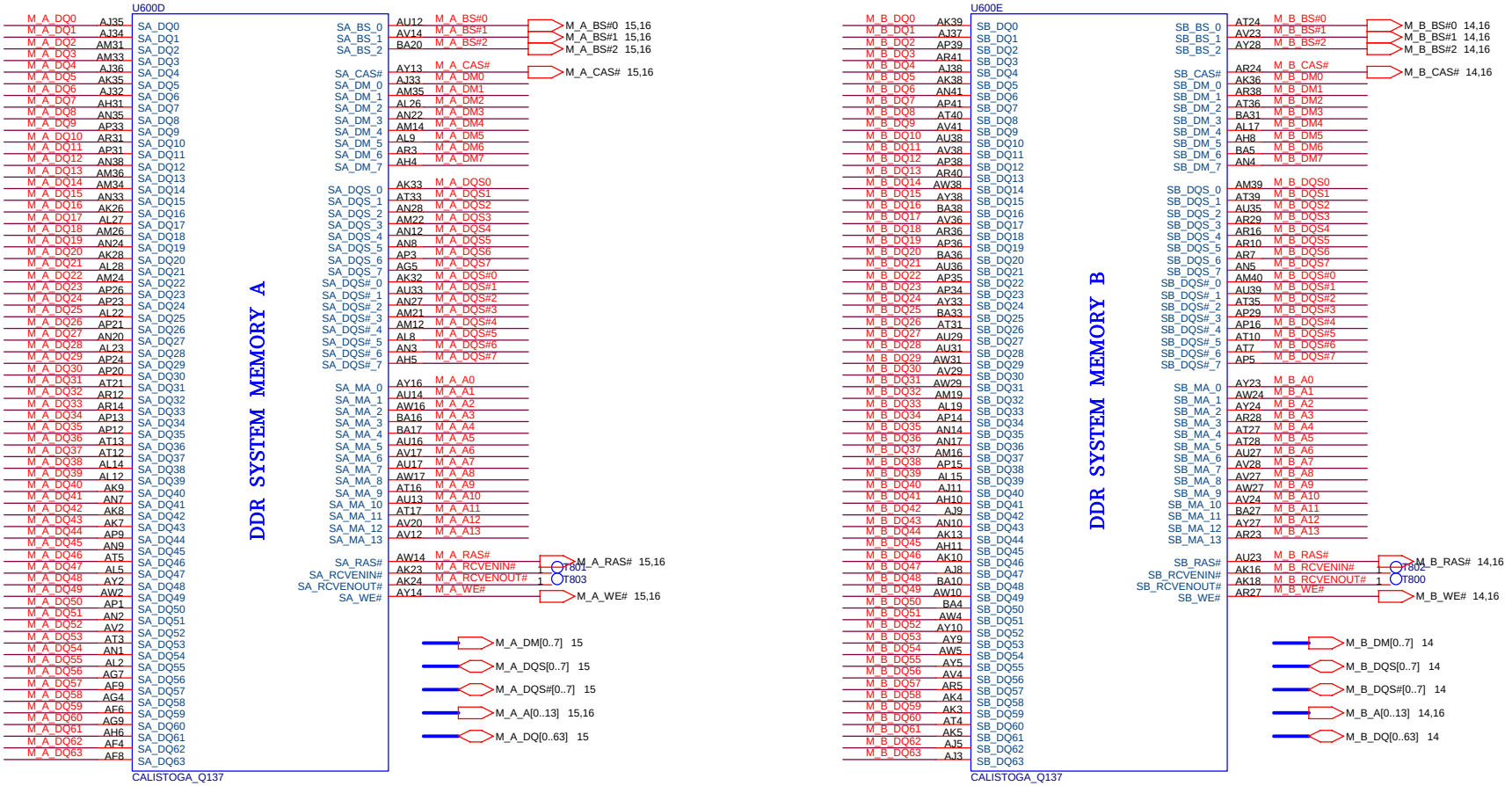
Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 5 of 63



ASUSTeK COMPUTER INC	Title : Calistoga MCH (1)		
	Engineer: Ping-Yen Tsai		
Size: B	Project Name: A3F		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 6 of 63		


U600C
CALISTOGA_Q137
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
U600B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
+3VS
+1.5VS_PCIE
M_VREF_MCH
+1.8V
R700 1.5KOhm 1%
R701 24.9Ohm 1%
R702 10KOhm
R703 10KOhm
R704 10KOhm
R705 10KOhm
R706 10KOhm
R707 10KOhm
R708 100KOhm
R709 40.2Ohm /
R710 40.2Ohm /
R711 80.6Ohm 1%
R712 80.6Ohm 1%
R713 150Ohm 1%
R714 150Ohm 1%
R715 150Ohm 1%
R716 4.99KOhm 1%
R717 100Ohm
R718 150Ohm 1%
R719 150Ohm 1%
R720 150Ohm 1%
R721 39Ohm
R722 39Ohm
R723 255Ohm 1%
R724 0Ohm /
Layout Note:
Route as short as possible
U700 74LVC1G32GV
U701 74LVC1G32GV
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Title : Calistoga PCI-E (2)
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 7 of 63



ASUSTeK COMPUTER INC

Title : Calistoga DDR2 (3)

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 8 of 63

Layout Note:
Place filter components close to GMCH

Layout Note:
Caps should be on Top layer

+1.5VS_PCIE
VCC3G
+1.5VS_3GPLL
1500 mA

L901 120Ohm/100Mhz — CE900 150UF/4V / C901 10UF/10V C902 10UF/10V — GND GND GND
L902 30Ohm/100Mhz — C903 0.1UF/10V C904 10UF/10V — GND GND
VCCA_3GPLL
+1.5VS_VCCAUX
L900 80Ohm/100Mhz — CE902 470UF/2.5V C908 0.1UF/10V — GND GND
VCCAUX 1900 mA
+1.5VS_DPLLA
L903 30Ohm/100Mhz — CE903 / C911 470UF/2.5V 0.1UF/10V — GND GND
VCCA_DPLLA 50 mA
+1.5VS_DPLLB
L905 30Ohm/100Mhz — CE904 / C917 470UF/2.5V 0.1UF/10V — GND GND
VCCA_DPLLB 50 mA
+1.5VS_HPLL
L906 120Ohm/100Mhz — C922 22UF/6.3V C923 0.1UF/10V — GND GND
VCCA_HPLL 45 mA
+1.5VS_MPLL
L907 120Ohm/100Mhz — C926 22UF/6.3V C927 0.1UF/10V — GND GND
VCCA_MPLL 45 mA

Layout Note:
0.1uF caps in 1.5VS_xPLL need to be located as edge caps within 200 mils.

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge

GMCH VCORE

+VCCP — +1.05VS 3500 mA — +VCCP_GMCH
JP900 SHORT_PIN / JP901 SHORT_PIN /

+1.5VS
VCCD_LVDS 20 mA
Pin A28 B28 C28
C909 0.1UF/10V C910 10UF/10V — GND GND

+1.5VS
VCCD_TVDAC
Pin D21
C912 0.022UF/25V C913 0.1UF/10V — GND GND
24 mA
+1.5VS
VCCD_QTVDAC
H19 C28
C918 0.022UF/25V C919 0.1UF/10V — GND GND

Layout Note:
These Caps should be within 250 mils of edge of GMCH

+2.5VS
VCC_SYNC
Pin H22
C931 0.1UF/10V — GND

VCCA_LVDS
Pin A38 10 mA
C900 0.01UF/25V C932 0.1UF/10V — GND GND

VCCA_3GBG
Pin G41 2 mA
C933 0.1UF/10V — GND

VCCTX_LVDS 60 mA
Pin A30 B30 C30
C934 0.1UF/10V C935 4.7UF/10V — GND GND

R904 10Ohm — +VCCP_GMCH_R — D901 BAT54C — +VCCP_GMCH

70 mA
L908 120Ohm/100Mhz
VCCA_CRTDAC
Pin E21 F21
+2.5VS_CRTDAC
C944 0.022UF/25V C945 0.1UF/10V — GND GND

Layout Note:
These Caps should be within 250 mils of edge of GMCH

+3VS
VCC_HV 40 mA
Pin A23 B23 B25
C942 10UF/10V C943 0.1UF/10V — GND GND

U600H

	H22	VCCSYNC
+1.5VS_PCIE	C30	VCC_TXLVDS0
	B30	VCC_TXLVDS1
	A30	VCC_TXLVDS2
	AJ41	VCC3G0
	AB41	VCC3G1
	Y41	VCC3G2
	V41	VCC3G3
+1.5VS_3GPLL	R41	VCC3G4
+2.5VS	N41	VCC3G5
	L41	VCC3G6
	AC33	VCCA_3GPLL
+2.5VS_CRTDAC	G41	VCCA_3GBG
	H41	VSSA_3GBG
GND	F21	VCCA_CRTDAC0
	E21	VCCA_CRTDAC1
	G21	VSSA_CRTDAC
+1.5VS_DPLLA	B26	VCCA_DPLLA
+1.5VS_DPLLB	C39	VCCA_DPLLB
+1.5VS_HPLL	AE1	VCCA_HPLL
+2.5VS	A38	VCCA_LVDS
	B39	VSSA_LVDS
+1.5VS_MPLL	AE2	VCCA_MPLL
+3VS_TVBG	H20	VCCA_TVBG
	G20	VSSA_TVBG
+3VS_TVDACA	E19	VCCA_TVDACA0
	F19	VCCA_TVDACA1
+3VS_TVDACB	C20	VCCA_TVDACB0
	D20	VCCA_TVDACB1
+3VS_TVDACC	E20	VCCA_TVDACC0
	F20	VCCA_TVDACC1
+1.5VS	AH1	VCCD_HMPLL0
	AH2	VCCD_HMPLL1
+1.5VS	A28	VCCD_LVDS0
	B28	VCCD_LVDS1
	C28	VCCD_LVDS2
+1.5VS	D21	VCCD_TVDAC
+3VS	A23	VCC_HV0
	B23	VCC_HV1
	B25	VCC_HV2
+1.5VS	H19	VCCD_QTVDAC
+1.5VS_VCCAUX	AK31	VCCAUX0
	AF31	VCCAUX1
	AE31	VCCAUX2
	AC31	VCCAUX3
	AL30	VCCAUX4
	AK30	VCCAUX5
	AJ30	VCCAUX6
	AH30	VCCAUX7
	AG30	VCCAUX8
	AF30	VCCAUX9
	AE30	VCCAUX10
	AD30	VCCAUX11
	AC30	VCCAUX12
	AG29	VCCAUX13
	AF29	VCCAUX14
	AE29	VCCAUX15
	AD29	VCCAUX16
	AC29	VCCAUX17
	AG28	VCCAUX18
	AF28	VCCAUX19
	AE28	VCCAUX20
	AH22	VCCAUX21
	AJ21	VCCAUX22
	AH21	VCCAUX23
	AJ20	VCCAUX24
	AH20	VCCAUX25
	AH19	VCCAUX26
	P19	VCCAUX27
	P16	VCCAUX28
	AH15	VCCAUX29
	P15	VCCAUX30
	AH14	VCCAUX31
	AG14	VCCAUX32
	AF14	VCCAUX33
	AE14	VCCAUX34
	Y14	VCCAUX35
	AE13	VCCAUX36
	AF12	VCCAUX37
	AE12	VCCAUX38
	AD12	VCCAUX39
		VCCAUX40

CALISTOGA_Q137

POWER

+VCCP_AGTL+

VTT_0	AC14
VTT_1	AB14
VTT_2	W14
VTT_3	V14
VTT_4	T14
VTT_5	R14
VTT_6	P14
VTT_7	N14
VTT_8	M14
VTT_9	L14
VTT_10	AD13
VTT_11	AC13
VTT_12	AB13
VTT_13	AA13
VTT_14	Y13
VTT_15	W13
VTT_16	V13
VTT_17	U13
VTT_18	T13
VTT_19	R13
VTT_20	N13
VTT_21	M13
VTT_22	L13
VTT_23	AB12
VTT_24	AA12
VTT_25	Y12
VTT_26	W12
VTT_27	V12
VTT_28	U12
VTT_29	T12
VTT_30	R12
VTT_31	P12
VTT_32	N12
VTT_33	M12
VTT_34	L12
VTT_35	R11
VTT_36	P11
VTT_37	N11
VTT_38	M11
VTT_39	R10
VTT_40	P10
VTT_41	N10
VTT_42	M10
VTT_43	P9
VTT_44	N9
VTT_45	M9
VTT_46	R8
VTT_47	P8
VTT_48	N8
VTT_49	M8
VTT_50	P7
VTT_51	N7
VTT_52	M7
VTT_53	R6
VTT_54	P6
VTT_55	M6
VTT_56	A6
VTT_57	R5
VTT_58	P5
VTT_59	N5
VTT_60	M5
VTT_61	P4
VTT_62	N4
VTT_63	M4
VTT_64	R3
VTT_65	P3
VTT_66	N3
VTT_67	M3
VTT_68	R2
VTT_69	P2
VTT_70	M2
VTT_71	D2
VTT_72	AB1
VTT_73	R1
VTT_74	P1
VTT_75	N1
VTT_76	M1

VTTLF_CAP3 — C928 0.47UF/16V — GND
VTTLF_CAP2 — C936 0.47UF/16V — GND
VTTLF_CAP1 — C937 0.22UF/6.3V — GND

Layout Note:
These Caps used in +3VS_TVDACx should be within 250 mils of edge of GMCH

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS
+2.5VS should be placed within 200 mils of edge.

+VCCP_AGTL+ — +VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH — +VCCP_GMCH 10,42
+1.5VS_PCIE — +1.5VS_PCIE 7
+3VS — +3VS 4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
+2.5VS — +2.5VS 13,36,54
+1.5VS — +1.5VS 10,20,26,36,42,52

+VCCP_AGTL+
800 mA
C905 4.7UF/10V C906 2.2UF/6.3V — C907 0.22UF/6.3V CE901 330UF/2V 11G08D233722 — GND

Layout Note:
Place on the edge

Layout Note:
Place in cavity

+3VS +3VS_DAC — R900 0Ohm / — R901 10Ohm — +1.5VS_DAC — D900 BAT54C — +1.5VS
L904 180Ohm/100Mhz — C914 10UF/10V — GND

Total Power Consumption 120 mA

+3VS_TVBG — C915 0.022UF/25V C916 0.1UF/10V — VCCA_TVBG Pin H20
+3VS_TVDACA — C920 0.022UF/25V C921 0.1UF/10V — VCCA_TVDACA Pin E19 F19
+3VS_TVDACB — C924 0.022UF/25V C925 0.1UF/10V — VCCA_TVDACB Pin C20 D20
+3VS_TVDACC — C929 0.022UF/25V C930 0.1UF/10V — VCCA_TVDACC Pin E20 F20
GND

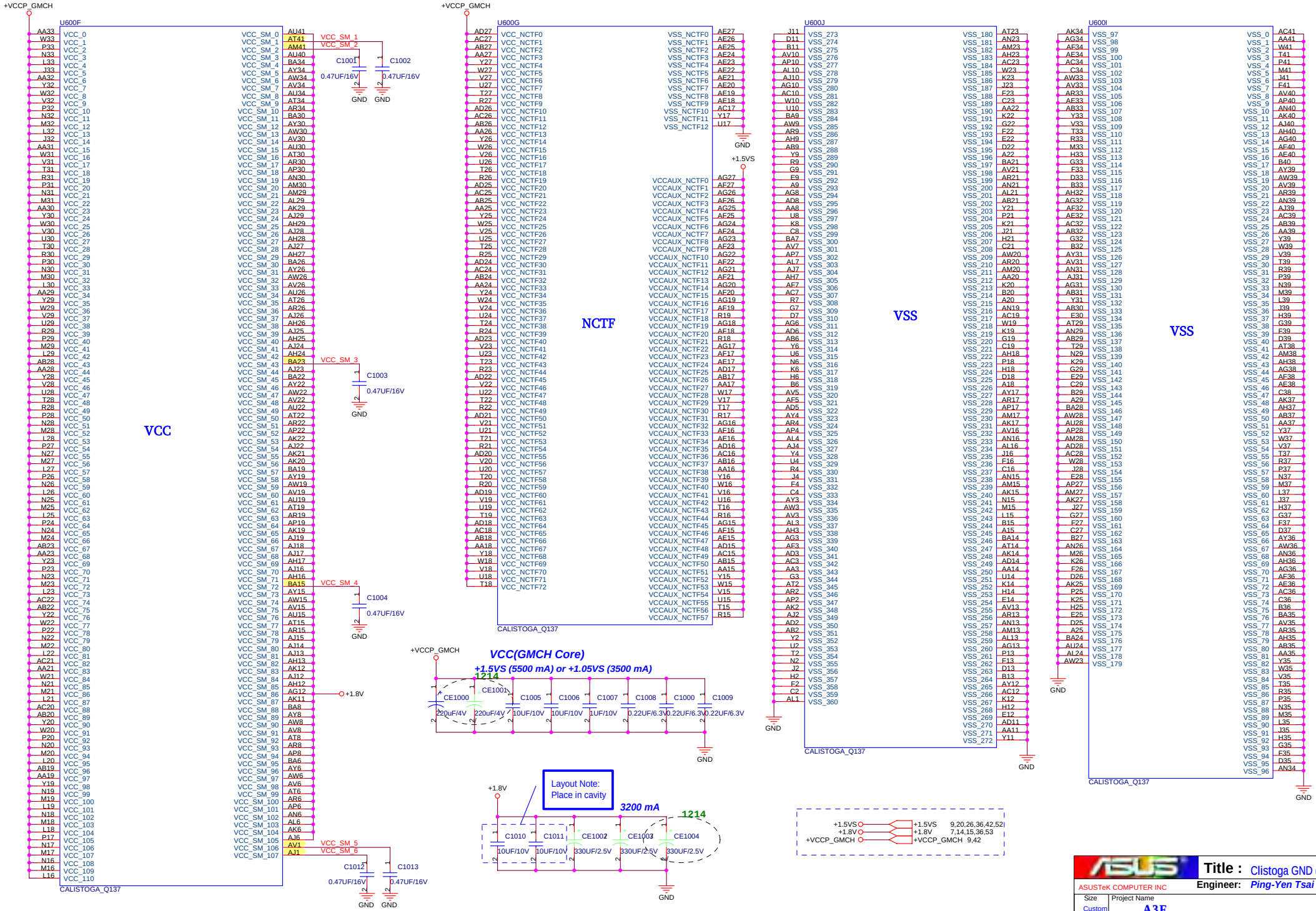
+3VS — +5V — R902 10KOhm — 3VS_DAC_EN — C938 0.1UF/50V — C939 4.7UF/16V — GND
12/1
U900 SI9183DT: VIN, GND, SD#, VOUT, FB
3VS_DAC_ADJ — R903 35.7KOhm — +3VS_DAC — C941 4.7UF/16V — GND
C940 0.1UF/50V — R905 20KOhm — GND

ASUSTeK COMPUTER INC
Engineer: *Ping-Yen Tsai*

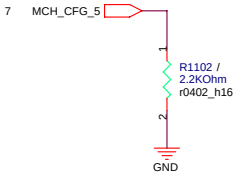
Title : Calistoga Power (4)

Size	Project Name	Rev
A3	A3F	2.0

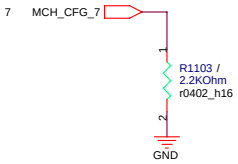
Date: Wednesday, January 18, 2006 Sheet 9 of 63



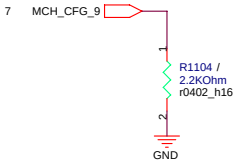
Title :	Clistoga GND (5)
ASUSTeK COMPUTER INC	Engineer: Ping-Yen Tsai
Size: Custom	Project Name: A3F
Rev: 2.0	
Date: Wednesday, January 18, 2006	Sheet 10 of 63



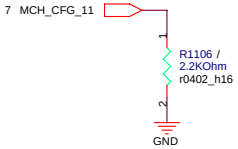
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



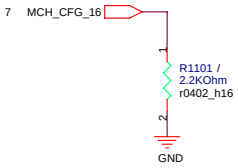
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



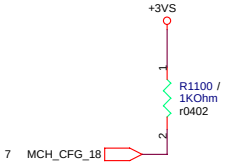
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



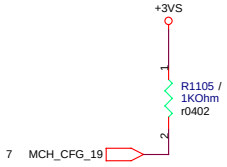
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



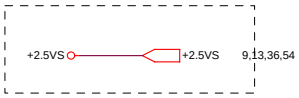
CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

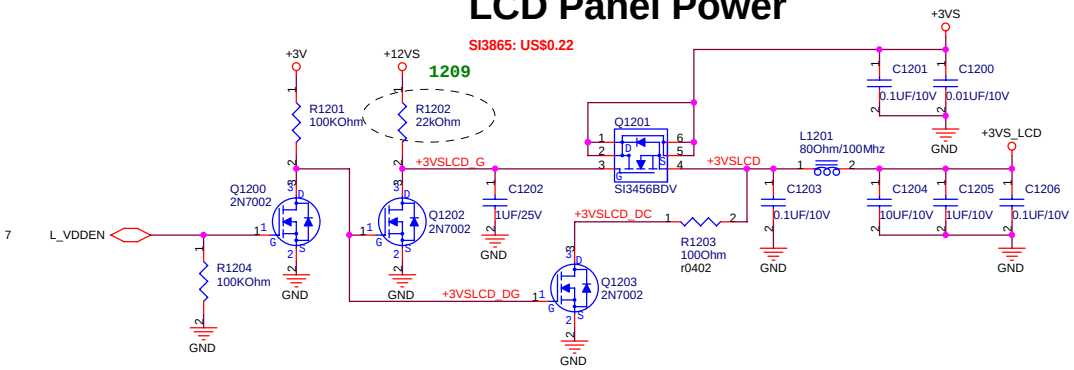
CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



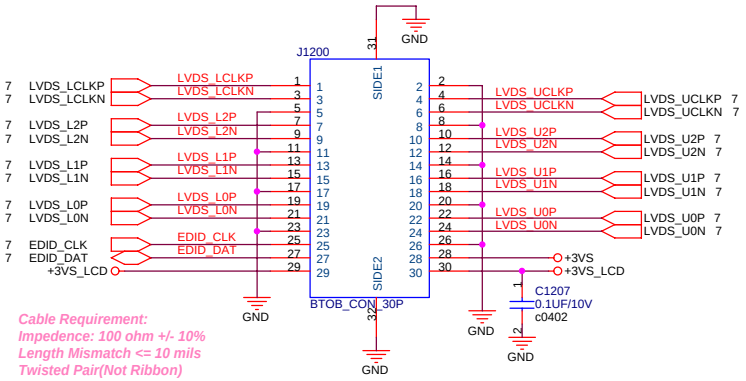
ASUSTeK COMPUTER INC
Title : Calistoga Strapping
Engineer: *Ping-Yen Tsai*
Size: Custom | Project Name: A3F | Rev: 2.0
Date: Wednesday, January 18, 2006 | Sheet 11 of 63

LCD Panel Power

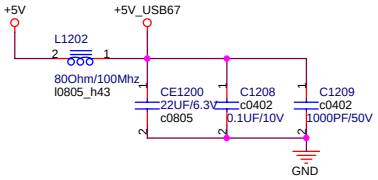
3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

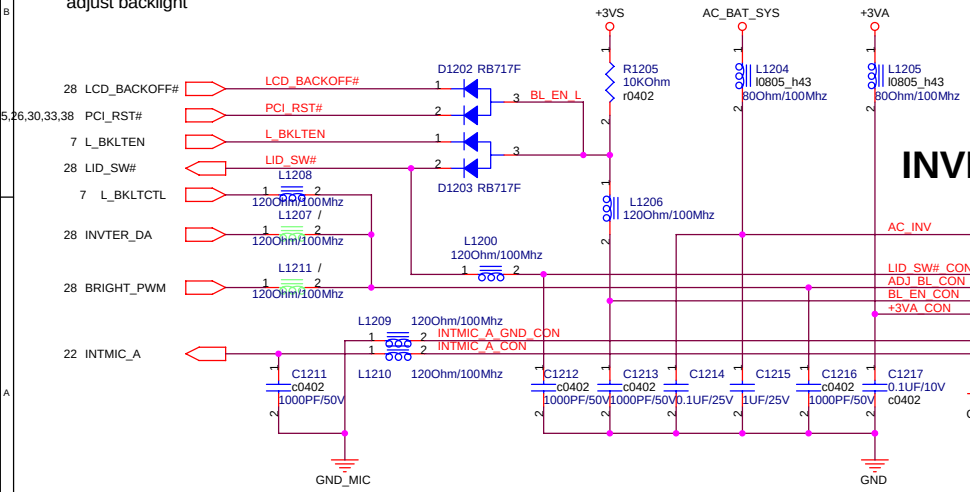


LCD Backlight Control

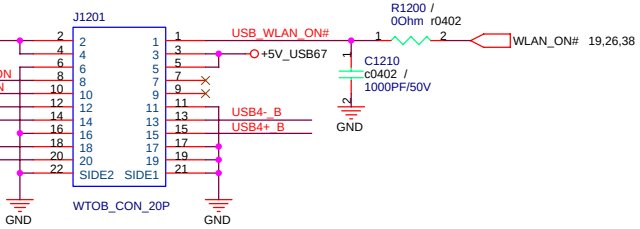
BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 14.1W LCD Panel

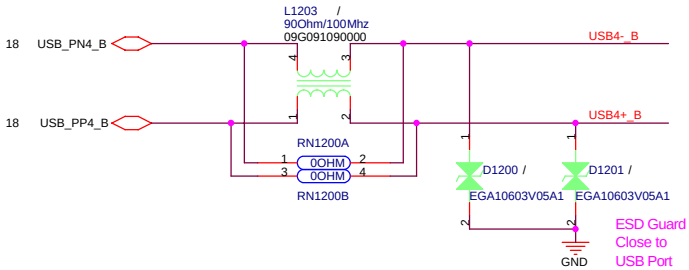


INVERTER Interface



700V rms@5 mA rms
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

USB4 For CMOS Camera



ESD Guard Close to USB Port

ASUSTeK COMPUTER INC

Title : LVDS & INVERTER

Engineer: *Ping-Yen Tsai*

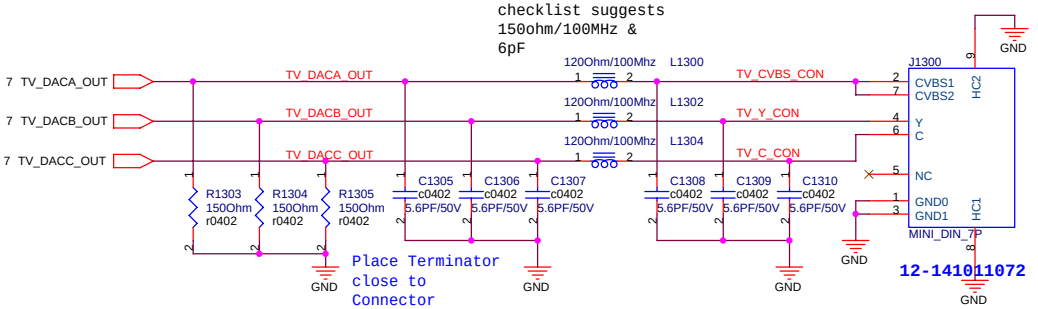
Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 12 of 63

TV OUT

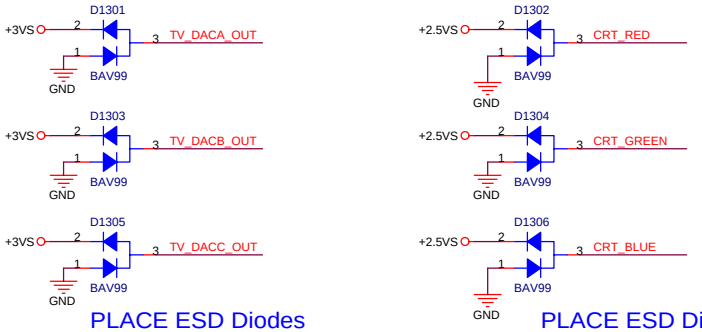
12G14101107D

checklist suggests
150ohm/100MHz &
6pF



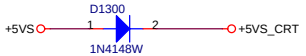
Place Terminator close to Connector

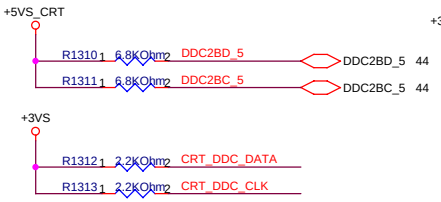
12-141011072

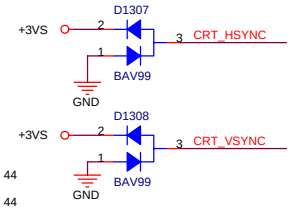


PLACE ESD Diodes near TV port

PLACE ESD Diodes near VGA port

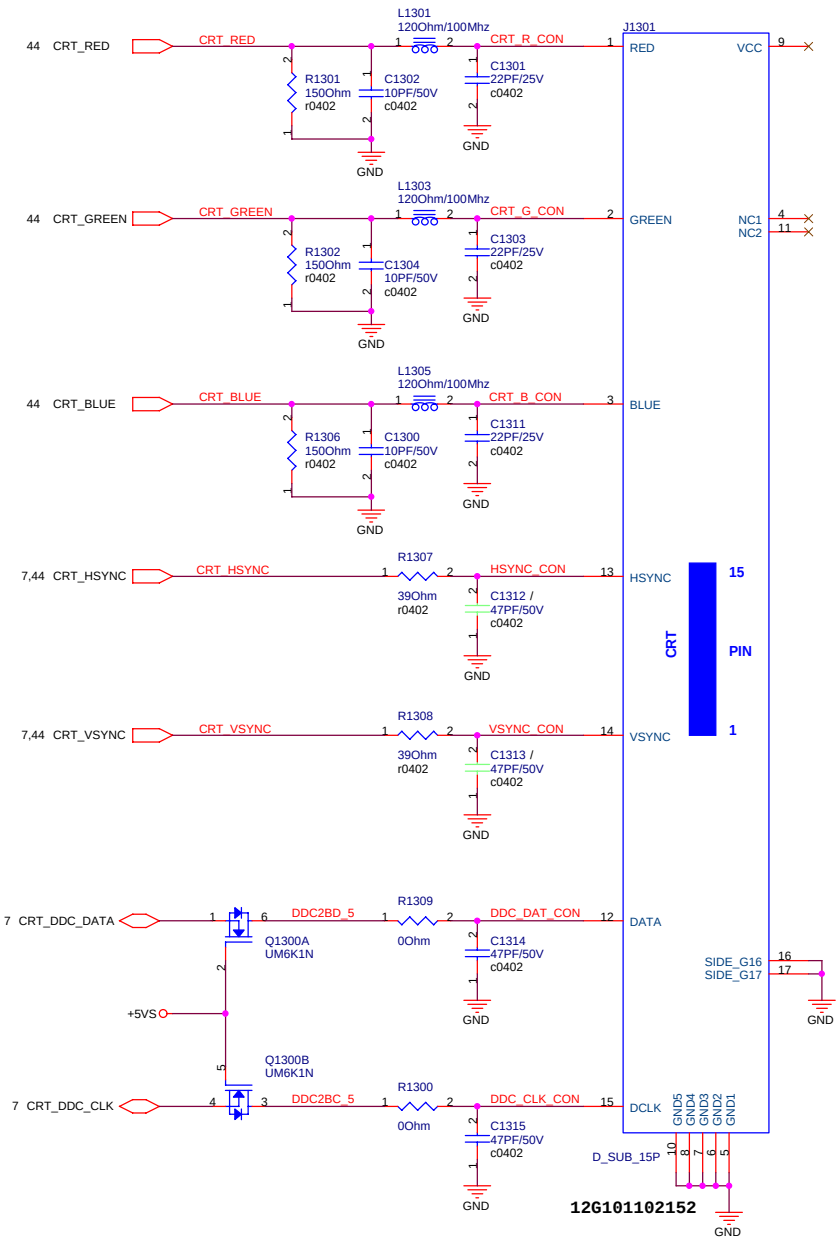






CRT OUT

checklist suggests 47ohm/100MHz



12G101102152

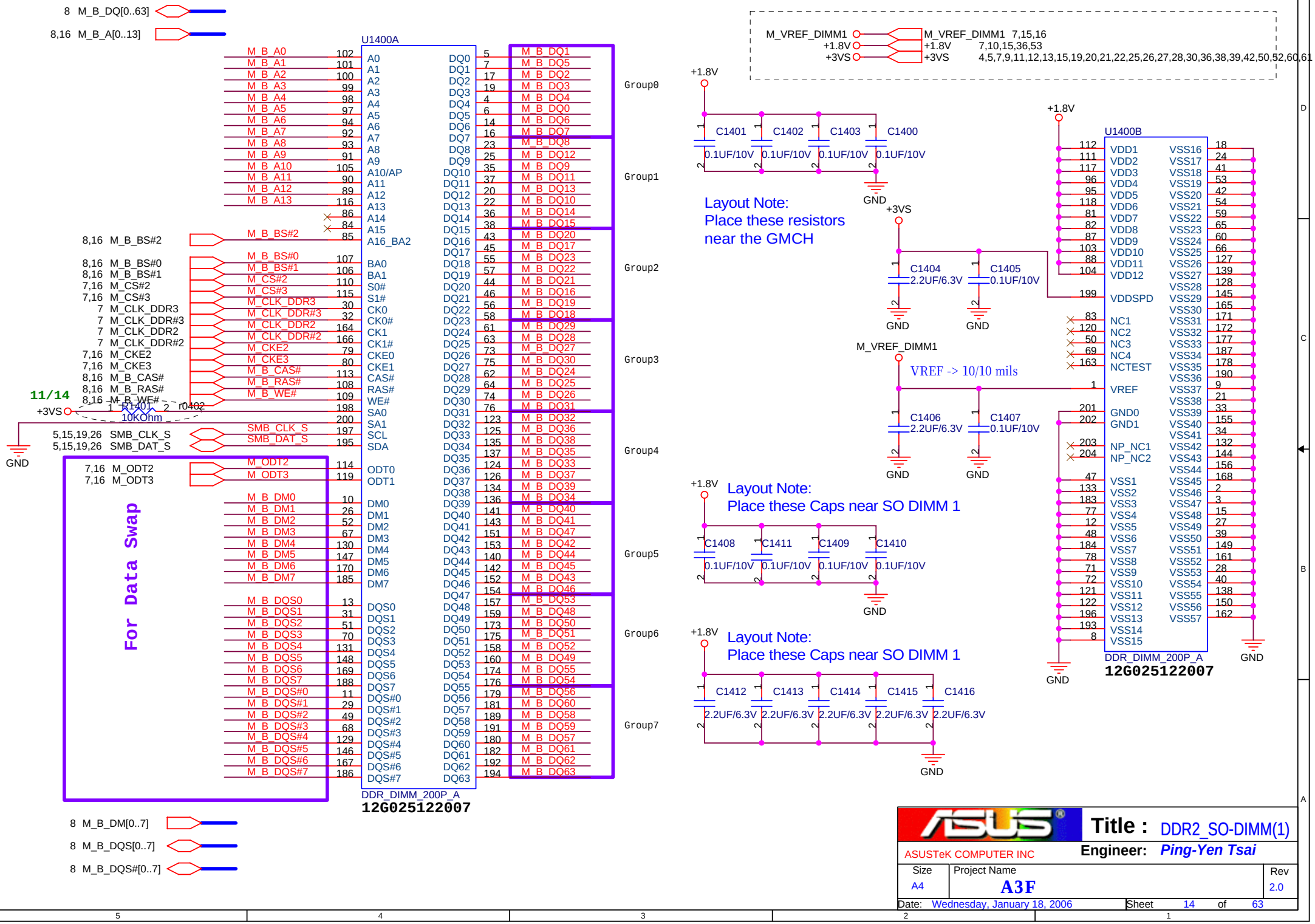
ASUSTeK COMPUTER INC

Title : CRT & TV OUT

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 13 of 63


8 M_B_DQ[0..63]
8,16 M_B_A[0..13]
U1400A
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2
M_B_BS#2
8,16 M_B_BS#2
M_B_BS#0 M_B_BS#1 M_CS#2 M_CS#3 M_CLK_DDR3 M_CLK_DDR#3 M_CLK_DDR2 M_CLK_DDR#2 M_CKE2 M_CKE3 M_CAS# M_RAS# M_WE#
BA0 BA1 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#
8,16 M_B_BS#0
8,16 M_B_BS#1
7,16 M_CS#2
7,16 M_CS#3
7 M_CLK_DDR3
7 M_CLK_DDR#3
7 M_CLK_DDR2
7 M_CLK_DDR#2
7,16 M_CKE2
7,16 M_CKE3
8,16 M_B_CAS#
8,16 M_B_RAS#
8,16 M_B_WE#
11/14
+3VS
R1401 10KOhm r0402
GND
SMB_CLK_S SMB_DAT_S
SA0 SA1 SCL SDA
5,15,19,26 SMB_CLK_S
5,15,19,26 SMB_DAT_S
M_ODT2 M_ODT3
ODT0 ODT1
7,16 M_ODT2
7,16 M_ODT3
For Data Swap
M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7 M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
M_B_DQ1 M_B_DQ5 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ0 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ12 M_B_DQ9 M_B_DQ11 M_B_DQ13 M_B_DQ10 M_B_DQ14 M_B_DQ15 M_B_DQ20 M_B_DQ17 M_B_DQ23 M_B_DQ22 M_B_DQ21 M_B_DQ16 M_B_DQ19 M_B_DQ18 M_B_DQ29 M_B_DQ28 M_B_DQ27 M_B_DQ30 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ31 M_B_DQ32 M_B_DQ36 M_B_DQ38 M_B_DQ35 M_B_DQ33 M_B_DQ37 M_B_DQ39 M_B_DQ34 M_B_DQ40 M_B_DQ41 M_B_DQ47 M_B_DQ42 M_B_DQ44 M_B_DQ45 M_B_DQ43 M_B_DQ46 M_B_DQ53 M_B_DQ48 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ49 M_B_DQ55 M_B_DQ54 M_B_DQ56 M_B_DQ60 M_B_DQ58 M_B_DQ59 M_B_DQ57 M_B_DQ61 M_B_DQ62 M_B_DQ63
Group0 Group1 Group2 Group3 Group4 Group5 Group6 Group7
DDR_DIMM_200P_A
12G025122007
8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]
M_VREF_DIMM1
+1.8V
+3VS
M_VREF_DIMM1 7,15,16
+1.8V 7,10,15,36,53
+3VS 4,5,7,9,11,12,13,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
Layout Note:
Place these resistors
near the GMCH
C1401 C1402 C1403 C1400
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V
C1404 2.2UF/6.3V
C1405 0.1UF/10V
C1406 2.2UF/6.3V
C1407 0.1UF/10V
VREF -> 10/10 mils
Layout Note:
Place these Caps near SO DIMM 1
C1408 C1411 C1409 C1410
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V
Layout Note:
Place these Caps near SO DIMM 1
C1412 C1413 C1414 C1415 C1416
2.2UF/6.3V 2.2UF/6.3V 2.2UF/6.3V 2.2UF/6.3V 2.2UF/6.3V
U1400B
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDDSPD
NC1 NC2 NC3 NC4 NCTEST VREF
GND0 GND1
NP_NC1 NP_NC2
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15
VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57
DDR_DIMM_200P_A
12G025122007
Title : DDR2_SO-DIMM(1)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A4
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 14 of 63

Green Part Number:12G025122006
Green Part Number:12-025122006

8 M_A_DQ[0..63]
8,16 M_A_A[0..13]

J1500A

M_A_A0	102	A0	DQ0	5	M_A_DQ5		
M_A_A1	101	A1	DQ1	7	M_A_DQ4		
M_A_A2	100	A2	DQ2	17	M_A_DQ2		
M_A_A3	99	A3	DQ3	19	M_A_DQ3		
M_A_A4	98	A4	DQ4	4	M_A_DQ1		
M_A_A5	97	A5	DQ5	6	M_A_DQ0		
M_A_A6	94	A6	DQ6	14	M_A_DQ6		
M_A_A7	92	A7	DQ7	16	M_A_DQ7		
M_A_A8	93	A8	DQ8	23	M_A_DQ13		
M_A_A9	91	A9	DQ9	25	M_A_DQ8		
M_A_A10	105	A10/AP	DQ10	35	M_A_DQ10		
M_A_A11	90	A11	DQ11	37	M_A_DQ11	Group1	
M_A_A12	89	A12	DQ12	20	M_A_DQ12		
M_A_A13	116	A13	DQ13	22	M_A_DQ14		
	86	A14	DQ14	36	M_A_DQ15		
	84	A15	DQ15	38	M_A_DQ9		
M_A_BS#2	85	A16_BA2	DQ16	43	M_A_DQ16		
			DQ17	45	M_A_DQ21		
M_A_BS#0	107	BA0	DQ18	55	M_A_DQ23		
M_A_BS#1	106	BA1	DQ19	57	M_A_DQ19		
M_CS#0	110	S0#	DQ20	44	M_A_DQ20	Group2	
M_CS#1	115	S1#	DQ21	46	M_A_DQ17		
M_CLK_DDR0	30	CK0	DQ22	56	M_A_DQ18		
M_CLK_DDR#0	32	CK0#	DQ23	58	M_A_DQ22		
M_CLK_DDR1	164	CK1	DQ24	61	M_A_DQ24		
M_CLK_DDR#1	166	CK1#	DQ25	63	M_A_DQ25		
M_CKE0	79	CKE0	DQ26	73	M_A_DQ26		
M_CKE1	80	CKE1	DQ27	75	M_A_DQ27	Group3	
M_A_CAS#	113	CAS#	DQ28	62	M_A_DQ28		
M_A_RAS#	108	RAS#	DQ29	64	M_A_DQ29		
M_A_WE#	109	WE#	DQ30	74	M_A_DQ30		
	198	SA0	DQ31	76	M_A_DQ31		
	200	SA1	DQ32	123	M_A_DQ36		
SMB_CLK_S	197	SCL	DQ33	125	M_A_DQ37		
SMB_DAT_S	195	SDA	DQ34	135	M_A_DQ35		
			DQ35	137	M_A_DQ34		
M_ODT0	114	ODT0	DQ36	124	M_A_DQ32	Group4	
M_ODT1	119	ODT1	DQ37	126	M_A_DQ33		
			DQ38	134	M_A_DQ39		
M_A_DM0	10	DM0	DQ39	136	M_A_DQ38		
M_A_DM1	26	DM1	DQ40	141	M_A_DQ45		
M_A_DM2	52	DM2	DQ41	143	M_A_DQ41		
M_A_DM3	67	DM3	DQ42	151	M_A_DQ47		
M_A_DM4	130	DM4	DQ43	153	M_A_DQ46		
M_A_DM5	147	DM5	DQ44	140	M_A_DQ44	Group5	
M_A_DM6	170	DM6	DQ45	142	M_A_DQ40		
M_A_DM7	185	DM7	DQ46	152	M_A_DQ43		
			DQ47	154	M_A_DQ42		
M_A_DQS0	13	DQS0	DQ48	157	M_A_DQ48		
M_A_DQS1	31	DQS1	DQ49	159	M_A_DQ49		
M_A_DQS2	51	DQS2	DQ50	173	M_A_DQ50		
M_A_DQS3	70	DQS3	DQ51	175	M_A_DQ51		
M_A_DQS4	131	DQS4	DQ52	158	M_A_DQ53	Group6	
M_A_DQS5	148	DQS5	DQ53	160	M_A_DQ52		
M_A_DQS6	169	DQS6	DQ54	174	M_A_DQ54		
M_A_DQS7	188	DQS7	DQ55	176	M_A_DQ55		
M_A_DQS#0	11	DQS#0	DQ56	179	M_A_DQ60		
M_A_DQS#1	29	DQS#1	DQ57	181	M_A_DQ56		
M_A_DQS#2	49	DQS#2	DQ58	189	M_A_DQ63		
M_A_DQS#3	68	DQS#3	DQ59	191	M_A_DQ59	Group7	
M_A_DQS#4	129	DQS#4	DQ60	180	M_A_DQ61		
M_A_DQS#5	146	DQS#5	DQ61	182	M_A_DQ57		
M_A_DQS#6	167	DQS#6	DQ62	192	M_A_DQ58		
M_A_DQS#7	186	DQS#7	DQ63	194	M_A_DQ62		

DDR2_DIMM_200P_REV

For Data Swap

GND

8,16 M_A_BS#2
8,16 M_A_BS#0
8,16 M_A_BS#1
7,16 M_CS#0
7,16 M_CS#1
7 M_CLK_DDR0
7 M_CLK_DDR#0
7 M_CLK_DDR1
7 M_CLK_DDR#1
7,16 M_CKE0
7,16 M_CKE1
8,16 M_A_CAS#
8,16 M_A_RAS#
8,16 M_A_WE#
5,14,19,26 SMB_CLK_S
5,14,19,26 SMB_DAT_S
7,16 M_ODT0
7,16 M_ODT1

8 M_A_DM[0..7]
8 M_A_DQS[0..7]
8 M_A_DQS#[0..7]

GMCH=====>SODIMM1=>SODIMM0

+1.8V → +1.8V 7,10,14,36,53
+3VS → +3VS 4,5,7,9,11,12,13,14,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
M_VREF_DIMM0 → M_VREF_DIMM0 7,14,16

J1500B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR2_DIMM_200P_REV

+1.8V
+3VS
C1501 2.2UF/6.3V
C1502 0.1UF/10V
GND
M_VREF_DIMM0
VREF -> 10/10 mils
C1503 2.2UF/6.3V
C1504 0.1UF/10V

+1.8V
Layout Note:
Place these Caps near SO DIMM 0
C1500 0.1UF/10V
C1505 0.1UF/10V
C1506 0.1UF/10V
C1507 0.1UF/10V
GND

+1.8V
Layout Note:
Place these Caps near SO DIMM 0
C1508 2.2UF/6.3V
C1509 2.2UF/6.3V
C1510 2.2UF/6.3V
C1511 2.2UF/6.3V
C1512 2.2UF/6.3V
GND

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM(0)	
	Engineer: Ping-Yen Tsai	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 15 of 63	

+0.9VS

NEED TO SWAP

1	56Ohm	16	RN1601A	M_CKE2
2	56Ohm	15	RN1601B	M_B_BS#2
3	56Ohm	14	RN1601C	M_B_A12
4	56Ohm	13	RN1601D	M_B_A9
5	56Ohm	12	RN1601E	M_CKE3
6	56Ohm	11	RN1601F	M_B_A8
7	56Ohm	10	RN1601G	M_B_A7
8	56Ohm	9	RN1601H	M_B_A11
1	56Ohm	16	RN1602A	M_B_A5
2	56Ohm	15	RN1602B	M_B_A3
3	56Ohm	14	RN1602C	M_B_A6
4	56Ohm	13	RN1602D	M_B_A4
5	56Ohm	12	RN1602E	M_B_A1
6	56Ohm	11	RN1602F	M_B_A2
7	56Ohm	10	RN1602G	M_B_A0
8	56Ohm	9	RN1602H	M_B_BS#1
1	56Ohm	16	RN1603A	M_B_RAS#
2	56Ohm	15	RN1603B	M_B_A10
3	56Ohm	14	RN1603C	M_ODT2
4	56Ohm	13	RN1603D	M_B_A13
5	56Ohm	12	RN1603E	M_CS#2
6	56Ohm	11	RN1603F	M_B_CAS#
7	56Ohm	10	RN1603G	M_B_BS#0
8	56Ohm	9	RN1603H	M_B_WE#
1	56Ohm	2	RN1604A	
3	56Ohm	4	RN1604B	
5	56Ohm	6	RN1604C	M_CS#3
7	56Ohm	8	RN1604D	M_ODT3
1	56Ohm	16	RN1605A	M_A_A4
2	56Ohm	15	RN1605B	M_A_A11
3	56Ohm	14	RN1605C	M_A_A7
4	56Ohm	13	RN1605D	M_A_A9
5	56Ohm	12	RN1605E	M_A_A12
6	56Ohm	11	RN1605F	M_A_BS#2
7	56Ohm	10	RN1605G	M_CKE1
8	56Ohm	9	RN1605H	M_CKE0
1	56Ohm	16	RN1606A	
2	56Ohm	15	RN1606B	
3	56Ohm	14	RN1606C	M_A_BS#0
4	56Ohm	13	RN1606D	M_A_A10
5	56Ohm	12	RN1606E	M_A_A0
6	56Ohm	11	RN1606F	M_A_A6
7	56Ohm	10	RN1606G	M_A_A5
8	56Ohm	9	RN1606H	M_A_A8
1	56Ohm	16	RN1607A	M_A_A13
2	56Ohm	15	RN1607B	M_A_RAS#
3	56Ohm	14	RN1607C	M_A_BS#1
4	56Ohm	13	RN1607D	M_A_A2
5	56Ohm	12	RN1607E	M_A_CAS#
6	56Ohm	11	RN1607F	M_A_WE#
7	56Ohm	10	RN1607G	M_A_A3
8	56Ohm	9	RN1607H	M_A_A1
1	56Ohm	2	RN1608A	M_ODT0
3	56Ohm	4	RN1608B	M_CS#0
5	56Ohm	6	RN1608C	M_CS#1
7	56Ohm	8	RN1608D	M_ODT1

M_A_A[0..13] 8,15
M_A_BS#[0..2] 8,15
M_A_CAS# 8,15
M_A_RAS# 8,15
M_A_WE# 8,15

M_B_A[0..13] 8,14
M_B_BS#[0..2] 8,14
M_B_CAS# 8,14
M_B_RAS# 8,14
M_B_WE# 8,14

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

M_VREF_DIMM0 → M_VREF_DIMM0 7,14,15
M_VREF_DIMM1 → M_VREF_DIMM1 7,14,15
M_VREF_MCH → M_VREF_MCH 7,14,15
+0.9VS → +0.9VS 36,53

+0.9VS
L1600 (1, 2) 120Ohm/100Mhz
→ M_VREF_DIMM1
→ M_VREF_MCH
→ M_VREF_DIMM0

+0.9VS

C1601	C1602	C1603	C1604	C1605	C1606	C1607	C1608	C1609	C1610	C1600	C1611	C1612			
c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402			
0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V			

GND

Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+0.9VS

C1613	C1614	C1615	C1616	C1617	C1618	C1619	C1620	C1621	C1622	C1623	C1624	C1625			
c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402			
0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V			

GND

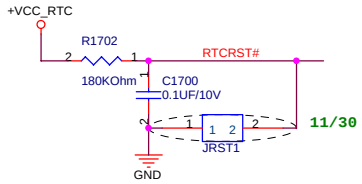
ASUSTeK COMPUTER INC

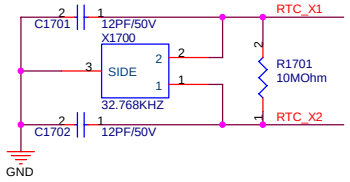
Title : DDR2 TERM

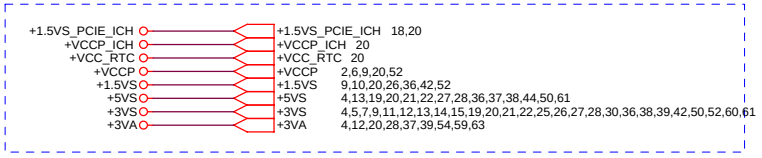
Engineer: *Ping-Yen Tsai*

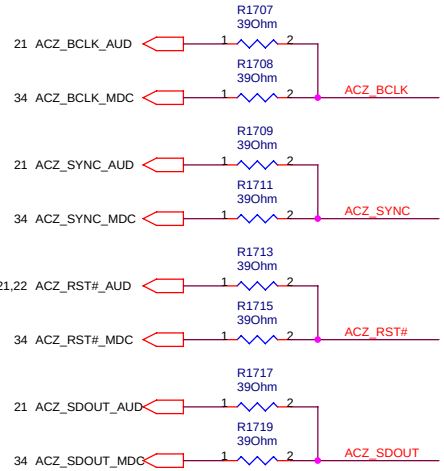
Size	Project Name	Rev
A4	A3F	2.0

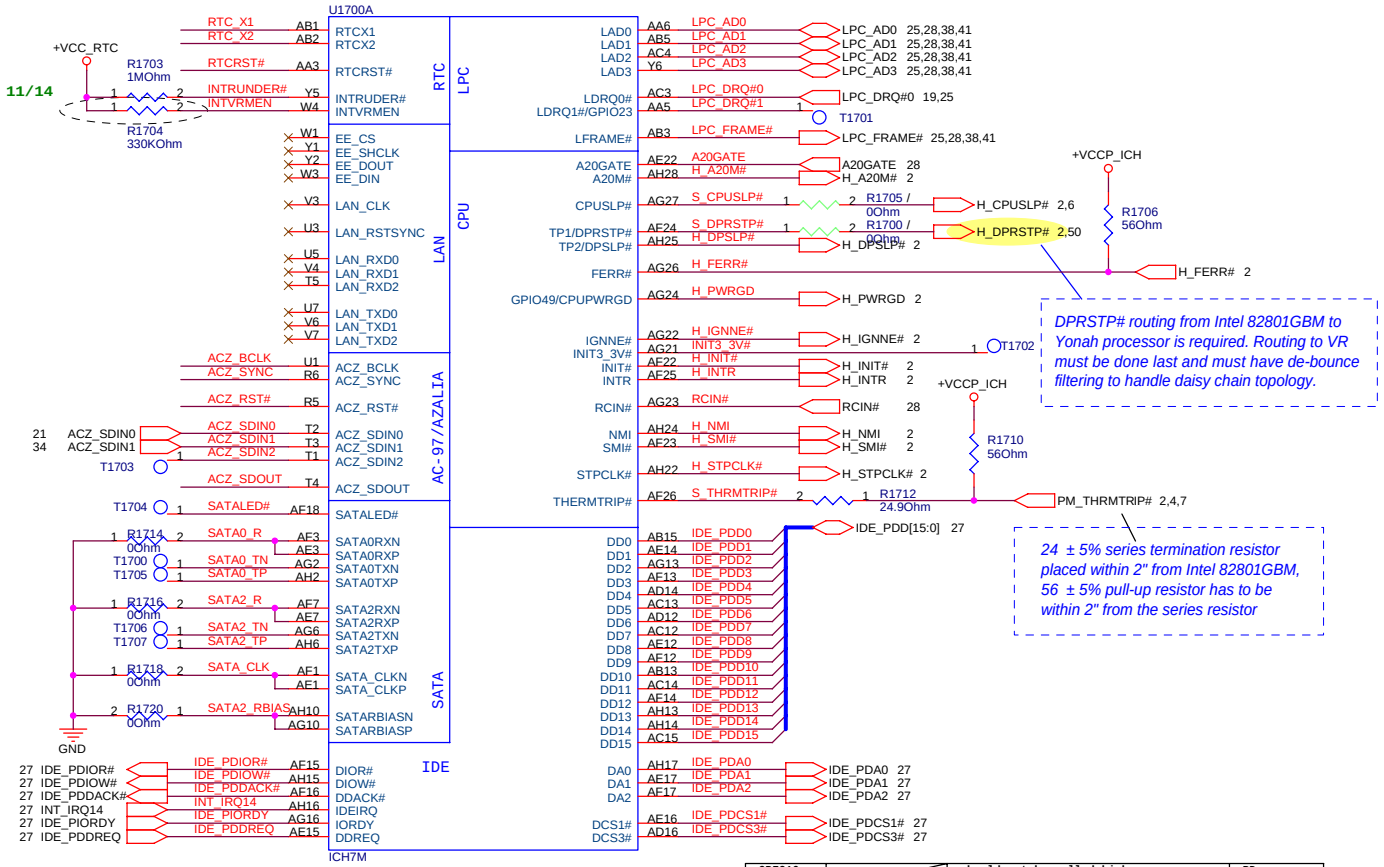
Date: Wednesday, January 18, 2006 Sheet 16 of 63











ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

Title : ICH7-M (1/4)

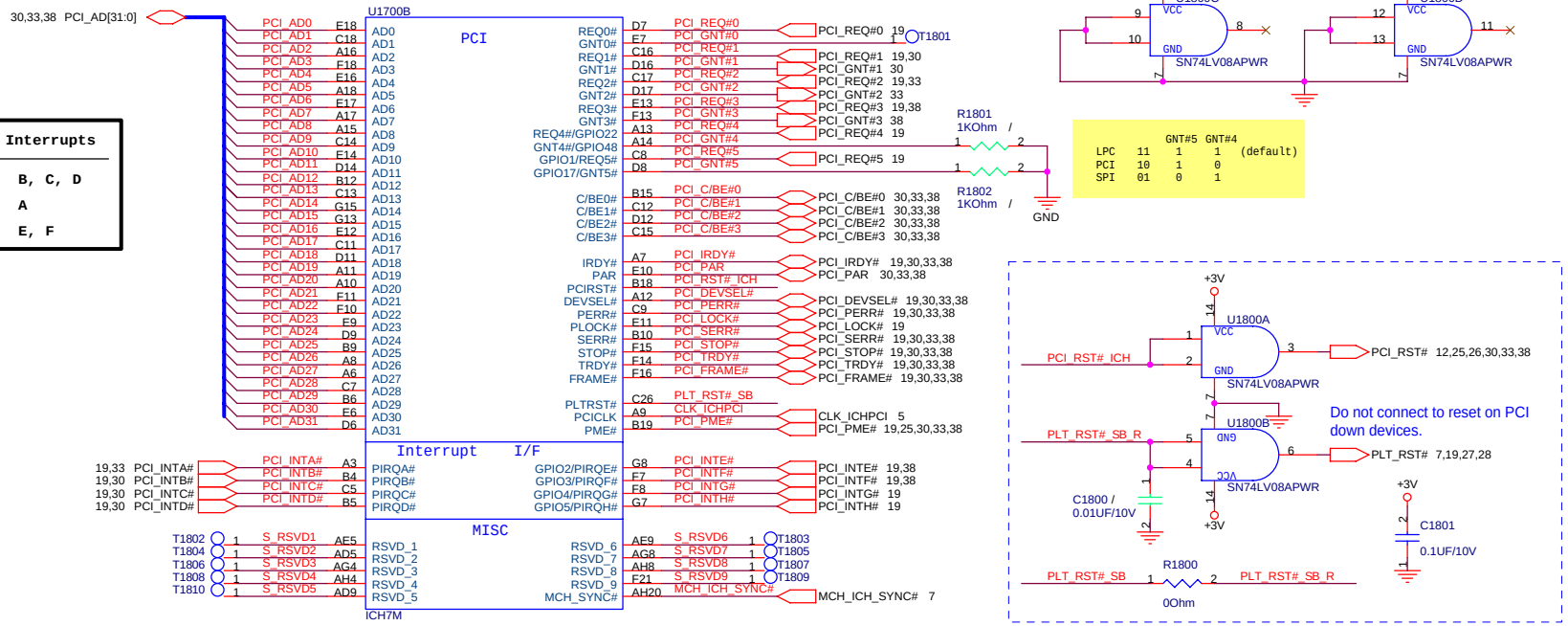
ASUSTeK COMPUTER INC Engineer: Ping-Yen Tsai

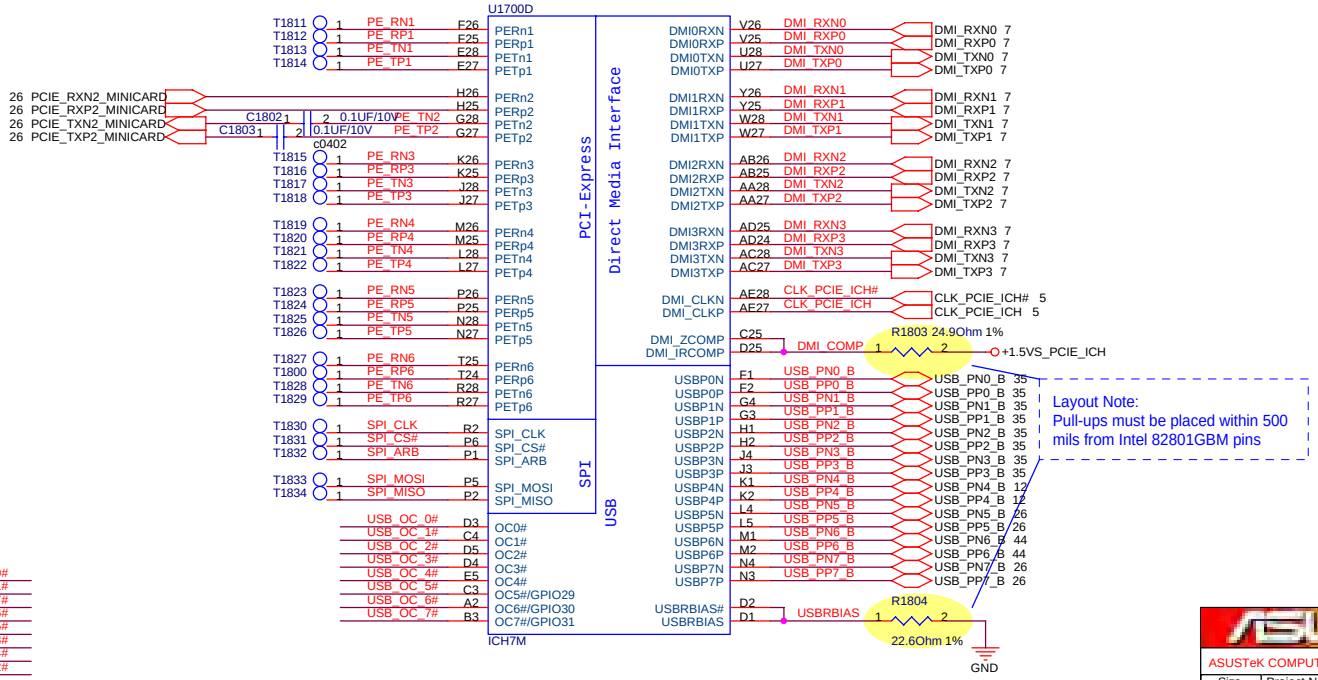
Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 17 of 63

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A
Mini-PCI	AD19	REQ3#/GNT3#	E, F





Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

USB Devices

Port 0	Conn. 0
Port 1	Conn. 1
Port 2	Conn. 2
Port 3	Conn. 3
Port 4	NC
Port 5	Bluetooth
Port 6	CMOS Camera
Port 7	Mini Card

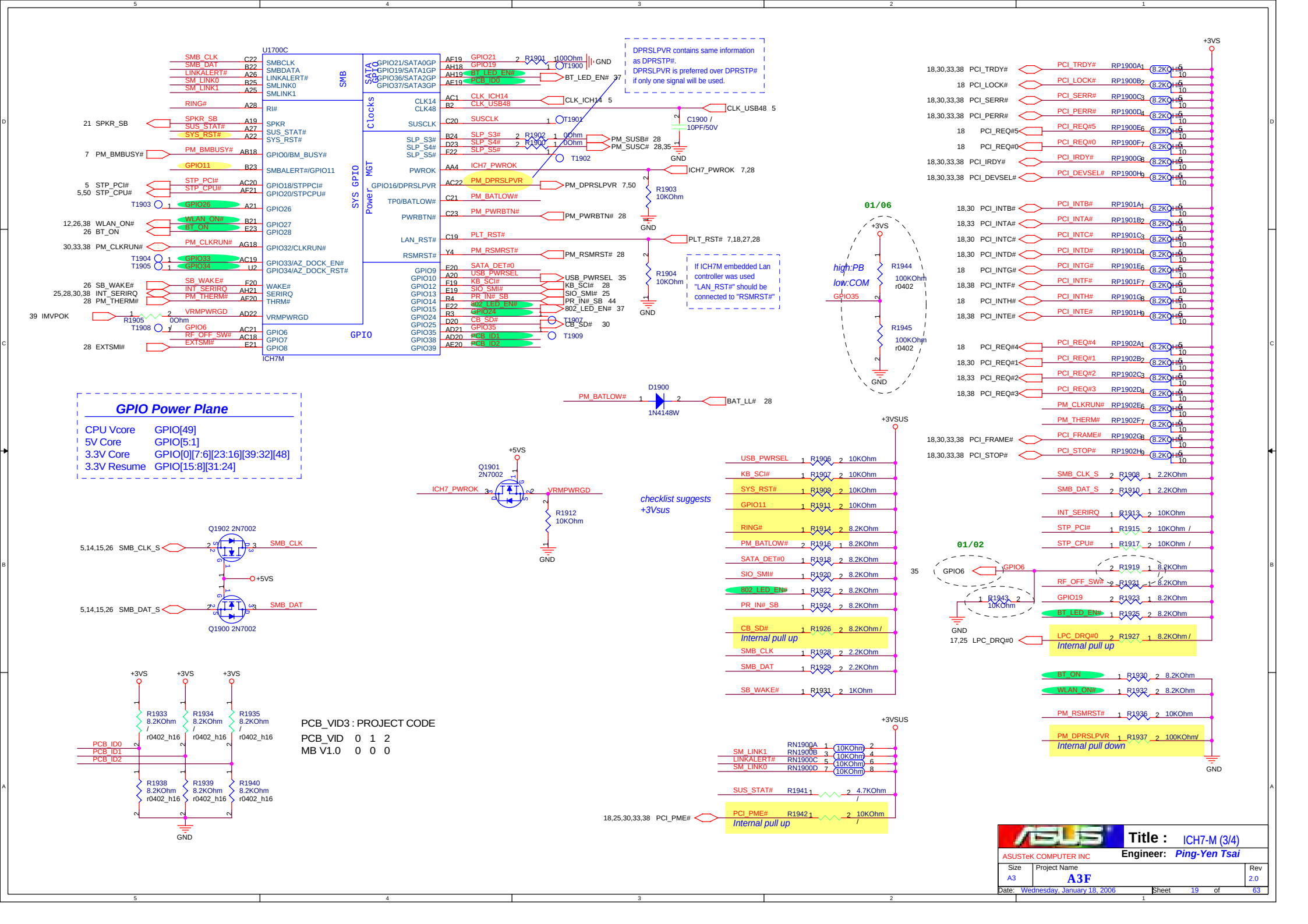
ASUSTeK COMPUTER INC

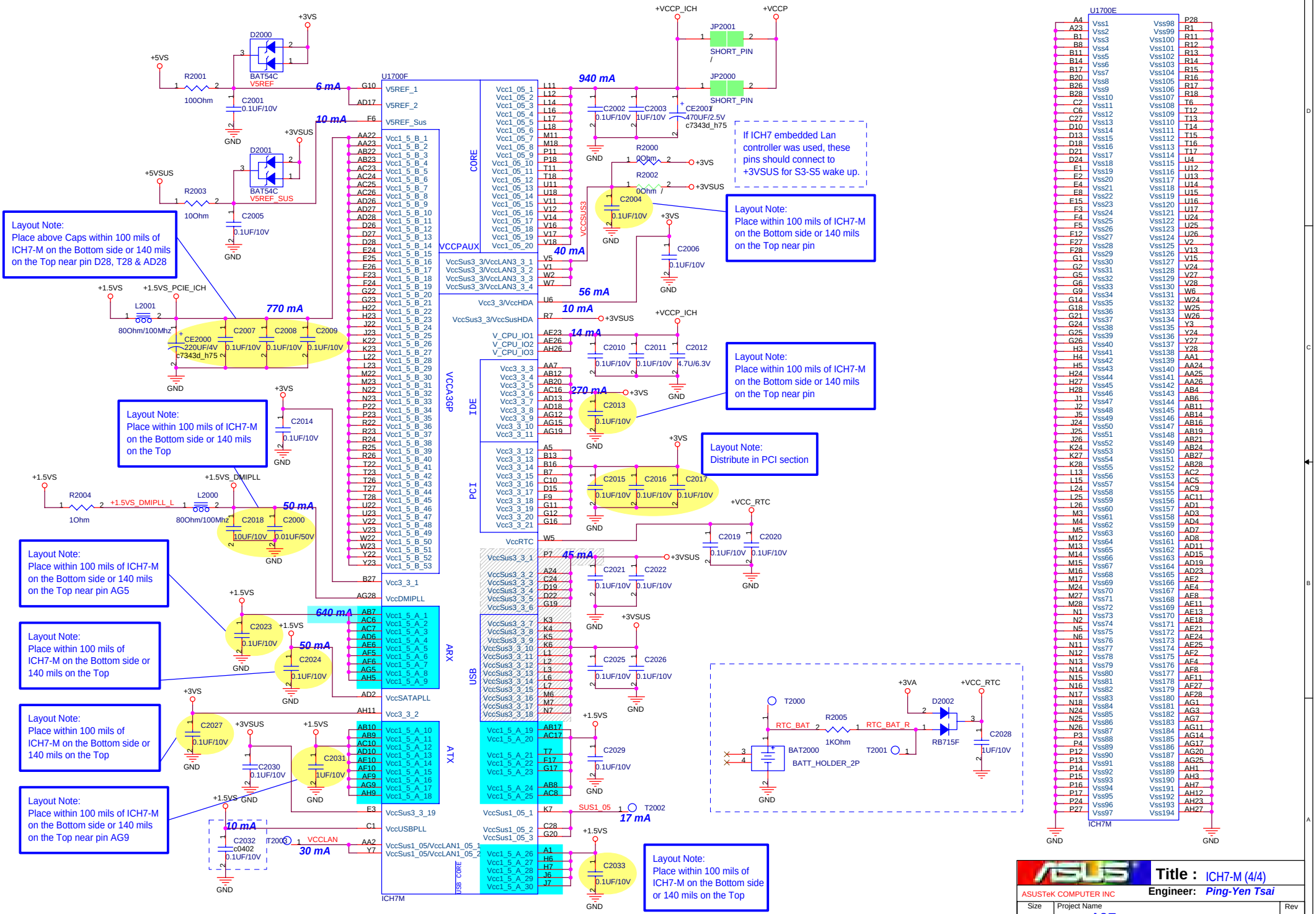
Title : ICH7-M (2/4)

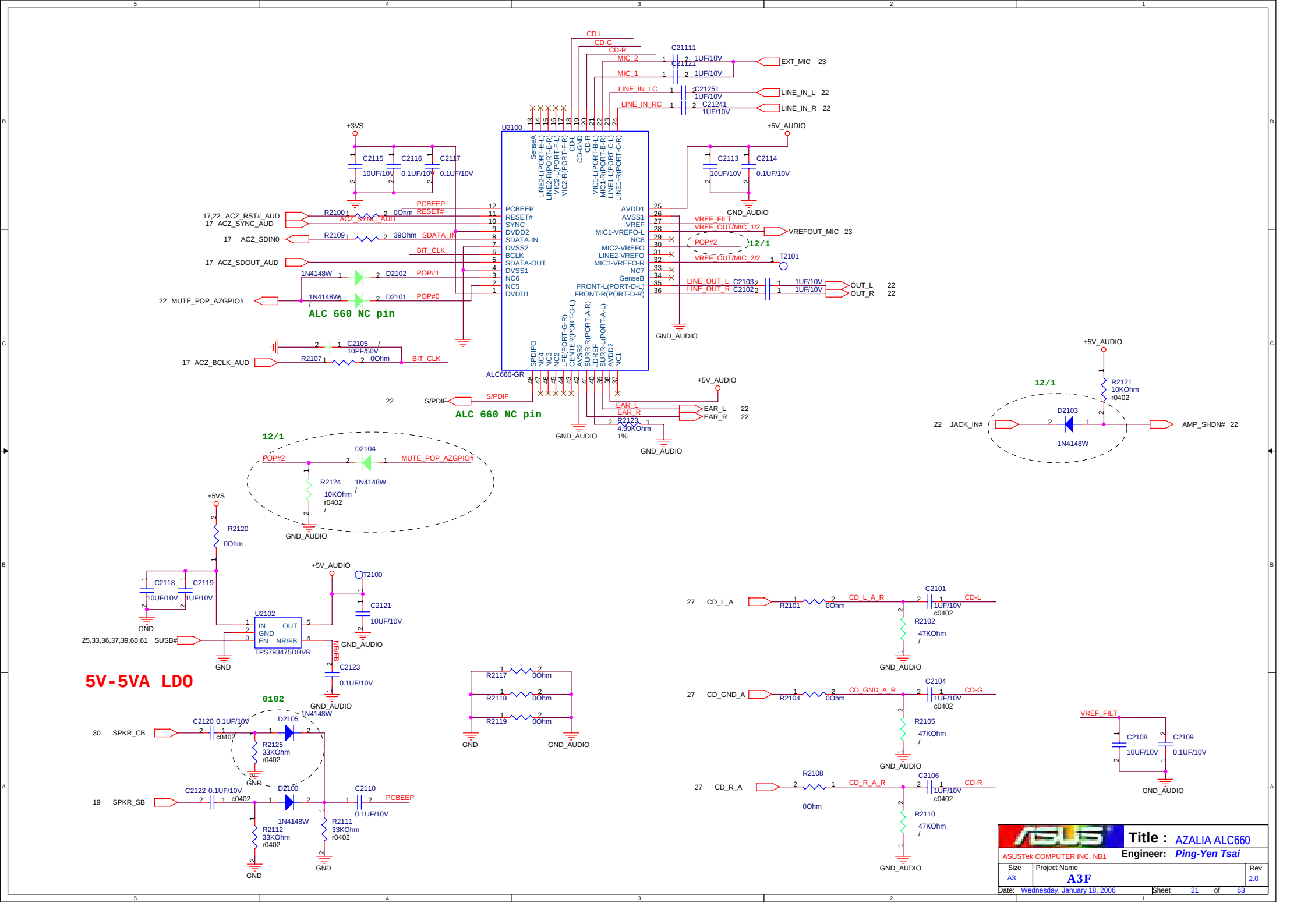
Engineer: Ping-Yen Tsai

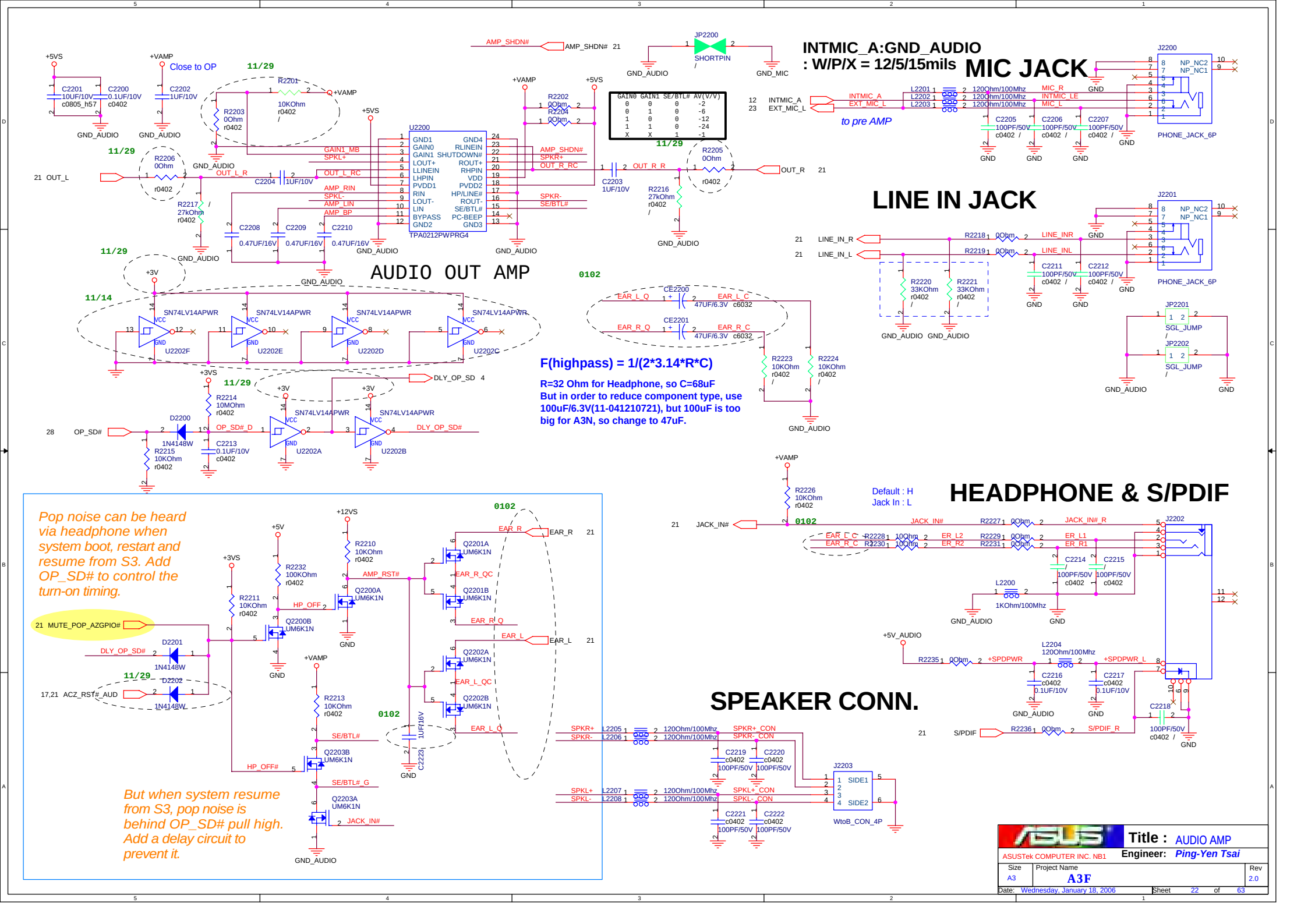
Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 18 of 63


U1700C
SMB_CLK C22
SMB_DAT B22
LINKALERT# A26
SM_LINK0 B25
SM_LINK1 A25
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
SMB
RING# A28
RI#
21 SPKR_SB
SPKR_SB A19
SUS_STAT# A27
SYS_RST# A22
SPKR
SUS_STAT#
SYS_RST#
7 PM_BMBUSY#
PM_BMBUSY# AB18
GPIO0/BM_BUSY#
GPIO11 B23
SMBALERT#/GPIO11
5 STP_PCI#
5,50 STP_CPU#
STP_PCI# AC20
STP_CPU# AF21
GPIO18/STPPCI#
GPIO20/STPCPU#
T1903
GPIO26 A21
GPIO26
12,26,38 WLAN_ON#
26 BT_ON
WLAN_ON# B21
BT_ON E23
GPIO27
GPIO28
30,33,38 PM_CLKRUN#
PM_CLKRUN# AG18
GPIO32/CLKRUN#
T1904
T1905
GPIO33 AC19
GPIO34 U2
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
26 SB_WAKE#
25,28,30,38 INT_SERIRQ
28 PM_THERM#
SB_WAKE# F20
INT_SERIRQ AH21
PM_THERM# AE20
WAKE#
SERIRQ
THRM#
39 IMVPOK
R1905 0Ohm
R1908
VRMPWRGD AD22
GPIO6 AC21
RF_OFF_SW# AC18
EXTSMI# E21
VRMPWRGD
GPIO6
GPIO7
GPIO8
28 EXTSMI#
ICH7M
SYS GPIO
SATA
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
Clocks
CLK14
CLK48
SUSCLK
Power MGT
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
GPIO
AF19 GPIO21
AH18 GPIO19
AH19 BT_LED_EN#
AE19 PCB_ID0
R1901 100Ohm
T1900
GND
BT_LED_EN# 37
AC1 CLK_ICH14
B2 CLK_USB48
CLK_ICH14 5
CLK_USB48 5
C20 SUSCLK
T1901
C1900 / 10PF/50V
B24 SLP_S3#
D23 SLP_S4#
F22 SLP_S5#
R1902 0Ohm
R1903 0Ohm
PM_SUSB# 28
PM_SUSC# 28,35
T1902
GND
AA4 ICH7_PWROK
ICH7_PWROK 7,28
AC22 PM_DPRSLPVR
PM_DPRSLPVR 7,50
R1903 10KOhm
C21 PM_BATLOW#
C23 PM_PWRBTN#
PM_PWRBTN# 28
GND
C19 PLT_RST#
PLT_RST# 7,18,27,28
Y4 PM_RSMRST#
PM_RSMRST# 28
R1904 10KOhm
GND
F20 SATA_DET#0
A20 USB_PWRSEL
F19 KB_SCI#
E19 SIO_SMI#
R4 PR_IN#_SB
F22 802_LED_EN#
GPIO24
R3
D20 CB_SD#
AD21 GPIO35
AD20 PCB_ID1
AE20 PCB_ID2
USB_PWRSEL 35
KB_SCI# 28
SIO_SMI# 25
PR_IN#_SB 44
802_LED_EN# 37
T1907
CB_SD# 30
T1909
DPRSLPVR contains same information as DPRSTP#.
DPRSLPVR is preferred over DPRSTP# if only one signal will be used.
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"
GPIO Power Plane
CPU Vcore GPIO[49]
5V Core GPIO[5:1]
3.3V Core GPIO[0][7:6][23:16][39:32][48]
3.3V Resume GPIO[15:8][31:24]
PM_BATLOW# 1 2 BAT_LL# 28
D1900
1N4148W
+5VS
Q1901 2N7002
ICH7_PWROK 3
VRMPWRGD
R1912 10KOhm
GND
checklist suggests +3Vsus
+3VSUS
USB_PWRSEL R1906 10KOhm
KB_SCI# R1907 10KOhm
SYS_RST# R1909 10KOhm
GPIO11 R1911 10KOhm
RING# R1914 8.2KOhm
PM_BATLOW# R1916 8.2KOhm
SATA_DET#0 R1918 8.2KOhm
SIO_SMI# R1920 8.2KOhm
802_LED_EN# R1922 8.2KOhm
PR_IN#_SB R1924 8.2KOhm
CB_SD# R1926 8.2KOhm /
Internal pull up
SMB_CLK R1928 2.2KOhm
SMB_DAT R1929 2.2KOhm
SB_WAKE# R1931 1KOhm
Q1902 2N7002
5,14,15,26 SMB_CLK_S
SMB_CLK
+5VS
5,14,15,26 SMB_DAT_S
SMB_DAT
Q1900 2N7002
+3VS
R1933 8.2KOhm / r0402_h16
R1934 8.2KOhm / r0402_h16
R1935 8.2KOhm / r0402_h16
PCB_ID0
PCB_ID1
PCB_ID2
R1938 8.2KOhm r0402_h16
R1939 8.2KOhm r0402_h16
R1940 8.2KOhm r0402_h16
GND
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB V1.0 0 0 0
+3VSUS
RN1900A 10KOhm
RN1900B 10KOhm
RN1900C 10KOhm
RN1900D 10KOhm
SM_LINK1
LINKALERT#
SM_LINK0
SUS_STAT# R1941 4.7KOhm /
PCI_PME# R1942 10KOhm /
Internal pull up
18,25,30,33,38 PCI_PME#
01/06
+3VS
high:PB
low:COM
GPIO35
R1944 100KOhm r0402
R1945 100KOhm r0402
GND
+3VS
18,30,33,38 PCI_TRDY# RP1900A 8.2KOhm
18 PCI_LOCK# RP1900B 8.2KOhm
18,30,33,38 PCI_SERR# RP1900C 8.2KOhm
18,30,33,38 PCI_PERR# RP1900D 8.2KOhm
18 PCI_REQ#5 RP1900E 8.2KOhm
18 PCI_REQ#0 RP1900F 8.2KOhm
18,30,33,38 PCI_IRDY# RP1900G 8.2KOhm
18,30,33,38 PCI_DEVSEL# RP1900H 8.2KOhm
18,30 PCI_INTB# RP1901A 8.2KOhm
18,33 PCI_INTA# RP1901B 8.2KOhm
18,30 PCI_INTC# RP1901C 8.2KOhm
18,30 PCI_INTD# RP1901D 8.2KOhm
18 PCI_INTG# RP1901E 8.2KOhm
18,38 PCI_INTF# RP1901F 8.2KOhm
18 PCI_INTH# RP1901G 8.2KOhm
18,38 PCI_INTE# RP1901H 8.2KOhm
18 PCI_REQ#4 RP1902A 8.2KOhm
18,30 PCI_REQ#1 RP1902B 8.2KOhm
18,33 PCI_REQ#2 RP1902C 8.2KOhm
18,38 PCI_REQ#3 RP1902D 8.2KOhm
PM_CLKRUN# RP1902E 8.2KOhm
PM_THERM# RP1902F 8.2KOhm
18,30,33,38 PCI_FRAME# RP1902G 8.2KOhm
18,30,33,38 PCI_STOP# RP1902H 8.2KOhm
SMB_CLK_S R1908 2.2KOhm
SMB_DAT_S R1910 2.2KOhm
INT_SERIRQ R1913 10KOhm
STP_PCI# R1915 10KOhm /
STP_CPU# R1917 10KOhm /
01/02
35 GPIO6
GPIO6 R1919 8.2KOhm
RF_OFF_SW# R1921 8.2KOhm
R1943 10KOhm
GPIO19 R1923 8.2KOhm
BT_LED_EN# R1925 8.2KOhm
GND
17,25 LPC_DRQ#0
LPC_DRQ#0 R1927 8.2KOhm /
Internal pull up
BT_ON R1930 8.2KOhm
WLAN_ON# R1932 8.2KOhm
PM_RSMRST# R1936 10KOhm
PM_DPRSLPVR R1937 100KOhm/
Internal pull down
GND
Title : ICH7-M (3/4)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 19 of 63


Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Distribute in PCI section
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
U1700F
ICH7M
U1700E
ICH7M
CORE
VCCPAUX
VCCA96P
IDE
PCI
USB
ARX
ATX
USB CORE
6 mA
10 mA
770 mA
940 mA
40 mA
56 mA
10 mA
14 mA
270 mA
50 mA
640 mA
50 mA
45 mA
17 mA
10 mA
30 mA
Title : ICH7-M (4/4)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 20 of 63

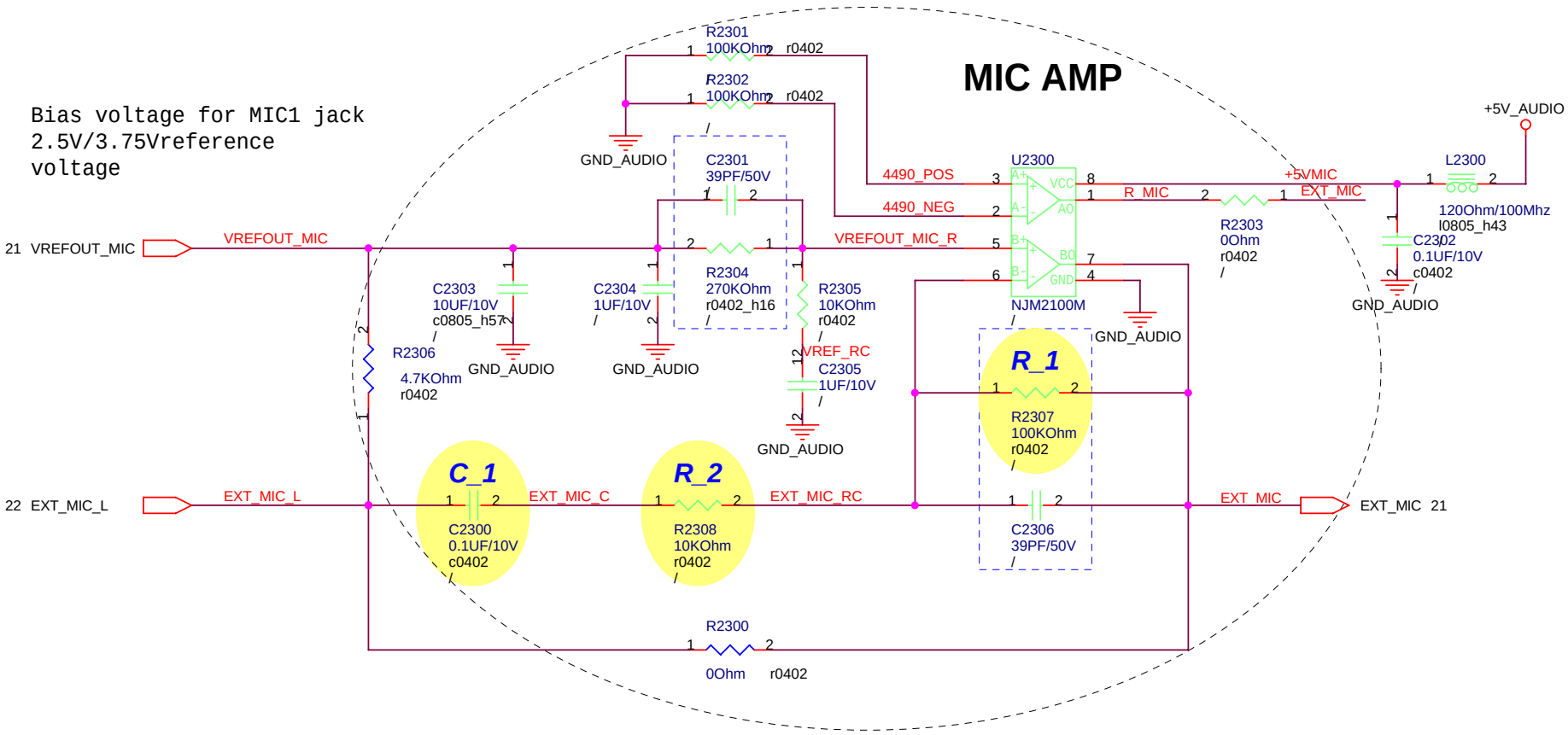

U2100
ALC660-GR
ALC 660 NC pin
ALC 660 NC pin
5V-5VA LDO
U2102
TPS793475DBVR
Title : AZALIA ALC660
ASUSTek COMPUTER INC. NB1
Engineer: Ping-Yen Tsai
Project Name A3F
Size A3
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 21 of 63


INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils
MIC JACK
LINE IN JACK
AUDIO OUT AMP
HEADPHONE & S/PDIF
SPEAKER CONN.
F(highpass) = 1/(2*3.14*R*C)
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.
Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.
Close to OP
to pre AMP
Default : H
Jack In : L
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB1
Engineer: Ping-Yen Tsai
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 22 of 63

1214

MIC AMP

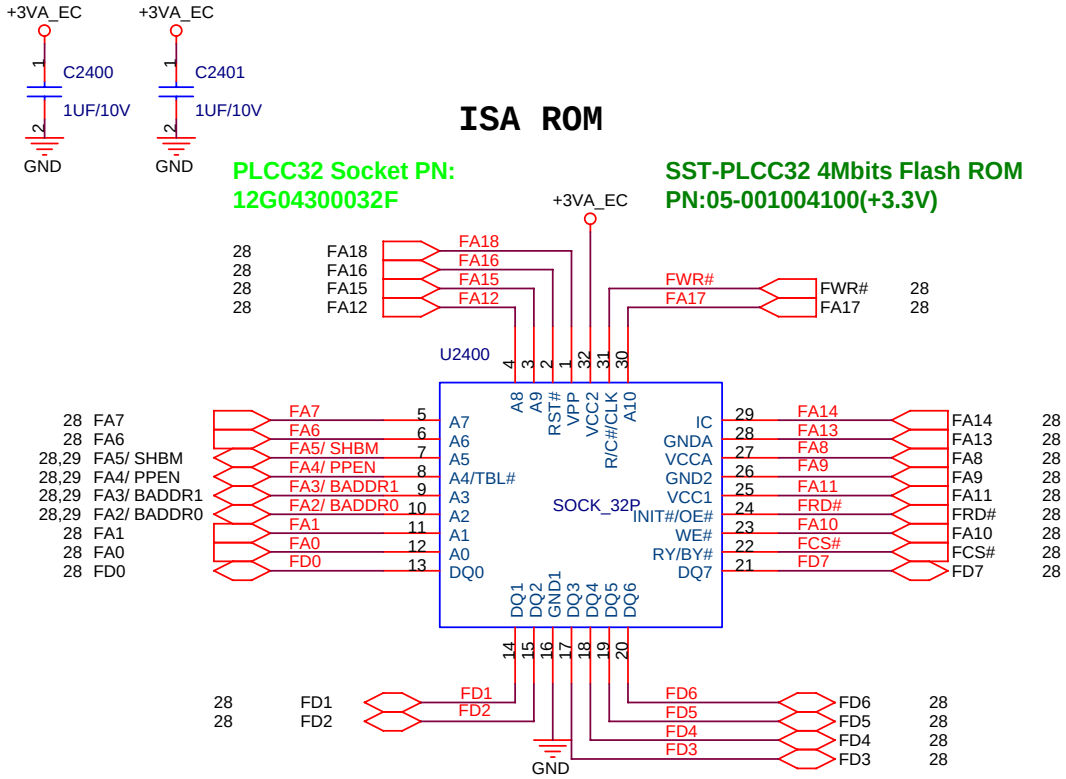
Bias voltage for MIC1 jack
2.5V/3.75Vreference
voltage



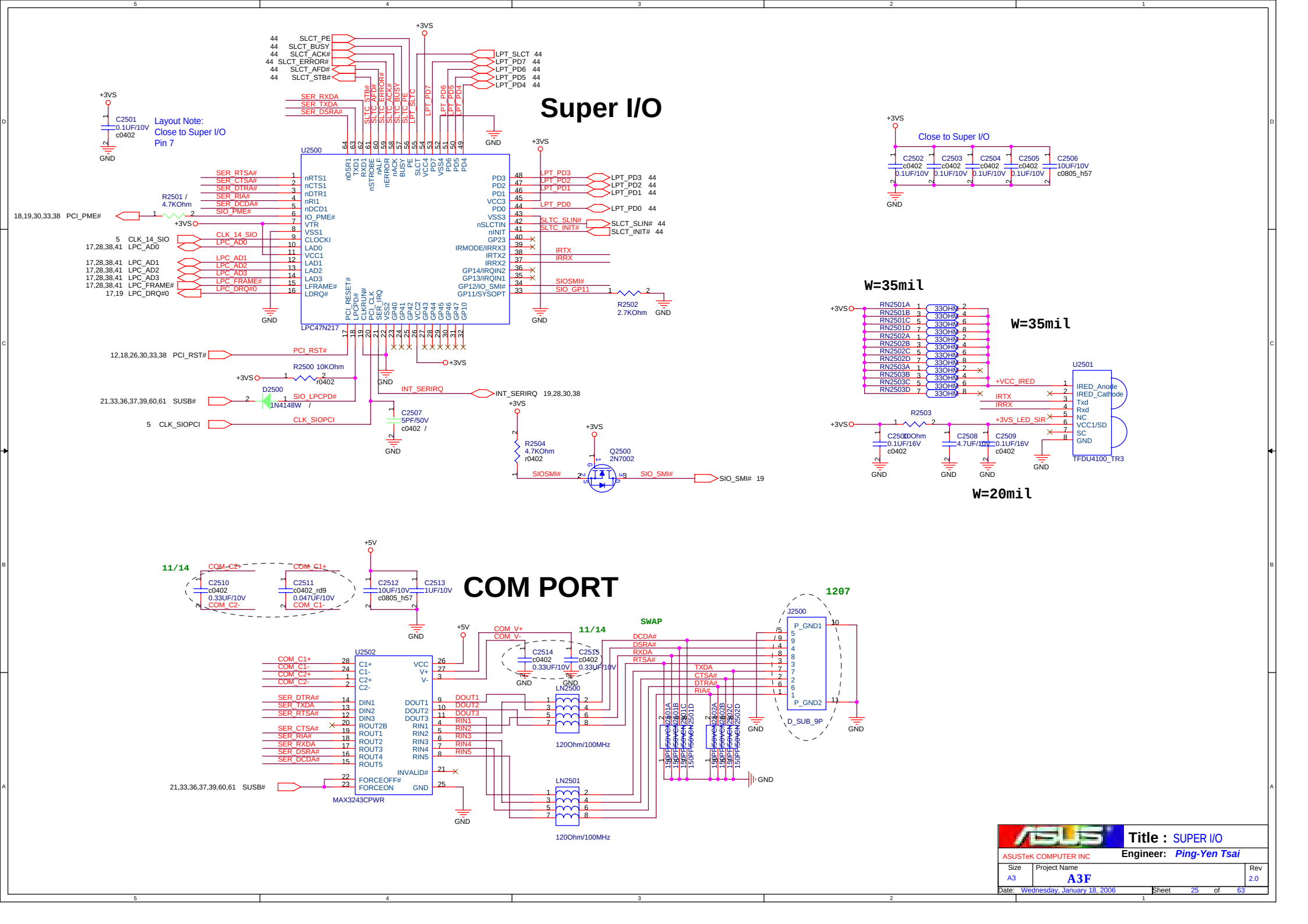
High-Pass Filter Cutoff Frequency
Fc = 1 / (2*3.14*C_1*R_2) = 159 Hz

Gain = - R_1 / R_2 = -10

ASUSTek COMPUTER INC. NB1	Title : MIC Pre-AMP	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 23 of 63	



ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 24 of 63	


Super I/O
COM PORT
Layout Note:
Close to Super I/O
Pin 7
Close to Super I/O
W=35mil
W=35mil
W=20mil
U2500
LPC47N217
U2501
TFDU4100_TR3
U2502
MAX3243CPWR
J2500
D_SUB_9P
LN2500
LN2501
120Ohm/100MHz
120Ohm/100MHz
SWAP
11/14
11/14
1207
Title : SUPER I/O
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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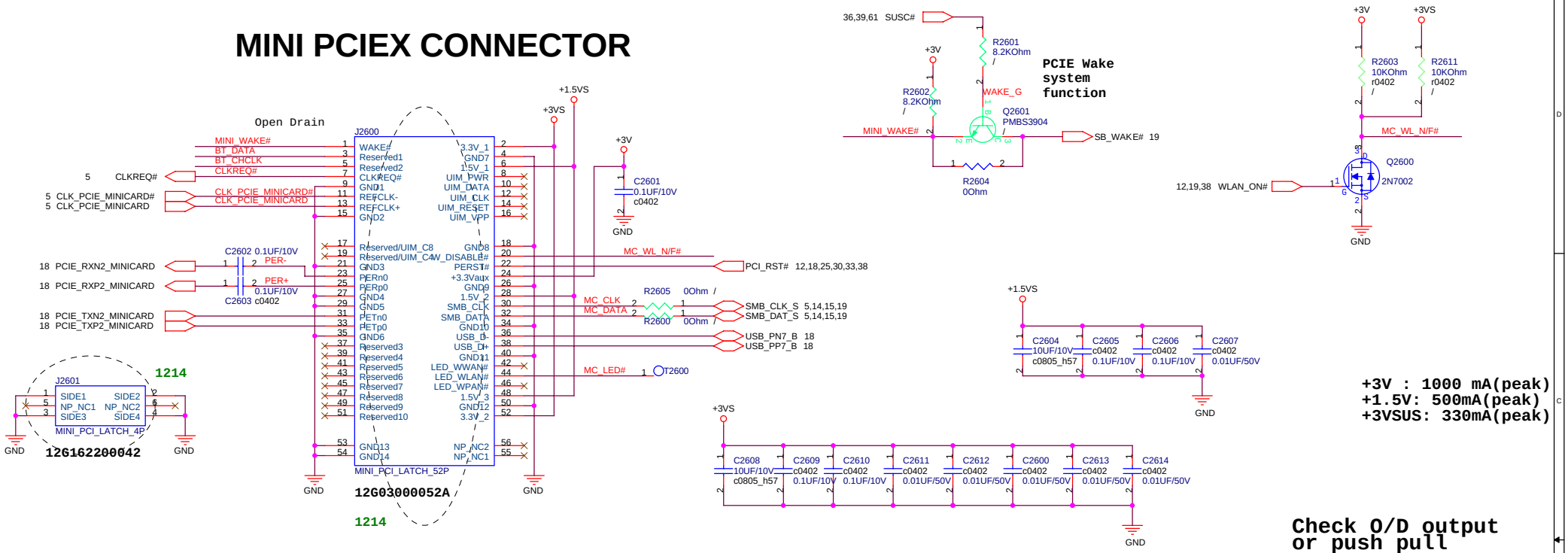
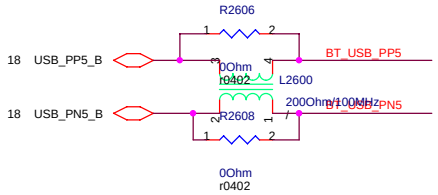
MINI PCIEX CONNECTOR

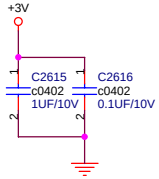


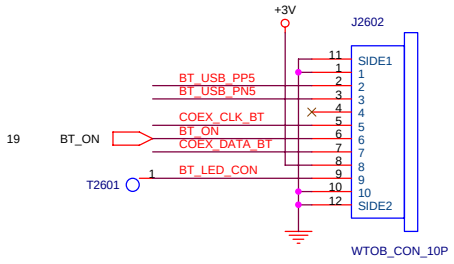
+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)

Check O/D output or push pull

BLUETOOTH CONNECTOR



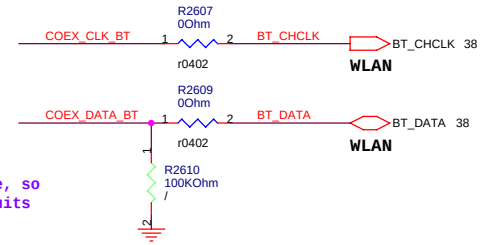




Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT

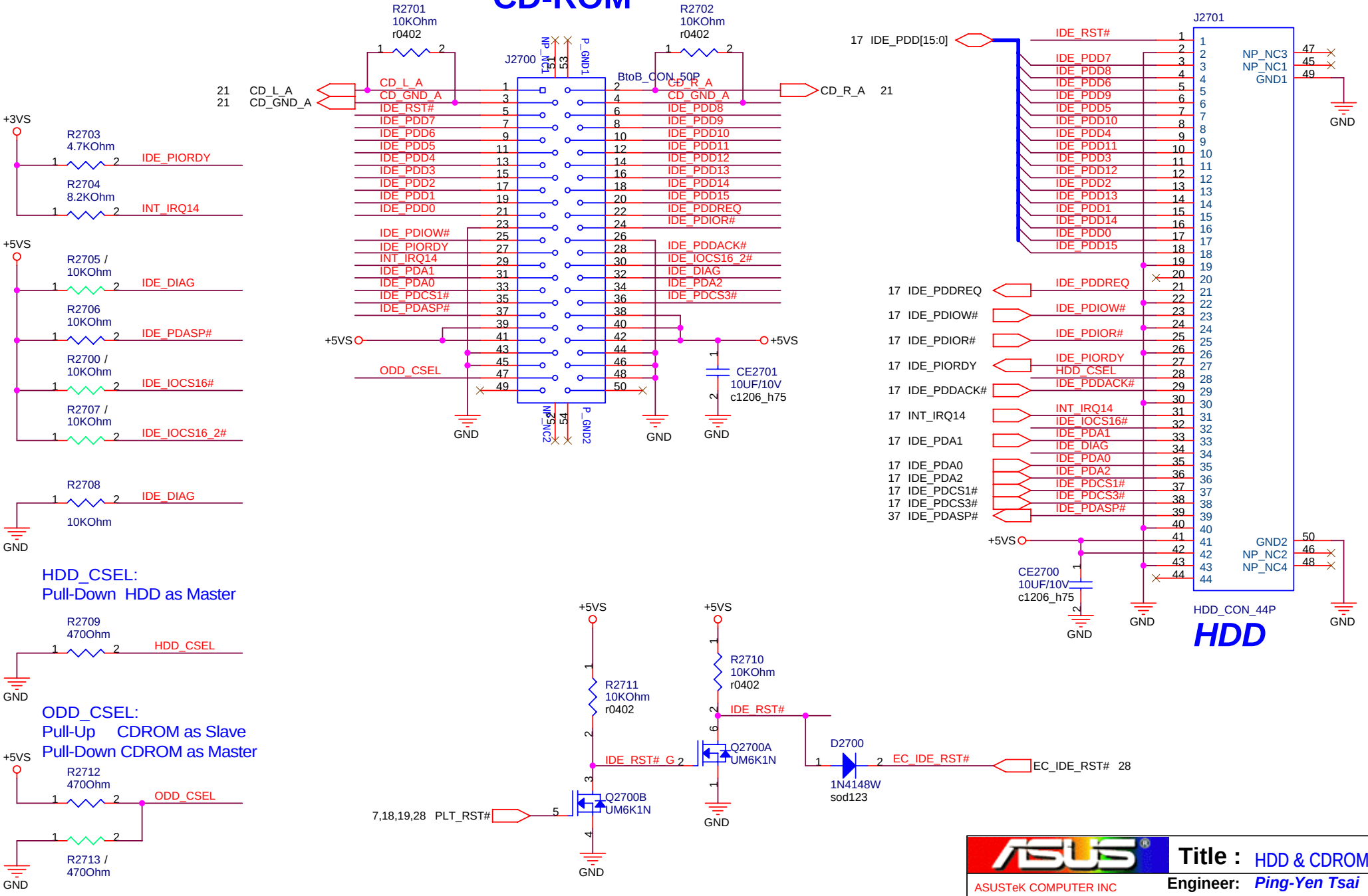
BT_ON 3.3V at GPIO38

BT Module has no leakage, so discard PMOS block circuits



ASUSTeK COMPUTER INC	Title : MINI PCIEX (TV) & BT Conn	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 26 of 63	

CD-ROM



ASUSTeK COMPUTER INC

Title : HDD & CDROM

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A4	**A3F**	2.0

Date: Wednesday, January 18, 2006 Sheet 27 of 63

TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

Follow A4 Keyboard

U2800 — IT8510TE

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 CLK_ECPCI LPC_FRAME# PLT_RST# INT_SERIRQ EXTSMI# ECSCI# A20GATE RCIN# EC_RST# PWUREQ#

FRD# FWR# FCS# FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7 FA0 FA1 FA2/ BADDR0 FA3/ BADDR1 FA4/ PPEN FA5/ SHBM FA6 FA7 FA8 FA9 FA10 FA11 FA12 FA13 FA14 FA15 FA16 FA17 FA18 FA19

KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15

EC_XIN EC_XOUT

EXT_PS2_CLK EXT_PS2_DAT PS2CLK1 PS2DAT1

SMCLK_BAT SMDATA_BAT SMB1_CLK SMB1_DAT

BAT0_AD EC_ADC1 AC_AD EC_ADC3 KB_ID0 KB_ID1

FAN0_DA EC_DAC1 INVTER_DA BATSEL_2P#

BRIGHT_PWM FAN_PWM EC_GPA2 EC_GPA3 CHG_LED_UP# PWR_LED_UP# EC_GPA6 LCD_BACKOFF#

NUM_LED CAP_LED SCRL_LED THRO_CPU

DJ_LED# EMAIL_LED# ACIN_OC# OP_SD# BAT_IN_OC# EC_IDE_RST#

PM_SUSB# PM_SUSC# PR_IN# EC PB_IN#_EC EC_GPD5 FAN0_TACH EC_GPD7

EMAIL# INTERNET# MARATHON# DISTP# PWRSW#_EC EC_GPE5 LID_EC# EC_GPE7

TPAD_CLK TPAD_DAT PWRLMT# DJ_SW#

THRM_CPU# EC_GPC5 PMTHERM# AC_APR_UC#

EC_GPH0 VSUS_GD# IMVPOK# PM_PWRBTN# SUSC_EC# SUSB_EC# CPU_VRON PM_RSMRST#

EC_GPI0 WATCHDOG# EC_GPI2 CHG_EN# PRECHG BAT_LL# BAT_LEARN

SMBus: SMCLK_BAT 40, SMDATA_BAT 40, SMB1_CLK 4, SMB1_DAT 4

ADC: BAT0_AD 29, AC_AD 29

DAC: FAN0_DA 4, INVTER_DA 12, BATSEL_2P# 57

GPIO: BRIGHT_PWM 12, CHG_LED_UP# 37, PWR_LED_UP# 37, LCD_BACKOFF# 12, NUM_LED 37, CAP_LED 37, SCRL_LED 37, DJ_LED# 37, EMAIL_LED# 37, ACIN_OC# 59, OP_SD# 22, BAT_IN_OC# 59, EC_IDE_RST# 27, PM_SUSB# 19, PM_SUSC# 19,35, PB_IN#_EC 44, FAN0_TACH 4, EMAIL# 37, INTERNET# 37, MARATHON# 37, DISTP# 37, PWRSW#_EC 37, PWRLMT# 57, DJ_SW# 37, THRM_CPU# 4, VSUS_ON 4,51, PM_PWRBTN# 19, SUSC_EC# 39, SUSB_EC# 39, CPU_VRON 50, PM_RSMRST# 19, ICH7_PWROK 7,19, CHG_EN# 57, PRECHG 57, BAT_LL# 19, BAT_LEARN 57

to Battery

to Thermal

no define

watchdog

D2801 RB715F — OVER_TEMP# 4, PM_THERM# 19

D2802 1N4148W

RN2801A–D 8.2KOHM — EXT_PS2_CLK, EXT_PS2_DAT, PS2CLK1, PS2DAT1

RN2802A–D 4.7KOHM — TPAD_CLK, TPAD_DAT, SMB1_CLK, SMB1_DAT

RN2803A–D 8.2KOHM — A20GATE, RCIN#, KB_ID0, KB_ID1

R2801 10KOhm BAT_IN_OC#; R2802 10KOhm ACIN_OC#; R2803 4.7KOhm SMCLK_BAT; R2804 4.7KOhm SMDATA_BAT; R2805 10KOhm DJ_SW#; R2819 10KOhm LID_EC#; R2822 100KOhm PWRLMT#; R2806 10KOhm EXTSMI#; R2807 10KOhm PM_PWRBTN# (r0402)

R2808 100KOhm (SUSB_EC#); R2809 100KOhm (SUSC_EC#); RN2805A 10KOhm (PM_SUSB#); RN2805B 10KOhm (PM_SUSC#)

R2811 10KOhm r0402 (AC_APR_UC#); Q2800 2N7002 — AC_APR_UC 57,59

D2803 1N4148W (LID_EC# → LID_SW# 12); R2820 0Ohm r0402

R2810 0Ohm; C2805 10UF/10V; C2806 0.1UF/10V; C2800 0.1UF/10V

J2800 FPC_CON_28P — KSO7 KSO0 KSI1 KSI7 KSO9 KSI6 KSI5 KSO3 KSI4 KSI2 KSO1 KSI3 KSI0 KSO13 KSO5 KSO2 KSO4 KSO8 KSO6 KSO11 KSO10 KSO12 KSO14 KSO15 KB_ID0 KB_ID1

R2812 100Ohm (EC_GPH0 → VSUS_ON); R2813 0Ohm (EC_GPI0 → ICH7_PWROK); R2818 0Ohm (ECSCI# → KB_SCI# 19)

R2815 / 10MOhm; R2816 0Ohm; R2817 0Ohm; R2821 0Ohm (51,60 FORCE_OFF#)

X2800 SIDE 32.768KHZ; C2809 12PF/50V; C2814 12PF/50V

close to EC

Cload=12.5PF

JP2800 1MM_OPEN_5MIL

RN2804A–D 10KOhm — EMAIL# INTERNET# DISTP# MARATHON#

C2810–C2813 0.1UF/10V

Layout Note: Close to Switch

Q2801 2N7002 (THRO_CPU → H_PROCHOT_S# 2)

1205

Change threshold = 2.9V

tD = 0.69*10^6*CD ps = 6.9 ms

U2801 CD OUT VDD NC GND — RN5VD29CA; EC_RST_SW# 37 → EC_RST#; C2807 1UF/10V; C2808 0.1UF/10V

ASUSTek COMPUTER INC

Title : EC IT8510TE

Engineer: Ping-Yen Tsai

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 28 of 63

EC Hardware Strap

Strap value sampled after VSTBY power up reset

+3VA_EC

PNPCFG base address set by SWCBAHR/SWCBALR

R2901 / 10KOhm r0402

FA2/ BADDR0 → FA2/ BADDR0 24,28

R2905 10KOhm r0402

GND

+3VA_EC

R2902 10KOhm r0402

FA3/ BADDR1 → FA3/ BADDR1 24,28

R2906 / 10KOhm r0402

GND

BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory

+3VA_EC

R2909 10KOhm r0402

FA5/ SHBM → FA5/ SHBM 24,28

R2912 / 10KOhm r0402

GND

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

+3VA_EC

R2900 / 10KOhm r0402

FA4/ PPEN → FA4/ PPEN 24,28

R2913 10KOhm r0402

GND

PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

EC ADC

Battery

BAT **16.8V**

R2903 / 18KOhm r0402_h16

BAT0_R_AD

R2904 / 1KOhm

R2907 / 3.92KOhm

D2901 / 1N4148W

D2902 / 1N4148W

+3VACC

BAT0_AD 28

C2900 / 0.1UF/10V c0402

GND

Adaptor

A/D_DOCK_IN **19V**

3V

R2908 / 20KOhm

AC_R_AD

R2910 / 1KOhm

R2911 / 3.74KOhm

D2903 / 1N4148W

D2900 / 1N4148W

+3VACC

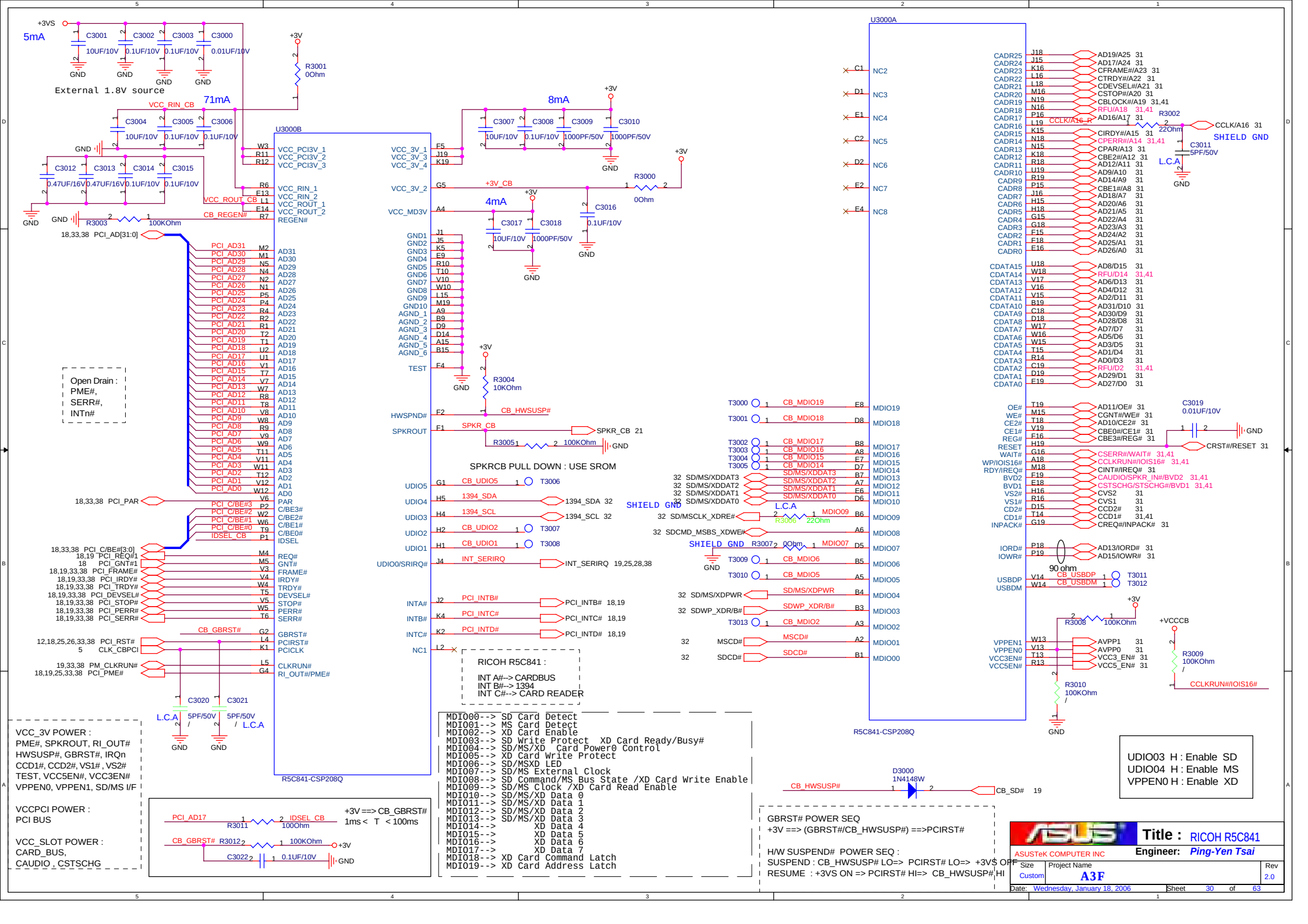
AC_AD 28

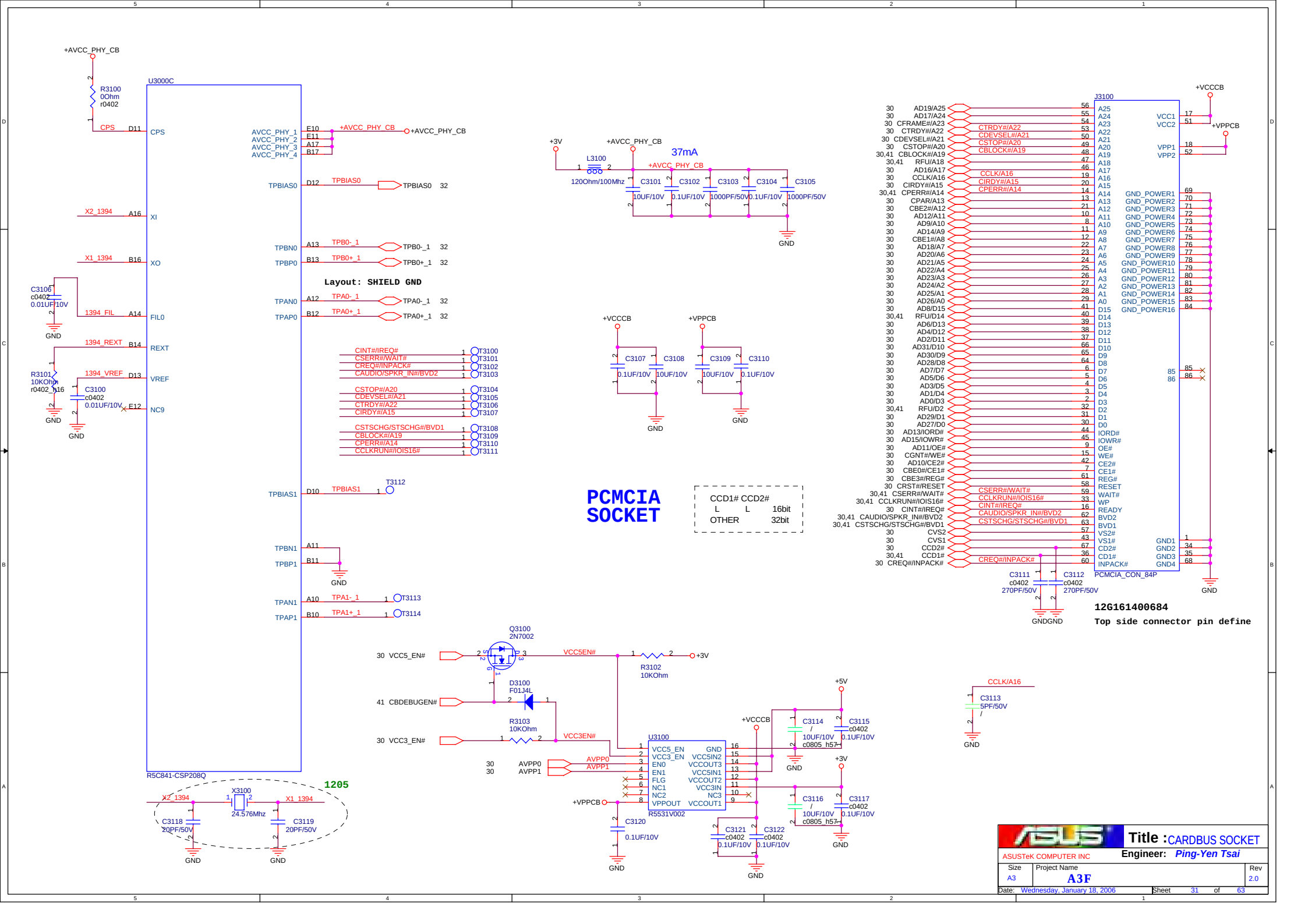
2.99V

C2901 / 0.1UF/10V c0402

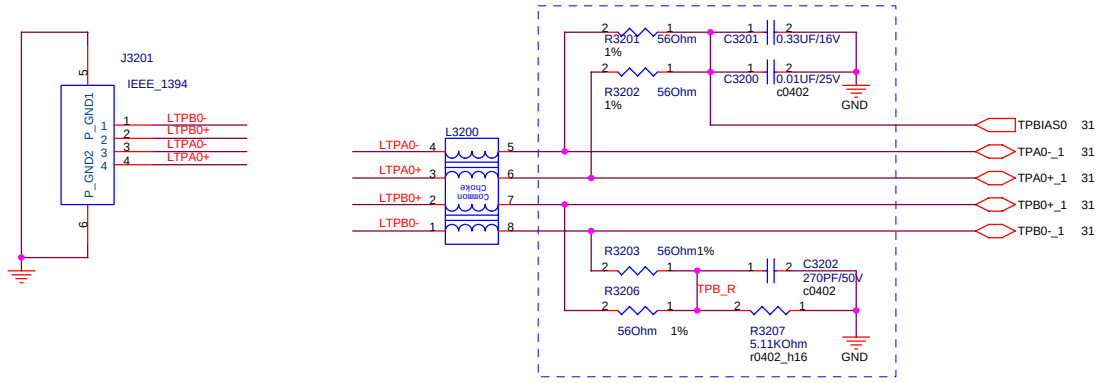
GND

ASUSTek COMPUTER INC	Title : EC IT8510TE(2/2)	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 29 of 63	

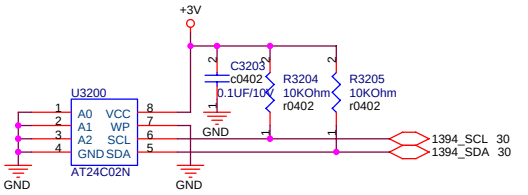

+3VS
5mA
C3001 10UF/10V
C3002 0.1UF/10V
C3003 0.1UF/10V
C3000 0.01UF/10V
GND
External 1.8V source
+3V
R3001 0Ohm
71mA
VCC_RIN_CB
C3004 10UF/10V
C3005 0.1UF/10V
C3006 0.1UF/10V
C3012 0.47UF/16V
C3013 0.47UF/16V
C3014 0.1UF/10V
C3015 0.1UF/10V
VCC_ROUT_CB
CB_REGEN#
R3003 100KOhm
18,33,38 PCI_AD[31:0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
18,33,38 PCI_PAR
PAR
PCI_C/BE#3 PCI_C/BE#2 PCI_C/BE#1 PCI_C/BE#0
C/BE3# C/BE2# C/BE1# C/BE0#
IDSEL_CB
IDSEL
18,33,38 PCI_C/BE#[3:0]
18,19 PCI_REQ#1
18 PCI_GNT#1
18,19,33,38 PCI_FRAME#
18,19,33,38 PCI_IRDY#
18,19,33,38 PCI_TRDY#
18,19,33,38 PCI_DEVSEL#
18,19,33,38 PCI_STOP#
18,19,33,38 PCI_PERR#
18,19,33,38 PCI_SERR#
REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
CB_GBRST#
GBRST#
12,18,25,26,33,38 PCI_RST#
5 CLK_CBPCI
PCIRST# PCICLK
19,33,38 PM_CLKRUN#
18,19,25,33,38 PCI_PME#
CLKRUN# RI_OUT#/PME#
C3020 5PF/50V
C3021 5PF/50V
L.C.A
U3000B
R5C841-CSP208Q
Open Drain :
PME#,
SERR#,
INTn#
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
PCI_AD17 R3011 IDSEL_CB 100Ohm
CB_GBRST# R3012 100KOhm +3V
C3022 0.1UF/10V GND
+3V ==> CB_GBRST#
1ms < T < 100ms
VCC_3V_1 VCC_3V_3 VCC_3V_4
VCC_3V_2
VCC_MD3V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND_1 AGND_2 AGND_3 AGND_4 AGND_5 AGND_6
TEST
8mA
C3007 10UF/10V
C3008 0.1UF/10V
C3009 1000PF/50V
C3010 1000PF/50V
+3V_CB
R3000 0Ohm
4mA
C3017 10UF/10V
C3018 1000PF/50V
C3016 0.1UF/10V
R3004 10KOhm
HWSPND#
CB_HWSUSP#
SPKROUT
SPKR_CB
R3005 100KOhm
SPKR_CB 21
SPKRCB PULL DOWN : USE SROM
UDIO5 CB_UDIO5 T3006
UDIO4 1394_SDA 1394_SDA 32
UDIO3 1394_SCL 1394_SCL 32
UDIO2 CB_UDIO2 T3007
UDIO1 CB_UDIO1 T3008
UDIO0/SRIRQ# INT_SERIRQ INT_SERIRQ 19,25,28,38
INTA# PCI_INTB# PCI_INTB# 18,19
INTB# PCI_INTC# PCI_INTC# 18,19
INTC# PCI_INTD# PCI_INTD# 18,19
NC1
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
U3000A
NC2 NC3 NC4 NC5 NC6 NC7 NC8
T3000 CB_MDIO19 MDIO19
T3001 CB_MDIO18 MDIO18
T3002 CB_MDIO17 MDIO17
T3003 CB_MDIO16 MDIO16
T3004 CB_MDIO15 MDIO15
T3005 CB_MDIO14 MDIO14
32 SD/MS/XDDAT3 MDIO13
32 SD/MS/XDDAT2 MDIO12
32 SD/MS/XDDAT1 MDIO11
32 SD/MS/XDDAT0 MDIO10
SHIELD GND
L.C.A
32 SD/MSCLK_XDRE# R3006 22Ohm MDIO09
32 SDCMD_MSBS_XDWE# MDIO08
SHIELD GND R3007 0Ohm MDIO07
T3009 CB_MDIO6 MDIO06
T3010 CB_MDIO5 MDIO05
32 SD/MS/XDPWR MDIO04
32 SDWP_XDR/B# MDIO03
T3013 CB_MDIO2 MDIO02
32 MSCD# MDIO01
32 SDCD# MDIO00
R5C841-CSP208Q
CADR25 CADR24 CADR23 CADR22 CADR21 CADR20 CADR19 CADR18 CADR17 CADR16 CADR15 CADR14 CADR13 CADR12 CADR11 CADR10 CADR9 CADR8 CADR7 CADR6 CADR5 CADR4 CADR3 CADR2 CADR1 CADR0
AD19/A25 AD17/A24 CFRAME#/A23 CTRDY#/A22 CDEVSEL#/A21 CSTOP#/A20 CBLOCK#/A19 RFU/A18 AD16/A17
CCLK/A16_R R3002 22Ohm CCLK/A16 31
SHIELD GND
C3011 5PF/50V
L.C.A
CIRDY#/A15 CPERR#/A14 CPAR/A13 CBE2#/A12 AD12/A11 AD9/A10 AD14/A9 CBE1#/A8 AD18/A7 AD20/A6 AD21/A5 AD22/A4 AD23/A3 AD24/A2 AD25/A1 AD26/A0
CDATA15 CDATA14 CDATA13 CDATA12 CDATA11 CDATA10 CDATA9 CDATA8 CDATA7 CDATA6 CDATA5 CDATA4 CDATA3 CDATA2 CDATA1 CDATA0
AD8/D15 RFU/D14 AD6/D13 AD4/D12 AD2/D11 AD31/D10 AD30/D9 AD28/D8 AD7/D7 AD5/D6 AD3/D5 AD1/D4 AD0/D3 RFU/D2 AD29/D1 AD27/D0
OE# WE# CE2# CE1# REG# RESET WAIT# WP/IOIS16# RDY/IREQ# BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
AD11/OE# CGNT#/WE# AD10/CE2# CBE0#/CE1# CBE3#/REG#
C3019 0.01UF/10V
GND
CRST#/RESET
CSERR#/WAIT# CCLKRUN#/IOIS16# CINT#/IREQ# CAUDIO/SPKR_IN#/BVD2 CSTSCHG/STSCHG#/BVD1
IORD# IOWR#
AD13/IORD# AD15/IOWR#
90 ohm
USBDP USBDM
CB_USBDP T3011
CB_USBDM T3012
R3008 100KOhm
+VCCCB
VPPEN1 VPPEN0 VCC3EN# VCC5EN#
AVPP1 AVPP0 VCC3_EN# VCC5_EN#
R3009 100KOhm
CCLKRUN#/IOIS16#
R3010 100KOhm
CB_HWSUSP#
D3000 1N4148W
CB_SD# 19
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 30 of 63

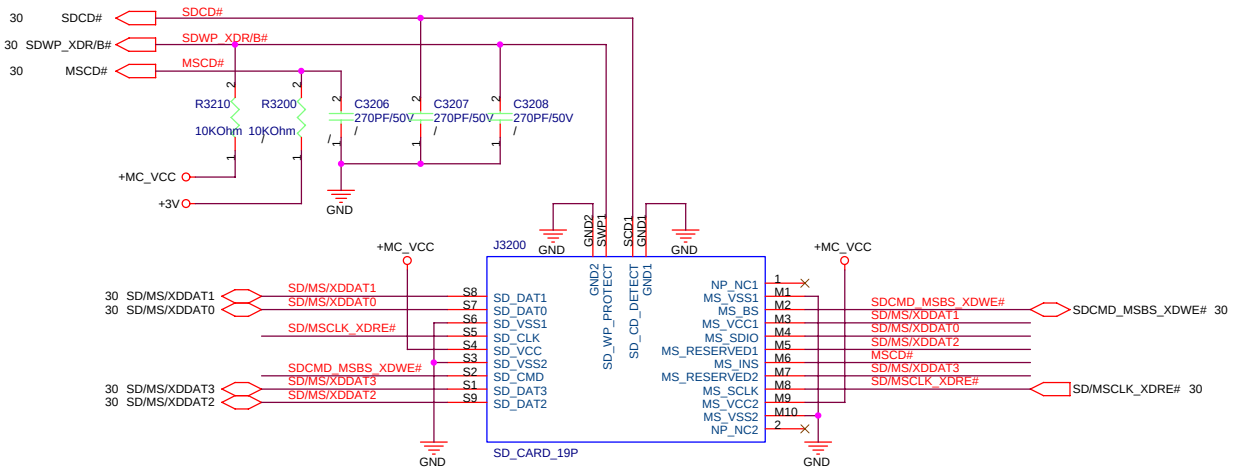


ASUSTeK COMPUTER INC	Title : CARDBUS SOCKET		
	Engineer: *Ping-Yen Tsai*		
Size: A3	Project Name: **A3F**		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 31 of 63		

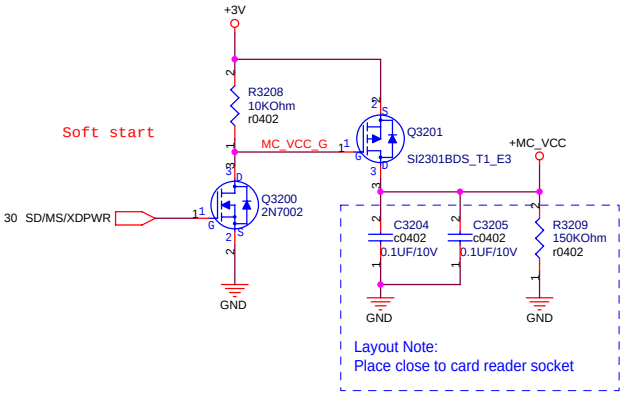


1. Close to R5C841
2. The area is as compact as possible,length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maxmium is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

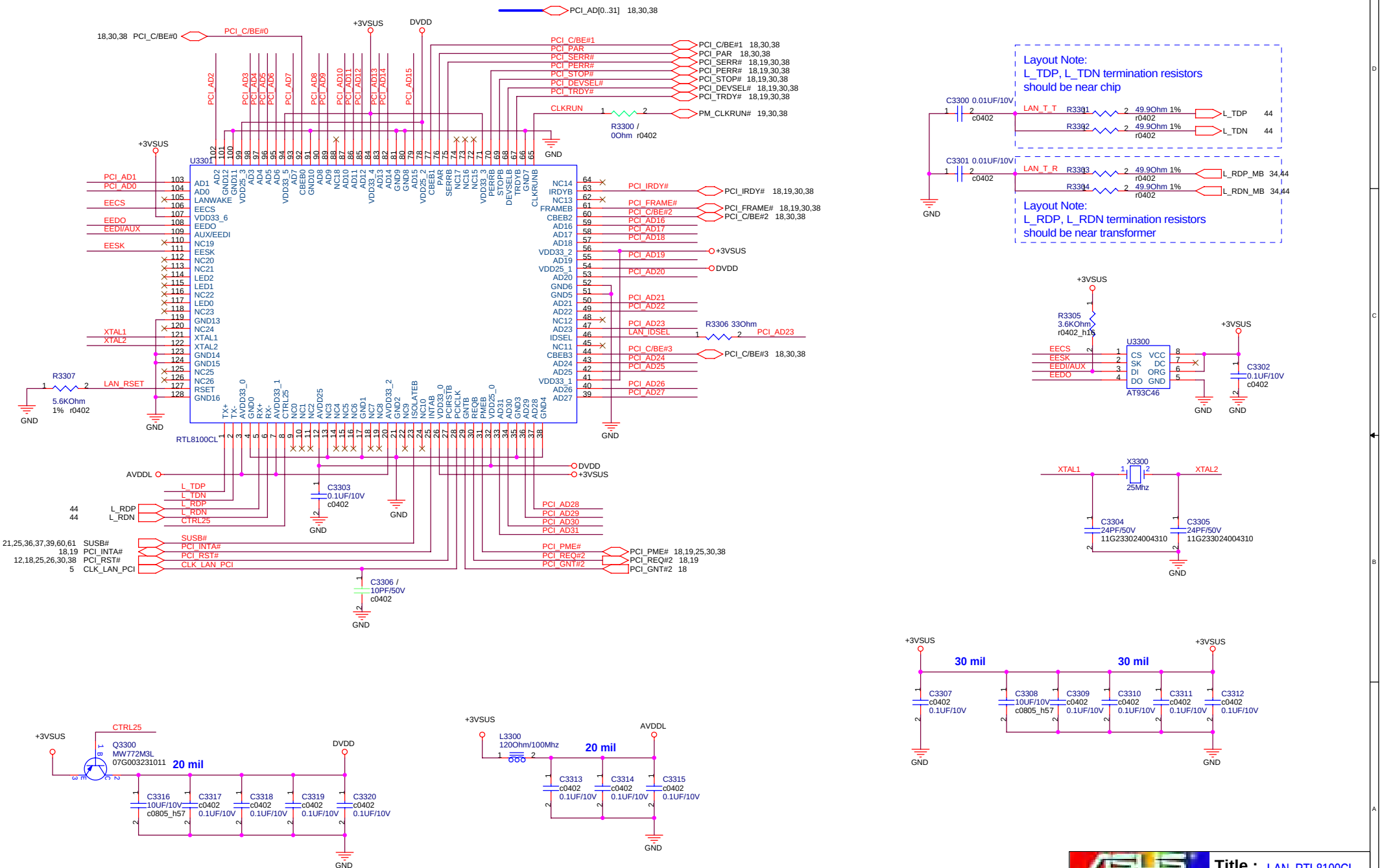




Layout: SHIELD GND

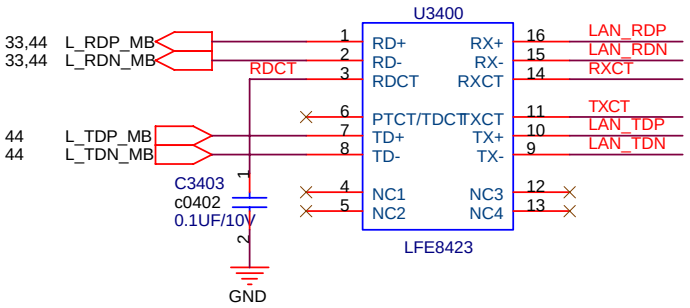


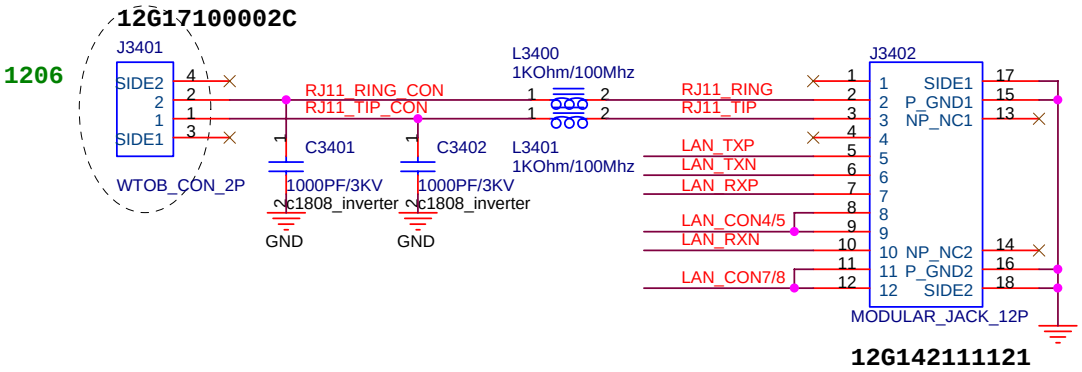
ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 32 of 63	



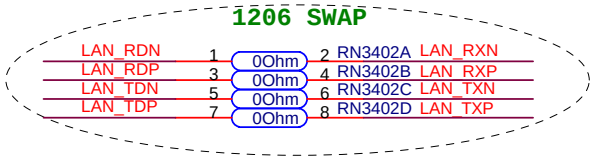
ASUSTek COMPUTER INC. NB6	Title : LAN_RTL8100CL	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 33 of 63	

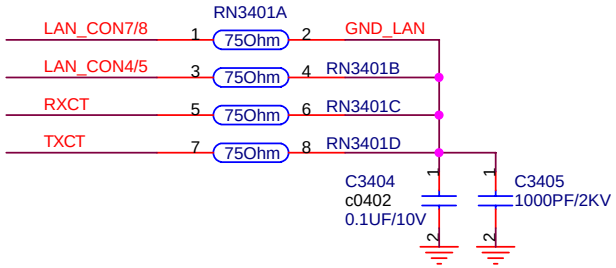
LAN PORT

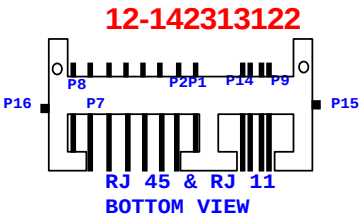




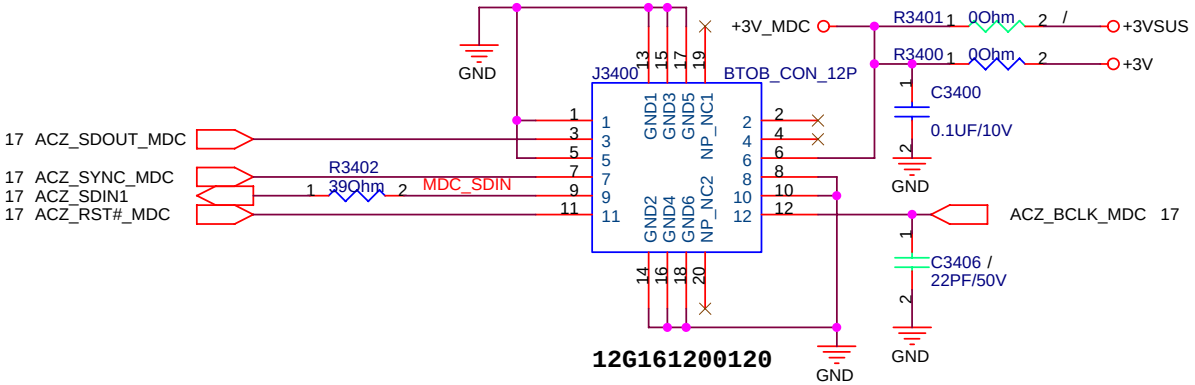
12G142111121





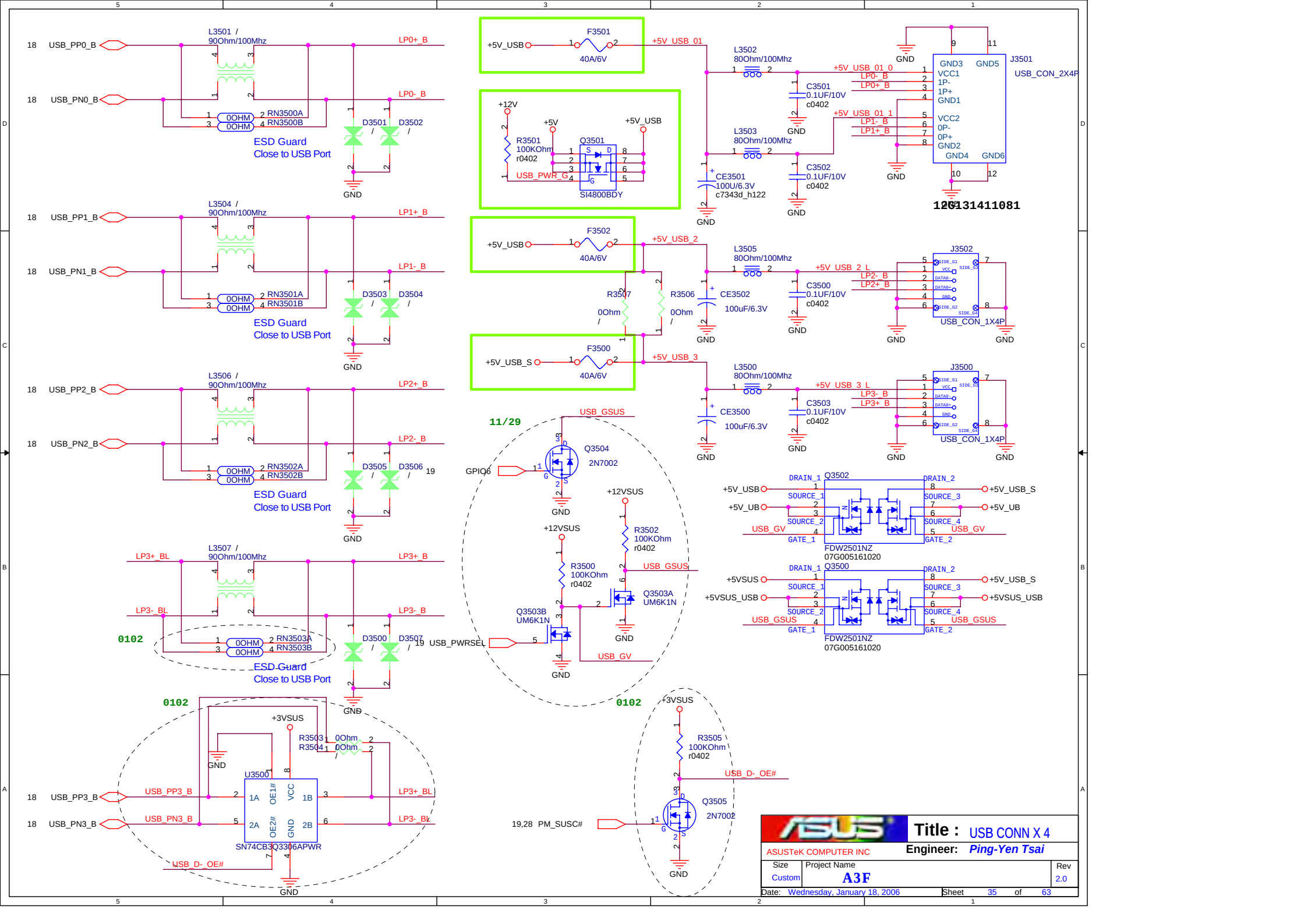


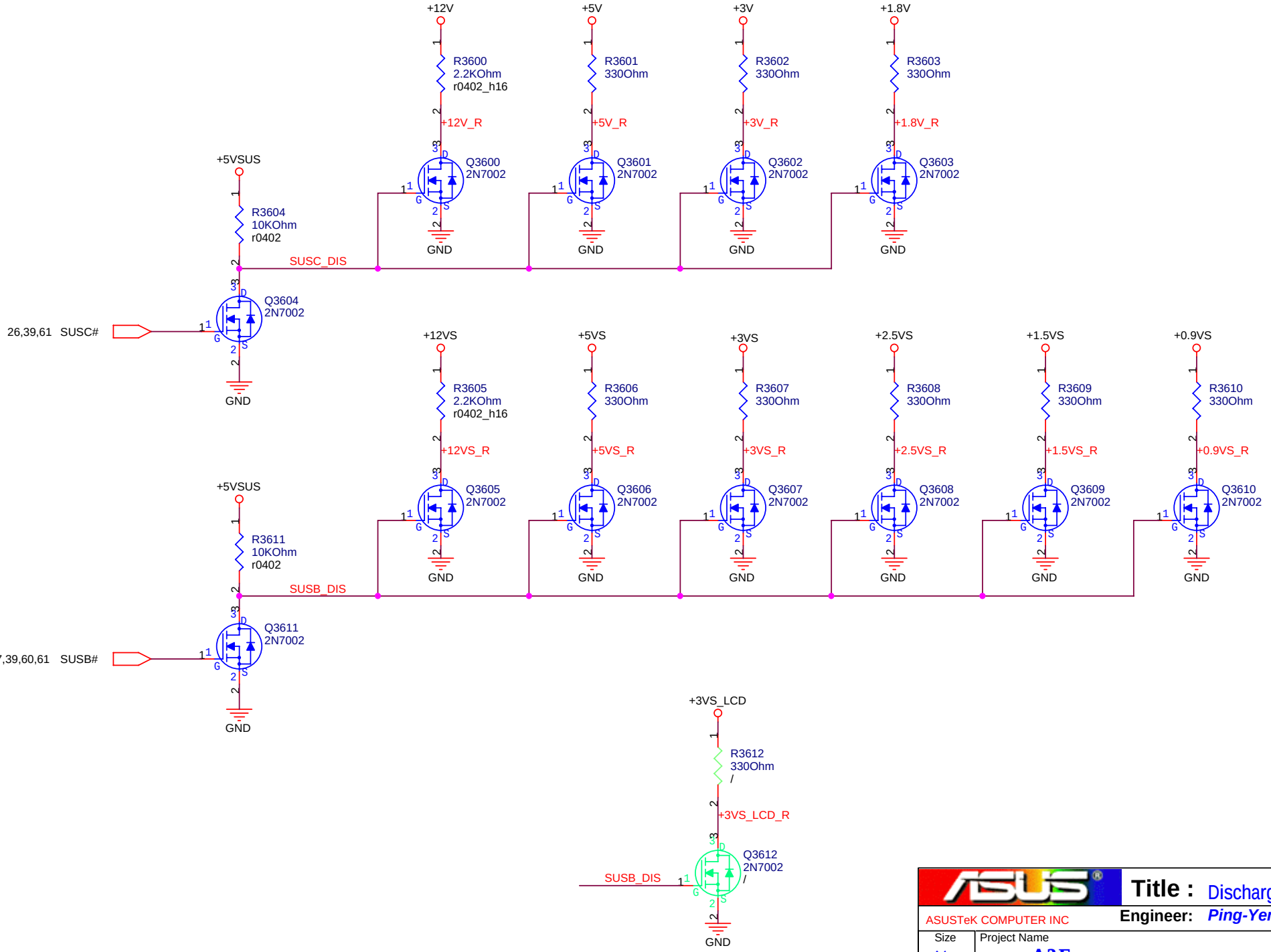
MDC Conn



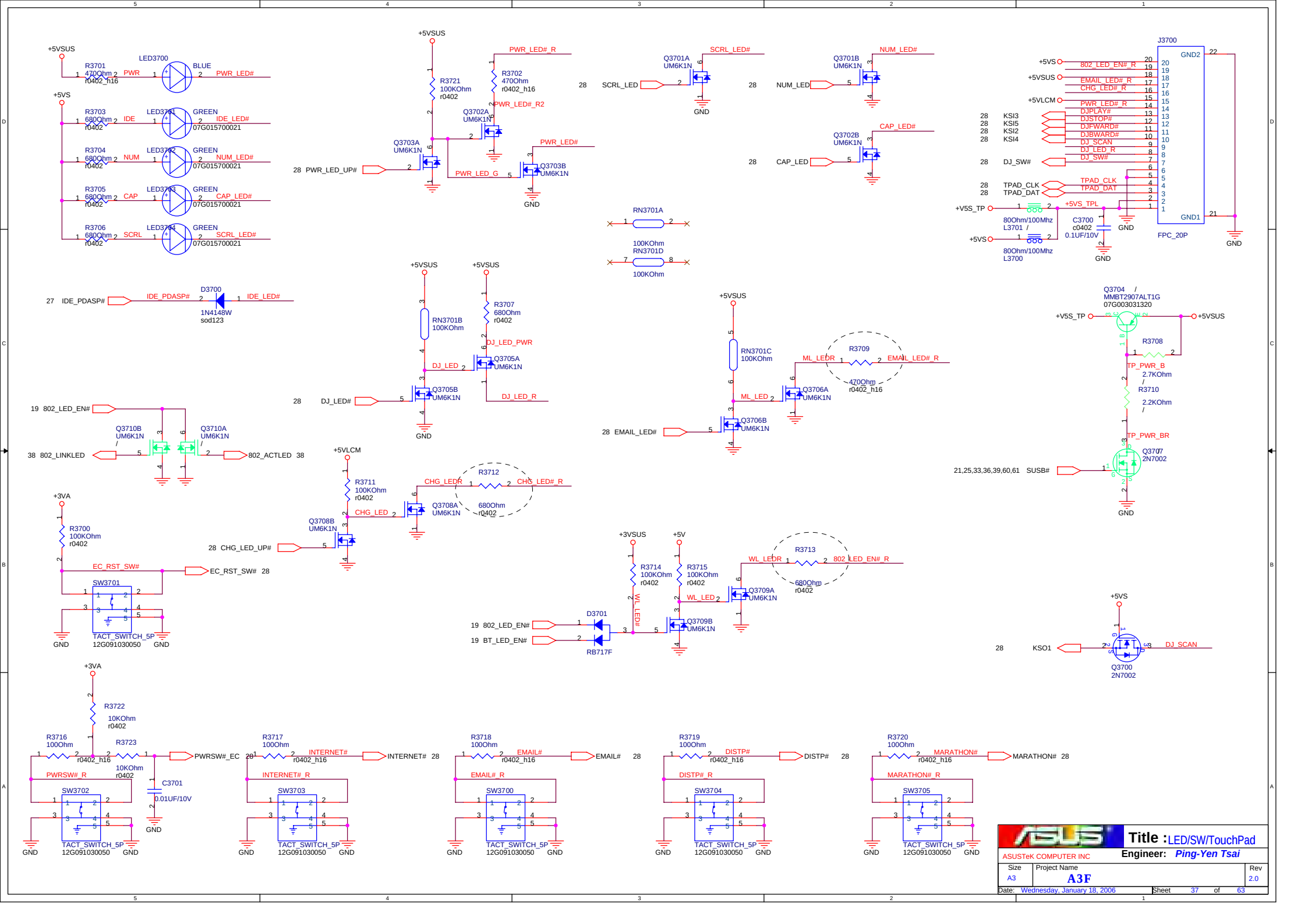
12G161200120

ASUSTeK COMPUTER INC	Title : RJ11/45 & MDC	
	Engineer: Ping-Yen Tsai	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 34 of 63	


18 USB_PP0_B
18 USB_PN0_B
L3501 / 90Ohm/100Mhz
RN3500A
RN3500B
0OHM
ESD Guard
Close to USB Port
LP0+_B
LP0-_B
D3501
D3502
GND
18 USB_PP1_B
18 USB_PN1_B
L3504 / 90Ohm/100Mhz
RN3501A
RN3501B
LP1+_B
LP1-_B
D3503
D3504
18 USB_PP2_B
18 USB_PN2_B
L3506 / 90Ohm/100Mhz
RN3502A
RN3502B
LP2+_B
LP2-_B
D3505
D3506
19
LP3+_BL
LP3-_BL
L3507 / 90Ohm/100Mhz
RN3503A
RN3503B
LP3+_B
LP3-_B
D3500
D3507
19 USB_PWRSEL
0102
0102
+3VSUS
R3503 0Ohm
R3504 0Ohm
U3500
SN74CB3Q3306APWR
1A
2A
1B
2B
OE1#
OE2#
VCC
GND
USB_PP3_B
USB_PN3_B
LP3+_BL
LP3-_BL
USB_D-_OE#
F3501
+5V_USB
40A/6V
+5V_USB_01
+12V
+5V
+5V_USB
R3501 100KOhm r0402
Q3501
SI4800BDY
USB_PWR_G
L3502 80Ohm/100Mhz
L3503 80Ohm/100Mhz
C3501 0.1UF/10V c0402
C3502 0.1UF/10V c0402
CE3501 100U/6.3V c7343d_h122
+5V_USB_01_0
+5V_USB_01_1
LP0-_B
LP0+_B
LP1-_B
LP1+_B
J3501
USB_CON_2X4P
GND3
GND5
VCC1
1P-
1P+
GND1
VCC2
0P-
0P+
GND2
GND4
GND6
1206131411081
F3502
+5V_USB_2
R3507 0Ohm
R3506 0Ohm
CE3502 100uF/6.3V
L3505 80Ohm/100Mhz
C3500 0.1UF/10V c0402
+5V_USB_2_L
LP2-_B
LP2+_B
J3502
USB_CON_1X4P
F3500
+5V_USB_S
+5V_USB_3
CE3500 100uF/6.3V
L3500 80Ohm/100Mhz
C3503 0.1UF/10V c0402
+5V_USB_3_L
LP3-_B
LP3+_B
J3500
USB_CON_1X4P
11/29
USB_GSUS
Q3504
2N7002
GPIO6
+12VSUS
R3502 100KOhm r0402
R3500 100KOhm r0402
Q3503A UM6K1N
Q3503B UM6K1N
USB_GV
Q3502
+5V_USB_S
+5V_UB
FDW2501NZ
07G005161020
Q3500
+5VSUS
+5VSUS_USB
R3505 100KOhm r0402
USB_D-_OE#
Q3505
2N7002
19,28 PM_SUSC#
ASUSTeK COMPUTER INC
Title : USB CONN X 4
Engineer: Ping-Yen Tsai
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 35 of 63



ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 36 of 63	



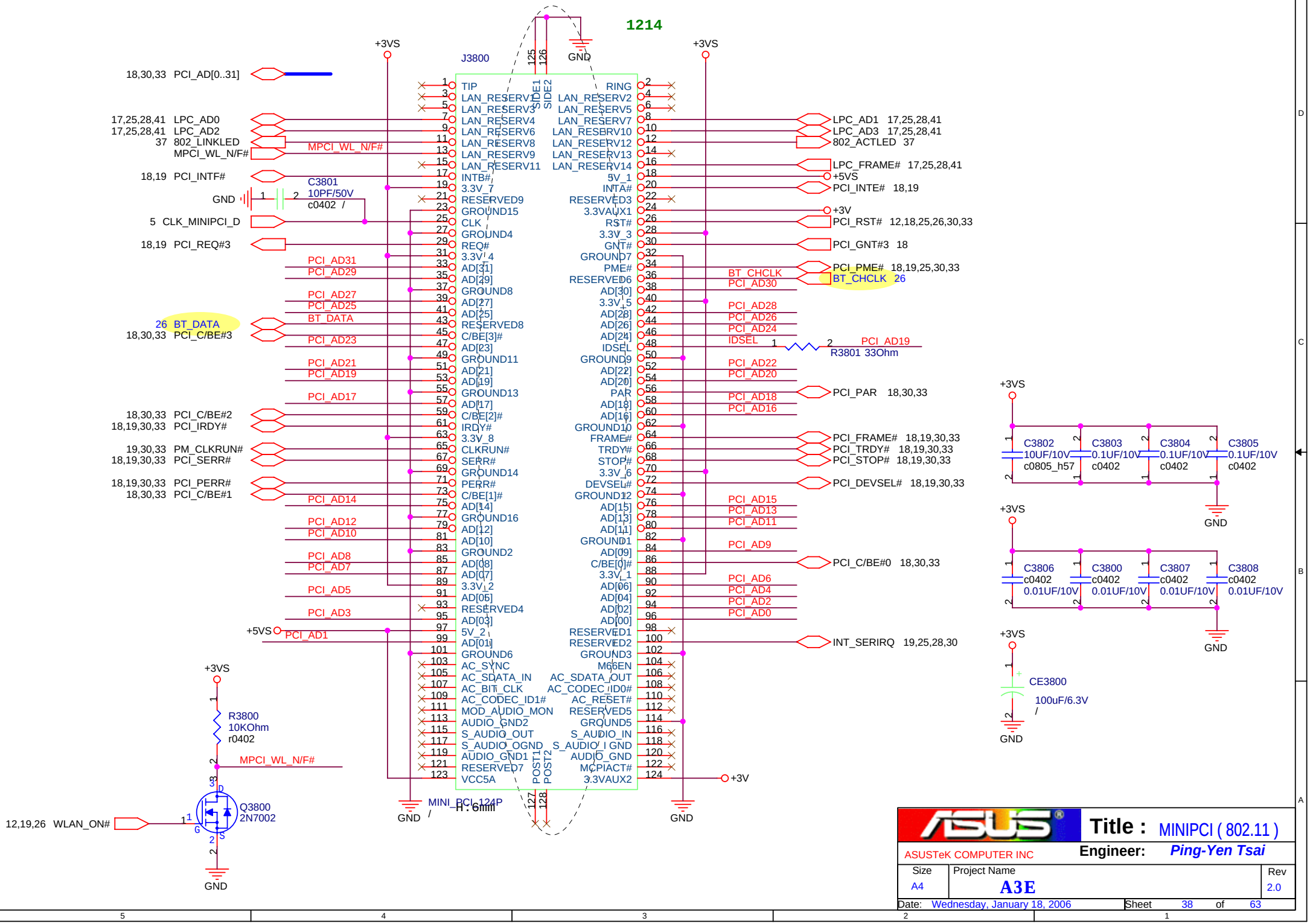
ASUSTeK COMPUTER INC

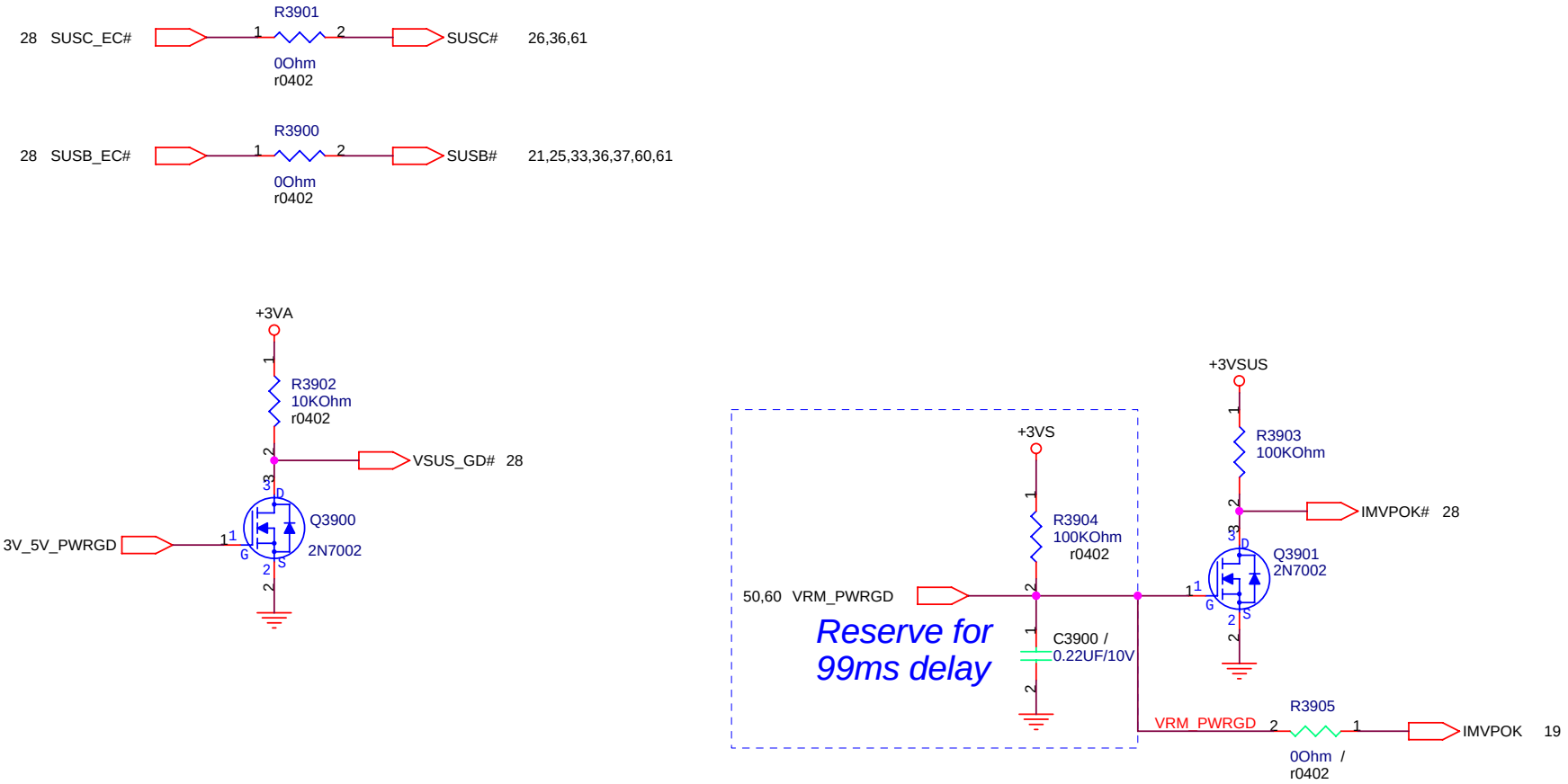
Title : LED/SW/TouchPad

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	**A3F**	2.0

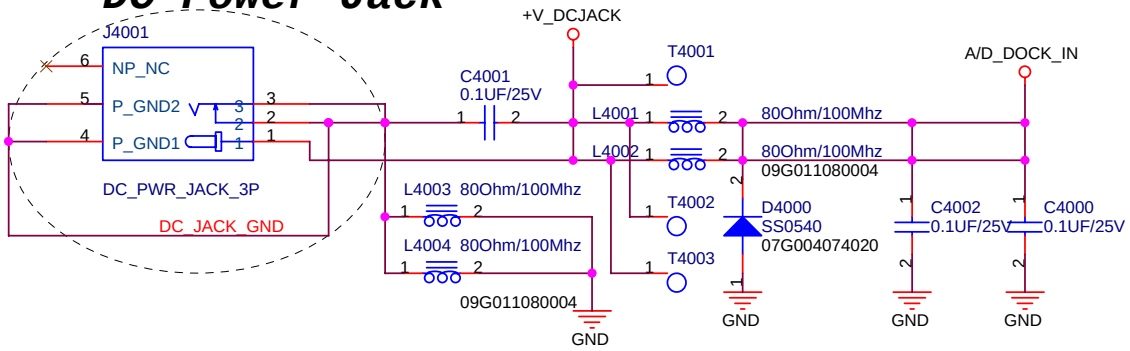
Date: Wednesday, January 18, 2006 Sheet 37 of 63

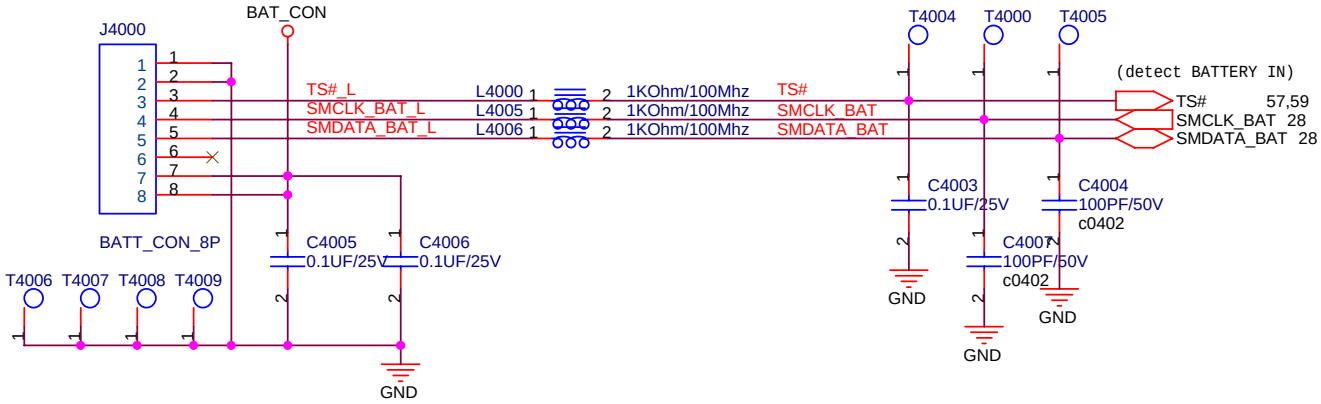

1214
J3800
MINI_PCI_124P
H: 6mm
18,30,33 PCI_AD[0..31]
17,25,28,41 LPC_AD0
17,25,28,41 LPC_AD2
37 802_LINKLED
MPCI_WL_N/F#
18,19 PCI_INTF#
GND
C3801
10PF/50V
c0402 /
5 CLK_MINIPCI_D
18,19 PCI_REQ#3
PCI_AD31
PCI_AD29
PCI_AD27
PCI_AD25
26 BT_DATA
18,30,33 PCI_C/BE#3
PCI_AD23
PCI_AD21
PCI_AD19
PCI_AD17
18,30,33 PCI_C/BE#2
18,19,30,33 PCI_IRDY#
19,30,33 PM_CLKRUN#
18,19,30,33 PCI_SERR#
18,19,30,33 PCI_PERR#
18,30,33 PCI_C/BE#1
PCI_AD14
PCI_AD12
PCI_AD10
PCI_AD8
PCI_AD7
PCI_AD5
PCI_AD3
+5VS
PCI_AD1
+3VS
R3800
10KOhm
r0402
MPCI_WL_N/F#
Q3800
2N7002
12,19,26 WLAN_ON#
GND
TIP
LAN_RESERV1
LAN_RESERV3
LAN_RESERV4
LAN_RESERV6
LAN_RESERV8
LAN_RESERV9
LAN_RESERV11
INTB#
3.3V_7
RESERVED9
GROUND15
CLK
GROUND4
REQ#
3.3V_4
AD[31]
AD[29]
GROUND8
AD[27]
AD[25]
RESERVED8
C/BE[3]#
AD[23]
GROUND11
AD[21]
AD[19]
GROUND13
AD[17]
C/BE[2]#
IRDY#
3.3V_8
CLKRUN#
SERR#
GROUND14
PERR#
C/BE[1]#
AD[14]
GROUND16
AD[12]
AD[10]
GROUND2
AD[08]
AD[07]
3.3V_2
AD[05]
RESERVED4
AD[03]
5V_2
AD[01]
GROUND6
AC_SYNC
AC_SDATA_IN
AC_BIT_CLK
AC_CODEC_ID1#
MOD_AUDIO_MON
AUDIO_GND2
S_AUDIO_OUT
S_AUDIO_OGND
AUDIO_GND1
RESERVED7
VCC5A
SIDE1
SIDE2
POST1
POST2
RING
LAN_RESERV2
LAN_RESERV5
LAN_RESERV7
LAN_RESERV10
LAN_RESERV12
LAN_RESERV13
LAN_RESERV14
5V_1
INTA#
RESERVED3
3.3VAUX1
RST#
3.3V_3
GNT#
GROUND7
PME#
RESERVED6
AD[30]
3.3V_5
AD[28]
AD[26]
AD[24]
IDSEL
GROUND9
AD[22]
AD[20]
PAR
AD[18]
AD[16]
GROUND10
FRAME#
TRDY#
STOP#
3.3V_6
DEVSEL#
GROUND12
AD[15]
AD[13]
AD[11]
GROUND1
AD[09]
C/BE[0]#
3.3V_1
AD[06]
AD[04]
AD[02]
AD[00]
RESERVED1
RESERVED2
GROUND3
M66EN
AC_SDATA_OUT
AC_CODEC_ID0#
AC_RESET#
RESERVED5
GROUND5
S_AUDIO_IN
S_AUDIO_I GND
AUDIO_GND
MCPIACT#
3.3VAUX2
LPC_AD1 17,25,28,41
LPC_AD3 17,25,28,41
802_ACTLED 37
LPC_FRAME# 17,25,28,41
+5VS
PCI_INTE# 18,19
+3V
PCI_RST# 12,18,25,26,30,33
PCI_GNT#3 18
PCI_PME# 18,19,25,30,33
BT_CHCLK 26
BT_CHCLK
PCI_AD30
PCI_AD28
PCI_AD26
PCI_AD24
IDSEL
PCI_AD19
R3801 33Ohm
PCI_AD22
PCI_AD20
PCI_PAR 18,30,33
PCI_AD18
PCI_AD16
PCI_FRAME# 18,19,30,33
PCI_TRDY# 18,19,30,33
PCI_STOP# 18,19,30,33
PCI_DEVSEL# 18,19,30,33
PCI_AD15
PCI_AD13
PCI_AD11
PCI_AD9
PCI_C/BE#0 18,30,33
PCI_AD6
PCI_AD4
PCI_AD2
PCI_AD0
INT_SERIRQ 19,25,28,30
C3802
10UF/10V
c0805_h57
C3803
0.1UF/10V
c0402
C3804
0.1UF/10V
c0402
C3805
0.1UF/10V
c0402
C3806
c0402
0.01UF/10V
C3800
c0402
0.01UF/10V
C3807
c0402
0.01UF/10V
C3808
c0402
0.01UF/10V
CE3800
100uF/6.3V
/
Title : MINIPCI (802.11)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A4
Project Name A3E
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 38 of 63



ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 39 of 63	

DC Power Jack

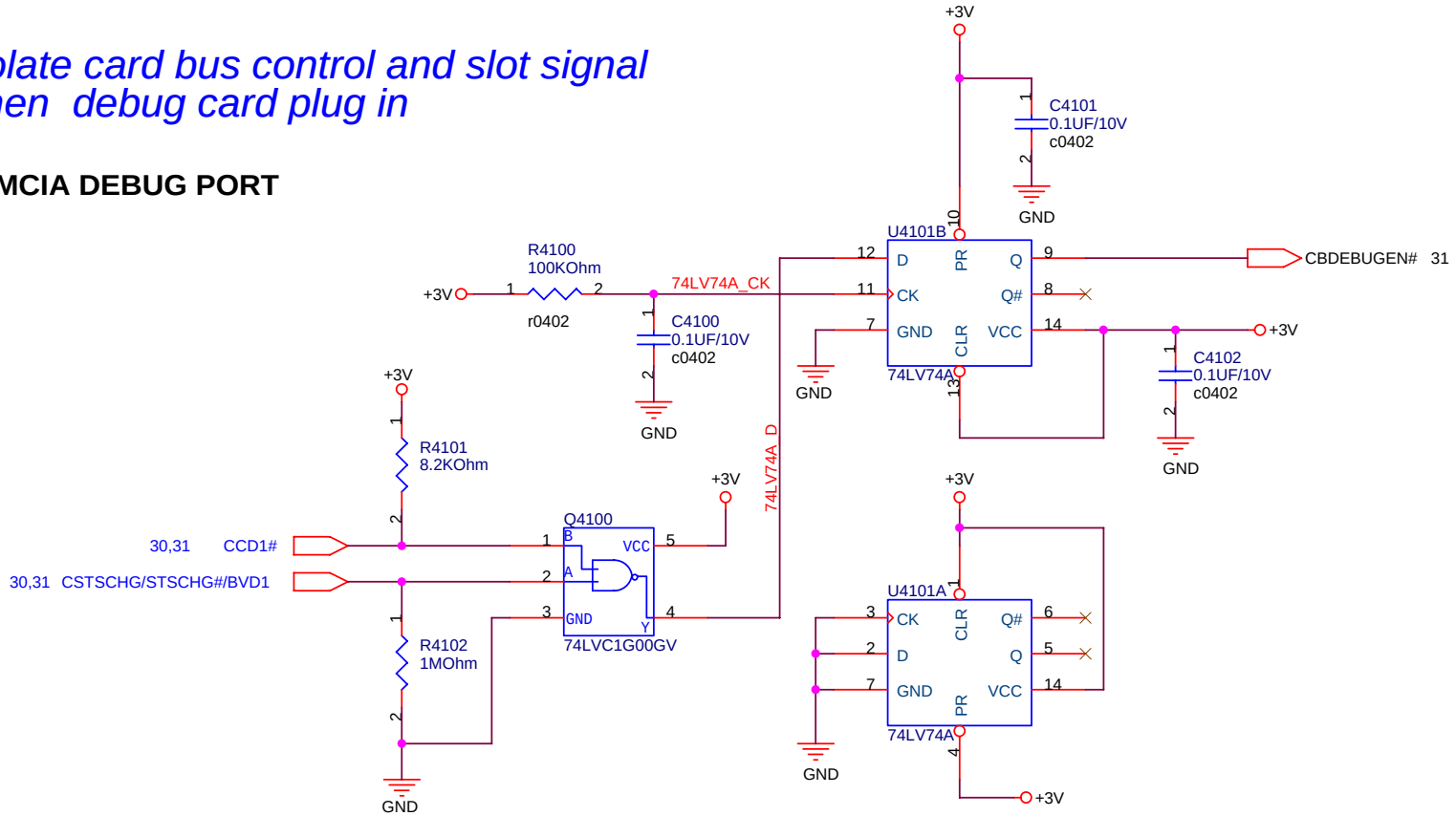


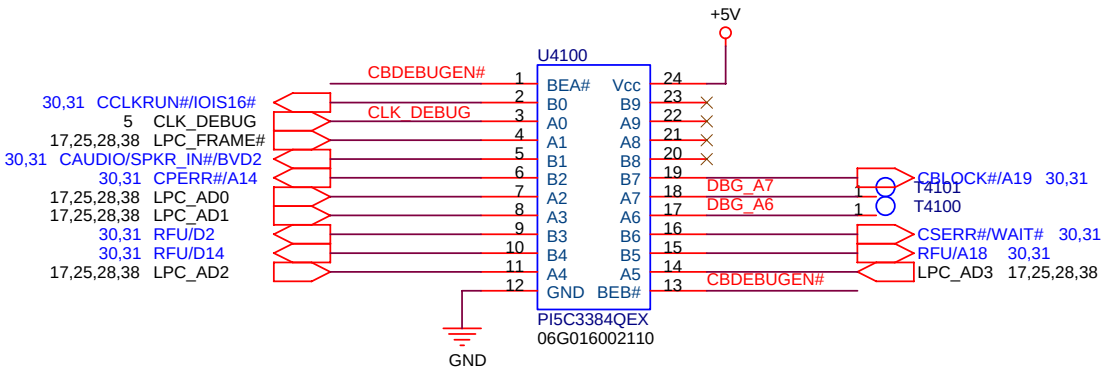


ASUSTeK COMPUTER INC	Title : DC/ BATT IN	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 40 of 63	

Isolate card bus control and slot signal when debug card plug in

PCMCIA DEBUG PORT





ASUSTeK COMPUTER INC	Title : PCMCIA Debug	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 41 of 63	

A

H4201
S315D91N /

H4203
S315D91N /

H4207
S315D91N /

H4208
S315D91N /

H4209
S315D91N /

H4210
S315D91N /

H4211
S315D91N /

H4212
S315D91N /

H4213
S315D91N /

H4215
S315D91N /

B

H4214
S295D91N /

H4216
S295D91N /

H_Calistoga

H4225
A40M20-50
13GN7K10M340

H4231

L4E_1A
13GN7510M270

H4228
A40M20-50

H4226

L4E_1A

H4223

L4E_1A

E

H4232
C197D91 /

H4233
C197D91 /

C

H4235
2DRILL_D79N_D91N_1 /

D

H4234
2DRILL_D79N_D91N /

U4202
EMI_SPRING_PAD

I_CPU

H4202
C268D138 /

H4204
C268D138 /

H4205
C268D138 /

H4206
C268D138 /

GND

G_MDC

H4230

L4E_1A

H4229

L4E_1A

J

H4224
CT197RB173X268D91 /

H4227
CT197RB173X268D91 /

For EMI

U4200
smd591x197

U4201
smd591x197

+VCCP_GMCH

C4202
0.1UF/10V /

C4203
0.1UF/10V /

+1.5VS

+3VS

C4200
0.1UF/10V /

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: Ping-Yen Tsai	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 42 of 63	

R1.1

11/14 1. Change resistor number from R1 to R1401
2. Change R1704 value from 10K to 330K
3. Add U2202 C D E F
4. Change C2511 value from 0.1uF to 0.047uF(11G232147316360)
5. Change C2510, C2514 and C2515 value from 0.1uF to 0.33uF(11G232333436030)

11/29 1. Remove R409
2. USB port (J3500) power control on shutdown of AC mode
3. Change U2202 power source form "+3VS" to "+3V" to solve pop noise
4. Add D2202 1N 4148W P/N 07G001001612 to solve pop noise when power off
5. Remove R2201 and mount R2203 to change Gain Setting

12/1 1. Change component D2103 DAP202K to 1N4148W P/N 07G001001612
2. Add Components 10K Ohm & 1N4148W P/N 07G001001612 and connect U2100 pin 30
3. Change J1500,U900,U2502,U3400,H4225,H4226,H4228,H4229,H4230 ,H4223,H4231,Q4400 to green part

12/2 1. Change Thermal Sensor to SO-8 MAX6657
2. USB4-->Camera, USB6-->PB

12/5 1.Change material CE1200, F3500, F3501, F3502
2. Add EC new function-->THRO_CPU
3. Change X3100, C3118, C3119 J3401 part number

12/7 1.Change J2500 footprint

12/9 1.Change R1202 value

R2.0

1/2 1. BOM Add R1943, Remove R1919
2. BOM Add D2105, R2125
3. BOM Add C2223
4. BOM Add R3505, Q3505, U3500
5. Schematics Add R3503, R3504 but don't mount
6. Schematics Add R4418~R4424 but don't mount

1/4 1. change R3709, R3712 & R3713 value

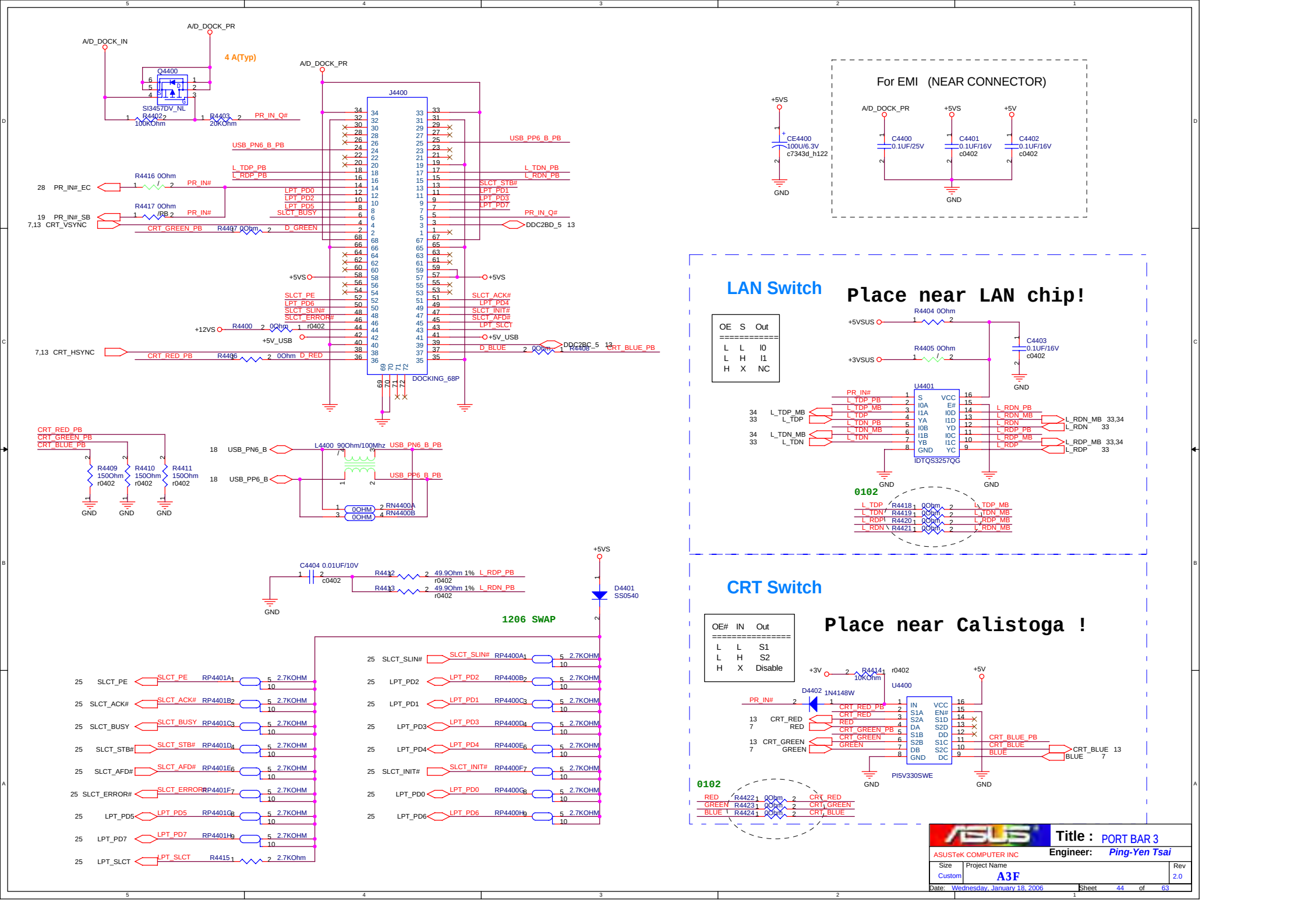
1/6 1. Add Power schematics & GPIO35 (Add R1944,R1945)

1/9 1. Remove JP3500, Add R3506, R3507

1/10 1. Add R415, BOM remove R408 Q403

1/11 1. Change C404 to 0.47uF
2. Change DJ JACK part number

ASUSTeK COMPUTER INC	Title : HISTORY	
	Engineer: *Ping-Yen Tsai*	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 43 of 63	


A/D_DOCK_PR
A/D_DOCK_IN
4 A(Typ)
Q4400
SI3457DV_NL
R4402 100KOhm
R4403 20KOhm
PR_IN_Q#
J4400
DOCKING_68P
USB_PN6_B_PB
USB_PP6_B_PB
L_TDP_PB
L_RDP_PB
L_TDN_PB
L_RDN_PB
SLCT_STB#
LPT_PD1
LPT_PD3
LPT_PD7
LPT_PD0
LPT_PD2
LPT_PD5
SLCT_BUSY
PR_IN#
PR_IN_Q#
DDC2BD_5
R4416 0Ohm
R4417 0Ohm
28 PR_IN#_EC
19 PR_IN#_SB
7,13 CRT_VSYNC
CRT_GREEN_PB
R4407 0Ohm
D_GREEN
+5VS
SLCT_PE
LPT_PD6
SLCT_SLIN#
SLCT_ERROR#
SLCT_ACK#
LPT_PD4
SLCT_INIT#
SLCT_AFD#
LPT_SLCT
+12VS
R4400 0Ohm
r0402
+5V_USB
D_BLUE
DDC2BC_5
R4408
CRT_BLUE_PB
7,13 CRT_HSYNC
CRT_RED_PB
R4406
0Ohm
D_RED
CRT_GREEN_PB
CRT_BLUE_PB
R4409 150Ohm r0402
R4410 150Ohm r0402
R4411 150Ohm r0402
GND
18 USB_PN6_B
18 USB_PP6_B
L4400 90Ohm/100Mhz
RN4400A 0OHM
RN4400B 0OHM
C4404 0.01UF/10V
c0402
R4412 49.9Ohm 1% L_RDP_PB
R4413 49.9Ohm 1% L_RDN_PB
r0402
D4401 SS0540
1206 SWAP
RP4401A
RP4401B
RP4401C
RP4401D
RP4401E
RP4401F
RP4401G
RP4401H
RP4400A
RP4400B
RP4400C
RP4400D
RP4400E
RP4400F
RP4400G
RP4400H
5 2.7KOHM 10
R4415 2.7Khm
For EMI (NEAR CONNECTOR)
CE4400 100U/6.3V c7343d_h122
C4400 0.1UF/25V
C4401 0.1UF/16V c0402
C4402 0.1UF/16V c0402
LAN Switch
OE S Out
L L I0
L H I1
H X NC
Place near LAN chip!
R4404 0Ohm
R4405 0Ohm
C4403 0.1UF/16V c0402
+5VSUS
+3VSUS
U4401
IDTQS3257QG
PR_IN#
L_TDP_MB
L_TDP
L_TDN_MB
L_TDN
L_RDN_PB
L_RDN_MB
L_RDN
L_RDP_PB
L_RDP_MB
L_RDP
L_RDN_MB 33,34
L_RDN 33
L_RDP_MB 33,34
L_RDP 33
0102
R4418 0Ohm
R4419 0Ohm
R4420 0Ohm
R4421 0Ohm
CRT Switch
OE# IN Out
L L S1
L H S2
H X Disable
Place near Calistoga !
+3V
R4414 10KOhm
D4402 1N4148W
U4400
PI5V330SWE
CRT_RED_PB
CRT_RED
RED
CRT_GREEN_PB
CRT_GREEN
GREEN
CRT_BLUE_PB
CRT_BLUE
BLUE
CRT_BLUE 13
BLUE 7
0102
R4422 0Ohm
R4423 0Ohm
R4424 0Ohm
Title : PORT BAR 3
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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Title	<Title>
Size A	Document Number A3F
Rev	2.0
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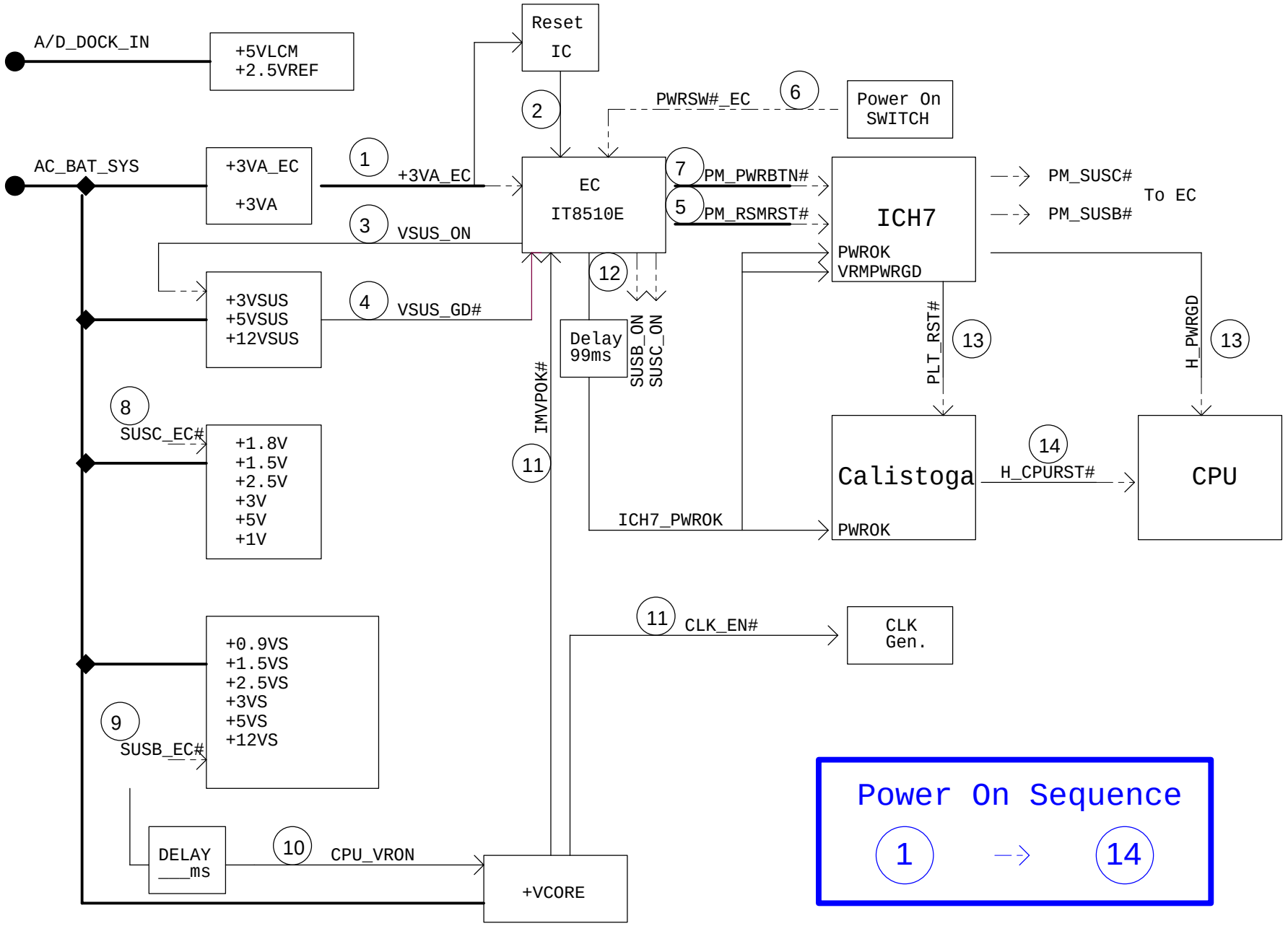
Sheet	45 of 63



ASUSTeK COMPUTER INC	Title : FLOWCHART	
	Engineer: Ping-Yen Tsai	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 46 of 63	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARD READER	AD17	1	D
CARDBUS	AD17	1	B
1394	AD17	1	C
MINIPCI (802.11a/b/g)	AD19	3	E,F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

ICH7-M GPIO	A3F	Note	Volt
GPIO08	EXTSMI#		+3VSUS
GPIO09	SATA_DET#0		+3VSUS
GPIO12	KBCSCI#		+3VSUS
GPIO13	SIO_SMI#		+3VSUS
GPIO14	PWRLED_1Hz		+3VSUS
GPIO15	802_LED_EN#		+3VSUS
GPIO25	CB_SD#		+3VSUS
GPIO27	WLAN_ON#		+3VSUS
GPIO28	BT_ON		+3VSUS
GPIO36	BT_LED_EN#		+3VS
GPIO37	PCB_ID0		+3VS
GPIO38	PCB_ID1		+3VS
GPIO39	PCB_ID2		+3VS

Title : SYSTEM RESOURCE

ASUSTeK COMPUTER INC Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 47 of 63

Title	<Title>
Size: CustomA3F	Document Number:
Rev: 2.0	
Date: Wednesday, January 18, 2006	Sheet 48 of 63

Title	<Title>
Size A	Document Number A3F
Rev	2.0
Date:	Wednesday, January 18, 2006
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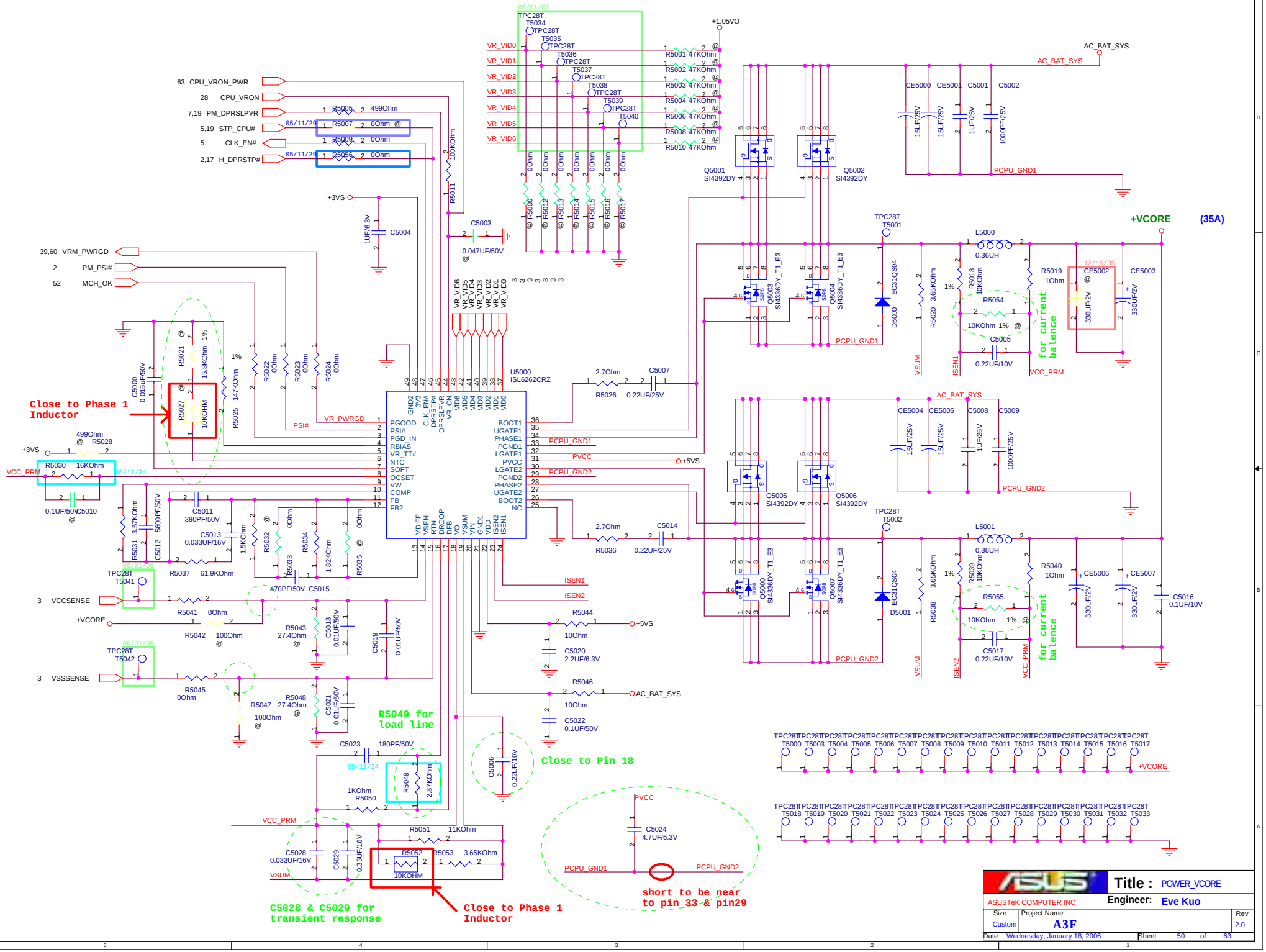
63 CPU_VRON_PWR
28 CPU_VRON
7,19 PM_DPRSLPVR
5,19 STP_CPU#
5 CLK_EN#
2,17 H_DPRSTP#
39,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
+1.05VO
+3VS
+5VS
+VCORE (35A)
AC_BAT_SYS
U5000
ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND1
VDD
ISEN2
ISEN1
VR_PWRGD
PCPU_GND1
PCPU_GND2
VCC_PRM
VCCSENSE
VSSSENSE
VSUM
Q5001 SI4392DY
Q5002 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5005 SI4392DY
Q5006 SI4392DY
Q5007 SI4336DY_T1_E3
Q5000 SI4336DY_T1_E3
D5000 EC31QS04
D5001 EC31QS04
L5000 0.36UH
L5001 0.36UH
Close to Phase 1 Inductor
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
for current balence
for current balence
C5028 & C5029 for transient response
short to be near to pin 33 & pin29
Title : POWER_VCORE
ASUSTeK COMPUTER INC
Engineer: Eve Kuo
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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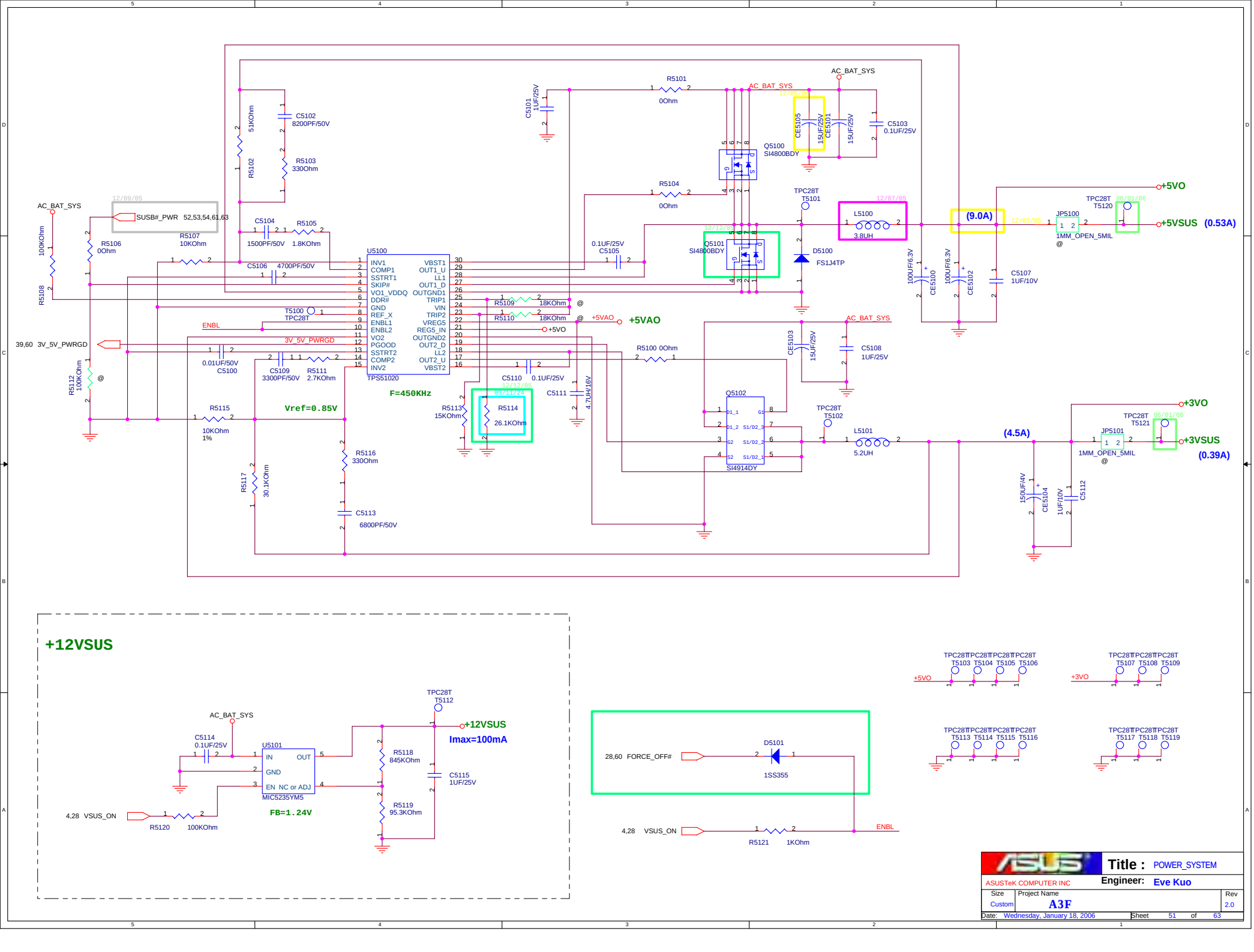


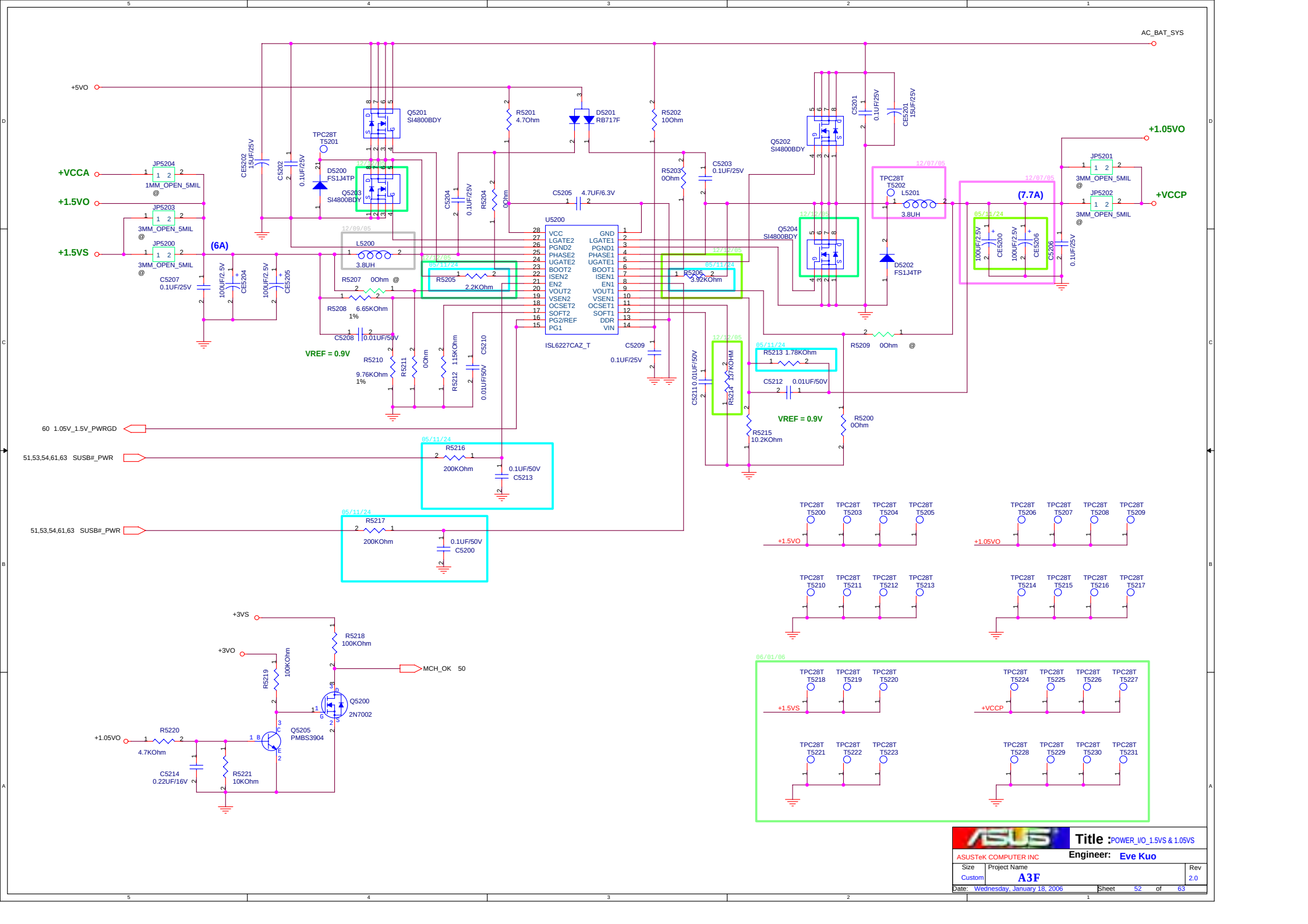
ASUSTeK COMPUTER INC

Title : POWER_SYSTEM

Engineer: Eve Kuo

Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 51 of 63


AC_BAT_SYS
+5VO
+VCCA
+1.5VO
+1.5VS
(6A)
JP5204
1MM_OPEN_5MIL
JP5203
3MM_OPEN_5MIL
JP5200
3MM_OPEN_5MIL
CE5202 15UF/25V
C5202 0.1UF/25V
TPC28T T5201
D5200 FS1J4TP
Q5201 SI4800BDY
Q5203 SI4800BDY
R5201 4.7Ohm
D5201 RB717F
R5202 10Ohm
R5203 0Ohm
C5203 0.1UF/25V
C5204 0.1UF/25V
R5204 0Ohm
C5205 4.7UF/6.3V
U5200
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
ISL6227CAZ_T
L5200 3.8UH
R5205 2.2KOhm
R5206 3.92KOhm
R5207 0Ohm @
R5208 6.65KOhm 1%
C5208 0.01UF/50V
VREF = 0.9V
R5210 9.76KOhm 1%
R5211 0Ohm
R5212 115KOhm
C5210 0.01UF/50V
C5209 0.1UF/25V
C5207 0.1UF/25V
CE5204 100UF/2.5V
CE5205 100UF/2.5V
Q5202 SI4800BDY
Q5204 SI4800BDY
C5201 0.1UF/25V
CE5201 15UF/25V
TPC28T T5202
L5201 3.8UH
D5202 FS1J4TP
(7.7A)
CE5200 100UF/2.5V
CE5206 100UF/2.5V
C5206 0.1UF/25V
+1.05VO
+VCCP
JP5201
JP5202
3MM_OPEN_5MIL
R5213 1.78KOhm
R5209 0Ohm @
C5212 0.01UF/50V
C5211 0.01UF/50V
R5214 127KOHM
R5215 10.2KOhm
R5200 0Ohm
VREF = 0.9V
60 1.05V_1.5V_PWRGD
51,53,54,61,63 SUSB#_PWR
R5216 200KOhm
C5213 0.1UF/50V
R5217 200KOhm
C5200 0.1UF/50V
+3VS
+3VO
R5218 100KOhm
R5219 100KOhm
MCH_OK 50
Q5200 2N7002
Q5205 PMBS3904
R5220 4.7KOhm
C5214 0.22UF/16V
R5221 10KOhm
TPC28T T5200
TPC28T T5203
TPC28T T5204
TPC28T T5205
TPC28T T5206
TPC28T T5207
TPC28T T5208
TPC28T T5209
TPC28T T5210
TPC28T T5211
TPC28T T5212
TPC28T T5213
TPC28T T5214
TPC28T T5215
TPC28T T5216
TPC28T T5217
TPC28T T5218
TPC28T T5219
TPC28T T5220
TPC28T T5221
TPC28T T5222
TPC28T T5223
TPC28T T5224
TPC28T T5225
TPC28T T5226
TPC28T T5227
TPC28T T5228
TPC28T T5229
TPC28T T5230
TPC28T T5231
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC
Engineer: Eve Kuo
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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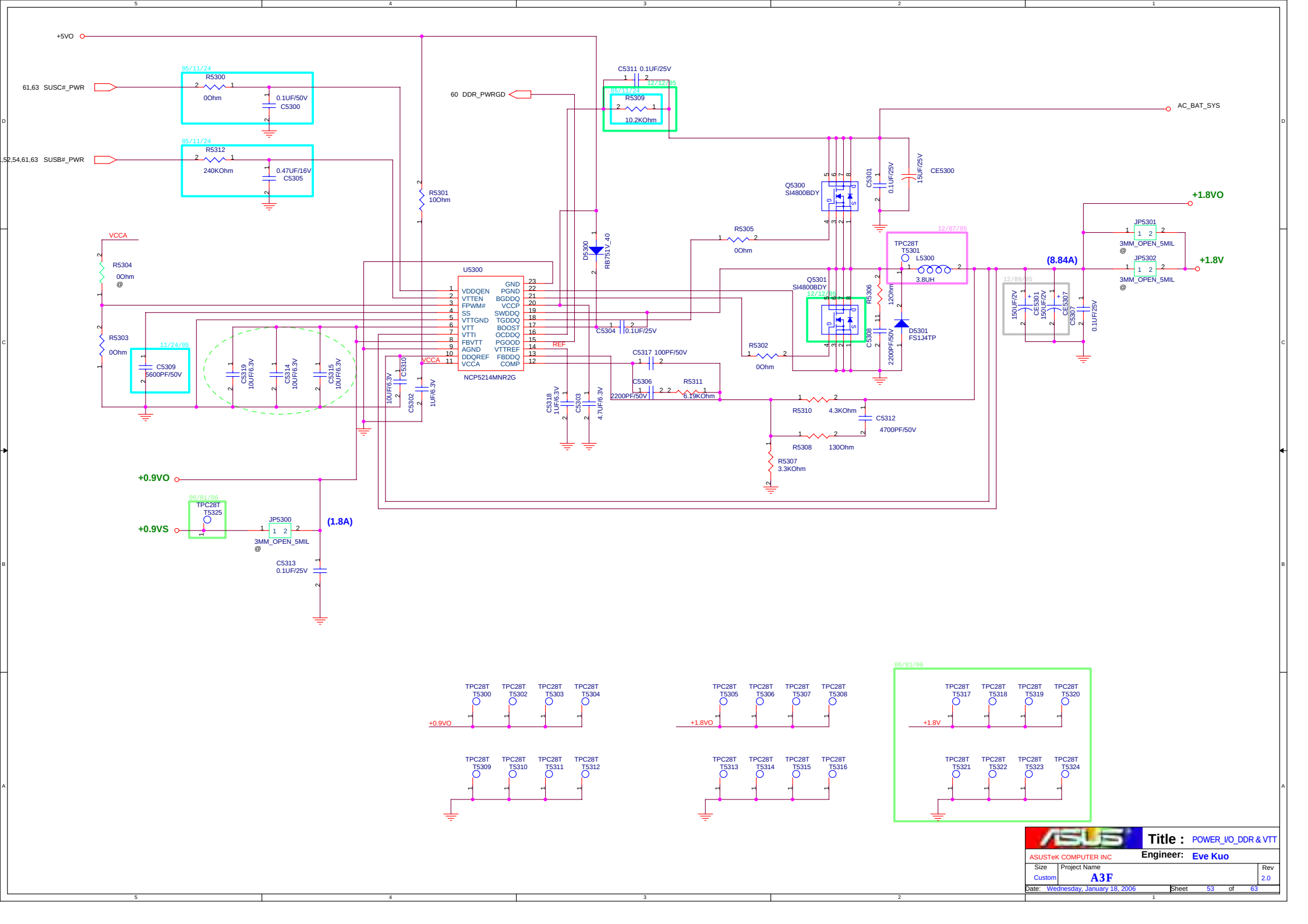
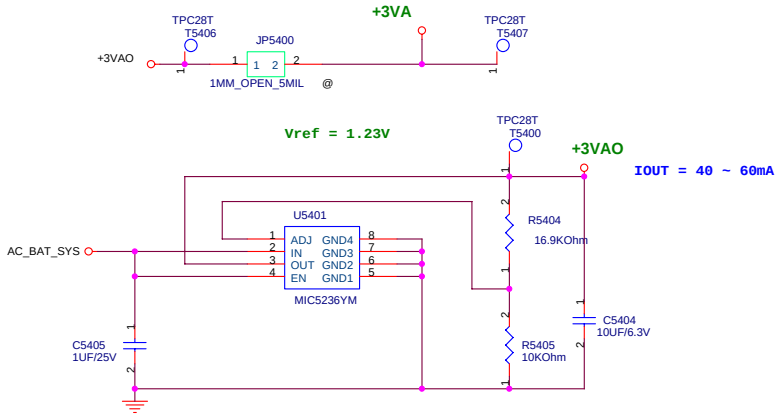
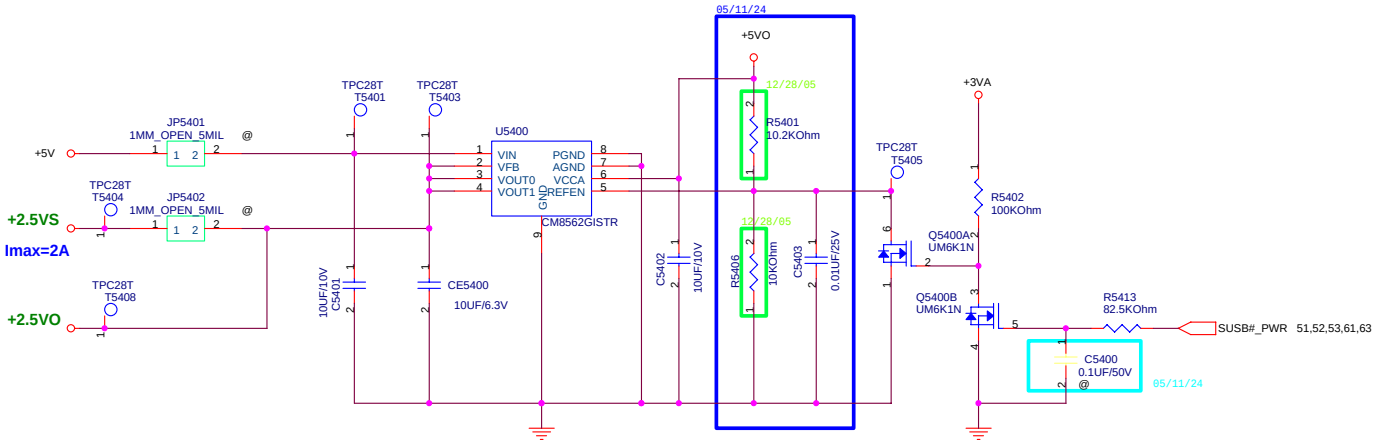


ASUSTeK COMPUTER INC	Title : POWER_I/O_DDR & VTT	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 53 of 63	

+3VA0



+2.5VS



ASUSTeK COMPUTER INC	Title : POWER_I/O_+3VA & +2.5VS	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 54 of 63	

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date

R2.0

Item	Before	After	Reason	Owner	Date

Title : N/A

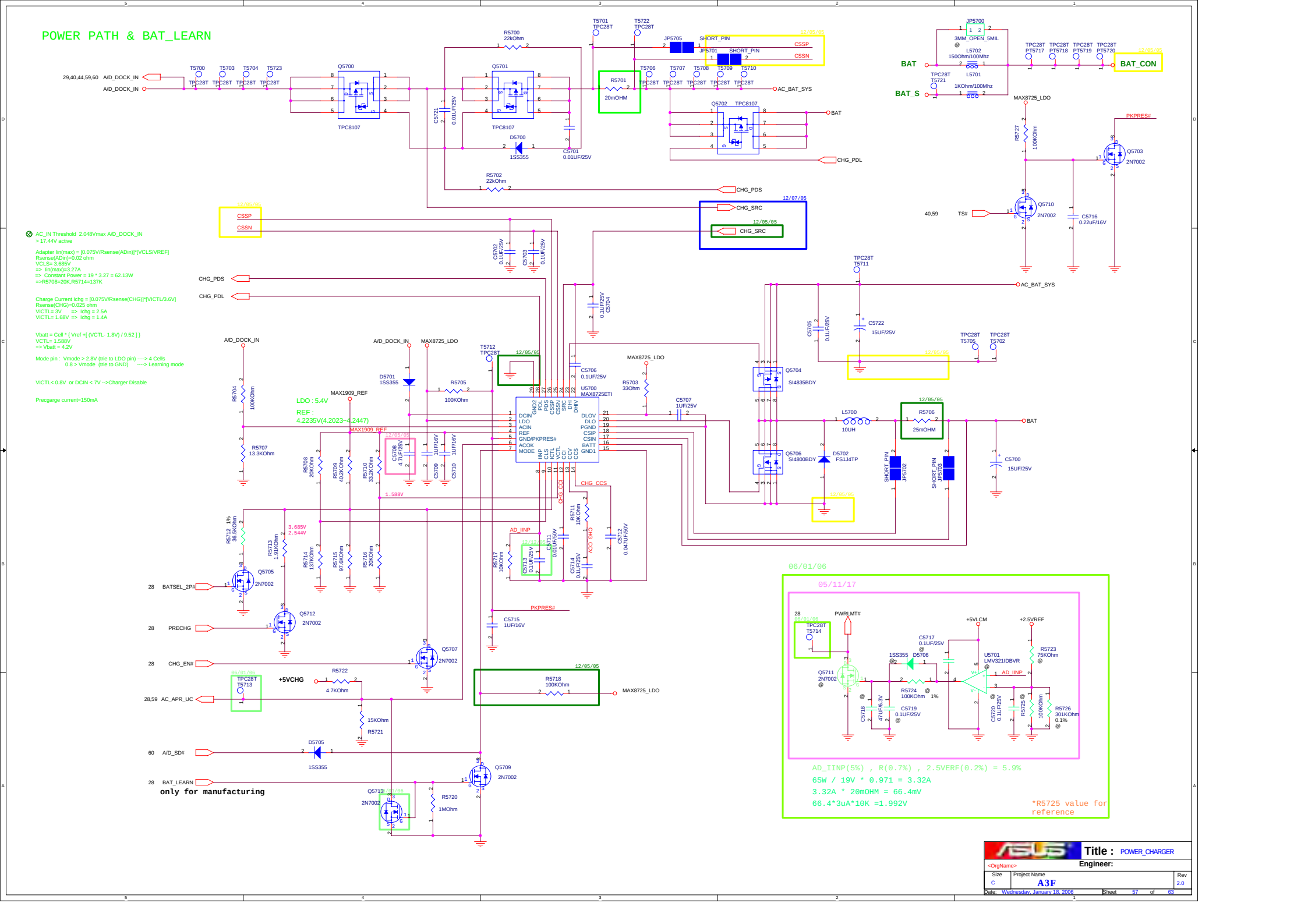
Engineer: Eve Kuo

ASUSTeK COMPUTER INC

Size	Project Name	Rev
C	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 56 of 63

POWER PATH & BAT_LEARN



Title : POWER_CHARGER			
<OrgName>	Engineer:		
Size: C	Project Name: A3F		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 57 of 63		

Title : N/A

Engineer: Eve Kuo

ASUSTeK COMPUTER INC

Size	Project Name	Rev
C	A3F	2.0

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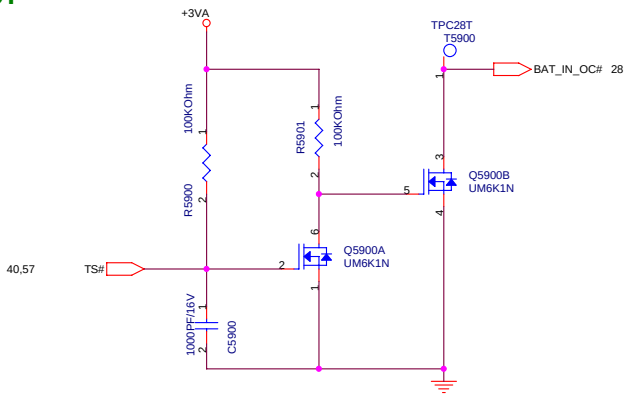
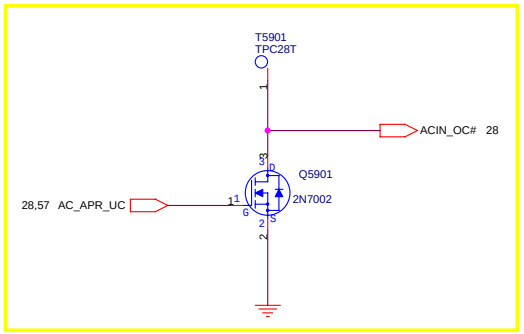
BATTERY IN DETECT

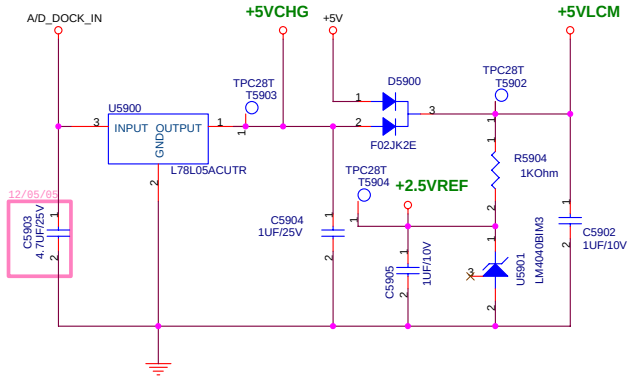


ADAPTER IN DETECT

05/11/07

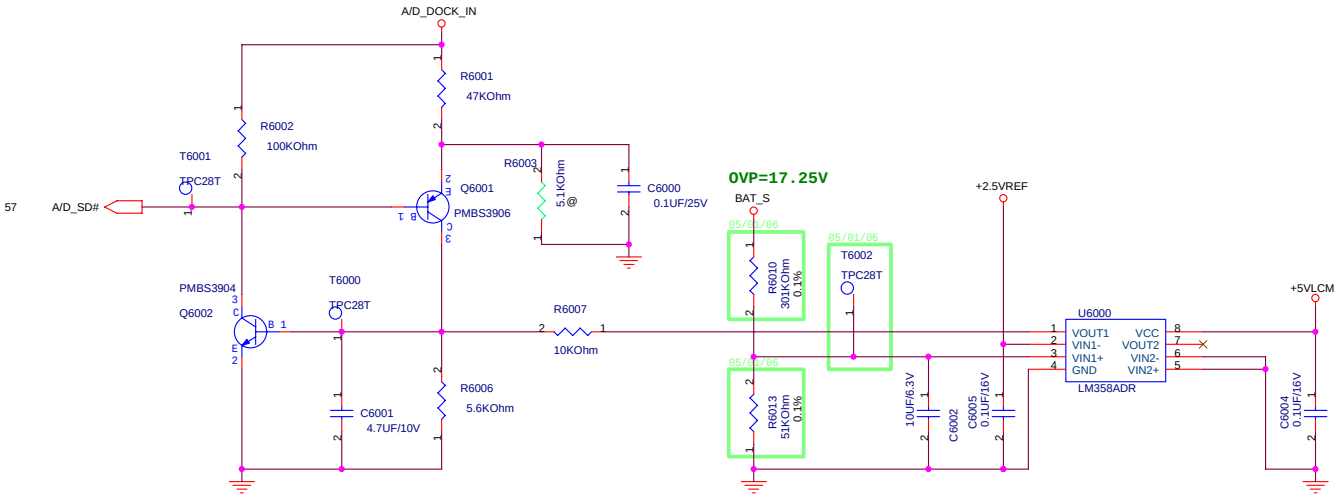


+5VLCM, +5VCHG & +2.5VREF

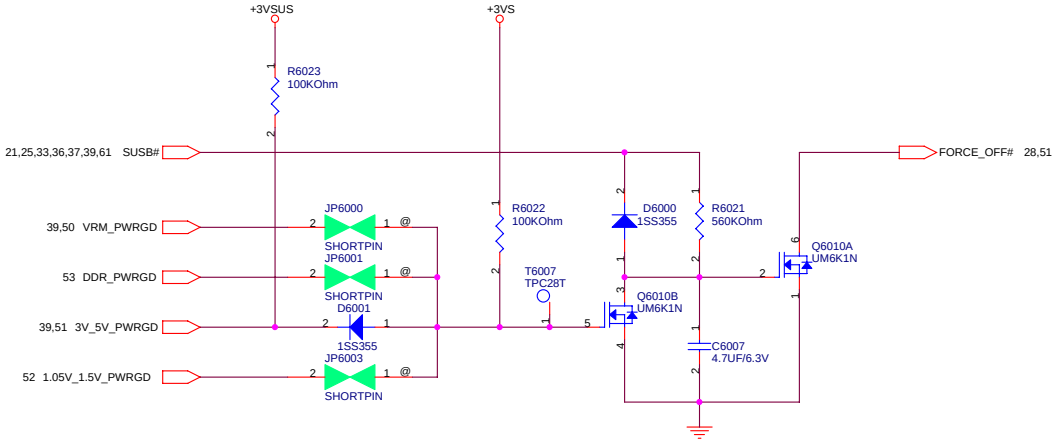


ASUSTeK COMPUTER INC	Title : POWER_DETECT	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 59 of 63	

BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER



TPC28T T6003 1 VRM_PWRGD
TPC28T T6004 1 DDR_PWRGD
TPC28T T6005 1 3V_5V_PWRGD
TPC28T T6006 1 1.05V_1.5V_PWRGD

ASUSTeK COMPUTER INC	Title : POWER_PROTECT	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
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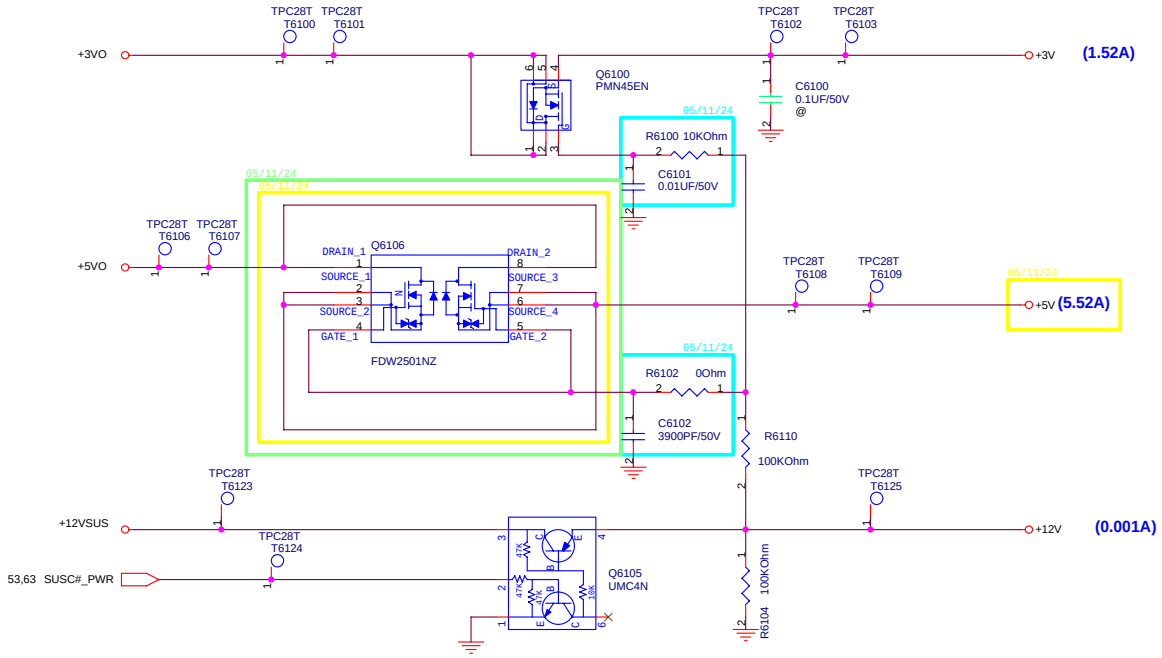
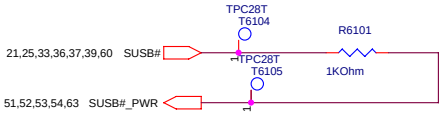
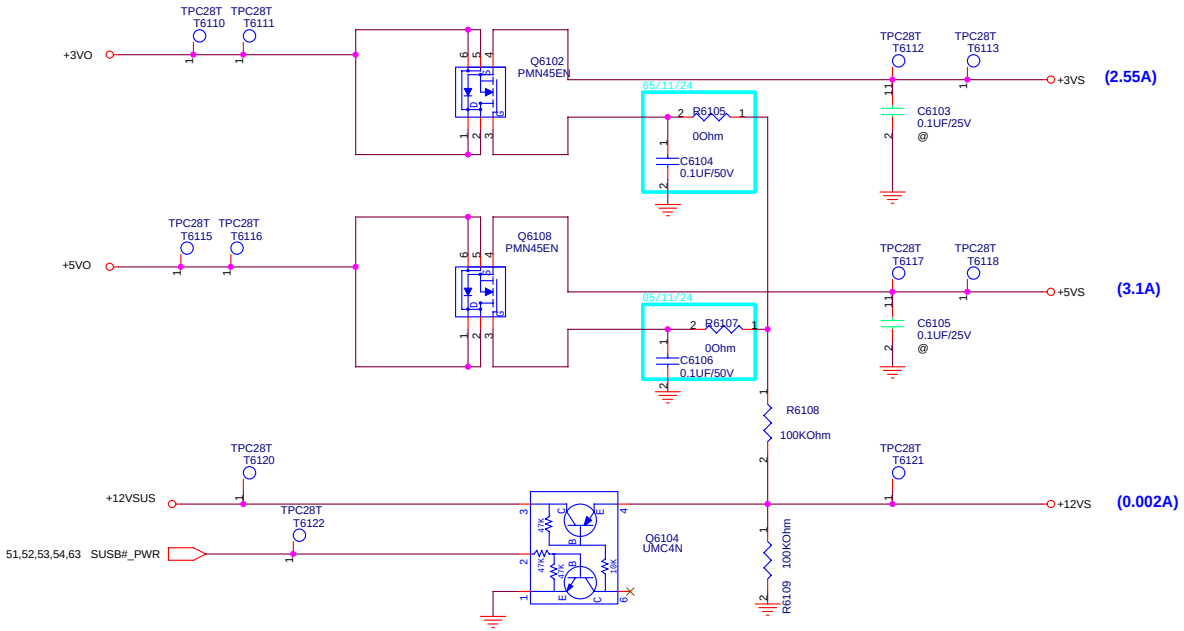
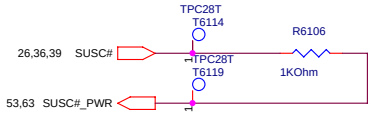
SUSC#_PWR POWER





SUSB#_PWR POWER





Title :	POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC	Engineer:	Eve Kuo
Size: Custom	Project Name: A3F	Rev: 2.0
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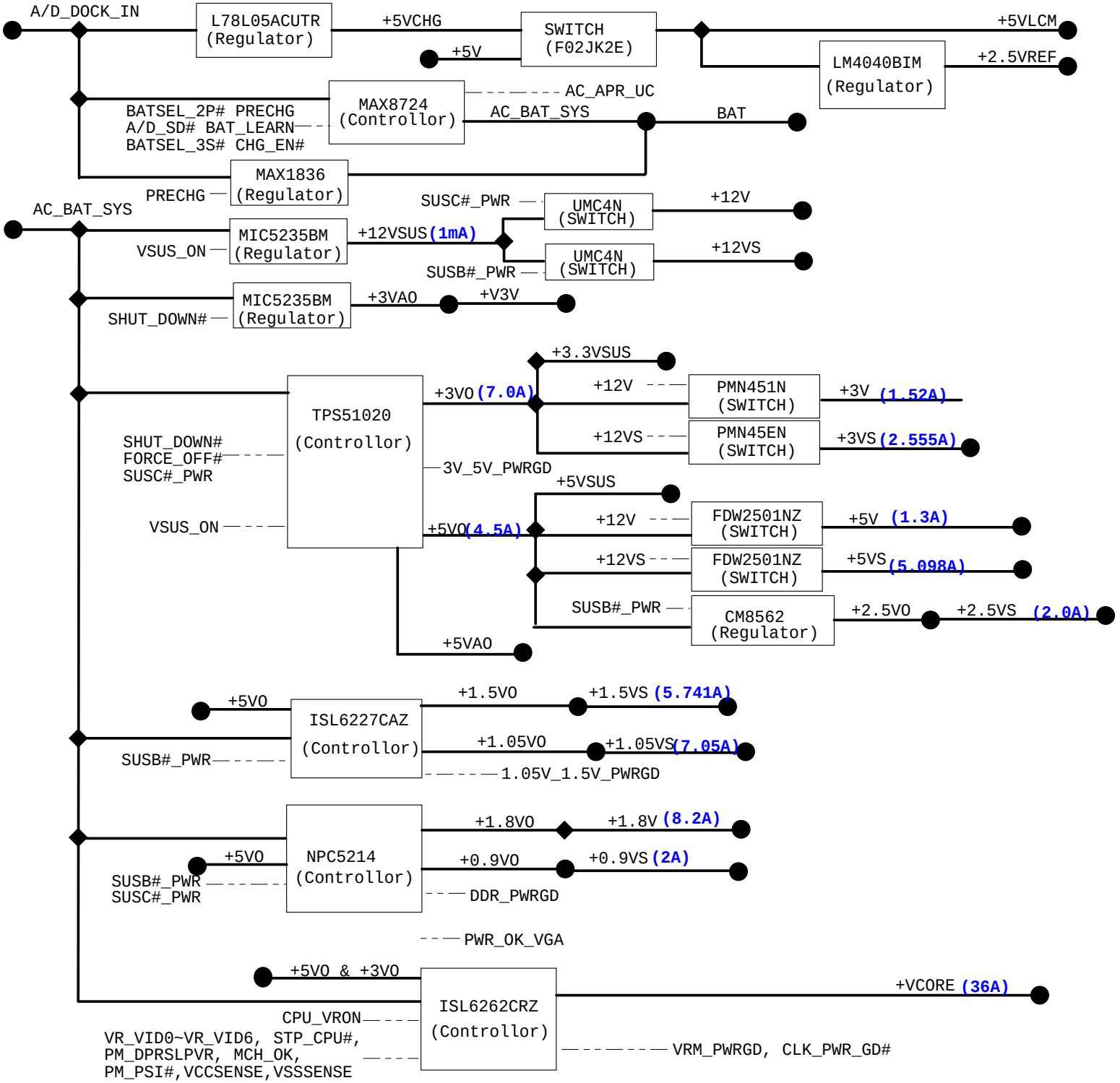

ASUSTeK COMPUTER INC	Title : POWER_FLOWCHART	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
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AC_BAT_SYS → AC_BAT_SYS 12,50,51,52,53,54,57

+3VA → +3VA 4,12,20,28,37,39,54,59

+5VO → +5VO 51,52,53,54,61

+3VO → +3VO 51,52,61

+3VSUS → +3VSUS 18,19,20,28,33,34,35,37,39,44,51,60

+5VSUS → +5VSUS 20,35,36,37,44,51

+3V → +3V 12,18,22,26,30,31,32,34,36,38,41,44,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

+12VSUS → +12VSUS 35,51,61

+12V → +12V 4,35,36,61

+12VS → +12VS 12,22,36,44,61

+5V → +5V 9,12,22,25,31,35,36,37,41,44,54,59,61

+5VS → +5VS 4,13,19,20,21,22,27,28,36,37,38,44,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,13,36,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,36,53

+0.9VS → +0.9VS 16,36,53

BAT → BAT 29,57

+5VCHG → +5VCHG 57,59

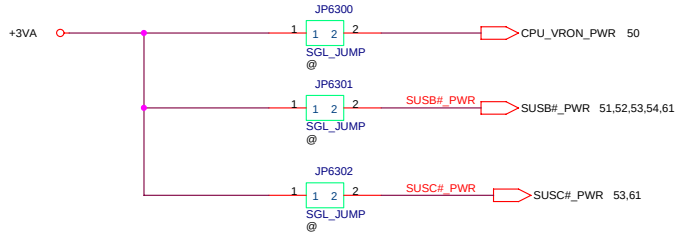
+5VLCM → +5VLCM 37,57,59,60

+2.5VREF → +2.5VREF 57,59,60

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 40,57

FOR POWER TEST



ASUSTeK COMPUTER INC	Title : POWER_SIGNAL		
	Engineer: Eve Kuo		
Size: Custom	Project Name: A3F		Rev: 2.0
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