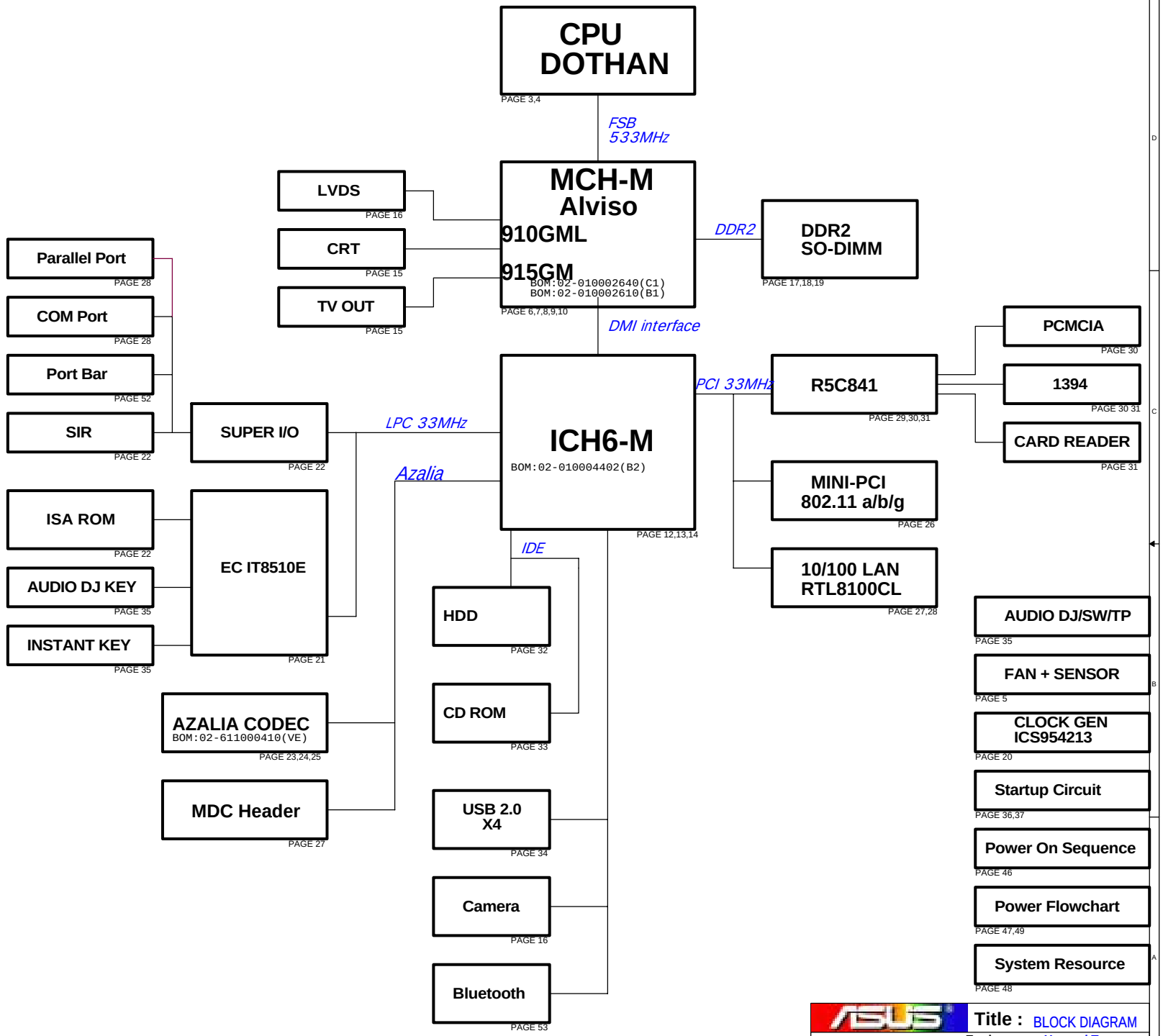
A3H CONTEXT



Title : BLOCK DIAGRAM		
ASUSTeK COMPUTER INC	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 1 of 53	

REVISION LIST

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
~~+1.5VSUS~~	~~1.5V~~	~~270 mA~~
+1.8V	1.8V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	18 mils

37.5 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN2	9.5 mils

42 OHM	WIDTH
TOP/BOT	9 mils
IN1/IN2	7.5 mils

50 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN2	5 mils

55 OHM	WIDTH
TOP/BOT	5.5 mils
IN1/IN2	4.5 mils

75 OHM	WIDTH
TOP/BOT	4 mils
IN1/IN3	3.5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 4 mils
IN1/IN2	7.5 mils/ 4 mils

85 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 4 mils
IN1/IN2	4.5 mils/ 4 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 5 mils
IN1/IN2	4.5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	6 mils/ 11 mils
IN1/IN2	5 mils/ 12 mils

110 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 13 mils
IN1/IN2	4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 GND
L3 IN1
L4 IN2
L5 GND
L6 BOT

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```
SIGNAL  IN:   VR_VID[0..5]
              PM_DPRSLPVR
              STP_CPU#
              PM_PSI#
              CPU_VRON
              MCH_OK
        OUT:  DELAY_VR_PWRGD
              CLK_PWR_GD#

POWER   IN:   AC_BAT_SYS
              +5VO
              +3VO
        OUT:  +VCORE
```

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```
SIGNAL   IN:  SUSC#_PWR
              VSUS_ON

POWER    IN:  AC_BAT_SYS

         OUT: +12VO
              +3VO
              +5VO
```

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```
SIGNAL  IN: SUSB#_PWR
            SUSC#_PWR
            CPU_VRON

POWER   IN: AC_BAT_SYS
            +5VO

       OUT: +1.8V
            +1.5VS
            +2.5VS
            +VCC_GMCH_CORE
            +5VALWAYS
            +3VALWAYS
            +VCCP
```

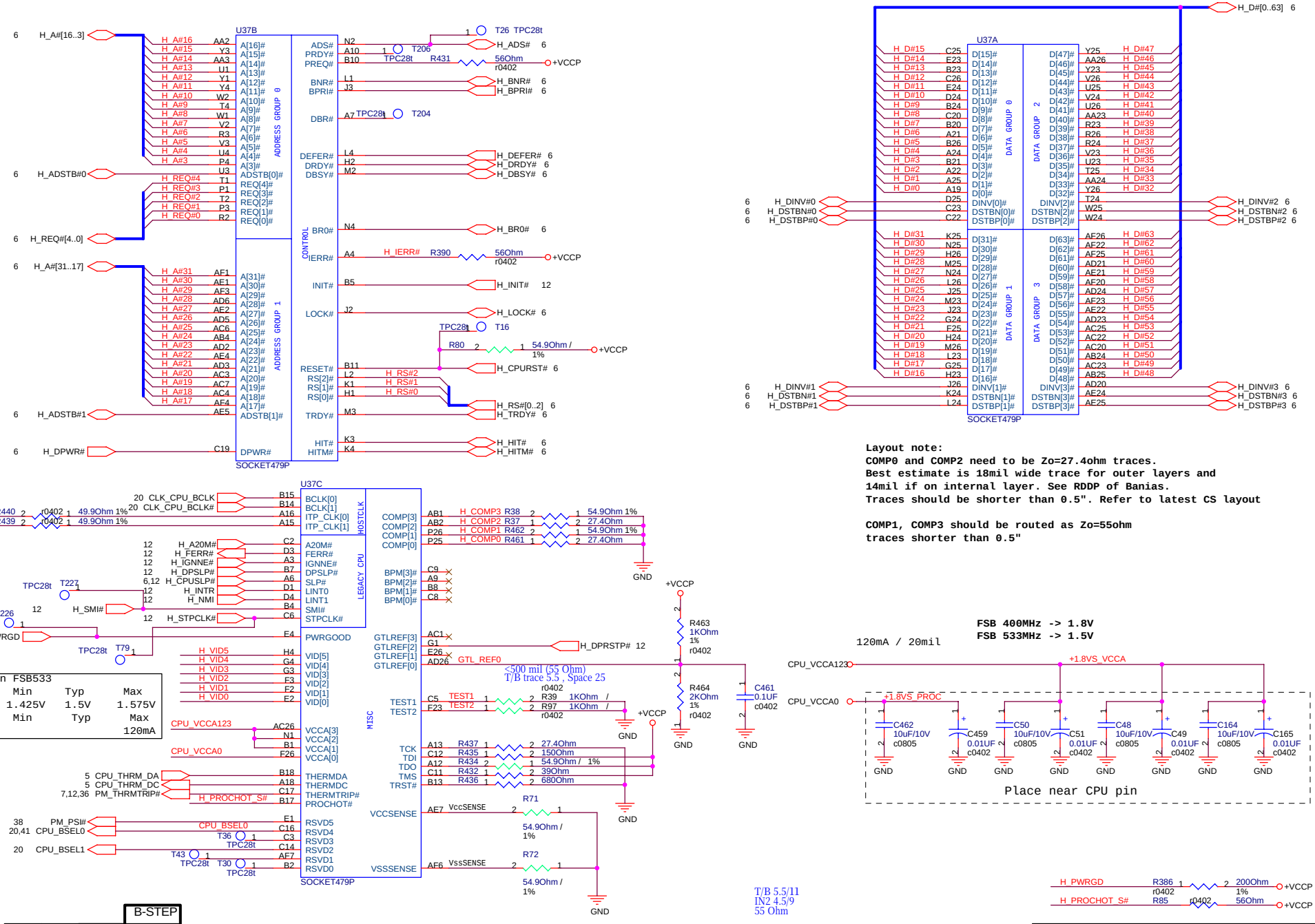
PAGE 41

```
SIGNAL  IN: SUSB#_PWR

POWER   IN: +3V
            +1.8V

       OUT: +0.9VS
```

ASUSTeK COMPUTER INC	Title : REVISION LIST	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 2 of 53	


U37B
SOCKET479P
ADDRESS GROUP 0
ADDRESS GROUP 1
CONTROL
H_A#[16..3]
H_ADSTB#0
H_REQ#[4..0]
H_A#[31..17]
H_ADSTB#1
H_DPWR#
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BR0#
H_IERR#
H_INIT#
H_LOCK#
H_CPURST#
H_RS#[0..2]
H_TRDY#
H_HIT#
H_HITM#
+VCCP
U37A
SOCKET479P
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
H_D#[0..63]
H_DINV#0
H_DSTBN#0
H_DSTBP#0
H_DINV#1
H_DSTBN#1
H_DSTBP#1
H_DINV#2
H_DSTBN#2
H_DSTBP#2
H_DINV#3
H_DSTBN#3
H_DSTBP#3
U37C
SOCKET479P
HOSTCLK
LEGACY CPU
MISC
CLK_CPU_BCLK
CLK_CPU_BCLK#
H_A20M#
H_FERR#
H_IGNNE#
H_DPSLP#
H_CPUSLP#
H_INTR
H_NMI
H_SMI#
H_STPCLK#
H_PWRGD
H_DPRSTP# 12
GTL_REF0
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
CPU_VCCA123
CPU_VCCA0
CPU_THRM_DA
CPU_THRM_DC
PM_THRMTRIP#
H_PROCHOT_S#
PM_PSI#
CPU_BSEL0
CPU_BSEL1
H_COMP3 R38 54.9Ohm 1%
H_COMP2 R37 27.4Ohm
H_COMP1 R462 54.9Ohm 1%
H_COMP0 R461 27.4Ohm
R440 49.9Ohm 1%
R439 49.9Ohm 1%
R80 54.9Ohm / 1%
R463 1KOhm 1% r0402
R464 2KOhm 1% r0402
C461 0.1UF c0402
R71 54.9Ohm / 1%
R72 54.9Ohm / 1%
R437 27.4Ohm
R435 150Ohm
R434 54.9Ohm / 1%
R432 39Ohm
R436 680Ohm
R386 200Ohm 1%
R85 56Ohm
R481 0Ohm r0402
R480 0Ohm r0402
RN27A
RN27B
RN27C
RN27D
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID1
VR_VID0
C462 10uF/10V c0805
C459 0.01UF c0402
C50 10uF/10V c0805
C51 0.01UF c0402
C48 10uF/10V c0805
C49 0.01UF c0402
C164 10uF/10V c0805
C165 0.01UF c0402
+1.8VS_VCCA
+1.8VS_PROC
120mA / 20mil
Place near CPU pin
FSB 400MHz -> 1.8V
FSB 533MHz -> 1.5V
<500 mil (55 Ohm)
T/B trace 5.5 , Space 25
T/B 5.5/11
IN2 4.5/9
55 Ohm
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
Bclk FSB BSEL1 B-STEP BSEL0
100 400 0 1
133 533 0 0
Title : DOTHAN CPU (1)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 3 of 53

Dothan FSB533	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

+VCCP

+VCORE

U37D

VCC

SOCKET479P

U37E

GND

SOCKET479P

GND

GND

MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

+VCCP

CE4 150U/4.0V

C100 0.1UF c0402
C442 0.1UF c0402
C99 0.1UF c0402
C441 0.1UF c0402
C127 0.1UF c0402
C412 0.1UF c0402
C407 0.1UF c0402
C128 0.1UF c0402
C408 0.1UF c0402

GND

U69 SPRING_SQ31 /

U70 SPRING_SQ31 /

For EMI

+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

C443 0.1UF c0402
C414 10uF/10V c0805
C434 10uF/10V c0805

GND

ASUSTeK COMPUTER INC

Title : DOTHAN CPU (2)

Engineer: Howard Tu

Size	Project Name	Rev
Custom	A3H	2.0

Date: Tuesday, August 09, 2005 Sheet 4 of 53

Fan Speed Control

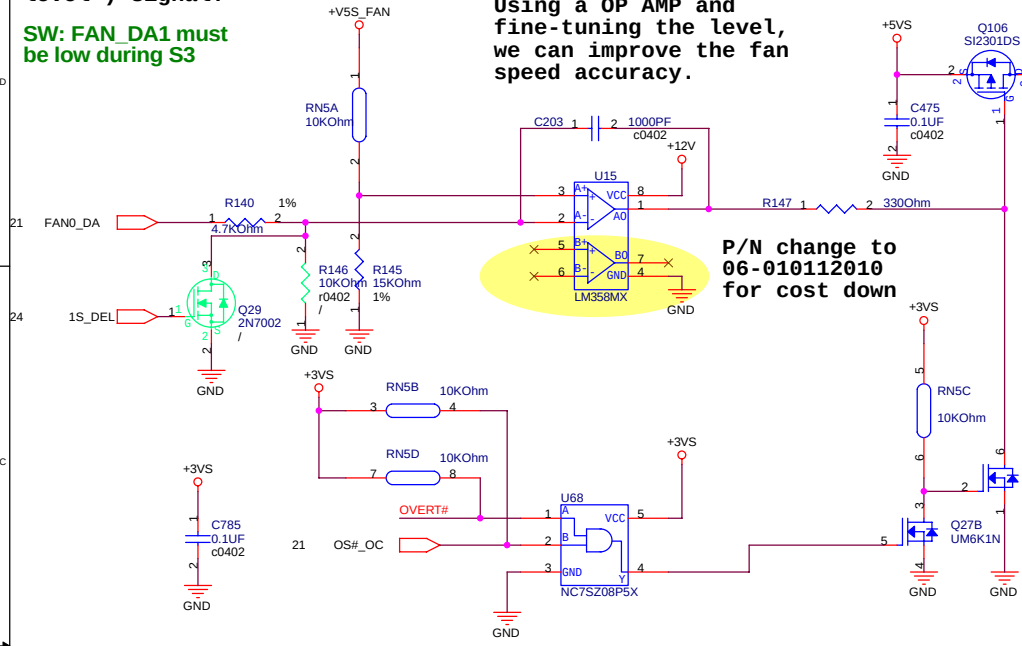
CPU FAN

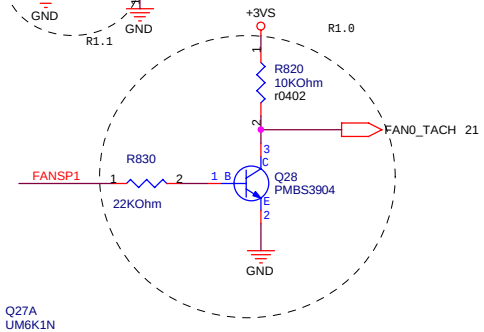
KBC will issue a analog (a voltage level) signal.

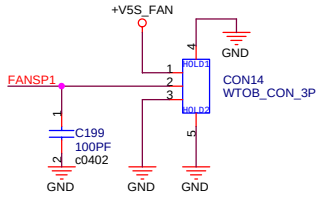
SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

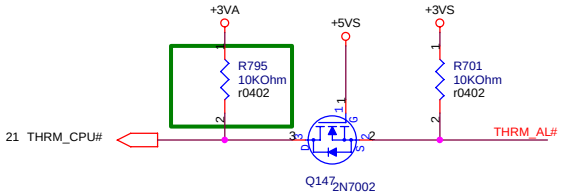
P/N change to 06-010112010 for cost down







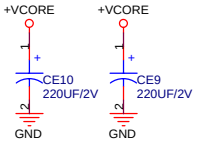
U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.



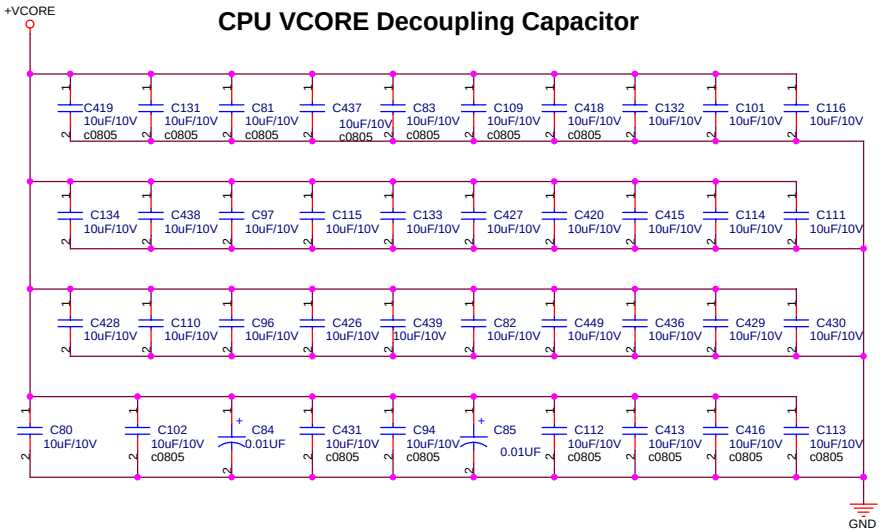
Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



CPU VCORE Decoupling Capacitor

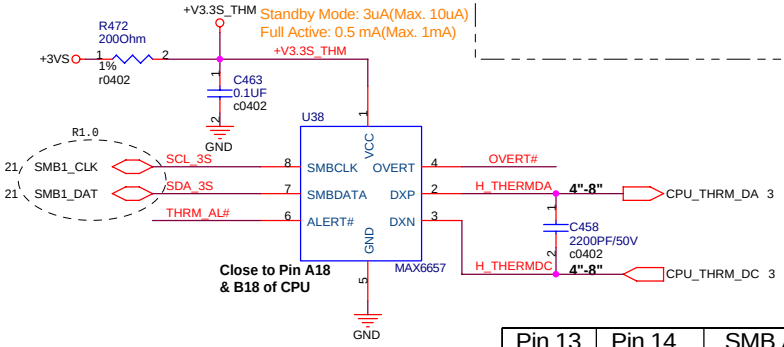


Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

Four 200 uF are located in IMVP4



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

Title : THER-SENSOR,FAN

ASUSTeK COMPUTER INC

Engineer: Howard Tu

Size	Project Name	Rev
Custom	A3H	2.0

Date: Tuesday, August 09, 2005 Sheet 5 of 53

In OrCAD circuit,ALVISO PM P/N :02-010002600

But we have to use ALVISO GM P/N : 02-010002610 in BOM list

H_XRCOMP 12/20mils
R380 24.9Ohm 1% GND
+VCCP
R379 54.9Ohm 1%
H_XSCOMP 5.5/20 mils

+VCCP
R414 221Ohm 1% r0402
H_XSWING 12/20mils
R413 100Ohm 1% r0402
C398 0.1UF c0402
C399 10uF/10V c0805
GND GND GND

H_YRCOMP 12/20mils
R433 24.9Ohm 1% GND

+VCCP
R420 54.9Ohm 1%
H_YSCOMP 5.5/20 mils

+VCCP
R429 221Ohm 1% r0402
H_YSWING 12/20mils
R430 100Ohm 1% r0402
C405 0.1UF c0402
C409 10uF/10V c0805
GND GND GND

3 H_D#[0..63]

U36D

H_D#0	E4	HD0#	HA3#	G9	H_A#3
H_D#1	E1	HD1#	HA4#	C9	H_A#4
H_D#2	F4	HD2#	HA5#	E9	H_A#5
H_D#3	H7	HD3#	HA6#	B7	H_A#6
H_D#4	F2	HD4#	HA7#	A10	H_A#7
H_D#5	F1	HD5#	HA8#	F9	H_A#8
H_D#6	E3	HD6#	HA9#	D8	H_A#9
H_D#7	D3	HD7#	HA10#	B10	H_A#10
H_D#8	K7	HD8#	HA11#	E10	H_A#11
H_D#9	F2	HD9#	HA12#	G10	H_A#12
H_D#10	J7	HD10#	HA13#	D9	H_A#13
H_D#11	J8	HD11#	HA14#	E11	H_A#14
H_D#12	H6	HD12#	HA15#	F10	H_A#15
H_D#13	F3	HD13#	HA16#	G11	H_A#16
H_D#14	K8	HD14#	HA17#	G13	H_A#17
H_D#15	H5	HD15#	HA18#	C10	H_A#18
H_D#16	H1	HD16#	HA19#	C11	H_A#19
H_D#17	H2	HD17#	HA20#	D11	H_A#20
H_D#18	K5	HD18#	HA21#	C12	H_A#21
H_D#19	K6	HD19#	HA22#	B13	H_A#22
H_D#20	J4	HD20#	HA23#	A12	H_A#23
H_D#21	G3	HD21#	HA24#	F12	H_A#24
H_D#22	H3	HD22#	HA25#	G12	H_A#25
H_D#23	J1	HD23#	HA26#	E12	H_A#26
H_D#24	L5	HD24#	HA27#	C13	H_A#27
H_D#25	K4	HD25#	HA28#	B11	H_A#28
H_D#26	J5	HD26#	HA29#	D13	H_A#29
H_D#27	P7	HD27#	HA30#	A13	H_A#30
H_D#28	L7	HD28#	HA31#	F13	H_A#31
H_D#29	J3	HD29#			
H_D#30	P5	HD30#	HADS#	F8	H_ADS#
H_D#31	L3	HD31#	HADSTB0#	B9	H_ADSTB#0
H_D#32	U7	HD32#	HADSTB1#	E13	H_ADSTB#1
H_D#33	V6	HD33#	HVREF	J11	
H_D#34	R6	HD34#	HBNR#	A5	H_BNR#
H_D#35	R5	HD35#	HBPR#	D5	H_BPRI#
H_D#36	P3	HD36#	HBREQ0#	E7	H_BREQ#0
H_D#37	T8	HD37#	HCPURST#	H10	H_CPURST#
H_D#38	R7	HD38#			
H_D#39	R8	HD39#	HCLKINN	AB1	CLK_MCH_BCLK# 20
H_D#40	U8	HD40#	HCLKINP	AB2	CLK_MCH_BCLK 20
H_D#41	R4	HD41#			
H_D#42	T4	HD42#	HDBSY#	C6	H_DBSY# 3
H_D#43	T5	HD43#	HDEFER#	E6	H_DEFER# 3
H_D#44	R1	HD44#	HDINV0#	H8	H_DINV#0
H_D#45	T3	HD45#	HDINV1#	K3	H_DINV#1
H_D#46	V8	HD46#	HDINV2#	T7	H_DINV#2
H_D#47	U6	HD47#	HDINV3#	U5	H_DINV#3
H_D#48	W6	HD48#	HDPWR#	G6	
H_D#49	U3	HD49#	HDRDY#	F7	H_DRDY# 3
H_D#50	V5	HD50#	HDSTBN0#	G4	H_DSTBN#0
H_D#51	W8	HD51#	HDSTBN1#	K1	H_DSTBN#1
H_D#52	W7	HD52#	HDSTBN2#	R3	H_DSTBN#2
H_D#53	U2	HD53#	HDSTBN3#	V3	H_DSTBN#3
H_D#54	U1	HD54#	HDSTBP0#	G5	H_DSTBP#0
H_D#55	Y5	HD55#	HDSTBP1#	K2	H_DSTBP#1
H_D#56	Y2	HD56#	HDSTBP2#	R2	H_DSTBP#2
H_D#57	V4	HD57#	HDSTBP3#	W4	H_DSTBP#3
H_D#58	Y7	HD58#	HEDRDY#	F6	TP_H_EDRDY#
H_D#59	W1	HD59#	HHIT#	D4	H_HIT# 3
H_D#60	W3	HD60#	HHITM#	D6	H_HITM# 3
H_D#61	Y3	HD61#	HLOCK#	B3	
H_D#62	Y6	HD62#	HPCREQ#	A11	TP_H_PCREQ#
H_D#63	W2	HD63#	HREQ0#	A7	H_REQ#0
			HREQ1#	D7	H_REQ#1
H_XRCOMP	C1	HXRCOMP	HREQ2#	B8	H_REQ#2
H_XSCOMP	C2	HXSCOMP	HREQ3#	C7	H_REQ#3
H_XSWING	D1	HXSWING	HREQ4#	A8	H_REQ#4
H_YRCOMP	T1	HYRCOMP	HRS0#	A4	H_RS#0
H_YSCOMP	L1	HYSCOMP	HRS1#	C5	H_RS#1
H_YSWING	P1	HYSWING	HRS2#	B4	H_RS#2
			HCPUSLP#	G8	R42 1 2 0Ohm r0402
			HTRDY#	B5	H_TRDY# 3

HOST

ALVISO_BGA1257

H_A#[31..3] 3

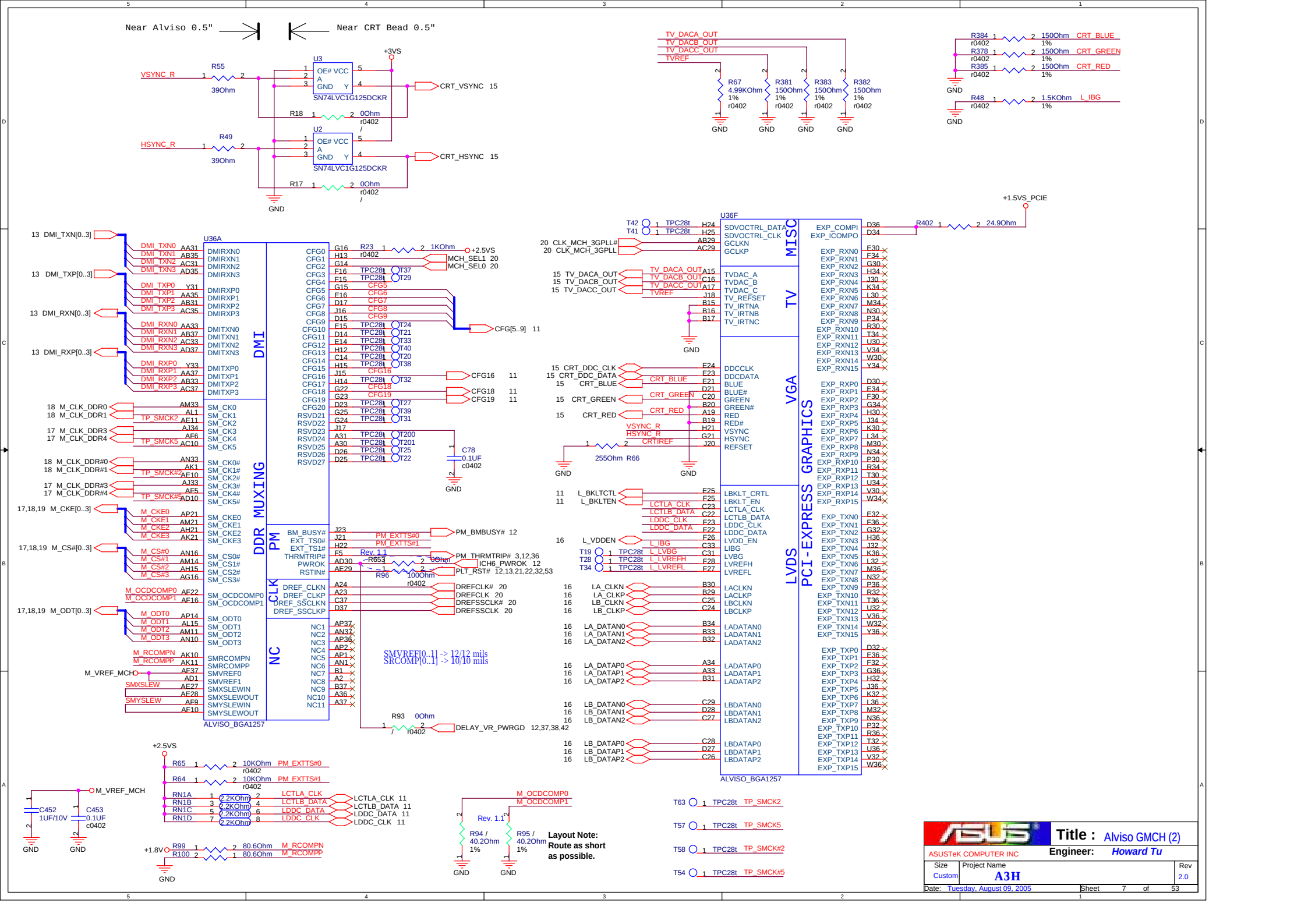
H_LOCK# 3
H_REQ#[4..0] 3
H_RS#[0..2] 3
H_CPUSLP# 3,12

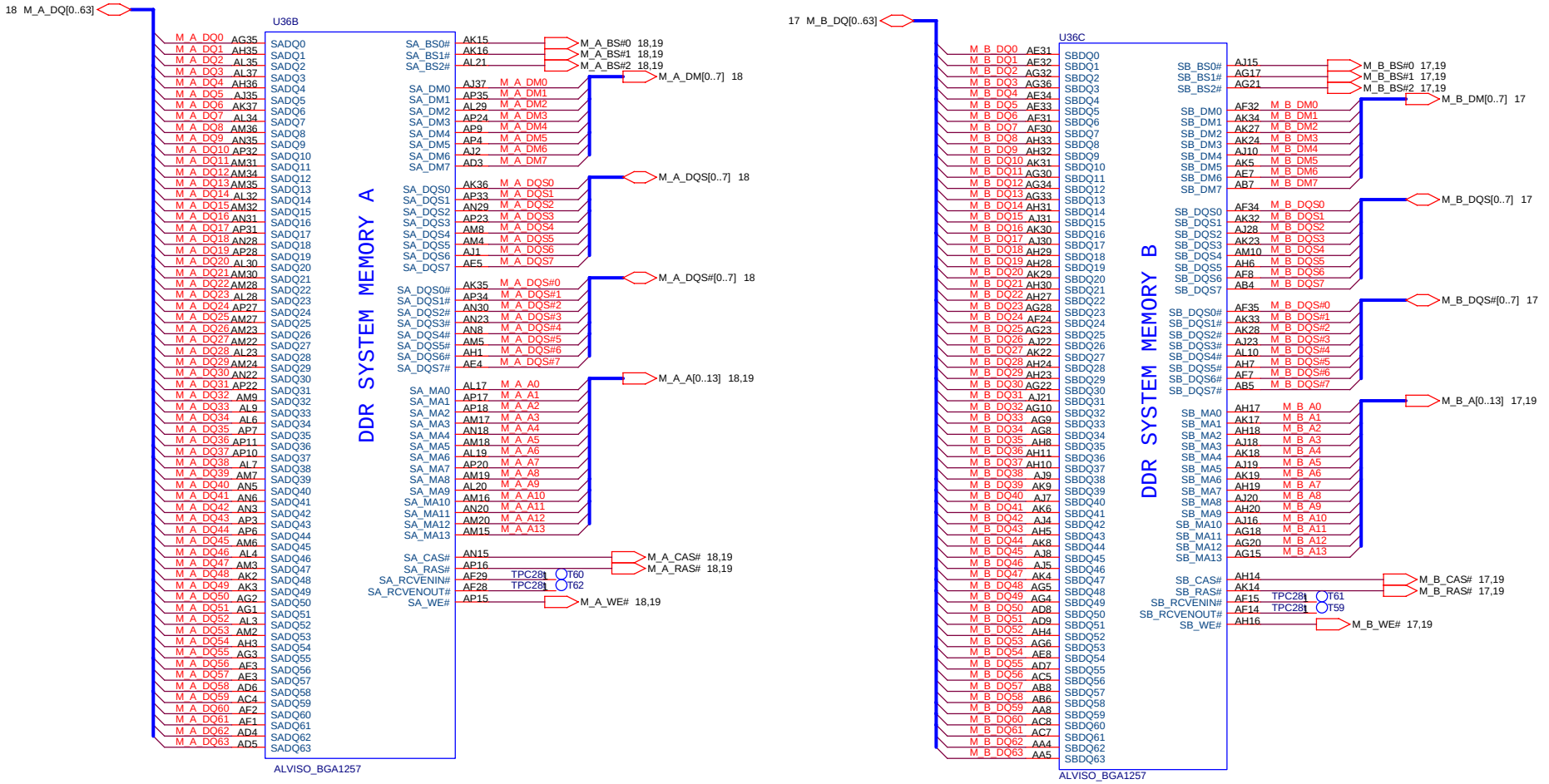
T35 TPC28t
T199 TPC28t

+VCCP
R74 100Ohm 1% r0402 <500 mil (55 Ohm) T/B trace 5.5 , Space 25
H_VREF
R70 200Ohm r0402 1%
C77 0.1UF c0402
GND GND

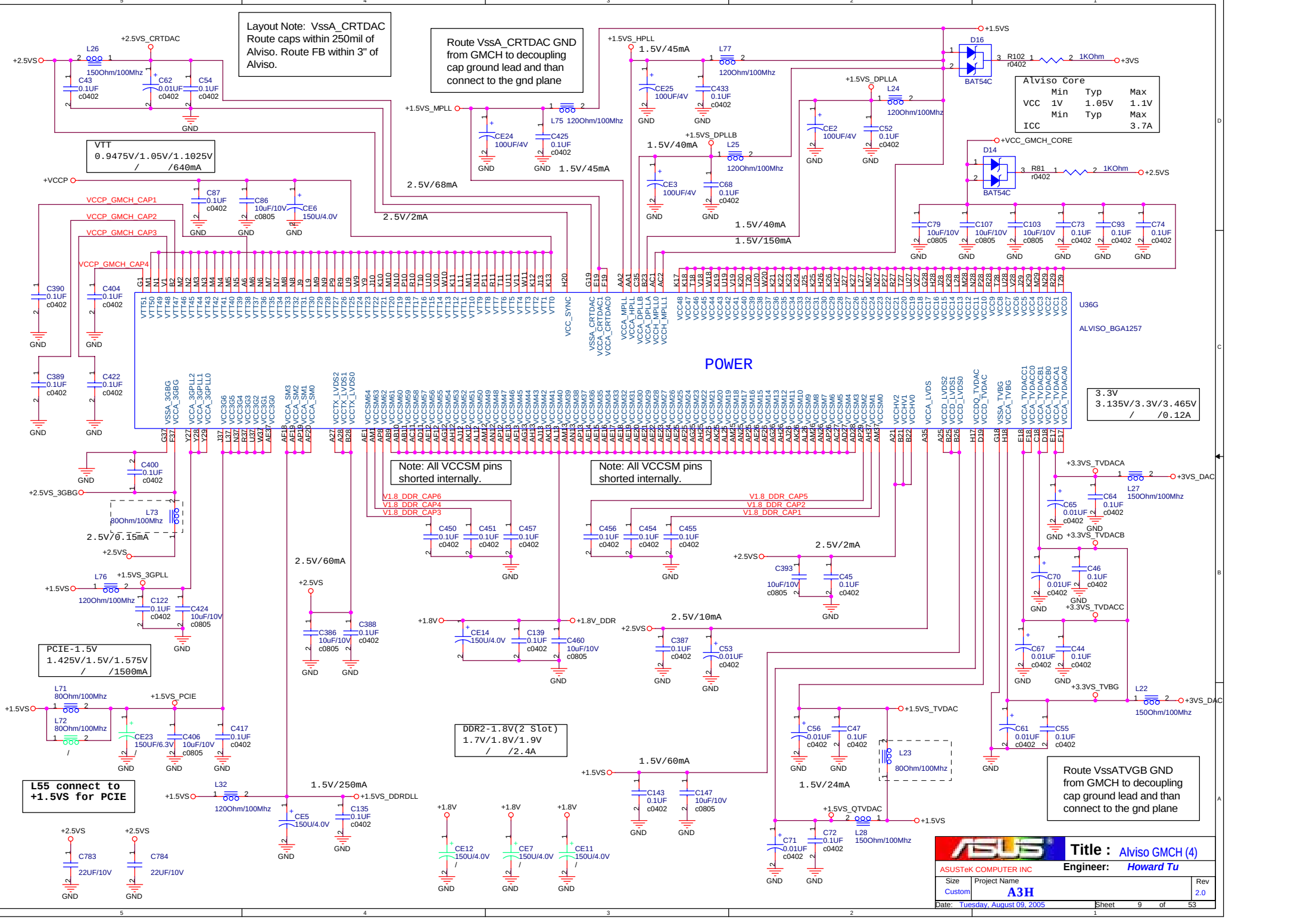
Dothan A : R282 NO STUFF

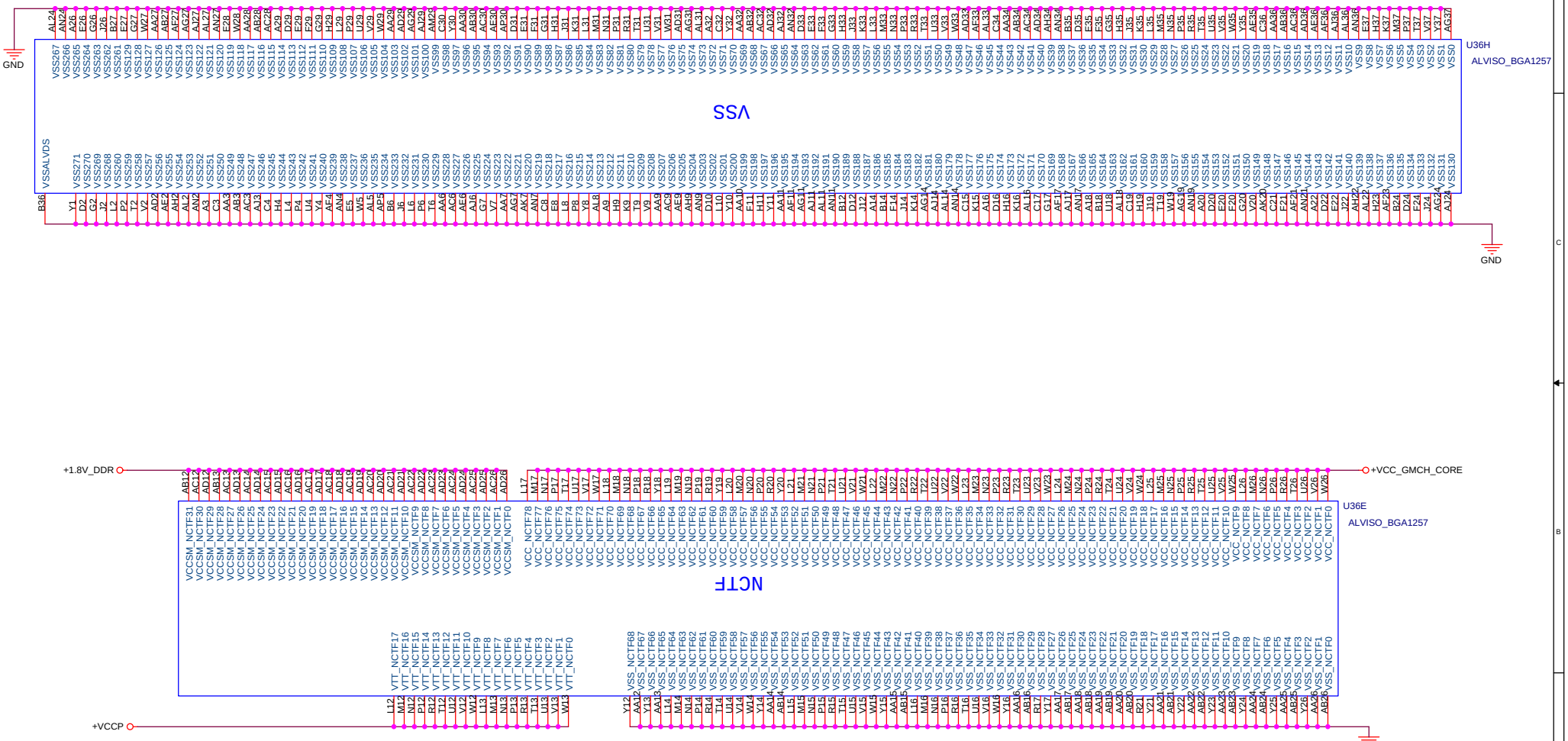
ASUSTeK COMPUTER INC	Title : Alviso GMCH (1)		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 6 of 53		


Near Alviso 0.5"
Near CRT Bead 0.5"
U3
SN74LVC1G125DCKR
U2
SN74LVC1G125DCKR
+3VS
VSYNC_R
HSYNC_R
R55
R49
39Ohm
R18
R17
0Ohm
r0402
CRT_VSYNC 15
CRT_HSYNC 15
GND
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TVREF
R67 4.99KOhm 1% r0402
R381 150Ohm 1% r0402
R383 150Ohm 1% r0402
R382 150Ohm 1% r0402
R384 150Ohm 1% r0402 CRT_BLUE
R378 150Ohm 1% r0402 CRT_GREEN
R385 150Ohm 1% r0402 CRT_RED
R48 1.5KOhm 1% r0402 L_IBG
U36A
ALVISO_BGA1257
DMI
DDR MUXING
PM
CLK
NC
U36F
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
+1.5VS_PCIE
R402 24.9Ohm
13 DMI_TXN[0..3]
13 DMI_TXP[0..3]
13 DMI_RXN[0..3]
13 DMI_RXP[0..3]
18 M_CLK_DDR0
18 M_CLK_DDR1
17 M_CLK_DDR3
17 M_CLK_DDR4
18 M_CLK_DDR#0
18 M_CLK_DDR#1
17 M_CLK_DDR#3
17 M_CLK_DDR#4
17,18,19 M_CKE[0..3]
17,18,19 M_CS#[0..3]
17,18,19 M_ODT[0..3]
M_VREF_MCH
SMXSLEW
SMYSLEW
CFG[5..9] 11
CFG16 11
CFG18 11
CFG19 11
C78 0.1UF c0402
R23 1KOhm
MCH_SEL1 20
MCH_SEL0 20
+2.5VS
PM_BMBUSY# 12
PM_THRMTRIP# 3,12,36
ICH6_PWROK 12
PLT_RST# 12,13,21,22,32,53
R653 0Ohm
R96 100Ohm r0402
DREFCLK# 20
DREFCLK 20
DREFSSCLK# 20
DREFSSCLK 20
SMVREF[0..1] -> 12/12 mils
SRCOMP[0..1] -> 10/10 mils
R93 0Ohm r0402
DELAY_VR_PWRGD 12,37,38,42
20 CLK_MCH_3GPLL#
20 CLK_MCH_3GPLL
15 TV_DACA_OUT
15 TV_DACB_OUT
15 TV_DACC_OUT
15 CRT_DDC_CLK
15 CRT_DDC_DATA
15 CRT_BLUE
15 CRT_GREEN
15 CRT_RED
VSYNC_R
HSYNC_R
CRTIREF
255Ohm R66
11 L_BKLTCTL
11 L_BKLTEN
16 L_VDDEN
L_IBG
L_LVBG
L_LVREFH
L_LVREFL
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
16 LA_CLKN
16 LA_CLKP
16 LB_CLKN
16 LB_CLKP
16 LA_DATAN0
16 LA_DATAN1
16 LA_DATAN2
16 LA_DATAP0
16 LA_DATAP1
16 LA_DATAP2
16 LB_DATAN0
16 LB_DATAN1
16 LB_DATAN2
16 LB_DATAP0
16 LB_DATAP1
16 LB_DATAP2
T42 TPC28t
T41 TPC28t
T19 TPC28t
T28 TPC28t
T34 TPC28t
T63 TPC28t TP_SMCK2
T57 TPC28t TP_SMCK5
T58 TPC28t TP_SMCK#2
T54 TPC28t TP_SMCK#5
C452 1UF/10V
C453 0.1UF c0402
+2.5VS
R65 10KOhm PM_EXTTS#0
R64 10KOhm PM_EXTTS#1
RN1A 2.2KOhm
RN1B 2.2KOhm
RN1C 2.2KOhm
RN1D 2.2KOhm
LCTLA_CLK 11
LCTLB_DATA 11
LDDC_DATA 11
LDDC_CLK 11
+1.8V
R99 80.6Ohm M_RCOMPN
R100 80.6Ohm M_RCOMPP
M_OCDCOMP0
M_OCDCOMP1
Rev. 1.1
R94 / 40.2Ohm 1%
R95 / 40.2Ohm 1%
Layout Note:
Route as short as possible.
Title : Alviso GMCH (2)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 7 of 53



ASUSTeK COMPUTER INC	Title : Alviso GMCH (3)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 8 of 53	


Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Alviso Core
Min Typ Max
VCC 1V 1.05V 1.1V
Min Typ Max
ICC 3.7A
VTT
0.9475V/1.05V/1.1025V
/ /640mA
POWER
U36G
ALVISO_BGA1257
3.3V
3.135V/3.3V/3.465V
/ /0.12A
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PCIE-1.5V
1.425V/1.5V/1.575V
/ /1500mA
DDR2-1.8V(2 Slot)
1.7V/1.8V/1.9V
/ /2.4A
L55 connect to +1.5VS for PCIE
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Title : Alviso GMCH (4)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 9 of 53

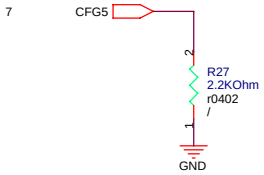


ASUSTeK COMPUTER INC		Title :	Alviso GMCH (5)
		Engineer:	Howard Tu
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 10 of 53		

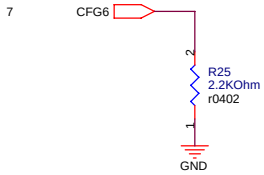
CFG[2:0] are HVCMOS (+2.5VS)
CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
CFG[19..18] have internal pulldown resistors./HVCMOS(+2.5VS)/
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)

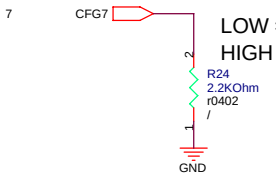


CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)



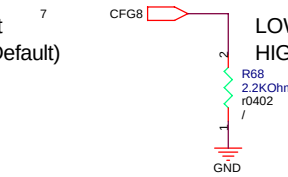
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

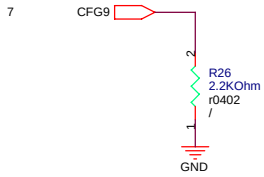


CFG8 : PCI-X POWER Saving

LOW = PCI-X POWER Saving
HIGH (Default)

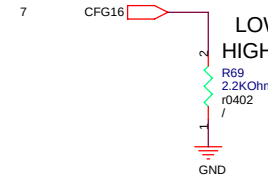


CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



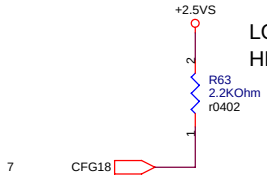
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



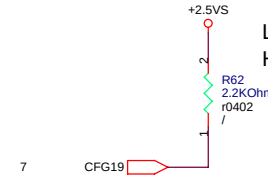
CFG18 : VCC SELECT

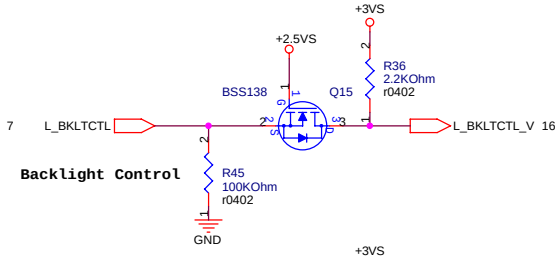
LOW = 1.05V (Default)
HIGH = 1.5V



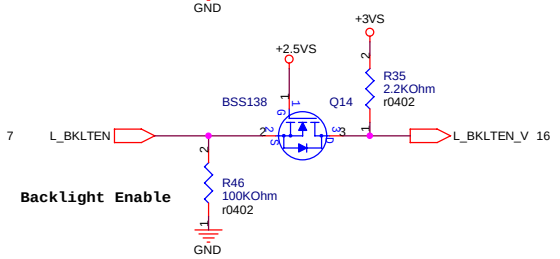
CFG19 : VTT SELECT

LOW = 1.05V (Default)
HIGH = 1.2V

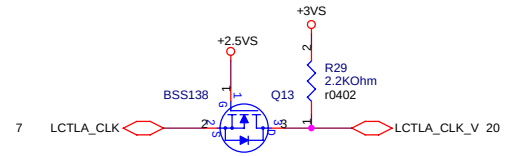




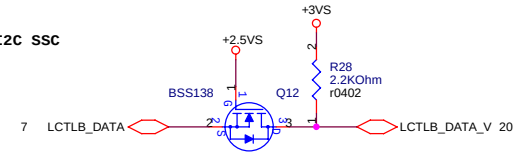
Backlight Control

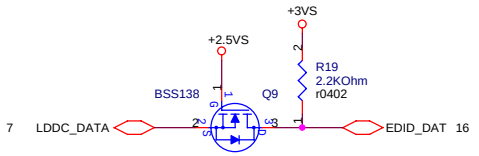


Backlight Enable

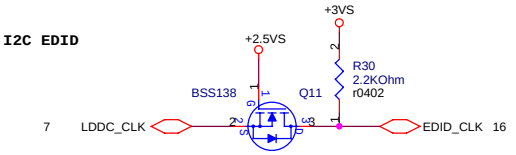


I2C SSC





I2C EDID



ASUSTeK COMPUTER INC	Title : GMCH Strapping	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 11 of 53	

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

U20C

U20D

ICH6_M

PLACE WITHIN 500mils of ICH6 ball

INTERNAL PULL-UP PULL-DOWN : RESERVED

H_CPUSLP# R193 : B STEP NO STUFF
H_DPRSTP# R231 : A STEP NO STUFF

INTERNAL PULL-DOWN PULL-UP : NO REBOOT

GPIO21: Program as Output
GPIO23: Program as Output
GPIO27: BT_LED_EN#,+3VSUS
GPIO28: not use
GPIO33: BL_ON,+3VS

TP_3 INTERNAL PULL-UP PULL-DOWN : PCI Express Port chain test

DELAY 18~25ms

BAT HOLDER P/N:
12-201110121
Rev 1.2

RTC BAT P/N: 07-016202032

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2" from the series resistor

Title :	ICH6_M (1)	
ASUSTeK COMPUTER INC	Engineer:	Howard Tu
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 12 of 53	

PLT_RST#
ICH6,Alviso/KBC/FWH/HDD

U20A

ICH6_M

U20B

ICH6_M

PLACE within 500 mils of ICH.

PLACE within 500 mils of ICH.
5.5mil/8mil

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK , AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , SDD[7] , PDDREQ , SDDREQ , SPKR , USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
EE_DIN , EE_DOUT , GNT[B:A]# , GNT[5]# , GPIO[17:16] , LAD[3:0]# , LDRQ[1:0] , LAN_RXD[2:0] , PME# , PWRBTN#

(USB 4 for CAMERA)
(USB 5 no use)

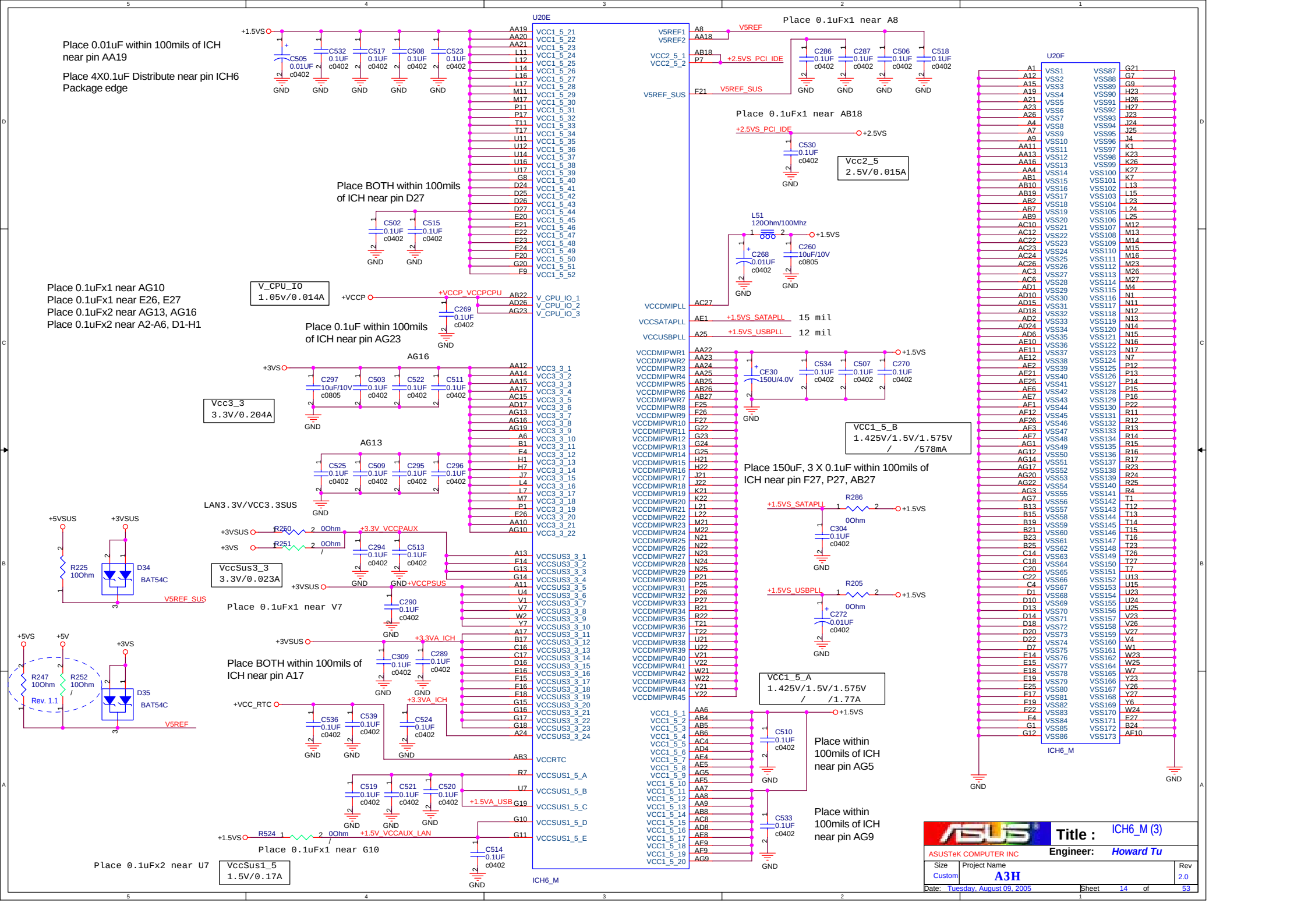
Rev. 1.1
Change value form 8.2K to 100K

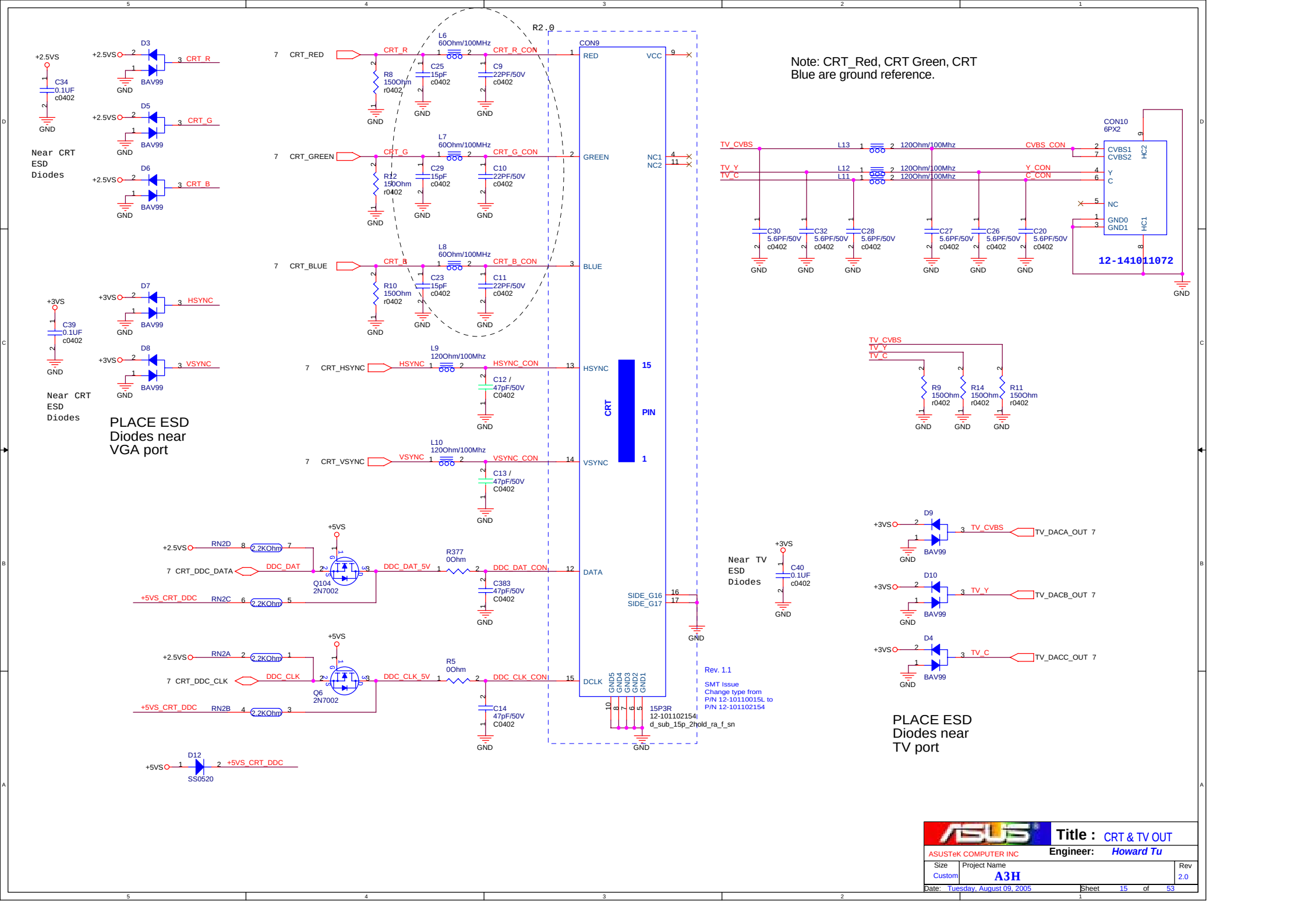
INTERNAL PULL-UP
PULL-DOWN : Boot BIOS destination select

INTERNAL PULL-UP
PULL-DOWN :TOP-BLOCK SWAP

PCB_VID	0	1	2
A3H	0	0	0
A3A	0	0	1

Title :	ICH6_M (2)
ASUSTeK COMPUTER INC	Engineer: Howard Tu
Size: Custom	Project Name: A3H
Rev: 2.0	
Date: Tuesday, August 09, 2005	Sheet 13 of 53


Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1
V_CPU_IO 1.05v/0.014A
Place 0.1uF within 100mils of ICH near pin AG23
AG16
Vcc3_3 3.3V/0.204A
AG13
LAN3.3V/VCC3.3SUS
VccSus3_3 3.3V/0.023A
Place 0.1uFx1 near V7
Place BOTH within 100mils of ICH near pin A17
Place 0.1uFx1 near G10
Place 0.1uFx2 near U7
VccSus1_5 1.5V/0.17A
Place 0.1uFx1 near A8
Place 0.1uFx1 near AB18
Vcc2_5 2.5V/0.015A
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
VCC1_5_B 1.425V/1.5V/1.575V / /578mA
VCC1_5_A 1.425V/1.5V/1.575V / /1.77A
Place within 100mils of ICH near pin AG5
Place within 100mils of ICH near pin AG9
U20E
U20F
ICH6_M
Title : ICH6_M (3)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 14 of 53

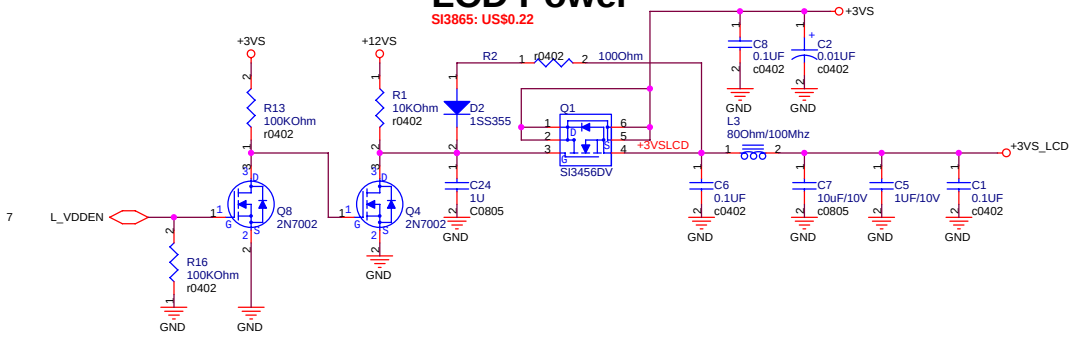

R2.0
Note: CRT_Red, CRT Green, CRT Blue are ground reference.
Near CRT ESD Diodes
Near CRT ESD Diodes
PLACE ESD Diodes near VGA port
Near TV ESD Diodes
PLACE ESD Diodes near TV port
CON9
CON10 6PX2
12-141011072
15P3R 12-101102154 d_sub_15p_2hold_ra_f_sn
Rev. 1.1
SMT Issue
Change type from P/N 12-10110015L to P/N 12-101102154
Q104 2N7002
Q6 2N7002
SS0520
Title : CRT & TV OUT
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 15 of 53

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

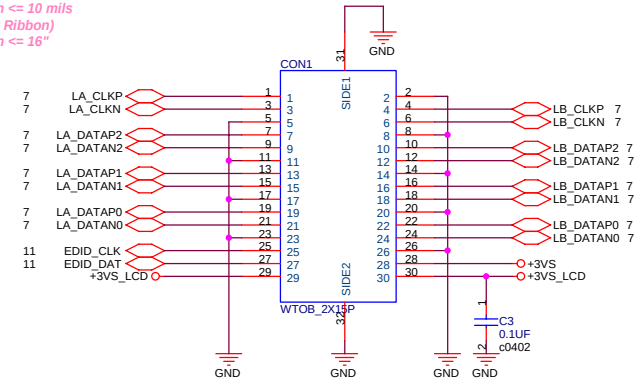
LCD Power

SI3865: US$0.22

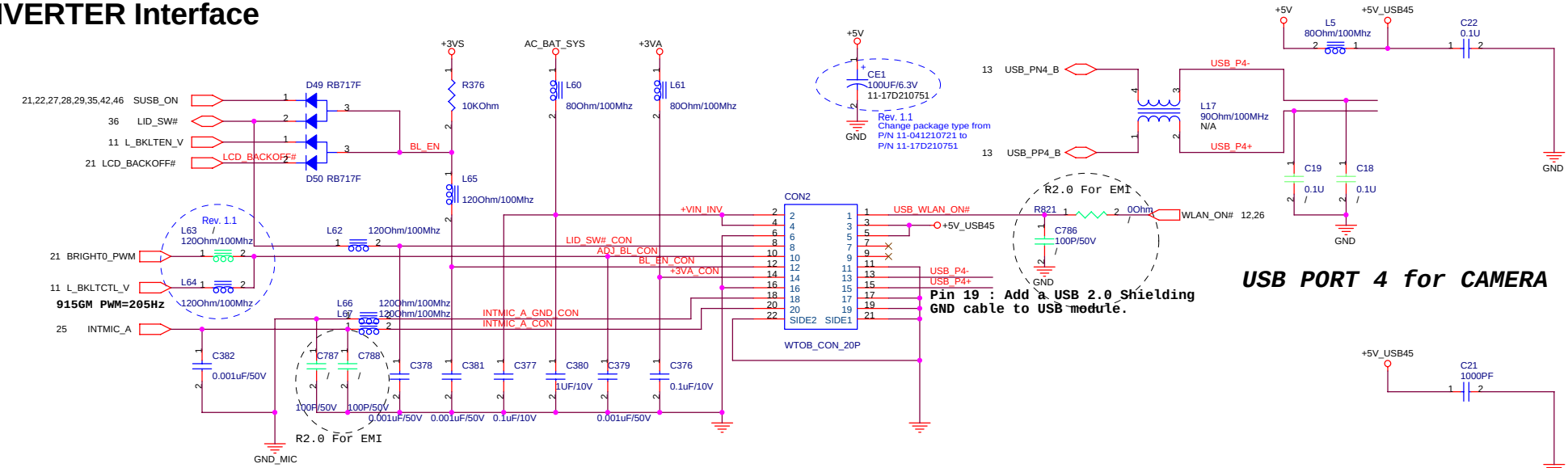


Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface



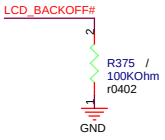
INVERTER Interface



USB PORT 4 for CAMERA

BIOS
ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

A3H/A3A don't use USB PORT 5 for WLAN

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 16 of 53	

For crosstalk

Change to PN:12-02512200B

M_CLK_DDR3
C486 10PF PLACE NEAR SO-DIMM_0 c0402
M_CLK_DDR#3
M_CLK_DDR4
C487 10PF PLACE NEAR SO-DIMM_0 c0402
M_CLK_DDR#4

8,19 M_B_A[0..13]
M_B_DQ[0..63] 8

CON15A

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10/AP
M_B_A11 90 A11
M_B_A12 89 A12
M_B_A13 116 A13
86 A14
84 A15
8,19 M_B_BS#2 85 A16_BA2
8,19 M_B_BS#0 107 BA0
8,19 M_B_BS#1 106 BA1
7,19 M_CS#2 110 S0#
7,19 M_CS#3 115 S1#
7 M_CLK_DDR3 30 CK0
7 M_CLK_DDR#3 32 CK0#
7 M_CLK_DDR4 164 CK1
7 M_CLK_DDR#4 166 CK1#
7,19 M_CKE2 79 CKE0
7,19 M_CKE3 80 CKE1
8,19 M_B_CAS# 113 CAS#
8,19 M_B_RAS# 108 RAS#
8,19 M_B_WE# 109 WE#
198 SA0
200 SA1
12,18,20 SMB_CLK_S 197 SCL
12,18,20 SMB_DAT_S 195 SDA
7,19 M_ODT2 114 ODT0
7,19 M_ODT3 119 ODT1
8 M_B_DM[0..7]
M_B_DM0 10 DM0
M_B_DM1 26 DM1
M_B_DM2 52 DM2
M_B_DM3 67 DM3
M_B_DM4 130 DM4
M_B_DM5 147 DM5
M_B_DM6 170 DM6
M_B_DM7 185 DM7
8 M_B_DQS[0..7]
M_B_DQS0 13 DQS0
M_B_DQS1 31 DQS1
M_B_DQS2 51 DQS2
M_B_DQS3 70 DQS3
M_B_DQS4 131 DQS4
M_B_DQS5 148 DQS5
M_B_DQS6 169 DQS6
M_B_DQS7 188 DQS7
8 M_B_DQS#[0..7]
M_B_DQS#0 11 DQS#0
M_B_DQS#1 29 DQS#1
M_B_DQS#2 49 DQS#2
M_B_DQS#3 68 DQS#3
M_B_DQS#4 129 DQS#4
M_B_DQS#5 146 DQS#5
M_B_DQS#6 167 DQS#6
M_B_DQS#7 186 DQS#7

DQ0 5 M_B_DQ4
DQ1 7 M_B_DQ5
DQ2 17 M_B_DQ7
DQ3 19 M_B_DQ6
DQ4 4 M_B_DQ1
DQ5 6 M_B_DQ0
DQ6 14 M_B_DQ2
DQ7 16 M_B_DQ3
DQ8 23 M_B_DQ13
DQ9 25 M_B_DQ8
DQ10 35 M_B_DQ15
DQ11 37 M_B_DQ14
DQ12 20 M_B_DQ9
DQ13 22 M_B_DQ12
DQ14 36 M_B_DQ10
DQ15 38 M_B_DQ11
DQ16 43 M_B_DQ21
DQ17 45 M_B_DQ20
DQ18 55 M_B_DQ23
DQ19 57 M_B_DQ19
DQ20 44 M_B_DQ16
DQ21 46 M_B_DQ17
DQ22 56 M_B_DQ18
DQ23 58 M_B_DQ22
DQ24 61 M_B_DQ25
DQ25 63 M_B_DQ24
DQ26 73 M_B_DQ26
DQ27 75 M_B_DQ27
DQ28 62 M_B_DQ29
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DQ30 74 M_B_DQ31
DQ31 76 M_B_DQ30
DQ32 123 M_B_DQ33
DQ33 125 M_B_DQ32
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DQ35 137 M_B_DQ35
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DQ37 126 M_B_DQ36
DQ38 134 M_B_DQ38
DQ39 136 M_B_DQ39
DQ40 141 M_B_DQ45
DQ41 143 M_B_DQ44
DQ42 151 M_B_DQ47
DQ43 153 M_B_DQ46
DQ44 140 M_B_DQ40
DQ45 142 M_B_DQ41
DQ46 152 M_B_DQ42
DQ47 154 M_B_DQ43
DQ48 157 M_B_DQ48
DQ49 159 M_B_DQ49
DQ50 173 M_B_DQ50
DQ51 175 M_B_DQ55
DQ52 158 M_B_DQ52
DQ53 160 M_B_DQ53
DQ54 174 M_B_DQ51
DQ55 176 M_B_DQ54
DQ56 179 M_B_DQ60
DQ57 181 M_B_DQ57
DQ58 189 M_B_DQ63
DQ59 191 M_B_DQ58
DQ60 180 M_B_DQ61
DQ61 182 M_B_DQ56
DQ62 192 M_B_DQ59
DQ63 194 M_B_DQ62

DDR2_DIMM_200P_REV

R513 10KOhm r0402 +3VS
R512 10KOhm r0402 GND

+1.8V_DIMM
CON15B

112 VDD1
111 VDD2
117 VDD3
96 VDD4
95 VDD5
118 VDD6
81 VDD7
82 VDD8
87 VDD9
103 VDD10
88 VDD11
104 VDD12
199 VDDSPD
83 NC1
120 NC2
50 NC3
69 NC4
163 NCTEST
1 VREF
201 GND0
202 GND1
203 NP_NC1
204 NP_NC2
47 VSS1
133 VSS2
183 VSS3
77 VSS4
12 VSS5
48 VSS6
184 VSS7
78 VSS8
71 VSS9
72 VSS10
121 VSS11
122 VSS12
196 VSS13
193 VSS14
8 VSS15
18 VSS16
24 VSS17
41 VSS18
53 VSS19
42 VSS20
54 VSS21
59 VSS22
65 VSS23
60 VSS24
66 VSS25
127 VSS26
139 VSS27
128 VSS28
145 VSS29
165 VSS30
171 VSS31
172 VSS32
177 VSS33
187 VSS34
178 VSS35
190 VSS36
9 VSS37
21 VSS38
33 VSS39
155 VSS40
34 VSS41
132 VSS42
144 VSS43
156 VSS44
168 VSS45
2 VSS46
3 VSS47
15 VSS48
27 VSS49
39 VSS50
149 VSS51
161 VSS52
28 VSS53
40 VSS54
138 VSS55
150 VSS56
162 VSS57

DDR2_DIMM_200P_REV

+3VS
C480 0.1UF c0402 GND
C479 0.1UF c0402 GND

VREF -> 10/10 mils
M_VREF_DIMM0
C477 2.2uF/6.3V GND
C481 0.1UF c0402 GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V_DIMM
C484 0.1UF c0402 GND
C248 0.1UF c0402 GND
C483 0.1UF c0402 GND
C482 0.1UF c0402 GND

Layout Note: Place these Caps near SO DIMM 0

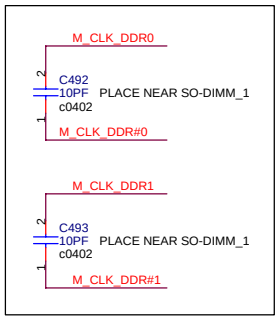
Layout Note: Place these High-Freq decoupling Caps near the GMCH

+1.8V_DIMM
C156 0.1UF c0402 GND
C149 0.1UF c0402 GND
C142 0.1UF c0402 GND
C151 0.1UF c0402 GND

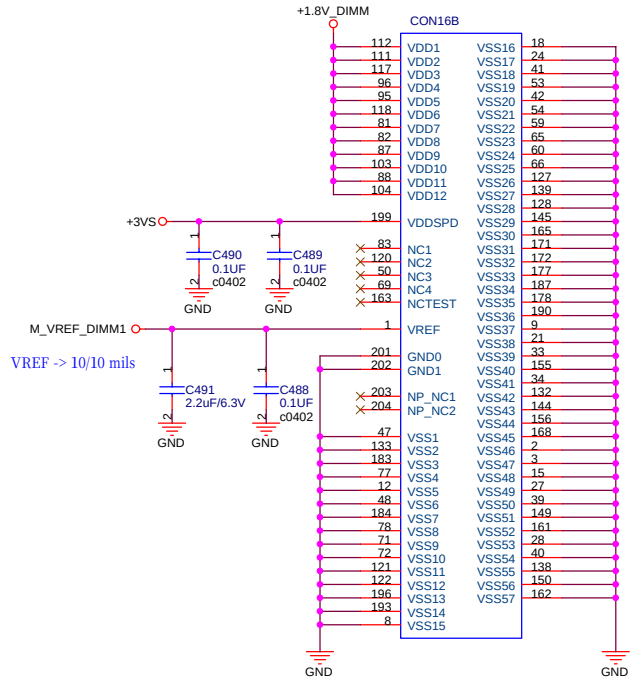
+1.8V
C478 2.2uF/6.3V GND
C244 2.2uF/6.3V GND
C243 2.2uF/6.3V GND
C246 2.2uF/6.3V GND
C245 2.2uF/6.3V GND
+1.8V_DIMM

ASUSTeK COMPUTER INC	Title : DDR2_SO-DIMM_0	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 17 of 53	

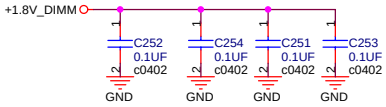
For crosstalk



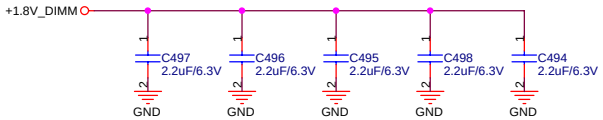
Change to PN:12-02512200A



Layout Note: Place these Caps near SO DIMM 1

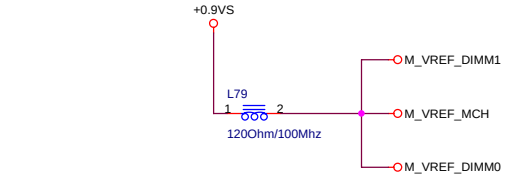


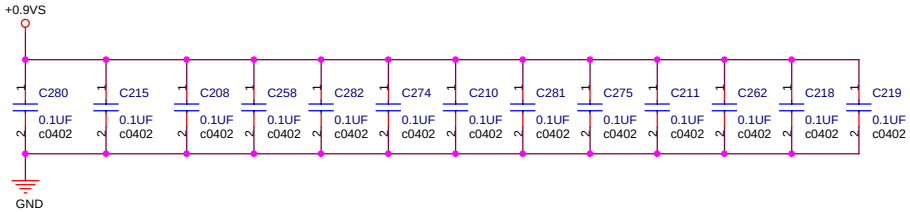
Layout Note: Place these Caps near SO DIMM 1



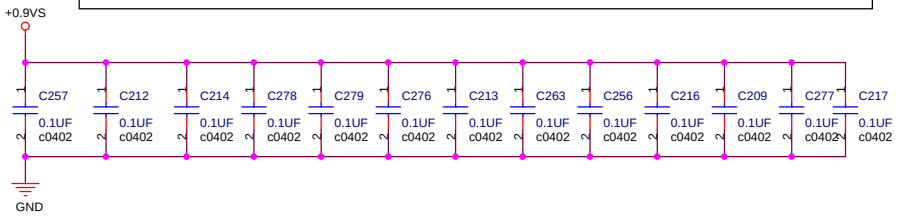
SO-DIMM 1 is placed father from the GMCH than SO-DIMM 0

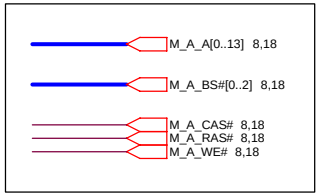
ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_1	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 18 of 53	

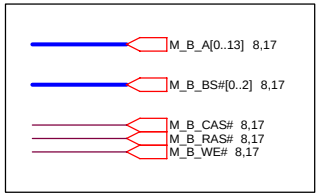


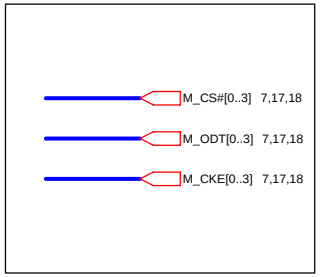


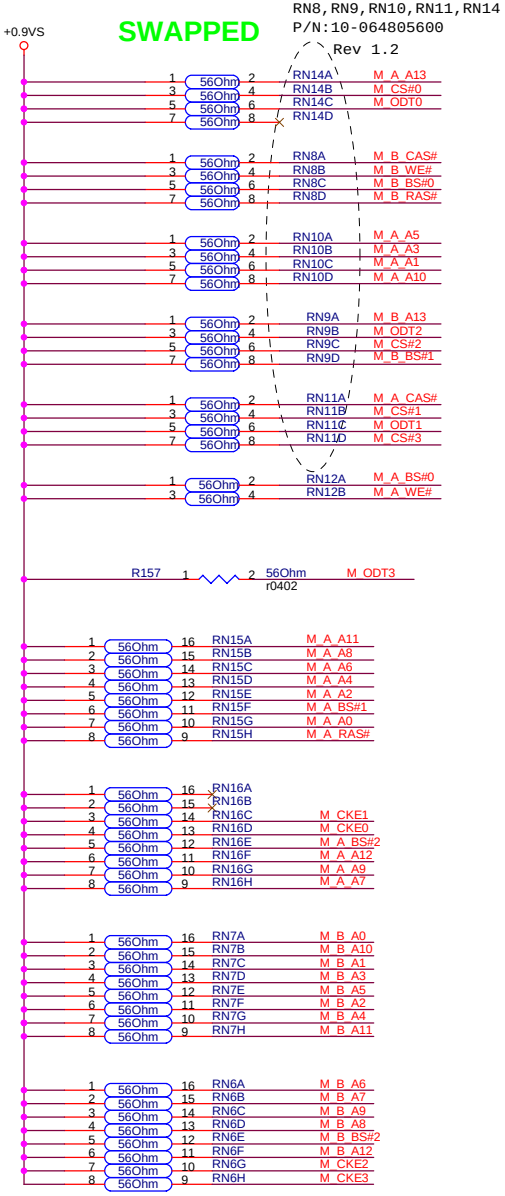
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



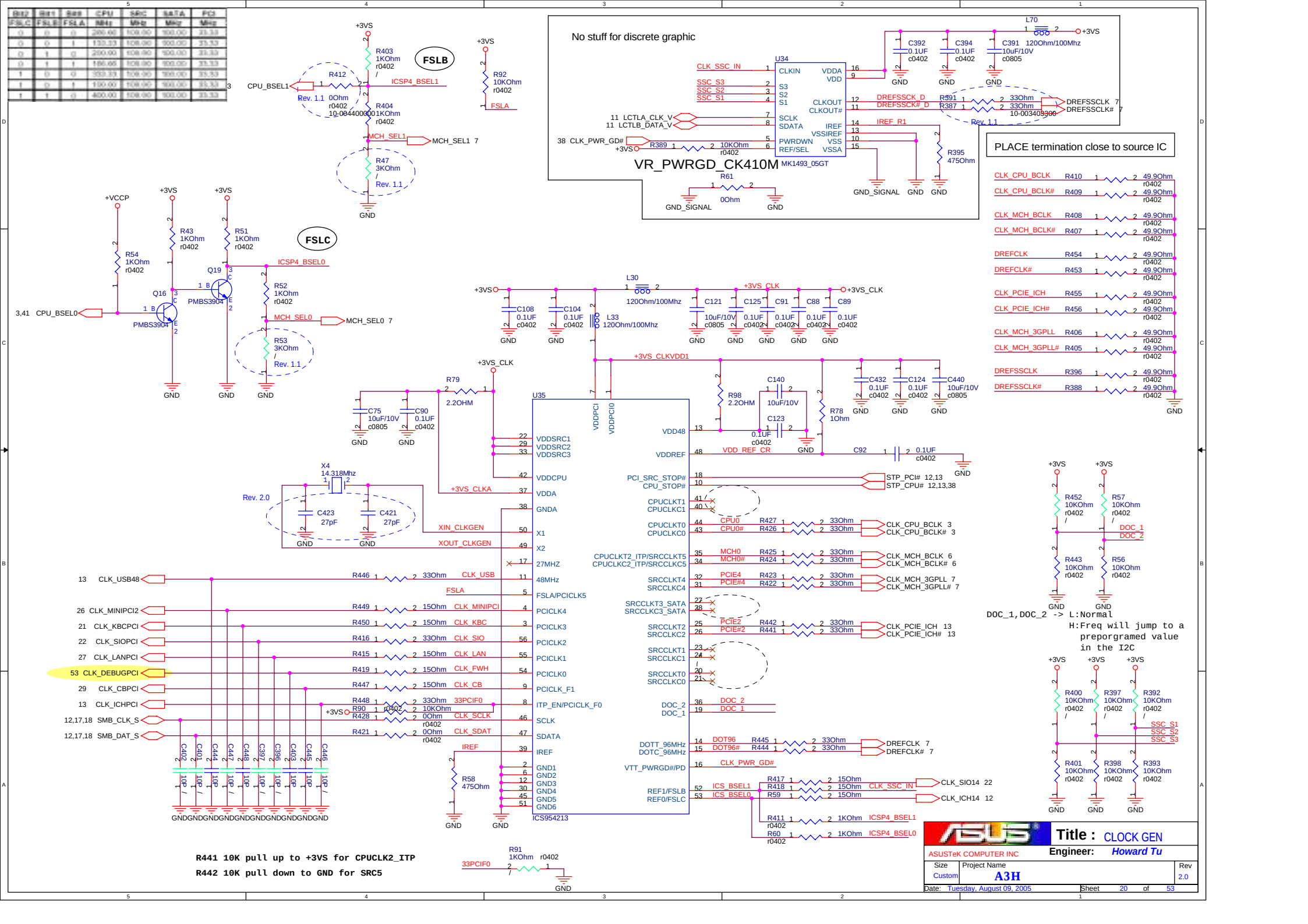


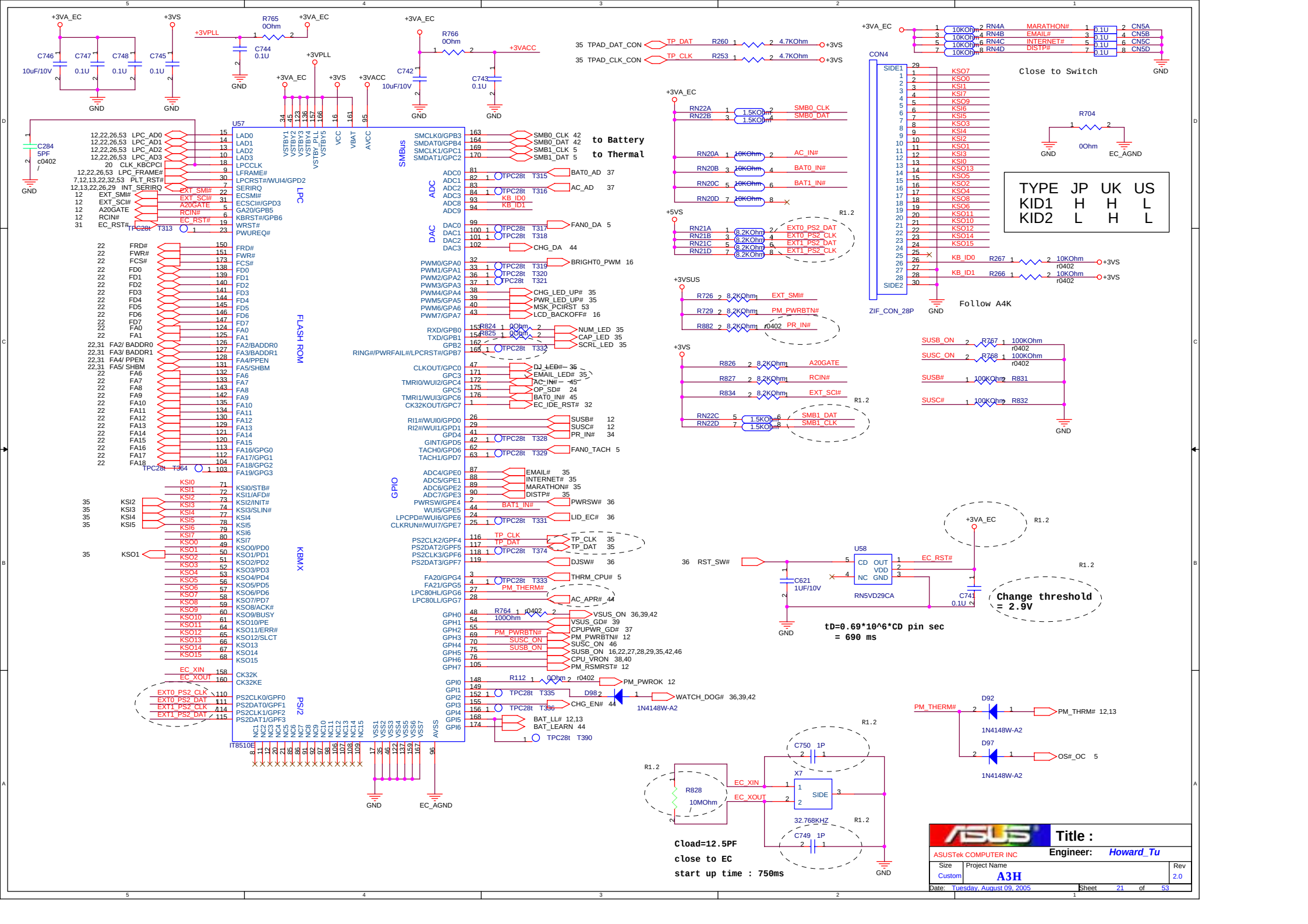




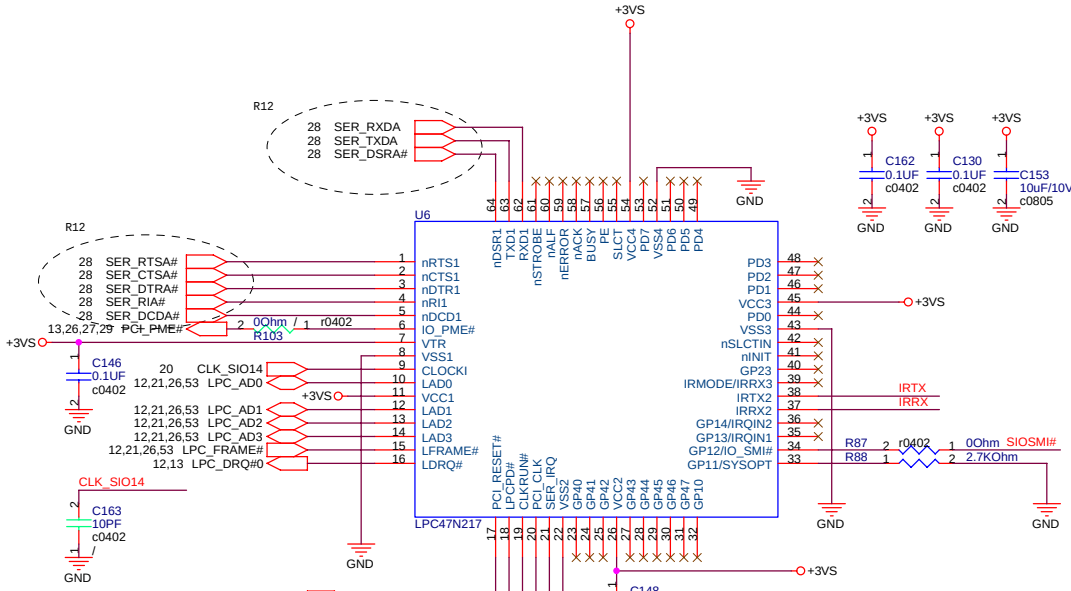


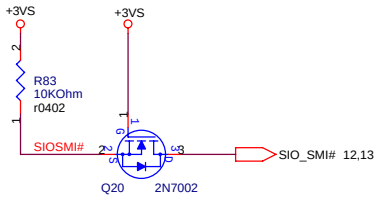
ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 19 of 53	


No stuff for discrete graphic
VR_PWRGD_CK410M
MK1493_05GT
PLACE termination close to source IC
FSLB
FSLC
ICS954213
R441 10K pull up to +3VS for CPUCLK2_ITP
R442 10K pull down to GND for SRC5
DOC_1,DOC_2 -> L:Normal
H:Freq will jump to a preporgramed value in the I2C
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 20 of 53


U57
IT8510E
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
Close to Switch
Follow A4K
Change threshold = 2.9V
tD=0.69*10^6*CD pin sec = 690 ms
Cload=12.5PF close to EC start up time : 750ms
TYPE JP UK US
KID1 H H L
KID2 L H L
Title :
ASUSTek COMPUTER INC
Engineer: Howard_Tu
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 21 of 53

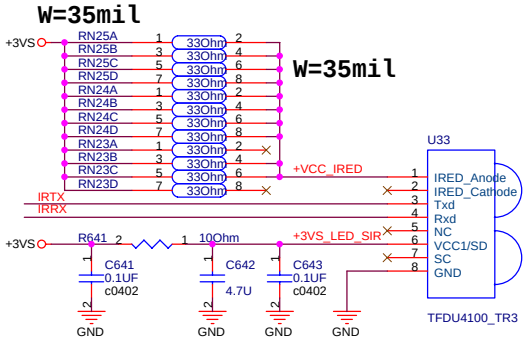
Super I/O





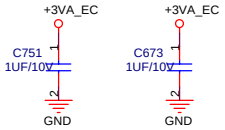
Keep From Leakage Current

W=35mil



W=35mil

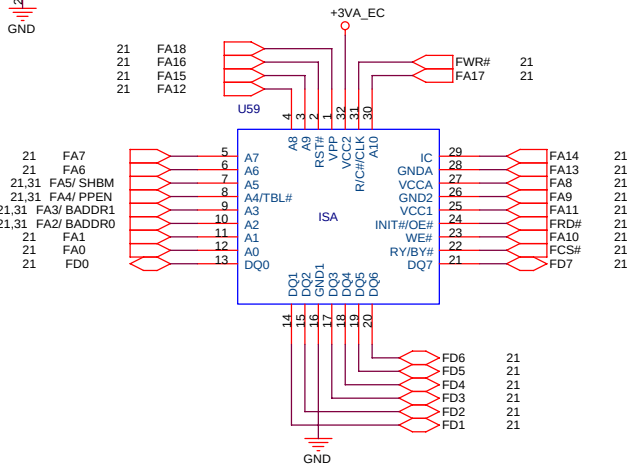
W=20mil



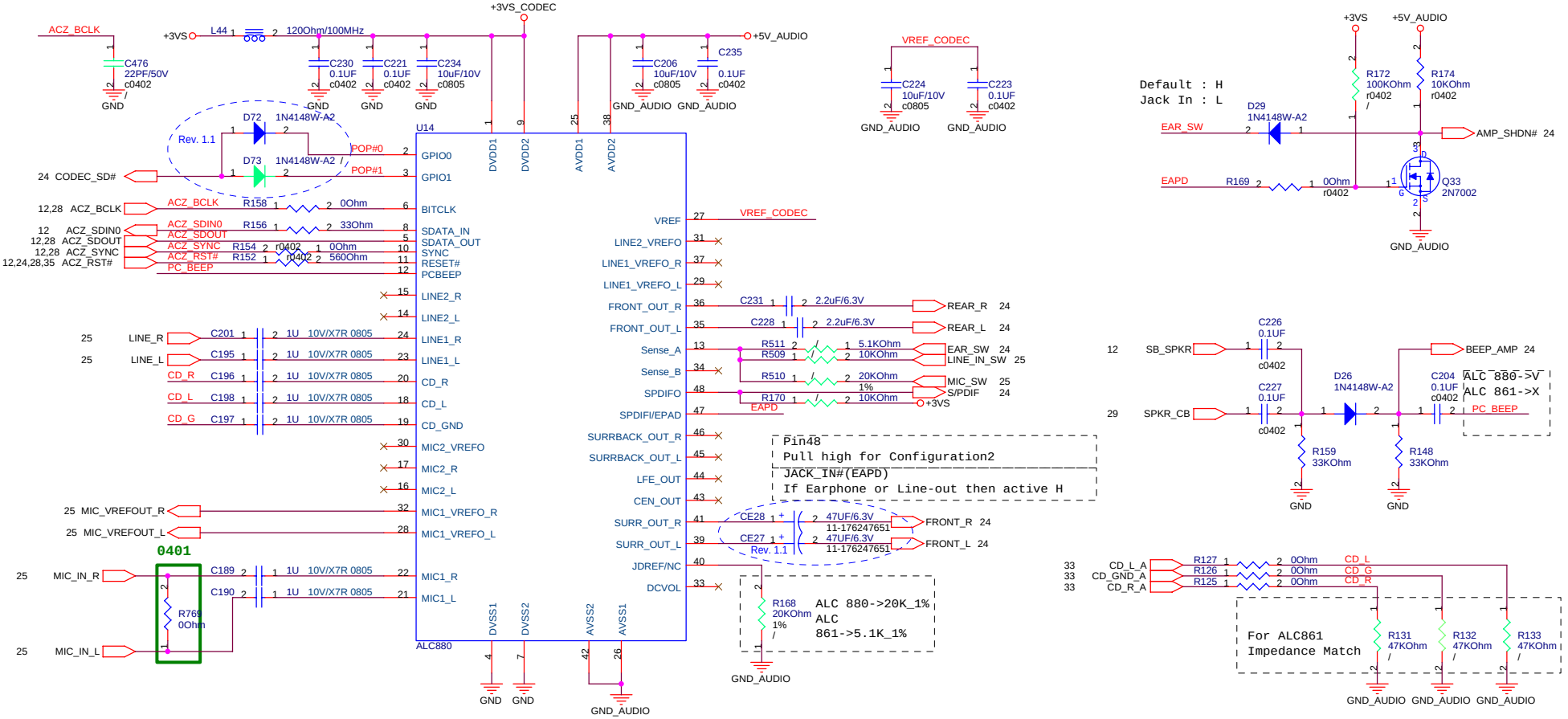
PLCC32 Socket
PN:12-043000323

PLCC32 4Mbits Flash ROM
PN:05G001014110(+3.3V)

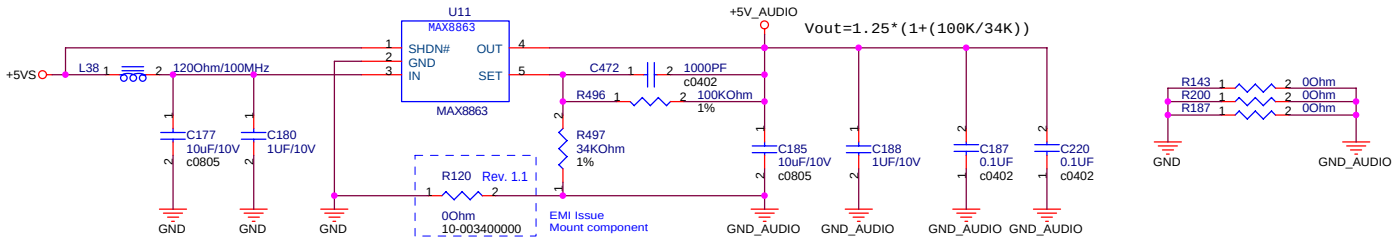
TSOP 4Mbits Flash ROM
PN:05-001004100(+3.3V)



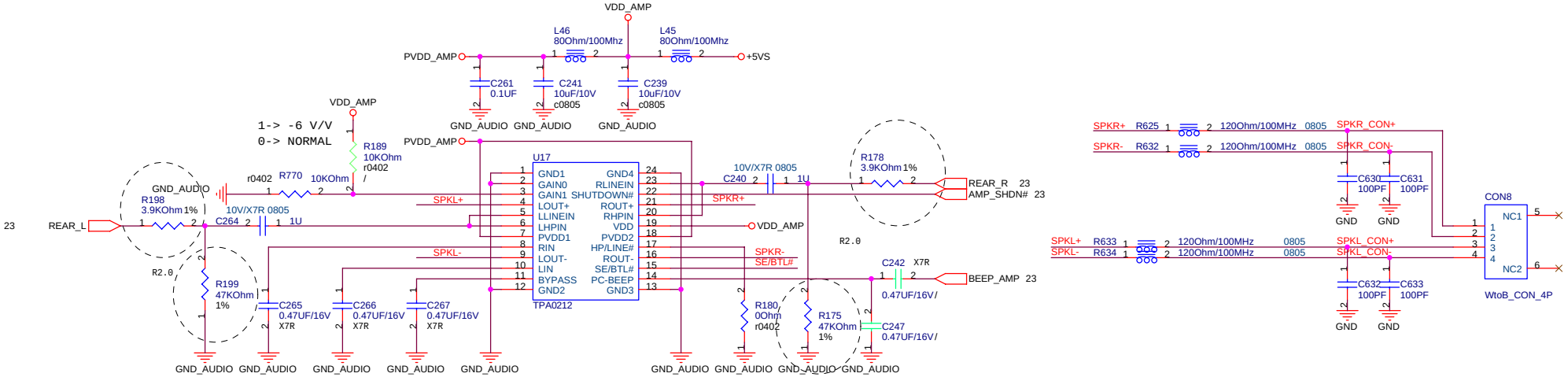
ASUSTeK COMPUTER INC	Title : FWH / SIO / SIR	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 22 of 53	

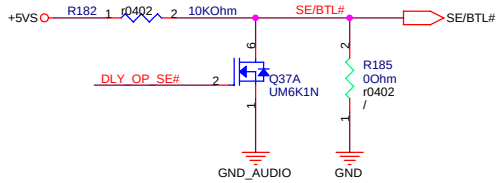


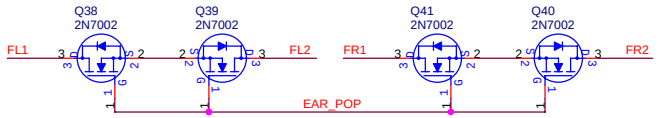
ALC880/ALC861

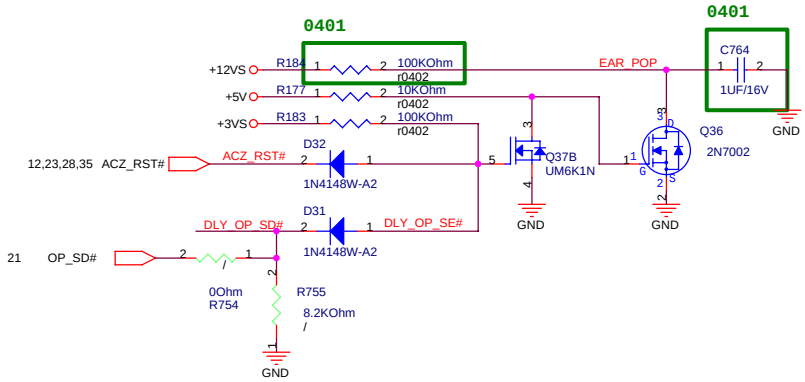


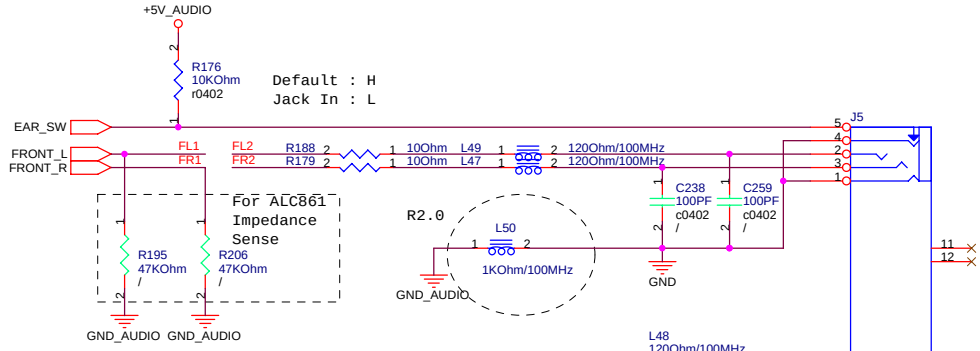
ASUSTek COMPUTER INC. NB1	Title : AZALIA		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 23 of 53		

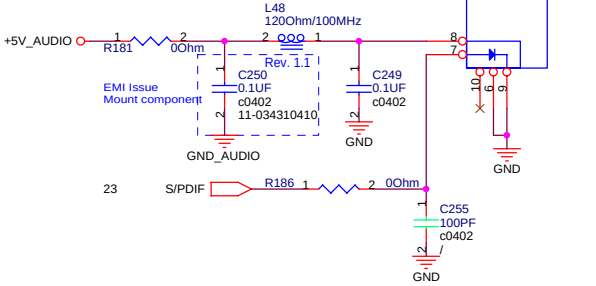


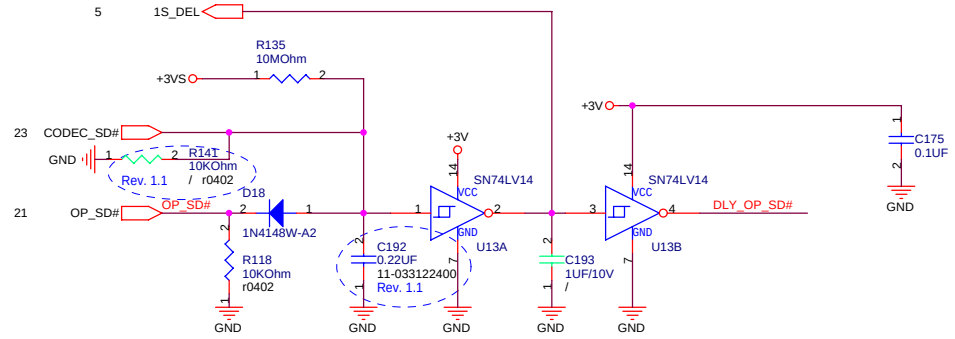












ASUSTeK COMPUTER INC

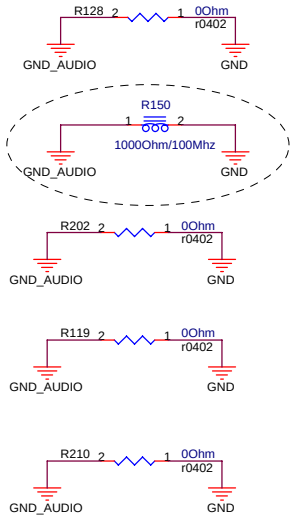
Title : 2 CHANNEL AMP

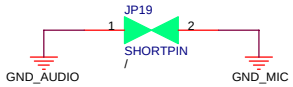
Engineer: Howard Tu

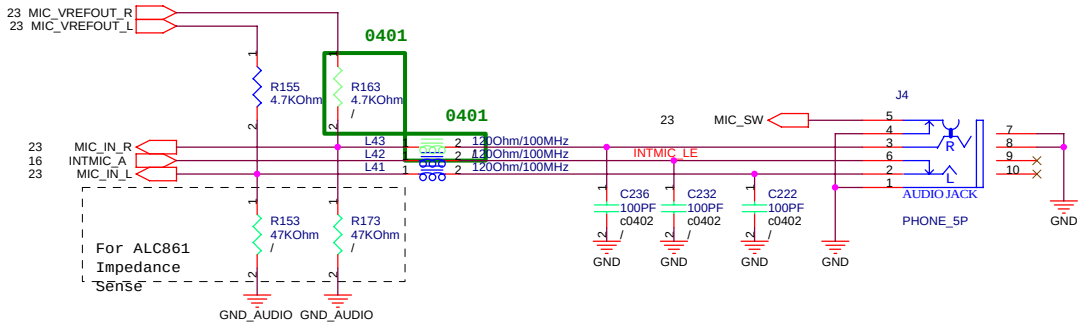
Size	Project Name	Rev
Custom	A3H	2.0

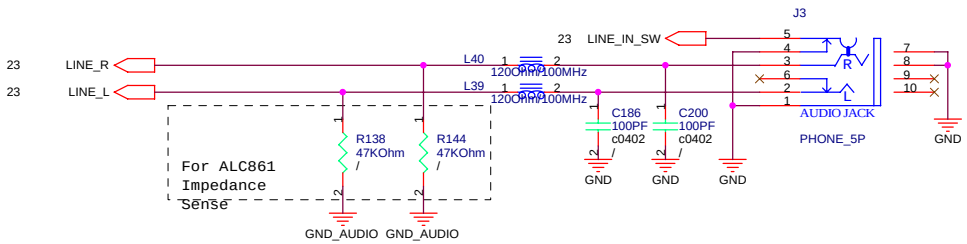
Date: Tuesday, August 09, 2005 Sheet 24 of 53

INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

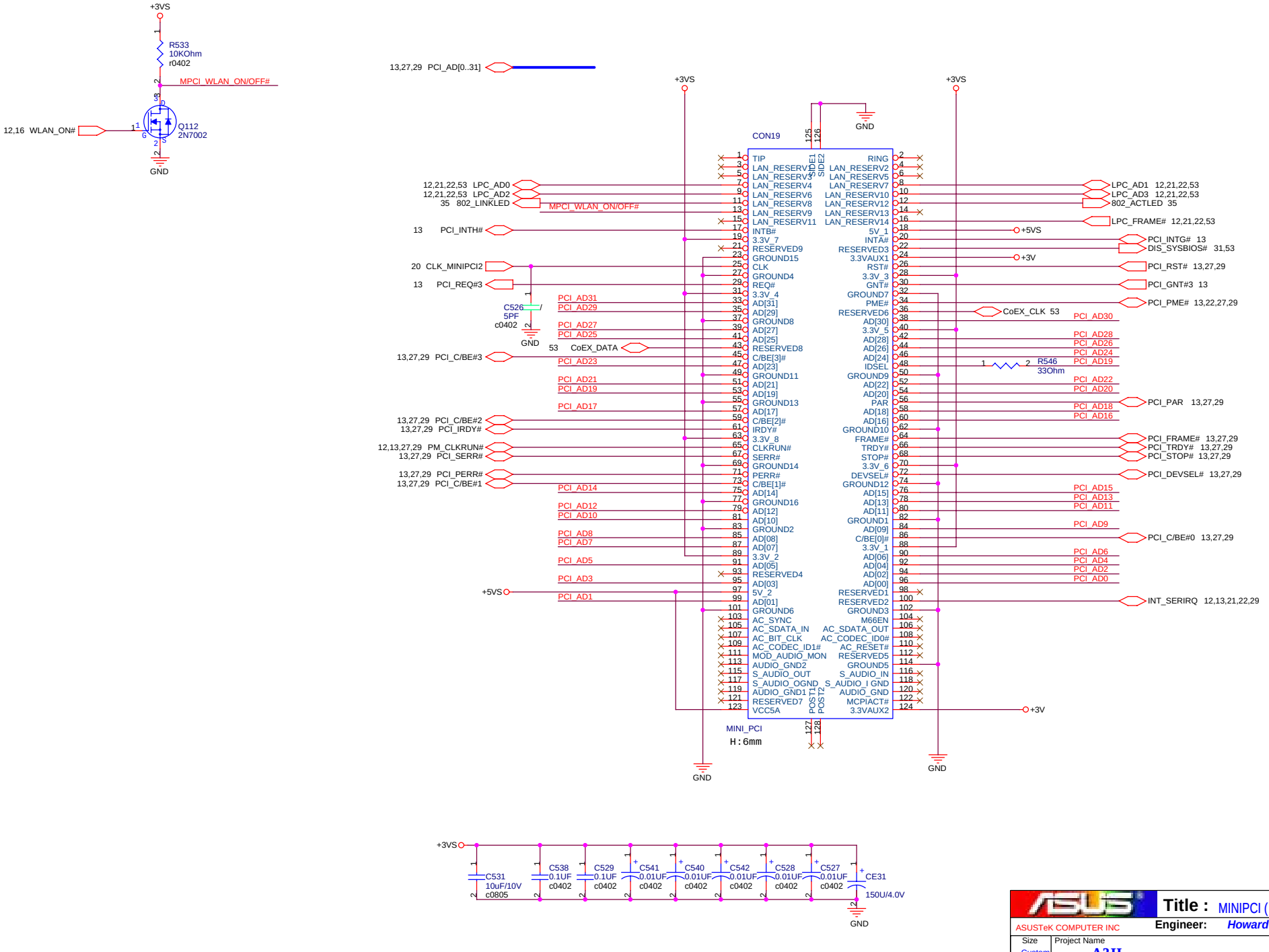




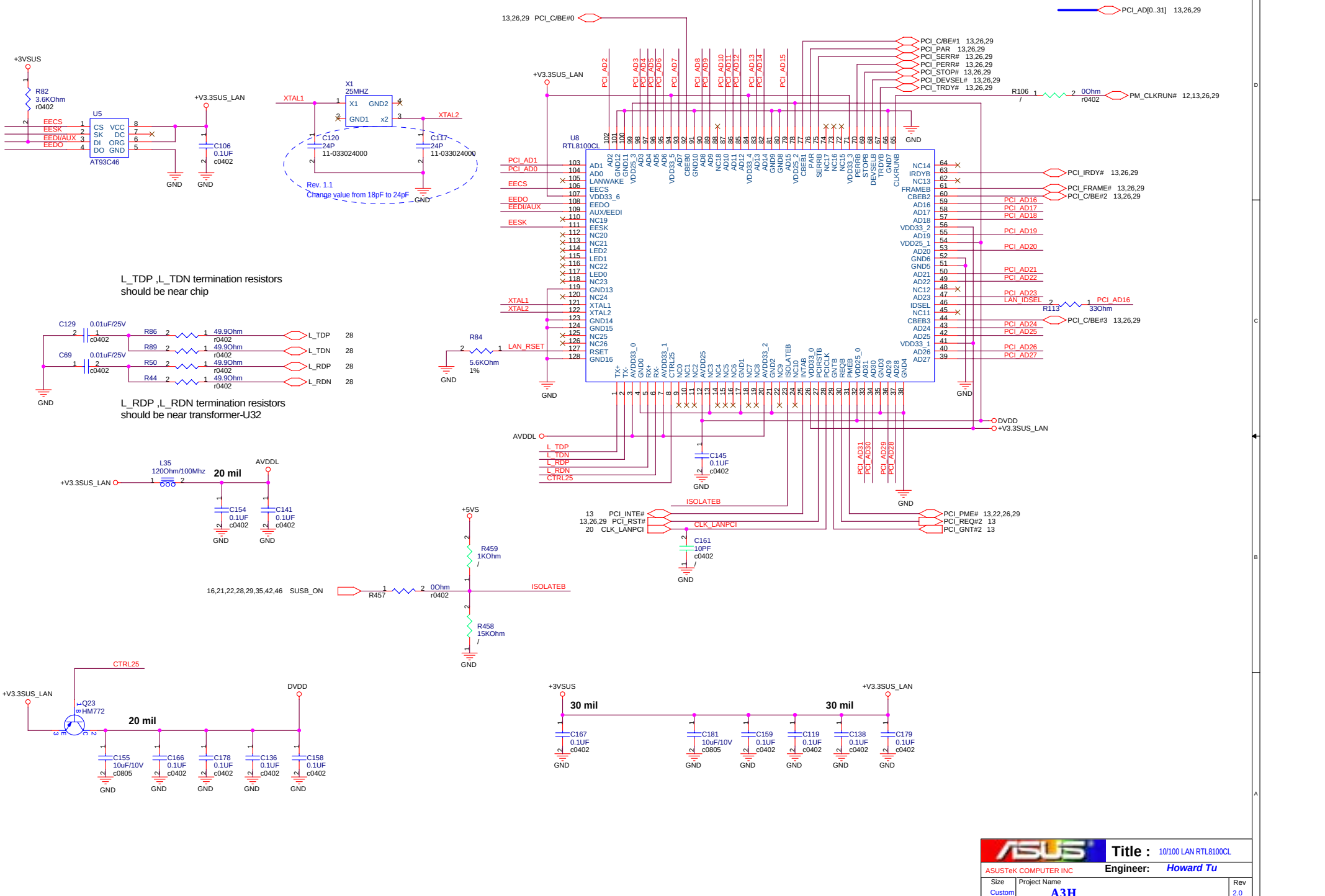




ASUSTeK COMPUTER INC	Title : MIC / Line-IN Jack	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 25 of 53	

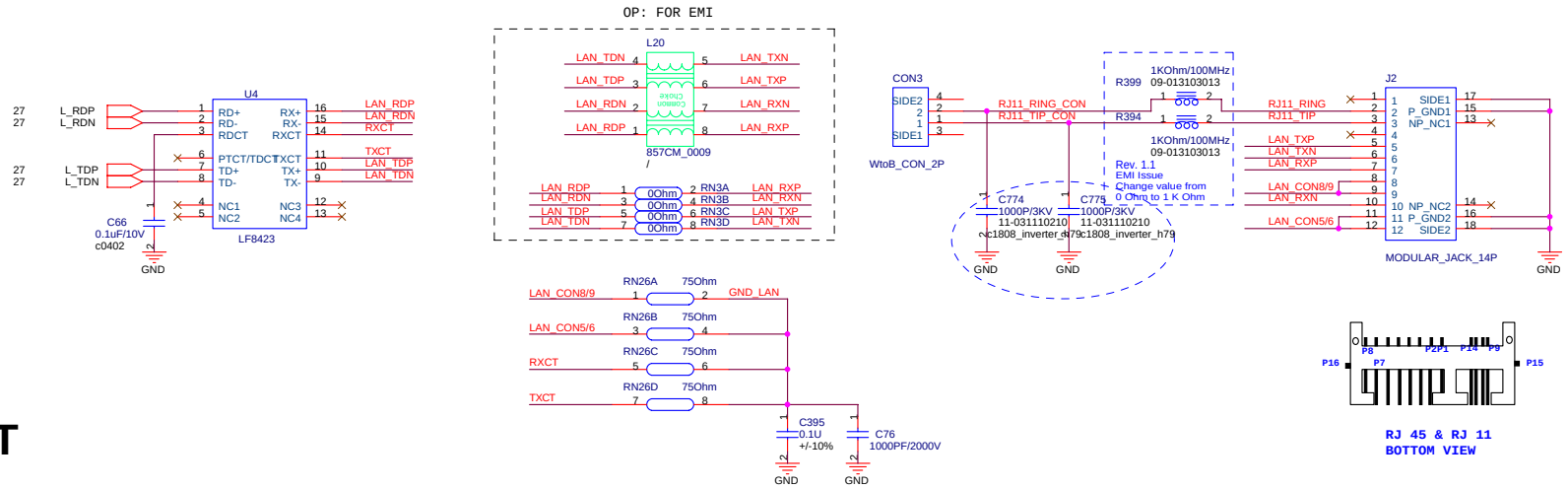


ASUSTeK COMPUTER INC	Title : MINIPCI (802.11)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 26 of 53	



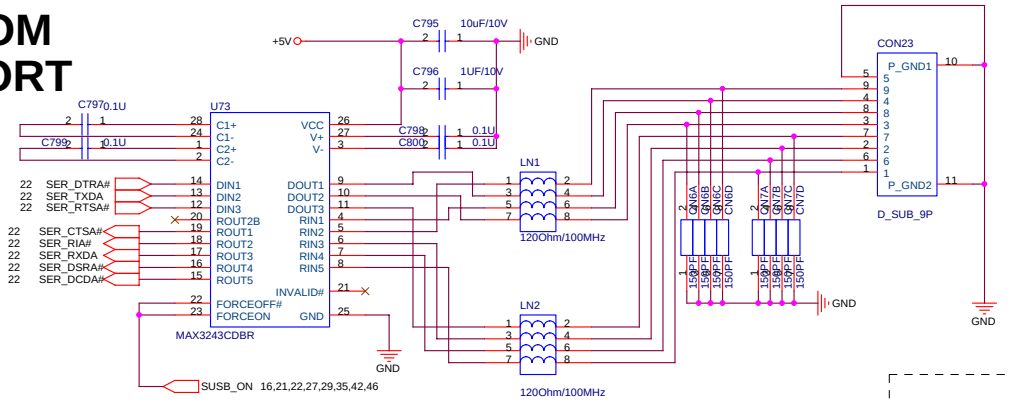
ASUSTeK COMPUTER INC	Title : 10/100 LAN RTL8100CL		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 27 of 53		

LAN PORT



RJ 45 & RJ 11
BOTTOM VIEW

COM PORT

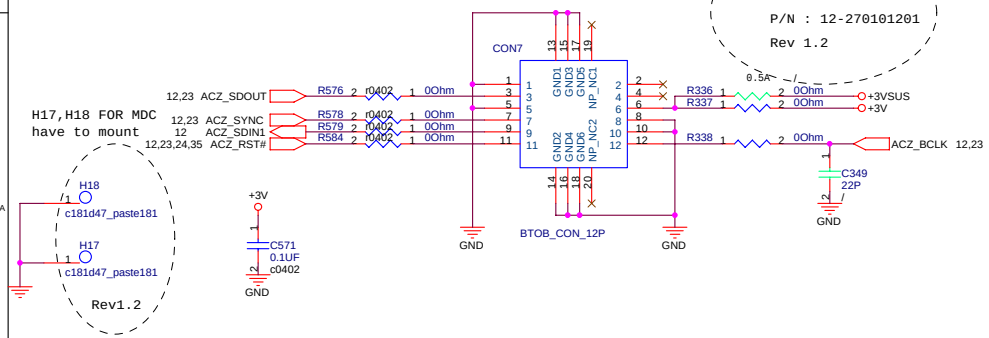


SWAP

PRINT PORT

MDC

P/N : 12-270101201
Rev 1.2



For MDC module

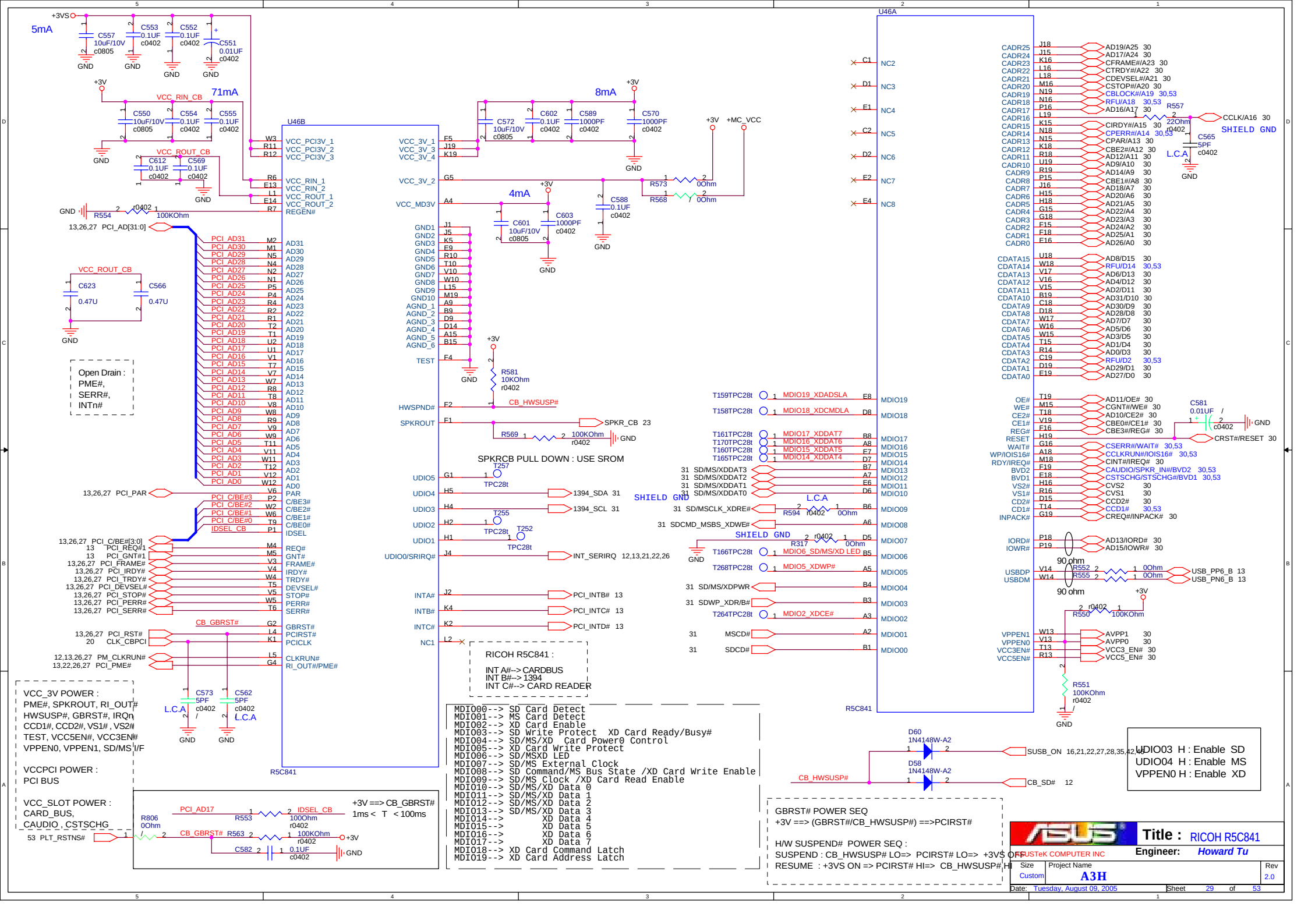
ASUSTeK COMPUTER INC

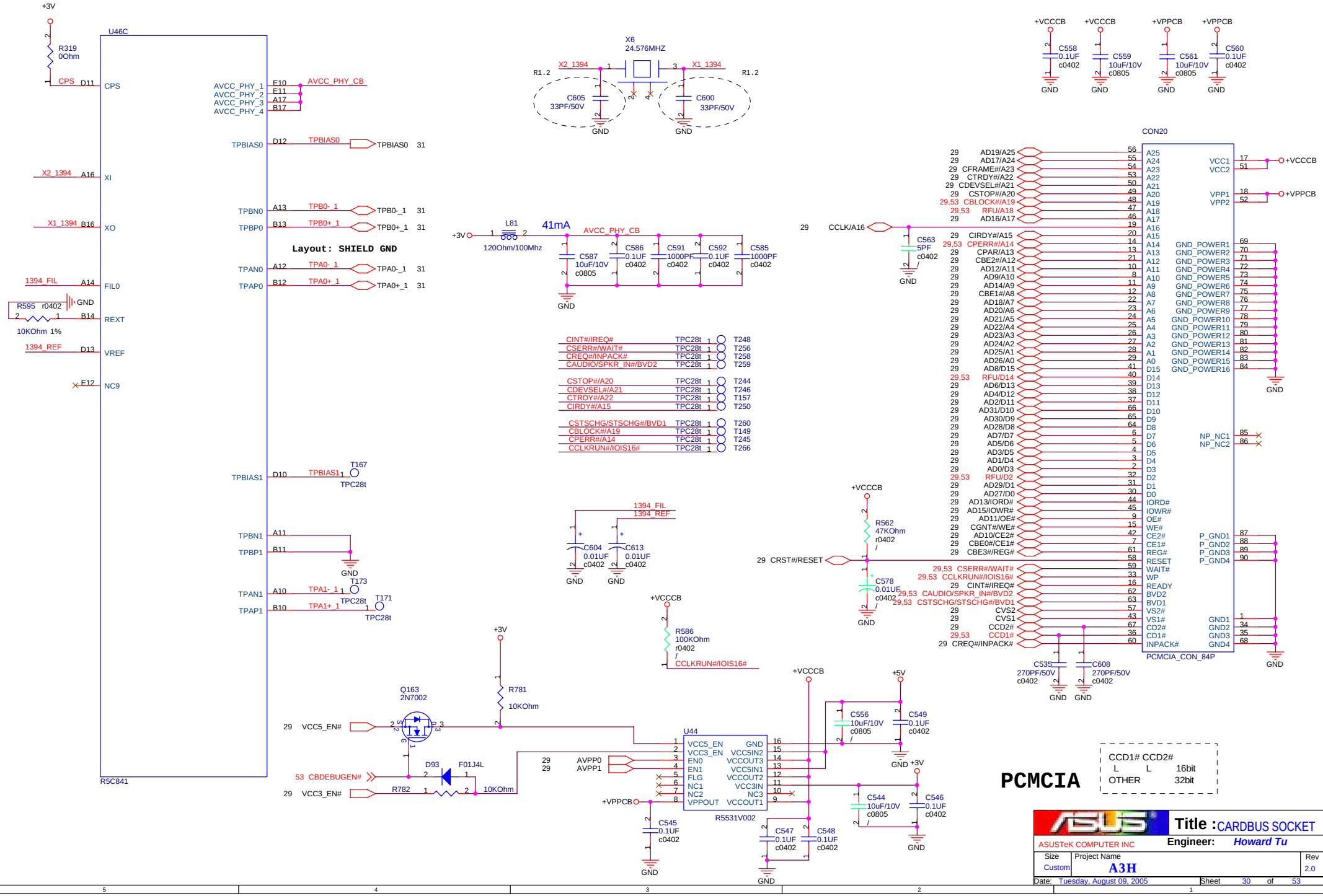
Title : RJ11+45,MDC,PRN

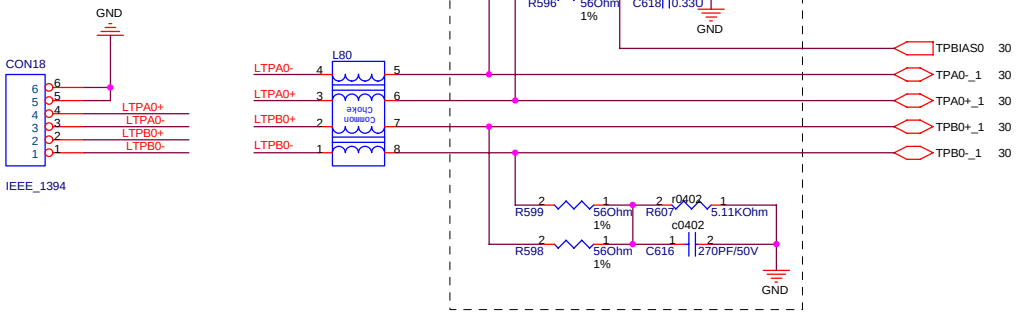
Engineer: Howard Tu

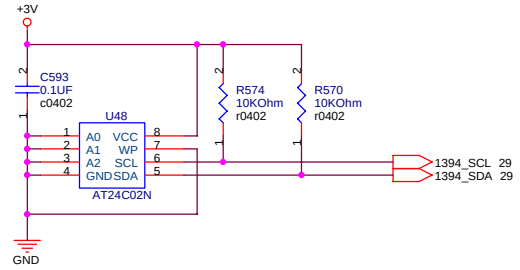
Size	Project Name	Rev
Custom	A3H	2.0

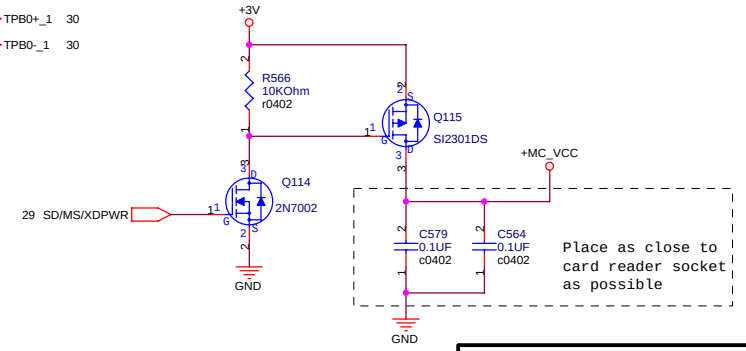
Date: Tuesday, August 09, 2005 Sheet 28 of 53


5mA
71mA
8mA
4mA
U46B
U46A
R5C841
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
Engineer: Howard Tu
ASUSTeK COMPUTER INC
Size: Custom
Project Name: A3H
Rev: 2.0
Date: Tuesday, August 09, 2005
Sheet 29 of 53


U46C
R5C841
Layout: SHIELD GND
X6
24.576MHZ
CON20
PCMCIA_CON_84P
U44
R5531V002
Q163
2N7002
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Project Name
A3H
Size
Custom
Rev
2.0
Date: Tuesday, August 09, 2005
Sheet 30 of 53





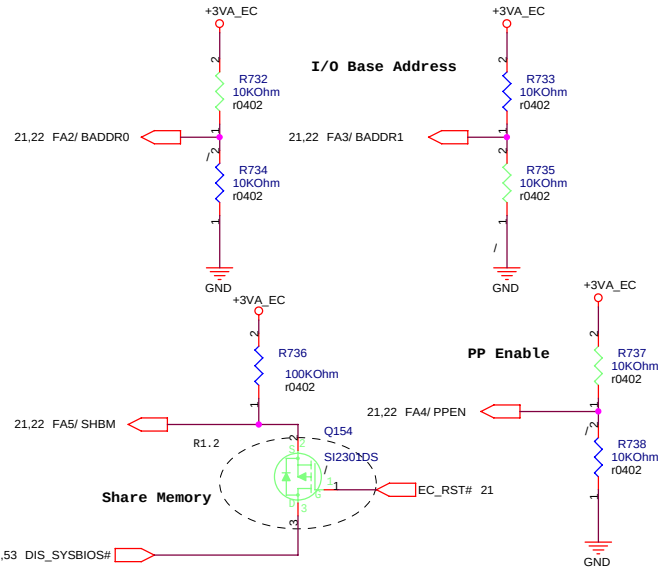


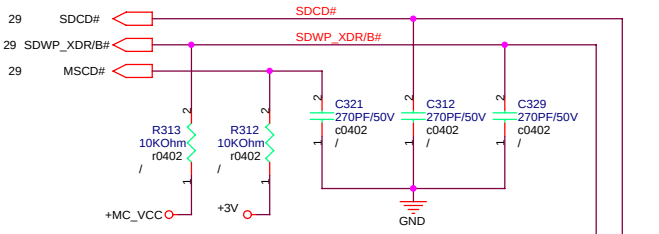
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

Hardware Strap Pin

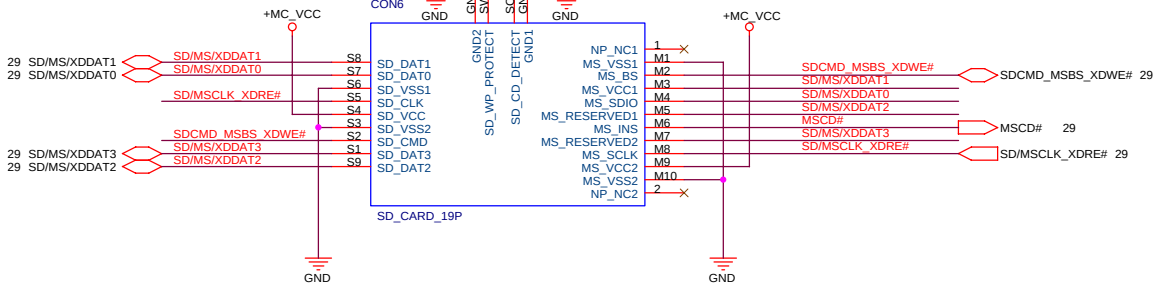
BADDR0/FA2	BADDR1/FA3	PORT
0	0	2E/2F
0	1	SWCBAHR/SWCBALR
1	0	4E/4F
1	1	RESERVED
FA4 0		FLASH TRI-STATE DISABLE
	1	FLASH TRI-STATE ENABLE
FA5 0		SHARE HOST BIOS MEMORY DISABLE
	1	SHARE HOST BIOS MEMORY ENABLE

EC Hardware Strap

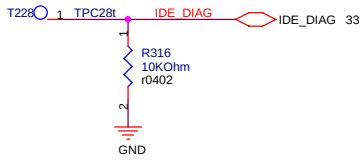




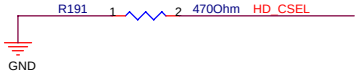
Layout: SHIELD GND

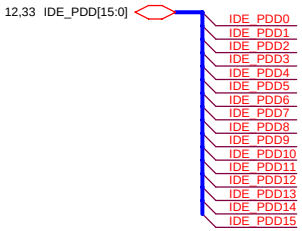


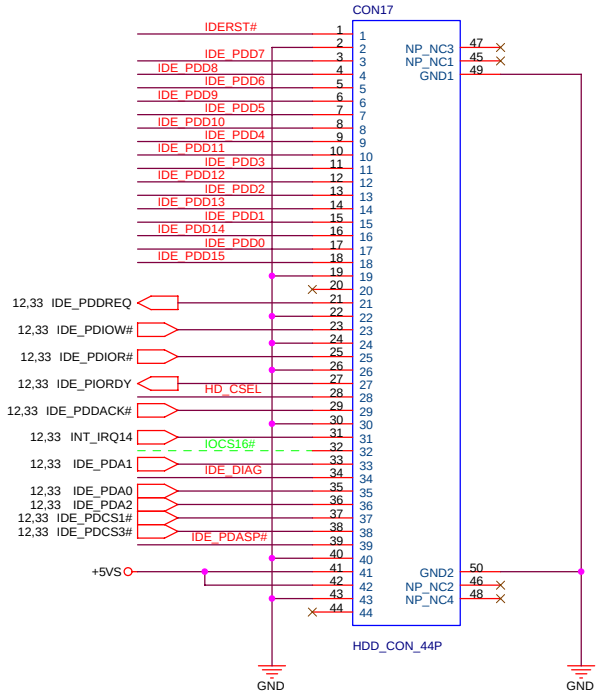
ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 31 of 53		

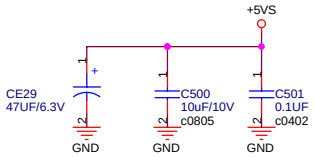


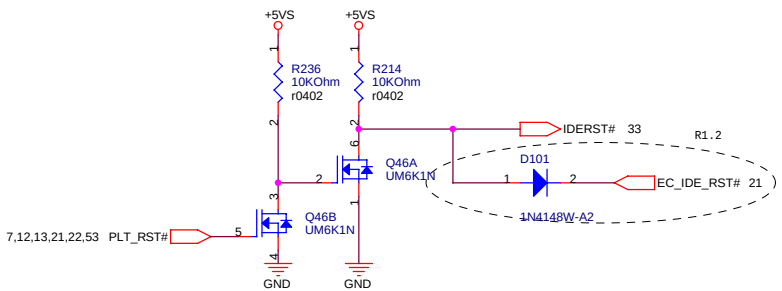
HD_CSEL : Pull-Down, HDD as Master

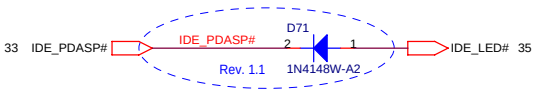












ASUSTeK COMPUTER INC	Title : HDD CONNECTOR	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 32 of 53	

For EMI test (place on TOP layer)

0119

stitching cap.

+VCCP

C760
0.1uF/10V
c0402

GND

+VCC_GMCH_CORE

C763

+1.5VS

0.1uF/10V
c0402

12,32 IDE_PDD[15:0]

+5VS

+5VS

R335
10KOhm
r0402

R354
10KOhm
r0402

CON21

P_GND1

NP_NC1

23 CD_R_A

CD_GND_A

IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15

12,32 IDE_PDDREQ
IDE_PDDREQ
12,32 IDE_PDIOR#
IDE_PDIOR#

12,32 IDE_PDDACK#
IDE_PDDACK#

32 IDE_DIAG
IDE_DIAG
12,32 IDE_PDA2
IDE_PDA2
12,32 IDE_PDCS3#
IDE_PDCS3#

IDERST#
IDE_PDD7
IDE_PDD6
IDE_PDD5
IDE_PDD4
IDE_PDD3
IDE_PDD2
IDE_PDD1
IDE_PDD0

IDE_PDIOW#
IDE_PIORDY
INT_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDASP#

CD_L_A 23
CD_GND_A 23
IDERST# 32

IDE_PDIOW# 12,32
IDE_PIORDY 12,32
INT_IRQ14 12,32
IDE_PDA1 12,32
IDE_PDA0 12,32
IDE_PDCS1# 12,32
IDE_PDASP# 32

R217 0Ohm

Change net name from IDE_PDASP#2 to IDE_PDASP# Rev. 1.1

CD_CSEL

cd_rom_50p2

P_GND2

NP_NC2

C323
0.1UF
c0402

C326
10uF/10V
c0805

GND

+5VS

R310
470Ohm

R311
470Ohm

Rev. 1.1

CD_CSEL

CD_CSEL:
Pull-Down is Master
Pull-High is Slave

Rev 1.2

H28
H29
H30
H31
H32
H33
C28D28N

stamp hole

H8
H7
H6
H9
C268D138

GND

CPU

H1
H11
H19
H14
H16
H21
H3
H5
H12
H15
H22
H13
H4
H10
C91D91N

H2
H20
C79D79N

H24
H25
H23
c181d47_paste181

ALVISO

0401

H26
CT197CB87D47
13-N7K10M340

H27
CT197CB87D47
13-N7K10M340

Holes for ALVISO have to mount

R110
0Ohm
r0402

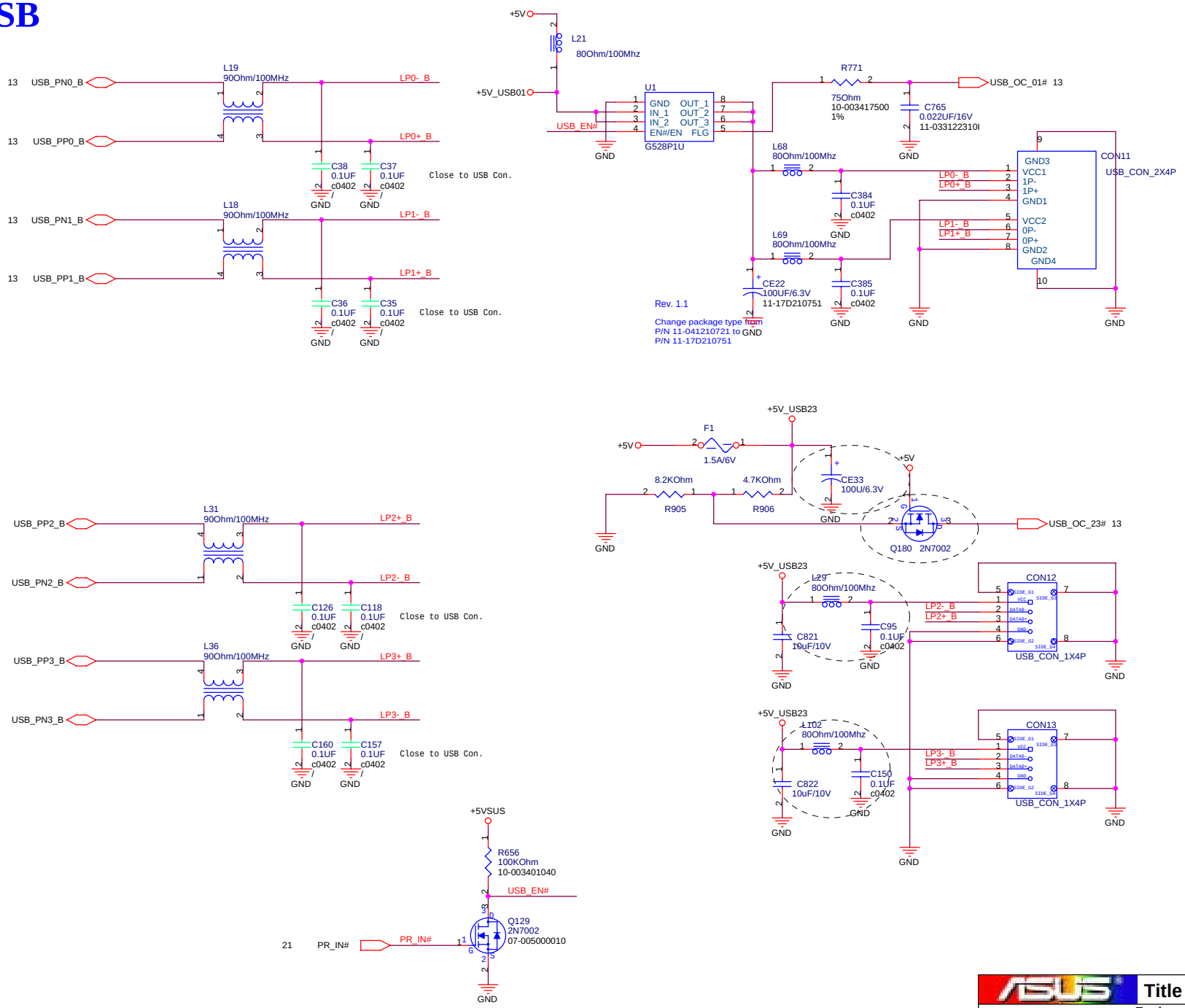
R111
0Ohm
r0402

SN74LV14
VCC
GND
U13F
U13E

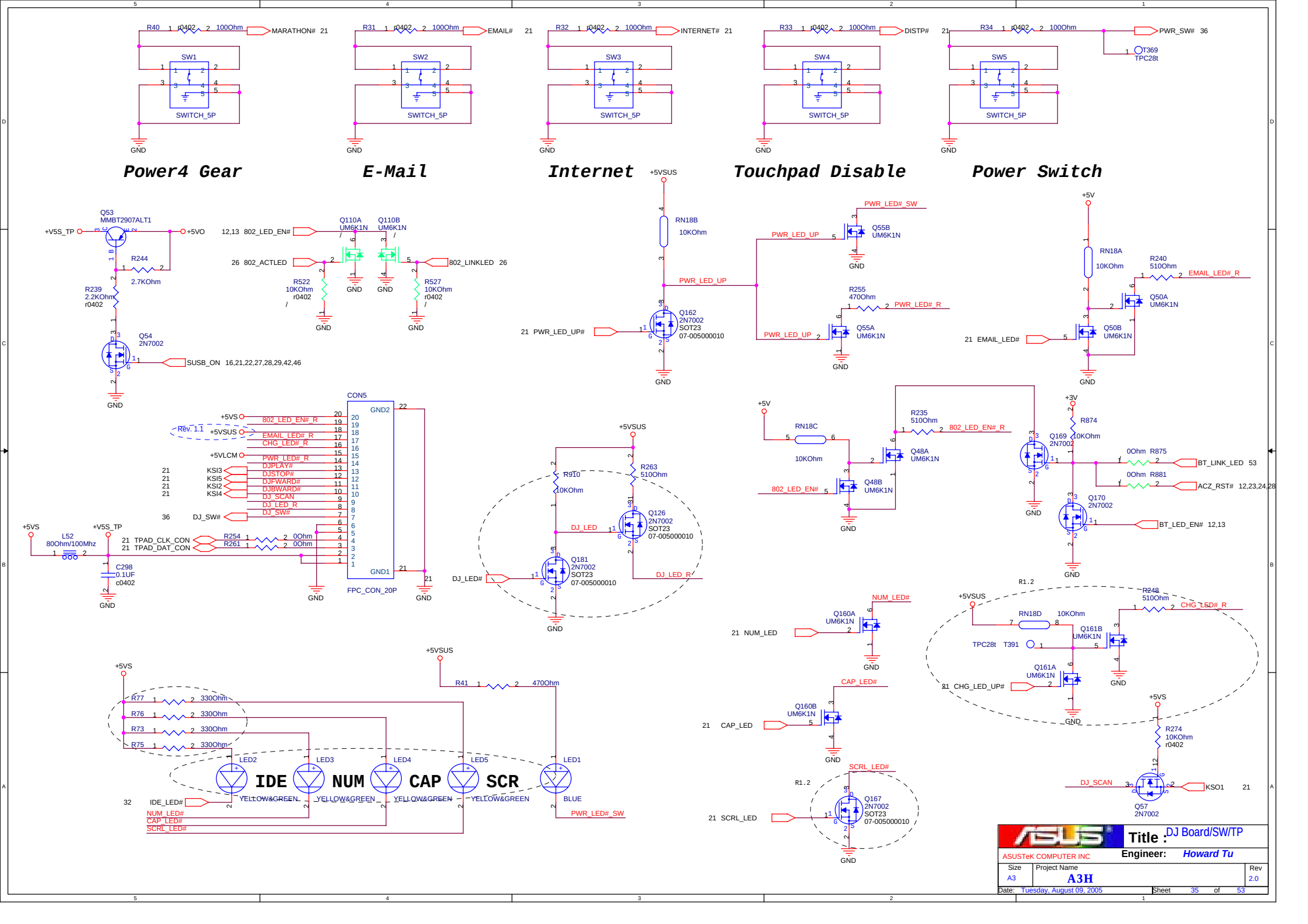
GND

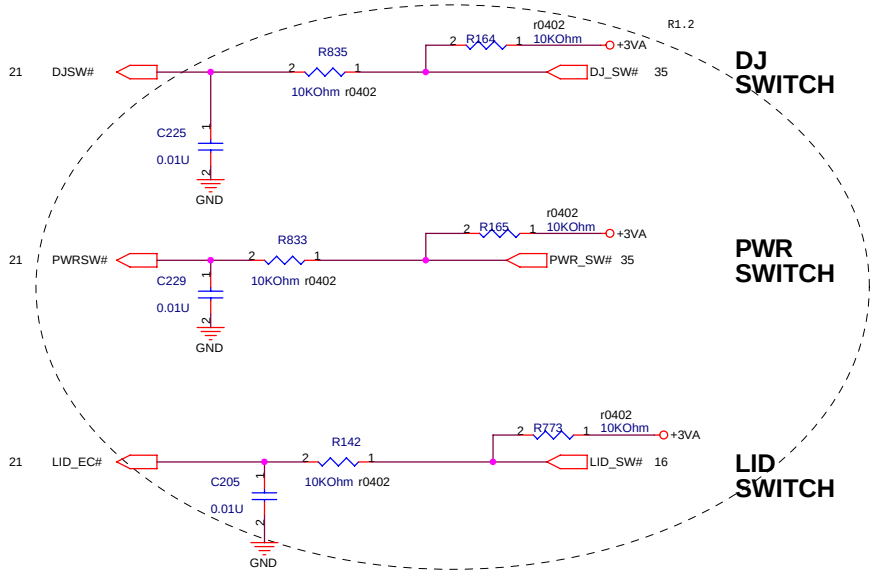
Title : CDROM		
ASUSTeK COMPUTER INC	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 33 of 53	

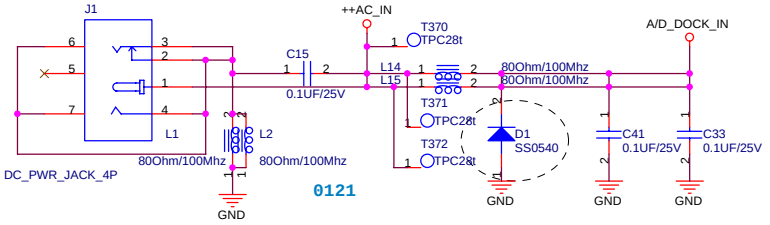
USB

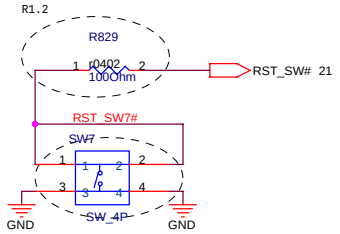


ASUSTeK COMPUTER INC	Title : USB CONN		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 34 of 53		


R40 r0402 100Ohm MARATHON# 21
SW1 SWITCH_5P
GND
Power4 Gear
R31 r0402 100Ohm EMAIL# 21
SW2 SWITCH_5P
GND
E-Mail
R32 r0402 100Ohm INTERNET# 21
SW3 SWITCH_5P
GND
Internet
R33 r0402 100Ohm DISTP# 21
SW4 SWITCH_5P
GND
Touchpad Disable
R34 r0402 100Ohm PWR_SW# 36
T369 TPC28t
SW5 SWITCH_5P
GND
Power Switch
Q53 MMBT2907ALT1
+V5S_TP
+5VO
R244 2.7KOhm
R239 2.2KOhm r0402
Q54 2N7002
SUSB_ON 16,21,22,27,28,29,42,46
GND
12,13 802_LED_EN#
Q110A UM6K1N
Q110B UM6K1N
26 802_ACTLED
802_LINKLED 26
R522 10KOhm r0402
R527 10KOhm r0402
GND
+5VSUS
RN18B 10KOhm
PWR_LED_UP
21 PWR_LED_UP#
Q162 2N7002 SOT23 07-005000010
PWR_LED# SW
Q55B UM6K1N
Q55A UM6K1N
R255 470Ohm
PWR_LED# R
+5V
RN18A 10KOhm
R240 510Ohm
EMAIL_LED# R
Q50A UM6K1N
Q50B UM6K1N
21 EMAIL_LED#
CON5
FPC_CON_20P
Rev. 1.1
+5VS
+5VSUS
+5VLCM
802_LED_EN# R
EMAIL_LED# R
CHG_LED# R
PWR_LED# R
DJPLAY#
DJSTOP#
DJFWARD#
DJBWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
21 KSI3
21 KSI5
21 KSI2
21 KSI4
36 DJ_SW#
GND1
GND2
21 TPAD_CLK_CON
21 TPAD_DAT_CON
R254 0Ohm
R261 0Ohm
L52 80Ohm/100Mhz
C298 0.1UF c0402
R910 10KOhm
R263 510Ohm
Q126 2N7002 SOT23 07-005000010
Q181 2N7002 SOT23 07-005000010
DJ_LED
DJ_LED#
DJ_LED_R
RN18C 10KOhm
R235 510Ohm
802_LED_EN# R
Q48A UM6K1N
Q48B UM6K1N
+3V
R874 10KOhm
Q169 2N7002
Q170 2N7002
0Ohm R875
0Ohm R881
BT_LINK_LED 53
ACZ_RST# 12,23,24,28
BT_LED_EN# 12,13
R41 470Ohm
R77 330Ohm
R76 330Ohm
R73 330Ohm
R75 330Ohm
LED1 BLUE
LED2 YELLOW&GREEN
LED3 YELLOW&GREEN
LED4 YELLOW&GREEN
LED5 YELLOW&GREEN
IDE
NUM
CAP
SCR
32 IDE_LED#
NUM_LED#
CAP_LED#
SCRL_LED#
PWR_LED# SW
Q160A UM6K1N
Q160B UM6K1N
Q161A UM6K1N
Q161B UM6K1N
21 NUM_LED
21 CAP_LED
21 SCRL_LED
21 CHG_LED_UP#
R1.2
R248 510Ohm
CHG_LED# R
RN18D 10KOhm
TPC28t T391
R274 10KOhm r0402
DJ_SCAN
KSO1 21
Q57 2N7002
Q167 2N7002 SOT23 07-005000010
Title : DJ Board/SW/TP
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size A3
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 35 of 53





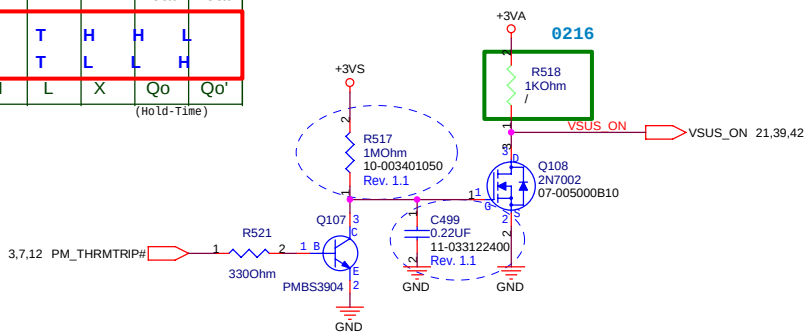


74HC74 TRUTH TABLE

Rev 1.2

PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

(Hold-Time)



System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.5VS, +2.5V, +VCCP
SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS
M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS

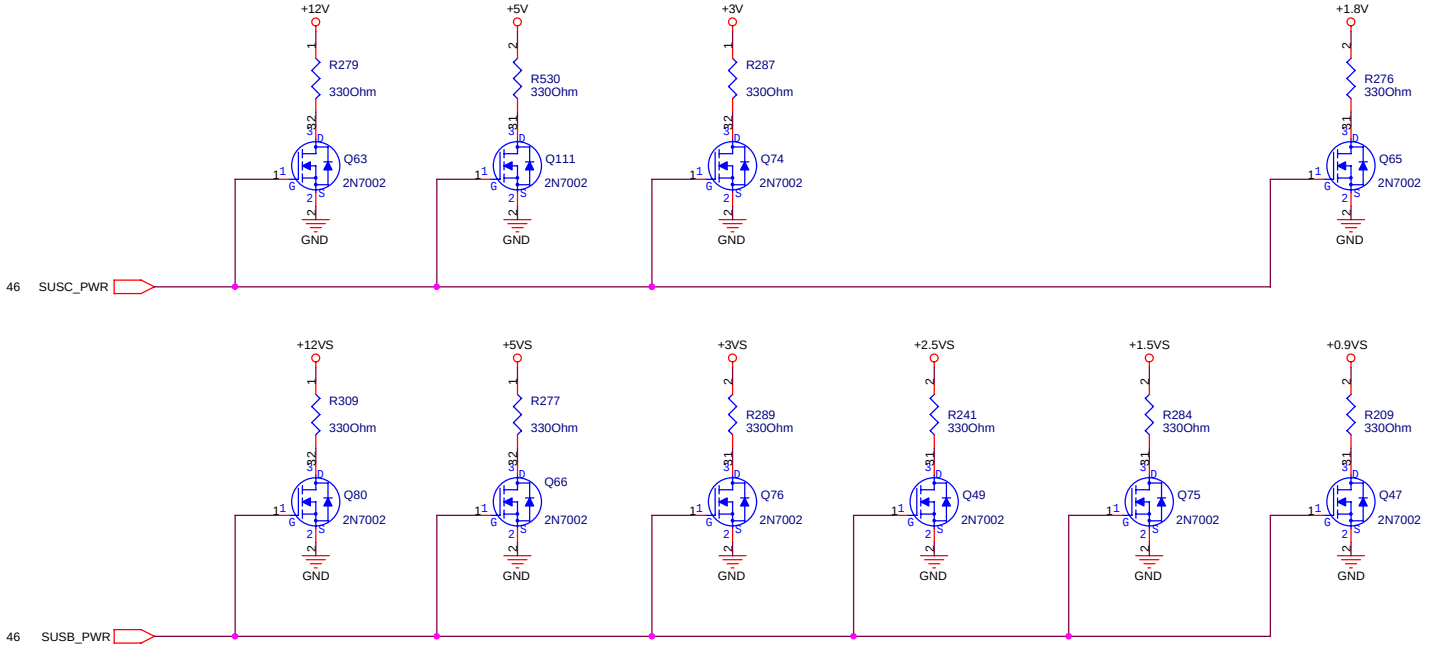
ASUSTeK COMPUTER INC

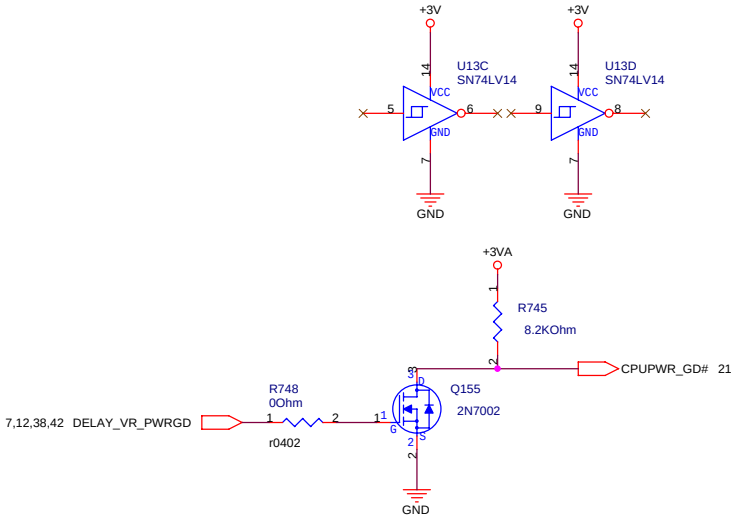
Title : Startup Circuit (1)

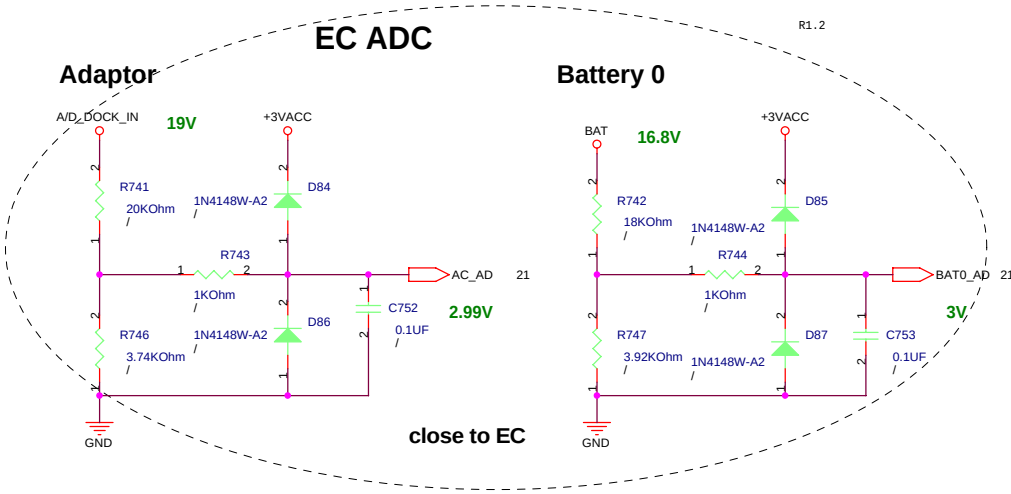
Engineer: Howard Tu

Size	Project Name	Rev
Custom	A3H	2.0

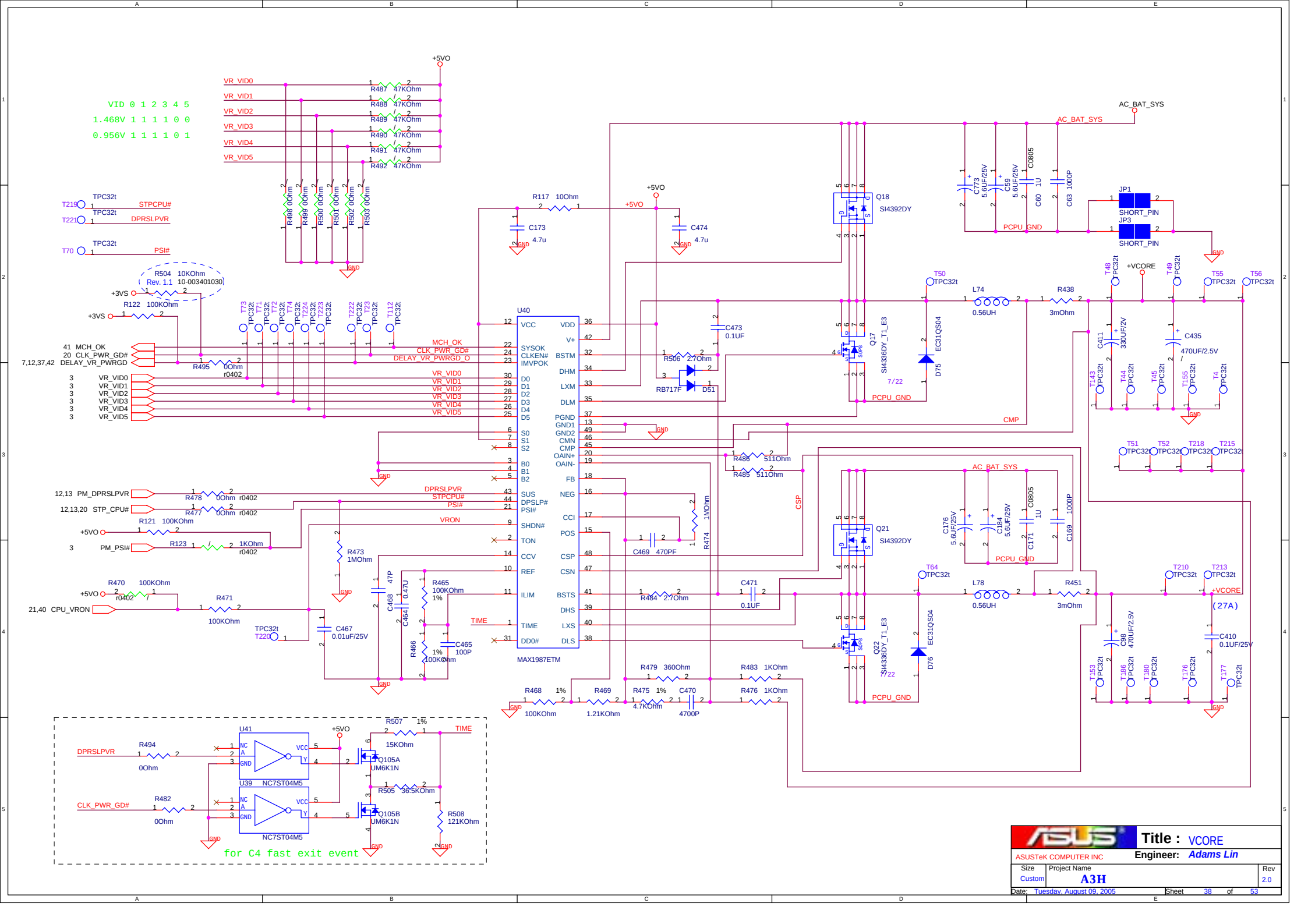
Date: Tuesday, August 09, 2005 Sheet 36 of 53







ASUSTeK COMPUTER INC	Title : Startup Circuit (2)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 37 of 53	


VID 0 1 2 3 4 5
1.468V 1 1 1 1 0 0
0.956V 1 1 1 1 0 1
MAX1987ETM
for C4 fast exit event
Title : VCORE
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
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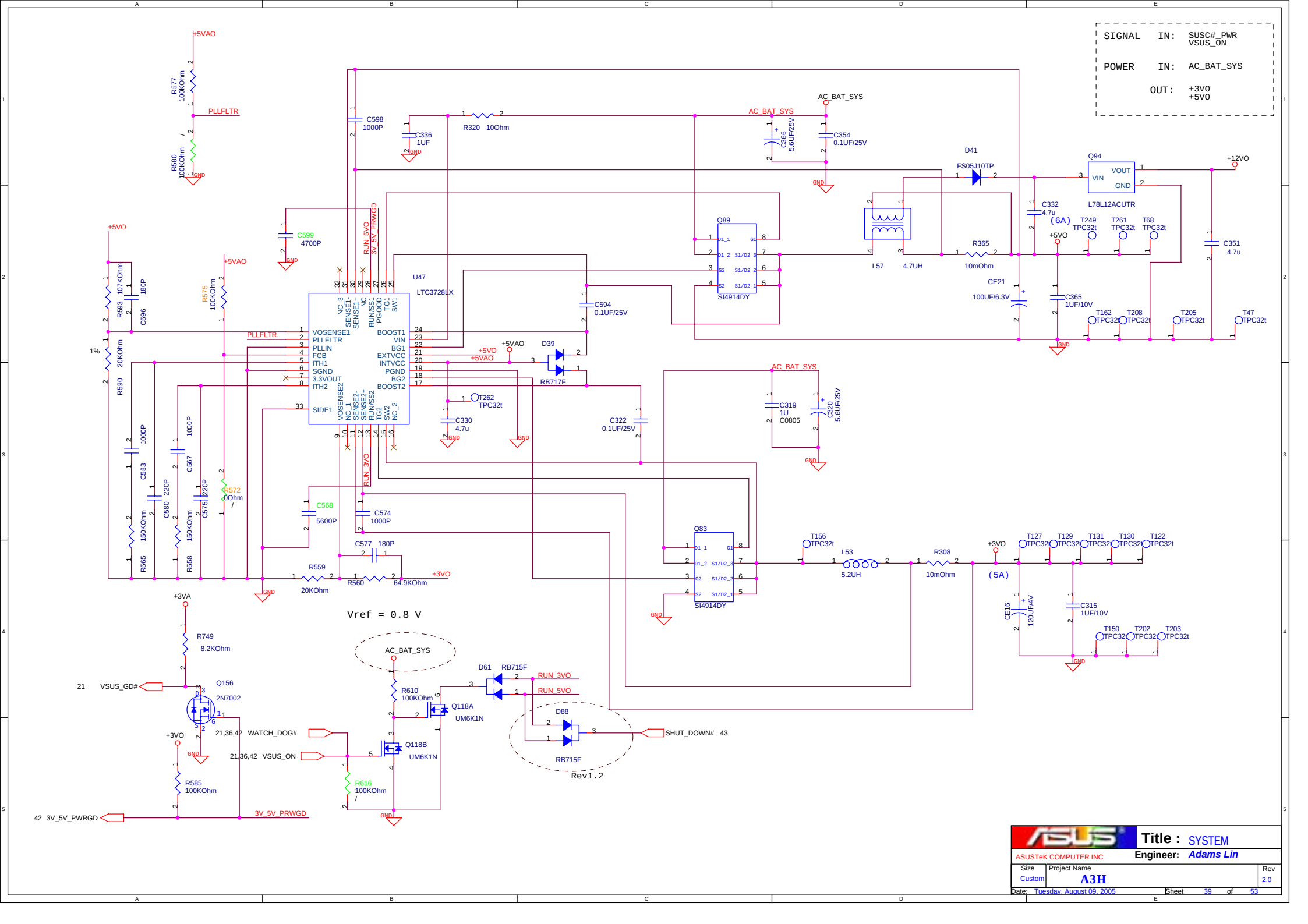
SIGNAL IN: SUSC#_PWR
VSUS_ON
POWER IN: AC_BAT_SYS
OUT: +3VO
+5VO
U47
LTC3728LX
Q89
SI4914DY
Q83
SI4914DY
Q94
L78L12ACUTR
D41
FS05J10TP
D39
RB717F
D61
RB715F
D88
RB715F
Q156
2N7002
Q118A
UM6K1N
Q118B
UM6K1N
L57 4.7UH
L53 5.2UH
R308 10mOhm
R365 10mOhm
R320 10Ohm
R559 20KOhm
R560 64.9KOhm
Vref = 0.8 V
Rev1.2
Title : SYSTEM
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
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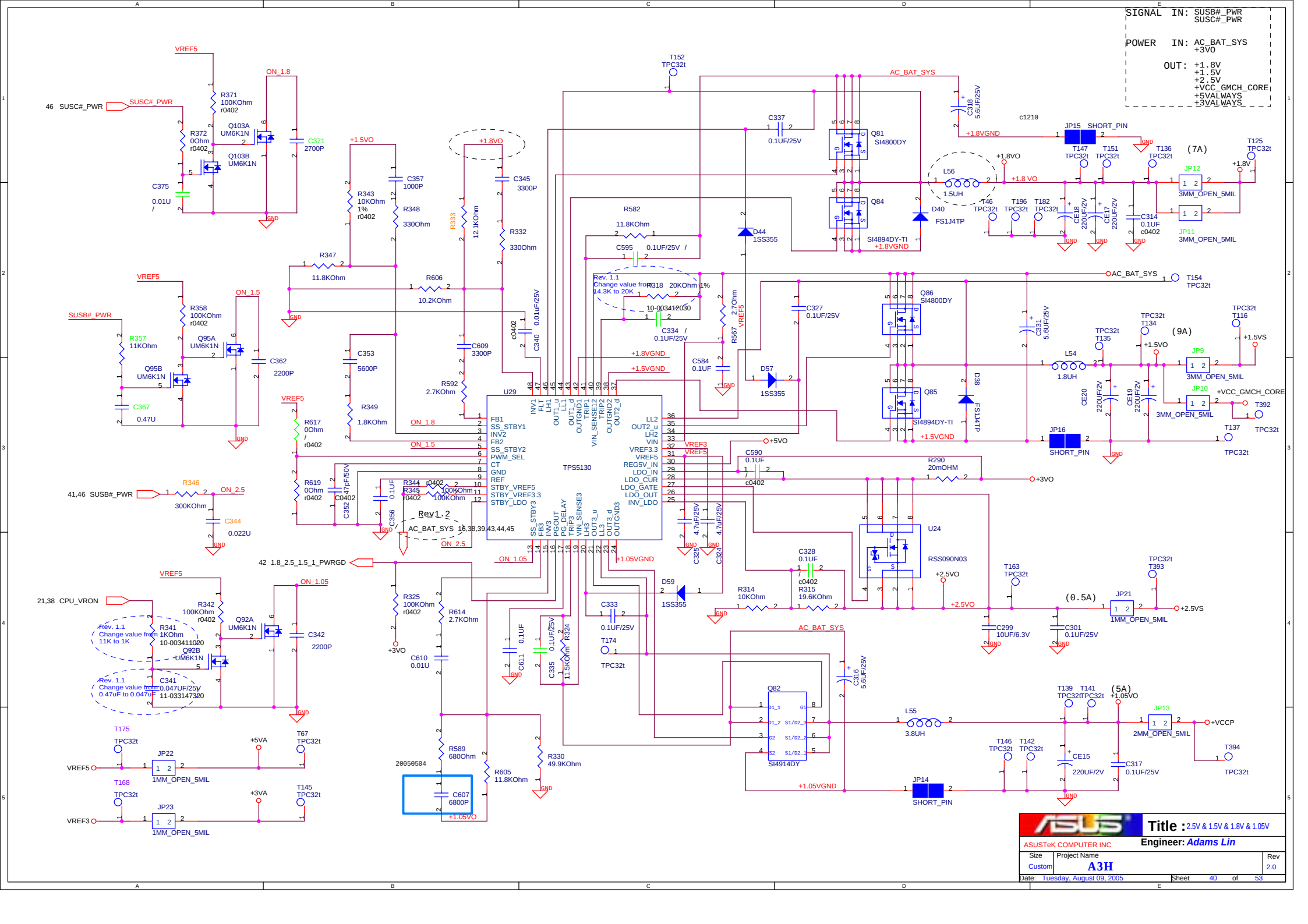

SIGNAL IN: SUSB#_PWR
SUSC#_PWR
POWER IN: AC_BAT_SYS
+3VO
OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS
TPS5130
Rev1.2
RSS090N03
SI4914DY
SI4894DY-TI
SI4800DY
FS1J4TP
1SS355
Title : 2.5V & 1.5V & 1.8V & 1.05V
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Project Name A3H
Size Custom
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 40 of 53

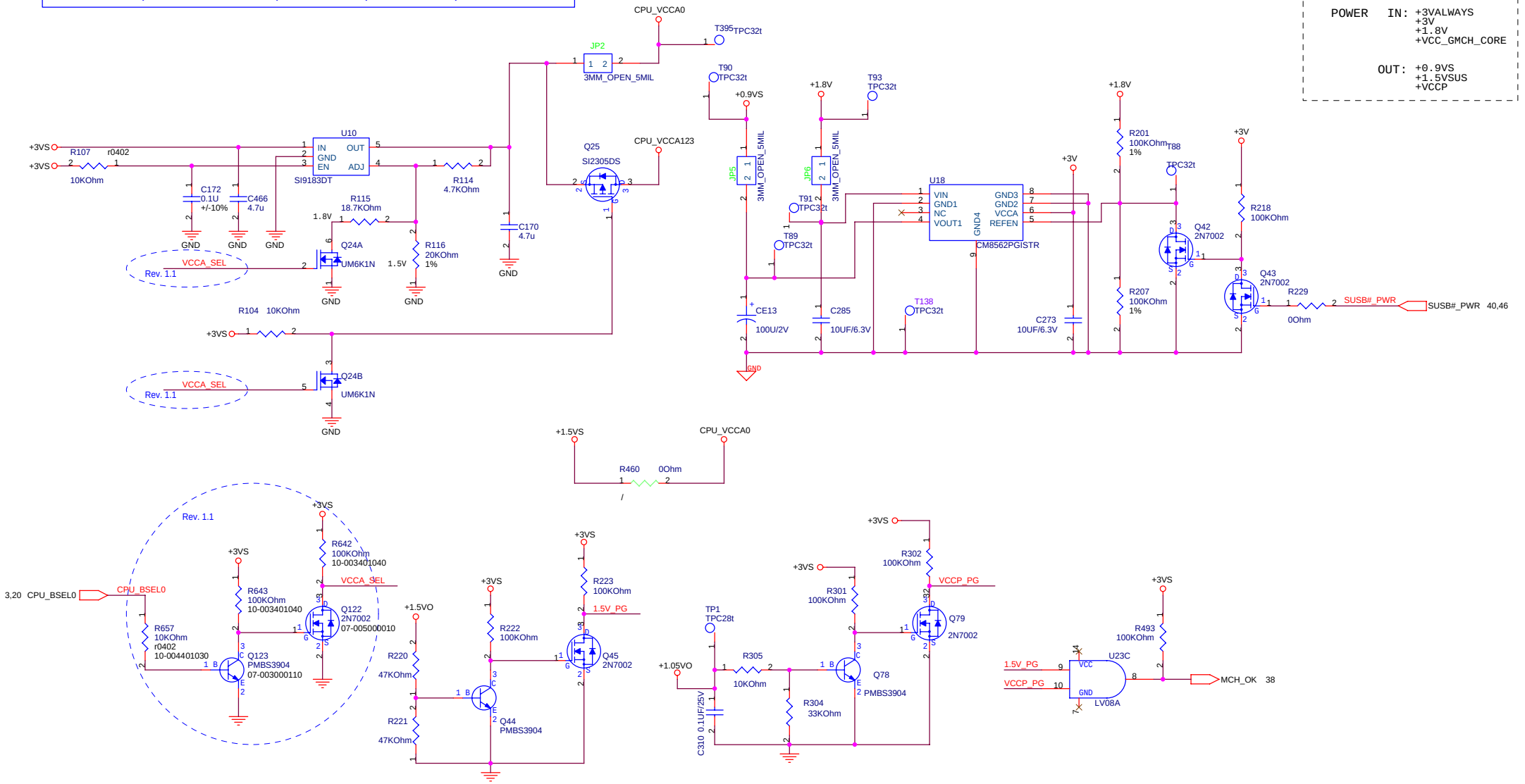
For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V

For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

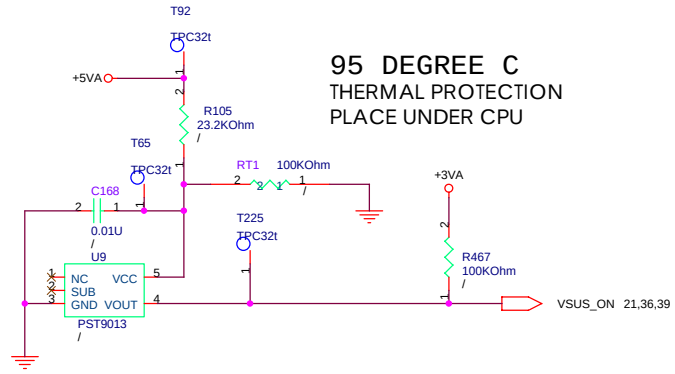
SIGNAL IN: SUSB#_PWR
CPU_VRON

POWER IN: +3VALWAYS
+3V
+1.8V
+VCC_GMCH_CORE

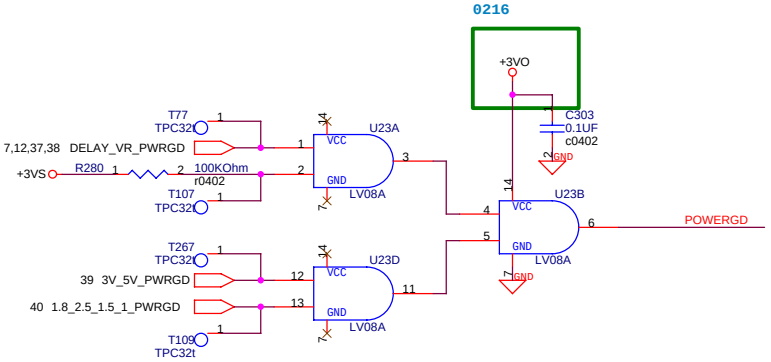
OUT: +0.9VS
+1.5VSUS
+VCCP

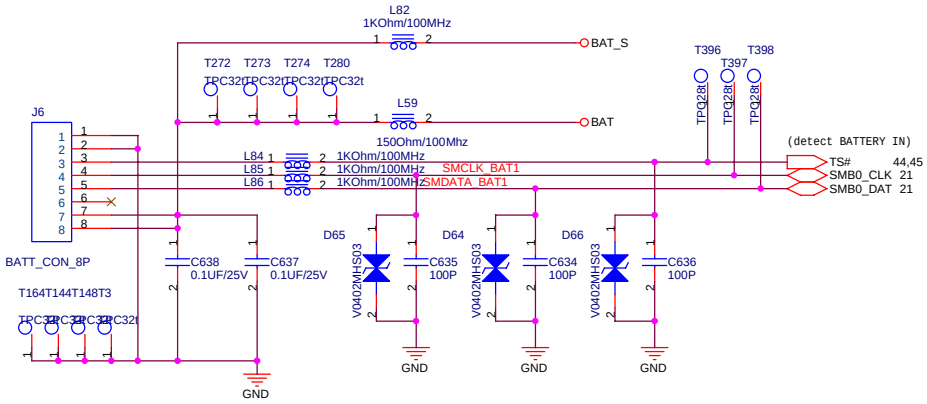


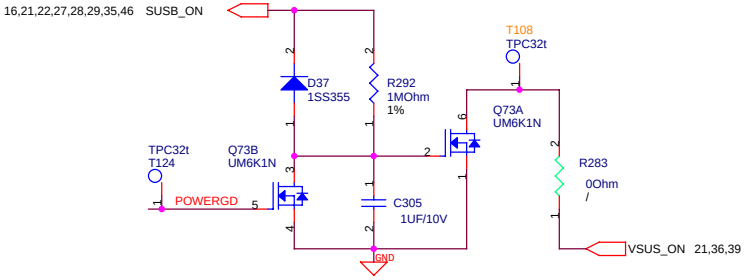
ASUSTeK COMPUTER INC	Title : 1.5VA & DDR2	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 41 of 53	



95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU







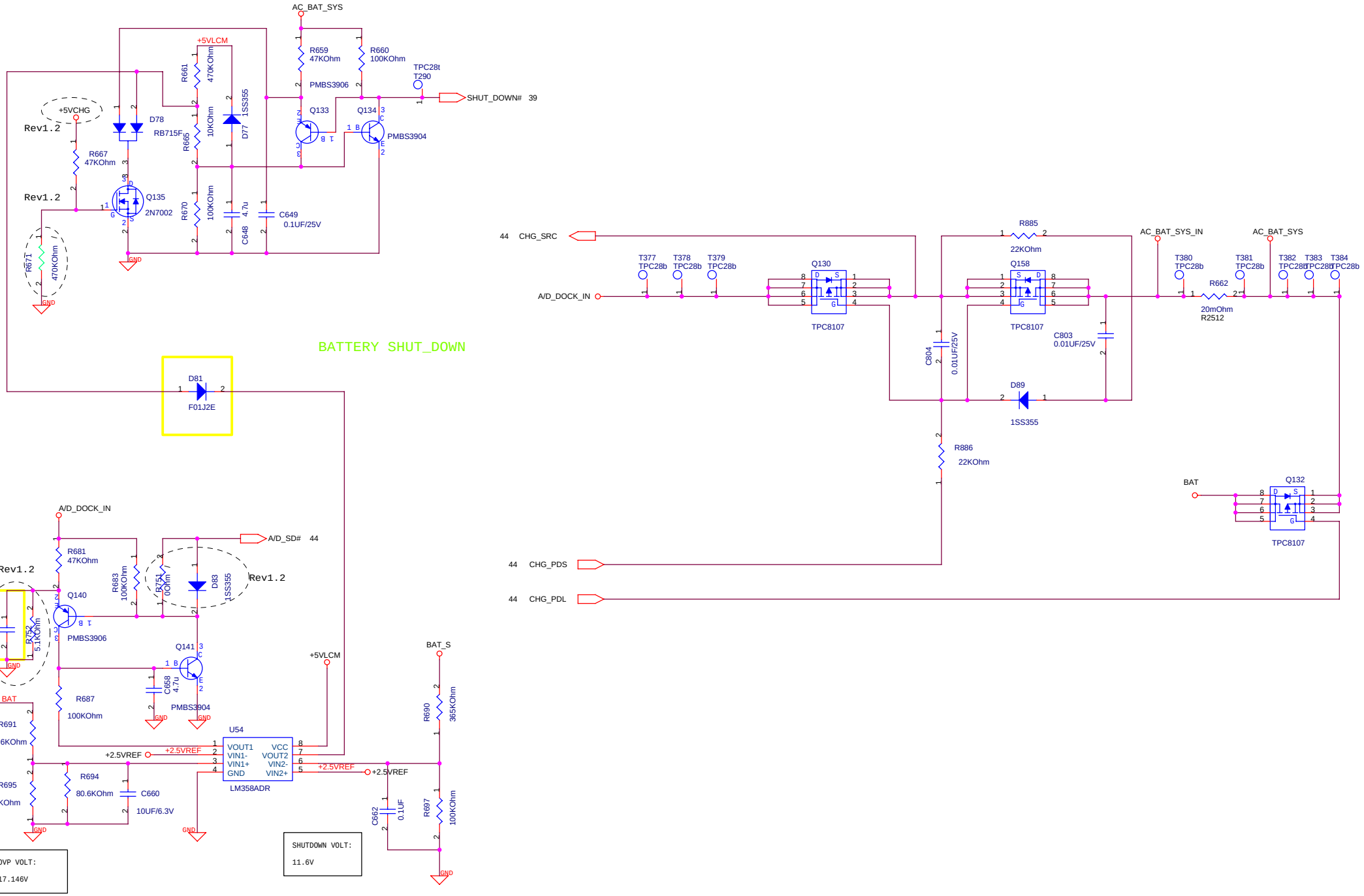
ASUSTeK COMPUTER INC

Title : BAT CONNECT

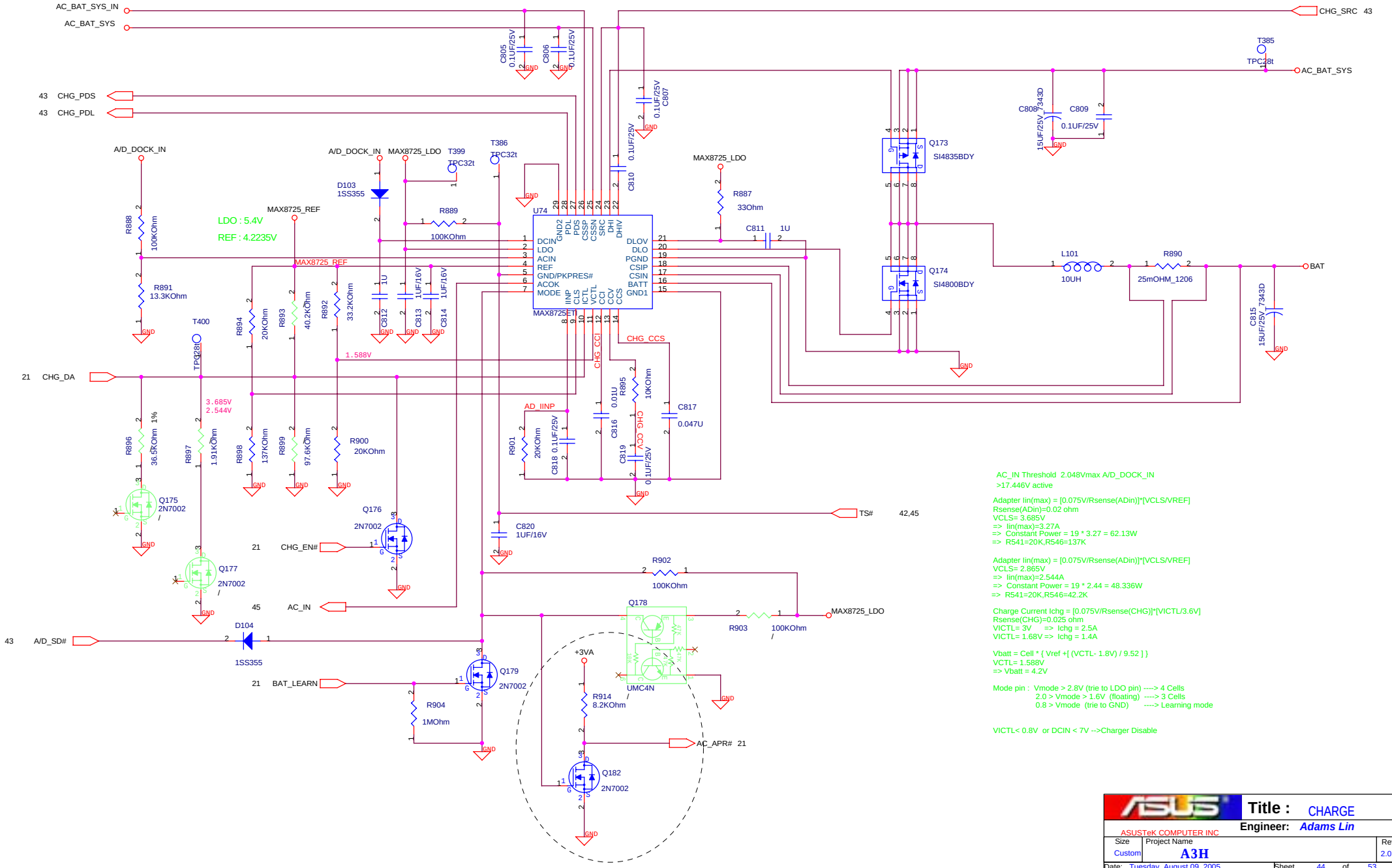
Engineer: Adams Lin

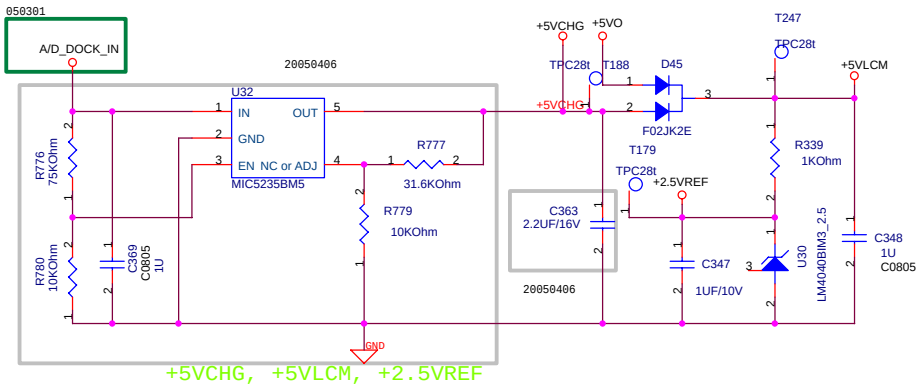
Size	Project Name	Rev
Custom	A3H	2.0

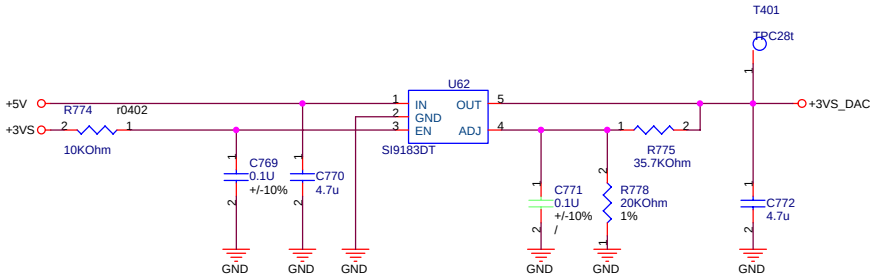
Date: Tuesday, August 09, 2005 Sheet 42 of 53



Title :	CHARGE
Engineer:	Adams Lin
ASUSTeK COMPUTER INC	
Size: Custom	Project Name: A3H
Rev:	2.0
Date:	Tuesday, August 09, 2005
Sheet	43 of 53


AC_BAT_SYS_IN
AC_BAT_SYS
CHG_SRC 43
43 CHG_PDS
43 CHG_PDL
A/D_DOCK_IN
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
U74
MAX8725ETI
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
Q173 SI4835BDY
Q174 SI4800BDY
L101 10UH
R890 25mOHM_1206
BAT
21 CHG_DA
CHG_CCS
CHG_CCI
AD_IINP
TS# 42,45
21 CHG_EN#
45 AC_IN
43 A/D_SD#
21 BAT_LEARN
AC_APR# 21
+3VA
Q175 2N7002
Q176 2N7002
Q177 2N7002
Q178 UMC4N
Q179 2N7002
Q182 2N7002
D103 1SS355
D104 1SS355
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.446V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R541=20K,R546=137K
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V
=> Iin(max)=2.544A
=> Constant Power = 19 * 2.44 = 48.336W
=> R541=20K,R546=42.2K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Title : CHARGE
Engineer: Adams Lin
ASUSTeK COMPUTER INC
Size Custom
Project Name A3H
Rev 2.0
Date: Tuesday, August 09, 2005
Sheet 44 of 53

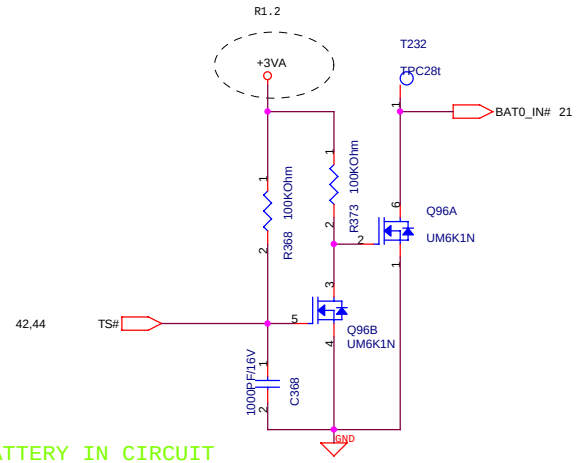


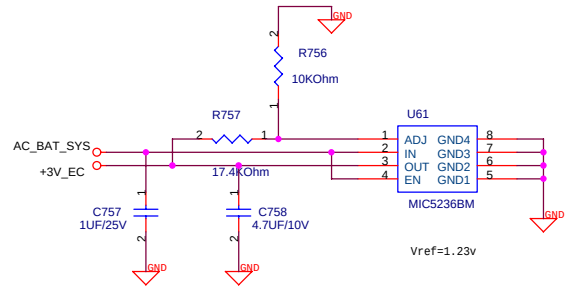


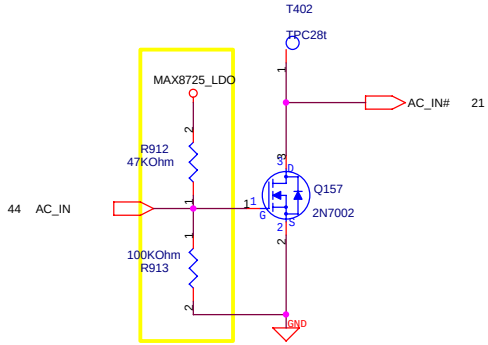
Ref: 1.24V

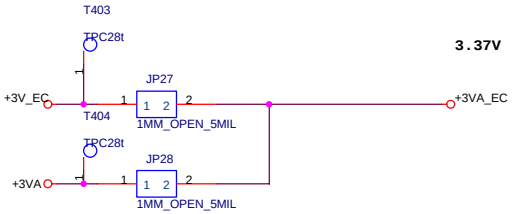
ON: EN>2V (A/D_DOCK_IN:17V)

OFF: EN<0.6V(A/D_DOCK_IN:5.1V)

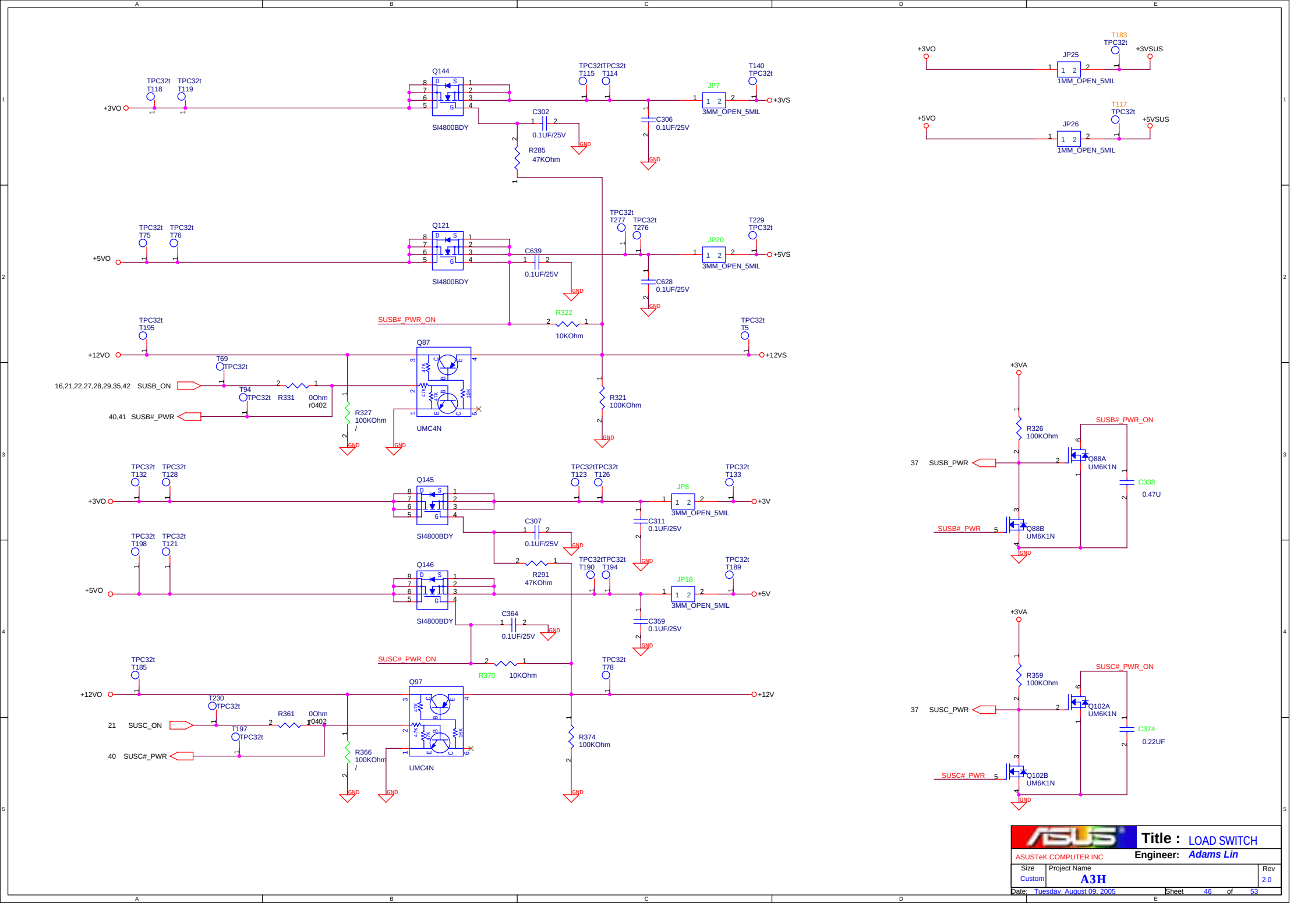




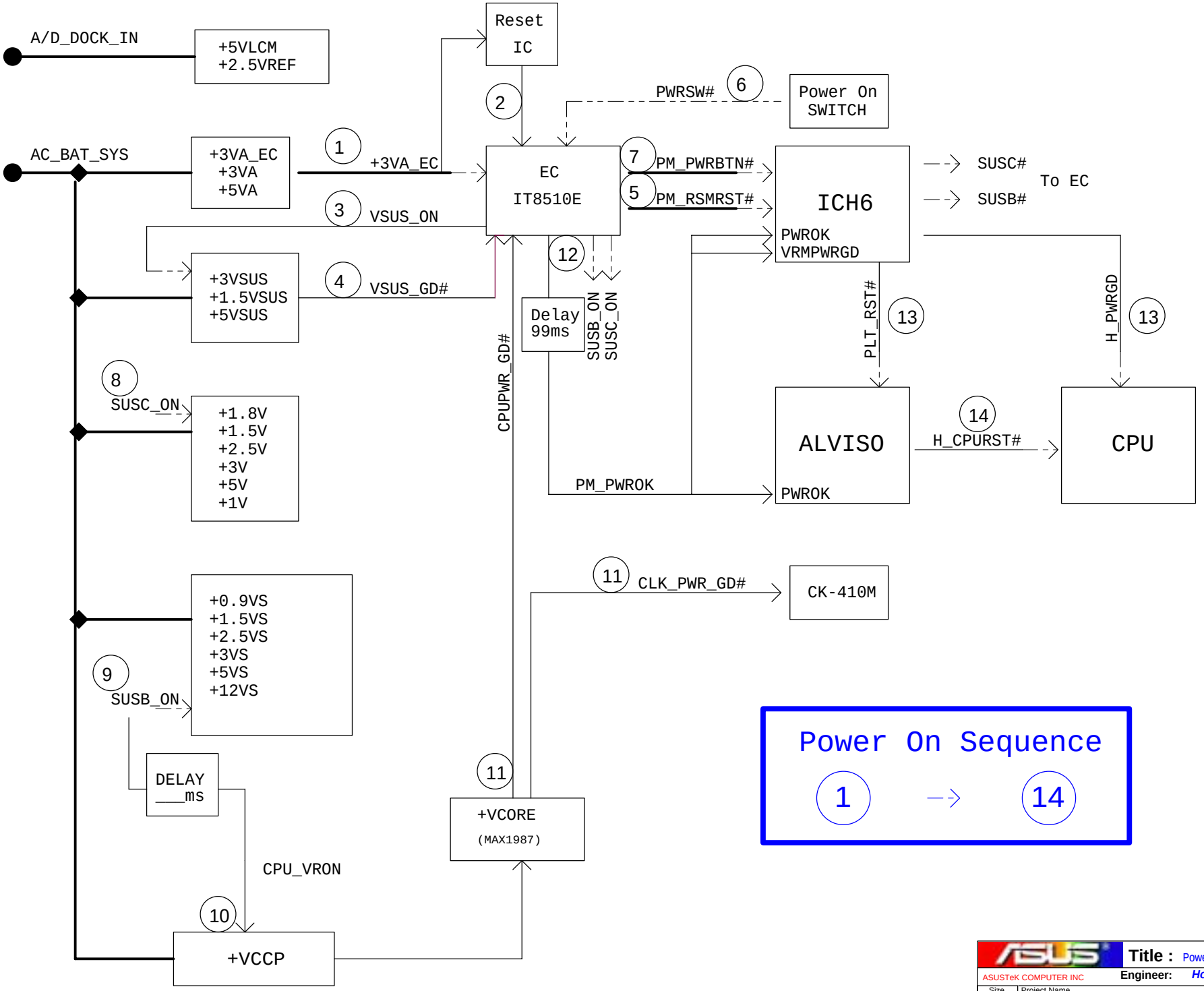




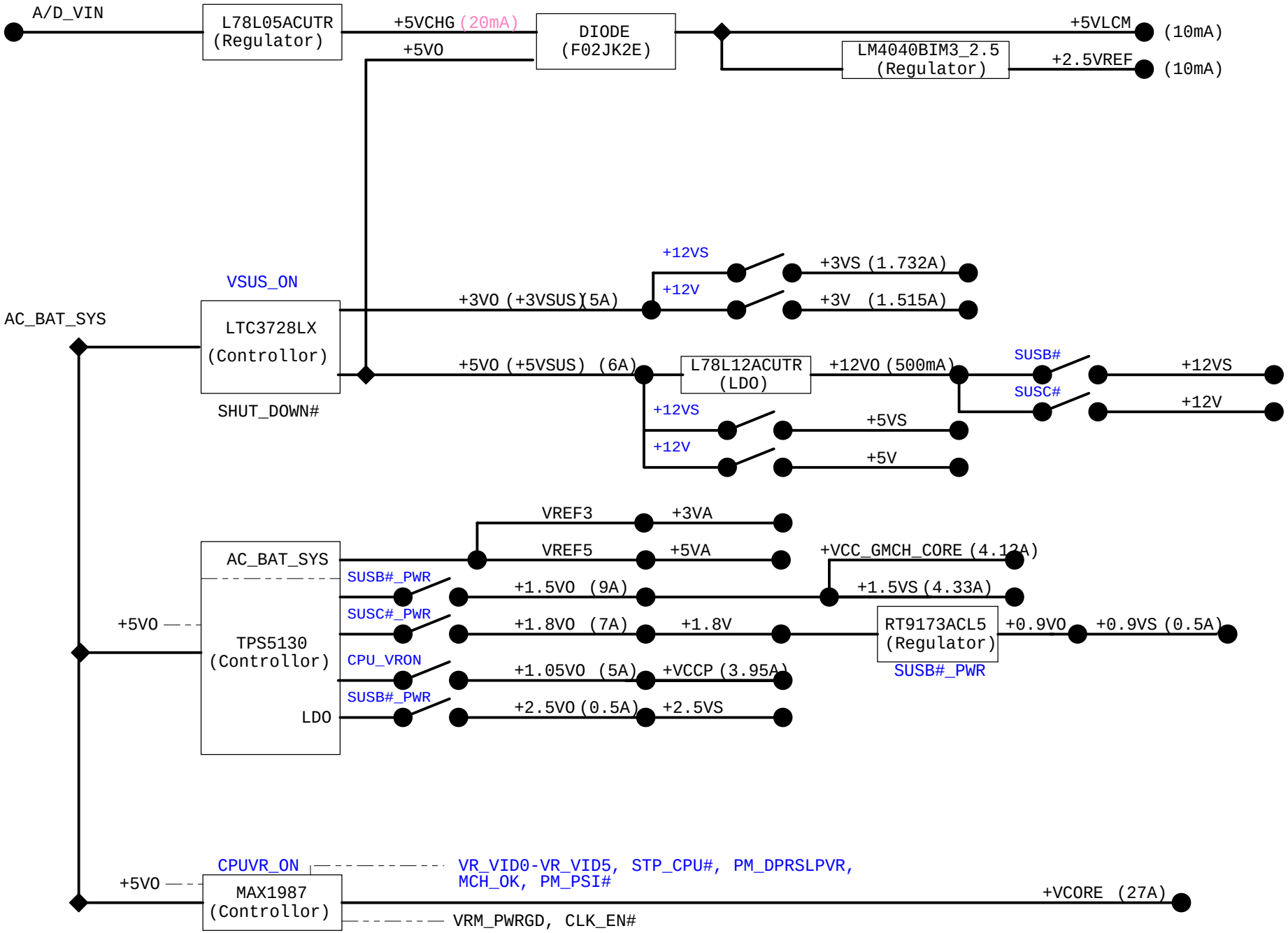
ASUSTeK COMPUTER INC	Title : BATLOW/SD#	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 45 of 53	



ASUSTeK COMPUTER INC	Title : LOAD SWITCH	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 46 of 53	



ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 47 of 53		



ASUSTeK COMPUTER INC	Title : POWER FLOWCHART	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 48 of 53	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

0221

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

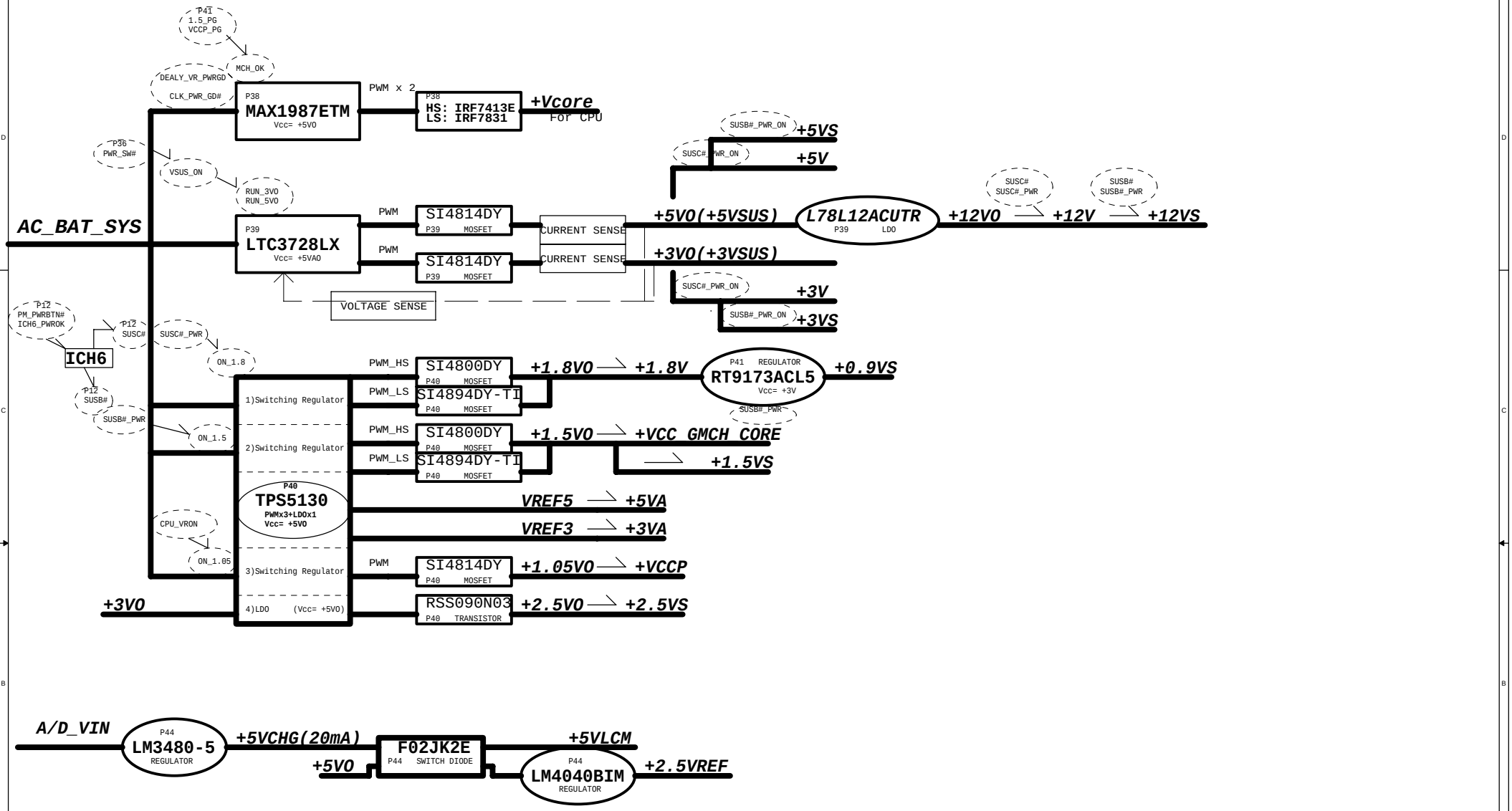
KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Title : System Resource

ASUSTeK COMPUTER INC Engineer: Howard Tu

Size	Project Name	Rev
Custom	A3H	2.0

Date: Tuesday, August 09, 2005 Sheet 49 of 53



ASUSTeK COMPUTER INC	Title : Power Flow Diagram	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3H	Rev: 2.0
Date: Tuesday, August 09, 2005	Sheet 50 of 53	

Rev.	Data	Description
1.0	050701	Initial release
1.1	050719	BT can't detect : remove C16, C17 USB port 2,3 OC function : change pull-high resistor from 8.2K to 100K (add R911)
	050720	Change CE26 PN:11-176247651(Oxide Cap)
	050725	Delete Port Bar Function: **For LAN (Remove)** L87 R836,R837,R842,R846,R839,R840 C794,C792 Q168 D102 U71 **For CRT (Remove)** L88,L89,L90 R843,R844,R845,R909 D105 U72 **For PWR (Remove)** CE32,C789,C790,C791,C793 R841 **For Print Port (Remove)** RP5,RP6,R816 D96 CON22
	050726	SWAP GPB7,GPC3 function (Reserved for CIR) Change TP_CLK,TP_DAT to PS2 channel 2 Change EXT0_PS2_CLK,EXT0_PS2_DAT to PS2 channel 0 Change EXT1_PS2_CLK,EXT1_PS2_DAT to PS2 channel 1
	050727	A3H Delete Function: **For TV OUT (Remove)** CON10,C20,C26,C27,C28,C30,C32,C40 L11,L12,L13 R9,R11,R14 D9,D10,D4 **For Audio DJ (Remove)** Q181,Q126,R910,R263 **A3H use 910GML, A3Ac use 915GM** **A3H PCB ID option**

Rev.	Data	Description
	050727	**Remove For Port Bar & COM Port detect** R871,R872
	050728	A3H Delete Function: **For TV OUT PWR** **remove** L27,C64,C46,C44,L22,C55 L23,C47,L28,C72 C772,R775,R778,C771,U62,C770,C769,R774 **change** R67,R381,R383,R382 change to 0ohm (10-004400000) C65,C70,C67,C61,C56,C71 change to 0ohm (10-004400000)
	050728	A3H Delete Function: **remove SIO, IrDA, COM Port** **SIO** C137,C153,C130,C162,C148,C152,C163,C146 R103,R83,R87,R88,R101 Q20,D17,U6 **IrDA** C643,C642,C641 R641,RN23,RN24,RN25,U33 **COM Port** C795,C796,C798,C800,C797,C799,CN6,CN7 LN1,LN2 CON23,U73
	050803	R235,R240,R248,R263 change to 470ohm (10-003404710)
	05'01/05	

ASUSTeK COMPUTER INC

Title : HISTORY

Engineer: *Howard Tu*

Size	Project Name	Rev
A3	A3H	2.0

Date: Tuesday, August 09, 2005 Sheet 51 of 53

Rev.	Data	Description
1.1	050701	Initial release
	050726	AC_IN can't pull up : add R913(100K) and R912(47K)
	050728	LED flash when AC plug in Pull high to AC_BAT_SYS
	050801	Fix when battery in OVP mode, the battery LED is always ON Add R914,Q182 (GPG7)

ASUSTeK COMPUTER INC

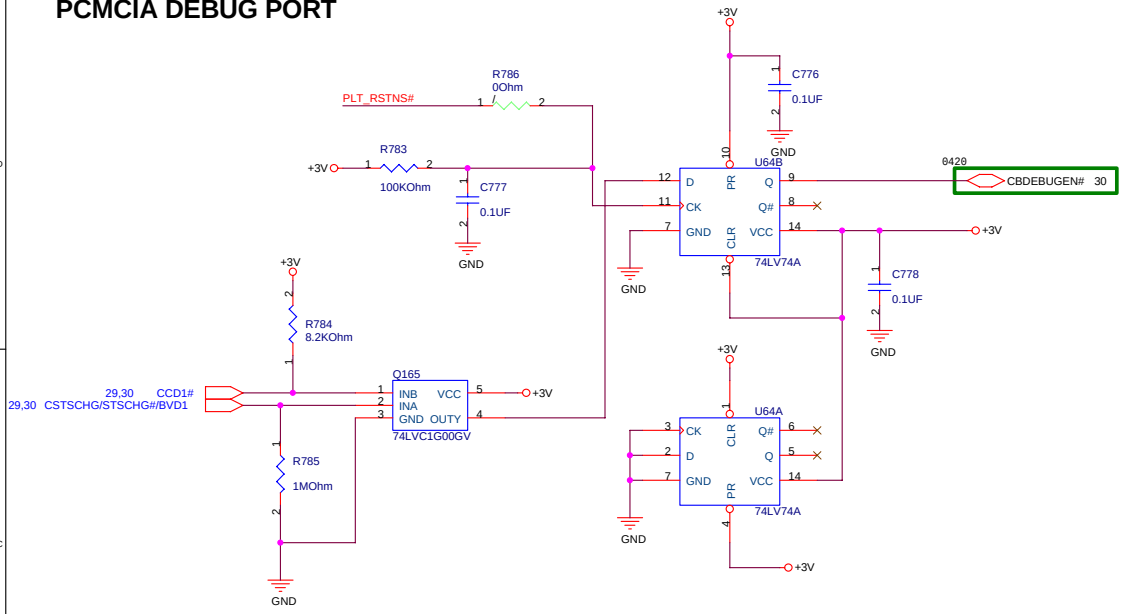
Title : HISTORY(PWR)

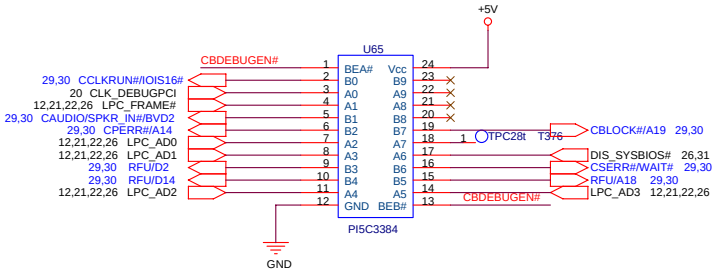
Engineer: *Howard Tu*

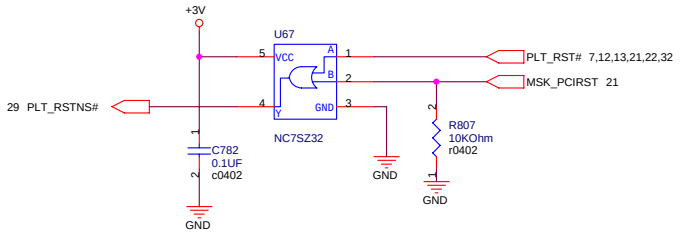
Size	Project Name	Rev
Custom	A3H	2.0

Date: Tuesday, August 09, 2005 Sheet 52 of 53

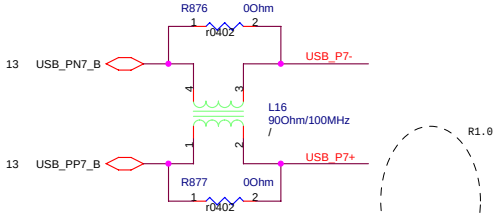
PCMCIA DEBUG PORT



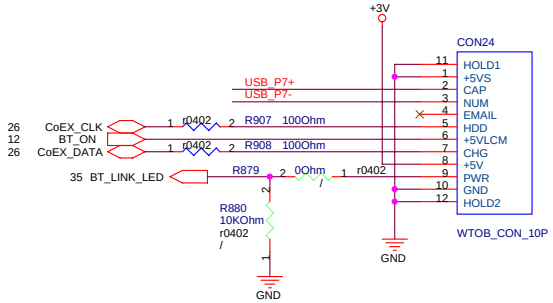




Bluetooth



For Intel Wireless
CoExistence System



ASUSTek COMPUTER INC

Title : Debug Part

Engineer: Howard_Tu

Size	Project Name	Rev
Custom	A3H	2.0

Date: Tuesday, August 09, 2005 Sheet 53 of 53