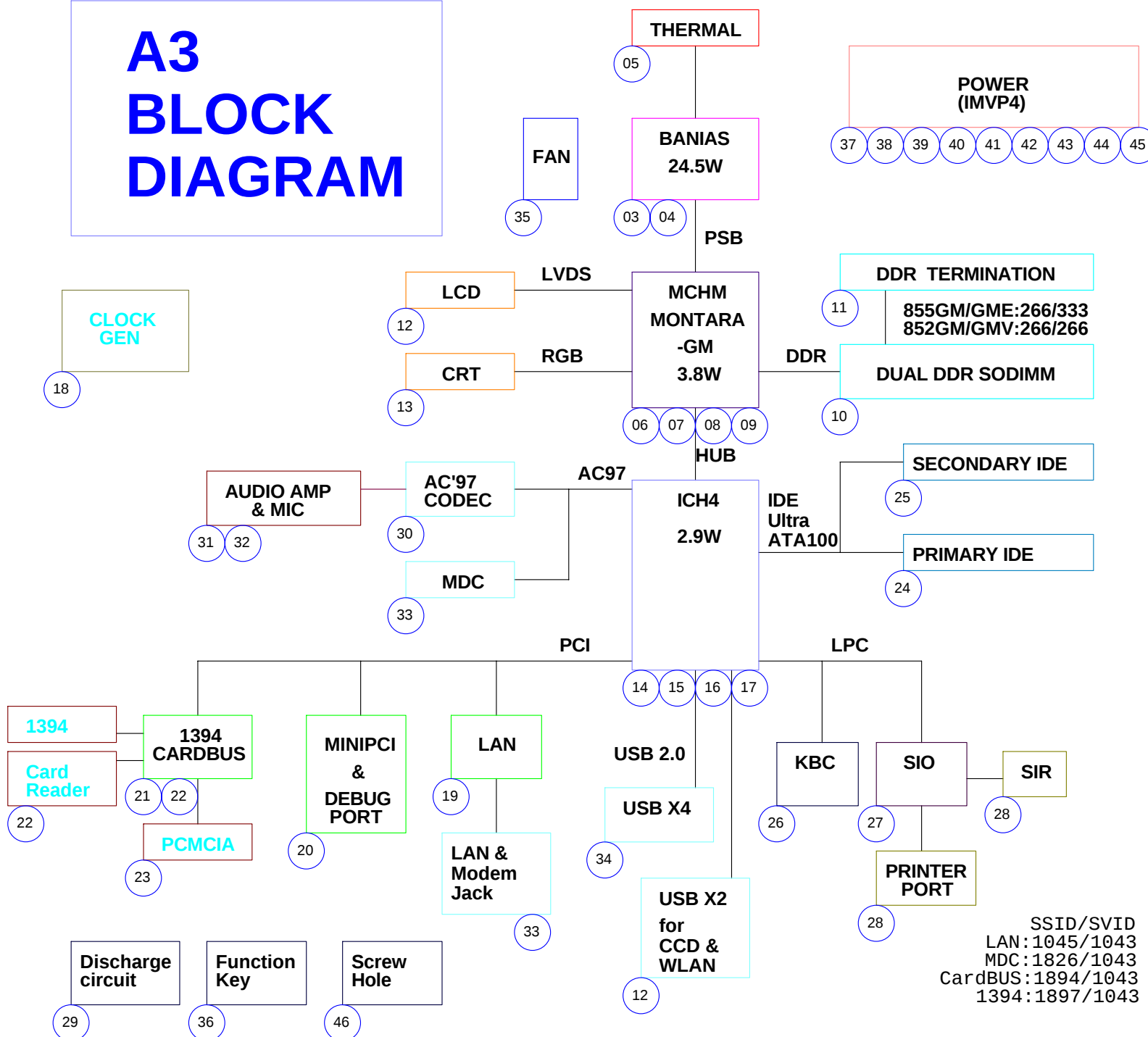


A3 BLOCK DIAGRAM



FILE LIST

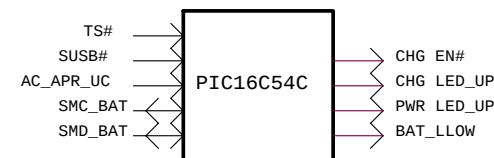
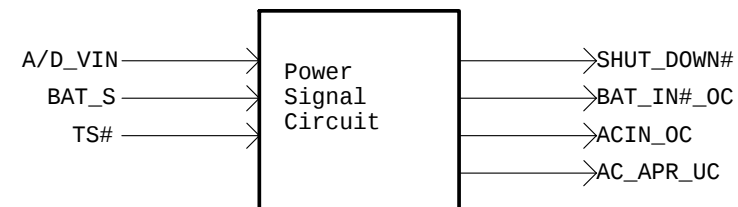
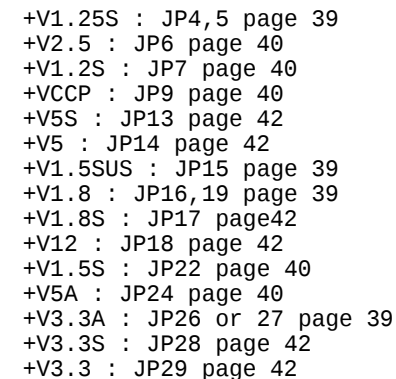
01

- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-BANIAS(HOST)
- 04_CPU-BANIAS(PWR)
- 05_THERMAL
- 06_NB-MCHM(DDR)
- 07_NB-MCHM(HOST)
- 08_NB-MCHM(VGA)
- 09_NB-MCHM(PWR)
- 10_DUAL DDR SODIMM
- 11_DDR TERMINATION
- 12_LVDS & BACKLIGHT
- 13_CRT CONNECTOR
- 14_ICH4-M(HUB_PCI)
- 15_ICH4-M(H_U_IDE_PM)
- 16_ICH4-M(PWR)
- 17_ICH4-M_PULLUP
- 18_CLOCK-ICS950815
- 19_LAN-RTL8100CL
- 20_MINIPCI
- 21_CB1394-R5C593(1)
- 22_CB1394-R5C593(2)
- 23_PCMCIA SOCKET
- 24_IDE-HD
- 25_IDE-ODD
- 26_KBC-M38857
- 27_SIO-ITE7805
- 28_IR&LPT_PORT
- 29_DISCHARGE CIRCUIT
- 30_CODEC-ALC650
- 31_AUDIO AMP
- 32_MIC
- 33_MDC&RJ45&RJ11
- 34_USB
- 35_FAN&Audio DJ
- 36_FUNCTION KEY
- 37_PWR & RESET SEQ
- 38_VCORE
- 39_1.25V&1.8V
- 40_2.5V&1.5V&1.35V&1.05V
- 41_SYSTEM
- 42_LOAD SWITCH
- 43_CHARGER
- 44_PIC16C54
- 45_BATLOW/SD#
- 46_SCREW HOLE & M/B SETTING
- 47_REVISION(1)
- 48_REVISION(2)
- 49_REVISION(3)

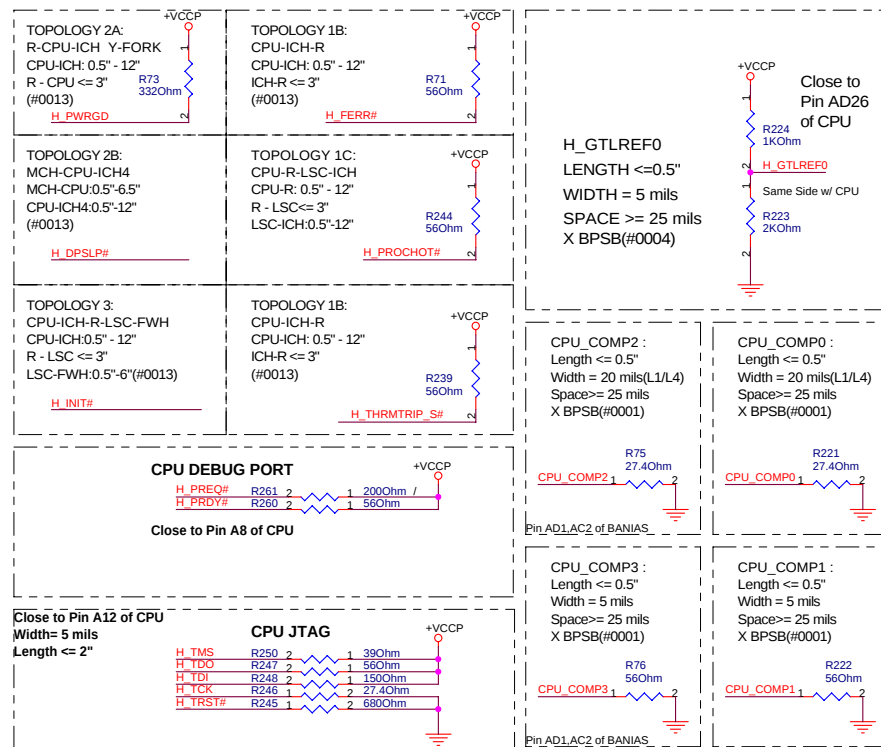
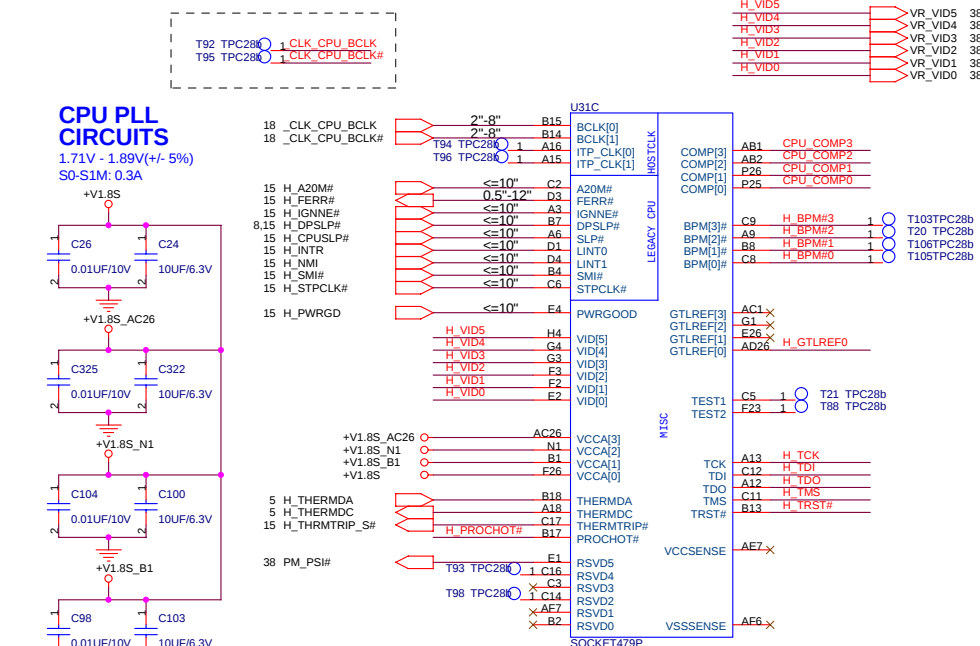
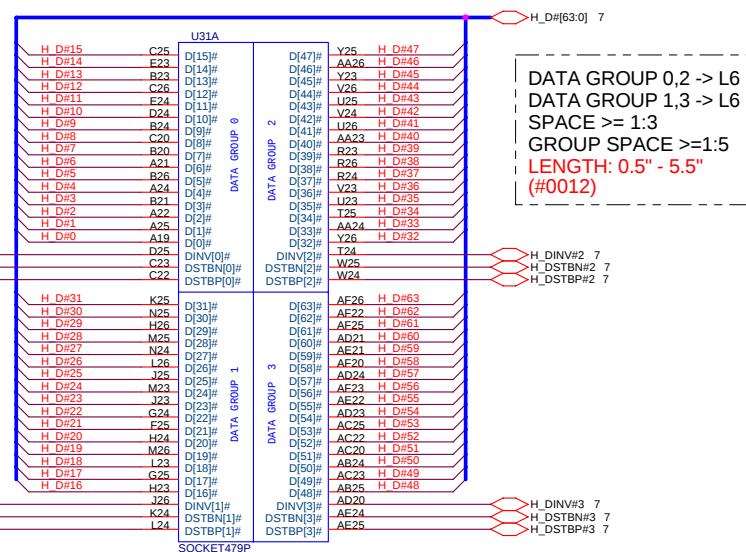
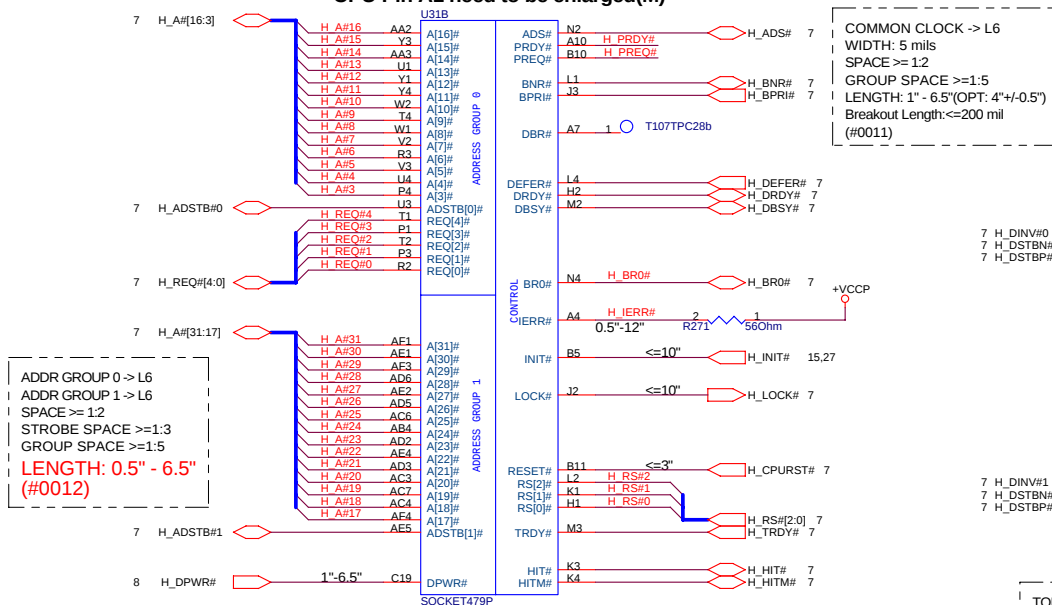
SSID/SVID
LAN:1045/1043
MDC:1826/1043
CardBUS:1894/1043
1394:1897/1043

Battery in : 16.8 ~ 11.6V

PM_STPCPU#., PM DPRSLPVR., PCI#., MCH_OK., CLK_EN#



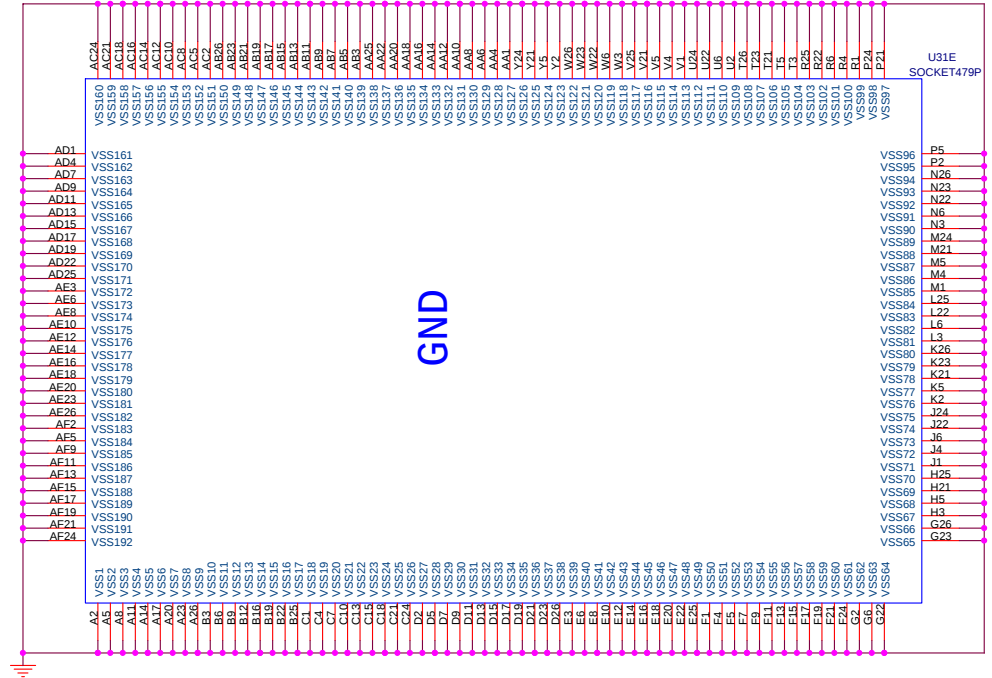
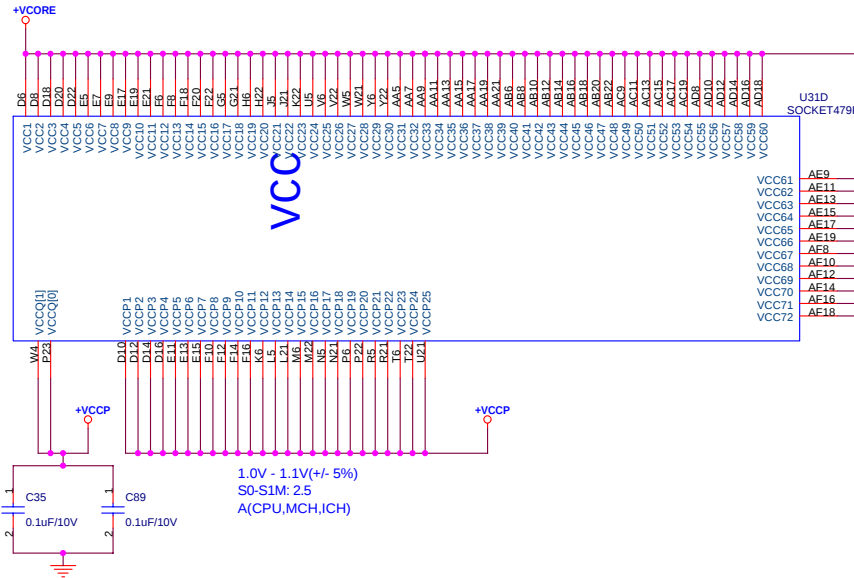
CPU Pin A1 need to be enlarged(M)



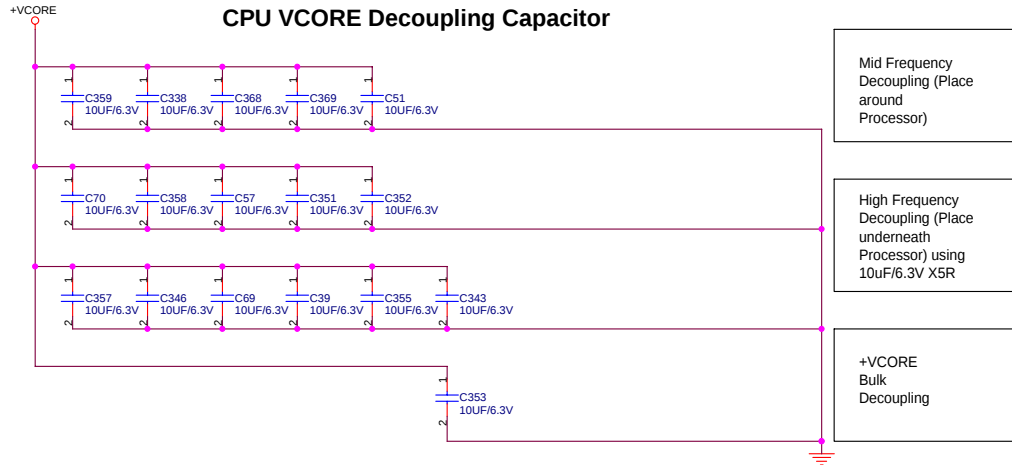
2025

HFM(1.3GHz-1.7GHz): 1.468V
LFM(600MHz): 0.956V

0.745V - 1.356V(+/- 1.5%)
C0: 25 A
C3: 7.59A
C4: 0.9A

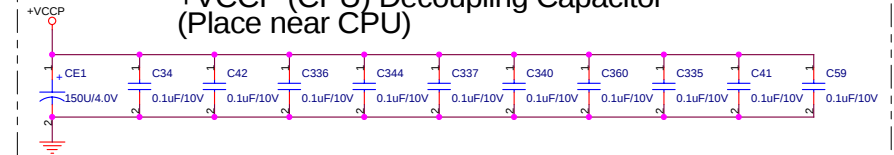


CPU VCORE Decoupling Capacitor



M3N : Four 200 uF are located in IMVP4
A3N : Delete 10uF/6.3V from 35pcs to 17pcs

+VCCP (CPU) Decoupling Capacitor (Place near CPU)



Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS

12 mils

=====GND

10 mils

```
=====H_THERMDA(10 mils)
```

```
10 mils
=====H_THERMDC(10 mils)
```

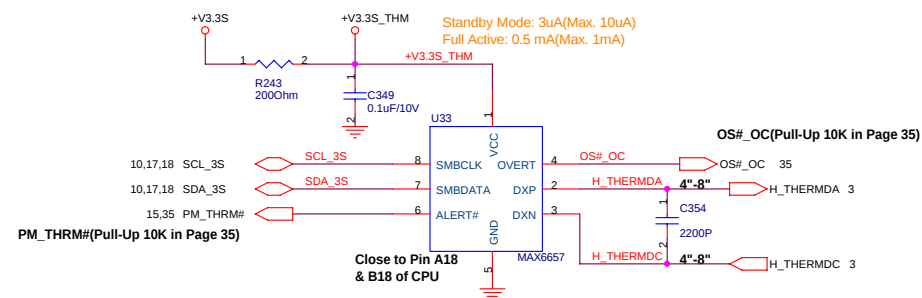
10 mils

=====GND

12 mils

-----OTHER SIGNALS

Avoid BPSB,Power

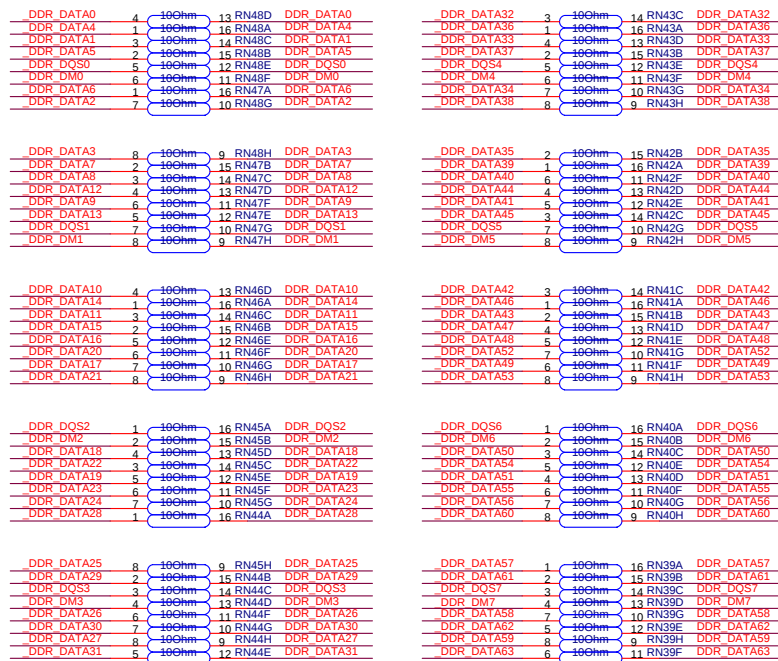


3.8W

Thermal Power: ~3.8W

LxWxH=37.5x37.5x2.58

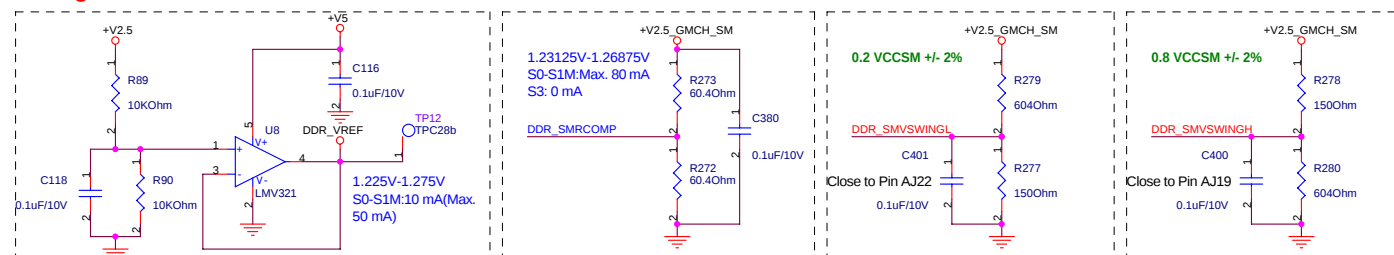
1107



20A3L

1.23125V-1.26875V
 SO-S1M:Max. 80 mA
 S3: 0 mA

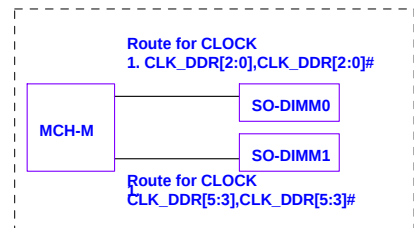
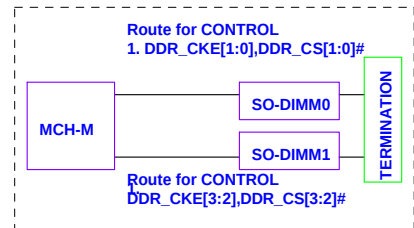
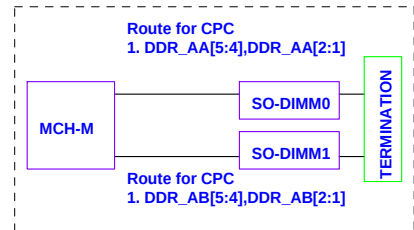
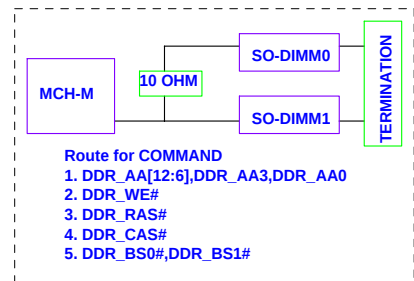
Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.



DDR_DATA[63:0] 10.11
 DDR_DM[7:0] 10.11
 DDR_DQS[7:0] 10.11

(MCH-Sighting041)

M-GM system memory interface generates single pulse CKE events which may cause intermittent hangs and display corruptions when using Micron and Infineon SO-DIMMs.



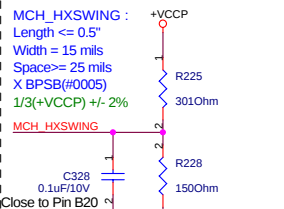
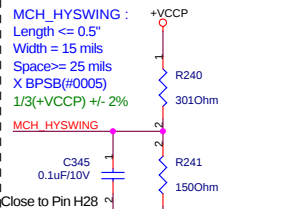
MCH_HLZCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space >= 25 mils
X BPSB(#0002)

MCH_HLZCOMP

MCH_HYRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space >= 25 mils
X BPSB(#0002)



MCH_HXRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space >= 25 mils
X BPSB(#0002)



3 H_A#([31:3])

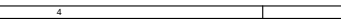
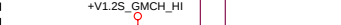
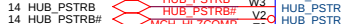
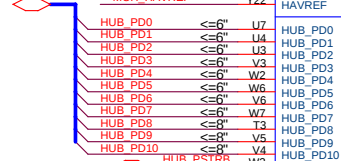
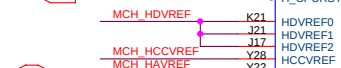
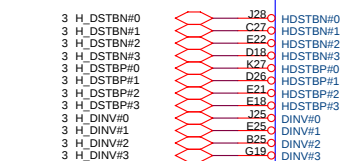
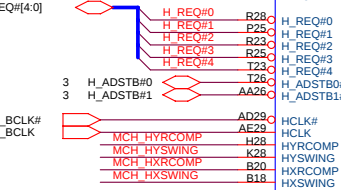
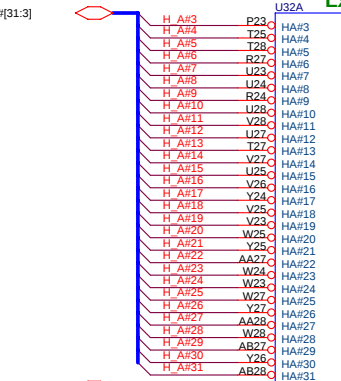
3 H_REQ#([4:0])

18 _CLK_MCH_BCLK#
18 _CLK_MCH_BCLK

3 H_CPURST#

14 HUB_PD[10:0]

+V1.2S_GMCH_HI



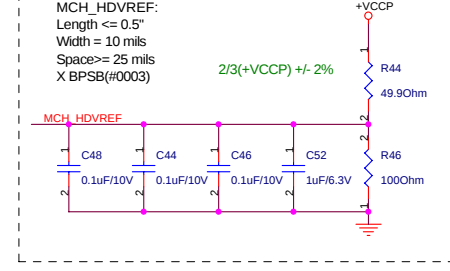
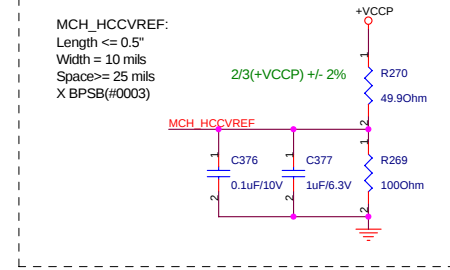
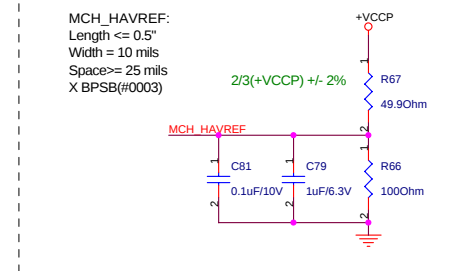
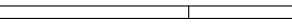
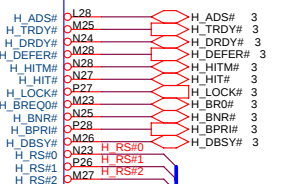
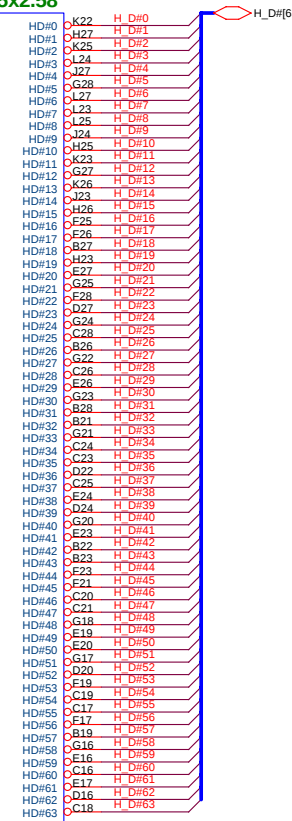
LxWxH=37.5x37.5x2.58

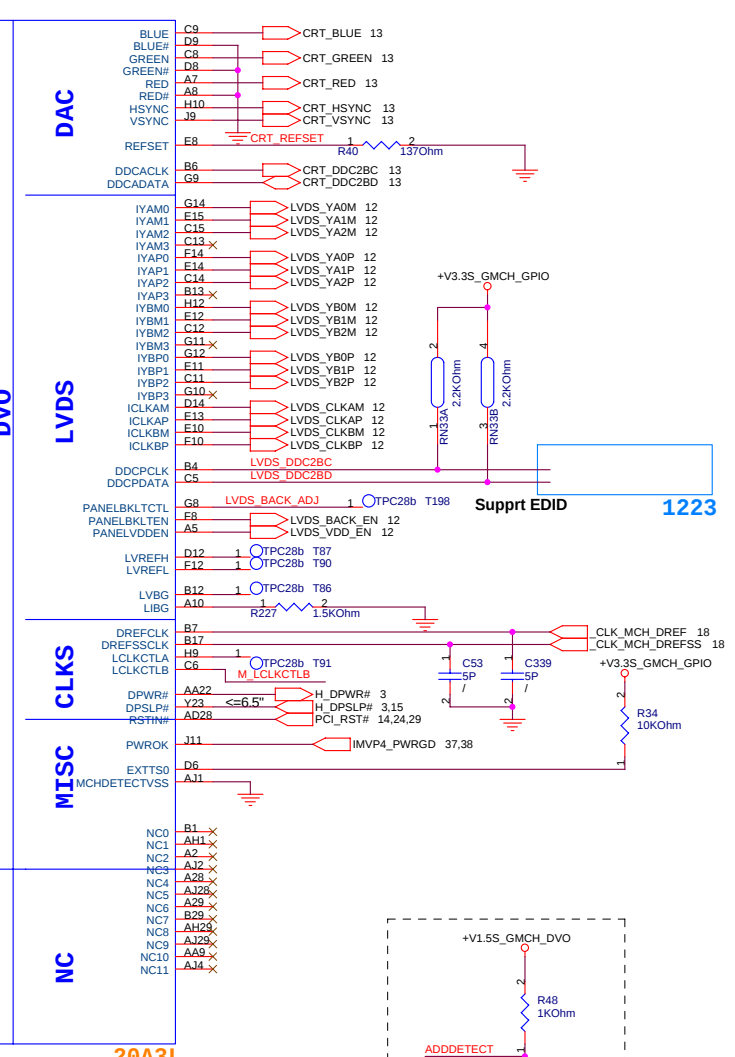
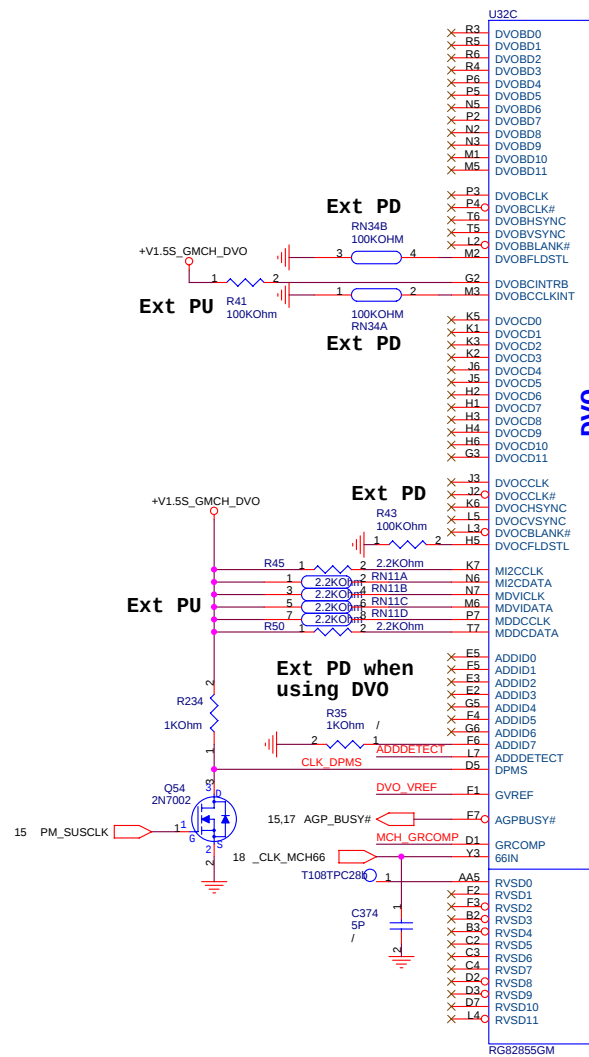
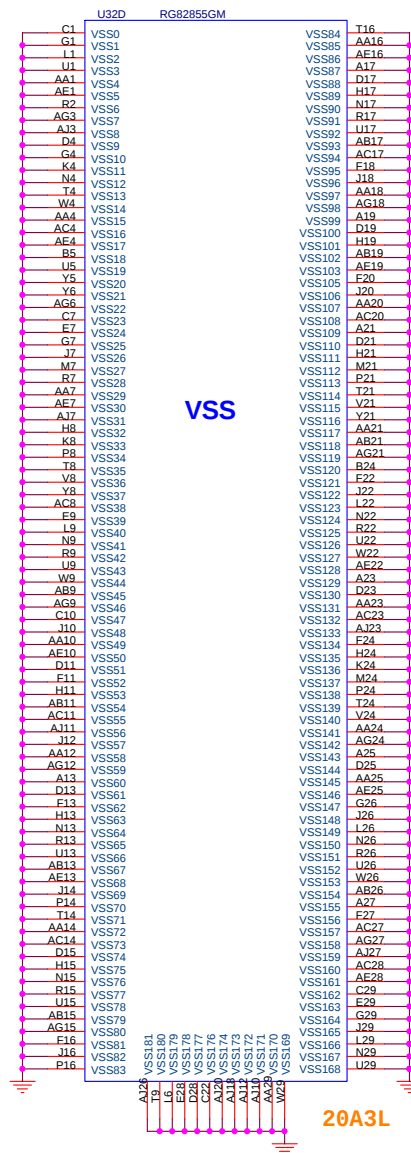
HOST

HUB I/F

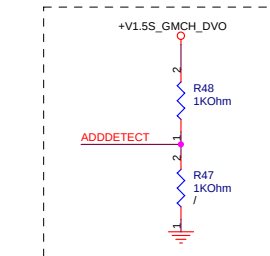
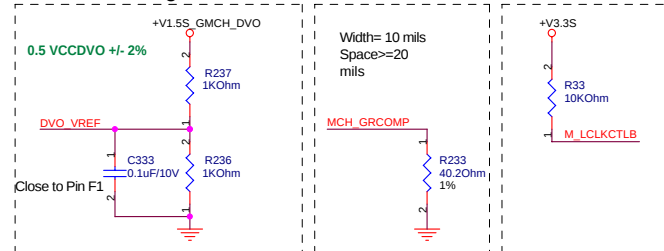
20A3L

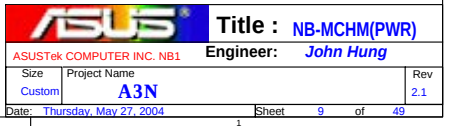
2025



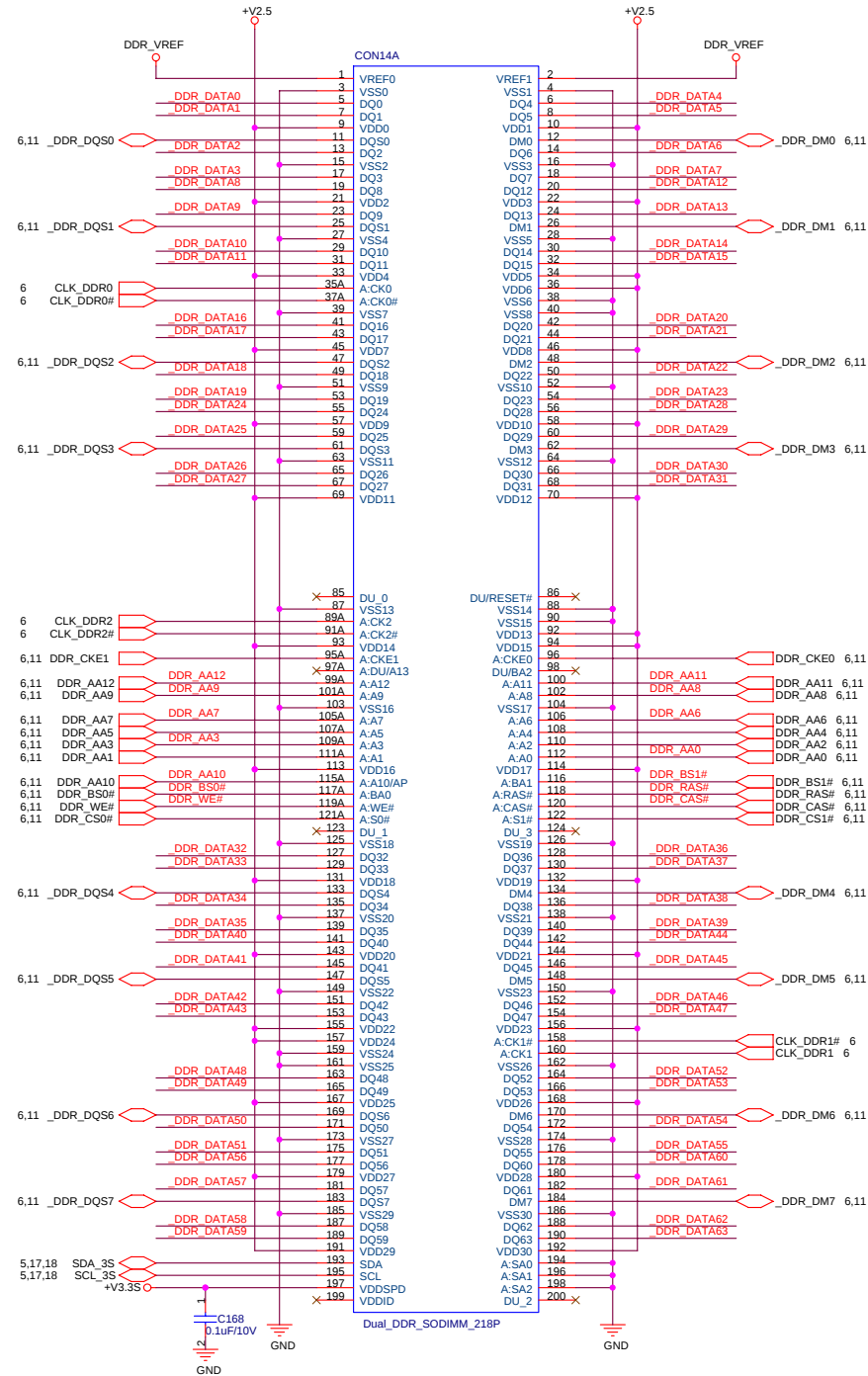


When no using DVO

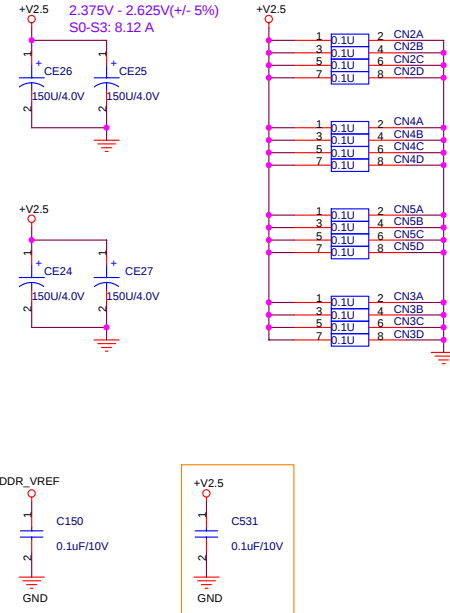




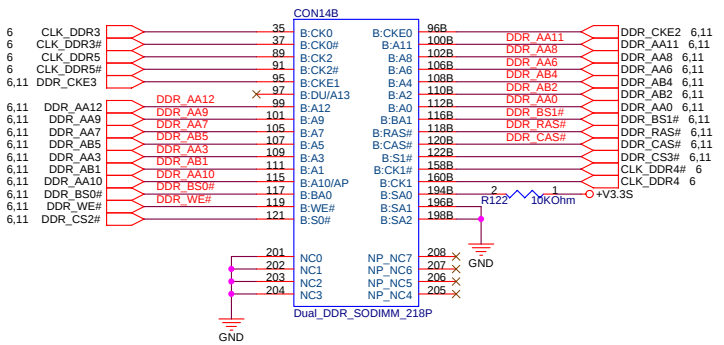
6.11 _DDR_DATA[63:0]



FOR +V2.5 DECOUPLING

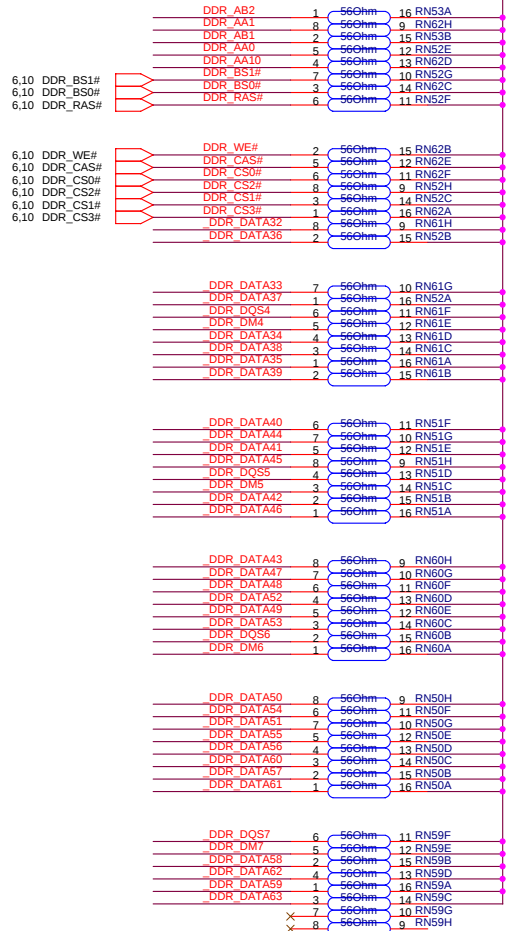
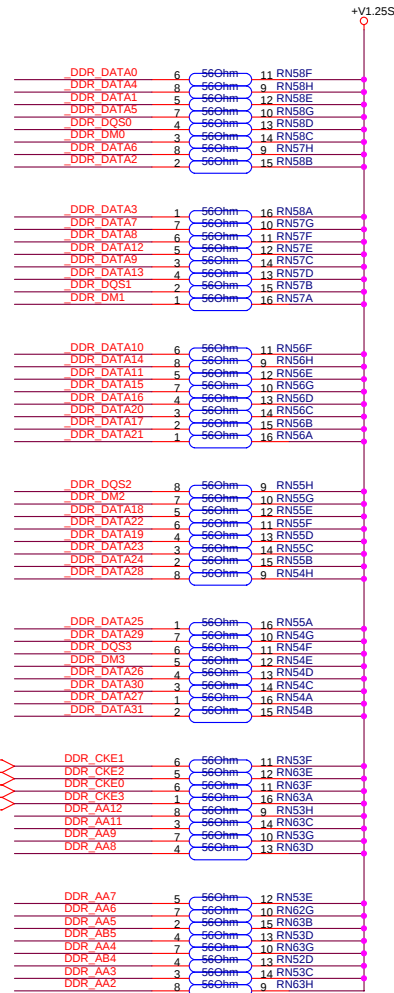


2024
EMI : Close to DDR
socket power plane
of +V2.5

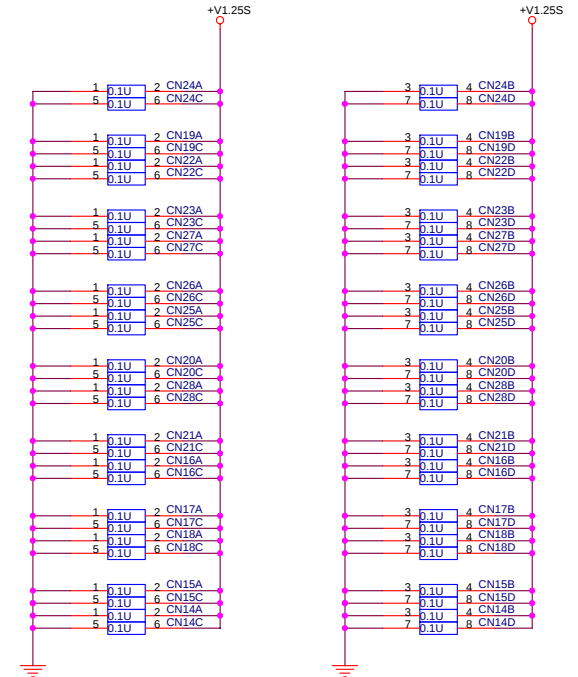


DDR TERMINATION

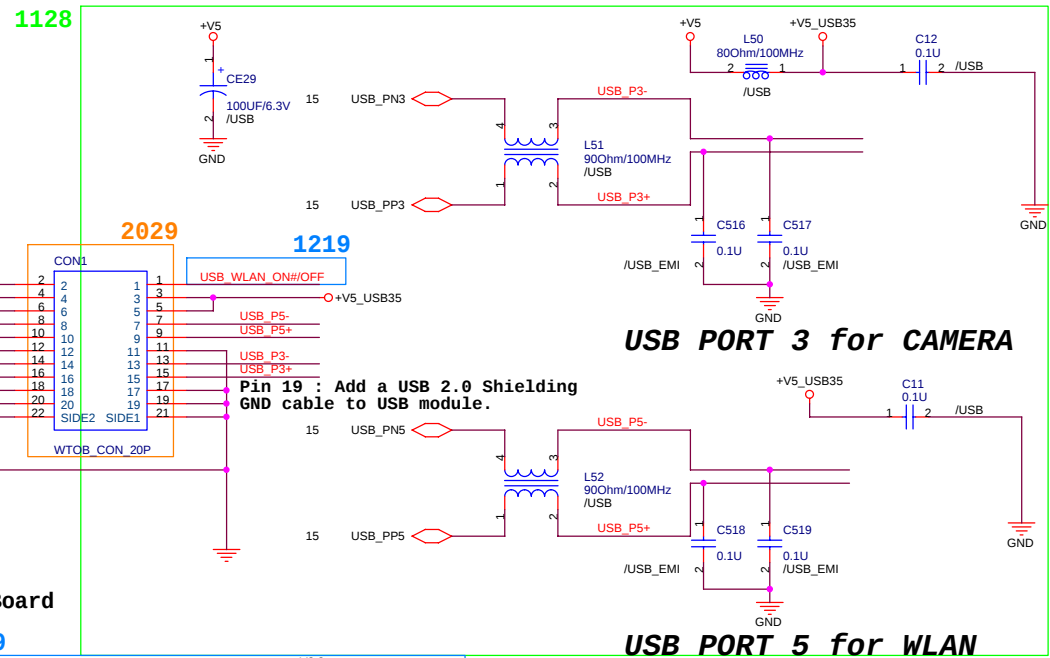
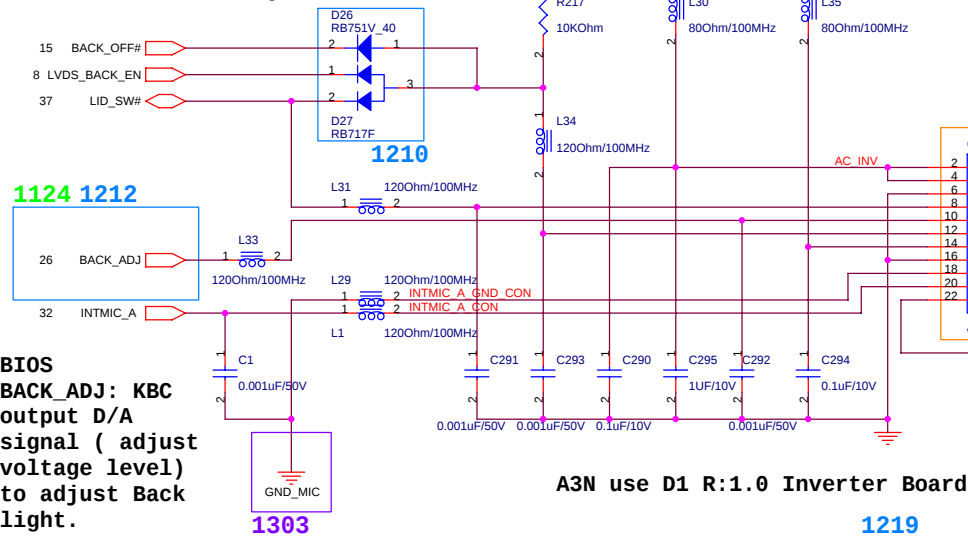
6,10 _DDR_DATA[63:0]
6,10 _DDR_DM[8:0]
6,10 _DDR_DQS[8:0]
6,10 _DDR_AA[12:0]
6,10 _DDR_AB[2:1]
6,10 _DDR_AB[5:4]



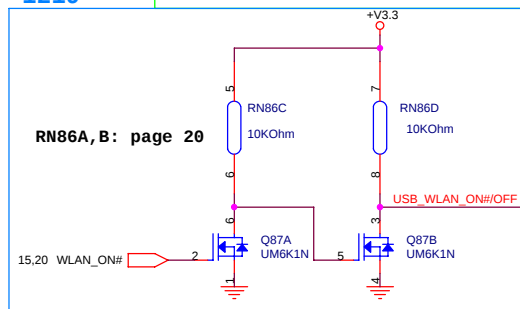
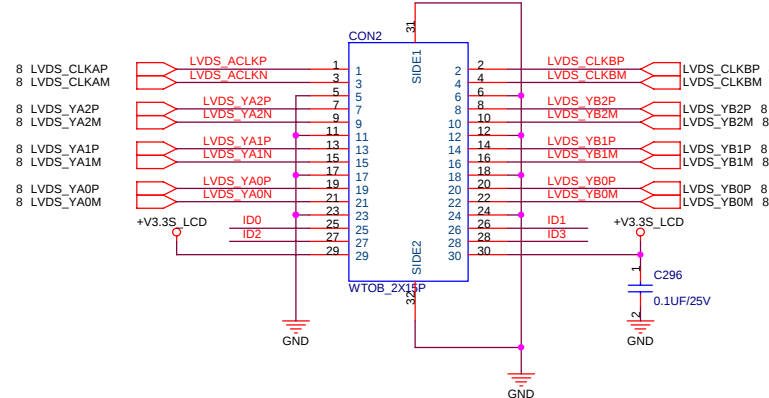
FOR +V1.25S DECOUPLING



BIOS
BACK_OFF#:When user push "Fn+F7"
 button, BIOS active this pin to
 turn off back light.

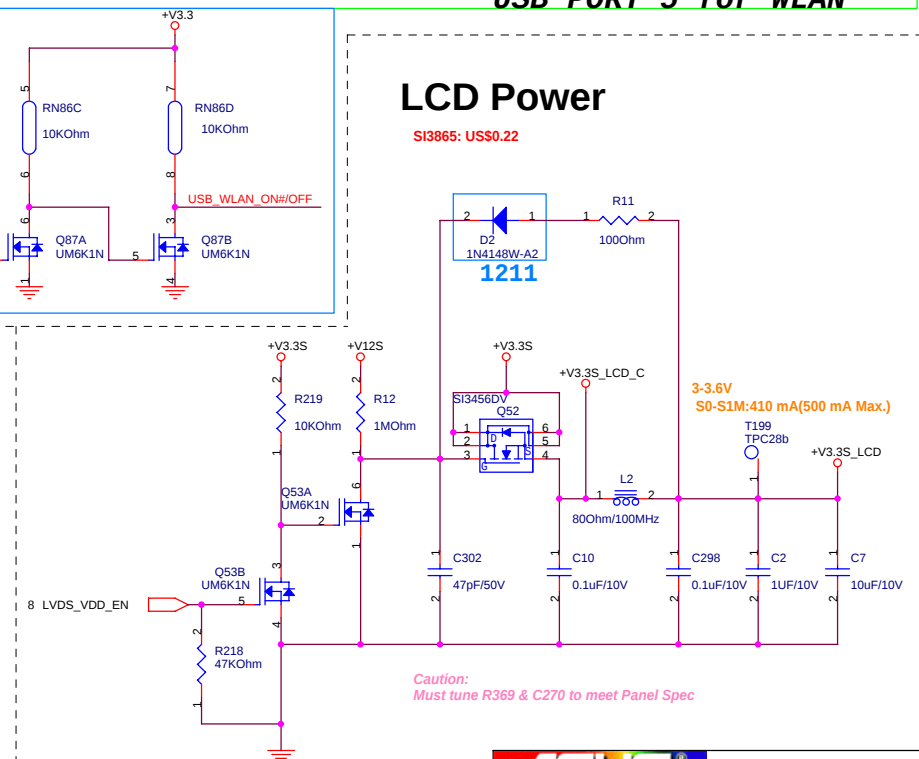
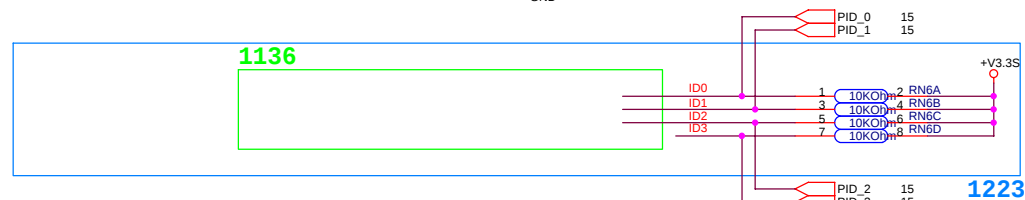


LCD	CABLE ID:	PID3	PID2	PID1	PID0
14.1	XGA	1	1	1	1
15.1	XGA	1	1	0	1
15.1	SXGA+	1	0	1	1



LCD Power

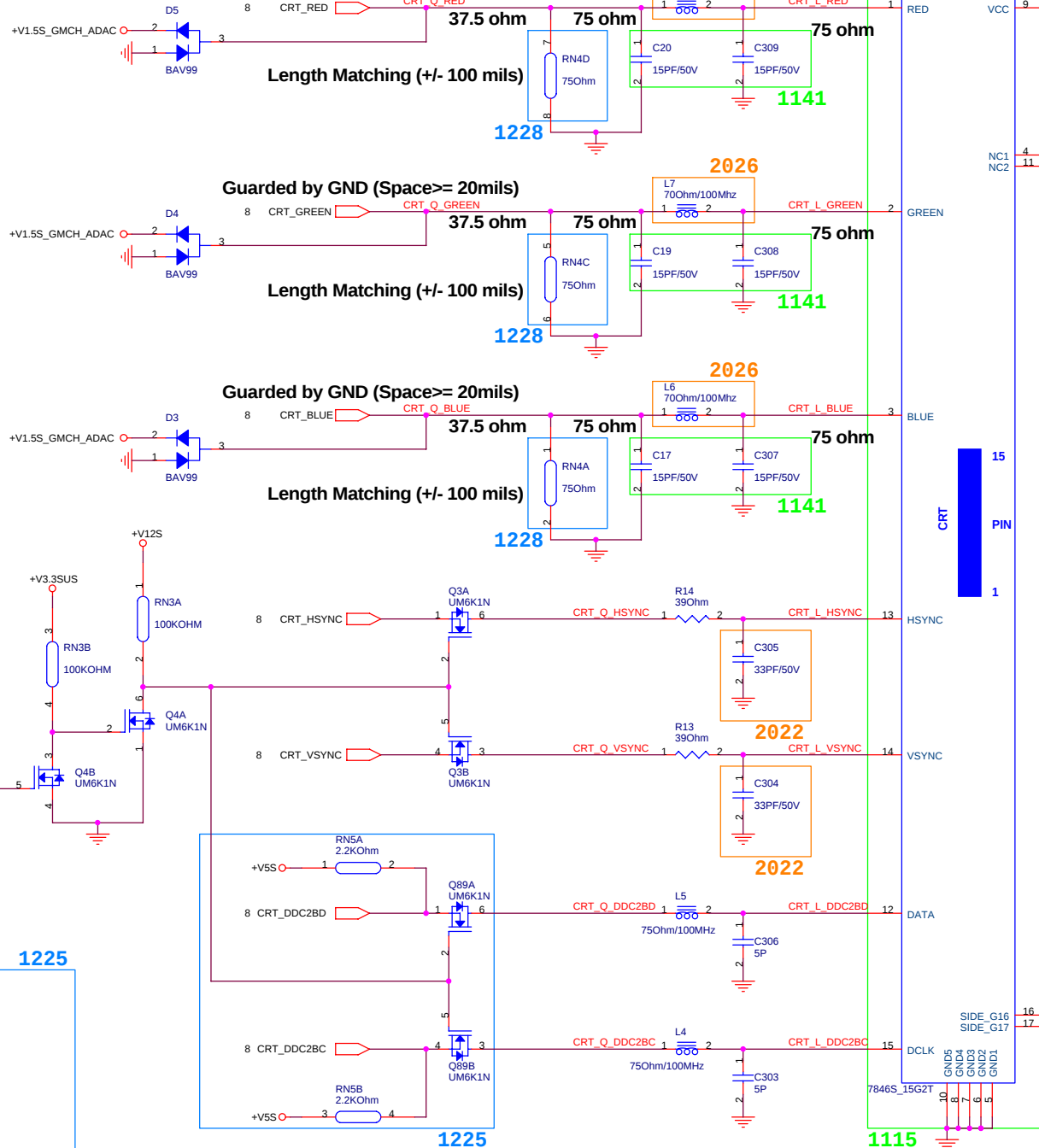
SI3865: US\$0.22



Place Pi-Filter close to CRT
(≤ 200 mils) 2026

Guarded by GND (Space ≥ 20 mils)

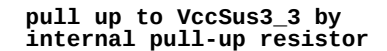
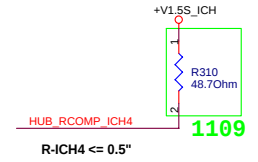
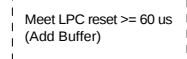
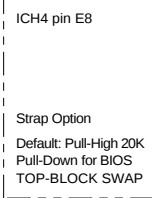
Length Matching (+/- 100 mils)



19,20,21,22 PCI_AD[31:0]

U20A

IDSEL	PCI_AD?
CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16



USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Pair Width/Space: 7/10 mils
Impedance: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Space: >= 50 mils

LxWxH=31x31x2.38

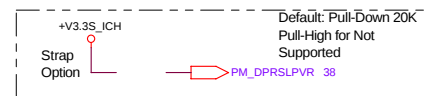
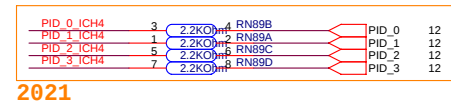
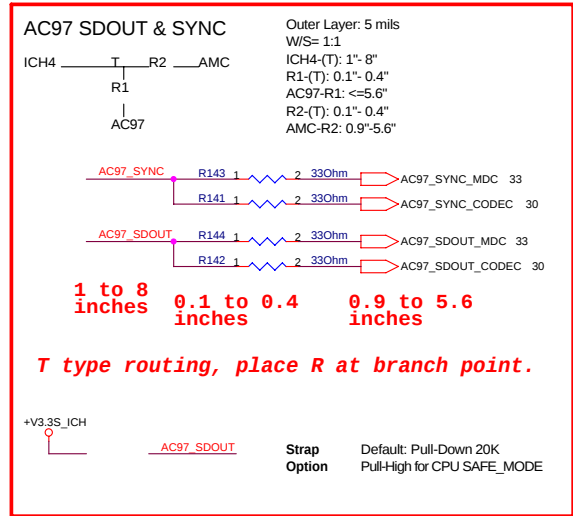
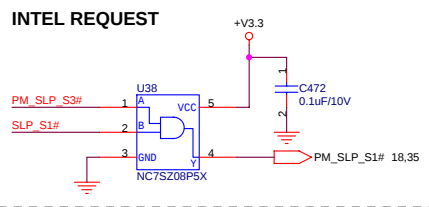
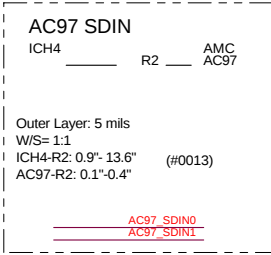
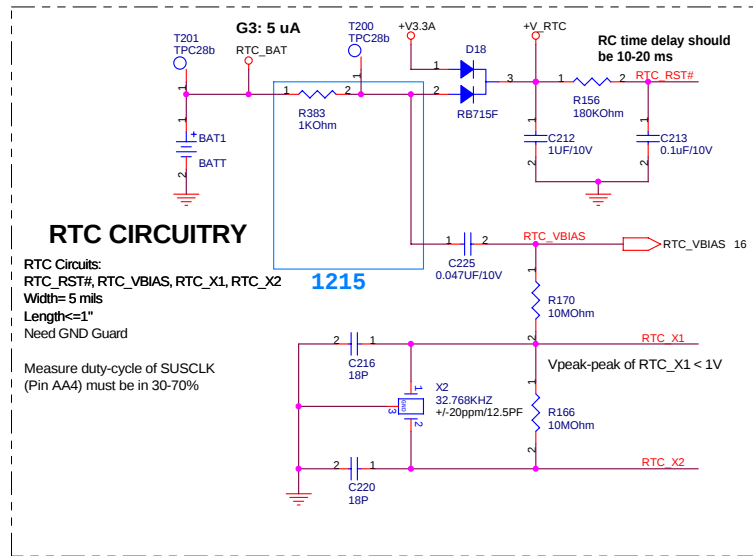
LxWxH=31x31x2.38

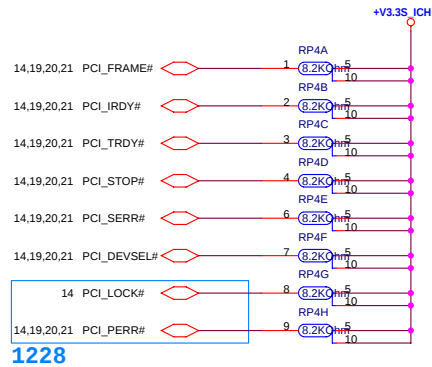
IDE I/F:
Width: 5 mils
Space: 7 mils
Length: <= 8"
Match: <= 500 mils

IDE I/F:
Width: 5 mils
Space: 7 mils
Length: <= 8"
Match: <= 500 mils

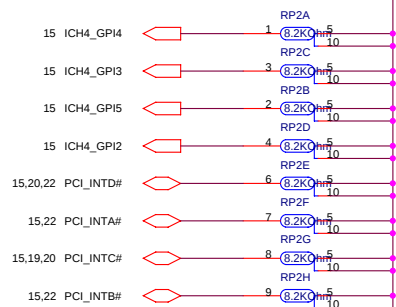
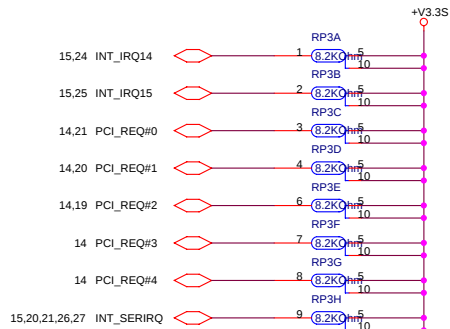
USBRBIAS:
WS: 5/5 mils
Length: <= 0.5"

GPIO[32:43] default:
Output High
ICH4 EDS R:1.0 page 10-94
10.10.8, 10.10.9

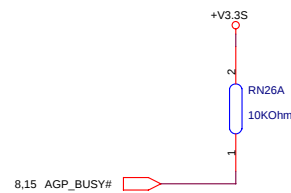
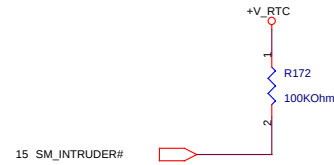
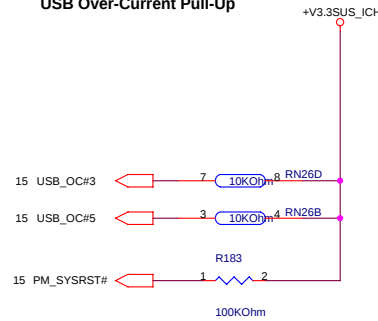




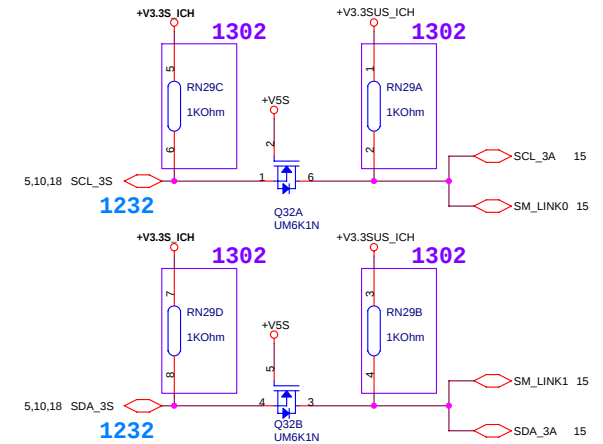
Can Swap



USB Over-Current Pull-Up

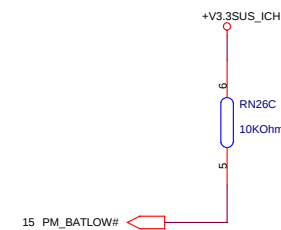


ICH4 SMLink & SMBus must be tied together



BATTERY LOW

ICH4



FS4	FS3	FUNCTION
0	0	100MHz
0	1	133MHz (D)
1	0	200MHz
1	1	166MHz

CLK33 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: same as CLK66

CLK66 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: +/- 100 mils

CLK_EN# is OD for MAX1987

1105

1106

FS1	FS0	FUNCTION
0	0	66 MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz

I2C address: D2H
3.3V+/-5%
S1M: 40 mA
S0: 360 mA

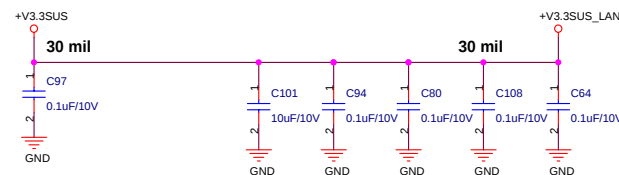
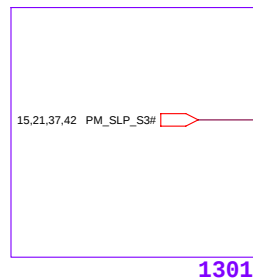
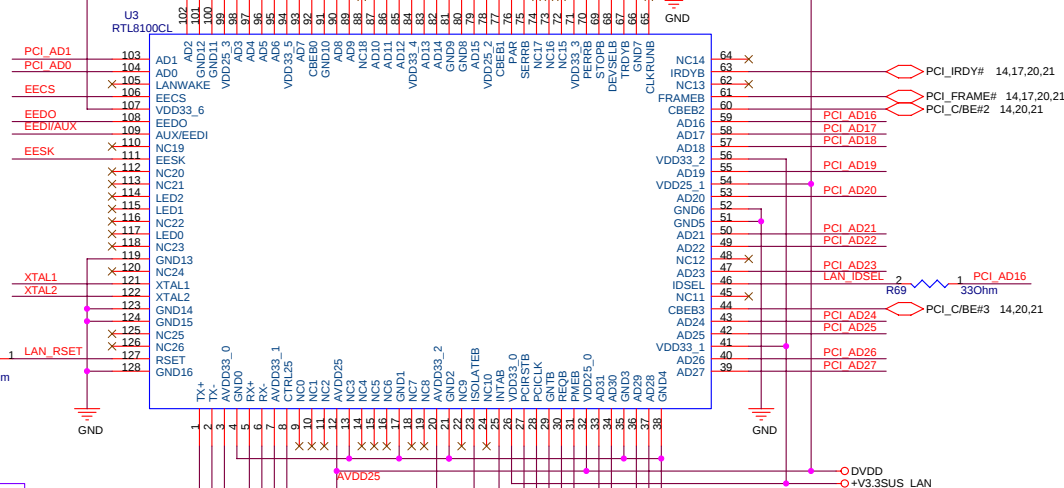
CLK_CPU_BCLK# must be low in C3

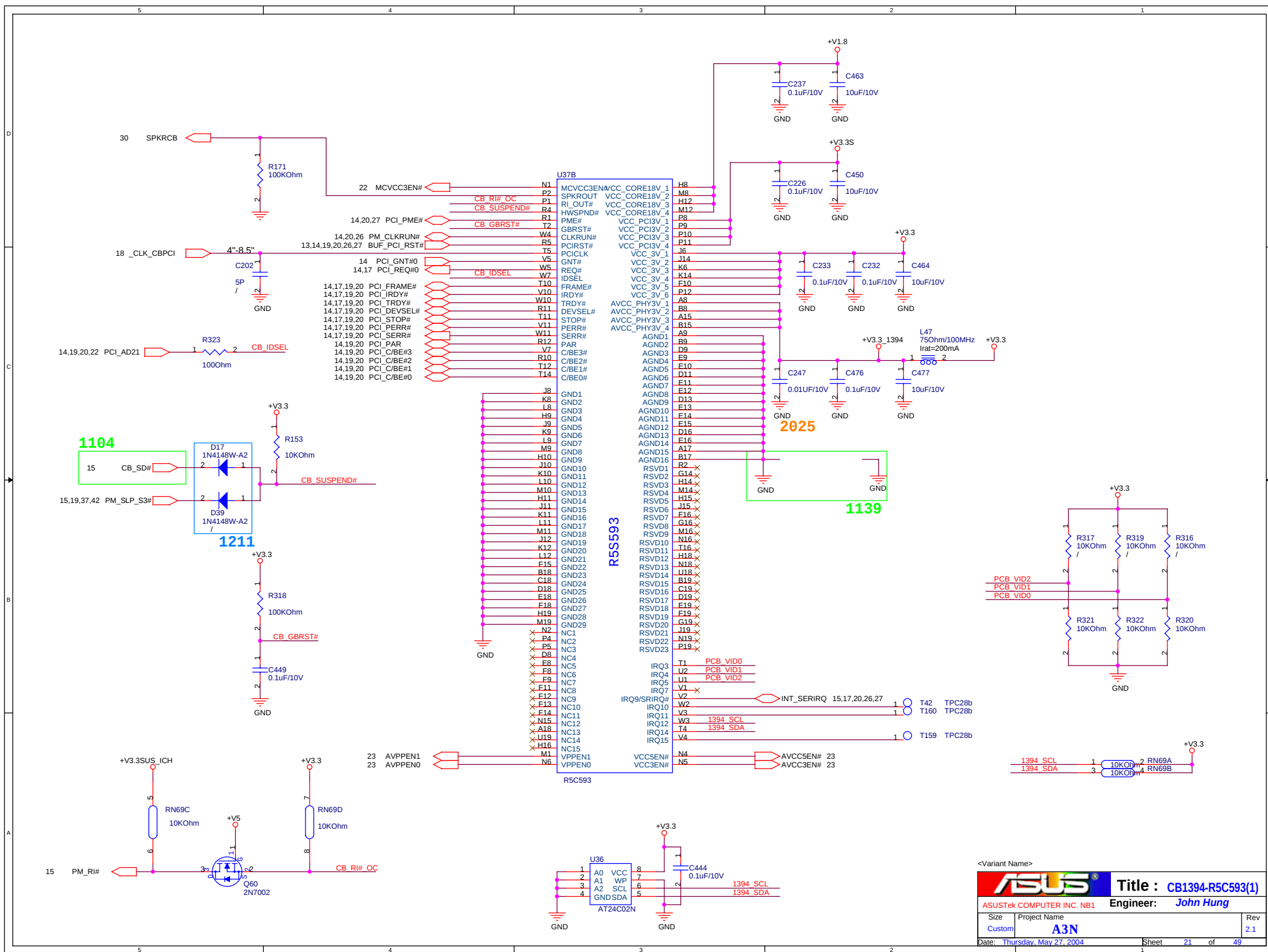
HOST_CLK GROUP
In L3 or L6
Pair Width/Space: 4/4 mils
Group Space: >= 25 mils
Length Match: +/- 10 mils

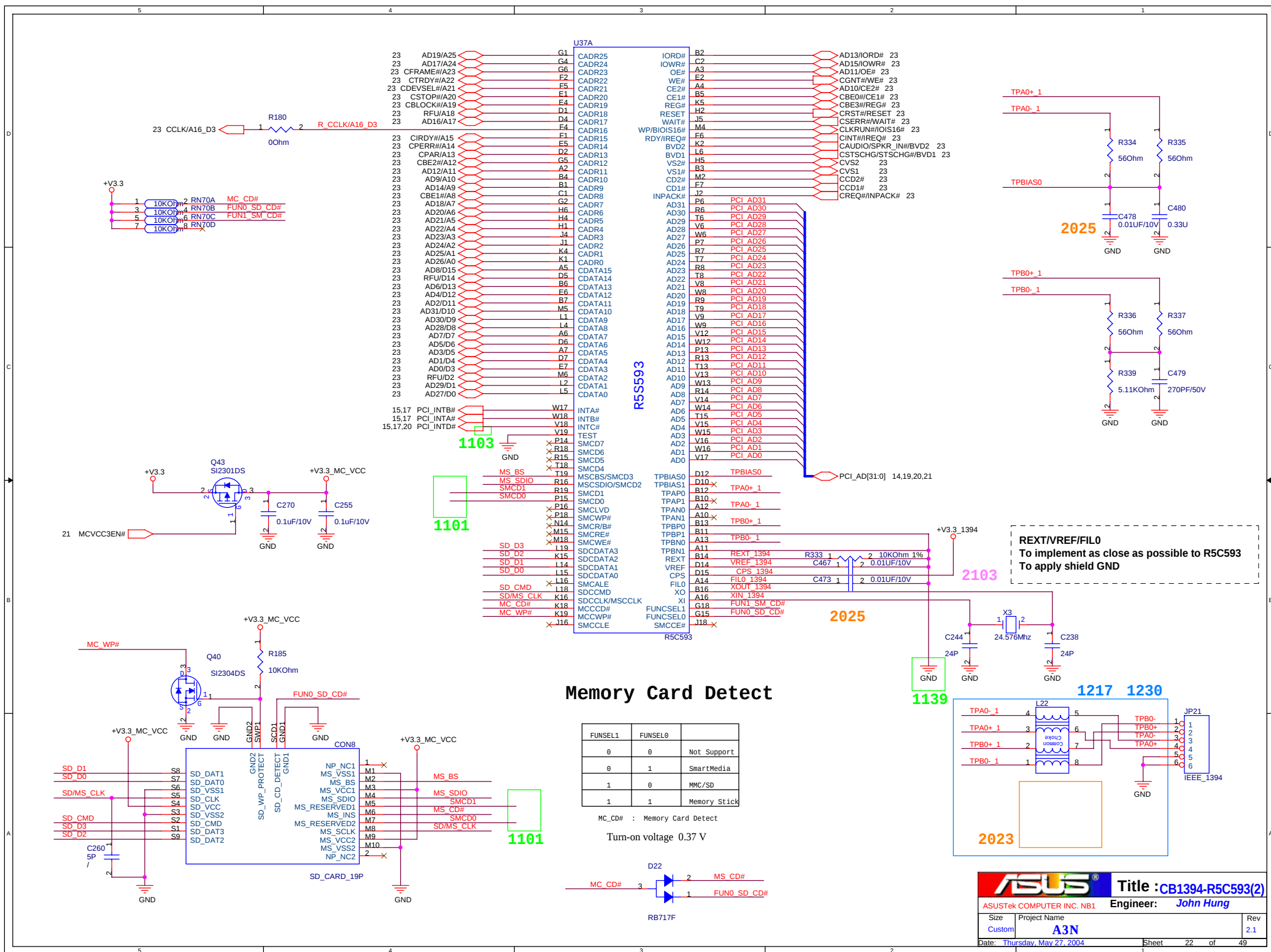
EMI

1142

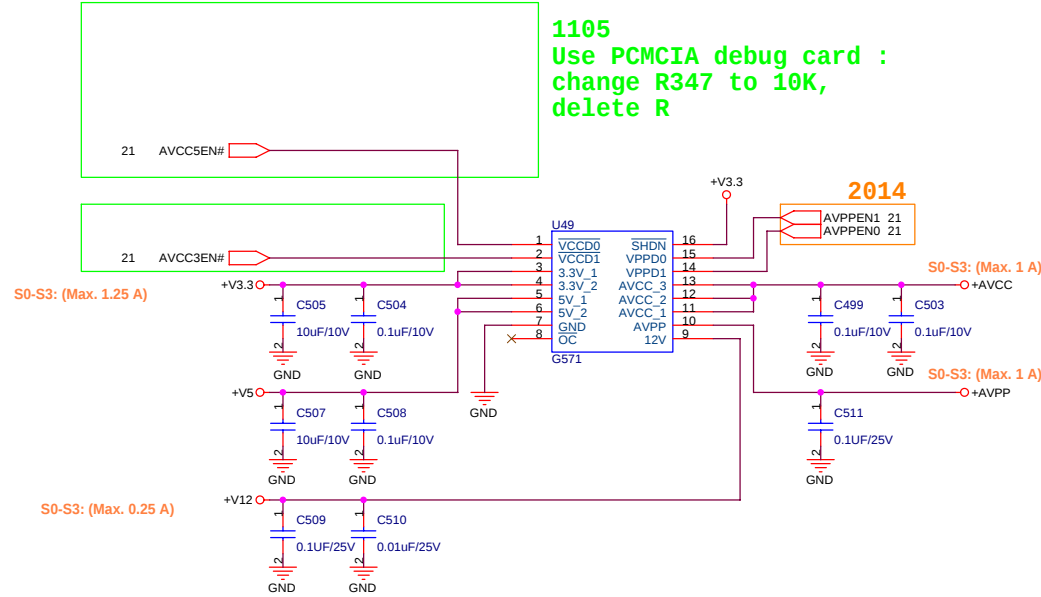
1142



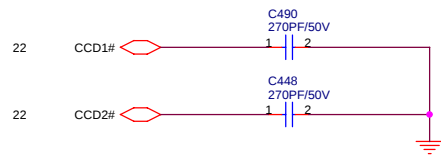




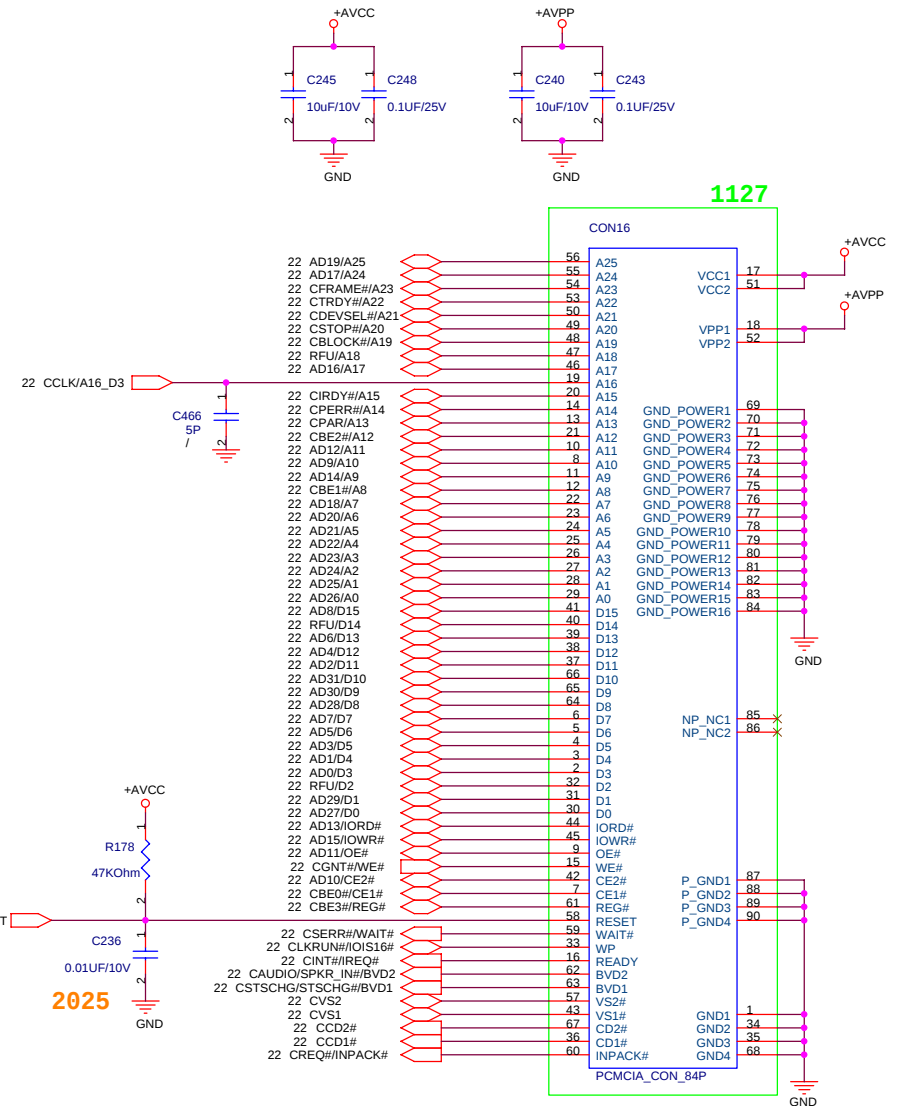
CB POWER SWITCH



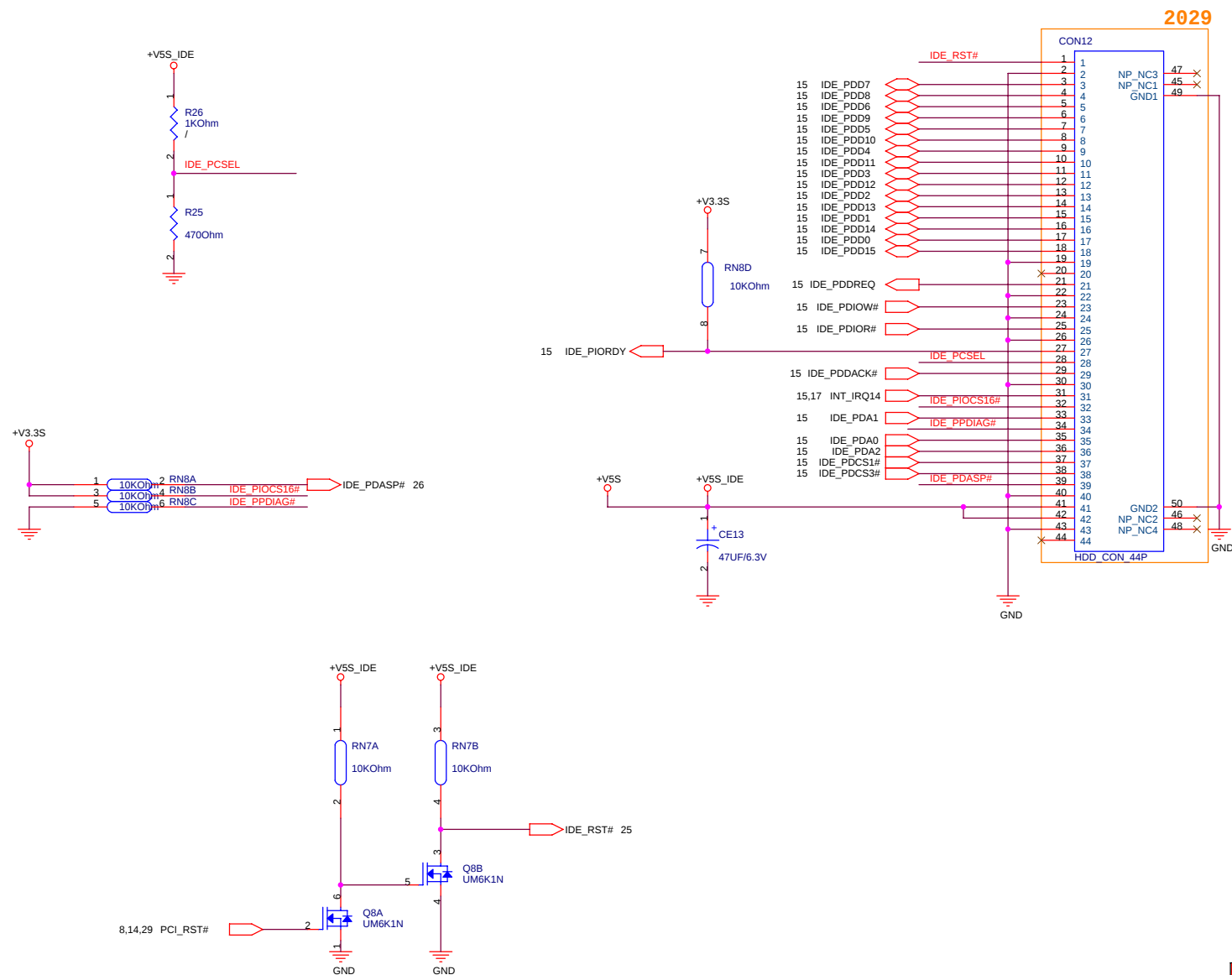
CB DE-BOUNCE

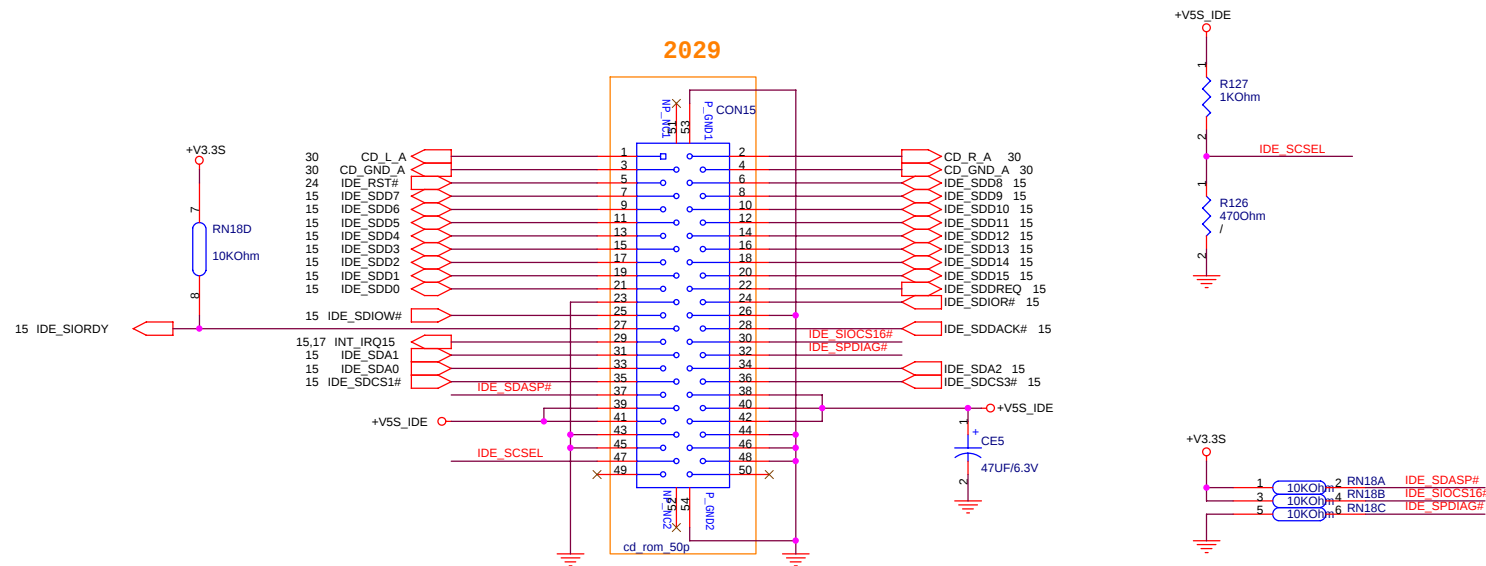


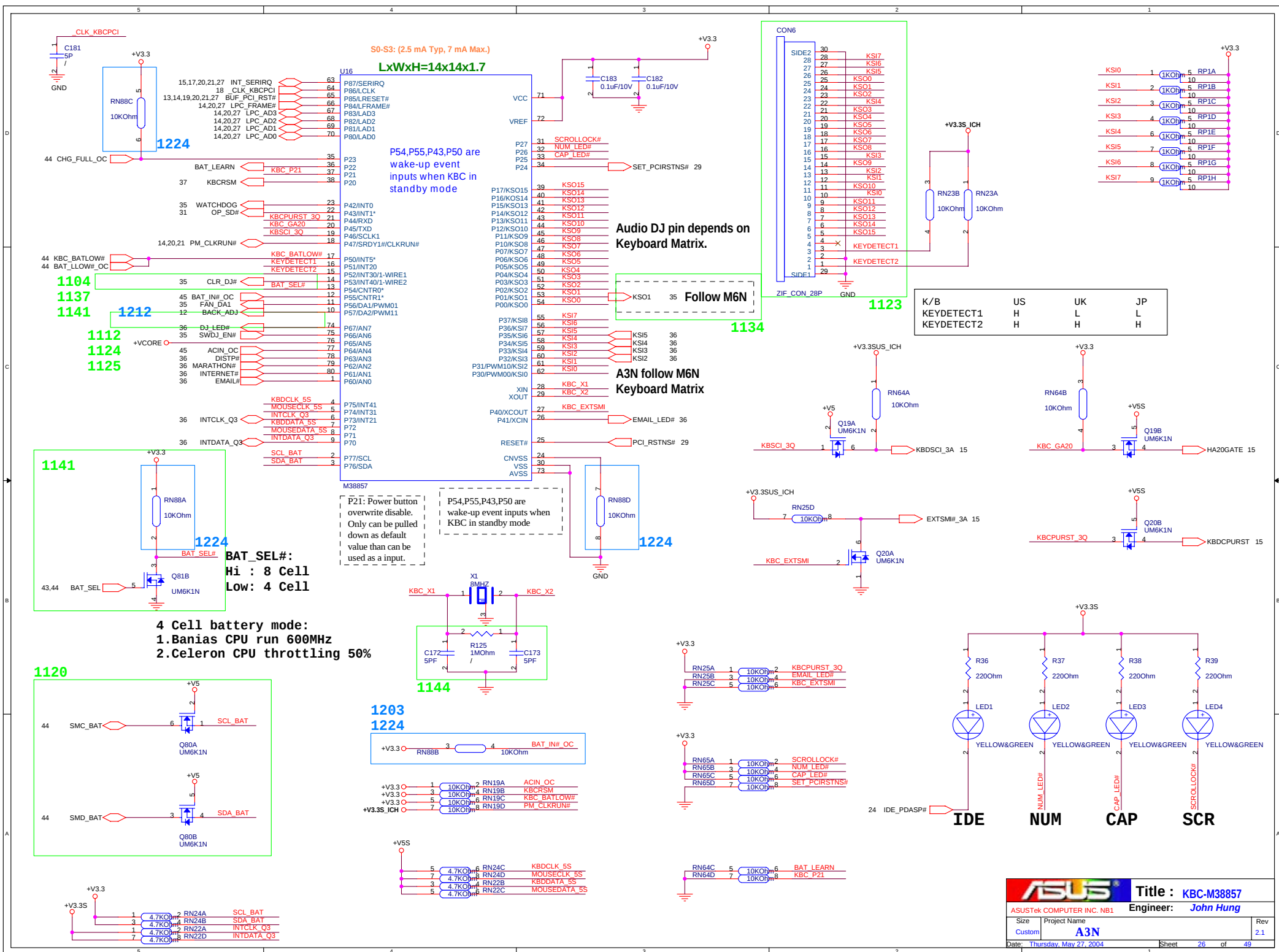
CB SOCKET



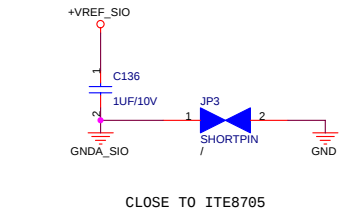
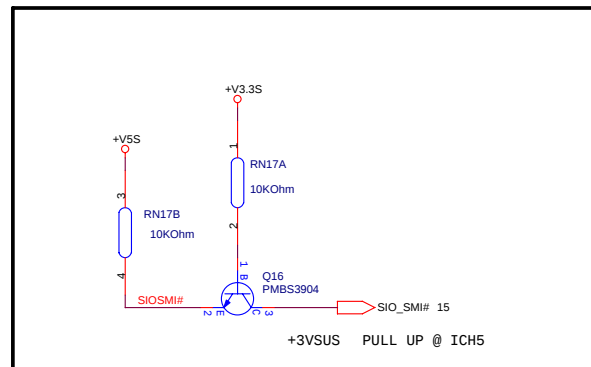
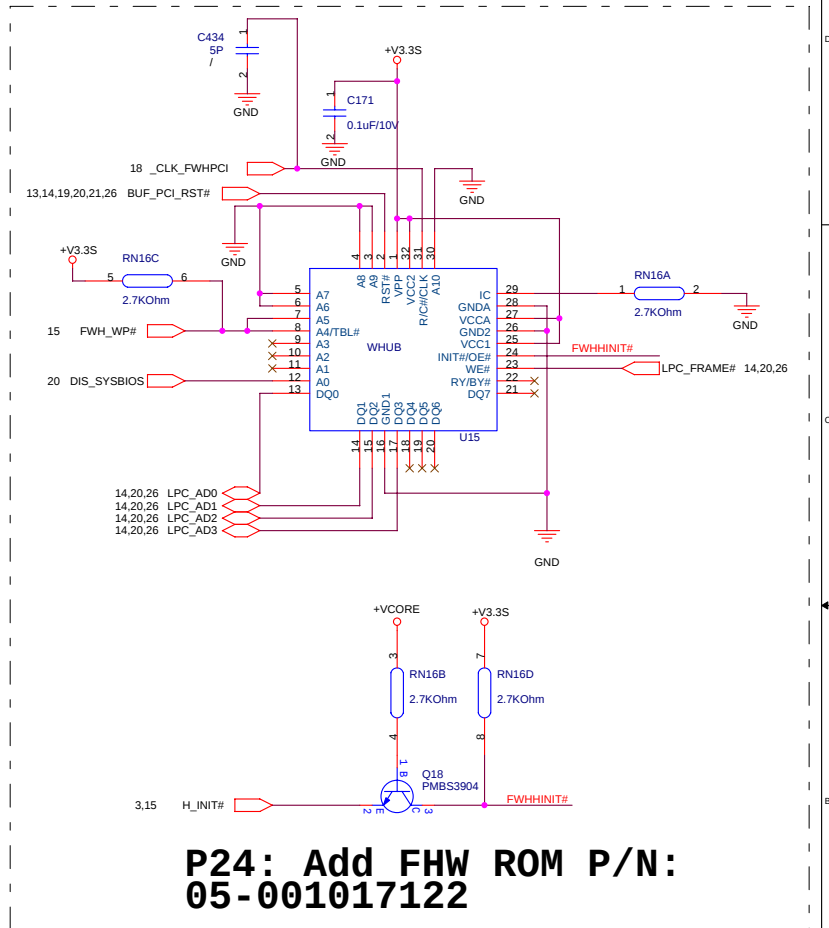
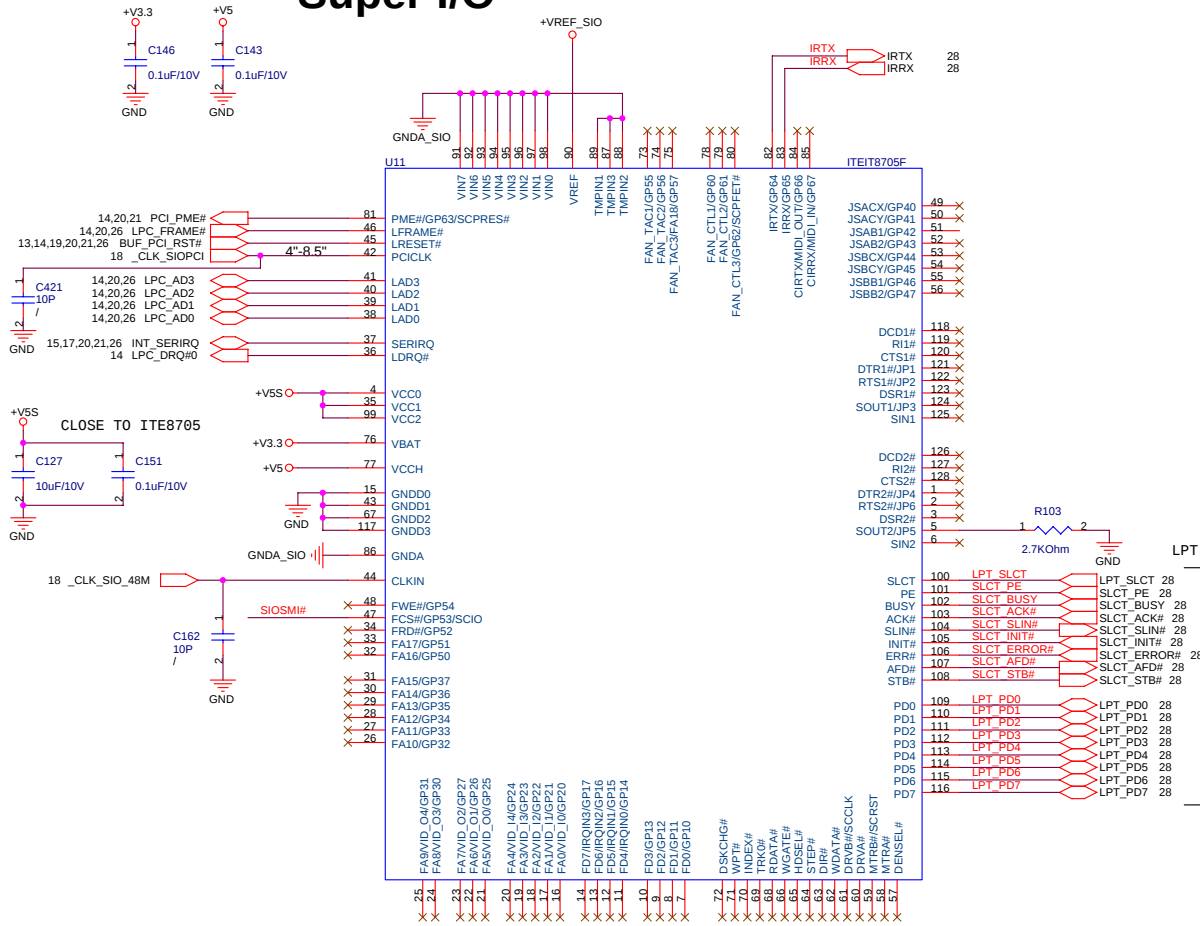
<Variant Name>

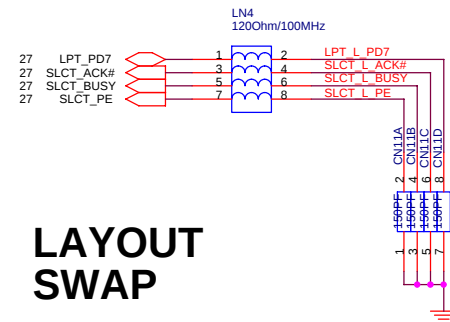
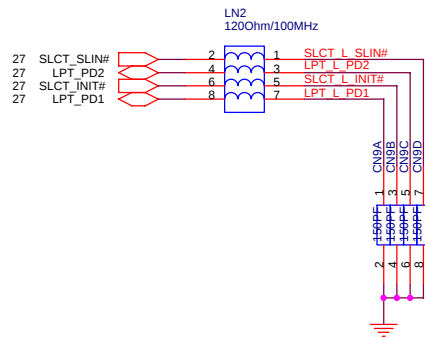






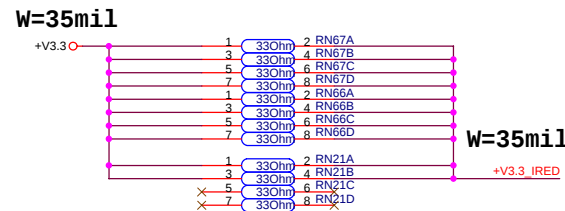
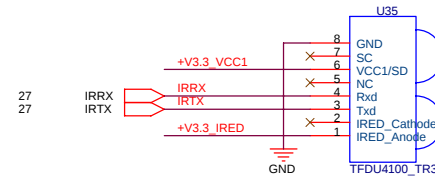
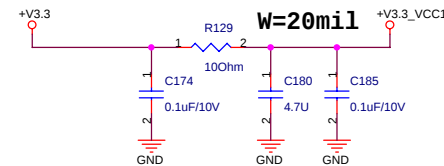
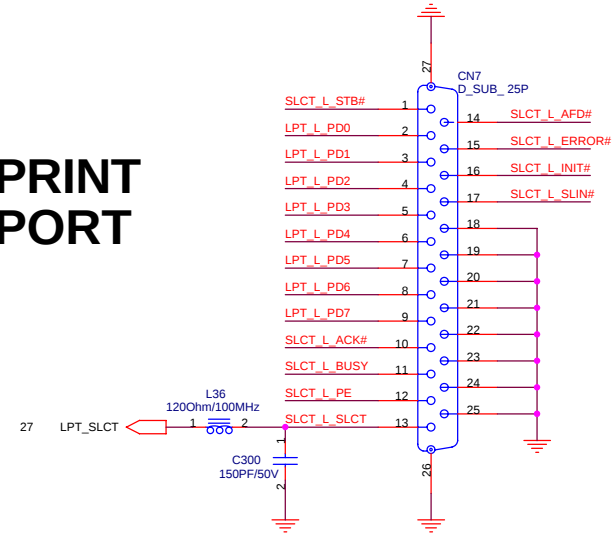
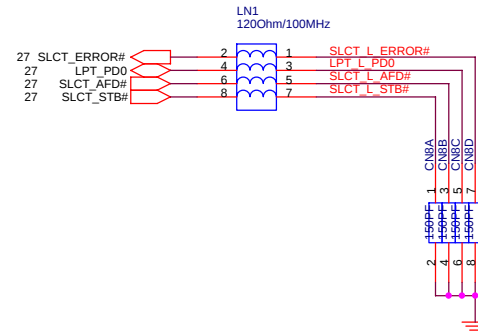
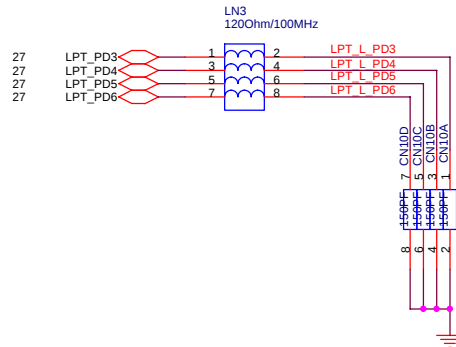
Super I/O



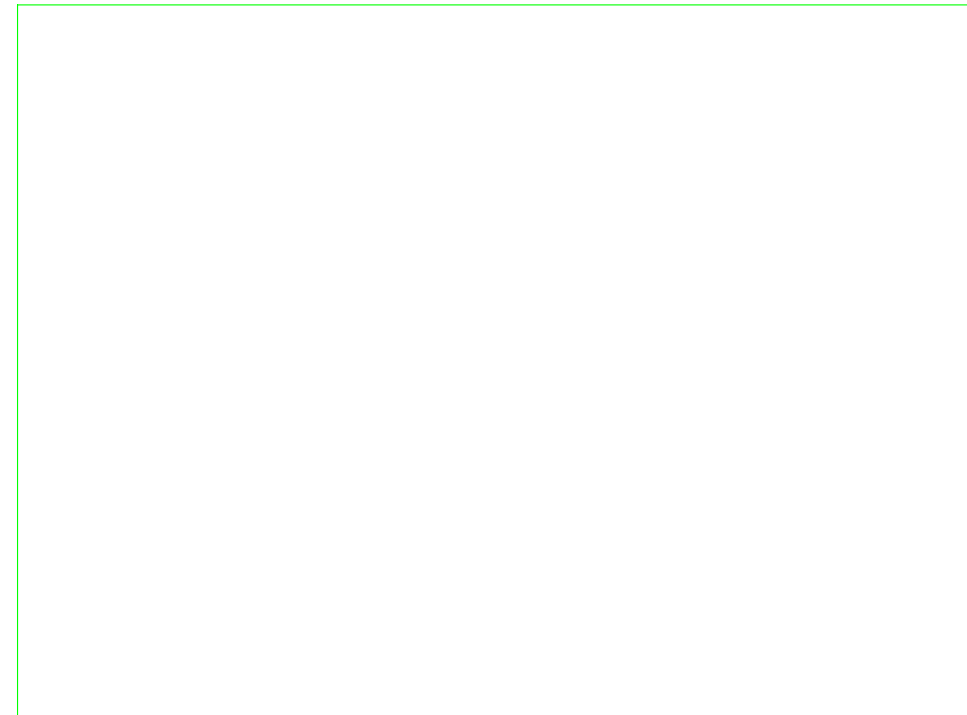


LAYOUT
SWAP

PRINT
PORT

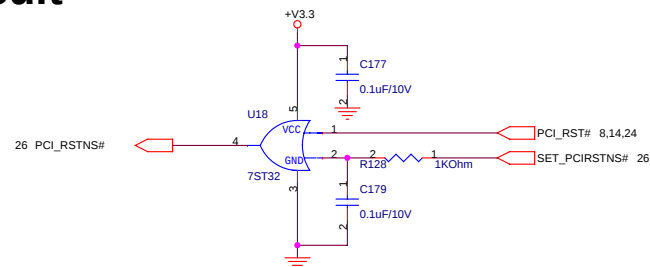


PCMCIA DEBUG Card

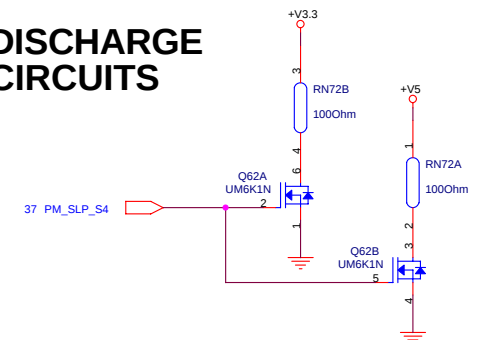


1105

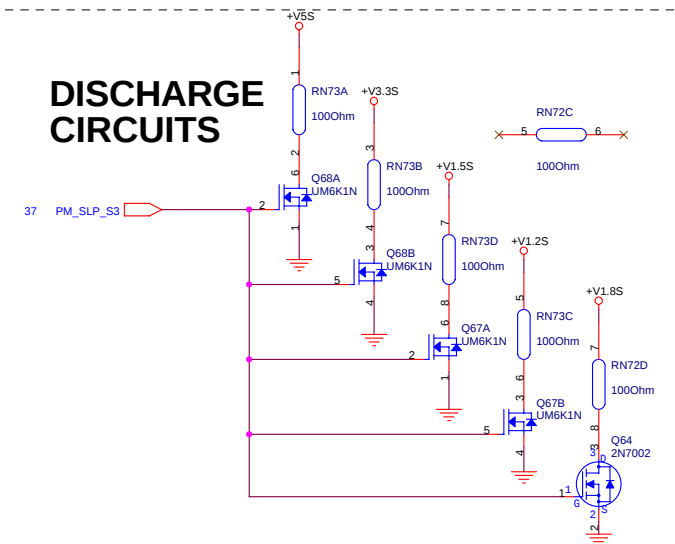
PCI_RSTNS# Gen Circuit



DISCHARGE CIRCUITS



DISCHARGE CIRCUITS



2024 R1.2 BOM change to 09-013103013

1230
2010
2103

R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.

$f(\text{highpass}) = \frac{1}{2\pi \cdot 3.14 \cdot R \cdot C} = 73$
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.

2018

R:1.2. For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.
1207

R:2.1 Use "OP_SD#", speaker will have "POP" noise after logo display when turn on system. Don't use "OP_SD#".

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

R1.2 BOM change to 09-013103013

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

2018

But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.

Prevent "POP" noise at speaker.

$$f(\text{highpass}) = \frac{1}{2\pi \cdot 3.14 \cdot C(\text{IL}) \cdot R(\text{IL})} = 500$$

$$f(\text{lowpass}) = \frac{1}{2\pi \cdot 3.14 \cdot C(150P) \cdot R(10K)} = 106K$$

BTL Gain = $-\frac{R(\text{FL})}{R(\text{IL})} = -\frac{10K}{10K} = -1$

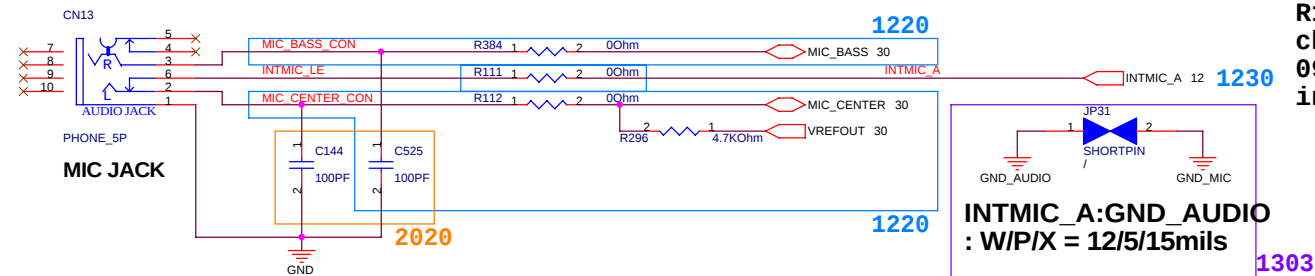
Speaker W = $\frac{V^2}{R} = \frac{V^2}{40hm} = 1W$

Can use 1W(40hm) speaker

1220

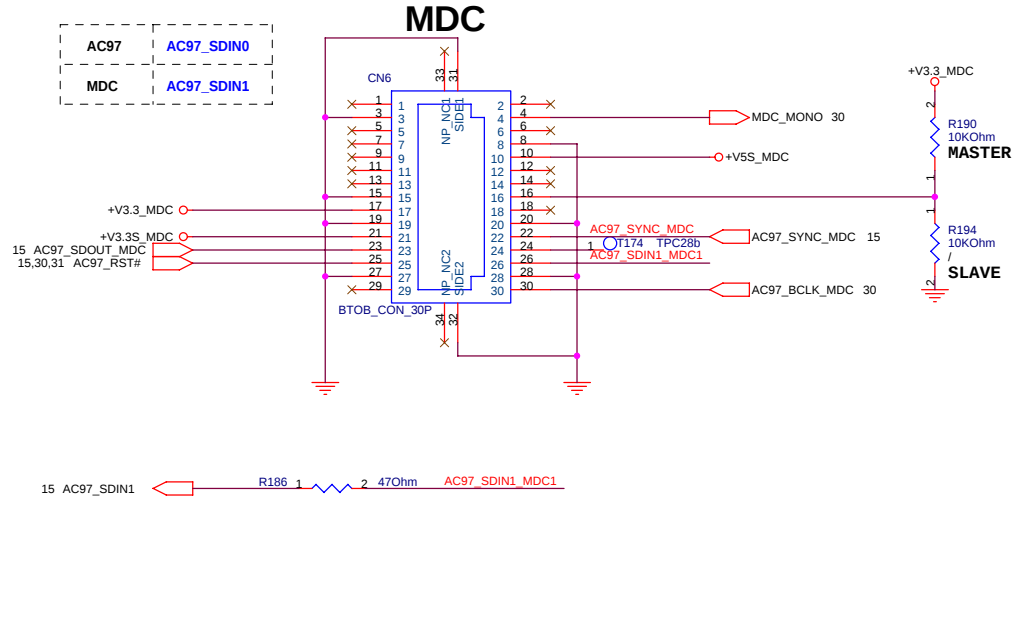
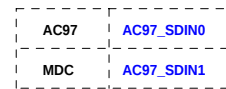
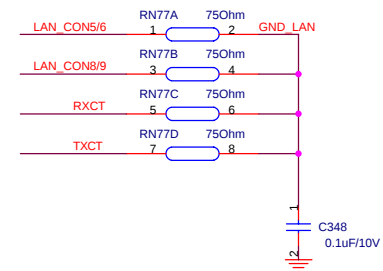
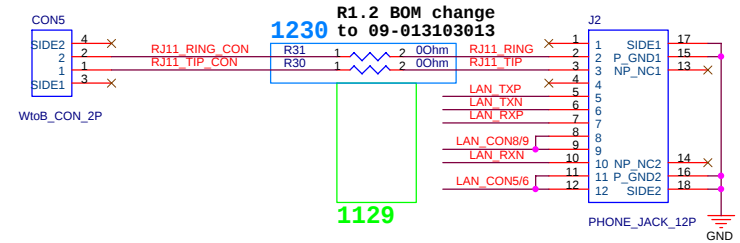
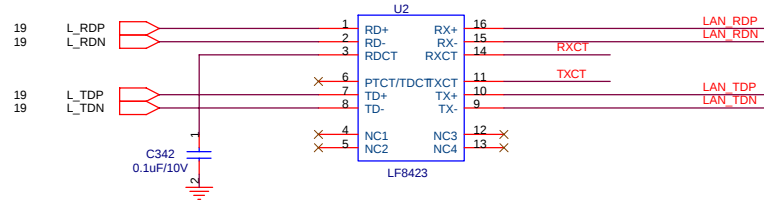
MIC OP CIRCUIT

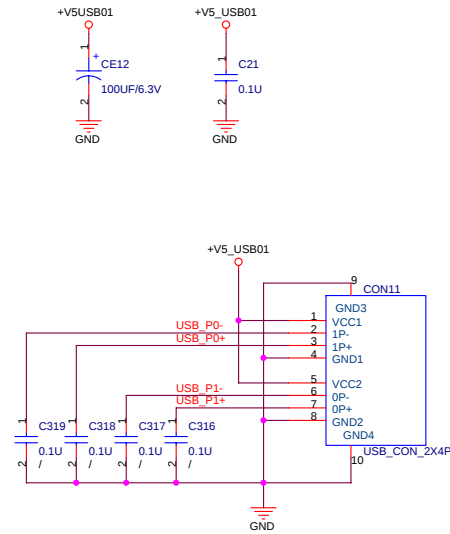
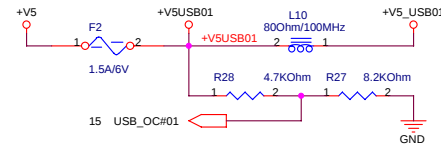
MIC JACK



R111 & R112
change to
09-013103013
in R1.2 BOM

OP: FOR EMI



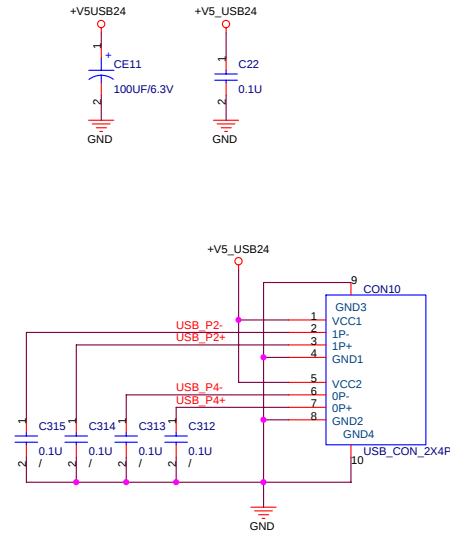
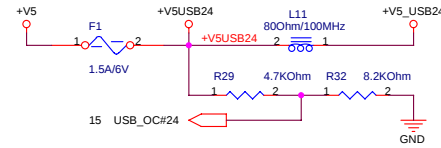


USB PORT 0 & PORT 1

2023
R & L Co-Lay

1128

**USB PORT 3 for CAMERA
Change to page 12**



USB PORT 2 & PORT 4

2023
R & L Co-Lay

1128

**USB PORT 5 for WLAN
Change to page 12**

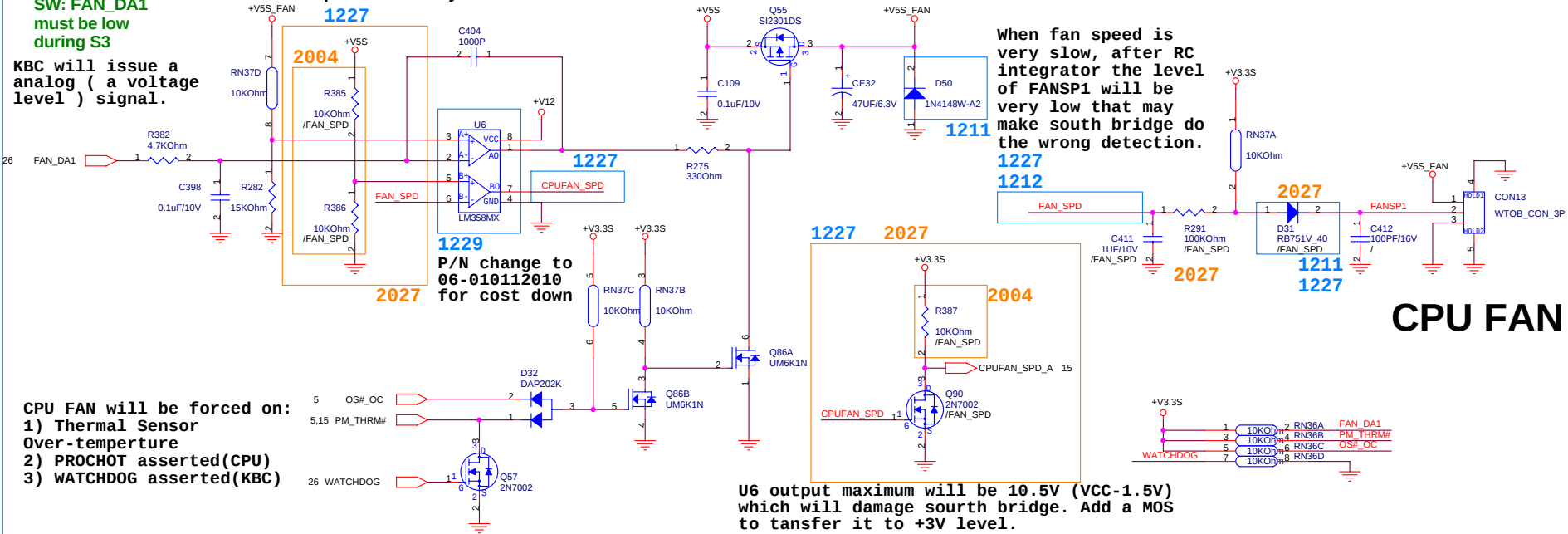
Fan Speed Control

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



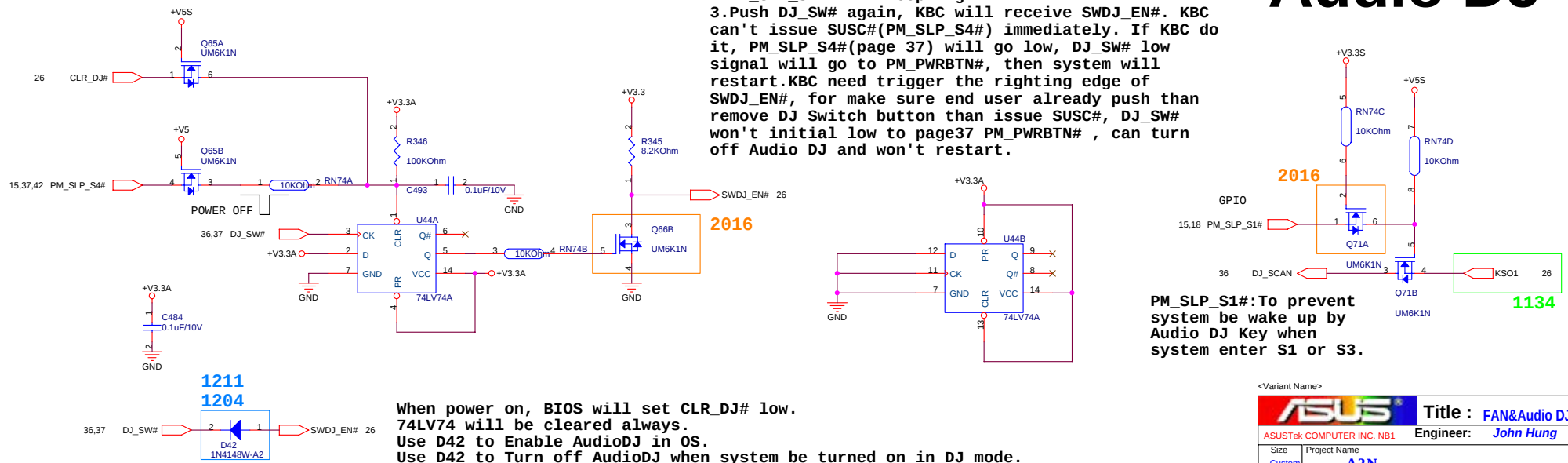
CPU FAN will be forced on:

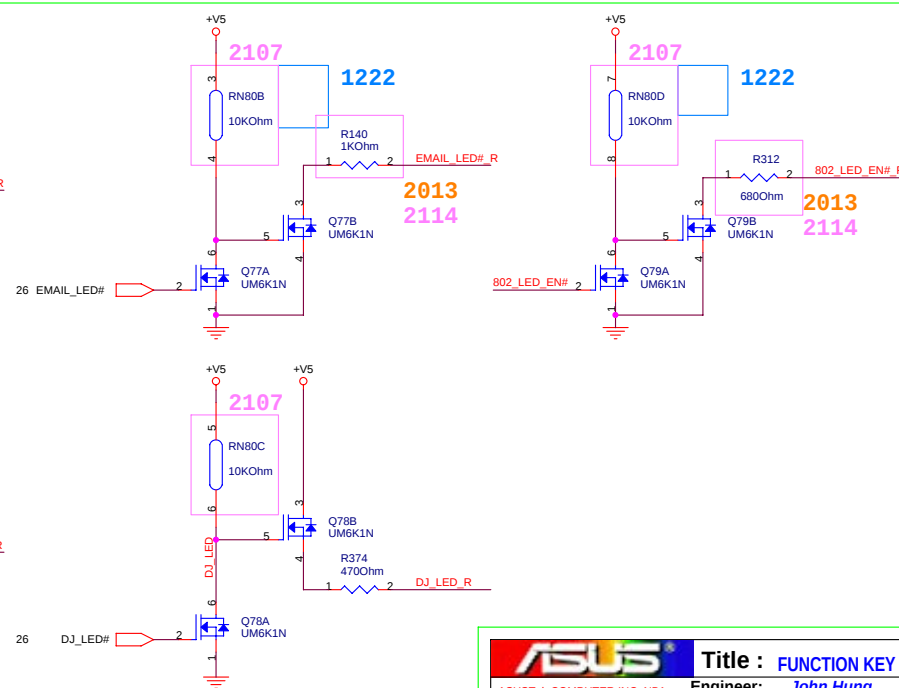
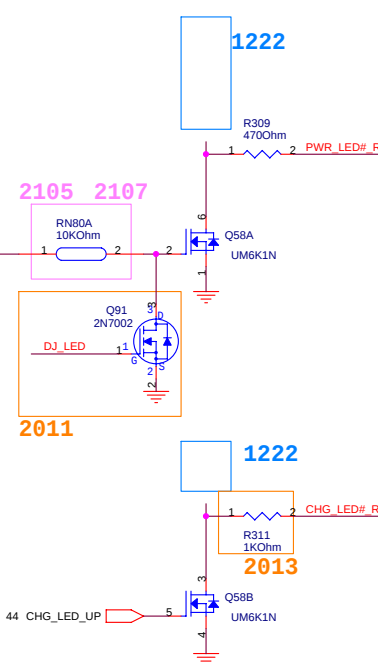
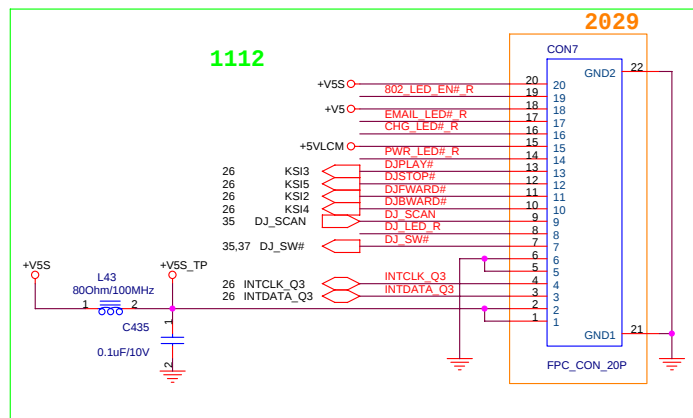
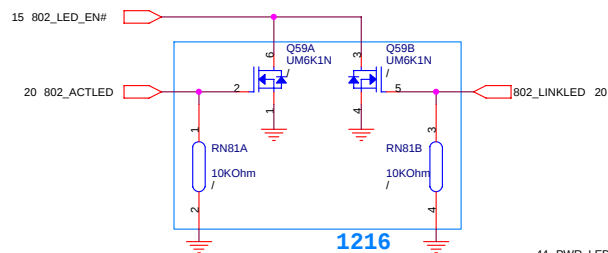
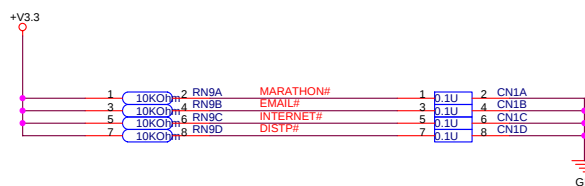
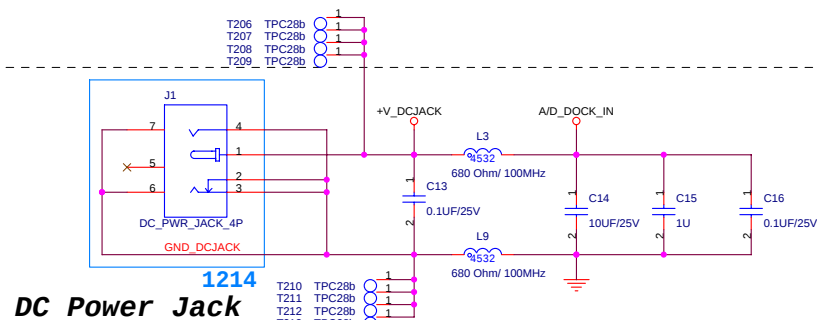
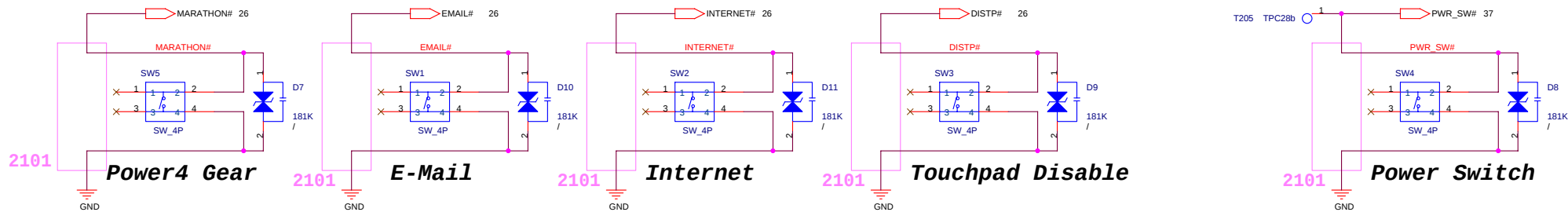
- 1) Thermal Sensor Over-temperature
- 2) PROCHOT asserted(CPU)
- 3) WATCHDOG asserted(KBC)

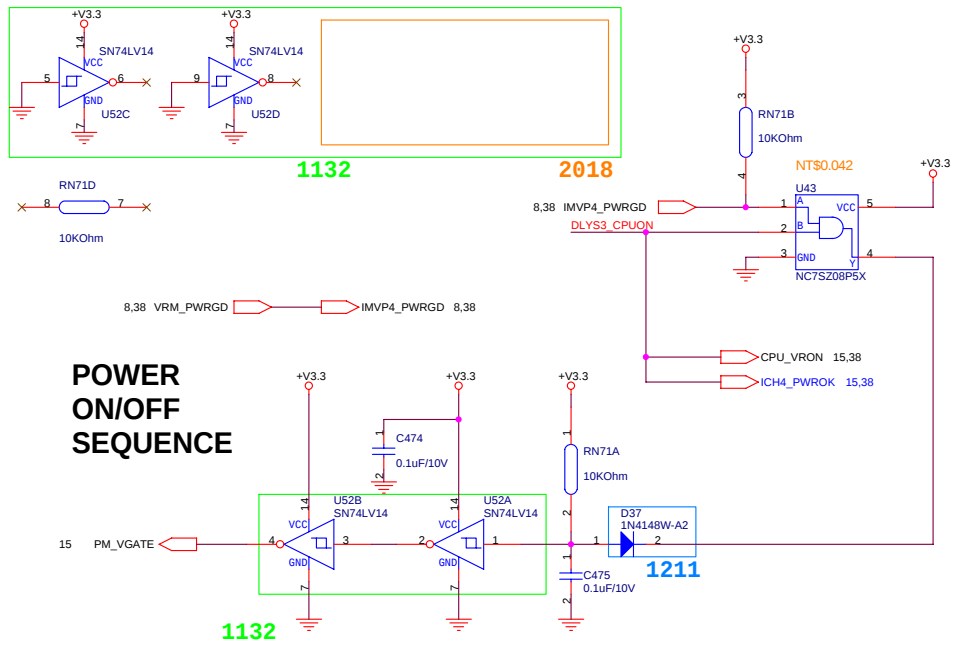
SWDJ_EN# function :

- 1.Push DJ_SW#, turn on Audio DJ.
- 2.PM_SLP_S4# will keep high.
- 3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.

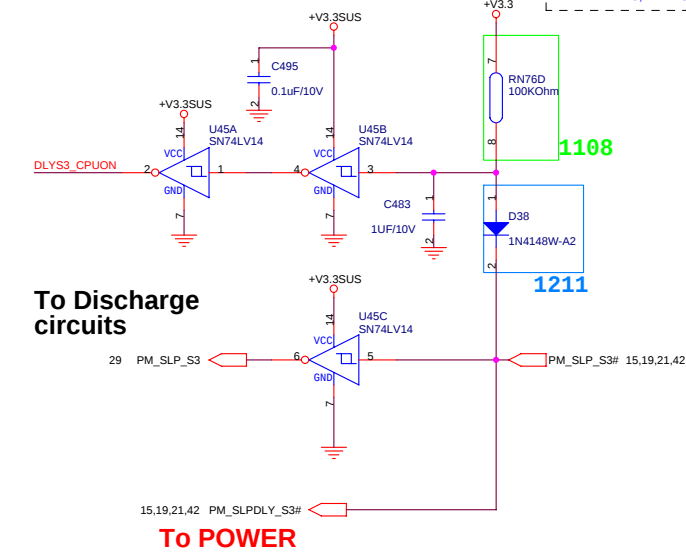
Audio DJ



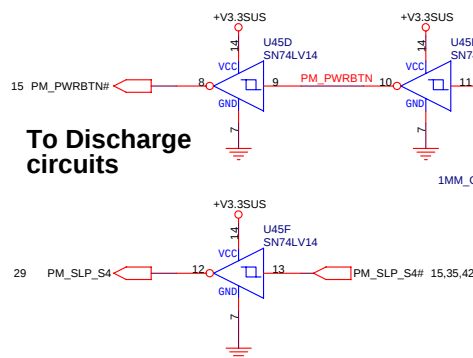




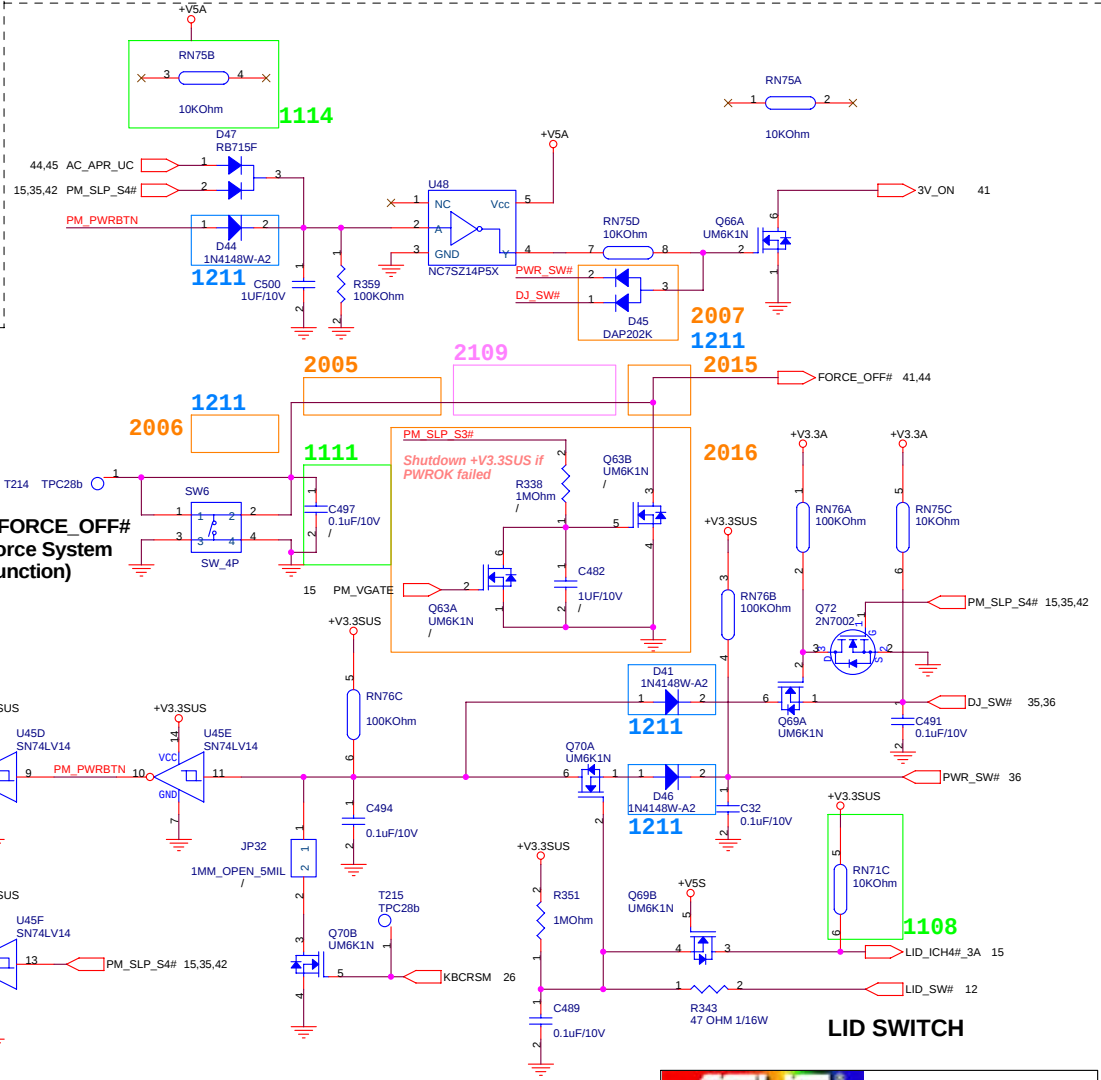
System Power Sequence
 +VCCRTC -> RTCRST# -> V5REFSUS -> 3.3/1.8VSUS -> RSMRST# -> SLP_S4# -> SLP_S3# -> VCCLAN -> LANPWROK -> V5REF -> VCC -> VCORE -> PWROK -> VGATE
 SUSSTAT# -> PCIRST#
 CPU : +VCORE, +VCCP, +V1.8S
 NB : +V1.2S, +V1.5S, +2.5V, +VCCP
 SB : +V1.5SUS, +V3.3SUS, +VCCP, +V1.5S, +V3.3S
 DDR : +V2.5, +V1.2S, +V1.25S

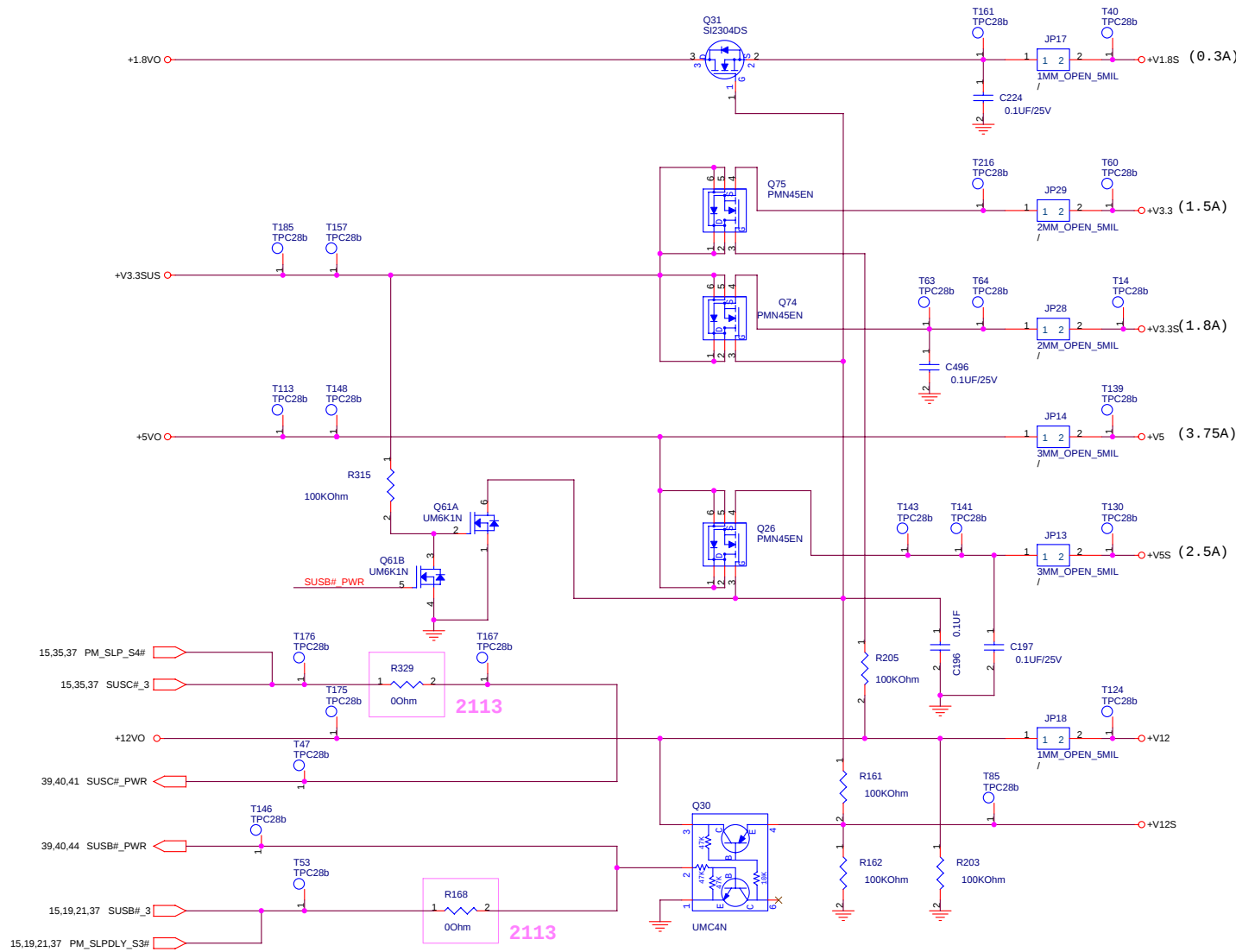


To Discharge circuits



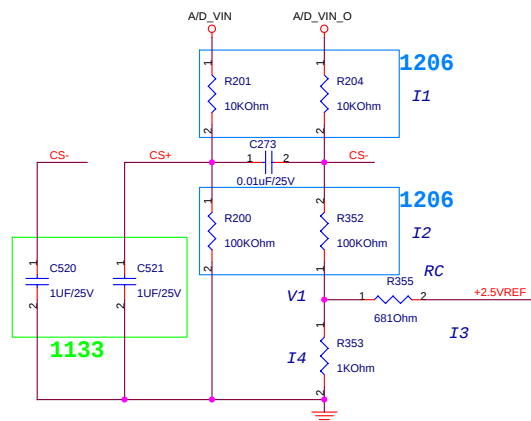
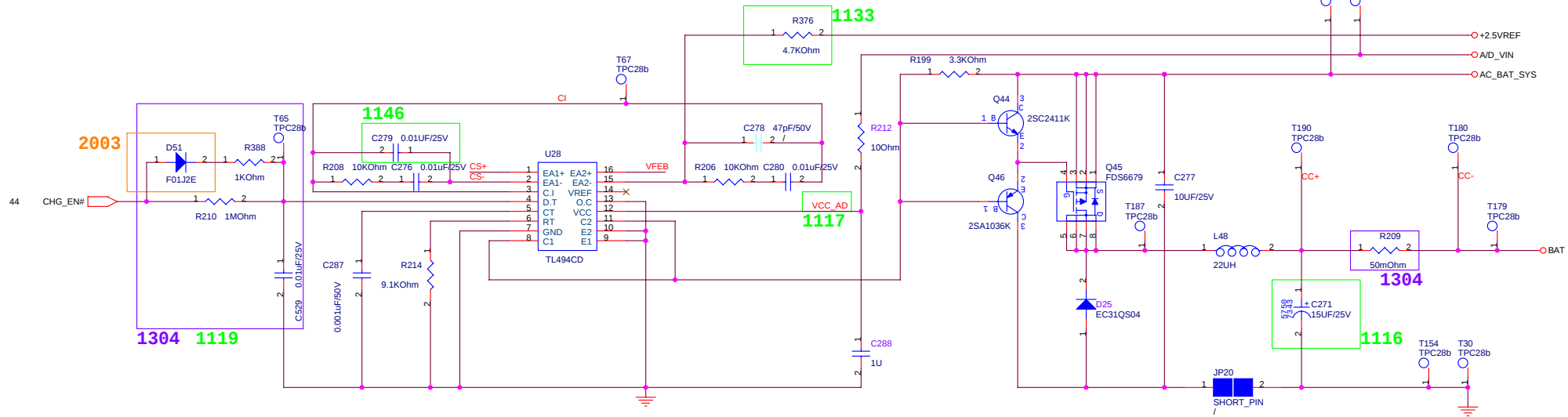
(Set FORCE_OFF# as Force System Off function)





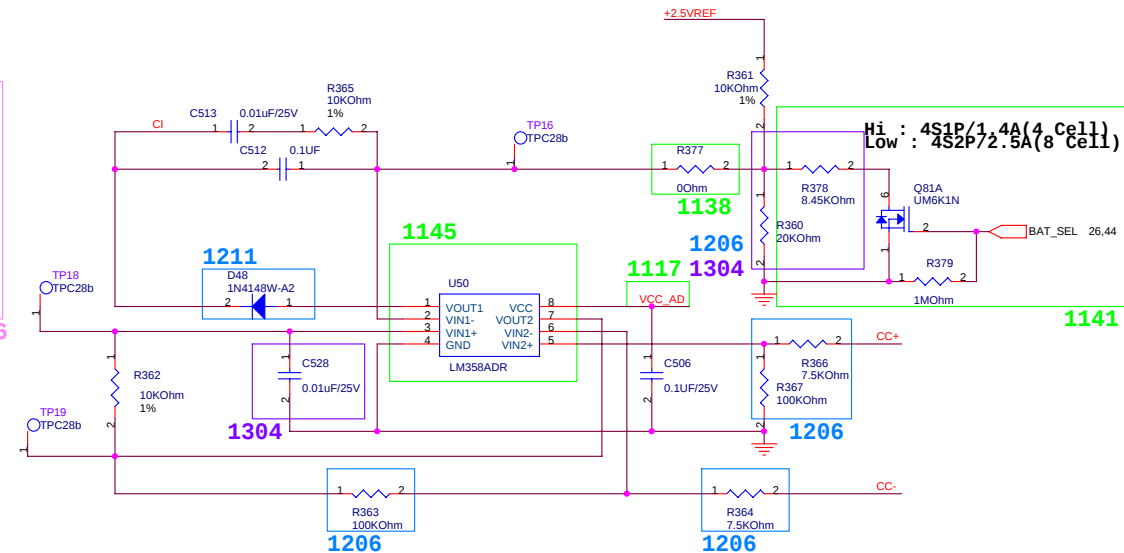
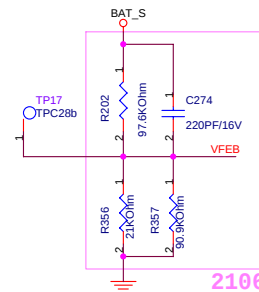
<Variant Name>

		Title : LOAD SYWITCH	
ASUSTek COMPUTER INC. NB1		Engineer: Adams Lin	
Size	Project Name	A3N	Rev 2.1
Custom			
Date: Thursday, May 27, 2004		Sheet 42 of 49	

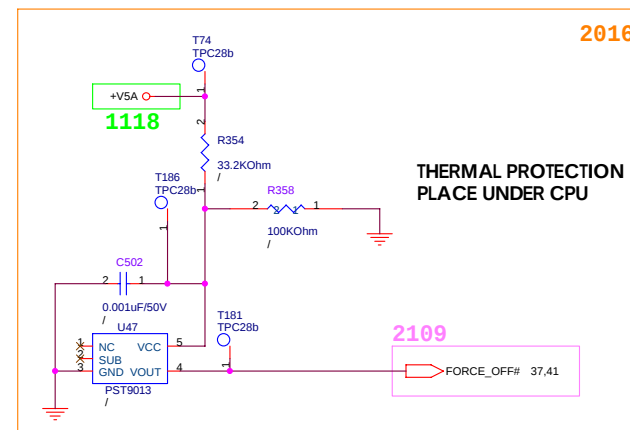
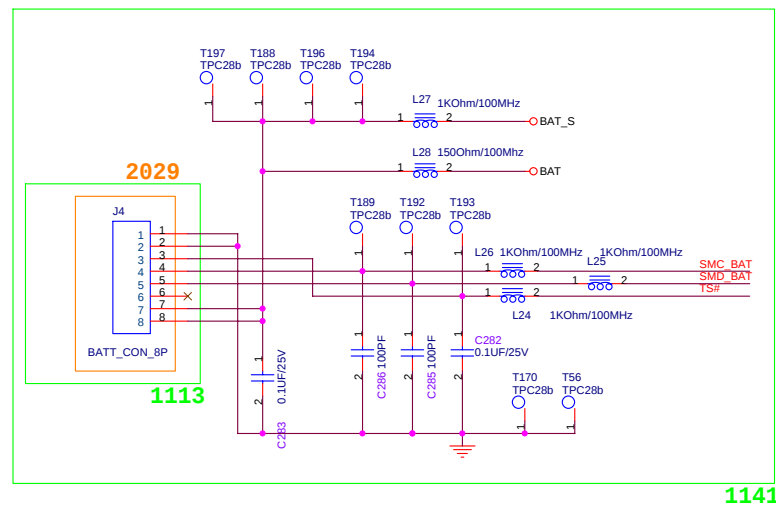
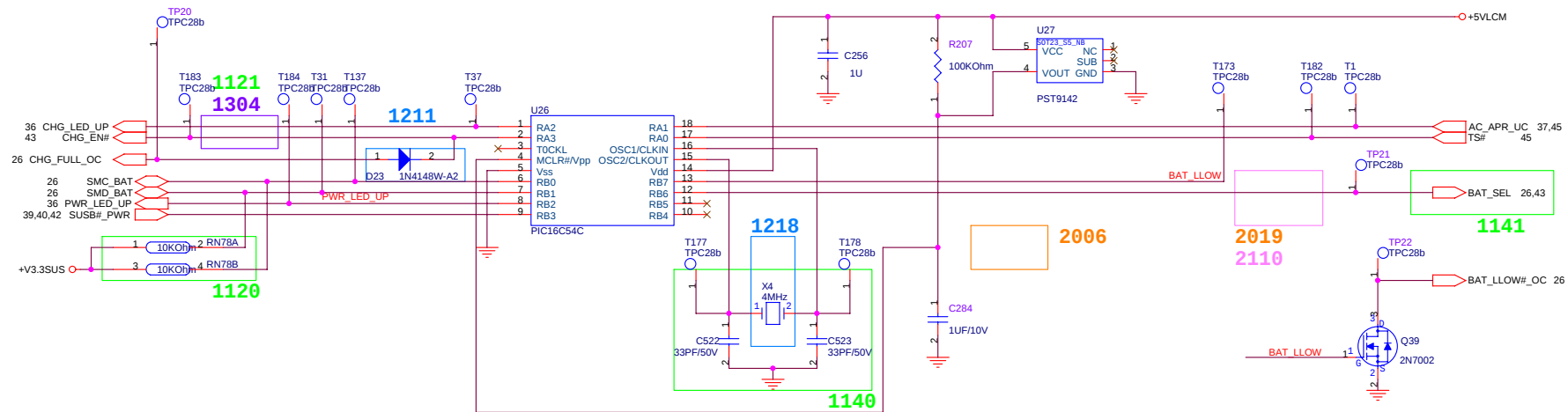


Current sharing = 3.1A

$A/D_VIN=19V$ $A/D_VIN_O=19V-3.1A*50mohm=18.845V$
 $CS+=CS-=19*(100/110)=17.272727V$
 $I1=(18.845V-17.272727V)/10K=0.15723mA$
 $V1=17.272727V-(0.15723mA*100K)=1.5497V$
 $I4=1.5497V/1K=1.5497mA$
 $I3=1.5497mA-0.15723mA=1.39247mA$
 $RC=(2.5V-1.5497V)/1.39247mA=681\ ohm$



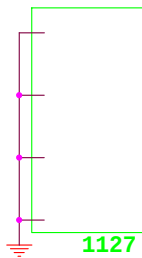
<Variant Name>



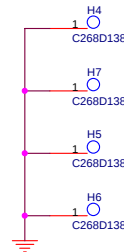
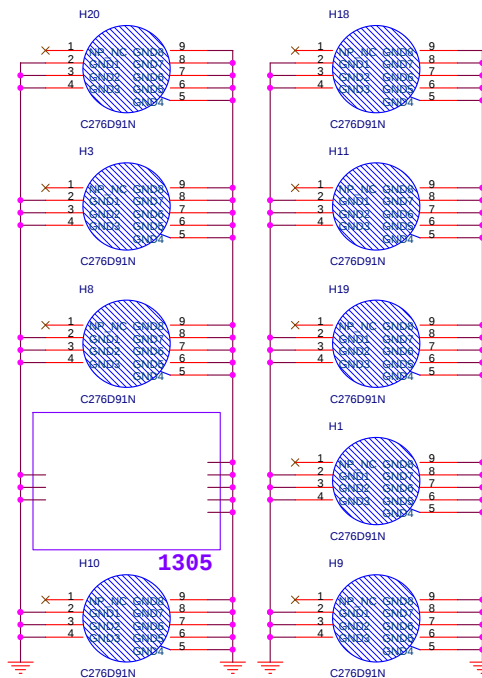
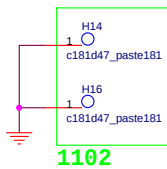
<Variant Name>

		Title : PIC16C54	
ASUSTek COMPUTER INC. NB1		Engineer: Adams Lin	
Size Custom	Project Name A3N		Rev 2.1
Date: Thursday, May 27, 2004		Sheet 44 of 49	

SCREW HOLE



For MDC module



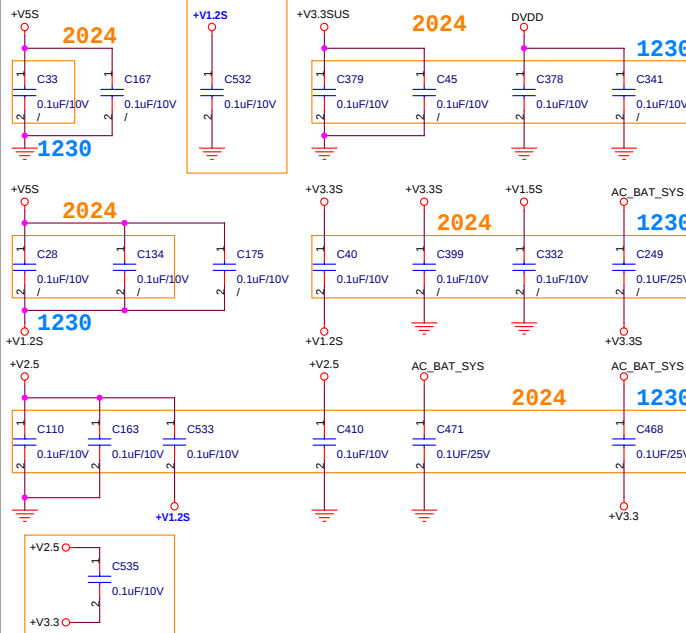
CPU Throttling(BIOS setting): 100 degree C.
System shutdown(BIOS setting) : 110 degree C.
~~H/W shutdown(page 44, U47 , no load) : 105 degree C(need fine turn R354).~~

Short Pad location:
Page37: JP32
Page39: JP4, 5, 15, 16, 19, 26, 27
Page40: JP6, 7, 9, 22, 24
Page42: JP13, 14, 17, 18, 28, 29

Don't Short Pad: JP26

JP4: +V2.5 --Power In
JP5: +V1.25S
JP6: +V2.5
JP7: +V1.2S
JP9: +VCCP
JP13: +V5S
JP14: +V5
JP15: +V1.5SUS
JP16: +V2.5 --Power IN
JP17: +V1.8S
JP18: +V12
JP19: +V1.8
JP22: +V1.5S
JP24: VREF5 --> +V5A
JP26: +3VALWAYS_T --> +V3.3A(open)
JP27: +3VALWAYS_M --> +V3.3A(short)
JP28: +V3.3S
JP29: +V3.3
JP32: KBCRSM

EMI



PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 20 mils

37.5 OHM WIDTH

TOP/BOT 12 mils

42 OHM WIDTH

TOP/BOT 10 mils

55 OHM WIDTH

TOP/BOT 5 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 9 mils/ 5 mils

90 OHM WIDTH/SPACE

TOP/BOT 7 mils/ 10 mils

100 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#0

MINIPCI PCI_REQ#1

LAN PCI_REQ#2

PCI_GNT#

CB&1394 PCI_REQ#0

MINIPCI PCI_REQ#1

LAN PCI_REQ#2

IDSEL

CB&1394 PCI_AD21

MINIPCI PCI_AD20

LAN PCI_AD16

PCI_INT#

CB&1394 PCI_INTB/A/D#

MINIPCI PCI_INTC/D#

LAN PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

Rev	Date	Description
R1.0	03/12/19	1. Initial release.
R1.1 Green Block	04/02/03	1. Connect SDD0,SDD1 for RICOH request. Page 22. 2. Add MDC screw hole P/N & footprint. Page 46. 3. Connect CardBus chip INTC to PCI_INTD#. page 22. 4. Change CB_SD# location from KBC to ICH4 GPIO25. page 15,21,26. 5. Delete PCMCIA debug card function. page 18,23,29. 6. Host clock frequency select failed.Add a pull-down R to FS3 so that FS[4:3]=00 and Host clock frequency=100MHz. page18. 7. Load wrong value. Change RN39~RN48 from 560hm to 100hm. page 6. 8. Load wrong value. Change pull-up RN . page 37. 9. The value in M3N schematic is wrong. Change HUB_RCOMP_ICH4 pull-up R from 48.7K0hm to 48.70hm. page 14. 10. Modify +V3S to +V3.3S. page 30. 11. Can not boot in battery mode.Remove C497. page 37. 12. Modify 20-pin connector pin define and add DJ_LED function for new touchpad. page 26,36. 13. Due to height limitation, change BATT CONN. page 44. 14. Remove the pull-up RN75B because AC_APR_UC has been pulled-up in page 45. page 37. 15. Change CRT CONN because the original one was reversed. page 12. 16. C271 change form 10UF/25V/X5R to 15UF/25V/POSCAP. page 43. 17. U50 VCC change from +5VLCM to VCC_AD(19V). page 43. 18. For wrong connection, change R354 pull-up power plane from +5V0 to +5VA. page 44. 19. Change R210 from 47K to 470K/0402. page 43. 20. Add RN78 to pull high SMC_BAT and SMD_BAT, and add UM6K1N to prevent leakage current into KBC. page 26,44. 21. For Power RD request, add R370 to CHG_EN#. page 44. 22. Replace RN32 with 3 single 100K resistor. page 45. 23. Change KB CONN pin definition because R1.0 was reversed. page 26. 24. Remove INVTER_A from KBC and load L33 because BIOS RD decide to use NB to control the pannel backlight. page 12,26. 25. Because P67/AN8 of KBC38857 cannot receive PWM signal, move CPUFAN_SPD_A to P57/DA2/PWM11 of KBC38857. page 26. 26. Change LEDs' power to 5V level. page 36. 27. Modify PCMCIA socket footprint. page 23,46. 28. Combine connector : Change CON1,delete CON3,CON4. page 12, 34. 29. Swap LAN connection(J2 pin5-12) for wrong connecting. page 33. 30. Modify PM_RSMRST# circuit. page 37. 31. For cost down, change X5,X7. page 19,30. 32. Combine two NC7SZ14P5 into one SN74LV14APWR for cost down.page 37. 33. To reduce jitter when charging, add R376,C520&C521. page 43. 34. For M6N R1.1 wrong connection, change Audio DJ DJ_SCAN pin from KS04 to KS01. page 26,35. 35. For Power RD request, add two beads L53&L54 at Vin Side. page 38. 36. Modify EDID and panel ID optional circuit. page 12. 37. Change CLR_DJ# to P53 because P54 of M38857 cannot be configured as output. page 26. 38. Add R377 for Power RD request. page 43. 39. Based on Ricoh's suggestion, remove CB_AGND and connect all AGND to generic GND. page 21,22. 40. For cost down, change X4. page 44. 41. Modify for battery 4S2P and 4S1P application. page 26,43,44. 42. For EMI RD request, change Cap of CRT Pi-filter from 3.3pF to 15pF. page 13. 43. Delete spread spectrum IC ICS91718 circuit because few model use it and not easy to buy. page 18.

Rev	Date	Description
R1.1 Green Block	04/02/03	44. Change C172 & C173 from 22pF to 5pF and unload R125 to obtain more accurate 8MHz frequency. page 26. 45. For cost down, Power RD request to change Q9&Q11 to 07-005198012, U30 to 06-006002411, and U50 to 06-010112010. page 38,43,45. 46. For Power RD request, change , C266 from 33pF to 220pF, C279 from 0.1uF to 0.01uF. page 41,43. 47. Change U29 P/N for ME. page 31.
R1.2 Blue Block	04/02/19	1. LAN_RST# changes to 10K Ohm pull-down to GND. Page 15. 2. To be able to hear low frequency in headphone mode, change C423 & C424 from 10uF/10V to CE30,CE31 47uF/6.3V. Page 31. 3. Pull high BAT_IN#_OC, whose OC means Open Collector, to +V3.3 at KBC. Page 26. 4. There is only one SS0540 in A3N, change to 1SS355. page 35. 5. The power of LCD EEPROM connect to +V3.3S_LCD. When BIOS want to read EEPROM data, the EEPROM is still OFF,because +V3.3S_LCD is not enabled at this moment. Change EEPROM power to +V3.3S. page 12. 6. Change R360,R363,R364,R366,R367,R378 value for charger at C.C. mode and change R200,R201,R204,R352 at C.S. mode to get more accurate current limit value. page 43. 7. Add de-POP(reduce pop noise) circuit. page 31. 8. Change Fan control function from PWM mode to DC mode. page 35. 9. Based on Power RD's request, change Q33,R169,R148,R324. page 40,41. 10. S5N can not turn on some panels since its diodes in inverter circuit have higher forward voltage. Follow S5N, change DAP202K and 1SS35 in inverter circuit to Schottky diode RB717F and RB751V-40 respectively. page 12. 11. Electrical characteristics of diode 1SS35 and 1N4148-A2 can be compatible, but 1N4148-A2 has lower price. For cost down, change 1SS355 to 1N4148-A2. page 12,16,21,35,37,40,43,44,45. 12. Change "Back light adjust" function from North Bridge to KBC. Change "CUPFAN_SPD_A" from KBC to ICH4 for BIOS request. page 8,12,26,35. 13. For cost down, change audio AMP from APA2020A to G1420. page 31. 14. A3N R1.1 uses the same AC_IN jack as L3F, which was found easy to be damaged. Change it to solidier one used on A2. page 36. 15. Follow M6N and W1N to modify RTC circuit. page 15. 16. Un-mount Q59 and RN81 to control WLAN led directly from SB's GPIO pin: 802_LED_EN#. page 36. 17. Swap 1394 TPB0+/-,TPA0+/- for smoother layout. page 22. 18. X4 is dip type and at top side which may be lost in SMT IR re-flow for bottom side. Change X4 to SMD type. page 44. 19. Add mini-PCI and USB WLAN hardware disable circuit page 12,15,20. 20. QT report a bug: The "Center/Subwoofer Speaker Out" is invalid after setting "Number of Speakers" to 6-channel mode for 5.1 speaker output and then executed "Speaker Test". Modify relative circuit. page 30,32. 21. Fine tune audio amp low-pass frequency. page 31. 22. Delete RN79 because after experiment we find it can be un-mounted. page 36. 23. Remove LCD EDID relative circuit. page 8,12. 24. Combin R191,R308,R380 and R381 into 4R8P RN88. page 26. 25. Follow S5N to modify CRT_DDC circuit to prevent current leakage. page 13. 26. Although crystal DIP type is cheaper than SMD type, but costs more manpower. Change X5 and X7 back to SMD type. page 19,30. 27. Improve accuracy of reading fan speed. page 35. 28. Swap RN4 and pin8,9 of RP4 for smoother layout. page 13,17. 29. For cost down, change U6 and U12 NS LM358MX (06-010008000) to TI LM358ADR (06-010112010). page 30,35. 30. For EMI RD's request to modify BOM. page 18,19,22,30,31,32,33,46. 31. Add description of choosing 855GM or 852GM/GME/GMV platform by changing R148. page 40. 32. Debug code will stop at "A0" or "06". Modify SMBus layout: 1. Daisy chain routing. 2.Don't cross power plane when the trace refer to power plane. Page 17.

Rev	Date	Description
R1.3 Purple Block	04/03/11	1. Pin23, ISOLATEB, of LAN 8100CL need to be low in S3. Follow MB P4PE-X to connect it with PM_SLP_S3#. page 19. 2. Debug Code will stop at "13". Change SMBus Pull-High RN29 from 4.7KOhm(0402) to 1KOhm(0603). page 17. 3. Improve MIC layout. page 12,32. 4. For Power RD's request to modify charger circuit. page 43,44. 5. Delete screw hole H2, to prevent CN7 short with H2. Layout engineer create a new screw hole. page 46. 6. For Power RD's request to modify BOM. Change R108 from 100K to 75K for OCP, un-mount R93 and mount R94 to meet Intel CPU spec. page 38.
R2.0 Orange Block	04/04/15	1. Sometimes Debug Code will stop at "00" in ON/OFF test. Modify power sequence circuit , delete R163. page 38,40. 2. Based on request came from factory to update all testpoints' symbol because all testpins are changed from 75mil to 68mil. All pages that include test points. 3. Power team request, cost down D51 part. page43. 4. Fine-tune R385,R386 and R387 to get more accurate level of fan ON/OFF detection. page35. 5. When system with battery only. System can't be power on after push Force OFF button SW6. Because SW6 connect to SHUT_DOWN#, but this signal will be latch low(power design: when battery low, page 46 : battery low detect circuit will issue low than latch it.) when it is at low state. Don't connect SHUT_DOWN# to SW6 at page 37.(SHUT_DOWN# already connected to 3V_ON at page 41. Connect SW6 to U25, and change D40 to 1N4148(delete at item 2015). Page 37. 6. Because A3N use SW6 as "Force OFF" button ,not "Reset" button. We don't need connect SW6 to PIC16C54C. Delete D24.page37,44. 7. Can't turn on Audio DJ when system only with battery and no adapter. Because +V3.3SUS will be turn off when system only with battery. Need turn on +V3.3SUS by connect DJ_SW# to 3V_ON. Change D45 to DAP202K. Page 37. 8. LAN crystal accurate is 39.2ppm, it can't meet spec. +/-30ppm). Change from 15pF to 18pF to meet spec. page 19. 9. Some system can't boot by battery only. Because signal "SHUTDOWN#" be latch at low state. Change R6 value from 470K to 100K. Page 45. 10.QT bug : Noise occur from headphone via speaker out jack. Change R124,R298,R285 from Bead to 0 ohm. Page 30,31. 11.The Power LED should not be bright when enabled Audio DJ in power off mode. Page 36. 12.The inductor will cause the 2.5V power control loop unstable. Change L40 to R389 Page 19. 13. Balance the LED Brightness. Fine tune R value,R140 470-->220,R311,R312 470-->1K. Page 36. 14. G571(U49) 593 Control Signal(U37) VPPD0 : VPPEN1 VPPD1 : VPPEN0 Otherwise, CardBus Card may be destroyed. Page 23. 15. When issue OTP_RESET#, system can't be turn off & display white screen. Because LTC3728 can't be shutdown by only put low 3V_ON. Need shutdown +V3.3SUS & +V50 at the same time. Delete D40. Page 37. 16. Change Q63,Q66,Q71 and no load Q63,R338,C482,R354,R358,C502,U47 for cost down. page 35,37,44. 17. Add test point for Taipei Factory request. page 6,12,15,16,19,30,36,37,38,39,42,43,44 18. QT bug: Pop noise can be heard via headphone when system boot, restart and resume from S3. Modify De-Pop circuit. page 31,37. 19. Taipei factory request : Add R391 for different battery charge current test at 8 cells and 4 cells. Page44.

Rev	Date	Description
R2.0 Orange Block	04/04/27	20. EMI request, load C144, C525. page 32. 21. ICH4 GPIO [24:43] , default state is output high, if PID_[0:3] be connected to GND by LCD cable, these GPIO will issue +V3.3(default output high) short to GND during system power on. Add R=2.2K to prevent this kind of situation. Page 15. 22. Measurement team Problem: VGA EA fail below items 1,V-SYNC:under shoot over 30% of high level voltage range. 2,H-SYNC:over shoot over 30% of high level voltage range, under shoot over 30% of high level voltage range. Change Change C304, C305 from 5pF to 33pF. Page 13. 23. EMI request use Choke on USB & 1394 ports. Delete option R, don't co-layout. Page 22,34. 24. EMI request : Add C531,C532,C533,C535. Delete C147,C433. Change C110,C163 connection. Change C410 location. Change C378,C379,C410,C163,C110 to 0.1uF/10V. Change C471,C468 to 0.1uF/25V. Change C45,C33,C28,C134,C332,C399,C341 to 0.1uF/10V and don't load. Change C40 to 0.1uF/10V. Change C249 to 0.1uF/25V and don't load.Page 10,46. Change R104 from 0 ohm to bead. Page 31. 25. Change C26,C98,C104,C325(page3), C362(page7), C324,C329(page9), C436(page14), C190,C441(page16), C366,C367(page19), C247(page21), C467,C473,C478(page22), C236(page23), C209,C210,C211,C242(page40), from 0.01uF/25V to 0.01uF/10V. Use 10V is OK. 26. Measurement team Problem: VGA EA fail in rise time and fall time of RGB signal at resolution 1024X768 at 60Hz. Change L6,L7,L8 from 750hm/100MHZ to 700hm/100MHZ. Page 13. 27. Load FAN on/off component : /FAN_SPD. page 35. 28. Change L53,L54 from 09-012400000 to 09-012400001 for cost down. page38. 29. CON1,CON7,CON12,CON15 and J4 change to formal P/N. page 12,24,25,36,44. A3L. For A3L platform : change U32 to 852GM, R148. page 6,7,8,9,40.
R2.1 Pink Block	04/05/14	1. For ESD test fail at switch, If we want to use ESD protect diode, we can't connect switch pin 1&2, pin3&4 to make sure the energy will go through ESD diode : SW1-5. page36. 2. Forget pull high at D54.3. Add R392 pull high to +V3.3S. page 31. 3. For cost down. Delete R=0 OHM. R389,R331,R124,R298,R285,R281,R276(no load),R290(no load) page 19,22,30,31 4. QT report that a "pop" noise occurs when booting. This is because the timing of OP_SD# to control audio AMP ON. Change D49 from DAP2020K to 1N4148W-A2 to control the AMP shutdown only the JACK_IN#, and control SE/BTL# by D54.3. page 31. 5. In audio DJ mode, DJ_LED turns on Q91 and PWR_LED_UP will connect to GND which may damage PIC. Use RN80A to prevent it. page 36. 6. Power RD modification: Delete 0 Ohm: R135,R136,R137 Delete U24, change Q34 to 3904 and add R393,R394. Change R202,R356,R357 BOM to modify BAT CV tolerance to more accurate. Delet Q5,Q1,C18,R9,R10,RN2 and add R395. page 40,43,45. 7. Swap RN80 for smoother layout. page 36. 8. QT bug: when booting or being idle, two A3 with USB CCD module will sometimes appear "Hi-speed device plug into low-speed hub" in Windows XP/2000. Adjust USBRBIAS and USBRBIAS# external resistor R138 from 18.2ohm to 22.6ohm. page 15. 9. For TPE_ENG Power RD's request to unify OTP_RESET#, FORCE_OFF#_SW and FORCE_OFF# into single name: FORCE_OFF#. page 37,44.

Rev	Date	Description
R2.1 Pink Block	04/05/18	10. About 2019 item, factory don't need it now. Delete R391. page 44. 11. C117 don't need use 25V, change to 4.7uF/10V. page 9. 12. Factory found that there are two A3 systems will fail at On Off test. Net " PM DPRSLPVR" crosstalk with net " AC_BAT_SYS". Add a 20pF at R106.2 or change R106 from 1K to 0 OHM can solve this issue. Change R106 to 0 OHM. Page 38. 13. Power request. Don't need use 1K ohm, change R100,R292,R329,R168 from 1K to 0 ohm. Page 38,42. 14. Fine tune E-mail LED (R140 : from 220 to 1K)& Wireless LED (R312 : from 1K to 680) for customer's request. Page 36.
R2.2	04/06/01	1. For Vendor request : Pin footprint diameter is 1.0mm+/-0.05, but ASUS rule is diameter*diameter =(L*L+W*W). Modify Battery Connector J1 as vendor spec. Page 44.