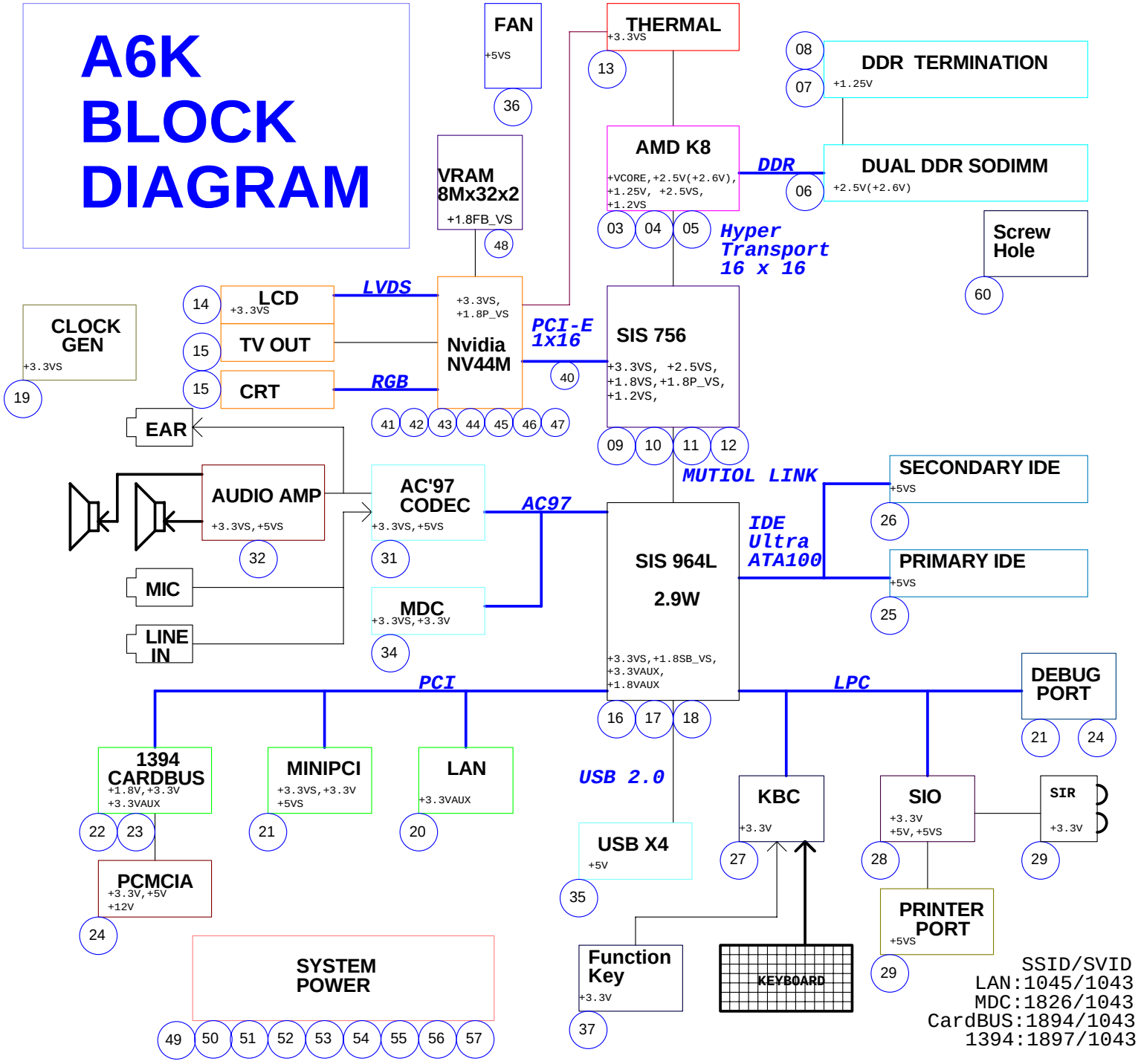
A6K BLOCK DIAGRAM



FILE LIST 01

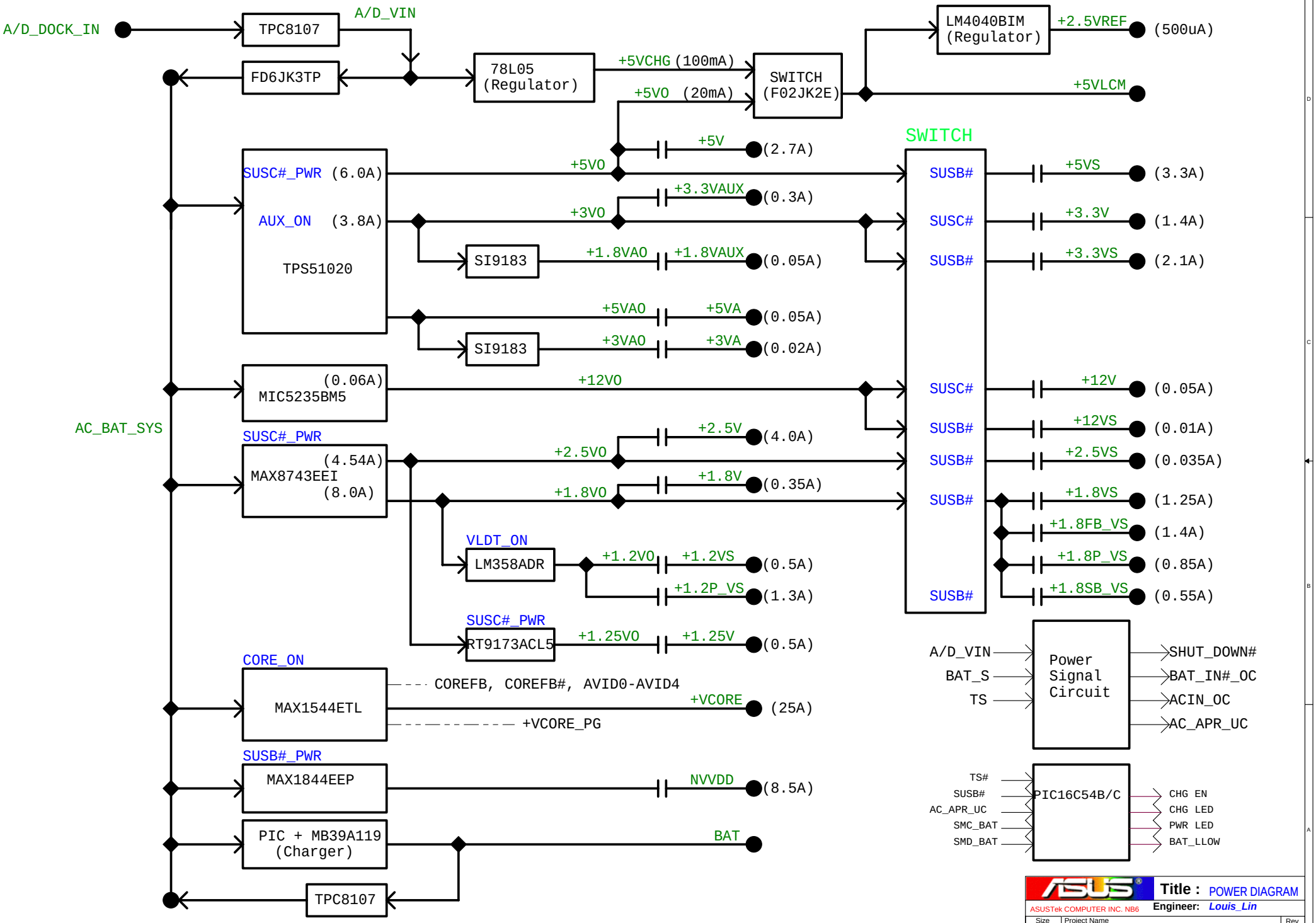
ASUSTek COMPUTER INC. NB6

Title : BLOCK DIAGRAM

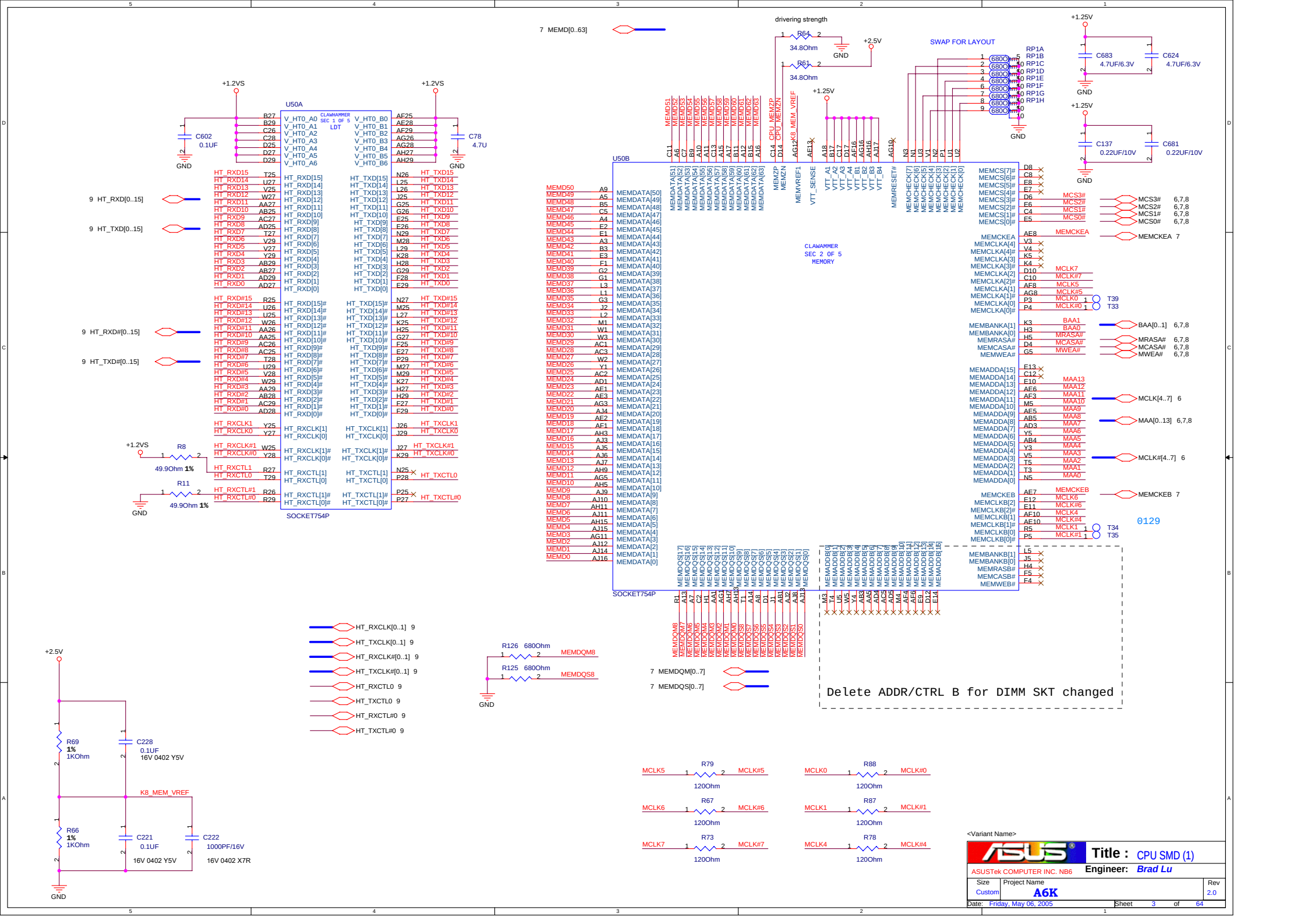
Engineer: Brad Lu

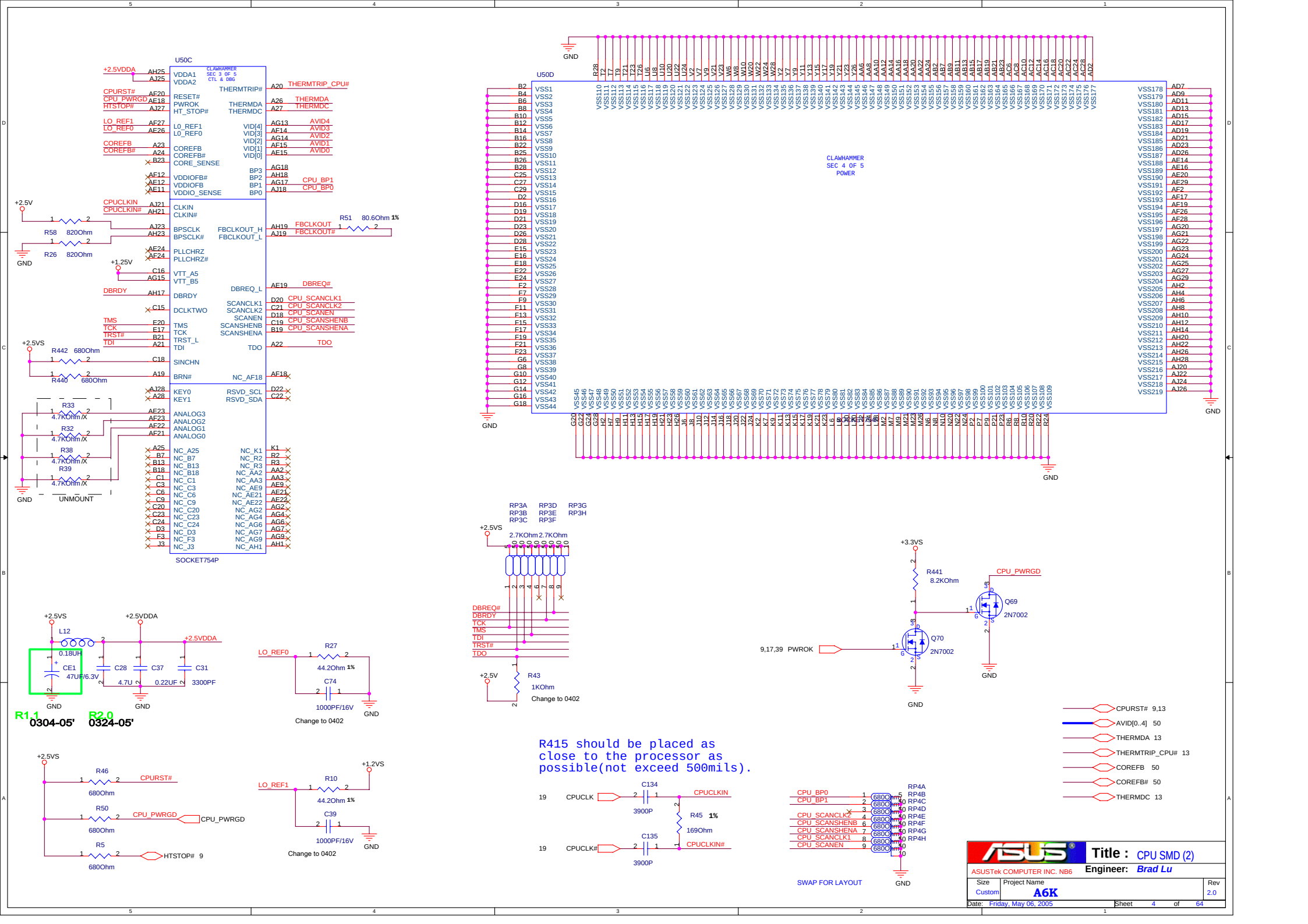
Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 1 of 64



Title : POWER DIAGRAM		
ASUSTek COMPUTER INC. NB6	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 2 of 64	

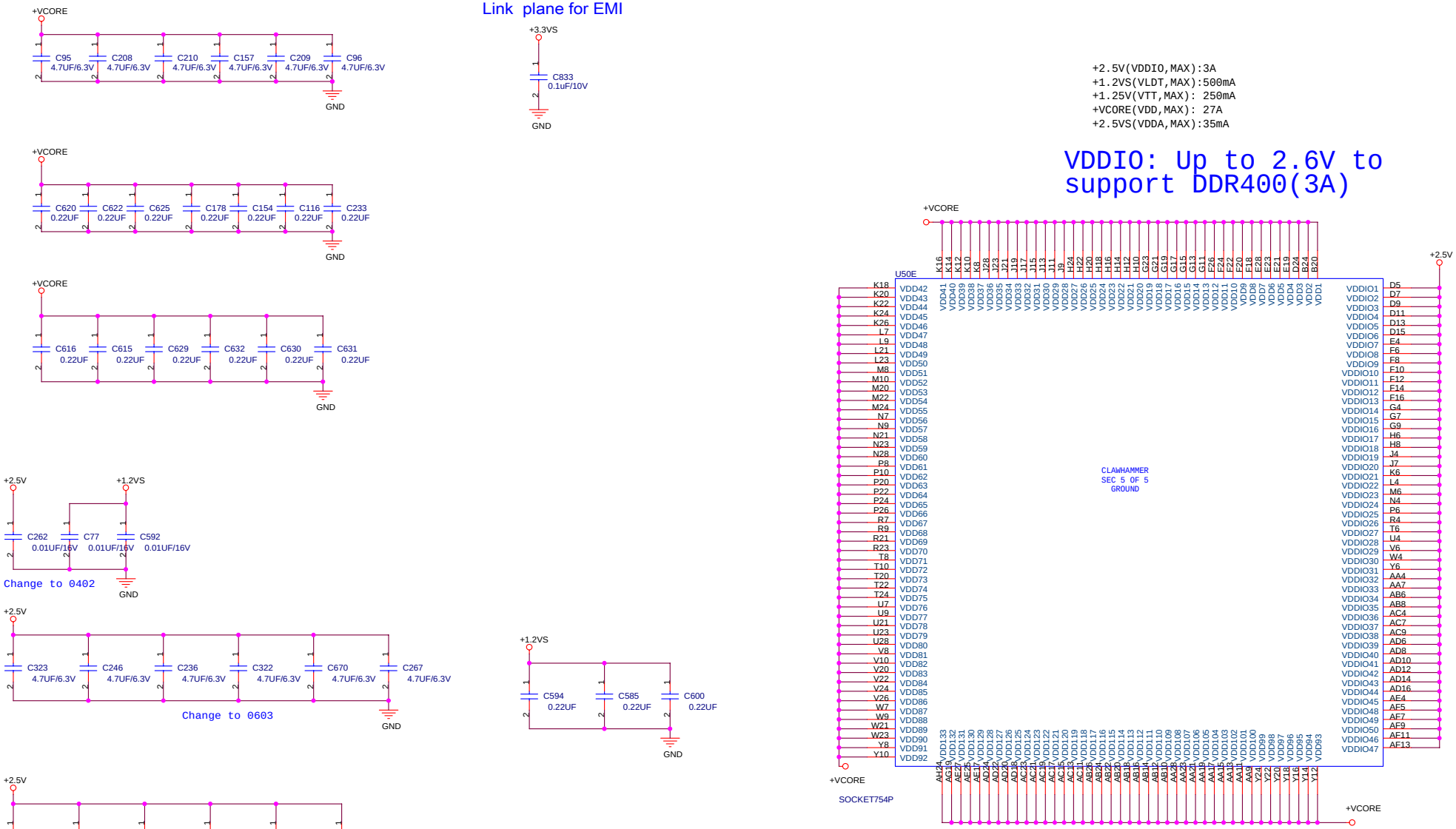

U50A
CLAWHAMMER
SEC 1 OF 5
LDT
SOCKET754P
U50B
CLAWHAMMER
SEC 2 OF 5
MEMORY
SOCKET754P
SWAP FOR LAYOUT
drivering strength
Delete ADDR/CTRL B for DIMM SKT changed
0129
+1.2VS
+2.5V
+1.25V
GND
C602 0.1UF
C78 4.7U
C683 4.7UF/6.3V
C624 4.7UF/6.3V
C137 0.22UF/10V
C681 0.22UF/10V
R64 34.8Ohm
R61 34.8Ohm
R8 49.9Ohm 1%
R11 49.9Ohm 1%
R69 1% 1KOhm
C228 0.1UF 16V 0402 Y5V
R66 1% 1KOhm
C221 0.1UF 16V 0402 Y5V
C222 1000PF/16V 16V 0402 X7R
K8_MEM_VREF
R126 680Ohm
R125 680Ohm
R79 120Ohm
R67 120Ohm
R73 120Ohm
R88 120Ohm
R87 120Ohm
R78 120Ohm
RP1A RP1B RP1C RP1D RP1E RP1F RP1G RP1H
680Ohm
9 HT_RXD[0..15]
9 HT_TXD[0..15]
9 HT_RXD#[0..15]
9 HT_TXD#[0..15]
HT_RXCLK[0..1] 9
HT_TXCLK[0..1] 9
HT_RXCLK#[0..1] 9
HT_TXCLK#[0..1] 9
HT_RXCTL0 9
HT_TXCTL0 9
HT_RXCTL#0 9
HT_TXCTL#0 9
7 MEMD[0..63]
7 MEMDQM[0..7]
7 MEMDQS[0..7]
MCS3# 6,7,8
MCS2# 6,7,8
MCS1# 6,7,8
MCS0# 6,7,8
MEMCKEA 7
BAA[0..1] 6,7,8
MRASA# 6,7,8
MCASA# 6,7,8
MWEA# 6,7,8
MCLK[4..7] 6
MAA[0..13] 6,7,8
MCLK#[4..7] 6
MEMCKEB 7
T39
T33
T34
T35
<Variant Name>
Title : CPU SMD (1)
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 3 of 64


U50C
CLAWHAMMER
SEC 3 OF 5
CTL & DBG
SOCKET754P
U50D
CLAWHAMMER
SEC 4 OF 5
POWER
UNMOUNT
R1.1
0304-05'
R2.0
0324-05'
Change to 0402
Change to 0402
R415 should be placed as close to the processor as possible(not exceed 500mils).
SWAP FOR LAYOUT
Title : CPU SMD (2)
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size
Custom
Project Name
A6K
Rev
2.0
Date: Friday, May 06, 2005
Sheet 4 of 64

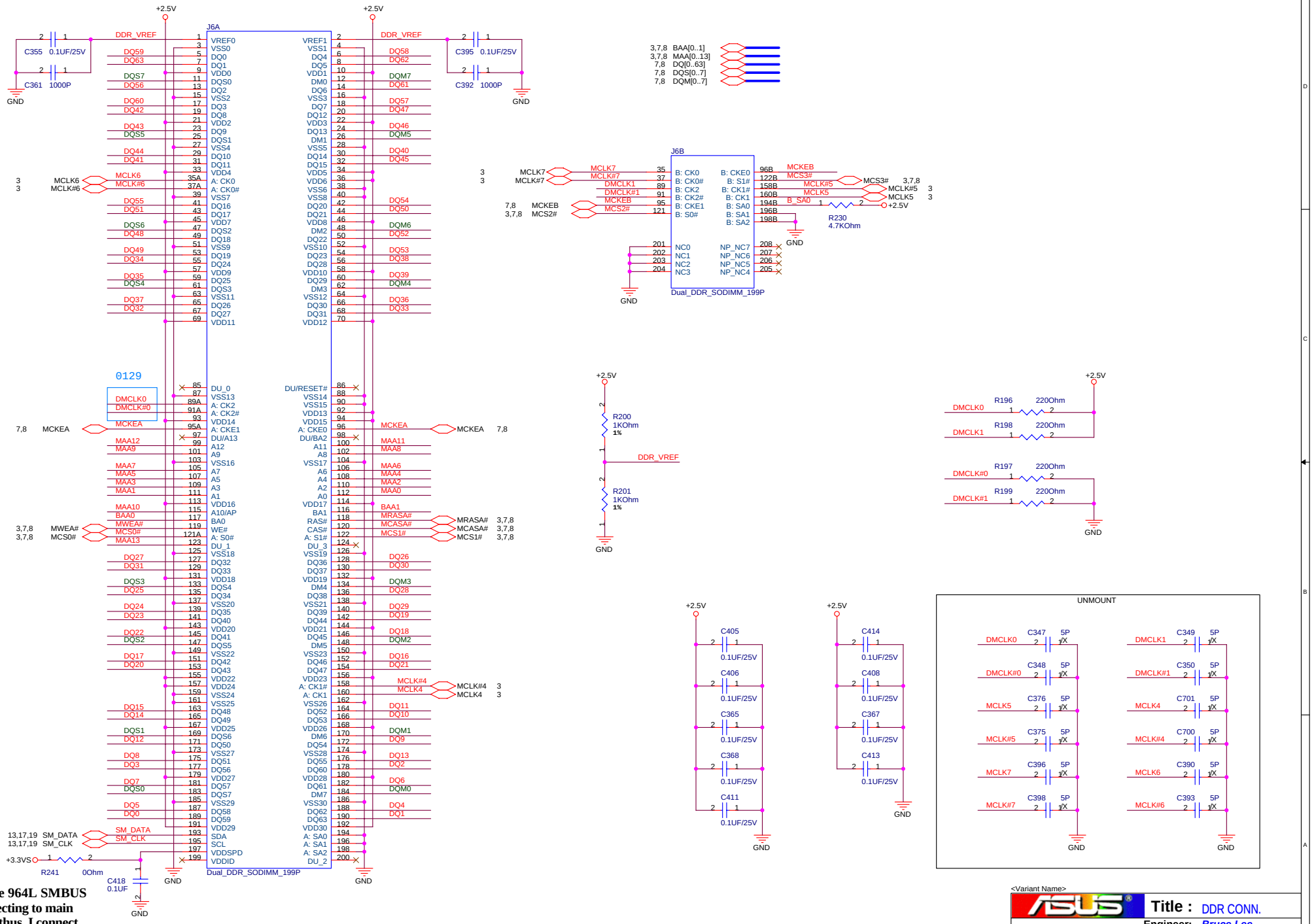
Link plane for EMI

+2.5V(VDDIO,MAX):3A
+1.2VS(VLDT,MAX):500mA
+1.25V(VTT,MAX): 250mA
+VCORE(VDD,MAX): 27A
+2.5VS(VDDA,MAX):35mA

VDDIO: Up to 2.6V to support DDR400(3A)



ASUSTek COMPUTER INC. NB6	Title : CPU (3)		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005	Sheet 5 of 64		



Because 964L SMBUS is connecting to main power, thus, I connect VDDSPD to +V3.3S

<Variant Name>

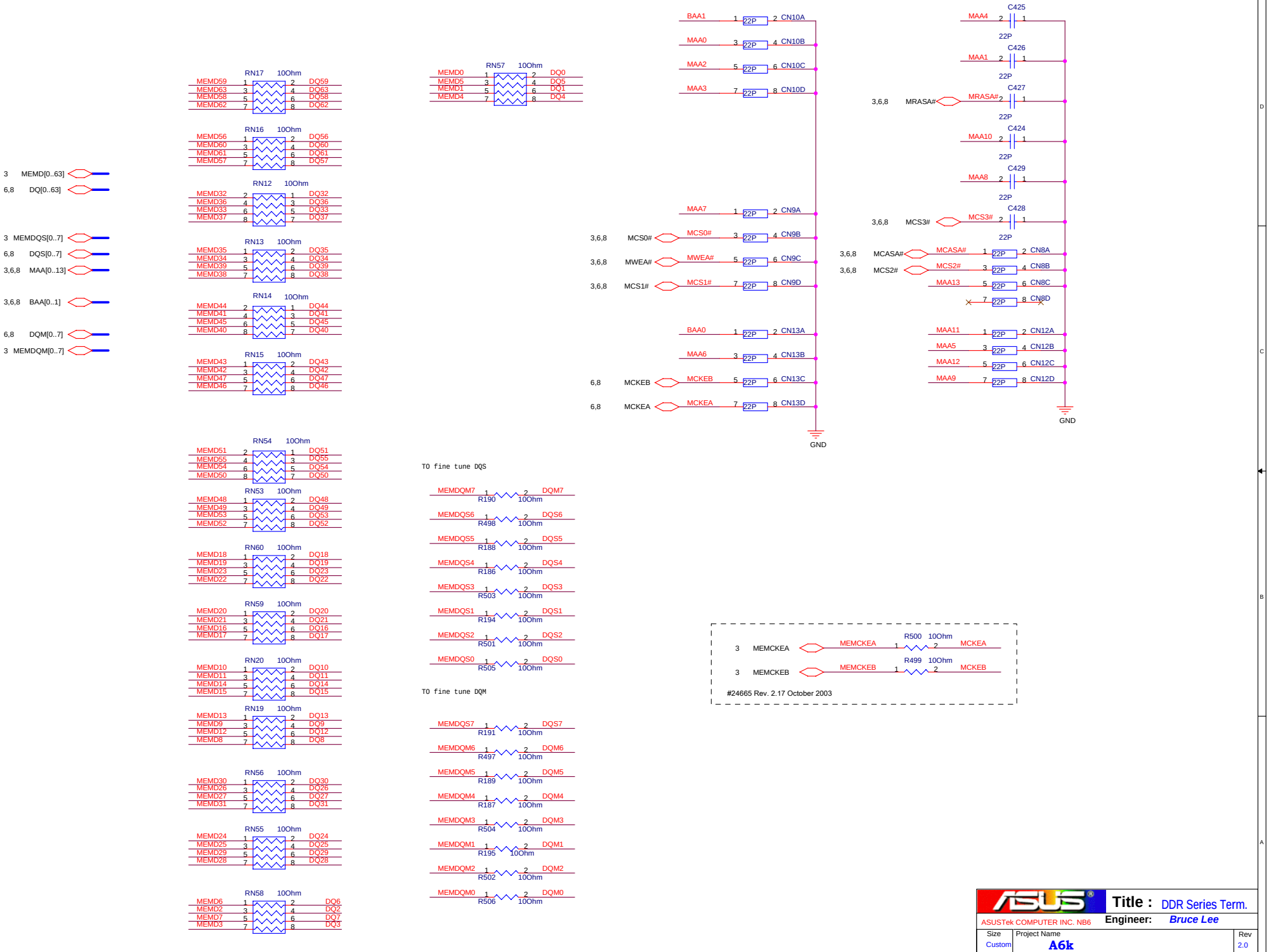
ASUSTek COMPUTER INC. NB6

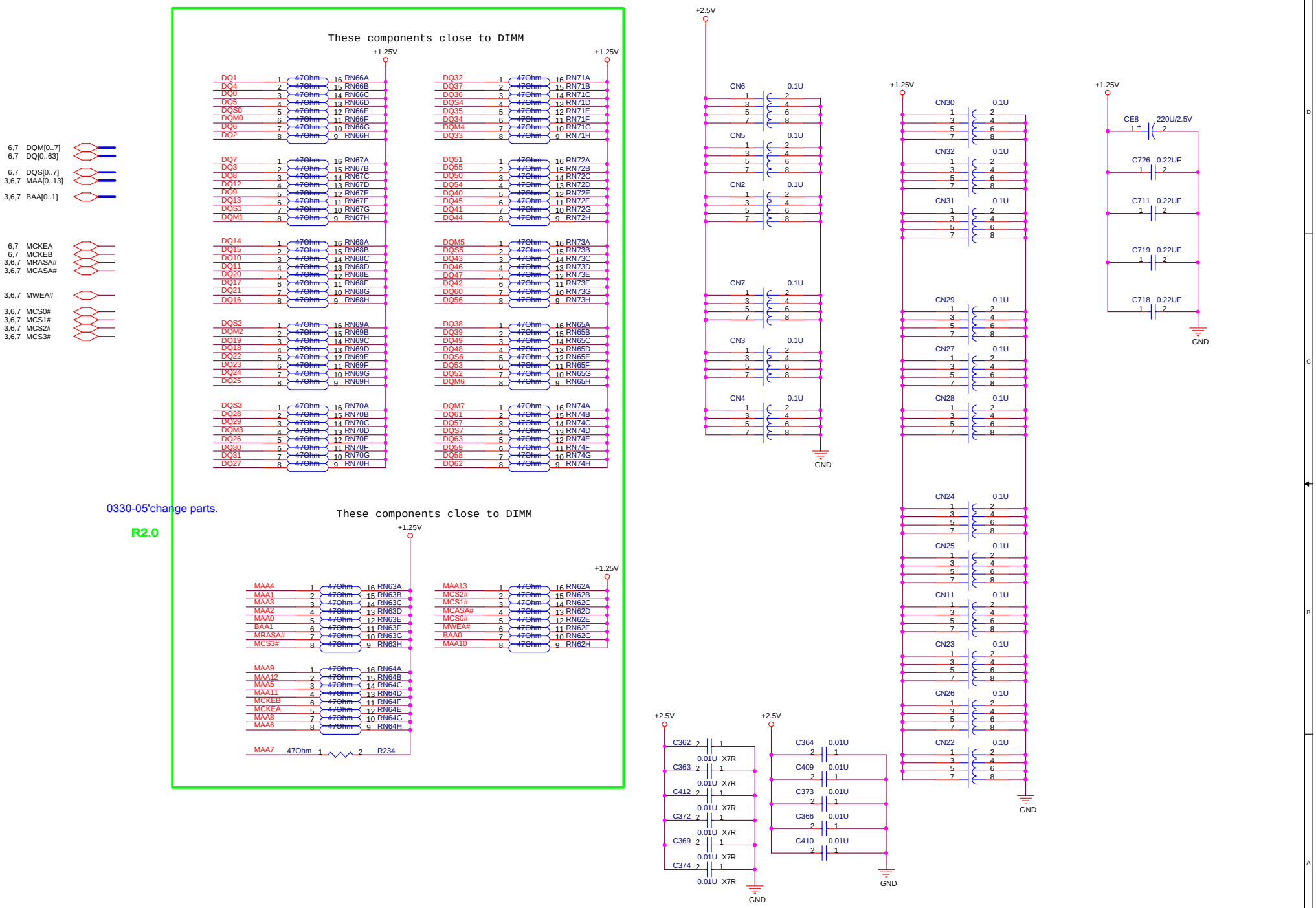
Title : DDR CONN.

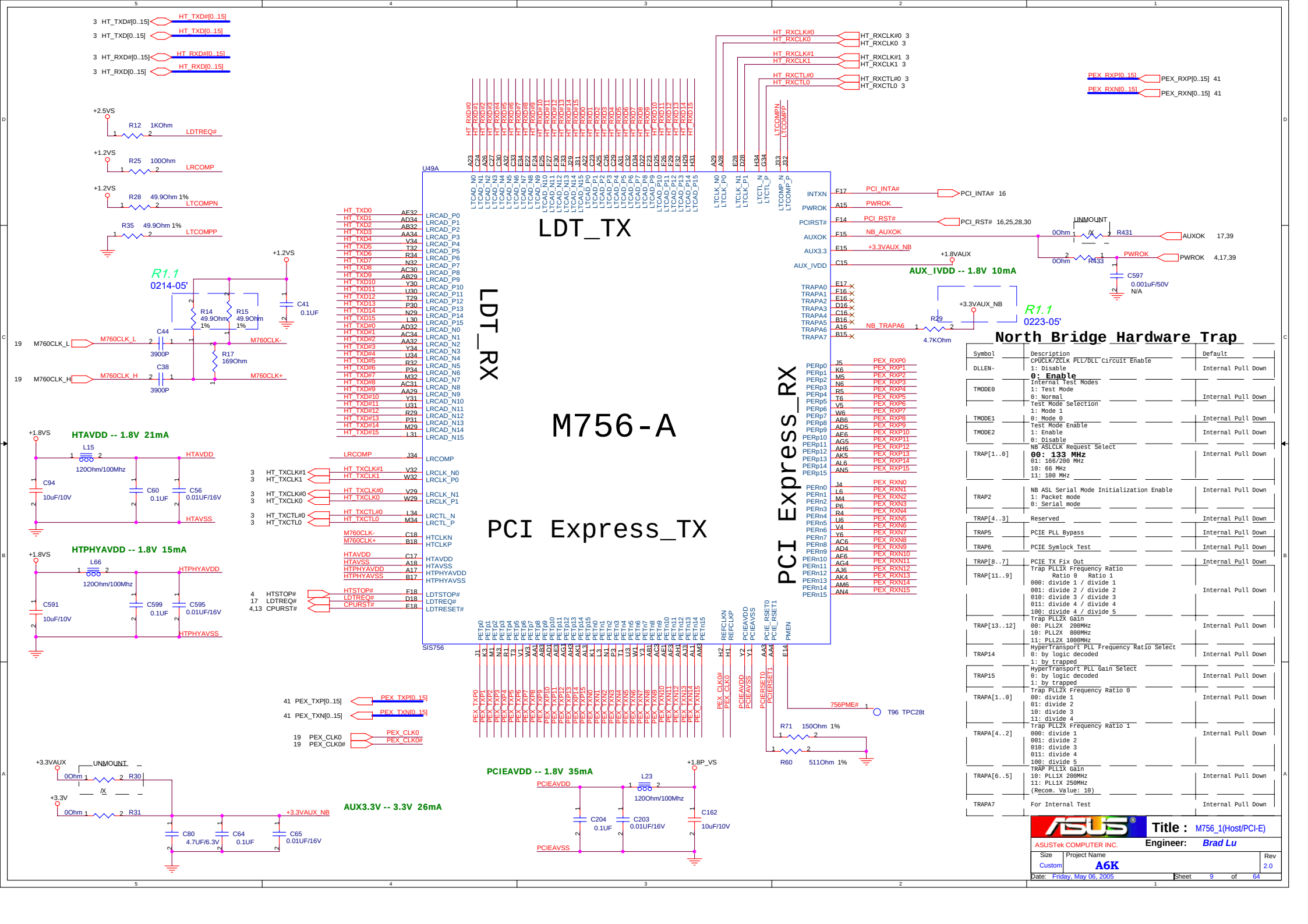
Engineer: Bruce Lee

Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 6 of 64


3 MEMD[0..63]
6,8 DQ[0..63]
3 MEMDQS[0..7]
6,8 DQS[0..7]
3,6,8 MAA[0..13]
3,6,8 BAA[0..1]
6,8 DQM[0..7]
3 MEMDQM[0..7]
RN17 10Ohm
MEMD59 MEMD63 MEMD58 MEMD62 DQ59 DQ63 DQ58 DQ62
RN16 10Ohm
MEMD56 MEMD60 MEMD61 MEMD57 DQ56 DQ60 DQ61 DQ57
RN12 10Ohm
MEMD32 MEMD36 MEMD33 MEMD37 DQ32 DQ36 DQ33 DQ37
RN13 10Ohm
MEMD35 MEMD34 MEMD39 MEMD38 DQ35 DQ34 DQ39 DQ38
RN14 10Ohm
MEMD44 MEMD41 MEMD45 MEMD40 DQ44 DQ41 DQ45 DQ40
RN15 10Ohm
MEMD43 MEMD42 MEMD47 MEMD46 DQ43 DQ42 DQ47 DQ46
RN54 10Ohm
MEMD51 MEMD55 MEMD54 MEMD50 DQ51 DQ55 DQ54 DQ50
RN53 10Ohm
MEMD48 MEMD49 MEMD53 MEMD52 DQ48 DQ49 DQ53 DQ52
RN60 10Ohm
MEMD18 MEMD19 MEMD23 MEMD22 DQ18 DQ19 DQ23 DQ22
RN59 10Ohm
MEMD20 MEMD21 MEMD16 MEMD17 DQ20 DQ21 DQ16 DQ17
RN20 10Ohm
MEMD10 MEMD11 MEMD14 MEMD15 DQ10 DQ11 DQ14 DQ15
RN19 10Ohm
MEMD13 MEMD9 MEMD12 MEMD8 DQ13 DQ9 DQ12 DQ8
RN56 10Ohm
MEMD30 MEMD26 MEMD27 MEMD31 DQ30 DQ26 DQ27 DQ31
RN55 10Ohm
MEMD24 MEMD25 MEMD29 MEMD28 DQ24 DQ25 DQ29 DQ28
RN58 10Ohm
MEMD6 MEMD2 MEMD7 MEMD3 DQ6 DQ2 DQ7 DQ3
RN57 10Ohm
MEMD0 MEMD5 MEMD1 MEMD4 DQ0 DQ5 DQ1 DQ4
TO fine tune DQS
MEMDQM7 R190 10Ohm DQM7
MEMDQS6 R498 10Ohm DQS6
MEMDQS5 R188 10Ohm DQS5
MEMDQS4 R186 10Ohm DQS4
MEMDQS3 R503 10Ohm DQS3
MEMDQS1 R194 10Ohm DQS1
MEMDQS2 R501 10Ohm DQS2
MEMDQS0 R505 10Ohm DQS0
TO fine tune DQM
MEMDQS7 R191 10Ohm DQS7
MEMDQM6 R497 10Ohm DQM6
MEMDQM5 R189 10Ohm DQM5
MEMDQM4 R187 10Ohm DQM4
MEMDQM3 R504 10Ohm DQM3
MEMDQM1 R195 10Ohm DQM1
MEMDQM2 R502 10Ohm DQM2
MEMDQM0 R506 10Ohm DQM0
BAA1 MAA0 MAA2 MAA3 22P CN10A CN10B CN10C CN10D
MAA7 MCS0# MWEA# MCS1# 22P CN9A CN9B CN9C CN9D
3,6,8 MCS0#
3,6,8 MWEA#
3,6,8 MCS1#
BAA0 MAA6 MCKEB MCKEA 22P CN13A CN13B CN13C CN13D
6,8 MCKEB
6,8 MCKEA
GND
C425 C426 C427 C424 C429 C428 22P
MAA4 MAA1 MRASA# MAA10 MAA8 MCS3#
3,6,8 MRASA#
3,6,8 MCS3#
MCASA# MCS2# MAA13 22P CN8A CN8B CN8C CN8D
3,6,8 MCASA#
3,6,8 MCS2#
MAA11 MAA5 MAA12 MAA9 22P CN12A CN12B CN12C CN12D
GND
3 MEMCKEA MEMCKEA R500 10Ohm MCKEA
3 MEMCKEB MEMCKEB R499 10Ohm MCKEB
#24665 Rev. 2.17 October 2003
Title : DDR Series Term.
ASUSTek COMPUTER INC. NB6
Engineer: Bruce Lee
Size Custom
Project Name A6k
Rev 2.0
Date: Friday, May 06, 2005
Sheet 7 of 64


These components close to DIMM
+1.25V
DQ1 DQ4 DQ0 DQ5 DQS0 DQM0 DQ6 DQ2 RN66A RN66B RN66C RN66D RN66E RN66F RN66G RN66H
DQ7 DQ3 DQ8 DQ12 DQ9 DQ13 DQS1 DQM1 RN67A RN67B RN67C RN67D RN67E RN67F RN67G RN67H
DQ14 DQ15 DQ10 DQ11 DQ20 DQ17 DQ21 DQ16 RN68A RN68B RN68C RN68D RN68E RN68F RN68G RN68H
DQS2 DQM2 DQ19 DQ18 DQ22 DQ23 DQ24 DQ25 RN69A RN69B RN69C RN69D RN69E RN69F RN69G RN69H
DQS3 DQ28 DQ29 DQM3 DQ26 DQ30 DQ31 DQ27 RN70A RN70B RN70C RN70D RN70E RN70F RN70G RN70H
DQ32 DQ37 DQ36 DQS4 DQ35 DQ34 DQM4 DQ33 RN71A RN71B RN71C RN71D RN71E RN71F RN71G RN71H
DQ51 DQ55 DQ50 DQ54 DQ40 DQ45 DQ41 DQ44 RN72A RN72B RN72C RN72D RN72E RN72F RN72G RN72H
DQM5 DQS5 DQ43 DQ46 DQ47 DQ42 DQ60 DQ56 RN73A RN73B RN73C RN73D RN73E RN73F RN73G RN73H
DQ38 DQ39 DQ49 DQ48 DQS6 DQ53 DQS2 DQM6 RN65A RN65B RN65C RN65D RN65E RN65F RN65G RN65H
DQM7 DQ61 DQ57 DQS7 DQ63 DQ59 DQ58 DQ62 RN74A RN74B RN74C RN74D RN74E RN74F RN74G RN74H
47Ohm
6,7 DQM[0..7]
6,7 DQ[0..63]
6,7 DQS[0..7]
3,6,7 MAA[0..13]
3,6,7 BAA[0..1]
6,7 MCKEA
6,7 MCKEB
3,6,7 MRASA#
3,6,7 MCASA#
3,6,7 MWEA#
3,6,7 MCS0#
3,6,7 MCS1#
3,6,7 MCS2#
3,6,7 MCS3#
0330-05'change parts.
R2.0
These components close to DIMM
+1.25V
MAA4 MAA1 MAA3 MAA2 MAA0 BAA1 MRASA# MCS3# RN63A RN63B RN63C RN63D RN63E RN63F RN63G RN63H
MAA13 MCS2# MCS1# MCASA# MCS3# MWEA# BAA0 MAA10 RN62A RN62B RN62C RN62D RN62E RN62F RN62G RN62H
MAA9 MAA12 MAA5 MAA11 MCKEB MCKEA MAA8 MAA6 RN64A RN64B RN64C RN64D RN64F RN64E RN64G RN64H
MAA7 47Ohm R234
+2.5V
CN6 CN5 CN2 CN7 CN3 CN4 0.1U
GND
+1.25V
CN30 CN32 CN31 CN29 CN27 CN28 CN24 CN25 CN11 CN23 CN26 CN22 0.1U
GND
CE8 220U/2.5V
C726 C711 C719 C718 0.22UF
GND
+2.5V
C362 C363 C412 C372 C369 C374 0.01U X7R
GND
+2.5V
C364 C409 C373 C366 C410 0.01U
GND
ASUSTek COMPUTER INC. NB6
Title : DDR VTT Term.
Engineer: Bruce Lee
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 8 of 64



North Bridge Hardware Trap

Symbol	Description	Default
DLLEN-	CPUCLK/ZCLK PLL/DLL Circuit Enable 1: Disable **0: Enable**	Internal Pull Down
TMODE0	Internal Test Modes 1: Test Mode 0: Normal	Internal Pull Down
TMODE1	Test Mode Selection 1: Mode 1 0: Mode 0	Internal Pull Down
TMODE2	Test Mode Enable 1: Enable 0: Disable	Internal Pull Down
TRAP[1..0]	NB ASLCLK Request Select **00: 133 MHz** 01: 166/200 MHz 10: 66 MHz 11: 100 MHz	Internal Pull Down
TRAP2	NB ASL Serial Mode Initialization Enable 1: Packet mode 0: Serial mode	Internal Pull Down
TRAP[4..3]	Reserved	Internal Pull Down
TRAP5	PCIE PLL Bypass	Internal Pull Down
TRAP6	PCIE Symlock Test	Internal Pull Down
TRAP[8..7]	PCIE TX Fix Out	Internal Pull Down
TRAP[11..9]	Trap PLL1X Frequency Ratio Ratio 0 Ratio 1 000: divide 1 / divide 1 001: divide 2 / divide 2 010: divide 3 / divide 3 011: divide 4 / divide 4 100: divide 4 / divide 5	Internal Pull Down
TRAP[13..12]	Trap PLL2X Gain 00: PLL2X 200MHz 10: PLL2X 800MHz 11: PLL2X 1000MHz	Internal Pull Down
TRAP14	HyperTransport PLL Frequency Ratio Select 0: by logic decoded 1: by trapped	Internal Pull Down
TRAP15	HyperTransport PLL Gain Select 0: by logic decoded 1: by trapped	Internal Pull Down
TRAPA[1..0]	Trap PLL2X Frequency Ratio 0 00: divide 1 01: divide 2 10: divide 3 11: divide 4	Internal Pull Down
TRAPA[4..2]	Trap PLL2X Frequency Ratio 1 000: divide 1 001: divide 2 010: divide 3 011: divide 4 100: divide 5	Internal Pull Down
TRAPA[6..5]	TRAP PLL1X Gain 10: PLL1X 200MHz 11: PLL1X 250MHz (Recom. Value: 10)	Internal Pull Down
TRAPA7	For Internal Test	Internal Pull Down

ASUSTek COMPUTER INC.

Title : M756_1(Host/PCI-E)

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 9 of 64

The differences between the traces of MuTIOL Strobes and Data in each group should be smaller than 0.05",and strobes need guide GND trace

U49B

M756-2

MuTIOL

Trap

0105-05'

19 CLK_ZIP_NB — CLK_ZIP_NB — AM16 ZCLK

16 ZUREQ — ZUREQ — AL24 ZUREQ
16 ZDREQ — ZDREQ — AP23 ZDREQ

16 ZSTB0# — ZSTB0# — AL20 ZSTB0#
16 ZSTB0 — ZSTB0 — AM20 ZSTB0

16 ZSTB1# — ZSTB1# — AN19 ZSTB1#
16 ZSTB1 — ZSTB1 — AP19 ZSTB1

16 ZAD[0..16] — ZAD[0..16]

The differences between the traces of MuTIOL Strobes and Data should be smaller than 0.05"

ZAD2	AJ23	ZAD2	
ZAD0	AK23	ZAD0	
ZAD5	AJ21	ZAD5	
ZAD3	AK21	ZAD3	
ZAD10	AJ19	ZAD10	
ZAD8	AK19	ZAD8	
ZAD13	AJ17	ZAD13	
ZAD11	AK17	ZAD11	
ZAD4	AL22	ZAD4	
ZAD1	AM22	ZAD1	
ZAD7	AN21	ZAD7	
ZAD6	AP21	ZAD6	
ZAD12	AL18	ZAD12	
ZAD9	AM18	ZAD9	
ZAD15	AN17	ZAD15	
ZAD14	AP17	ZAD14	
ZAD16	AN23	ZAD16	

ZVREF — AP24 — ZVREF

ZCMP_N — AN24 — ZCMP_N
ZCMP_P — AM24 — ZCMP_P

Z1XAVDD — AK16 — Z1XAVDD
Z1XAVSS — AL16 — Z1XAVSS

Z4XAVDD — AP16 — Z4XAVDD
Z4XAVSS — AN16 — Z4XAVSS

AP9 VSSP16
AP11 VSSP17
AN11 VSSP18
AP10 VSSP19
AN10 VSSP20

ENTEST — AK31 — ENTEST — R101 1 2 0Ohm

DLLEN# — AK29 — CPUDLLENN — 1 T108 TPC28t

TESTMODE2 AL34
TESTMODE1 AL33
TESTMODE0 AL32

TRAP15 AM33
TRAP14 AM34
TRAP13 AN33
TRAP12 AM32
TRAP11 AN32
TRAP10 AP32
TRAP9 AL31
TRAP8 AM31
TRAP7 AN31
TRAP6 AP31
TRAP5 AK30
TRAP4 AL30
TRAP3 AM30
TRAP2 AN30
TRAP1 AP30
TRAP0 AJ29

DB15 AP27
DB14 AN27
DB13 AM27
DB12 AL27
DB11 AK27
DB10 AJ27
DB9 AP28
DB8 AN28
DB7 AM28
DB6 AL28
DB5 AK28
DB4 AJ28
DB3 AP29
DB2 AN29
DB1 AM29
DB0 AL29

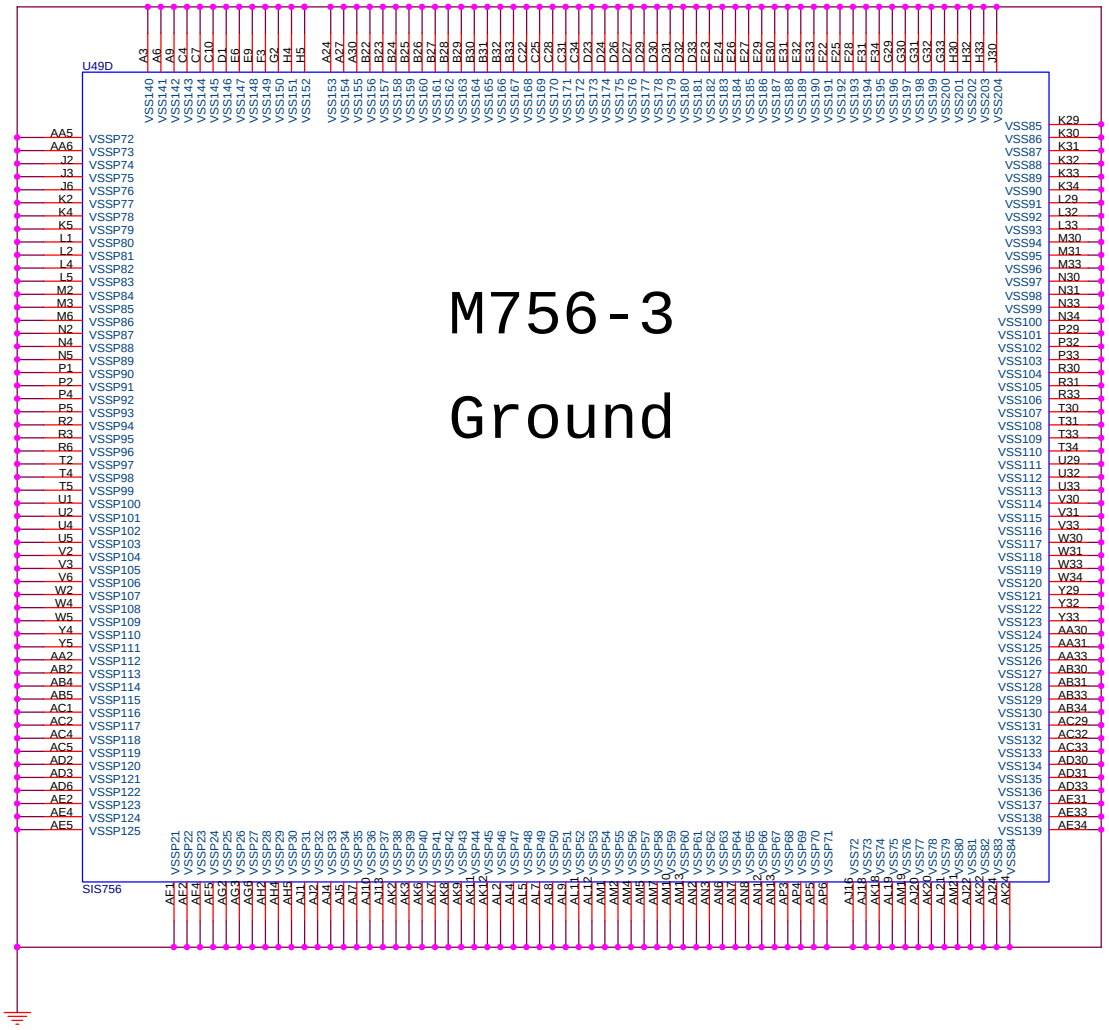
Place near M756 chip.

+1.8VS
R108 56Ohm ZCMP_N
MuTIOL 1.0 Vref=0.5 *VCC1.8
R116 150Ohm 1%
C295 0.1uF/10V
C294 10uF/10V
MuTIOL 2.0 Vref=0.25 *VCC1.8 ZVREF
R123 49.9Ohm 1%
C298 0.1uF/10V
R106 56Ohm ZCMP_P

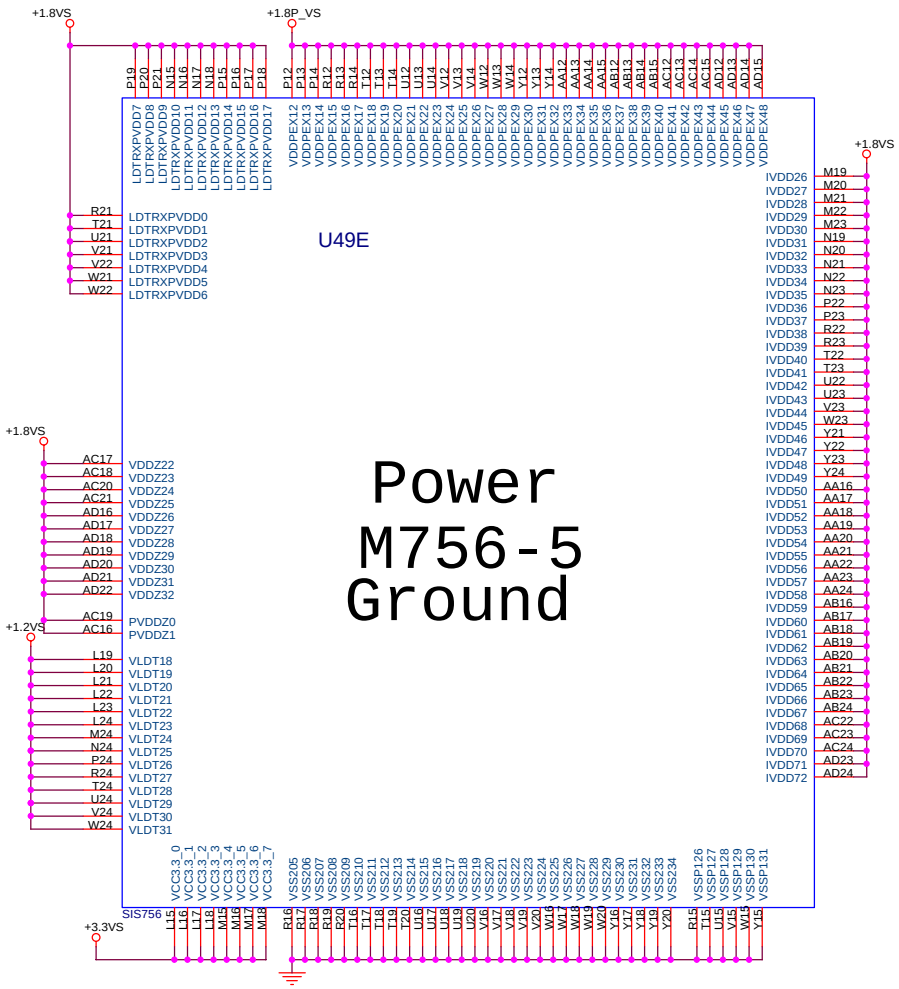
+1.8VS
L29 120Ohm/100Mhz Z1XAVDD
C278 0.1UF
C279 0.01UF/16V Z1XAVSS
Z1XAVDD-- 1.8V 9mA

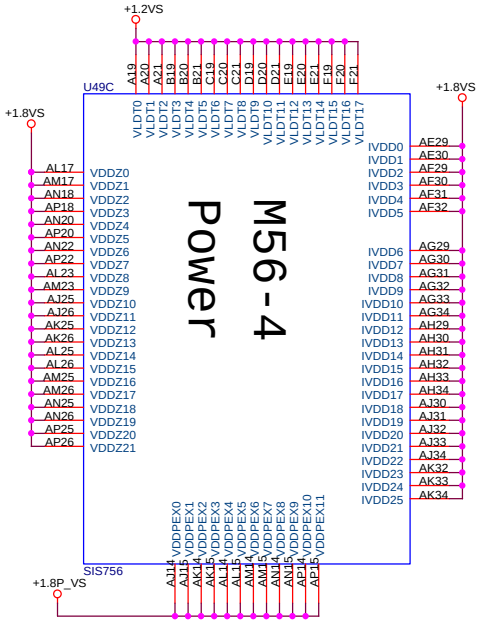
+1.8VS
L34 120Ohm/100Mhz Z4XAVDD
C297 10uF/10V
C291 0.01UF/16V
C292 0.1UF Z4XAVSS
Z4XAVDD-- 1.8V 14mA

ASUSTek COMPUTER INC.	Title : SIS756-2 MuTIOL		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005	Sheet 10 of 64		

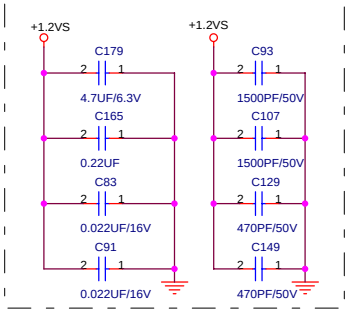


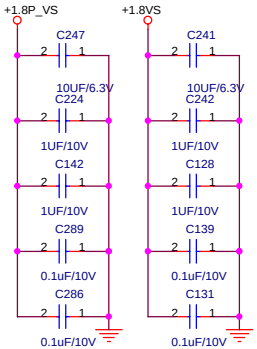
ASUSTek COMPUTER INC.	Title : M756_3		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005	Sheet 11 of 64		

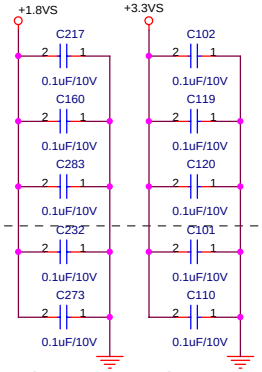




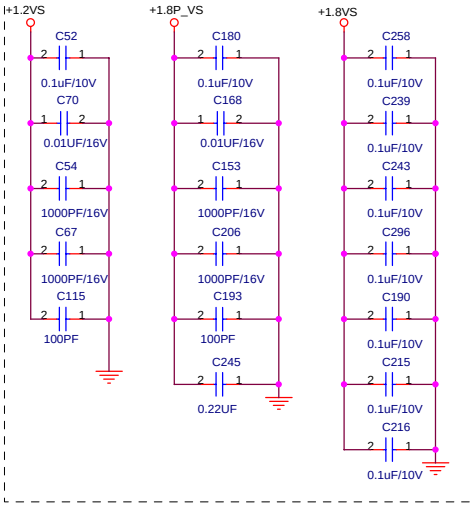
LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.





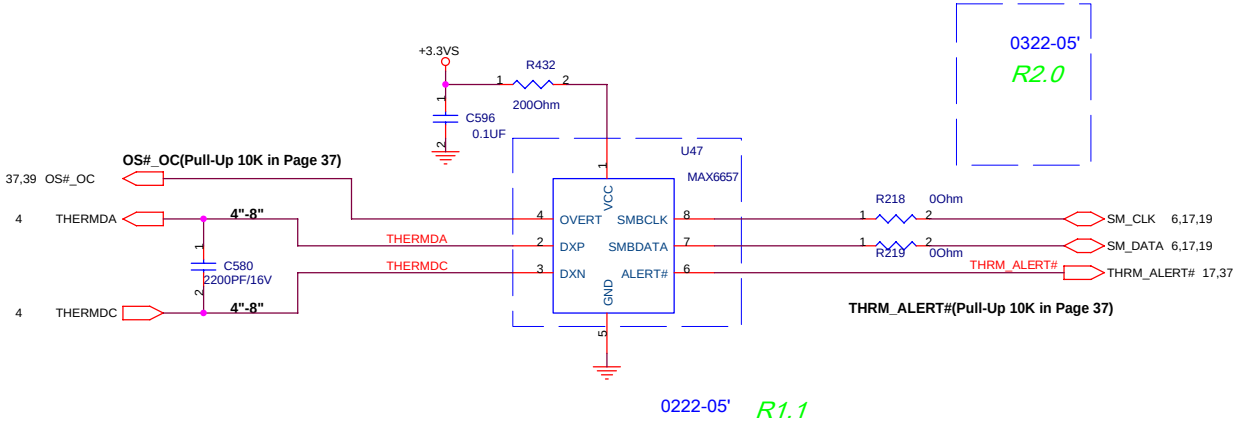


Place these capacitors under NB solder side.

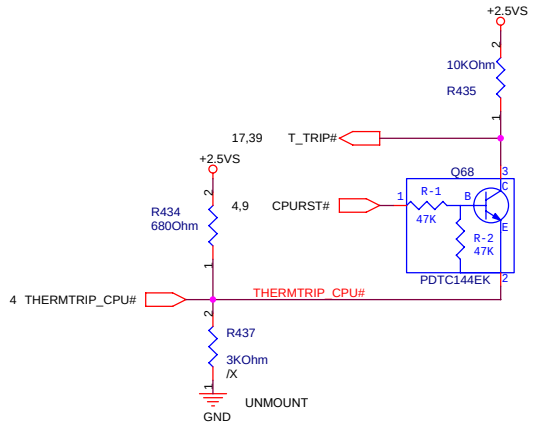


+3.3VS(VCC3, MAX):29mA
+1.8VS(VDDZ, MAX):119mA
+1.8VS(IVDD, MAX):1.783A
+1.8VS(VDDPEX, MAX):1164mA
+1.2VS(VLDT, MAX):153mA

ASUSTek COMPUTER INC.	Title : M756_4(POWER)	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 12 of 64	



0222-05' *R1.1*



THERMAL

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSTek COMPUTER INC. NB6	Title : THERMAL	
	Engineer: *Brad Lu*	
Size: A3	Project Name: **A6K**	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 13 of 64	

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output D/A signal (adjust voltage level) to adjust Back light.

A3K used D1 R:1.0 Inverter Board

USB PORT 3 for CAMERA

LCD Power

SI3865: US$0.22

LCD CABLE ID:	PID3	PID2	PID1	PID0
15.1 XGA	1	1	0	1
15.1 SXGA+	1	0	1	1
15.4 WXGA	1	1	1	0
15.4 WSXGA+	0	1	1	1

0114-05' CON1 Changed to "12-17001030A"

R1.1 0225-05' cancel next version

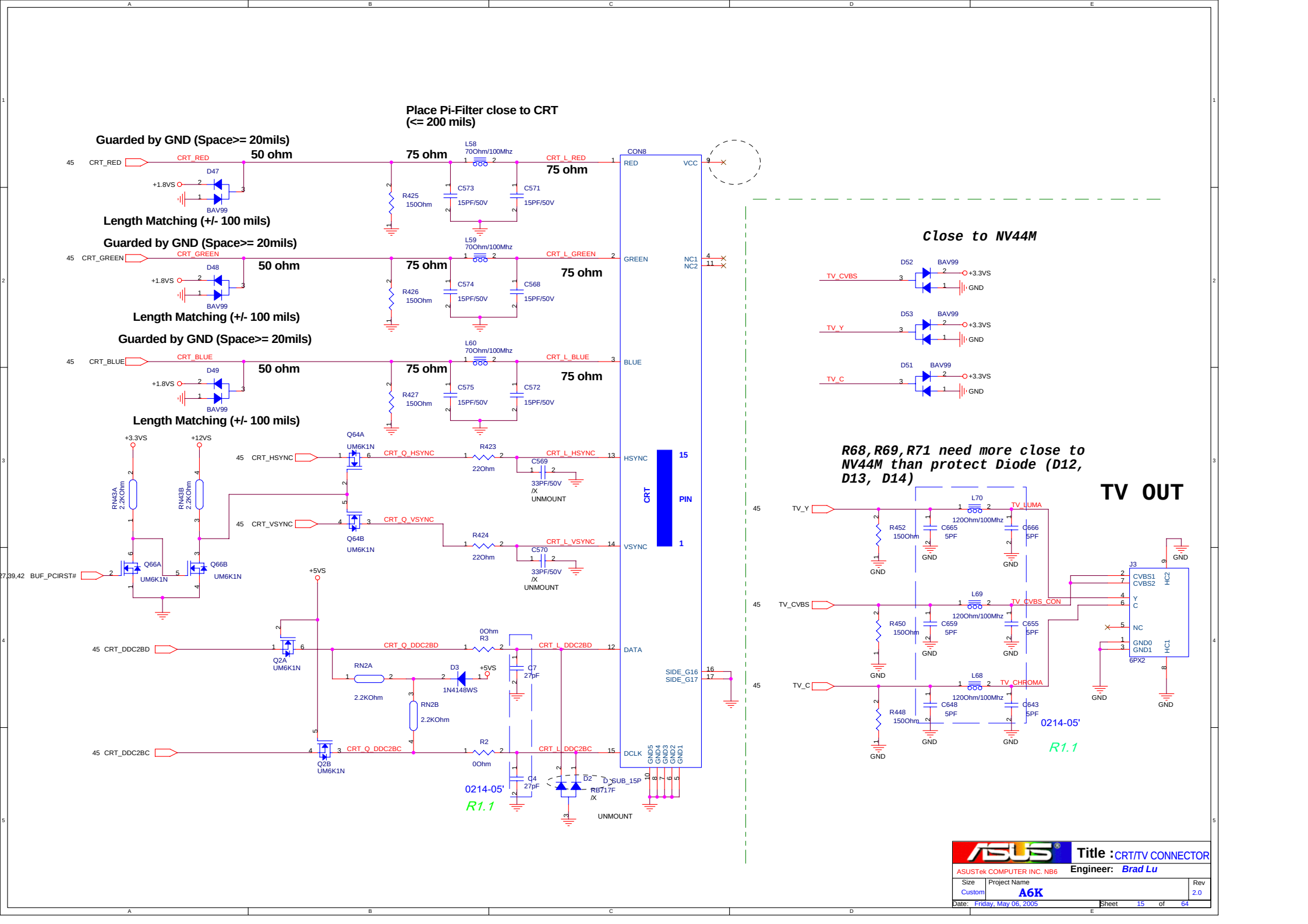
R1.1 0222-05'

R2.0 0324-05'

3-3.6V S0-S1M:410 mA(500 mA Max.)

Caution: Must tune R1404 & C1415 to meet Panel Spec

Title :	LVDS & BACKLIGHT
ASUSTek COMPUTER INC. NB6	Engineer: Brad Lu
Size: Custom	Project Name: A6K
Rev: 2.0	
Date: Friday, May 06, 2005	Sheet 14 of 64


Place Pi-Filter close to CRT
(<= 200 mils)
Guarded by GND (Space>= 20mils)
50 ohm
75 ohm
75 ohm
Length Matching (+/- 100 mils)
Guarded by GND (Space>= 20mils)
50 ohm
75 ohm
75 ohm
Length Matching (+/- 100 mils)
Guarded by GND (Space>= 20mils)
50 ohm
75 ohm
75 ohm
Length Matching (+/- 100 mils)
CRT_RED
CRT_GREEN
CRT_BLUE
D47
D48
D49
BAV99
+1.8VS
L58 70Ohm/100Mhz
L59 70Ohm/100Mhz
L60 70Ohm/100Mhz
R425 150Ohm
R426 150Ohm
R427 150Ohm
C573 15PF/50V
C571 15PF/50V
C574 15PF/50V
C568 15PF/50V
C575 15PF/50V
C572 15PF/50V
CRT_L_RED
CRT_L_GREEN
CRT_L_BLUE
CON8
RED
GREEN
BLUE
VCC
NC1
NC2
CRT
15
PIN
1
+3.3VS
+12VS
RN43A 2.2KOhm
RN43B 2.2KOhm
Q64A UM6K1N
Q64B UM6K1N
Q66A UM6K1N
Q66B UM6K1N
CRT_HSYNC
CRT_VSYNC
CRT_Q_HSYNC
CRT_Q_VSYNC
R423 22Ohm
R424 22Ohm
C569 33PF/50V /X UNMOUNT
C570 33PF/50V /X UNMOUNT
CRT_L_HSYNC
CRT_L_VSYNC
HSYNC
VSYNC
BUF_PCIRST#
+5VS
Q2A UM6K1N
Q2B UM6K1N
CRT_DDC2BD
CRT_DDC2BC
CRT_Q_DDC2BD
CRT_Q_DDC2BC
CRT_L_DDC2BD
CRT_L_DDC2BC
0Ohm R3
R2 0Ohm
RN2A 2.2KOhm
RN2B 2.2KOhm
D3 1N4148WS
C7 27pF
C4 27pF
D2 RB717F /X
D_SUB_15P
UNMOUNT
DATA
DCLK
SIDE_G16
SIDE_G17
GND5
GND4
GND3
GND2
GND1
0214-05'
R1.1
Close to NV44M
D52 BAV99
D53 BAV99
D51 BAV99
TV_CVBS
TV_Y
TV_C
+3.3VS
GND
R68,R69,R71 need more close to NV44M than protect Diode (D12, D13, D14)
TV OUT
L70 120Ohm/100Mhz
L69 120Ohm/100Mhz
L68 120Ohm/100Mhz
R452 150Ohm
R450 150Ohm
R448 150Ohm
C665 5PF
C666 5PF
C659 5PF
C655 5PF
C648 5PF
C643 5PF
TV_LUMA
TV_CVBS_CON
TV_CHROMA
J3
CVBS1
CVBS2
Y
C
NC
GND0
GND1
HC2
HC1
6PX2
0214-05'
R1.1
ASUSTek COMPUTER INC. NB6
Title : CRT/TV CONNECTOR
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 15 of 64

IDSEL	PCI_AD?	INT	PCI_REQ#?
CB&1394	PCI_AD21	INTB#	PCI_REQ#0
MINIPCI	PCI_AD20	INTC#	PCI_REQ#1
LAN	PCI_AD22	INTD#	PCI_REQ#2

U19A

SIS964L

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <=
500 mils

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <=
500 mils

Check!

UNMOUNT

pull up to VccSus3_3
by internal pull-up
resistor

UNMOUNT

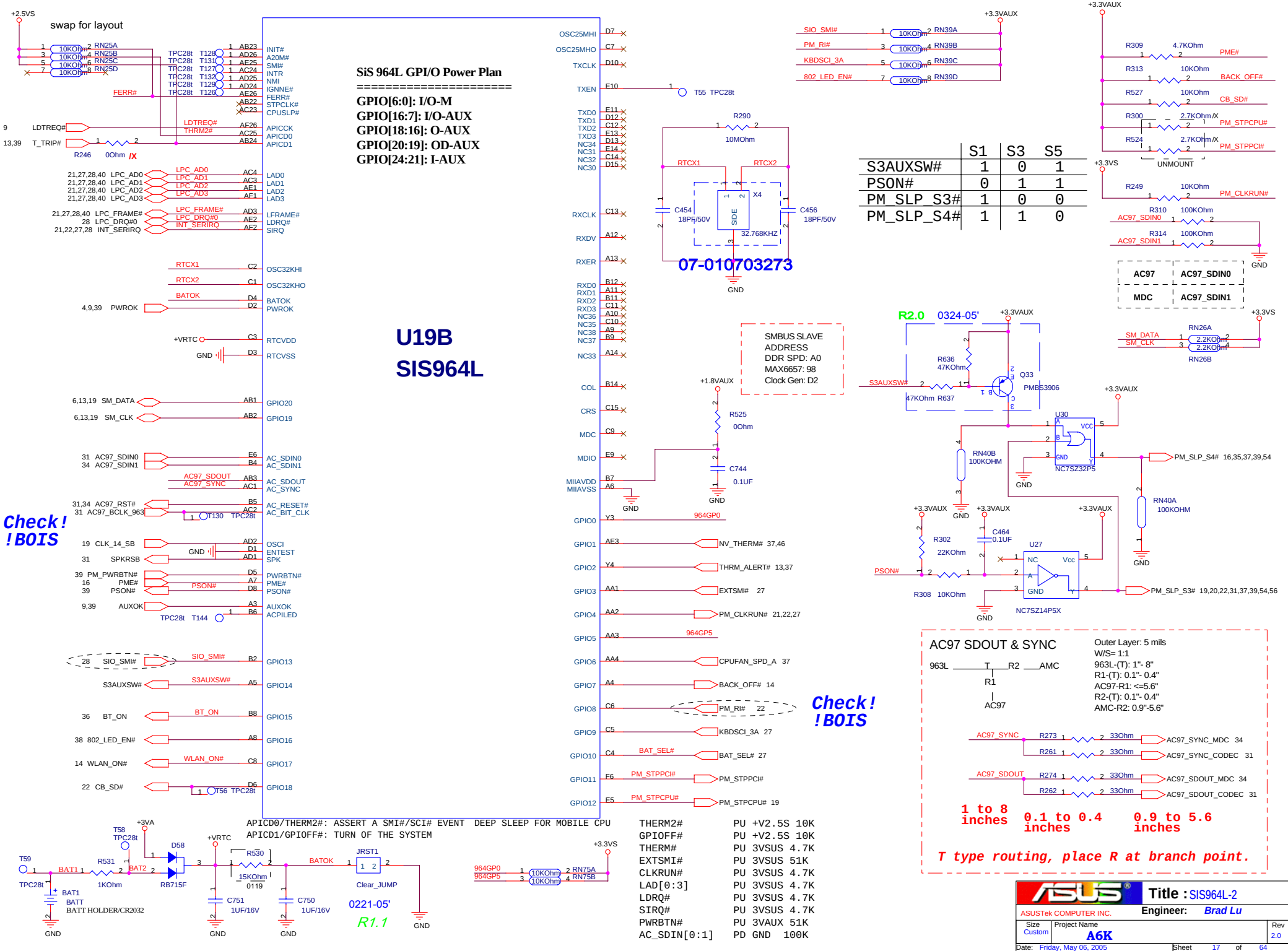
0324-05' R2.0

R2.0 0316-05'

Meet LPC reset >= 60 us
(Add Buffer)

0221-05'
R1.1

ASUSTek COMPUTER INC. NB6		Title : SIS964L-1	
		Engineer: Brad Lu	
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005		Sheet 16 of 64	



	S1	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
PM_SLP_S3#	1	0	0
PM_SLP_S4#	1	1	0

+3.3VS
OVDD/PVDD: 55 mA

+1.8SB_VS
IVDD: 517.4 mA
VDDZ : 19.9 mA
IDEAVDD: 6.9 mA

+1.8VAUX
IVDDAUX: 31.1 mA
MIIAVDD: 2.3 mA
USBPVDD: 7.9 mA
USBCMPAVDD18: 8.5 mA

+3.3VAUX
OVDD_AUX/PVDD_AUX: 52 mA
MIIAVDD: 10 mA
USBVDD33: 1 mA
USBCMPAVDD33: 3.6 mA

+1.8V
USBVDD18: 274.1 mA

UNMOUNT
R526 10MOhm /X
X8
12MHZ
OSC12MOUT
OSC12MIN
CHANGE TO 30PPM
C749 15PF/50V
C733 15PF/50V
GND

U19C
SIS964L

OSC12MHI
OSC12MHO
UV0+
UV0-
UV1+
UV1-
UV2+
UV2-
UV3+
UV3-
UV4+
UV4-
UV5+
UV5-
UV6+
UV6-
UV7+
UV7-
OC0#
OC1#
OC2#
OC3#
OC4#
OC5#
OC6#
OC7#
USBREF
UVDD33_1
UVDD33_2
UVDD33_3
UVDD18_1
UVDD18_2
UVDD18_3
UVDD18_4
UVDD18_5
UVDD18_6
UVDD18_7
UVDD18_8
UVDD18_9
UVDD18_10
USBPVDD18
USBPVSS18
USBCMPAVDD18
USBCMPAVSS18
USBCMPAVDD33
USBCMPAVSS33
IVDD_AUX4
IVDD_AUX5
NC47
NC48
NC42
NC43
NC41
NC49
NC46
NC44
NC40
NC50
NC45
NC39
IVDD3
IVDD4
IVDD5
IVDD6
IVDD1
IVDD12
IVDD22
VSS55
IVDD13
VSS8
IVDD11
VSS9
EESK/GPIO21
EEDI/GPIO22
EEDO/GPIO23
EECS/GPIO24
IPB_OUT0
IPB_OUT1
TRAP0
TRAP1

USB_PP0
USB_PN0
USB_PP1
USB_PN1
USB_PP2
USB_PN2
USB_PP3
USB_PN3
USB_PP4
USB_PN4
USB_PP5
USB_PN5

USBOC#0
USBOC#1
USBOC#2
USBOC#3
USBOC#4
USBOC#5
USBOC#6
USBOC#7

SL6
SL8
SL4
SL5
SL7
SL3
SL2
SL1

R305 127Ohm
L73 120Ohm/100Mhz
L74 120Ohm/100Mhz
L72 120Ohm/100Mhz

C746 0.1UF
C739 0.1UF
C737 0.1UF
C735 0.1UF
C732 10uF/10V
C738 0.1UF
C742 0.1UF
C740 0.1UF
C736 0.1UF

R307 4.7KOhm
R306 4.7KOhm
R304 22Ohm
R303 22Ohm

T146 TPC28t
T145 TPC28t

EECS_964
EEDO_964
IPB_OUT0
IPB_OUT1

Connect to +V1.8AUX if USB wakeup has supported in S3 & S5

964L Strap Pin

SiS 964L Strap Pin	0	1	Default
IPB_OUT0(MuTIOL 1G Clock PLL)	enable	disable	0
IPB_OUT1(MuTIOL Operation Mode Select)	Partial-Swin	Full-Swin	0
AC_SYNC(PCI Clock PLL)	enable	disable	0
Trap [1:0] (MuTIOL Operation Frequency Select)	133MHz	66MHz	0
OC4-(SB debug mode)	enable	disable	1

RN34A USBOC#7
RN34B USBOC#6
RN34C USBOC#5
RN34D USBOC#2
RN37A USBOC#3
RN37B USBOC#0
RN37C USBOC#4
RN37D USBOC#1
10KOhm

USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils

U19D
SIS964L

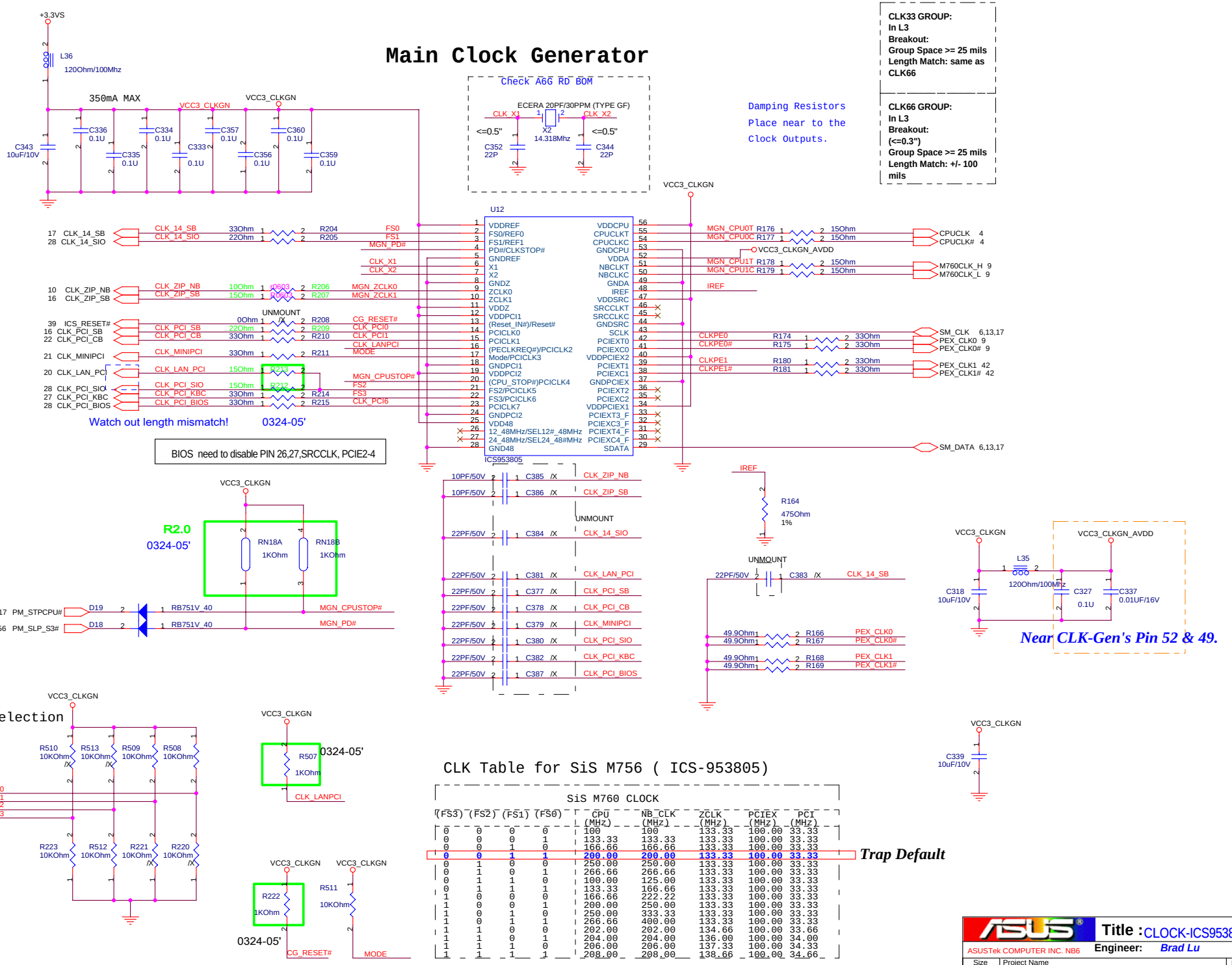
VDDZ2
VDDZ1
VDDZ3
VDDZ4
VDDZ6
VDDZ5
VDDZ7
VDDZ9
VDDZ8
IVDD16
IVDD17
IVDD19
IVDD21
IVDD10
IVDD9
IVDD8
IVDD7
IVDD2
IVDD23
IVDD20
IVDD18
IVDD15
IVDD14
PVDD5
PVDD1
PVDD3
PVDD2
PVDD7
PVDD6
PVDD4
OVDD8
OVDD6
OVDD5
OVDD4
OVDD3
OVDD2
OVDD1
OVDD13
OVDD12
OVDD11
OVDD10
OVDD9
OVDD7
VTT1
VTT2
IVDD_AUX3
IVDD_AUX1
IVDD_AUX2
OVDD_AUX1
OVDD_AUX2
OVDD_AUX5
OVDD_AUX3
OVDD_AUX4
OVDD_AUX6
OVDD_AUX7
OVDD_AUX8
OVDD_AUX9
OVDD_AUX10
PVDD_AUX1
PVDD_AUX2
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC19
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS47
VSS48
VSS49
VSS52
VSS53
VSS54
VSZ1
VSZ2
VSZ3
VSZ4
VSZ6
VSZ7
VSZ8
USBVSS20
USBVSS21
USBVSS22
USBVSS23
USBVSS24
USBVSS25
USBVSS26
USBVSS27
USBVSS4
USBVSS8
USBVSS12
USBVSS16
USBVSS3
USBVSS7
USBVSS19
USBVSS11
USBVSS15
USBVSS2
USBVSS6
USBVSS18
USBVSS10
USBVSS14
USBVSS1
USBVSS5
USBVSS17
USBVSS9
USBVSS13
USBVSS28
USBVSS29
USBVSS30
USBVSS31
USBVSS32
USBVSS33
USBVSS34
USBVSS35
VSS7
VSS4
VSS17
VSS14
VSS3
VSS11
VSS6
VSS2
VSS16
VSS13
VSS1
VSS10
VSS5
VSS15
VSS12
VSS45
VSS46
VSS50
VSS51
VSS18
VSS19
VSZ5
VSZ9
VSZ10

+1.8SB_VS
+3.3VS
+2.5VS
+1.8VAUX
+3.3VAUX
+3.3V
+1.8V
+1.8V_UVDD
+3.3V_UVDD
+IVDD_AUX
+IVDD_AUX

C748 0.1UF
C741 0.1UF
C721 0.1UF
C723 0.1UF
C731 0.1UF
C734 0.1UF
C728 0.1UF
C720 0.1UF
C438 0.1UF
C445 0.1UF
Placed under 964

ASUSTek COMPUTER INC.
Title : SIS964L-3
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 18 of 64

Main Clock Generator

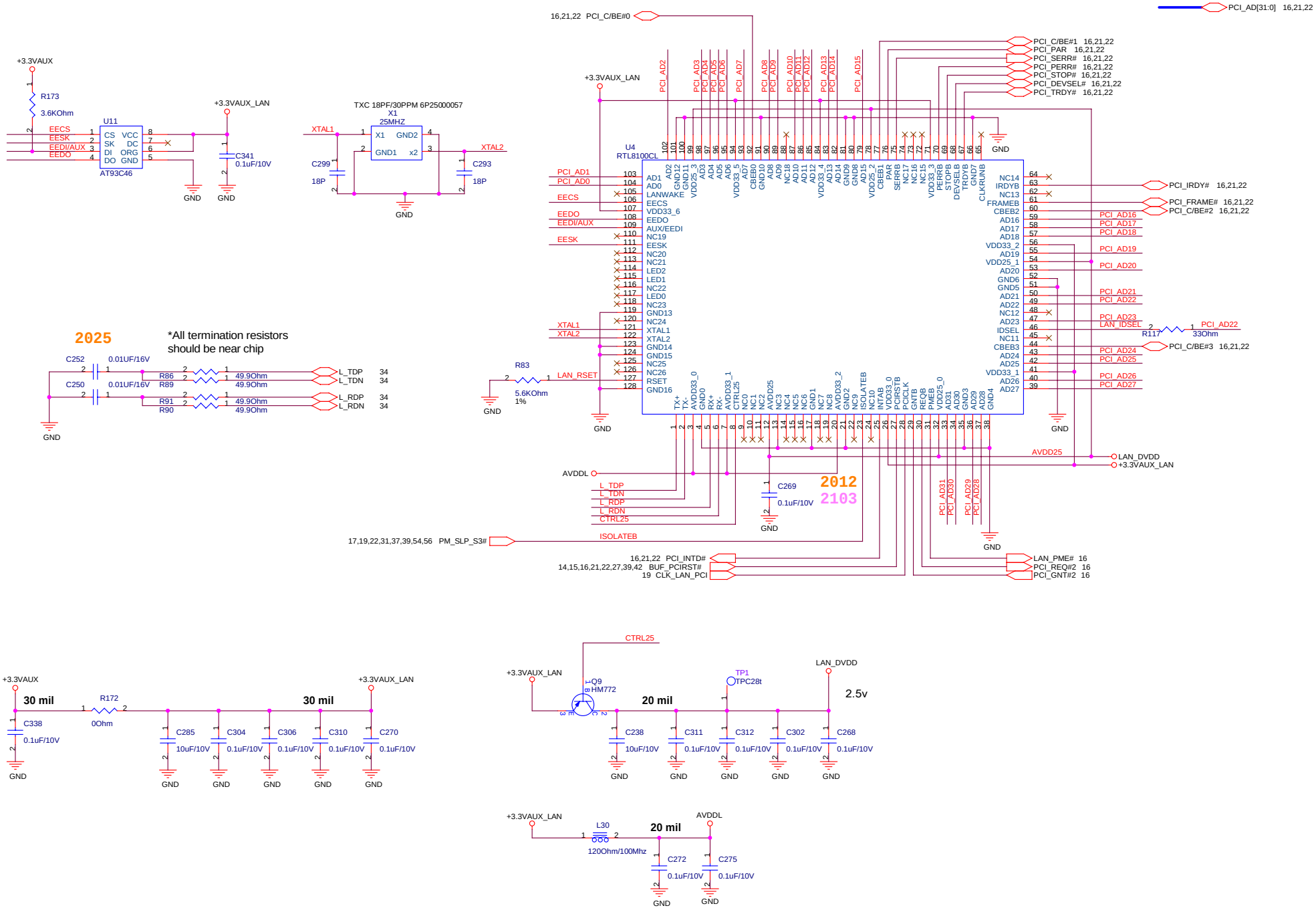


CLK Table for SiS M756 (ICS-953805)

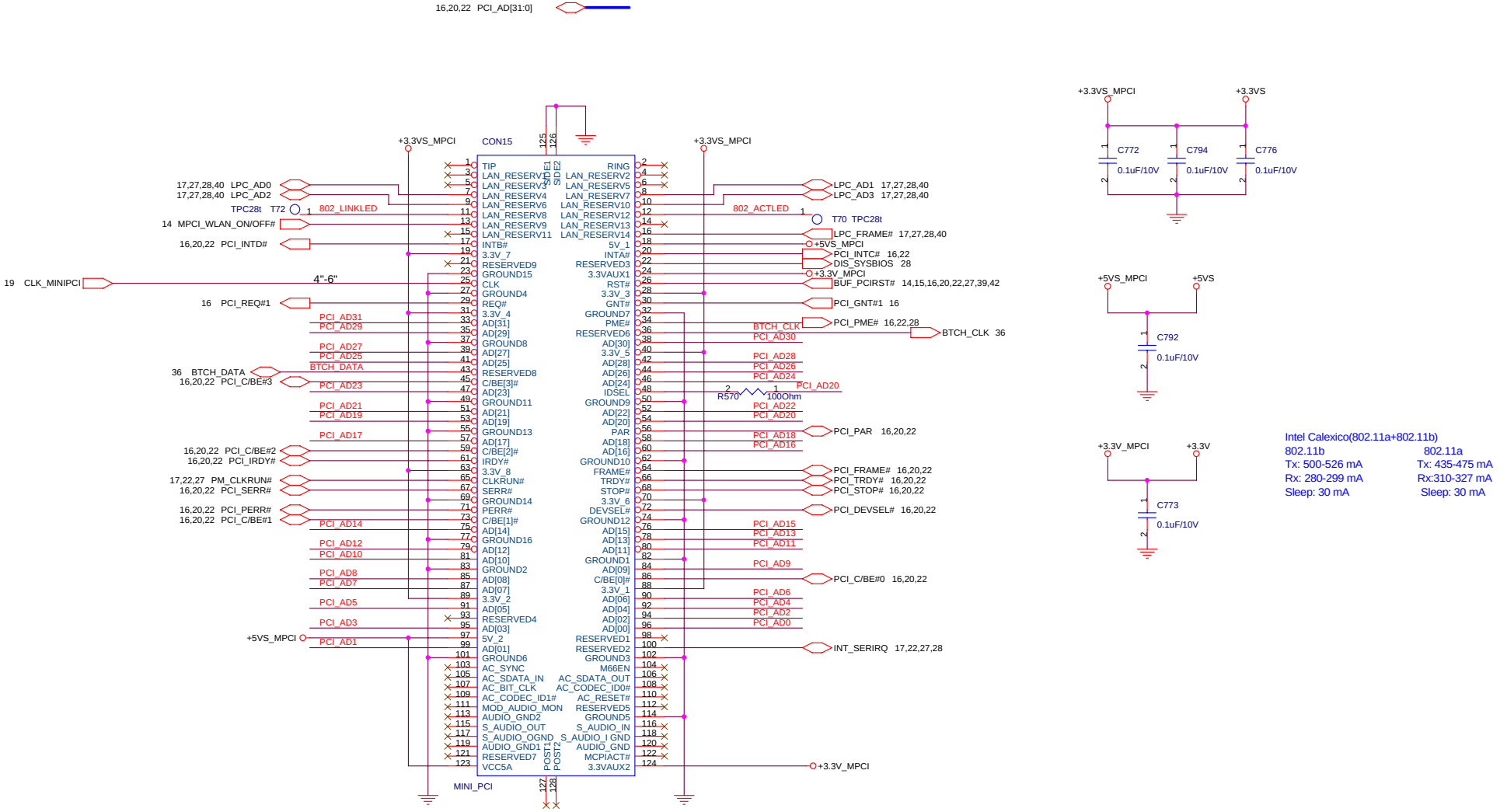
SiS M760 CLOCK

(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	NB_CLK (MHz)	ZCLK (MHz)	PCIEX (MHz)	PCI (MHz)	
0	0	0	0	100	100	133.33	100.00	33.33	
0	0	0	1	133.33	133.33	133.33	100.00	33.33	
0	0	1	0	166.66	166.66	133.33	100.00	33.33	
0	**0**	**1**	**1**	**200.00**	**200.00**	**133.33**	**100.00**	**33.33**	***Trap Default***
0	1	0	0	250.00	250.00	133.33	100.00	33.33	
0	1	0	1	266.66	266.66	133.33	100.00	33.33	
0	1	1	0	100.00	125.00	133.33	100.00	33.33	
0	1	1	1	133.33	166.66	133.33	100.00	33.33	
1	0	0	0	166.66	222.22	133.33	100.00	33.33	
1	0	0	1	200.00	250.00	133.33	100.00	33.33	
1	0	1	0	250.00	333.33	133.33	100.00	33.33	
1	0	1	1	266.66	400.00	133.33	100.00	33.33	
1	1	0	0	202.00	202.00	134.66	100.00	33.66	
1	1	0	1	204.00	204.00	136.00	100.00	34.00	
1	1	1	0	206.00	206.00	137.33	100.00	34.33	
1	1	1	1	208.00	208.00	138.66	100.00	34.66	

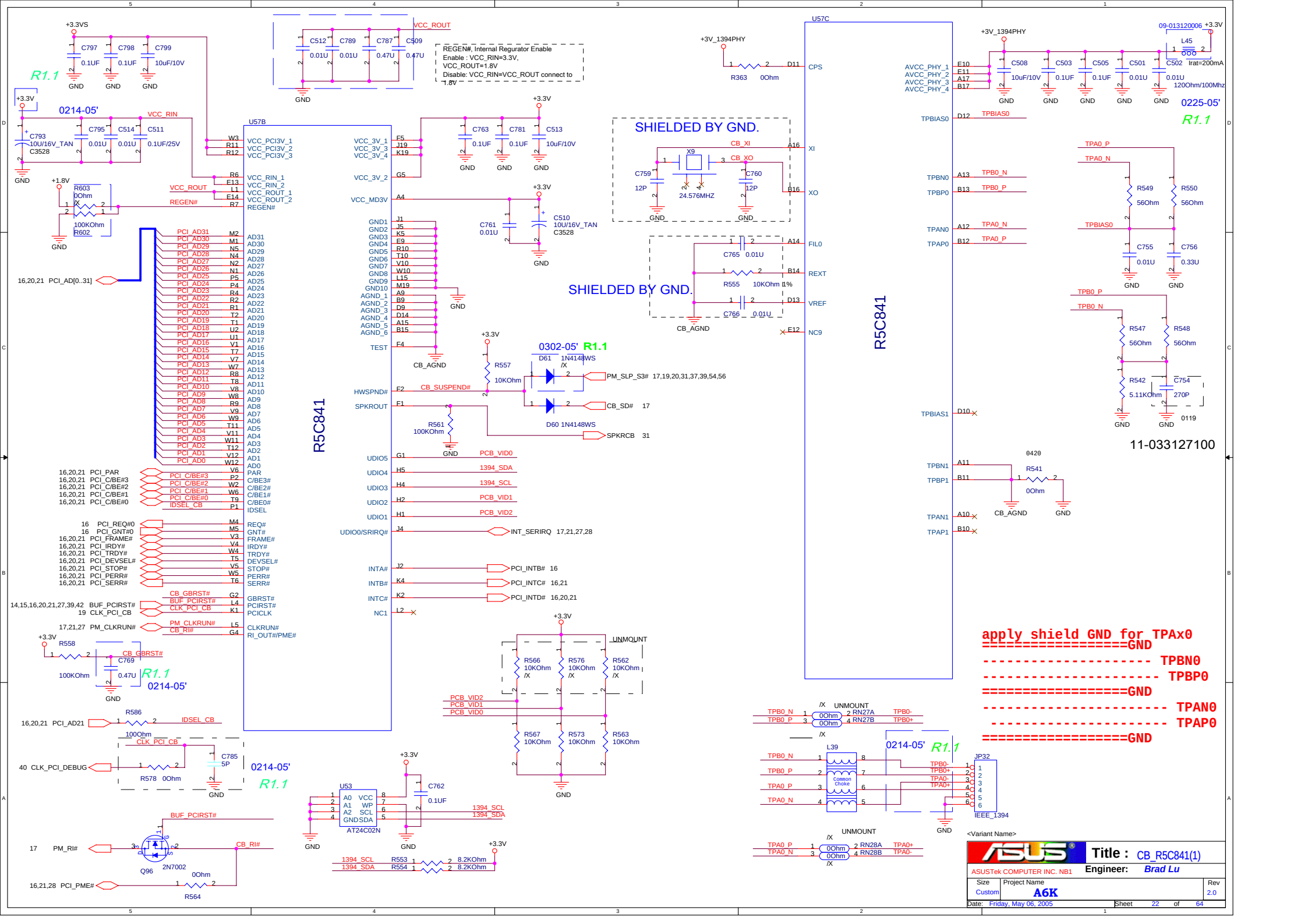
ASUSTek COMPUTER INC. NB6	Title : CLOCK-ICS953805	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 19 of 64	



ASUSTek COMPUTER INC. NB6	Title : LAN-RTL8100CL	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 20 of 64	



ASUSTek COMPUTER INC. NB6	Title : MINIPCI	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 21 of 64	


R5C841
U57B
U57C
R5C841
SHIELDED BY GND.
SHIELDED BY GND.
REGEN#, Internal Regurator Enable
Enable : VCC_RIN=3.3V,
VCC_ROUT=1.8V
Disable: VCC_RIN=VCC_ROUT connect to 1.8V
0214-05' R1.1
0302-05' R1.1
0225-05' R1.1
0214-05' R1.1
0214-05' R1.1
11-033127100
apply shield GND for TPAx0
==========GND
---------- TPBN0
---------- TPBP0
==========GND
---------- TPAN0
---------- TPAP0
==========GND
Title : CB_R5C841(1)
ASUSTek COMPUTER INC. NB1
Engineer: Brad Lu
Size: Custom
Project Name: A6K
Rev: 2.0
Date: Friday, May 06, 2005
Sheet 22 of 64

MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

藍色pin腳名稱的訊號
是要經由MUX分離的訊號
以避免841的假的LPC訊號
跟SYSTEM的LPC訊號相衝突

U57A

C1 NC2
D1 NC3
E1 NC4
C2 NC5
D2 NC6
E2 NC7
E4 NC8

CADR25 J18 AD19/A25 24
CADR24 J15 AD17/A24 24
CADR23 K16 CFRAME#/A23 24
CADR22 L16 CTRDY#/A22 24
CADR21 L18 CDEVSEL#/A21 24
CADR20 M16 CSTOP#/A20 24
CADR19 N19 CBLOCK#/A19 24,40
CADR18 N16 C_RFU/A18 40
CADR17 P16 AD16/A17 24
CADR16 L19 R_CCLK/A16_D3
R581 22Ohm
CCLK/A16_D3 24
C780 5P
CADR15 K15 CIRDY#/A15 24
CADR14 N18 C_CPERR#/A14 40
CADR13 N15 CPAR/A13 24
CADR12 K18 CBE2#/A12 24
CADR11 R18 AD12/A11 24
CADR10 U19 AD9/A10 24
CADR9 R19 AD14/A9 24
CADR8 P15 CBE1#/A8 24
CADR7 J16 AD18/A7 24
CADR6 H15 AD20/A6 24
CADR5 H18 AD21/A5 24
CADR4 G15 AD22/A4 24
CADR3 G18 AD23/A3 24
CADR2 F15 AD24/A2 24
CADR1 F18 AD25/A1 24
CADR0 E16 AD26/A0 24

CDATA15 U18 AD8/D15 24
CDATA14 W18 C_RFU/D14 40
CDATA13 V17 AD6/D13 24
CDATA12 V16 AD4/D12 24
CDATA11 V15 AD2/D11 24
CDATA10 B19 AD31/D10 24
CDATA9 C18 AD30/D9 24
CDATA8 D18 AD28/D8 24
CDATA7 W17 AD7/D7 24
CDATA6 W16 AD5/D6 24
CDATA5 W15 AD3/D5 24
CDATA4 T15 AD1/D4 24
CDATA3 R14 AD0/D3 24
CDATA2 C19 C_RFU/D2 40
CDATA1 D19 AD29/D1 24
CDATA0 E19 AD27/D0 24

+VCCCB
R556 100KOhm

OE# T19 AD11/OE# 24
WE# M15 CGNT#/WE# 24
CE2# T18 AD10/CE2# 24
CE1# V19 CBE0#/CE1# 24
REG# F16 CBE3#/REG# 24
RESET H19 CRST#/RESET 24
WAIT# G16 C_CSERR#/WAIT# 40
WP/IOIS16# A18 C_CCLKRUN#/IOIS16# 40
RDY/IREQ# M18 CINT#/IREQ# 24
BVD2 F19 C_CAUDIO/SPKR_IN#/BVD2 40
BVD1 E18 C_STSCHG/STSCHG#/BVD1 40
VS2# R16 CVS2 24
VS1# R15 CVS1 24
CD2# D15 CCD2# 24
CD1# T14 CCD1# 24,40
INPACK# G19 CREQ#/INPACK# 24

IORD# P18 AD13/IORD# 24
IOWR# P19 AD15/IOWR# 24

USBDP V14
USBDM W14

+3.3V
R599 100KOhm
VPPEN1 W13 VPP_EN1 24
VPPEN0 V13 VPP_EN0 24
VCC3EN# T13 VCC3_EN# 24
VCC5EN# R13 VCC5_EN# 24

R5C841

E8 MDIO19
D8 MDIO18
B8 MDIO17
A8 MDIO16
E7 MDIO15
D7 MDIO14
B7 MDIO13
A7 MDIO12
E6 MDIO11
D6 MDIO10
B6 MDIO09
A6 MDIO08
D5 MDIO07
B5 MDIO06
A5 MDIO05
B4 MDIO04
B3 MDIO03
A3 MDIO02
A2 MDIO01
B1 MDIO00

SD_D3/MSCD3
SD_D2/MSCD2
SD_D1/MSCD1
SD_D0/MSCD0
SD/MS_CLK [2] R551 22Ohm
SD_CMD/MS_BS
GND R552 0Ohm
SD/MS_PWR_EN#
SD_WP#
MS_CD#
SD_CD#

0324-05' R2.0

R2.0 0324-05'

+3.3V
Q98 SI2301BDS
+3.3V_MC_VCC
+12V
C782 0.1UF
C783 0.1UF
R634 150KOhm
R579 100KOhm
GND
R2.0 0324-05'

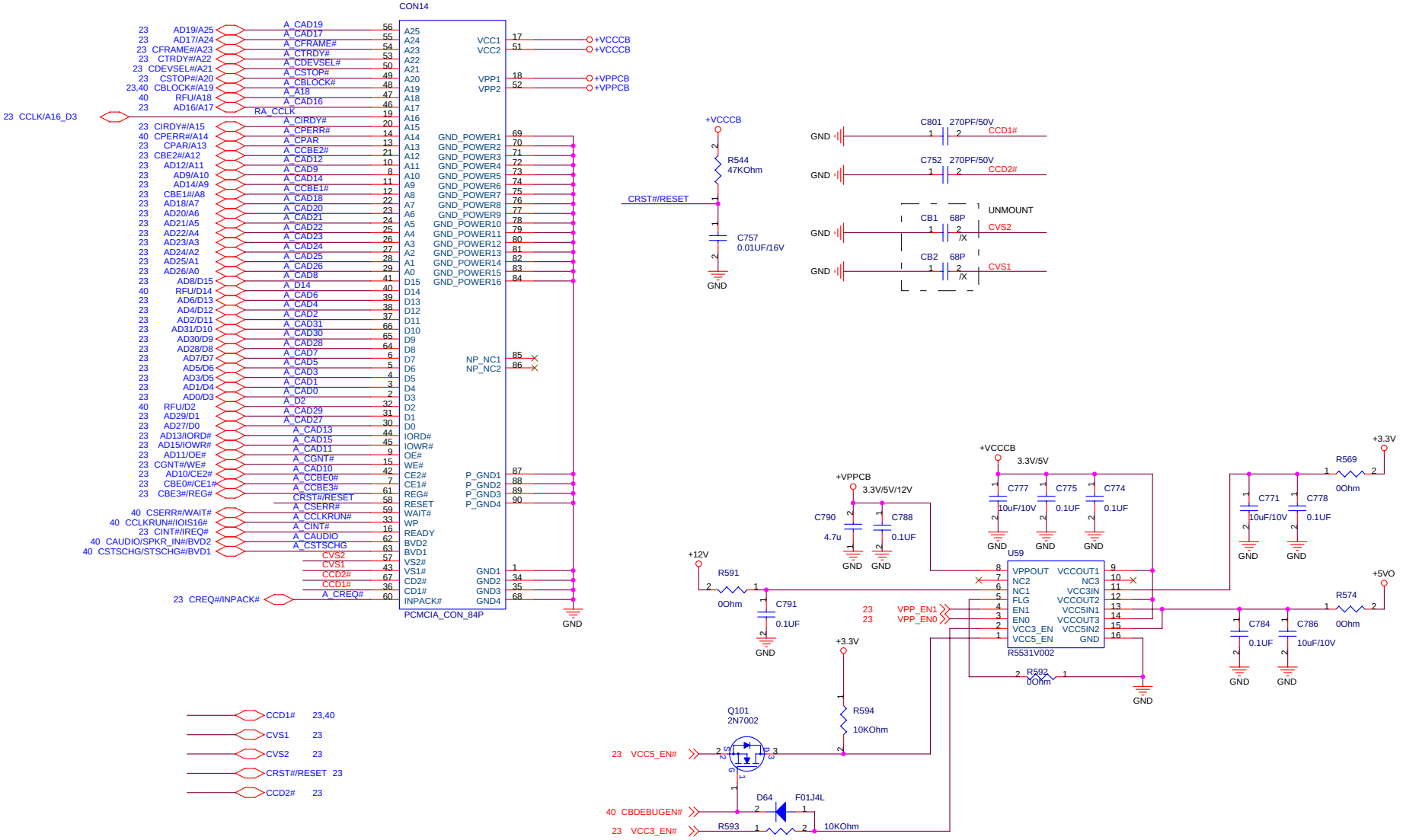
SD/MS_PWR_EN# 1
Q99 PDTC144EK
R-1 47K
R-2 47K
GND

SD_WP#
SD_CD#
+3.3V_MC_VCC
GND
CON6
SD_D1/MSCD1
SD_D0/MSCD0
SD/MS_CLK
SD_CMD/MS_BS
SD_D3/MSCD3
SD_D2/MSCD2
C767 33P
Fix MMC Card Can't be identified.
0427-05'
SD_DAT1
SD_DAT0
SD_VSS1
SD_CLK
SD_VCC
SD_VSS2
SD_CMD
SD_DAT3
SD_DAT2
SD_WP_PROTECT
SD_CD_DETECT
NP_NC1
MS_VSS1
MS_BS
MS_VCC1
MS_SDIO
MS_RESERVED1
MS_INS
MS_RESERVED2
MS_SCLK
MS_VCC2
MS_VSS2
NP_NC2
SD_CARD_19P

<Variant Name>

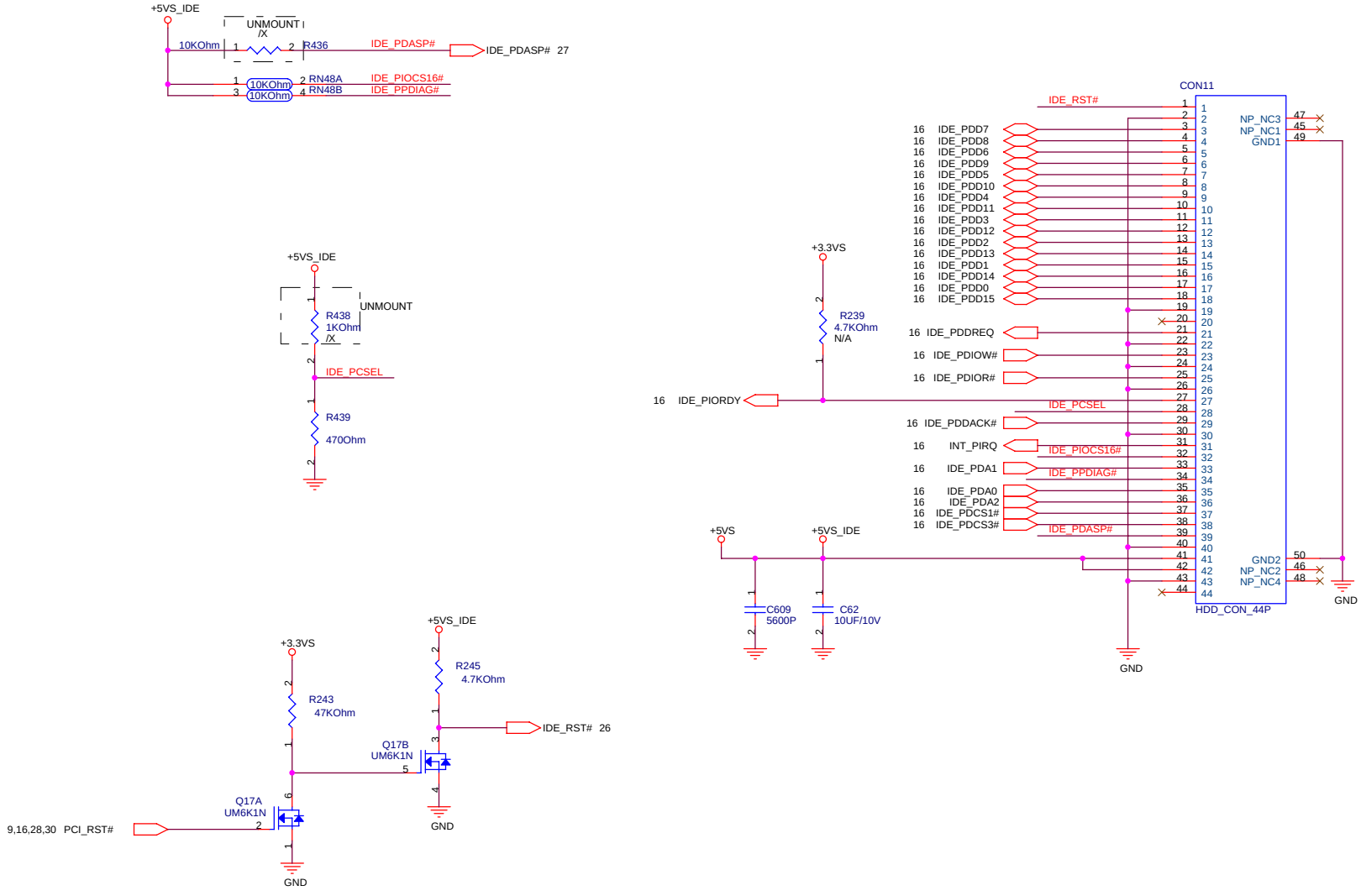
ASUSTek COMPUTER INC. NB1	Title : CB_R5C841 (2)	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 23 of 64	

PCMCIA SOCKET

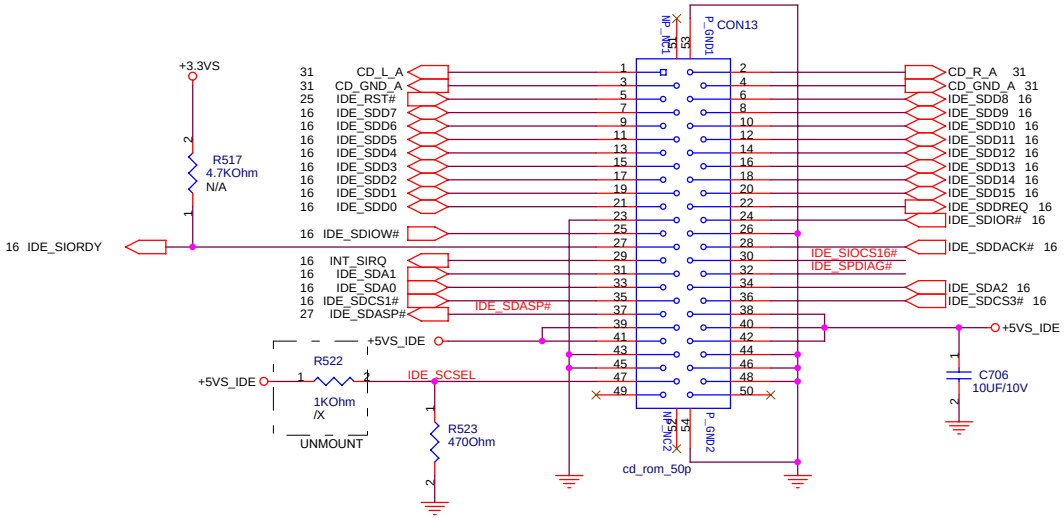


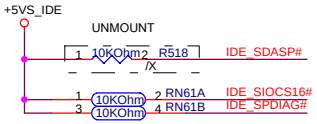
<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : PCMCIA	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 24 of 64	



ASUSTek COMPUTER INC. NB6	Title : HDD Connector	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 25 of 64	





ASUSTek COMPUTER INC. NB6	Title : ODD Connector	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 26 of 64	

P23,P43 excahnged by BIOS's request

Daisy-Chain in layout

S0-S3: (2.5 mA Typ, 7 mA Max.)

LxWxH=14x14x1.7

U22

M38857

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

Audio DJ pin depends on Keyboard Matrix.

Follow M6N

A3N follow M6N Keyboard Matrix

P21: Power button overwrite disable. Only can be pulled down as default value than can be used as a input.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell

4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%

OC MEAN OPEN DRAIN

CON4

ZIF_CON_28P

K/B	US	UK	JP
KEYDETECT1	H	L	L
KEYDETECT2	H	H	L

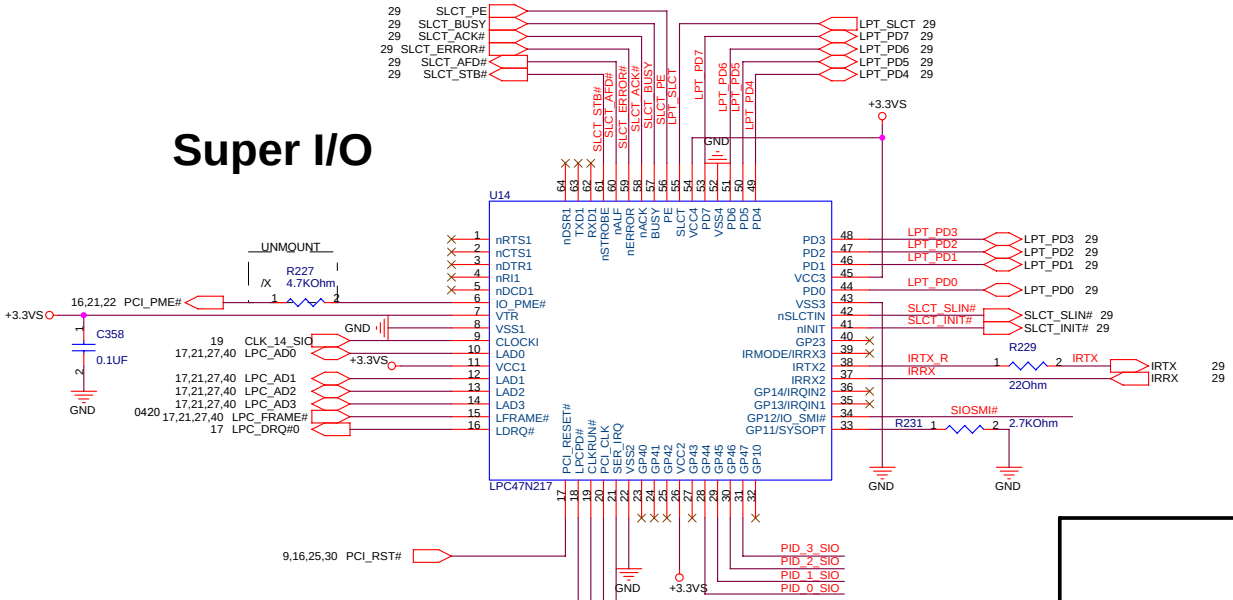
IDE

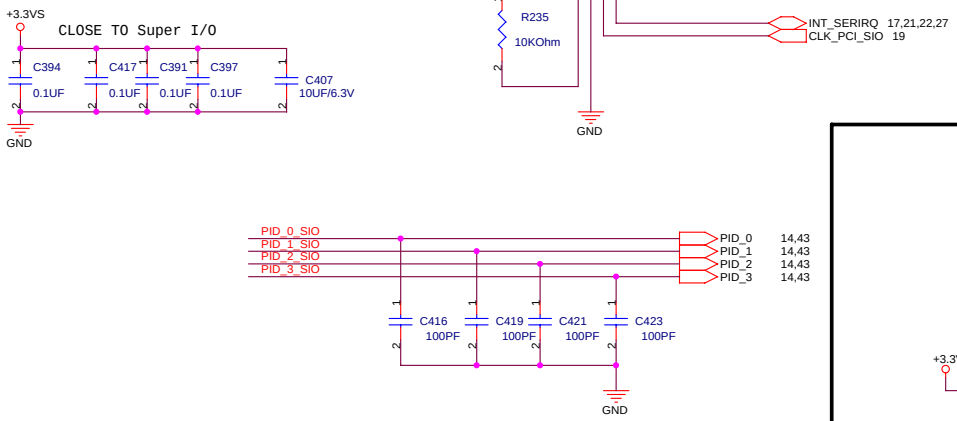
NUM CAP SCR

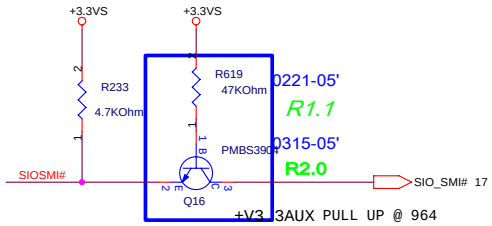
R1.1

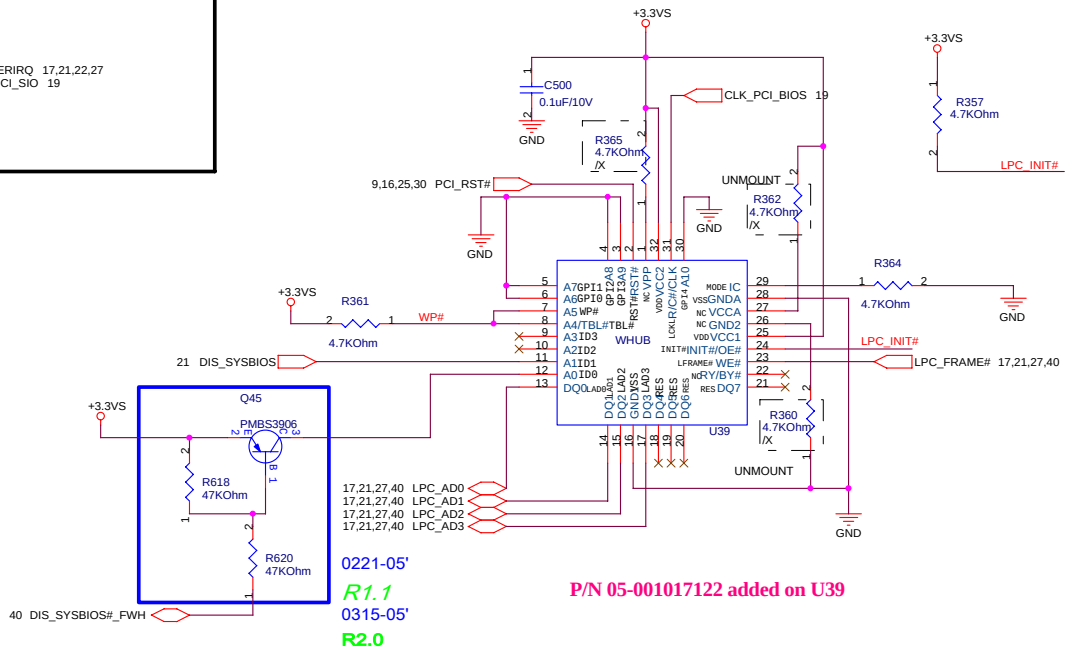
Title : KBC-M38857			
ASUSTek COMPUTER INC. NB6	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005	Sheet 27 of 64		

Super I/O





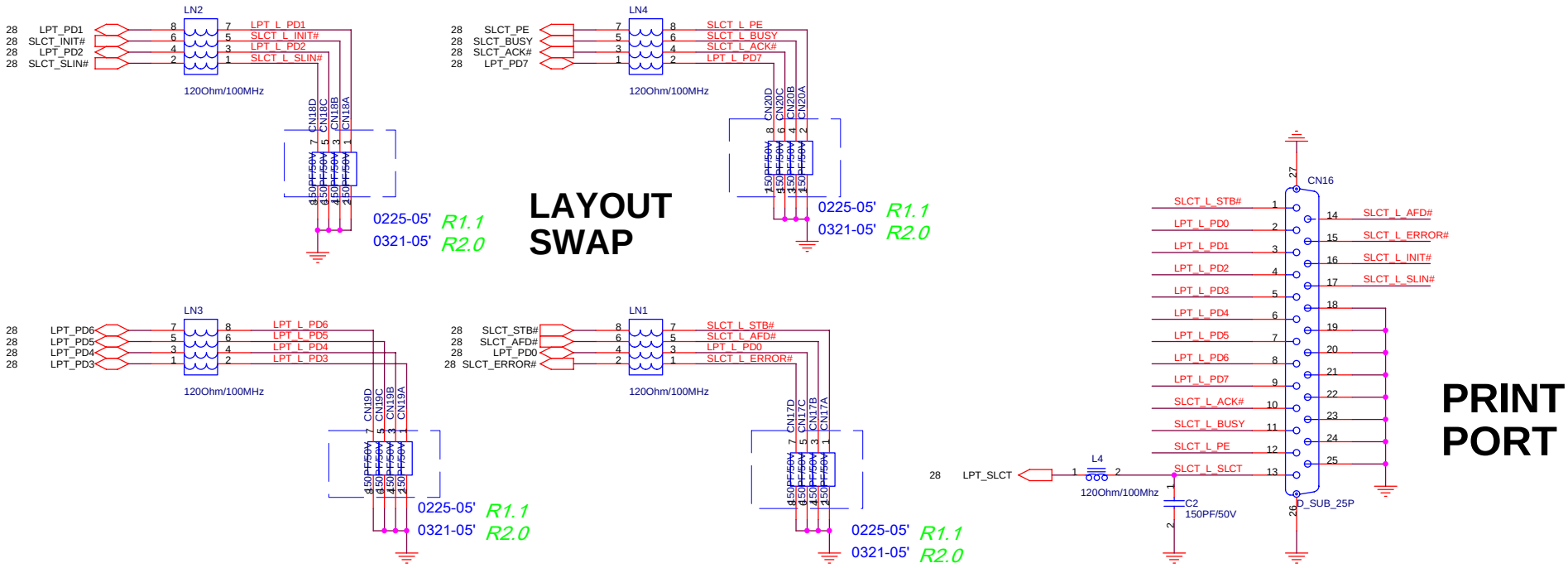


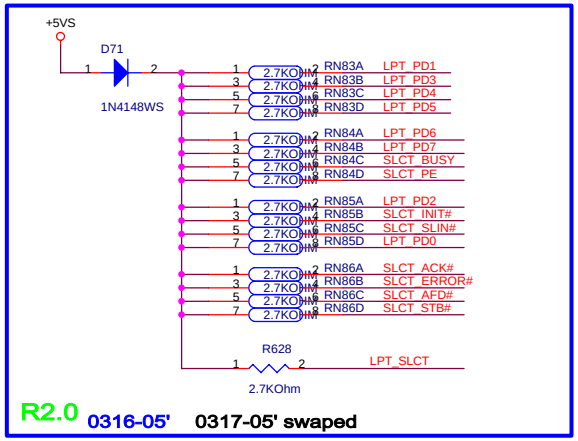


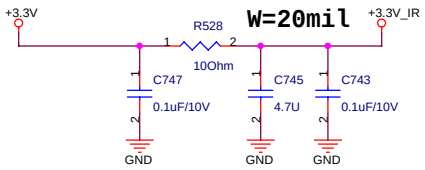
Nomal : OPEN
DB Card Disable MB BIOS : LOW
DB Card Enable MB BIOS : HI

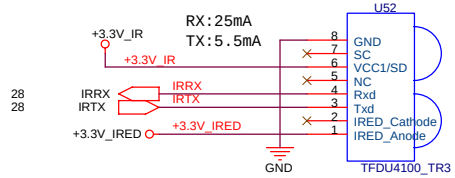
ID[0:3] : internal Pull-down 20K~100K

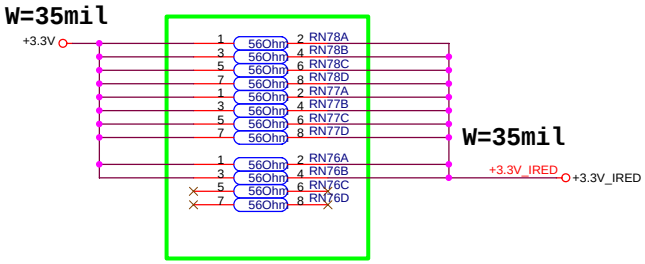
ASUSTek COMPUTER INC. NB6	Title : LPC47N217 & BIOS	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 28 of 64	









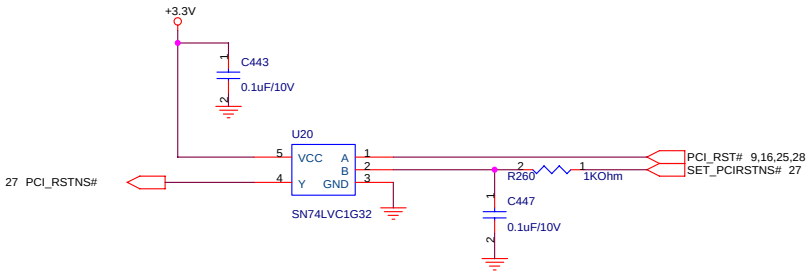


ASUSTek COMPUTER INC. NB6	Title : IR & LPT PORT	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 29 of 64	

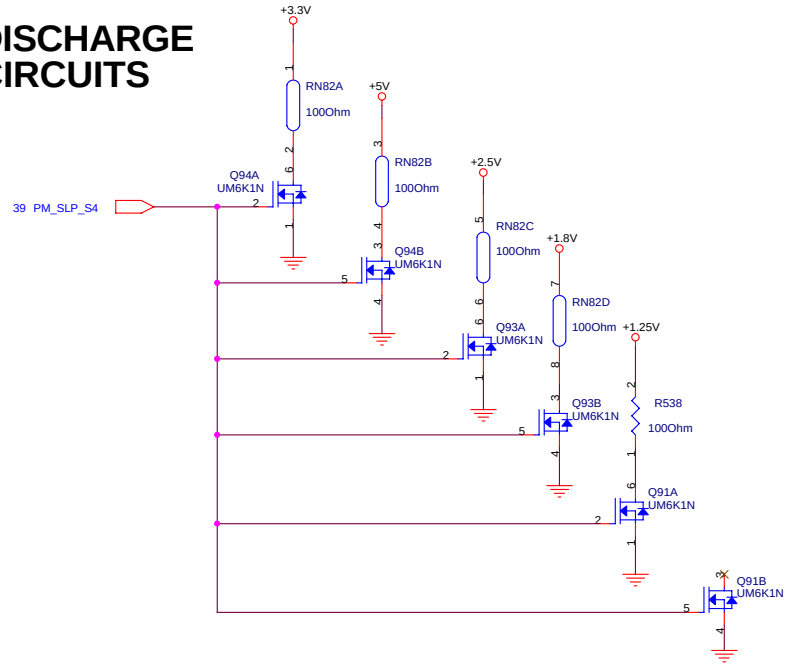
PCMCIA DEBUG Card

1105

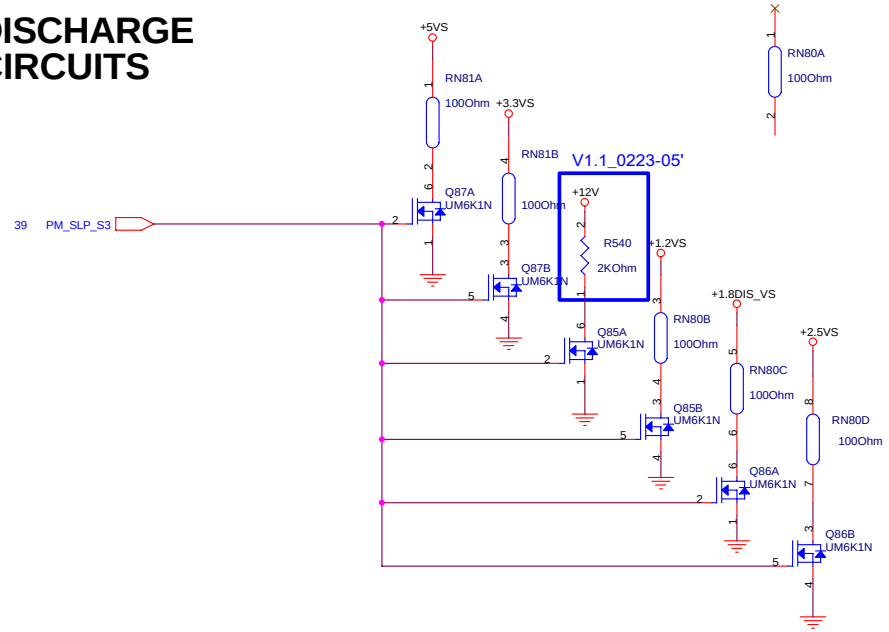
PCI_RSTNS# Gen Circuit



DISCHARGE CIRCUITS



DISCHARGE CIRCUITS



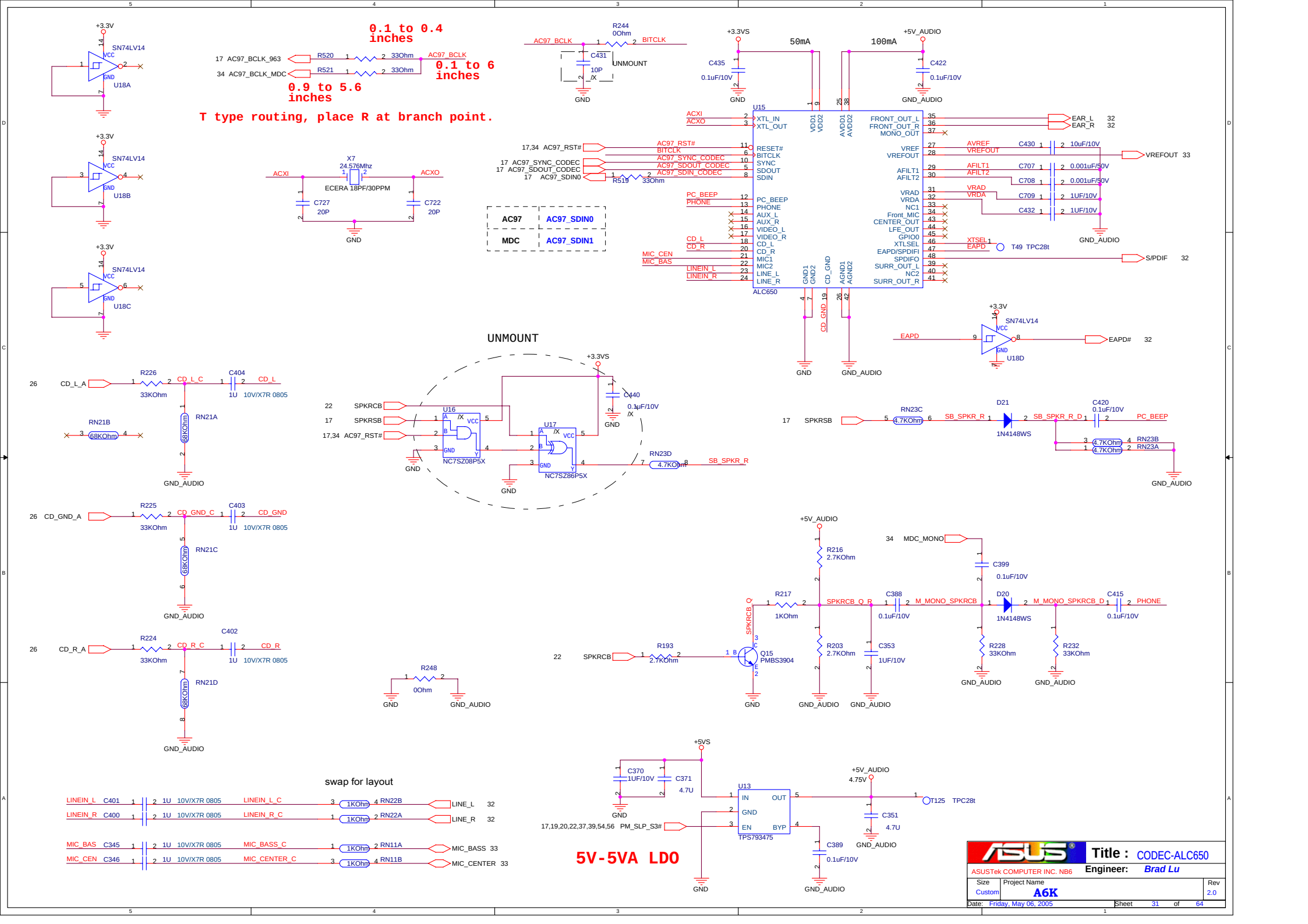
ASUSTek COMPUTER INC. NB6

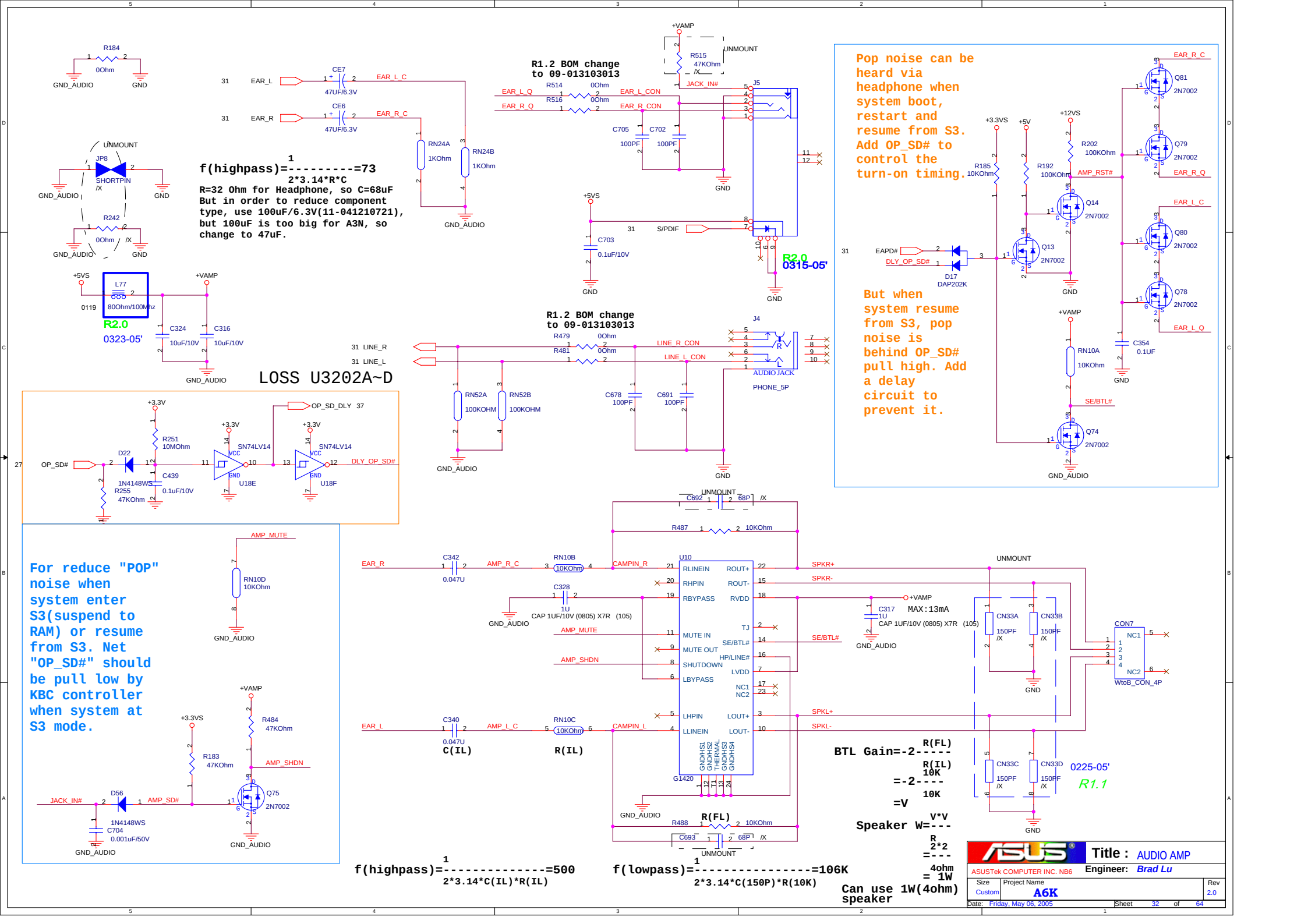
Title : Discharge circuit

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	2.0

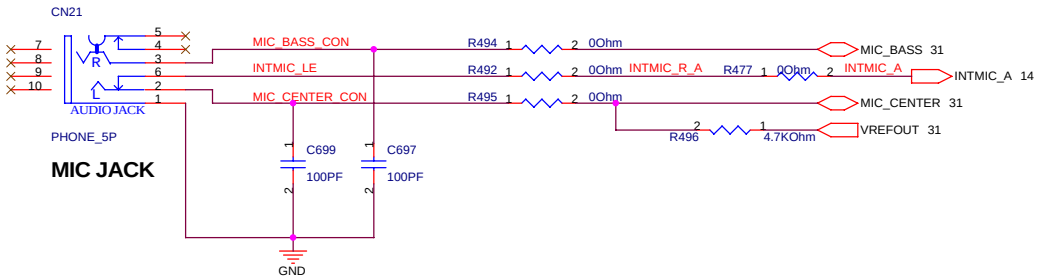
Date: Friday, May 06, 2005 Sheet 30 of 64

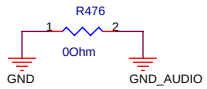

0.1 to 0.4 inches
0.1 to 6 inches
0.9 to 5.6 inches
T type routing, place R at branch point.
UNMOUNT
swap for layout
5V-5VA LDO
ALC650
SN74LV14
NC7SZ08P5X
NC7SZ86P5X
TPS793475
PMBS3904
1N4148WS
ECERA 18PF/30PPM
AC97 SDIN0
MDC AC97_SDIN1
Title : CODEC-ALC650
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Project Name A6K
Size Custom
Rev 2.0
Date: Friday, May 06, 2005
Sheet 31 of 64

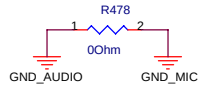

R184
0Ohm
GND_AUDIO
GND
UNMOUNT
JP8
SHORTPIN
/X
R242
0Ohm
/X
31 EAR_L
CE7
47UF/6.3V
EAR_L_C
31 EAR_R
CE6
47UF/6.3V
EAR_R_C
RN24A
1KOhm
RN24B
1KOhm
f(highpass)=1/(2*3.14*R*C)=73
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.
+5VS
L77
0119
80Ohm/100Mhz
+VAMP
R2.0
0323-05'
C324
10uF/10V
C316
10uF/10V
LOSS U3202A~D
R1.2 BOM change to 09-013103013
+VAMP
R515
47KOhm
/X
UNMOUNT
JACK_IN#
J5
EAR_L_Q
EAR_R_Q
R514
R516
0Ohm
EAR_L_CON
EAR_R_CON
C705
100PF
C702
100PF
+5VS
31 S/PDIF
C703
0.1uF/10V
R2.0
0315-05'
Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.
+3.3VS
+5V
+12VS
R185
10KOhm
R192
100KOhm
R202
100KOhm
AMP_RST#
EAPD#
DLY_OP_SD#
D17
DAP202K
Q13
2N7002
Q14
2N7002
Q81
2N7002
Q79
2N7002
Q80
2N7002
Q78
2N7002
Q74
2N7002
EAR_R_C
EAR_R_Q
EAR_L_C
EAR_L_Q
C354
0.1UF
RN10A
10KOhm
SE/BTL#
R1.2 BOM change to 09-013103013
31 LINE_R
31 LINE_L
R479
R481
0Ohm
LINE_R_CON
LINE_L_CON
J4
AUDIO JACK
PHONE_5P
RN52A
100KOHM
RN52B
100KOHM
C678
100PF
C691
100PF
27 OP_SD#
D22
1N4148WS
R255
47KOhm
R251
10MOhm
C439
0.1uF/10V
SN74LV14
U18E
U18F
OP_SD_DLY
DLY_OP_SD#
For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.
AMP_MUTE
RN10D
10KOhm
+VAMP
+3.3VS
R484
47KOhm
R183
47KOhm
AMP_SHDN
JACK_IN#
D56
1N4148WS
C704
0.001uF/50V
AMP_SD#
Q75
2N7002
EAR_R
C342
0.047U
AMP_R_C
RN10B
10KOhm
CAMPIN_R
C328
1U
CAP 1UF/10V (0805) X7R (105)
EAR_L
C340
0.047U
AMP_L_C
RN10C
10KOhm
CAMPIN_L
C(IL)
R(IL)
U10
RLINEIN
RHPIN
RBYPASS
MUTE IN
MUTE OUT
SHUTDOWN
LBYPASS
LHPIN
LLINEIN
ROUT+
ROUT-
RVDD
TJ
SE/BTL#
HP/LINE#
LVDD
NC1
NC2
LOUT+
LOUT-
G1420
C692
68P
/X
R487
10KOhm
R488
10KOhm
C693
68P
/X
SPKR+
SPKR-
SPKL+
SPKL-
C317
1U
CAP 1UF/10V (0805) X7R (105)
MAX:13mA
CN33A
150PF
/X
CN33B
150PF
/X
CN33C
150PF
/X
CN33D
150PF
/X
CON7
WtoB_CON_4P
f(highpass)=1/(2*3.14*C(IL)*R(IL))=500
f(lowpass)=1/(2*3.14*C(150P)*R(10K))=106K
BTL Gain=-2*R(FL)/R(IL)=-2*10K/10K=V
Speaker W=V*V/R=2*2/4ohm=1W
Can use 1W(4ohm) speaker
0225-05'
R1.1
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 32 of 64

MIC OP CIRCUIT

MIC JACK





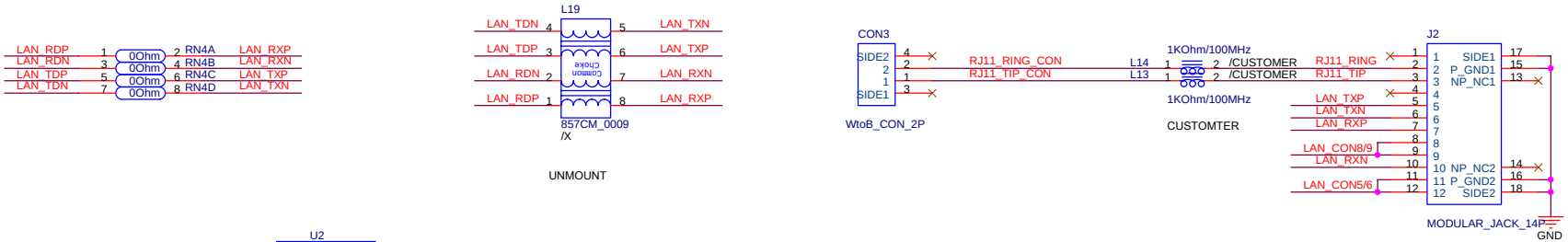


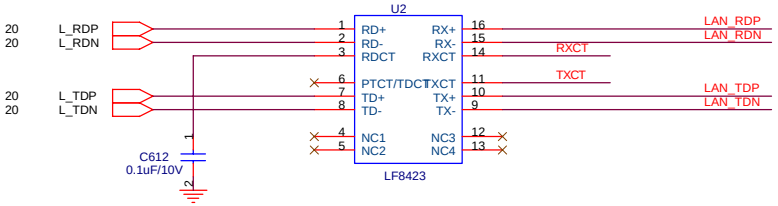
INTMIC_A:GND_AUDIO : W/P/X = 12/5/15mils

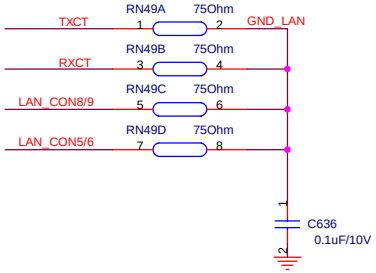
R111 & R112 change to 09-013103013 in R1.2 BOM

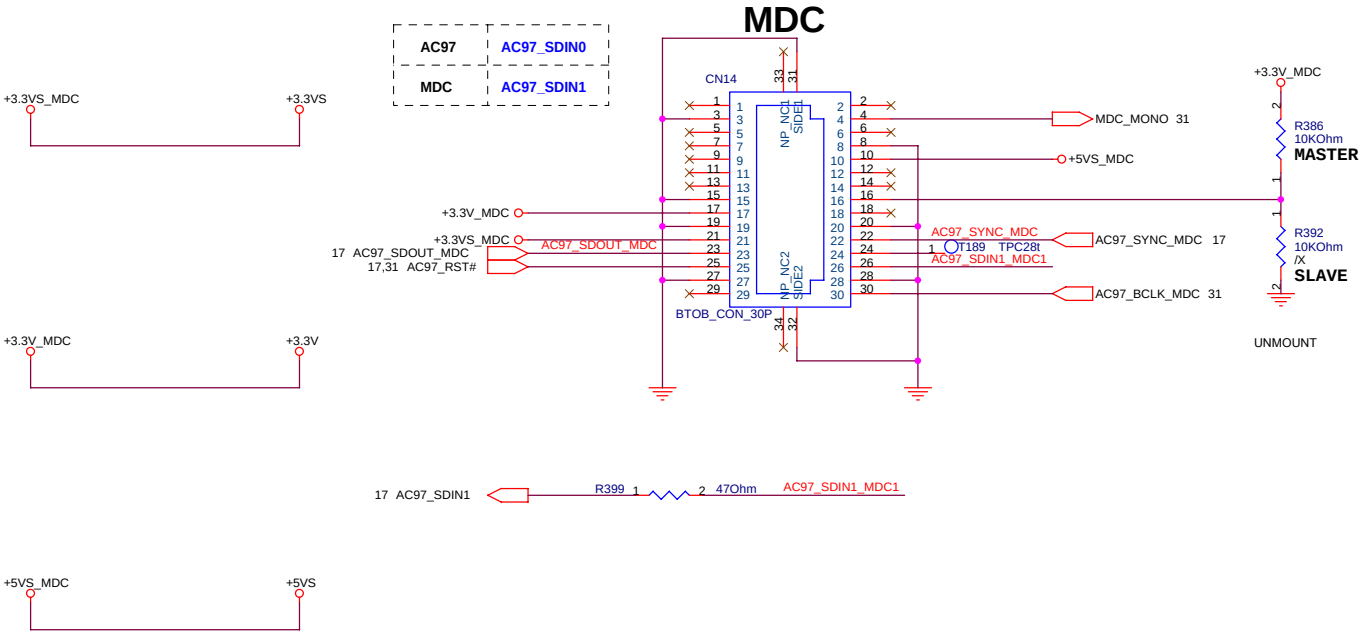
ASUSTek COMPUTER INC. NB6	Title : MIC	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 33 of 64	

OP: FOR EMI

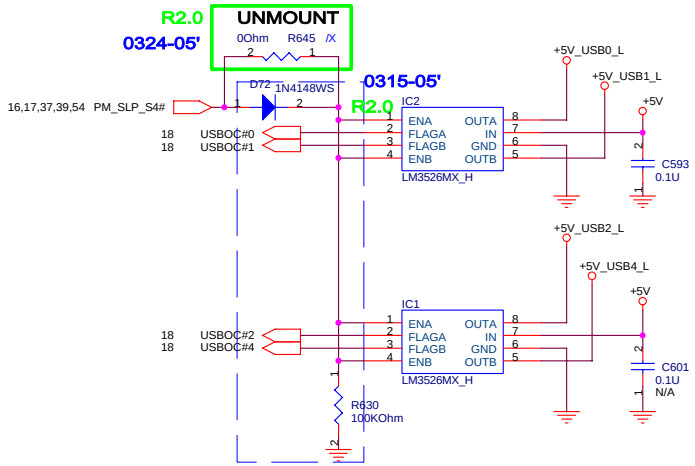


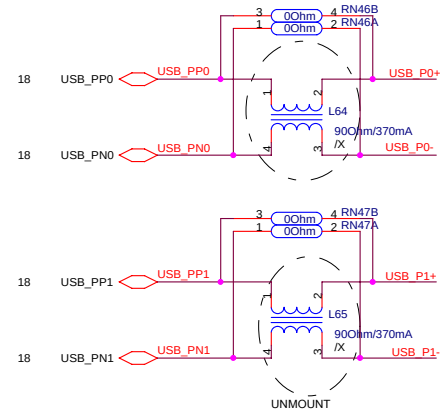


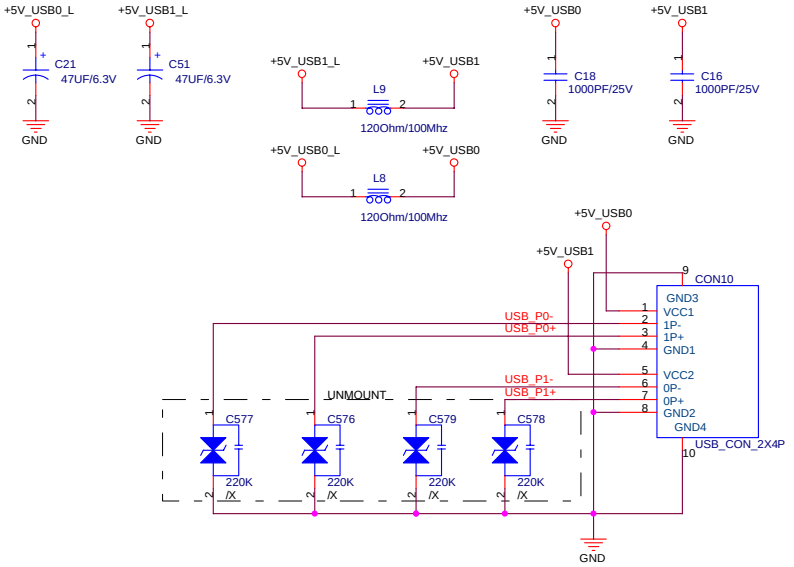




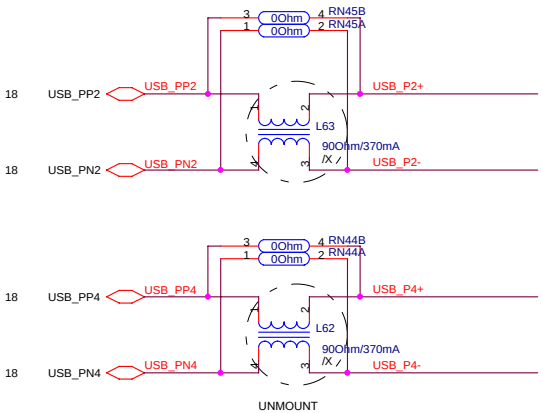
ASUSTek COMPUTER INC. NB6	Title : MDC & RJ45 & RJ11	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 34 of 64	

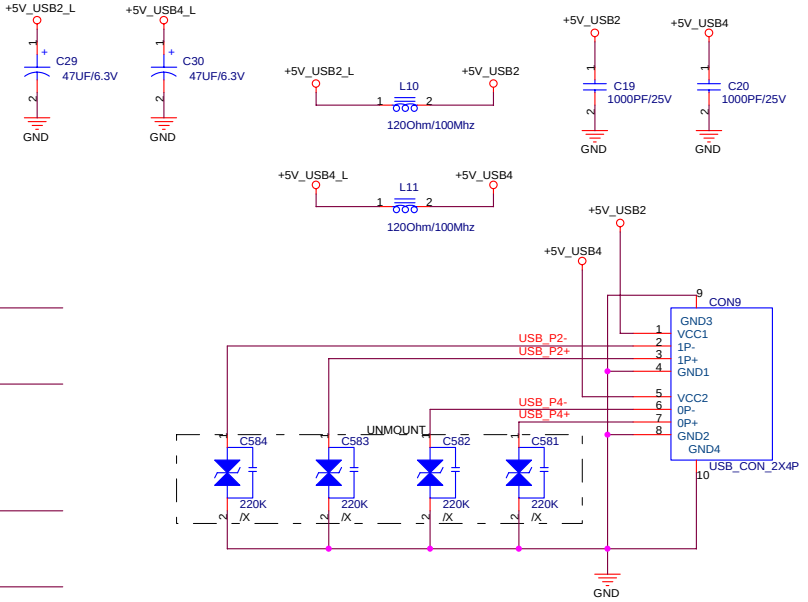






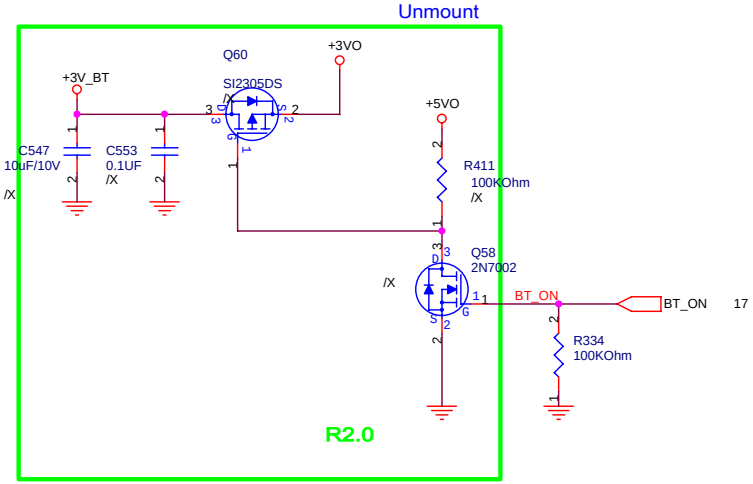
USB PORT 0 & PORT 1



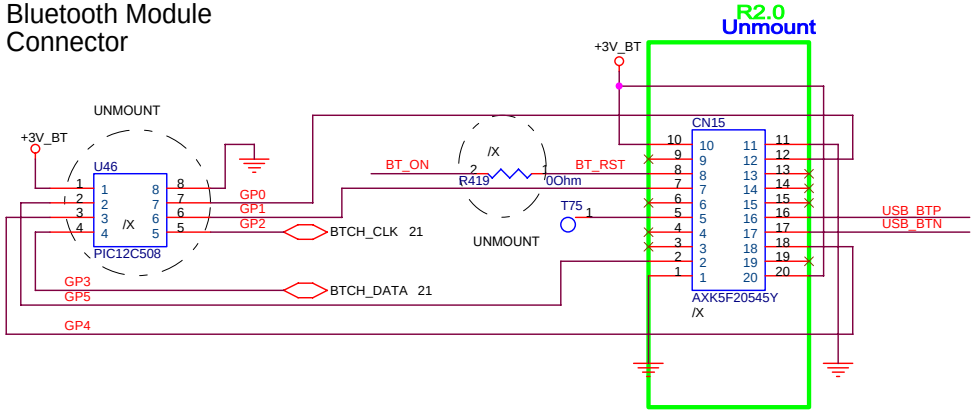


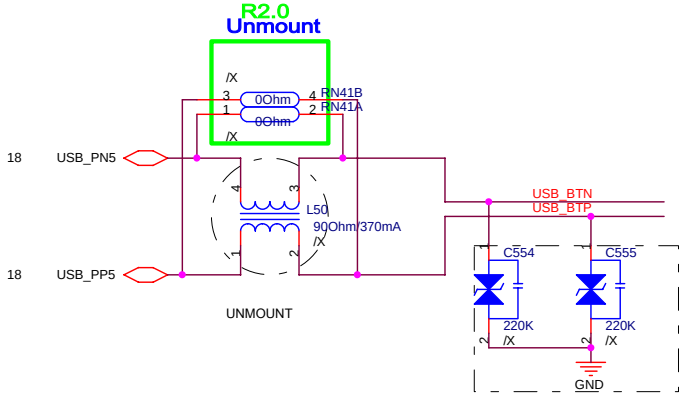
USB PORT 2 & PORT 4

ASUSTek COMPUTER INC. NB6	Title : USB	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 35 of 64	



Bluetooth Module Connector





USB PORT 5 for Bluetooth Module

ASUSTek COMPUTER INC. NB6	Title : BT_UGPZ5	
	Engineer: *Bruce Lee*	
Size: B	Project Name: **A6K**	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 36 of 64	

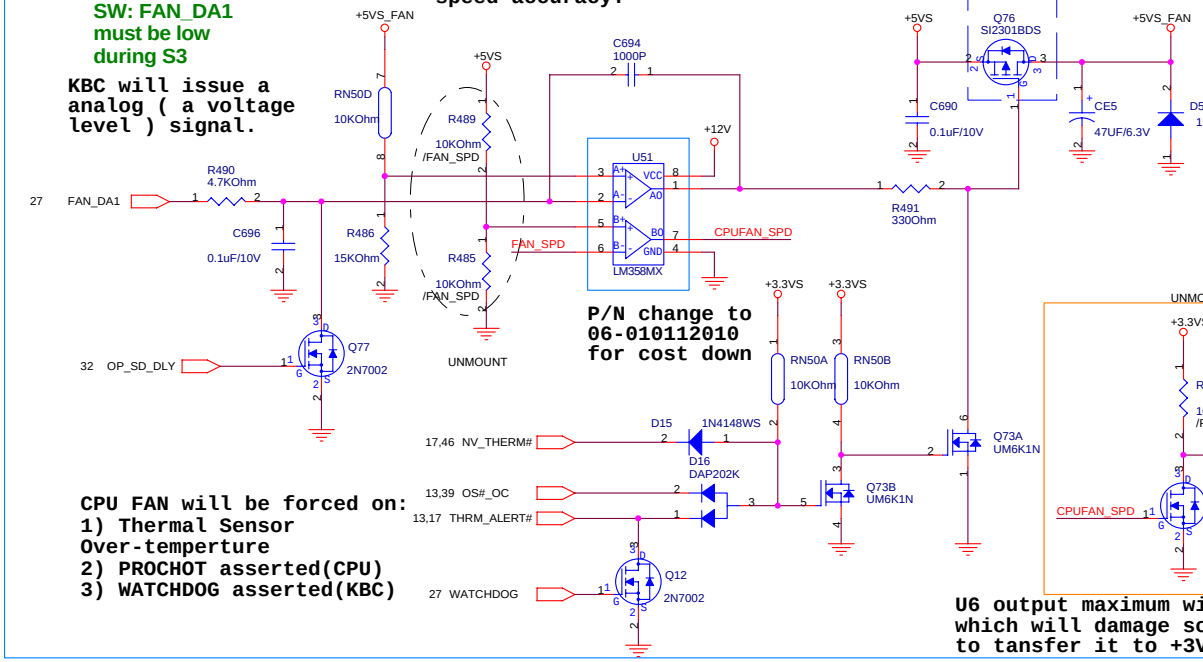
Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

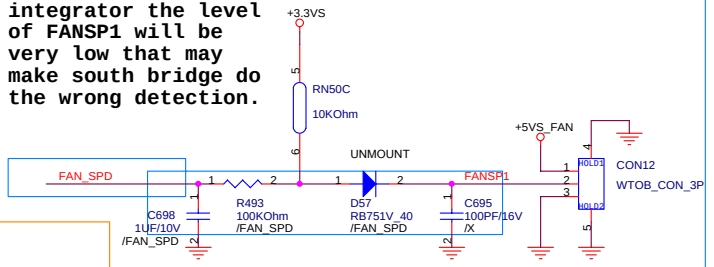
SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.

R2.0 0324-05'

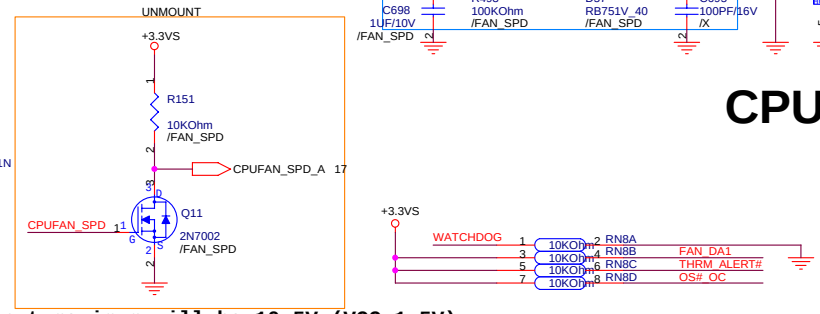


When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



CPU FAN

CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

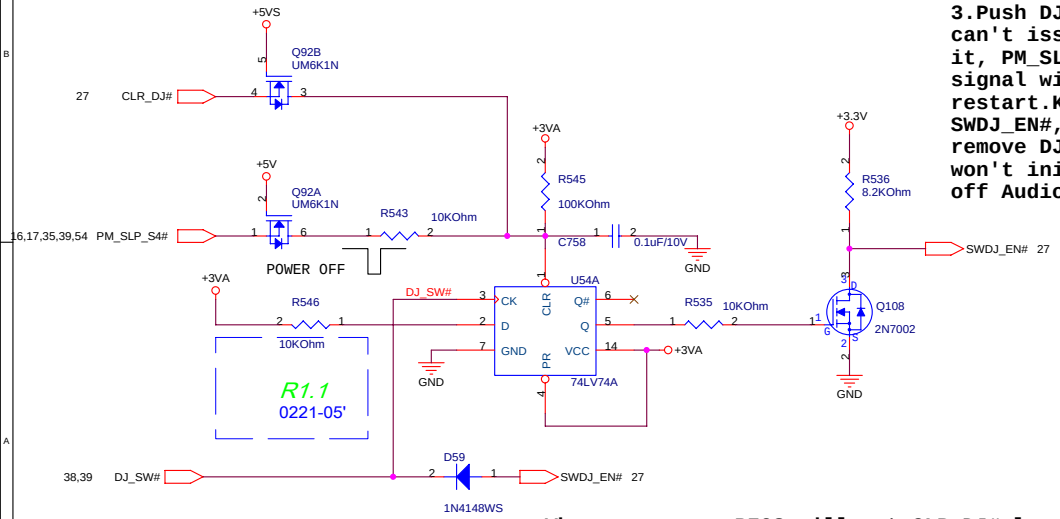


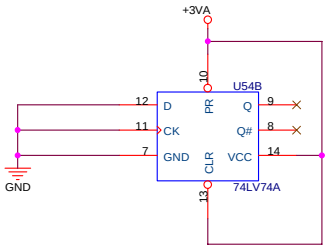
U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

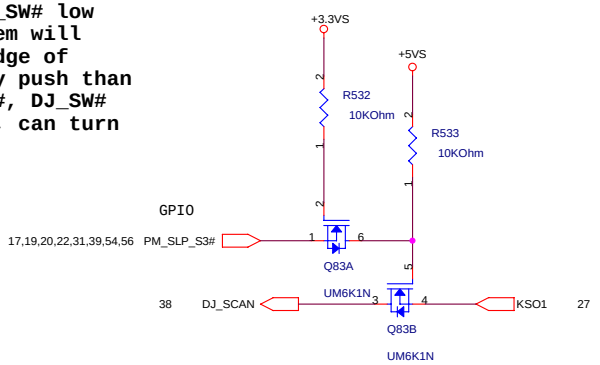
SWAP FOR LAYOUT

Audio DJ

SWDJ_EN# function :
1.Push DJ_SW#, turn on Audio DJ.
2.PM_SLP_S4# will keep high.
3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.

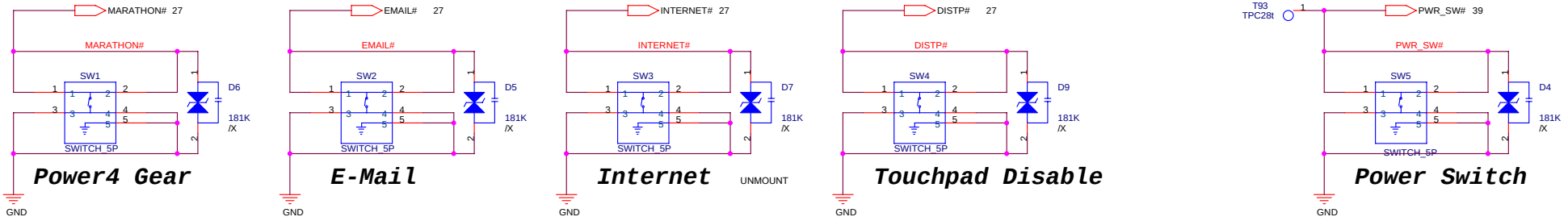


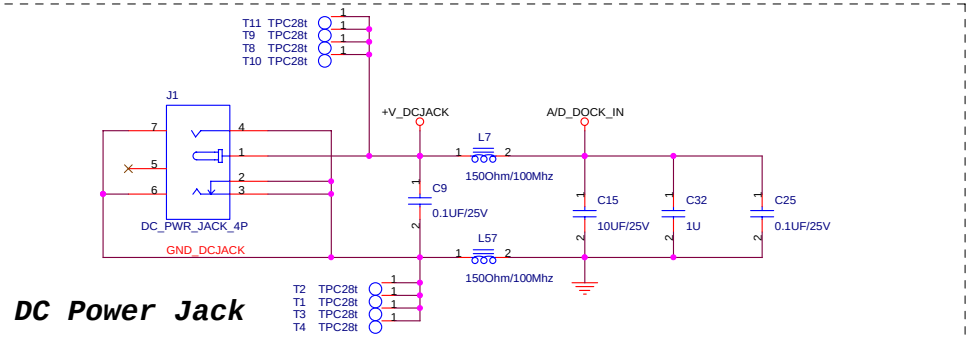


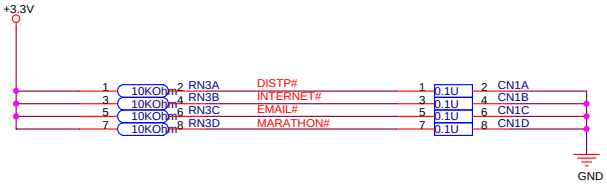


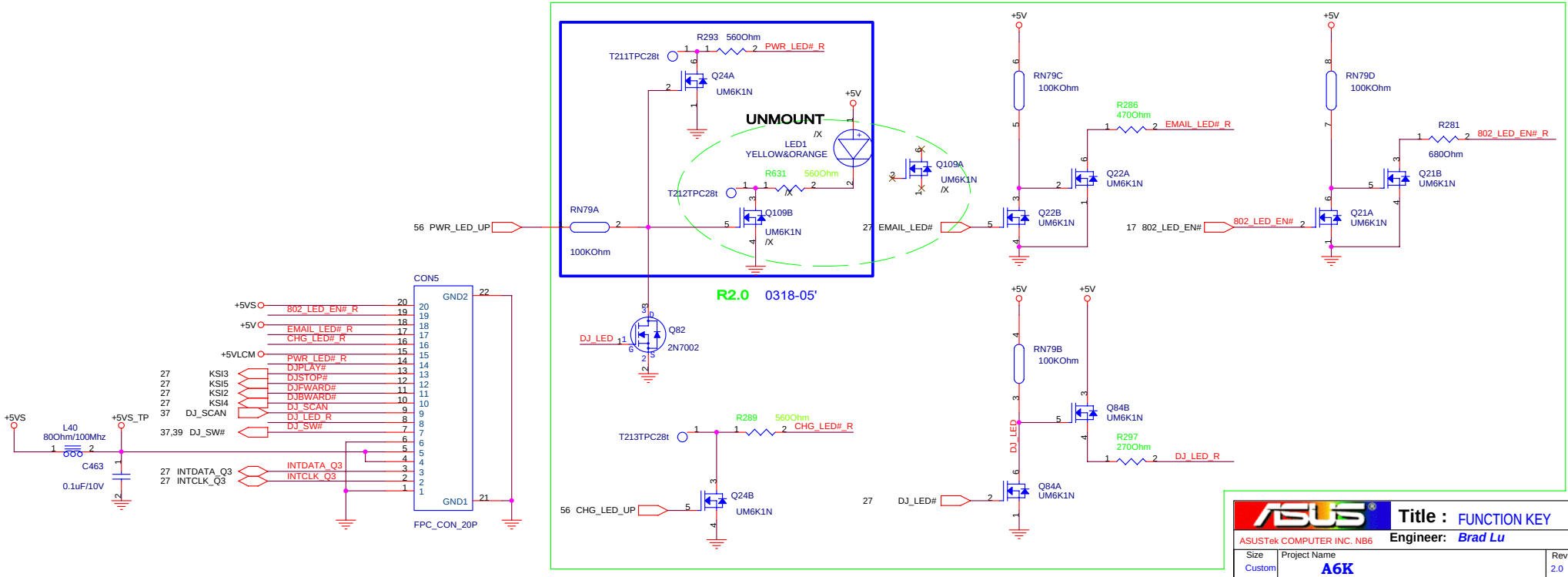
When power on, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D34 to Enable AudioDJ in OS.
Use D34 to Turn off AudioDJ when system be turned on in DJ mode.

ASUSTek COMPUTER INC. NB6	Title : FAN&Audio DJ	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 37 of 64	

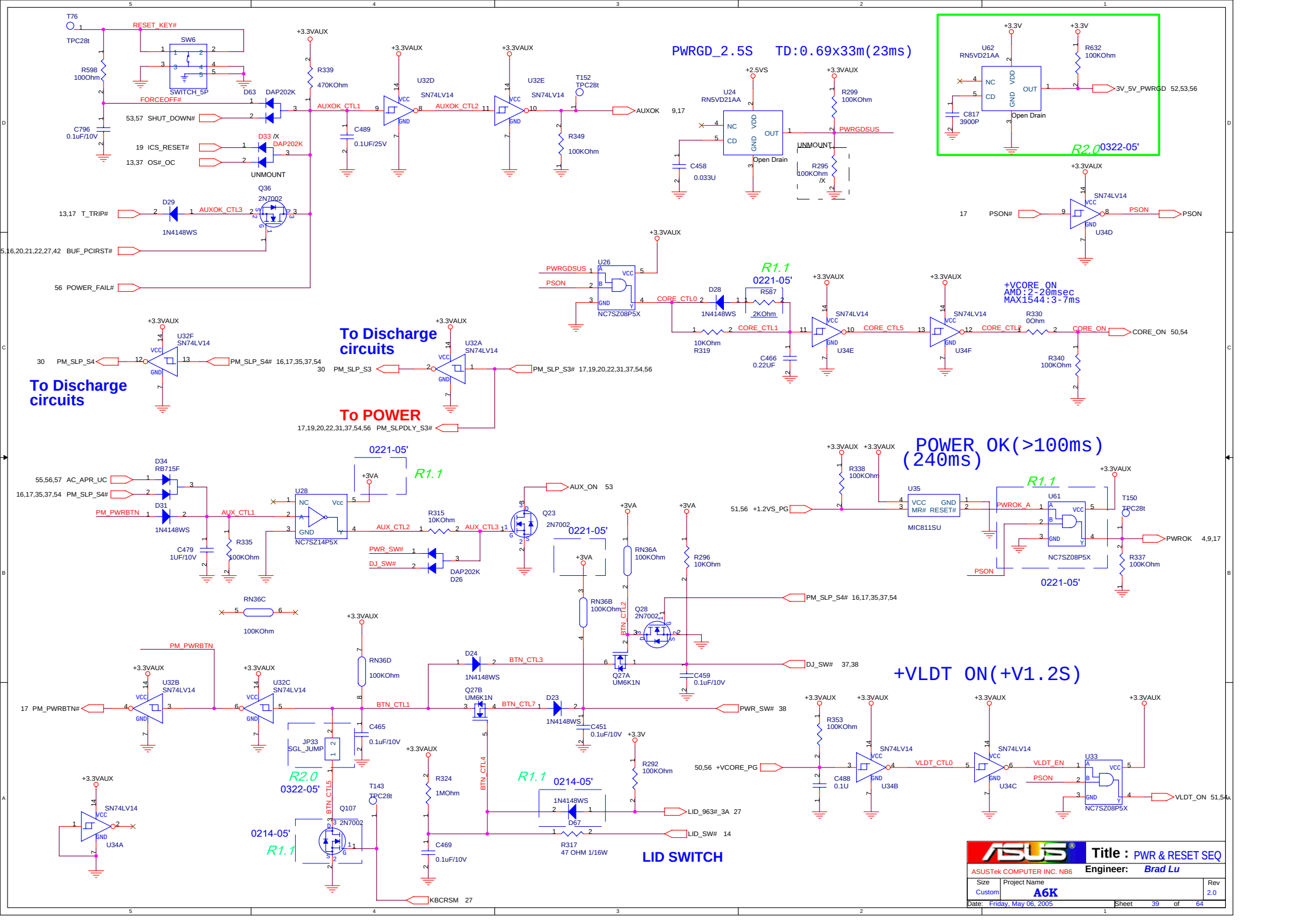


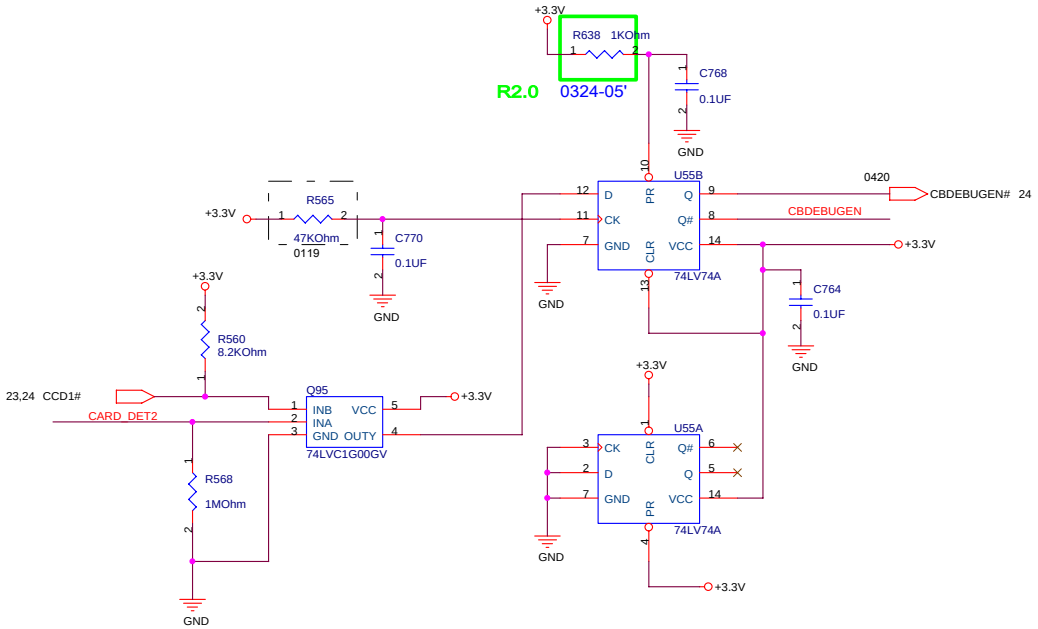






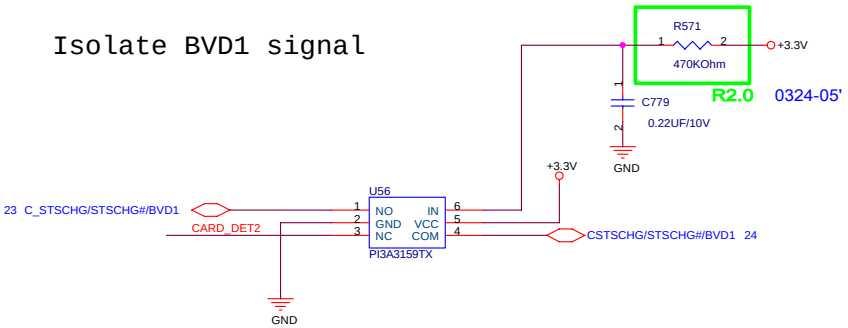
ASUSTek COMPUTER INC. NB6	Title : FUNCTION KEY		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005	Sheet 38 of 64		


PWRGD_2.5S TD:0.69x33m(23ms)
To Discharge circuits
To Discharge circuits
To POWER
+VCORE_ON
AMD:2-20msec
MAX1544:3-7ms
POWER_OK(>100ms)
(240ms)
+VLDT_ON(+V1.2S)
LID SWITCH
R1.1
0221-05'
R2.0
0322-05'
0214-05'
Title : PWR & RESET SEQ
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 39 of 64



RC value may need to tuned for each product.

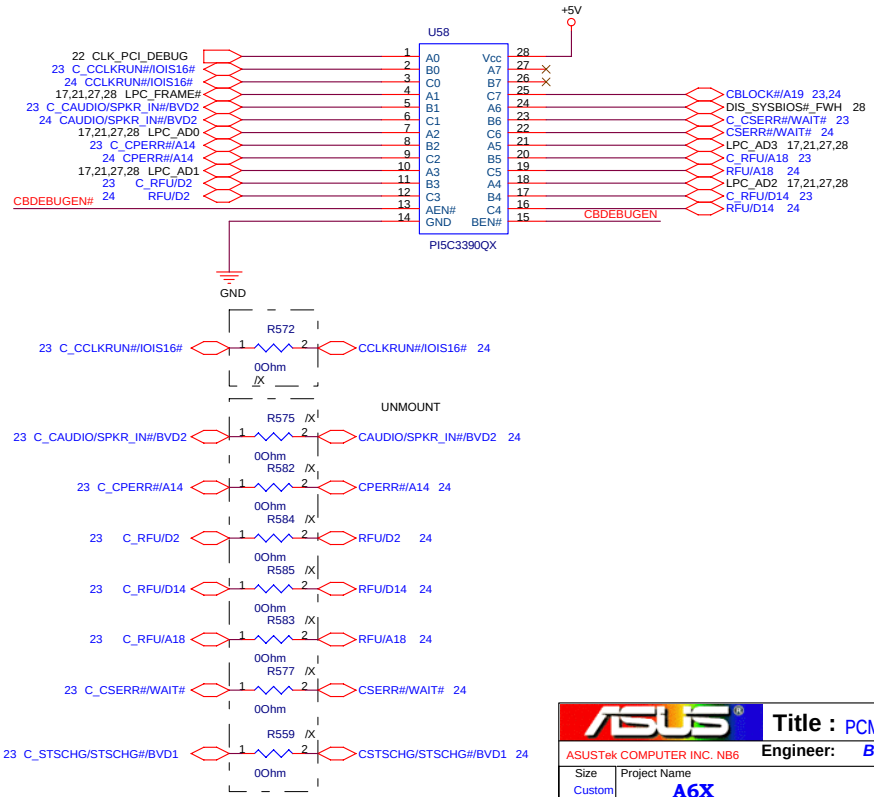
Isolate BVD1 signal



When +3V on, select BVD1 to CARD_DET2 for RC delay time

PCMCIA DEBUG PORT

Isolate card bus control and slot signal when debug card plug in



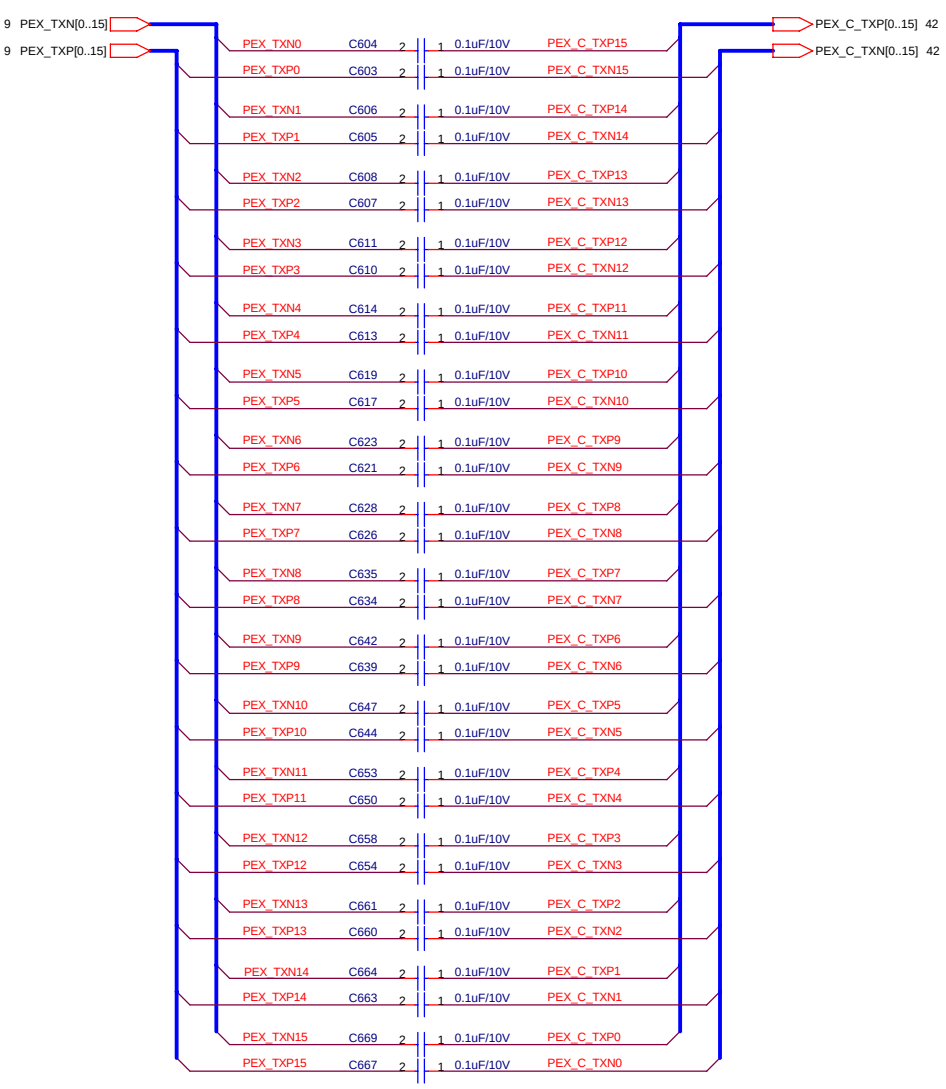
ASUSTek COMPUTER INC. NB6

Title : PCMCIA DEBUG

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6X	2.0

Date: Friday, May 06, 2005 Sheet 40 of 64



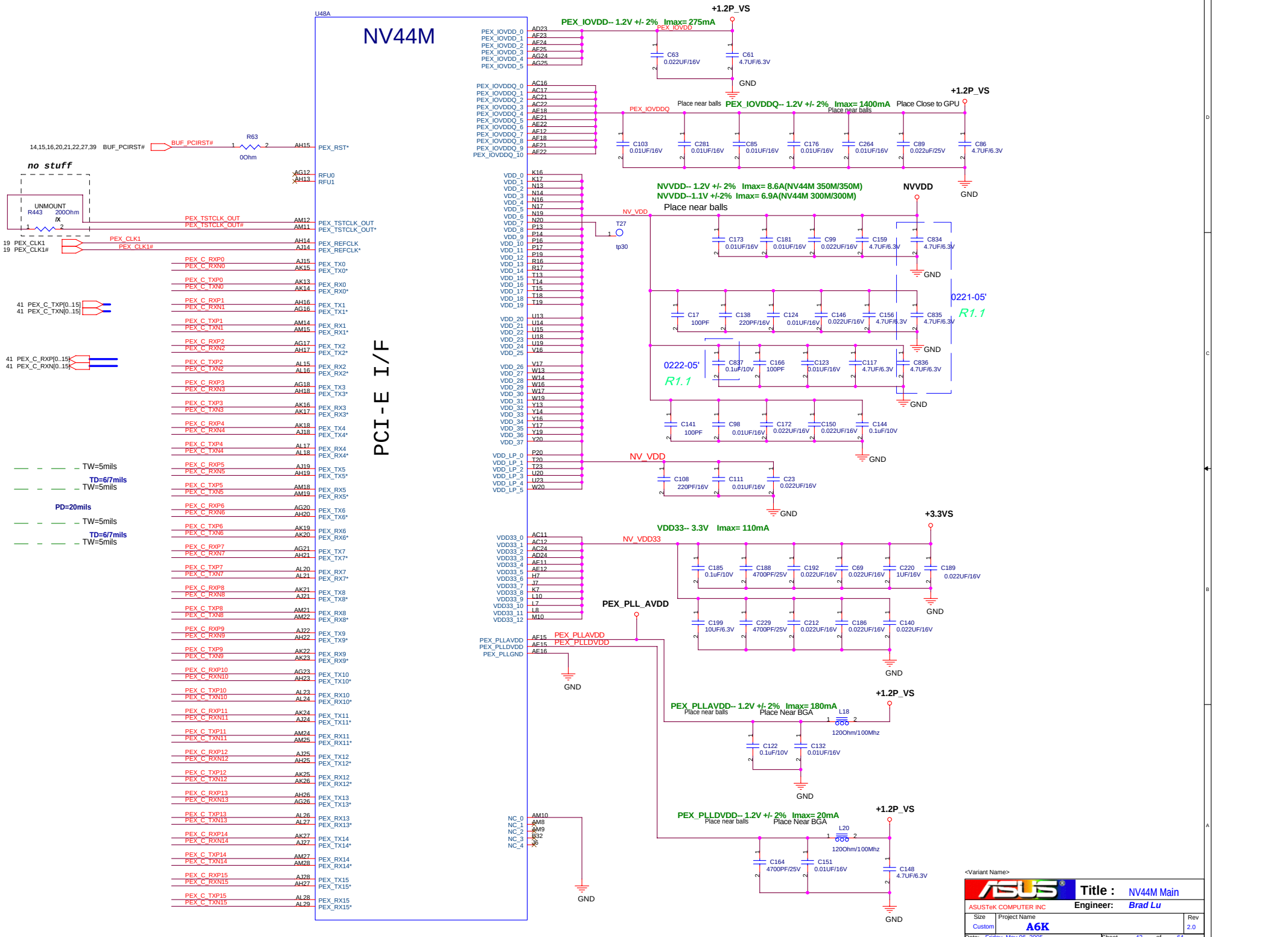
PLACE these 0402 AC coupling caps close to sis756.

TX P&N [0..15] PIN SWAP FOR LAYOUT

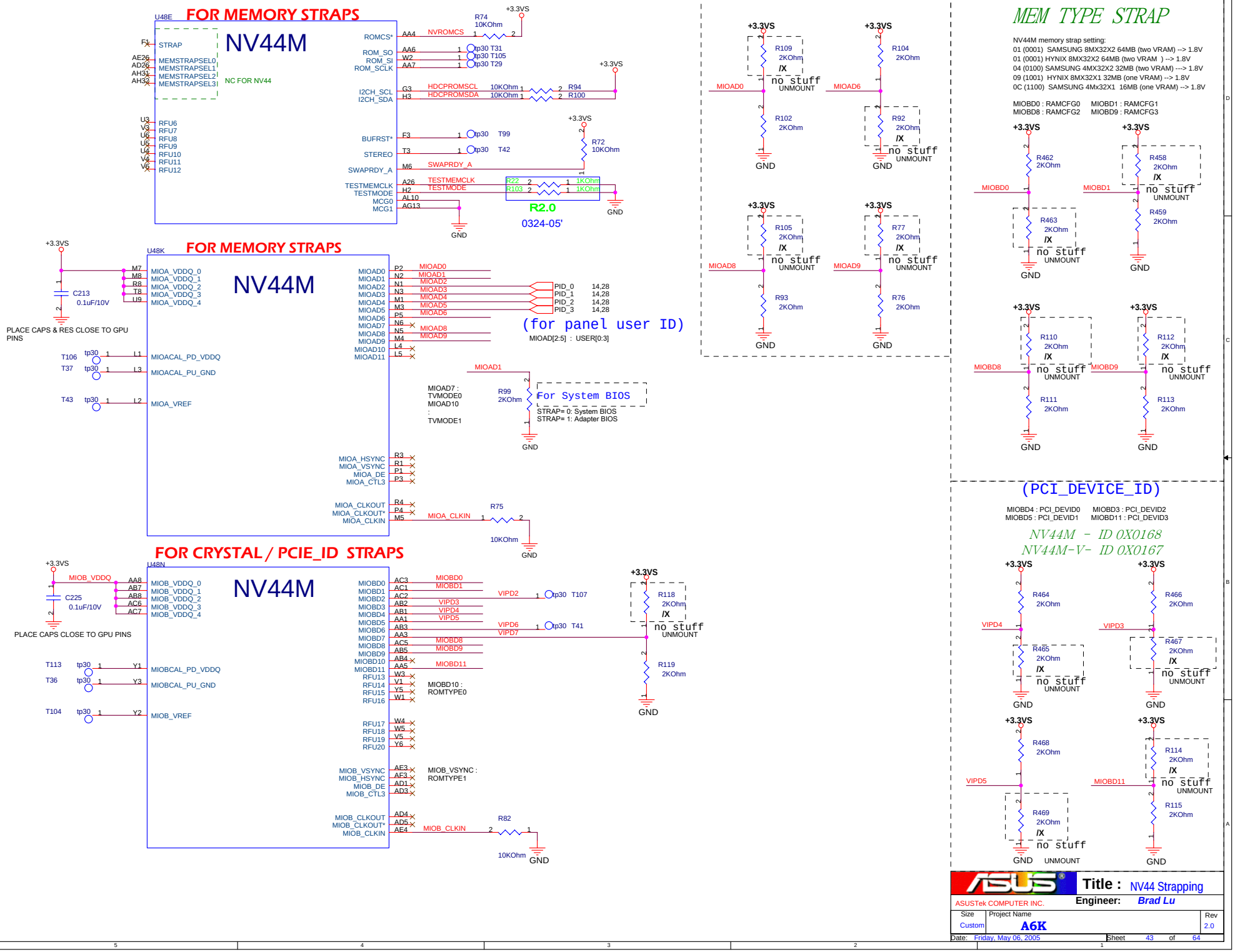
PLACE these 0402 AC coupling caps close to nv44m

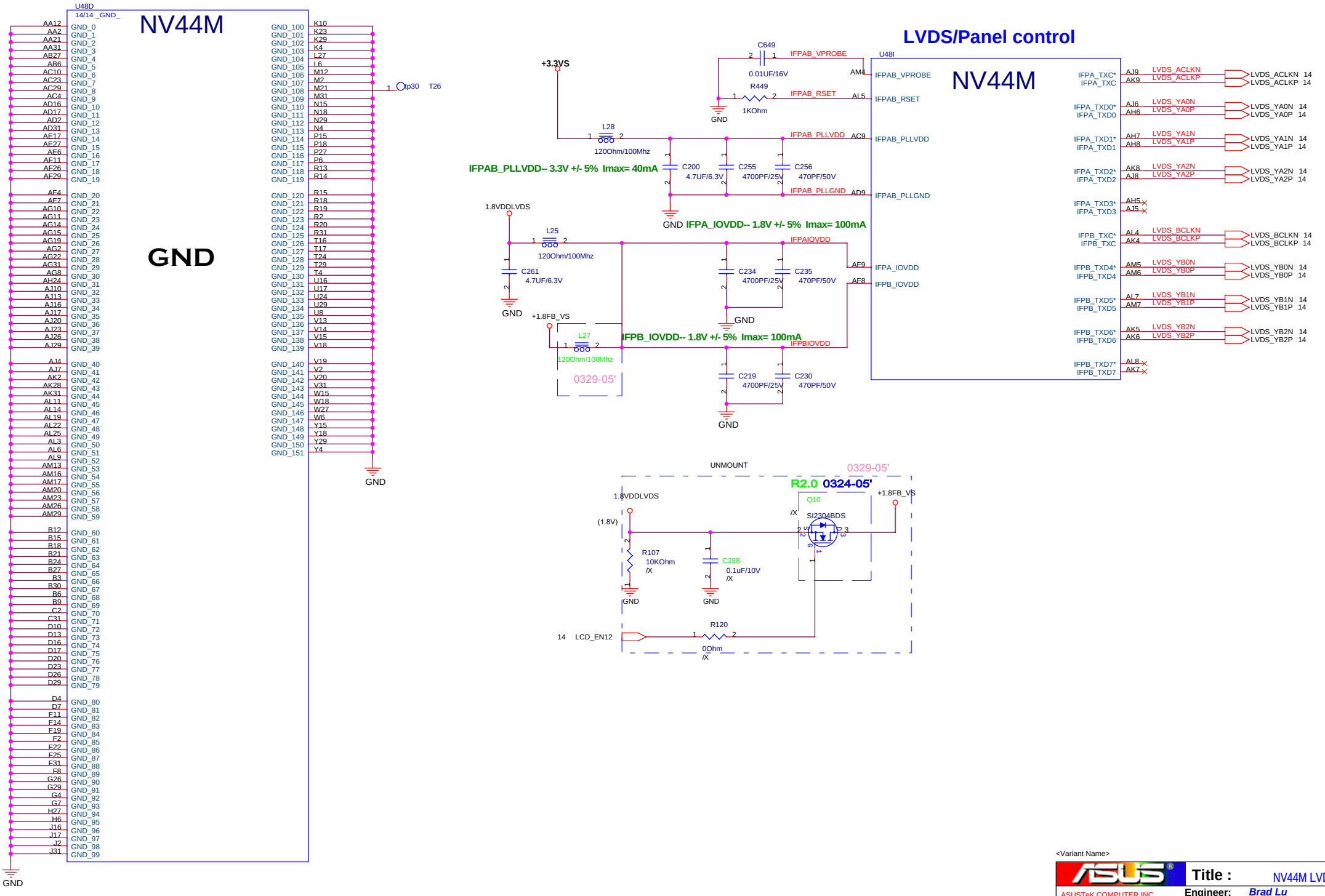
RX P&N 0.2.7.9.11.13.14.15 PIN SWAP FOR LAYOUT

ASUSTeK COMPUTER INC	Title : PCIE AC COUPLE	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 41 of 64	



<Variant Name>
Title : NV44M Main
ASUSTeK COMPUTER INC
Engineer: Brad Lu
Size: Custom
Project Name: A6K
Rev: 2.0
Date: Friday, May 06, 2005
Sheet 42 of 64


FOR MEMORY STRAPS
U48E
NV44M
STRAP
MEMSTRAPSEL0
MEMSTRAPSEL1
MEMSTRAPSEL2
MEMSTRAPSEL3
NC FOR NV44
RFU6
RFU7
RFU8
RFU9
RFU10
RFU11
RFU12
ROMCS*
ROM_SO
ROM_SI
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*
STEREO
SWAPRDY_A
TESTMEMCLK
TESTMODE
MCG0
MCG1
NVROMCS
HDCPROMSCL
HDCPROMSDA
SWAPRDY_A
TESTMEMCLK
TESTMODE
R74 10KOhm
R94 10KOhm
R100 10KOhm
R72 10KOhm
R22 1KOhm
R103 1KOhm
+3.3VS
GND
R2.0
0324-05'
FOR MEMORY STRAPS
U48K
NV44M
C213 0.1uF/10V
PLACE CAPS & RES CLOSE TO GPU PINS
MIOA_VDDQ_0
MIOA_VDDQ_1
MIOA_VDDQ_2
MIOA_VDDQ_3
MIOA_VDDQ_4
MIOACAL_PD_VDDQ
MIOACAL_PU_GND
MIOA_VREF
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11
PID_0 14,28
PID_1 14,28
PID_2 14,28
PID_3 14,28
(for panel user ID)
MIOAD[2:5] : USER[0:3]
MIOAD7 : TVMODE0
MIOAD10 : TVMODE1
R99 2KOhm
For System BIOS
STRAP= 0: System BIOS
STRAP= 1: Adapter BIOS
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CTL3
MIOA_CLKOUT
MIOA_CLKOUT*
MIOA_CLKIN
R75 10KOhm
FOR CRYSTAL / PCIE_ID STRAPS
U48N
NV44M
C225 0.1uF/10V
PLACE CAPS CLOSE TO GPU PINS
MIOB_VDDQ_0
MIOB_VDDQ_1
MIOB_VDDQ_2
MIOB_VDDQ_3
MIOB_VDDQ_4
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
RFU13
RFU14
RFU15
RFU16
RFU17
RFU18
RFU19
RFU20
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_CLKOUT
MIOB_CLKOUT*
MIOB_CLKIN
VIPD2
VIPD3
VIPD4
VIPD5
VIPD6
VIPD7
MIOBD10 : ROMTYPE0
MIOB_VSYNC : ROMTYPE1
R118 2KOhm /X no stuff UNMOUNT
R119 2KOhm
R82 10KOhm
R109 2KOhm /X no stuff UNMOUNT
R102 2KOhm
R104 2KOhm
R92 2KOhm /X no stuff UNMOUNT
R105 2KOhm /X no stuff UNMOUNT
R93 2KOhm
R77 2KOhm /X no stuff UNMOUNT
R76 2KOhm
MEM TYPE STRAP
NV44M memory strap setting:
01 (0001) SAMSUNG 8MX32X2 64MB (two VRAM) --> 1.8V
01 (0001) HYNIX 8MX32X2 64MB (two VRAM) --> 1.8V
04 (0100) SAMSUNG 4MX32X2 32MB (two VRAM) --> 1.8V
09 (1001) HYNIX 8MX32X1 32MB (one VRAM) --> 1.8V
0C (1100) SAMSUNG 4Mx32X1 16MB (one VRAM) --> 1.8V
MIOBD0 : RAMCFG0
MIOBD1 : RAMCFG1
MIOBD8 : RAMCFG2
MIOBD9 : RAMCFG3
R462 2KOhm
R463 2KOhm /X no stuff UNMOUNT
R458 2KOhm /X no stuff UNMOUNT
R459 2KOhm
R110 2KOhm /X no stuff UNMOUNT
R111 2KOhm
R112 2KOhm /X no stuff UNMOUNT
R113 2KOhm
(PCI_DEVICE_ID)
MIOBD4 : PCI_DEVID0
MIOBD3 : PCI_DEVID2
MIOBD5 : PCI_DEVID1
MIOBD11 : PCI_DEVID3
NV44M - ID 0X0168
NV44M-V- ID 0X0167
R464 2KOhm
R465 2KOhm /X no stuff UNMOUNT
R466 2KOhm
R467 2KOhm /X no stuff UNMOUNT
R468 2KOhm
R469 2KOhm /X no stuff UNMOUNT
R114 2KOhm /X no stuff UNMOUNT
R115 2KOhm
Title : NV44 Strapping
ASUSTek COMPUTER INC.
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 43 of 64


U48D
14/14 _GND_
NV44M
GND
LVDS/Panel control
U48I
NV44M
+3.3VS
C649
0.01UF/16V
IFPAB_VPROBE
R449
1KOhm
IFPAB_RSET
GND
L28
120Ohm/100Mhz
IFPAB_PLLVDD
C200
4.7UF/6.3V
C255
4700PF/25V
C256
470PF/50V
IFPAB_PLLVDD-- 3.3V +/- 5% Imax= 40mA
IFPAB_PLLGND
GND
IFPA_IOVDD-- 1.8V +/- 5% Imax= 100mA
1.8VDDLVDS
L25
120Ohm/100Mhz
IFPAIOVDD
C261
4.7UF/6.3V
C234
4700PF/25V
C235
470PF/50V
IFPA_IOVDD
IFPB_IOVDD
+1.8FB_VS
L27
120Ohm/100Mhz
IFPB_IOVDD-- 1.8V +/- 5% Imax= 100mA
IFPBIOVDD
0329-05'
C219
4700PF/25V
C230
470PF/50V
UNMOUNT
0329-05'
R2.0 0324-05'
1.8VDDLVDS
(1.8V)
Q10
SI2304BDS
/X
R107
10KOhm
/X
C288
0.1uF/10V
/X
+1.8FB_VS
R120
0Ohm
/X
14 LCD_EN12
IFPA_TXC*
IFPA_TXC
IFPA_TXD0*
IFPA_TXD0
IFPA_TXD1*
IFPA_TXD1
IFPA_TXD2*
IFPA_TXD2
IFPA_TXD3*
IFPA_TXD3
IFPB_TXC*
IFPB_TXC
IFPB_TXD4*
IFPB_TXD4
IFPB_TXD5*
IFPB_TXD5
IFPB_TXD6*
IFPB_TXD6
IFPB_TXD7*
IFPB_TXD7
LVDS_ACLKN
LVDS_ACLKP
LVDS_YA0N
LVDS_YA0P
LVDS_YA1N
LVDS_YA1P
LVDS_YA2N
LVDS_YA2P
LVDS_BCLKN
LVDS_BCLKP
LVDS_YB0N
LVDS_YB0P
LVDS_YB1N
LVDS_YB1P
LVDS_YB2N
LVDS_YB2P
tp30 T26
<Variant Name>
Title : NV44M LVDS
ASUSTeK COMPUTER INC
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
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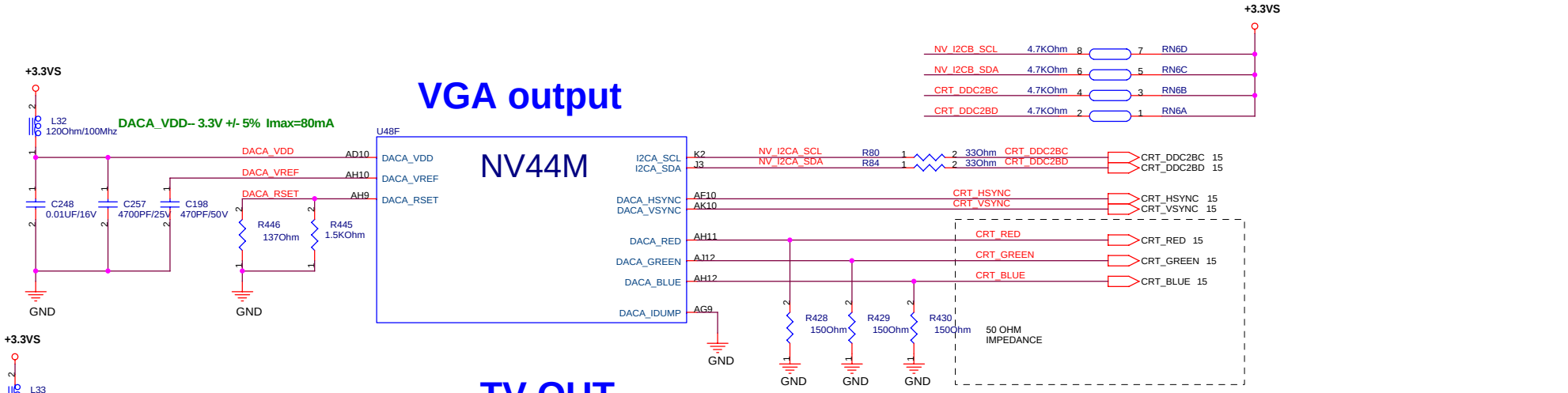
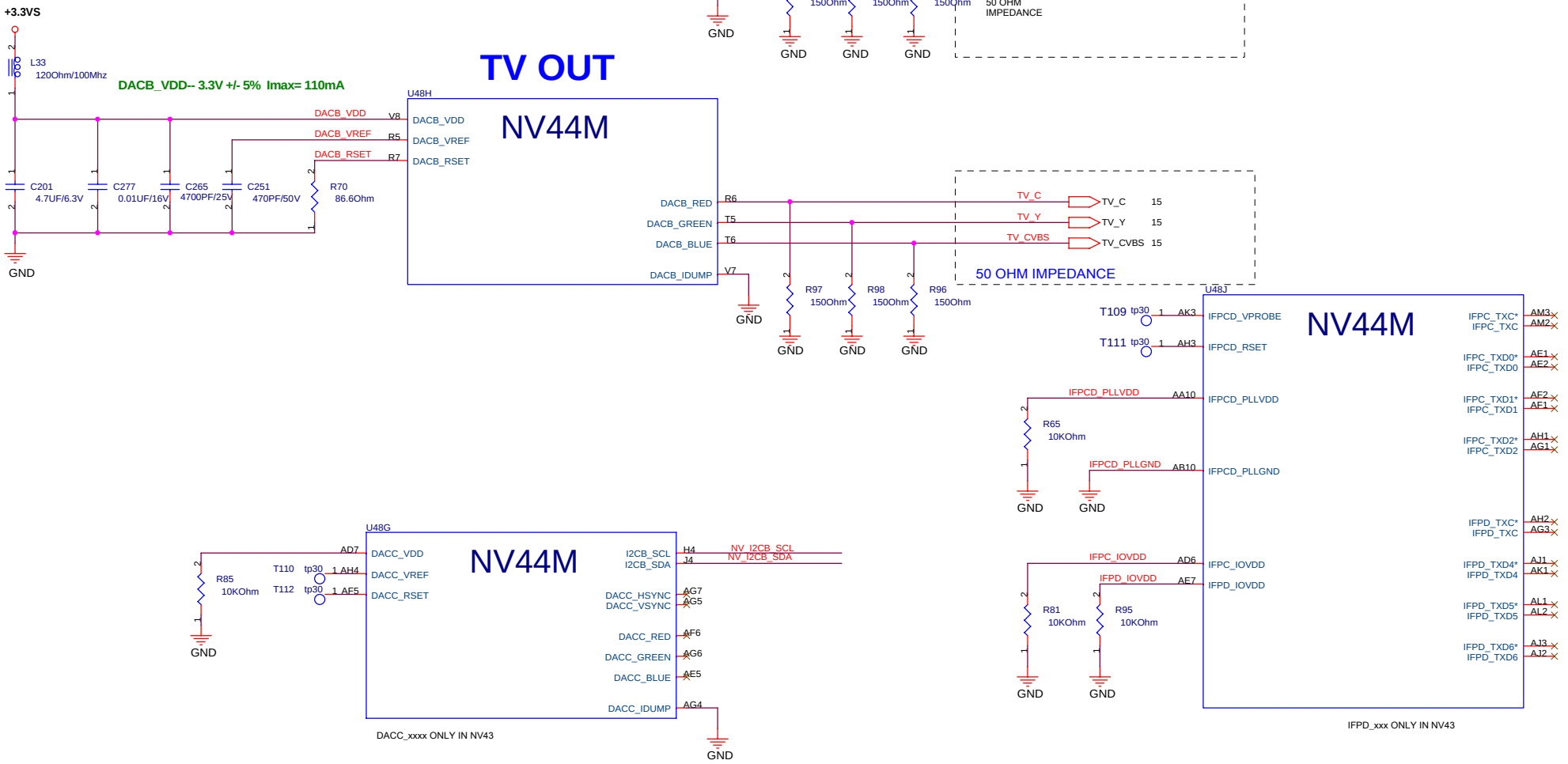
VGA output



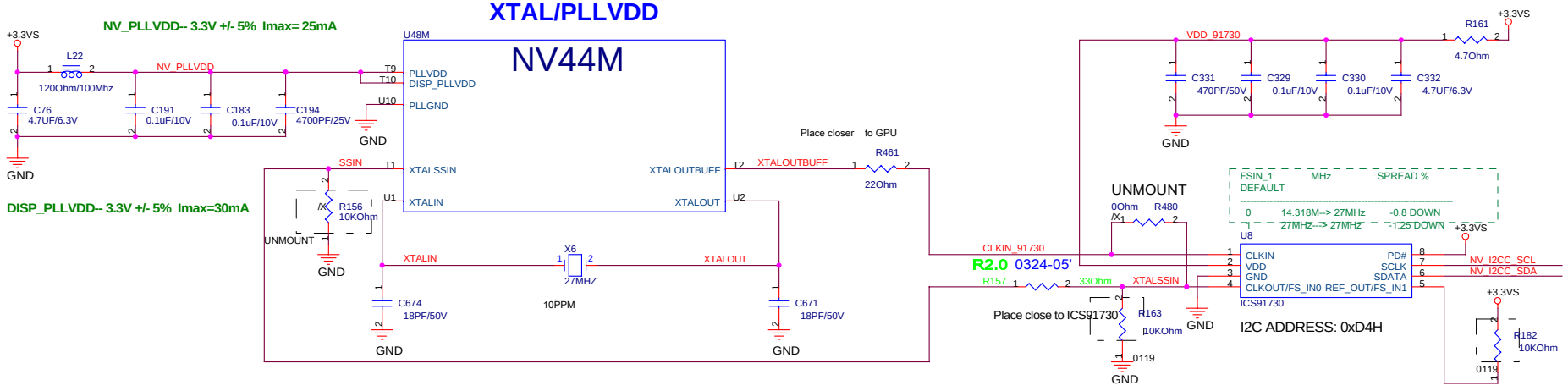
TV OUT

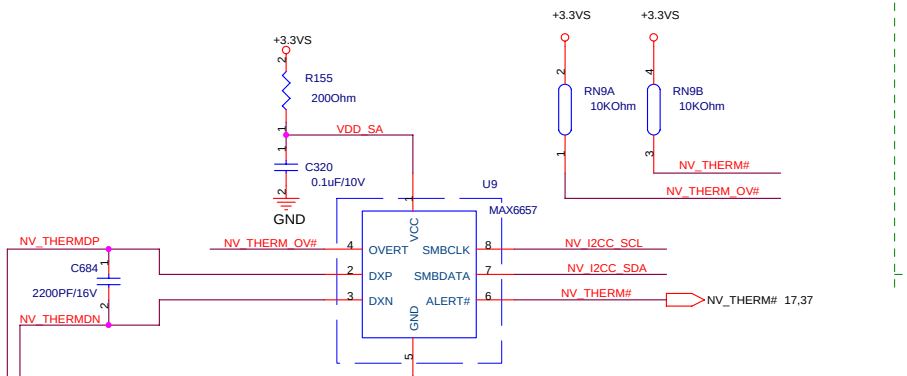


<Variant Name>

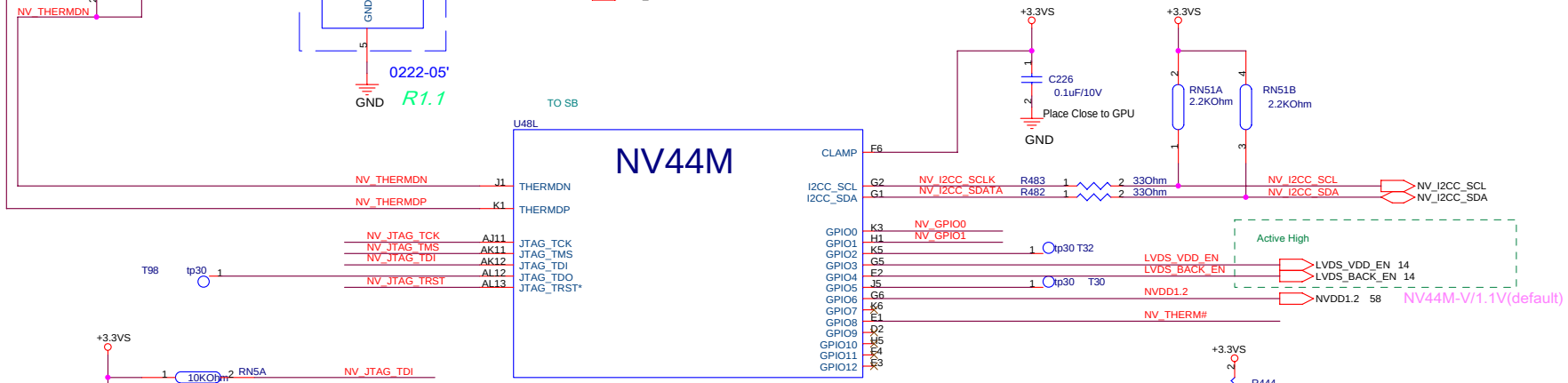
ASUSTeK COMPUTER INC	Title : MV44 VGA/TV Out	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 45 of 64	

XTAL/PLLVDD





GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOT PLUG
1	IN	N/A	2ND DVI HOT PLUG
2	OUT	HIGH	BACKLIGHT BRIGHTNESS
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID0
6	OUT	HIGH	NVVDD VID1
7	OUT	HIGH	FBVDD VID0
8	IN	LOW	THERMAL SHUTDOWN
9	OUT	LOW	FAN PWM



GPIO & JTAG

<variant_name>

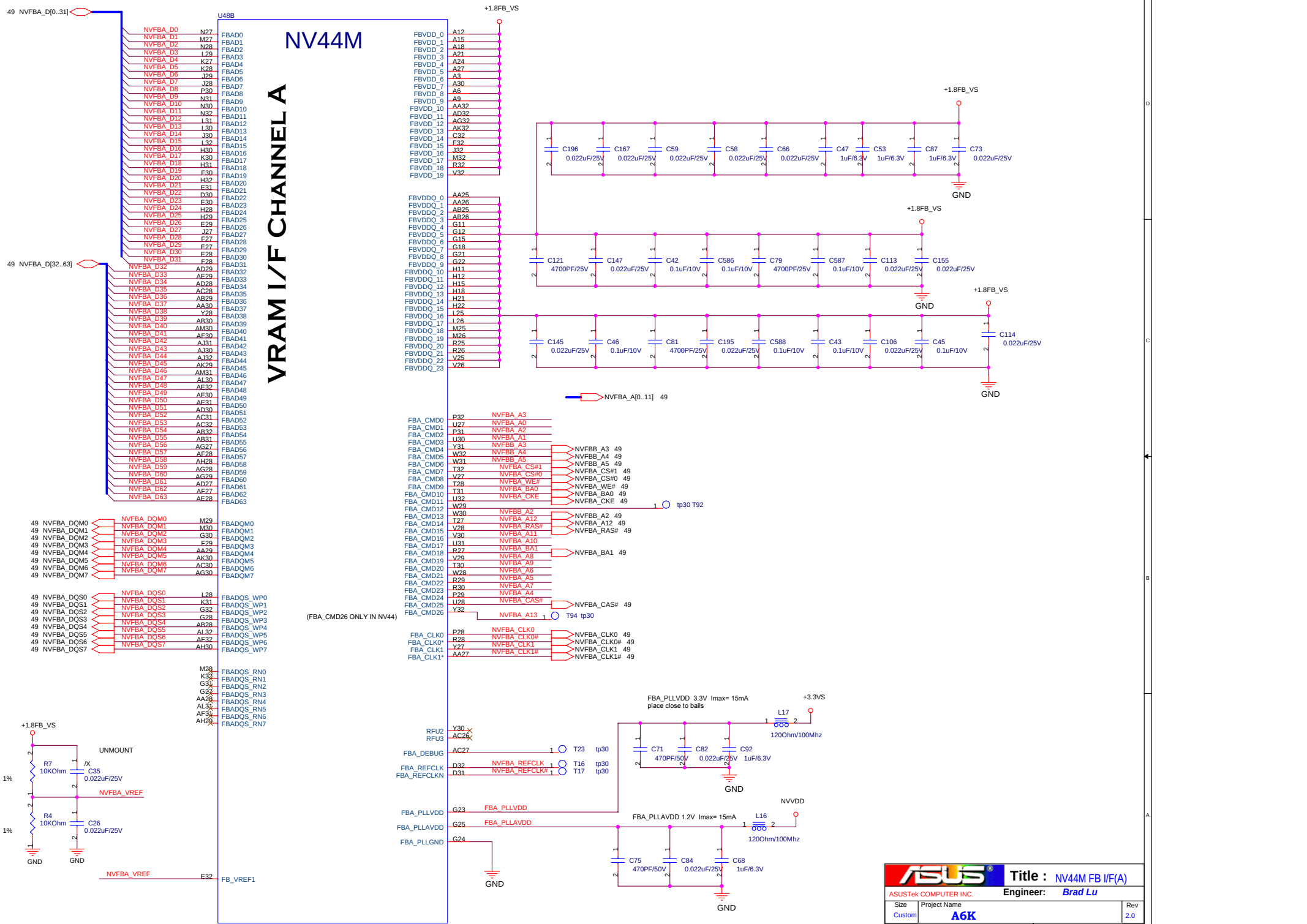
ASUSTeK COMPUTER INC

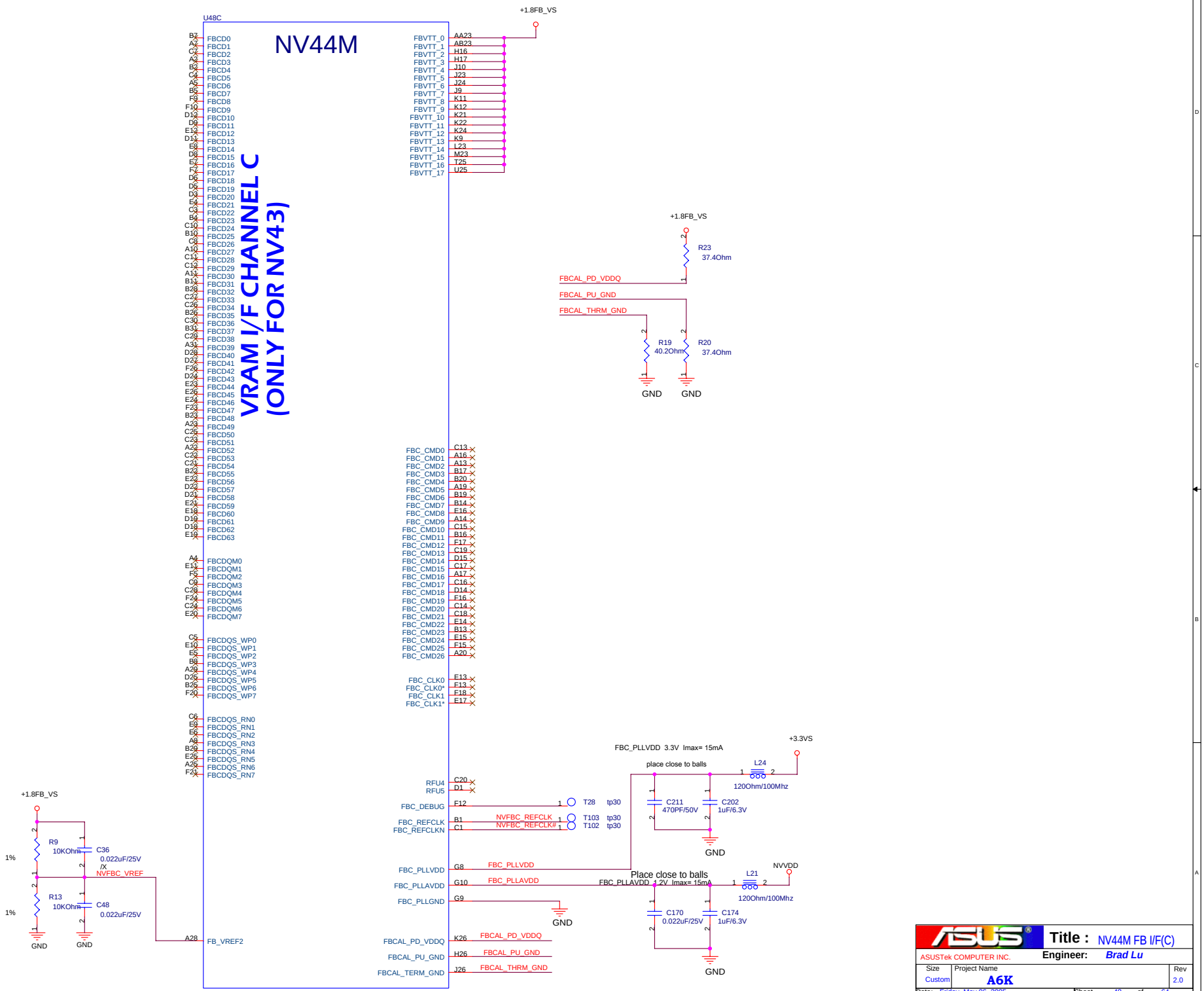
Title : NV Spread Spectrum

Engineer: Brad Lu

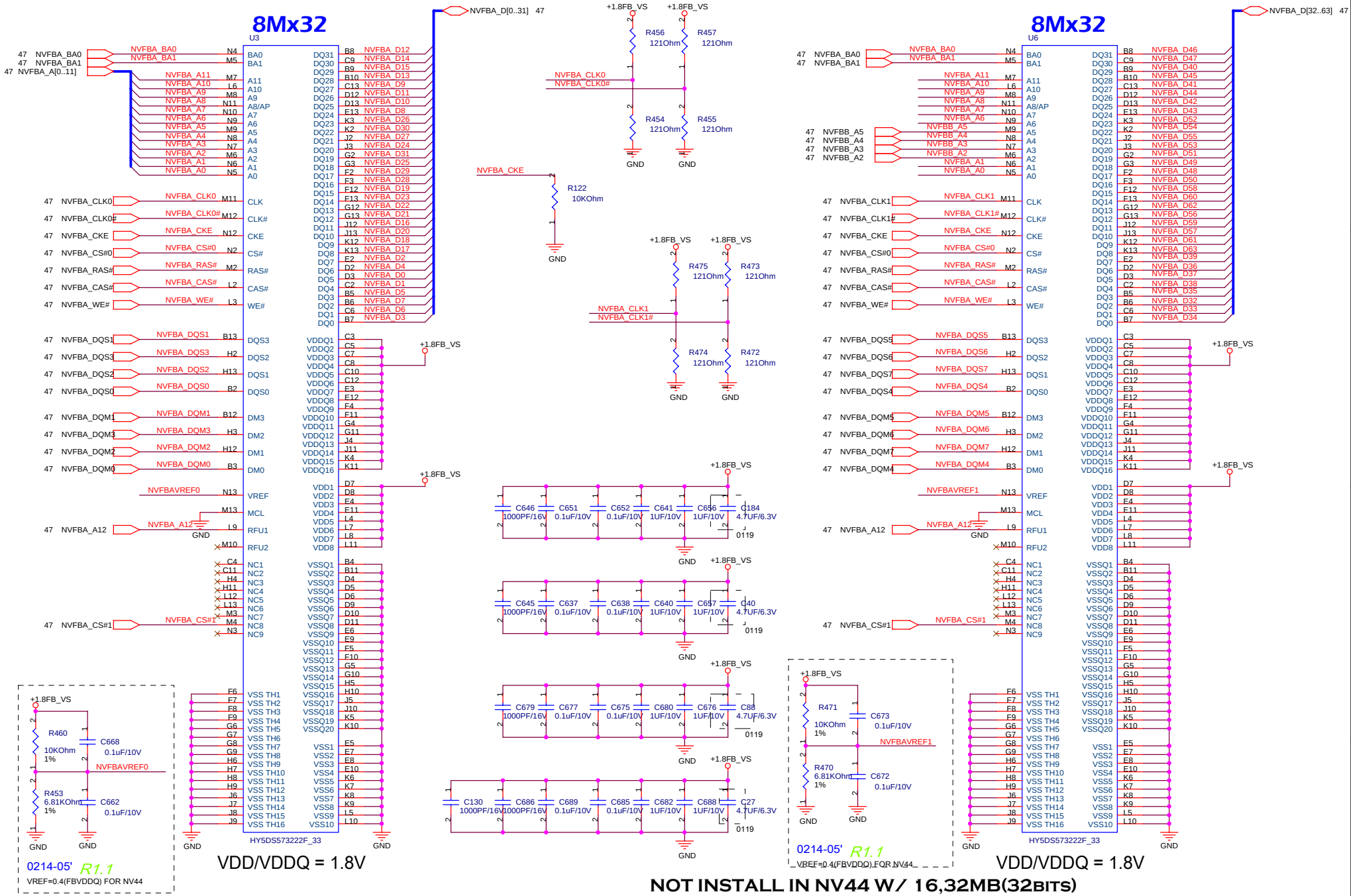
Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 46 of 64


NV44M
VRAM I/F CHANNEL A
U48B
49 NVFBA_D[0..31]
49 NVFBA_D[32..63]
NVFBA_D0
NVFBA_D1
NVFBA_D2
NVFBA_D3
NVFBA_D4
NVFBA_D5
NVFBA_D6
NVFBA_D7
NVFBA_D8
NVFBA_D9
NVFBA_D10
NVFBA_D11
NVFBA_D12
NVFBA_D13
NVFBA_D14
NVFBA_D15
NVFBA_D16
NVFBA_D17
NVFBA_D18
NVFBA_D19
NVFBA_D20
NVFBA_D21
NVFBA_D22
NVFBA_D23
NVFBA_D24
NVFBA_D25
NVFBA_D26
NVFBA_D27
NVFBA_D28
NVFBA_D29
NVFBA_D30
NVFBA_D31
NVFBA_D32
NVFBA_D33
NVFBA_D34
NVFBA_D35
NVFBA_D36
NVFBA_D37
NVFBA_D38
NVFBA_D39
NVFBA_D40
NVFBA_D41
NVFBA_D42
NVFBA_D43
NVFBA_D44
NVFBA_D45
NVFBA_D46
NVFBA_D47
NVFBA_D48
NVFBA_D49
NVFBA_D50
NVFBA_D51
NVFBA_D52
NVFBA_D53
NVFBA_D54
NVFBA_D55
NVFBA_D56
NVFBA_D57
NVFBA_D58
NVFBA_D59
NVFBA_D60
NVFBA_D61
NVFBA_D62
NVFBA_D63
FBAD0
FBAD1
FBAD2
FBAD3
FBAD4
FBAD5
FBAD6
FBAD7
FBAD8
FBAD9
FBAD10
FBAD11
FBAD12
FBAD13
FBAD14
FBAD15
FBAD16
FBAD17
FBAD18
FBAD19
FBAD20
FBAD21
FBAD22
FBAD23
FBAD24
FBAD25
FBAD26
FBAD27
FBAD28
FBAD29
FBAD30
FBAD31
FBAD32
FBAD33
FBAD34
FBAD35
FBAD36
FBAD37
FBAD38
FBAD39
FBAD40
FBAD41
FBAD42
FBAD43
FBAD44
FBAD45
FBAD46
FBAD47
FBAD48
FBAD49
FBAD50
FBAD51
FBAD52
FBAD53
FBAD54
FBAD55
FBAD56
FBAD57
FBAD58
FBAD59
FBAD60
FBAD61
FBAD62
FBAD63
+1.8FB_VS
FBVDD_0
FBVDD_1
FBVDD_2
FBVDD_3
FBVDD_4
FBVDD_5
FBVDD_6
FBVDD_7
FBVDD_8
FBVDD_9
FBVDD_10
FBVDD_11
FBVDD_12
FBVDD_13
FBVDD_14
FBVDD_15
FBVDD_16
FBVDD_17
FBVDD_18
FBVDD_19
FBVDDQ_0
FBVDDQ_1
FBVDDQ_2
FBVDDQ_3
FBVDDQ_4
FBVDDQ_5
FBVDDQ_6
FBVDDQ_7
FBVDDQ_8
FBVDDQ_9
FBVDDQ_10
FBVDDQ_11
FBVDDQ_12
FBVDDQ_13
FBVDDQ_14
FBVDDQ_15
FBVDDQ_16
FBVDDQ_17
FBVDDQ_18
FBVDDQ_19
FBVDDQ_20
FBVDDQ_21
FBVDDQ_22
FBVDDQ_23
C196 0.022uF/25V
C167 0.022uF/25V
C59 0.022uF/25V
C58 0.022uF/25V
C66 0.022uF/25V
C47 1uF/6.3V
C53 1uF/6.3V
C87 1uF/6.3V
C73 0.022uF/25V
GND
C121 4700PF/25V
C147 0.022uF/25V
C42 0.1uF/10V
C586 0.1uF/10V
C79 4700PF/25V
C587 0.1uF/10V
C113 0.022uF/25V
C155 0.022uF/25V
C145 0.022uF/25V
C46 0.1uF/10V
C81 4700PF/25V
C195 0.022uF/25V
C588 0.1uF/10V
C43 0.1uF/10V
C106 0.022uF/25V
C45 0.1uF/10V
C114 0.022uF/25V
NVFBA_A[0..11] 49
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
(FBA_CMD26 ONLY IN NV44)
NVFBA_A3
NVFBA_A0
NVFBA_A2
NVFBA_A1
NVFBB_A3
NVFBB_A4
NVFBB_A5
NVFBA_CS#1
NVFBA_CS#0
NVFBA_WE#
NVFBA_BA0
NVFBA_CKE
NVFBB_A2
NVFBA_A12
NVFBA_RAS#
NVFBA_A11
NVFBA_A10
NVFBA_BA1
NVFBA_A8
NVFBA_A9
NVFBA_A6
NVFBA_A5
NVFBA_A7
NVFBA_A4
NVFBA_CAS#
NVFBA_A13
NVFBB_A3 49
NVFBB_A4 49
NVFBB_A5 49
NVFBA_CS#1 49
NVFBA_CS#0 49
NVFBA_WE# 49
NVFBA_BA0 49
NVFBA_CKE 49
tp30 T92
NVFBB_A2 49
NVFBA_A12 49
NVFBA_RAS# 49
NVFBA_BA1 49
NVFBA_CAS# 49
T94 tp30
FBA_CLK0
FBA_CLK0*
FBA_CLK1
FBA_CLK1*
NVFBA_CLK0
NVFBA_CLK0#
NVFBA_CLK1
NVFBA_CLK1#
NVFBA_CLK0 49
NVFBA_CLK0# 49
NVFBA_CLK1 49
NVFBA_CLK1# 49
49 NVFBA_DQM0
49 NVFBA_DQM1
49 NVFBA_DQM2
49 NVFBA_DQM3
49 NVFBA_DQM4
49 NVFBA_DQM5
49 NVFBA_DQM6
49 NVFBA_DQM7
NVFBA_DQM0
NVFBA_DQM1
NVFBA_DQM2
NVFBA_DQM3
NVFBA_DQM4
NVFBA_DQM5
NVFBA_DQM6
NVFBA_DQM7
FBADQM0
FBADQM1
FBADQM2
FBADQM3
FBADQM4
FBADQM5
FBADQM6
FBADQM7
49 NVFBA_DQS0
49 NVFBA_DQS1
49 NVFBA_DQS2
49 NVFBA_DQS3
49 NVFBA_DQS4
49 NVFBA_DQS5
49 NVFBA_DQS6
49 NVFBA_DQS7
NVFBA_DQS0
NVFBA_DQS1
NVFBA_DQS2
NVFBA_DQS3
NVFBA_DQS4
NVFBA_DQS5
NVFBA_DQS6
NVFBA_DQS7
FBADQS_WP0
FBADQS_WP1
FBADQS_WP2
FBADQS_WP3
FBADQS_WP4
FBADQS_WP5
FBADQS_WP6
FBADQS_WP7
FBADQS_RN0
FBADQS_RN1
FBADQS_RN2
FBADQS_RN3
FBADQS_RN4
FBADQS_RN5
FBADQS_RN6
FBADQS_RN7
RFU2
RFU3
FBA_DEBUG
FBA_REFCLK
FBA_REFCLKN
NVFBA_REFCLK
NVFBA_REFCLK#
T23 tp30
T16 tp30
T17 tp30
FBA_PLLVDD
FBA_PLLAVDD
FBA_PLLGND
FBA_PLLVDD 3.3V Imax= 15mA
place close to balls
+3.3VS
L17
120Ohm/100Mhz
C71 470PF/50V
C82 0.022uF/25V
C92 1uF/6.3V
NVVDD
FBA_PLLAVDD 1.2V Imax= 15mA
L16
120Ohm/100Mhz
C75 470PF/50V
C84 0.022uF/25V
C68 1uF/6.3V
+1.8FB_VS
UNMOUNT
R7 10KOhm 1%
C35 0.022uF/25V
R4 10KOhm 1%
C26 0.022uF/25V
NVFBA_VREF
FB_VREF1
Title : NV44M FB I/F(A)
ASUSTek COMPUTER INC.
Engineer: Brad Lu
Size: Custom
Project Name: A6K
Rev: 2.0
Date: Friday, May 06, 2005
Sheet 47 of 64



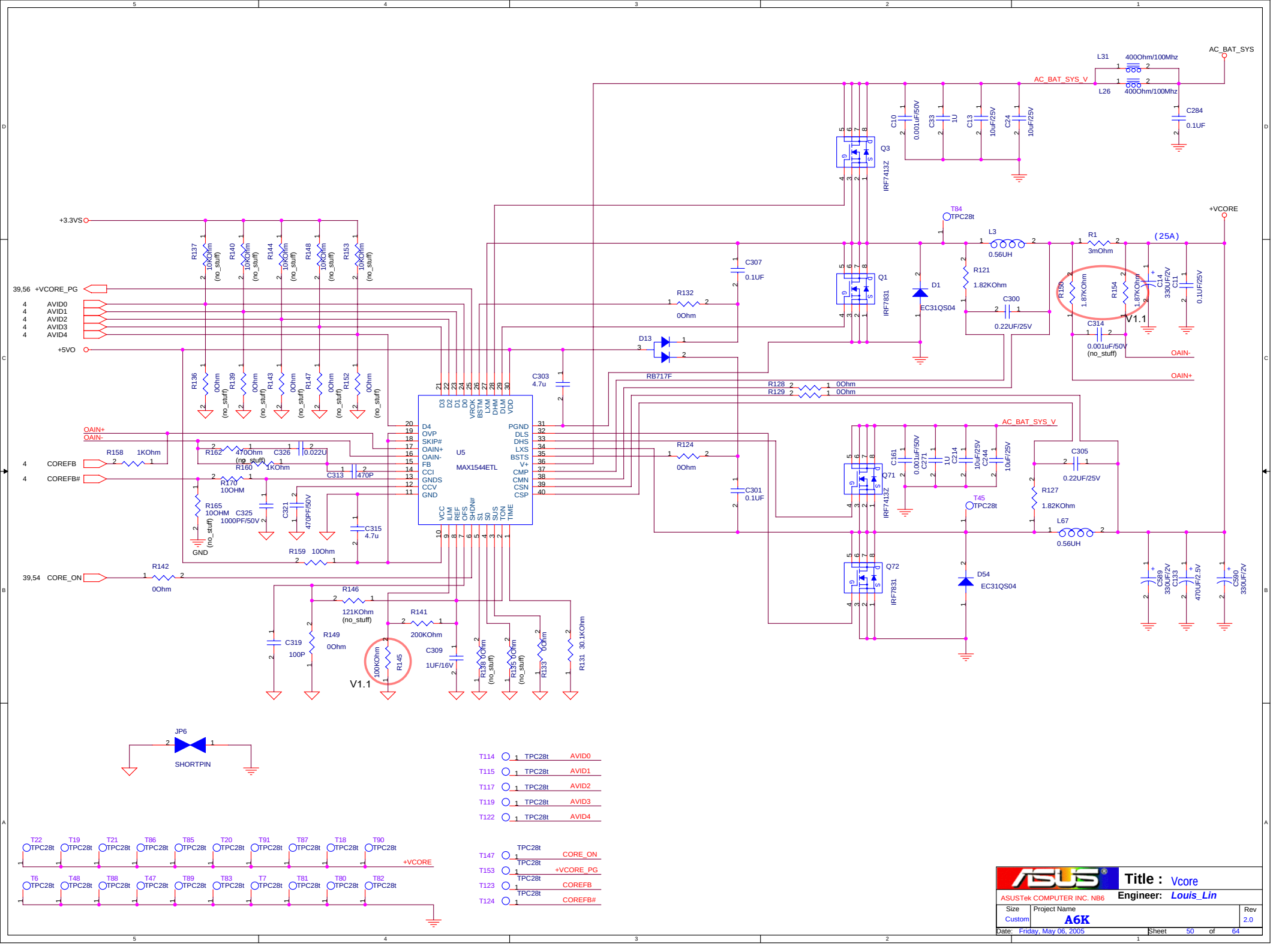
ASUSTek COMPUTER INC.	Title : NV44M FB I/F(C)		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005	Sheet 48 of 64		

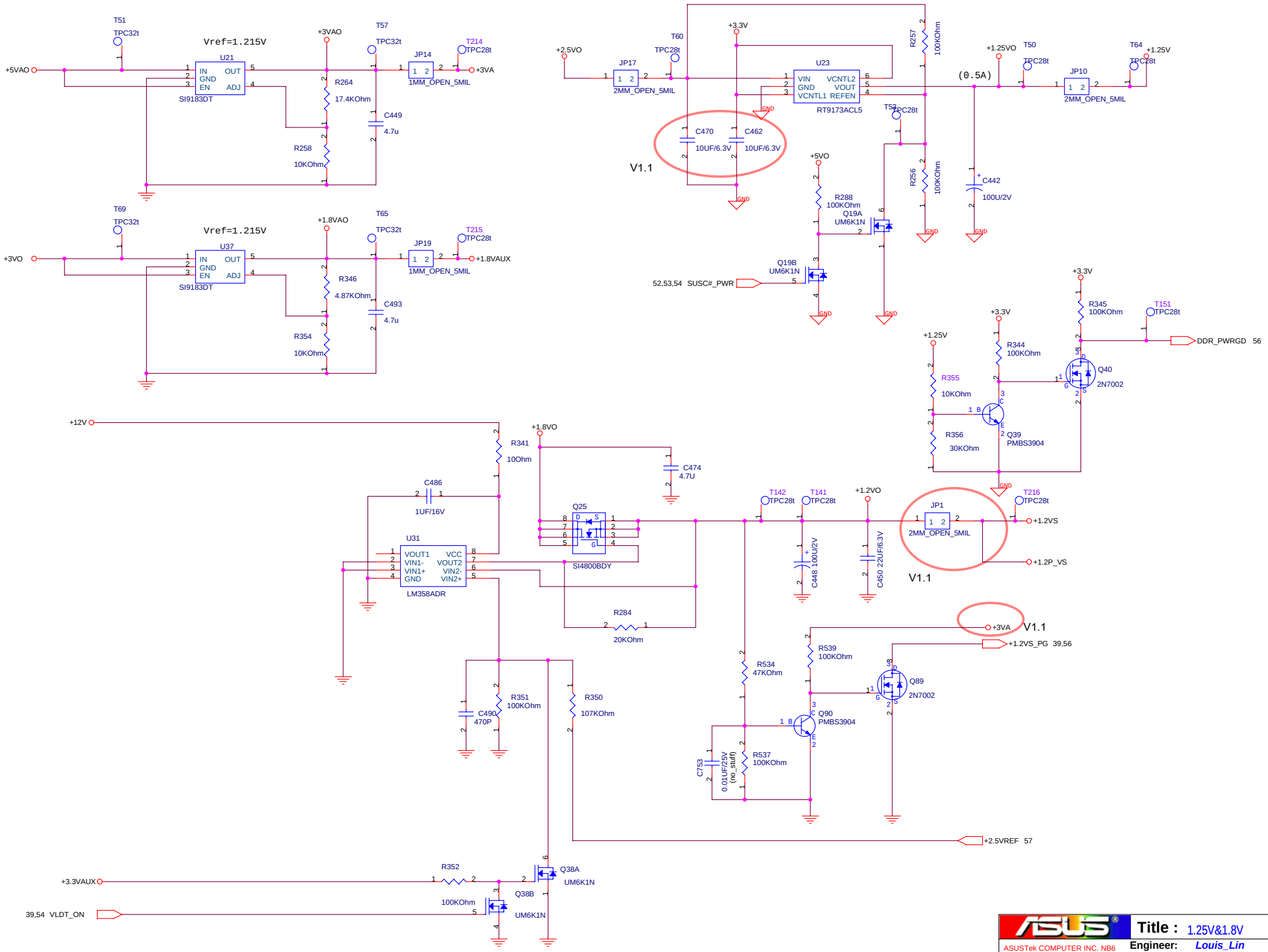


VRAM 16MB/32MB CHANNEL A (NOT INSTALL FOR MEP43/44)

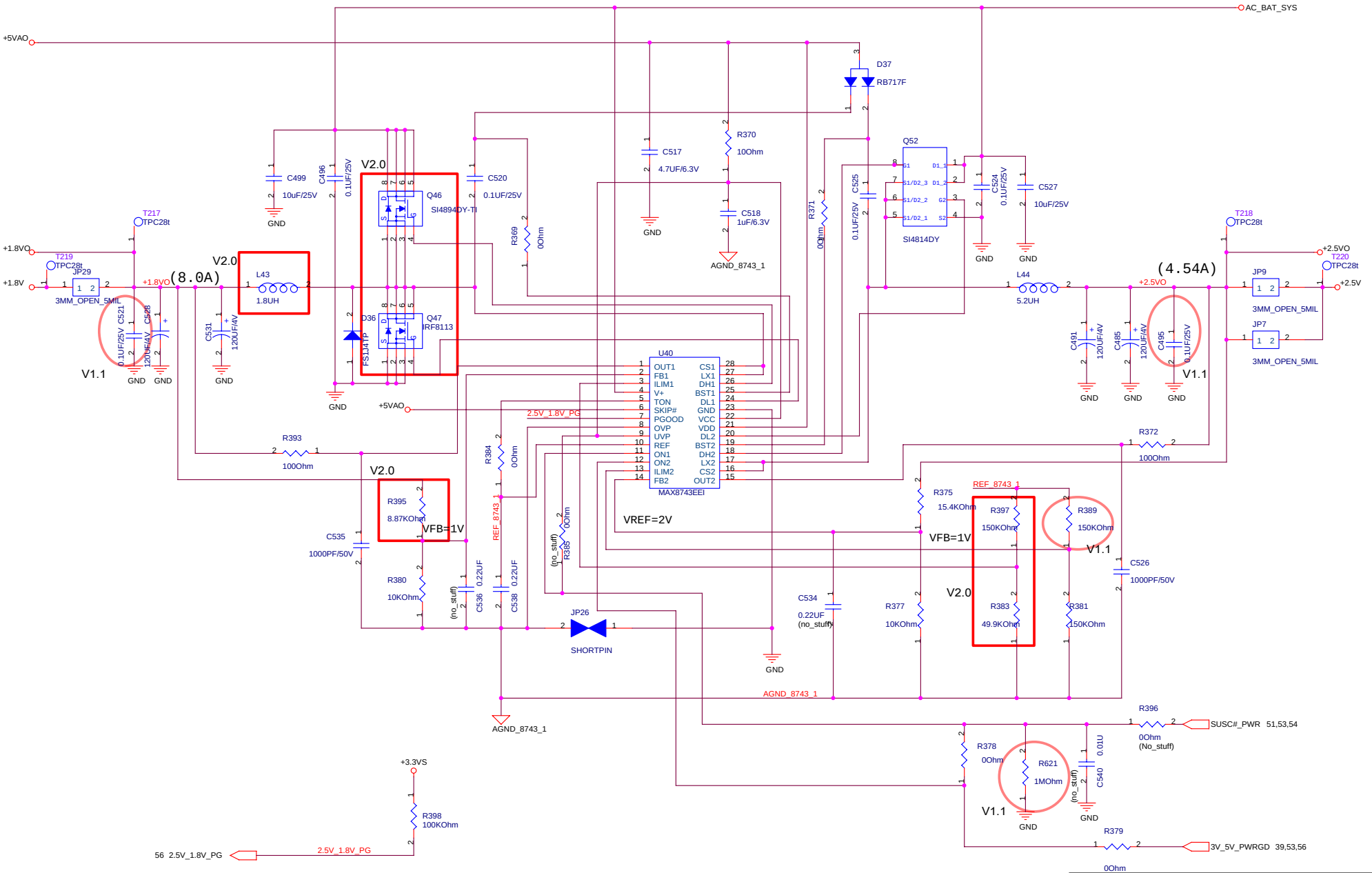
Samsung "03-15124E013" for K4D553235F-GC33 300MHz 600Mbps/pin

ASUSTek COMPUTER INC.	Title : NV44M VRAM	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 49 of 64	

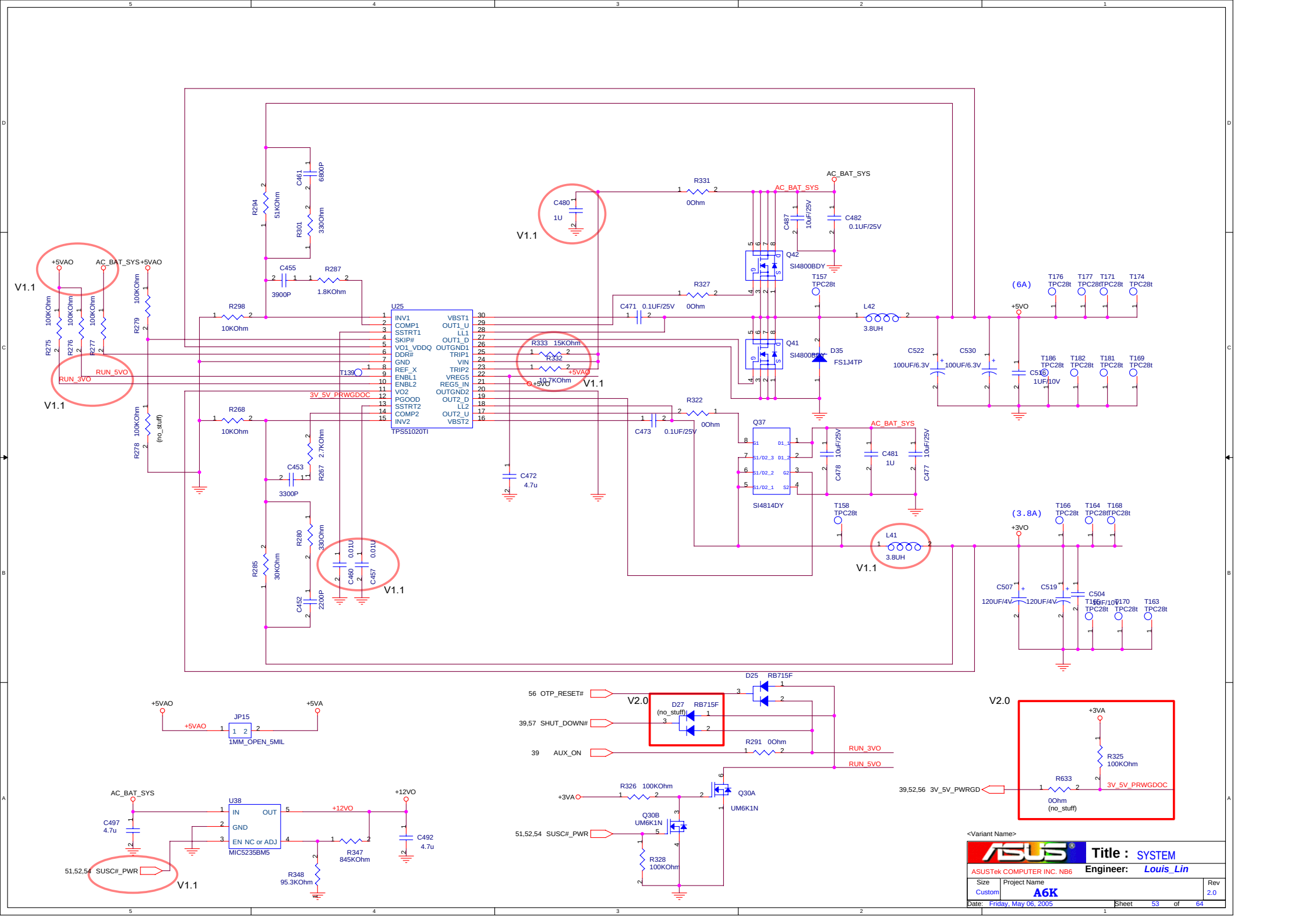

AC_BAT_SYS
AC_BAT_SYS_V
L31 400Ohm/100Mhz
L26 400Ohm/100Mhz
C284 0.1UF
C10 0.001uF/50V
C33 1U
C13 10uF/25V
C24 10uF/25V
Q3 IRF7413Z
+VCORE
T84 TPC28t
L3 0.56UH
R1 3mOhm
(25A)
R121 1.82KOhm
C300 0.22UF/25V
D1 EC31QS04
Q1 IRF7831
C307 0.1UF
R132 0Ohm
D13 RB717F
R128 0Ohm
R129 0Ohm
R150 1.87KOhm
R154 1.87KOhm
C314 0.001uF/50V (no_stuff)
C14 330UF/2V
C11 0.1UF/25V
V1.1
OAIN-
OAIN+
+3.3VS
39,56 +VCORE_PG
4 AVID0
4 AVID1
4 AVID2
4 AVID3
4 AVID4
+5VO
R137 10KOhm (no_stuff)
R140 10KOhm (no_stuff)
R144 10KOhm (no_stuff)
R148 10KOhm (no_stuff)
R153 10KOhm (no_stuff)
R136 0Ohm (no_stuff)
R139 0Ohm (no_stuff)
R143 0Ohm (no_stuff)
R147 0Ohm (no_stuff)
R152 0Ohm (no_stuff)
C303 4.7u
U5 MAX1544ETL
D3 D2 D1 D0 VROK BSTM LXM DHM DLM VDD
D4 OVP SKIP# OAIN+ OAIN- FB CCI GNDS CCV GND
PGND DLS DHS LXS BSTS V+ CMP CMN CSN CSP
VCC ILIM REF OFS SHDN# SI SO SUS TON TIME
OAIN+
OAIN-
4 COREFB
4 COREFB#
R158 1KOhm
R162 470Ohm (no_stuff)
C326 0.022U
R160 1KOhm
C313 470P
R170 10OHM
R165 10OHM (no_stuff)
C325 1000PF/50V
C221 470PF/50V
C315 4.7u
GND
R159 10Ohm
R124 0Ohm
C301 0.1UF
Q71 IRF7413Z
C161 0.001uF/50V
C271 1U
C214 10uF/25V
C244 10uF/25V
C305 0.22UF/25V
R127 1.82KOhm
L67 0.56UH
T45 TPC28t
D54 EC31QS04
Q72 IRF7831
C89 330UF/2V
C53 470UF/2.5V
C90 330UF/2V
39,54 CORE_ON
R142 0Ohm
R146 121KOhm (no_stuff)
R141 200KOhm
C319 100P
R149 0Ohm
R145 100KOhm
C309 1UF/16V
R138 0Ohm (no_stuff)
R135 0Ohm (no_stuff)
R133 0Ohm
R131 30.1KOhm
V1.1
JP6
SHORTPIN
T114 TPC28t AVID0
T115 TPC28t AVID1
T117 TPC28t AVID2
T119 TPC28t AVID3
T122 TPC28t AVID4
T147 TPC28t CORE_ON
T153 TPC28t +VCORE_PG
T123 TPC28t COREFB
T124 TPC28t COREFB#
T22 T19 T21 T86 T85 T20 T91 T87 T18 T90 TPC28t
T6 T48 T88 T47 T89 T83 T7 T81 T80 T82 TPC28t
+VCORE
Title : Vcore
ASUSTek COMPUTER INC. NB6
Engineer: Louis_Lin
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 50 of 64



ASUSTek COMPUTER INC. NB6	Title : 1.25V&1.8V	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 51 of 64	

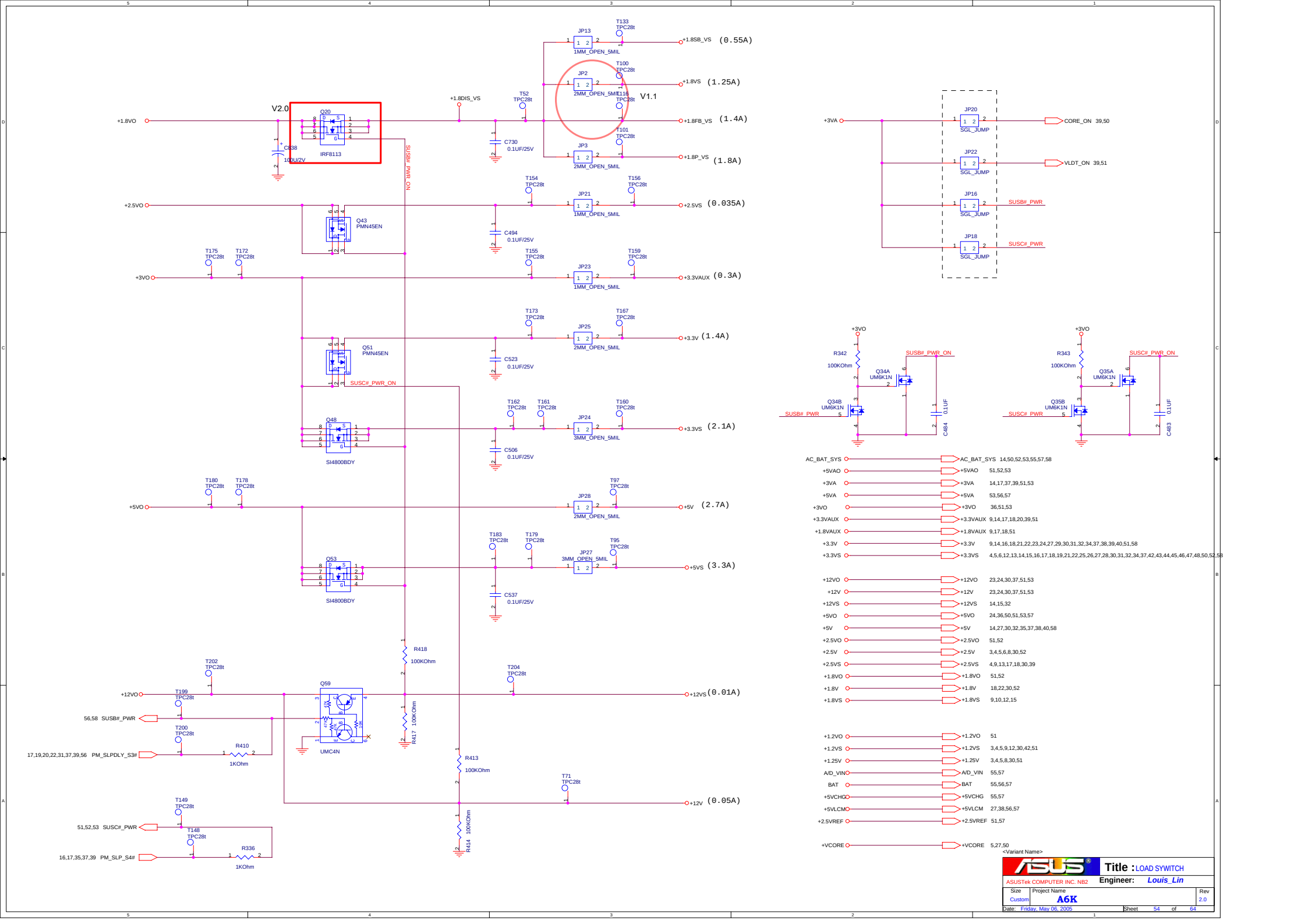


ASUSTek COMPUTER INC. NB6	Title : 1.8V & 2.5V	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 52 of 64	



<Variant Name>

ASUSTek COMPUTER INC. NB6	Title : SYSTEM	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 53 of 64	

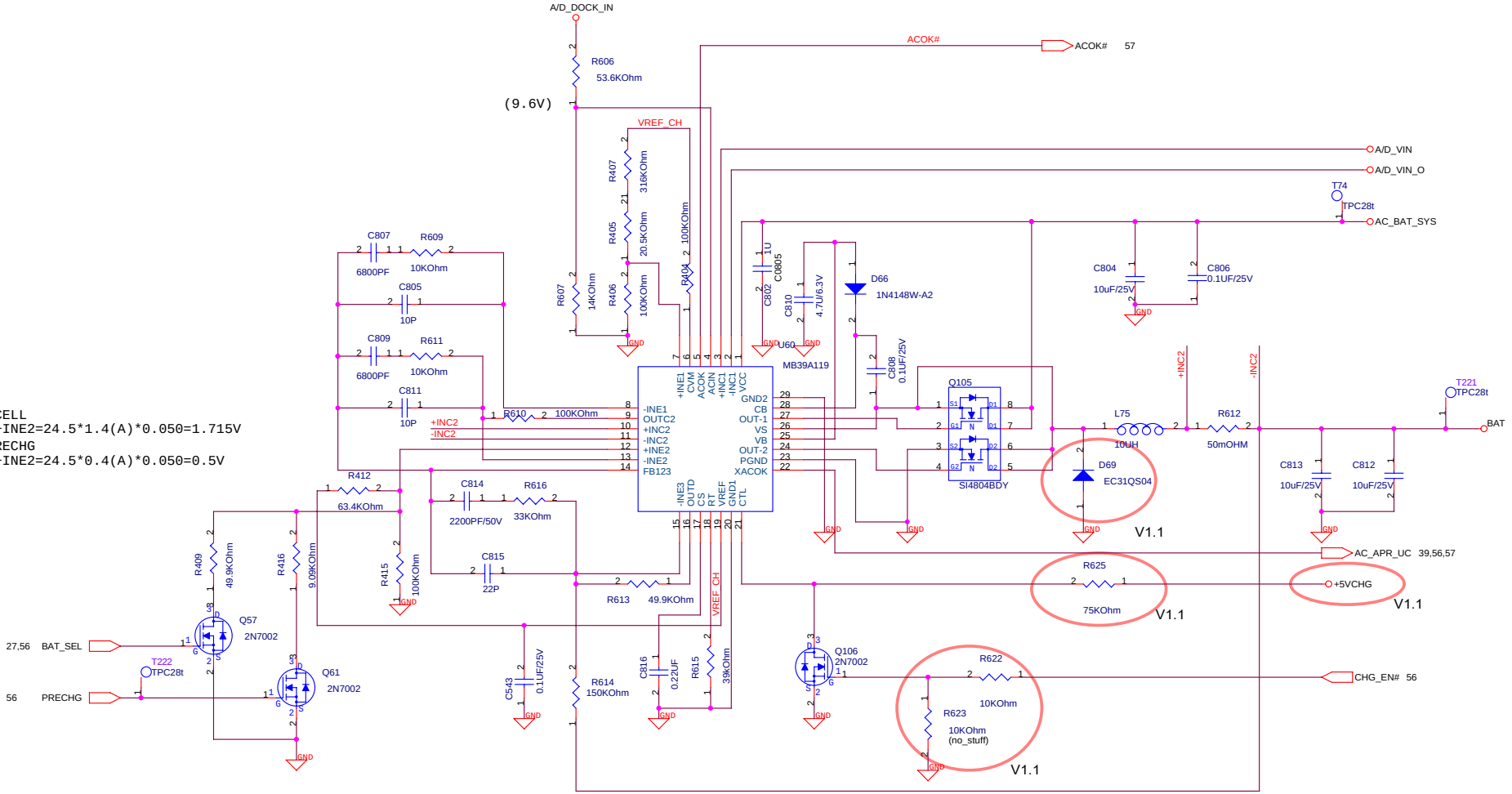

V2.0
V1.1
Q20
IRF8113
C638
100U/2V
+1.8VO
+1.8DIS_VS
T52
TPC28t
C730
0.1UF/25V
JP13
1MM_OPEN_5MIL
T133
TPC28t
+1.8SB_VS (0.55A)
JP2
2MM_OPEN_5MIL
T100
TPC28t
+1.8VS (1.25A)
T116
TPC28t
JP3
2MM_OPEN_5MIL
T101
TPC28t
+1.8FB_VS (1.4A)
+1.8P_VS (1.8A)
SUSB#_PWR_ON
+2.5VO
Q43
PMN45EN
C494
0.1UF/25V
T154
TPC28t
JP21
1MM_OPEN_5MIL
T156
TPC28t
+2.5VS (0.035A)
+3VO
T175
TPC28t
T172
TPC28t
T155
TPC28t
JP23
1MM_OPEN_5MIL
T159
TPC28t
+3.3VAUX (0.3A)
T173
TPC28t
JP25
2MM_OPEN_5MIL
T167
TPC28t
+3.3V (1.4A)
Q51
PMN45EN
C523
0.1UF/25V
SUSC#_PWR_ON
Q48
SI4800BDY
T162
TPC28t
T161
TPC28t
JP24
3MM_OPEN_5MIL
T160
TPC28t
+3.3VS (2.1A)
C506
0.1UF/25V
+5VO
T180
TPC28t
T178
TPC28t
JP28
2MM_OPEN_5MIL
T97
TPC28t
+5V (2.7A)
Q53
SI4800BDY
T183
TPC28t
T179
TPC28t
JP27
3MM_OPEN_5MIL
T95
TPC28t
+5VS (3.3A)
C537
0.1UF/25V
R418
100KOhm
+12VO
T202
TPC28t
T199
TPC28t
Q59
UMC4N
T204
TPC28t
+12VS (0.01A)
56,58 SUSB#_PWR
T200
TPC28t
R410
1KOhm
17,19,20,22,31,37,39,56 PM_SLPDLY_S3#
R417
100KOhm
R413
100KOhm
T71
TPC28t
+12V (0.05A)
T149
TPC28t
51,52,53 SUSC#_PWR
T148
TPC28t
R336
1KOhm
16,17,35,37,39 PM_SLP_S4#
R414
100KOhm
SUSB#_PWR_ON
SUSC#_PWR_ON
+3VA
JP20
SGL_JUMP
CORE_ON 39,50
JP22
SGL_JUMP
VLDT_ON 39,51
JP16
SGL_JUMP
SUSB#_PWR
JP18
SGL_JUMP
SUSC#_PWR
R342
100KOhm
Q34A
UM6K1N
Q34B
UM6K1N
SUSB#_PWR
C484
0.1UF
R343
100KOhm
Q35A
UM6K1N
Q35B
UM6K1N
SUSC#_PWR
C483
0.1UF
AC_BAT_SYS
+5VAO
+3VA
+5VA
+3VO
+3.3VAUX
+1.8VAUX
+3.3V
+3.3VS
+12VO
+12V
+12VS
+5VO
+5V
+2.5VO
+2.5V
+2.5VS
+1.8VO
+1.8V
+1.8VS
+1.2VO
+1.2VS
+1.25V
A/D_VIN
BAT
+5VCHG
+5VLCM
+2.5VREF
+VCORE
AC_BAT_SYS 14,50,52,53,55,57,58
+5VAO 51,52,53
+3VA 14,17,37,39,51,53
+5VA 53,56,57
+3VO 36,51,53
+3.3VAUX 9,14,17,18,20,39,51
+1.8VAUX 9,17,18,51
+3.3V 9,14,16,18,21,22,23,24,27,29,30,31,32,34,37,38,39,40,51,58
+3.3VS 4,5,6,12,13,14,15,16,17,18,19,21,22,25,26,27,28,30,31,32,34,37,42,43,44,45,46,47,48,50,52,58
+12VO 23,24,30,37,51,53
+12V 23,24,30,37,51,53
+12VS 14,15,32
+5VO 24,36,50,51,53,57
+5V 14,27,30,32,35,37,38,40,58
+2.5VO 51,52
+2.5V 3,4,5,6,8,30,52
+2.5VS 4,9,13,17,18,30,39
+1.8VO 51,52
+1.8V 18,22,30,52
+1.8VS 9,10,12,15
+1.2VO 51
+1.2VS 3,4,5,9,12,30,42,51
+1.25V 3,4,5,8,30,51
A/D_VIN 55,57
BAT 55,56,57
+5VCHG 55,57
+5VLCM 27,38,56,57
+2.5VREF 51,57
+VCORE 5,27,50
<Variant Name>
Title : LOAD SYWITCH
ASUSTek COMPUTER INC. NB2
Engineer: Louis_Lin
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
Sheet 54 of 64

+Vbat=(R1+R2)/R2*4.2
+Vbat=(30k+10k)/10k*4.2=16.8V

V+INE2=24.5*Ichg(A)*Rs1
V+INE2=24.5*2.5(A)*0.050=3.062V Vref=5.000V
DEFAULT R(low)=100K
R(hi)=(5/3.062-1)*100K=63.3K

V+INE1=25*Iin(A)*Rs2
V+INE1=25*4.58(A)*0.010=1.145V
DEFAULT R(low)=100K
R(hi)=(5/1.145-1)*10K=336.68K

4CELL
V+INE2=24.5*1.4(A)*0.050=1.715V
PRECHG
V+INE2=24.5*0.4(A)*0.050=0.5V



<Variant Name>

Title : CHARGER
ASUSTek COMPUTER INC. NB6
Engineer: Louis_Lin
Size: Custom
Project Name: A6K
Rev: 2.0
Date: Friday, May 06, 2005
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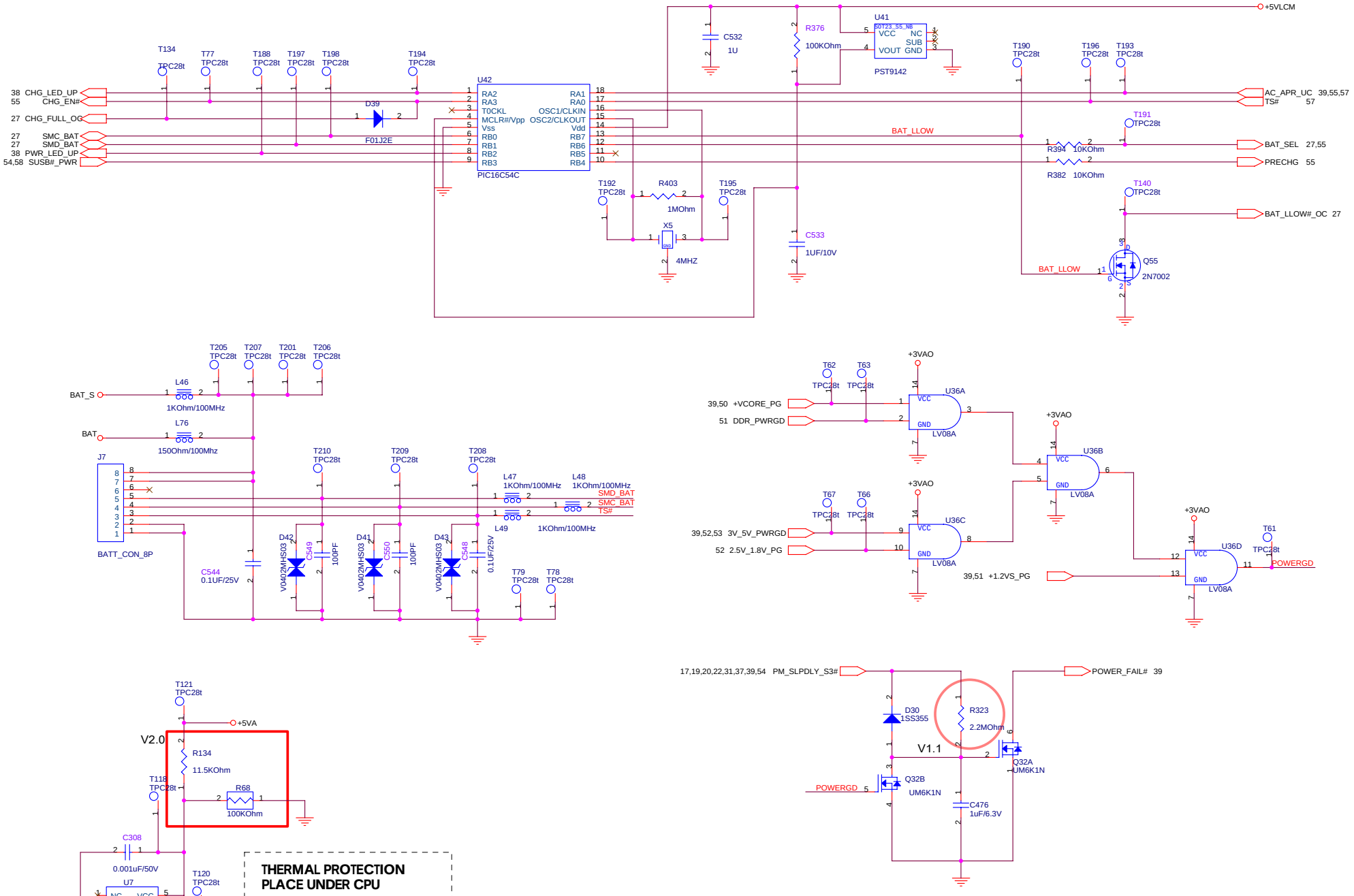
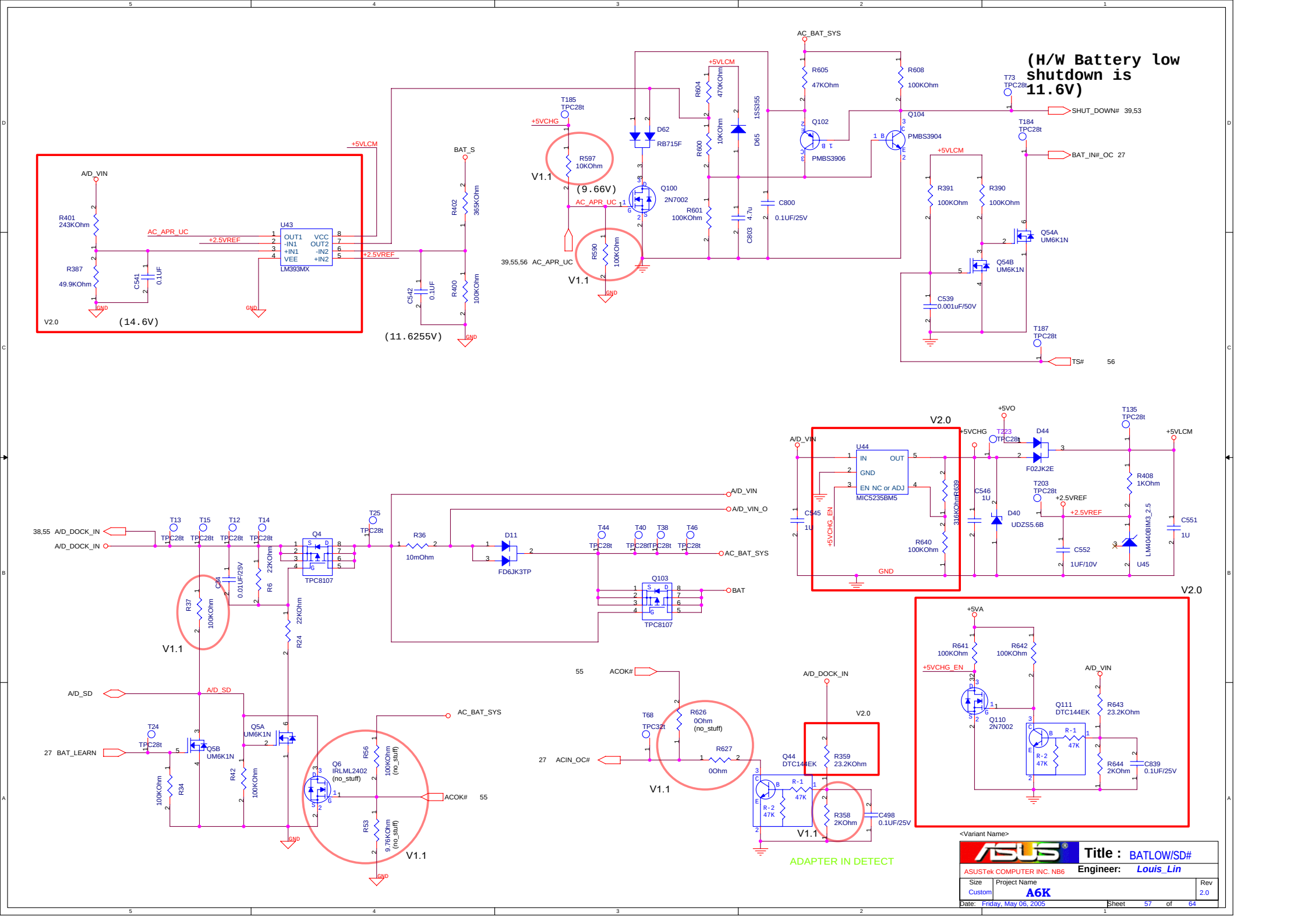


<Variant Name>

ASUSTek COMPUTER INC. NB6	Title : PIC16C54	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Friday, May 06, 2005	Sheet 56 of 64	


(H/W Battery low shutdown is 11.6V)
AC_BAT_SYS
A/D_VIN
R401 243KOhm
R387 49.9KOhm
C541 0.1UF
U43
LM393MX
AC_APR_UC
+2.5VREF
+5VLCM
BAT_S
R402 365KOhm
R400 100KOhm
C542 0.1UF
(14.6V)
(11.6255V)
V2.0
T185 TPC28t
+5VCHG
R597 10KOhm
V1.1
(9.66V)
D62 RB715F
R604 470KOhm
R600 10KOhm
D65 1SS355
Q100 2N7002
R601 100KOhm
C803 4.7u
C800 0.1UF/25V
R590 100KOhm
39,55,56 AC_APR_UC
R605 47KOhm
R608 100KOhm
Q102 PMBS3906
Q104 PMBS3904
T73 TPC28t
SHUT_DOWN# 39,53
T184 TPC28t
BAT_IN#_OC 27
R391 100KOhm
R390 100KOhm
Q54A UM6K1N
Q54B UM6K1N
C539 0.001uF/50V
T187 TPC28t
TS# 56
V2.0
A/D_VIN
U44
MIC5235BM5
+5VCHG
+5VO
T223 TPC28t
D44 F02JK2E
T135 TPC28t
+5VLCM
R408 1KOhm
C545 1U
+5VCHG_EN
R640 100KOhm
R639 316KOhm
C546 1U
D40 UDZS5.6B
T203 TPC28t
+2.5VREF
C552 1UF/10V
LM4040BIM3_2.5
U45
C551 1U
GND
38,55 A/D_DOCK_IN
A/D_DOCK_IN
T13 TPC28t
T15 TPC28t
T12 TPC28t
T14 TPC28t
Q4 TPC8107
T25 TPC28t
R36 10mOhm
D11 FD6JK3TP
A/D_VIN
A/D_VIN_O
AC_BAT_SYS
T44 TPC28t
T40 TPC28t
T38 TPC28t
T46 TPC28t
Q103 TPC8107
BAT
R37 100KOhm
C534 0.01UF/25V
R6 22KOhm
R24 22KOhm
V1.1
A/D_SD
T24 TPC28t
27 BAT_LEARN
Q5A UM6K1N
Q5B UM6K1N
R34 100KOhm
R42 100KOhm
Q6 IRLML2402 (no_stuff)
R56 100KOhm (no_stuff)
R53 9.76KOhm (no_stuff)
ACOK# 55
55 ACOK#
T68 TPC32t
R626 0Ohm (no_stuff)
R627 0Ohm
27 ACIN_OC#
V1.1
A/D_DOCK_IN
V2.0
Q44 DTC144EK
R359 23.2KOhm
R358 2KOhm
C498 0.1UF/25V
V1.1
ADAPTER IN DETECT
V2.0
+5VA
R641 100KOhm
R642 100KOhm
+5VCHG_EN
Q110 2N7002
A/D_VIN
Q111 DTC144EK
R643 23.2KOhm
R644 2KOhm
C839 0.1UF/25V
<Variant Name>
Title : BATLOW/SD#
ASUSTek COMPUTER INC. NB6
Engineer: Louis_Lin
Size Custom
Project Name A6K
Rev 2.0
Date: Friday, May 06, 2005
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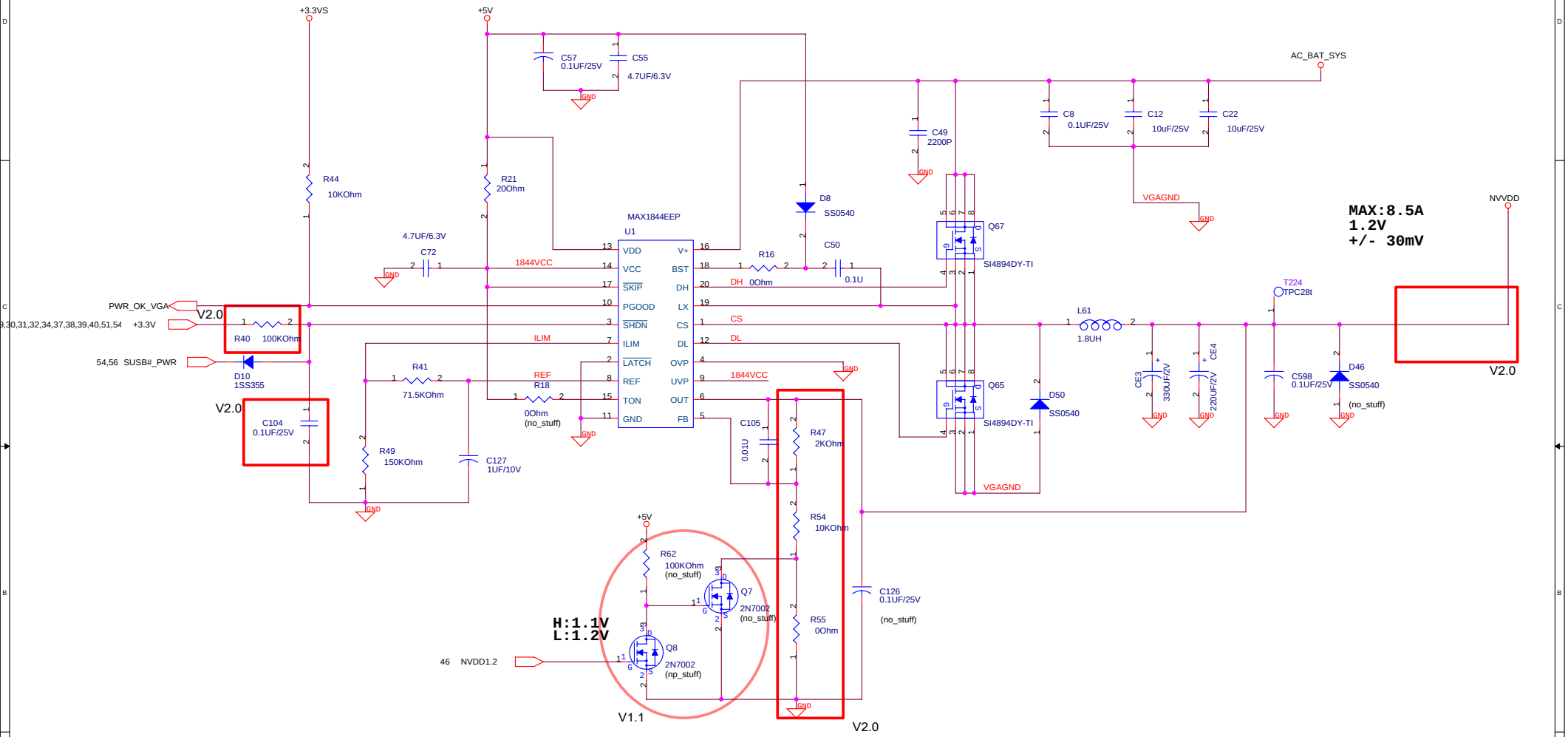


<Variant Name>

Title : VGACORE

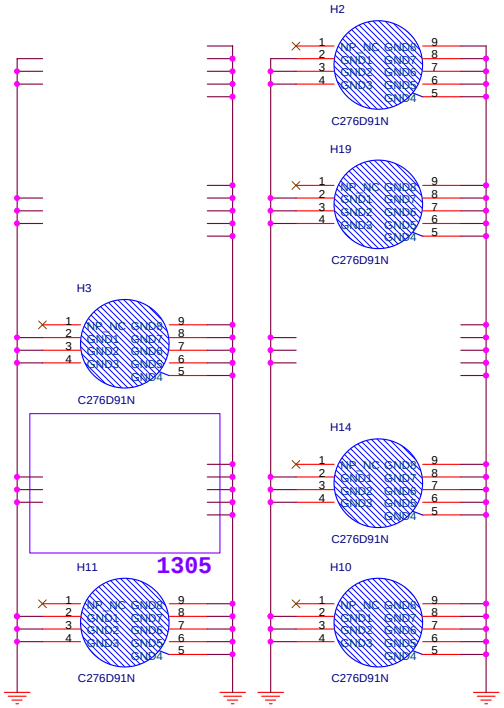
ASUSTek COMPUTER INC. NB6

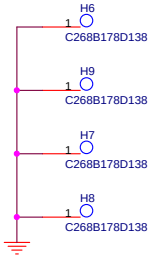
Engineer: Louis_Lin

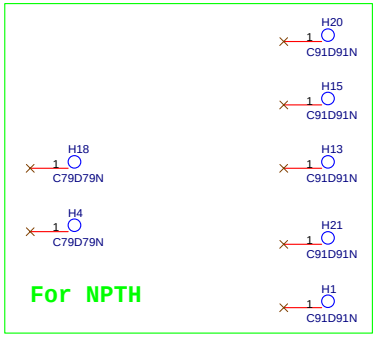
Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 58 of 64

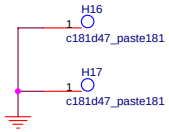
SCREW HOLE





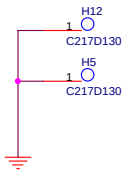


For MDC module



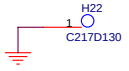
P/N 13-N7510M270

For NB fix sink

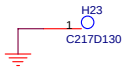


P/N 13-NCF10M010

For NV44M-V fix sink



Heat sink



CPU Throttling(BIOS setting): 90 degree C.
System shutdown(BIOS setting) : 100 degree C.
H/W shutdown(page 44, U47 , no load) : 105 degree C.

Short Pad location:
Page39: JP4,5,15,16,19,26,27
Page40: JP6,7,9,22,24
Page42: JP13,14,17,18,28,29

Don't Short Pad: JP26

JP4:+V2.5 --Power In
JP5:+V1.25S
JP6:+V2.5
JP7:+V1.2S
JP9:+VCCP
JP13:+V5S
JP14:+V5
JP15:+V1.5SUS
JP16:+V2.5 --Power IN
JP17:+V1.8S
JP18:+V12
JP19:+V1.8
JP22:+V1.5S
JP24: VREF5-->+V5A
JP26:+3VALWAYS_T-->+V3.3A(open)
JP27:+3VALWAYS_M-->+V3.3A(short)
JP28:+V3.3S
JP29:+V3.3

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	20 mils

37.5 OHM	WIDTH
TOP/BOT	12 mils

42 OHM	WIDTH
TOP/BOT	10 mils

55 OHM	WIDTH
TOP/BOT	5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	7 mils/ 10 mils

100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#

CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

<Variant Name>

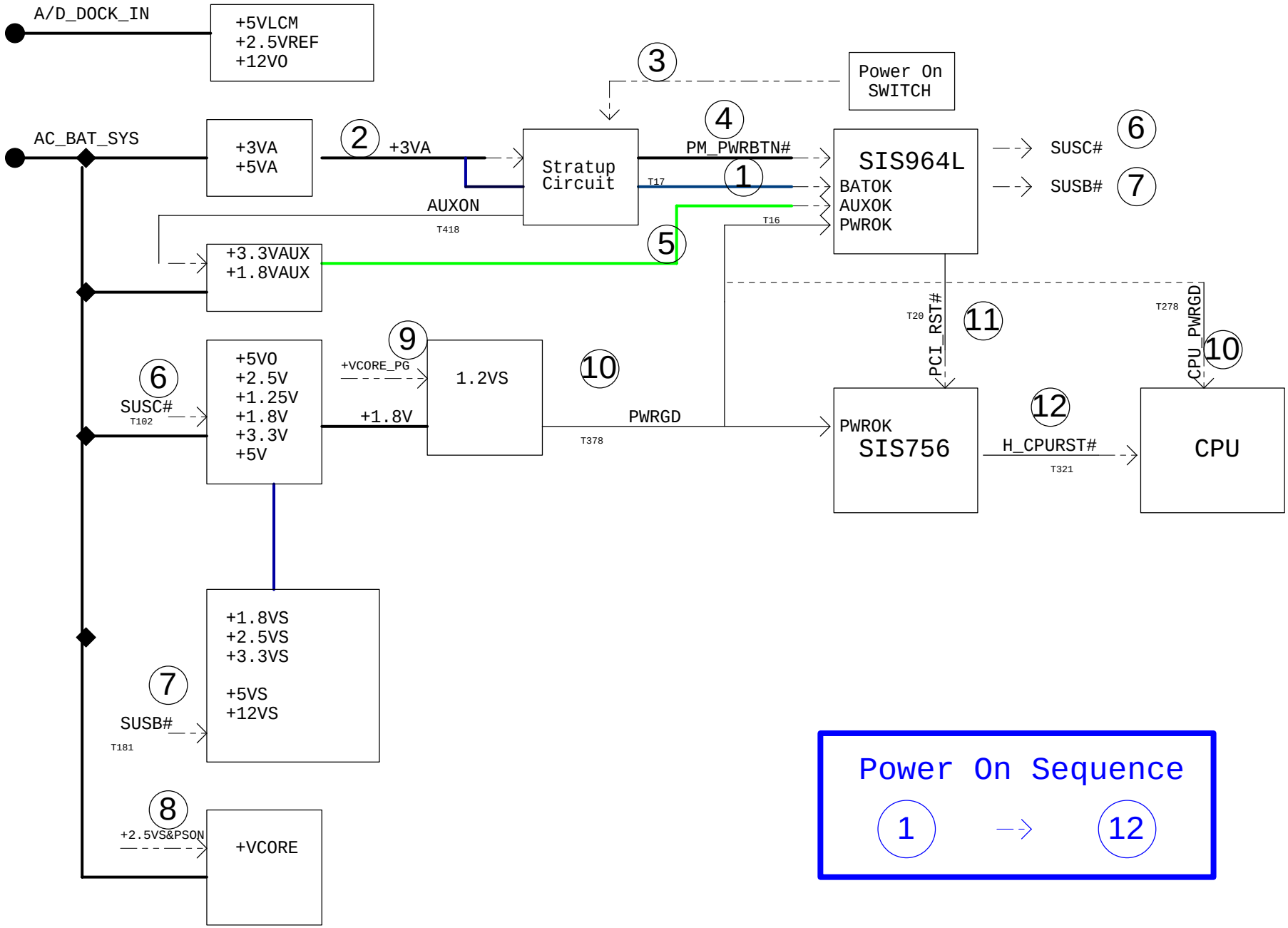
ASUSTek COMPUTER INC. NB6

Title : SCREW HOLE

Engineer:

Size	Project Name	Rev
Custom	A6U	2.0

Date: Friday, May 06, 2005 Sheet 59 of 64



ASUSTeK COMPUTER INC		Title : Power On Sequence	
		Engineer:	
Size: Custom	Project Name: A6K		Rev: 2.0
Date: Friday, May 06, 2005		Sheet 60 of 64	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN_RTL8100CL	AD22	2	D
CARD READER	AD21	0	B
CARDBUS	AD21	0	C
1394	AD21	0	D
MINIPCI (802.11a/b/g)	AD20	1	C,D

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010010x (A4)
Thermal Sensor (SA56004)	0101110x (5C)
PIC	1001001x (92)

SiS964L GPIO	SIGNAL NAME	I/O	Volt
GPIO 0		P-U	+3.3VS
GPIO 1	NV_THERM#	INPUT	+3.3VS
GPIO 2	THRM_ALERT#	INPUT	+3.3VS
GPIO 3	EXTSMI#	INPUT	+3.3VS
GPIO 4	PM_CLKRUN#	OUTPUT	+3.3VS
GPIO 5		P-U	+3.3VS
GPIO 6	CPUFAN_SPD_A	INPUT	+3.3VS
GPIO 7	BACK_OFF#	OUTPUT	+3.3VAUX
GPIO 8	PM_RI#	INPUT	+3.3VAUX
GPIO 9	KBDSCI_3A	INPUT	+3.3VAUX
GPIO 10	LID_963#_3A	INPUT	+3.3VAUX
GPIO 11	PM_STPPCI#	OUTPUT	+3.3VAUX
GPIO 12	PM_STPCPU#	OUTPUT	+3.3VAUX
GPIO 13	SIO_SMI#	INPUT	+3.3VAUX
GPIO 14	S3AUXSW#	OUTPUT	+3.3VAUX
GPIO 15	BT_ON	P-L	+3.3VAUX
GPIO 16	802_LED_EN#	OUTPUT	+3.3VAUX
GPIO 17	WLAN_ON#	OUTPUT	+3.3VAUX
GPIO 18	CB_SD#	OUTPUT	+3.3VAUX
GPIO 19	SM_CLK	OUTPUT	+3.3VS
GPIO 20	SM_DATA	I/O	+3.3VS
GPIO 21		NC	+3.3VAUX
GPIO 22		NC	+3.3VAUX
GPIO 23		P-L	+3.3VAUX
GPIO 24		P-U	+3.3VAUX

KBC GPIO	A6K	
P23	OP_SD#	
P22	BAT_LEARN	
P21	(KB_P21)	
P20	KBCRSM	
P42	(WATCHDOG)	
P43	CHG_FULL_OC	
P44	KB_CPURST	
P45	KB_GATEA20	
P46	KBCSCI	
P47	PM_CLKRUN#	
P50	KBC_BAT_LLOW#	
P51	KEYDETECT1	
P52	KEYDETECT2	
P53	CLR_DJ#	
P54	BAT_SEL	
P55	BAT1_IN#_OC	
P56	(FAN_DA1)	
P57	ADJ_BL	
P67	DJ_LED#	
P66	SWDJ_EN#	
P65	+VCORE	
P64	ACIN_OC	
P63	DISTP	
P62	MARATHON#	
P61	INTERNET#	
P60	EMAIL#	
P75	(KB_CLK)	
P74	(MS_CLK)	
P73	TPAD_CLK	
P72	(KB_DAT)	
P71	(MS_DAT)	
P70	TPAD_DAT	
P77	BAT_SMC	
P76	BAT_SMD	
P27	SCROLLLOCK#	
P26	NUM_LED#	
P25	CAP_LED#	
P24	SET_PLTRSTNS#	
P40	EXT_SMI	
P41	EMAIL_LED#	

ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 61 of 64

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

ASUSTek COMPUTER INC. NB6

Title : SECOND SOURCE

Engineer:

Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 62 of 64

REVISION LIST

POWER INTERFACE

SIGNALS	TYPE	POWER

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.55V	27.3A
+1.25V	1.25V	0.725A
NVVDD	1.1/1.2V	8.62A
+2.5V	2.5V	5.55A
+1.8VAUX	1.8V	50mA
+1.2P_VS	1.2V	1.875A
+1.2VS	1.2V	635mA
+1.8VS	1.8V	2.521A
+1.8V	1.8V	415 mA
+1.8FB_VS	1.8V	2A
+2.5VS	2.5V	0.035A
+3.3V	3.3V	1.925A
+3.3VS	3.3V	2.955A
+5VS	5V	4.7A
+5V	5V	3.865A
+5VA	5V	0.05A
+12V	12V	0.05A
+12VS	12V	0.01A
+3.3VAUX	3.3V	0.417A
+3VA	3.3V	0.02A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	22 mils
IN1/IN3	16 mils

37.5 OHM	WIDTH
TOP/BOT	13.5 mils
IN1/IN3	10 mils

42 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN3	8.5 mils

55 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN3	5 mils

75 OHM	WIDTH
TOP/BOT	2.5 mils
IN1/IN3	2 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	8 mils/ 4 mils
IN1/IN3	8 mils/ 3.5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 5 mils
IN1/IN3	5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	4 mils/ 6 mils
IN1/IN3	4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD22

PCIE Device

PEG

NVIDIA NV44M

PCIE Giga NIC

N/A

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 IN1
L4 IN2
L5 GND
L6 BOT

PAGE 49

SIGNAL	IN:	AVID[0:4]
		CORE_ON
		COREFB
		COREFB#
	OUT:	+VCORE_PG
POWER	IN:	AC_BAT_SYS
		+5VO
		+3.3VS
	OUT:	+VCORE

PAGE 50

SIGNAL	IN:	VLDT_ON
		+2.5VREF
		SUSC#_PWR
	OUT:	DDR_PWRGD
		+1.2VS_PG
POWER	IN:	+5VAO
		+12V
		+3VO
		+3VAUX
		+2.5VO
		+1.25V
		+3.3V
		+5VO
		+1.8VO
	OUT:	+3VA
		+1.8VAUX
		+1.25V
		+1.2VS
		+1.2P_VS

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SIGNAL	IN:	SUSC#_PWR
	OUT:	2.5V_1.8V_PG
POWER	IN:	AC_BAT_SYS
		+3.3VS
		+5VAO
	OUT:	+2.5V
		+1.8V

PAGE 52

SIGNAL	IN:	SUSC#_PWR
		OTP_RESET#
		SHUT_DOWN#
		AUX_ON
	OUT:	3V_5V_PWRGD
POWER	IN:	AC_BAT_SYS
		+3VA
		+3.3VS
		+VCC_GMCH_CORE
		+5VAO
	OUT:	+5VA
		+5VO
		+12VO
		+3VO

ASUSTeK COMPUTER INC

Title : REVISION LIST

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 63 of 64

Rev	Date	Description
R1.00	04/6/28	1. Initial release.
R1.1	02/14/05'	1.R14&R15 be changed from 75 ohm to 49.9 ohm,P-9.follow SIS. 2.Q26A be changed to "D67" to prevent body diode leakage current,p-39. 3.Q26B be changed to "Q107",P-39. 4.R453&R475 be changed from 10kohm to 6.81kohm,P-49.follow NVIDIA. 5.R578 & C758 be changed to mounting. 6.JP32 CON pin definition be corrected. 7.Enable R5C841 internal regulator,P-22. VCC_RIN= +3.3V 8.C769 be changed from 0.1uf to 0.47uf,P-22. globe reset timing. 9.Audio Jack "J5" be changed from "12-140001088" to "12-140001081",P-32. 10.C665,C666,C659,C655,C643,C648 be changed from 330pf to 5pf,P-15. 11.C4 & C7 be changed from 5pf to 27pf and mounted,P-15
	02/21/05'	1.Added C834,C835,C836 at NVVDD,P-42. reduce ripple. 2.Added R587 and U61 ,P-39. meet K8 CPU power off sequency. 3.Changed U28 power source from +5VA to +3VA,P-39.prevent quiescent current. 4.Changed RN28B pull up power source from +3.3VAUX to +3VA,P-39.prevent quiescent current. 5.Removed Q88B ,P-37.DJ_SW# latched sequency . 6.Q16 and Q45 be changed ,P-28.parts Preparing. 7.Added D68 ,P27.LED flash when ODD running. 8.Added JRST1,P-17. subbattery reset asserted. 9.Added R617 47KOHM pull low ,P-16
	02/22/05'	1.Added R624 and changed R130 from 10k ohm to 47kohm,P-14. white screen when entry and resuming in S3. 2.Added C837,P-42.EMI 3.Changed thermal sensor for cost.
	02/23/05'	1.Changed R29 pin2 power source from +3.3VAUX to +3.3VAUX_NB,P-9.
	02/25/05'	1.CN17/CN18/CN19/CN20/CN33 parts be changed for cost! 2.R264 unmount,p-9.duplicate
R2.0	03/15/05'	1.Added D72 & R630,P-35. Prevent leakage current. 2.Changed part of phone jack ,P-32
	03/16/05'	1.Connected "R629" of LAN_PME# to "PME#",P-16.support wake up LAN in S4. 2.LPT port pull-up 2.7kohm,P-29.for QA+PRO test fail.
	03/17/05'	1.Seperated common resistor for power LED,P-38
	03/21/05'	1.Changed parts CN17,CN18,CN19,CN20,P-29.soucer request.
	03/22/05'	1.Cancel JP11 & JP12 ,P-14. 2.Added JP33,P-39.factory request. 3.Added U62 and R632,P-39.Power sequency.
	03/23/05'	1.Cancel R171 and add L77,p-32 Change power source of audio amplifier.

Rev	Date	Description
R2.0	03/24/05'	1.Changed "CE1"from 120uf to 47uf,P-4.Cost down. 2.Q10 be changed part number,P-44. Old part EOL. 3.Added R638 and R571,p-40. 4.Q76 be changed part number.P-7.Old part EOL. 5 Added R634,P-23.Solved auto launch from resum. 6.Q98 be changed part number.P-21.Old part EOL. 7.Changde Q33,R636,R637,P-17.Meterial shortage.

ASUSTek COMPUTER INC. NB6

Title : REVISION(1)

Engineer: Bruce Lee

Size	Project Name	Rev
Custom	A6K	2.0

Date: Friday, May 06, 2005 Sheet 64 of 64