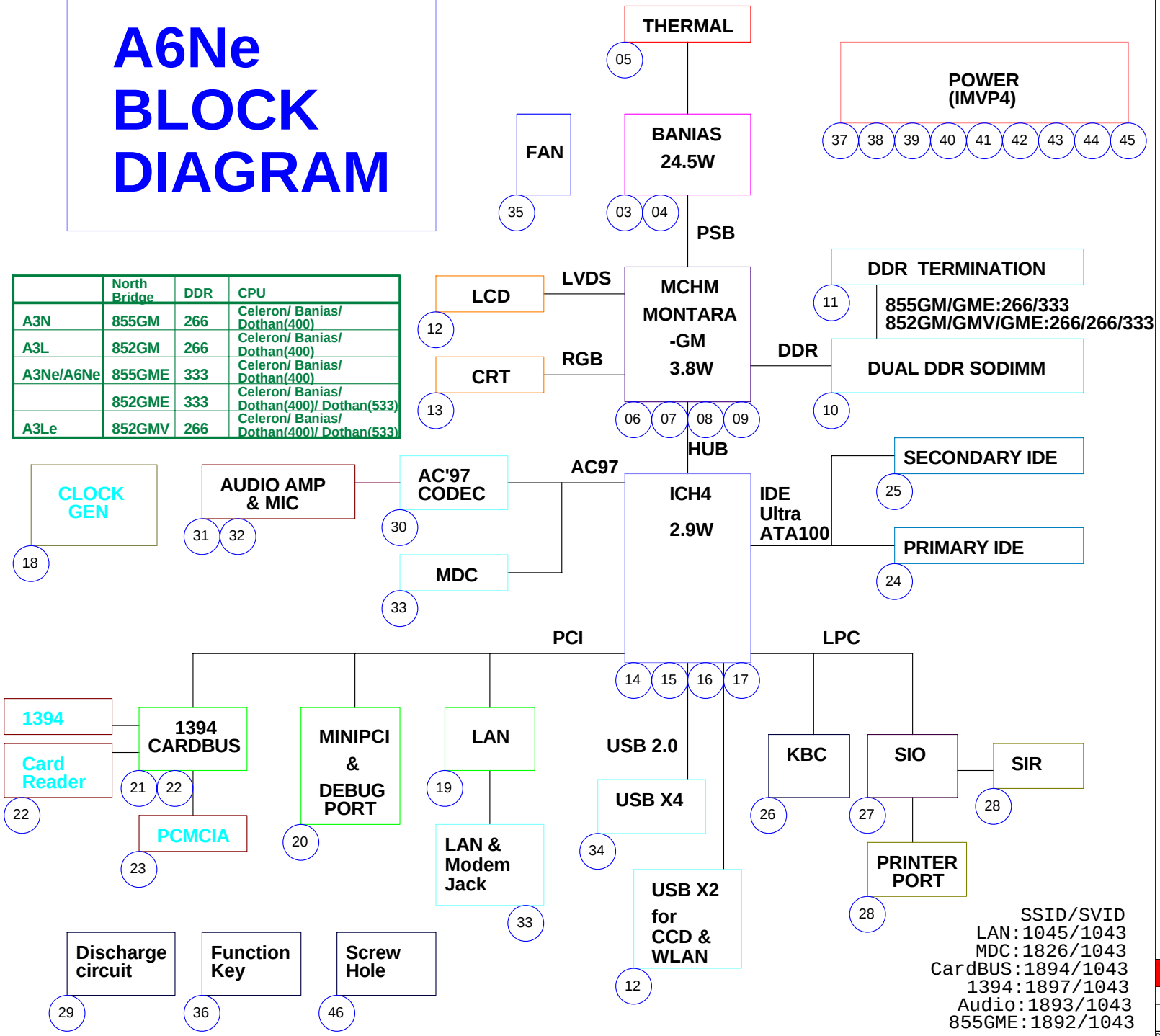
A6Ne BLOCK DIAGRAM



	North Bridge	DDR	CPU
A3N	855GM	266	Celeron/ Banias/ Dothan(400)
A3L	852GM	266	Celeron/ Banias/ Dothan(400)
A3Ne/A6Ne	855GME	333	Celeron/ Banias/ Dothan(400)
	852GME	333	Celeron/ Banias/ Dothan(400)/ Dothan(533)
A3Le	852GMV	266	Celeron/ Banias/ Dothan(400)/ Dothan(533)

SSID/SVID
LAN:1045/1043
MDC:1826/1043
CardBUS:1894/1043
1394:1897/1043
Audio:1893/1043
855GME:1892/1043

FILE LIST

01

01_BLOCK DIAGRAM
02_POWER DIAGRAM
03_CPU-BANIAS(HOST)
04_CPU-BANIAS(PWR)
05_THERMAL
06_NB-MCHM(DDR)
07_NB-MCHM(HOST)
08_NB-MCHM(VGA)
09_NB-MCHM(PWR)
10_DUAL DDR SODIMM
11_DDR TERMINATION
12_LVDS & BACKLIGHT
13_CRT CONNECTOR
14_ICH4-M(HUB_PCI)
15_ICH4-M(H_U_IDE_PM)
16_ICH4-M(PWR)
17_ICH4-M_PULLUP
18_CLOCK-ICS950815
19_LAN-RTL8100CL
20_MINIPCI
21_CB1394-R5C593(1)
22_CB1394-R5C593(2)
23_PCMCIA SOCKET
24_IDE-HD
25_IDE-ODD
26_KBC-M38857
27_SIO-ITE7805
28_IR&LPT_PORT
29_DISCHARGE CIRCUIT
30_CODEC-ALC650
31_AUDIO AMP
32_MIC
33_MDC&RJ45&RJ11
34_USB
35_FAN&Audio DJ
36_FUNCTION KEY
37_PWR & RESET SEQ
38_VCORE
39_1.25V&1.8V
40_2.5V&1.5V&1.35V&1.05V
41_SYSTEM
42_LOAD SWITCH
43_CHARGER
44_PIC16C54
45_BATLOW/SD#
46_SCREW HOLE & M/B SETTING
47_REVISION(1)
48_REVISION(2)
49_REVISION(3)
50_REVISION(4)

ASUSTek COMPUTER INC. NB1

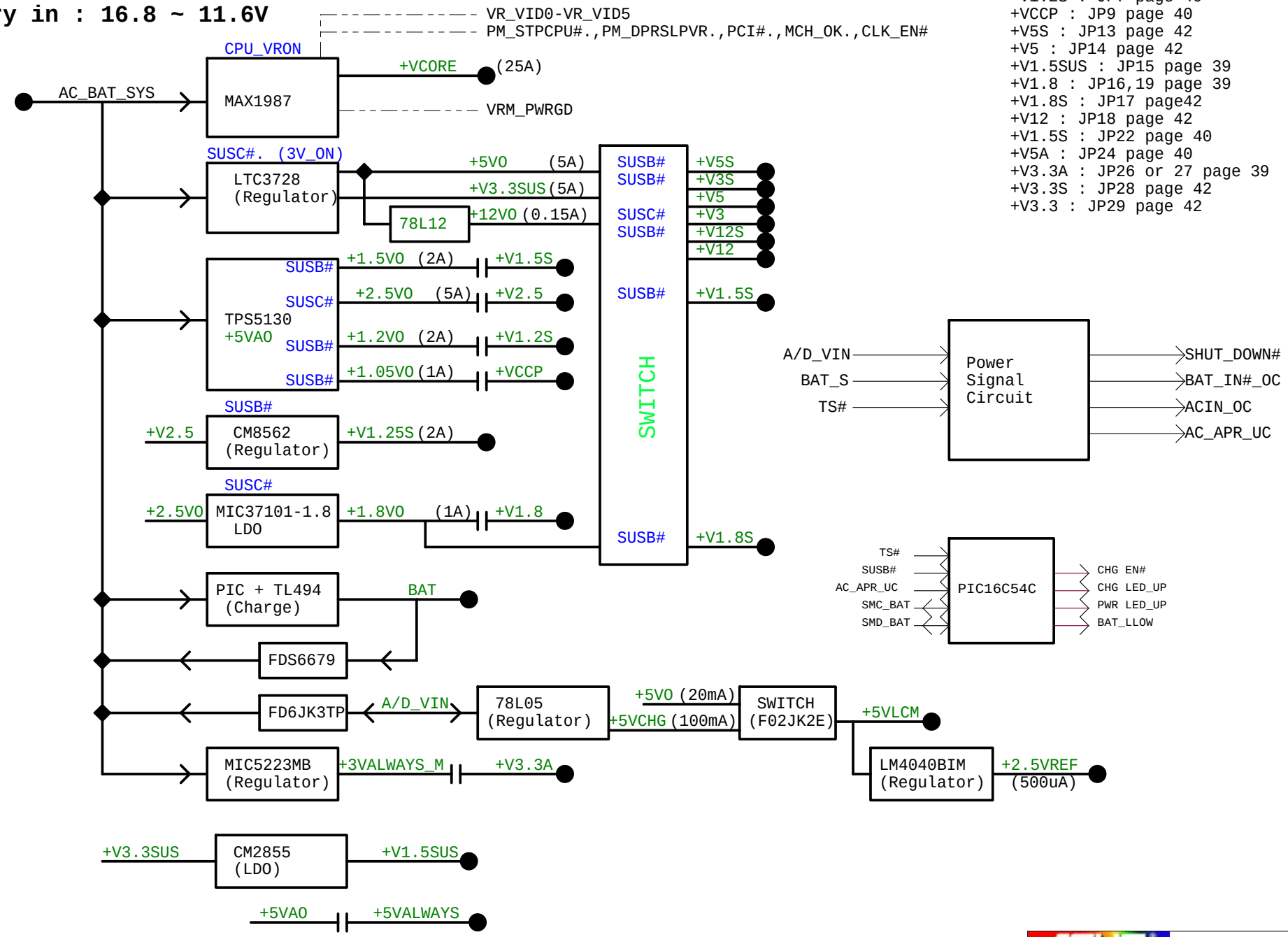
Title : BLOCK DIAGRAM

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 1 of 51

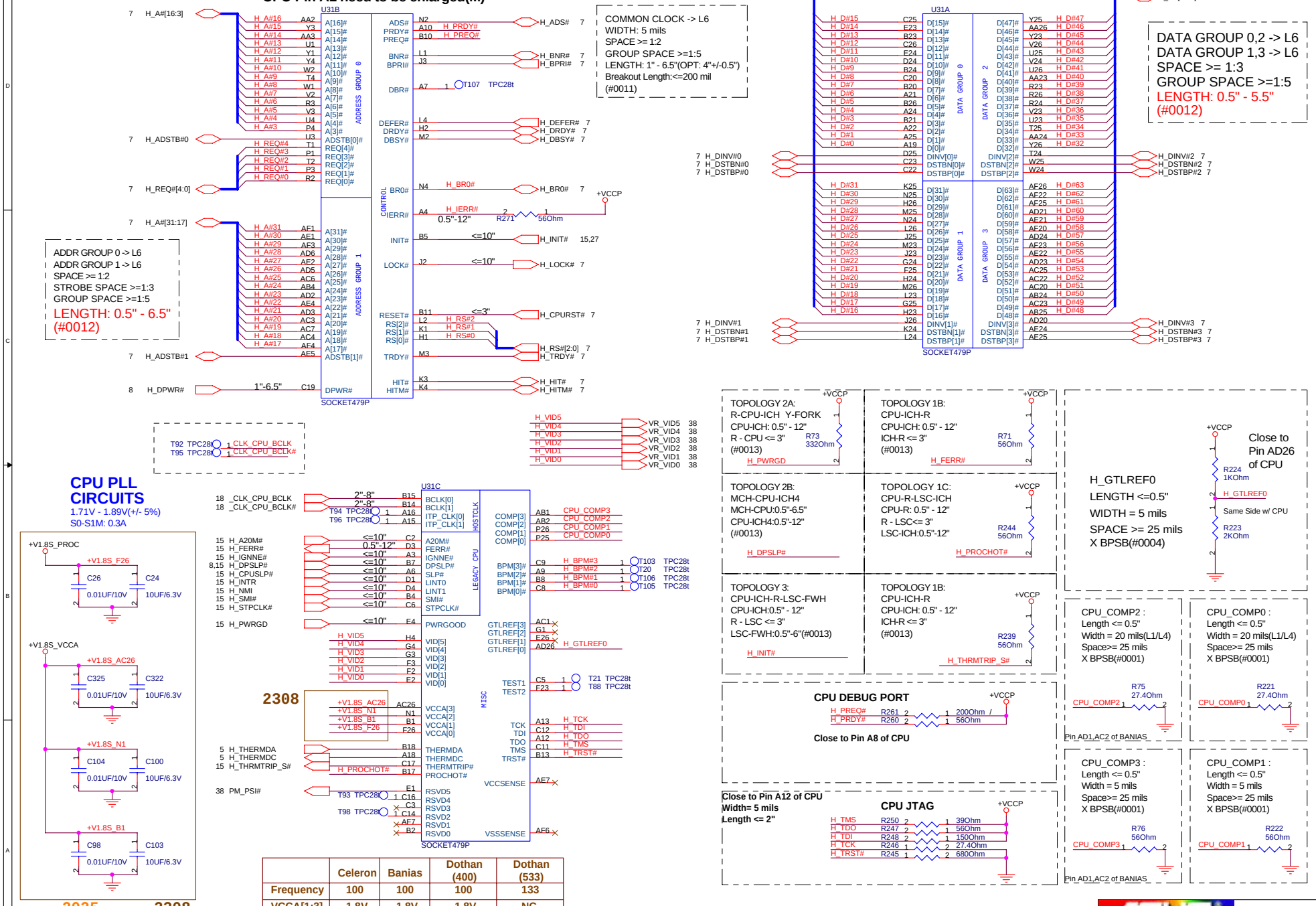
System work voltage
Adapter in : 19.5 ~18.5 V
Battery in : 16.8 ~ 11.6V



+V1.25S : JP4,5 page 39
+V2.5 : JP6 page 40
+V1.2S : JP7 page 40
+VCCP : JP9 page 40
+V5S : JP13 page 42
+V5 : JP14 page 42
+V1.5SUS : JP15 page 39
+V1.8 : JP16,19 page 39
+V1.8S : JP17 page42
+V12 : JP18 page 42
+V1.5S : JP22 page 40
+V5A : JP24 page 40
+V3.3A : JP26 or 27 page 39
+V3.3S : JP28 page 42
+V3.3 : JP29 page 42

ASUSTek COMPUTER INC. NB1	Title : POWER DIAGRAM	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 2 of 51	

CPU Pin A1 need to be enlarged(M)



	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4			Pin 1,2

ASUS

Title : CPU-BANIAS(HOST)

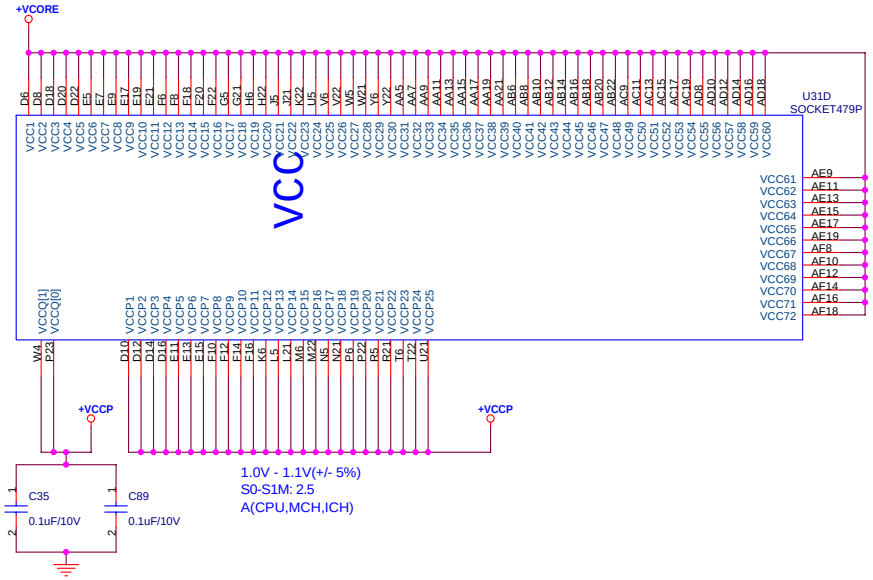
ASUSTek COMPUTER INC. NB1 Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

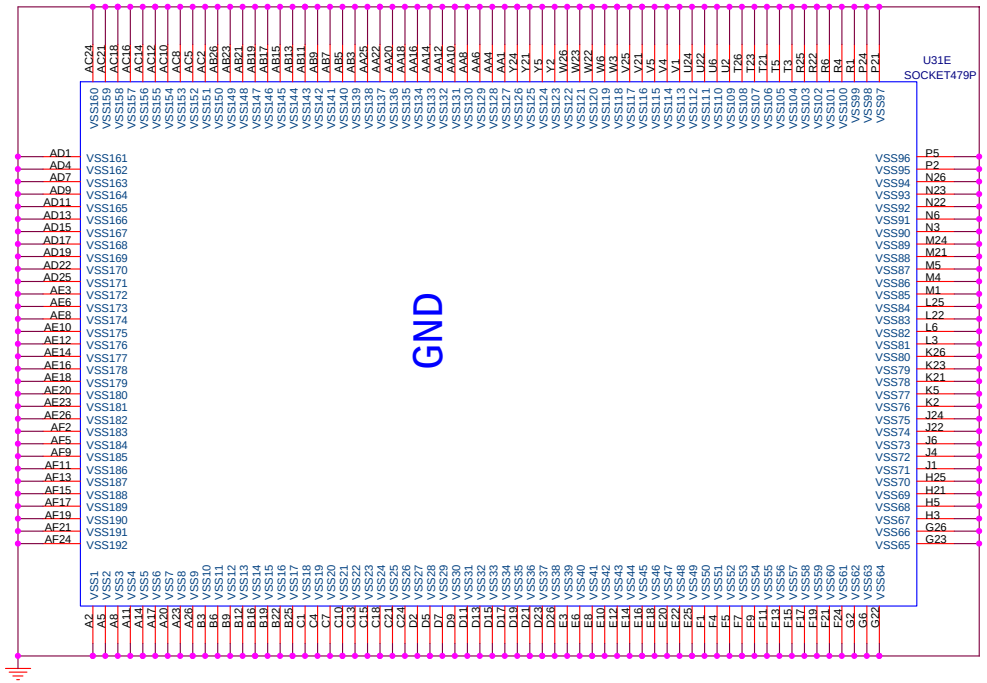
Date: Thursday, October 14, 2004 Sheet 3 of 51

HFM(1.3GHz-1.7GHz): 1.468V
LFM(600MHz): 0.956V

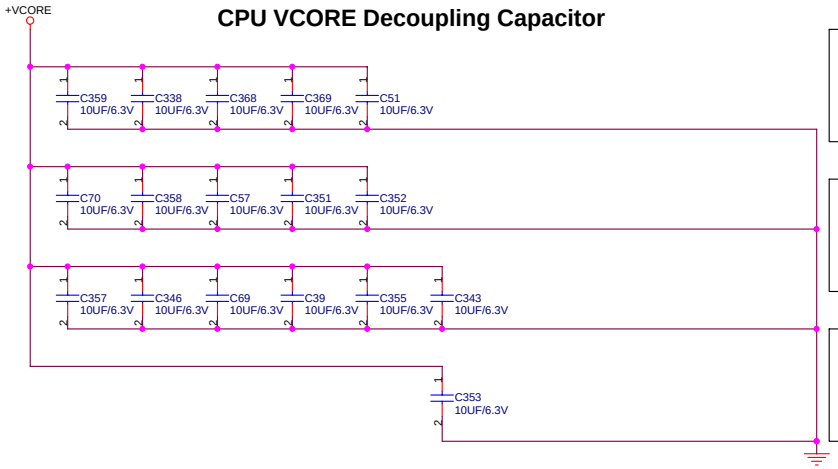
0.745V - 1.356V(+/- 1.5%)
C0: 25 A
C3: 7.59A
C4: 0.9A



1.0V - 1.1V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)



CPU VCORE Decoupling Capacitor



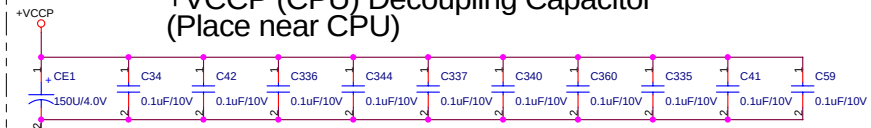
Mid Frequency Decoupling (Place around Processor)

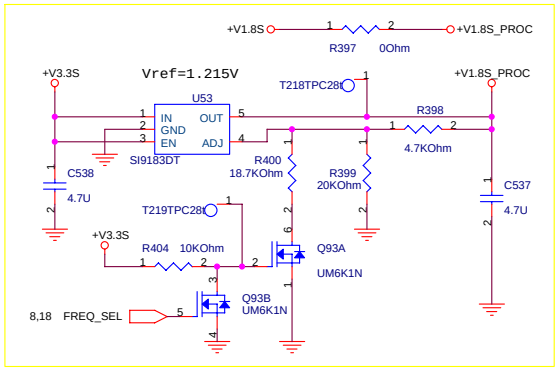
High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

M3N : Four 200 uF are located in IMVP4
A3N : Delete 10uF/6.3V from 35pcs to 17pcs

+VCCP (CPU) Decoupling Capacitor (Place near CPU)





2308

For A3N/A3NE/A3L:
Load R397

For A3LE:
Load C537, C538, Q93, R398, R399, R400, R404, U53

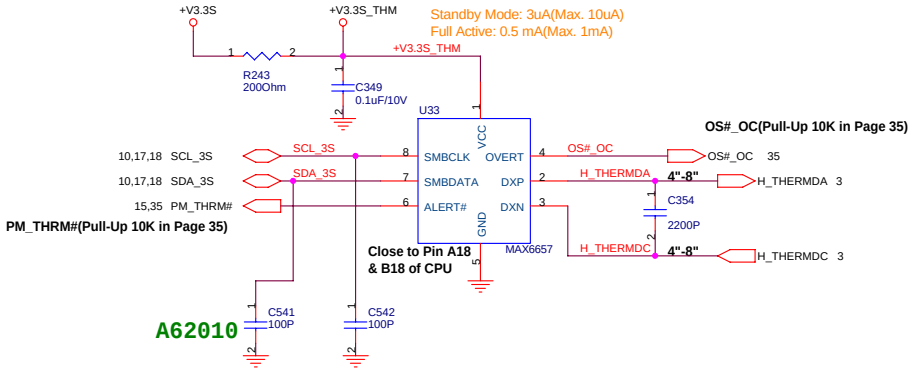
A61004

ASUS	Title : CPU-BANIAS(PWR)	
ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 4 of 51	

Route H_THERMDA and H_THERMDC
on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



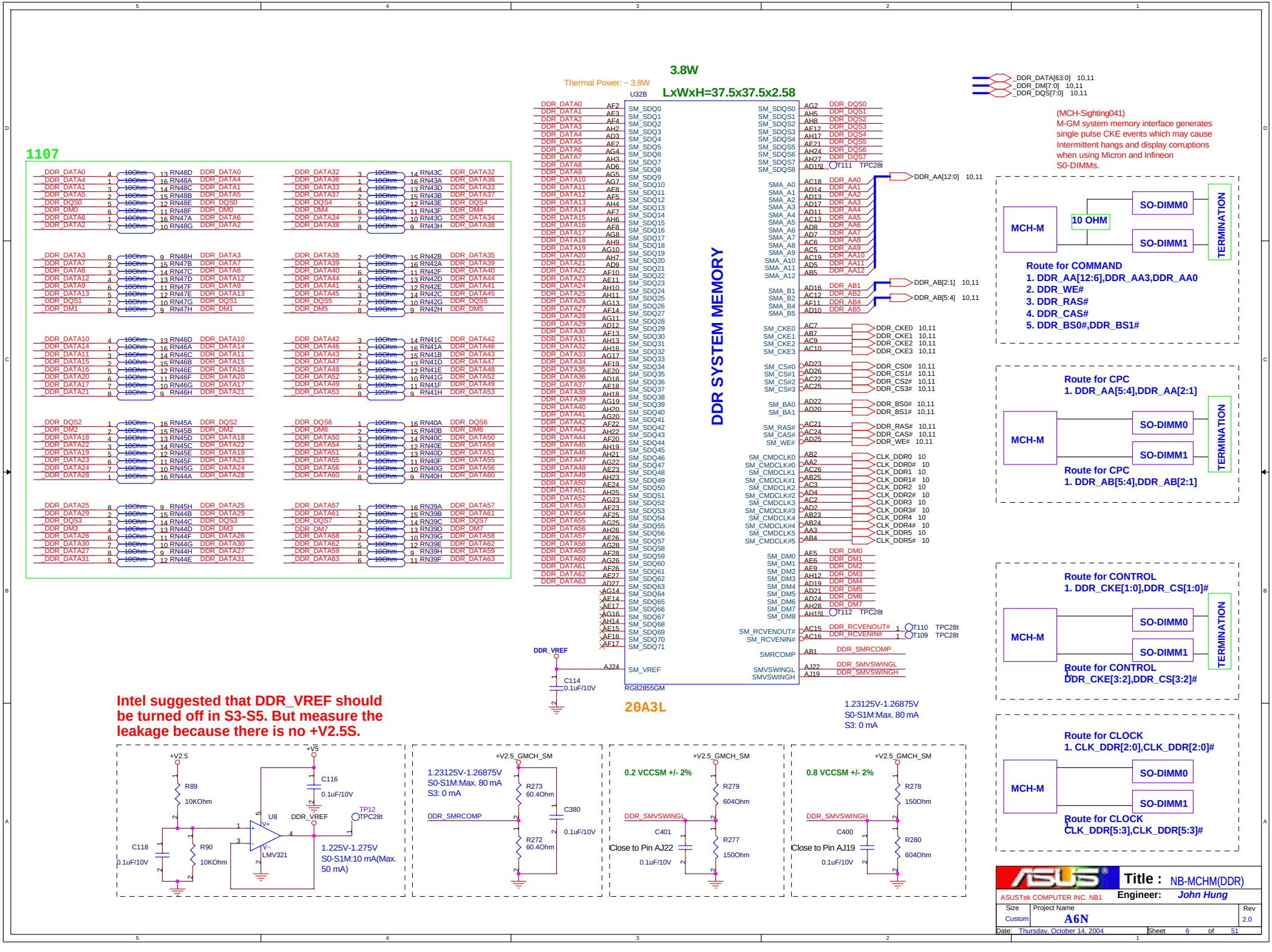
ASUSTek COMPUTER INC. NB1

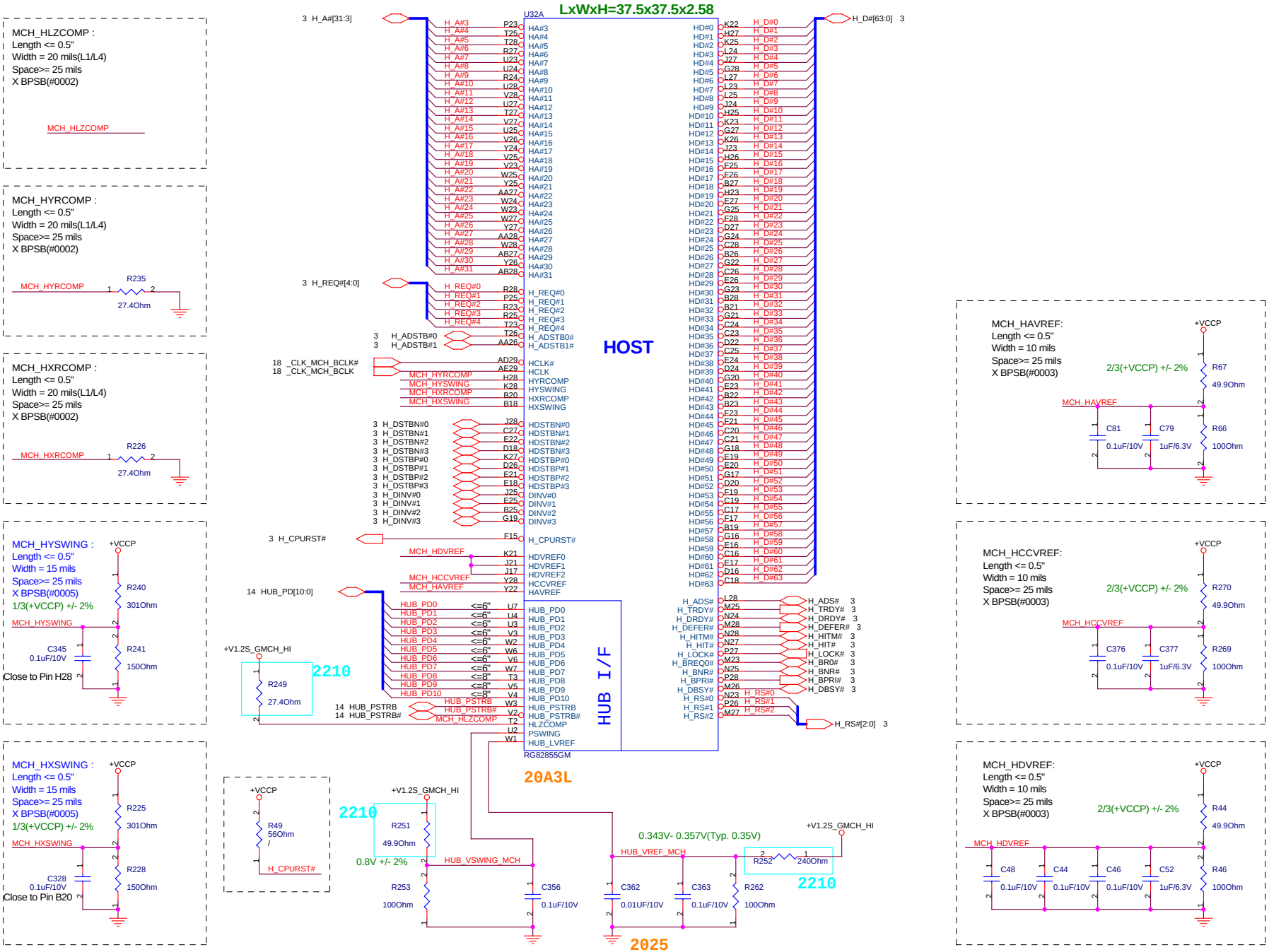
Title : THERMAL

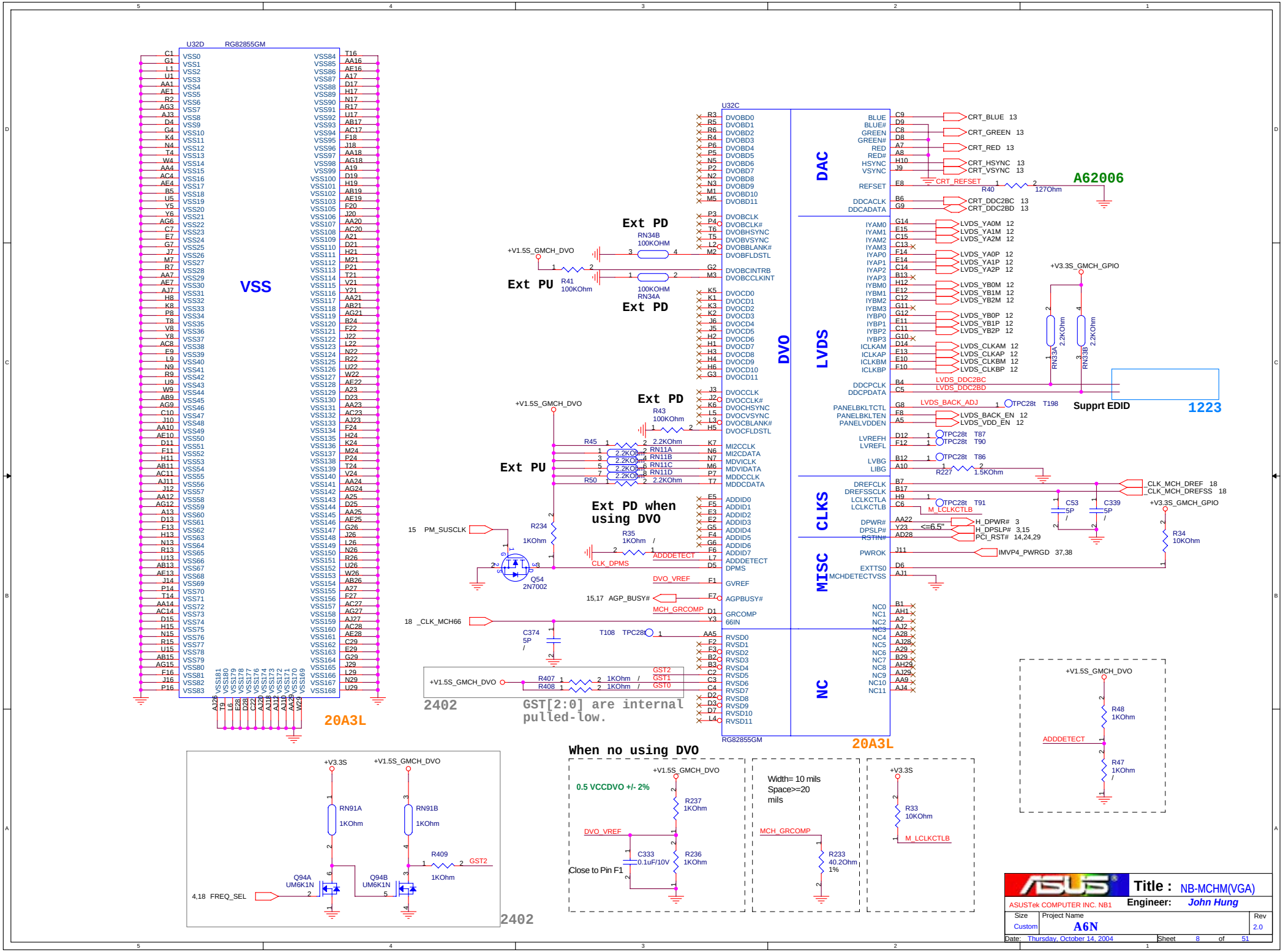
Engineer: John Hung

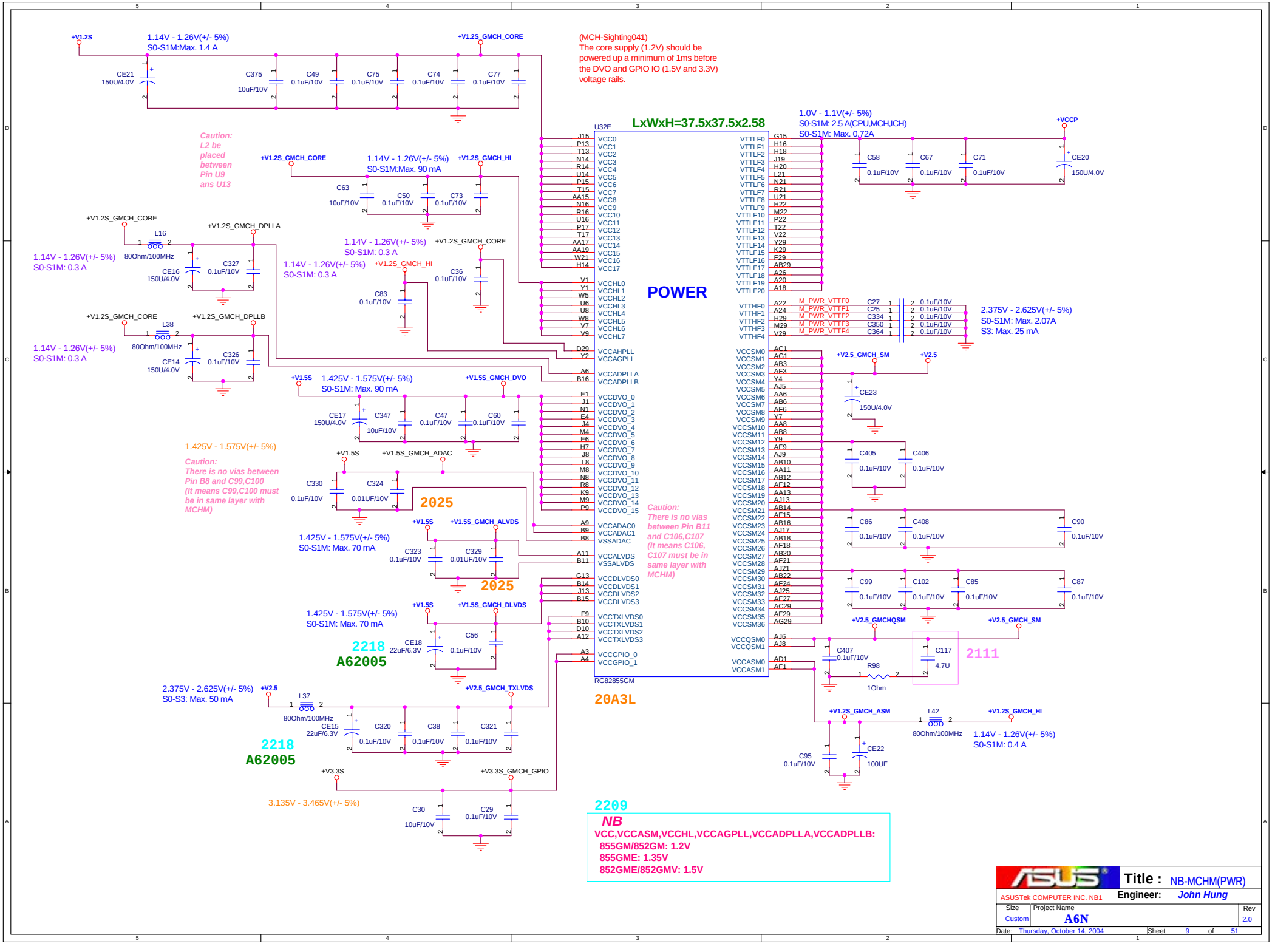
Size	Project Name	Rev
Custom	A6N	2.0

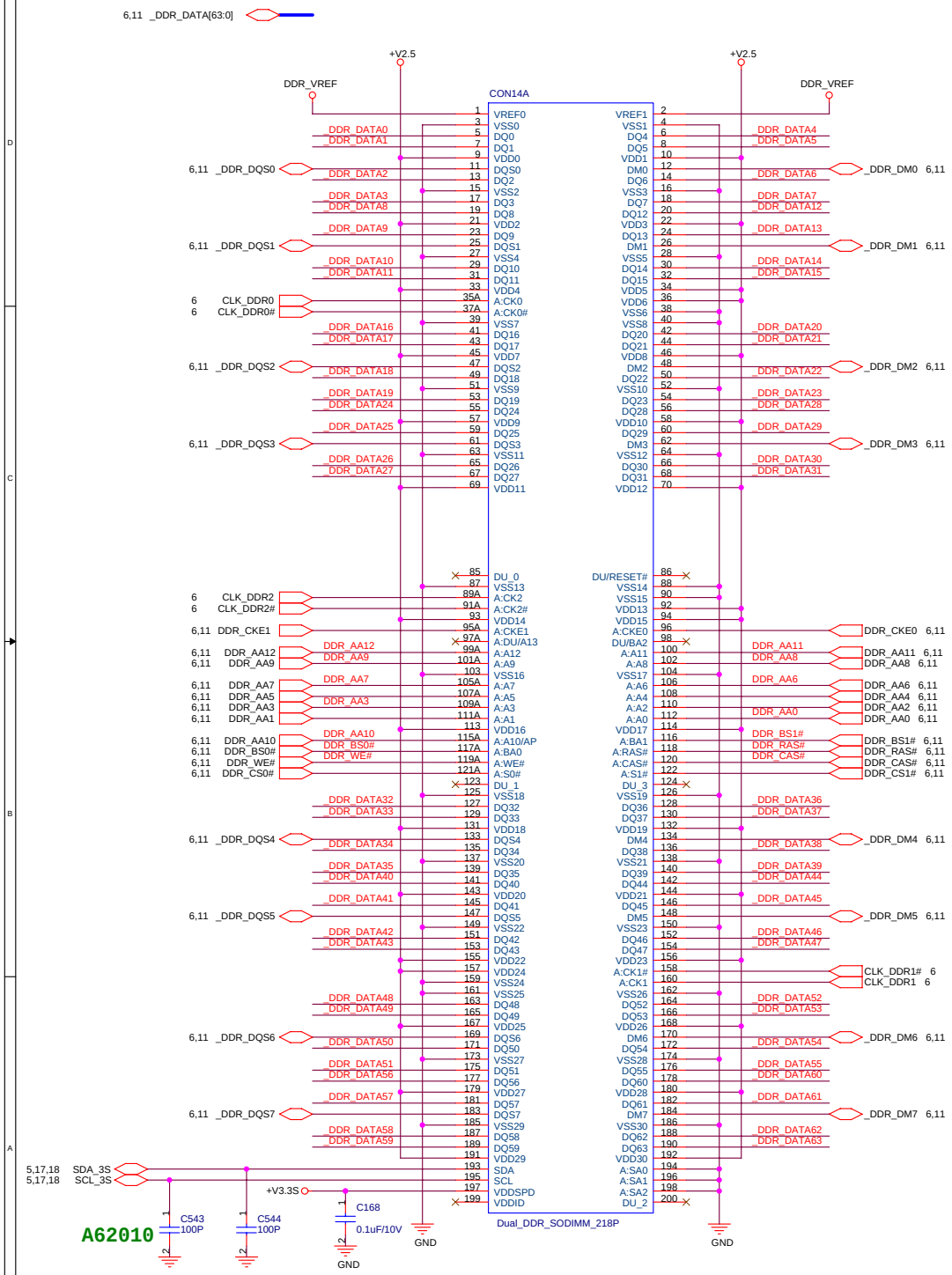
Date: Thursday, October 14, 2004 Sheet 5 of 51


1107
RN48D DDR_DATA0
RN48A DDR_DATA4
RN48C DDR_DATA1
RN48B DDR_DATA5
RN48E DDR_DQS0
RN48F DDR_DM0
RN47A DDR_DATA6
RN48G DDR_DATA2
RN43C DDR_DATA32
RN43A DDR_DATA36
RN43D DDR_DATA33
RN43B DDR_DATA37
RN43E DDR_DQS4
RN43F DDR_DM4
RN43G DDR_DATA34
RN43H DDR_DATA38
RN48H DDR_DATA3
RN47B DDR_DATA7
RN47C DDR_DATA8
RN47D DDR_DATA12
RN47F DDR_DATA9
RN47E DDR_DATA13
RN47G DDR_DQS1
RN47H DDR_DM1
RN42B DDR_DATA35
RN42A DDR_DATA39
RN42F DDR_DATA40
RN42D DDR_DATA44
RN42E DDR_DATA41
RN42C DDR_DATA45
RN42G DDR_DQS5
RN42H DDR_DM5
RN46D DDR_DATA10
RN46A DDR_DATA14
RN46C DDR_DATA11
RN46B DDR_DATA15
RN46E DDR_DATA16
RN46F DDR_DATA20
RN46G DDR_DATA17
RN46H DDR_DATA21
RN41C DDR_DATA42
RN41A DDR_DATA46
RN41B DDR_DATA43
RN41D DDR_DATA47
RN41E DDR_DATA48
RN41G DDR_DATA52
RN41F DDR_DATA49
RN41H DDR_DATA53
RN45A DDR_DQS2
RN45B DDR_DM2
RN45D DDR_DATA18
RN45C DDR_DATA22
RN45E DDR_DATA19
RN45F DDR_DATA23
RN45G DDR_DATA24
RN44A DDR_DATA28
RN40A DDR_DQS6
RN40B DDR_DM6
RN40C DDR_DATA50
RN40E DDR_DATA54
RN40D DDR_DATA51
RN40F DDR_DATA55
RN40G DDR_DATA56
RN40H DDR_DATA60
RN45H DDR_DATA25
RN44B DDR_DATA29
RN44C DDR_DQS3
RN44D DDR_DM3
RN44F DDR_DATA26
RN44G DDR_DATA30
RN44H DDR_DATA27
RN44E DDR_DATA31
RN39A DDR_DATA57
RN39B DDR_DATA61
RN39C DDR_DQS7
RN39D DDR_DM7
RN39G DDR_DATA58
RN39E DDR_DATA62
RN39H DDR_DATA59
RN39F DDR_DATA63
10OHm
3.8W
Thermal Power: ~ 3.8W
LxWxH=37.5x37.5x2.58
U32B
DDR SYSTEM MEMORY
RG82855GM
20A3L
DDR_VREF
C114
0.1uF/10V
1.23125V-1.26875V
S0-S1M:Max. 80 mA
S3: 0 mA
_DDR_DATA[63:0] 10,11
_DDR_DM[7:0] 10,11
_DDR_DQS[7:0] 10,11
DDR_AA[12:0] 10,11
DDR_AB[2:1] 10,11
DDR_AB[5:4] 10,11
(MCH-Sighting041)
M-GM system memory interface generates single pulse CKE events which may cause Intermittent hangs and display corruptions when using Micron and Infineon S0-DIMMs.
MCH-M
10 OHM
SO-DIMM0
SO-DIMM1
TERMINATION
Route for COMMAND
1. DDR_AA[12:6],DDR_AA3,DDR_AA0
2. DDR_WE#
3. DDR_RAS#
4. DDR_CAS#
5. DDR_BS0#,DDR_BS1#
Route for CPC
1. DDR_AA[5:4],DDR_AA[2:1]
Route for CPC
1. DDR_AB[5:4],DDR_AB[2:1]
Route for CONTROL
1. DDR_CKE[1:0],DDR_CS[1:0]#
Route for CONTROL
DDR_CKE[3:2],DDR_CS[3:2]#
Route for CLOCK
1. CLK_DDR[2:0],CLK_DDR[2:0]#
Route for CLOCK
CLK_DDR[5:3],CLK_DDR[5:3]#
Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.
+V2.5
R89
10KOhm
C118
0.1uF/10V
R90
10KOhm
+V5
C116
0.1uF/10V
U8
LMV321
DDR_VREF
TP12
TPC28t
1.225V-1.275V
S0-S1M:10 mA(Max. 50 mA)
+V2.5_GMCH_SM
1.23125V-1.26875V
S0-S1M:Max. 80 mA
S3: 0 mA
DDR_SMRCOMP
R273
60.4Ohm
R272
60.4Ohm
C380
0.1uF/10V
0.2 VCCSM +/- 2%
DDR_SMVSWINGL
C401
Close to Pin AJ22
0.1uF/10V
R279
604Ohm
R277
150Ohm
0.8 VCCSM +/- 2%
DDR_SMVSWINGH
C400
Close to Pin AJ19
0.1uF/10V
R278
150Ohm
R280
604Ohm
Title : NB-MCHM(DDR)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 6 of 51

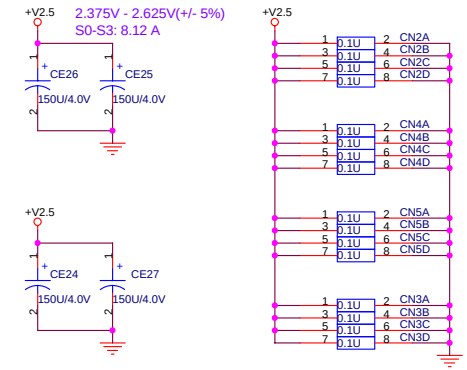

LxWxH=37.5x37.5x2.58
U32A
HOST
HUB I/F
RG82855GM
20A3L
MCH_HLZCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)
MCH_HYRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)
MCH_HXRCOMP :
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0002)
MCH_HYSWING :
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%
Close to Pin H28
MCH_HXSWING :
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%
Close to Pin B20
MCH_HAVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)
2/3(+VCCP) +/- 2%
MCH_HCCVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)
2/3(+VCCP) +/- 2%
MCH_HDVREF:
Length <= 0.5"
Width = 10 mils
Space>= 25 mils
X BPSB(#0003)
2/3(+VCCP) +/- 2%
0.8V +/- 2%
0.343V- 0.357V(Typ. 0.35V)
2210
2025
R249:
27.4ohm (10-003412704) for 855GM/852GM
37.4ohm (10-003413704) for 855GME
48.7ohm (10-003414807) for 852GME/852GMV
R251:
49.9ohm (10-003414909) for 855GM/852GM
68.1ohm (10-003416801) for 855GME
86.6ohm (10-003418606) for 852GME/852GMV
R252:
240ohm (10-003412410) for 855GM/852GM
287ohm (10-003412817) for 855GME
324ohm (10-003413214) for 852GME/852GMV
Title : NB-MCHM(HOST)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 7 of 51

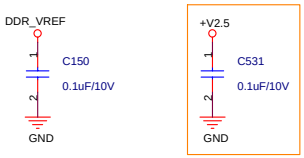

U32D RG82855GM
VSS
20A3L
U32C
DVO
DAC
LVDS
CLKS
MISC
NC
RG82855GM
20A3L
A62006
Supprt EDID
1223
Ext PD
Ext PU
Ext PD when using DVO
RN34B 100KOHM
RN34A 100KOHM
R41 100KOhm
R43 100KOhm
R45 2.2KOhm
R50 2.2KOhm
RN11A 2.2KOhm
RN11B 2.2KOhm
RN11C 2.2KOhm
RN11D 2.2KOhm
R234 1KOhm
R35 1KOhm
Q54 2N7002
R407 1KOhm
R408 1KOhm
GST[2:0] are internal pulled-low.
2402
When no using DVO
0.5 VCCDVO +/- 2%
Close to Pin F1
R237 1KOhm
R236 1KOhm
C333 0.1uF/10V
Width= 10 mils
Space>=20 mils
R233 40.2Ohm 1%
R33 10KOhm
M_LCLKCTLB
R48 1KOhm
R47 1KOhm
ADDDETECT
RN91A 1KOhm
RN91B 1KOhm
R409 1KOhm
Q94A UM6K1N
Q94B UM6K1N
4,18 FREQ_SEL
Title : NB-MCHM(VGA)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 8 of 51


+V1.2S
1.14V - 1.26V(+/- 5%)
S0-S1M:Max. 1.4 A
+V1.2S_GMCH_CORE
CE21 150U/4.0V
C375 10uF/10V
C49 0.1uF/10V
C75 0.1uF/10V
C74 0.1uF/10V
C77 0.1uF/10V
(MCH-Sighting041)
The core supply (1.2V) should be powered up a minimum of 1ms before the DVO and GPIO IO (1.5V and 3.3V) voltage rails.
LxWxH=37.5x37.5x2.58
U32E
POWER
RG82855GM
20A3L
1.0V - 1.1V(+/- 5%)
S0-S1M: 2.5 A(CPU,MCH,ICH)
S0-S1M: Max. 0.72A
+VCCP
C58 0.1uF/10V
C67 0.1uF/10V
C71 0.1uF/10V
CE20 150U/4.0V
Caution:
L2 be placed between Pin U9 ans U13
+V1.2S_GMCH_CORE
1.14V - 1.26V(+/- 5%)
S0-S1M:Max. 90 mA
+V1.2S_GMCH_HI
C63 10uF/10V
C50 0.1uF/10V
C73 0.1uF/10V
+V1.2S_GMCH_CORE
+V1.2S_GMCH_DPLLA
L16
80Ohm/100MHz
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
CE16 150U/4.0V
C327 0.1uF/10V
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
+V1.2S_GMCH_HI
C83 0.1uF/10V
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
+V1.2S_GMCH_CORE
C36 0.1uF/10V
+V1.2S_GMCH_CORE
+V1.2S_GMCH_DPLLB
L38
80Ohm/100MHz
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
CE14 150U/4.0V
C326 0.1uF/10V
+V1.5S
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 90 mA
+V1.5S_GMCH_DVO
CE17 150U/4.0V
C347 10uF/10V
C47 0.1uF/10V
C60 0.1uF/10V
1.425V - 1.575V(+/- 5%)
Caution:
There is no vias between Pin B8 and C99,C100 (It means C99,C100 must be in same layer with MCHM)
+V1.5S
+V1.5S_GMCH_ADAC
C330 0.1uF/10V
C324 0.01UF/10V
2025
+V1.5S
+V1.5S_GMCH_ALVDS
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 70 mA
C323 0.1uF/10V
C329 0.01UF/10V
2025
+V1.5S
+V1.5S_GMCH_DLVDS
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 70 mA
CE18 22uF/6.3V
C56 0.1uF/10V
2218
A62005
2.375V - 2.625V(+/- 5%)
S0-S3: Max. 50 mA
+V2.5
L37
80Ohm/100MHz
CE15 22uF/6.3V
C320 0.1uF/10V
C38 0.1uF/10V
C321 0.1uF/10V
+V2.5_GMCH_TXLVDS
2218
A62005
+V3.3S
+V3.3S_GMCH_GPIO
3.135V - 3.465V(+/- 5%)
C30 10uF/10V
C29 0.1uF/10V
M_PWR_VTTF0 C27
M_PWR_VTTF1 C25
M_PWR_VTTF2 C334
M_PWR_VTTF3 C350
M_PWR_VTTF4 C364
0.1uF/10V
2.375V - 2.625V(+/- 5%)
S0-S1M: Max. 2.07A
S3: Max. 25 mA
+V2.5_GMCH_SM
+V2.5
CE23 150U/4.0V
C405 0.1uF/10V
C406 0.1uF/10V
C86 0.1uF/10V
C408 0.1uF/10V
C90 0.1uF/10V
C99 0.1uF/10V
C102 0.1uF/10V
C85 0.1uF/10V
C87 0.1uF/10V
+V2.5_GMCHQSM
+V2.5_GMCH_SM
C407 0.1uF/10V
R98 1Ohm
C117 4.7U
2111
Caution:
There is no vias between Pin B11 and C106,C107 (It means C106, C107 must be in same layer with MCHM)
+V1.2S_GMCH_ASM
L42
80Ohm/100MHz
+V1.2S_GMCH_HI
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.4 A
C95 0.1uF/10V
CE22 100UF
2209
NB
VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB:
855GM/852GM: 1.2V
855GME: 1.35V
852GME/852GMV: 1.5V
Title : NB-MCHM(PWR)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 9 of 51

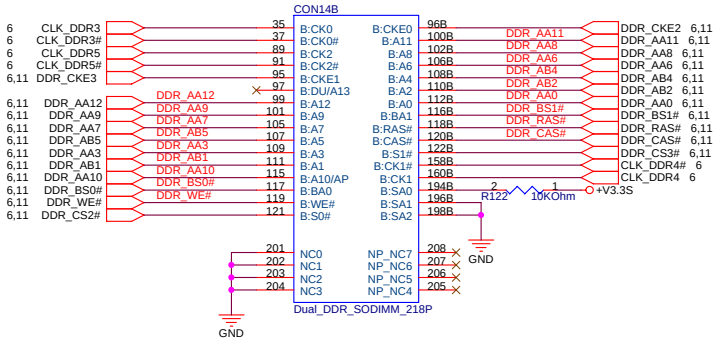


FOR +V2.5 DECOUPLING

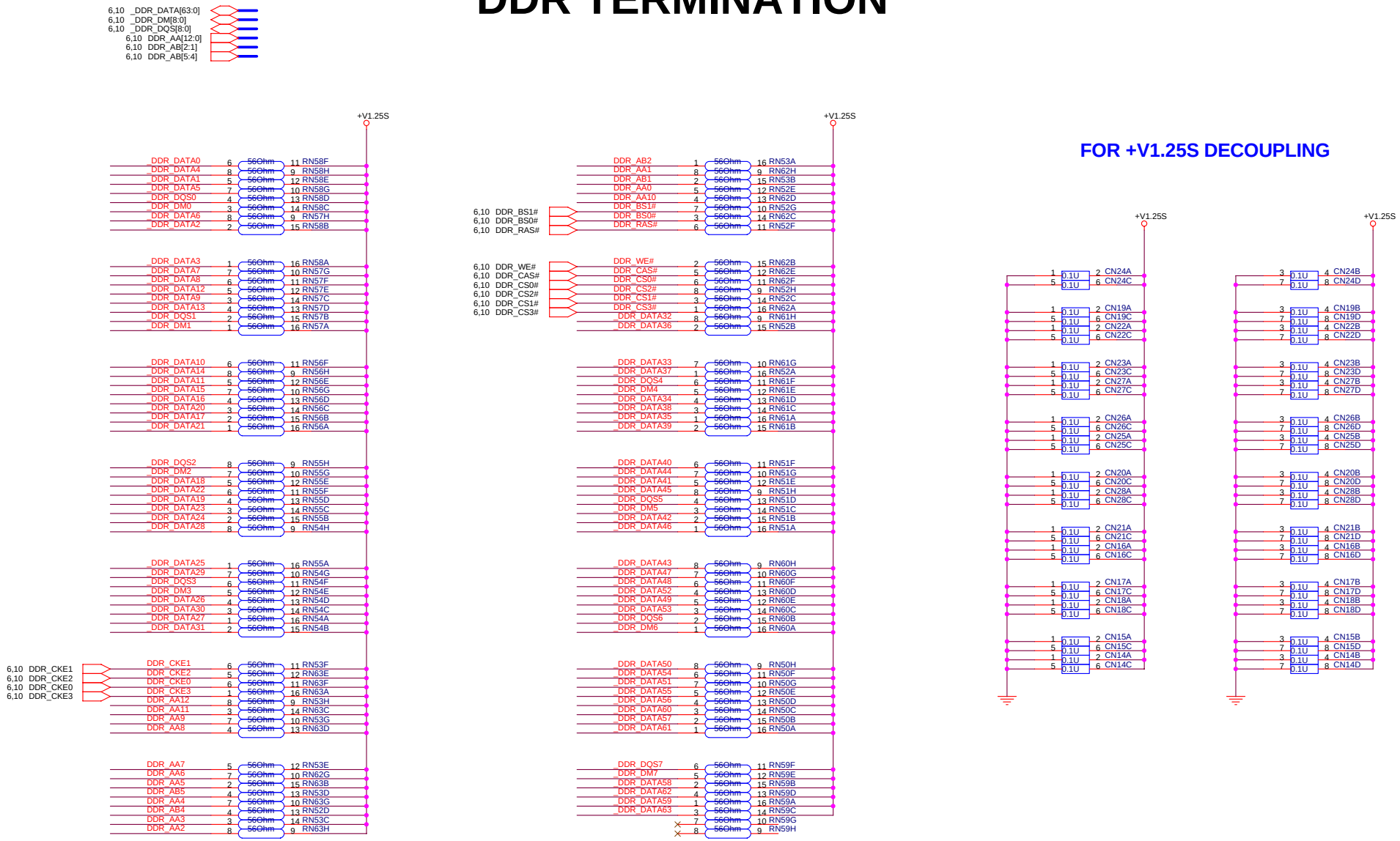




2024
EMI : Close to DDR socket power plane of +V2.5



DDR TERMINATION



ASUS	Title : DDR TERMINATION	
ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 11 of 51	

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output D/A signal (adjust voltage level) to adjust Back light.

A3N use D1 R:1.0 Inverter Board

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

USB PORT 5 for CAMERA

LCD	CABLE ID:	PID3	PID2	PID1	PID0
14.1	XGA	1	1	1	1
15.1	XGA	1	1	0	1
15.1	SXGA+	1	0	1	1
15.1	WXGA	1	1	1	0
15.1	WSXGA+	0	1	1	1

RN86A,B: page 20

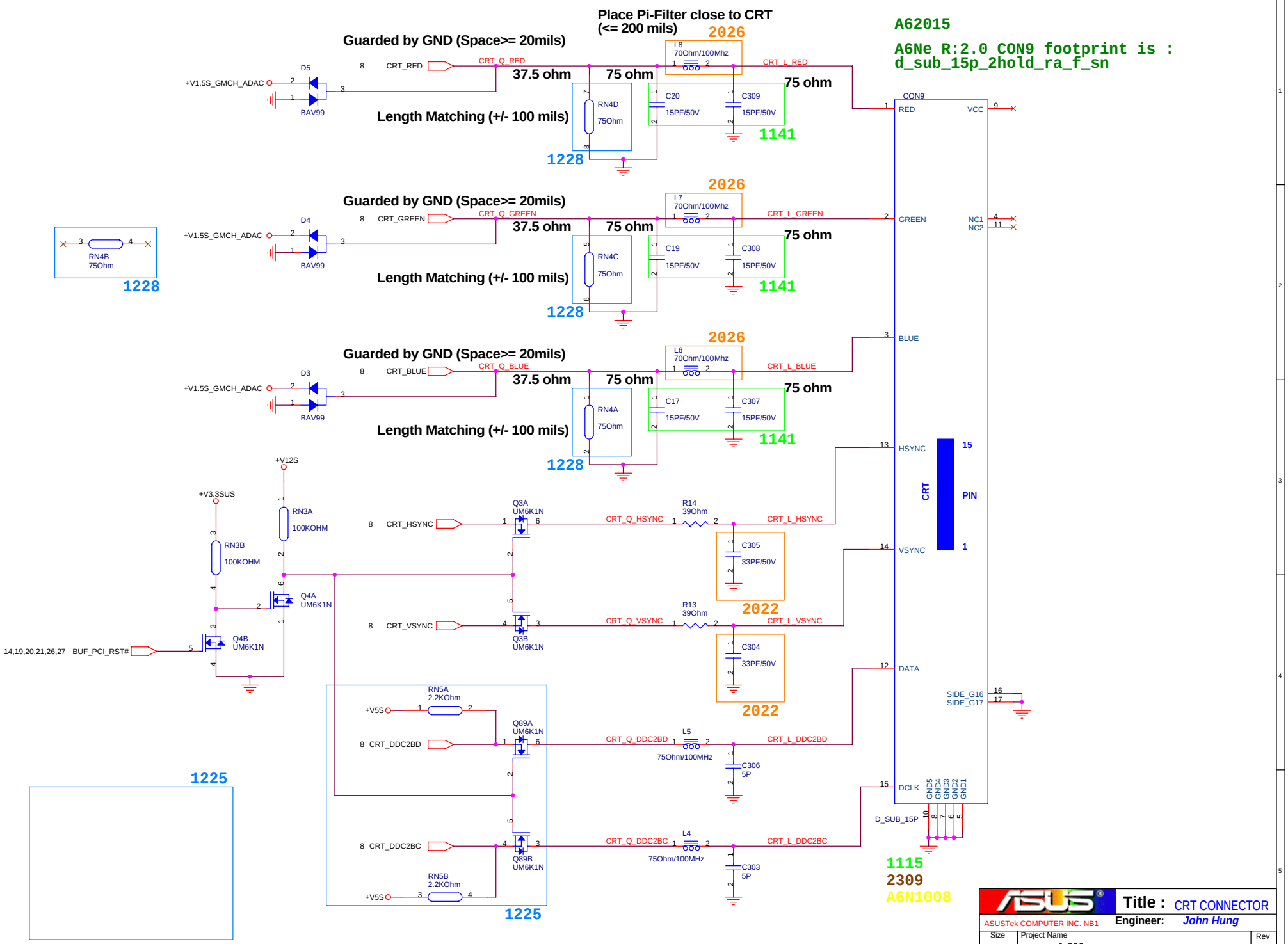
LCD Power

SI3865: US$0.22

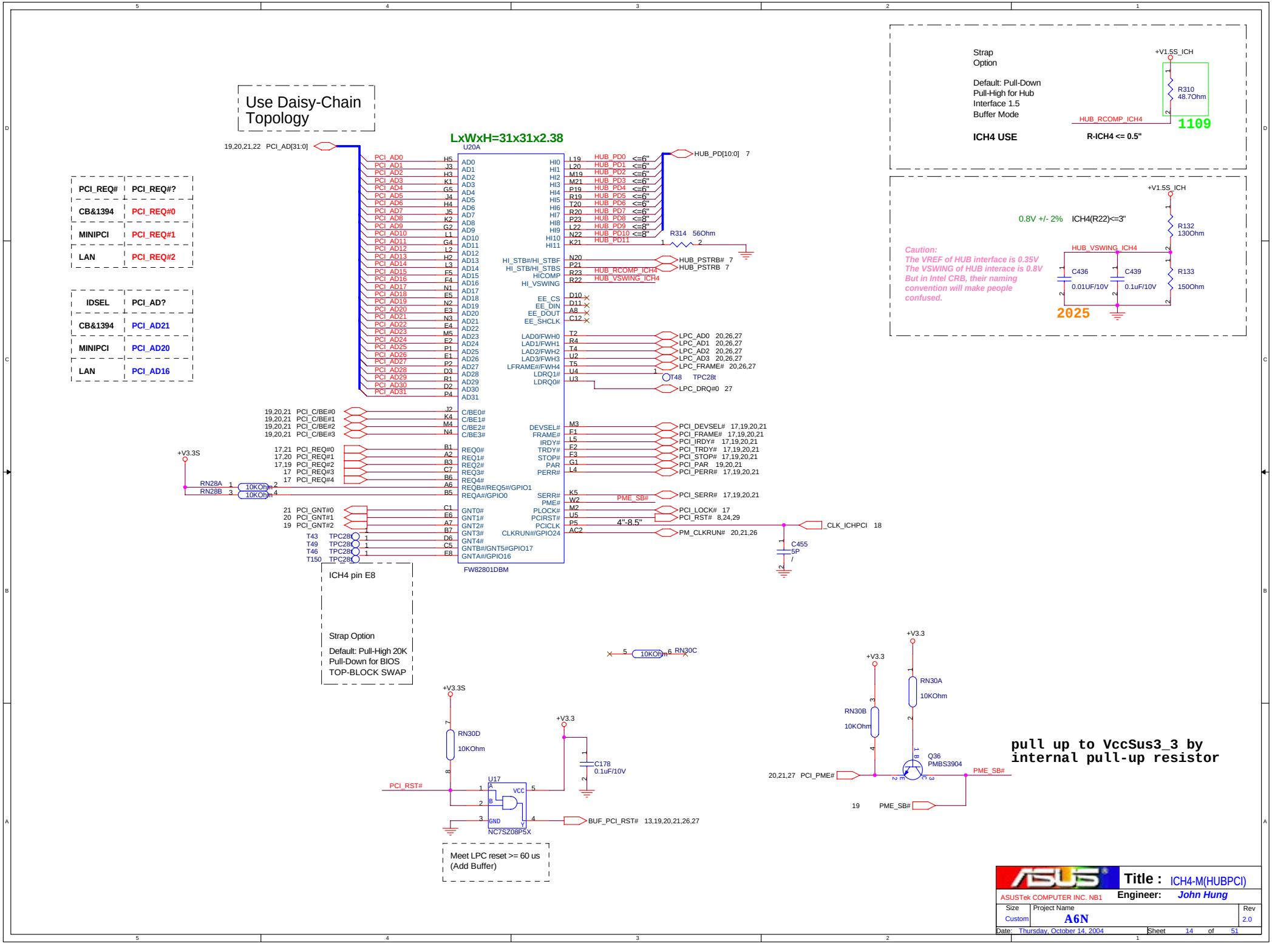
3-3.6V
S0-S1M:410 mA(500 mA Max.)

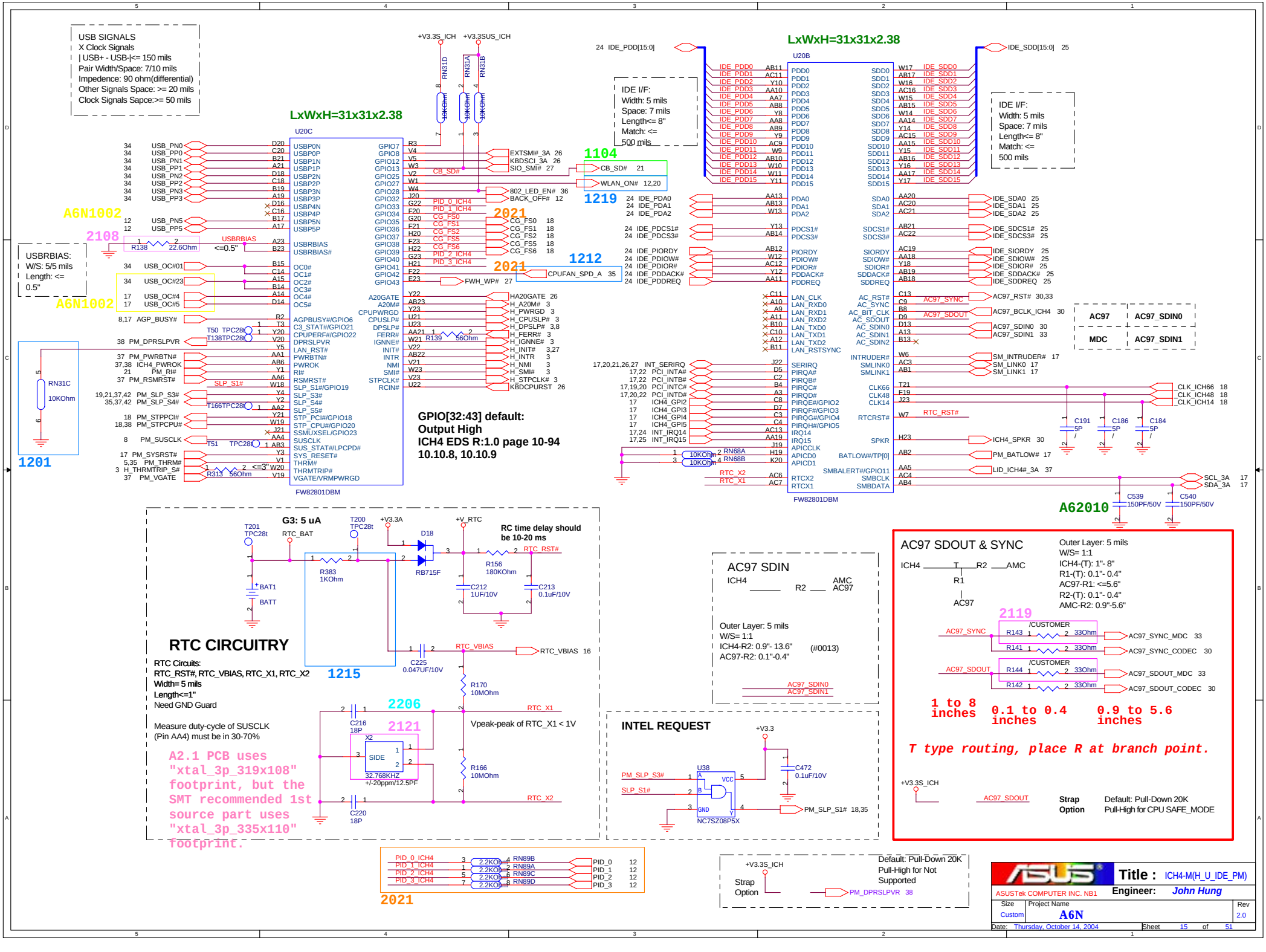
Caution:
Must tune R369 & C270 to meet Panel Spec

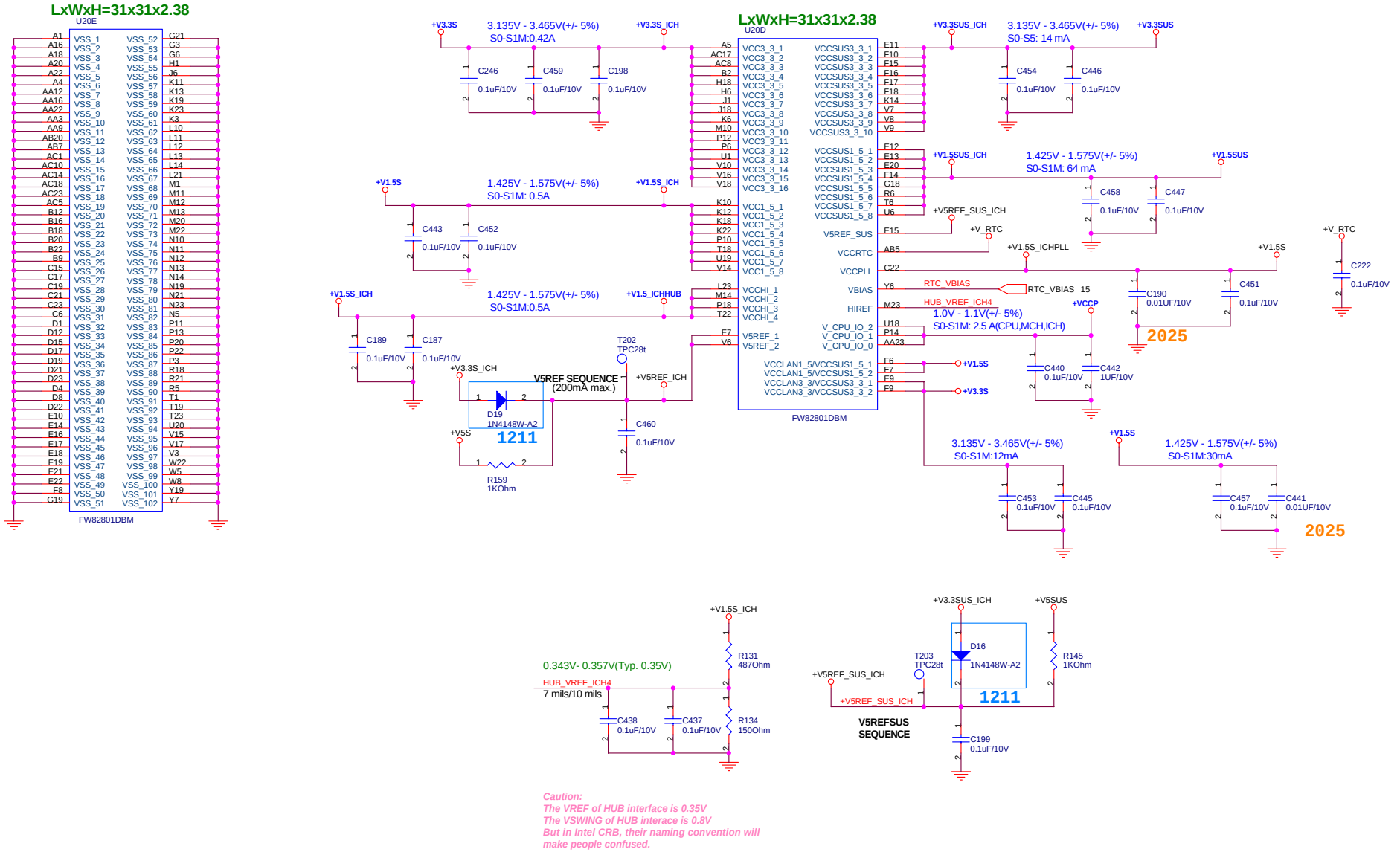
ASUS
Title : LVDS & BACKLIGHT
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size: Custom
Project Name: A6N
Rev: 2.0
Date: Thursday, October 14, 2004
Sheet 12 of 51



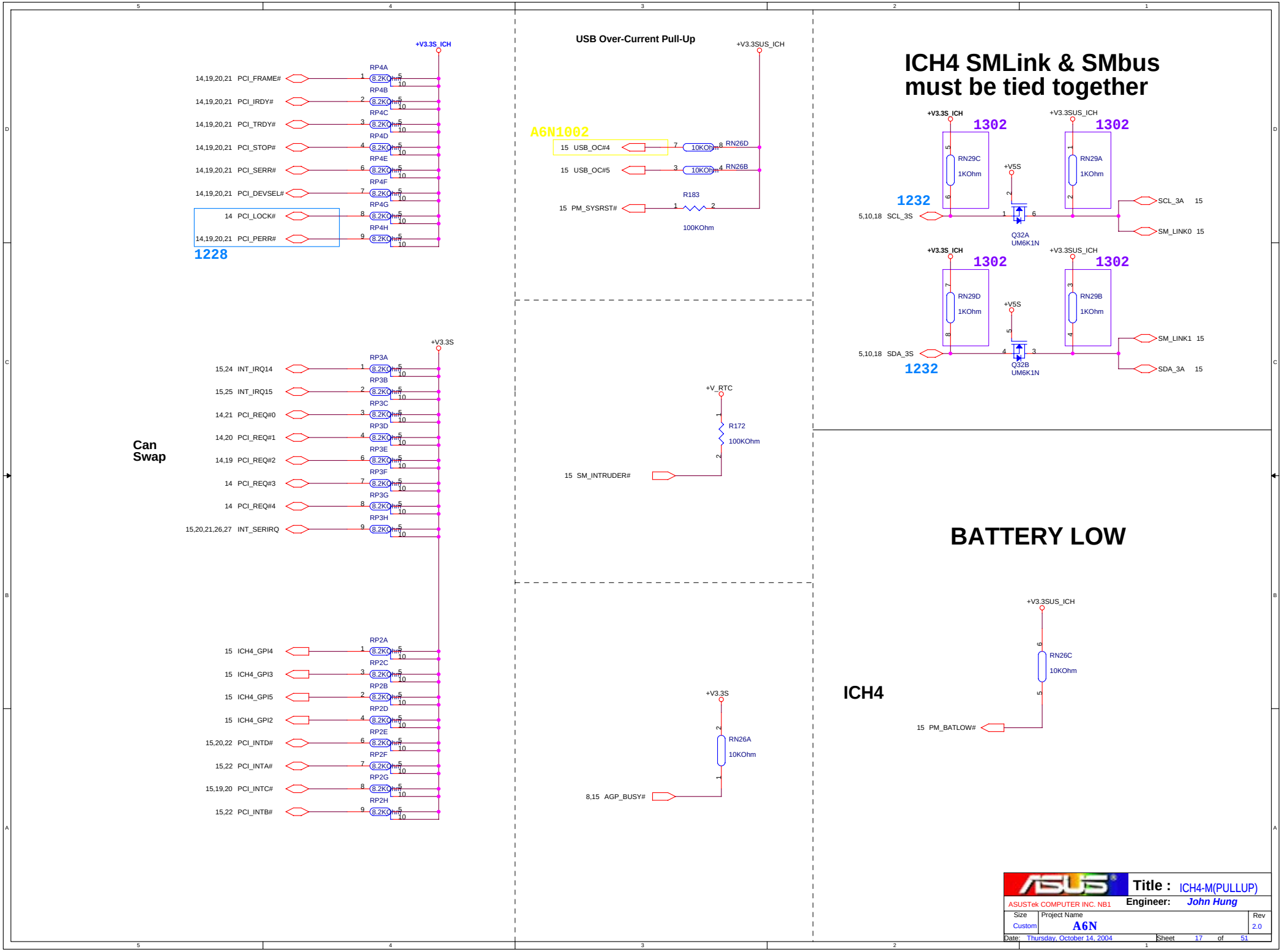
ASUS	Title : CRT CONNECTOR		
ASUSTek COMPUTER INC. NB1	Engineer: John Hung		
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 13 of 51		

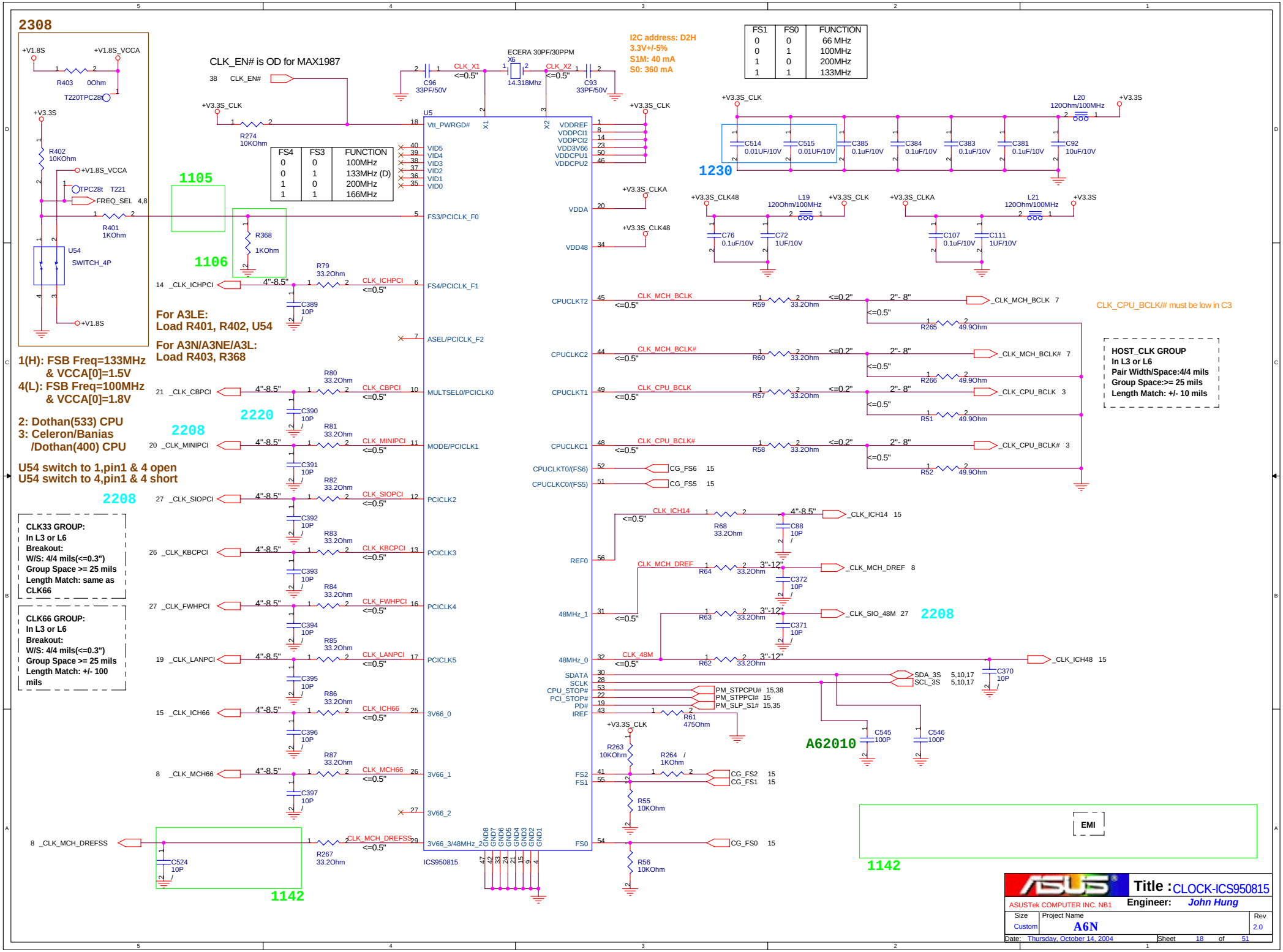

Use Daisy-Chain Topology
LxWxH=31x31x2.38
U20A
FW82801DBM
19,20,21,22 PCI_AD[31:0]
HUB_PD[10:0] 7
PCI_REQ# PCI_REQ?
CB&1394 PCI_REQ#0
MINIPCI PCI_REQ#1
LAN PCI_REQ#2
IDSEL PCI_AD?
CB&1394 PCI_AD21
MINIPCI PCI_AD20
LAN PCI_AD16
R314 56Ohm
HUB_PSTRB# 7
HUB_PSTRB 7
LPC_AD0 20,26,27
LPC_AD1 20,26,27
LPC_AD2 20,26,27
LPC_AD3 20,26,27
LPC_FRAME# 20,26,27
LPC_DRQ#0 27
PCI_DEVSEL# 17,19,20,21
PCI_FRAME# 17,19,20,21
PCI_IRDY# 17,19,20,21
PCI_TRDY# 17,19,20,21
PCI_STOP# 17,19,20,21
PCI_PAR 19,20,21
PCI_PERR# 17,19,20,21
PCI_SERR# 17,19,20,21
PCI_LOCK# 17
PCI_RST# 8,24,29
PM_CLKRUN# 20,21,26
CLK_ICHPCI 18
C455 5P
+V3.3S
RN28A 10KOhm
RN28B 10KOhm
ICH4 pin E8
Strap Option
Default: Pull-High 20K
Pull-Down for BIOS
TOP-BLOCK SWAP
RN30C 10KOhm
+V3.3S
RN30D 10KOhm
+V3.3
C178 0.1uF/10V
U17
NC7SZ08P5X
PCI_RST#
BUF_PCI_RST# 13,19,20,21,26,27
Meet LPC reset >= 60 us
(Add Buffer)
+V3.3
RN30A 10KOhm
RN30B 10KOhm
Q36 PMBS3904
20,21,27 PCI_PME#
PME_SB#
19 PME_SB#
pull up to VccSus3_3 by internal pull-up resistor
Strap Option
Default: Pull-Down
Pull-High for Hub
Interface 1.5
Buffer Mode
ICH4 USE
+V1.5S_ICH
R310 48.7Ohm
HUB_RCOMP_ICH4
1109
R-ICH4 <= 0.5"
0.8V +/- 2%
ICH4(R22)<=3"
R132 130Ohm
HUB_VSWING_ICH4
C436 0.01UF/10V
C439 0.1uF/10V
R133 150Ohm
2025
Caution:
The VREF of HUB interface is 0.35V
The VSWING of HUB interace is 0.8V
But in Intel CRB, their naming convention will make people confused.
Title : ICH4-M(HUBPCI)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 14 of 51

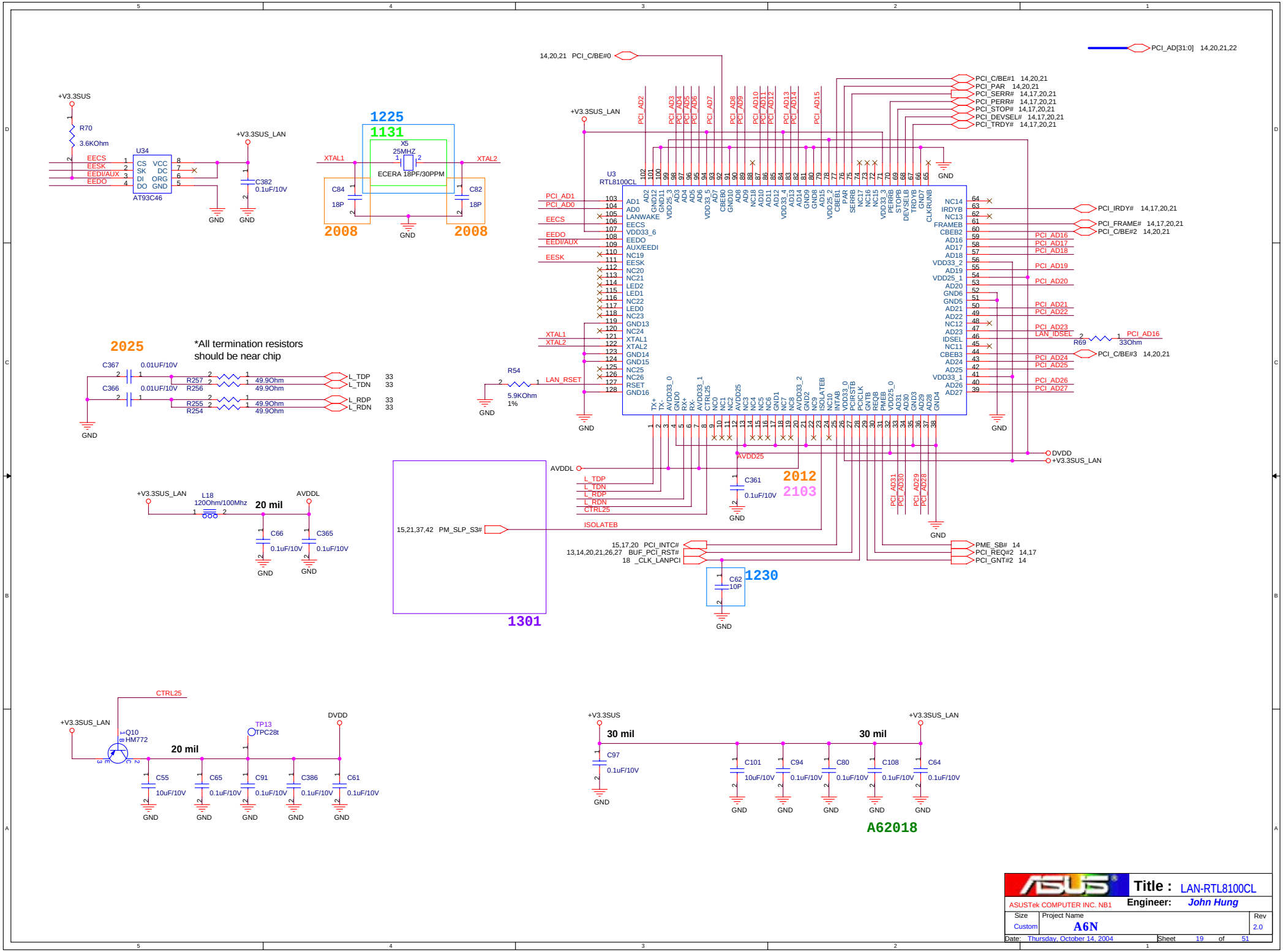

USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Pair Width/Space: 7/10 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils
LxWxH=31x31x2.38
U20C
FW82801DBM
A6N1002
2108
USBRBIAS:
W/S: 5/5 mils
Length: <= 0.5"
1201
RN31C
10KOhm
GPIO[32:43] default:
Output High
ICH4 EDS R:1.0 page 10-94
10.10.8, 10.10.9
1104
1219
1212
2021
IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils
LxWxH=31x31x2.38
U20B
FW82801DBM
AC97
AC97_SDIN0
MDC
AC97_SDIN1
A62010
G3: 5 uA
RC time delay should be 10-20 ms
RTC CIRCUITRY
RTC Circuits:
RTC_RST#, RTC_VBIAS, RTC_X1, RTC_X2
Width= 5 mils
Length<=1"
Need GND Guard
Measure duty-cycle of SUSCLK (Pin AA4) must be in 30-70%
A2.1 PCB uses "xtal_3p_319x108" footprint, but the SMT recommended 1st source part uses "xtal_3p_335x110" footprint.
1215
2206
2121
Vpeak-peak of RTC_X1 < 1V
AC97 SDIN
Outer Layer: 5 mils
W/S= 1:1
ICH4-R2: 0.9"- 13.6"
AC97-R2: 0.1"-0.4"
(#0013)
INTEL REQUEST
AC97 SDOUT & SYNC
Outer Layer: 5 mils
W/S= 1:1
ICH4-(T): 1"- 8"
R1-(T): 0.1"- 0.4"
AC97-R1: <=5.6"
R2-(T): 0.1"- 0.4"
AMC-R2: 0.9"-5.6"
2119
1 to 8 inches
0.1 to 0.4 inches
0.9 to 5.6 inches
T type routing, place R at branch point.
Strap Option
Default: Pull-Down 20K
Pull-High for CPU SAFE_MODE
Default: Pull-Down 20K
Pull-High for Not Supported
Title : ICH4-M(H_U_IDE_PM)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 15 of 51

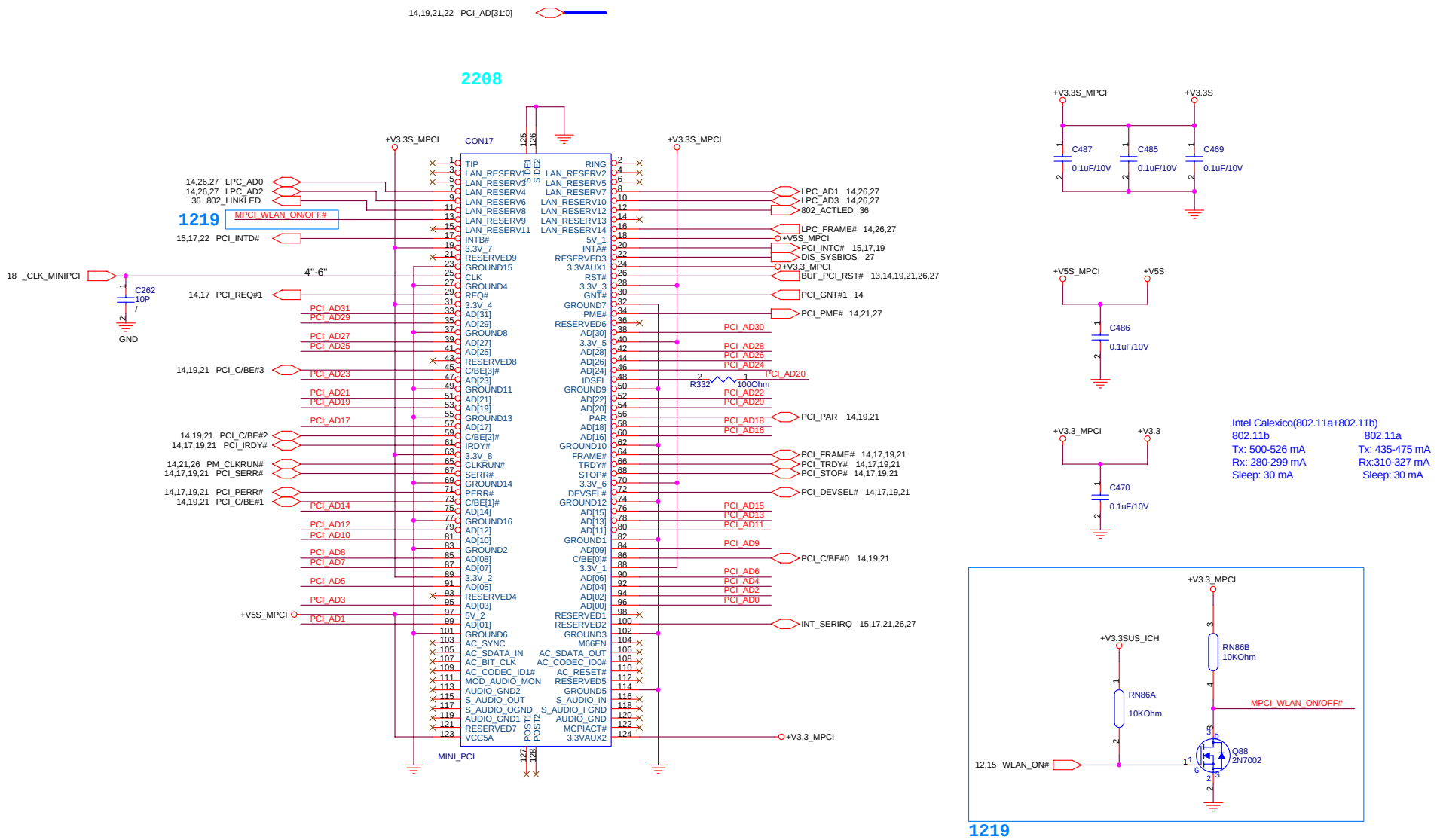


ASUSTek COMPUTER INC. NB1	Title : ICH4-M(PWR)
	Engineer: John Hung
Size: Custom	Project Name: A6N
Rev: 2.0	
Date: Thursday, October 14, 2004	Sheet 16 of 51

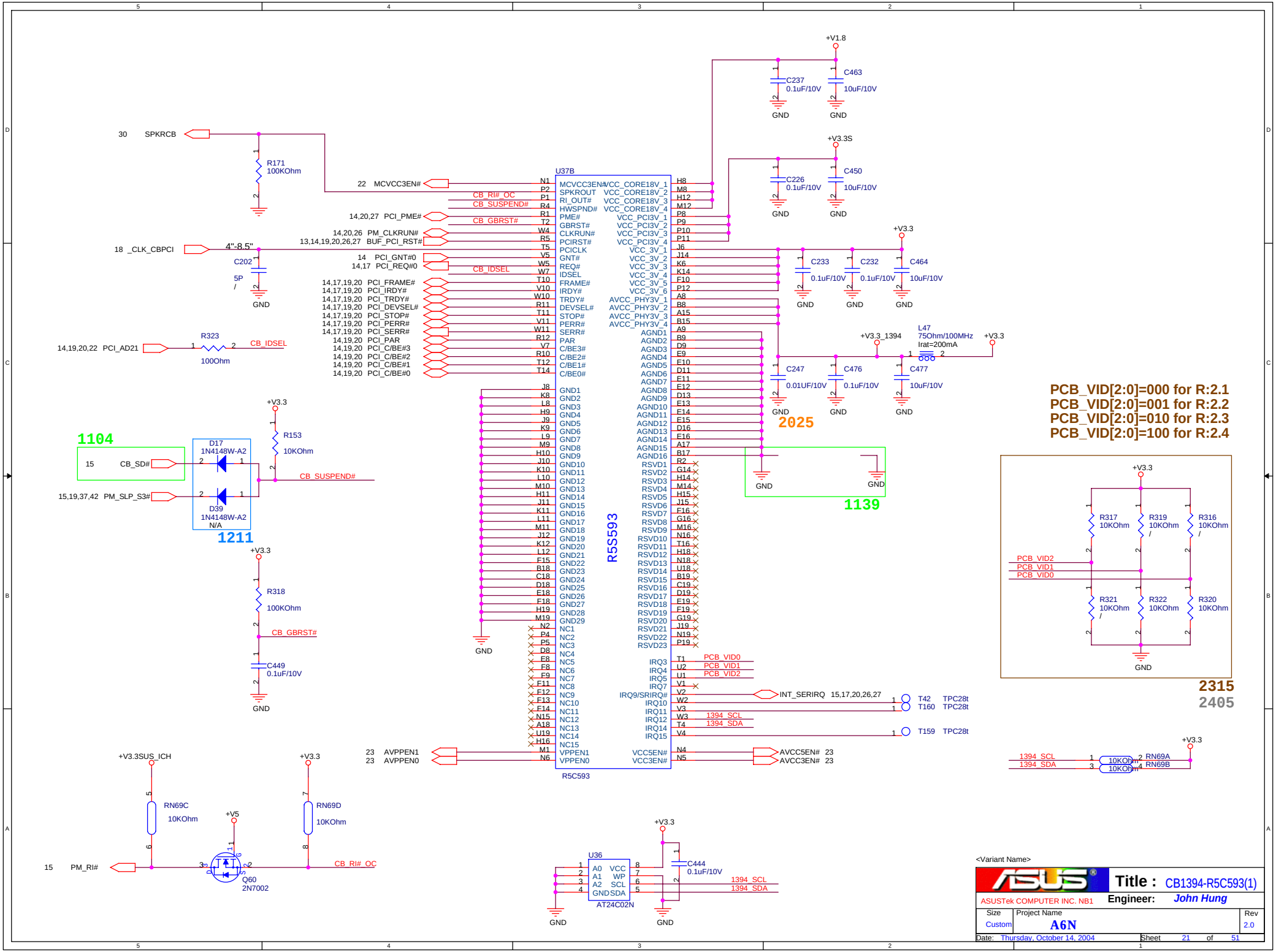

+V3.3S_ICH
14,19,20,21 PCI_FRAME# RP4A 8.2KOhm
14,19,20,21 PCI_IRDY# RP4B 8.2KOhm
14,19,20,21 PCI_TRDY# RP4C 8.2KOhm
14,19,20,21 PCI_STOP# RP4D 8.2KOhm
14,19,20,21 PCI_SERR# RP4E 8.2KOhm
14,19,20,21 PCI_DEVSEL# RP4F 8.2KOhm
14 PCI_LOCK# RP4G 8.2KOhm
14,19,20,21 PCI_PERR# RP4H 8.2KOhm
1228
USB Over-Current Pull-Up
+V3.3SUS_ICH
A6N1002
15 USB_OC#4 10KOhm RN26D
15 USB_OC#5 10KOhm RN26B
15 PM_SYSRST# R183 100KOhm
ICH4 SMLink & SMbus must be tied together
+V3.3S_ICH
+V3.3SUS_ICH
1302
RN29C 1KOhm
RN29A 1KOhm
+V5S
1232
5,10,18 SCL_3S
Q32A UM6K1N
SCL_3A 15
SM_LINK0 15
RN29D 1KOhm
RN29B 1KOhm
5,10,18 SDA_3S
Q32B UM6K1N
SM_LINK1 15
SDA_3A 15
Can Swap
+V3.3S
15,24 INT_IRQ14 RP3A 8.2KOhm
15,25 INT_IRQ15 RP3B 8.2KOhm
14,21 PCI_REQ#0 RP3C 8.2KOhm
14,20 PCI_REQ#1 RP3D 8.2KOhm
14,19 PCI_REQ#2 RP3E 8.2KOhm
14 PCI_REQ#3 RP3F 8.2KOhm
14 PCI_REQ#4 RP3G 8.2KOhm
15,20,21,26,27 INT_SERIRQ RP3H 8.2KOhm
+V_RTC
R172 100KOhm
15 SM_INTRUDER#
BATTERY LOW
ICH4
+V3.3SUS_ICH
RN26C 10KOhm
15 PM_BATLOW#
15 ICH4_GPI4 RP2A 8.2KOhm
15 ICH4_GPI3 RP2C 8.2KOhm
15 ICH4_GPI5 RP2B 8.2KOhm
15 ICH4_GPI2 RP2D 8.2KOhm
15,20,22 PCI_INTD# RP2E 8.2KOhm
15,22 PCI_INTA# RP2F 8.2KOhm
15,19,20 PCI_INTC# RP2G 8.2KOhm
15,22 PCI_INTB# RP2H 8.2KOhm
+V3.3S
RN26A 10KOhm
8,15 AGP_BUSY#
Title : ICH4-M(PULLUP)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 17 of 51

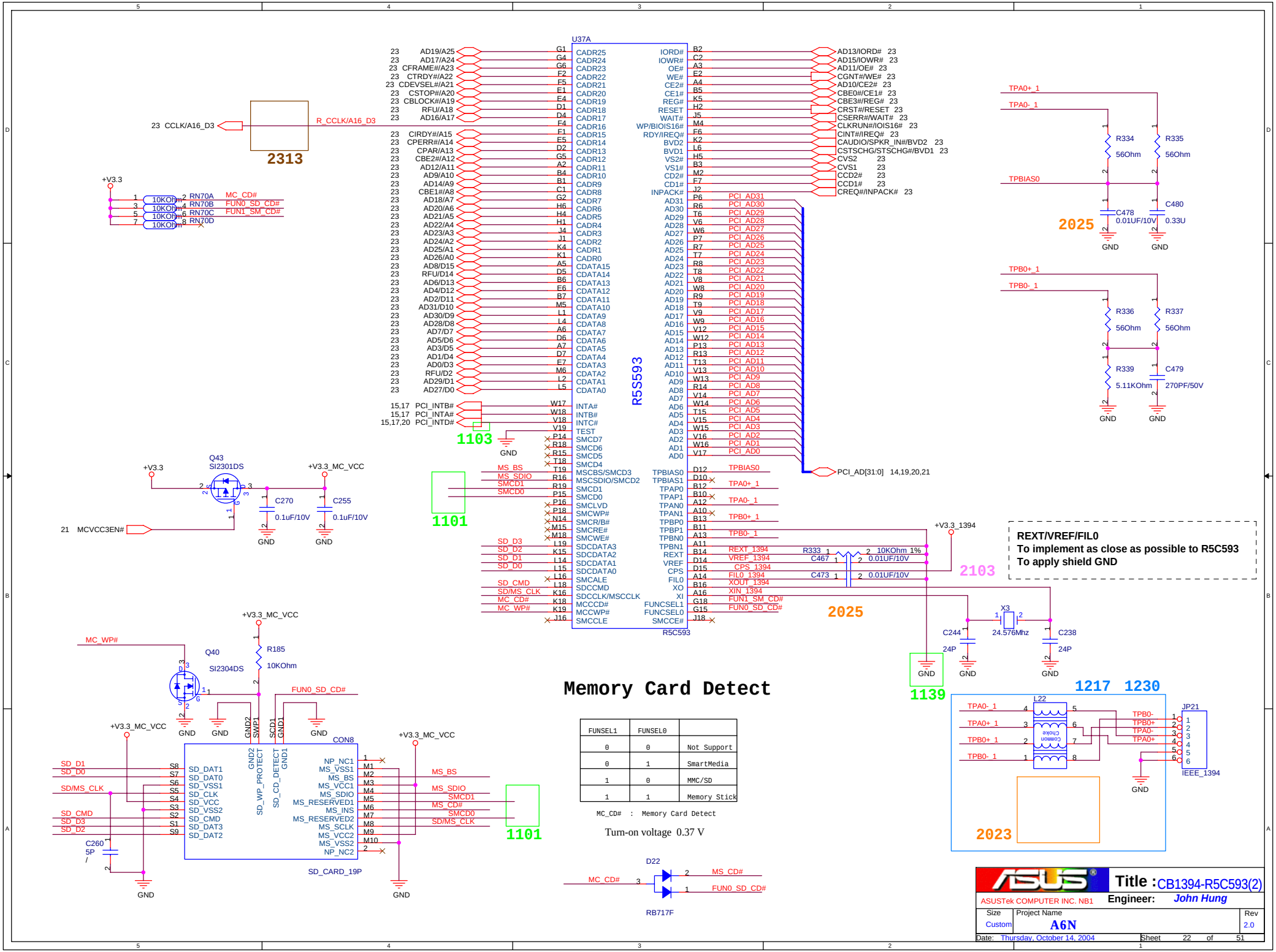

2308
+V1.8S
+V1.8S_VCCA
R403 0Ohm
T220TPC28t
+V3.3S
R402 10KOhm
+V1.8S_VCCA
TPC28t T221
FREQ_SEL 4,8
R401 1KOhm
U54
SWITCH_4P
+V1.8S
1(H): FSB Freq=133MHz & VCCA[0]=1.5V
4(L): FSB Freq=100MHz & VCCA[0]=1.8V
2: Dothan(533) CPU
3: Celeron/Banias /Dothan(400) CPU
U54 switch to 1,pin1 & 4 open
U54 switch to 4,pin1 & 4 short
2208
CLK33 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: same as CLK66
CLK66 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3")
Group Space >= 25 mils
Length Match: +/- 100 mils
CLK_EN# is OD for MAX1987
38 CLK_EN#
+V3.3S_CLK
R274 10KOhm
1105
1106
R368 1KOhm
For A3LE:
Load R401, R402, U54
For A3N/A3NE/A3L:
Load R403, R368
FS4 FS3 FUNCTION
0 0 100MHz
0 1 133MHz (D)
1 0 200MHz
1 1 166MHz
C96 33PF/50V
CLK_X1 <=0.5"
ECERA 30PF/30PPM
X6
14.318Mhz
CLK_X2 <=0.5"
C93 33PF/50V
U5
Vtt_PWRGD#
VID5
VID4
VID3
VID2
VID1
VID0
FS3/PCICLK_F0
FS4/PCICLK_F1
ASEL/PCICLK_F2
MULTSEL0/PCICLK0
MODE/PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5
3V66_0
3V66_1
3V66_2
3V66_3/48MHz_2
ICS950815
VDDREF
VDDPCI1
VDDPCI2
VDD3V66
VDDCPU1
VDDCPU2
VDDA
VDD48
CPUCLKT2
CPUCLKC2
CPUCLKT1
CPUCLKC1
CPUCLKT0/(FS6)
CPUCLKC0/(FS5)
REF0
48MHz_1
48MHz_0
SDATA
SCLK
CPU_STOP#
PCI_STOP#
PD#
IREF
FS2
FS1
FS0
_CLK_ICHPCI
_CLK_CBPCI
_CLK_MINIPCI
_CLK_SIOPCI
_CLK_KBCPCI
_CLK_FWHPCI
_CLK_LANPCI
_CLK_ICH66
_CLK_MCH66
_CLK_MCH_DREFSS
CLK_ICHPCI
CLK_CBPCI
CLK_MINIPCI
CLK_SIOPCI
CLK_KBCPCI
CLK_FWHPCI
CLK_LANPCI
CLK_ICH66
CLK_MCH66
CLK_MCH_DREFSS
R79 33.2Ohm
R80 33.2Ohm
R81 33.2Ohm
R82 33.2Ohm
R83 33.2Ohm
R84 33.2Ohm
R85 33.2Ohm
R86 33.2Ohm
R87 33.2Ohm
R267 33.2Ohm
C389 10P
C390 10P
C391 10P
C392 10P
C393 10P
C394 10P
C395 10P
C396 10P
C397 10P
C524 10P
2220
2208
1142
I2C address: D2H
3.3V+/-5%
S1M: 40 mA
S0: 360 mA
FS1 FS0 FUNCTION
0 0 66 MHz
0 1 100MHz
1 0 200MHz
1 1 133MHz
+V3.3S_CLK
L20 120Ohm/100MHz
+V3.3S
C514 0.01UF/10V
C515 0.01UF/10V
C385 0.1uF/10V
C384 0.1uF/10V
C383 0.1uF/10V
C381 0.1uF/10V
C92 10uF/10V
1230
+V3.3S_CLKA
+V3.3S_CLK48
L19 120Ohm/100MHz
C76 0.1uF/10V
C72 1UF/10V
L21 120Ohm/100MHz
C107 0.1uF/10V
C111 1UF/10V
CLK_MCH_BCLK
CLK_MCH_BCLK#
CLK_CPU_BCLK
CLK_CPU_BCLK#
R59 33.2Ohm
R60 33.2Ohm
R57 33.2Ohm
R58 33.2Ohm
R265 49.9Ohm
R266 49.9Ohm
R51 49.9Ohm
R52 49.9Ohm
<=0.2"
2"- 8"
_CLK_MCH_BCLK 7
_CLK_MCH_BCLK# 7
_CLK_CPU_BCLK 3
_CLK_CPU_BCLK# 3
CLK_CPU_BCLK/# must be low in C3
HOST_CLK GROUP
In L3 or L6
Pair Width/Space:4/4 mils
Group Space:>= 25 mils
Length Match: +/- 10 mils
CG_FS6 15
CG_FS5 15
CLK_ICH14
R68 33.2Ohm
C88 10P
_CLK_ICH14 15
CLK_MCH_DREF
R64 33.2Ohm
C372 10P
_CLK_MCH_DREF 8
R63 33.2Ohm
C371 10P
_CLK_SIO_48M 27
CLK_48M
R62 33.2Ohm
_CLK_ICH48 15
C370 10P
SDA_3S 5,10,17
SCL_3S 5,10,17
PM_STPCPU# 15,38
PM_STPPCI# 15
PM_SLP_S1# 15,35
R61 475Ohm
A62010
C545 100P
C546 100P
R263 10KOhm
R264 1KOhm
CG_FS2 15
CG_FS1 15
R55 10KOhm
CG_FS0 15
R56 10KOhm
EMI
Title : CLOCK-ICS950815
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 18 of 51


PCI_AD[31:0] 14,20,21,22
14,20,21 PCI_C/BE#0
PCI_C/BE#1 14,20,21
PCI_PAR 14,20,21
PCI_SERR# 14,17,20,21
PCI_PERR# 14,17,20,21
PCI_STOP# 14,17,20,21
PCI_DEVSEL# 14,17,20,21
PCI_TRDY# 14,17,20,21
+V3.3SUS
R70
3.6KOhm
U34
EECS
EESK
EEDI/AUX
EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46
+V3.3SUS_LAN
C382
0.1uF/10V
GND
1225
1131
X5
25MHZ
ECERA 18PF/30PPM
XTAL1
XTAL2
C84
18P
C82
18P
2008
2008
U3
RTL8100CL
PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2
LAN_RSET
R54
5.9KOhm
1%
PCI_IRDY# 14,17,20,21
PCI_FRAME# 14,17,20,21
PCI_C/BE#2 14,20,21
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
LAN_IDSEL
R69
33Ohm
PCI_C/BE#3 14,20,21
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
DVDD
+V3.3SUS_LAN
2025
*All termination resistors
should be near chip
C367
0.01UF/10V
C366
0.01UF/10V
R257
R256
R255
R254
49.9Ohm
L_TDP
L_TDN
L_RDP
L_RDN
33
AVDDL
AVDD25
C361
0.1uF/10V
2012
2103
L_TDP
L_TDN
L_RDP
L_RDN
CTRL25
ISOLATEB
15,21,37,42 PM_SLP_S3#
15,17,20 PCI_INTC#
13,14,20,21,26,27 BUF_PCI_RST#
18 _CLK_LANPCI
C62
10P
1230
1301
PME_SB# 14
PCI_REQ#2 14,17
PCI_GNT#2 14
+V3.3SUS_LAN
L18
120Ohm/100Mhz
20 mil
AVDDL
C66
0.1uF/10V
C365
0.1uF/10V
CTRL25
+V3.3SUS_LAN
Q10
HM772
20 mil
TP13
TPC28t
DVDD
C55
10uF/10V
C65
0.1uF/10V
C91
0.1uF/10V
C386
0.1uF/10V
C61
0.1uF/10V
+V3.3SUS
30 mil
+V3.3SUS_LAN
30 mil
C97
0.1uF/10V
C101
10uF/10V
C94
0.1uF/10V
C80
0.1uF/10V
C108
0.1uF/10V
C64
0.1uF/10V
A62018
Title : LAN-RTL8100CL
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 19 of 51

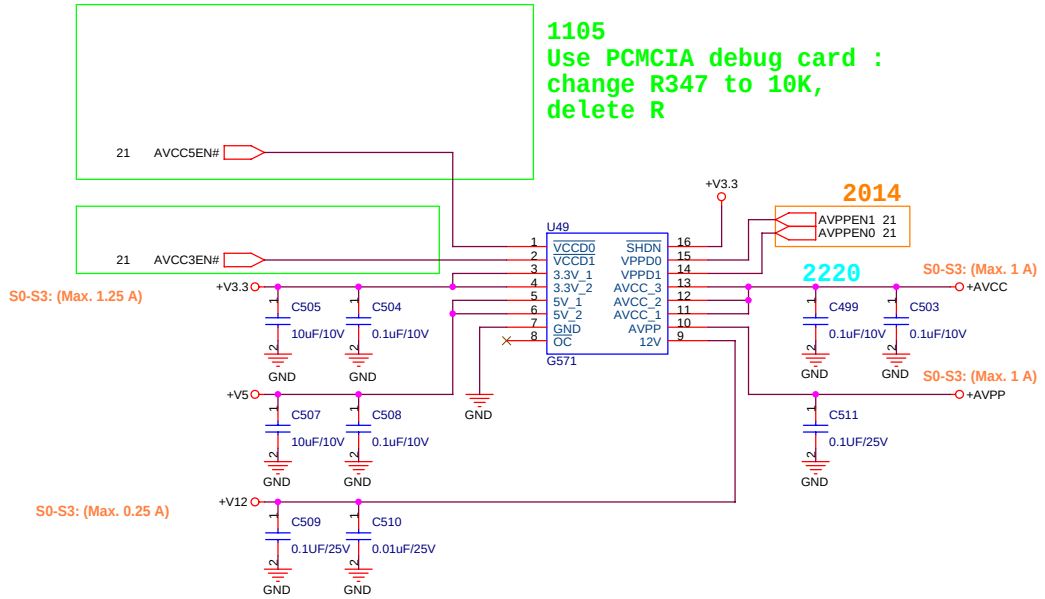


ASUSTek COMPUTER INC. NB1	Title : MINIPCI	Engineer: John Hung
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 20 of 51	

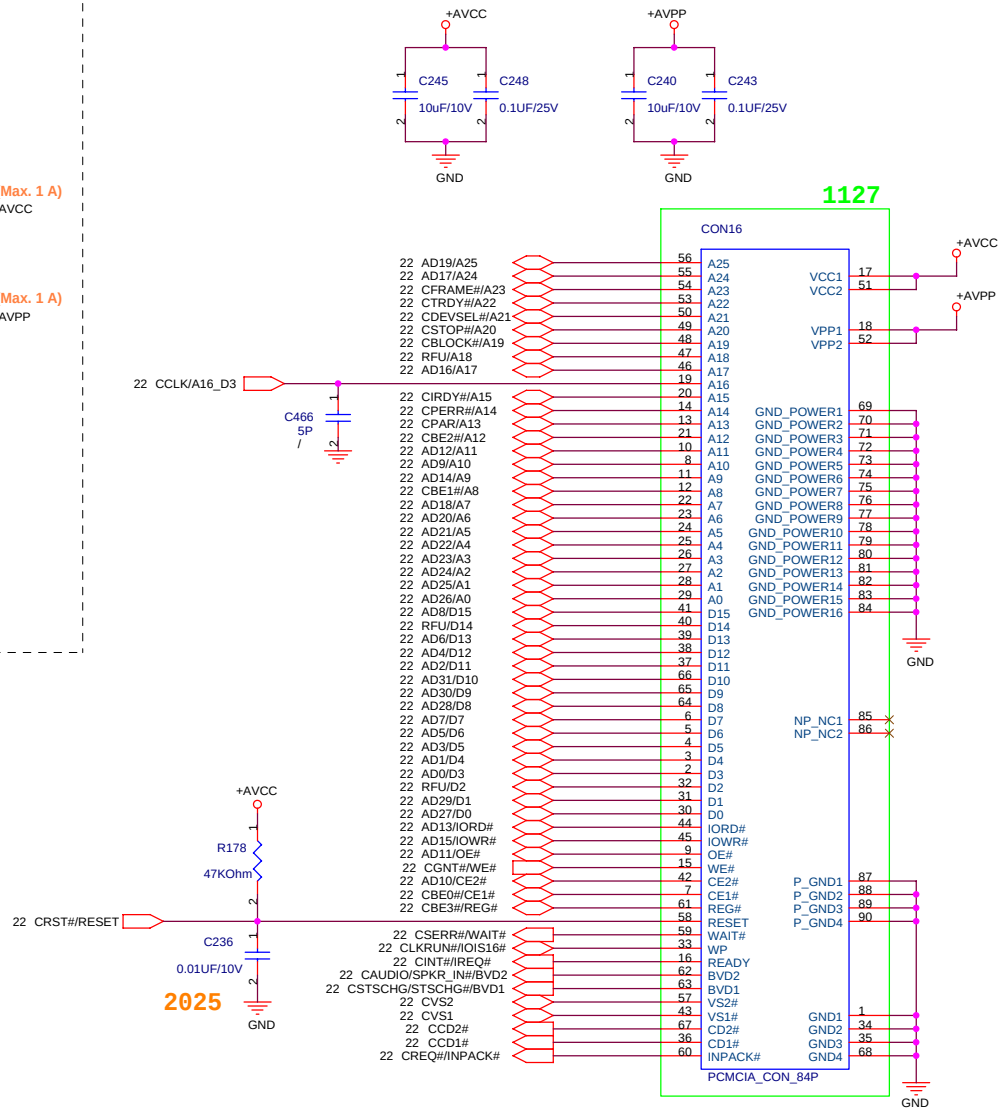

U37B
R5S593
R5C593
+V1.8
C237 0.1uF/10V
C463 10uF/10V
GND
+V3.3S
C226 0.1uF/10V
C450 10uF/10V
+V3.3
C233 0.1uF/10V
C232 0.1uF/10V
C464 10uF/10V
+V3.3_1394
L47 75Ohm/100MHz Irat=200mA
C247 0.01UF/10V
C476 0.1uF/10V
C477 10uF/10V
2025
1139
30 SPKRCB
R171 100KOhm
22 MCVCC3EN#
CB_RI#_OC
CB_SUSPEND#
14,20,27 PCI_PME#
CB_GBRST#
14,20,26 PM_CLKRUN#
13,14,19,20,26,27 BUF_PCI_RST#
18 _CLK_CBPCI
4"-8.5"
C202 5P
14 PCI_GNT#0
14,17 PCI_REQ#0
CB_IDSEL
14,17,19,20 PCI_FRAME#
14,17,19,20 PCI_IRDY#
14,17,19,20 PCI_TRDY#
14,17,19,20 PCI_DEVSEL#
14,17,19,20 PCI_STOP#
14,17,19,20 PCI_PERR#
14,17,19,20 PCI_SERR#
14,19,20 PCI_PAR
14,19,20 PCI_C/BE#3
14,19,20 PCI_C/BE#2
14,19,20 PCI_C/BE#1
14,19,20 PCI_C/BE#0
14,19,20,22 PCI_AD21
R323 100Ohm
1104
15 CB_SD#
15,19,37,42 PM_SLP_S3#
D17 1N4148W-A2
D39 1N4148W-A2 N/A
1211
R153 10KOhm
R318 100KOhm
C449 0.1uF/10V
PCB_VID[2:0]=000 for R:2.1
PCB_VID[2:0]=001 for R:2.2
PCB_VID[2:0]=010 for R:2.3
PCB_VID[2:0]=100 for R:2.4
R317 10KOhm
R319 10KOhm /
R316 10KOhm /
R321 10KOhm /
R322 10KOhm
R320 10KOhm
PCB_VID2
PCB_VID1
PCB_VID0
2315
2405
INT_SERIRQ 15,17,20,26,27
T42 TPC28t
T160 TPC28t
T159 TPC28t
1394_SCL
1394_SDA
RN69A 10KOhm
RN69B 10KOhm
23 AVPPEN1
23 AVPPEN0
AVCC5EN# 23
AVCC3EN# 23
+V3.3SUS_ICH
RN69C 10KOhm
RN69D 10KOhm
+V5
15 PM_RI#
Q60 2N7002
U36
AT24C02N
C444 0.1uF/10V
Title : CB1394-R5C593(1)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 21 of 51


U37A
R5C593
2313
23 CCLK/A16_D3
R_CCLK/A16_D3
+V3.3
RN70A
RN70B
RN70C
RN70D
MC_CD#
FUN0_SD_CD#
FUN1_SM_CD#
1103
1101
Q43
SI2301DS
+V3.3_MC_VCC
C270
0.1uF/10V
C255
0.1uF/10V
21 MCVCC3EN#
GND
PCI_AD[31:0] 14,19,20,21
TPBIAS0
TPA0+_1
TPA0-_1
TPB0+_1
TPB0-_1
R334
56Ohm
R335
56Ohm
C478
0.01UF/10V
C480
0.33U
2025
R336
56Ohm
R337
56Ohm
R339
5.11KOhm
C479
270PF/50V
+V3.3_1394
REXT/VREF/FIL0
To implement as close as possible to R5C593
To apply shield GND
2103
R333 10KOhm 1%
C467 0.01UF/10V
C473 0.01UF/10V
X3
24.576Mhz
C244
24P
C238
24P
1139
1217 1230
L22
Common Choke
JP21
IEEE_1394
2023
Q40
SI2304DS
R185
10KOhm
MC_WP#
FUN0_SD_CD#
CON8
SD_CARD_19P
C260
5P
/
Memory Card Detect
FUNSEL1 FUNSEL0
0 0 Not Support
0 1 SmartMedia
1 0 MMC/SD
1 1 Memory Stick
MC_CD# : Memory Card Detect
Turn-on voltage 0.37 V
D22
RB717F
MC_CD#
FUN0_SD_CD#
Title : CB1394-R5C593(2)
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 22 of 51

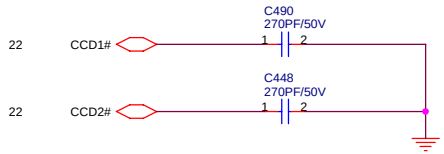
CB POWER SWITCH



CB SOCKET



CB DE-BOUNCE



<Variant Name>

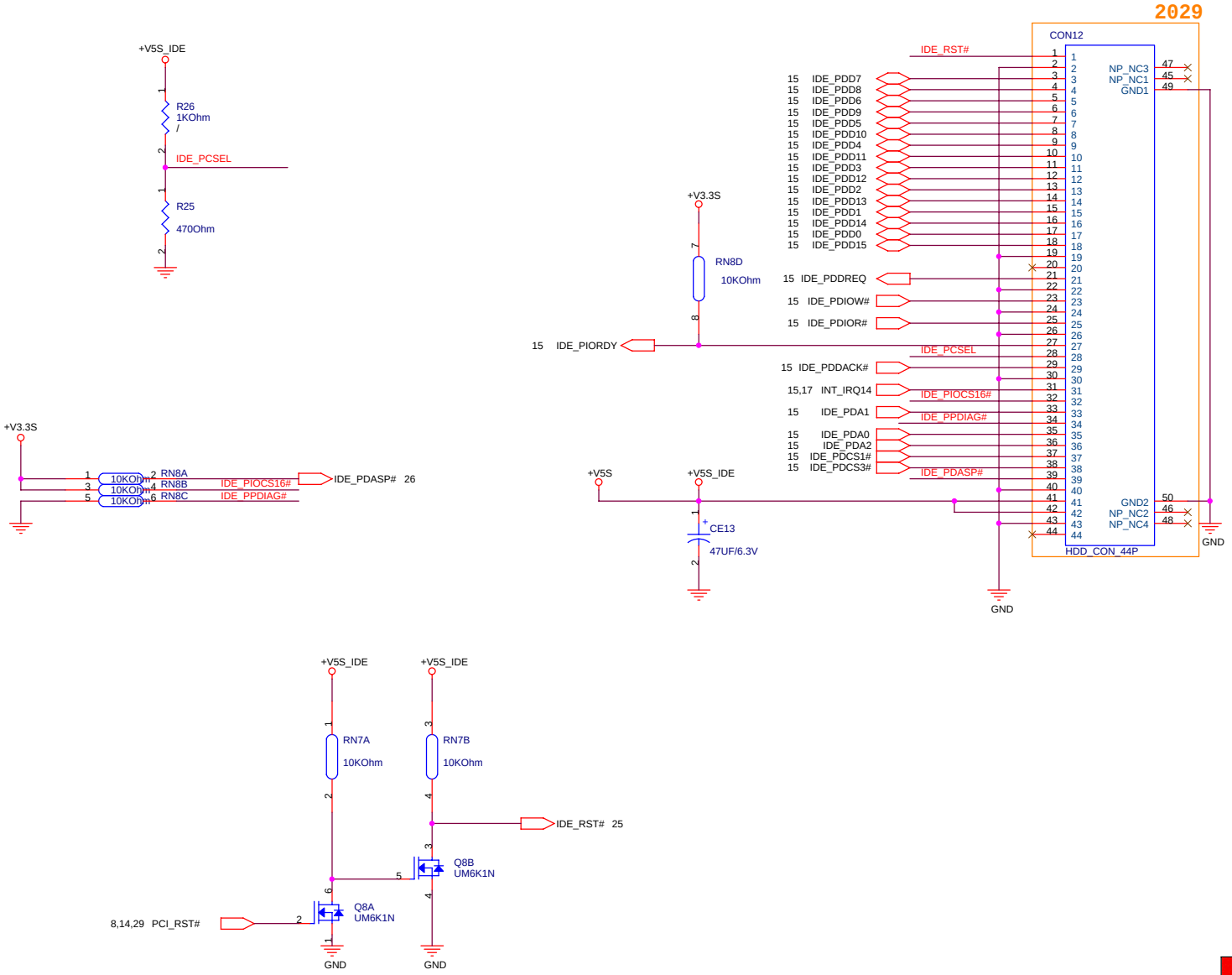
Title : PCMCIA SOCKET

ASUSTek COMPUTER INC. NB1

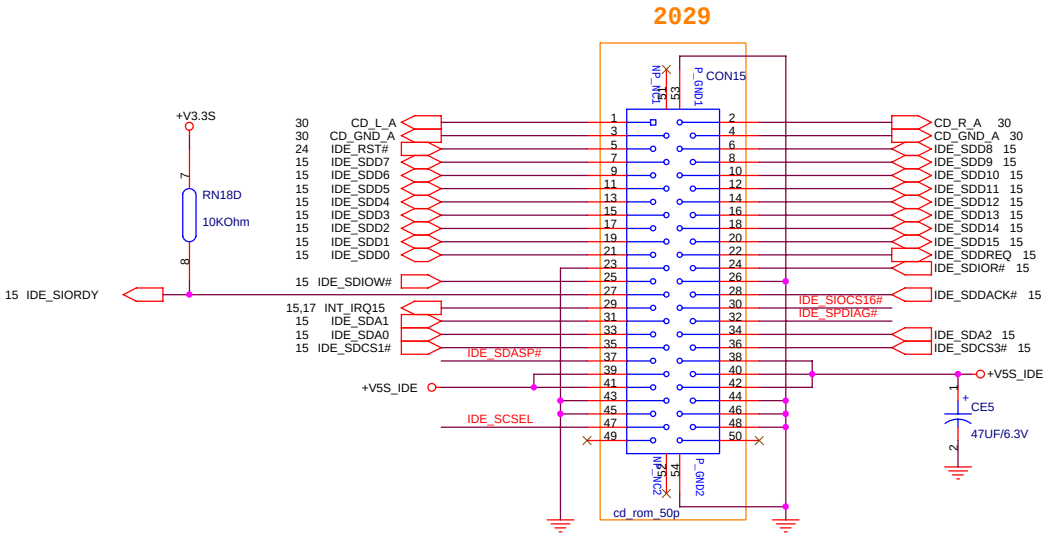
Engineer: John Hung

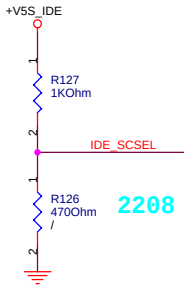
Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 23 of 51

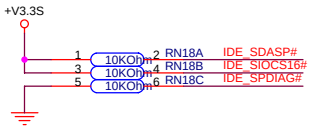


ASUSTek COMPUTER INC. NB1	Title : HDD Connector	
	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 24 of 51	

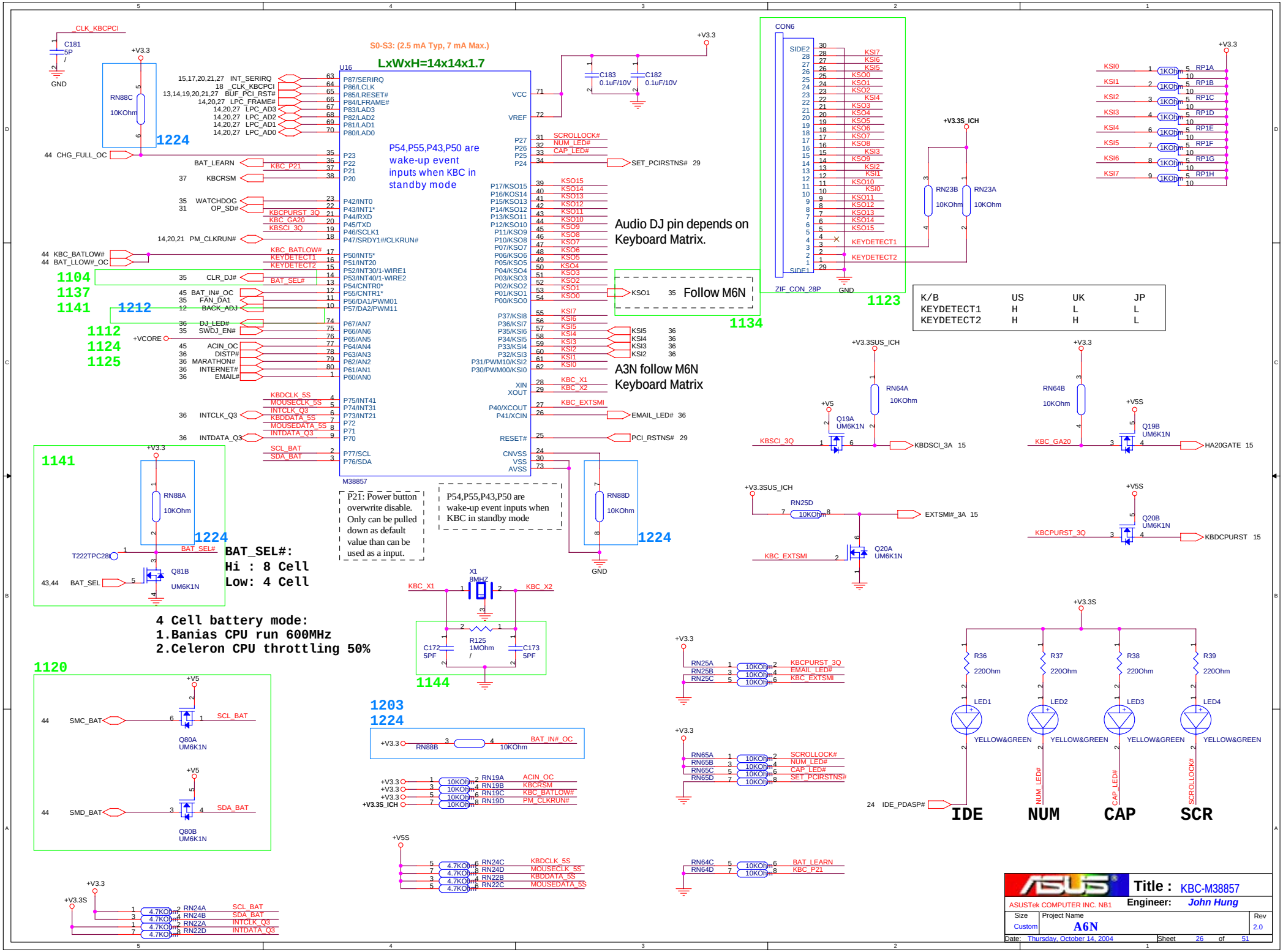




ASUS&EP ODD : Reverse type -- Pull high (Master)
HTC ODD : Normal type -- Pull low (Master)

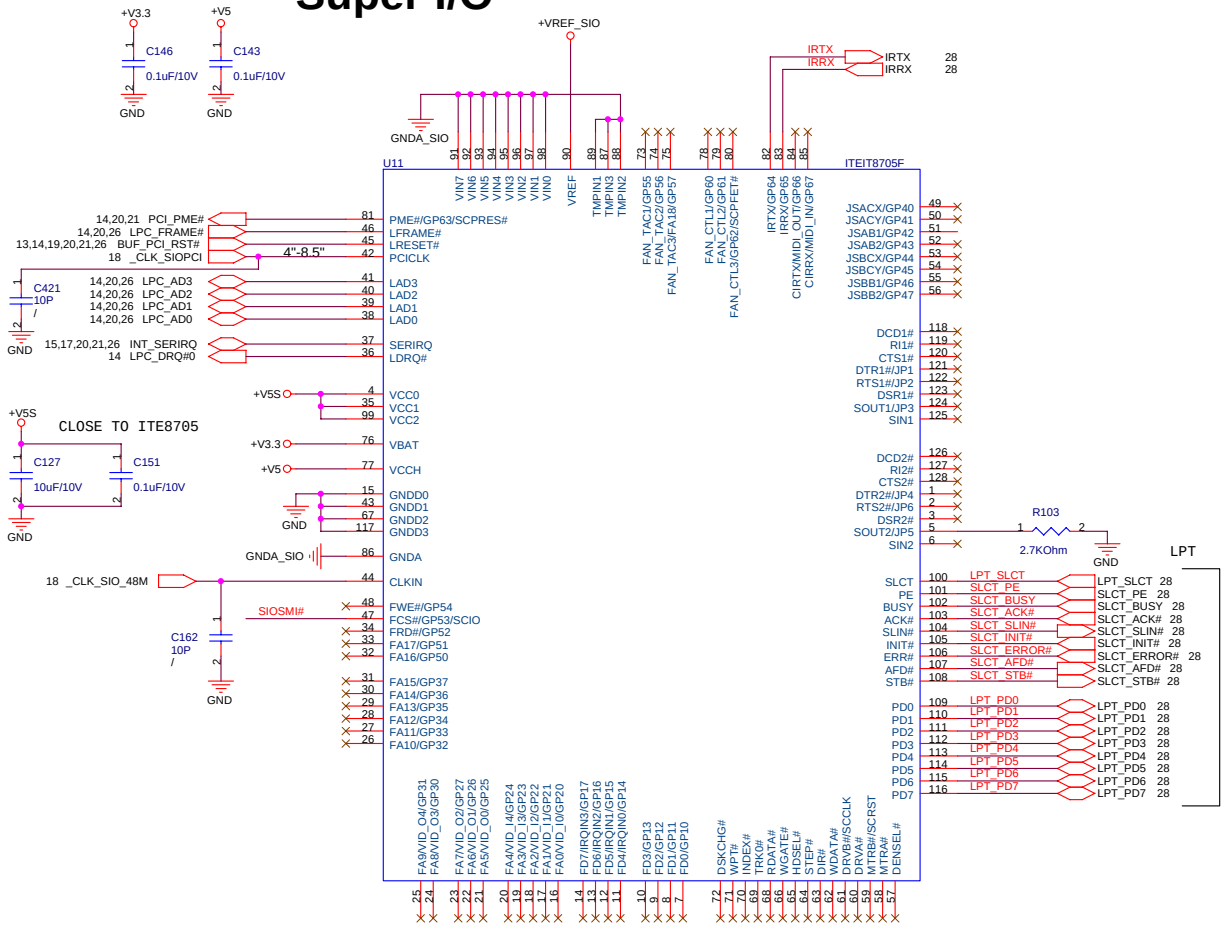


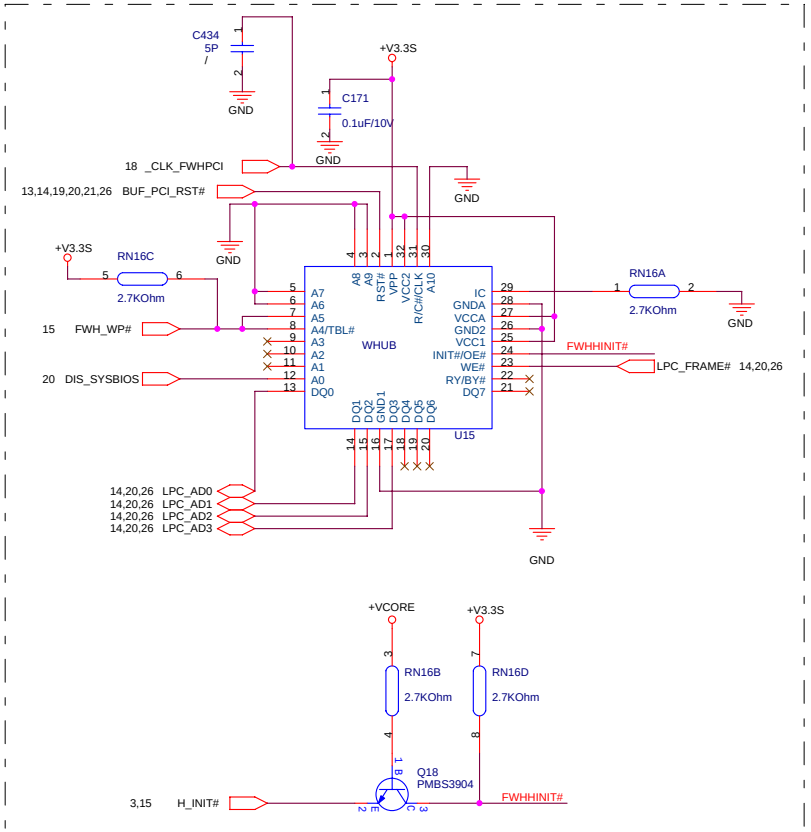
ASUSTek COMPUTER INC. NB1	Title : ODD Connector	Engineer: John Hung
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 25 of 51	


S0-S3: (2.5 mA Typ, 7 mA Max.)
LxWxH=14x14x1.7
U16
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Audio DJ pin depends on Keyboard Matrix.
Follow M6N
A3N follow M6N Keyboard Matrix
P21: Power button overwrite disable. Only can be pulled down as default value than can be used as a input.
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU throttling 50%
CON6
ZIF_CON_28P
K/B US UK JP
KEYDETECT1 H L L
KEYDETECT2 H H L
IDE
NUM
CAP
SCR
Title : KBC-M38857
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 26 of 51

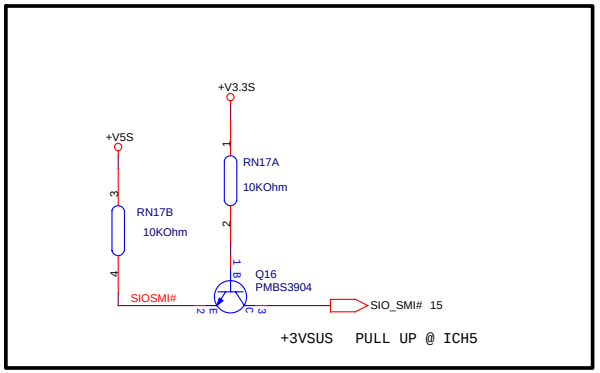
Super I/O

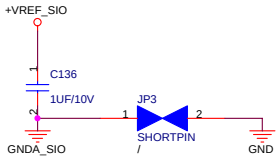
2208





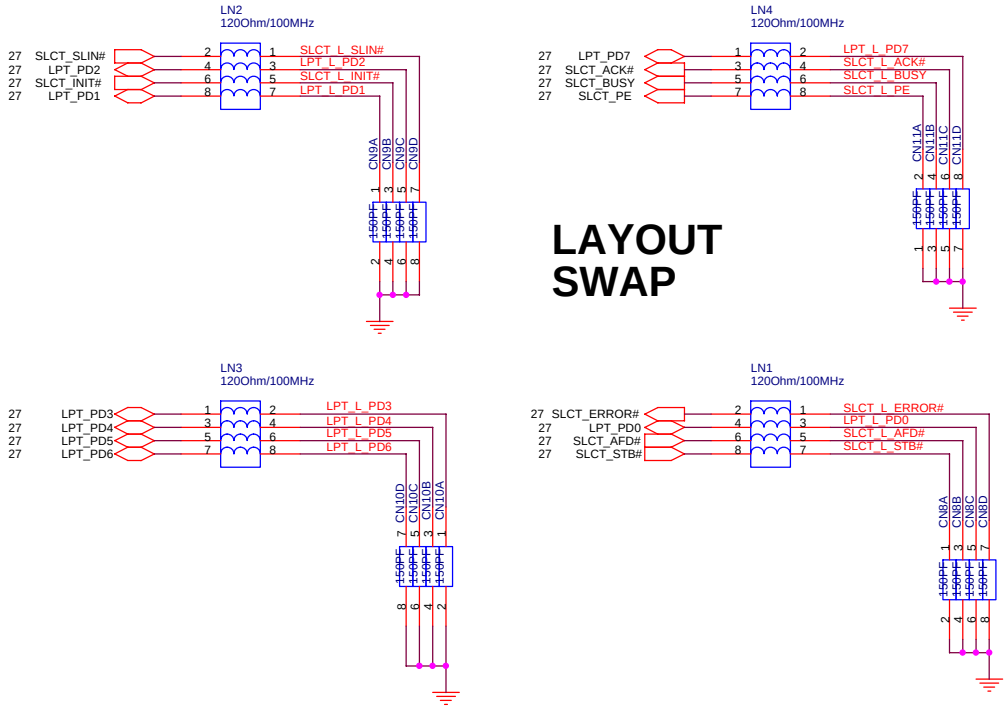
P24: Add FHW ROM P/N: 05-001017122



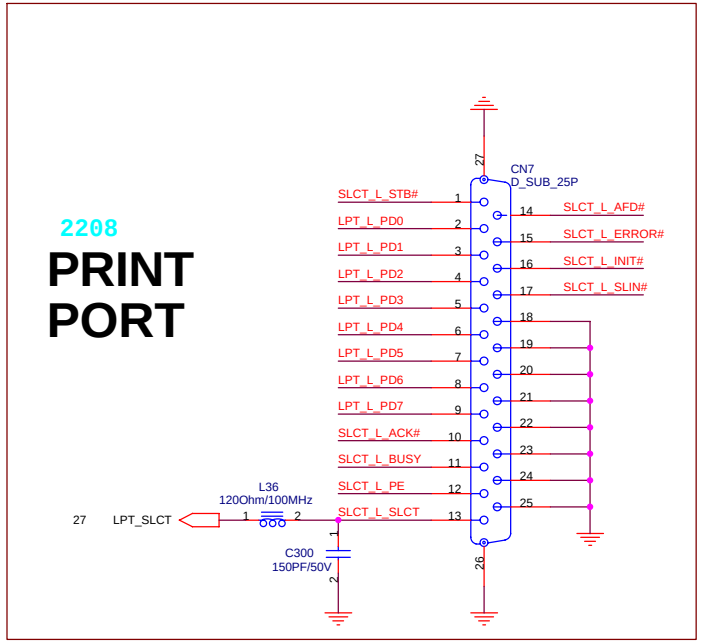


<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : SIO-ITE8705	Engineer: John Hung
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 27 of 51	

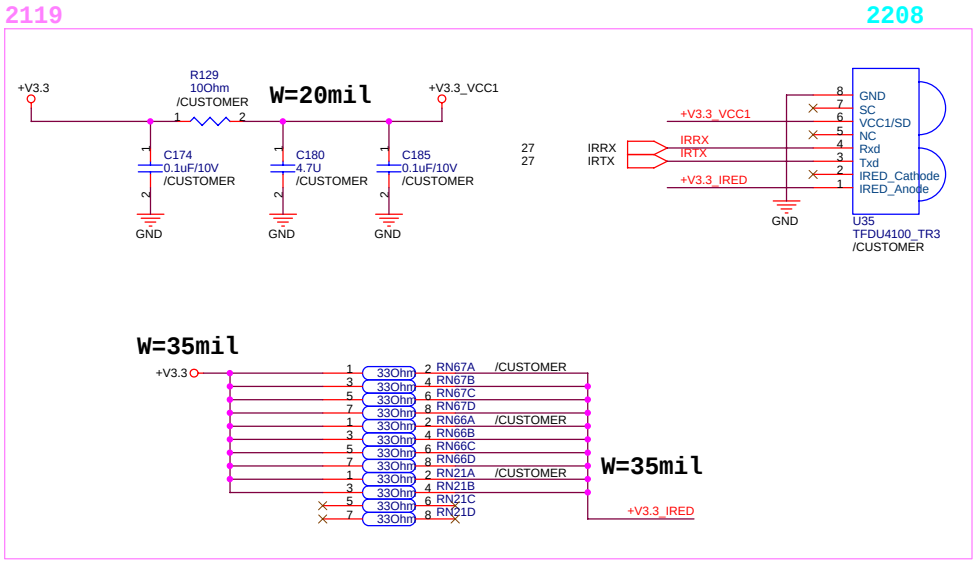


LAYOUT SWAP



A62015 2309

A6Ne R:2.0 footprint is : d_sub_25p_2hold_f_a3n

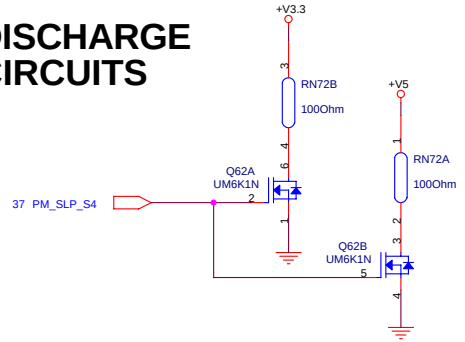


ASUS	Title :	
ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 28 of 51	

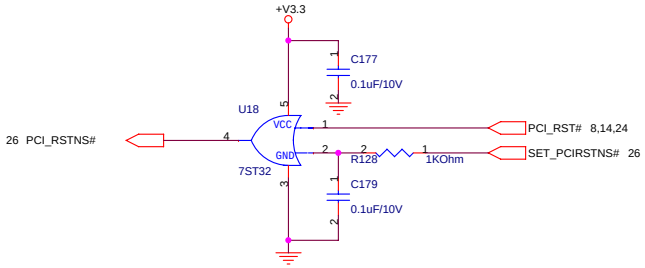
PCMCIA DEBUG Card

1105

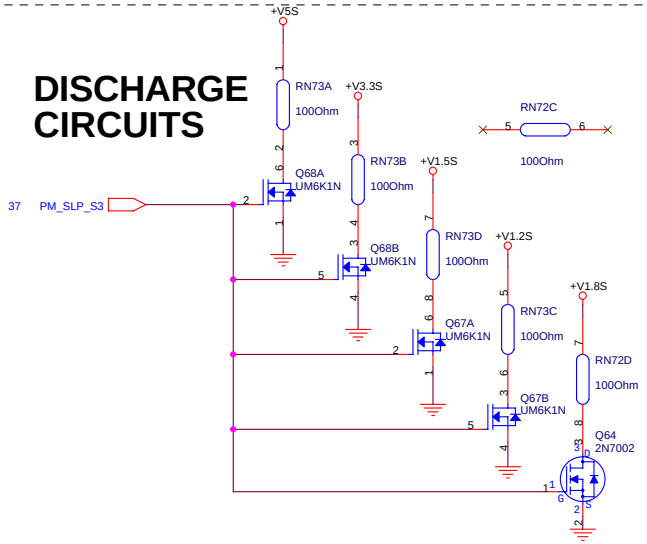
DISCHARGE CIRCUITS



PCI_RSTNS# Gen Circuit



DISCHARGE CIRCUITS



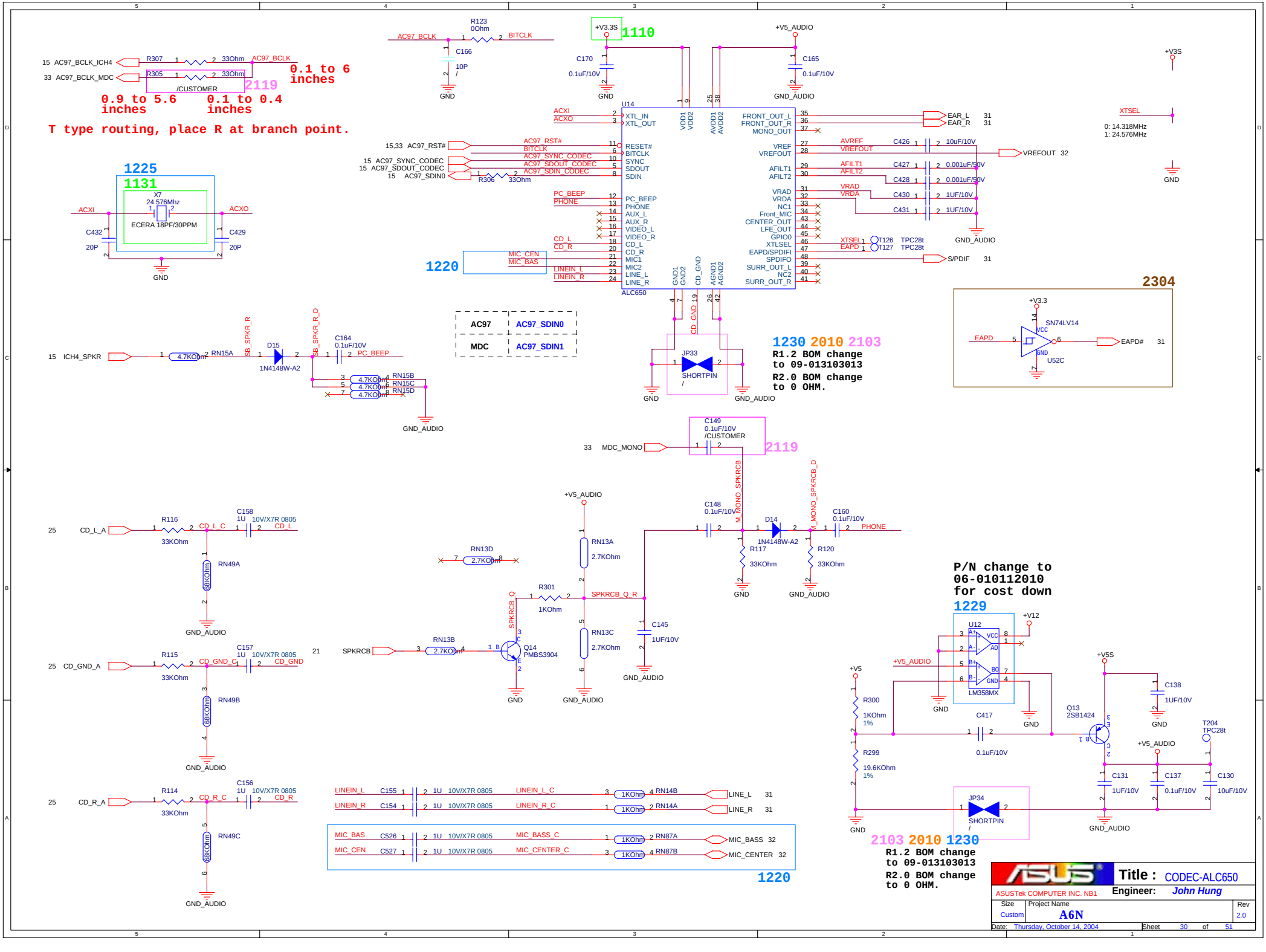
ASUSTek COMPUTER INC. NB1

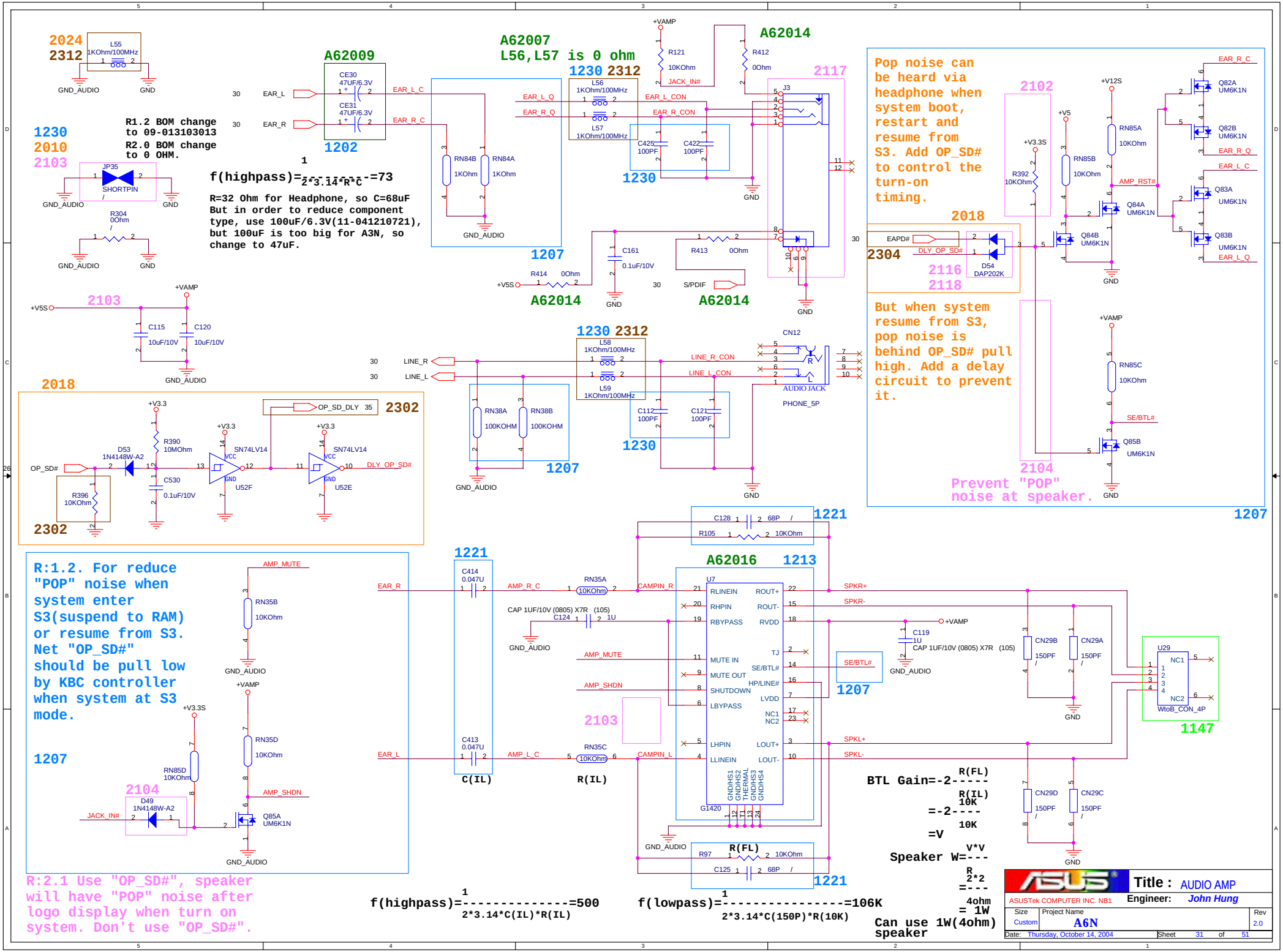
Title : Discharge circuit

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 29 of 51

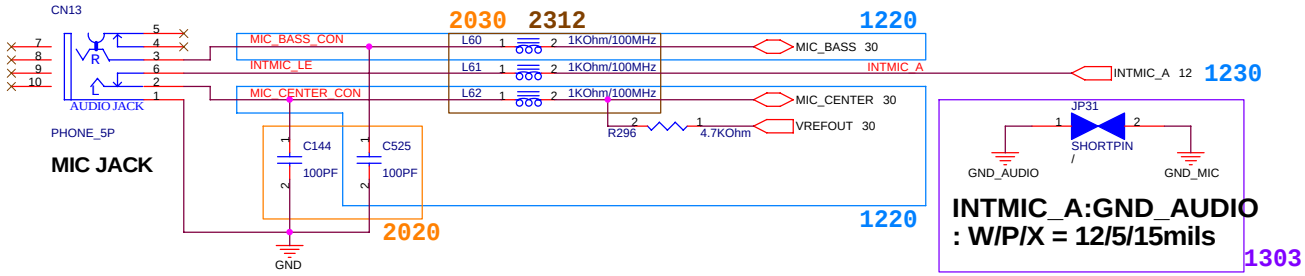

15 AC97_BCLK_ICH4
33 AC97_BCLK_MDC
R307 33Ohm
R305 33Ohm
/CUSTOMER
2119
AC97_BCLK
0.1 to 6 inches
0.9 to 5.6 inches
0.1 to 0.4 inches
T type routing, place R at branch point.
R123 0Ohm
AC97_BCLK
BITCLK
C166 10P
GND
+V3.3S
1110
C170 0.1uF/10V
+V5_AUDIO
C165 0.1uF/10V
GND_AUDIO
+V3S
U14
ACXI
ACXO
XTL_IN
XTL_OUT
VDD1 VDD2
AVDD1 AVDD2
FRONT_OUT_L
FRONT_OUT_R
MONO_OUT
EAR_L 31
EAR_R 31
XTSEL
0: 14.318MHz
1: 24.576MHz
15,33 AC97_RST#
AC97_RST#
BITCLK
AC97_SYNC_CODEC
AC97_SDOUT_CODEC
AC97_SDIN_CODEC
15 AC97_SYNC_CODEC
15 AC97_SDOUT_CODEC
15 AC97_SDIN0
R306 33Ohm
RESET#
BITCLK
SYNC
SDOUT
SDIN
VREF
VREFOUT
AVREF
VREFOUT
C426 10uF/10V
VREFOUT 32
AFILT1
AFILT2
C427 0.001uF/50V
C428 0.001uF/50V
VRAD
VRDA
C430 1UF/10V
C431 1UF/10V
GND_AUDIO
PC_BEEP
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_R
MIC1
MIC2
LINE_L
LINE_R
NC1
Front_MIC
CENTER_OUT
LFE_OUT
GPIO0
XTSEL
EAPD/SPDIFI
SPDIFO
SURR_OUT_L
NC2
SURR_OUT_R
XTSEL T126 TPC28t
EAPD T127 TPC28t
S/PDIF 31
CD_L
CD_R
MIC_CEN
MIC_BAS
LINEIN_L
LINEIN_R
1220
ALC650
GND1 GND2
CD_GND
AGND1 AGND2
1225
1131
X7 24.576Mhz
ECERA 18PF/30PPM
ACXI
ACXO
C432 20P
C429 20P
GND
AC97 AC97_SDIN0
MDC AC97_SDIN1
JP33 SHORTPIN
1230 2010 2103
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.
2304
+V3.3
SN74LV14
EAPD
EAPD# 31
U52C
15 ICH4_SPKR
4.7KOhm RN15A
SB_SPKR_R
SB_SPKR_R_D
D15 1N4148W-A2
C164 0.1uF/10V
PC_BEEP
RN15B 4.7KOhm
RN15C 4.7KOhm
RN15D 4.7KOhm
GND_AUDIO
C149 0.1uF/10V /CUSTOMER
2119
33 MDC_MONO
M_MONO_SPKRCB
M_MONO_SPKRCB_D
C148 0.1uF/10V
D14 1N4148W-A2
C160 0.1uF/10V
PHONE
R117 33KOhm
R120 33KOhm
25 CD_L_A
R116 33KOhm
CD_L_C
C158 1U 10V/X7R 0805
CD_L
RN49A 68KOhm
GND_AUDIO
RN13D 2.7KOhm
+V5_AUDIO
RN13A 2.7KOhm
R301 1KOhm
SPKRCB_Q_R
SPKRCB_Q
RN13C 2.7KOhm
C145 1UF/10V
25 CD_GND_A
R115 33KOhm
CD_GND_C
C157 1U 10V/X7R 0805
CD_GND
RN49B 68KOhm
21 SPKRCB
RN13B 2.7KOhm
Q14 PMBS3904
P/N change to 06-010112010 for cost down
1229
U12
LM358MX
+V12
+V5_AUDIO
+V5
R300 1KOhm 1%
R299 19.6KOhm 1%
C417 0.1uF/10V
Q13 2SB1424
+V5S
C138 1UF/10V
T204 TPC28t
C131 1UF/10V
C137 0.1uF/10V
C130 10uF/10V
JP34 SHORTPIN
2103 2010 1230
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.
25 CD_R_A
R114 33KOhm
CD_R_C
C156 1U 10V/X7R 0805
CD_R
RN49C 68KOhm
LINEIN_L C155 1U 10V/X7R 0805
LINEIN_L_C
RN14B 1KOhm
LINE_L 31
LINEIN_R C154 1U 10V/X7R 0805
LINEIN_R_C
RN14A 1KOhm
LINE_R 31
MIC_BAS C526 1U 10V/X7R 0805
MIC_BASS_C
RN87A 1KOhm
MIC_BASS 32
MIC_CEN C527 1U 10V/X7R 0805
MIC_CENTER_C
RN87B 1KOhm
MIC_CENTER 32
1220
ASUS
Title : CODEC-ALC650
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 30 of 51


2024
2312
L55
1KOhm/100MHz
GND_AUDIO
GND
A62009
CE30
47UF/6.3V
CE31
47UF/6.3V
EAR_L
EAR_R
EAR_L_C
EAR_R_C
1202
1230
2010
2103
JP35
SHORTPIN
R304
0Ohm
R1.2 BOM change to 09-013103013
R2.0 BOM change to 0 OHM.
f(highpass)=1/(2*3.14*R*C)=73
R=32 Ohm for Headphone, so C=68uF But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.
RN84B
1KOhm
RN84A
1KOhm
1207
A62007
L56,L57 is 0 ohm
1230 2312
L56
1KOhm/100MHz
L57
1KOhm/100MHz
EAR_L_Q
EAR_R_Q
EAR_L_CON
EAR_R_CON
C425
100PF
C422
100PF
+VAMP
R121
10KOhm
JACK_IN#
R412
0Ohm
A62014
2117
J3
C161
0.1uF/10V
R414
0Ohm
+V5S
R413
0Ohm
S/PDIF
2103
+VAMP
C115
10uF/10V
C120
10uF/10V
2018
+V3.3
OP_SD_DLY
2302
R390
10MOhm
D53
1N4148W-A2
OP_SD#
R396
10KOhm
C530
0.1uF/10V
SN74LV14
U52F
U52E
DLY_OP_SD#
LINE_R
LINE_L
L58
1KOhm/100MHz
L59
1KOhm/100MHz
RN38A
100KOHM
RN38B
100KOHM
C112
100PF
C121
100PF
LINE_R_CON
LINE_L_CON
CN12
AUDIO JACK
PHONE_5P
Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.
2102
+V3.3S
R392
10KOhm
+V5
+V12S
RN85A
10KOhm
RN85B
10KOhm
AMP_RST#
Q84A
UM6K1N
Q84B
UM6K1N
Q82A
UM6K1N
Q82B
UM6K1N
Q83A
UM6K1N
Q83B
UM6K1N
EAPD#
DLY_OP_SD#
2304
2116
2118
D54
DAP202K
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.
RN85C
10KOhm
SE/BTL#
Q85B
UM6K1N
2104
Prevent "POP" noise at speaker.
C128
68P
R105
10KOhm
1221
A62016
1213
U7
C414
0.047U
C413
0.047U
EAR_R
EAR_L
AMP_R_C
AMP_L_C
RN35A
10KOhm
RN35C
10KOhm
CAMPIN_R
CAMPIN_L
CAP 1UF/10V (0805) X7R (105)
C124
1U
RLINEIN
RHPIN
RBYPASS
MUTE IN
MUTE OUT
SHUTDOWN
LBYPASS
LHPIN
LLINEIN
ROUT+
ROUT-
RVDD
TJ
SE/BTL#
HP/LINE#
LVDD
NC1
NC2
LOUT+
LOUT-
GNDHS1
GNDHS2
THERMAL
GNDHS3
GNDHS4
G1420
SPKR+
SPKR-
SPKL+
SPKL-
AMP_MUTE
AMP_SHDN
C119
1U
CAP 1UF/10V (0805) X7R (105)
CN29B
150PF
CN29A
150PF
CN29D
150PF
CN29C
150PF
U29
NC1
NC2
WtoB_CON_4P
1147
R:1.2. For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.
1207
RN35B
10KOhm
+V3.3S
RN85D
10KOhm
2104
D49
1N4148W-A2
JACK_IN#
Q85A
UM6K1N
C(IL)
R(IL)
R97
R(FL)
10KOhm
C125
68P
R:2.1 Use "OP_SD#", speaker will have "POP" noise after logo display when turn on system. Don't use "OP_SD#".
f(highpass)=1/(2*3.14*C(IL)*R(IL))=500
f(lowpass)=1/(2*3.14*C(150P)*R(10K))=106K
BTL Gain=-2*R(FL)/R(IL)
=-2*10K/10K
=V
Speaker W=V*V/R
=2*2/4ohm
= 1W
Can use 1W(4ohm) speaker
ASUS
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 31 of 51

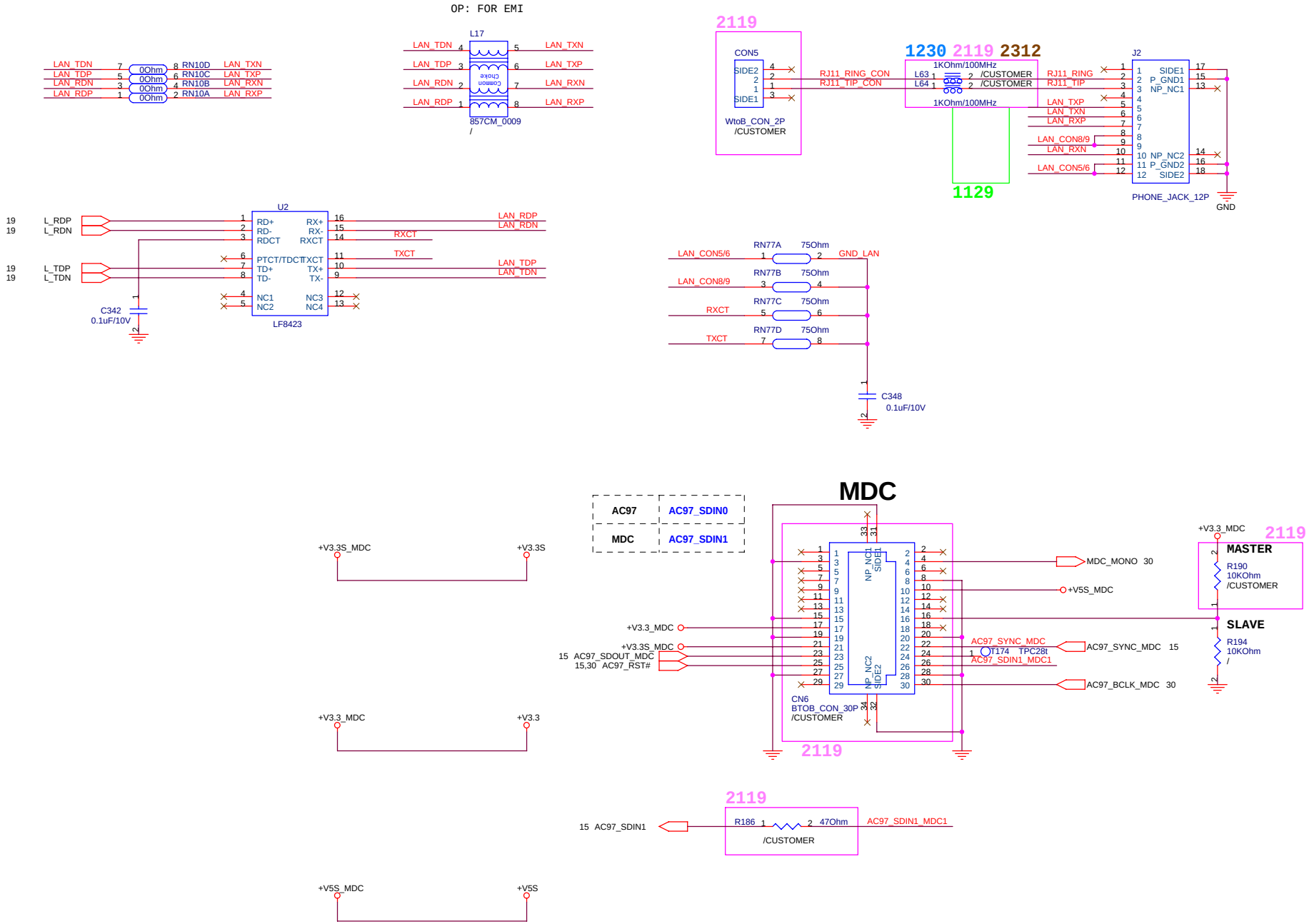
1220

MIC OP CIRCUIT

MIC JACK



ASUS	Title :	
ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 32 of 51	



MDC

ASUS

Title :

ASUSTek COMPUTER INC. NB1

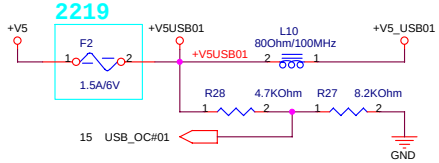
Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

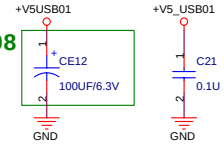
Date: Thursday, October 14, 2004 Sheet 33 of 51

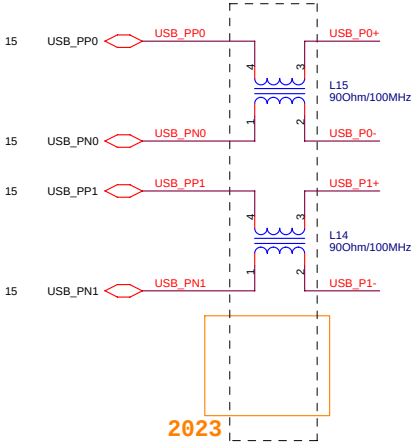
VPLP R:2.2 use 07-014110900 (
2nd source is 07-014110201)

2219



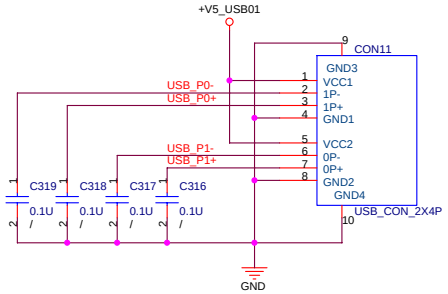
A62008





2023

R & L Co-Lay



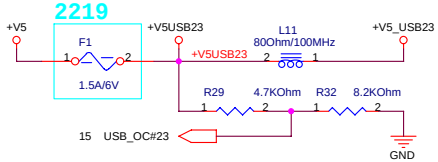
USB PORT 0 & PORT 1

1128

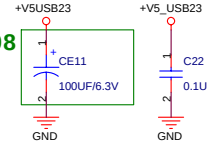
USB PORT 3 for CAMERA
Change to page 12

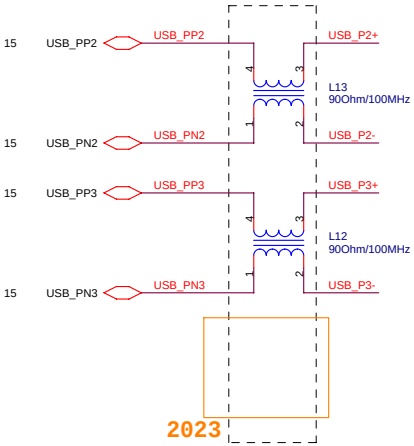
VPLP R:2.2 use 07-014110900 (
2nd source is 07-014110201)

2219



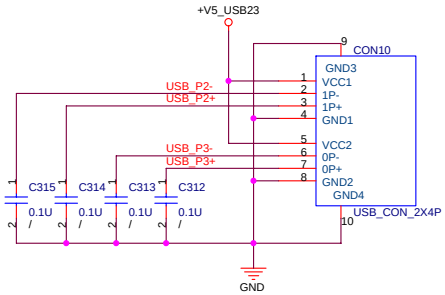
A62008





2023

R & L Co-Lay



A6N1002

USB PORT 2 & PORT 3

1128

USB PORT 4

A6N1002

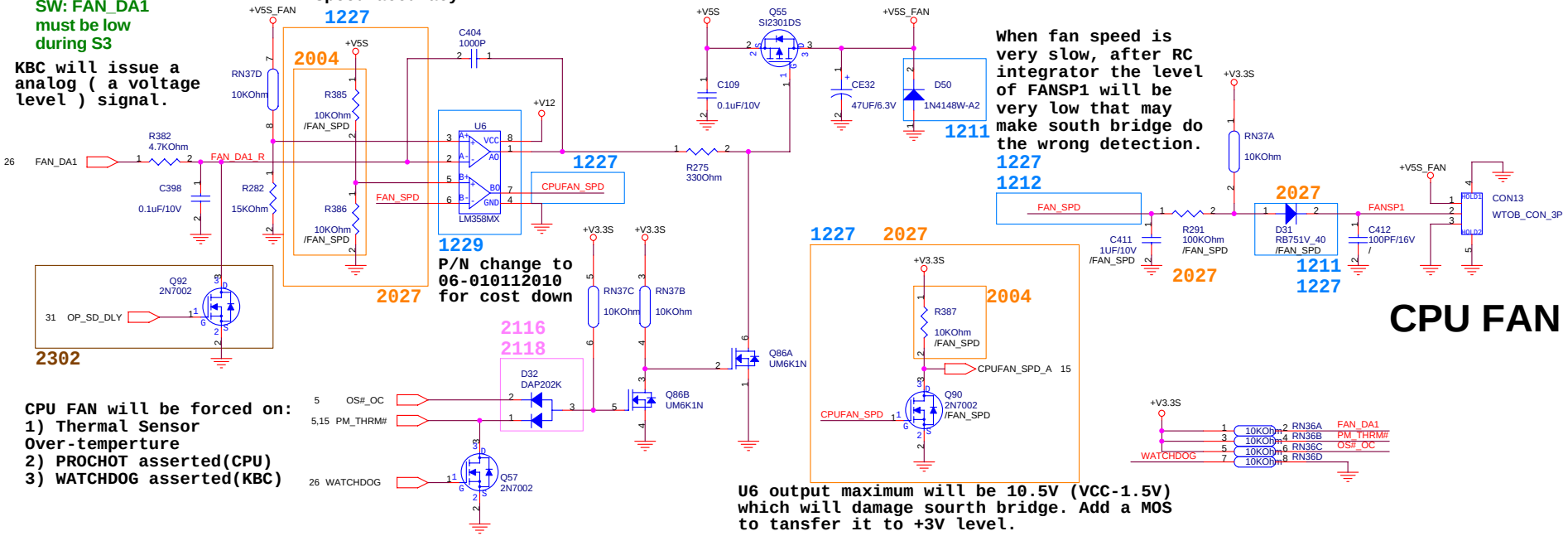
ASUS	Title : USB	
ASUSTek COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 34 of 51	

Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.



When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

1227
1212

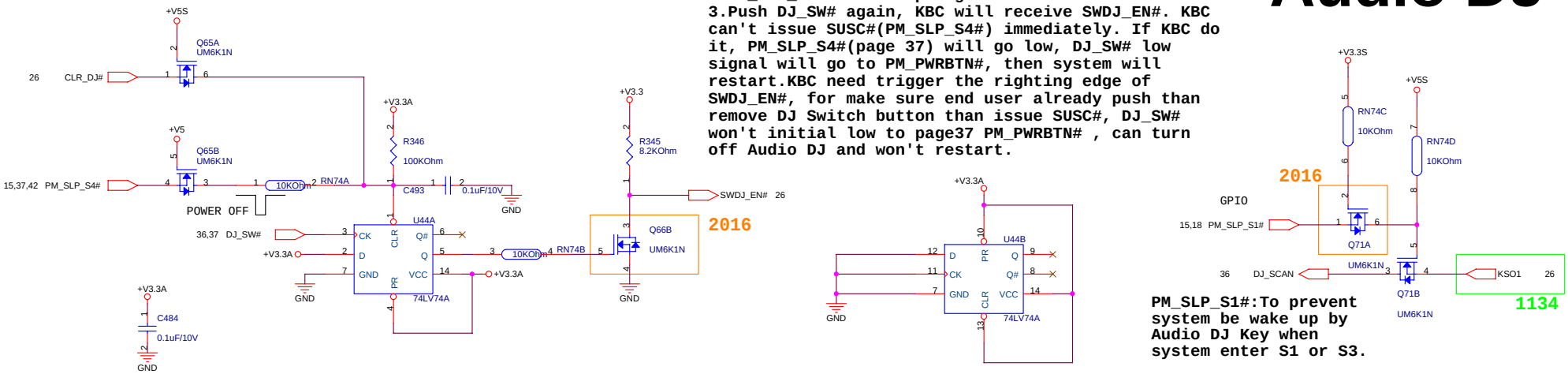
U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

CPU FAN

Audio DJ

SWDJ_EN# function :
1.Push DJ_SW#, turn on Audio DJ.
2.PM_SLP_S4# will keep high.
3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.

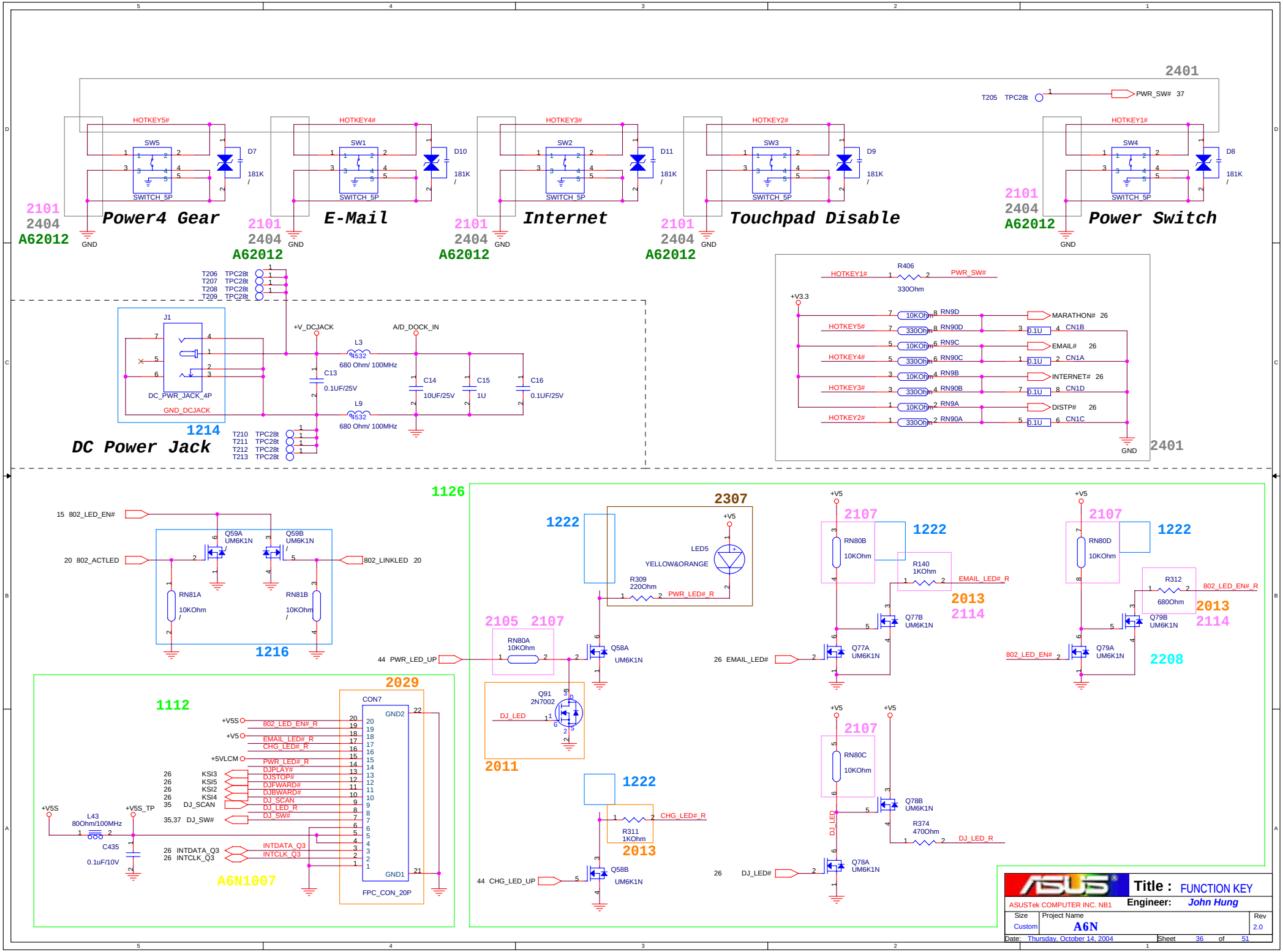


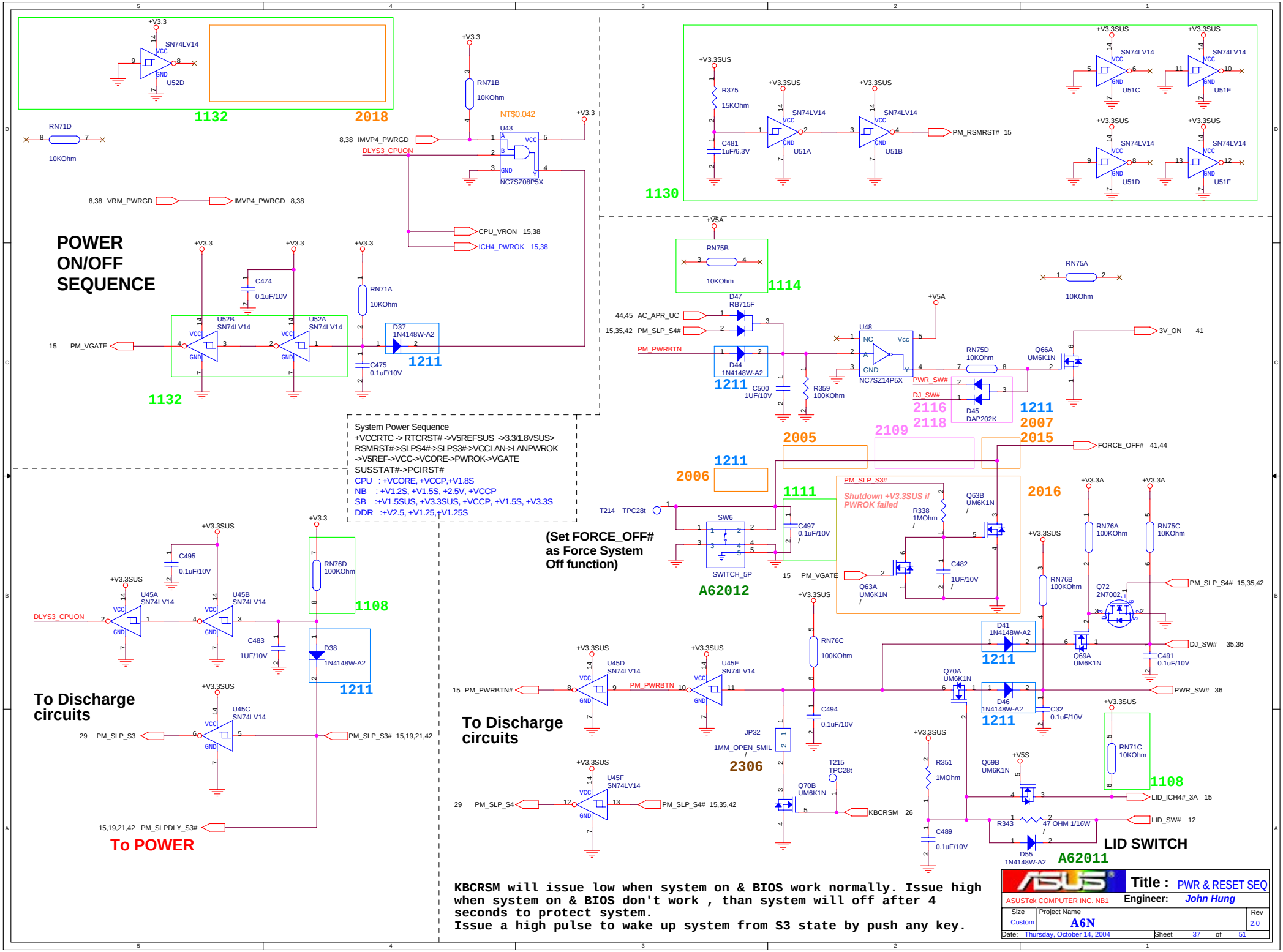
PM_SLP_S1#:To prevent system be wake up by Audio DJ Key when system enter S1 or S3.

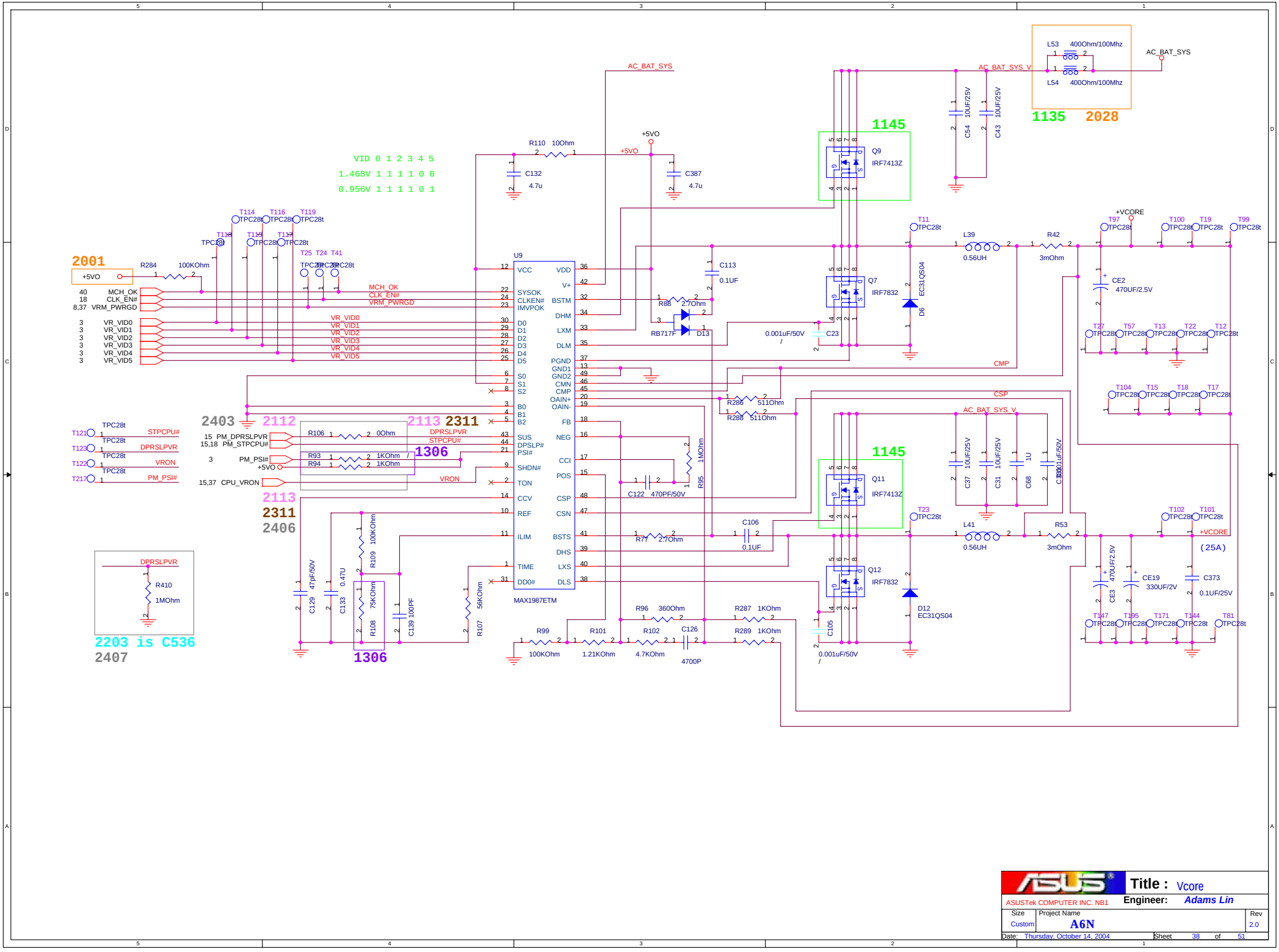
1211
1204

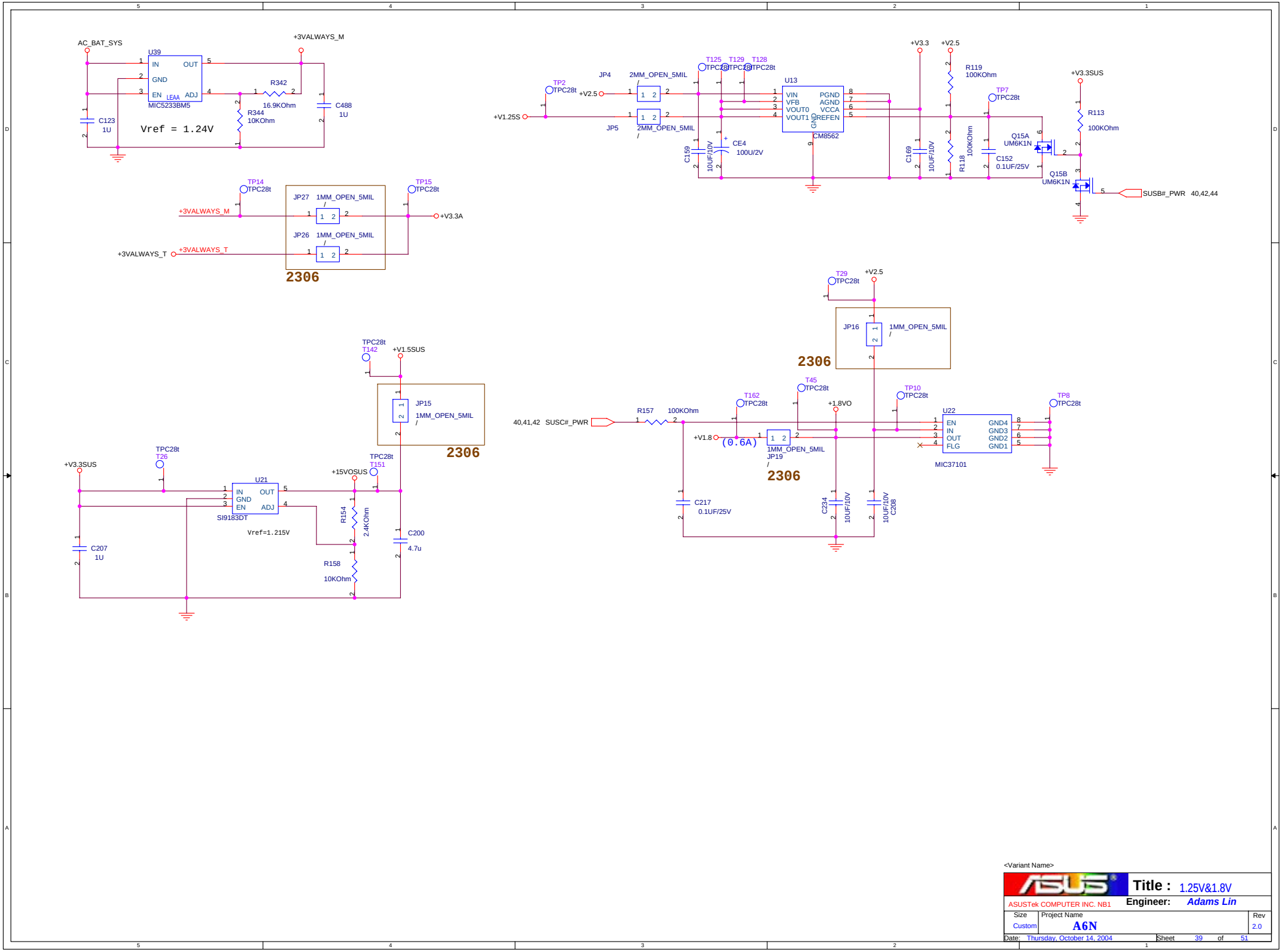
36,37 DJ_SW# — D42 1N4148W-A2 — SWDJ_EN# 26

When power on, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D42 to Enable AudioDJ in OS.
Use D42 to Turn off AudioDJ when system be turned on in DJ mode.


2401
T205 TPC28t
PWR_SW# 37
HOTKEY5#
HOTKEY4#
HOTKEY3#
HOTKEY2#
HOTKEY1#
SW5
SW1
SW2
SW3
SW4
SWITCH_5P
D7
D10
D11
D9
D8
181K
2101
2404
A62012
GND
Power4 Gear
E-Mail
Internet
Touchpad Disable
Power Switch
T206 TPC28t
T207 TPC28t
T208 TPC28t
T209 TPC28t
J1
DC_PWR_JACK_4P
GND_DCJACK
1214
DC Power Jack
+V_DCJACK
A/D_DOCK_IN
L3
L9
4532
680 Ohm/ 100MHz
C13
0.1UF/25V
C14
10UF/25V
C15
1U
C16
0.1UF/25V
T210 TPC28t
T211 TPC28t
T212 TPC28t
T213 TPC28t
R406
330Ohm
+V3.3
RN9D
RN90D
RN9C
RN90C
RN9B
RN90B
RN9A
RN90A
10KOhm
330Ohm
MARATHON# 26
EMAIL# 26
INTERNET# 26
DISTP# 26
CN1B
CN1A
CN1D
CN1C
0.1U
1126
15 802_LED_EN#
20 802_ACTLED
802_LINKLED 20
Q59A
UM6K1N
Q59B
UM6K1N
RN81A
RN81B
10KOhm
1216
1222
2307
LED5
YELLOW&ORANGE
R309
220Ohm
PWR_LED#_R
2105
2107
RN80A
10KOhm
Q58A
UM6K1N
44 PWR_LED_UP
Q91
2N7002
DJ_LED
2011
2107
RN80B
10KOhm
R140
1KOhm
EMAIL_LED#_R
2013
2114
Q77B
UM6K1N
Q77A
UM6K1N
26 EMAIL_LED#
RN80D
R312
680Ohm
802_LED_EN#_R
Q79B
UM6K1N
Q79A
UM6K1N
802_LED_EN#
2208
RN80C
Q78B
UM6K1N
R374
470Ohm
DJ_LED_R
Q78A
UM6K1N
26 DJ_LED#
R311
1KOhm
CHG_LED#_R
Q58B
UM6K1N
44 CHG_LED_UP
1112
2029
CON7
GND2
GND1
FPC_CON_20P
+V5S
+V5
+5VLCM
802_LED_EN#_R
EMAIL_LED#_R
CHG_LED#_R
PWR_LED#_R
DJPLAY#
DJSTOP#
DJFWARD#
DJBWARD#
DJ_SCAN
DJ_LED_R
DJ_SW#
26 KSI3
26 KSI5
26 KSI2
26 KSI4
35 DJ_SCAN
35,37 DJ_SW#
26 INTDATA_Q3
26 INTCLK_Q3
INTDATA_Q3
INTCLK_Q3
+V5S_TP
L43
80Ohm/100MHz
C435
0.1uF/10V
A6N1007
ASUS
Title : FUNCTION KEY
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 36 of 51

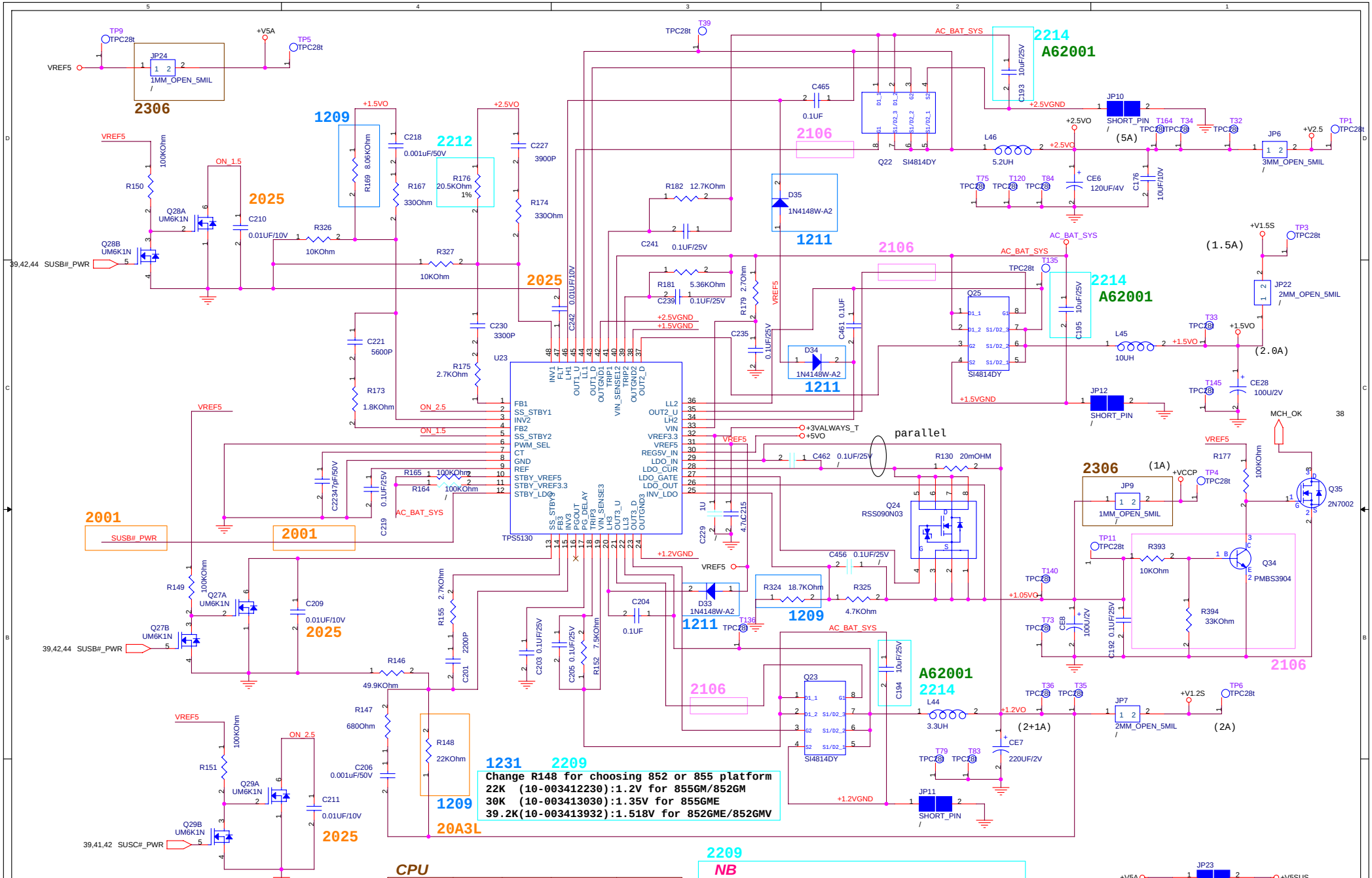

POWER ON/OFF SEQUENCE
System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.8VSUS>
RSMRST#->SLPS4#->SLPS3#->VCCLAN->LANPWROK
->V5REF->VCC->VCORE->PWROK->VGATE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+V1.8S
NB : +V1.2S, +V1.5S, +2.5V, +VCCP
SB :+V1.5SUS, +V3.3SUS, +VCCP, +V1.5S, +V3.3S
DDR :+V2.5, +V1.25,+V1.25S
(Set FORCE_OFF# as Force System Off function)
Shutdown +V3.3SUS if PWROK failed
To Discharge circuits
To POWER
LID SWITCH
KBCRSM will issue low when system on & BIOS work normally. Issue high when system on & BIOS don't work , than system will off after 4 seconds to protect system.
Issue a high pulse to wake up system from S3 state by push any key.
Title : PWR & RESET SEQ
ASUSTek COMPUTER INC. NB1
Engineer: John Hung
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 37 of 51


VID 0 1 2 3 4 5
1.468V 1 1 1 1 0 0
0.956V 1 1 1 1 0 1
2001
+5VO
R284 100KOhm
MCH_OK
CLK_EN#
VRM_PWRGD
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
U9
MAX1987ETM
VCC
SYSOK
CLKEN#
IMVPOK
D0
D1
D2
D3
D4
D5
S0
S1
S2
B0
B1
B2
SUS
DPSLP#
PSI#
SHDN#
TON
CCV
REF
ILIM
TIME
DD0#
VDD
V+
BSTM
DHM
LXM
DLM
PGND
GND1
GND2
CMN
CMP
OAIN+
OAIN-
FB
NEG
CCI
POS
CSP
CSN
BSTS
DHS
LXS
DLS
AC_BAT_SYS
R110 10Ohm
C132 4.7u
C387 4.7u
C113 0.1UF
R88 2.7Ohm
RB717F D13
C23 0.001uF/50V
R286 511Ohm
R288 511Ohm
R95 1MOhm
C122 470PF/50V
R77 2.7Ohm
C106 0.1UF
R96 360Ohm
R102 4.7KOhm
C126 4700P
R287 1KOhm
R289 1KOhm
R99 100KOhm
R101 1.21KOhm
C105 0.001uF/50V
Q9 IRF7413Z
Q7 IRF7832
Q11 IRF7413Z
Q12 IRF7832
D6 EC31QS04
D12 EC31QS04
1145
L53 400Ohm/100Mhz
L54 400Ohm/100Mhz
1135
2028
C54 10UF/25V
C43 10UF/25V
AC_BAT_SYS_V
L39 0.56UH
R42 3mOhm
L41 0.56UH
R53 3mOhm
+VCORE
CE2 470UF/2.5V
CE19 330UF/2V
C373 0.1UF/25V
(25A)
C37 10UF/25V
C31 10UF/25V
C68 1U
C 2001uF/50V
CMP
CSP
2403
2112
2113 2311
1306
R106 0Ohm
R93 1KOhm
R94 1KOhm
DPRSLPVR
STPCPU#
VRON
PM_PSI#
CPU_VRON
STPCPU#
DPRSLPVR
VRON
PM_PSI#
2113
2311
2406
R109 100KOhm
R108 75KOhm
C139 100PF
R107 56KOhm
C129 47pF/50V
C133 0.47U
R410 1MOhm
2203 is C536
2407
1306
Title : Vcore
ASUSTek COMPUTER INC. NB1
Engineer: Adams Lin
Size Custom
Project Name A6N
Rev 2.0
Date: Thursday, October 14, 2004
Sheet 38 of 51

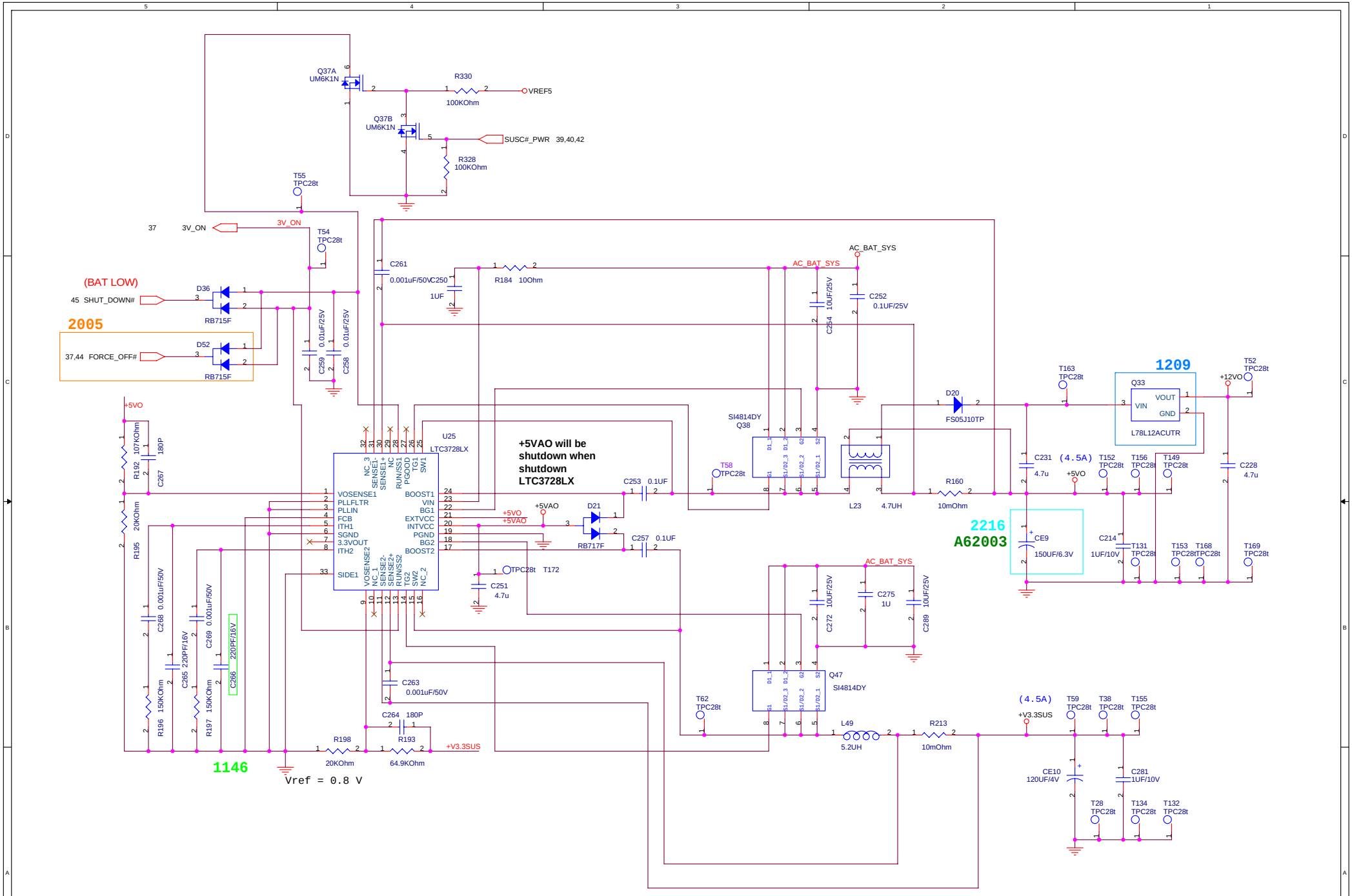


<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : 1.25V&1.8V	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 39 of 51	

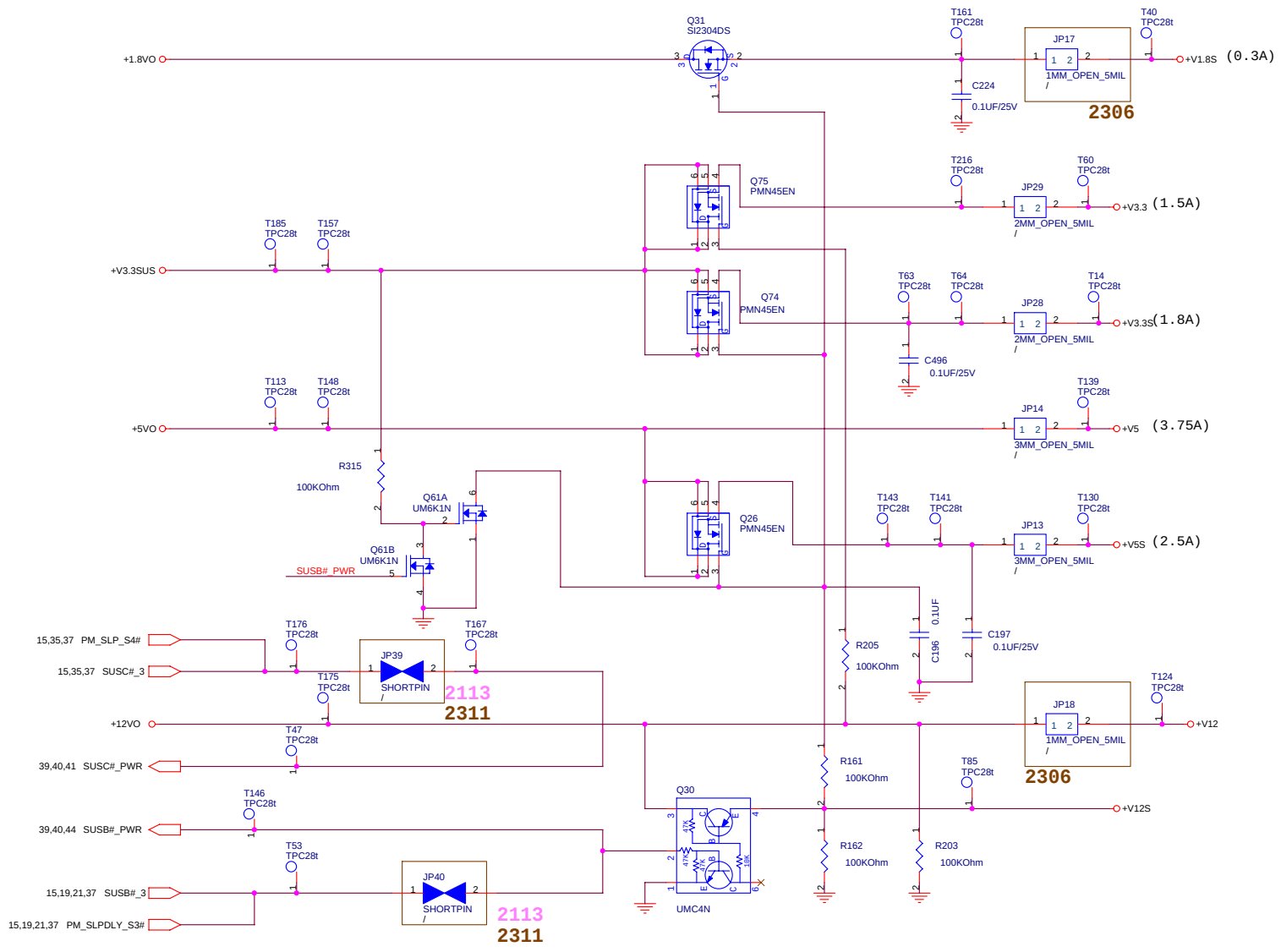


	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4			Pin 1,2



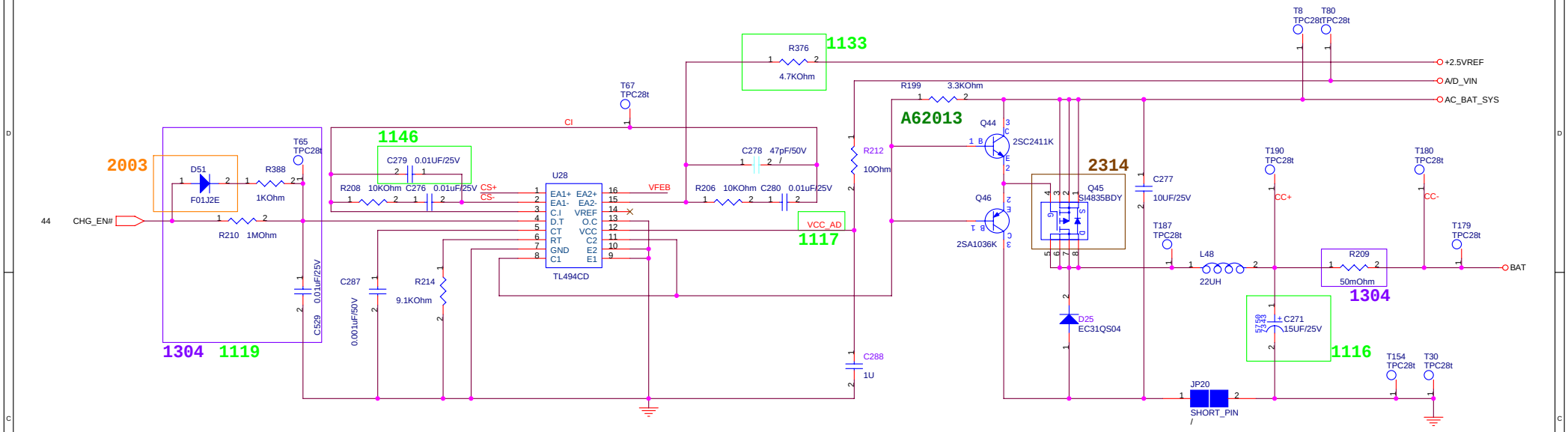
<Variant Name>

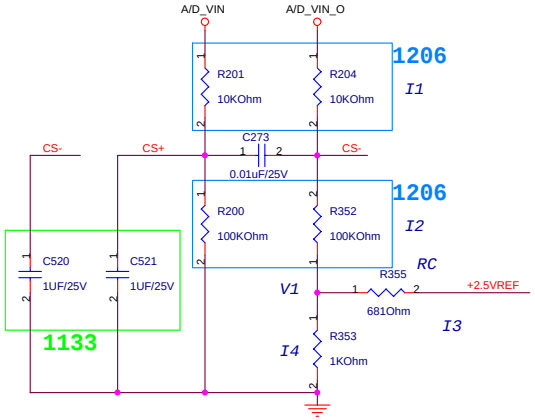
ASUS	Title : SYSTEM	
ASUSTek COMPUTER INC. NB1	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 41 of 51	



<Variant Name>

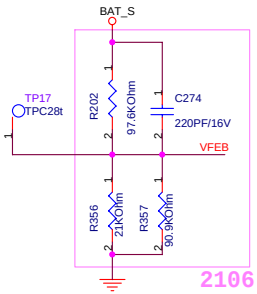
ASUSTek COMPUTER INC. NB1	Title : LOAD SYWITCH	
	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 42 of 51	

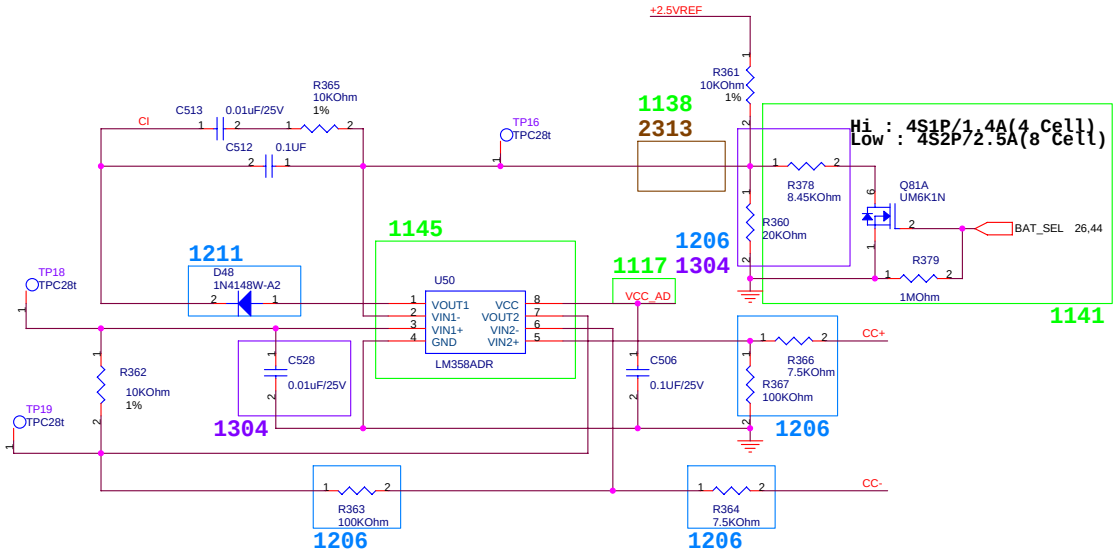




Current sharing = 3.1A

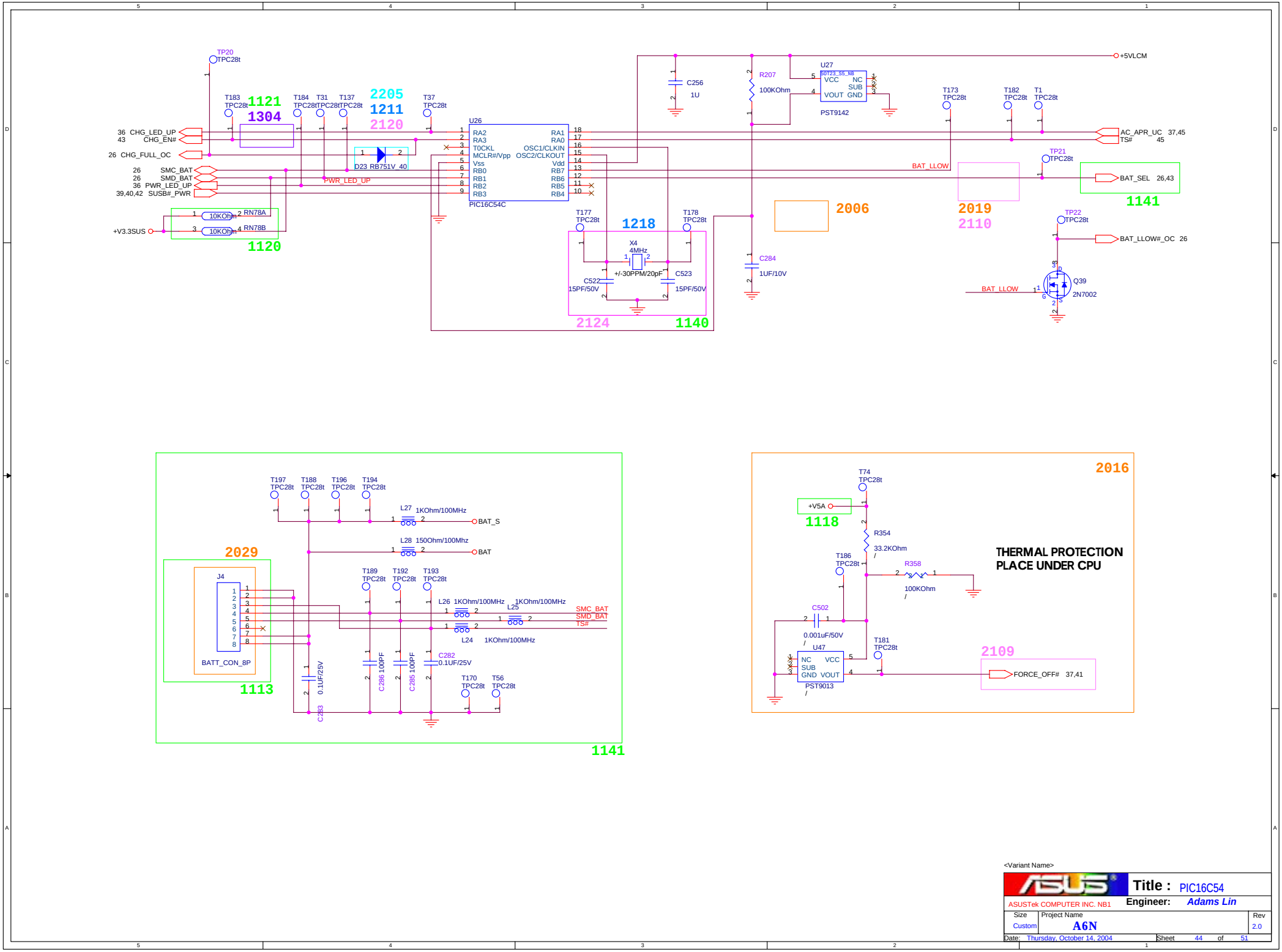
A/D_VIN=19V A/D_VIN_O=19V-3.1A*50mohm=18.845V
CS+=CS-=19*(100/110)=17.272727V
I1=(18.845V-17.272727V)/10K=0.15723mA
V1=17.272727V-(0.15723mA*100K)=1.5497V
I4=1.5497V/1K=1.5497mA
I3=1.5497mA-0.15723mA=1.39247mA
RC=(2.5V-1.5497V)/1.39247mA=681 ohm





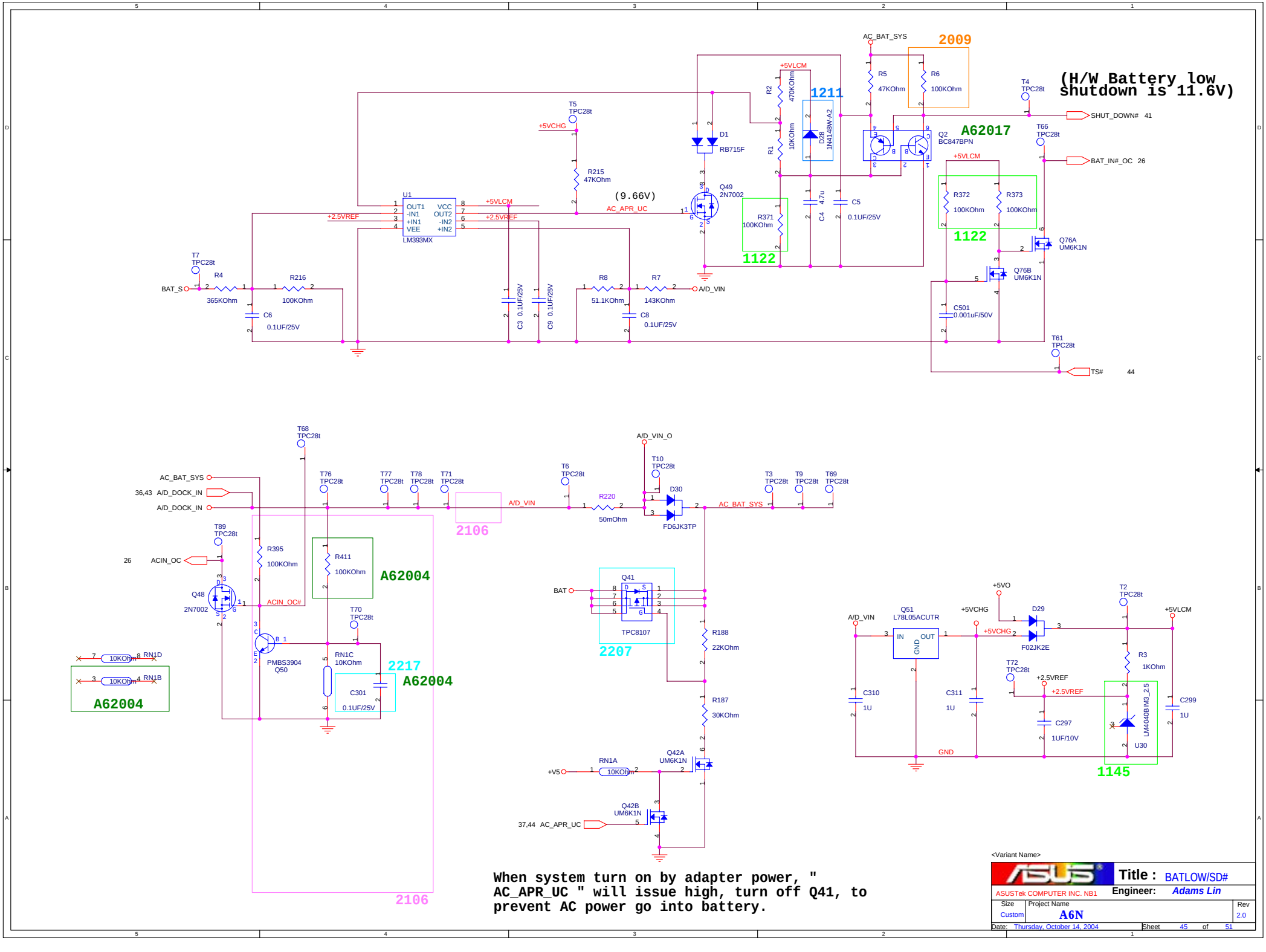
<Variant Name>

ASUS	Title : CHARGER	
ASUSTek COMPUTER INC. NB1	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 43 of 51	



<Variant Name>

ASUS	Title : PIC16C54	
ASUSTek COMPUTER INC. NB1	Engineer: Adams Lin	
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 44 of 51	

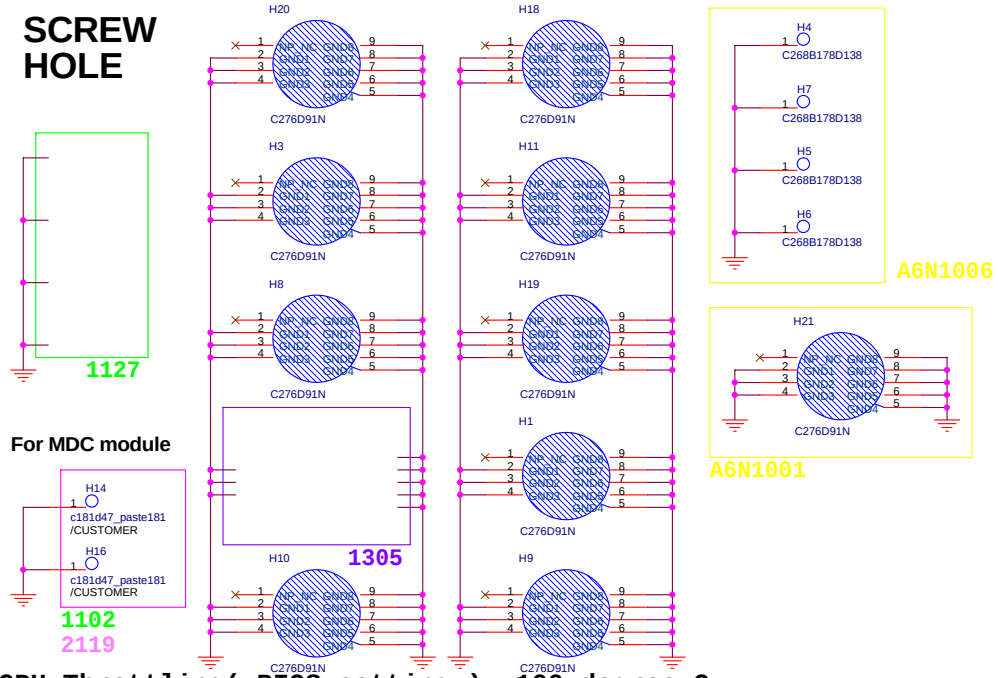


When system turn on by adapter power, " AC_APR_UC " will issue high, turn off Q41, to prevent AC power go into battery.

<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : BATLOW/SD#	Engineer: Adams Lin
Size: Custom	Project Name: A6N	Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 45 of 51	

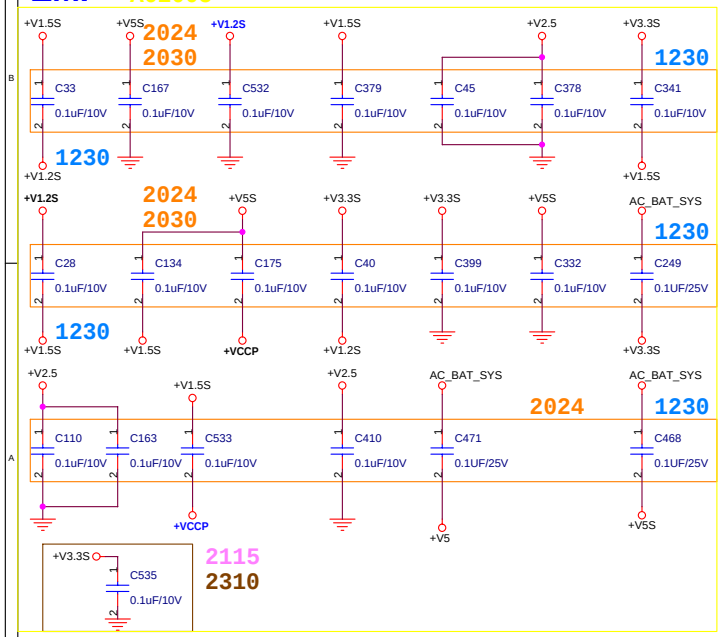
SCREW HOLE



CPU Throttling(BIOS setting): 100 degree C.
System shutdown(BIOS setting) : 110 degree C.
~~H/W shutdown(page 44, U47 , no load) : 105 degree C(Need fine turn R354).~~

EMI

A61005



Short Pad location:
Page37: JP32
Page39: JP4,5,15,16,19,26,27
Page40: JP6,7,9,22,24
Page42: JP13,14,17,18,28,29

Don't Short Pad: JP26
JP4:+V2.5 --Power In
JP5:+V1.25S
JP6:+V2.5(A6N bottom)
JP7:+V1.2S(A6N bottom)
JP9:+VCCP
JP13:+V5S
JP14:+V5
JP15:+V1.5SUS
JP16:+V2.5 --Power IN
JP17:+V1.8S
JP18:+V12
JP19:+V1.8
JP22:+V1.5S
JP24: VREF5-->+V5A(A6N top)
JP26:+3VALWAYS_T-->+V3.3A(open)
JP27:+3VALWAYS_M-->+V3.3A(short)
JP28:+V3.3S
JP29:+V3.3
JP32:KBCRSM

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	20 mils

37.5 OHM	WIDTH
TOP/BOT	12 mils

42 OHM	WIDTH
TOP/BOT	10 mils

55 OHM	WIDTH
TOP/BOT	5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	7 mils/ 10 mils

100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#

CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

Rev	Date	Description
R1.0	03/12/19	1. Initial release.
R1.1 Green Block	04/02/03	1. Connect SDD0,SDD1 for RICOH request. Page 22. 2. Add MDC screw hole P/N & footprint. Page 46. 3. Connect CardBus chip INTC to PCI_INTD#. page 22. 4. Change CB_SD# location from KBC to ICH4 GPIO25. page 15,21,26. 5. Delete PCMCIA debug card function. page 18,23,29. 6. Host clock frequency select failed.Add a pull-down R to FS3 so that FS[4:3]=00 and Host clock frequency=100MHz. page18. 7. Load wrong value. Change RN39~RN48 from 56Ohm to 10Ohm. page 6. 8. Load wrong value. Change pull-up RN . page 37. 9. The value in M3N schematic is wrong. Change HUB_RCOMP_ICH4 pull-up R from 48.7KOhm to 48.7Ohm. page 14. 10. Modify +V3S to +V3.3S. page 30. 11. Can not boot in battery mode.Remove C497. page 37. 12. Modify 20-pin connector pin define and add DJ_LED function for new touchpad. page 26,36. 13. Due to height limitation, change BATT CONN. page 44. 14. Remove the pull-up RN75B because AC_APR_UC has been pulled-up in page 45. page 37. 15. Change CRT CONN because the original one was reversed. page 12. 16. C271 change form 10UF/25V/X5R to 15UF/25V/POSCAP. page 43. 17. U50 VCC change from +5VLCM to VCC_AD(19V). page 43. 18. For wrong connection, change R354 pull-up power plane from +5VO to +5VA. page 44. 19. Change R210 from 47K to 470K/0402. page 43. 20. Add RN78 to pull high SMC_BAT and SMD_BAT, and add UM6K1N to prevent leakage current into KBC. page 26,44. 21. For Power RD request, add R370 to CHG_EN#. page 44. 22. Replace RN32 with 3 single 100K resistor. page 45. 23. Change KB CONN pin definition because R1.0 was reversed. page 26. 24. Remove INVTER_A from KBC and load L33 because BIOS RD decide to use NB to control the pannel backlight. page 12,26. 25. Because P67/AN8 of KBC38857 cannot receive PWM signal, move CPUFAN_SPD_A to P57/DA2/PWM11 of KBC38857. page 26. 26. Change LEDs' power to 5V level. page 36. 27. Modify PCMCIA socket footprint. page 23,46. 28. Combine connector : Change CON1,delete CON3,CON4. page 12, 34. 29. Swap LAN connection(J2 pin5~12) for wrong connecting. page 33. 30. Modify PM_RSMRST# circuit. page 37. 31. For cost down, change X5,X7. page 19,30. 32. Combine two NC7SZ14P5 into one SN74LV14APWR for cost down.page 37. 33. To reduce jitter when charging, add R376,C520&C521. page 43. 34. For M6N R1.1 wrong connection, change Audio DJ DJ_SCAN pin from KSO4 to KSO1. page 26,35. 35. For Power RD request, add two beads L53&L54 at Vin Side. page 38. 36. Modify EDID and panel ID optional circuit. page 12. 37. Change CLR_DJ# to P53 because P54 of M38857 cannot be configured as output. page 26. 38. Add R377 for Power RD request. page 43. 39. Based on Ricoh's suggestion, remove CB_AGND and connect all AGND to generic GND. page 21,22. 40. For cost down, change X4. page 44. 41. Modify for battery 4S2P and 4S1P application. page 26,43,44. 42. For EMI RD request, change Cap of CRT Pi-filter from 3.3pF to 15pF. page 13. 43. Delete spread spectrum IC ICS91718 circuit because few model use it and not easy to buy. page 18.

ASUSTek COMPUTER INC. NB1

Title : 2nd source

Engineer: *John Hung*

Size	Project Name	Rev
Custom	**A6N**	2.0

Date: Thursday, October 14, 2004 Sheet 47 of 51

Rev	Date	Description
R1.1 Green Block	04/02/03	44. Change C172 & C173 from 22pF to 5pF and unload R125 to obtain more accurate 8MHz frequency. page 26. 45. For cost down, Power RD request to change Q9&Q11 to 07-005198012, U30 to 06-006002411, and U50 to 06-010112010. page 38,43,45. 46. For Power RD request, change , C266 from 33pF to 220pF, C279 from 0.1uF to 0.01uF. page 41,43. 47. Change U29 P/N for ME. page 31.
R1.2 Blue Block	04/02/19	1. LAN_RST# changes to 10K Ohm pull-down to GND. Page 15. 2. To be able to hear low frequency in headphone mode, change C423 & C424 from 10uF/10V to CE30,CE31 47uF/6.3V. Page 31. 3. Pull high BAT_IN#_OC, whose OC means Open Collector, to +V3.3 at KBC. Page 26. 4. There is only one SS0540 in A3N, change to 1SS355. page 35. 5. The power of LCD EEPROM connect to +V3.3S_LCD. When BIOS want to read EEPROM data, the EEPROM is still OFF,because +V3.3S_LCD is not enabled at this moment. Change EEPROM power to +V3.3S. page 12. 6. Change R360,R363,R364,R366,R367,R378 value for charger at C.C. mode and change R200,R201,R204,R352 at C.S. mode to get more accurate current limit value. page 43. 7. Add de-POP(reduce pop noise) circuit. page 31. 8. Change Fan control function from PWM mode to DC mode. page 35. 9. Based on Power RD's request, change Q33,R169,R148,R324. page 40,41. 10. S5N can not turn on some panels since its diodes in inverter circuit have higher forward voltage. Follow S5N, change DAP202K and 1SS35 in inverter circuit to Schottky diode RB717F and RB751V-40 respectively. page 12. 11. Electrical characteristics of diode 1SS35 and 1N4148-A2 can be compatible, but 1N4148-A2 has lower price. For cost down, change 1SS355 to 1N4148-A2. page 12,16,21,35,37,40,43,44,45. 12. Change "Back light adjust" function from North Bridge to KBC. Change "CUPFAN_SPD_A" from KBC to ICH4 for BIOS request. page 8,12,26,35. 13. For cost down, change audio AMP from APA2020A to G1420. page 31. 14. A3N R1.1 uses the same AC_IN jack as L3F, which was found easy to be damaged. Change it to solider one used on A2. page 36. 15. Follow M6N and W1N to modify RTC circuit. page 15. 16. Un-mount Q59 and RN81 to control WLAN led directly from SB's GPIO pin: 802_LED_EN#. page 36. 17. Swap 1394 TPB0+/-,TPA0+/- for smoother layout. page 22. 18. X4 is dip type and at top side which may be lost in SMT IR re-flow for bottom side. Change X4 to SMD type. page 44. 19. Add mini-PCI and USB WLAN hardware disable circuit page 12,15,20. 20. QT report a bug: The "Center/Subwoofer Speaker Out" is invalid after setting "Number of Speakers" to 6-channel mode for 5.1 speaker output and then executed "Speaker Test". Modify relative circuit. page 30,32. 21. Fine tune audio amp low-pass frequency. page 31. 22. Delete RN79 because after experiment we find it can be un-mounted. page 36. 23. Remove LCD EDID relative circuit. page 8,12. 24. Combin R191,R308,R380 and R381 into 4R8P RN88. page 26. 25. Follow S5N to modify CRT_DDC circuit to prevent current leakage. page 13. 26. Although crystal DIP type is cheaper than SMD type, but costs more manpower. Change X5 and X7 back to SMD type. page 19,30. 27. Improve accuracy of reading fan speed. page 35. 28. Swap RN4 and pin8,9 of RP4 for smoother layout. page 13,17. 29. For cost down, change U6 and U12 NS LM358MX (06-010008000) to TI LM358ADR (06-010112010). page 30,35. 30. For EMI RD's request to modify BOM. page 18,19,22,30,31,32,33,46. 31. Add description of choosing 855GM or 852GM/GME/GMV platform by changing R148. page 40. **32. Debug code will stop at "A0" or "06". Modify SMBus layout: 1. Daisy chain routing. 2.Don't cross power plane when the trace refer to power plane. Page 17.**

Rev	Date	Description
R1.3 Purple Block	04/03/11	1. Pin23, ISOLATEB, of LAN 8100CL need to be low in S3. Follow MB P4PE-X to connect it with PM_SLP_S3#. page 19. **2. Debug Code will stop at "13". Change SMBus Pull-High RN29 from 4.7KOhm(0402) to 1KOhm(0603). page 17.** 3. Improve MIC layout. page 12,32. 4. For Power RD's request to modify charger circuit. page 43,44. 5. Delete screw hole H2, to prevent CN7 short with H2. Layout engineer create a new screw hole. page 46. 6. For Power RD's request to modify BOM. Change R108 from 100K to 75K for OCP, un-mount R93 and mount R94 to meet Intel CPU spec. page 38.
R2.0 Orange Block	04/04/15	1. Sometimes Debug Code will stop at "00" in ON/OFF test. Modify power sequence circuit , delete R163. page 38,40. 2. Based on request came from factory to update all testpoints' symbol because all testpins are changed from 75mil to 68mil. All pages that include test points. 3. Power team request, cost down D51 part. page43. 4. Fine-tune R385,R386 and R387 to get more accurate level of fan ON/OFF detection. page35. 5. When system with battery only. System can't be power on after push Force OFF button SW6. Because SW6 connect to SHUT_DOWN#, but this signal will be latch low(power design: when battery low, page 46 : battery low detect circuit will issue low than latch it.) when it is at low state. Don't connect SHUT_DOWN# to SW6 at page 37.(SHUT_DOWN# already connected to 3V_ON at page 41. Connect SW6 to U25, and change D40 to 1N4148(delete at item 2015). Page 37. 6. Because A3N use SW6 as "Force OFF" button ,not "Reset" button. We don't need connect SW6 to PIC16C54C. Delete D24.page37,44. 7. Can't turn on Audio DJ when system only with battery and no adapter. Because +V3.3SUS will be turn off when system only with battery. Need turn on +V3.3SUS by connect DJ_SW# to 3V_ON. Change D45 to DAP202K. Page 37. 8. LAN crystal accurate is 39.2ppm, it can't meet spec. +/-30ppm). Change from 15pF to 18pF to meet spec. page 19. 9. Some system can't boot by battery only. Because signal "SHUTDOWN#" be latch at low state. Change R6 value from 470K to 100K. Page 45. 10.QT bug : Noise occur from headphone via speaker out jack. Change R124,R298,R285 from Bead to 0 ohm. Page 30,31. 11.The Power LED should not be bright when enabled Audio DJ in power off mode. Page 36. 12.The inductor will cause the 2.5V power control loop unstable. Change L40 to R389 Page 19. 13. Balance the LED Brightness. Fine tune R value,R140 470-->220,R311,R312 470-->1K. Page 36. 14. G571(U49) 593 Control Signal(U37) VPPD0 : VPPEN1 VPPD1 : VPPEN0 Otherwise, CardBus Card may be destroyed. Page 23. 15. When issue OTP_RESET#, system can't be turn off & display white screen. Because LTC3728 can't be shutdown by only put low 3V_ON. Need shutdown +V3.3SUS & +5VO at the same time. Delete D40. Page 37. 16. Change Q63,Q66,Q71 and no load Q63,R338,C482,R354,R358,C502,U47 for cost down. page 35,37,44. 17. Add test point for Taipei Factory request. page 6,12,15,16,19,30,36,37,38,39,42,43,44 18. QT bug: Pop noise can be heard via headphone when system boot, restart and resume from S3. Modify De-Pop circuit. page 31,37. 19. Taipei factory request : Add R391 for different battery charge current test at 8 cells and 4 cells. Page44.

ASUS	Title : REVISION(2)		
ASUSTek COMPUTER INC. NB1	Engineer: John Hung		
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 48 of 51		

Rev	Date	Description
R2.0 Orange Block	04/04/27	20. EMI request, load C144, C525. page 32. 21. ICH4 GPIO [24:43] , default state is output high, if PID_[0:3] be connected to GND by LCD cable, these GPIO will issue +V3.3(default output high) short to GND during system power on. Add R=2.2K to prevent this kind of situration. Page 15. 22. Measurement team Problem: VGA EA fail below items 1,V-SYNC:under shoot over 30% of high level voltage range. 2,H-SYNC:over shoot over 30% of high level voltage range, under shoot over 30% of high level voltage range. Change Change C304, C305 from 5pF to 33pF. Page 13. 23. EMI request use Choke on USB & 1394 ports. Delete option R, don't co-layout. Page 22,34. 24. EMI request : Add C531,C532,C533,C535. Delete C147,C433. Change C110,C163 connection. Change C410 location. Change C378,C379,C410,C163,C110 to 0.1uF/10V. Change C471,C468 to 0.1uF/25V. Change C45,C33,C28,C134,C332,C399,C341 to 0.1uF/10V and don't load. Change C40 to 0.1uF/10V. Change C249 to 0.1uF/25V and don't load.Page 10,46. Change R104 from 0 ohm to bead. Page 31. 25. Change C26,C98,C104,C325(page3), C362(page7), C324,C329(page9), C436(page14), C190,C441(page16), C366,C367(page19), C247(page21), C467,C473,C478(page22), C236(page23), C209,C210,C211,C242(page40), from 0.01uF/25V to 0.01uF/10V. Use 10V is OK. 26. Measurement team Problem: VGA EA fail in rise time and fall time of RGB signal at resolution 1024X768 at 60Hz. Change L6,L7,L8 from 75Ohm/100MHz to 70Ohm/100MHz. Page 13. 27. Load FAN on/off component : /FAN_SPD. page 35. 28. Change L53,L54 from 09-012400000 to 09-012400001 for cost down. page38. 29. CON1,CON7,CON12,CON15 and J4 change to formal P/N. page 12,24,25,36,44. 30. For EMI RD's request, change R384 from 0 ohm to Ferrite bead, and add EMI capacitors: C28,C33,C45,C134,C167,C175,C332,C341,C399,C249. Page 32,46. A3L. For A3L platform : change U32 to 852GM, R148. page 6,7,8,9,40.
R2.1 Pink Block	04/05/14	1. For ESD test fail at switch, If we want to use ESD protect diode, we can't connect switch pin 1&2, pin3&4 to make sure the energy will go through ESD diode : SW1~5. page36. 2. Forget pull high at D54.3. Add R392 pull high to +V3.3S. page 31. 3. For cost down. Delete R=0 OHM. R389,R331,R124,R298,R285,R281,R276(no load),R290(no load). page 19,22,30,31 4. QT report that a "pop" noise occurs when booting. This is because the timing of OP_SD# to control audio AMP ON. Change D49 from DAP2020K to 1N4148W-A2 to control the AMP shutdown only the JACK_IN#, and control SE/BTL# by D54.3. page 31. 5. In audio DJ mode, DJ_LED turns on Q91 and PWR_LED_UP will connect to GND which may demage PIC. Use RN80A to prevent it. page 36. 6. Power RD modification: Delete 0 Ohm: R135,R136,R137 Delete U24, change Q34 to 3904 and add R393,R394. Change R202,R356,R357 BOM to modify BAT CV tolerance to more accurate. Delet Q5,Q1,C18,R9,R10,RN2 and add R395. page 40,43,45. 7. Swap RN80 for smoother layout. page 36. 8. QT bug: when booting or being idle, two A3 with USB CCD module will sometimes appear "Hi-speed device plug into low-speed hub" in Windows XP/2000. Adjust USBRBIAS and USBRBIAS# external resistor R138 from 18.2ohm to 22.6ohm. page 15.

Rev	Date	Description
R2.1 Pink Block	04/07/16	9. For TPE_ENG Power RD's request to unify OTP_RESET#, FORCE_OFF#_SW and FORCE_OFF# into single name: FORCE_OFF#. page 37,44. 10. About 2019 item, factory don't need it now. Delete R391. page 44. 11. C117 don't need use 25V, change to 4.7uF/10V. page 9. 12. Factory found that there are two A3 systems will fail at On Off test. Net " PM_DPRSLPVR" will be issued wrong status by Vcore Power IC MAX1987 when system on . Add a 20pF at R106.2 or change R106 from 1K to 0 OHM can solve this issue. Change R106 to 0 OHM. Page 38. 13. Power request. Don't need use 1K ohm, change R100,R292,R329,R168 from 1K to 0 ohm. Page 38,42. 14. Fine tune E-mail LED (R140 : from 220 to 1K)& Wireless LED (R312 : from 1K to 680) for customer's request. Page 36. 15. Because C535 will touch with the boss of C mechanical part. Don't load C535. Page 46. 16. Even we pull down pin 1 or pin 2 of DAP202K, the UM6K1N is still possible to be turn on. It is because that the maximum forward voltage of DAP202K is 1.2V but the gate threshold voltage of UM6K1N is 0.8V~1.5V. Change D32,D45 and D54 from DAP202K to RB717F since the maximum forward voltage of RB717F is only 0.37V. Page 31,35,37. 17. Phone jack (P/N: 12-140001087) used in A3N/L has been phased out. The vendor suggests us to use 12-140001088 as substitution. Page 31. 18. As R2.1 item 16, we changed D32,D45 and D54 from DAP202K to RB717F. But SMT reports that RB717F has smaller package than DAP202K such that may cause connection between RB717F and pad failed. In A3 design, the forward current will be no more than 0.5mA. According to DAP202K forward characteristics, it's impossible to reach the minimum threshold voltage of UM6K1N (0.8V). So it's safe to change D32, D45 and D54 from RB717F back to DAP202K. Page 31,35,37. 19. 5E customer doesn't need the MDC and SIR function, so A3L removes the relative components: R30, R31, R129, R143, R144, R186, R190, R305, RN21, RN66, RN67, C149, C174, C180, C185, CN6, CON5, H14, H16, U35. Page 15,28,30,33,46. 20. D23 uses DIODE 1N4148W-A2 but its larger forward voltage may makes KBC M38857 detect error. Change it to Schottky diode SS0540 that has smaller forward voltage. Page 44. 21. Taipei SMT reports that X2 (07-010303271) has open risk, and recommends us to use 07-010303273 as first source, 07-010303271 and 07-010703273 as second source for manufacturability improve. Page 15. 22. Factory found that there are some X4 part don't work. Change C522,C533 from 33pF to 15pF. Page 44.

ASUSTek COMPUTER INC. NB1

Title : REVISION(3)

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 49 of 51

Rev	Date	Description
R2.2 Light Blue Block	04/09/22	3. Refer to R2.1 item 12, reserve C536 but load 1M ohm for PM_DPRSLPVR. Page 38. 6. Modify layout footprint for R:2.1 item 21. Page 15. 7. Based on Power RD's request, change Q41 from 07-005151010 to 07-005159010 for cost down. Page 45. 8. 7H Project Vulpix : Remove Super I/O : U11,C143,C146,C127,C151,C136,R103,RN17,Q16,R82,R63. Page 27,18. Remove Printer Port : LN1,LN2,LN3,LN4,CN8,CN9,CN10,CN11,L36,CN7,C300. Page 28. Remove IR: R129,U35,C174,C180,C185,RN21,RN66,RN67. Page 28. Remove MiniPCI Port : CON17,C487,C485,C469,C486,C470,R332,R81. Page 20,18. Remove WLAN function : RN86,Q87,Q88,Q79,R312. Page 12,20,36. Remove USB CMOS camera & USB WLAN funciton : CE29,L51,L52,L50,C11,C12. Page 12. Set normal type ODD as master : No load R127, Load R126. Page 25. 9. Power "VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB" have different defined value in datasheet and RDDP. Confirmed with Intel FAE to get the final correct value, and will be phased in on R2.2 and R:2.4 BOM. Page 9,40. 10. R249,R251,R252 will have different value based on different North Bridge. All the corresponding values are listed in Page 7 and will be phase in on R2.2 and R:2.4 BOM. Page 7. 11. Because Vendor (CC&C) can't support hardware On/Off WLAN module function, don't load Q87 at R:2.2 & R2.4. Page 12. 12. Factory found that there are some DDR SO-DIMM(UNIFOSA,MOSEL)will fail during Memory test of Run-In test. Change R176 from 19.6K to 20.5K 1% , fine tune +V2.5 from 2.5V to 2.592V. Add SO-DIMM noise margin at R:2.2 & R:2.4. Page 40. 13.For 5E customer,don't need USB CMOS camera,no load L51,C12. Page12. 14. Change C193,194,195 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.5mm height(11-03B210621) to 2.0mm(11-031110621). Page 40. 15. For M/E request, add a second source 12-172010300 on CON2. Page 12. 16. Change CE9 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.8mm height(11-08D210711) to 1.8mm(11-08D215706). Page 41. 17.When the system temperature rise high due to the system running at heavy loading. The leak current(IR) of D30 schottky diode will be increased, the H/W AC detect circuit will make a wrong state. Net " ACIN_OC " will issue " high". Change C301 from 0.1uF to 1Kohm, it can solve this problem. Make sure it will issue "low" at this moment.Page 45. 18. For the request from 7H customer, change CE15,CE18 from Tantalum capacitor (11-015000220) to Oxi capacitor. Page 9. 2004/9/29 : Change at VPLP R:2.2, A3L R:2.4,A3Le R:2.4,A3Ne R:2.4. 19. For the request from 7H customer, follow the USB spec. , one port max current is 0.5A, so two ports max current is 1A. Change F1,F2 from 1.5A/6V polyswitch to 1.1A/6V polyswitch, P/N is 07-014110900 (2nd source is 07-014110201). Change at VPLP R:2.2 only. Page 34
	04/10/01	20. 7H customer found that there are some VPLP system use Bufferlo WLI-CB-AG54 Wireless LAN PC-card will fail at some channel when connect to Access Point. Add C390 with 10pF and change C499 from 0.1uF to 1000pF (11-034110241) to reduce clock and power noise. Modify VPLP BOM onley. Page 18,23.
	04/10/14	21. +V5A will issue leakage current to +V3.3SUS by U48.4 --> D45 --> RN76B when plug in Battery module only. Change C379 from 0.1uF to 1K ohm (10-004401020). Page 46.

Rev	Date	Description
R2.3 Brown Block	04/07/23	1. For Vendor request : Pin footprint diameter is 1.0mm+/-0.05, but ASUS rule is diameter*diameter =(L*L+W*W). Modify Battery Connector J1 as vendor spec. **NO FIX**. Page 44. 2. For Thermal RD request : Let the fan be off before BIOS control because it can let user doesn't feel the fan on-off noise obvious while system boot. Use OP_SD_DLY to control it. Page 31,35. 3. None (the same as R:2.2 item 1) 4. QT Bug: Noise occurred during system resume from S1. The timing of DLY_OP_SD# and AC97_RST# still can not prevent the pop noise. Realtek recommands to use pin47 EAPD to substitute AC97_RST#. This pin can be controlled by codec driver to meet our timing request. Page 30,31. 5. Change D23 to SCHOTTKY RB751V-40 to decrease part type. Page 44. 6. Modify short pad for factory's request. page 37(JP32), page 39(JP15,16,19,26,27), page 40(JP9,24), page 42(JP17,18). 7. For A3 series ID2 power switch, add a Blue LED,change R309 from 470 ohm to 220 ohm. Page 36. 8. Add CPU +VCCA power switch circuit to meet Celeron/ Banias/ Dothan(400)/ Dothan(533) CPU spec. Page 3,4,18. 9. Base on Factory SMT request : modify CN7 & CON9 footprint (only for 1.6mm thickness PCB). page 13,28. 10. Re-load C535 because the position is changed and will not touch with boss of C mechanical part. page 46. 11. Modify R106, R100, R292, R329, R168 to Short Pin JP36, JP37, JP38, JP39, JP40 for power function parts cost down. page 38,42. 12. To synchronize the parts in the schematic with BOM, change R104, R302, R303, R91, R92, R384, R111, R112, R31, R30 to L55, L56, L57, L58, L59, L60, L61, L62, L63, L64. page 31,32,33. 13. Remove 0 ohm: R377 and R180 for cost down. page 22,43. 14. Based on Power RD's request, change Q45 from 07-005151010 to 07-005159010 for cost down. Page 43. 15. BIOS RD request to distinguish PCB version by reading PCB_VID[2:0]. Change PCB_VID[2:0] configuration and add descriptions. Page 21. *. Because R:2.4 item 2. We can't phase in R:2.3.
R2.4 Gray Block	04/08/27	1. To improve ESD margin. Add De-Bounce circuit. Page 36. 2. Add GST[2:0] strap circuit for supporting Dothan 533 CPU. Page 8. 3. Taipei Factory repored that some A3N systems still failed(13/5000) in resuming from suspend to RAM. Power RD request to change JP36 back to R106 and change the value to 100K ohm. Page 38. 4. For EMI request. Connect switch pin 1&2, pin3&4 of SW1~5. page36. 5. Change PCB VID for R.2.4 page 21. 6. Remove JP37 and JP39. page36. 7. As R2.4 item 3, Power RD find the root cause: When system booting or resuming from S3, the siganl " PM_DPRSLPVR" from South Bridge, it will be floating in a short time(40ms) and cause +VCORE output wrong voltage(0.76V). Add a resistor 1M ohm between net " PM_DPRSLPVR" and GND in order to keep PM_DPRSLPVR at low state when floating. Add R106 = 0ohm and change C536 to R410 (1M ohm). page 38.

ASUS	Title : REVISION(4)		
ASUSTek COMPUTER INC. NB1	Engineer: John Hung		
Size: Custom	Project Name: A6N		Rev: 2.0
Date: Thursday, October 14, 2004	Sheet 50 of 51		

Rev	Date	Description
A6N R1.0 Yellow Block	04/08/27	1. Add a screw hole. page 46. 2. Delete WLAN USB port and swap some USB port for layout request. Delete L52,C518,C519,C11.Page 12,15,17,34. 3. Change all test point from S00050(part number) to S00049. All Pages. 4. Power team request : CM2855 will be phased out after 2004/09, change part to SI9183, change R398,R400 value, and delete R405.Page 4. 5. For EMI request, change capacitor connection. Page 46. 1. C33 +V1.2S-----+V1.5S 2. C378,C45 +V2.5-----GND 3. C379 +V1.5S------GND 4. C332 +V5S--------GND 5. C535 +V3.3S-------GND 6. C471 +V5 ----------+AC_BAT_SYS 7. C468 +V5S----------+AC_BAT_SYS 8. C533 +V1.5S----------+VCCP 9. C134 +V5S-------+V1.5S 10. C28 +V5S---------+V1.2S 11. C175 +V5S-----+VCCP 12. C341 +V3.3S--------+V1.5S 6. For layout request. Modify screw hole. page 46. 7. Swap pin1~6 of CON7 connection for new Touch Pad membrane. Page 36. 8. For ID team request. Change the color of CRT connector. Page 13.

Rev	Date	Description
A6N R2.0 Green Block	04/09/23	1. Change C193,194,195 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.5mm height(11-03B210621) to 2.0mm(11-031110621). Page 40. 2. For M/E request, add a second source 12-172010300 on CON2. Page 12. 3. Change CE9 for 7H customer's request about the gap betweed these capacitors and Mechanical C part. Change Cap from 2.8mm height(11-08D210711) to 1.8mm(11-08D215706). Page 41. 4. Power: When the system temperature rise high due to the system running at heavy loading. The leak current(IR) of D30 schottky diode will be increased, the H/W AC detect circuit will make a wrong state. Net " ACIN_OC " will issue " high". To solve this problem, change RN1B (10K ohm) to R411 (100K ohm) to make sure it will issue "low" at this moment. Change C301 from 1K to 0.1uF at A6Ne R:1.1 Page 45. 5. For the request from 7H customer, change CE15,CE18 from Tantalum capacitor (11-015000220) to Oxi capacitor. Page 9.
	04/09/30	6. Measurement team test fail at CRT function : Pattern: White cross hatch with one pixel lines on black background at 31 kHz. Change R40 from 137 ohm to 127 ohm. Page 8.
	04/09/30	7. Measurement team test fail at Audio quality : PC-D-A (Back Panel). Change L56,L57 from Bead to 0 ohm, P/N is 10-003400000. Page 31.
	04/09/30	8. Factory found that some Aluminum Electrolytic capacitor CE29, CE11, CE12 will fail at soldering process. Change them to OxiCap. Page 12,34.
	04/10/01	9. Factory found that some Aluminum Electrolytic capacitor CE30, CE31 will fail at soldering process. Change them to OxiCap. Page 31.
	04/10/06	10. Measurement team tested SMB waveform fail, fail item : Data & Clock will issue Glitch at falling edge. Add C541, C542, C543, C544, C539, C540, C545, C546 with 100pF to fine-tune SMBUS signal quality. Page 5,10,15,18.
	04/10/01	11. +V3.3A will issue leakage current to +V3.3SUS by CON1 pin 8,14 and L31, R343. Change R343 to diode D55. Page 37.
	04/10/01	12. A3 series tested fail at ESD function. To improve ESD function. Change 4pin Switch to 5pin switch. Add a GND pin. Page 36,37
	04/10/05	13. For the request from power team Adams, change R199 from 0603 to 0805 package. Page 43.
	04/10/05	14. For EMI engineer request, add R412, R413, R414 for test. Page 31.
	04/10/12	15. The position pin of CON9 & CN7 are base on 1.2mm PCB design, but A3& A6 PCB is 1.6mm. Modify the length of position pin of these connector. Page 13,28.
	04/10/12	16. For cost down , add 06-045021010 AUDIO AMP. TPA0102 (power is 1.5W)as first source and change original part (power is 2W) as second source. Page 31.
	04/10/12	17. For power team request. Change Q2 from UMZ1N(Not easy buy it) to BC847BPN. Page 45.
	04/10/14	18. +V5A will issue leakage current to +V3.3SUS by U48.4 --> D45 --> RN76B when plug in Battery module only. Change C108 from 0.1uF to 1K ohm (10-004401020). Page 19.

ASUSTek COMPUTER INC. NB1

Title : REVISION(3)

Engineer: John Hung

Size	Project Name	Rev
Custom	A6N	2.0

Date: Thursday, October 14, 2004 Sheet 51 of 51