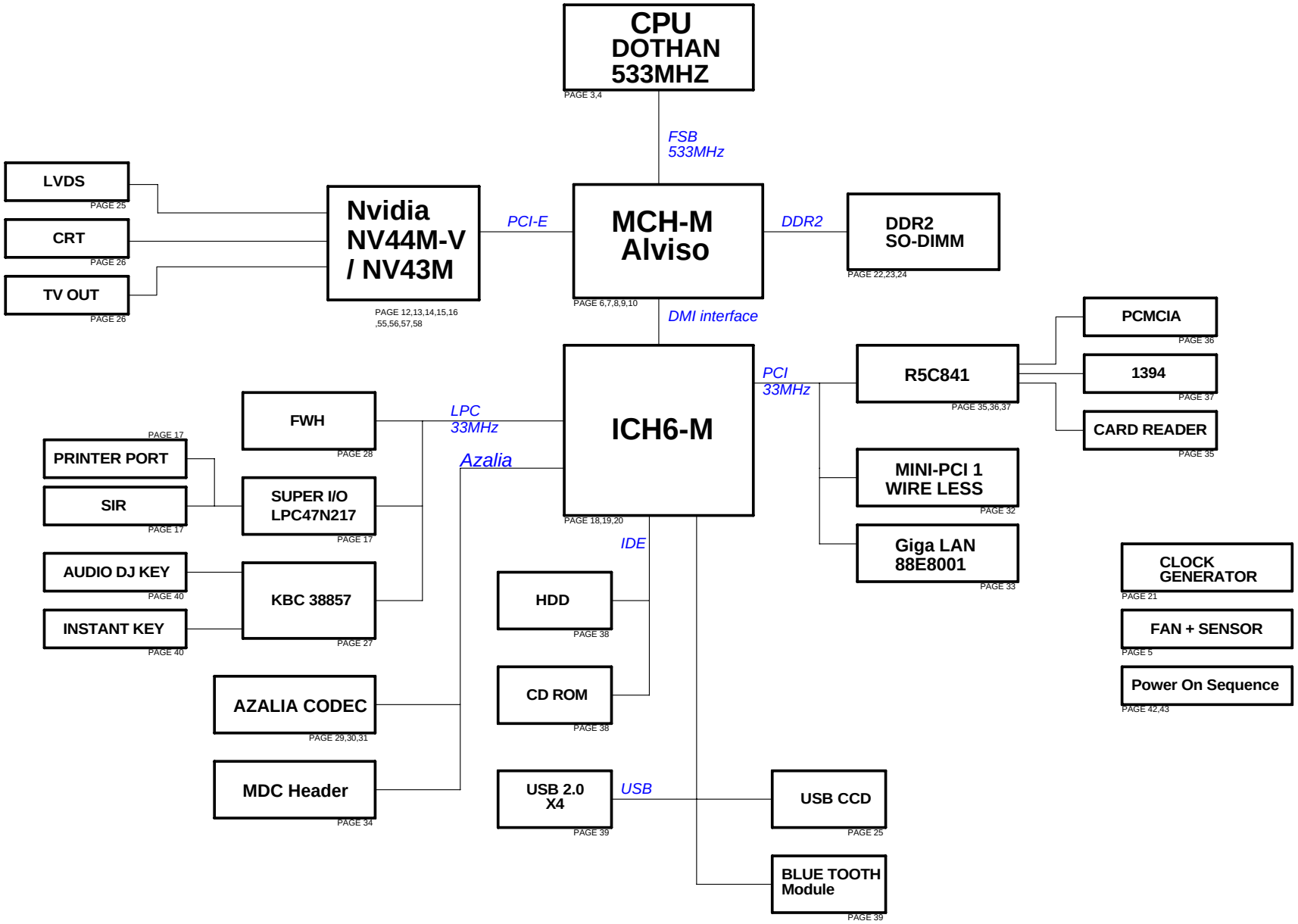
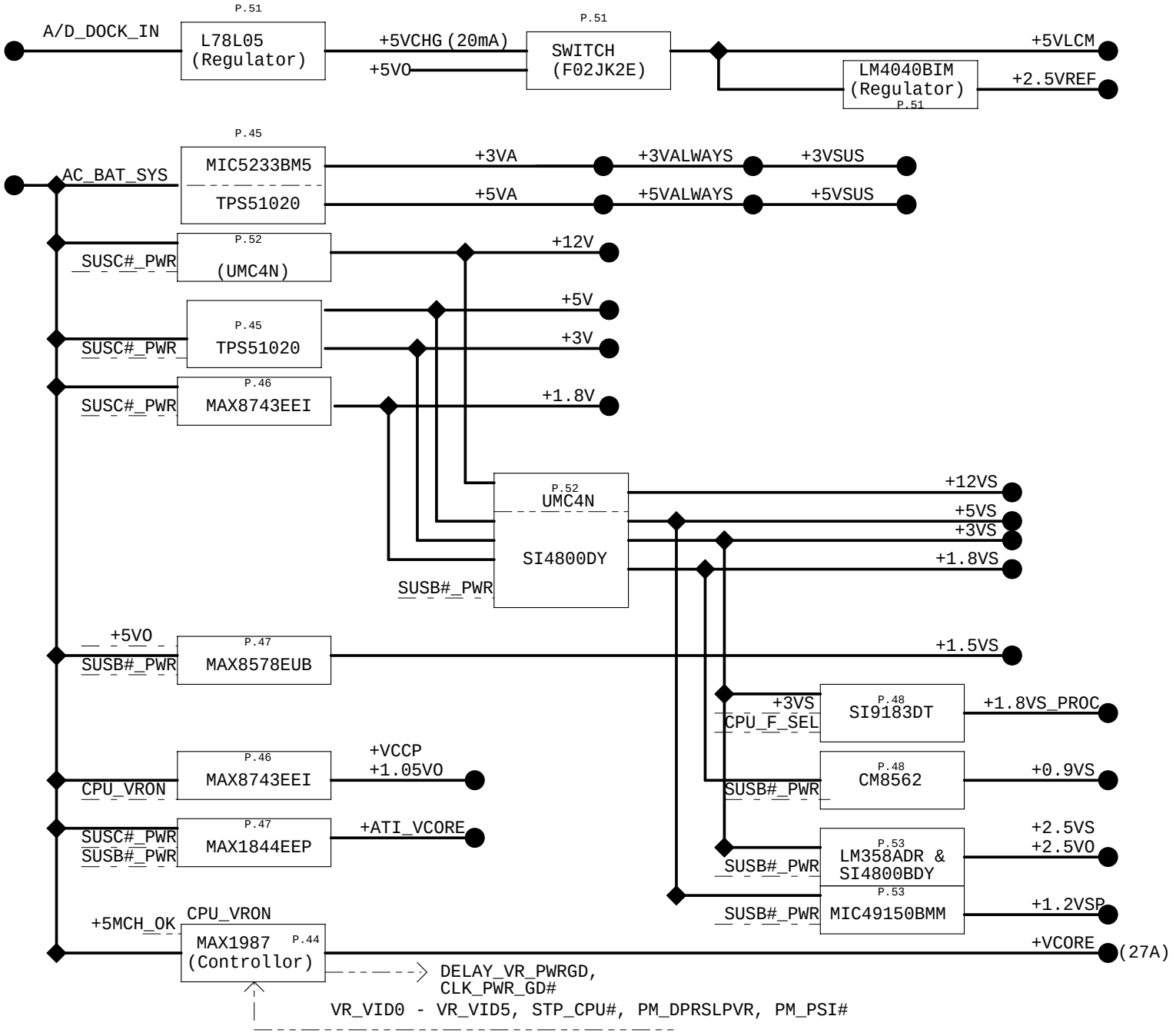
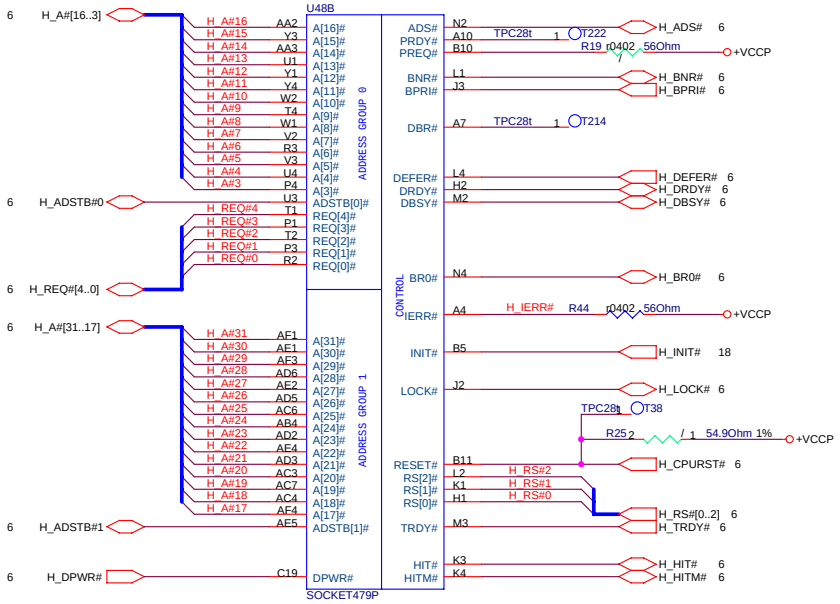
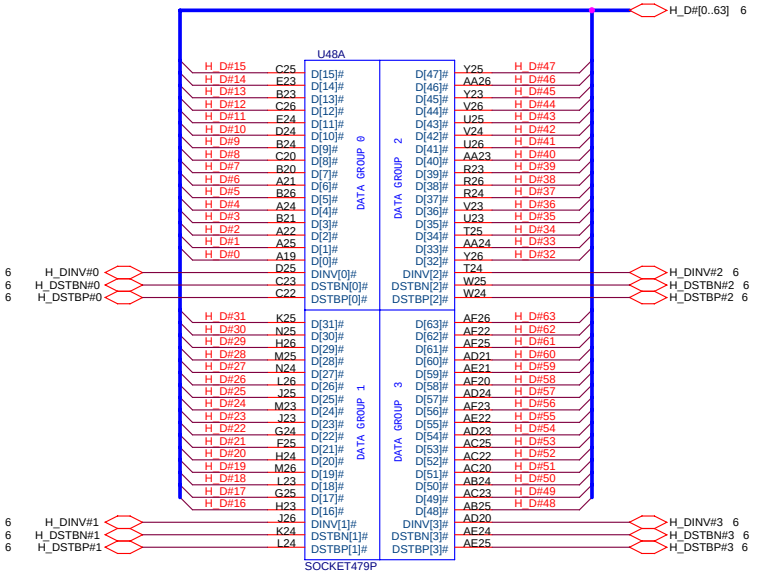


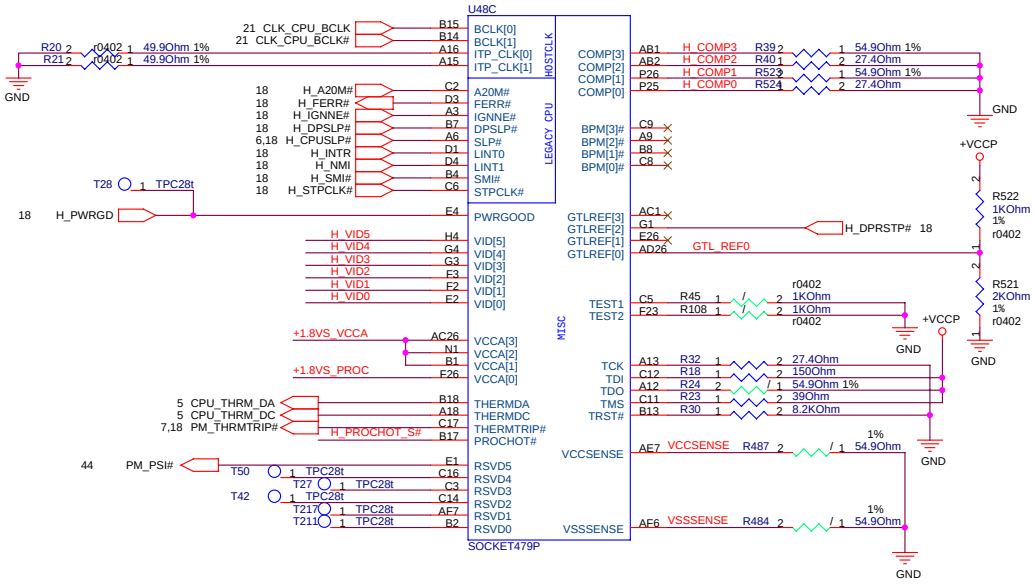
ASUS	Title : BLOCK DIAGRAM	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 1 of 58	



ASUS	Title : Power Block Diagram	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 2 of 58	





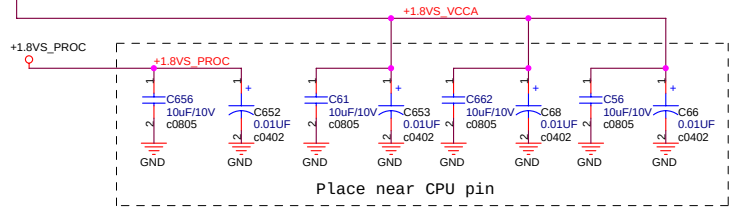


Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"

120mA / 20mil

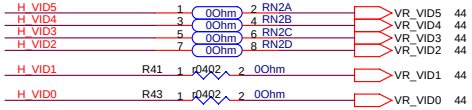
FSB 400MHz -> 1.8V
FSB 533MHz -> 1.5V



H_PWRGD R42 200Ohm 1%
H_PROCHOT_S# R22 56Ohm
+VCCP

			A-STEP	B-STEP
Bclk	FSB	BSEL1	BSEL0	BSEL0
100	400	0	0	1
133	533	0	1	0

Dothan FSB533			
	Min	Typ	Max
VCCA	1.425V	1.5V	1.575V
	Min	Typ	Max
ICCA			120mA



ASUS

Title : DOTHAN CPU(1)

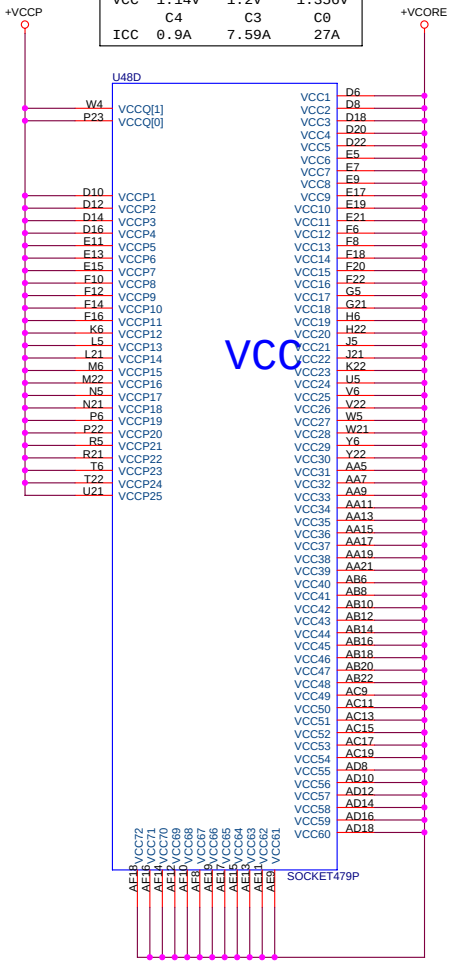
<OrgName>

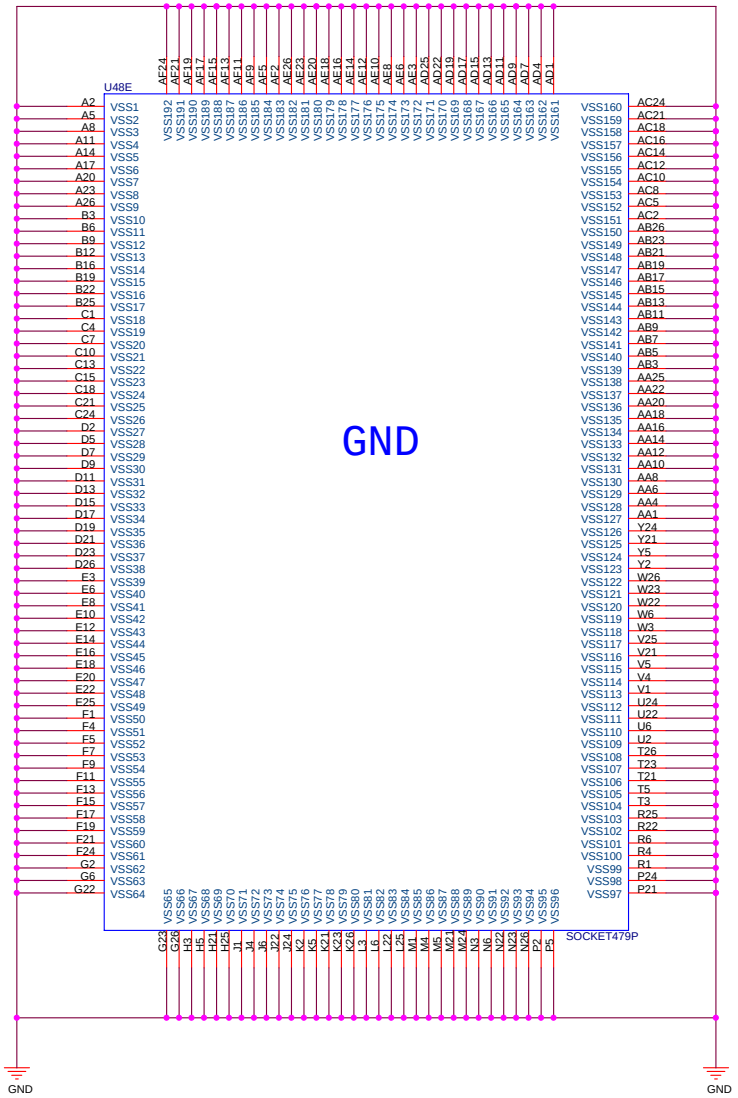
Engineer: *Mark Lin*

Size	Project Name	Rev
Custom	**A6VC**	2.0

Date: Tuesday, May 17, 2005 Sheet 3 of 58

Dothan FSB533			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A



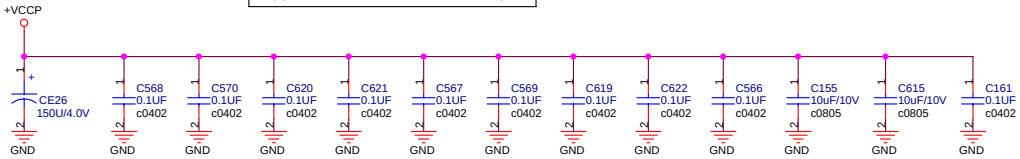


MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

Dothan FSB533			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)



+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

ASUS

Title : DOTHAN CPU(2)

<OrgName>

Engineer: Mark Lin

Size	Project Name	Rev
Custom	A6VC	2.0

Date: Tuesday, May 17, 2005 Sheet 4 of 58

Fan Speed Control

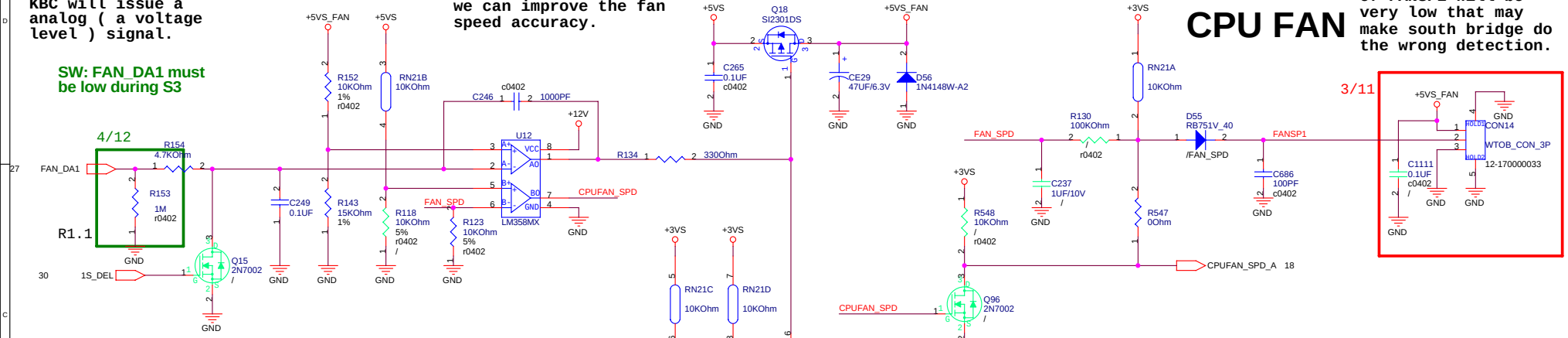
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

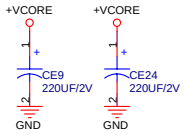
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

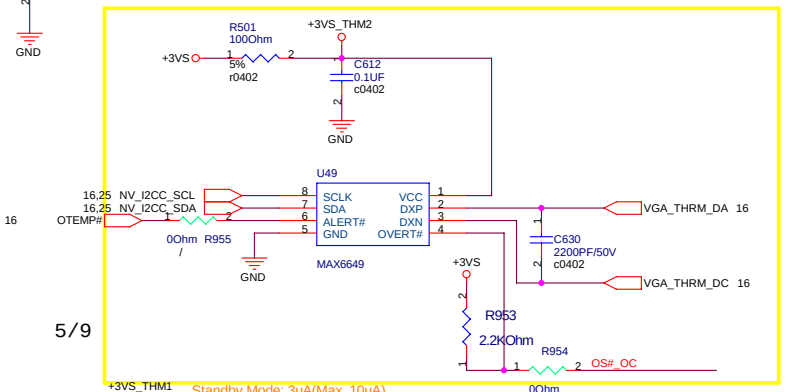
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN



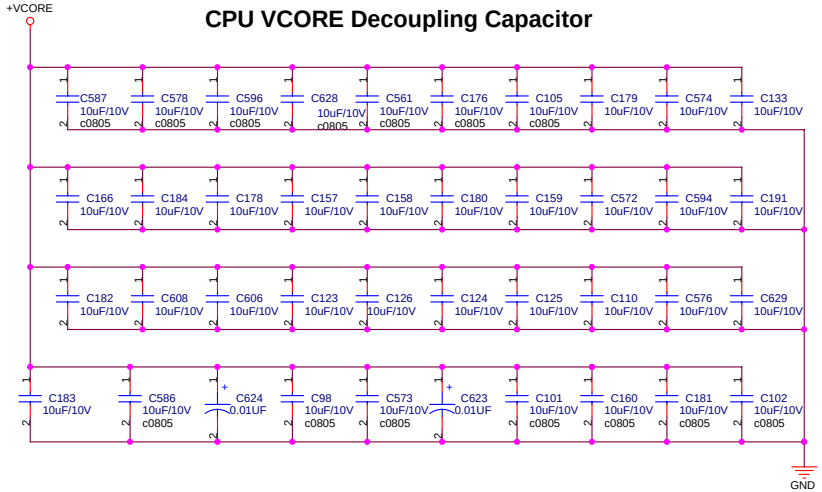
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)





Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

CPU VCORE Decoupling Capacitor



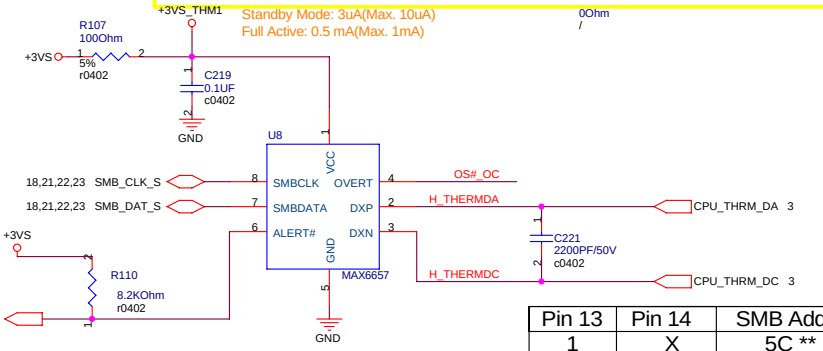
Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

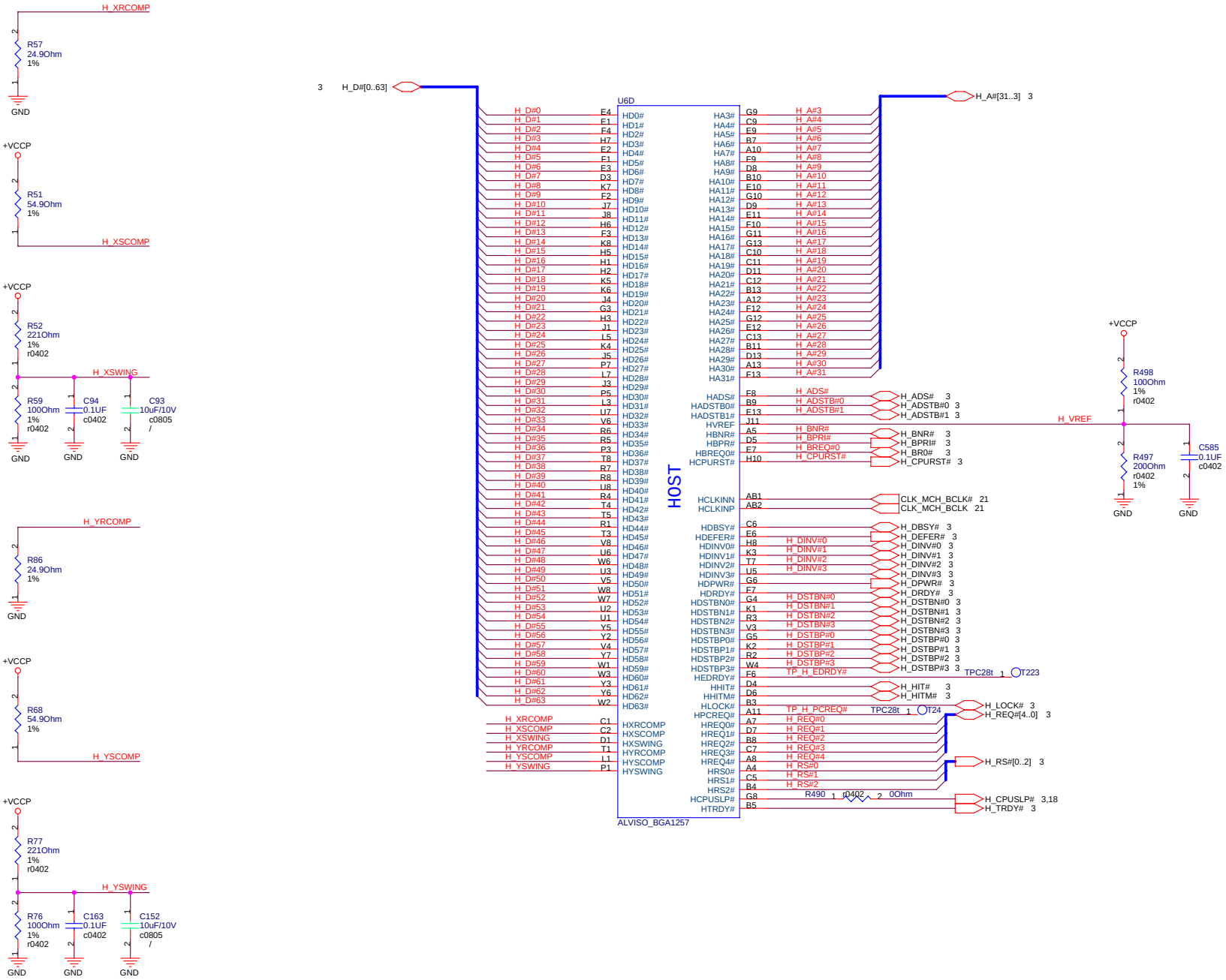
Four 200 uF are located in IMVP4

Close to Pin A18 & B18 of CPU

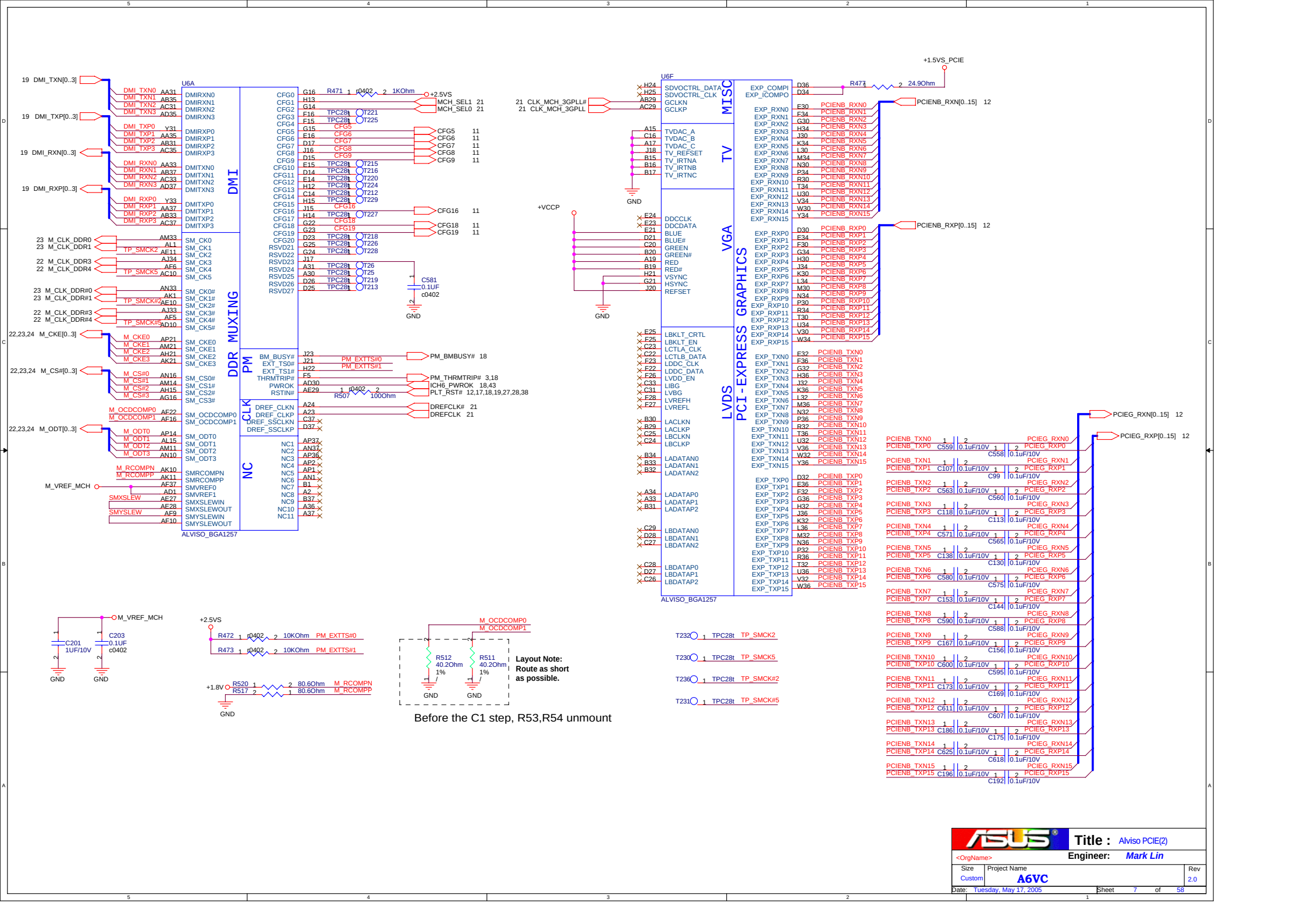


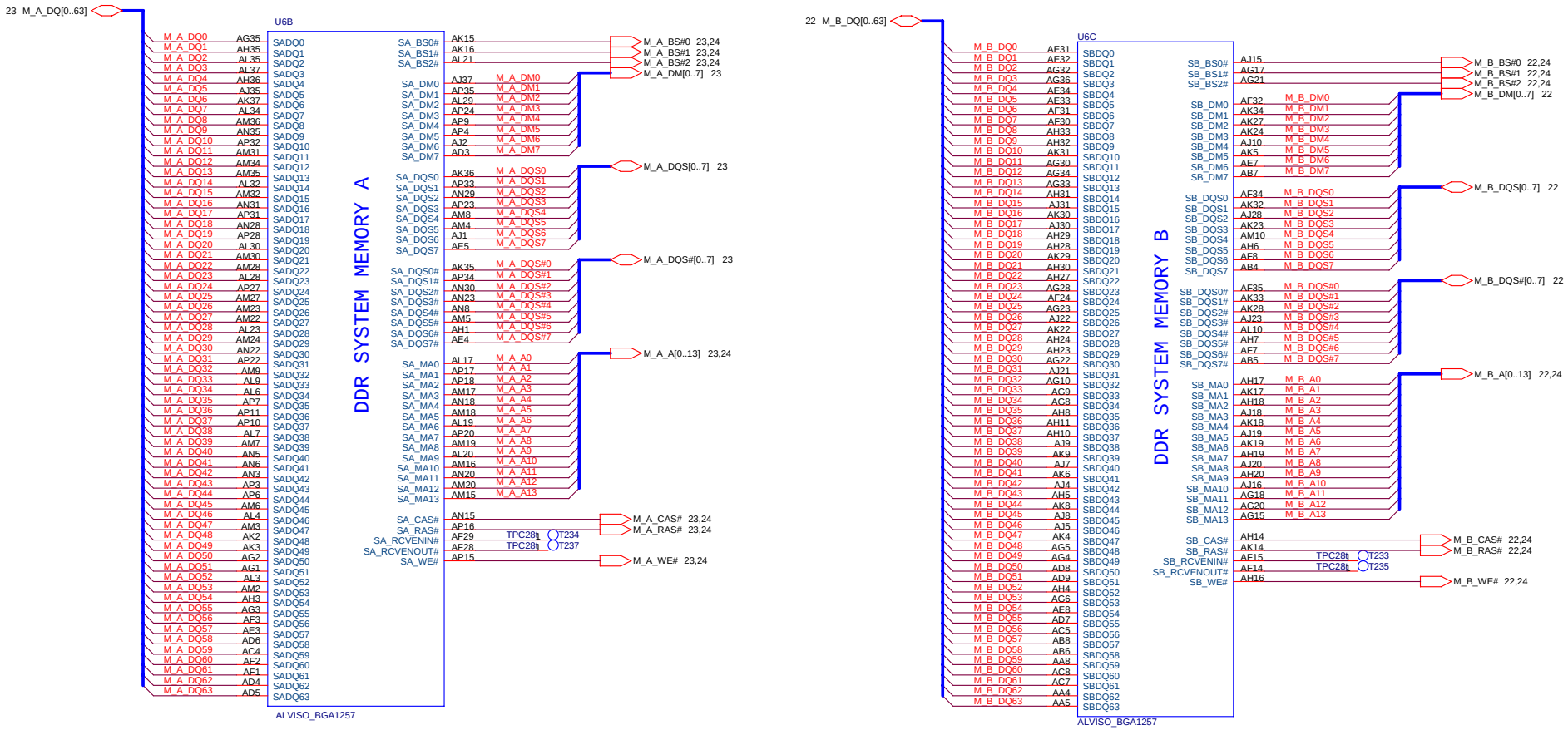
Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

ASUS	Title :	THERMAL SERSOR,FAN
<OrgName>	Engineer:	Mark Lin
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 5 of 58	

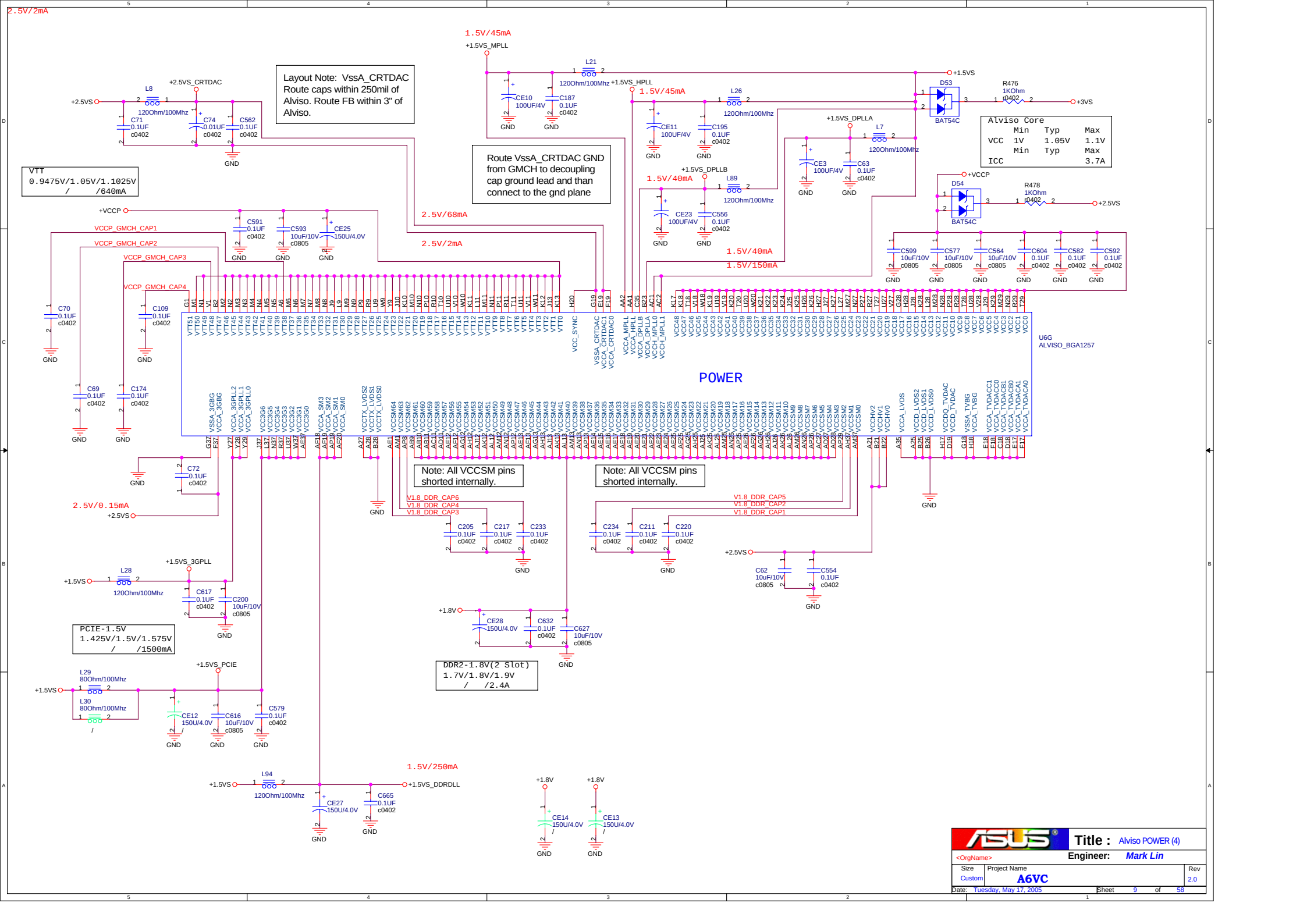


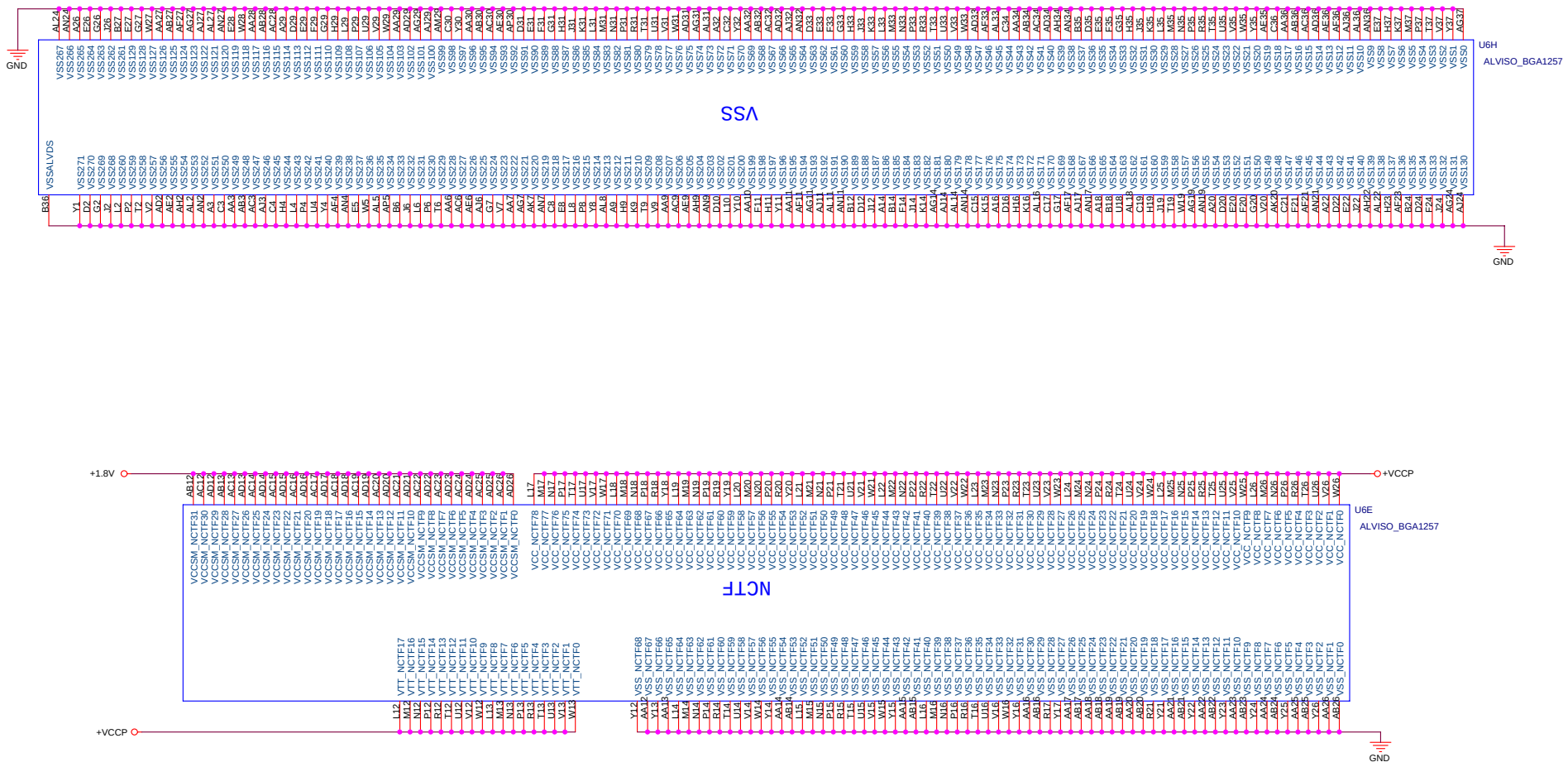
<OrgName>	Title : Alviso MCH(1)	
	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 6 of 58	


U6A
DMI
DDR MUXING
PM
CLK
NC
ALVISO_BGA1257
U6F
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO_BGA1257
+1.5VS_PCIE
+2.5VS
+1.8V
+VCCP
GND
MCH_SEL1 21
MCH_SEL0 21
CFG5 11
CFG6 11
CFG7 11
CFG8 11
CFG9 11
CFG16 11
CFG18 11
CFG19 11
PM_BMBUSY# 18
PM_THRMTRIP# 3,18
ICH6_PWROK 18,43
PLT_RST# 12,17,18,19,27,28,38
DREFCLK# 21
DREFCLK 21
PCIENB_RXN[0..15] 12
PCIENB_RXP[0..15] 12
PCIEG_RXN[0..15] 12
PCIEG_RXP[0..15] 12
Layout Note:
Route as short
as possible.
Before the C1 step, R53,R54 unmount
Title : Alviso PCIE(2)
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
Sheet 7 of 58



Title :	Alviso DDR2 SLOT (3)	
<OrgName>	Engineer:	Mark Lin
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 8 of 58	


2.5V/2mA
1.5V/45mA
+1.5VS_MPLL
Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
VTT
0.9475V/1.05V/1.1025V
/ /640mA
2.5V/68mA
2.5V/2mA
1.5V/40mA
1.5V/150mA
Alviso Core
Min Typ Max
VCC 1V 1.05V 1.1V
Min Typ Max
ICC 3.7A
POWER
U6G
ALVISO_BGA1257
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
2.5V/0.15mA
PCIE-1.5V
1.425V/1.5V/1.575V
/ /1500mA
DDR2-1.8V(2 Slot)
1.7V/1.8V/1.9V
/ /2.4A
1.5V/250mA
Title : Alviso POWER (4)
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
Sheet 9 of 58

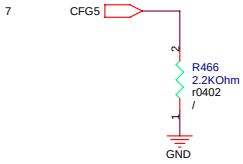


ASUS	Title :	Alviso GND (5)	
<OrgName>	Engineer:	Mark Lin	
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 10 of 58		

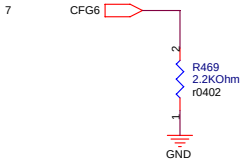
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present
(Default)

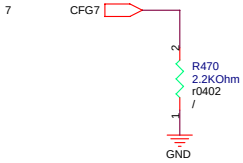
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)

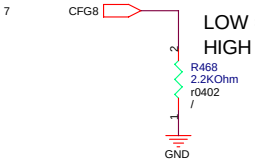


CFG7 : CPU STRAP



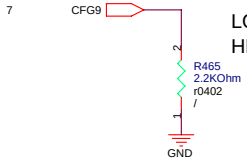
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG8 : PCI-X POWER Saving



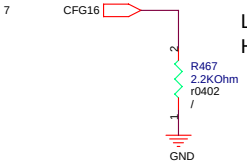
LOW = PCI-X POWER Saving
HIGH (Default)

CFG9 : PCIE GRAPHIC LANE



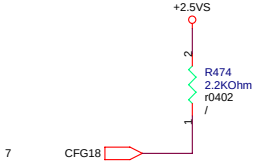
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

CFG16 : FSB DYNAMIC ODT



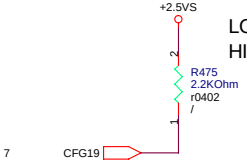
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG18 : VCC SELECT



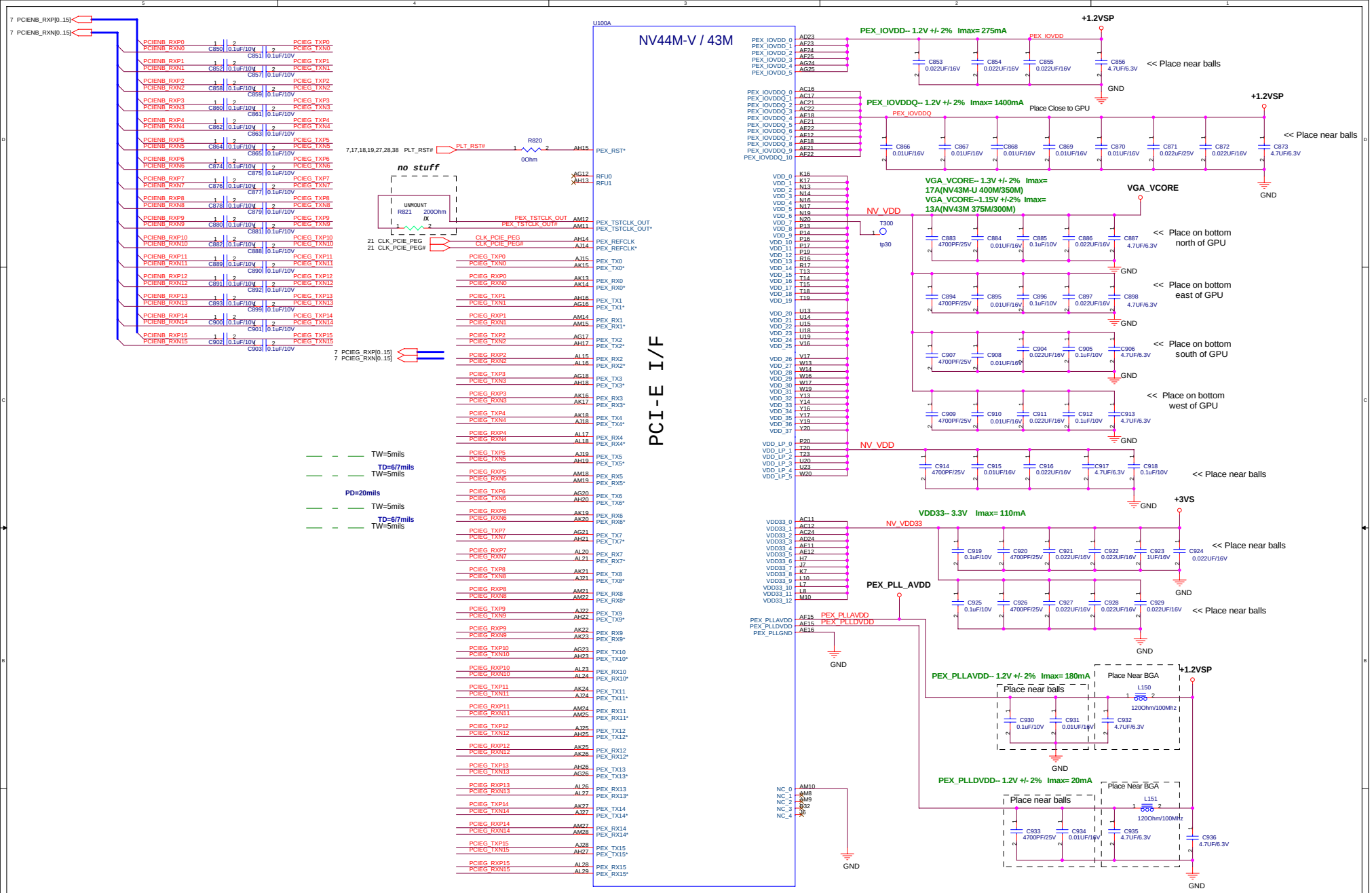
LOW = 1.05V (Default)
HIGH = 1.5V

CFG19 : VTT SELECT



LOW = 1.05V (Default)
HIGH = 1.2V

ASUS	Title : GMCH Strapping	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 11 of 58	


NV44M-V / 43M
PCI-E I/F
U100A
+1.2VSP
+3VS
VGA_VCORE
NV_VDD
PEX_PLL_AVDD
PEX_IOVDD-- 1.2V +/- 2% Imax= 275mA
PEX_IOVDDQ-- 1.2V +/- 2% Imax= 1400mA
VGA_VCORE-- 1.3V +/- 2% Imax= 17A(NV43M-U 400M/350M)
VGA_VCORE--1.15V +/-2% Imax= 13A(NV43M 375M/300M)
VDD33-- 3.3V Imax= 110mA
PEX_PLLAVDD-- 1.2V +/- 2% Imax= 180mA
PEX_PLLDVDD-- 1.2V +/- 2% Imax= 20mA
Place near balls
Place Close to GPU
Place Near BGA
<< Place near balls
<< Place on bottom north of GPU
<< Place on bottom east of GPU
<< Place on bottom south of GPU
<< Place on bottom west of GPU
no stuff
UNMOUNT
TW=5mils
TD=6/7mils
PD=20mils
GND
Title : NV44M-V MAIN
Engineer: Mark Lin
A6VC
Date: Tuesday, May 17, 2005
Sheet 12 of 58

FOR MEMORY STRAPS

U100E — NV44M-V / 43M

STRAP, MEMSTRAPSEL0, MEMSTRAPSEL1, MEMSTRAPSEL2, MEMSTRAPSEL3 (NC FOR NV44)

RFU6, RFU7, RFU8, RFU9, RFU10, RFU11, RFU12

ROMCS* — AA4 — NVROMCS — R822 10KOhm — +3VS

ROM_SO — AA6 — TPC28t T301

ROM_SI — W2 — TPC28t T302

ROM_SCLK — AA7 — TPC28t T303

I2CH_SCL — G3 — HDCPROMSCL — 10KOhm — R825 — +3VS

I2CH_SDA — H3 — HDCPROMSDA — 10KOhm — R826

BUFRST* — F3 — TPC28t T304

STEREO — T3 — TPC28t T305

SWAPRDY_A — M6 — SWAPRDY_A — R829 10KOhm — +3VS

TESTMEMCLK — A26 — TESTMEMCLK — R832 10KOhm

TESTMODE — H2 — TESTMODE — R833 10KOhm — GND

MCG0 — AL10

MCG1 — AG13 — GND

FOR MEMORY STRAPS

U100K — NV44M-V / 43M

+3VS — MIOA_VDDQ — M7, M8, R8, T8, U9 — MIOA_VDDQ_0..4

C937 0.1uF/10V

PLACE CAPS & RES CLOSE TO GPU PINS

T306 tp30 — MIOACAL_PD_VDDQ

T307 tp30 — MIOACAL_PU_GND

+3VS — T308 tp30 — MIOA_VREF

no stuff — R845 1KOhm

R846 1KOhm — C938 0.1UF — no stuff — GND

MIOAD0..MIOAD11 — P2, N2, N1, N3, M1, M3, P5, N6, N5, M4, L4, L5

MIOAD7 : TVMODE0

MIOAD10 : TVMODE1

MIOAD1 — R844 2KOhm — For System BIOS

STRAP= 0: System BIOS

STRAP= 1: Adapter BIOS

MIOA_HSYNC — R3

MIOA_VSYNC — R1

MIOA_DE — P1

MIOA_CTL3 — P3

MIOA_CLKOUT — R4

MIOA_CLKOUT* — P4

MIOA_CLKIN — M5 — MIOA_CLKIN — R847 — 10KOhm — GND

FOR CRYSTAL / PCIE_ID STRAPS

U100N — NV44M-V / 43M

+3VS — MIOB_VDDQ — AA8, AB7, AB8, AC6, AC7 — MIOB_VDDQ_0..4

C939 0.1uF/10V

PLACE CAPS CLOSE TO GPU PINS

T311 tp30 — MIOBCAL_PD_VDDQ

T312 tp30 — MIOBCAL_PU_GND

+3VS — T313 tp30 — MIOB_VREF

no stuff — R854 1KOhm

R857 1KOhm — C940 0.1UF — no stuff — GND

MIOBD0..MIOBD11 — AC3, AC1, AC2, AB2, AB1, AA1, AB3, AA3, AC5, AB5, AB4, AA5, W3

MIOBD10 : ROMTYPE0

RFU13, RFU14, RFU15, RFU16 — V1, Y5, W1

RFU17, RFU18, RFU19, RFU20 — W4, W5, V5, Y6

MIOB_VSYNC — AE3

MIOB_HSYNC — AF3

MIOB_DE — AD1

MIOB_CTL3 — AD3

MIOB_CLKOUT — AD4

MIOB_CLKOUT* — AD5

MIOB_CLKIN — AE4 — MIOB_CLKIN — R860 — 10KOhm — GND

MIOB_VSYNC : ROMTYPE1

VIPD2 — TPC28t T309 — R848 2KOhm

VIPD3

VIPD4

VIPD5

VIPD6 — TPC28t T310

VIPD7

R853 2KOhm — GND

MIOBD8

MIOBD9

MIOBD11

MEM TYPE STRAP

NV44M memory strap setting:

01 (0001) SAMSUNG 8MX32X2 64MB (two VRAM) --> 1.8V

01 (0001) HYNIX 8MX32X2 64MB (two VRAM) --> 1.8V

04 (0100) SAMSUNG 4MX32X2 32MB (two VRAM) --> 1.8V

09 (1001) HYNIX 8MX32X1 32MB (one VRAM) --> 1.8V

0C (1100) SAMSUNG 4MX32X1 16MB (one VRAM) --> 1.8V

MIOBD0 : RAMCFG0 MIOBD1 : RAMCFG1

MIOBD8 : RAMCFG2 MIOBD9 : RAMCFG3

MIOAD0 — R823 2KOhm — no stuff UNMOUNT — R827 2KOhm — GND

MIOAD6 — R824 2KOhm — R828 2KOhm — no stuff UNMOUNT — GND

MIOAD8 — R836 2KOhm — no stuff UNMOUNT — R838 2KOhm — GND

MIOAD9 — R837 2KOhm — no stuff UNMOUNT — R839 2KOhm — GND

MIOBD0 — R830 2KOhm — no stuff UNMOUNT — R835 2KOhm — GND

MIOBD1 — R831 2KOhm — no stuff UNMOUNT — R834 2KOhm — GND

MIOBD8 — R840 2KOhm — no stuff UNMOUNT — R842 2KOhm — GND UNMOUNT

MIOBD9 — R841 2KOhm — no stuff UNMOUNT — R843 2KOhm — GND

(PCI_DEVICE_ID)

MIOBD4 : PCI_DEVID0 MIOBD3 : PCI_DEVID2

MIOBD5 : PCI_DEVID1 MIOBD11 : PCI_DEVID3

NV43M - ID 0X0148

NV44M - ID 0X0168

NV44M-V- ID 0X0167

VIPD4 — R849 2KOhm — R852 2KOhm — no stuff UNMOUNT — GND

VIPD3 — R850 2KOhm — R851 2KOhm — no stuff UNMOUNT — GND

VIPD5 — R855 2KOhm — R859 2KOhm — no stuff UNMOUNT — GND UNMOUNT

MIOBD11 — R856 2KOhm — no stuff UNMOUNT — R858 2KOhm — GND

(for panel user ID)

MIOAD2 — R861 2KOhm

MIOAD3 — R862 2KOhm

MIOAD4 — R863 2KOhm

MIOAD5 — R864 2KOhm

ASUS

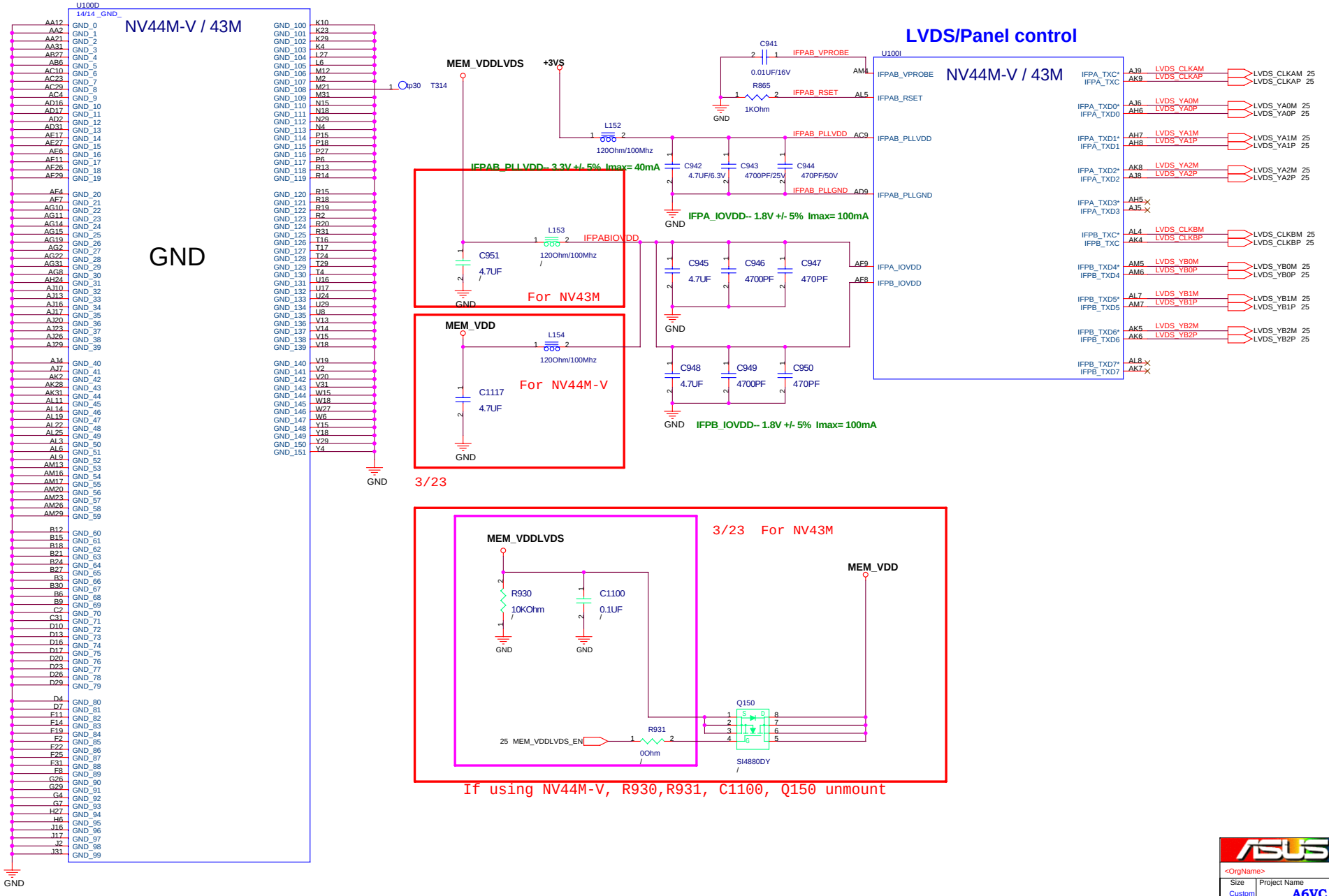
Title : NV44M-V Strapping

<OrgName>

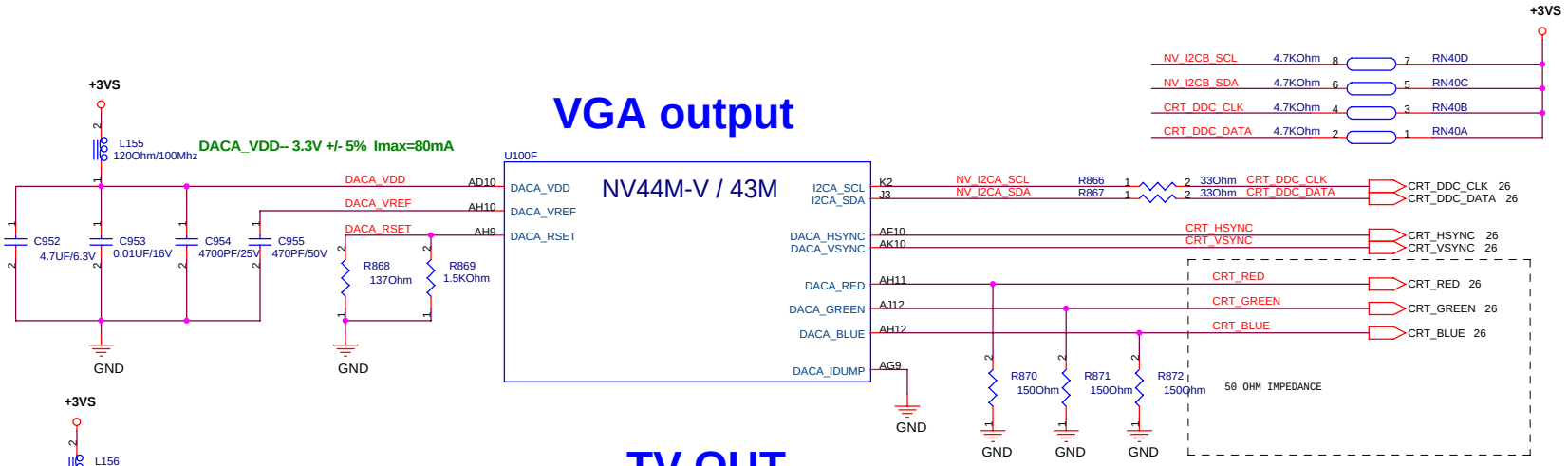
Engineer: Mark Lin

Size: Custom | Project Name: A6VC | Rev: 2.0

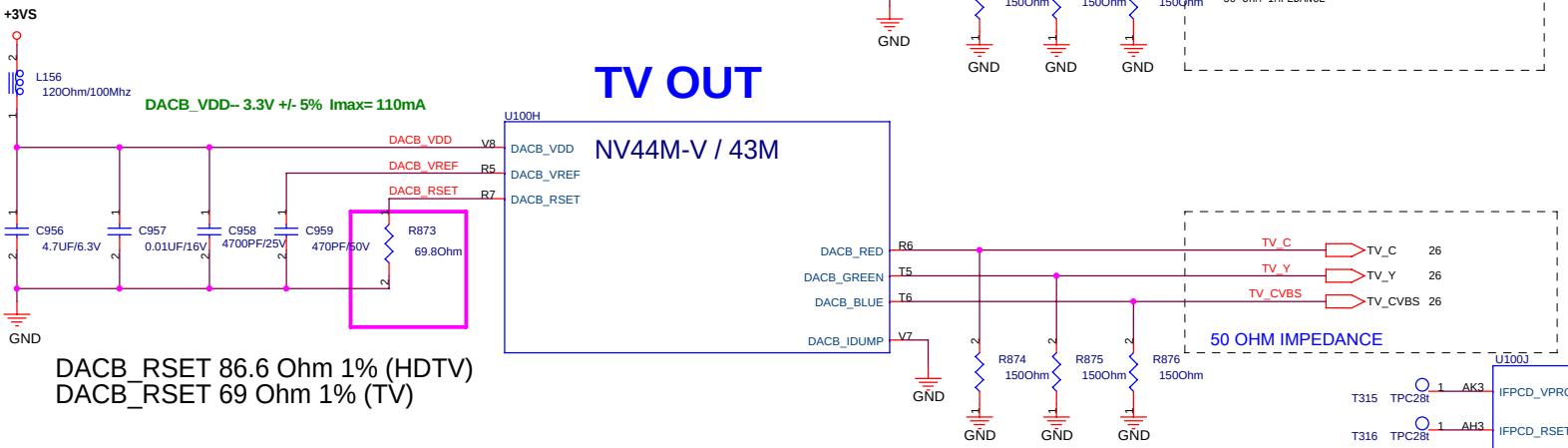
Date: Tuesday, May 17, 2005 | Sheet 13 of 58


LVDS/Panel control
U100D
14/14 _GND_
NV44M-V / 43M
GND
U100I
NV44M-V / 43M
MEM_VDDLVDS
+3VS
MEM_VDD
IFPAB_VPROBE
IFPAB_RSET
IFPAB_PLLVDD
IFPAB_PLLGND
IFPA_IOVDD
IFPB_IOVDD
IFPABIOVDD
IFPA_TXC*
IFPA_TXC
IFPA_TXD0*
IFPA_TXD0
IFPA_TXD1*
IFPA_TXD1
IFPA_TXD2*
IFPA_TXD2
IFPA_TXD3*
IFPA_TXD3
IFPB_TXC*
IFPB_TXC
IFPB_TXD4*
IFPB_TXD4
IFPB_TXD5*
IFPB_TXD5
IFPB_TXD6*
IFPB_TXD6
IFPB_TXD7*
IFPB_TXD7
LVDS_CLKAM
LVDS_CLKAP
LVDS_YA0M
LVDS_YA0P
LVDS_YA1M
LVDS_YA1P
LVDS_YA2M
LVDS_YA2P
LVDS_CLKBM
LVDS_CLKBP
LVDS_YB0M
LVDS_YB0P
LVDS_YB1M
LVDS_YB1P
LVDS_YB2M
LVDS_YB2P
C941
0.01UF/16V
R865
1KOhm
L152
120Ohm/100Mhz
C942
4.7UF/6.3V
C943
4700PF/25V
C944
470PF/50V
IFPAB_PLLVDD -- 3.3V +/- 5% Imax= 40mA
IFPA_IOVDD -- 1.8V +/- 5% Imax= 100mA
L153
120Ohm/100Mhz
C951
4.7UF
For NV43M
L154
120Ohm/100Mhz
C1117
4.7UF
For NV44M-V
C945
4.7UF
C946
4700PF
C947
470PF
C948
4.7UF
C949
4700PF
C950
470PF
IFPB_IOVDD -- 1.8V +/- 5% Imax= 100mA
3/23
3/23 For NV43M
R930
10KOhm
C1100
0.1UF
R931
0Ohm
Q150
SI4880DY
25 MEM_VDDLVDS_EN
If using NV44M-V, R930,R931, C1100, Q150 unmount
Title : NV44M-V LVDS
Engineer: Mark Lin
<OrgName>
Size
Custom
Project Name
A6VC
Rev
2.0
Date: Tuesday, May 17, 2005
Sheet 14 of 58

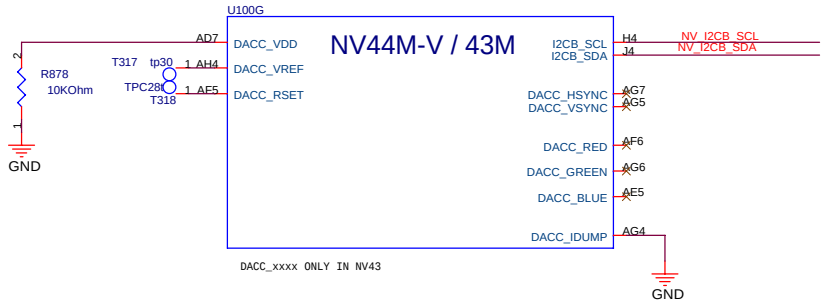
VGA output

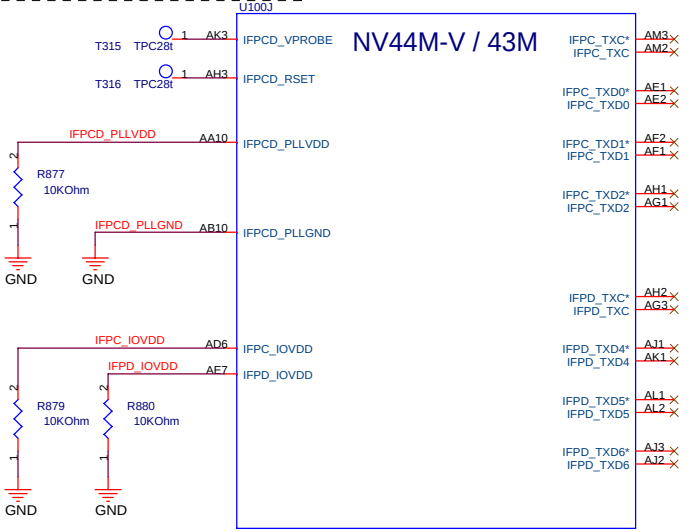


TV OUT



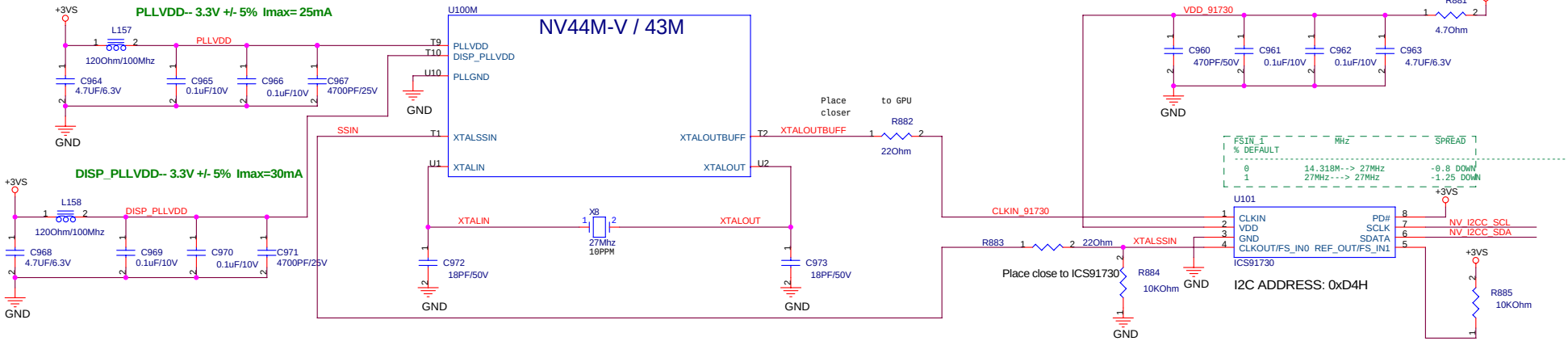
DACB_RSET 86.6 Ohm 1% (HDTV)
DACB_RSET 69 Ohm 1% (TV)





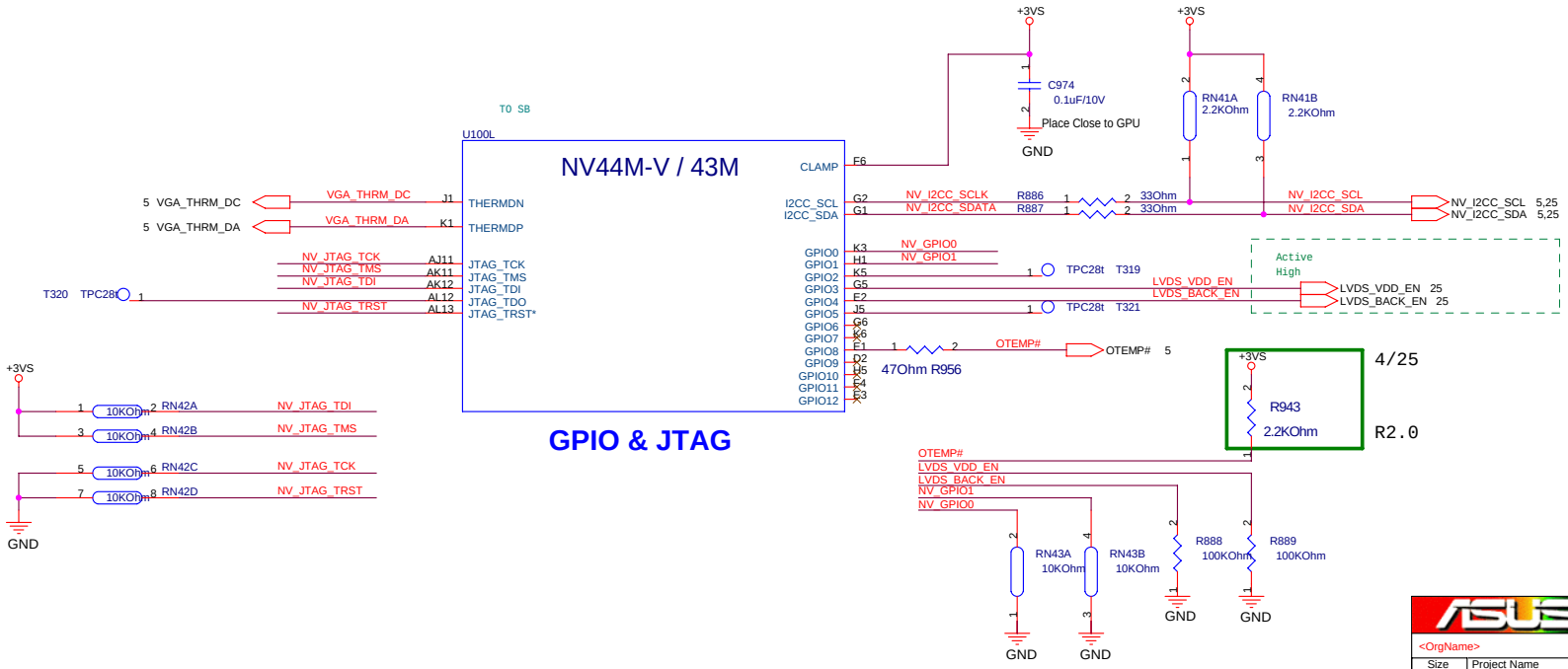
ASUS	Title : NV44M-V VGA/TV out		
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 15 of 58		

XTAL/PLLVDD



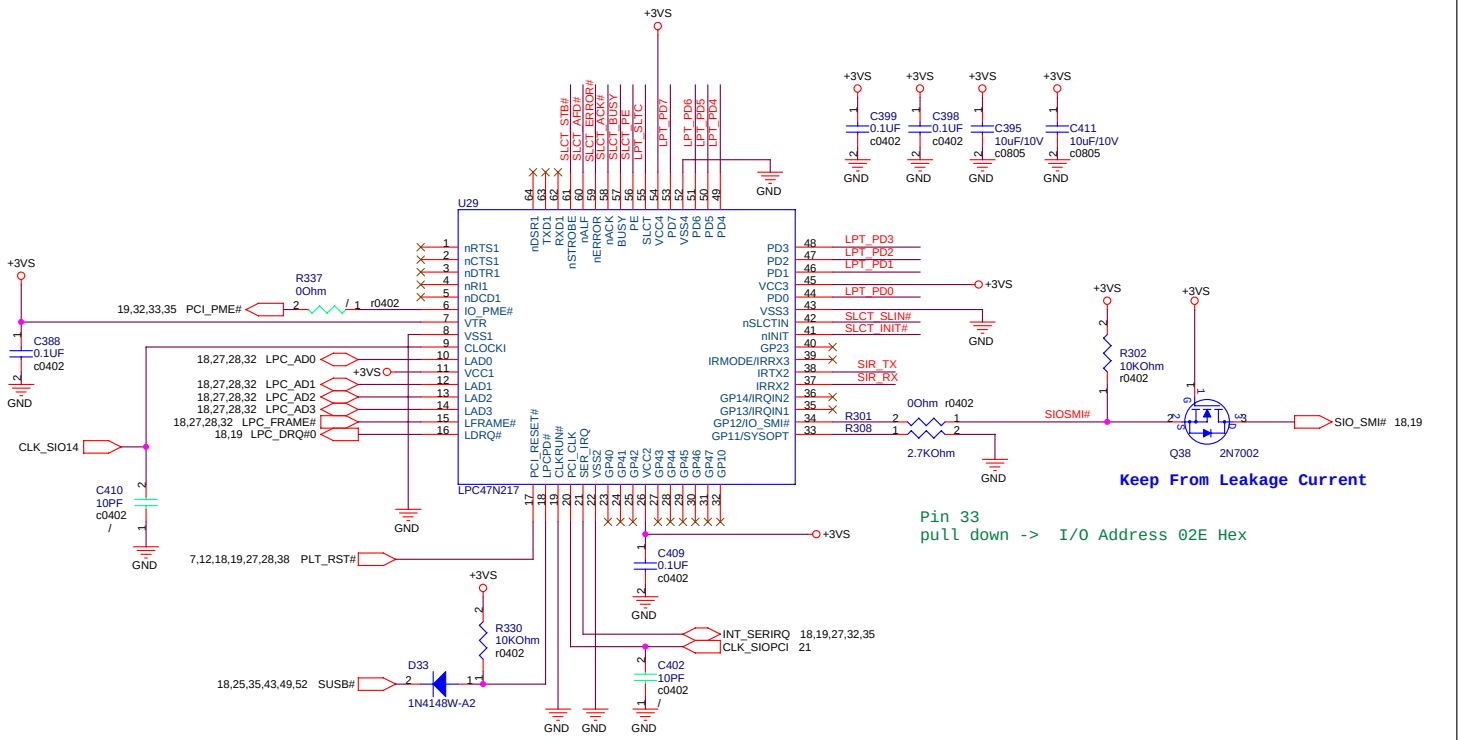
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOT PLUG
1	IN	N/A	2ND DVI HOT PLUG
2	OUT	HIGH	BACKLIGHT BRIGHTNESS
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID0
6	OUT	HIGH	NVVDD VID1
7	OUT	HIGH	FBVDD VID0
8 SHUTDOWN	IN	LOW	THERMAL
9	OUT	LOW	FAN PWM

GPIO & JTAG



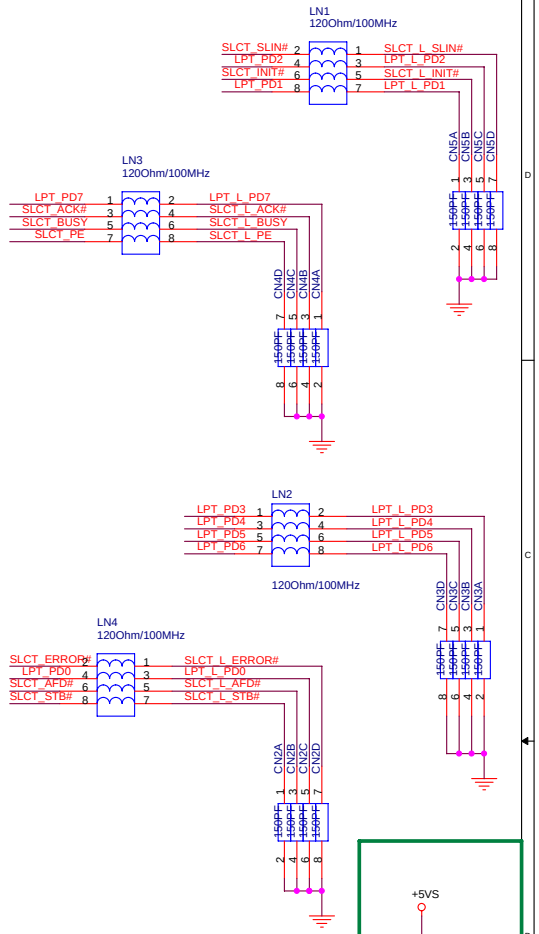
Title :	NV44M SSP GPIO/THERMAL	
<OrgName>	Engineer:	Mark Lin
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 16 of 58	

Super I/O



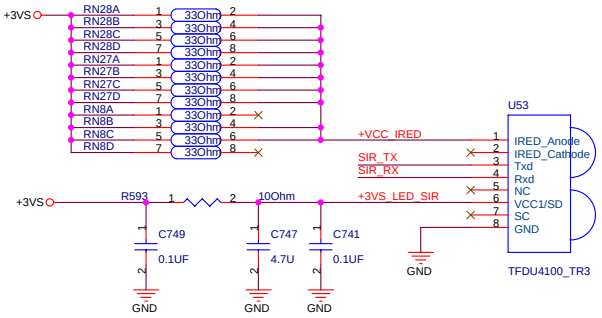
Keep From Leakage Current

Pin 33
pull down -> I/O Address 02E Hex

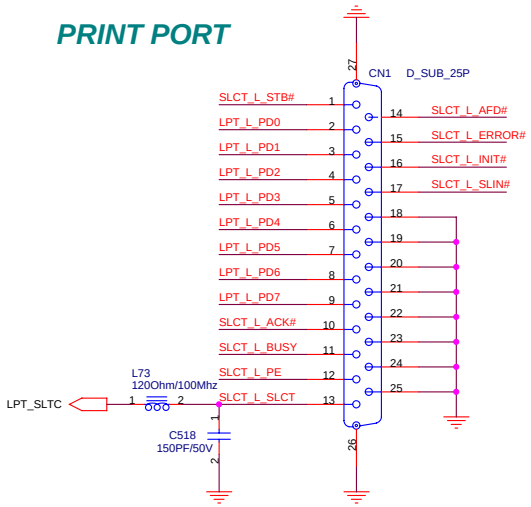


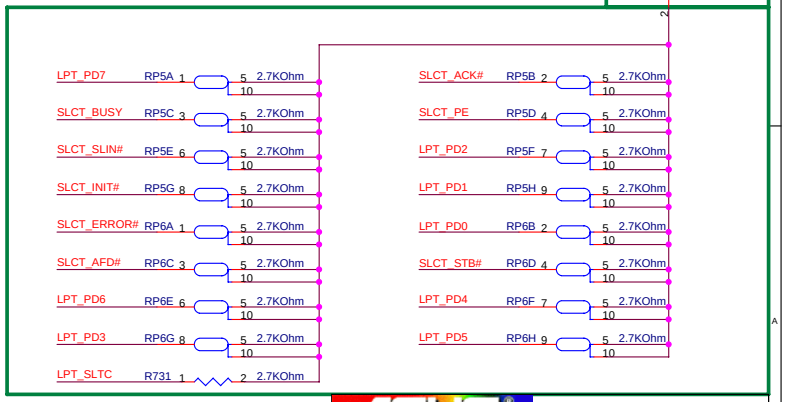
4/15

SIR



PRINT PORT





+5VS
D77 SS0540

ASUS

Title : SIO ITE8705F

<OrgName>

Engineer: *Mark Lin*

Size	Project Name	Rev
Custom	**A6VC**	2.0

Date: Tuesday, May 17, 2005 Sheet 17 of 58

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

PLACE WITHIN 500mils of ICH6 ball

INTERNAL PULL-UP
PULL-DOWN :
RESERVED

INTERNAL PULL-DOWN
PULL-UP : NO REBOOT

TP_3 INTERNAL PULL-UP
PULL-DOWN : PCI
Express Port chain test

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2" from the series resistor

RTC CMOS CLEAR

DELAY 18~25ms

U24C

ICH6_M

U24D

ICH6_M

Q48 2N7002

Q43 2N7002

Title : ICH6M - SATA, LPC, IDE (1)			
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 18 of 58		

PLT_RST#
ICH6,Alviso/M26/KBC/FWH/HDD

U24A

ICH6_M

U24B

ICH6_M

PLACE within 500 mils of ICH.
5.5mil/8mil

PLACE within 500 mils of ICH.

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK , AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , SDD[7] , PDDREQ , SDDREQ , SPKR , USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
EE_DIN , EE_DOUT , GNT[B:A]# , GNT[5]# , GPIO[17:16] , LAD[3:0]# , LDRQ[1:0] , LAN_RXD[2:0] , PME# , PWRBTN#

PCB_VID 0 1 2
MB V1.0 0 0 0

PCB_VID3 : PROJECT CODE

INTERNAL PULL-UP
PULL-DOWN : Boot BIOS destination select

INTERNAL PULL-UP
PULL-DOWN
:TOP-BLOCK SWAP

3/17

Title :	ICH6M - USB, PCI/E, PMIO (2)
<OrgName>	Engineer: Mark Lin
Size: Custom	Project Name: A6VC
Rev: 2.0	
Date: Tuesday, May 17, 2005	Sheet 19 of 58

Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge

Place BOTH within 100mils of ICH near pin D27

Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1

V_CPU_IO 1.05v/0.014A

Place 0.1uF within 100mils of ICH near pin AG23

Vcc3_3 3.3V/0.204A

VccSus3_3 3.3V/0.023A

Place 0.1uFx1 near V7

Place BOTH within 100mils of ICH near pin A17

Place 0.1uFx1 near G10

Place 0.1uFx1 near A8

Place 0.1uFx1 near AB18

Vcc2_5 2.5V/0.015A

Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27

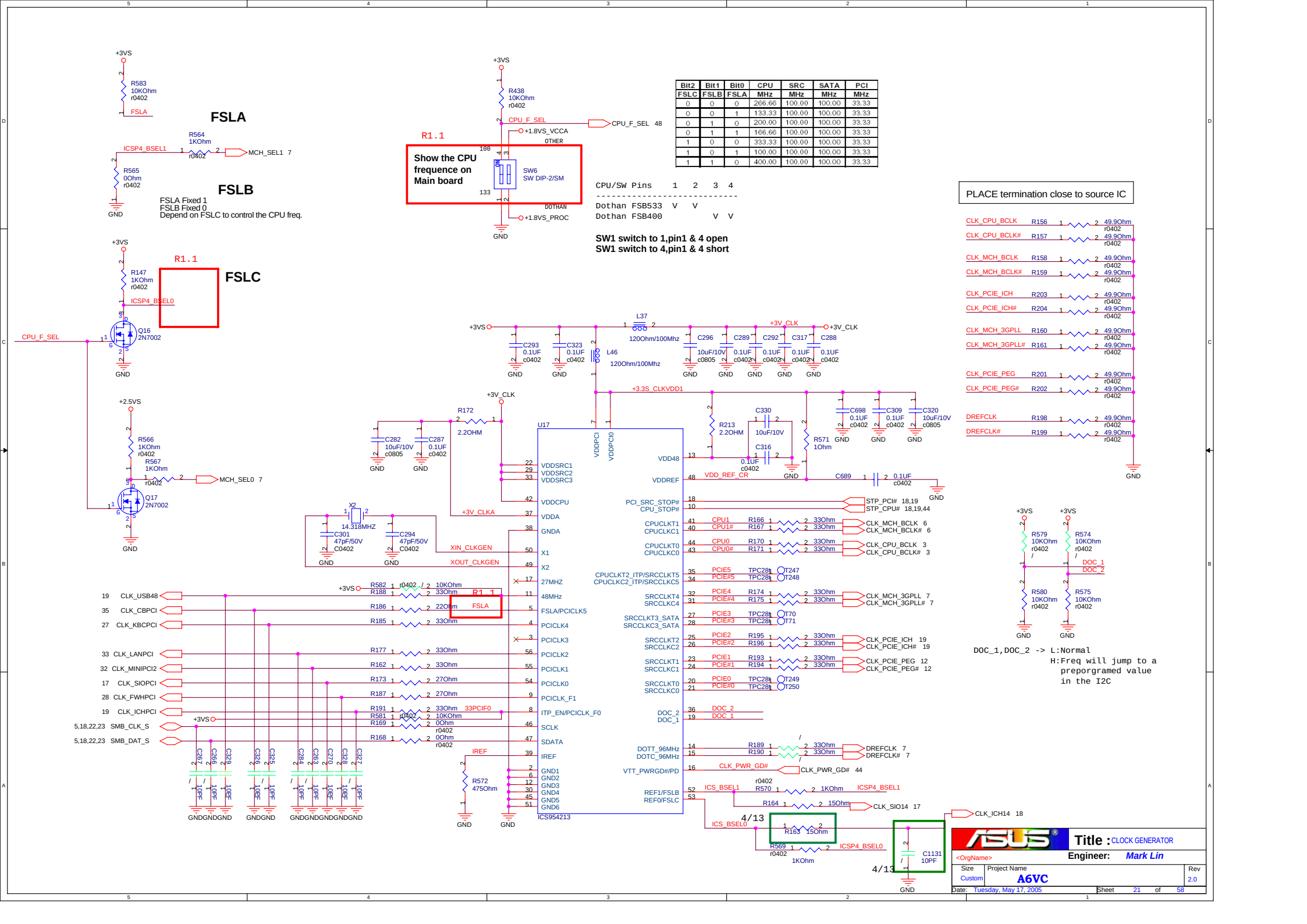
VCC1_5_B 1.425V/1.5V/1.575V / /578mA

VCC1_5_A 1.425V/1.5V/1.575V / /1.77A

Place within 100mils of ICH near pin AG5

Place within 100mils of ICH near pin AG9

Title : ICH6M - PWR, GND(3)			
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 20 of 58		



Bit2	Bit1	Bit0	CPU	SRC	SATA	PCI
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	266.66	100.00	100.00	33.33
0	0	1	133.33	100.00	100.00	33.33
0	1	0	200.00	100.00	100.00	33.33
0	1	1	166.66	100.00	100.00	33.33
1	0	0	333.33	100.00	100.00	33.33
1	0	1	100.00	100.00	100.00	33.33
1	1	0	400.00	100.00	100.00	33.33

NO STUFF *

M_CLK_DDR3

C303
10PF PLACE NEAR SO-DIMM_0
c0402
/

M_CLK_DDR#3

M_CLK_DDR4

C302
10PF PLACE NEAR SO-DIMM_0
c0402
/

M_CLK_DDR#4

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8,24 M_B_A[0..13]

M_B_DQ[0..63] 8

CON15B

M_B_A0 B102 B:A0
M_B_A1 B101 B:A1
M_B_A2 B100 B:A2
M_B_A3 B99 B:A3
M_B_A4 B98 B:A4
M_B_A5 B97 B:A5
M_B_A6 B94 B:A6
M_B_A7 B92 B:A7
M_B_A8 B93 B:A8
M_B_A9 B91 B:A9
M_B_A10 B105 B:A10/AP
M_B_A11 B90 B:A11
M_B_A12 B89 B:A12
M_B_A13 B116 B:A13
B86 B:A14
B84 B:A15
B85 B:A16_BA2

8,24 M_B_BS#2 B107 B:BA0
8,24 M_B_BS#0 B106 B:BA1
8,24 M_B_BS#1 B110 B:S0#
7,24 M_CS#2 B115 B:S1#
7,24 M_CS#3 B30 B:CK0
7 M_CLK_DDR3 B32 B:CK0#
7 M_CLK_DDR#3 B164 B:CK1
7 M_CLK_DDR4 B166 B:CK1#
7 M_CLK_DDR#4 B79 B:CKE0
7,24 M_CKE2 B80 B:CKE1
7,24 M_CKE3 B113 B:CBS#
8,24 M_B_CAS# B108 B:RAS#
8,24 M_B_RAS# B109 B:WE#
8,24 M_B_WE# B198 B:SA0
B200 B:SA1
5,18,21,23 SMB_CLK_S B197 B:SCL
5,18,21,23 SMB_DAT_S B195 B:SDA

R181 10KOhm r0402
R180 10KOhm r0402
+3VS
GND

7,24 M_ODT2 B114 B:ODT0
7,24 M_ODT3 B119 B:ODT1
8 M_B_DM[0..7]

M_B_DM0 B10 B:DM0
M_B_DM1 B26 B:DM1
M_B_DM2 B52 B:DM2
M_B_DM3 B67 B:DM3
M_B_DM4 B130 B:DM4
M_B_DM5 B147 B:DM5
M_B_DM6 B170 B:DM6
M_B_DM7 B185 B:DM7

8 M_B_DQS[0..7]

M_B_DQS0 B13 B:DQS0
M_B_DQS1 B31 B:DQS1
M_B_DQS2 B51 B:DQS2
M_B_DQS3 B70 B:DQS3
M_B_DQS4 B131 B:DQS4
M_B_DQS5 B148 B:DQS5
M_B_DQS6 B169 B:DQS6
M_B_DQS7 B188 B:DQS7
M_B_DQS#0 B11 B:DQS0#
M_B_DQS#1 B29 B:DQS1#
M_B_DQS#2 B49 B:DQS2#
M_B_DQS#3 B68 B:DQS3#
M_B_DQS#4 B129 B:DQS4#
M_B_DQS#5 B146 B:DQS5#
M_B_DQS#6 B167 B:DQS6#
M_B_DQS#7 B186 B:DQS7#

8 M_B_DQS#[0..7]

B:DQ0 B5 M_B_DQ1
B:DQ1 B7 M_B_DQ0
B:DQ2 B17 M_B_DQ2
B:DQ3 B19 M_B_DQ6
B:DQ4 B4 M_B_DQ5
B:DQ5 B6 M_B_DQ4
B:DQ6 B14 M_B_DQ7
B:DQ7 B16 M_B_DQ3
B:DQ8 B23 M_B_DQ9
B:DQ9 B25 M_B_DQ13
B:DQ10 B35 M_B_DQ11
B:DQ11 B37 M_B_DQ10
B:DQ12 B20 M_B_DQ12
B:DQ13 B22 M_B_DQ8
B:DQ14 B36 M_B_DQ15
B:DQ15 B38 M_B_DQ14
B:DQ16 B43 M_B_DQ16
B:DQ17 B45 M_B_DQ17
B:DQ18 B55 M_B_DQ19
B:DQ19 B57 M_B_DQ18
B:DQ20 B44 M_B_DQ21
B:DQ21 B46 M_B_DQ20
B:DQ22 B56 M_B_DQ22
B:DQ23 B58 M_B_DQ23
B:DQ24 B61 M_B_DQ29
B:DQ25 B63 M_B_DQ24
B:DQ26 B73 M_B_DQ30
B:DQ27 B75 M_B_DQ26
B:DQ28 B62 M_B_DQ28
B:DQ29 B64 M_B_DQ25
B:DQ30 B74 M_B_DQ27
B:DQ31 B76 M_B_DQ31
B:DQ32 B123 M_B_DQ32
B:DQ33 B125 M_B_DQ36
B:DQ34 B135 M_B_DQ38
B:DQ35 B137 M_B_DQ35
B:DQ36 B124 M_B_DQ33
B:DQ37 B126 M_B_DQ37
B:DQ38 B134 M_B_DQ39
B:DQ39 B136 M_B_DQ34
B:DQ40 B141 M_B_DQ44
B:DQ41 B143 M_B_DQ40
B:DQ42 B151 M_B_DQ47
B:DQ43 B153 M_B_DQ43
B:DQ44 B140 M_B_DQ45
B:DQ45 B142 M_B_DQ41
B:DQ46 B152 M_B_DQ46
B:DQ47 B154 M_B_DQ42
B:DQ48 B157 M_B_DQ53
B:DQ49 B159 M_B_DQ49
B:DQ50 B173 M_B_DQ50
B:DQ51 B175 M_B_DQ51
B:DQ52 B158 M_B_DQ48
B:DQ53 B160 M_B_DQ52
B:DQ54 B174 M_B_DQ54
B:DQ55 B176 M_B_DQ55
B:DQ56 B179 M_B_DQ57
B:DQ57 B181 M_B_DQ59
B:DQ58 B189 M_B_DQ62
B:DQ59 B191 M_B_DQ56
B:DQ60 B180 M_B_DQ61
B:DQ61 B182 M_B_DQ60
B:DQ62 B192 M_B_DQ58
B:DQ63 B194 M_B_DQ63

Layout Note: Place these High-Freq decoupling Caps near the GMCH

+1.8V
C637 0.1UF c0402
C635 0.1UF c0402
C633 0.1UF c0402
C636 0.1UF c0402
GND

Layout Note: Place these resistors near the GMCH

+1.8V
C638 2.2uF/6.3V
C631 2.2uF/6.3V
C667 2.2uF/6.3V
C644 2.2uF/6.3V
C670 2.2uF/6.3V
GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V
C354 0.1UF c0402
C355 0.1UF c0402
C352 0.1UF c0402
C353 0.1UF c0402
GND

B:VDD2 B111
B:VDD3 B117
B:VDD5 B95
B:VDD7 B81
B:VDD9 B87
B:VDD10 B103

B:VSS1 B47
B:VSS2 B133
B:VSS3 B183
B:VSS4 B77
B:VSS9 B71
B:VSS11 B121
B:VSS14 B193
B:VSS18 B41
B:VSS19 B53
B:VSS22 B59
B:VSS23 B65

B:VSS26 B127
B:VSS27 B139
B:VSS29 B145
B:VSS30 B165
B:VSS31 B171
B:VSS33 B177
B:VSS34 B187
B:VSS37 B9
B:VSS38 B21
B:VSS39 B33
B:VSS40 B155
B:VSS47 B3
B:VSS48 B15
B:VSS49 B27
B:VSS50 B39
B:VSS51 B149
B:VSS52 B161

+3VS
C332 0.1UF c0402
C331 0.1UF c0402
GND

B:VDDSPD B199

M_VREF_DIMM0
B:VREF B1
VREF -> 10/10 mils
C340 2.2uF/6.3V
C333 0.1UF c0402
GND

B:NC1 B83
B:NC2 B120
B:NC3 B50
B:NC4 B69
B:NCTEST B163

DDR_DIMM_331P

Layout Note: Place these Caps near SO DIMM 0

<OrgName>	Title : DDR2 SO-DIMM_0		
	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 22 of 58		

NO STUFF *

M_CLK_DDR0

C697 10PF PLACE NEAR SO-DIMM_1 c0402 / M_CLK_DDR#0

M_CLK_DDR1

C696 10PF PLACE NEAR SO-DIMM_1 c0402 / M_CLK_DDR#1

4/13

8,24 M_A_A[0..13]

8,24 M_A_BS#2

8,24 M_A_BS#0
8,24 M_A_BS#1
7,24 M_CS#0
7,24 M_CS#1
7 M_CLK_DDR0
7 M_CLK_DDR#0
7 M_CLK_DDR1
7 M_CLK_DDR#1
7,24 M_CKE0
7,24 M_CKE1
8,24 M_A_CAS#
8,24 M_A_RAS#
8,24 M_A_WE#

R577 10KOhm r0402
R576 10KOhm r0402
GND GND

5,18,21,22 SMB_CLK_S
5,18,21,22 SMB_DAT_S

7,24 M_ODT0
7,24 M_ODT1
8 M_A_DM[0..7]

8 M_A_DQS[0..7]

8 M_A_DQS#[0..7]

CON15A

M_A_A0 A102 A:A0
M_A_A1 A101 A:A1
M_A_A2 A100 A:A2
M_A_A3 A99 A:A3
M_A_A4 A98 A:A4
M_A_A5 A97 A:A5
M_A_A6 A94 A:A6
M_A_A7 A92 A:A7
M_A_A8 A93 A:A8
M_A_A9 A91 A:A9
M_A_A10 A105 A:A10/AP
M_A_A11 A90 A:A11
M_A_A12 A89 A:A12
M_A_A13 A116 A:A13
A86 A:A14
A84 A:A15
A85 A:A16_BA2

A107 A:BA0
A106 A:BA1
A110 A:S0#
A115 A:S1#
A30 A:CK0
A32 A:CK0#
A164 A:CK1
A166 A:CK1#
A79 A:CKE0
A80 A:CKE1
A113 A:CAS#
A108 A:RAS#
A109 A:WE#
A198 A:SA0
A200 A:SA1
A197 A:SCL
A195 A:SDA

A114 A:ODT0
A119 A:ODT1

M_A_DM0 A10 A:DM0
M_A_DM1 A26 A:DM1
M_A_DM2 A52 A:DM2
M_A_DM3 A67 A:DM3
M_A_DM4 A130 A:DM4
M_A_DM5 A147 A:DM5
M_A_DM6 A170 A:DM6
M_A_DM7 A185 A:DM7

M_A_DQS0 A13 A:DQS0
M_A_DQS1 A31 A:DQS1
M_A_DQS2 A51 A:DQS2
M_A_DQS3 A70 A:DQS3
M_A_DQS4 A131 A:DQS4
M_A_DQS5 A148 A:DQS5
M_A_DQS6 A169 A:DQS6
M_A_DQS7 A188 A:DQS7
M_A_DQS#0 A11 A:DQS0#
M_A_DQS#1 A29 A:DQS1#
M_A_DQS#2 A49 A:DQS2#
M_A_DQS#3 A68 A:DQS3#
M_A_DQS#4 A129 A:DQS4#
M_A_DQS#5 A146 A:DQS5#
M_A_DQS#6 A167 A:DQS6#
M_A_DQS#7 A186 A:DQS7#

A:DQ0 A5 M_A_DQ0
A:DQ1 A7 M_A_DQ1
A:DQ2 A17 M_A_DQ7
A:DQ3 A19 M_A_DQ2
A:DQ4 A4 M_A_DQ5
A:DQ5 A6 M_A_DQ4
A:DQ6 A14 M_A_DQ3
A:DQ7 A16 M_A_DQ6
A:DQ8 A23 M_A_DQ12
A:DQ9 A25 M_A_DQ13
A:DQ10 A35 M_A_DQ11
A:DQ11 A37 M_A_DQ14
A:DQ12 A20 M_A_DQ9
A:DQ13 A22 M_A_DQ8
A:DQ14 A36 M_A_DQ10
A:DQ15 A38 M_A_DQ15
A:DQ16 A43 M_A_DQ20
A:DQ17 A45 M_A_DQ21
A:DQ18 A55 M_A_DQ23
A:DQ19 A57 M_A_DQ22
A:DQ20 A44 M_A_DQ16
A:DQ21 A46 M_A_DQ17
A:DQ22 A56 M_A_DQ18
A:DQ23 A58 M_A_DQ19
A:DQ24 A61 M_A_DQ29
A:DQ25 A63 M_A_DQ26
A:DQ26 A73 M_A_DQ30
A:DQ27 A75 M_A_DQ28
A:DQ28 A62 M_A_DQ24
A:DQ29 A64 M_A_DQ25
A:DQ30 A74 M_A_DQ31
A:DQ31 A76 M_A_DQ27
A:DQ32 A123 M_A_DQ33
A:DQ33 A125 M_A_DQ32
A:DQ34 A135 M_A_DQ38
A:DQ35 A137 M_A_DQ34
A:DQ36 A124 M_A_DQ36
A:DQ37 A126 M_A_DQ37
A:DQ38 A134 M_A_DQ39
A:DQ39 A136 M_A_DQ35
A:DQ40 A141 M_A_DQ41
A:DQ41 A143 M_A_DQ40
A:DQ42 A151 M_A_DQ42
A:DQ43 A153 M_A_DQ47
A:DQ44 A140 M_A_DQ44
A:DQ45 A142 M_A_DQ45
A:DQ46 A152 M_A_DQ43
A:DQ47 A154 M_A_DQ46
A:DQ48 A157 M_A_DQ53
A:DQ49 A159 M_A_DQ48
A:DQ50 A173 M_A_DQ54
A:DQ51 A175 M_A_DQ55
A:DQ52 A158 M_A_DQ49
A:DQ53 A160 M_A_DQ52
A:DQ54 A174 M_A_DQ51
A:DQ55 A176 M_A_DQ50
A:DQ56 A179 M_A_DQ56
A:DQ57 A181 M_A_DQ62
A:DQ58 A189 M_A_DQ59
A:DQ59 A191 M_A_DQ58
A:DQ60 A180 M_A_DQ61
A:DQ61 A182 M_A_DQ60
A:DQ62 A192 M_A_DQ57
A:DQ63 A194 M_A_DQ63

M_A_DQ[0..63] 8

Layout Note: Place these Caps near SO DIMM 1

+1.8V

C693 0.1UF c0402
C692 0.1UF c0402
C694 0.1UF c0402
C695 0.1UF c0402
GND GND GND GND

A112 A:VDD1
A96 A:VDD4
A118 A:VDD6
A82 A:VDD8
A88 A:VDD11
A104 A:VDD12

A12 A:VSS5
A48 A:VSS6
A184 A:VSS7
A78 A:VSS8
A72 A:VSS10
A122 A:VSS12
A196 A:VSS13
A8 A:VSS15
A18 A:VSS16
A24 A:VSS17
A42 A:VSS20

A:VSS21 A54
A:VSS24 A60
A:VSS25 A66
A:VSS28 A128
A:VSS32 A172
A:VSS35 A178
A:VSS36 A190
A:VSS41 A34
A:VSS42 A132
A:VSS43 A144
A:VSS44 A156
A:VSS45 A168
A:VSS46 A2
A:VSS53 A28
A:VSS54 A40
A:VSS55 A138
A:VSS56 A150
A:VSS57 A162

GND

+3VS

C700 0.1UF c0402
C699 0.1UF c0402
GND GND

A199 A:VDDSPD

A:NC1 A83
A:NC2 A120
A:NC3 A50
A:NC4 A69
A:NCTEST A163

M_VREF_DIMM1 A1 A:VREF

VREF -> 10/10 mils

C322 2.2uF/6.3V
C319 0.1UF c0402
GND GND

NP_NC1 201
NP_NC2 202
NP_NC3 203
NP_NC4 204
GND1 205
GND2 206
GND3 208
GND4 207

DDR_DIMM1

GND

Layout Note: Place these Caps near SO DIMM 1

+1.8V

C357 2.2uF/6.3V
C691 2.2uF/6.3V
C690 2.2uF/6.3V
C358 2.2uF/6.3V
C359 2.2uF/6.3V
GND GND GND GND GND

SO-DIMM 1 is placed father from the GMCH than SO-DIMM 0

ASUS

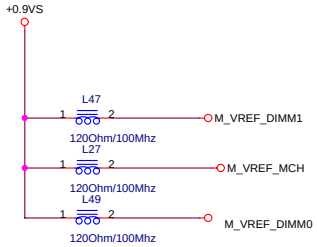
Title : DDR2 SO-DIMM_1

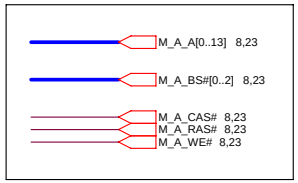
<OrgName>

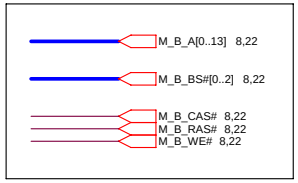
Engineer: Mark Lin

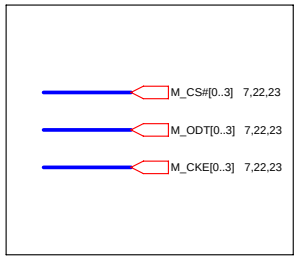
Size	Project Name	Rev
Custom	A6VC	2.0

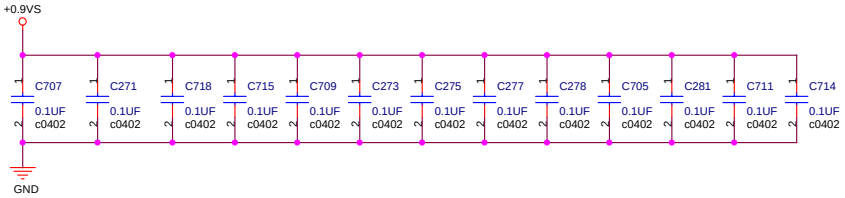
Date: Tuesday, May 17, 2005 Sheet 23 of 58



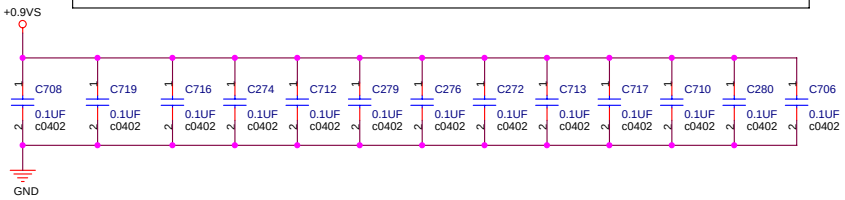




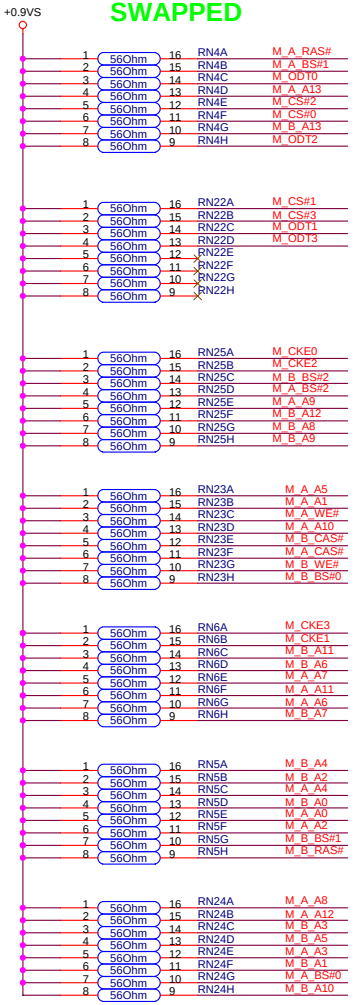




Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



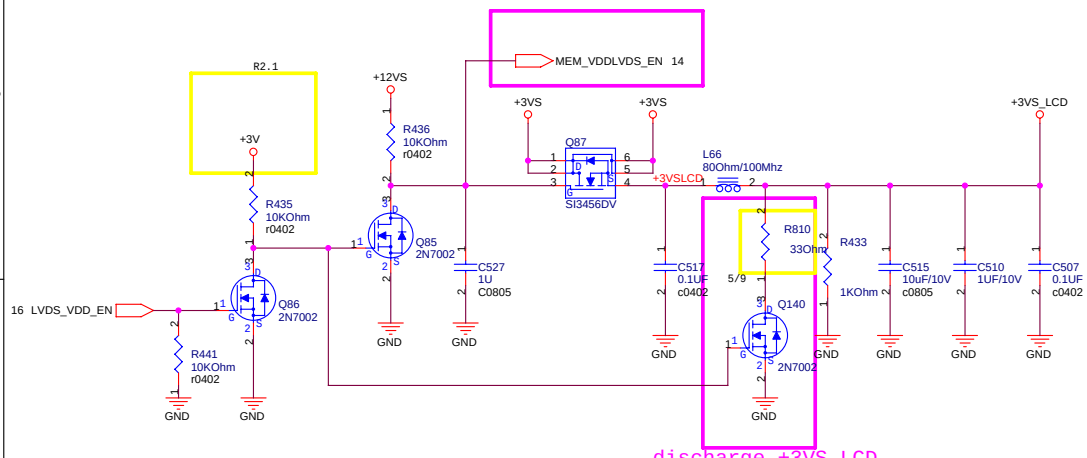
SWAPPED



ASUS	Title : DDR2 ADDRESS TERMINATION		
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 24 of 58		

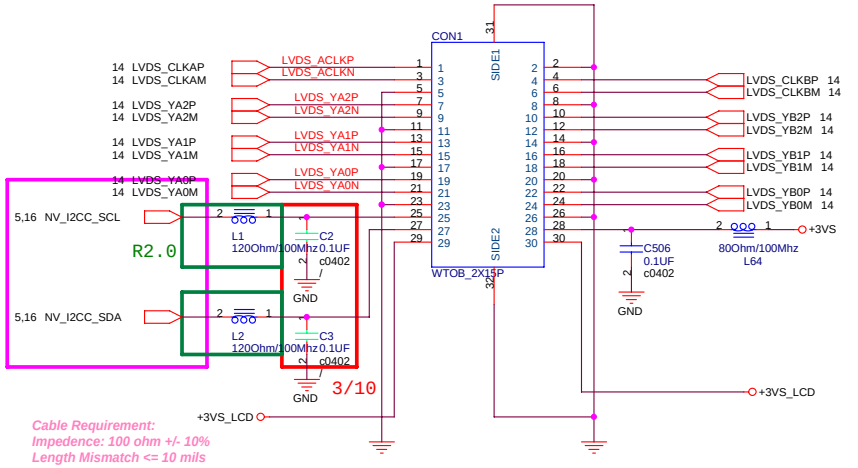
LCD Power

3V-3.6V
Full Active: 410 mA(Max. 500 mA)



discharge +3VS_LCD

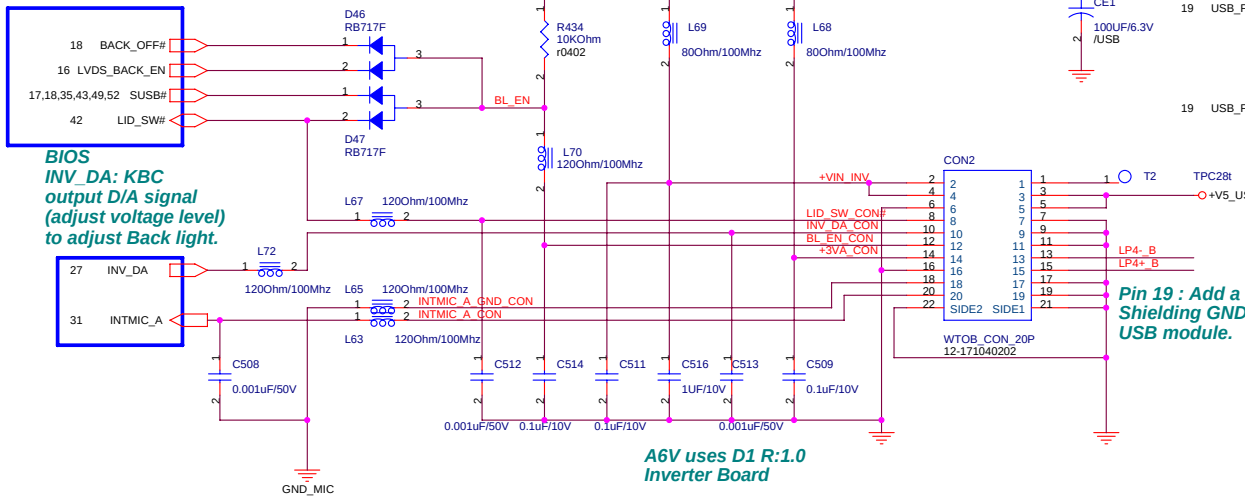
LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

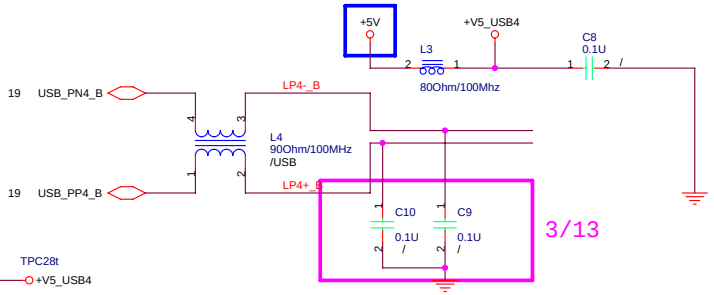
INVERTER Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.



BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

A6V uses D1 R:1.0 Inverter Board

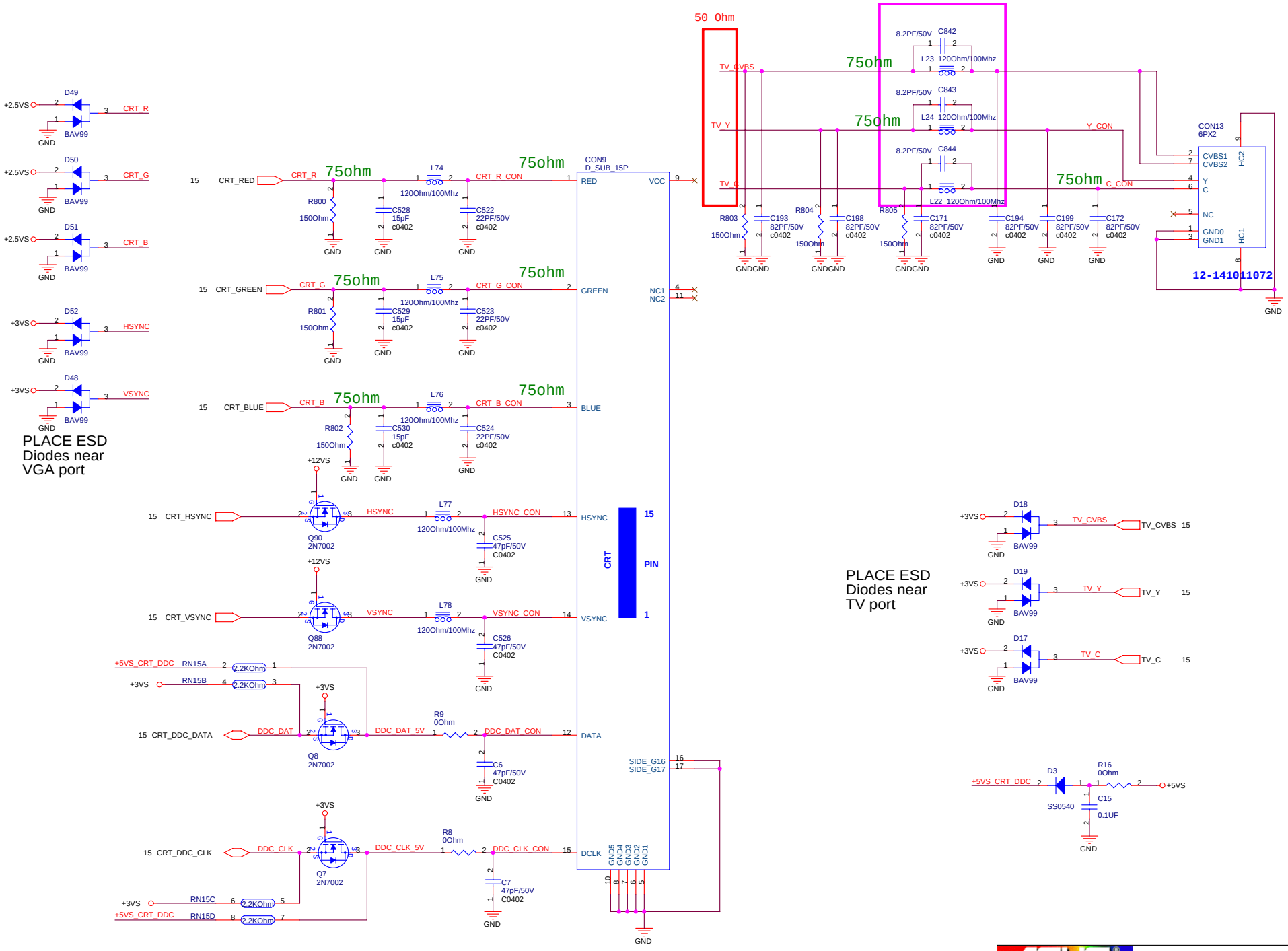


USB PORT 4 for USB CAMERA

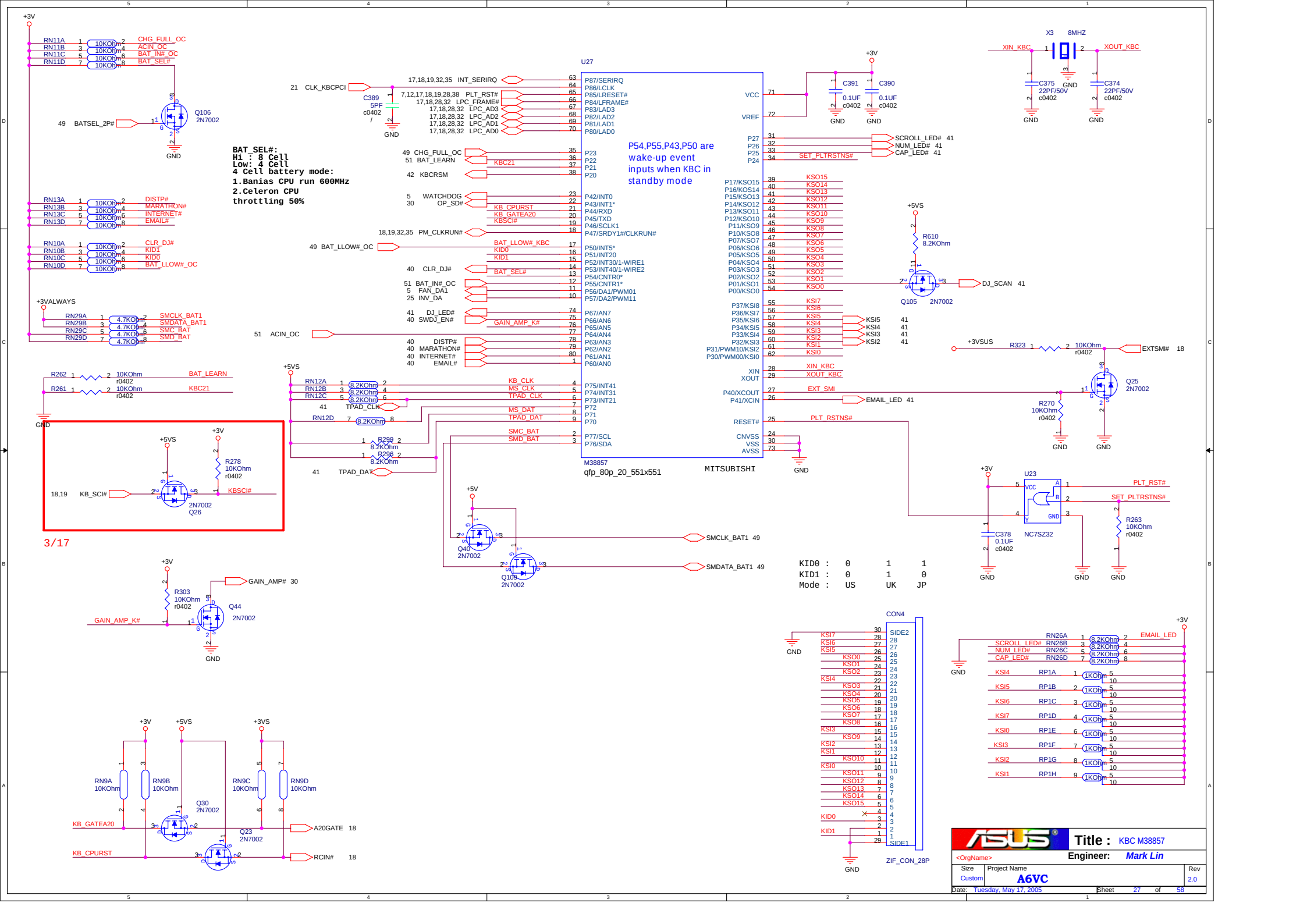
Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

A6V doesn't support USB WLAN function!

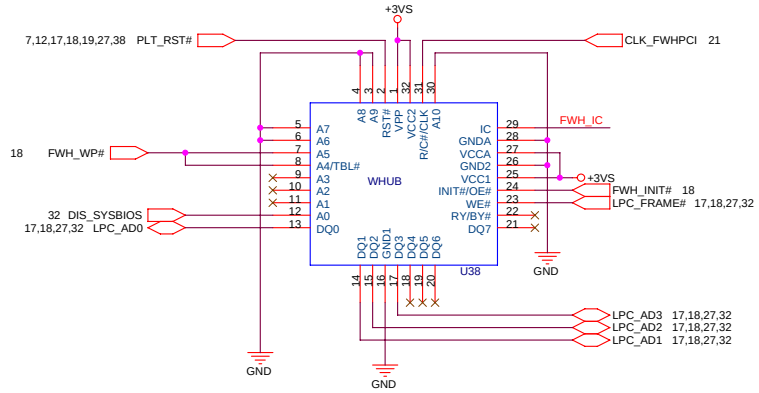
ASUS	Title : LVDS & INVERTER	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 25 of 58	



Title : TV , CRT CONNECTOR			
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 26 of 58		

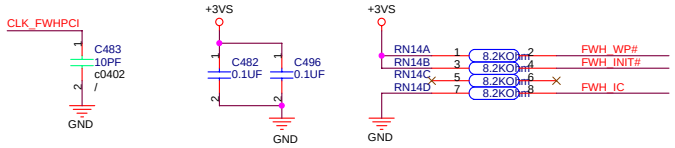

BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell
4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU
throttling 50%
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
U27
M38857
qfp_80p_20_551x551
MITSUBISHI
KID0 : 0 1 1
KID1 : 0 1 0
Mode : US UK JP
3/17
Title : KBC M38857
Engineer: Mark Lin
A6VC
Date: Tuesday, May 17, 2005
Sheet 27 of 58

FWH

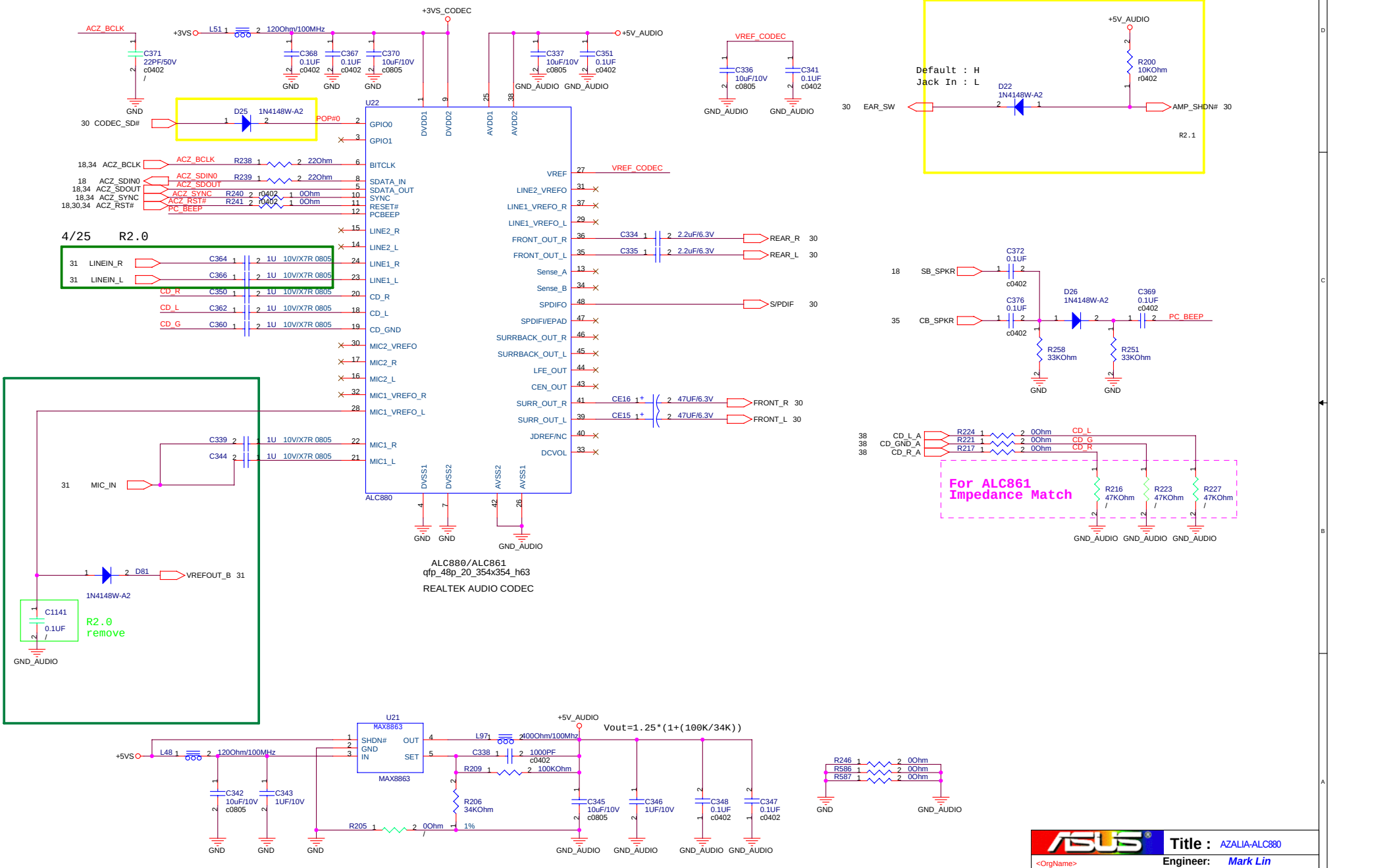


PLCC32 Socket Part Number :
12-043000321

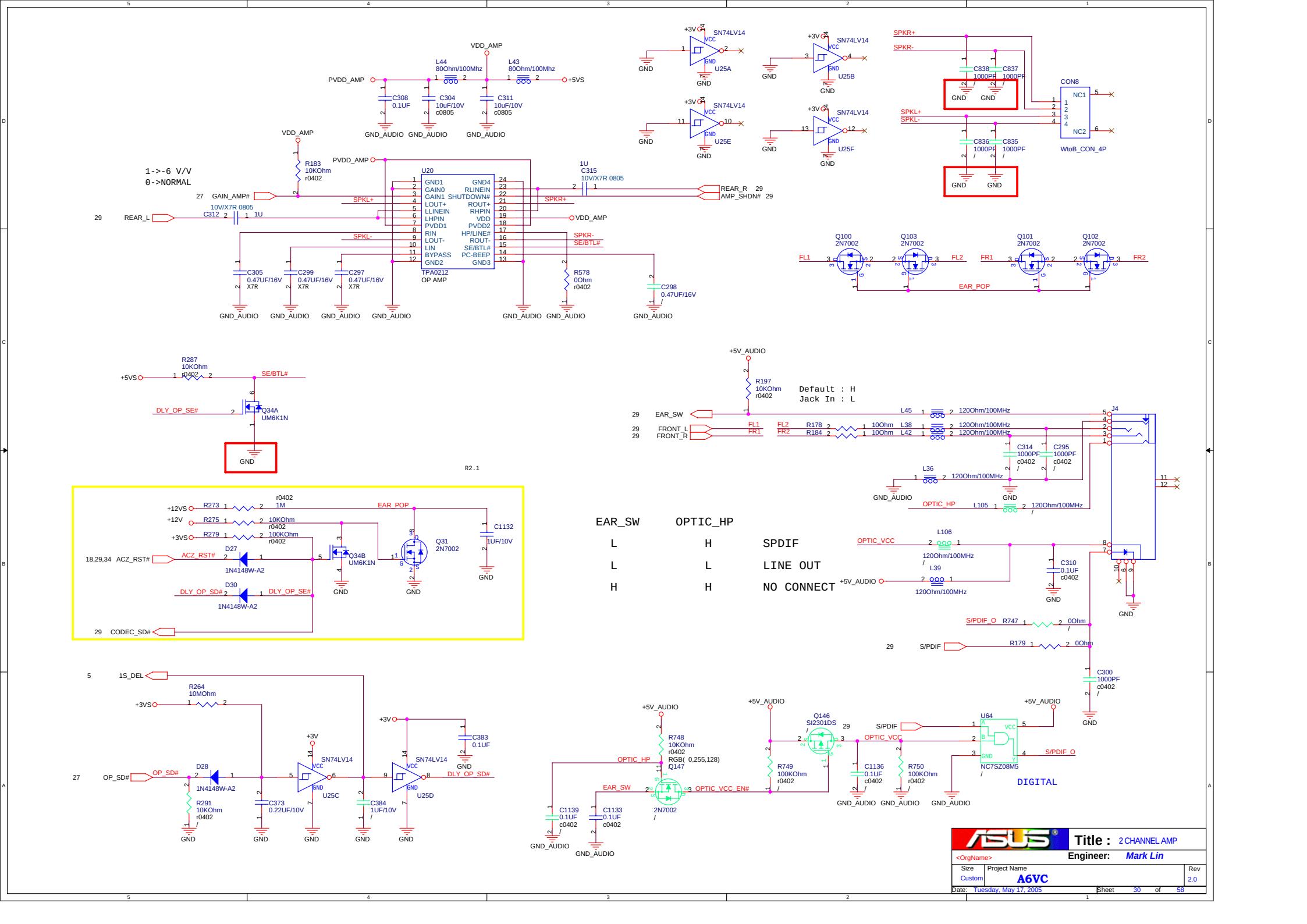
SST FWH/LPC Part Number :
05-001017122(燒)



<OrgName>	Title : FWH	
	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 28 of 58	



Title : AZALIA-ALC880		
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 29 of 58	


VDD_AMP
L44 80Ohm/100Mhz
L43 80Ohm/100Mhz
PVDD_AMP
+5VS
C308 0.1UF
C304 10uF/10V c0805
C311 10uF/10V c0805
GND_AUDIO
SN74LV14
U25A
U25B
U25E
U25F
GND
SPKR+
SPKR-
SPKL+
SPKL-
C838 1000PF
C837 1000PF
C836 1000PF
C835 1000PF
CON8
NC1
NC2
WtoB_CON_4P
1->-6 V/V
0->NORMAL
R183 10KOhm r0402
GAIN_AMP#
REAR_L
C312 10V/X7R 0805 1U
U20
GND1 GND4
GAIN0 RLINEIN
GAIN1 SHUTDOWN#
LOUT+ ROUT+
LLINEIN RHPIN
LHPIN VDD
PVDD1 PVDD2
RIN HP/LINE#
LOUT- ROUT-
LIN SE/BTL#
BYPASS PC-BEEP
GND2 GND3
TPA0212
OP AMP
1U C315 10V/X7R 0805
REAR_R
AMP_SHDN#
C305 0.47UF/16V X7R
C299 0.47UF/16V X7R
C297 0.47UF/16V X7R
R578 0Ohm r0402
C298 0.47UF/16V
Q100 2N7002
Q103 2N7002
Q101 2N7002
Q102 2N7002
FL1
FL2
FR1
FR2
EAR_POP
R287 10KOhm r0402
SE/BTL#
DLY_OP_SE#
Q34A UM6K1N
R2.1
+12VS
+12V
+3VS
R273 r0402 1M
R275 10KOhm r0402
R279 100KOhm r0402
ACZ_RST#
18,29,34 ACZ_RST#
D27 1N4148W-A2
Q34B UM6K1N
Q31 2N7002
C1132 1UF/10V
D30 1N4148W-A2
DLY_OP_SD#
CODEC_SD#
+5V_AUDIO
R197 10KOhm r0402
Default : H
Jack In : L
EAR_SW
FRONT_L
FRONT_R
R178 10Ohm
R184 10Ohm
L45 120Ohm/100MHz
L38 120Ohm/100MHz
L42 120Ohm/100MHz
L36 120Ohm/100MHz
L105 120Ohm/100MHz
J4
C314 1000PF c0402
C295 1000PF c0402
OPTIC_HP
EAR_SW OPTIC_HP
L H SPDIF
L L LINE OUT
H H NO CONNECT
OPTIC_VCC
L106 120Ohm/100MHz
L39 120Ohm/100MHz
C310 0.1UF c0402
S/PDIF_O
R747 0Ohm
S/PDIF
R179 0Ohm
C300 1000PF c0402
1S_DEL
R264 10MOhm
OP_SD#
D28 1N4148W-A2
R291 10KOhm r0402
C373 0.22UF/10V
C384 1UF/10V
C383 0.1UF
U25C
U25D
DLY_OP_SD#
R748 10KOhm r0402 RGB(0,255,128) Q147
2N7002
OPTIC_VCC_EN#
Q146 SI2301DS
R749 100KOhm r0402
R750 100KOhm r0402
C1136 0.1UF c0402
C1139 0.1UF c0402
C1133 0.1UF c0402
U64
NC7SZ08M5
DIGITAL
Title : 2 CHANNEL AMP
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
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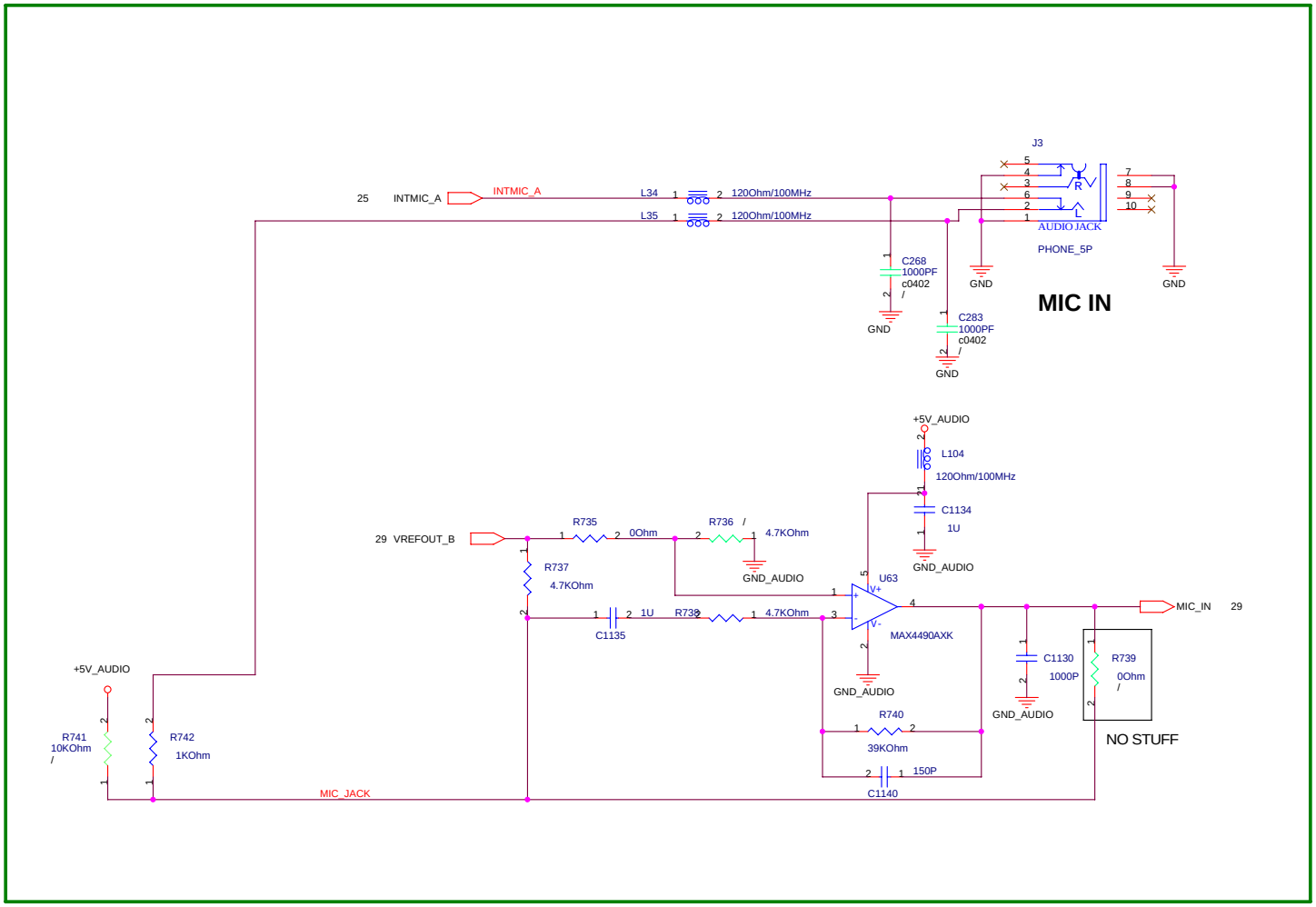
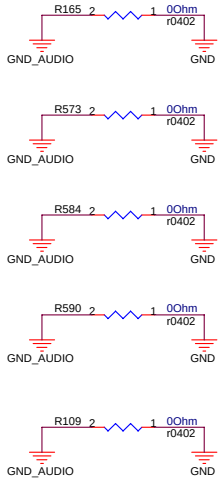
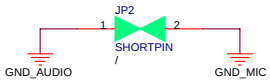
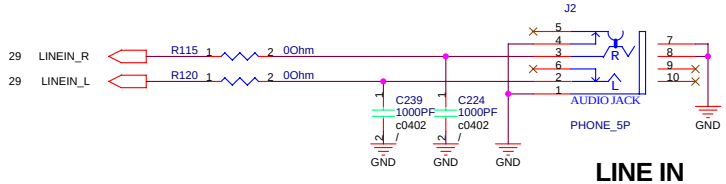


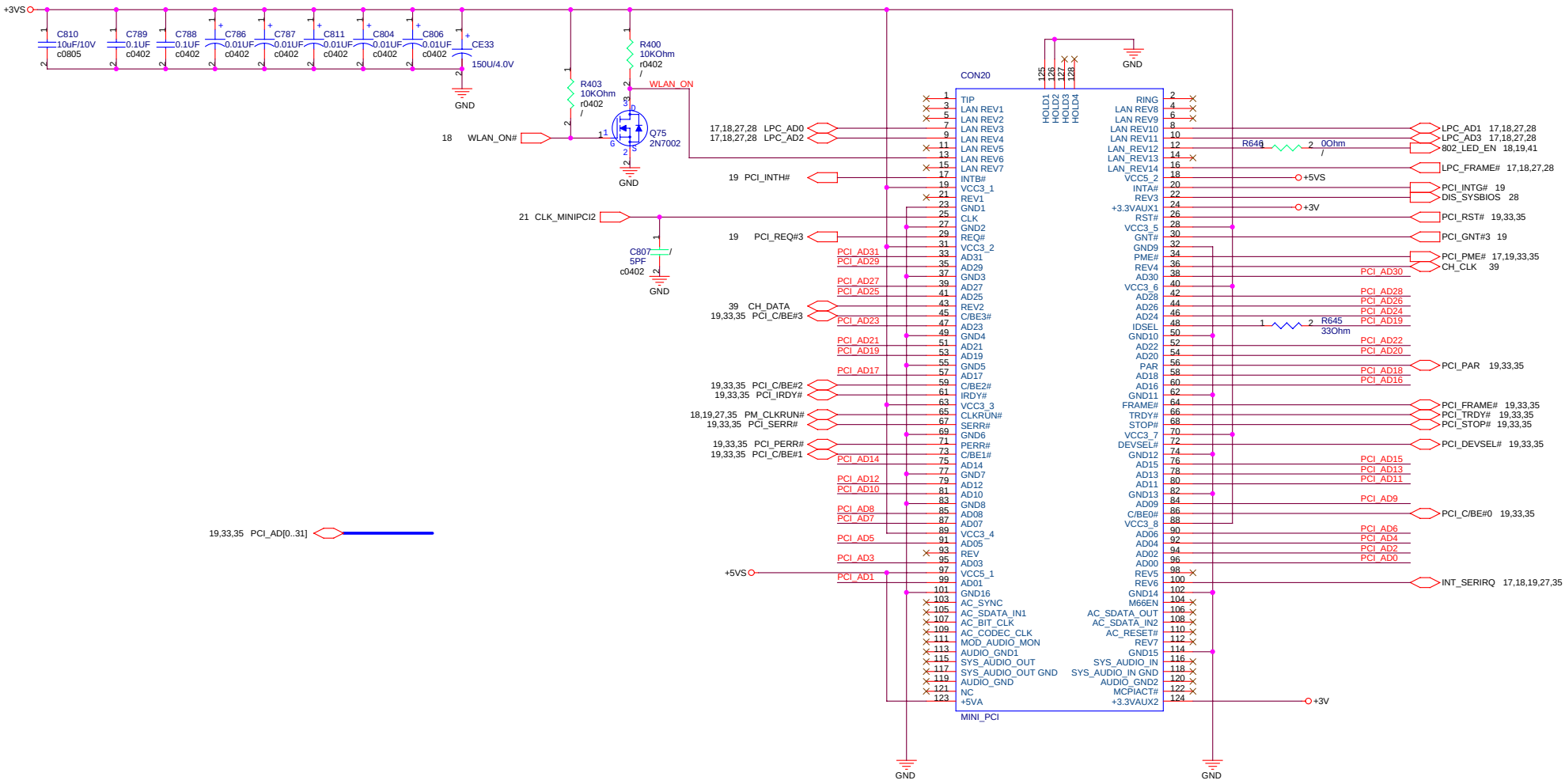


INTMIC_A:GND_AUDIO : W/P/X = 12/5/15mils

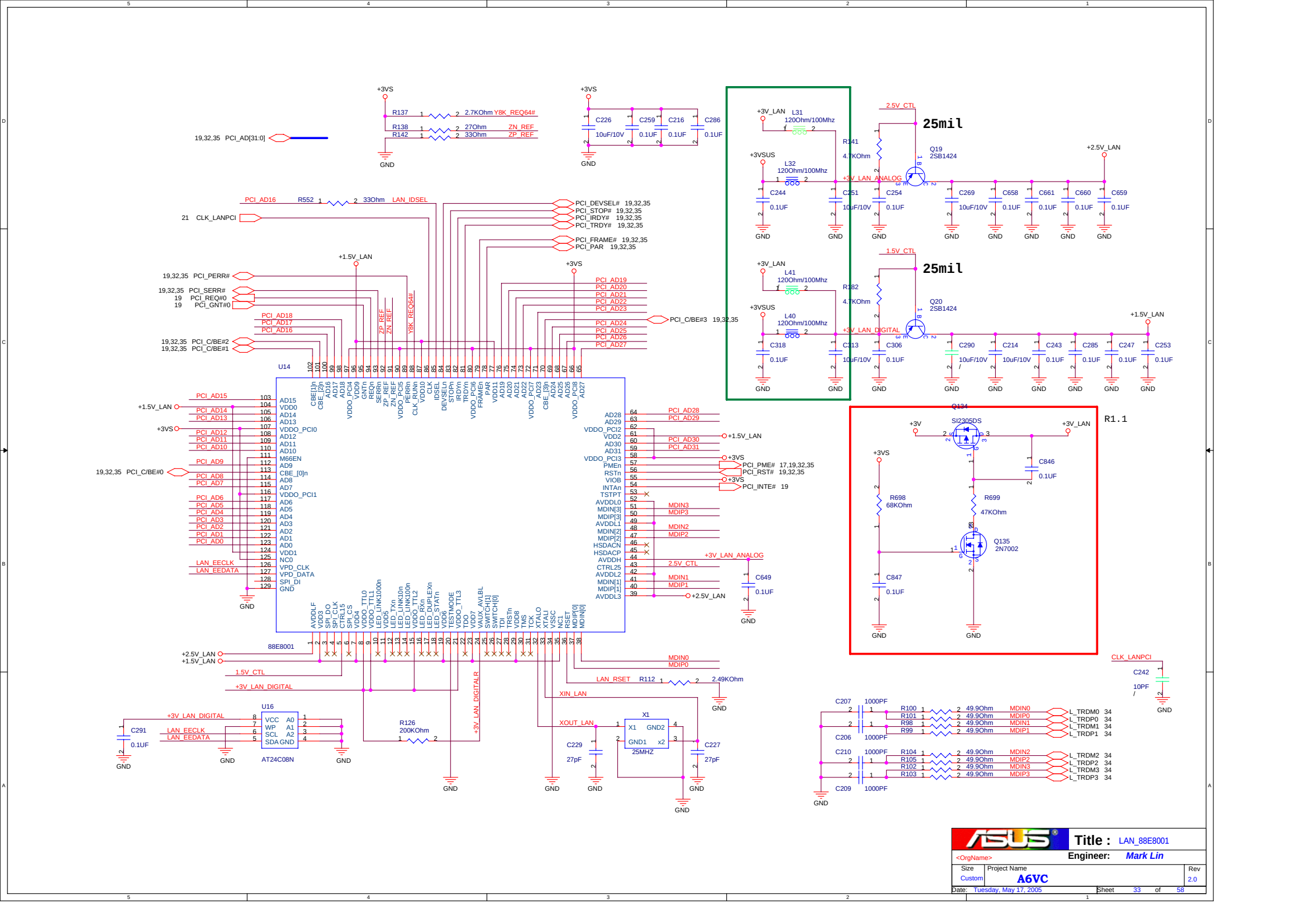


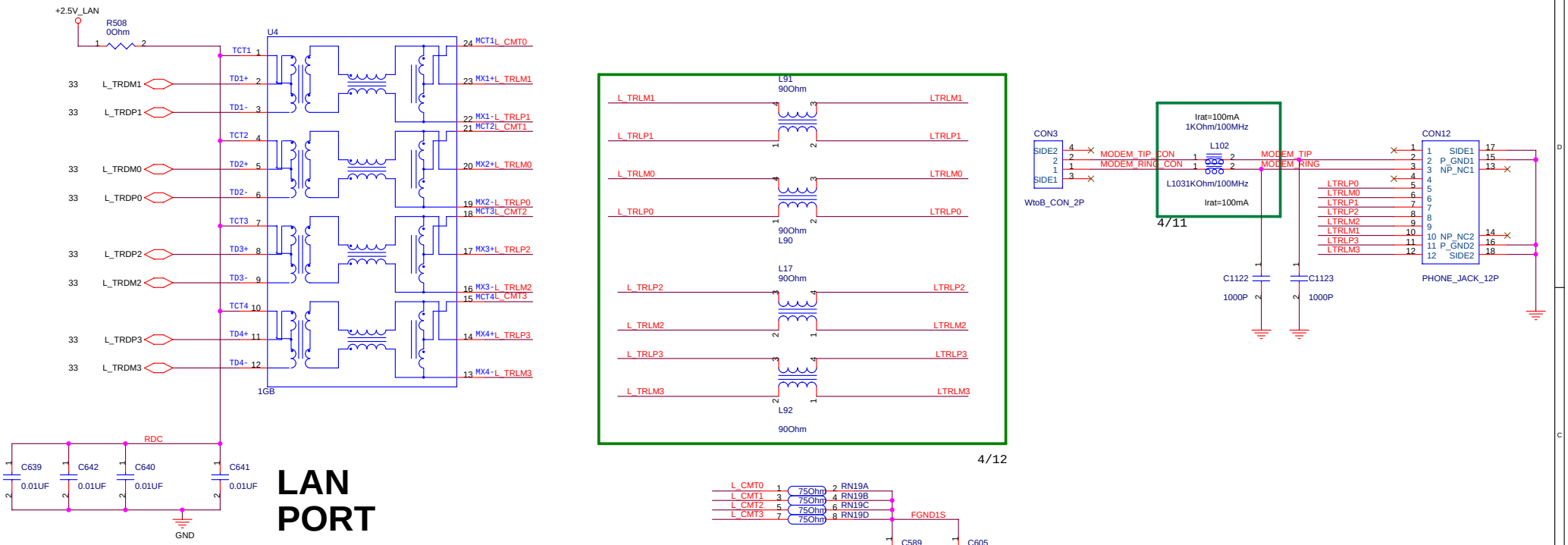


ASUS	Title : MIC,Line-IN Jack		
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 31 of 58		



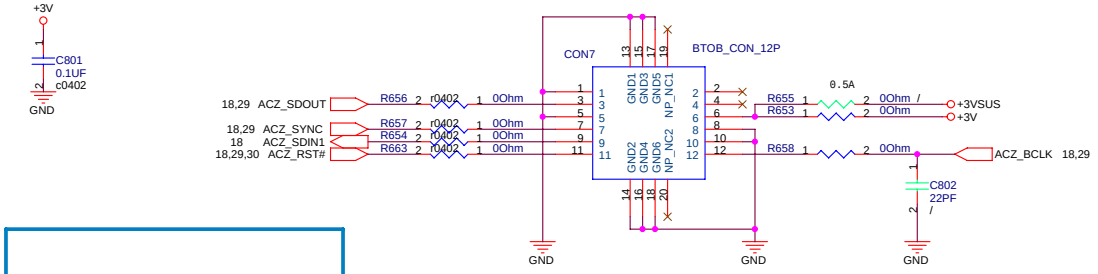
Title :	MINIPCI_WireLess(1)	
<OrgName>	Engineer:	Mark Lin
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 32 of 58	

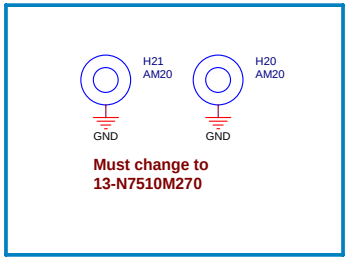

19,32,35 PCI_AD[31:0]
+3VS
R137 2.7KOhm Y8K_REQ64#
R138 27Ohm ZN_REF
R142 33Ohm ZP_REF
GND
C226 10uF/10V
C259 0.1UF
C216 0.1UF
C286 0.1UF
PCI_AD16
R552 33Ohm LAN_IDSEL
21 CLK_LANPCI
PCI_DEVSEL# 19,32,35
PCI_STOP# 19,32,35
PCI_IRDY# 19,32,35
PCI_TRDY# 19,32,35
PCI_FRAME# 19,32,35
PCI_PAR 19,32,35
+1.5V_LAN
19,32,35 PCI_PERR#
19,32,35 PCI_SERR#
19 PCI_REQ#0
19 PCI_GNT#0
PCI_AD18
PCI_AD17
PCI_AD16
19,32,35 PCI_C/BE#2
19,32,35 PCI_C/BE#1
ZP_REF
ZN_REF
Y8K_REQ64#
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_C/BE#3 19,32,35
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
U14
88E8001
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
19,32,35 PCI_C/BE#0
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
LAN_EECLK
LAN_EEDATA
PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31
PCI_PME# 17,19,32,35
PCI_RST# 19,32,35
PCI_INTE# 19
MDIN3
MDIP3
MDIN2
MDIP2
MDIN1
MDIP1
MDIN0
MDIP0
+3V_LAN_ANALOG
2.5V_CTL
C649 0.1UF
+2.5V_LAN
+1.5V_LAN
1.5V_CTL
+3V_LAN_DIGITAL
LAN_RSET R112 2.49KOhm
XIN_LAN
XOUT_LAN
+3V_LAN_DIGITALR
U16
AT24C08N
C291 0.1UF
R126 200KOhm
X1 25MHZ
C229 27pF
C227 27pF
+3V_LAN L31 120Ohm/100Mhz
+3VSUS L32 120Ohm/100Mhz
R241 4.7KOhm
Q19 2SB1424
25mil
2.5V_CTL
C244 0.1UF
C251 10uF/10V
C254 0.1UF
C269 10uF/10V
C658 0.1UF
C661 0.1UF
C660 0.1UF
C659 0.1UF
+3V_LAN L41 120Ohm/100Mhz
+3VSUS L40 120Ohm/100Mhz
R382 4.7KOhm
Q20 2SB1424
1.5V_CTL
C318 0.1UF
C313 10uF/10V
C306 0.1UF
C290 10uF/10V
C214 10uF/10V
C243 0.1UF
C285 0.1UF
C247 0.1UF
C253 0.1UF
Q134 SI2305DS
R1.1
R698 68KOhm
R699 47KOhm
Q135 2N7002
C846 0.1UF
C847 0.1UF
CLK_LANPCI
C242 10PF
C207 1000PF
C206 1000PF
C210 1000PF
C209 1000PF
R100 49.9Ohm MDIN0
R101 49.9Ohm MDIP0
R98 49.9Ohm MDIN1
R99 49.9Ohm MDIP1
R104 49.9Ohm MDIN2
R105 49.9Ohm MDIP2
R102 49.9Ohm MDIN3
R103 49.9Ohm MDIP3
L_TRDM0 34
L_TRDP0 34
L_TRDM1 34
L_TRDP1 34
L_TRDM2 34
L_TRDP2 34
L_TRDM3 34
L_TRDP3 34
Title : LAN_88E8001
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
Sheet 33 of 58



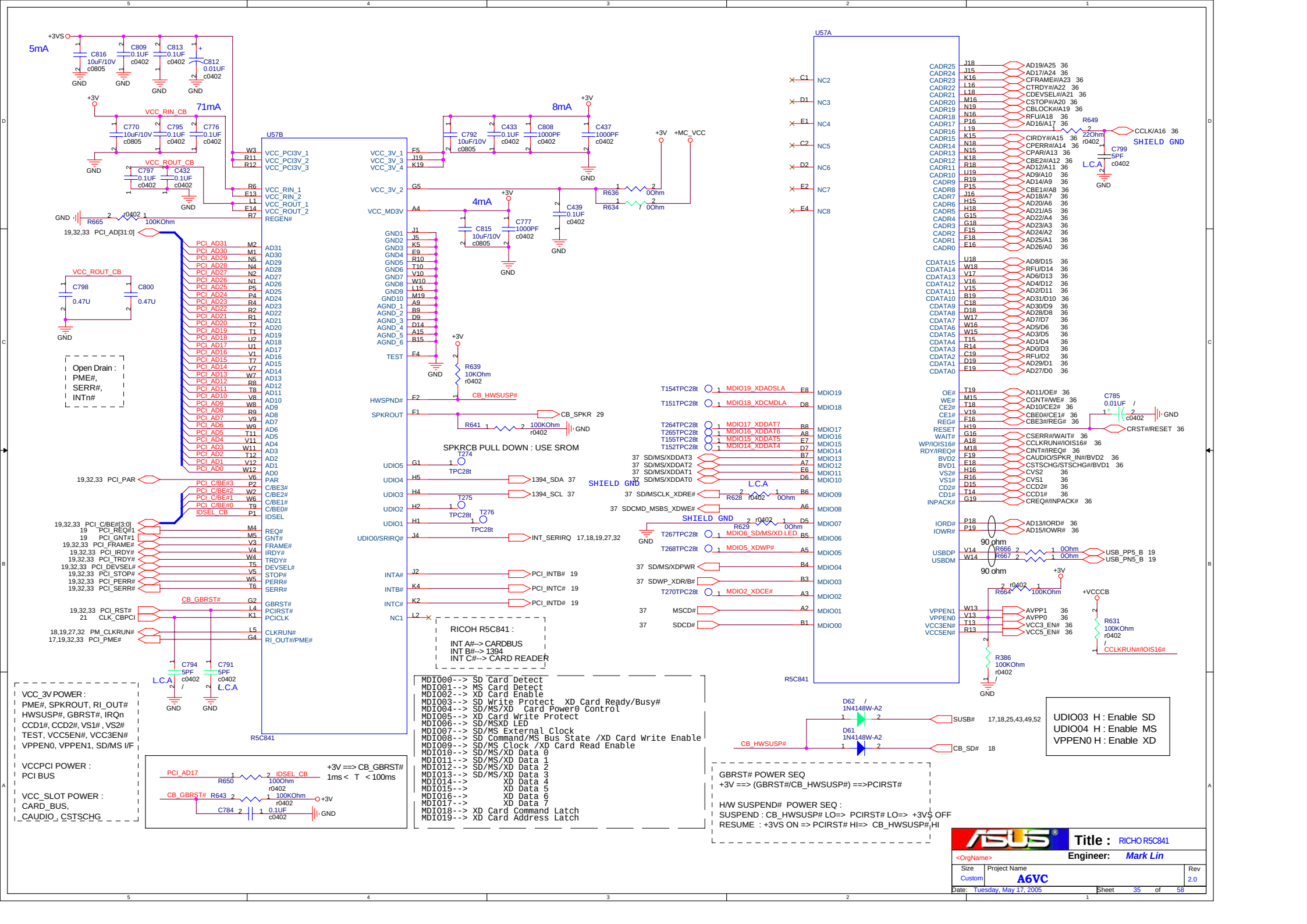
LAN PORT

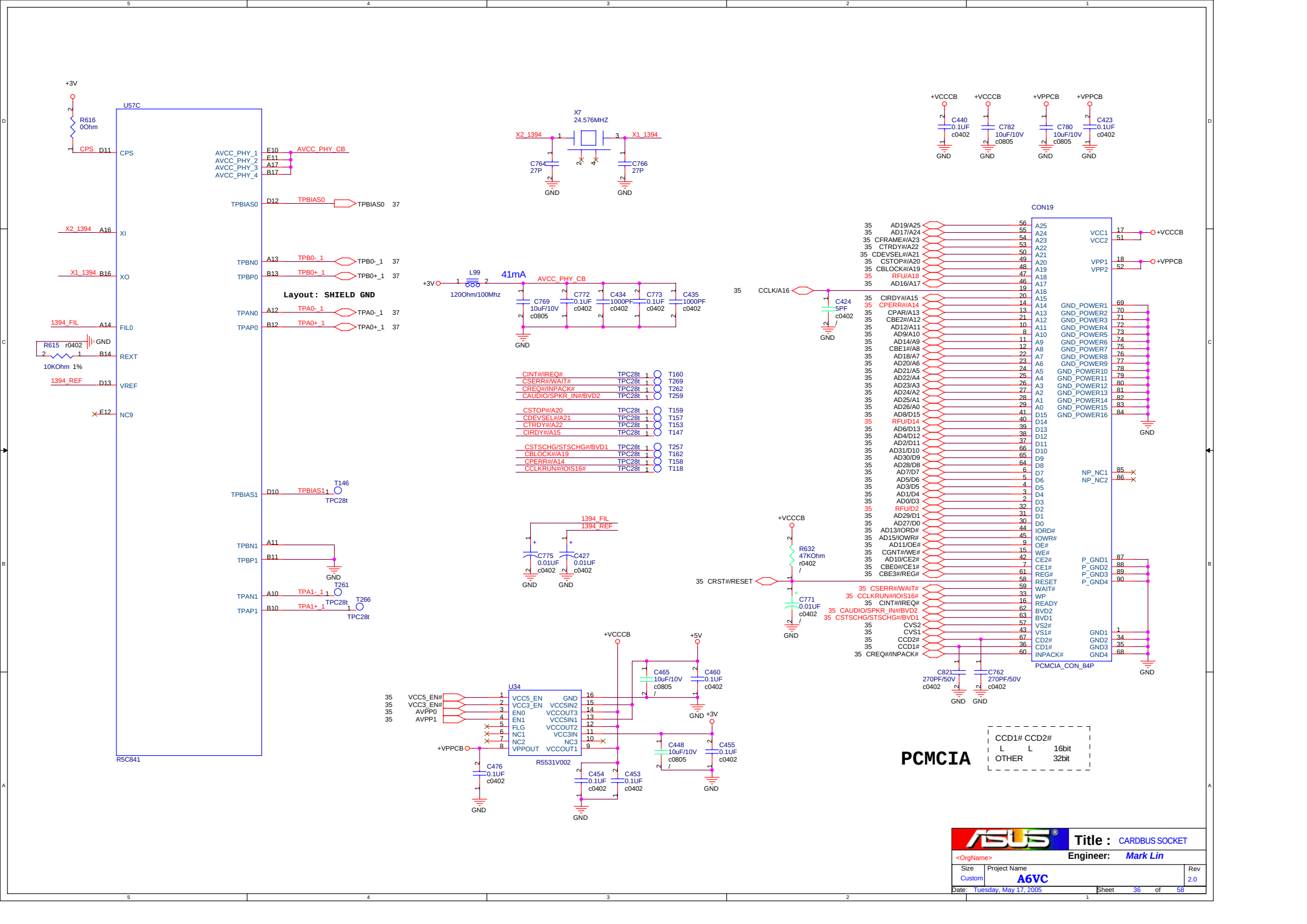
MDC





Title : RJ11+45 & MDC		
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 34 of 58	


5mA
71mA
8mA
4mA
U57B
U57A
R5C841
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP#,HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICHO R5C841
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
Sheet 35 of 58


+3V
R616
0Ohm
CPS
U57C
CPS D11
AVCC_PHY_1 E10
AVCC_PHY_2 E11
AVCC_PHY_3 A17
AVCC_PHY_4 B17
AVCC_PHY_CB
TPBIAS0 D12
TPBIAS0 37
X2_1394 A16
XI
X1_1394 B16
XO
TPBN0 A13
TPBP0 B13
TPB0-_1 37
TPB0+_1 37
Layout: SHIELD GND
TPAN0 A12
TPAP0 B12
TPA0-_1 37
TPA0+_1 37
1394_FIL A14
FIL0
R615 r0402
GND
10KOhm 1%
REXT B14
1394_REF D13
VREF
E12
NC9
TPBIAS1 D10
TPBIAS1
T146
TPC28t
TPBN1 A11
TPBP1 B11
TPAN1 A10
TPAP1 B10
TPA1-_1
TPA1+_1
T261
T266
R5C841
X7
24.576MHZ
X2_1394
X1_1394
C764
27P
C766
27P
L99
120Ohm/100Mhz
41mA
C769
10uF/10V
c0805
C772
0.1UF
c0402
C434
1000PF
c0402
C773
0.1UF
c0402
C435
1000PF
c0402
CINT#/IREQ#
CSERR#/WAIT#
CREQ#/INPACK#
CAUDIO/SPKR_IN#/BVD2
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CIRDY#/A15
CSTSCHG/STSCHG#/BVD1
CBLOCK#/A19
CPERR#/A14
CCLKRUN#/IOIS16#
TPC28t
T160
T269
T262
T259
T159
T157
T153
T147
T257
T162
T158
T118
1394_FIL
1394_REF
C775
0.01UF
c0402
C427
0.01UF
c0402
U34
VCC5_EN#
VCC3_EN#
AVPP0
AVPP1
VCC5_EN
VCC3_EN
EN0
EN1
FLG
NC1
NC2
VPPOUT
GND
VCC5IN2
VCCOUT3
VCC5IN1
VCCOUT2
VCC3IN
NC3
VCCOUT1
R5531V002
+VPPCB
C476
0.1UF
c0402
C454
0.1UF
c0402
C453
0.1UF
c0402
+VCCCB
+5V
C465
10uF/10V
c0805
C460
0.1UF
c0402
C448
10uF/10V
c0805
C455
0.1UF
c0402
+VCCCB
C440
0.1UF
c0402
C782
10uF/10V
c0805
+VPPCB
C780
10uF/10V
c0805
C423
0.1UF
c0402
CON19
CCLK/A16
C424
5PF
c0402
CRST#/RESET
R632
47KOhm
r0402
C771
0.01UF
c0402
AD19/A25
AD17/A24
CFRAME#/A23
CTRDY#/A22
CDEVSEL#/A21
CSTOP#/A20
CBLOCK#/A19
RFU/A18
AD16/A17
CIRDY#/A15
CPERR#/A14
CPAR/A13
CBE2#/A12
AD12/A11
AD9/A10
AD14/A9
CBE1#/A8
AD18/A7
AD20/A6
AD21/A5
AD22/A4
AD23/A3
AD24/A2
AD25/A1
AD26/A0
AD8/D15
RFU/D14
AD6/D13
AD4/D12
AD2/D11
AD31/D10
AD30/D9
AD28/D8
AD7/D7
AD5/D6
AD3/D5
AD1/D4
AD0/D3
RFU/D2
AD29/D1
AD27/D0
AD13/IORD#
AD15/IOWR#
AD11/OE#
CGNT#/WE#
AD10/CE2#
CBE0#/CE1#
CBE3#/REG#
CSERR#/WAIT#
CCLKRUN#/IOIS16#
CINT#/IREQ#
CAUDIO/SPKR_IN#/BVD2
CSTSCHG/STSCHG#/BVD1
CVS2
CVS1
CCD2#
CCD1#
CREQ#/INPACK#
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
IORD#
IOWR#
OE#
WE#
CE2#
CE1#
REG#
RESET
WAIT#
WP
READY
BVD2
BVD1
VS2#
VS1#
CD2#
CD1#
INPACK#
VCC1
VCC2
VPP1
VPP2
GND_POWER1
GND_POWER2
GND_POWER3
GND_POWER4
GND_POWER5
GND_POWER6
GND_POWER7
GND_POWER8
GND_POWER9
GND_POWER10
GND_POWER11
GND_POWER12
GND_POWER13
GND_POWER14
GND_POWER15
GND_POWER16
NP_NC1
NP_NC2
P_GND1
P_GND2
P_GND3
P_GND4
GND1
GND2
GND3
GND4
PCMCIA_CON_84P
C821
270PF/50V
c0402
C762
270PF/50V
c0402
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
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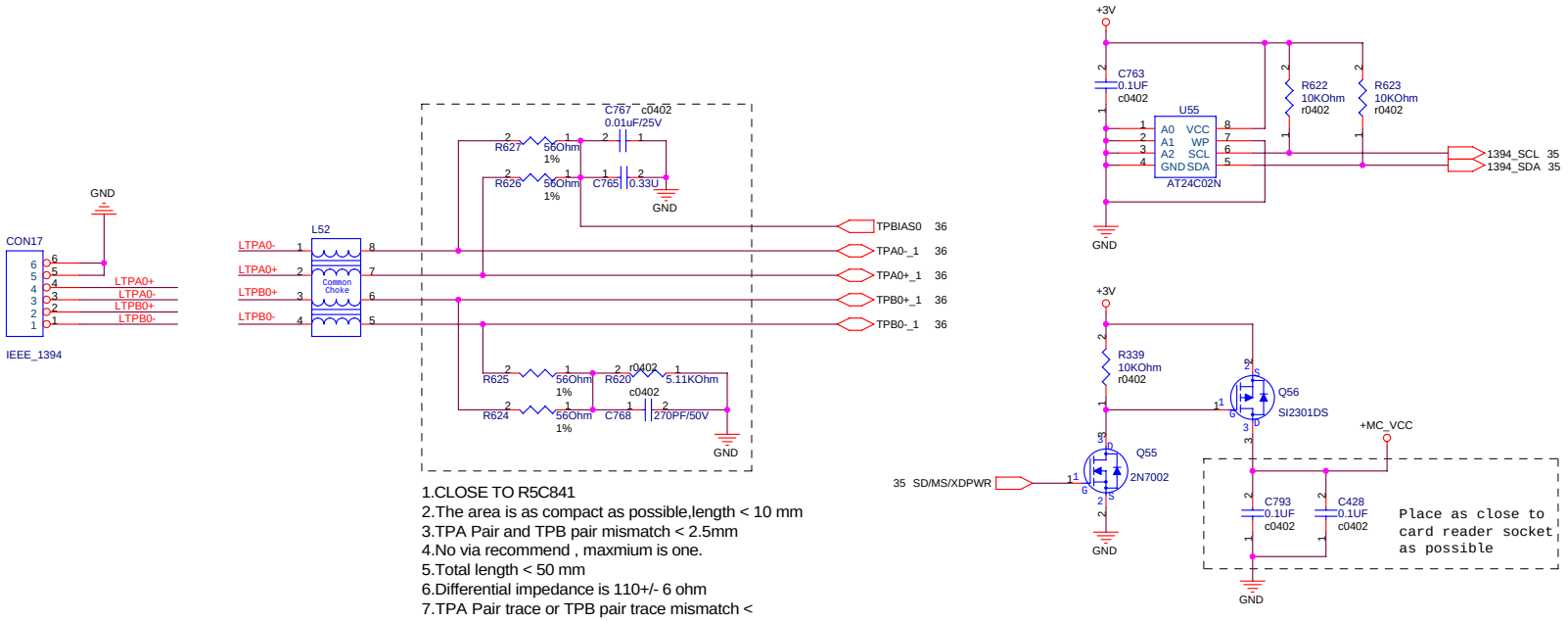
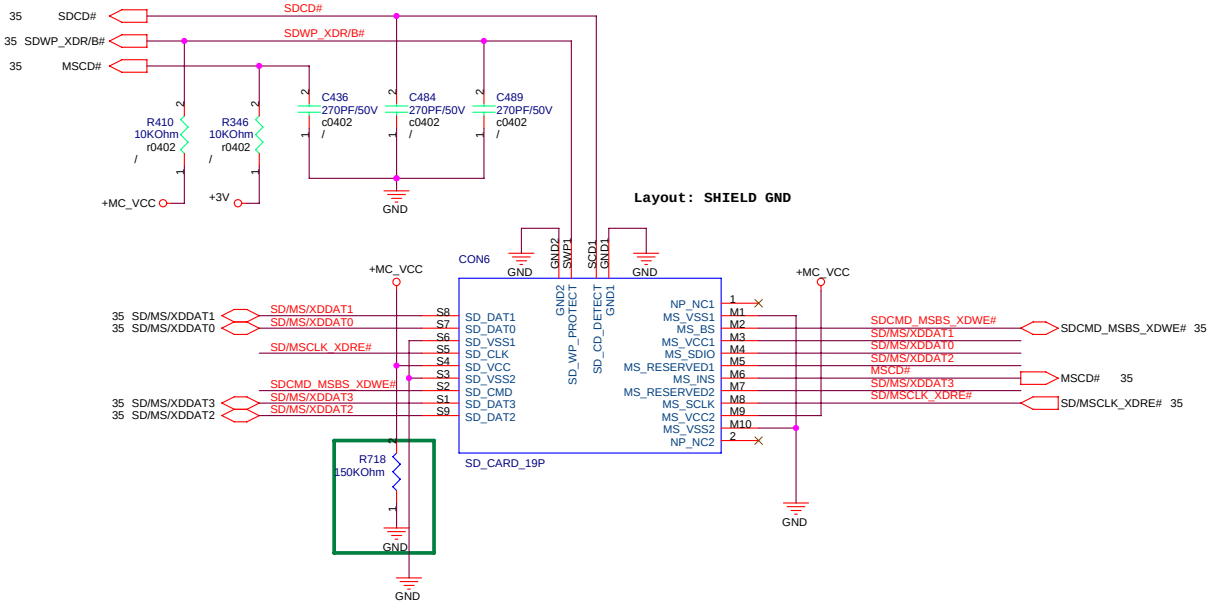
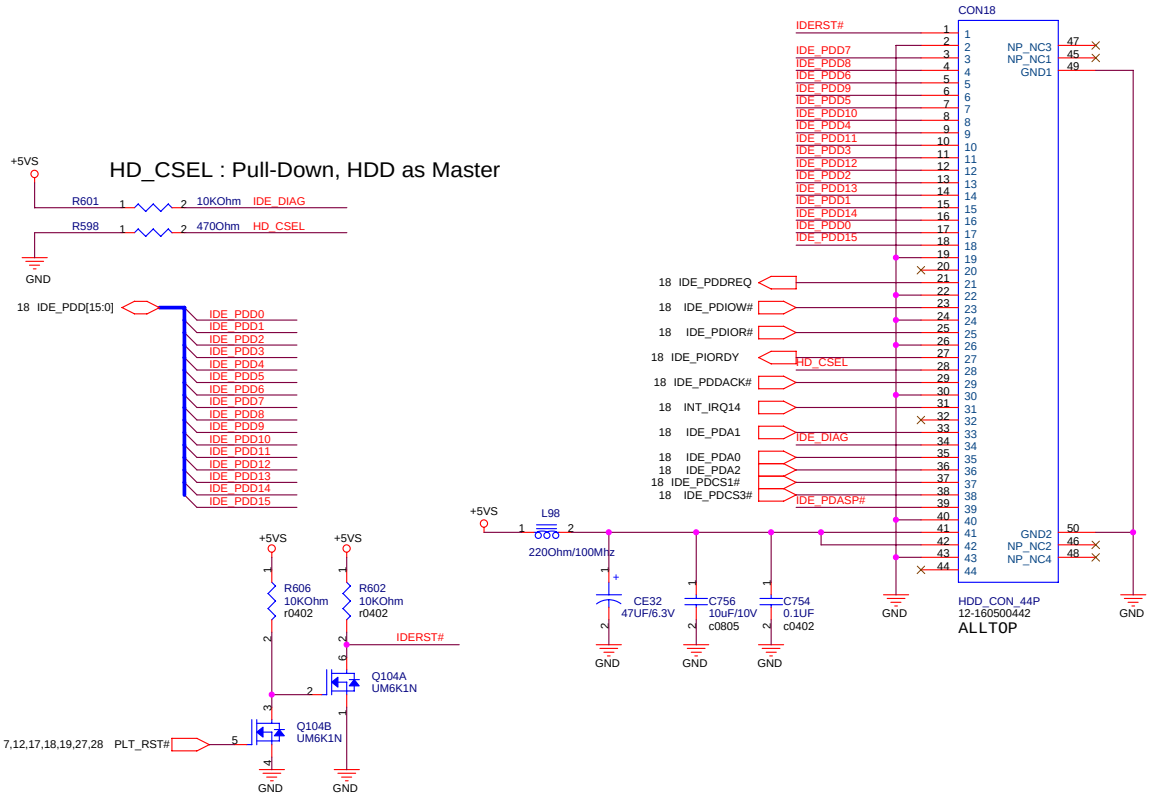


1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

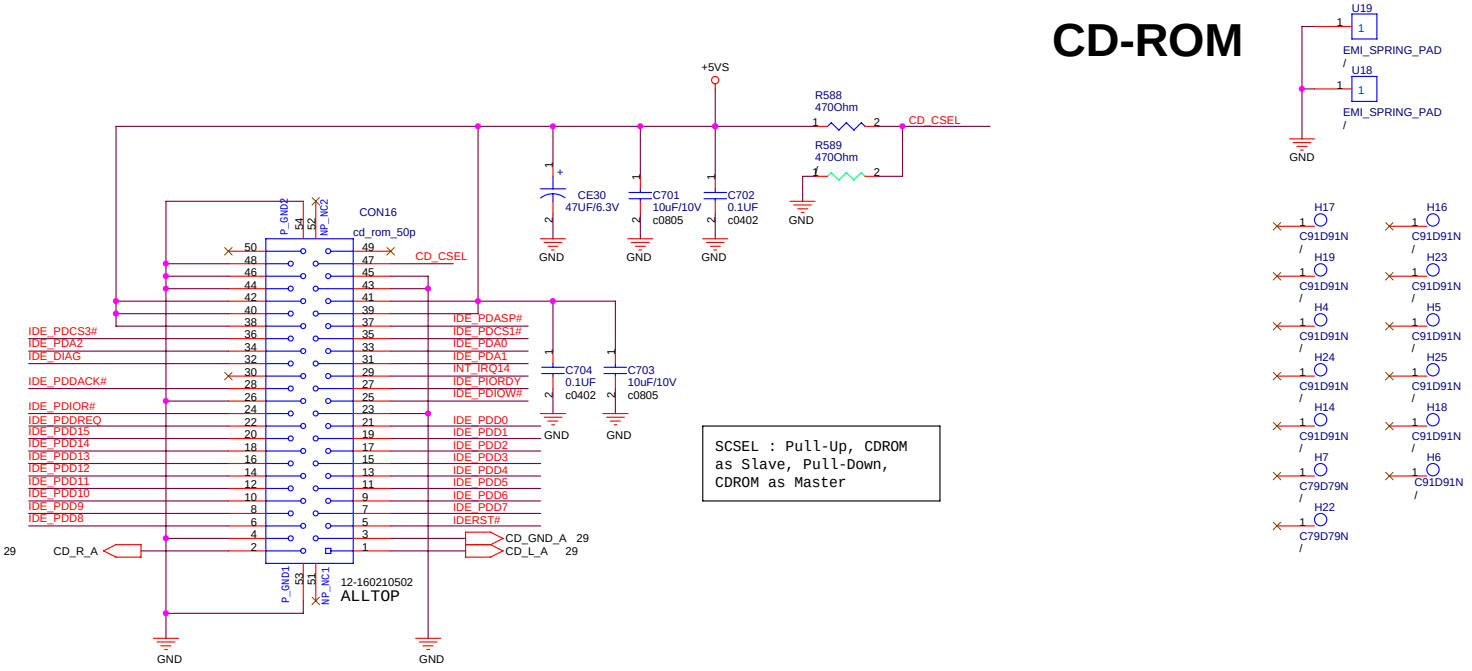


Title : 1394 & 4 IN 1 CON			
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 37 of 58		

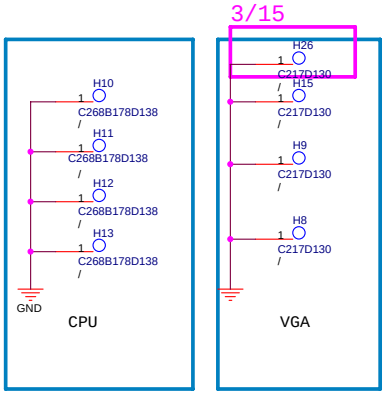
HDD



CD-ROM



SCSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master



ASUS	Title : HDD & CD-ROM	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
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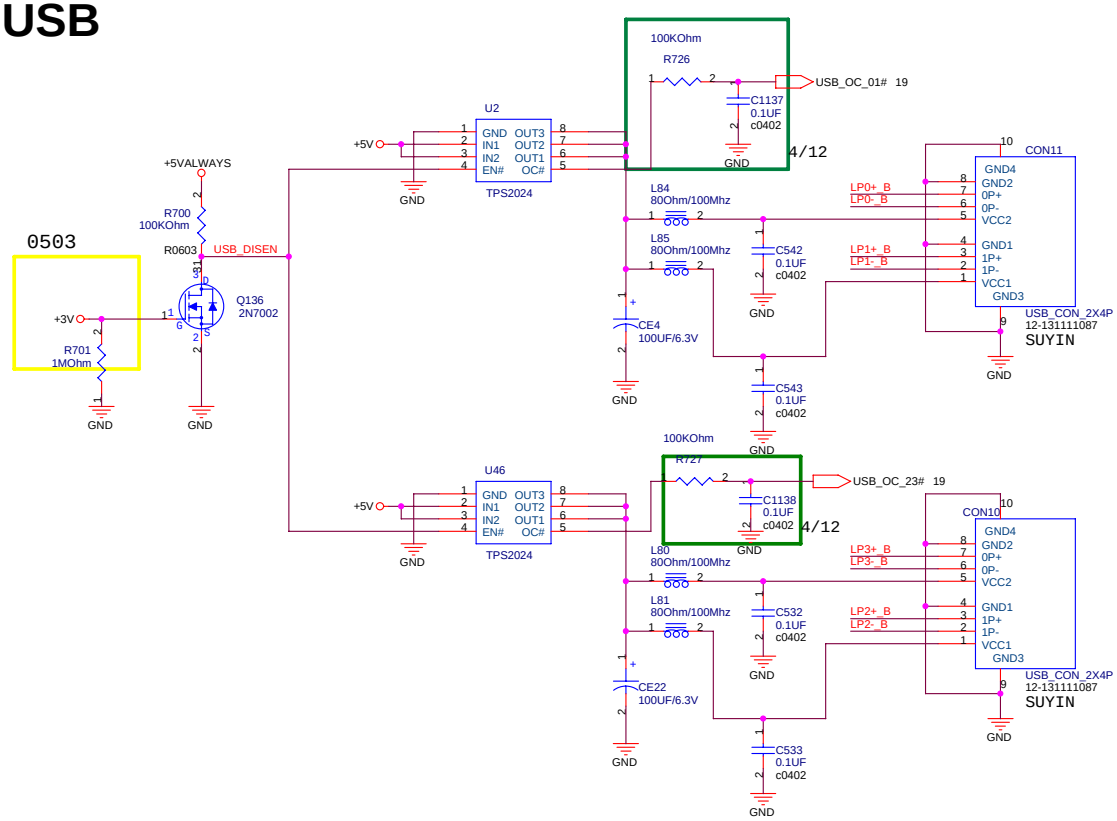
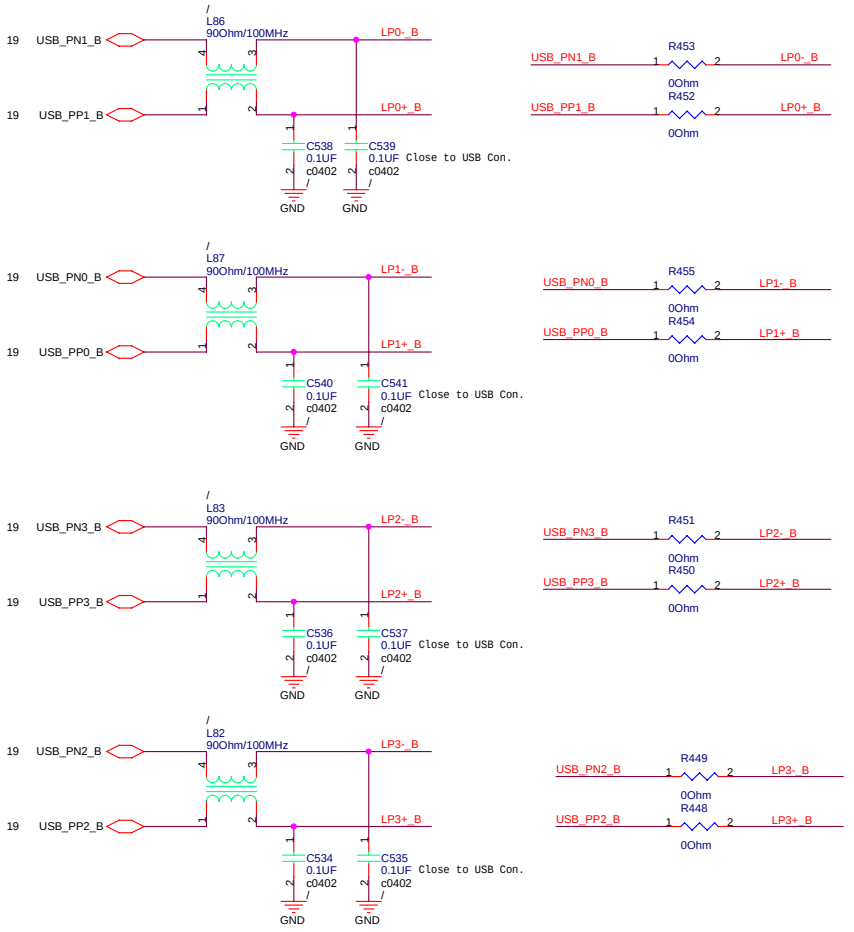
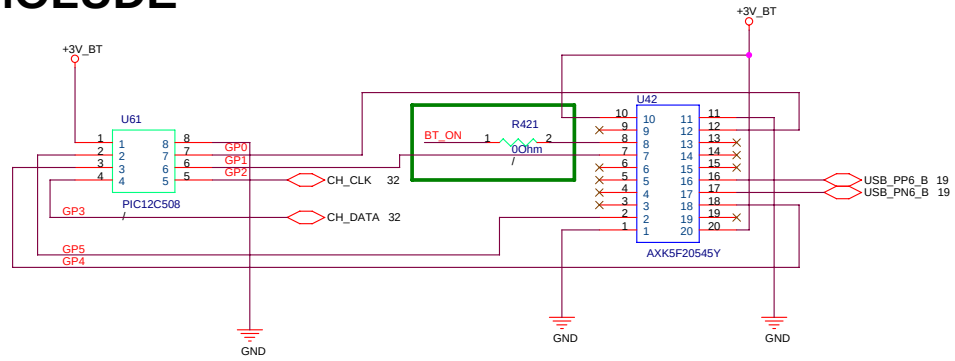
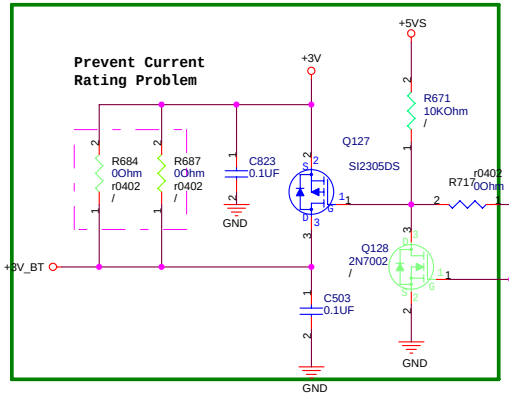
USB





BLUE TOOTH MOLUDE

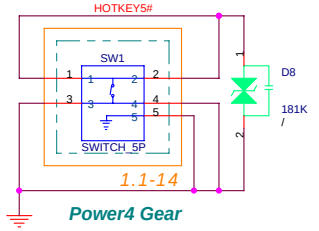


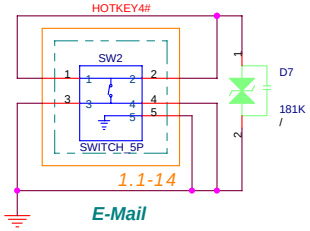


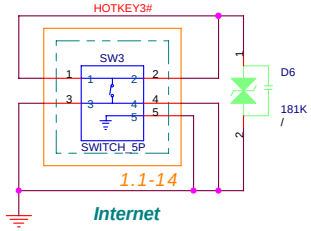
Title : USB & Bluse tooth module			
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 39 of 58		

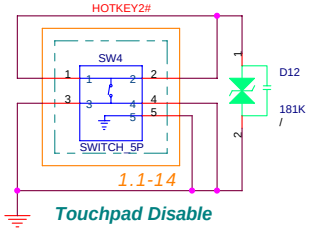
FUNCTION KEY

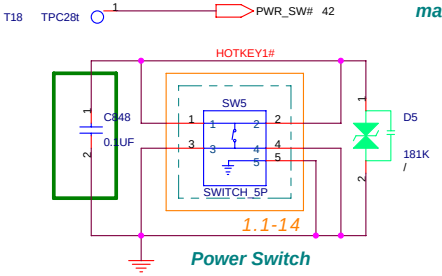
Uses 5-pin switch to improve ESD margin.

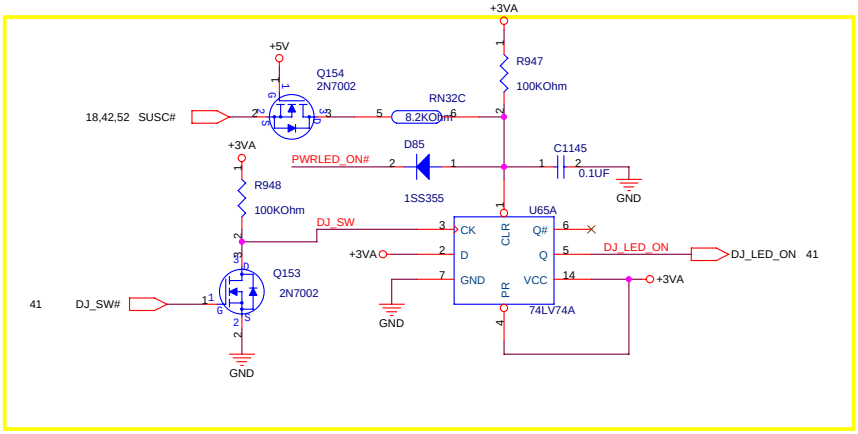




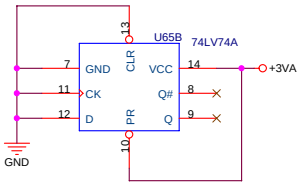


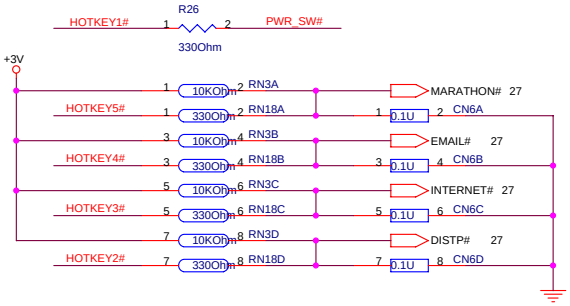


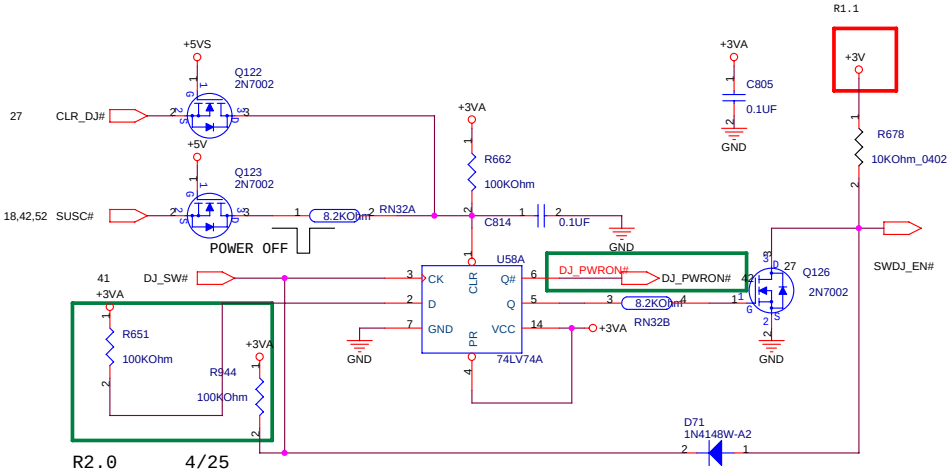




5/4







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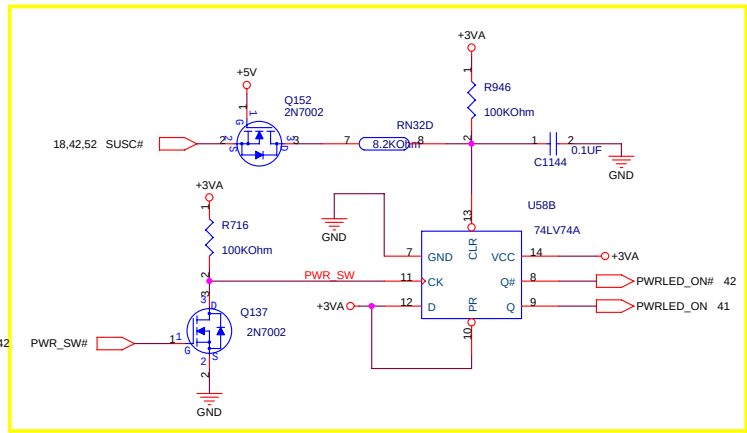
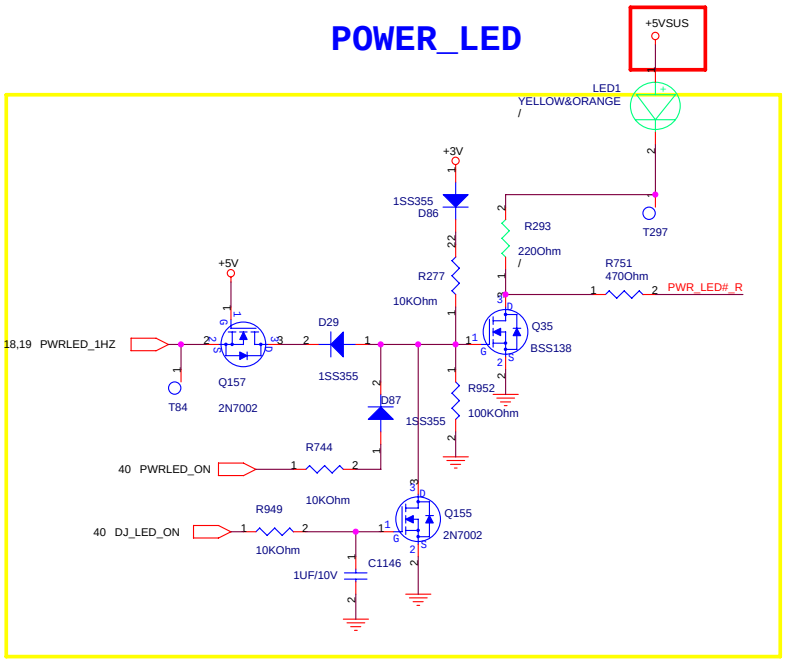
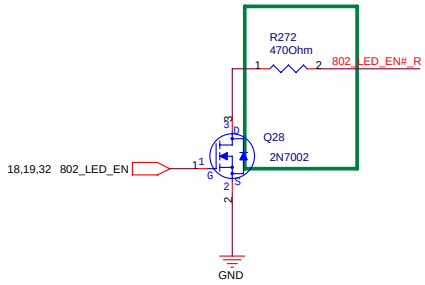


ASUS	Title : FUNCTION KEY & DJ	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 40 of 58	

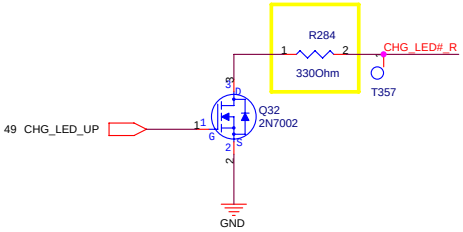


R2.0

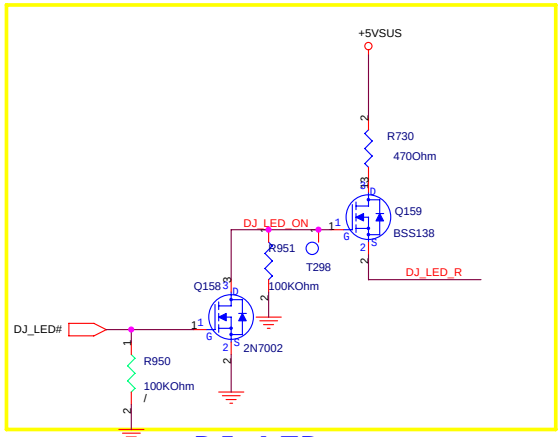


802_LED

5/3 R2.0

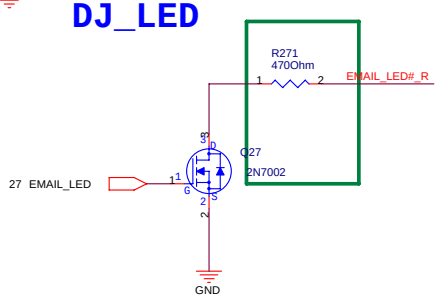


CHG_LED



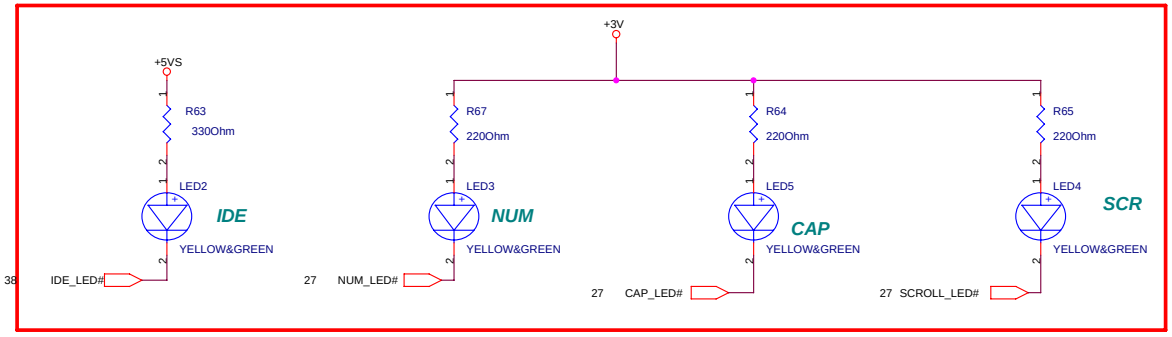
5/4

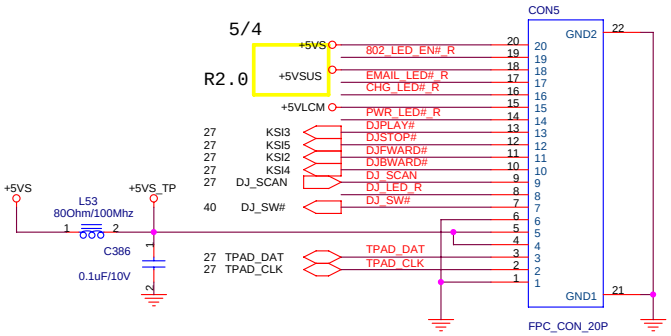
DJ_LED



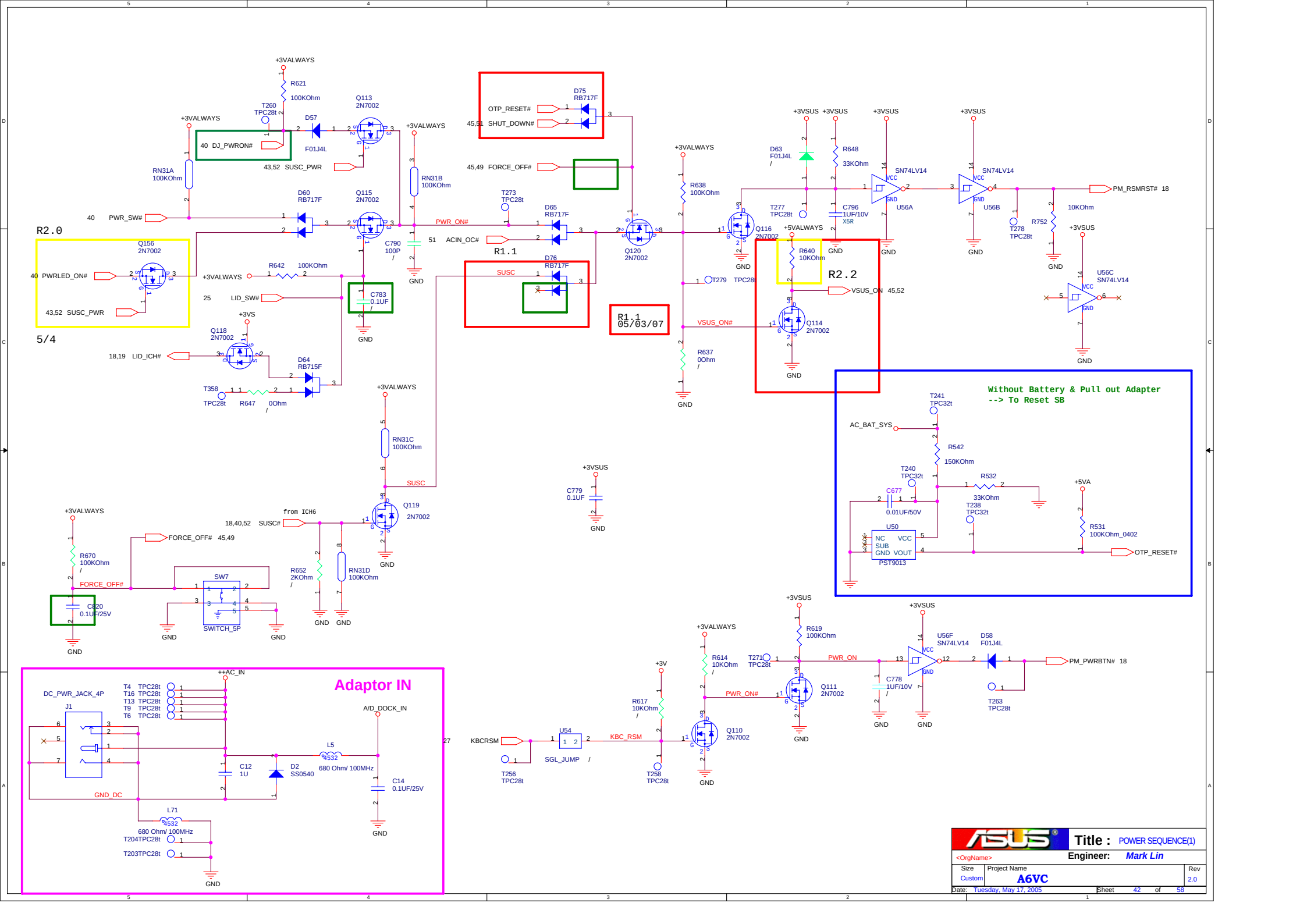
EMAIL_LED

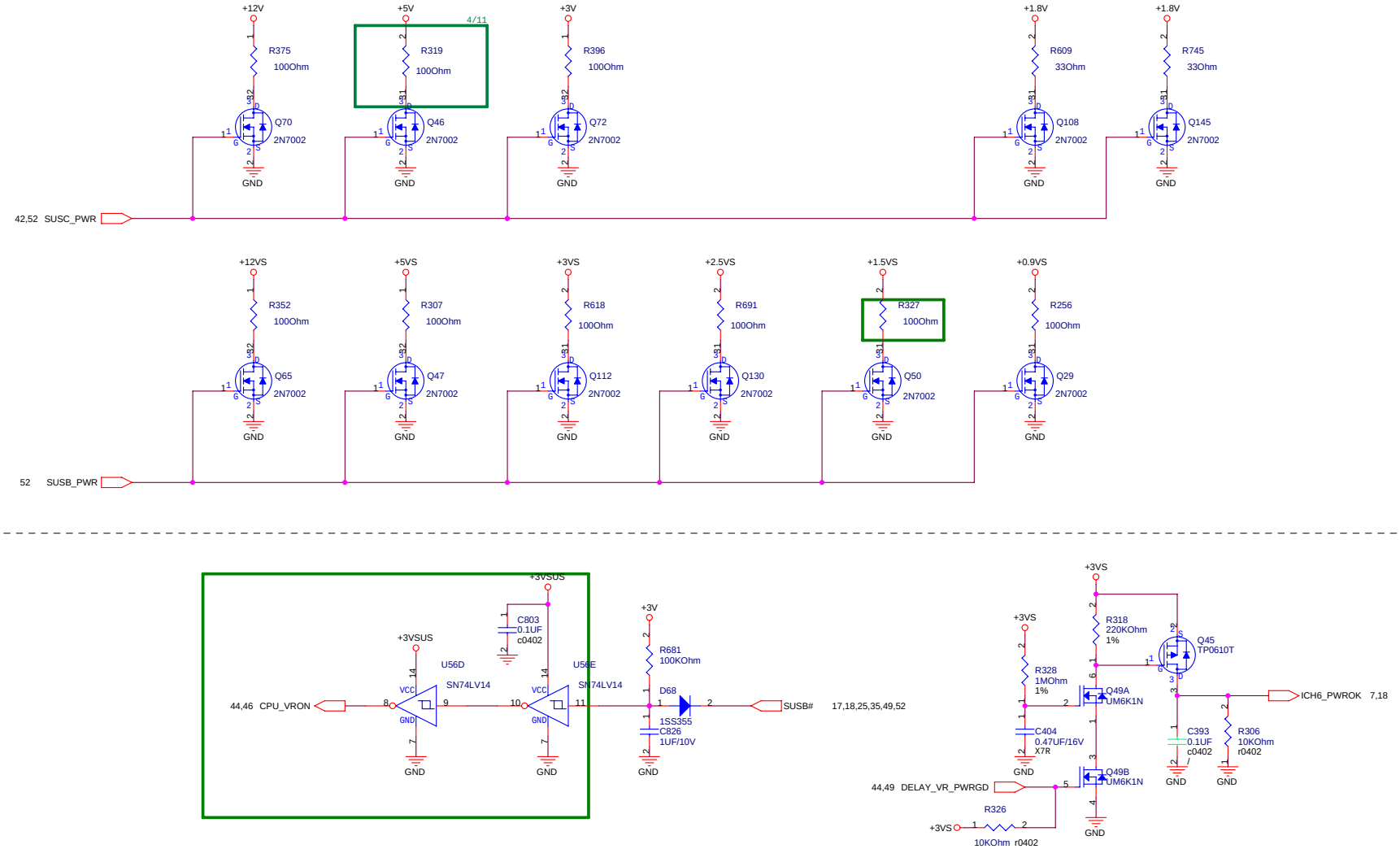
R1.1



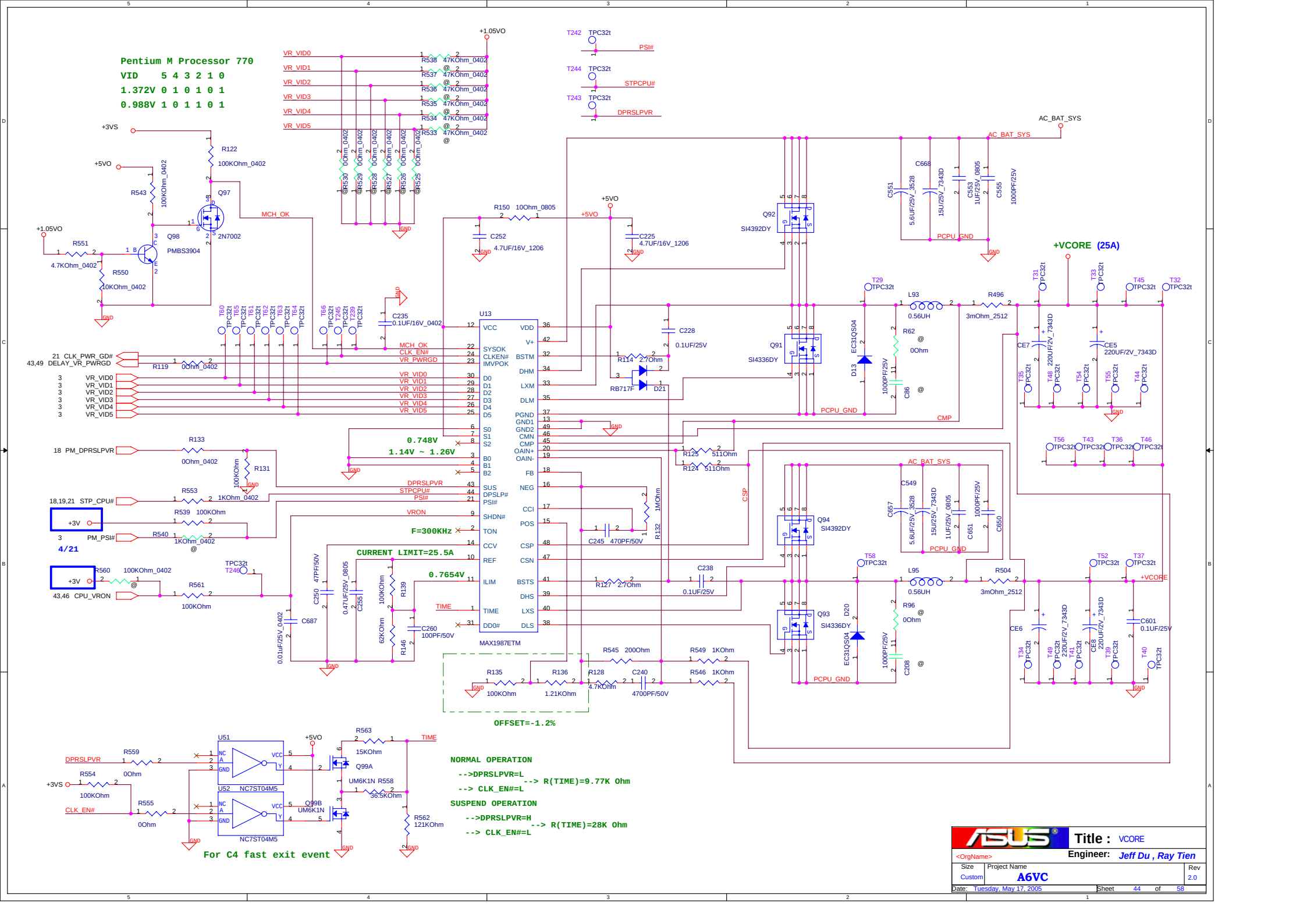


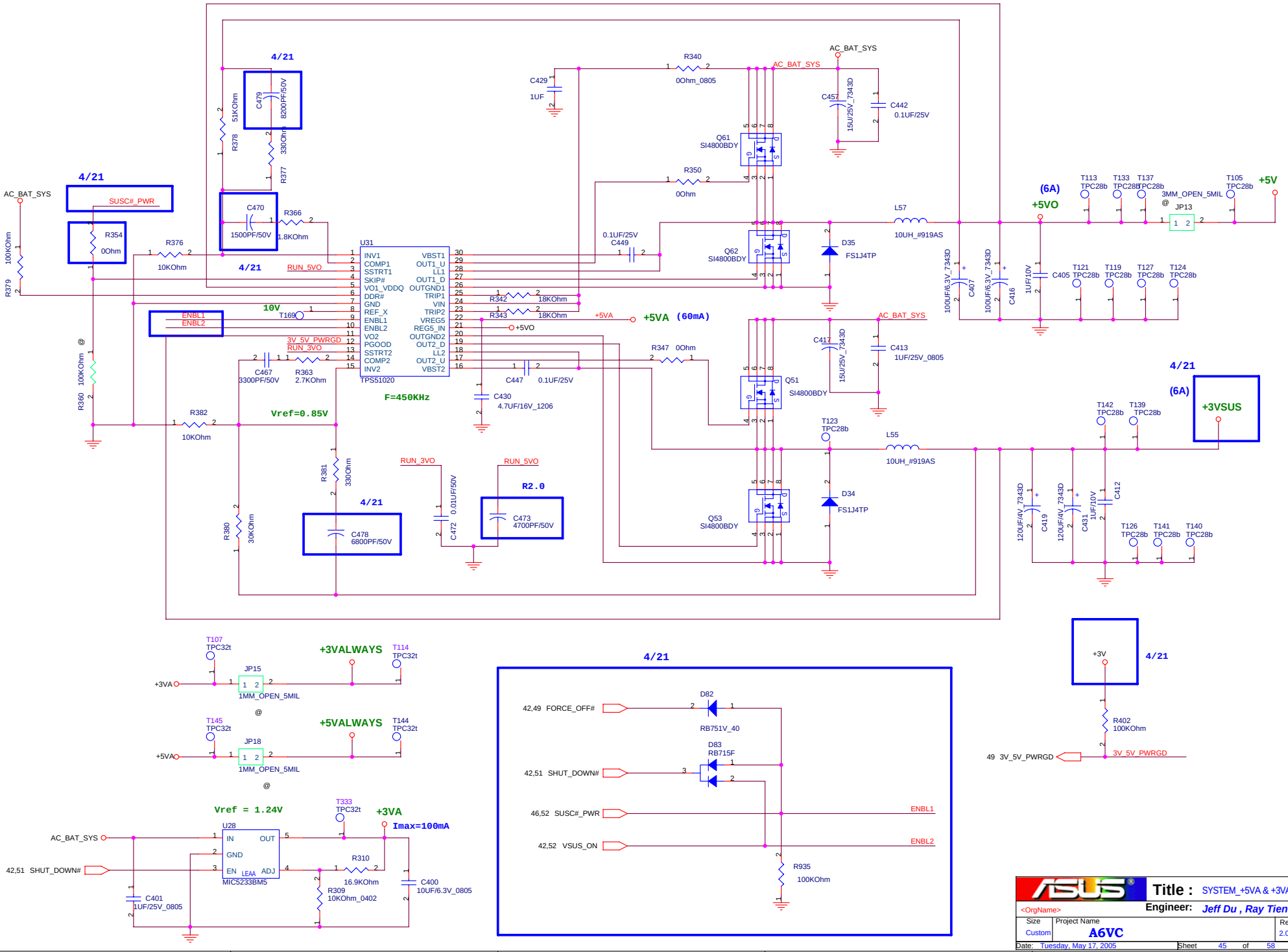
ASUS	Title : LED	
<OrgName>	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 41 of 58	


R2.0
5/4
R1.1
R1.1
05/03/07
R2.2
Without Battery & Pull out Adapter
--> To Reset SB
Adaptor IN
Title : POWER SEQUENCE(1)
Engineer: Mark Lin
A6VC
Date: Tuesday, May 17, 2005
Sheet 42 of 58

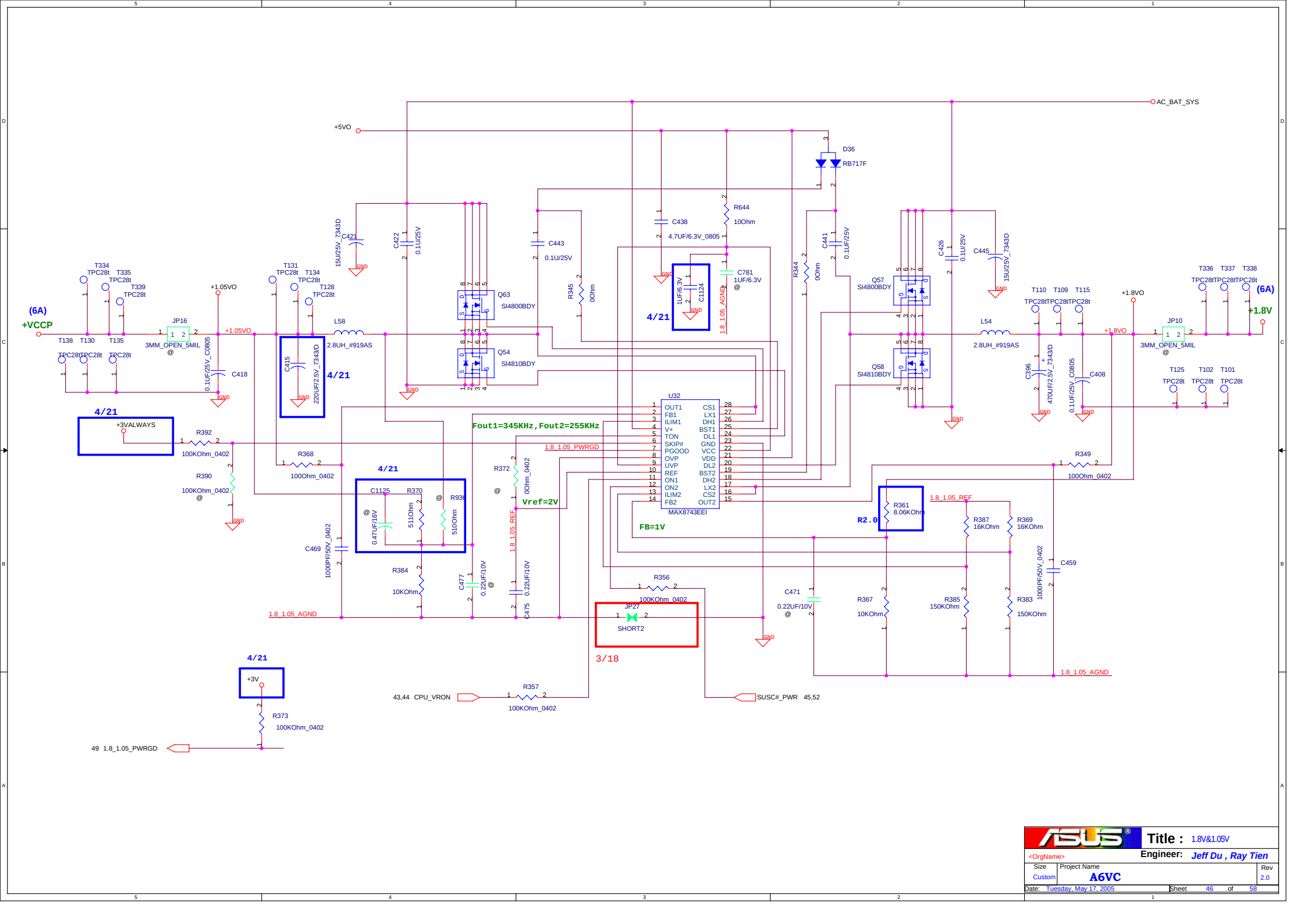


<OrgName>	Title : POWER SEQ (2)	
	Engineer: Mark Lin	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 43 of 58	

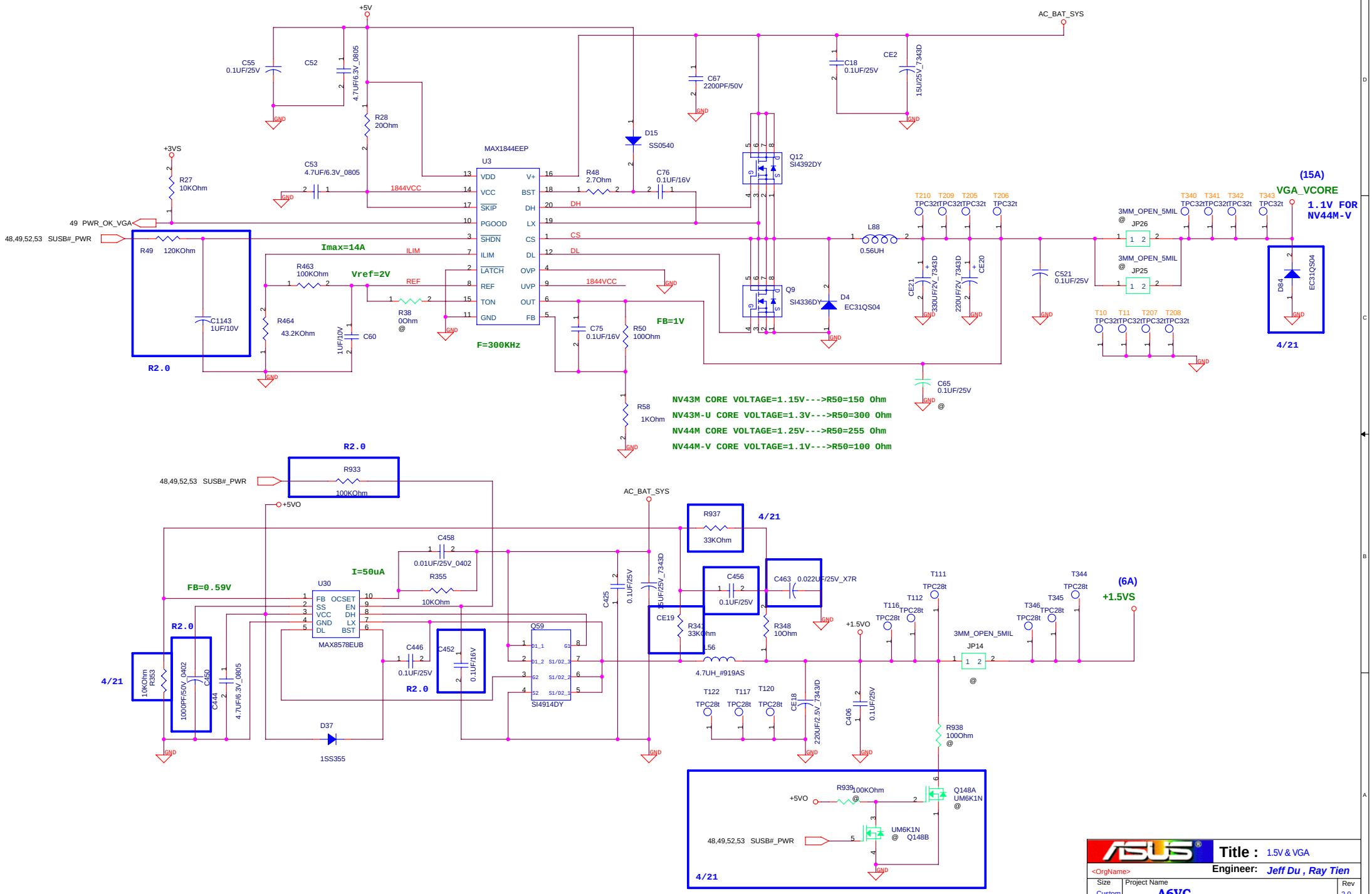

Pentium M Processor 770
VID 5 4 3 2 1 0
1.372V 0 1 0 1 0 1
0.988V 1 0 1 1 0 1
MAX1987ETM
U13
F=300KHz
CURRENT LIMIT=25.5A
0.748V
1.14V ~ 1.26V
0.7654V
OFFSET=-1.2%
+VCORE (25A)
NORMAL OPERATION
-->DPRSLPVR=L --> R(TIME)=9.77K Ohm
--> CLK_EN#=L
SUSPEND OPERATION
-->DPRSLPVR=H --> R(TIME)=28K Ohm
--> CLK_EN#=L
For C4 fast exit event
4/21
Title : VCORE
Engineer: Jeff Du , Ray Tien
A6VC
Tuesday, May 17, 2005



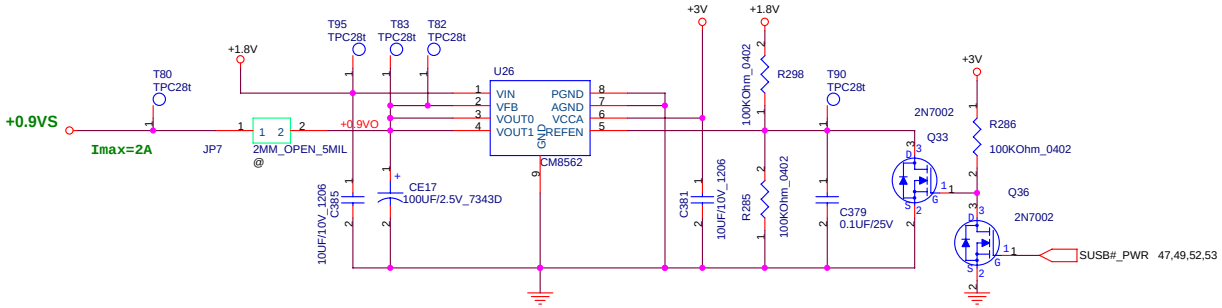
ASUS	Title :	SYSTEM_+5VA & +3VA	
<OrgName>	Engineer:	Jeff Du , Ray Tien	
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 45 of 58		

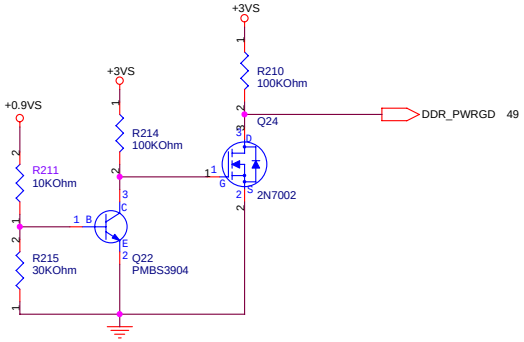


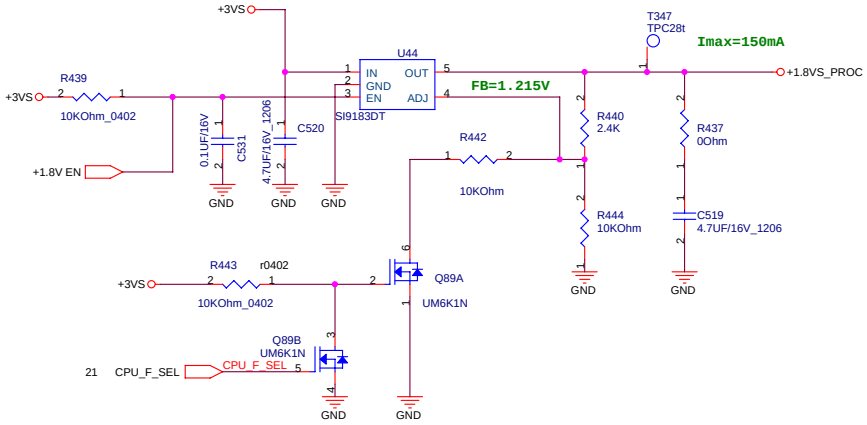
Title : 1.8V&1.05V			
<OrgName>	Engineer: Jeff Du , Ray Tien		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 46 of 58		



Title : 1.5V & VGA		
<OrgName>	Engineer: Jeff Du , Ray Tien	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 47 of 58	



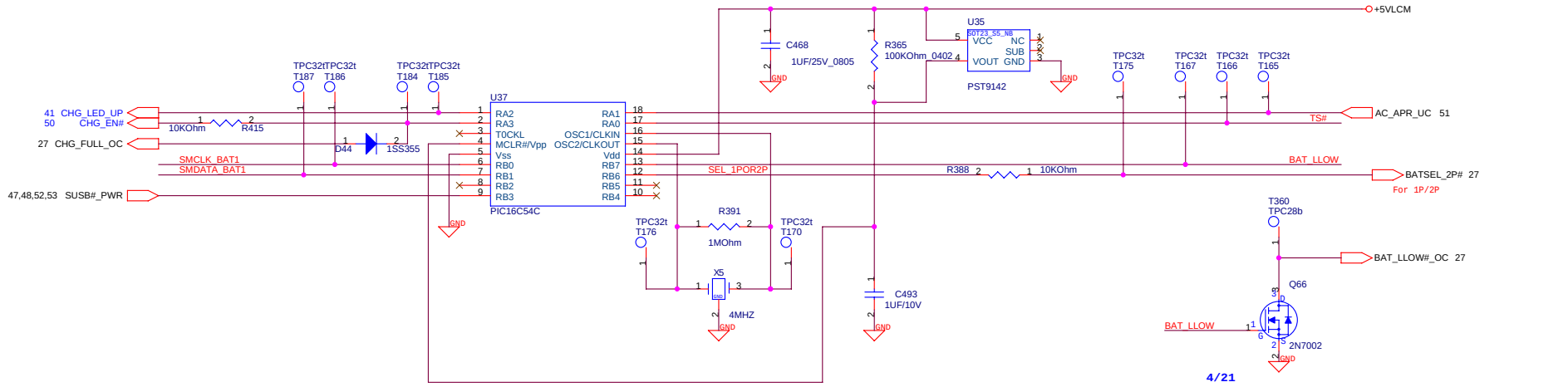




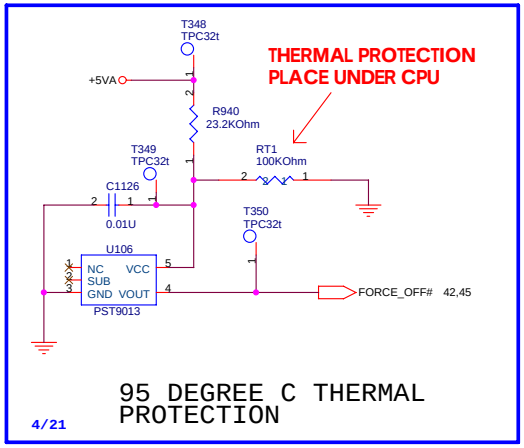
CPU_F_SEL-->H, OUT=1.5V (FSB=533MHz)

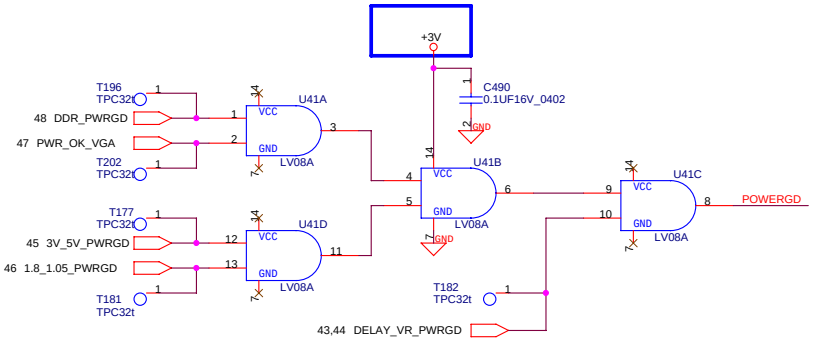
CPU_F_SEL-->L, OUT=1.8V (FSB=400MHz)

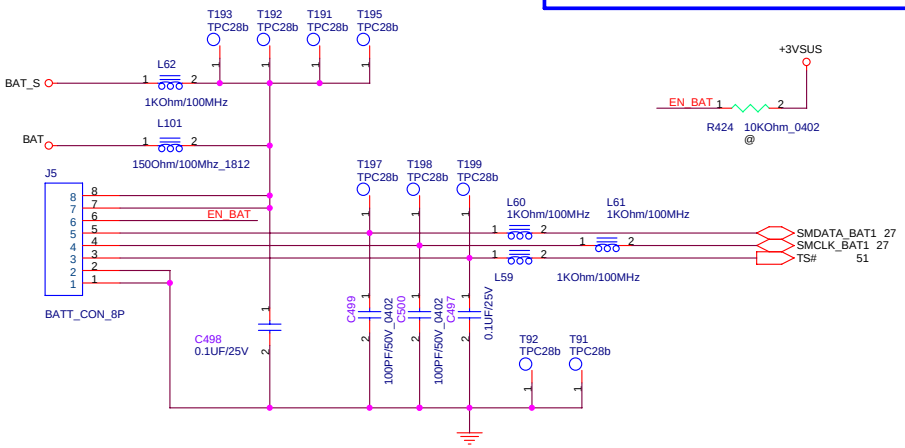
ASUS	Title : 1.5VA & +0.9VS	
<OrgName>	Engineer: Jeff Du , Ray Tien	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 48 of 58	

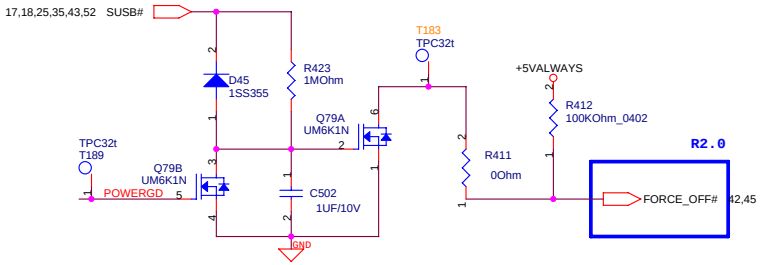


4/21

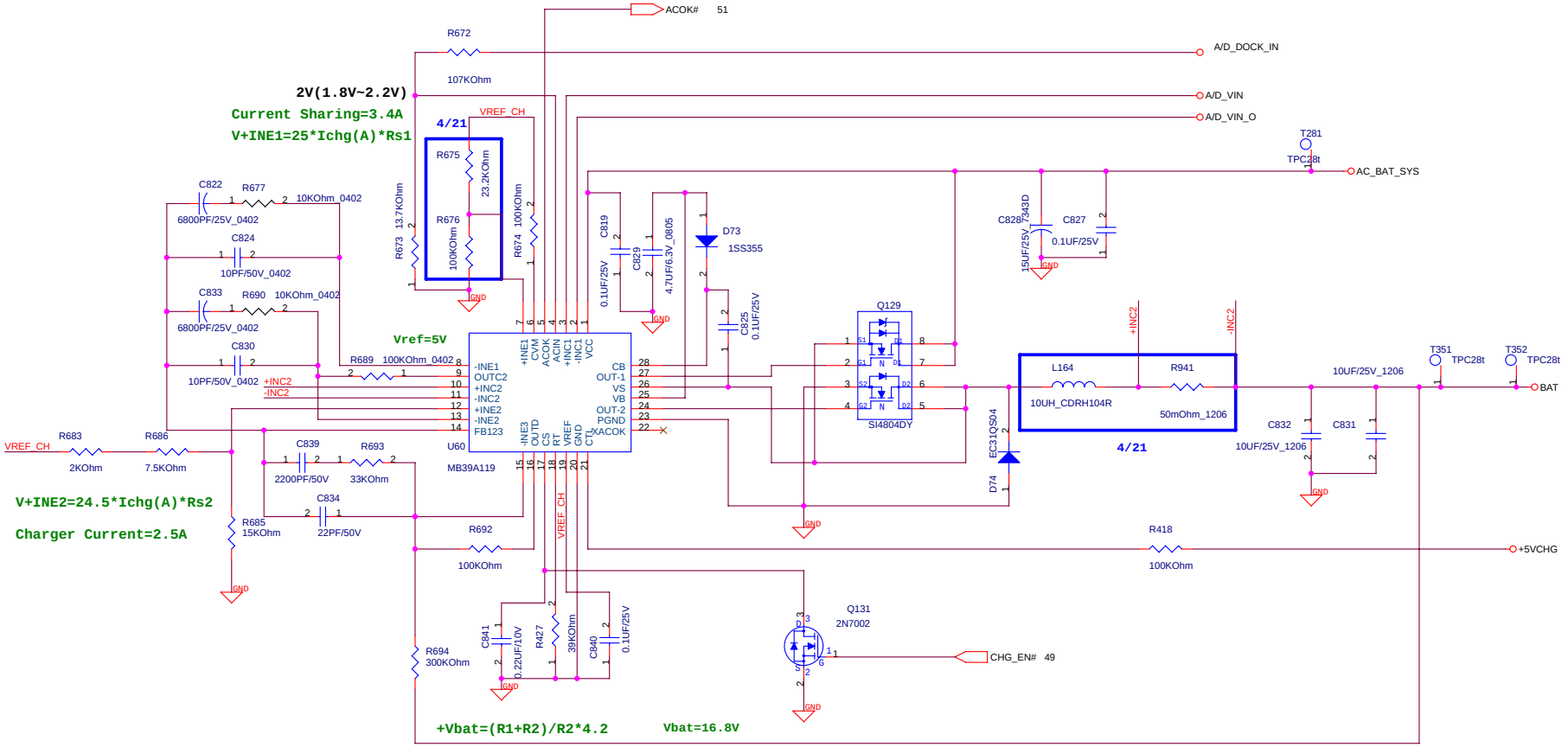




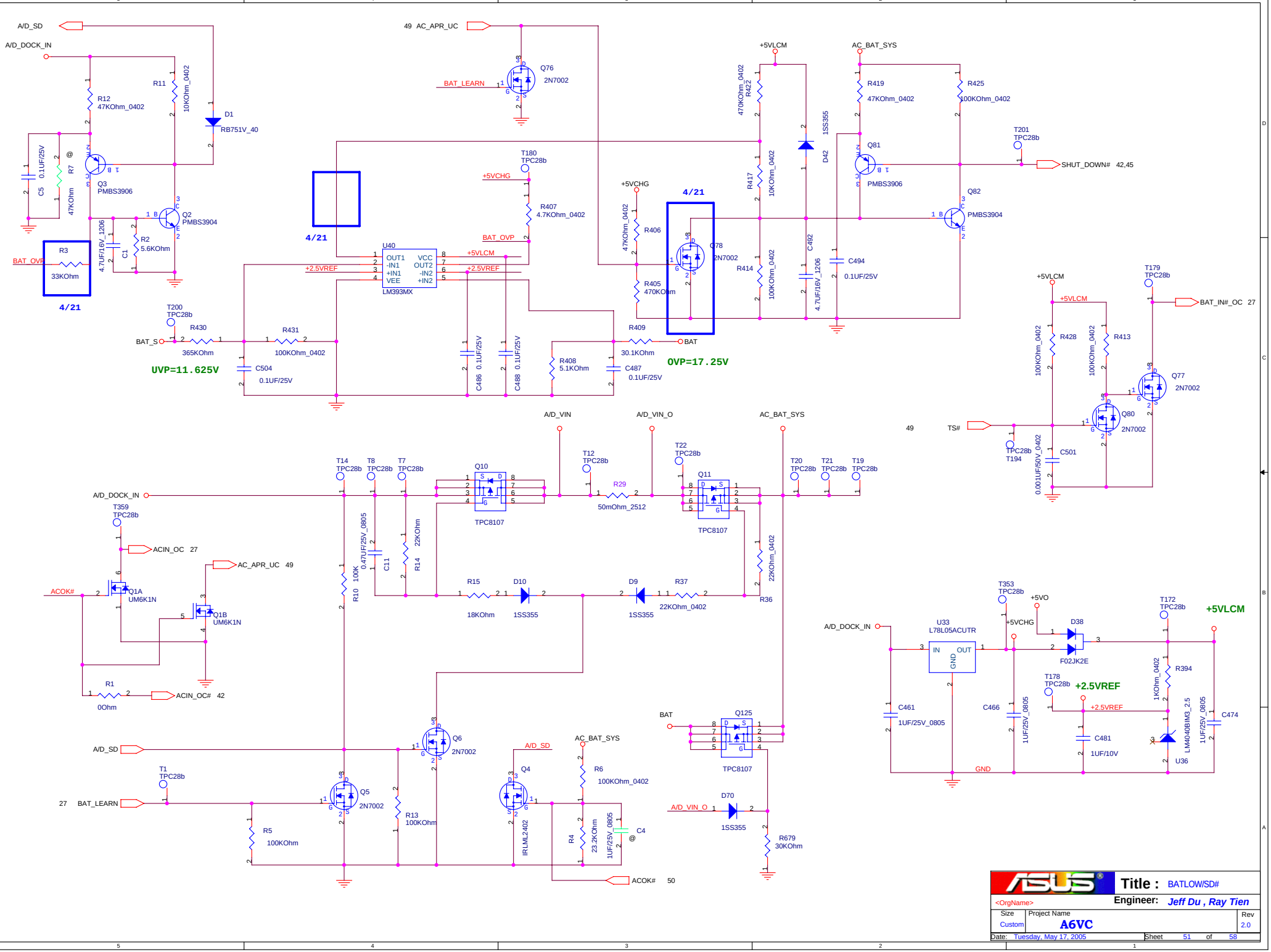




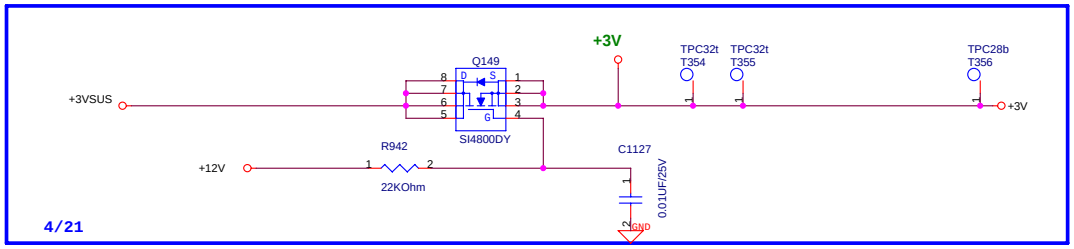
ASUS	Title : BAT CONNECT		
<OrgName>	Engineer: Jeff Du , Ray Tien		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 49 of 58		

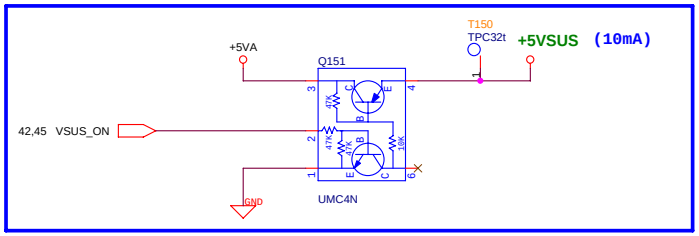


Title : CHARGE		
<OrgName>	Engineer: Jeff Du , Ray Tien	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 50 of 58	

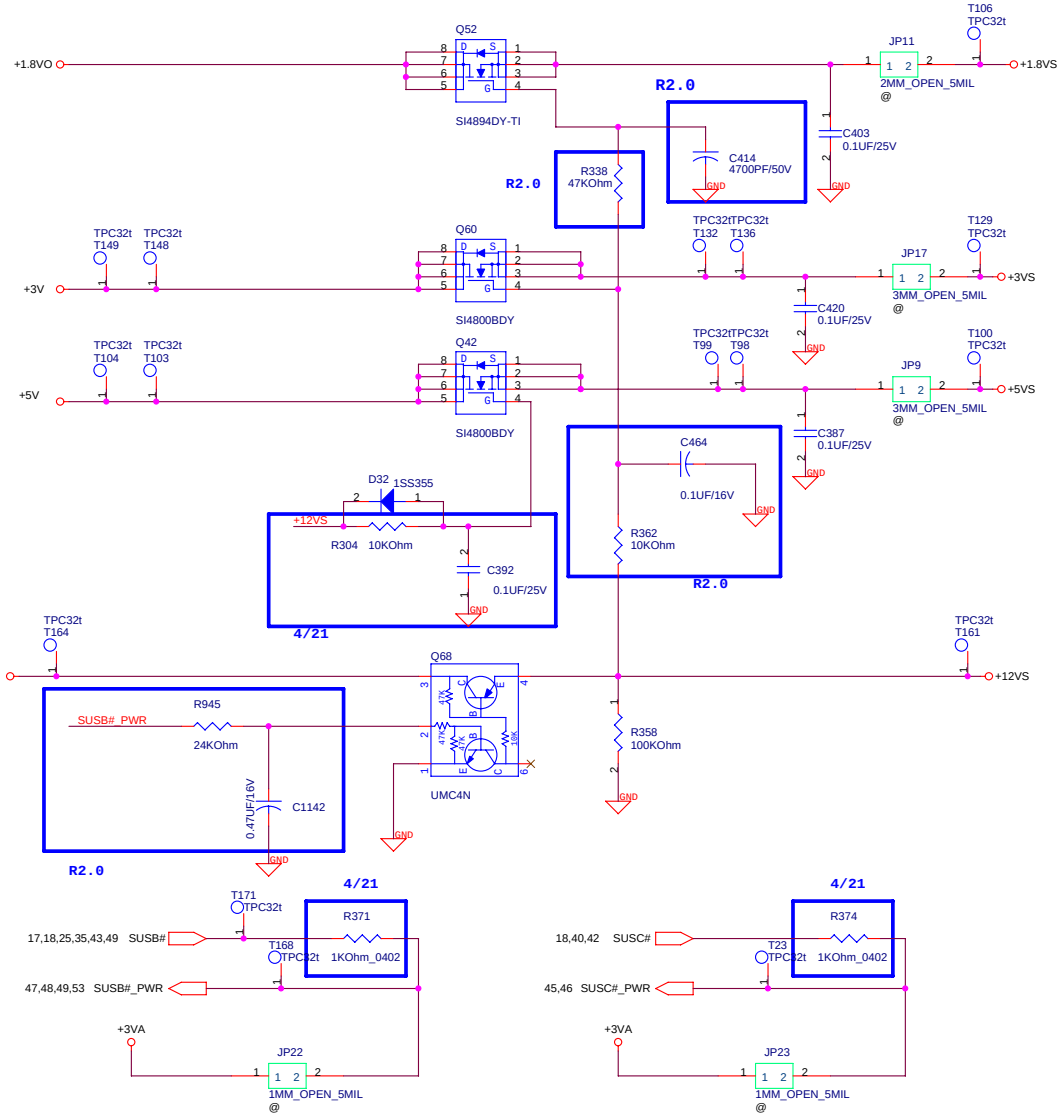


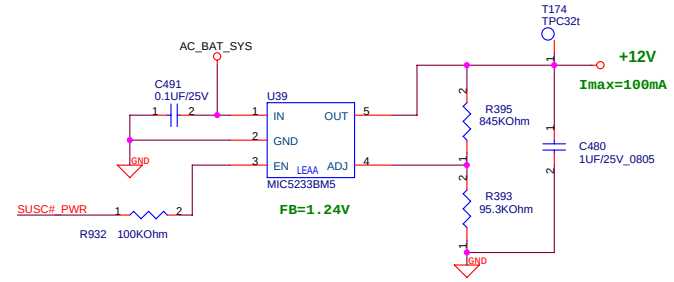
Title :	BATLOW/SD#	
<OrgName>	Engineer:	Jeff Du , Ray Tien
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 51 of 58	

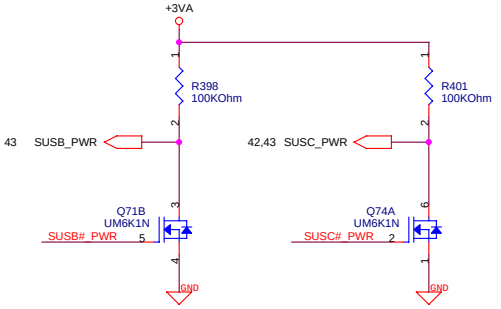




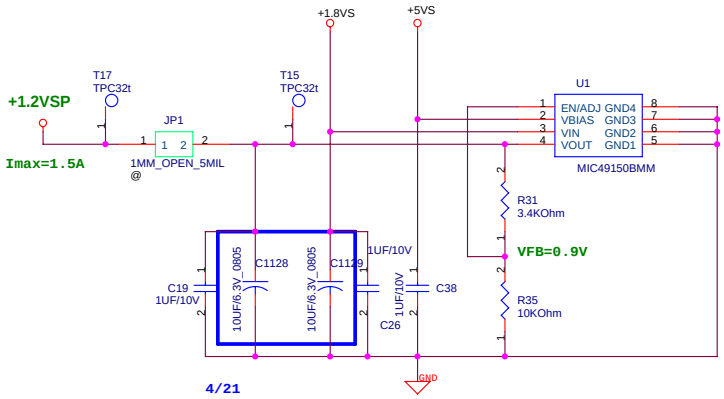
4/21

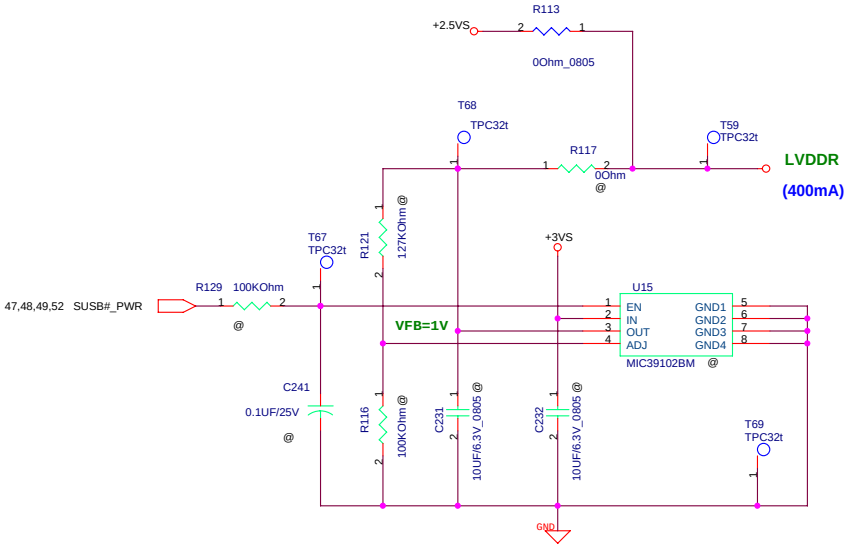




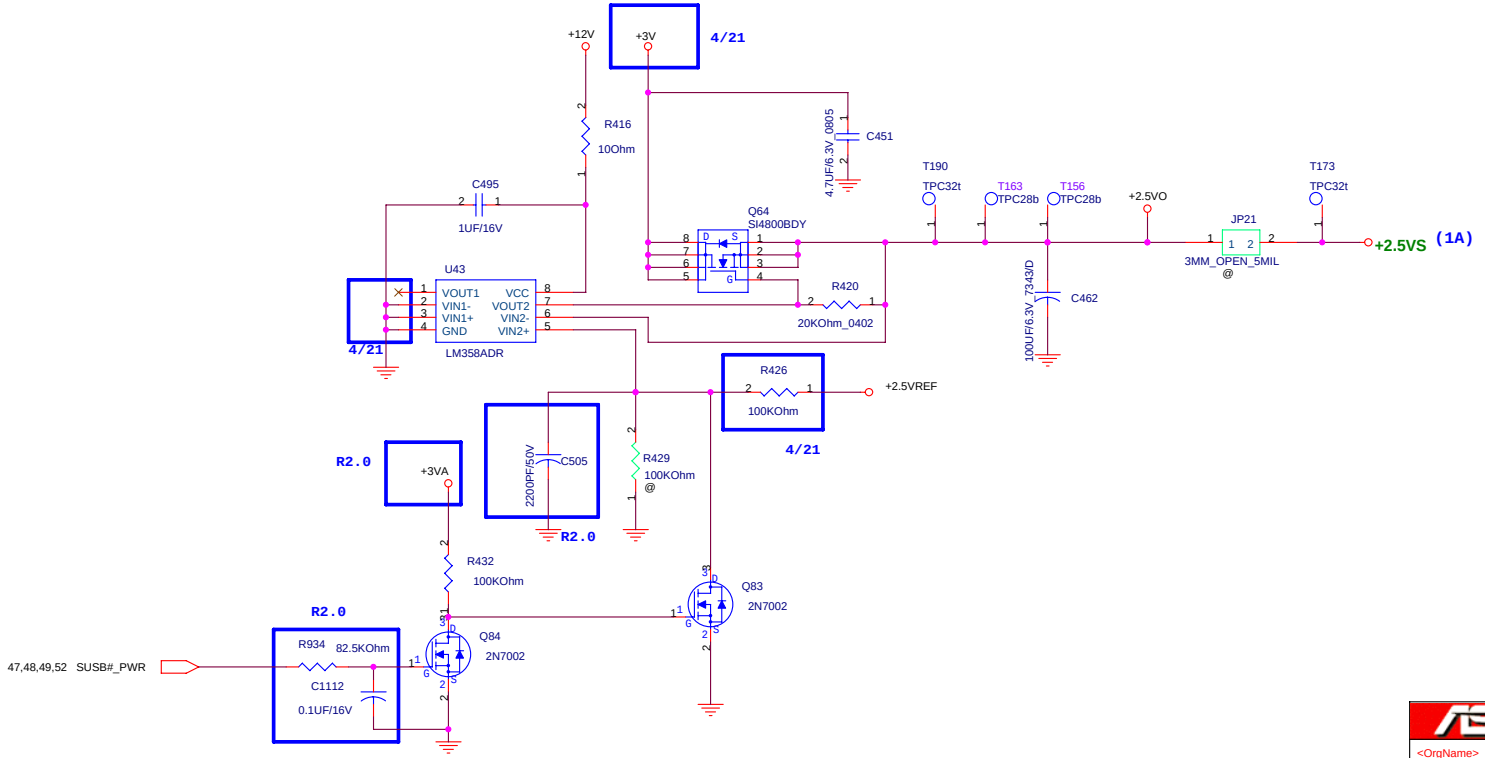


ASUS	Title : LOAD SWITCH		
<OrgName>	Engineer: Jeff Du , Ray Tien		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 52 of 58		

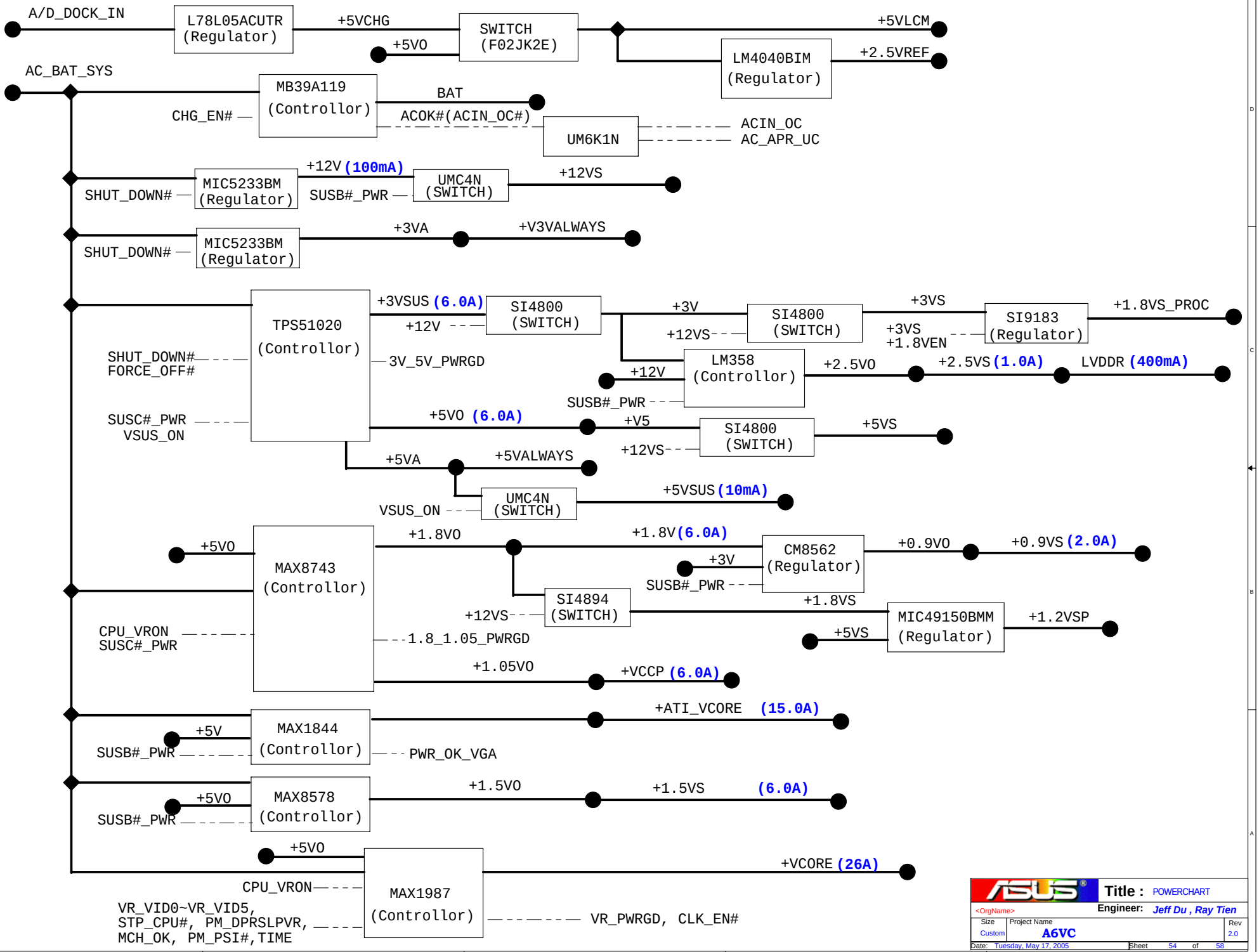




VGA PART



ASUS	Title :	VGA_PART & 2.5V
<OrgName>	Engineer:	Jeff Du , Ray Tien
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 53 of 58	



Title : POWERCHART		
<OrgName>	Engineer: Jeff Du , Ray Tien	
Size: Custom	Project Name: A6VC	Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 54 of 58	

VRAM I/F Channel A

NV44M-V / 43M

U100B

57 NVFBA_D[0..31]

NVFBA_D0 N27 FBAD0
NVFBA_D1 M27 FBAD1
NVFBA_D2 N28 FBAD2
NVFBA_D3 L29 FBAD3
NVFBA_D4 K27 FBAD4
NVFBA_D5 K28 FBAD5
NVFBA_D6 J29 FBAD6
NVFBA_D7 J28 FBAD7
NVFBA_D8 P30 FBAD8
NVFBA_D9 N31 FBAD9
NVFBA_D10 N30 FBAD10
NVFBA_D11 N32 FBAD11
NVFBA_D12 L31 FBAD12
NVFBA_D13 L30 FBAD13
NVFBA_D14 J30 FBAD14
NVFBA_D15 L32 FBAD15
NVFBA_D16 H30 FBAD16
NVFBA_D17 K30 FBAD17
NVFBA_D18 H31 FBAD18
NVFBA_D19 E30 FBAD19
NVFBA_D20 H32 FBAD20
NVFBA_D21 E31 FBAD21
NVFBA_D22 D30 FBAD22
NVFBA_D23 E30 FBAD23
NVFBA_D24 H28 FBAD24
NVFBA_D25 H29 FBAD25
NVFBA_D26 E29 FBAD26
NVFBA_D27 J27 FBAD27
NVFBA_D28 F27 FBAD28
NVFBA_D29 E27 FBAD29
NVFBA_D30 E28 FBAD30
NVFBA_D31 F28 FBAD31

57 NVFBA_D[32..63]

NVFBA_D32 AD29 FBAD32
NVFBA_D33 AE29 FBAD33
NVFBA_D34 AD28 FBAD34
NVFBA_D35 AC28 FBAD35
NVFBA_D36 AB29 FBAD36
NVFBA_D37 AA30 FBAD37
NVFBA_D38 Y28 FBAD38
NVFBA_D39 AB30 FBAD39
NVFBA_D40 AM30 FBAD40
NVFBA_D41 AF30 FBAD41
NVFBA_D42 AJ31 FBAD42
NVFBA_D43 AJ30 FBAD43
NVFBA_D44 AJ32 FBAD44
NVFBA_D45 AK29 FBAD45
NVFBA_D46 AM31 FBAD46
NVFBA_D47 AL30 FBAD47
NVFBA_D48 AE32 FBAD48
NVFBA_D49 AE30 FBAD49
NVFBA_D50 AE31 FBAD50
NVFBA_D51 AD30 FBAD51
NVFBA_D52 AC31 FBAD52
NVFBA_D53 AC32 FBAD53
NVFBA_D54 AB32 FBAD54
NVFBA_D55 AB31 FBAD55
NVFBA_D56 AG27 FBAD56
NVFBA_D57 AE28 FBAD57
NVFBA_D58 AH28 FBAD58
NVFBA_D59 AG28 FBAD59
NVFBA_D60 AG29 FBAD60
NVFBA_D61 AD27 FBAD61
NVFBA_D62 AE27 FBAD62
NVFBA_D63 AE28 FBAD63

57 NVFBA_DQM0 NVFBA_DQM0 M29 FBADQM0
57 NVFBA_DQM1 NVFBA_DQM1 M30 FBADQM1
57 NVFBA_DQM2 NVFBA_DQM2 G30 FBADQM2
57 NVFBA_DQM3 NVFBA_DQM3 F29 FBADQM3
57 NVFBA_DQM4 NVFBA_DQM4 AA29 FBADQM4
57 NVFBA_DQM5 NVFBA_DQM5 AK30 FBADQM5
57 NVFBA_DQM6 NVFBA_DQM6 AC30 FBADQM6
57 NVFBA_DQM7 NVFBA_DQM7 AG30 FBADQM7

57 NVFBA_DQS0 NVFBA_DQS0 L28 FBADQS_WP0
57 NVFBA_DQS1 NVFBA_DQS1 K31 FBADQS_WP1
57 NVFBA_DQS2 NVFBA_DQS2 G32 FBADQS_WP2
57 NVFBA_DQS3 NVFBA_DQS3 G28 FBADQS_WP3
57 NVFBA_DQS4 NVFBA_DQS4 AB28 FBADQS_WP4
57 NVFBA_DQS5 NVFBA_DQS5 AL32 FBADQS_WP5
57 NVFBA_DQS6 NVFBA_DQS6 AE32 FBADQS_WP6
57 NVFBA_DQS7 NVFBA_DQS7 AH30 FBADQS_WP7

M28 FBADQS_RN0
K32 FBADQS_RN1
G31 FBADQS_RN2
G27 FBADQS_RN3
AA28 FBADQS_RN4
AL31 FBADQS_RN5
AF31 FBADQS_RN6
AH29 FBADQS_RN7

MEM_VDD

UNMOUNT
R890 10KOhm 1% C1011 0.022uF/25V
NVFBA_VREF
R891 10KOhm 1% C1012 0.022uF/25V
GND GND

NVFBA_VREF F32 FB_VREF1

FBVDD_0 A12
FBVDD_1 A15
FBVDD_2 A18
FBVDD_3 A21
FBVDD_4 A24
FBVDD_5 A27
FBVDD_6 A3
FBVDD_7 A30
FBVDD_8 A6
FBVDD_9 A9
FBVDD_10 AA32
FBVDD_11 AD32
FBVDD_12 AG32
FBVDD_13 AK32
FBVDD_14 C32
FBVDD_15 F32
FBVDD_16 J32
FBVDD_17 M32
FBVDD_18 R32
FBVDD_19 V32

C975 0.022uF/25V C976 0.022uF/25V C977 0.022uF/25V C978 0.022uF/25V C979 0.022uF/25V C980 1uF/6.3V C981 0.022uF/25V C982 4.7uF/6.3V
GND

VDD--1.8V +/-2% Imax= 1.4A(NV43M-U 400M/350M)
VDD--1.8V +/-2% Imax= 1.3A(NV43M 375M/300M)

C983 4700PF/25V C984 0.022uF/25V C985 0.1uF/10V C986 0.1uF/10V C987 4700PF/25V C988 0.1uF/10V C989 0.022uF/25V C990 0.022uF/25V
GND

FBVDDQ_0 AA25
FBVDDQ_1 AA26
FBVDDQ_2 AB25
FBVDDQ_3 AB26
FBVDDQ_4 G11
FBVDDQ_5 G12
FBVDDQ_6 G15
FBVDDQ_7 G18
FBVDDQ_8 G21
FBVDDQ_9 G22
FBVDDQ_10 H11
FBVDDQ_11 H12
FBVDDQ_12 H15
FBVDDQ_13 H18
FBVDDQ_14 H21
FBVDDQ_15 H22
FBVDDQ_16 L25
FBVDDQ_17 L26
FBVDDQ_18 M25
FBVDDQ_19 M26
FBVDDQ_20 R25
FBVDDQ_21 R26
FBVDDQ_22 V25
FBVDDQ_23 V26

C991 4700PF/25V C992 0.022uF/25V C993 0.1uF/10V C994 0.1uF/10V C995 4700PF/25V C996 0.1uF/10V C997 4.7UF/6.3V C998 4.7UF/6.3V
GND

VDDQ--1.8V +/-2% Imax= 1.1A(NV43M-U 400M/350M)
VDDQ--1.8V +/-2% Imax= 1.0A(NV43M 375M/300M)

C999 0.022uF/25V C1000 0.1uF/10V C1001 4700PF/25V C1002 0.022uF/25V C1003 0.1uF/10V C1004 0.1uF/10V C1005 0.022uF/25V C1006 0.1uF/10V C1007 0.022uF/25V
GND

NVFBA_A[0..11] 57

FBA_CMD0 P32 NVFBA_A3
FBA_CMD1 U27 NVFBA_A0
FBA_CMD2 P31 NVFBA_A2
FBA_CMD3 U30 NVFBA_A1
FBA_CMD4 Y31 NVFBA_A3 NVFBB_A3 57
FBA_CMD5 W32 NVFBB_A4 NVFBB_A4 57
FBA_CMD6 W31 NVFBB_A5 NVFBB_A5 57
FBA_CMD7 T32 NVFBA_CS#1 NVFBA_CS#1 57
FBA_CMD8 V27 NVFBA_CS#0 NVFBA_CS#0 57
FBA_CMD9 T28 NVFBA_WE# NVFBA_WE# 57
FBA_CMD10 T31 NVFBA_BA0 NVFBA_BA0 57
FBA_CMD11 U32 NVFBA_CKE NVFBA_CKE 57
FBA_CMD12 W29 1 TPC28t T322
FBA_CMD13 W30 NVFBB_A2 NVFBB_A2 57
FBA_CMD14 T27 NVFBA_A12 NVFBA_A12 57
FBA_CMD15 V28 NVFBA_RAS# NVFBA_RAS# 57
FBA_CMD16 V30 NVFBA_A11
FBA_CMD17 U31 NVFBA_A10
FBA_CMD18 R27 NVFBA_BA1 NVFBA_BA1 57
FBA_CMD19 V29 NVFBA_A8
FBA_CMD20 T30 NVFBA_A9
FBA_CMD21 W28 NVFBA_A6
FBA_CMD22 R29 NVFBA_A5
FBA_CMD23 R30 NVFBA_A7
FBA_CMD24 P29 NVFBA_A4
FBA_CMD25 U28 NVFBA_CAS# NVFBA_CAS# 57
FBA_CMD26 Y32 NVFBA_A13 1 TPC28t T323

(FBA_CMD26 ONLY IN NV44)

FBA_CLK0 P28 NVFBA_CLK0 NVFBA_CLK0 57
FBA_CLK0* R28 NVFBA_CLK0# NVFBA_CLK0# 57
FBA_CLK1 Y27 NVFBA_CLK1 NVFBA_CLK1 57
FBA_CLK1* AA27 NVFBA_CLK1# NVFBA_CLK1# 57

3/25

+1.8VS MEM_VDD
JP4 1 2 1MM_OPEN_5MIL /
JP30 1 2 1MM_OPEN_5MIL /
JP3 1 2 1MM_OPEN_5MIL /

3/25

MEM_VDD
C1118 0.1uF/10V / C1119 0.1uF/10V /
GND

RFU2 Y30
RFU3 AC26
FBA_DEBUG AC27 1 TPC28t T324
FBA_REFCLK D32 NVFBA_REFCLK 1 TPC28t T325
FBA_REFCLKN D31 NVFBA_REFCLK# 1 TPC28t T326

FBA_PLLVDD 3.3V Imax= 15mA place close to balls
+3VS
L159 120Ohm/100Mhz
C1008 470PF/50V C1009 4700PF/25V C1010 4.7UF/6.3V
GND

FBA_PLLVDD G23 FBA_PLLVDD
FBA_PLLAVDD G25 FBA_PLLAVDD
FBA_PLLGND G24
GND

VGA_VCORE
FBA_PLLAVDD 1.2V Imax= 15mA
L160 120Ohm/100Mhz
C1013 470PF/50V C1014 4700PF/25V C1015 4.7UF/6.3V
GND

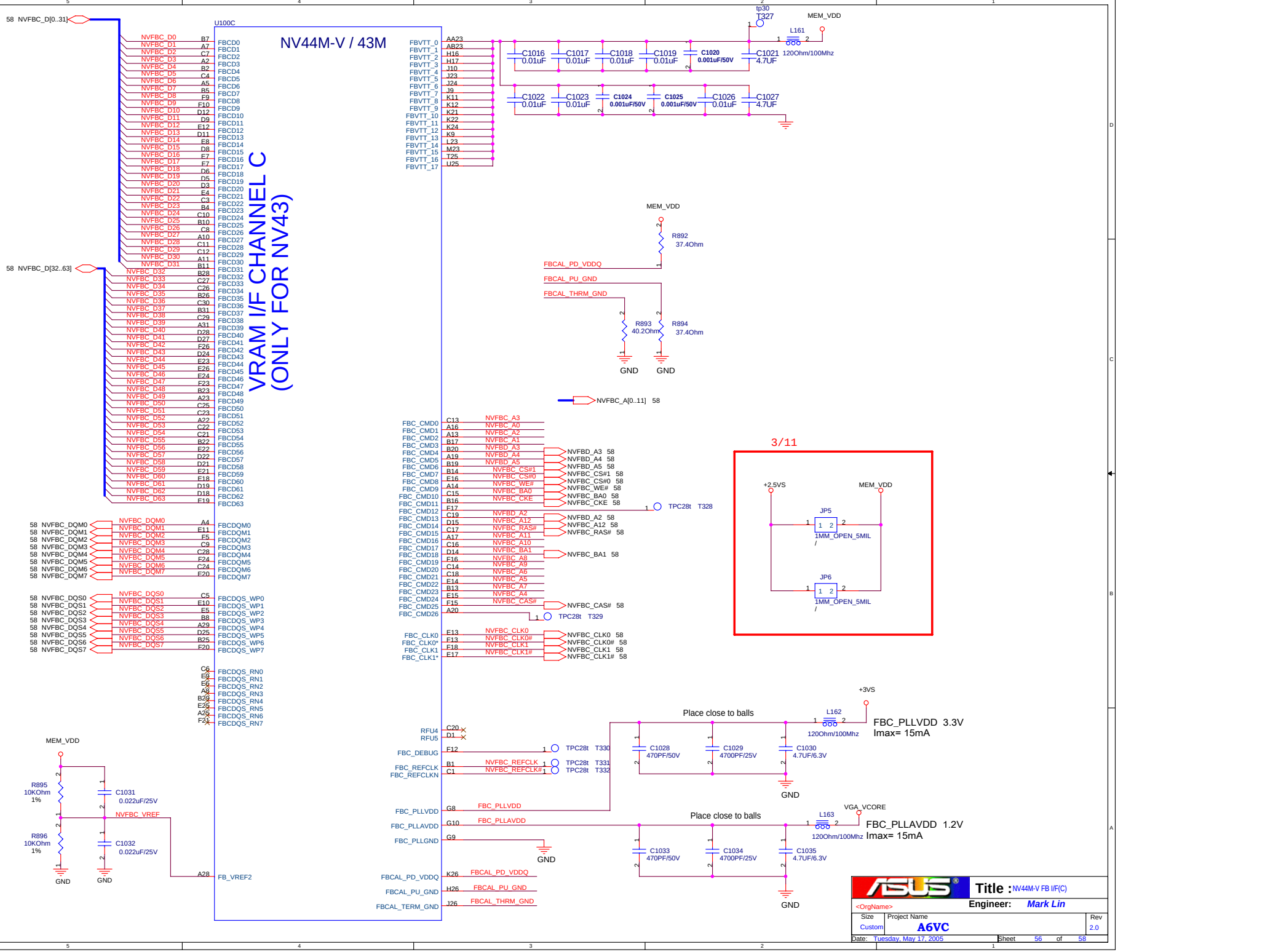
ASUS

Title : NV44M-V FB I/F(A)

<OrgName> Engineer: Mark Lin

Size	Project Name	Rev
Custom	A6VC	2.0

Date: Tuesday, May 17, 2005 Sheet 55 of 58


U100C
NV44M-V / 43M
VRAM I/F CHANNEL C
(ONLY FOR NV43)
58 NVFBC_D[0..31]
58 NVFBC_D[32..63]
NVFBC_D0 B7 FBCD0
NVFBC_D1 A7 FBCD1
NVFBC_D2 C7 FBCD2
NVFBC_D3 A2 FBCD3
NVFBC_D4 B2 FBCD4
NVFBC_D5 C4 FBCD5
NVFBC_D6 A5 FBCD6
NVFBC_D7 B5 FBCD7
NVFBC_D8 F9 FBCD8
NVFBC_D9 F10 FBCD9
NVFBC_D10 D12 FBCD10
NVFBC_D11 D9 FBCD11
NVFBC_D12 E12 FBCD12
NVFBC_D13 D11 FBCD13
NVFBC_D14 E8 FBCD14
NVFBC_D15 D8 FBCD15
NVFBC_D16 E7 FBCD16
NVFBC_D17 E7 FBCD17
NVFBC_D18 D6 FBCD18
NVFBC_D19 D5 FBCD19
NVFBC_D20 D3 FBCD20
NVFBC_D21 E4 FBCD21
NVFBC_D22 C3 FBCD22
NVFBC_D23 B4 FBCD23
NVFBC_D24 C10 FBCD24
NVFBC_D25 B10 FBCD25
NVFBC_D26 C9 FBCD26
NVFBC_D27 A10 FBCD27
NVFBC_D28 C11 FBCD28
NVFBC_D29 C12 FBCD29
NVFBC_D30 A11 FBCD30
NVFBC_D31 B11 FBCD31
NVFBC_D32 B28 FBCD32
NVFBC_D33 C27 FBCD33
NVFBC_D34 C26 FBCD34
NVFBC_D35 B26 FBCD35
NVFBC_D36 C30 FBCD36
NVFBC_D37 B31 FBCD37
NVFBC_D38 C29 FBCD38
NVFBC_D39 A31 FBCD39
NVFBC_D40 D28 FBCD40
NVFBC_D41 D27 FBCD41
NVFBC_D42 F26 FBCD42
NVFBC_D43 D24 FBCD43
NVFBC_D44 E23 FBCD44
NVFBC_D45 E26 FBCD45
NVFBC_D46 E24 FBCD46
NVFBC_D47 E23 FBCD47
NVFBC_D48 B23 FBCD48
NVFBC_D49 A23 FBCD49
NVFBC_D50 C25 FBCD50
NVFBC_D51 C23 FBCD51
NVFBC_D52 A22 FBCD52
NVFBC_D53 C22 FBCD53
NVFBC_D54 C21 FBCD54
NVFBC_D55 B22 FBCD55
NVFBC_D56 E22 FBCD56
NVFBC_D57 D22 FBCD57
NVFBC_D58 D21 FBCD58
NVFBC_D59 E21 FBCD59
NVFBC_D60 E18 FBCD60
NVFBC_D61 D19 FBCD61
NVFBC_D62 D18 FBCD62
NVFBC_D63 E19 FBCD63
58 NVFBC_DQM0 NVFBC_DQM0 A4 FBCDQM0
58 NVFBC_DQM1 NVFBC_DQM1 E11 FBCDQM1
58 NVFBC_DQM2 NVFBC_DQM2 E5 FBCDQM2
58 NVFBC_DQM3 NVFBC_DQM3 C9 FBCDQM3
58 NVFBC_DQM4 NVFBC_DQM4 C28 FBCDQM4
58 NVFBC_DQM5 NVFBC_DQM5 F24 FBCDQM5
58 NVFBC_DQM6 NVFBC_DQM6 C24 FBCDQM6
58 NVFBC_DQM7 NVFBC_DQM7 E20 FBCDQM7
58 NVFBC_DQS0 NVFBC_DQS0 C5 FBCDQS_WP0
58 NVFBC_DQS1 NVFBC_DQS1 E10 FBCDQS_WP1
58 NVFBC_DQS2 NVFBC_DQS2 E5 FBCDQS_WP2
58 NVFBC_DQS3 NVFBC_DQS3 B8 FBCDQS_WP3
58 NVFBC_DQS4 NVFBC_DQS4 A29 FBCDQS_WP4
58 NVFBC_DQS5 NVFBC_DQS5 D25 FBCDQS_WP5
58 NVFBC_DQS6 NVFBC_DQS6 B25 FBCDQS_WP6
58 NVFBC_DQS7 NVFBC_DQS7 F20 FBCDQS_WP7
C6 FBCDQS_RN0
E9 FBCDQS_RN1
E6 FBCDQS_RN2
A8 FBCDQS_RN3
B29 FBCDQS_RN4
E25 FBCDQS_RN5
A25 FBCDQS_RN6
F21 FBCDQS_RN7
MEM_VDD
R895 10KOhm 1%
R896 10KOhm 1%
C1031 0.022uF/25V
C1032 0.022uF/25V
NVFBC_VREF
GND
A28 FB_VREF2
FBVTT_0 AA23
FBVTT_1 AB23
FBVTT_2 H16
FBVTT_3 H17
FBVTT_4 J10
FBVTT_5 J23
FBVTT_6 J24
FBVTT_7 J9
FBVTT_8 K11
FBVTT_9 K12
FBVTT_10 K21
FBVTT_11 K22
FBVTT_12 K24
FBVTT_13 K9
FBVTT_14 L23
FBVTT_15 M23
FBVTT_16 T25
FBVTT_17 U25
C1016 0.01uF
C1017 0.01uF
C1018 0.01uF
C1019 0.01uF
C1020 0.001uF/50V
C1021 4.7UF
C1022 0.01uF
C1023 0.01uF
C1024 0.001uF/50V
C1025 0.001uF/50V
C1026 0.01uF
C1027 4.7UF
tp30
T327
MEM_VDD
L161 120Ohm/100Mhz
MEM_VDD
R892 37.4Ohm
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_THRM_GND
R893 40.2Ohm
R894 37.4Ohm
GND
GND
NVFBC_A[0..11] 58
FBC_CMD0 C13 NVFBC_A3
FBC_CMD1 A16 NVFBC_A0
FBC_CMD2 A13 NVFBC_A2
FBC_CMD3 B17 NVFBC_A1
FBC_CMD4 B20 NVFBD_A3
FBC_CMD5 A19 NVFBD_A4
FBC_CMD6 B19 NVFBD_A5
FBC_CMD7 B14 NVFBC_CS#1
FBC_CMD8 E16 NVFBC_CS#0
FBC_CMD9 A14 NVFBC_WE#
FBC_CMD10 C15 NVFBC_BA0
FBC_CMD11 B16 NVFBC_CKE
FBC_CMD12 F17
FBC_CMD13 C19 NVFBD_A2
FBC_CMD14 D15 NVFBC_A12
FBC_CMD15 C17 NVFBC_RAS#
FBC_CMD16 A17 NVFBC_A11
FBC_CMD17 C16 NVFBC_A10
FBC_CMD18 D14 NVFBC_BA1
FBC_CMD19 F16 NVFBC_A8
FBC_CMD20 C14 NVFBC_A9
FBC_CMD21 C18 NVFBC_A6
FBC_CMD22 E14 NVFBC_A5
FBC_CMD23 B13 NVFBC_A7
FBC_CMD24 E15 NVFBC_A4
FBC_CMD25 F15 NVFBC_CAS#
FBC_CMD26 A20
NVFBD_A3 58
NVFBD_A4 58
NVFBD_A5 58
NVFBC_CS#1 58
NVFBC_CS#0 58
NVFBC_WE# 58
NVFBC_BA0 58
NVFBC_CKE 58
TPC28t T328
NVFBD_A2 58
NVFBC_A12 58
NVFBC_RAS# 58
NVFBC_A11
NVFBC_BA1 58
NVFBC_CAS# 58
TPC28t T329
FBC_CLK0 E13 NVFBC_CLK0
FBC_CLK0* F13 NVFBC_CLK0#
FBC_CLK1 F18 NVFBC_CLK1
FBC_CLK1* E17 NVFBC_CLK1#
NVFBC_CLK0 58
NVFBC_CLK0# 58
NVFBC_CLK1 58
NVFBC_CLK1# 58
3/11
+2.5VS
MEM_VDD
JP5
1MM_OPEN_5MIL
JP6
1MM_OPEN_5MIL
RFU4 C20
RFU5 D1
FBC_DEBUG F12
TPC28t T330
FBC_REFCLK B1 NVFBC_REFCLK
FBC_REFCLKN C1 NVFBC_REFCLK#
TPC28t T331
TPC28t T332
FBC_PLLVDD G8 FBC_PLLVDD
FBC_PLLAVDD G10 FBC_PLLAVDD
FBC_PLLGND G9
GND
FBCAL_PD_VDDQ K26 FBCAL_PD_VDDQ
FBCAL_PU_GND H26 FBCAL_PU_GND
FBCAL_TERM_GND J26 FBCAL_THRM_GND
Place close to balls
+3VS
L162 120Ohm/100Mhz
FBC_PLLVDD 3.3V
Imax= 15mA
C1028 470PF/50V
C1029 4700PF/25V
C1030 4.7UF/6.3V
GND
Place close to balls
VGA_VCORE
L163 120Ohm/100Mhz
FBC_PLLAVDD 1.2V
Imax= 15mA
C1033 470PF/50V
C1034 4700PF/25V
C1035 4.7UF/6.3V
GND
Title : NV44M-V FB I/F(C)
<OrgName>
Engineer: Mark Lin
Size Custom
Project Name A6VC
Rev 2.0
Date: Tuesday, May 17, 2005
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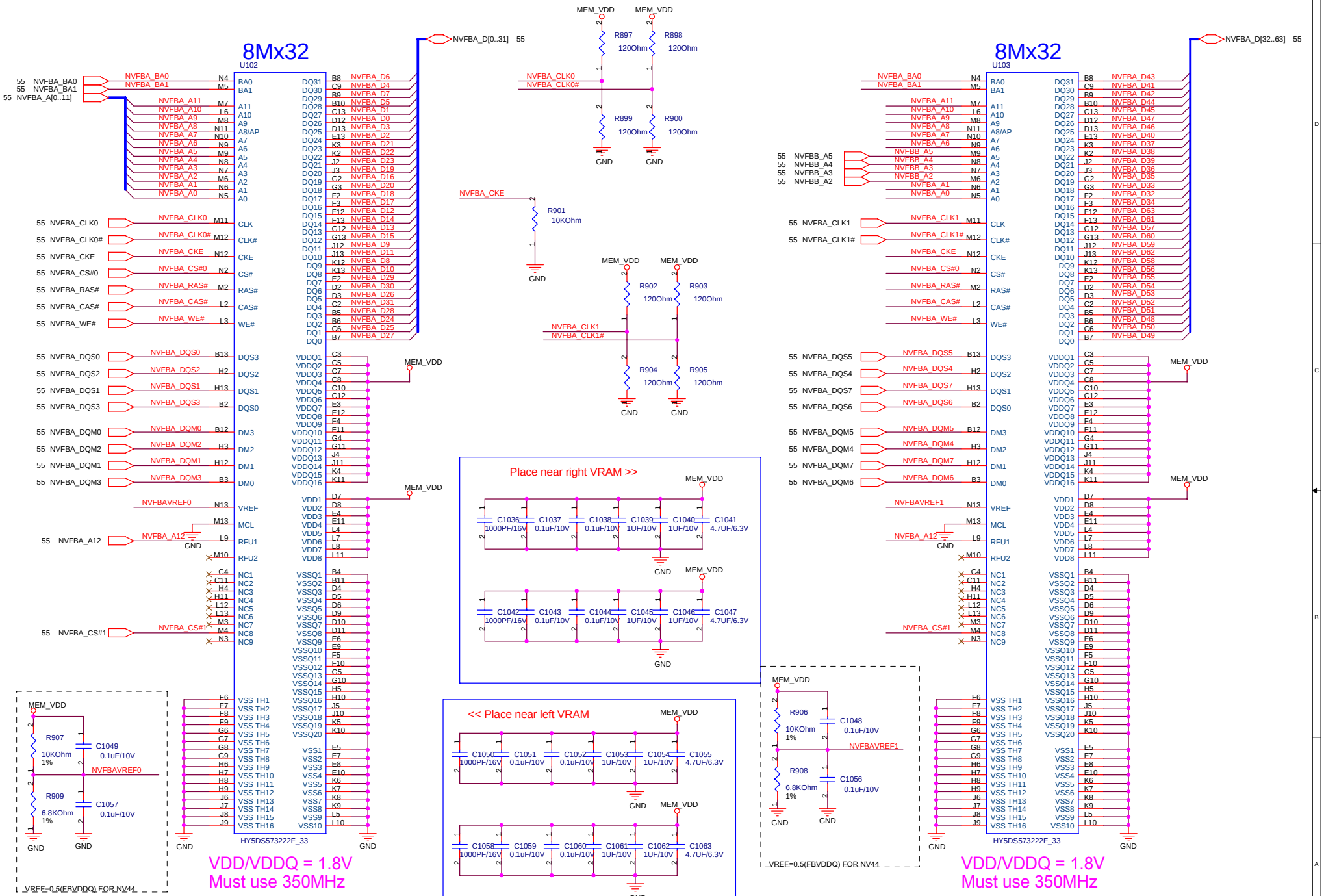
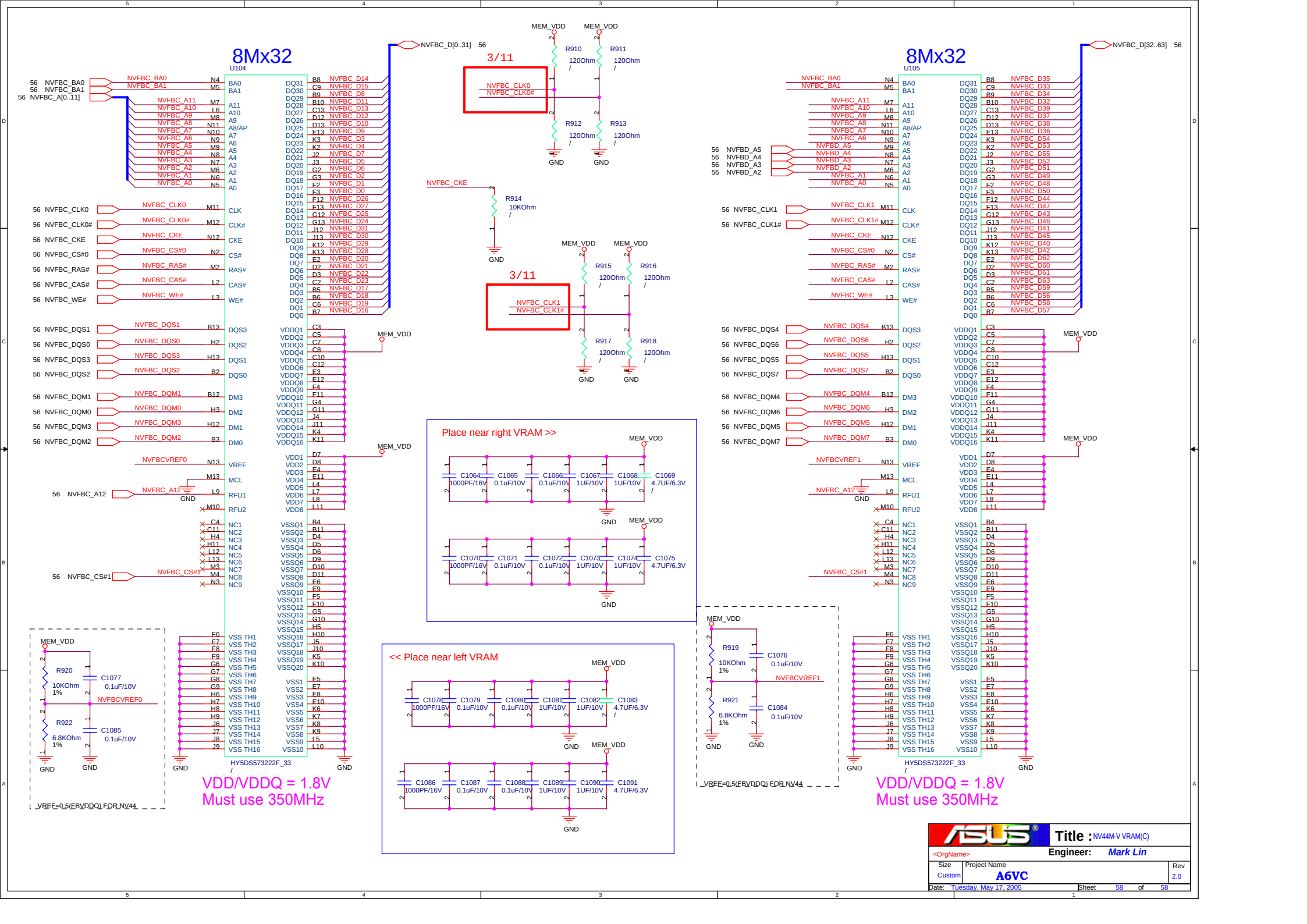


Title : NV44M-V VRAM(A)			
<OrgName>	Engineer: Mark Lin		
Size: Custom	Project Name: A6VC		Rev: 2.0
Date: Tuesday, May 17, 2005	Sheet 57 of 58		


8Mx32
U104
8Mx32
U105
3/11
3/11
Place near right VRAM >>
<< Place near left VRAM
VDD/VDDQ = 1.8V
Must use 350MHz
VDD/VDDQ = 1.8V
Must use 350MHz
VREF=0.5(FBVDDQ) FOR NV44
VREF=0.5(FBVDDQ) FOR NV44
HY5DS573222F_33
HY5DS573222F_33
Title : NV44M-V VRAM(C)
Engineer: Mark Lin
Project Name
A6VC
Size
Custom
Rev
2.0
Date: Tuesday, May 17, 2005
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