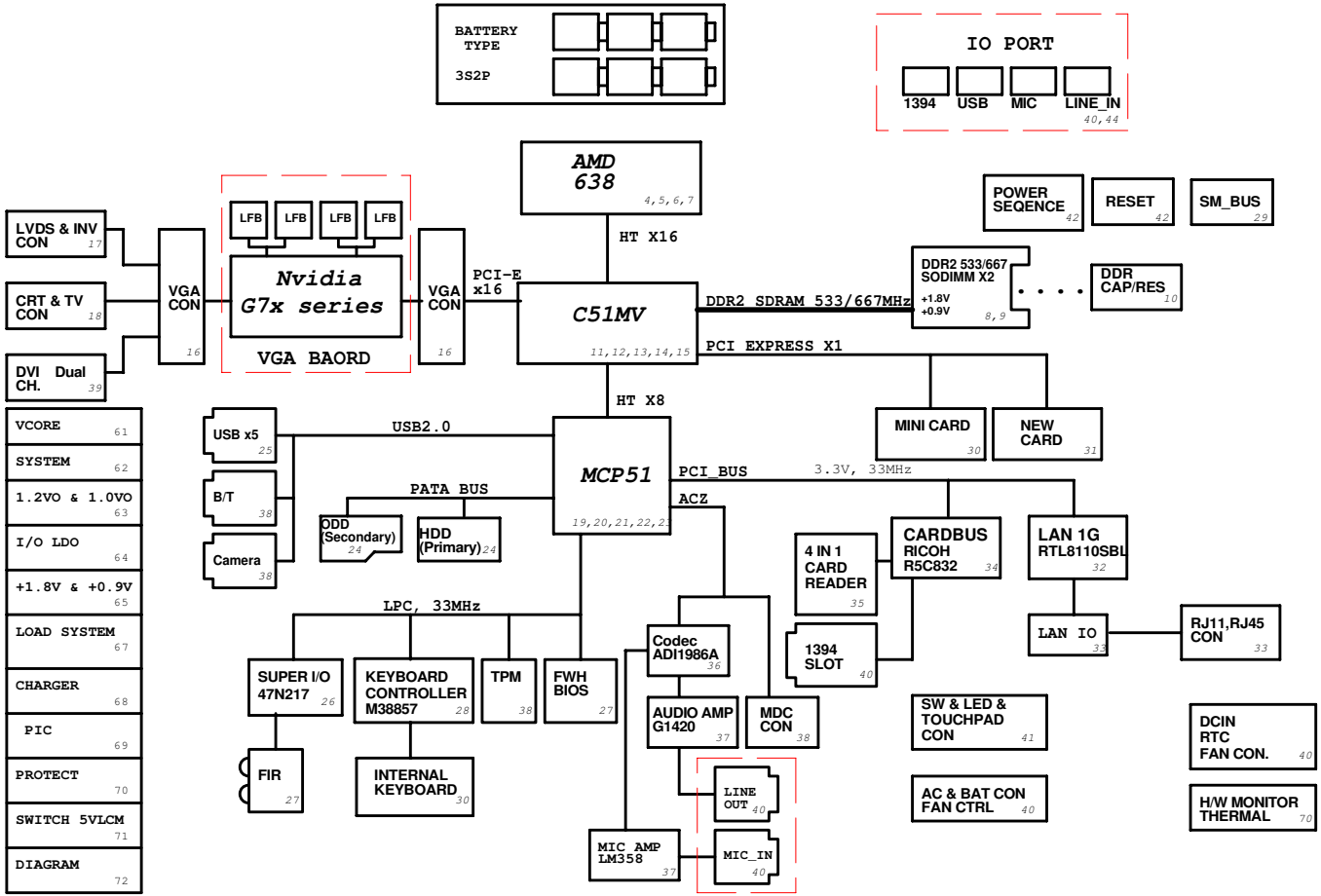
A8T/M SCHEMATIC R2.1

PAGE	Content
	SYSTEM PAGE REF.
4	AMD S1 CPU--HT
5	AMD S1 CPU--CNTL
6	AMD S1 CPU--DDR2
7	AMD S1 CPU--PWR/GND
8	DDR2 SO-DIMM_0
9	DDR2 SO-DIMM_1
10	DDR2 ADDRESS TERMINATION
11	C51M--HT TO CPU
12	C51M--HT TO MCP
13	C51M--PCI-E
14	C51M--CRT & LVDS
15	C51M--PWR/GND
16	VGA CONN
17	LVDS & INVERTER CONN
18	CRT & TV_OUT
19	MCP51--HT
20	MCP51--PCI
21	MCP51--IDE
22	MCP51--USB & HDA & GPIO
23	MCP51--PWR/GND
24	HDD & CD-ROM CONN
25	USB PORTS
26	SUPER I/O LPC47N217
27	BIOS & FIR
28	KBC 38857
29	SM BUS & POWER PORT
30	PCI-E--MINI CARD
31	PCI-E--NEW CARD
32	PCI--LAN RTL8110CL
33	RJ45 & RJ11
34	PCI--1394,CardReader R5C832
35	PCI--4 IN1 CON
36	AUDIO CODEC ALC660
37	AUDIO AMP G1420
38	MDC,B/T,TPM & DISCHG,HOLE
39	DVI CONN
40	ACIN, BAT, FAN, I/O PORT
41	SW & LED & TP
42	POWER-ON SEQUENCE
43	HISTORY
44	I/O PORT

PAGE	Content
	POWER PAGE REF.
61	POWER_VCORE
62	POWER_SYSTEM
63	POWER_I/O_1.2VO & 1.0VO
64	POWER_I/O_LDO
65	POWER_I/O_DDR2
66	POWER_VGA_CORE(Empty)
67	POWER_LOAD_SYSTEM
68	POWER_CHARGER
69	POWER_PIC
70	POWER_PROTECT
71	POWER_SWITCH_+5VLCM
72	POWER_DIAGRAM

A8T/M AMD S1/C51MV BLOCK DIAGRAM



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 2 OF 55		RELEASE DATE :	

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010001x (A2h)

MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWRLMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CR_VID2)	+3VSUS
GPIO_[11:16]		(CPU_VID[0:5])	+3VSUS
GPIO_17		(LID#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDIN0_AUD	+3VSUS
GPIO_23		ACZ_SDIN1_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	SIO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(RI#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

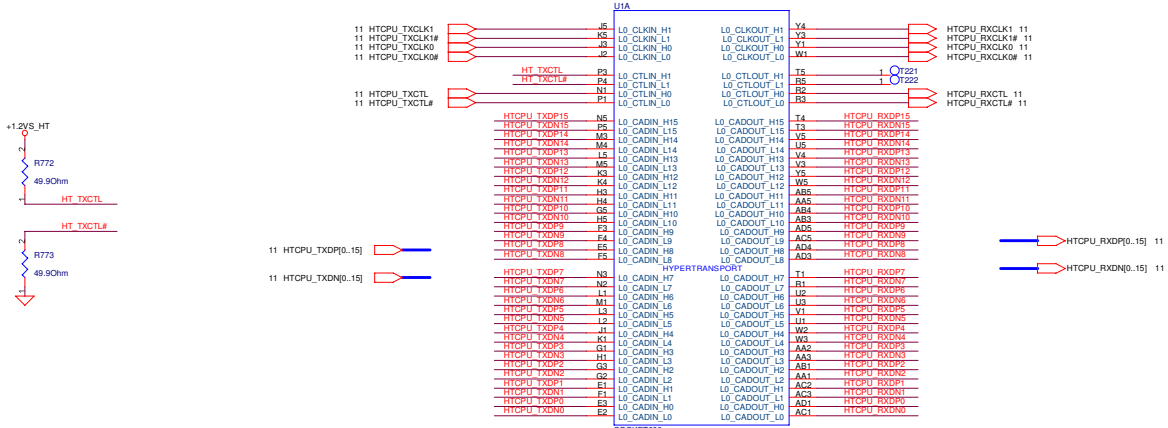
MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERM#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_P)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

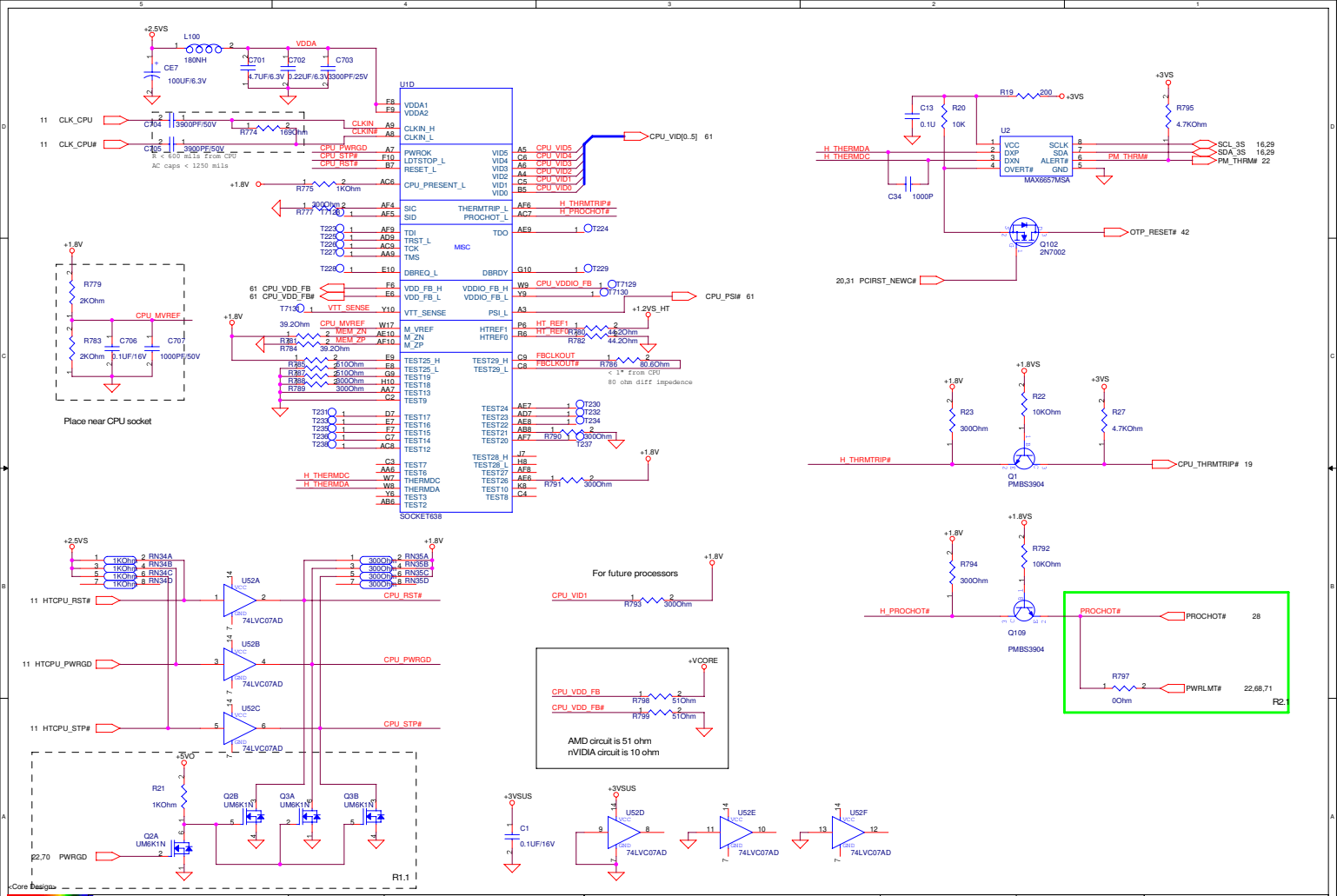
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 3 OF 55	DESCRIPTION: SCHEMATICS REF.	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



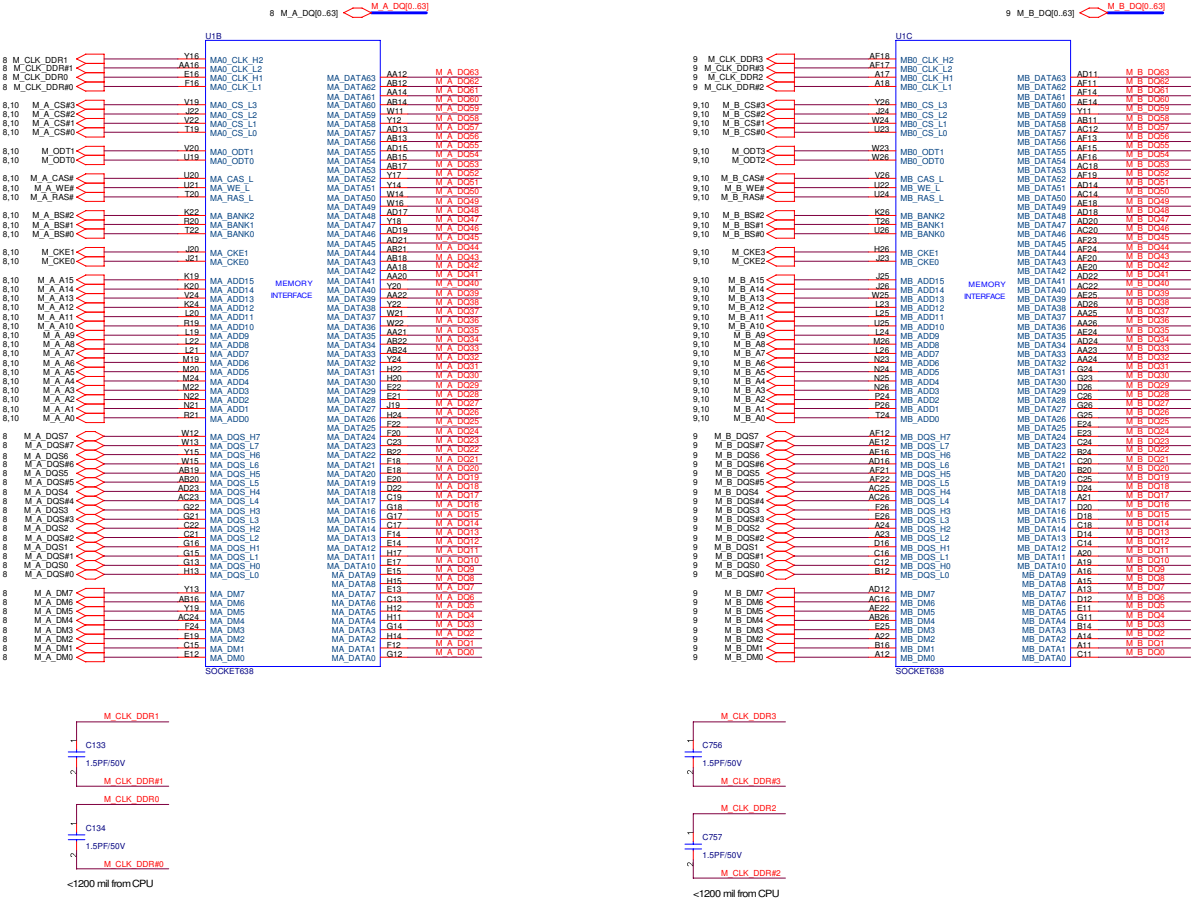
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU HT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 4 OF 55		RELEASE DATE :	



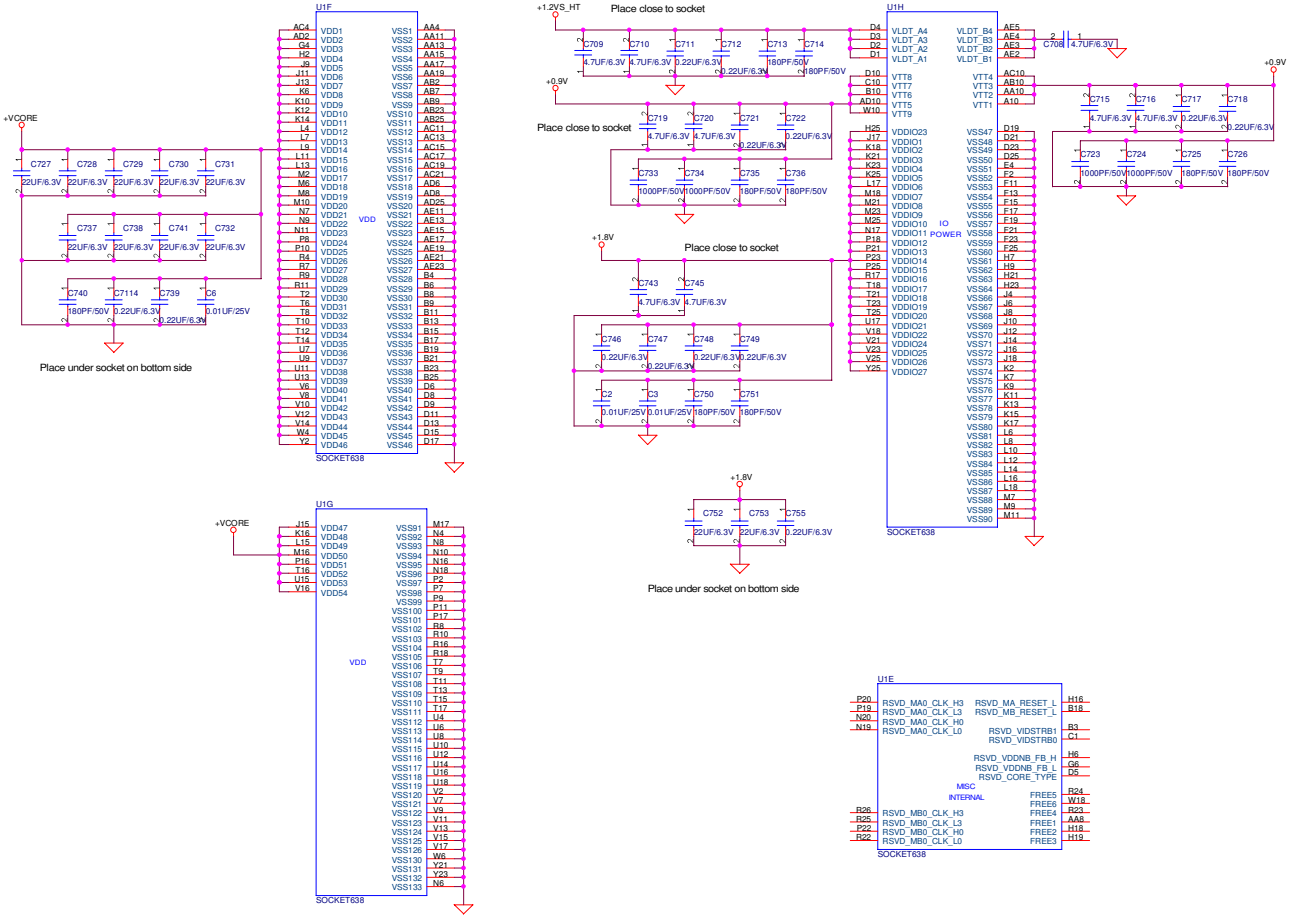
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU CNTL	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 5 OF 55		RELEASE DATE :		



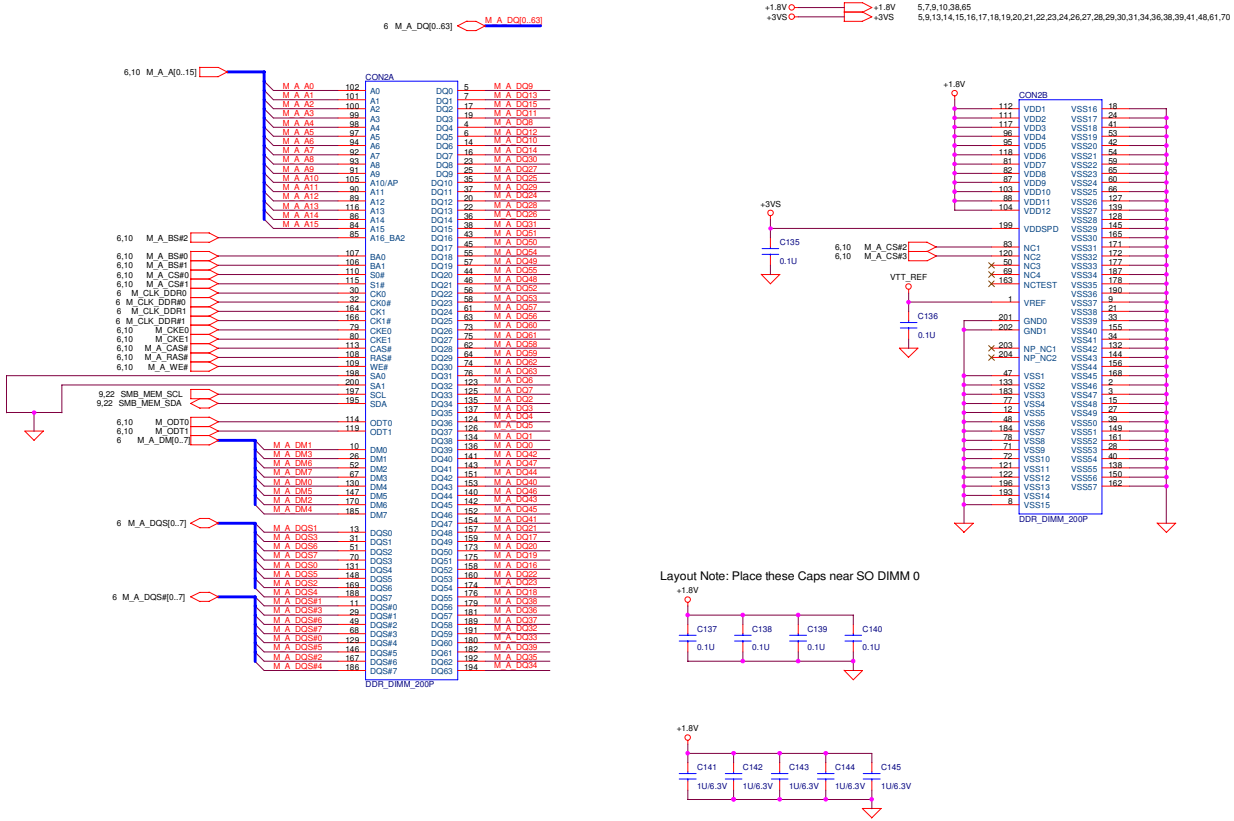
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU MEM	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 6 OF 55		RELEASE DATE :	



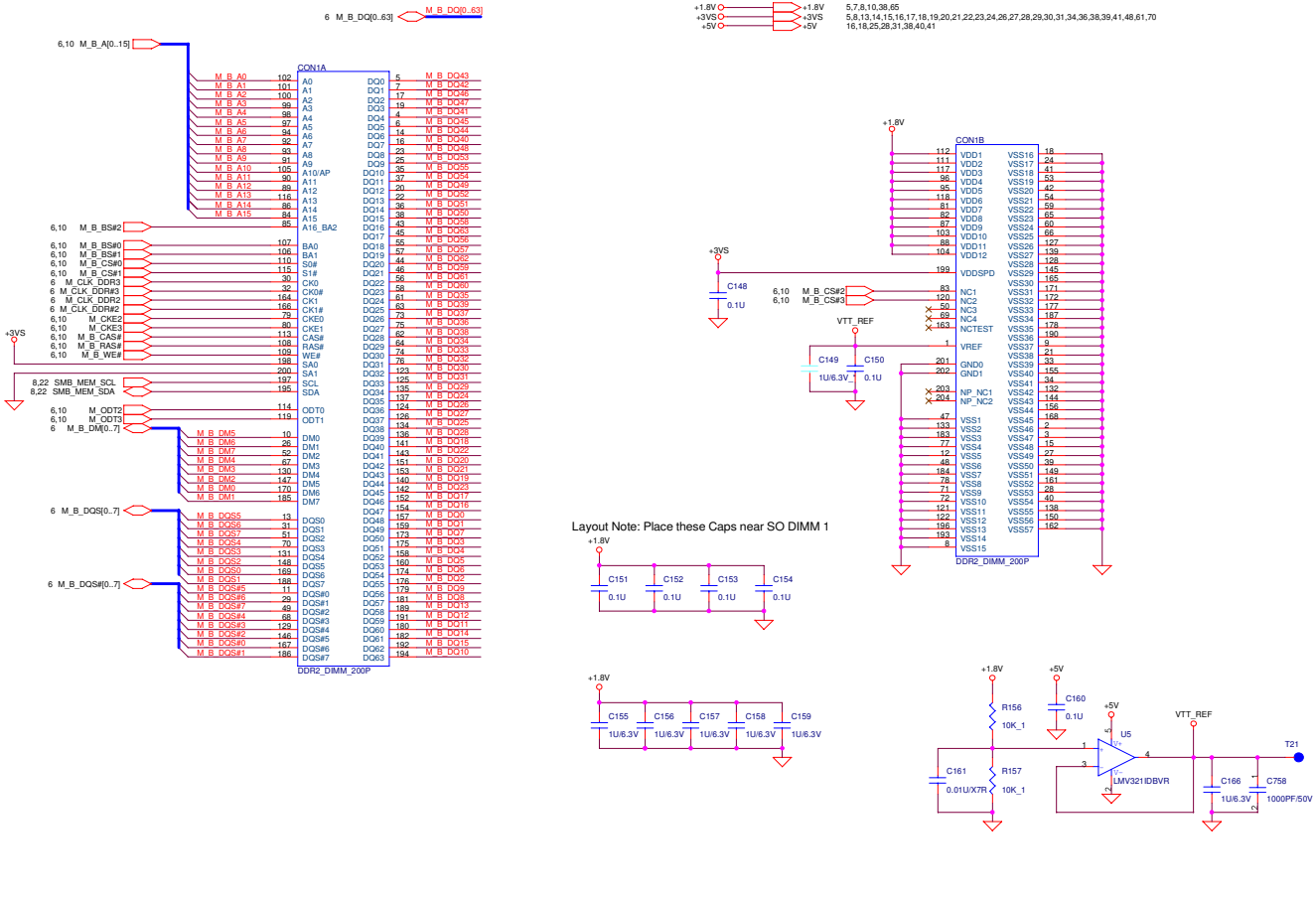
<Core Design>

PROJECT: **A8T**	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: *S1 CPU PWR/GND*	SCHEMATIC FILE NAME :	DESIGN ENGINEER : *Albert Su*
		SHEET 7 OF 55		RELEASE DATE :	



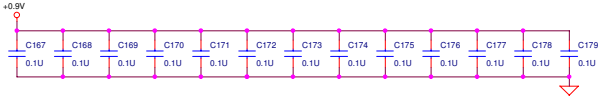
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 SO-DIMM0	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 8 OF 55		RELEASE DATE :	

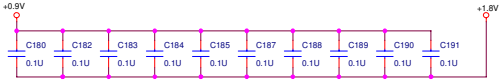


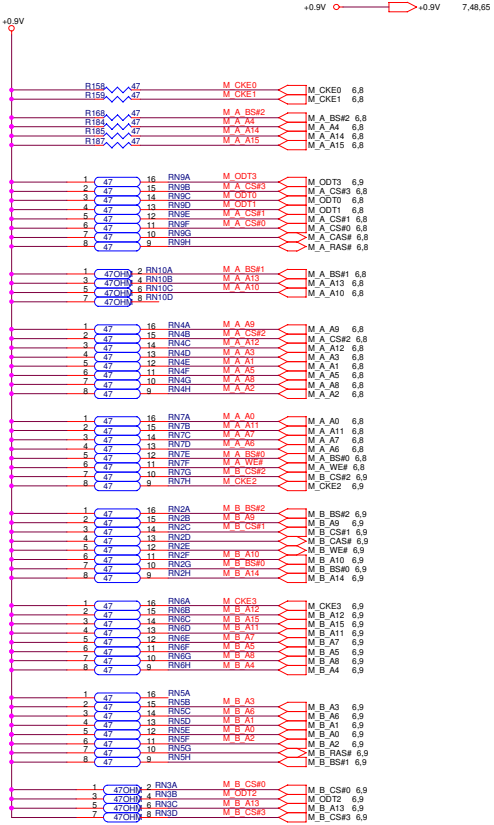
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 SO-DIMM1	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 9 OF 55		RELEASE DATE :		



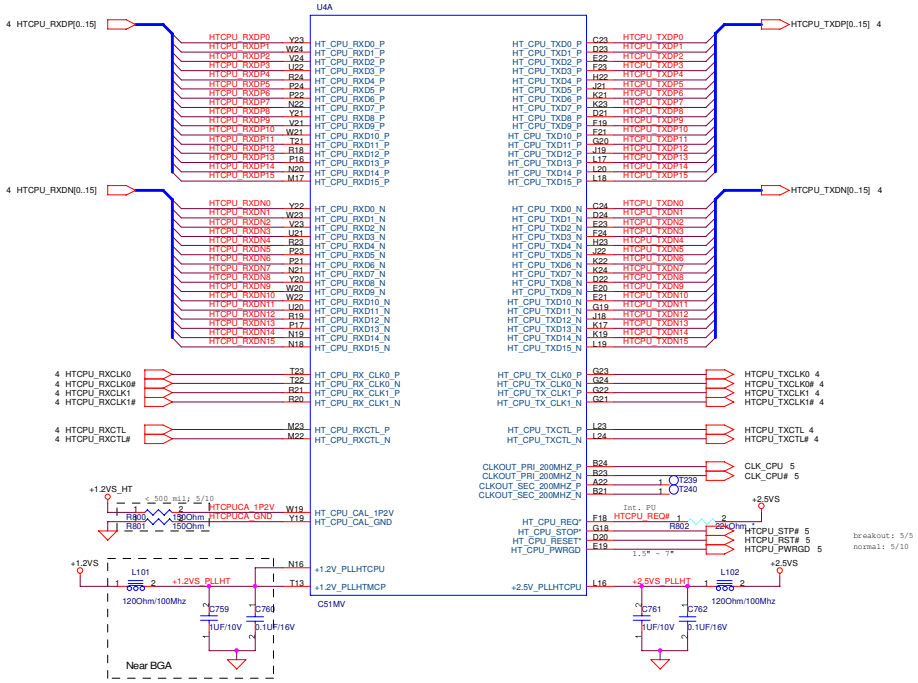
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V





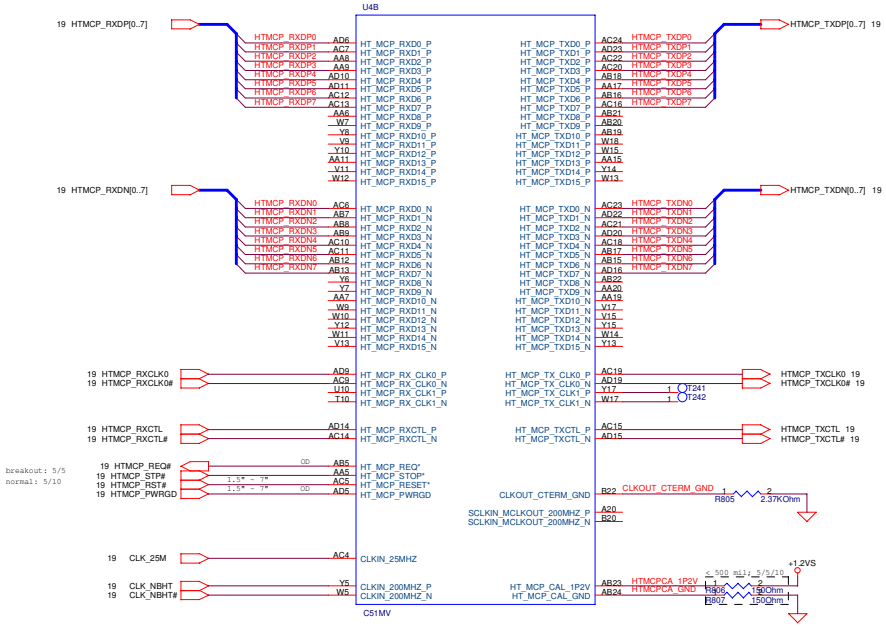
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 10 OF 55		RELEASE DATE :	



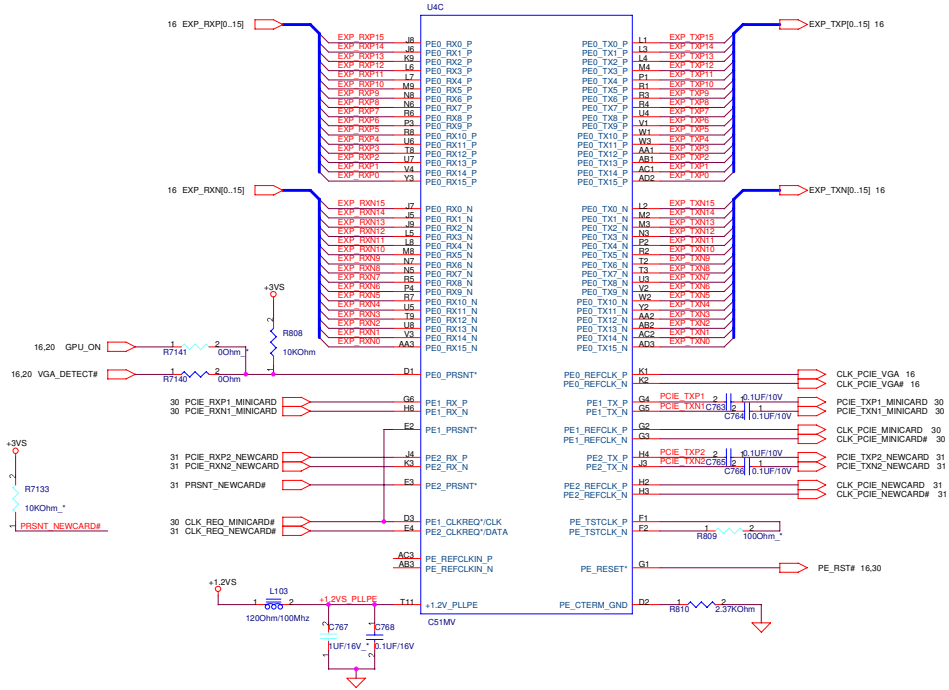
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 11 OF 55		RELEASE DATE :		



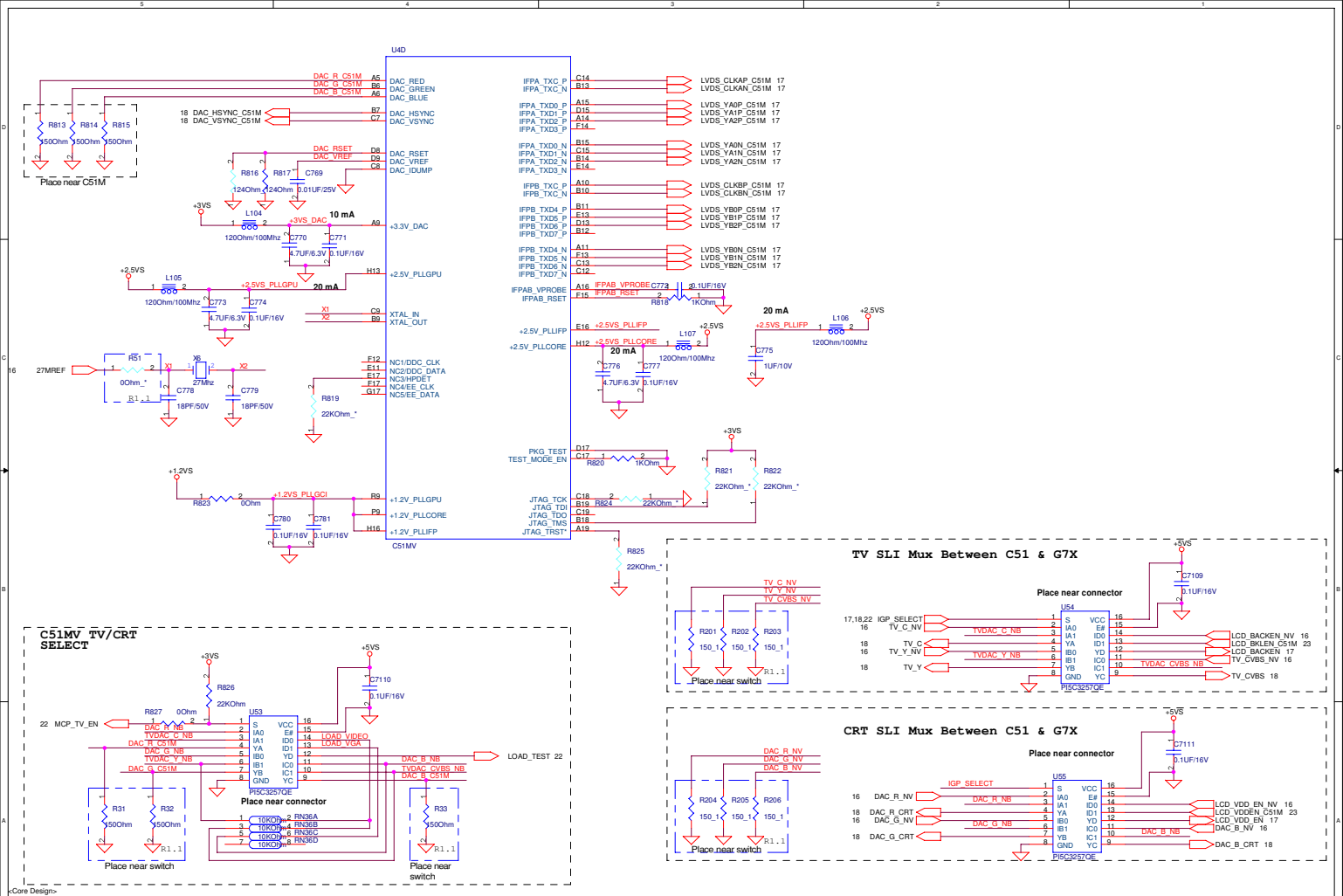
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT TO MCP	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 12 OF 55		RELEASE DATE :		



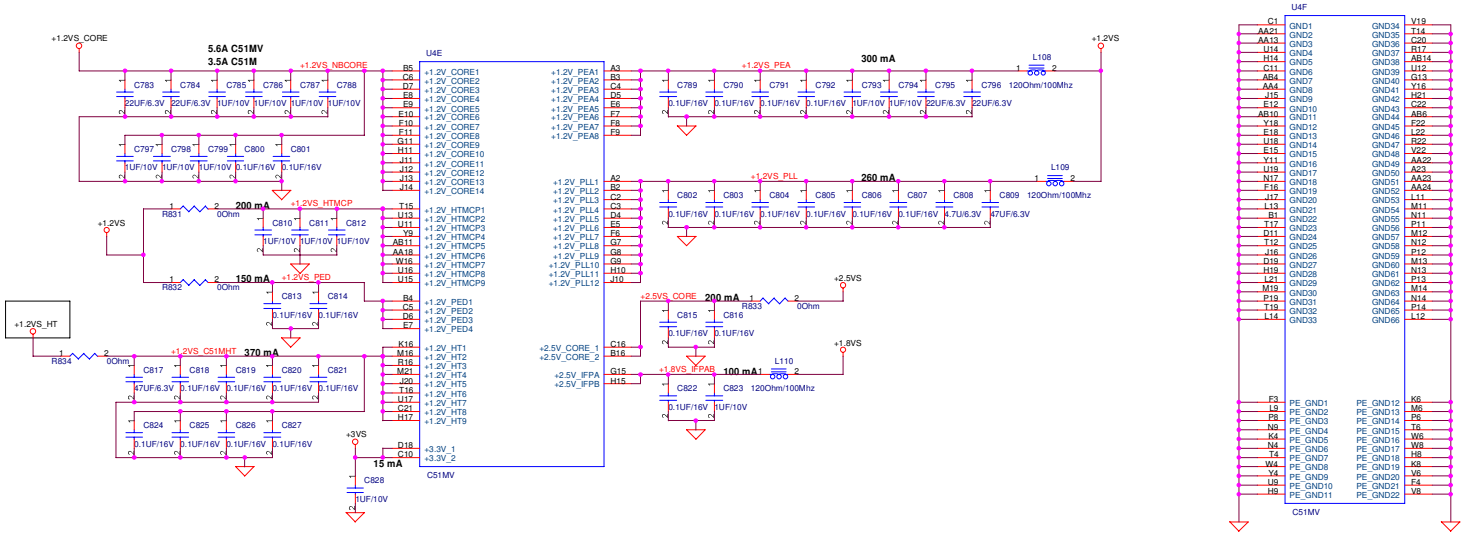
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PCI-E	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 13 OF 55		RELEASE DATE :	



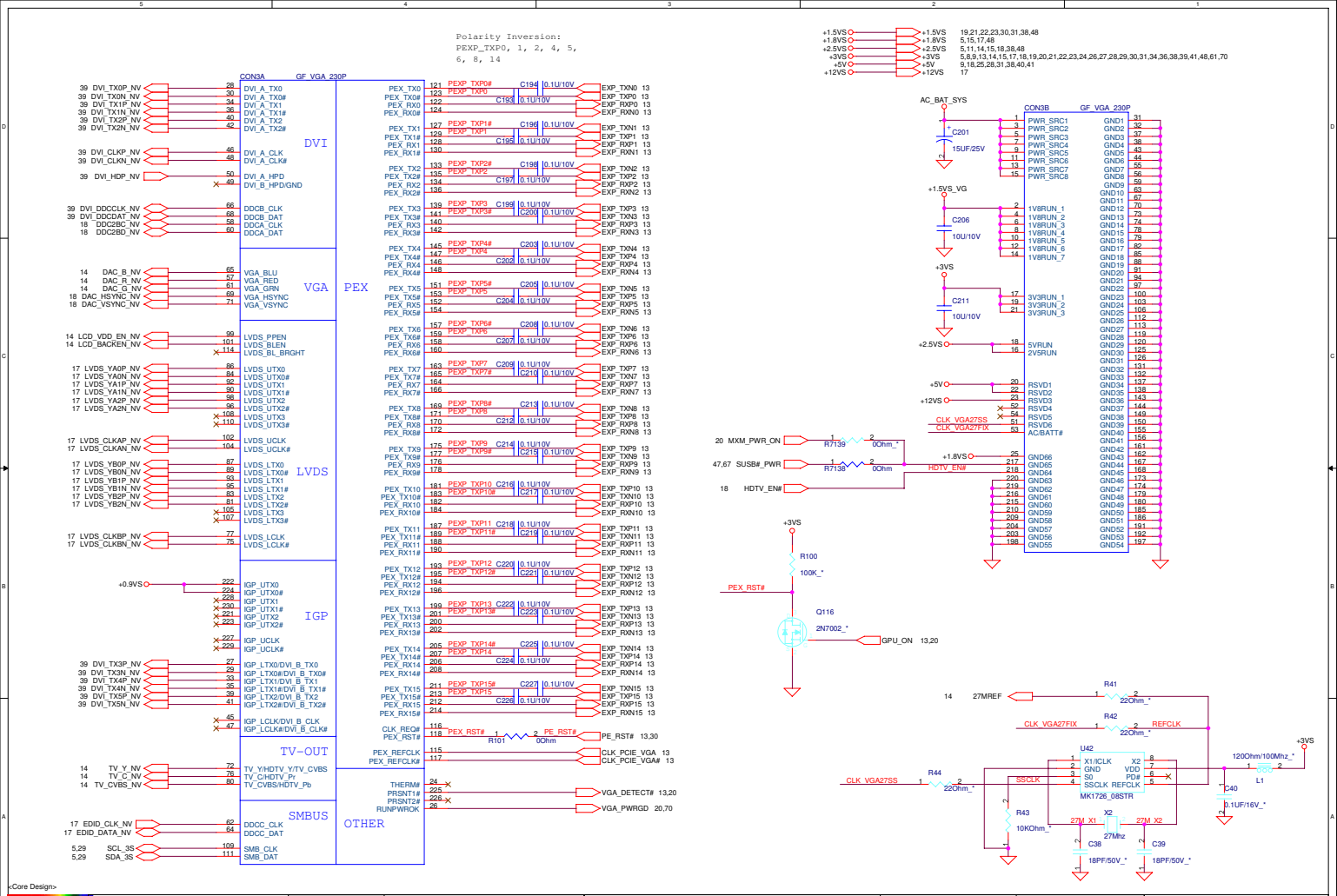
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M CRT&LVDS	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 14 OF 55		RELEASE DATE :		

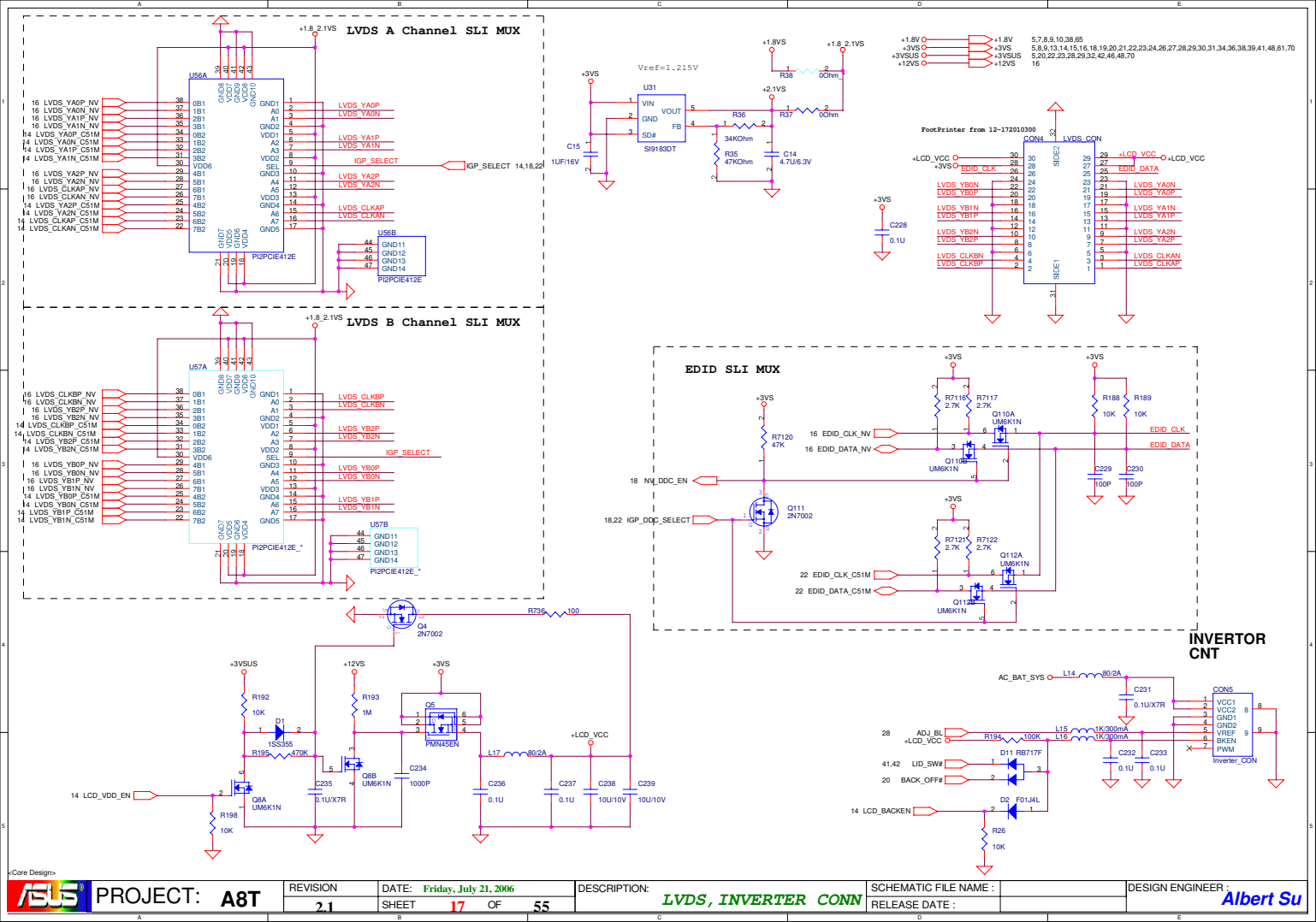


<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 15 OF 55		RELEASE DATE :	

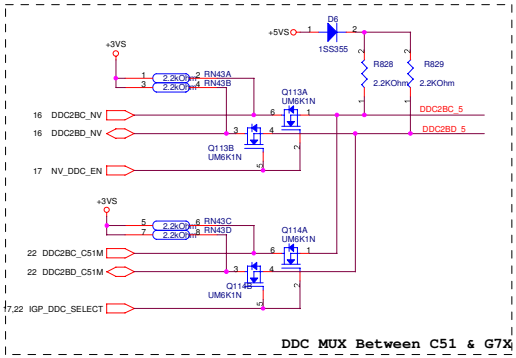


PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: VGA CONN	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 16 OF 55		RELEASE DATE :		

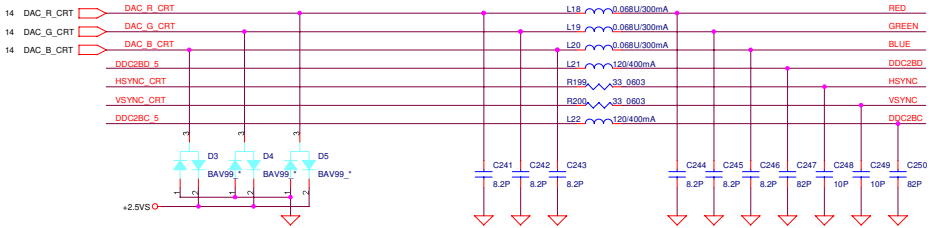


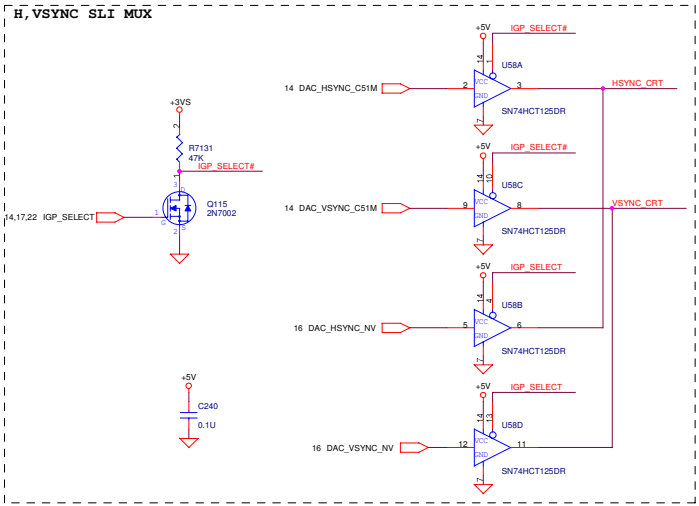
<Core Design>

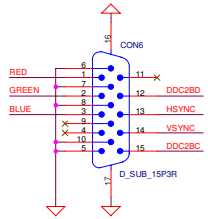
PROJECT: **A8T**	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: *LVDS, INVERTER CONN*	SCHEMATIC FILE NAME :		DESIGN ENGINEER : **Albert Su**
		SHEET 17 OF 55		RELEASE DATE :		

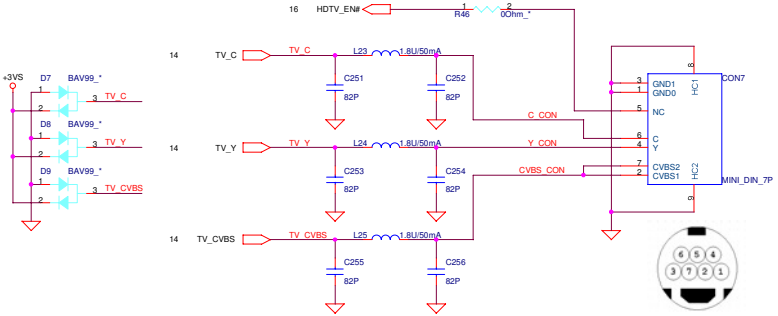

+3VS
+5VS
D6
1SS355
R828
2.2KOhm
R829
2.2KOhm
RN43A
RN43B
2.2KOhm
Q113A
UM6K1N
Q113B
UM6K1N
16 DDC2BC_NV
16 DDC2BD_NV
17 NV_DDC_EN
DDC2BC_5
DDC2BD_5
RN43C
RN43D
Q114A
UM6K1N
Q114B
UM6K1N
22 DDC2BC_C51M
22 DDC2BD_C51M
17,22 IGP_DDC_SELECT
DDC MUX Between C51 & G7X

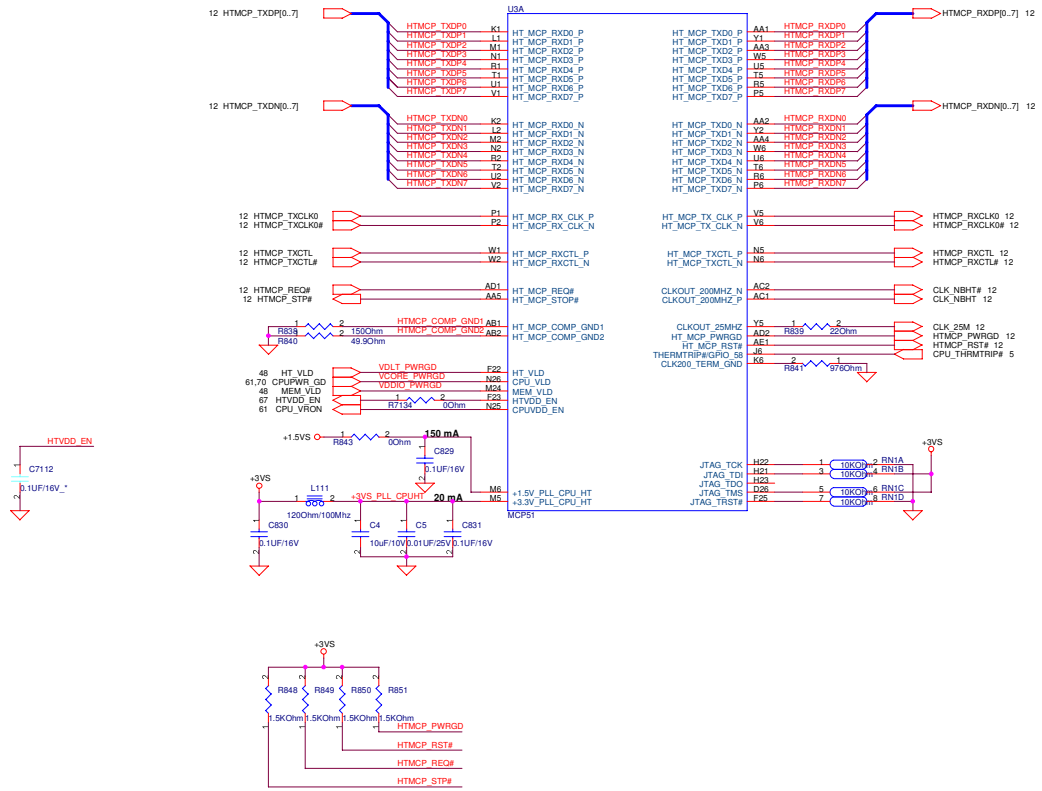

+2.5VS
+3VS
+5V
+5VS
5,11,14,15,16,38,48
5,8,9,13,14,15,16,17,19,20,21,22,23,24,26,27,28,29,30,31,34,36,38,39,41,48,61,70
9,16,25,28,31,38,40,41
14,23,24,28,29,36,37,38,39,40,41,61


14 DAC_R_CRT
14 DAC_G_CRT
14 DAC_B_CRT
DDC2BD_5
HSYNC_CRT
VSYNC_CRT
DDC2BC_5
D3 BAV99_*
D4 BAV99_*
D5 BAV99_*
+2.5VS
L18 0.068U/300mA
L19 0.068U/300mA
L20 0.068U/300mA
L21 120/400mA
R199 33_0603
R200 33_0603
L22 120/400mA
RED
GREEN
BLUE
DDC2BD
HSYNC
VSYNC
DDC2BC
C241 C242 C243 8.2P
C244 8.2P
C245 8.2P
C246 8.2P
C247 82P
C248 10P
C249 10P
C250 82P


H,VSYNC SLI MUX
+3VS
R7131
47K
IGP_SELECT#
Q115
2N7002
14,17,22 IGP_SELECT
+5V
C240
0.1U
U58A
U58C
U58B
U58D
SN74HCT125DR
14 DAC_HSYNC_C51M
14 DAC_VSYNC_C51M
16 DAC_HSYNC_NV
16 DAC_VSYNC_NV
HSYNC_CRT
VSYNC_CRT

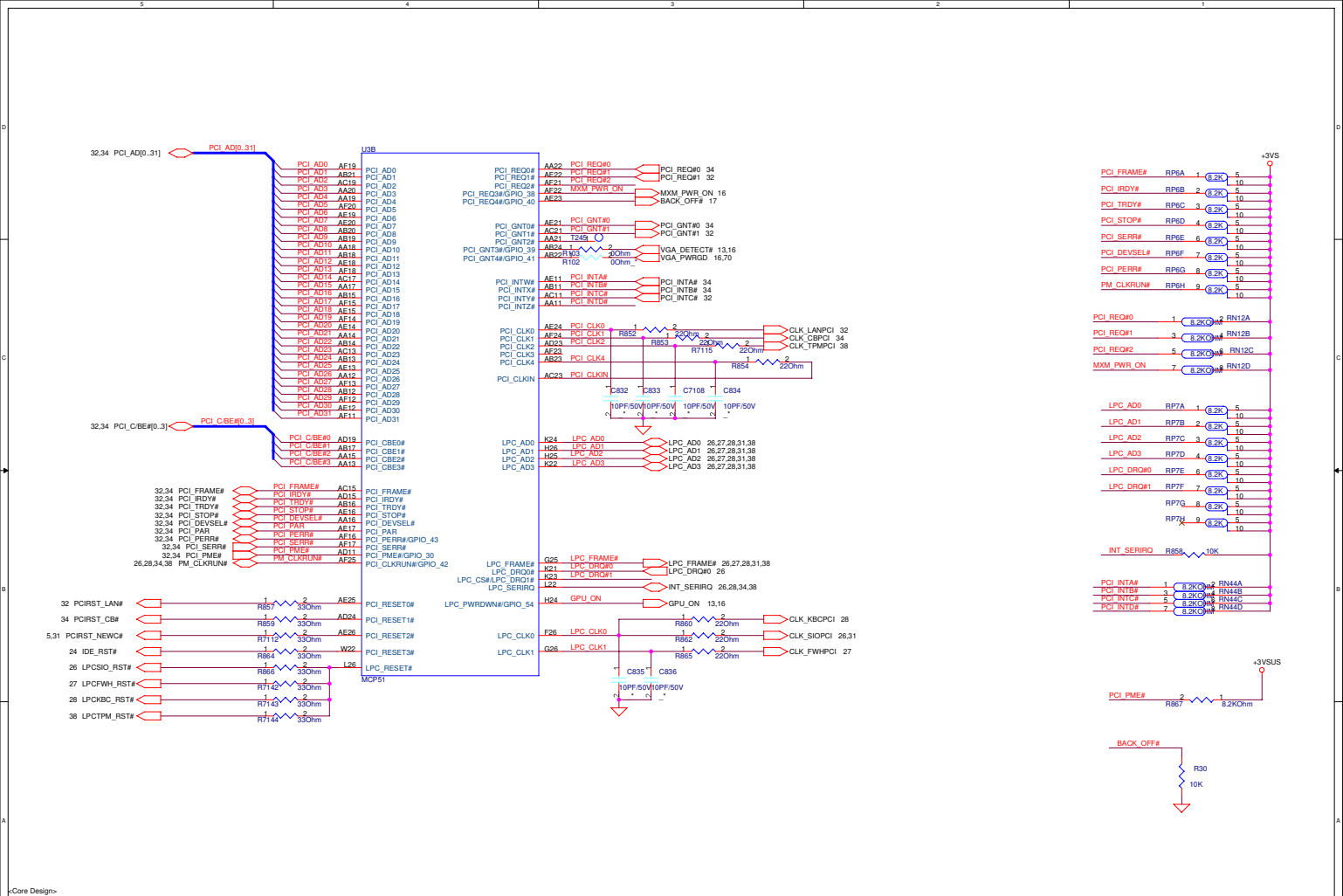

CON6
RED
GREEN
BLUE
DDC2BD
HSYNC
VSYNC
DDC2BC
D_SUB_15P3R


16 HDTV_EN#
R46 0Ohm_*
+3VS
D7 BAV99_*
D8 BAV99_*
D9 BAV99_*
TV_C
TV_Y
TV_CVBS
14 TV_C
14 TV_Y
14 TV_CVBS
L23 1.8U/50mA
L24 1.8U/50mA
L25 1.8U/50mA
C251 C252 C253 C254 C255 C256 82P
C_CON
Y_CON
CVBS_CON
CON7
GND1
GND0
NC
C
Y
CVBS2
CVBS1
MINI_DIN_7P



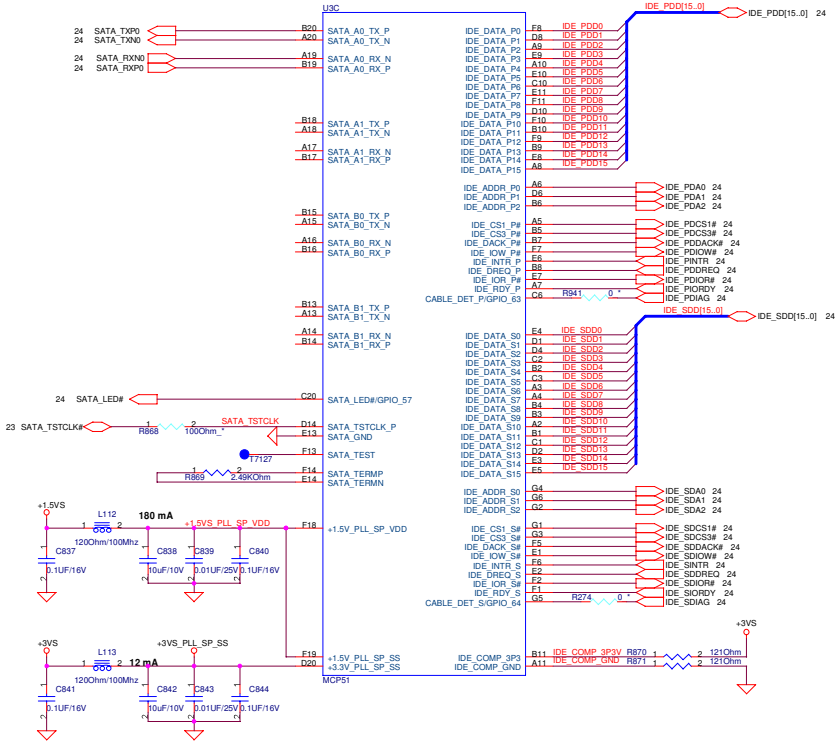
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 HT I/F	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 19 OF 55		RELEASE DATE :	



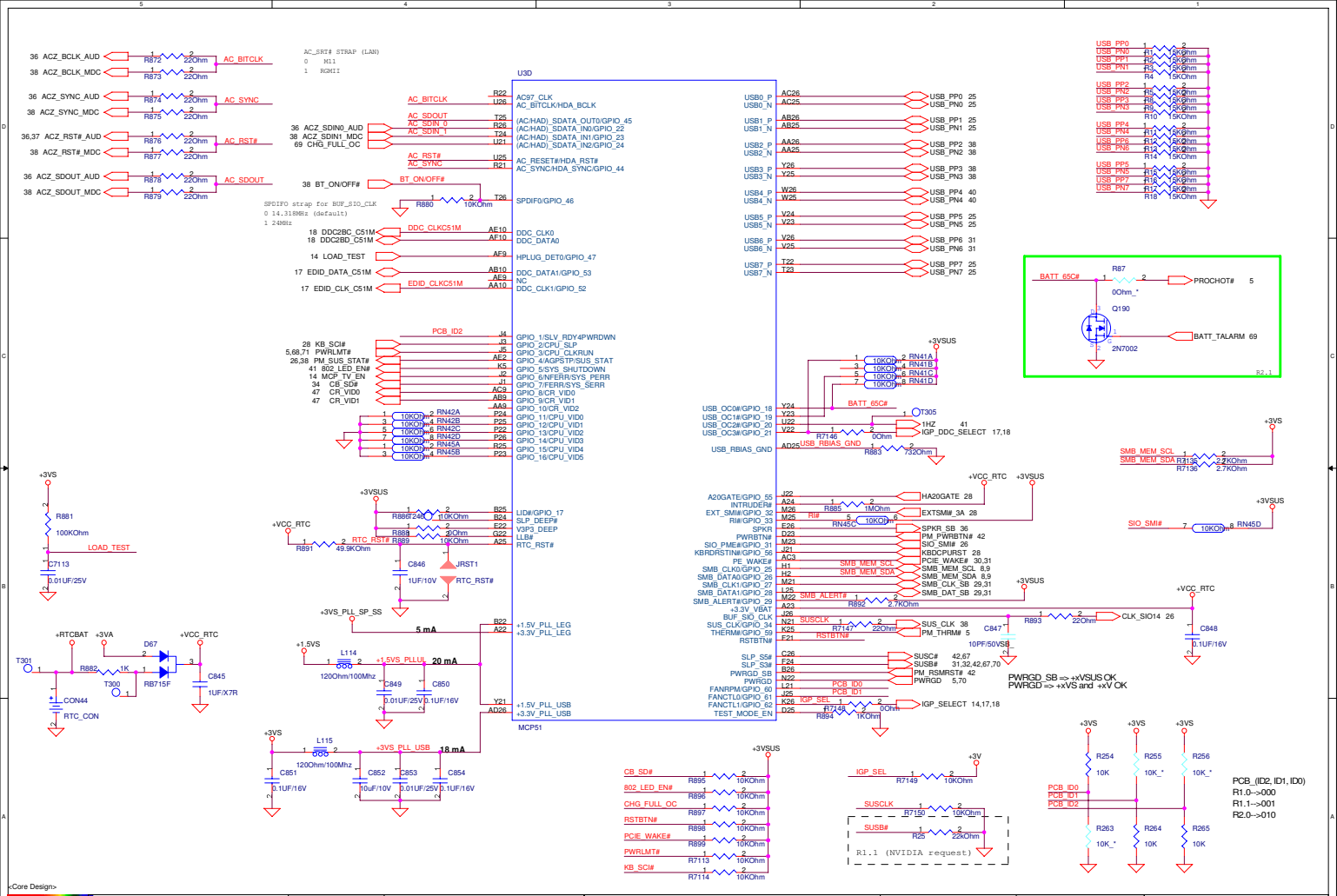
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PCI	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 20 OF 55		RELEASE DATE :		



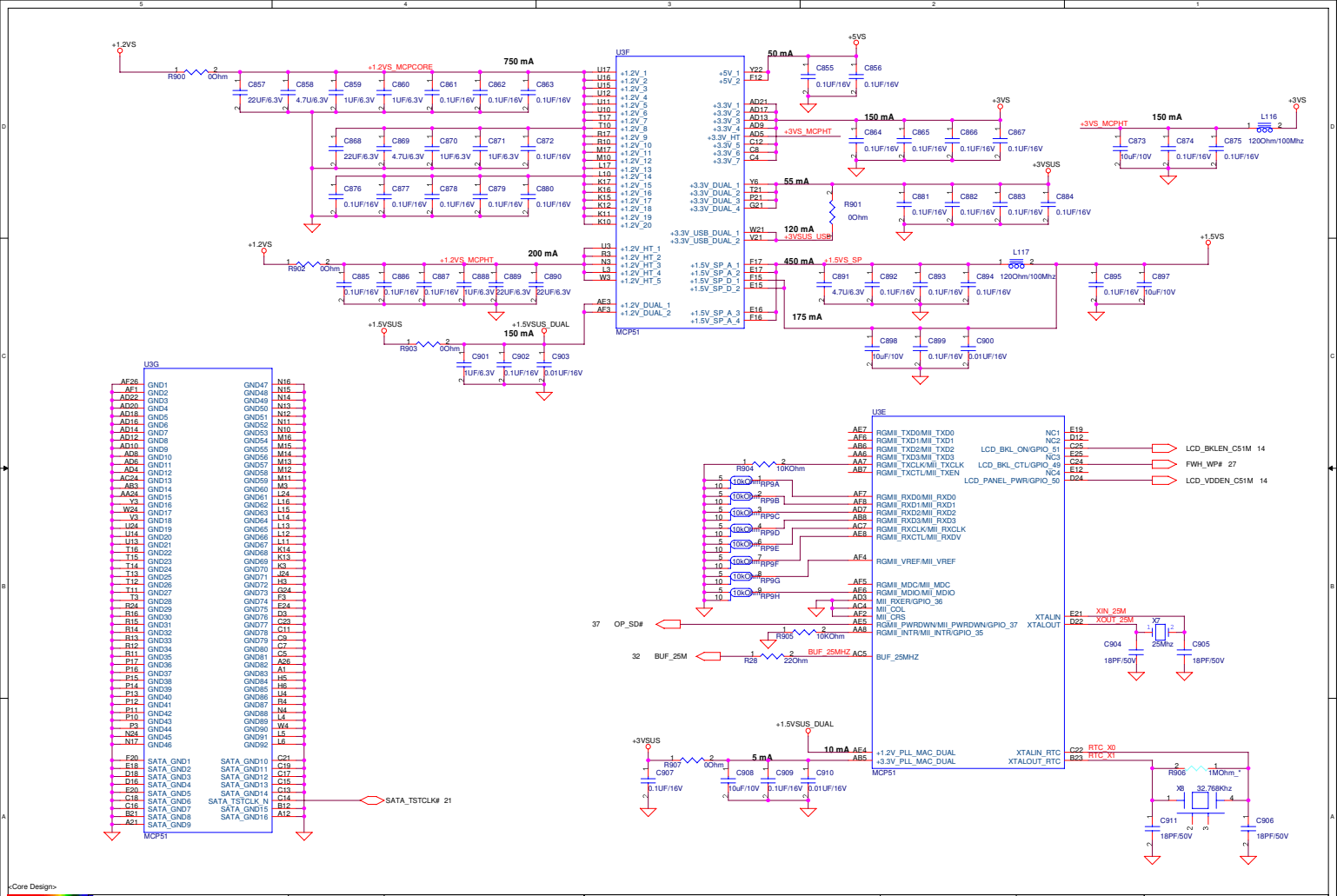
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 IDE	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 21 OF 55		RELEASE DATE :		



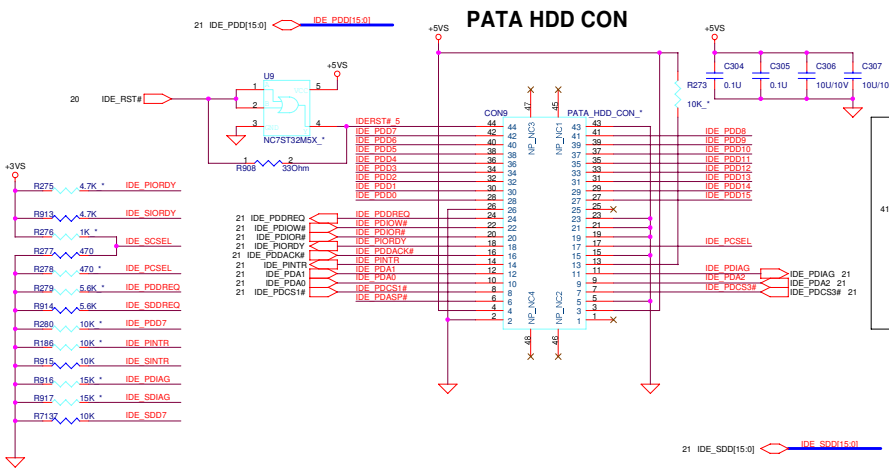
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 USB/HDA	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 22 OF 55		RELEASE DATE :		

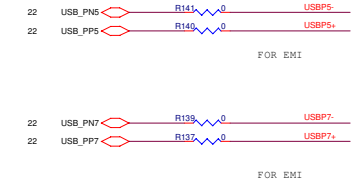


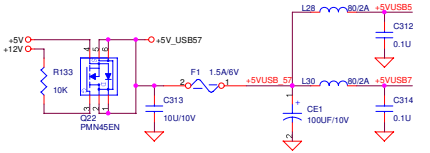
<Core Design>

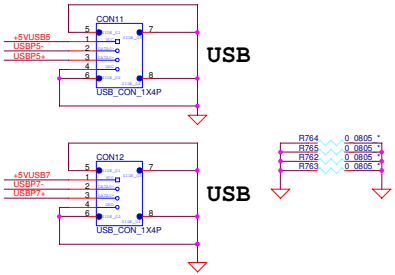
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 23 OF 55		RELEASE DATE :	

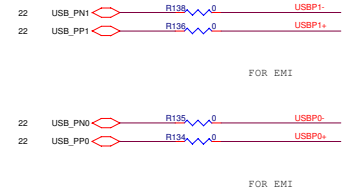


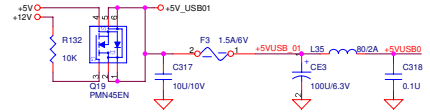
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: HDD & CD-ROM CONN	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 24 OF 55		RELEASE DATE :	

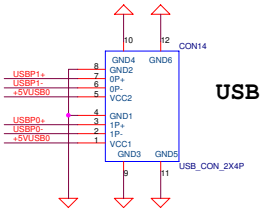






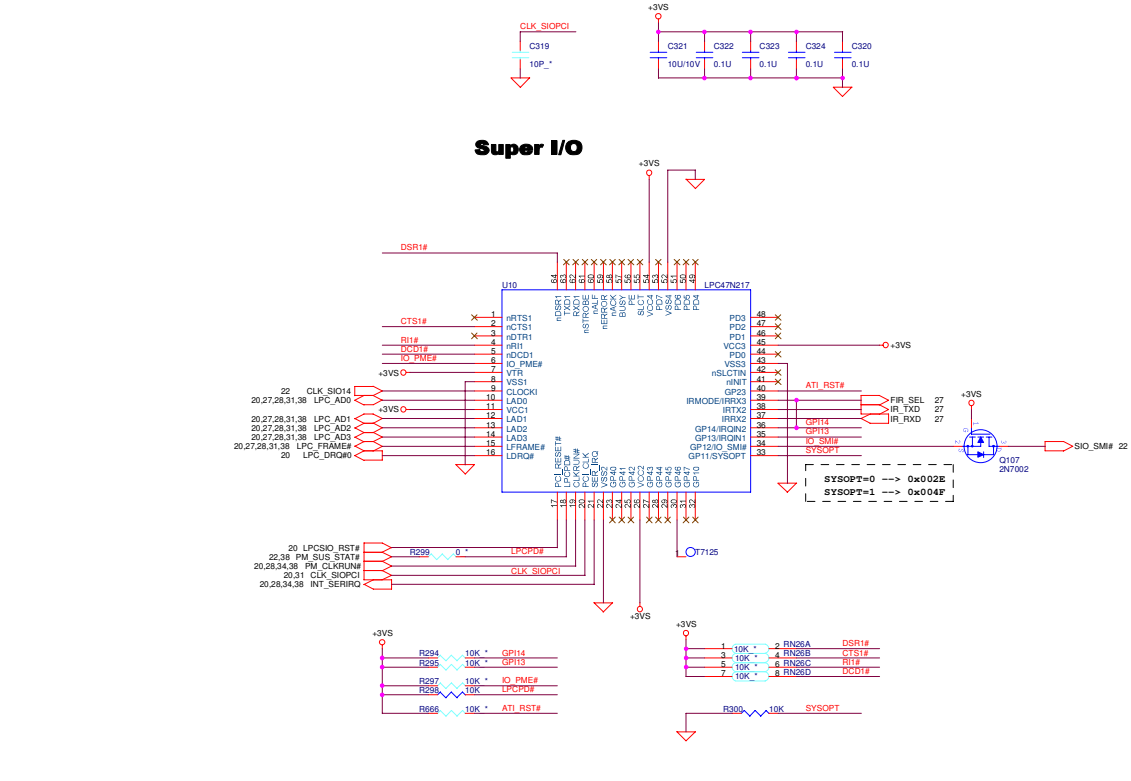






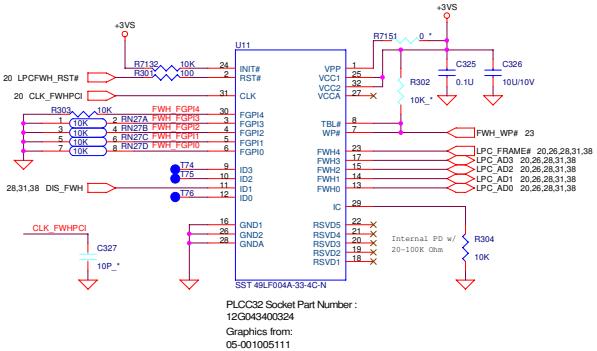
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: USB PORTS	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 25 OF 55		RELEASE DATE :	

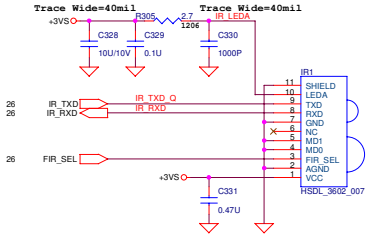


<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SUPER IO LPC47N217	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 26 OF 55		RELEASE DATE :	



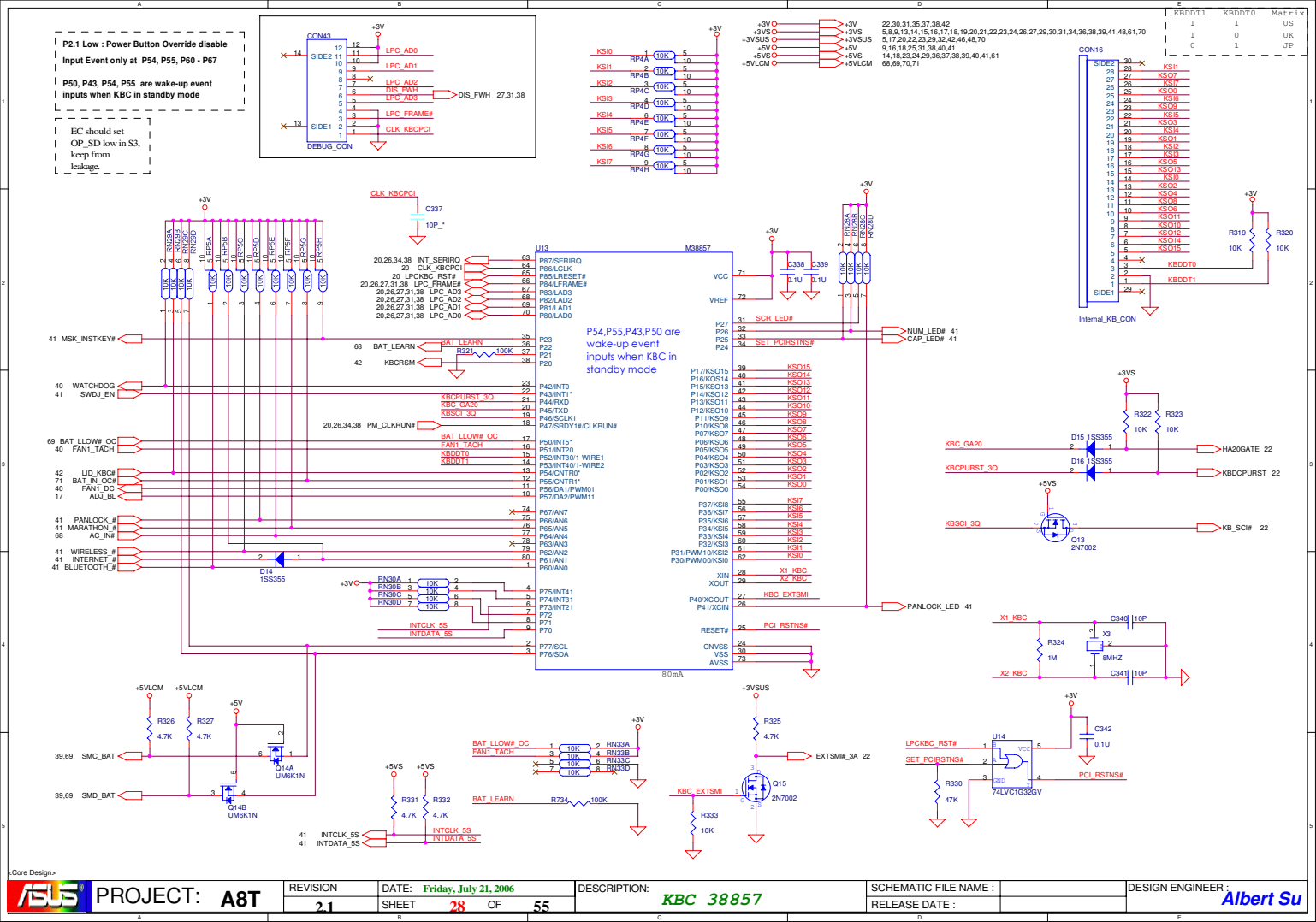
PLCC32 Socket Part Number :
12G043400324
Graphics from:
05-001005111



+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,30,31,34,36,38,39,41,48,61,70

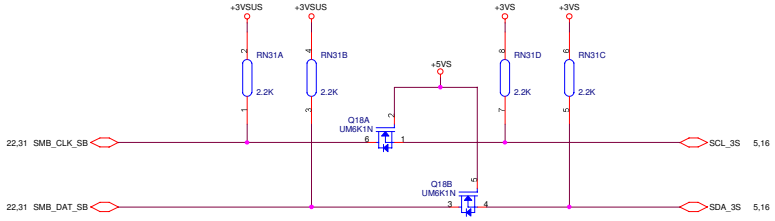
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 27 OF 55	DESCRIPTION: BIOS , IR	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: KBC 38857	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 28 OF 55		RELEASE DATE :		



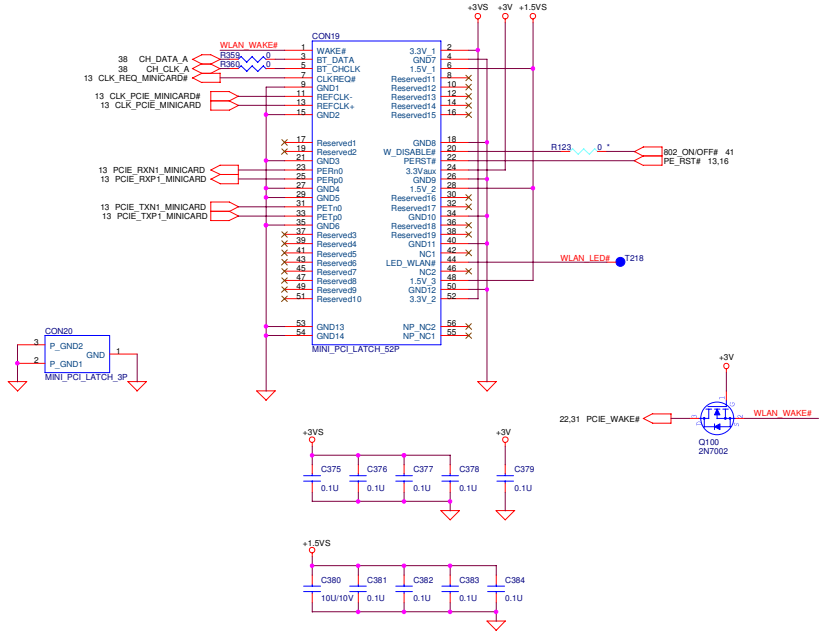
MCP51

Termal Sensor,
TPM

+3VA	+3VA	22,38,41,42,48,71
+3VSUS	+3VSUS	5,17,20,22,23,28,32,42,46,48,70
+0.9VS	+0.9VS	16
+1.5VS	+1.5VS	19,21,22,23,30,31,38,48
+2.5VS	+2.5VS	5,11,14,15,16,18,38,48
+3VS	+3VS	5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,34,36,38,39,41,48,61,70
+5VS	+5VS	14,18,23,24,28,36,37,38,39,40,41,61
+12VS	+12VS	16,17
+1.8V	+1.8V	5,7,8,9,10,38,65
+3V	+3V	22,28,30,31,35,37,38,42
+5V	+5V	9,16,18,25,28,31,38,40,41
+12V	+12V	25,40
+VCORE	+VCORE	5,7,61
+5VLCM	+5VLCM	28,68,69,70,71

<Core Design>

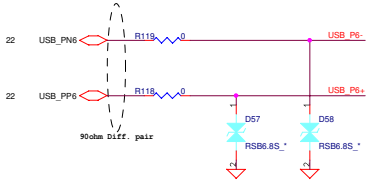
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SM BUS & POWER PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 29 OF 55		RELEASE DATE :	

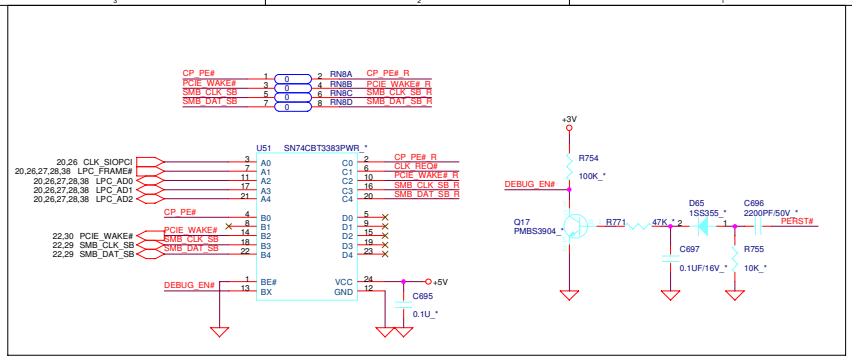


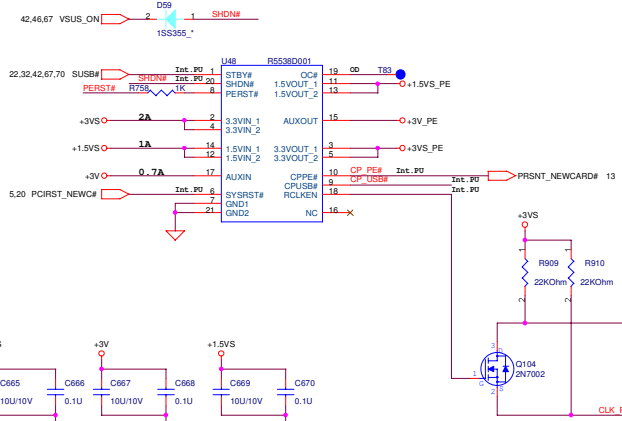
+1.5VS +1.5VS 19,21,22,23,31,38,48
+3V +3V 22,28,31,35,37,38,42
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,31,34,36,38,39,41,48,61,70

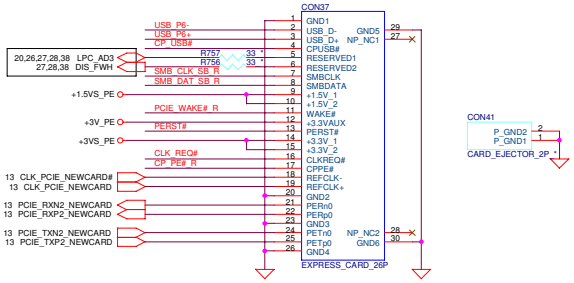
<Core Design>

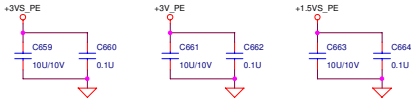
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MINI CARD	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 30 OF 55		RELEASE DATE :	







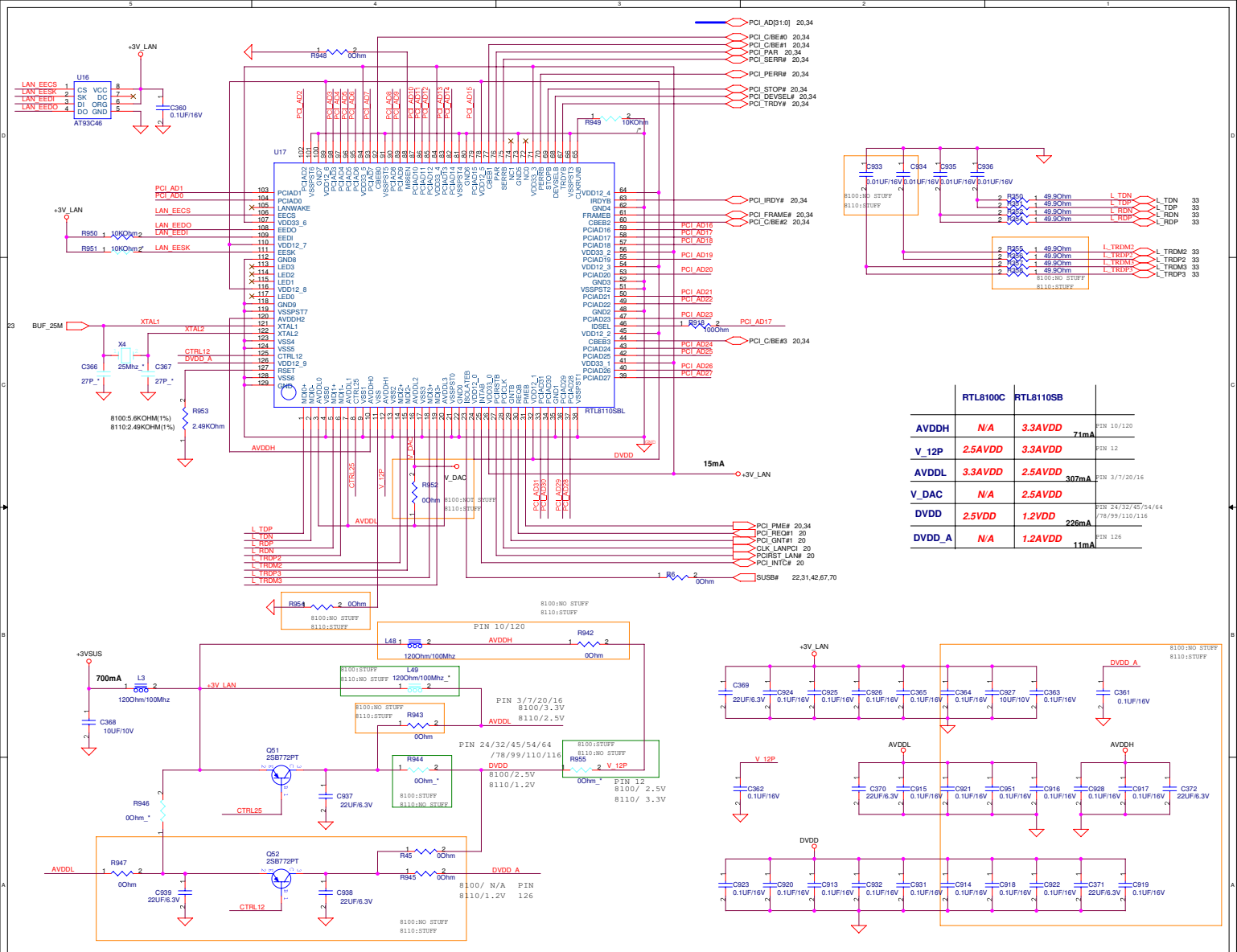




+1.5VS +1.5VS 19,21,22,23,30,38,48
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,34,36,38,39,41,48,61,70
+3V +3V 22,28,30,35,37,38,42

<Core Design>

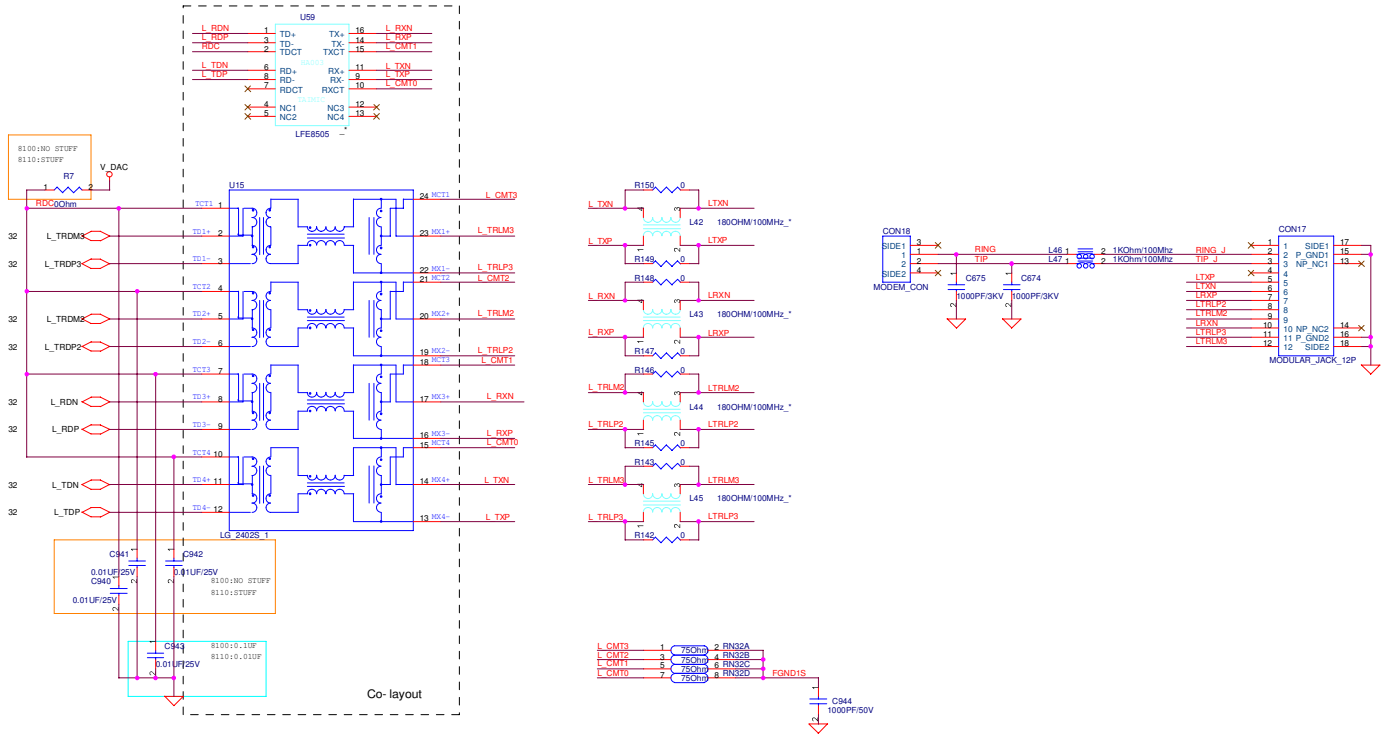
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: NEW CARD	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 31 OF 55		RELEASE DATE :		



	RTL8100C	RTL8110SB	
AVDDH	N/A	3.3AVDD	PIN 10/120
		71mA	
V_12P	2.5AVDD	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	
		307mA	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	
DVDD	2.5VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
		226mA	
DVDD_A	N/A	1.2AVDD	PIN 126
		11mA	

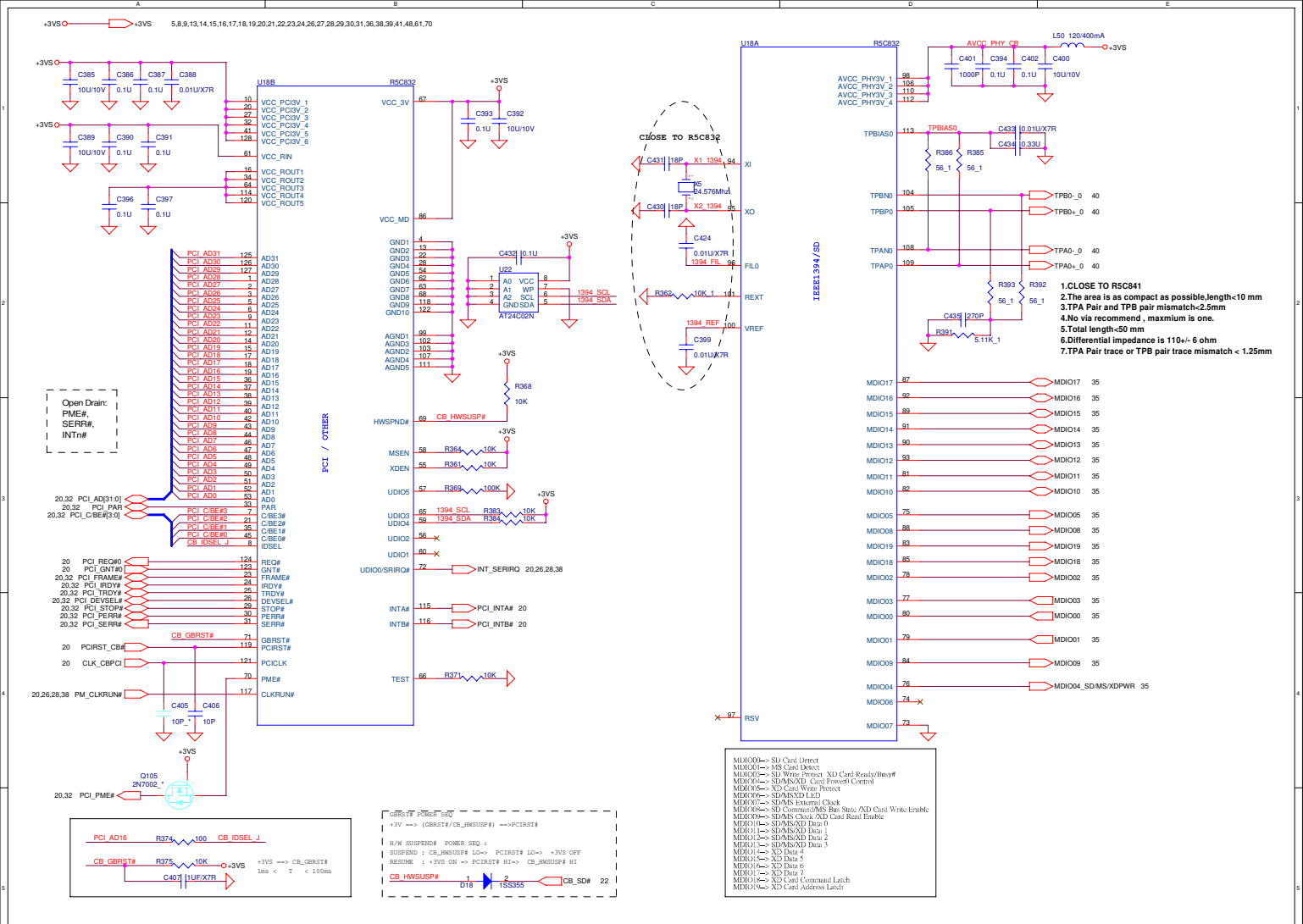
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 32 OF 55	DESCRIPTION: LAN -- RTL8110CL	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



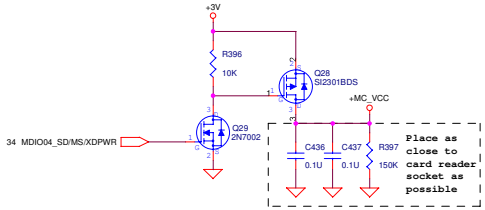
<Core Design>

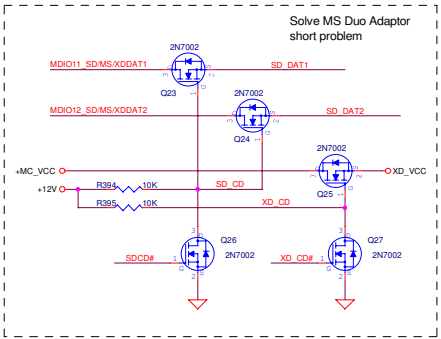
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 33 OF 55		RELEASE DATE :		

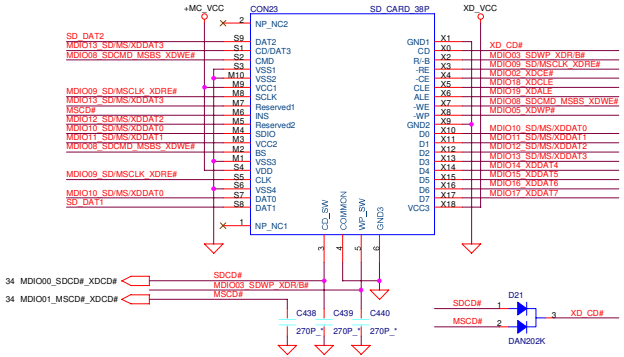


<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: PCI R5C832	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 34 OF 55		RELEASE DATE :		



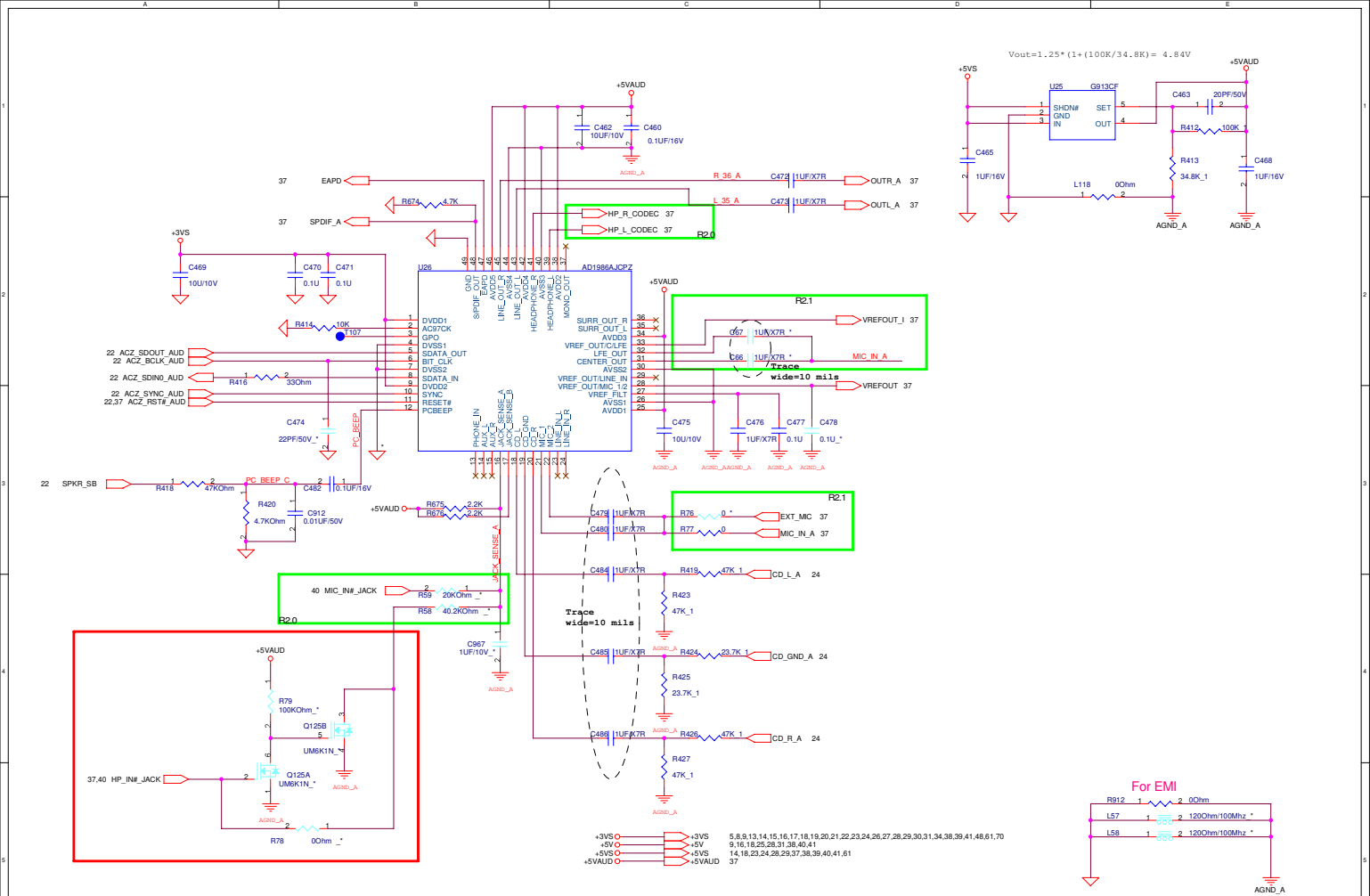




+3V +3V 22,28,30,31,37,38,42
+12V +12V 25,37,40,67

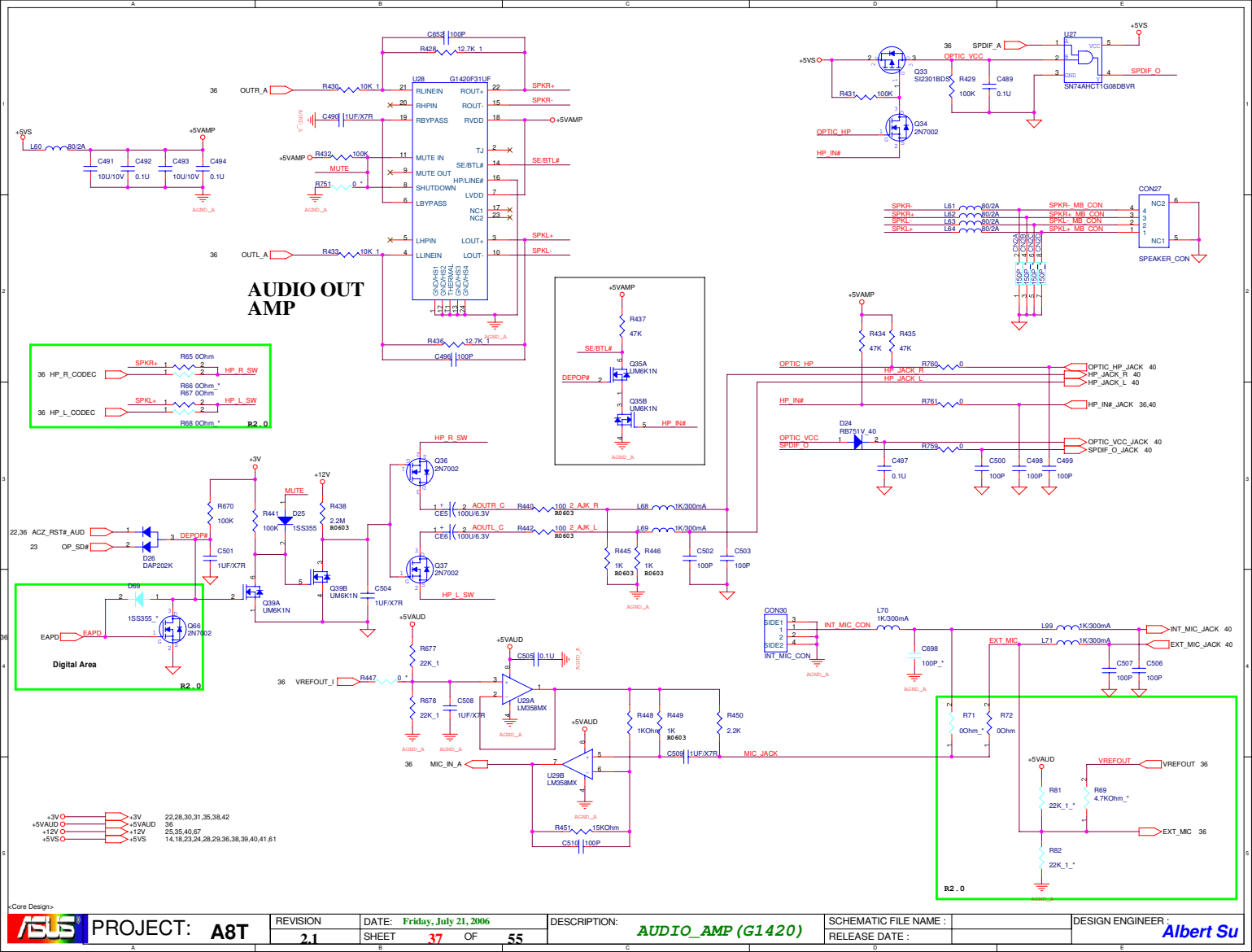
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 35 OF 55	DESCRIPTION: 4 IN 1 CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

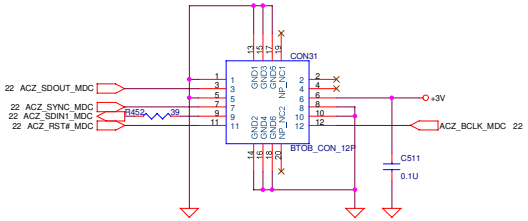
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 36 OF 55		RELEASE DATE :		



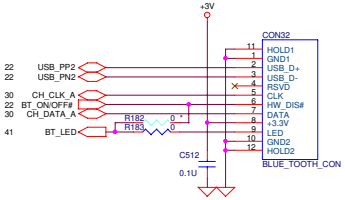
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: AUDIO_AMP (G1420)	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 37 OF 55		RELEASE DATE :		

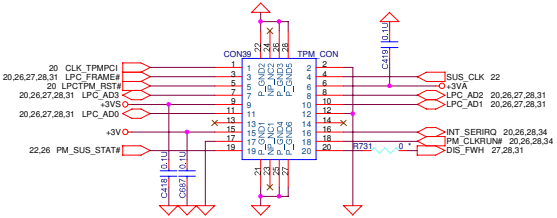
Azalia MDC MODEM CON



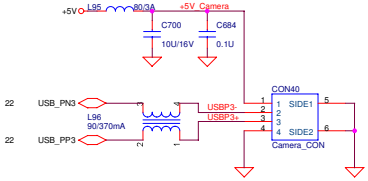
Bluetooth Module CON

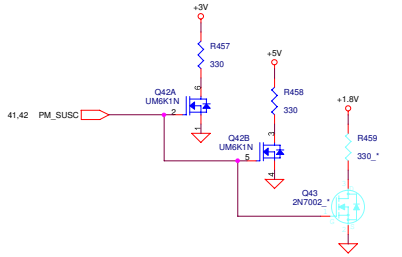


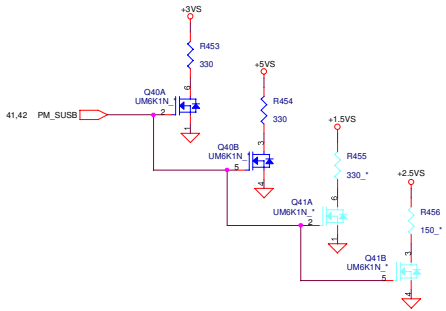
TPM Module CON

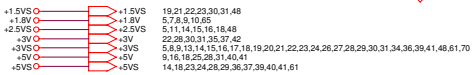


Camera Module CON



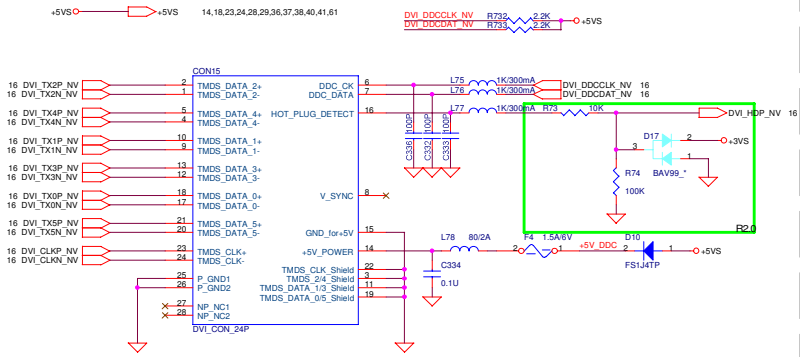


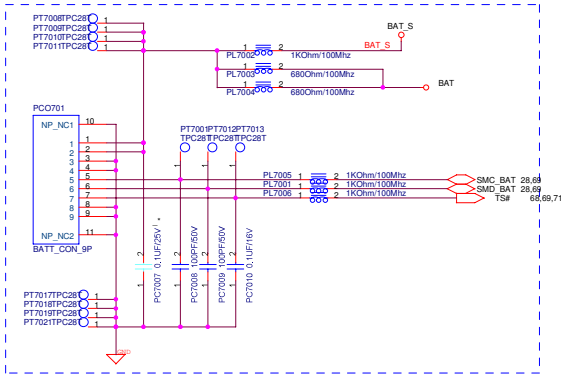


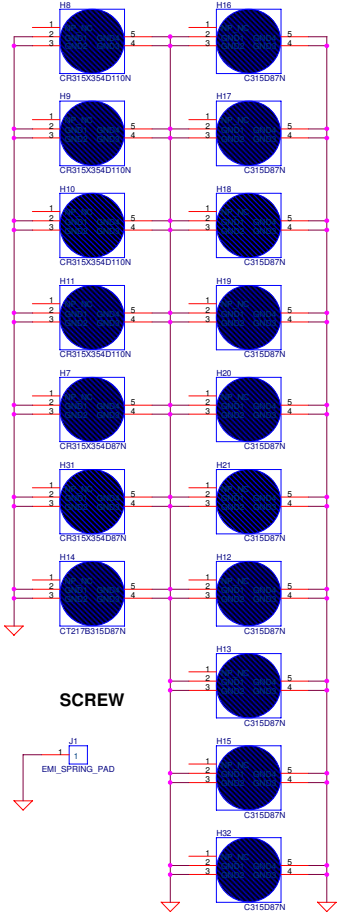


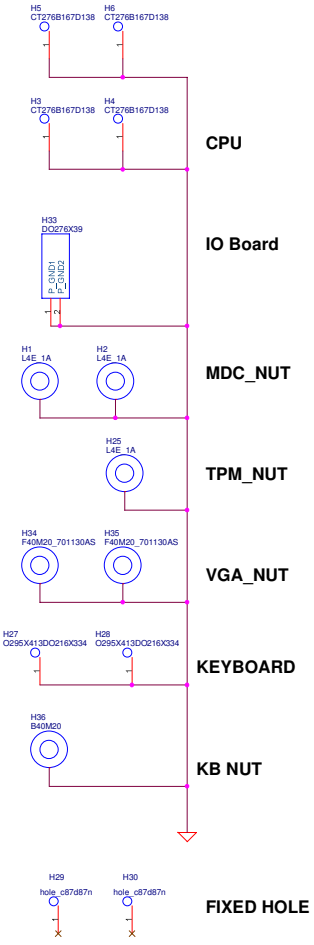
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MDC, B/T, TPM, Camera & DISCHG	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 38 OF 55		RELEASE DATE :		



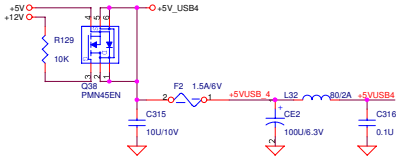


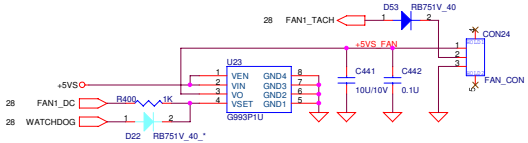




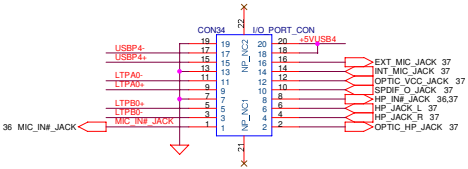
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DVI CONN & HOLE	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 39 OF 55		RELEASE DATE :		

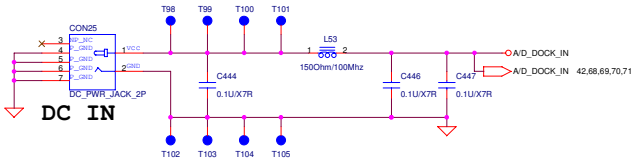




FAN CONTROL



I/O PORT

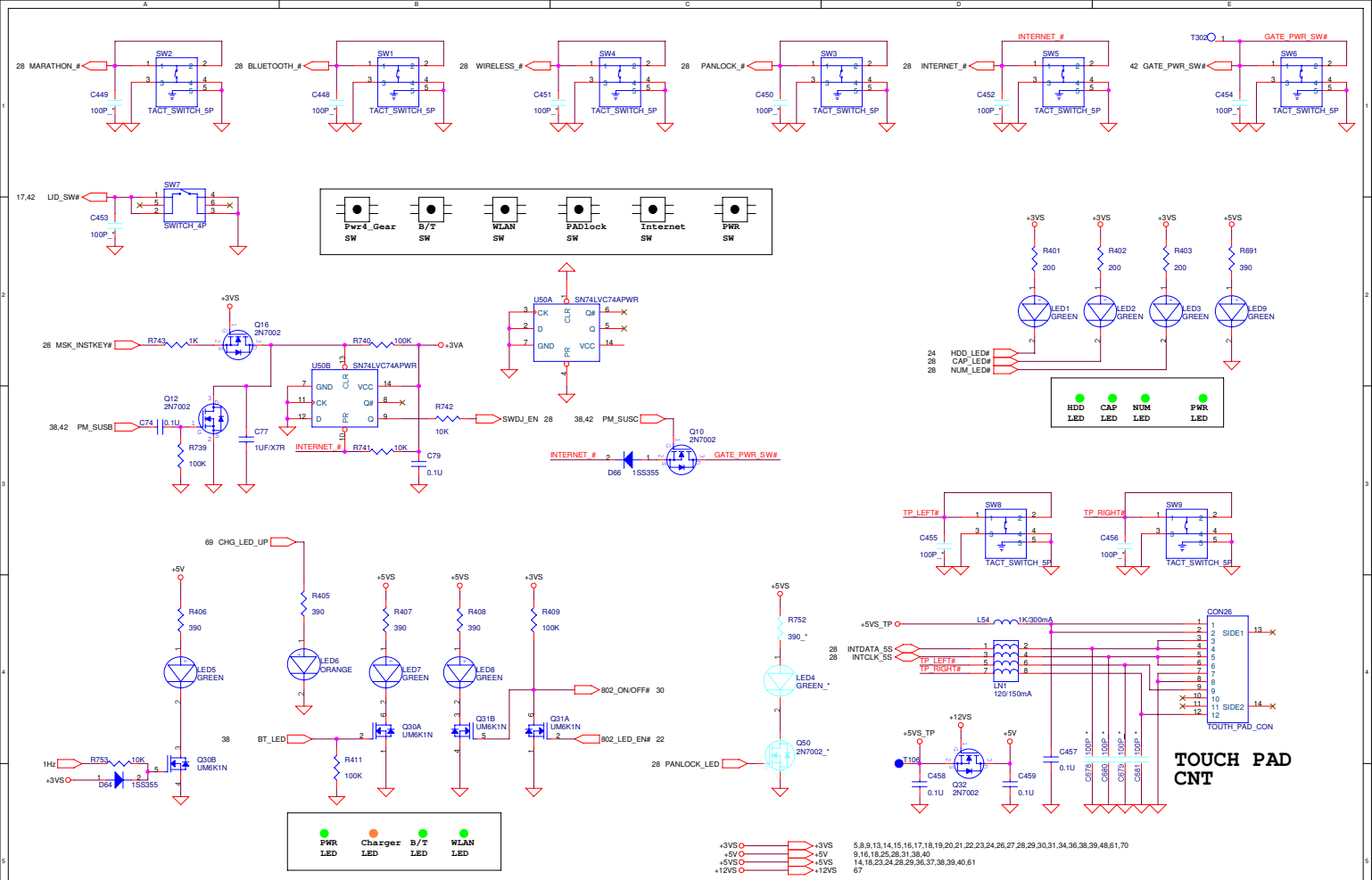


DC IN

ACIN_CONN

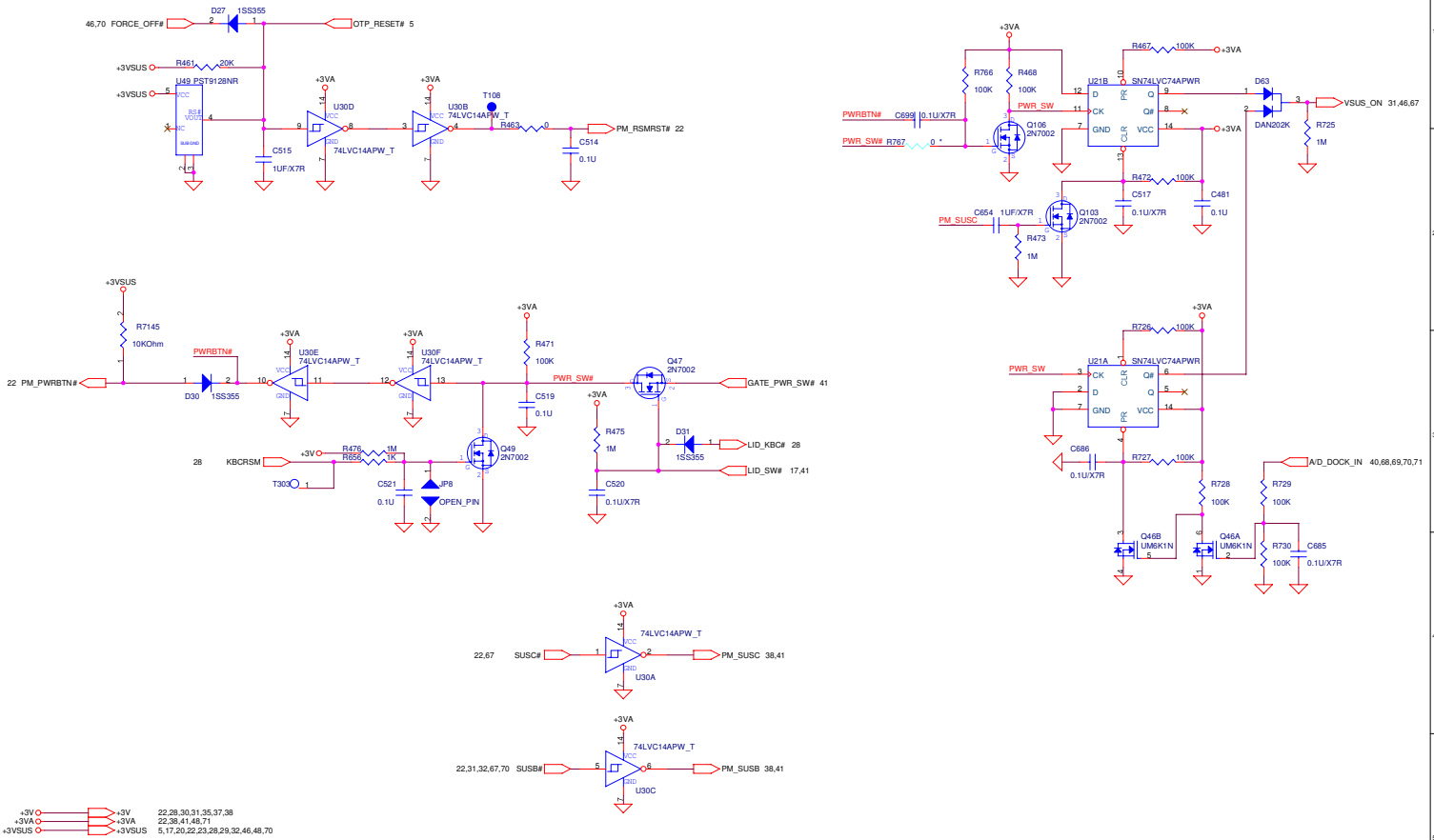
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 40 OF 55	DESCRIPTION: FAN_CTRL & ACIN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 41 OF 55	DESCRIPTION: SW & LED & TP	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



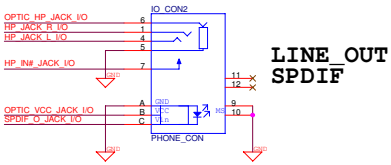
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 42 OF 55		RELEASE DATE :	

Revision History

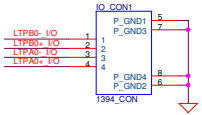
Power:

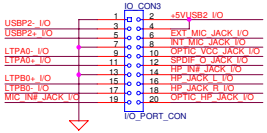
System:

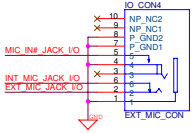


LINE_OUT
SPDIF

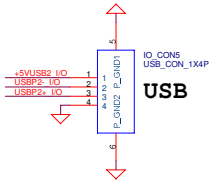
1394A



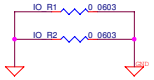




MIC

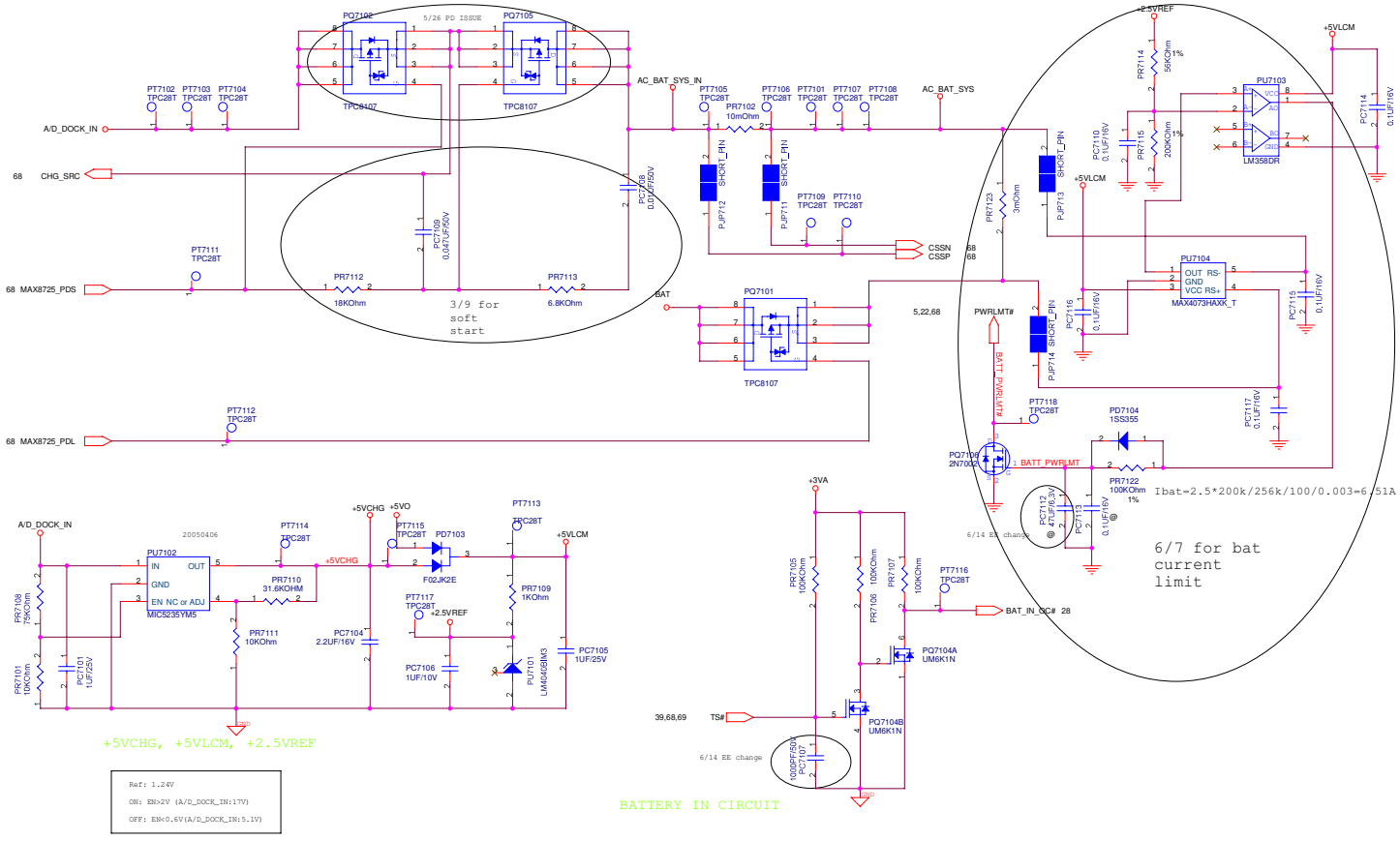


USB



<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 44 OF 55	DESCRIPTION: I/O PORT	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

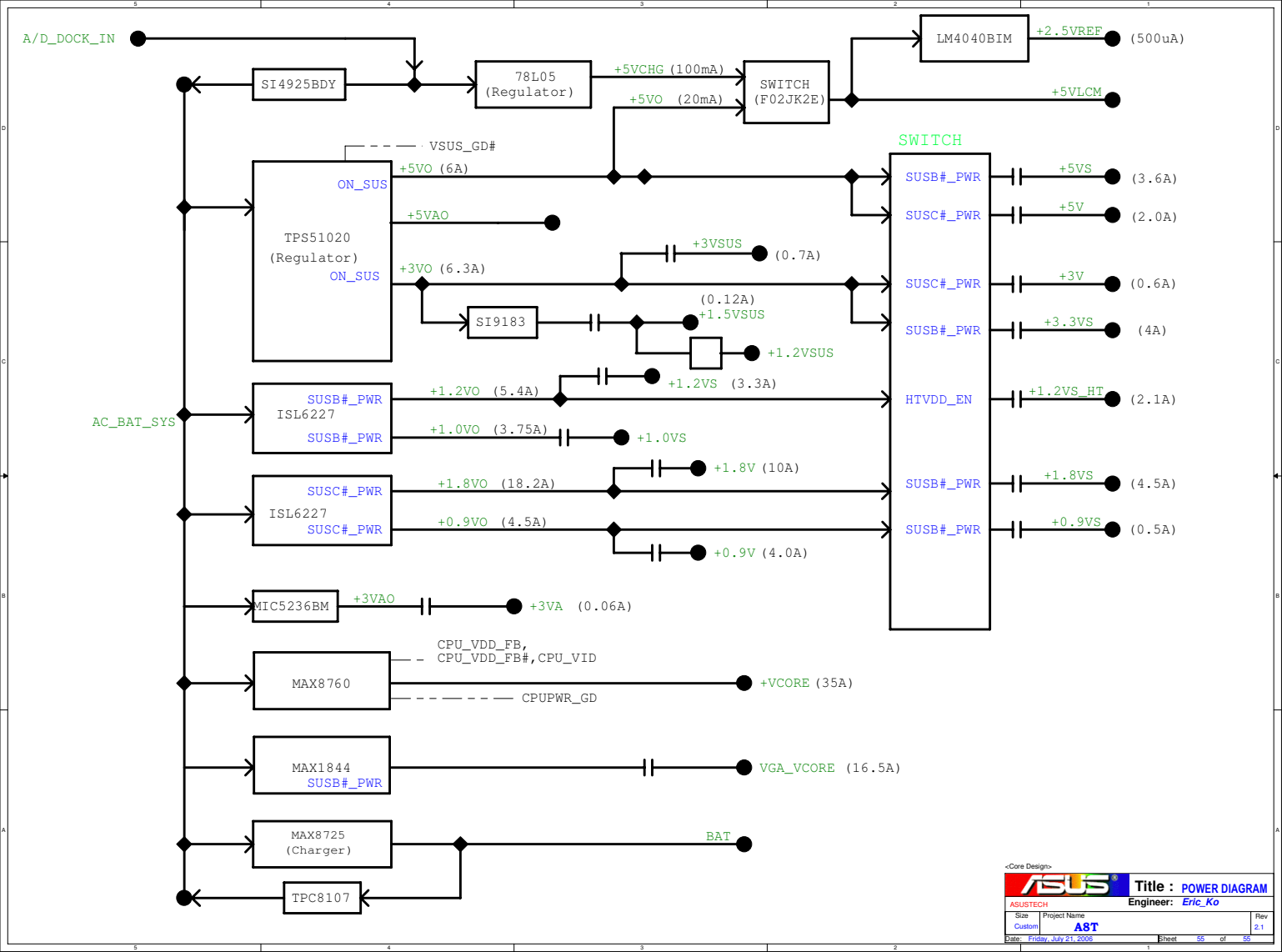
ASUSTECH

Title : POWER_SWITCH_5VLCM

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

Date: Friday, July 21, 2006 Sheet 54 of 55



<Core Design>

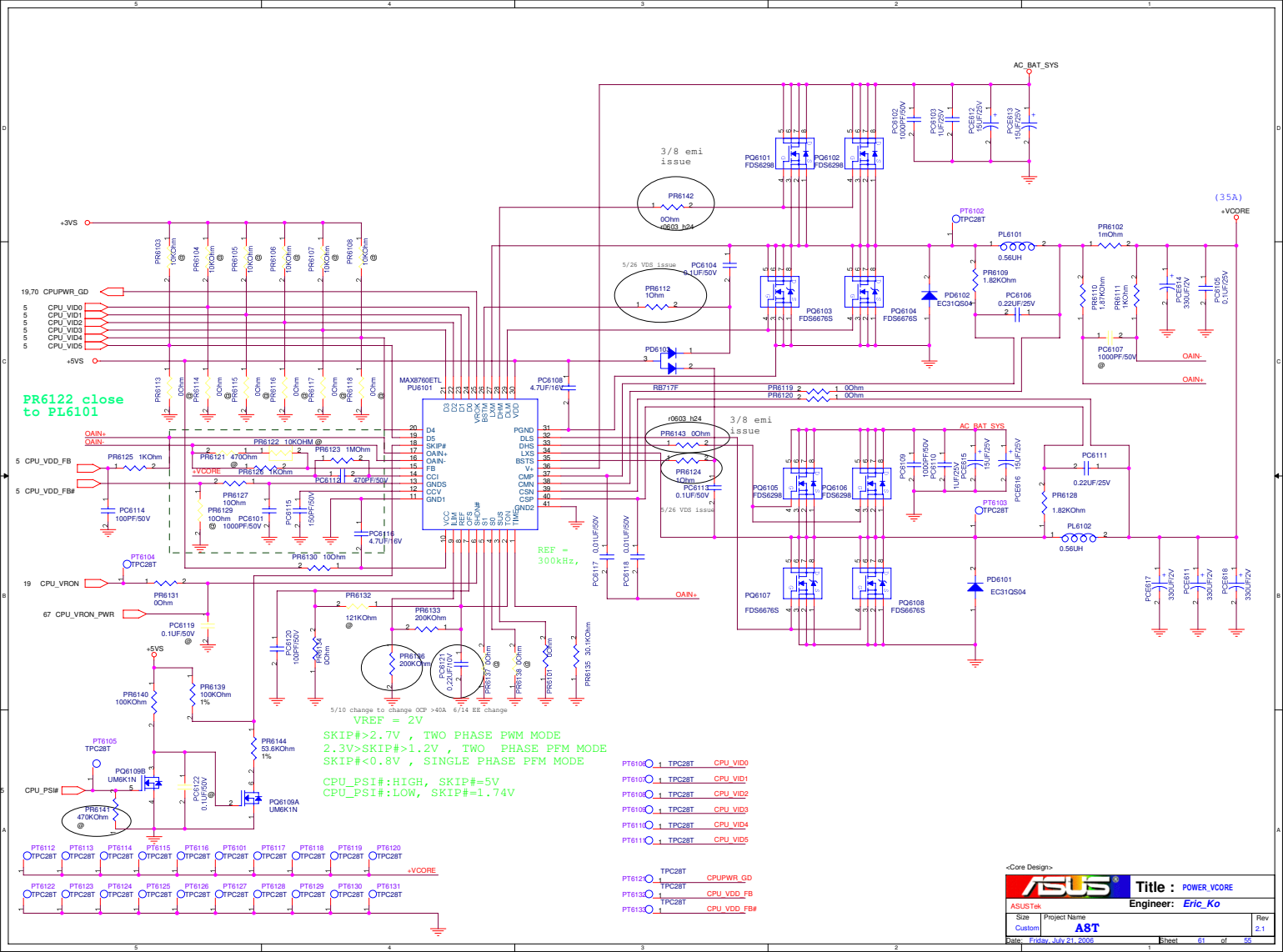
ASUSTECH

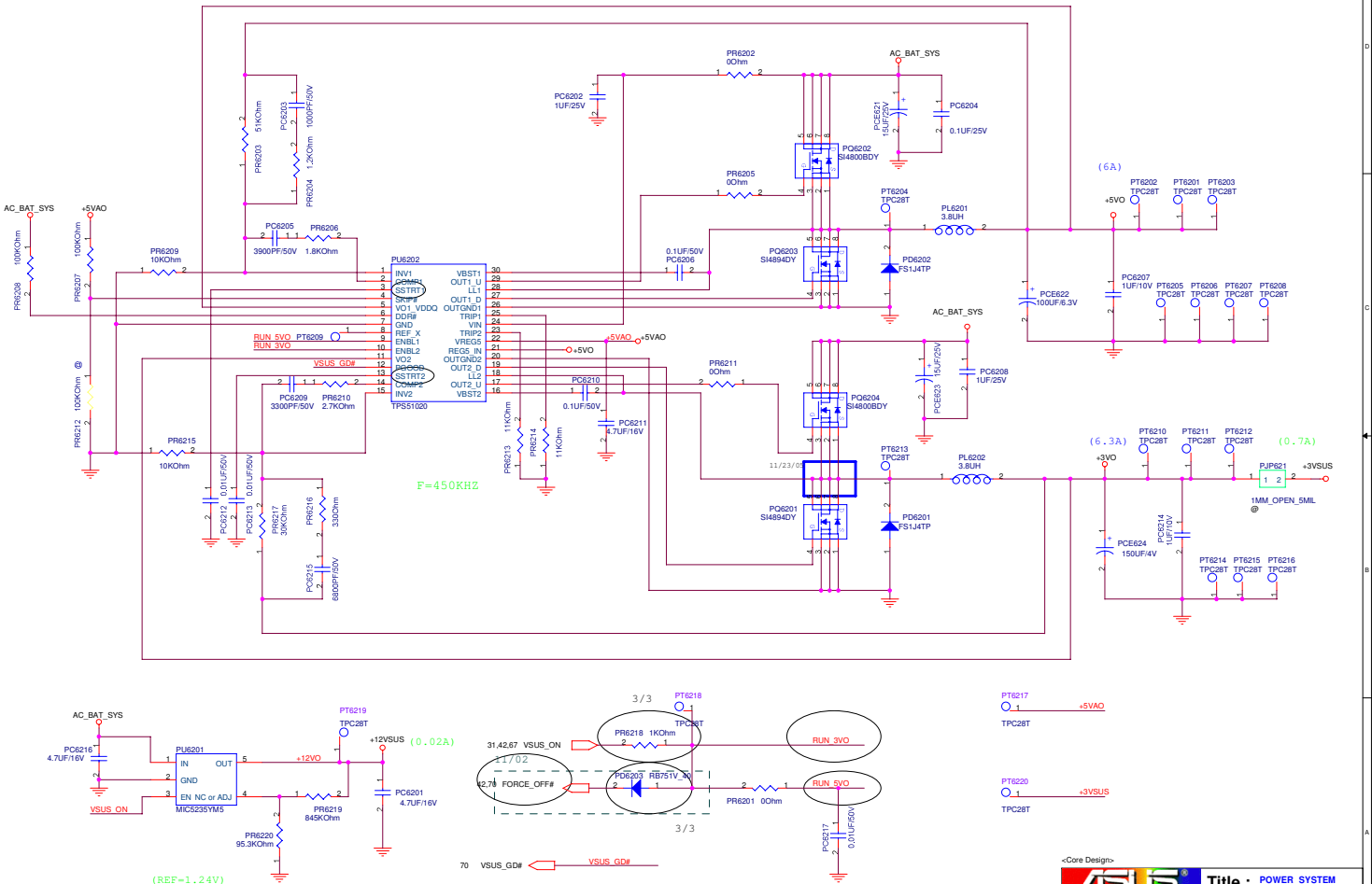
Title : POWER DIAGRAM

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

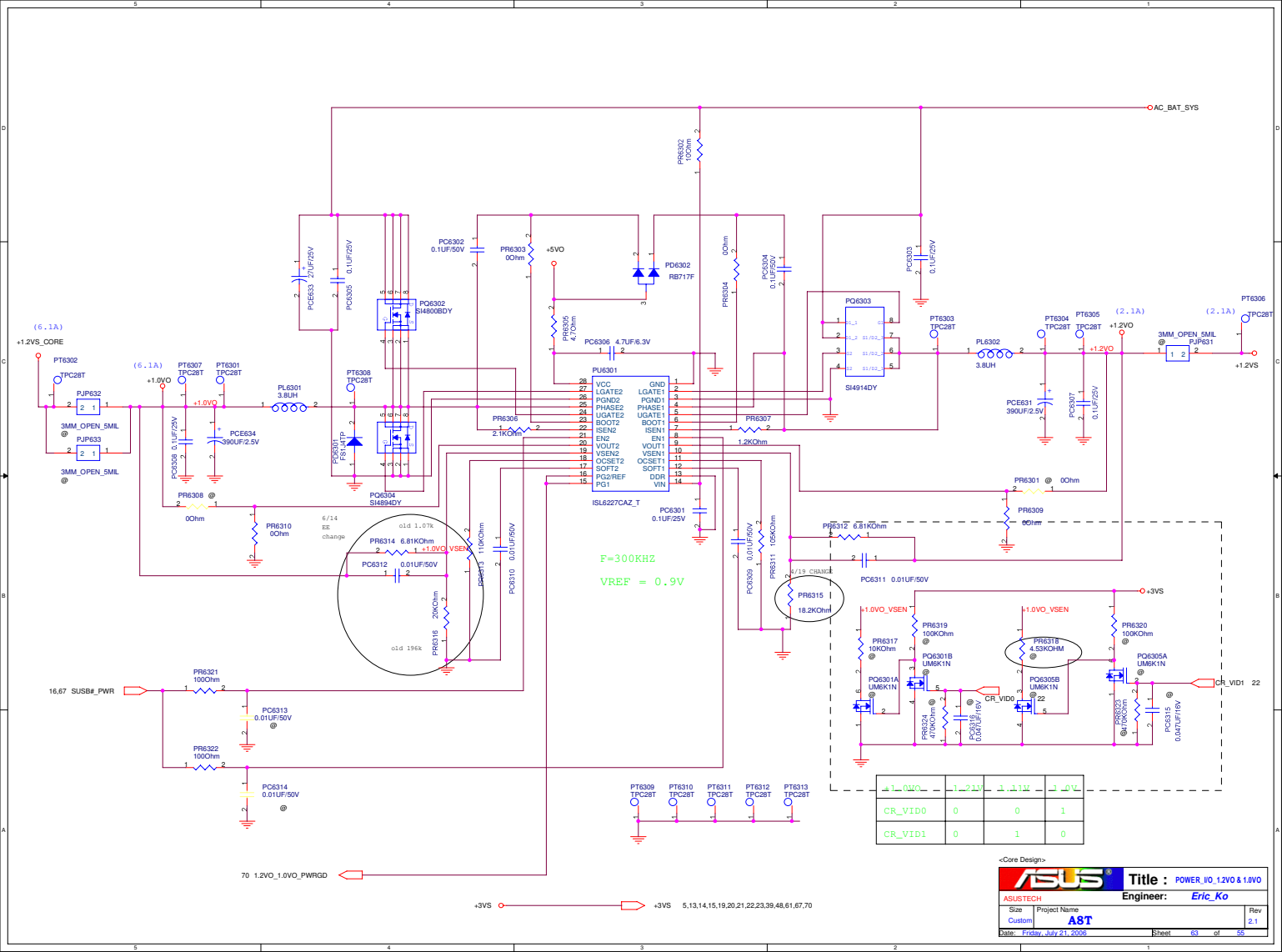
Date: Friday, July 21, 2006 Sheet 55 of 55


AC_BAT_SYS
3/8 emi issue
PR6142 0Ohm r0603_h24
PQ6101 FDS6298
PQ6102 FDS6298
PC6102 1000PF/50V
PC6103 1UF/25V
PC6612 150UF/25V
PC6613 150UF/25V
(35A)
+VCORE
PT6102 TPC28T
PL6101 0.56UH
PR6102 1mOhm
PR6109 1.82KOhm
PD6102 EC31QS04
PC6106 0.22UF/25V
PR6110 1.87KOhm
PR6111 1KOhm
PC6107 1000PF/50V
PC6104 0.1UF/50V
PR6112 1Ohm
5/26 VDS issue
PQ6103 FDS6676S
PQ6104 FDS6676S
PC6105 0.1UF/25V
OAIN-
OAIN+
+3VS
+5VS
19,70 CPUPWR_GD
5 CPU_VID0
5 CPU_VID1
5 CPU_VID2
5 CPU_VID3
5 CPU_VID4
5 CPU_VID5
PR6103 10KOhm
PR6104 10KOhm
PR6105 10KOhm
PR6106 10KOhm
PR6107 10KOhm
PR6108 10KOhm
PR6113 0Ohm
PR6114 0Ohm
PR6115 0Ohm
PR6116 0Ohm
PR6117 0Ohm
PR6118 0Ohm
PR6122 close to PL6101
MAX8760ETL PU6101
PC6108 4.7UF/16V
RB717F
PR6119 0Ohm
PR6120 0Ohm
PD6103
r0603_h24
PR6143 0Ohm
PR6124 10Ohm
PC6113 0.1UF/50V
PR6122 10KOHM
PR6123 1MOhm
PR6121 470Ohm
PC6112 470PF/50V
PR6125 1KOhm
PR6126 1KOhm
PR6127 10Ohm
PR6129 10Ohm
PC6101 1000PF/50V
PC6115 150PF/50V
PC6114 100PF/50V
PC6116 4.7UF/16V
PR6130 10Ohm
PC6117 0.01UF/50V
PC6118 0.01UF/50V
REF = 300kHz,
OAIN+
PQ6105 FDS6298
PQ6106 FDS6298
PC6109 1000PF/50V
PC6110 1UF/25V
PC6615 15UF/25V
PC6616 15UF/25V
PC6111 0.22UF/25V
PR6128 1.82KOhm
PT6103 TPC28T
PL6102 0.56UH
PD6101 EC31QS04
PQ6107 FDS6676S
PQ6108 FDS6676S
PC6617 330UF/2V
PC6611 330UF/2V
PC6618 330UF/2V
19 CPU_VRON
67 CPU_VRON_PWR
PT6104 TPC28T
PR6131 0Ohm
PC6119 0.1UF/50V
PR6132 121KOhm
PR6133 209KOhm
PR6134 0Ohm
PC6120 100PF/50V
PR6136 200KOhm
PC6121 0.22UF/10V
PR6137 0Ohm
PR6138 0Ohm
PR6101 0Ohm
PR6135 30.1KOhm
5/10 change to change OCP >40A 6/14 EE change
VREF = 2V
SKIP#>2.7V , TWO PHASE PWM MODE
2.3V>SKIP#>1.2V , TWO PHASE PFM MODE
SKIP#<0.8V , SINGLE PHASE PFM MODE
CPU_PSI#:HIGH, SKIP#=5V
CPU_PSI#:LOW, SKIP#=1.74V
PR6140 100KOhm
PR6139 100KOhm 1%
PR6144 53.6KOhm 1%
PT6105 TPC28T
CPU_PSI#
PQ6109B UM6K1N
PQ6109A UM6K1N
PC6122 0.1UF/50V
PR6141 470KOhm
PT6112 TPC28T
PT6113 TPC28T
PT6114 TPC28T
PT6115 TPC28T
PT6116 TPC28T
PT6101 TPC28T
PT6117 TPC28T
PT6118 TPC28T
PT6119 TPC28T
PT6120 TPC28T
PT6122 TPC28T
PT6123 TPC28T
PT6124 TPC28T
PT6125 TPC28T
PT6126 TPC28T
PT6127 TPC28T
PT6128 TPC28T
PT6129 TPC28T
PT6130 TPC28T
PT6131 TPC28T
+VCORE
PT6106 TPC28T CPU_VID0
PT6107 TPC28T CPU_VID1
PT6108 TPC28T CPU_VID2
PT6109 TPC28T CPU_VID3
PT6110 TPC28T CPU_VID4
PT6111 TPC28T CPU_VID5
PT6112 TPC28T CPUPWR_GD
PT6132 TPC28T CPU_VDD_FB
PT6133 TPC28T CPU_VDD_FB#
<Core Design>
ASUSTek
Title : POWER_VCORE
Engineer: Eric_Ko
Size Custom
Project Name A8T
Rev 2.1
Date: Friday, July 21, 2006
Sheet 61 of 55



<Core Design>

ASUSTECH	Title : POWER_SYSTEM	
	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 62 of 55	



	1_0VO	1_2VO	1_2VO	1_0VO
CR_VID0	0	0	1	
CR_VID1	0	1	0	

<Core Design>

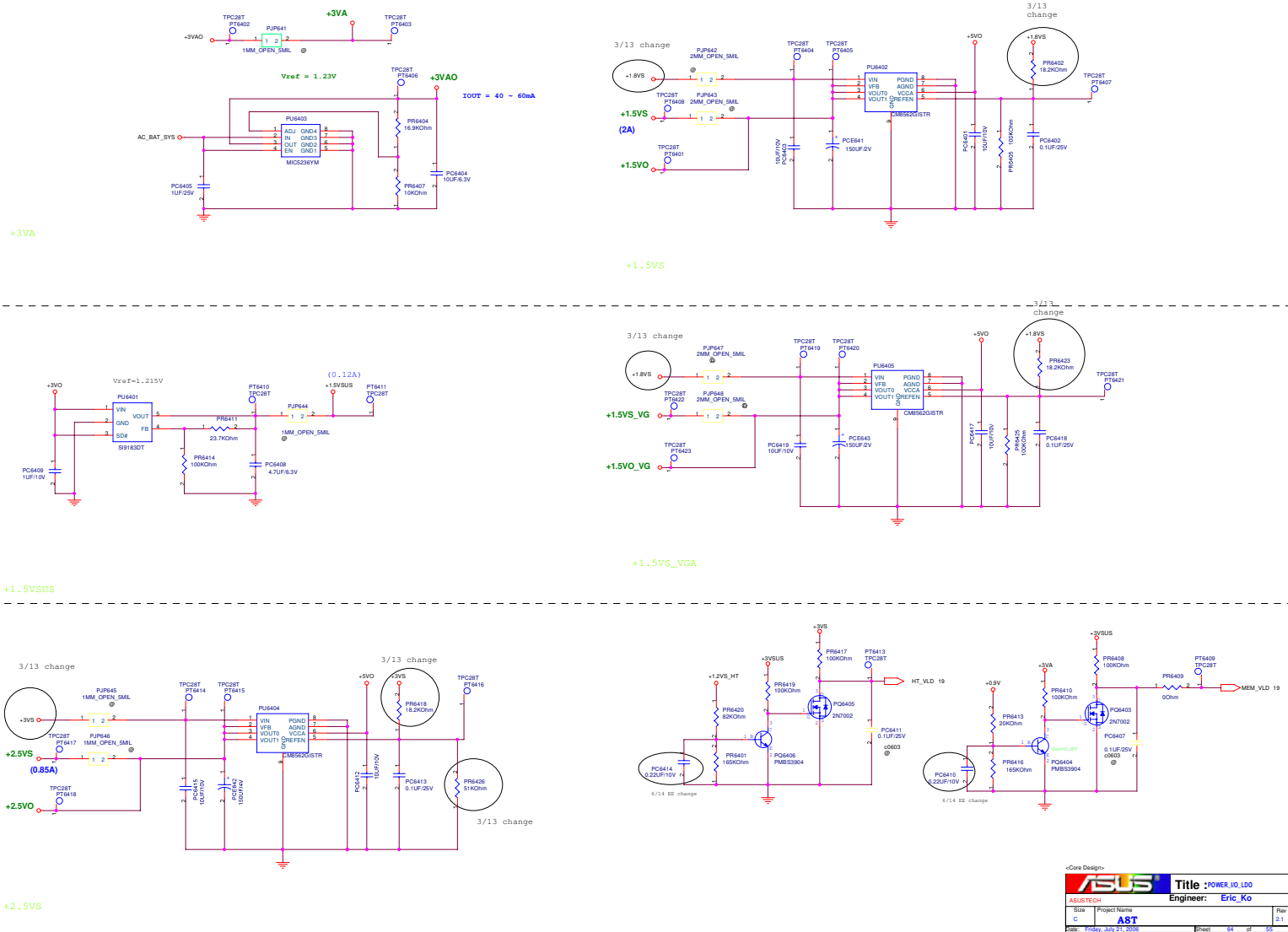
ASUSTECH

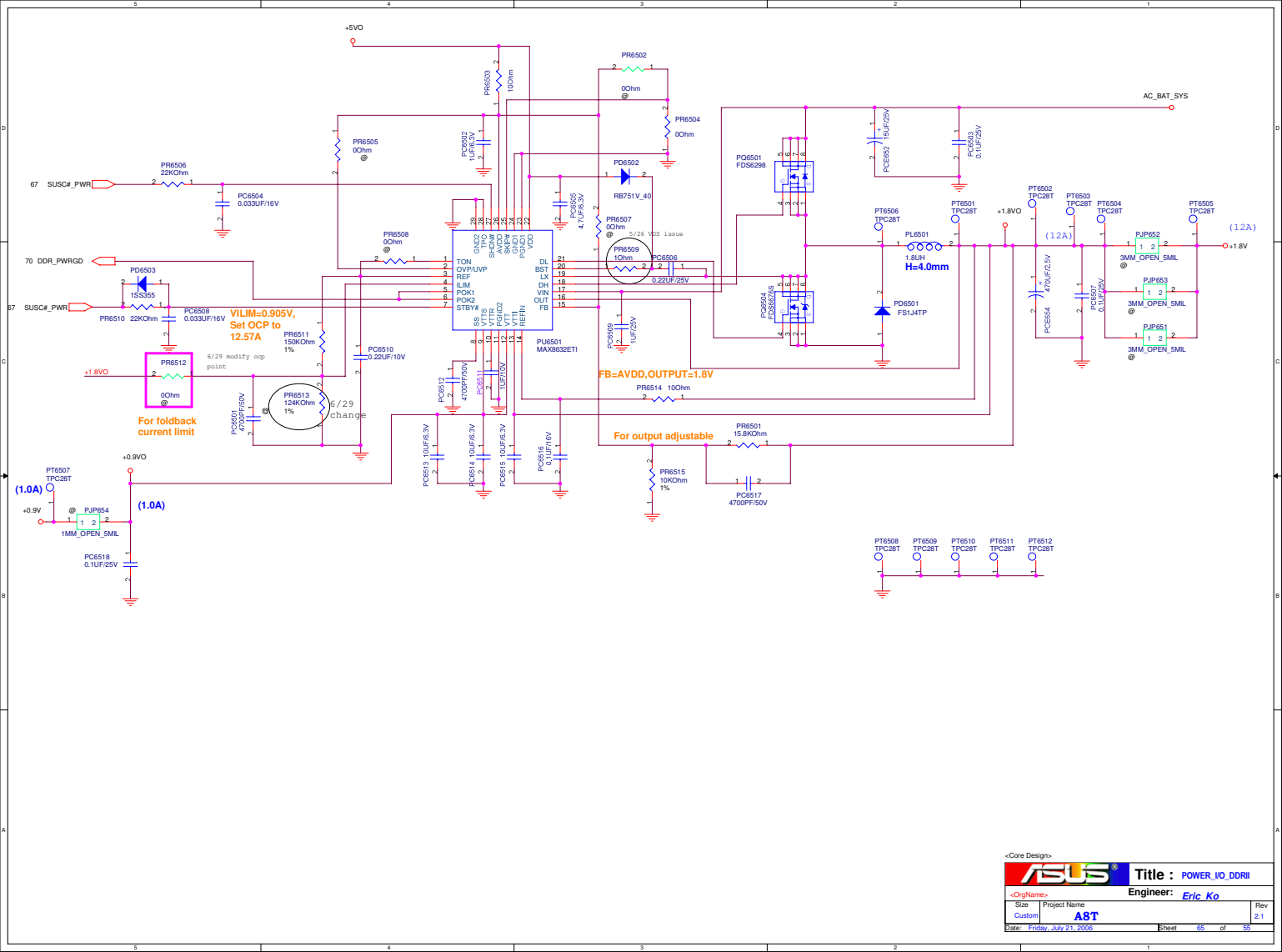
Title : POWER_I/O_1.2VO & 1.0VO

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

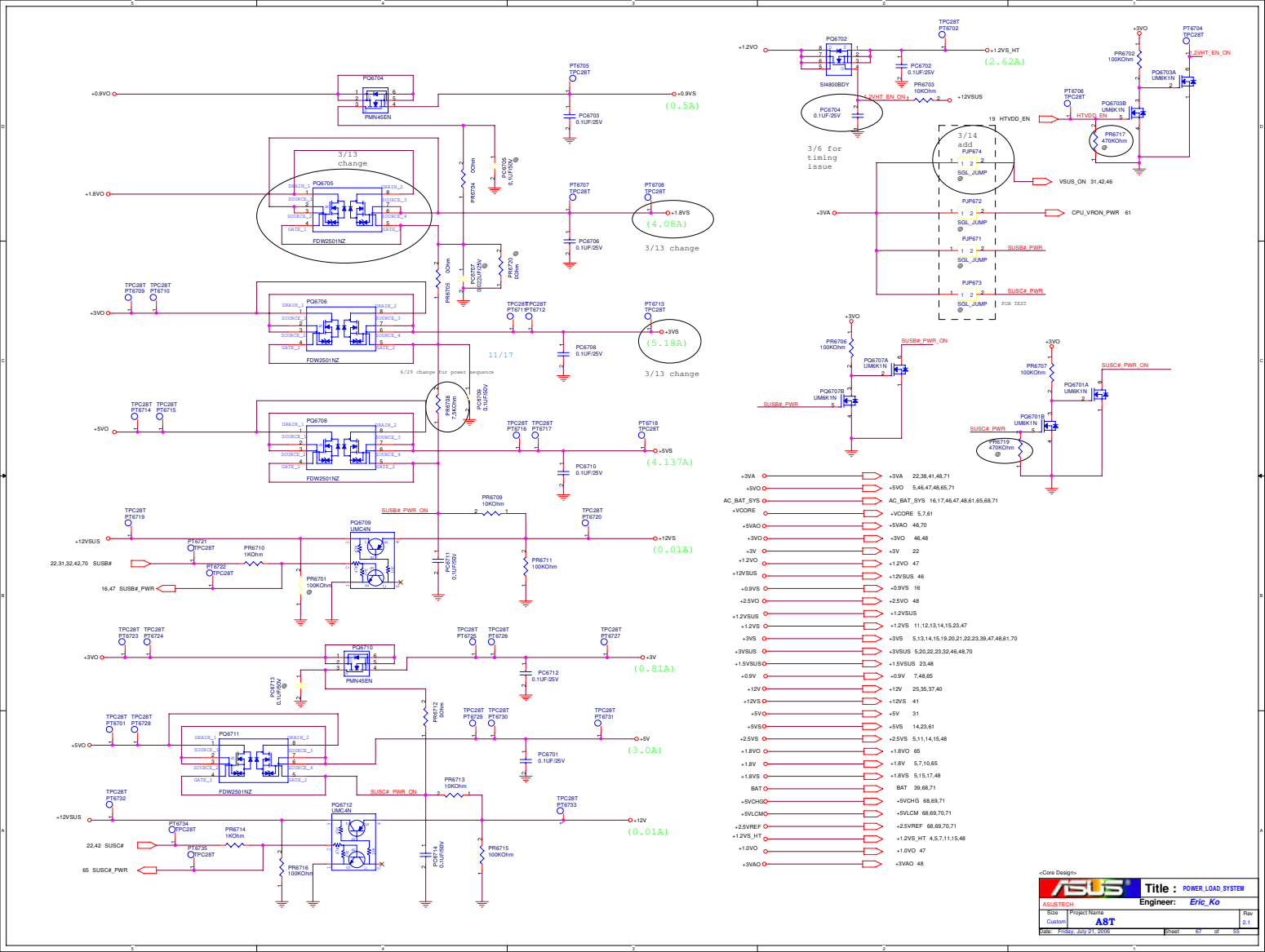
Date: Friday, July 21, 2006 Sheet 63 of 55


+3VA
Vref = 1.23V
+3VAO
IOUT = 40 ~ 60mA
AC_BAT_SYS
MIC5236YM
+1.5VS
(2A)
+1.5VO
3/13 change
+1.5VS_VG
+1.5VO_VG
+1.5VS_VGA
Vref=1.215V
(0.12A)
SI9183DT
+1.5VSUS
+2.5VS
(0.85A)
+2.5VS
+3VS
+5VO
+1.8VS
+1.2VS_HT
HT_VLD 19
MEM_VLD 19
+0.9V
6/14 EE change
CMB5620ISTR
ASUSTECH
Title :POWER_IO_LDO
Engineer: Eric_Ko
A8T
Date: Friday, July 21, 2006
Sheet 64 of 65



<Core Design>

<OrgName>	Title : POWER_I/O_DDRII	
	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 65 of 55	



+3VA	+3VA	22,38,41,48,71
+5VO	+5VO	5,46,47,48,65,71
AC_BAT_SYS	AC_BAT_SYS	16,17,46,47,48,61,65,68,71
+VCORE	+VCORE	5,7,61
+5VAO	+5VAO	46,70
+3VO	+3VO	46,48
+3V	+3V	22
+1.2VO	+1.2VO	47
+12VSUS	+12VSUS	46
+0.9VS	+0.9VS	16
+2.5VO	+2.5VO	48
+1.2VSUS	+1.2VSUS	
+1.2VS	+1.2VS	11,12,13,14,15,23,47
+3VS	+3VS	5,13,14,15,19,20,21,22,23,39,47,48,61,70
+3VSUS	+3VSUS	5,20,22,23,32,46,48,70
+1.5VSUS	+1.5VSUS	23,48
+0.9V	+0.9V	7,48,65
+12V	+12V	25,35,37,40
+12VS	+12VS	41
+5V	+5V	31
+5VS	+5VS	14,23,61
+2.5VS	+2.5VS	5,11,14,15,48
+1.8VO	+1.8VO	65
+1.8V	+1.8V	5,7,10,65
+1.8VS	+1.8VS	5,15,17,48
BAT	BAT	39,68,71
+5VCHGO	+5VCHG	68,69,71
+5VLCMO	+5VLCM	68,69,70,71
+2.5VREF	+2.5VREF	68,69,70,71
+1.2VS_HT	+1.2VS_HT	4,5,7,11,15,48
+1.0VO	+1.0VO	47
+3VAO	+3VAO	48

<Core Design>

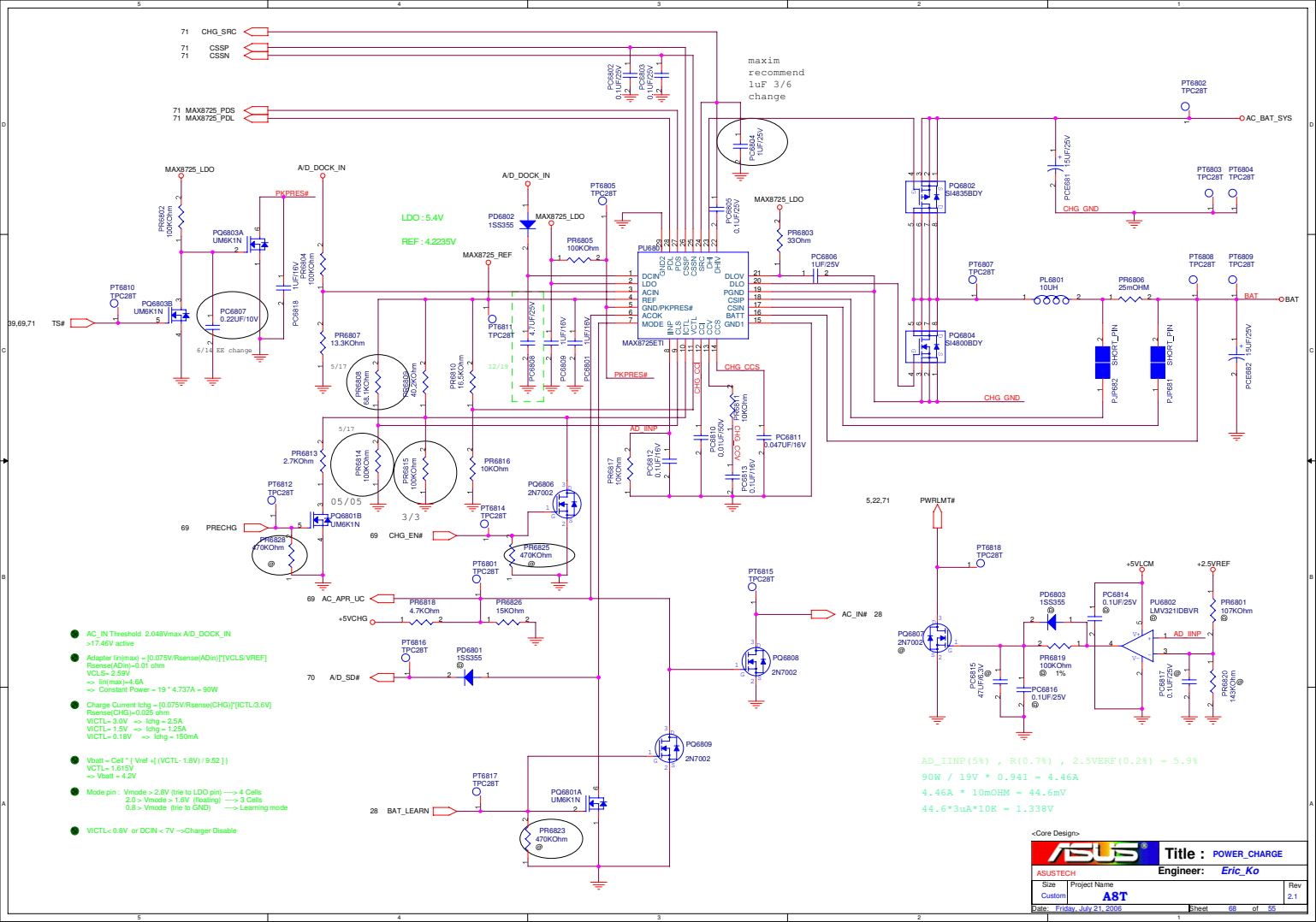
ASUSTECH

Title : POWER_LOAD_SYSTEM

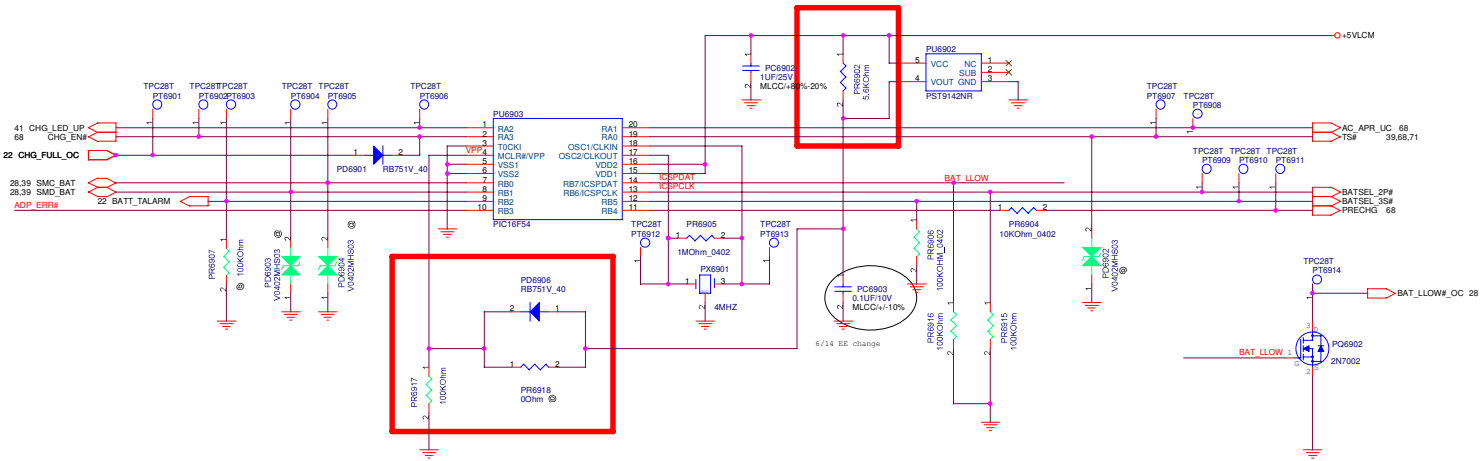
Engineer: Eric_Ko

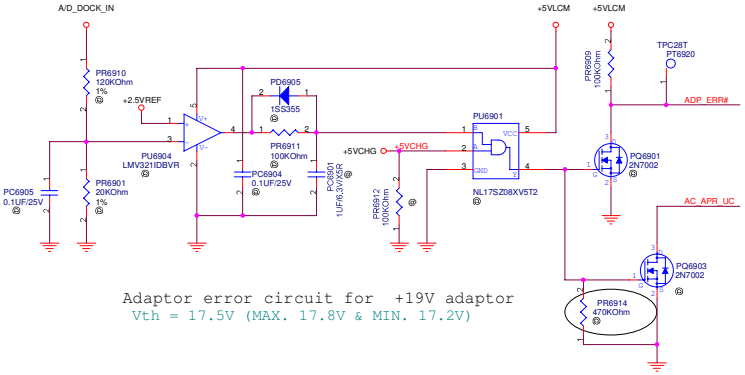
Size	Project Name	Rev
Custom	A8T	2.1

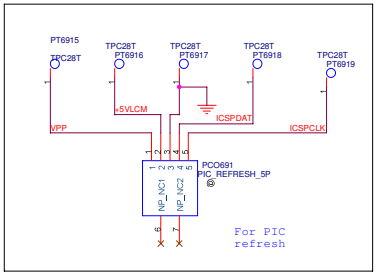
Date: Friday, July 21, 2006 Sheet 67 of 68

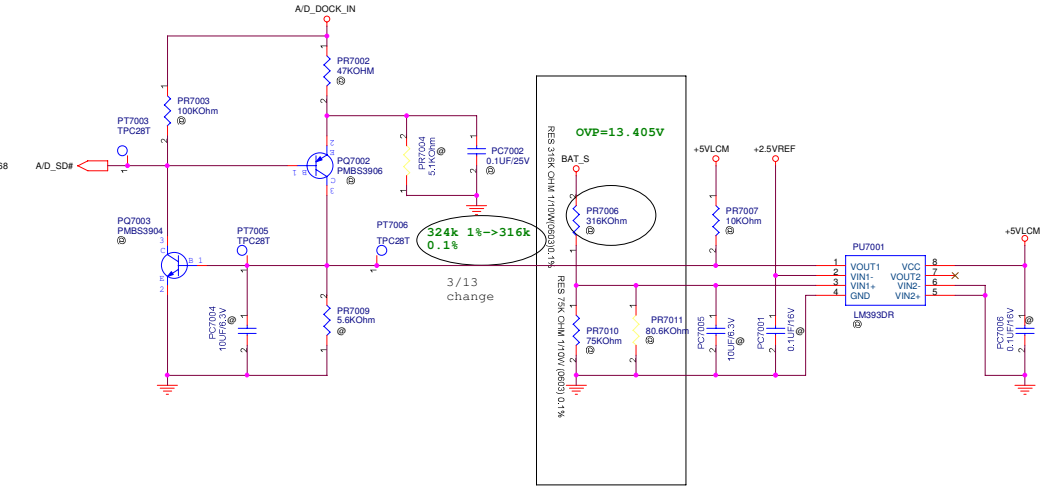

71 CHG_SRC
71 CSSP
71 CSSN
71 MAX8725_PDS
71 MAX8725_PDL
maxim recommend 1uF 3/6 change
AC_BAT_SYS
MAX8725_LDO
A/D_DOCK_IN
PKPRES#
LDO : 5.4V
REF : 4.2235V
MAX8725_REF
MAX8725ETI
CHG_GND
BAT
TS#
PRECHG
CHG_EN#
AC_APR_UC
A/D_SD#
BAT_LEARN
AD_IINP
PWRLMT#
AC_IN#
+5VCHG
+5VLCM
+2.5VREF
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.46V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01 ohm
VCLS= 2.59V
=> Iin(max)=4.6A
=> Constant Power = 19 * 4.737A = 90W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.0V => Ichg = 2.5A
VICTL= 1.5V => Ichg = 1.25A
VICTL= 0.18V => Ichg = 150mA
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.615V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
AD_IINP(5%) , R(0.7%) , 2.5VERF(0.2%) = 5.9%
90W / 19V * 0.941 = 4.46A
4.46A * 10mOHM = 44.6mV
44.6*3uA*10K = 1.338V
<Core Design>
ASUSTECH
Title : POWER_CHARGE
Engineer: Eric_Ko
Size: Custom
Project Name: A8T
Rev: 2.1
Date: Friday, July 21, 2006
Sheet 68 of 55

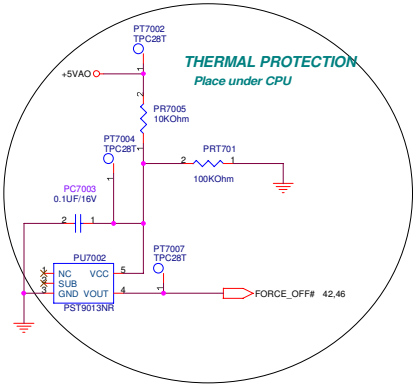
PIC16F54


41 CHG_LED_UP
68 CHG_EN#
22 CHG_FULL_OC
28,39 SMC_BAT
28,39 SMD_BAT
ADP_ERR#
22 BATT_TALARM
TPC28T PT6901
TPC28T PT6902
TPC28T PT6903
TPC28T PT6904
TPC28T PT6905
TPC28T PT6906
PD6901 RB751V_40
PR6907 100KOhm
PD6903 V0402MHS03
PD6904 V0402MHS03
PU6903
PIC16F54
RA2
RA3
T0CKI
MCLR#/VPP
VSS1
VSS2
RB0
RB1
RB2
RB3
RA1
RA0
OSC1/CLKIN
OSC2/CLKOUT
VDD2
VDD1
RB7/ICSPDAT
RB6/ICSPCLK
RB5
RB4
VPP
ICSPDAT
ICSPCLK
PC6902 1UF/25V MLCC/+80%-20%
PR6902 5.6KOhm
PU6902 PST9142NR
+5VLCM
TPC28T PT6907
TPC28T PT6908
AC_APR_UC 68
TS# 39,68,71
TPC28T PT6909
TPC28T PT6910
TPC28T PT6911
BATSEL_2P#
BATSEL_3S#
PRECHG 68
BAT_LLOW
TPC28T PT6912
PR6905 1MOhm_0402
TPC28T PT6913
PX6901 4MHZ
PR6906 100KOHM_0402
PR6904 10KOhm_0402
PD6902 V0402MHS03
PC6903 0.1UF/10V MLCC/+/-10%
PR6916 100KOhm
PR6915 100KOhm
6/14 EE change
TPC28T PT6914
BAT_LLOW#_OC 28
PQ6902 2N7002
PD6906 RB751V_40
PR6917 100KOhm
PR6918 0Ohm

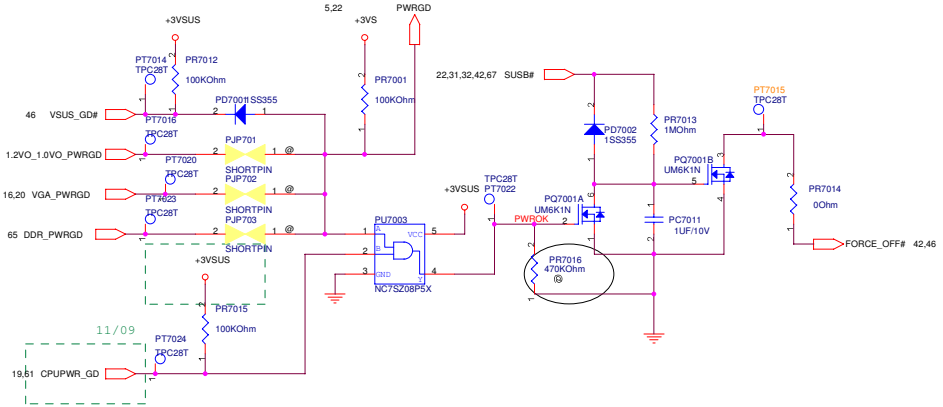

A/D_DOCK_IN
PR6910 120KOhm 1%
+2.5VREF
PU6904 LMV321IDBVR
PC6905 0.1UF/25V
PR6901 20KOhm 1%
PD6905 1SS355
PR6911 100KOhm
PC6904 0.1UF/25V
PC6901 1UF/6.3V/0603
+5VCHG
PR6912 100KOhm
PU6901
NL17SZ08X5T2
+5VLCM
+5VLCM
PR6909 100KOhm
TPC28T PT6920
ADP_ERR#
PQ6901 2N7002
AC_APR_UC
PQ6903 2N7002
PR6914 470KOhm
Adaptor error circuit for +19V adaptor
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)


PT6915
TPC28T PT6916
TPC28T PT6917
TPC28T PT6918
TPC28T PT6919
+5VLCM
VPP
ICSPDAT
ICSPCLK
PCO691 PIC_REFRESH_5P
NP_NC1
NP_NC2
For PIC refresh





6/14 EE change



<Core Design>

ASUSTECH	Title : POWER_PROTECT	
	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 70 of 55	