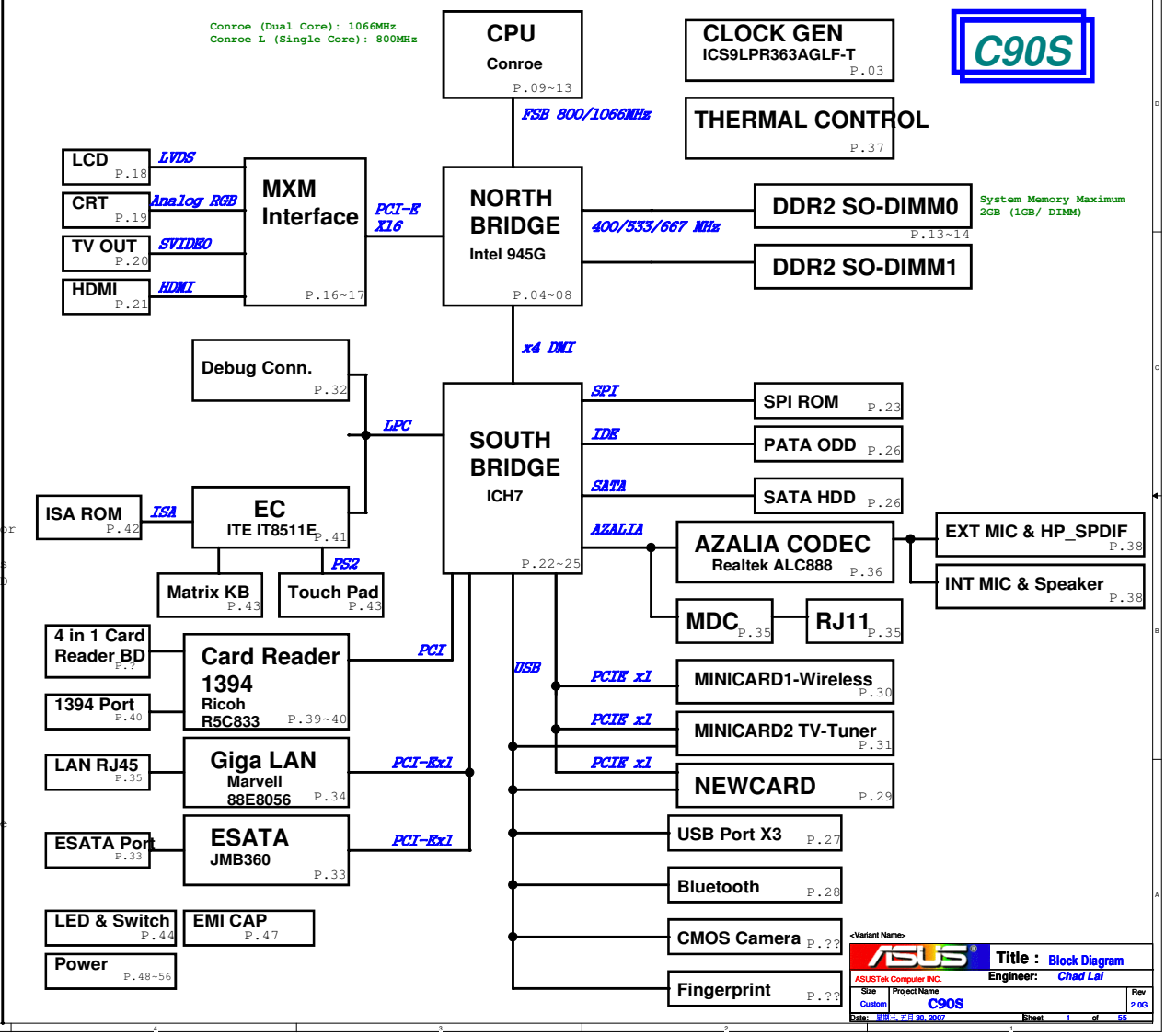
C90S 2.0G

2007_0206_0030



3. <P27>DAUGHTER to 40PIN

Rev	Date	Description
1.0	04/10/06	1. Initial release.(From Z84F)
1.1	08/08/06	1. Change Audio Codec from AD1988B to ALC888(Page 35) 2. Change AJ2, AJ3 to Azalia type 3. Correct RN2 Connection 4. Add PR5312, PR5313 to fix NANYA DIMM S3 fail issue(Page 62) 5. MXM_PWROK : remove R80(Page 19, Page 28) 6. PR5308 change to 1.2K 1% 0603(Page 62) 7. Change Inverter Connector type (12pin) & Pin define CON7(Page 22) 8. Remove : AR1, AR6, AR7, AR8, AR13, AR14, AR15, AR18, AR19, AR21, AR22, AR34, AC1, AC2, AC4, AC5, AC7, AC8, AC11, AC13, AC23, AC25, AC26, AC27, AU2, AQ6, AQ7, AQ9, AQ12 Add : AC81-AC85, AR71, ARN3, AD3, AD4, AL16
	08/10/06	1. Remove T100-T118(Page 41) 2. Add PU5901, PC5905, PC5906 for CIR Power(Page 64) 3. PR5308 change to 150K 1% 0603, PC5312 change to 1500PF 0603(Page 62) 4. Add PR5060, PR5061(Page 61) 5. PR5114 change to 27K 1% 0603(Page 60) 6. PR5722 change to 22K 1% 0603, Stuff PR5721(Page 59) 7. R77 change to 4.7K, Pull to +5VCHG for AC_OK(Page 20) 8. Change connection of L23, L24 9. Change CON18 P/N 10. Add D30, D31, D32, C175, C176, R136(Page 28)
	08/11/06	1. Add Audio Amp. AU100, AR100-AR103, AC100-AC107, non-stuff AC41(Page 36) 2. AC82 change to 1uF 0603, Add AU2, AC23, AC86, AC87, AR72, AR73, AJP1, AJP2, Remove AC12 3. Change MXM SMBus connection to EC, SMB1_CLK, SMB1_DAT(Page 28, Page19)
1.2	08/29/06	1. Change eSATA Controller from Sil3531 to JMB360(Page 31)
1.0G	11/03/2006	1. C90 1.0G Gerber out
1.1G	11/03/2006	ME modify 1. <P46>MB_PAD1 change to None PTH type 2. <P42>Fingerprint & TouchPad Connector change to 12G18340120F 3. <P27>DAUGHTER change to 40PIN 12G171010404 4. <P18>LVDS change to 30PIN 12G17001030P

Rev	Date	Description

<Variant Name>

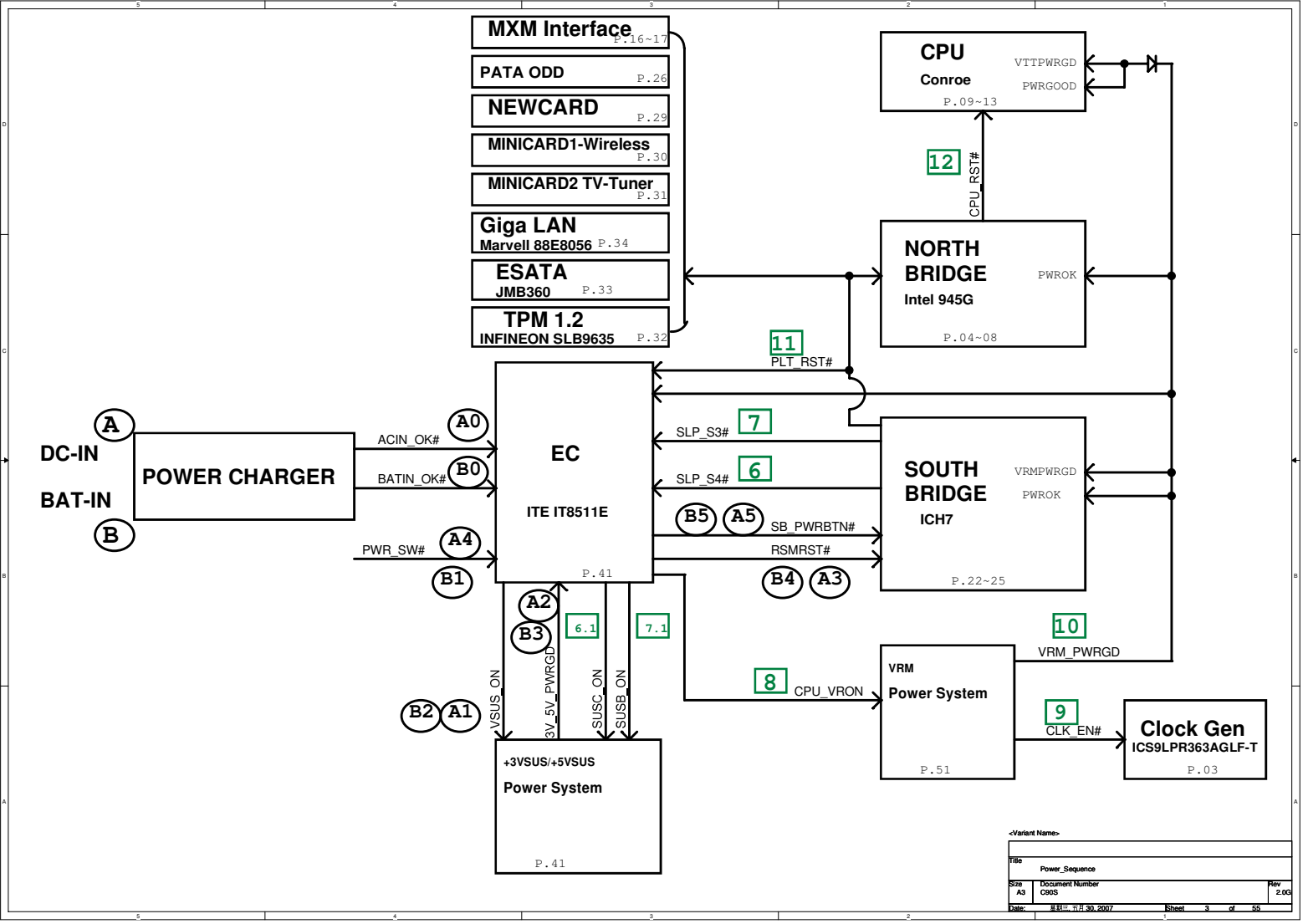
ASUSTek Computer INC.

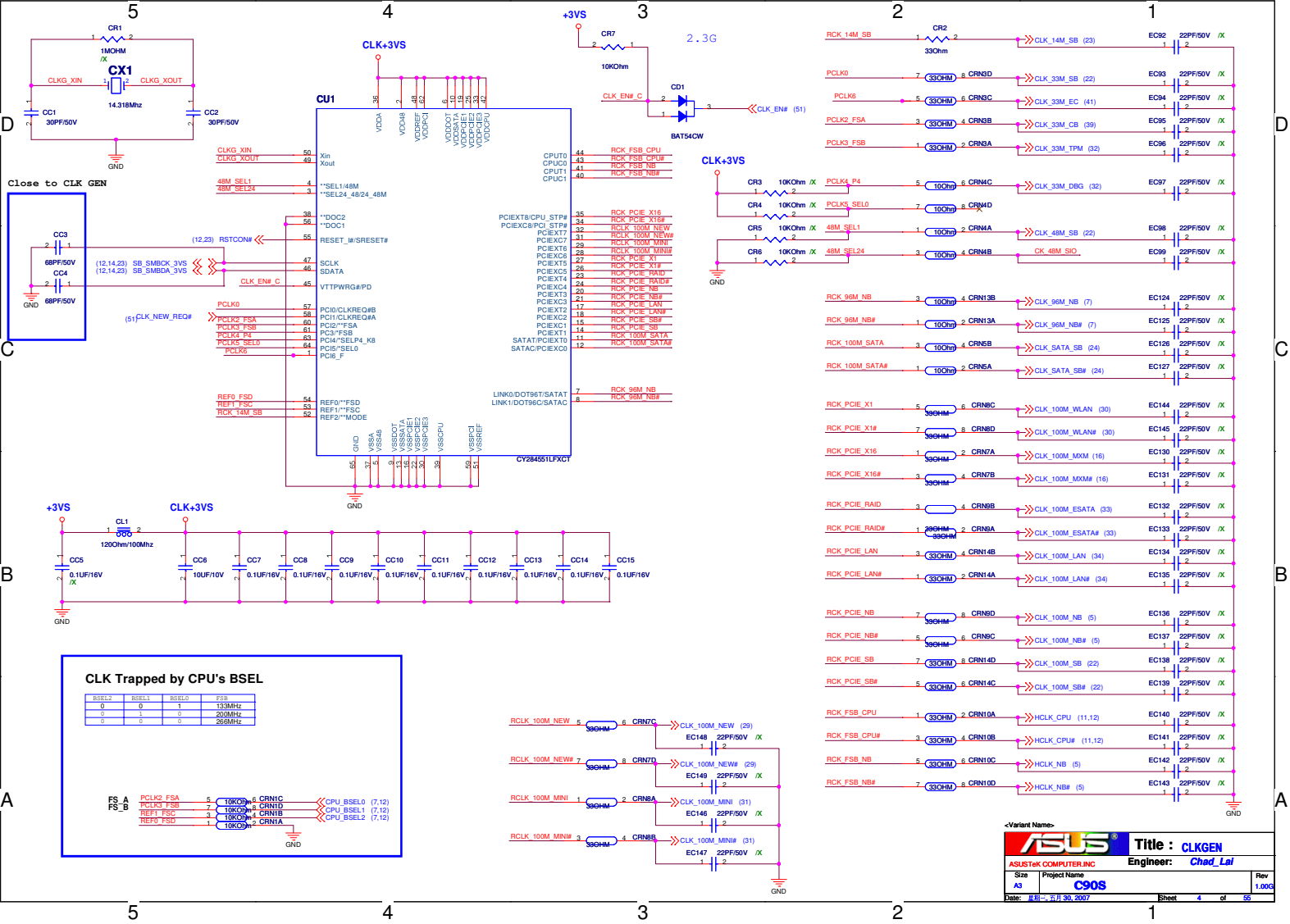
Title : History

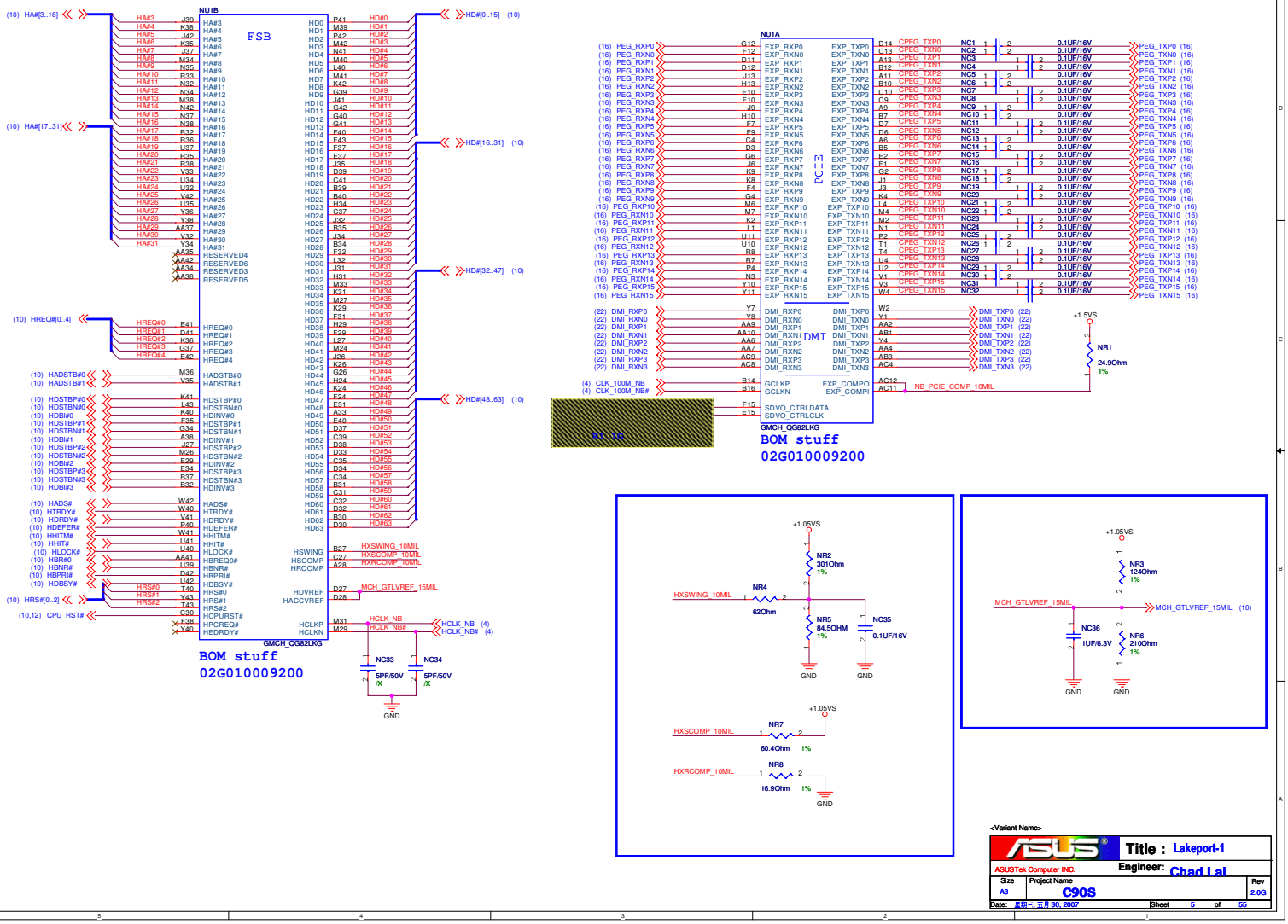
Engineer: Chad Lai

Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 六月 30, 2007 Sheet 2 of 55


MXM Interface
P.16~17
PATA ODD
P.26
NEWCARD
P.29
MINICARD1-Wireless
P.30
MINICARD2 TV-Tuner
P.31
Giga LAN
Marvell 88E8056
P.34
ESATA
JMB360
P.33
TPM 1.2
INFINEON SLB9635
P.32
CPU
Conroe
P.09~13
VTTPWRGD
PWRGOOD
12
CPU_RST#
NORTH BRIDGE
Intel 945G
P.04~08
PWROK
11
PLT_RST#
A
DC-IN
BAT-IN
B
POWER CHARGER
ACIN_OK#
BATIN_OK#
PWR_SW#
A0
B0
A4
B1
EC
ITE IT8511E
P.41
SLP_S3#
7
SLP_S4#
6
B5
A5
SB_PWRBTN#
RSMRST#
B4
A3
SOUTH BRIDGE
ICH7
P.22~25
VRMPWRGD
PWROK
A2
B3
6.1
7.1
10
VRM_PWRGD
VRM
Power System
P.51
8
CPU_VRON
9
CLK_EN#
Clock Gen
ICS9LPR363AGLF-T
P.03
B2
A1
VSUS_ON
3V_5V_PWRGD
SUSC_ON
SUSB_ON
+3VSUS/+5VSUS
Power System
P.41
<Variant Name>
Title
Power_Sequence
Size
A3
Document Number
C90S
Rev
2.0G
Date:
星期三, 六月 30, 2007
Sheet
3
of
55


CR1
1MOHM
/X
CX1
CLKG_XIN
CLKG_XOUT
14.318Mhz
CC1
30PF/50V
CC2
30PF/50V
GND
CLK+3VS
CU1
VDDA
VDD48
VDDREF
VDDPCI
VDDDOT
VDDSATA
VDDPCIE1
VDDPCIE2
VDDPCIE3
VDDCPU
CLKG_XIN
CLKG_XOUT
Xin
Xout
48M_SEL1
48M_SEL24
**SEL1/48M
**SEL24_48/24_48M
**DOC2
**DOC1
(12,23) RSTCON#
RESET_I#/SRESET#
(12,14,23) SB_SMBCK_3VS
(12,14,23) SB_SMBDA_3VS
SCLK
SDATA
CLK_EN# C
VTTPWRG#/PD
(51) CLK_NEW_REQ#
PCLK0
PCLK2_FSA
PCLK3_FSB
PCLK4_P4
PCLK5_SEL0
PCLK6
PCI0/CLKREQ#B
PCI1/CLKREQ#A
PCI2/**FSA
PCI3/*FSB
PCI4/*SELP4_K8
PCI5/*SEL0
PCI6_F
REF0_FSD
REF1_FSC
RCK_14M_SB
REF0/**FSD
REF1/**FSC
REF2/**MODE
GND
VSSA
VSSA48
VSSDOT
VSSPCI
VSSPCIE1
VSSPCIE2
VSSPCIE3
VSSCPU
VSSPCI
VSSREF
CY284551LFXCT
CPUT0
CPUC0
CPUT1
CPUC1
RCK_FSB_CPU
RCK_FSB_CPU#
RCK_FSB_NB
RCK_FSB_NB#
PCIEXT8/CPU_STP#
PCIEXC8/PCI_STP#
PCIEXT7
PCIEXC7
PCIEXT6
PCIEXC6
PCIEXT5
PCIEXC5
PCIEXT4
PCIEXC4
PCIEXT3
PCIEXC3
PCIEXT2
PCIEXC2
PCIEXC1
PCIEXT1
SATAT/PCIEXT0
SATAC/PCIEXC0
RCK_PCIE_X16
RCK_PCIE_X16#
RCK_100M_NEW
RCK_100M_NEW#
RCK_100M_MINI
RCK_100M_MINI#
RCK_PCIE_X1
RCK_PCIE_X1#
RCK_PCIE_RAID
RCK_PCIE_RAID#
RCK_PCIE_NB
RCK_PCIE_NB#
RCK_PCIE_LAN
RCK_PCIE_LAN#
RCK_PCIE_SB
RCK_PCIE_SB#
RCK_100M_SATA
RCK_100M_SATA#
LINK0/DOT96T/SATAT
LINK1/DOT96C/SATAC
RCK_96M_NB
RCK_96M_NB#
+3VS
CR7
10KOhm
2.3G
CLK_EN# C
CD1
BAT54CW
CLK_EN# (51)
CLK+3VS
CR3 10KOhm /X
CR4 10KOhm /X
CR5 10KOhm /X
CR6 10KOhm /X
PCLK4_P4
PCLK5_SEL0
48M_SEL1
48M_SEL24
GND
Close to CLK GEN
CC3
68PF/50V
CC4
68PF/50V
GND
+3VS
CL1
120Ohm/100Mhz
CLK+3VS
CC5 0.1UF/16V /X
CC6 10UF/10V
CC7 0.1UF/16V
CC8 0.1UF/16V
CC9 0.1UF/16V
CC10 0.1UF/16V
CC11 0.1UF/16V
CC12 0.1UF/16V
CC13 0.1UF/16V
CC14 0.1UF/16V
CC15 0.1UF/16V
GND
CLK Trapped by CPU's BSEL
BSEL2 BSEL1 BSEL0 FSB
0 0 1 133MHz
0 1 0 200MHz
0 0 0 266MHz
FS_A
FS_B
PCLK2_FSA
PCLK3_FSB
REF1_FSC
REF0_FSD
10KOhm CRN1C
10KOhm CRN1D
10KOhm CRN1B
10KOhm CRN1A
CPU_BSEL0 (7,12)
CPU_BSEL1 (7,12)
CPU_BSEL2 (7,12)
GND
RCK_14M_SB
CR2
33Ohm
CLK_14M_SB (23)
EC92 22PF/50V /X
PCLK0
33OHM CRN3D
CLK_33M_SB (22)
EC93 22PF/50V /X
PCLK6
33OHM CRN3C
CLK_33M_EC (41)
EC94 22PF/50V /X
PCLK2_FSA
33OHM CRN3B
CLK_33M_CB (39)
EC95 22PF/50V /X
PCLK3_FSB
33OHM CRN3A
CLK_33M_TPM (32)
EC96 22PF/50V /X
10Ohm CRN4C
CLK_33M_DBG (32)
EC97 22PF/50V /X
10Ohm CRN4D
10Ohm CRN4A
CLK_48M_SB (22)
EC98 22PF/50V /X
10Ohm CRN4B
CK_48M_SIO
EC99 22PF/50V /X
RCK_96M_NB
10Ohm CRN13B
CLK_96M_NB (7)
EC124 22PF/50V /X
RCK_96M_NB#
10Ohm CRN13A
CLK_96M_NB# (7)
EC125 22PF/50V /X
RCK_100M_SATA
10Ohm CRN5B
CLK_SATA_SB (24)
EC126 22PF/50V /X
RCK_100M_SATA#
10Ohm CRN5A
CLK_SATA_SB# (24)
EC127 22PF/50V /X
RCK_PCIE_X1
39OHM CRN8C
CLK_100M_WLAN (30)
EC144 22PF/50V /X
RCK_PCIE_X1#
39OHM CRN8D
CLK_100M_WLAN# (30)
EC145 22PF/50V /X
RCK_PCIE_X16
39OHM CRN7A
CLK_100M_MXM (16)
EC130 22PF/50V /X
RCK_PCIE_X16#
39OHM CRN7B
CLK_100M_MXM# (16)
EC131 22PF/50V /X
RCK_PCIE_RAID
CRN9B
CLK_100M_ESATA (33)
EC132 22PF/50V /X
RCK_PCIE_RAID#
39OHM CRN9A
CLK_100M_ESATA# (33)
EC133 22PF/50V /X
RCK_PCIE_LAN
33OHM CRN14B
CLK_100M_LAN (34)
EC134 22PF/50V /X
RCK_PCIE_LAN#
33OHM CRN14A
CLK_100M_LAN# (34)
EC135 22PF/50V /X
RCK_PCIE_NB
39OHM CRN9D
CLK_100M_NB (5)
EC136 22PF/50V /X
RCK_PCIE_NB#
39OHM CRN9C
CLK_100M_NB# (5)
EC137 22PF/50V /X
RCK_PCIE_SB
33OHM CRN14D
CLK_100M_SB (22)
EC138 22PF/50V /X
RCK_PCIE_SB#
33OHM CRN14C
CLK_100M_SB# (22)
EC139 22PF/50V /X
RCK_FSB_CPU
33OHM CRN10A
HCLK_CPU (11,12)
EC140 22PF/50V /X
RCK_FSB_CPU#
33OHM CRN10B
HCLK_CPU# (11,12)
EC141 22PF/50V /X
RCK_FSB_NB
33OHM CRN10C
HCLK_NB (5)
EC142 22PF/50V /X
RCK_FSB_NB#
33OHM CRN10D
HCLK_NB# (5)
EC143 22PF/50V /X
GND
RCLK_100M_NEW
39OHM CRN7C
CLK_100M_NEW (29)
EC148 22PF/50V /X
RCLK_100M_NEW#
39OHM CRN7D
CLK_100M_NEW# (29)
EC149 22PF/50V /X
RCLK_100M_MINI
39OHM CRN8A
CLK_100M_MINI (31)
EC146 22PF/50V /X
RCLK_100M_MINI#
39OHM CRN8B
CLK_100M_MINI# (31)
EC147 22PF/50V /X
GND
<Variant Name>
ASUSTeK COMPUTER.INC
Title : CLKGEN
Engineer: Chad_Lai
Size A3
Project Name C90S
Rev 1.00G
Date: 星期一, 五月 30, 2007
Sheet 4 of 55



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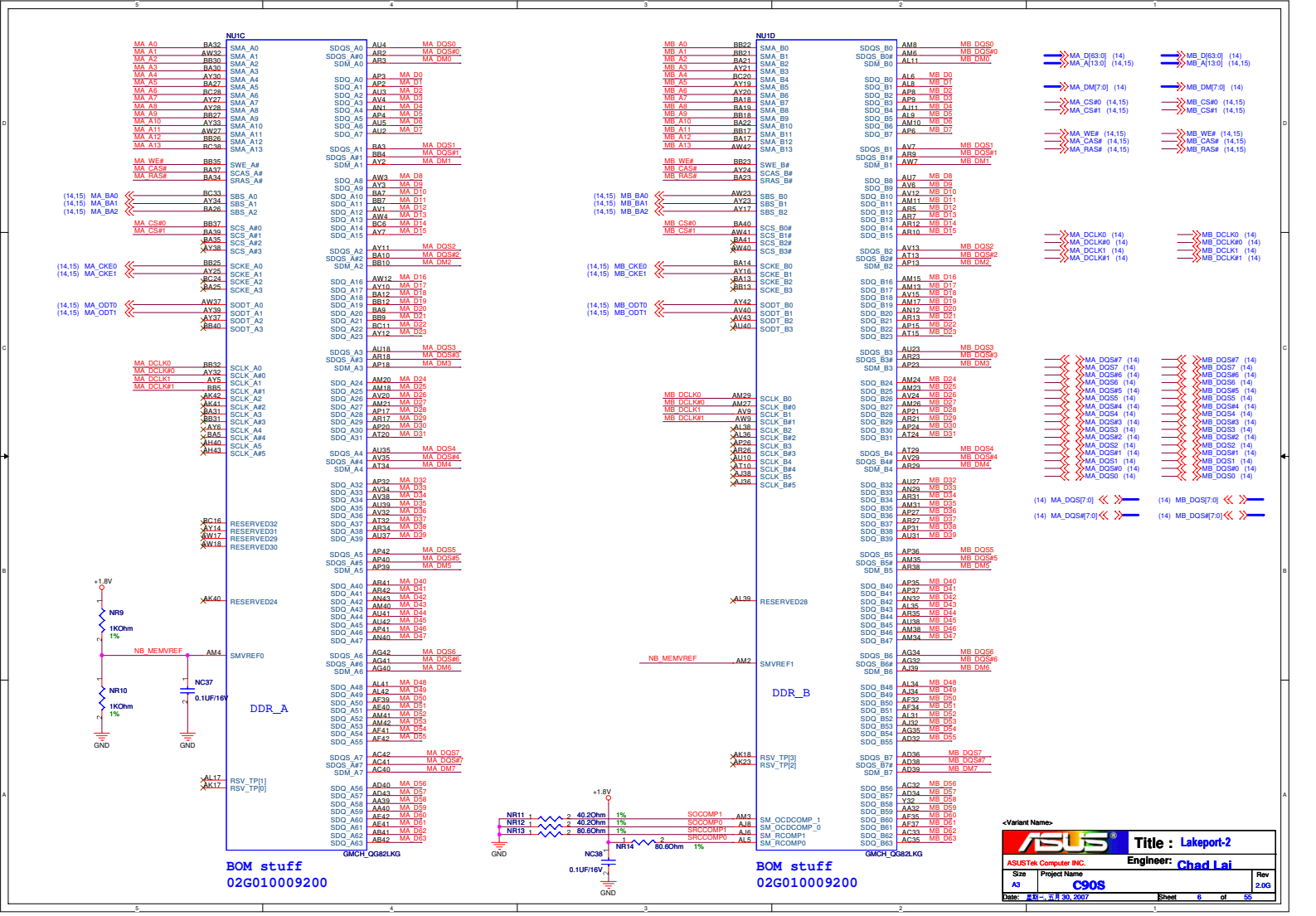
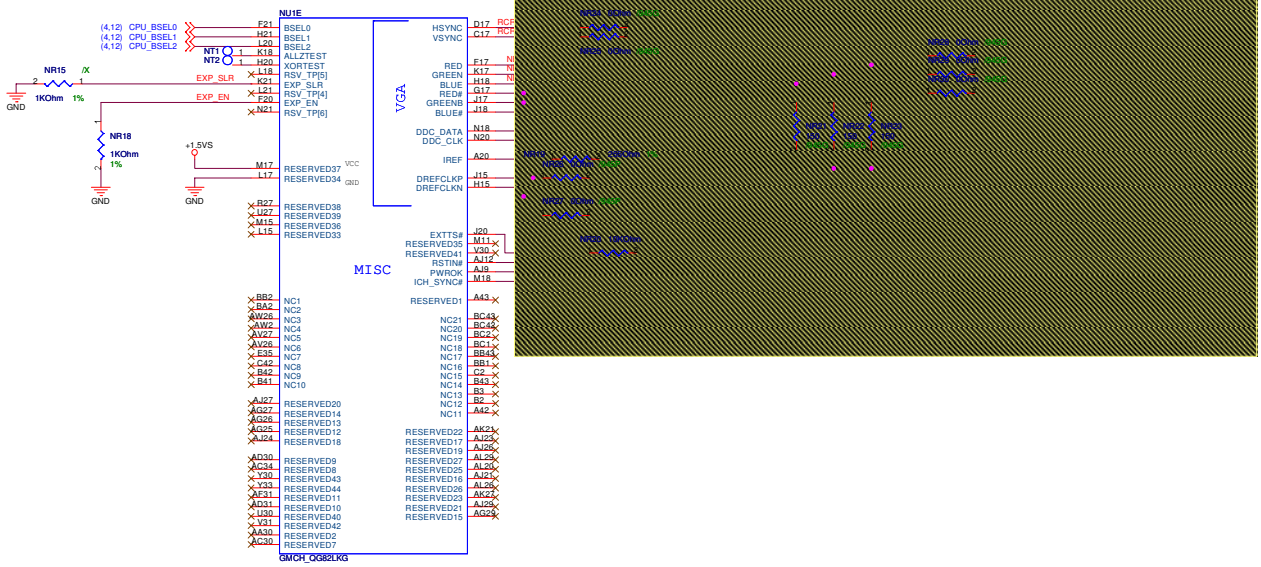
ASUSTek Computer INC.	Title : Lakeport-1	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期一, 五月 30, 2007	Sheet 5 of 55	


NU1C
NU1D
DDR_A
DDR_B
BOM stuff
02G010009200
GMCH_QG82LKG
NR9
1KOhm
1%
NR10
NC37
0.1UF/16V
NB_MEMVREF
NR11
NR12
NR13
40.2Ohm
80.6Ohm
NR14
NC38
SOCOMP1
SOCOMP0
SRCCOMP1
SRCCOMP0
SM_OCDCOMP_1
SM_OCDCOMP_0
SM_RCOMP1
SM_RCOMP0
+1.8V
GND
<Variant Name>
Title : Lakeport-2
ASUSTek Computer INC.
Engineer: Chad Lai
Size A3
Project Name C90S
Rev 2.0G
Date: 星期一, 五月 30, 2007
Sheet 6 of 55

* EXP_SLR : PCIEX16 Lane Reversal Strap Selection
0 : Reverse
1 : Normal (IPU)



<Variant Name>

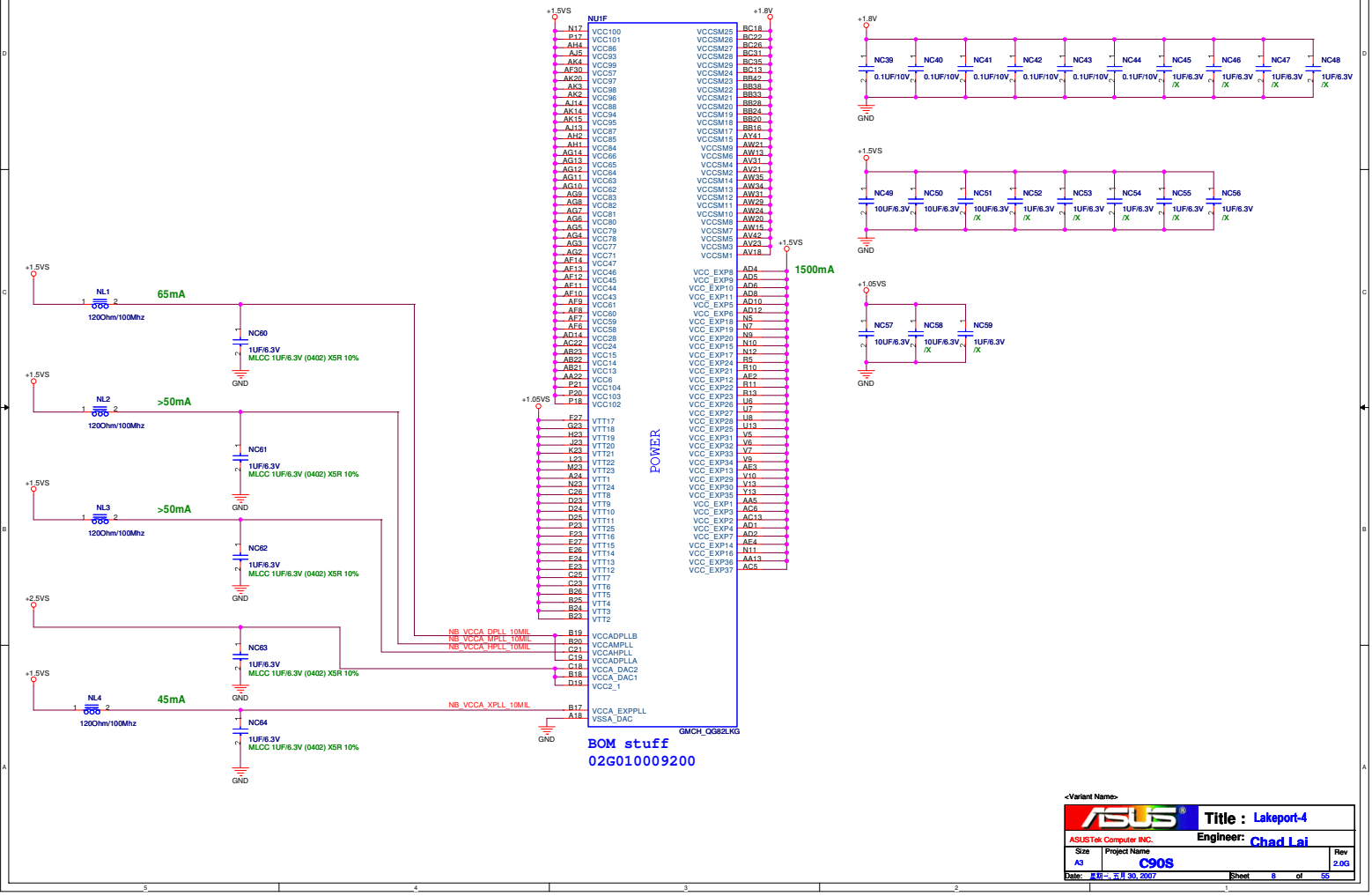
ASUSTek Computer INC.

Title : Lakeport-3

Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期一, 五月 30, 2007 Sheet 7 of 55



<Variant Name>

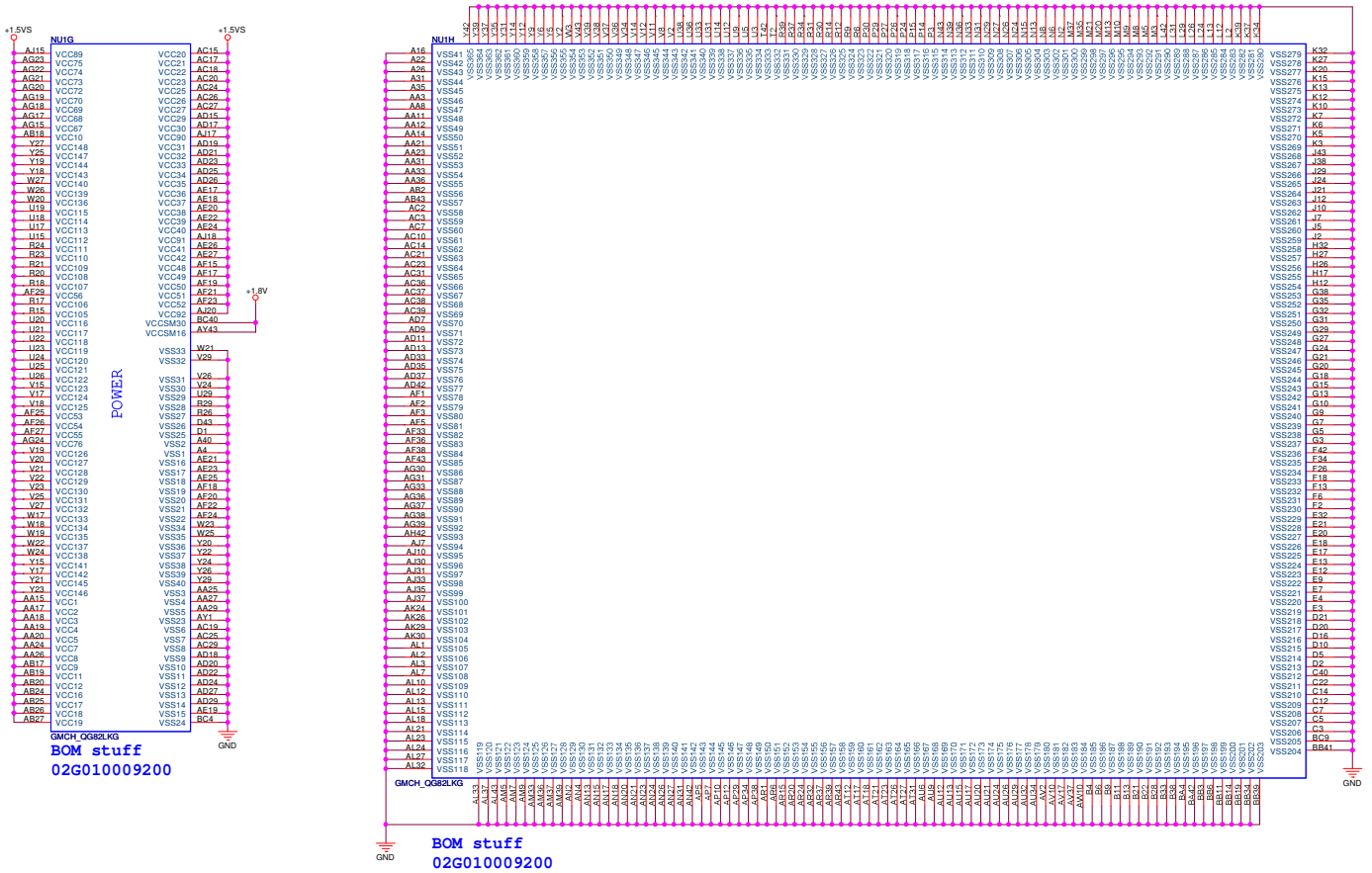
ASUSTek Computer INC.

Title : Lakeport-4

Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期一, 五月 30, 2007 Sheet 8 of 55



<Variant Name>

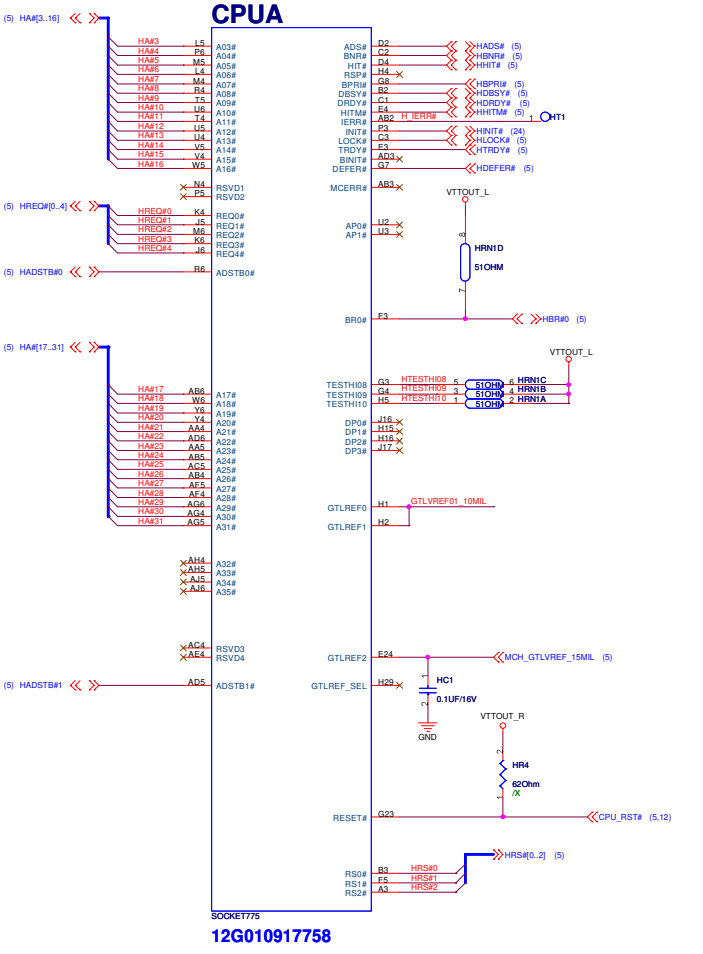
ASUSTek Computer INC.

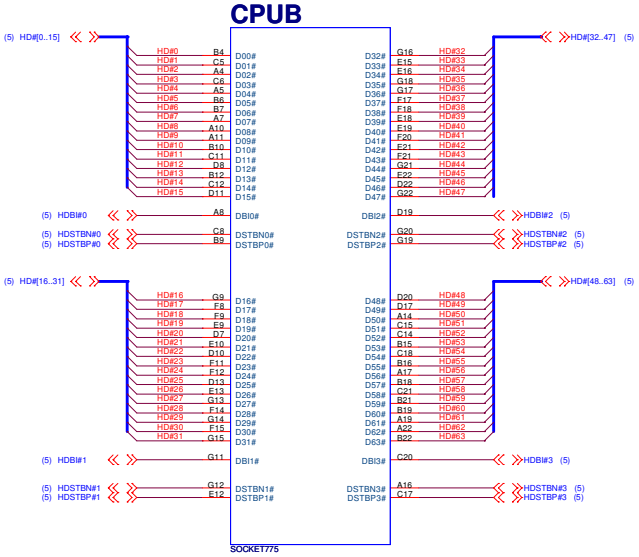
Title : Lakeport -5

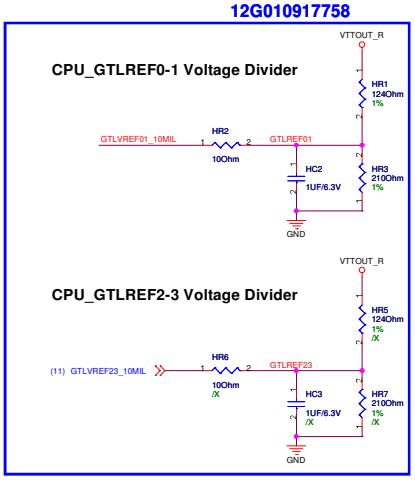
Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期一, 五月 30, 2007 Sheet 9 of 55



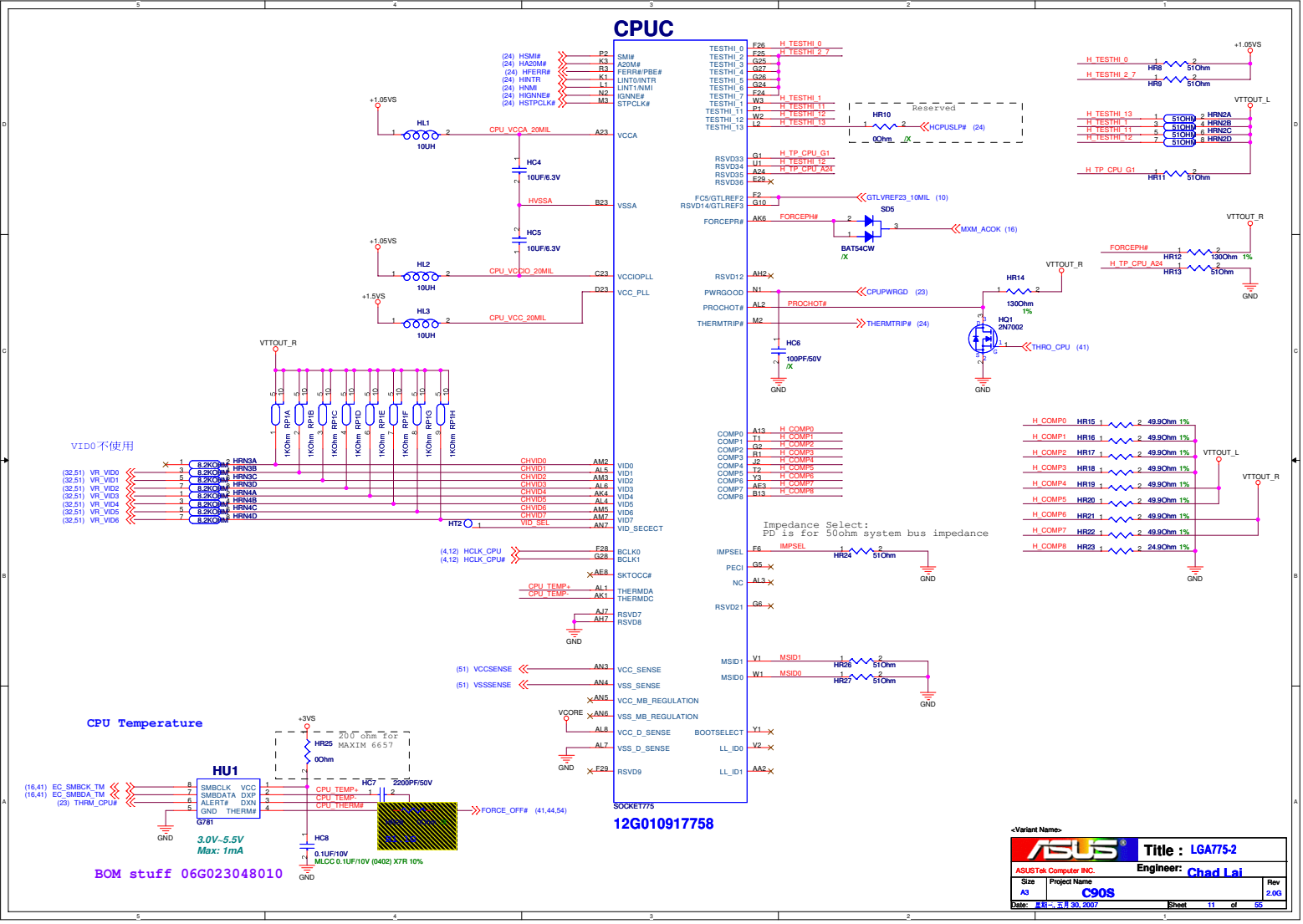


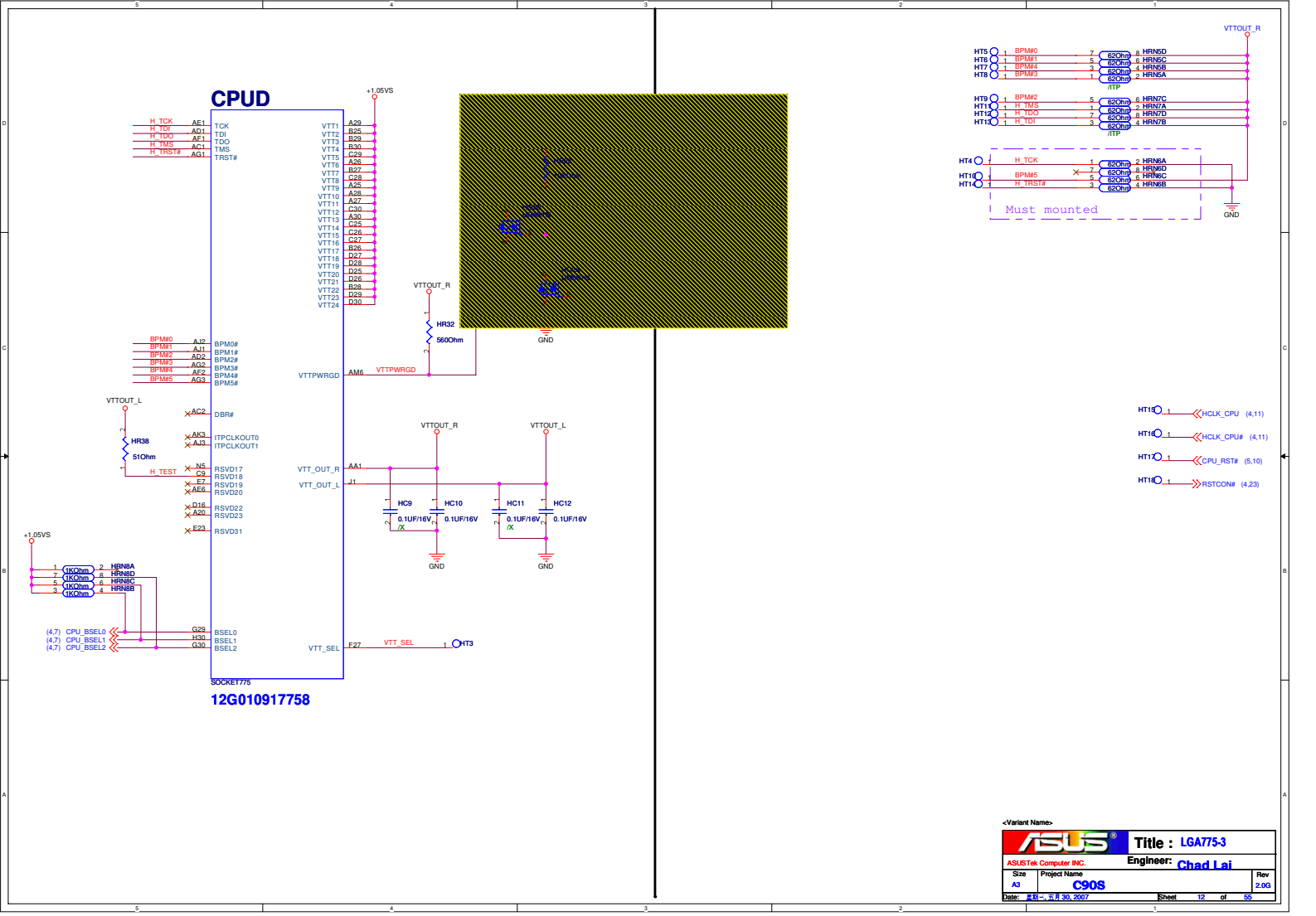


CPU SOCKET目前 料號是:12G010917758
CPU SOCKET 料號:12G010917758 change to 12G01090775N

<Variant Name>

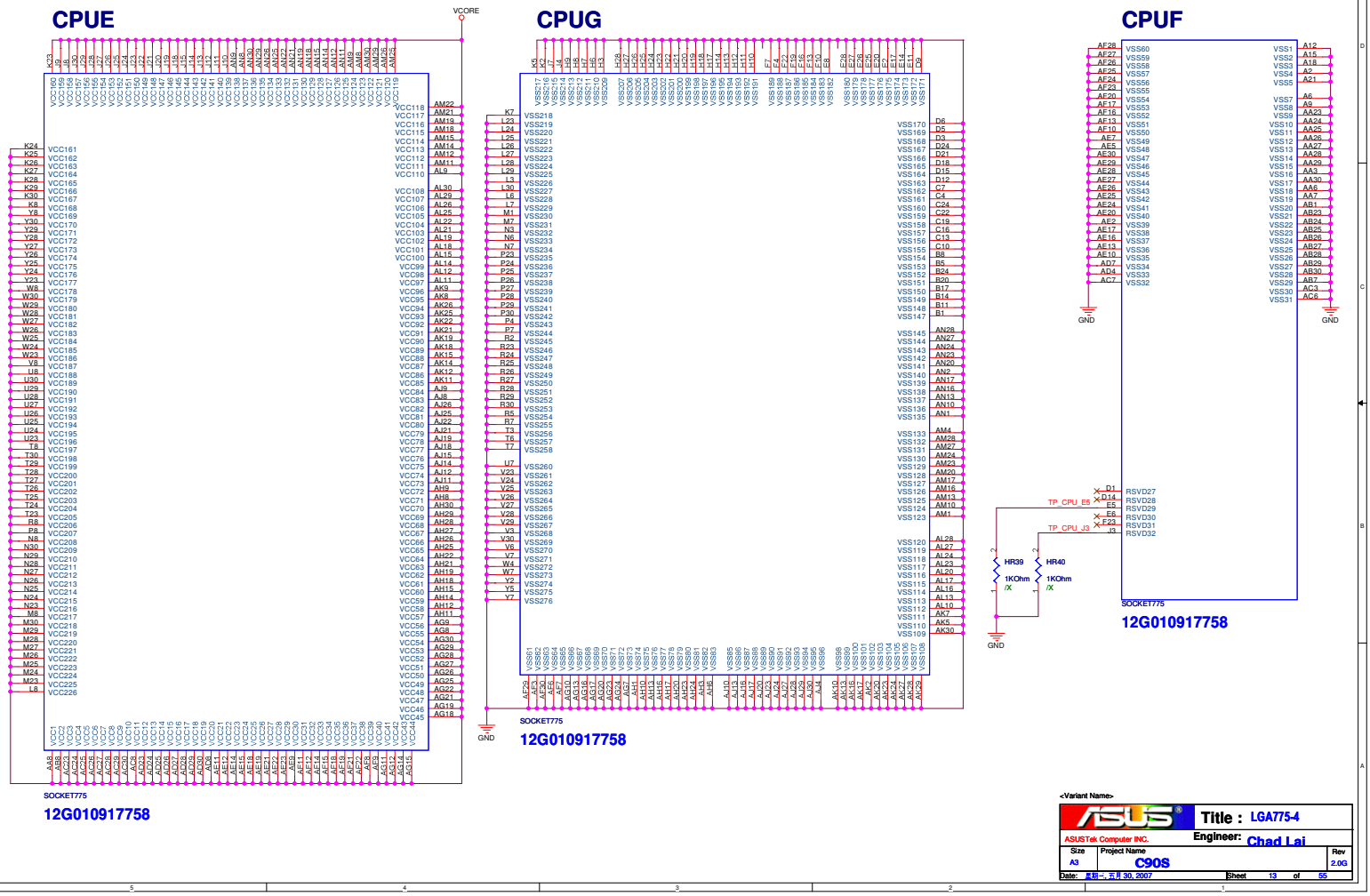
ASUSTek Computer INC.	Title : LGA775-1	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期一, 五月 30, 2007	Sheet 10 of 55	


CPUC
SOCKET775
12G010917758
VID0不使用
CPU Temperature
HU1
BOM stuff 06G023048010
3.0V~5.5V
Max: 1mA
Impedance Select:
PD is for 50ohm system bus impedance
Reserved
Title : LGA775-2
ASUSTek Computer INC.
Engineer: Chad Lai
Size A3
Project Name C90S
Rev 2.0G
Date: 星期一, 五月 30, 2007
Sheet 11 of 55



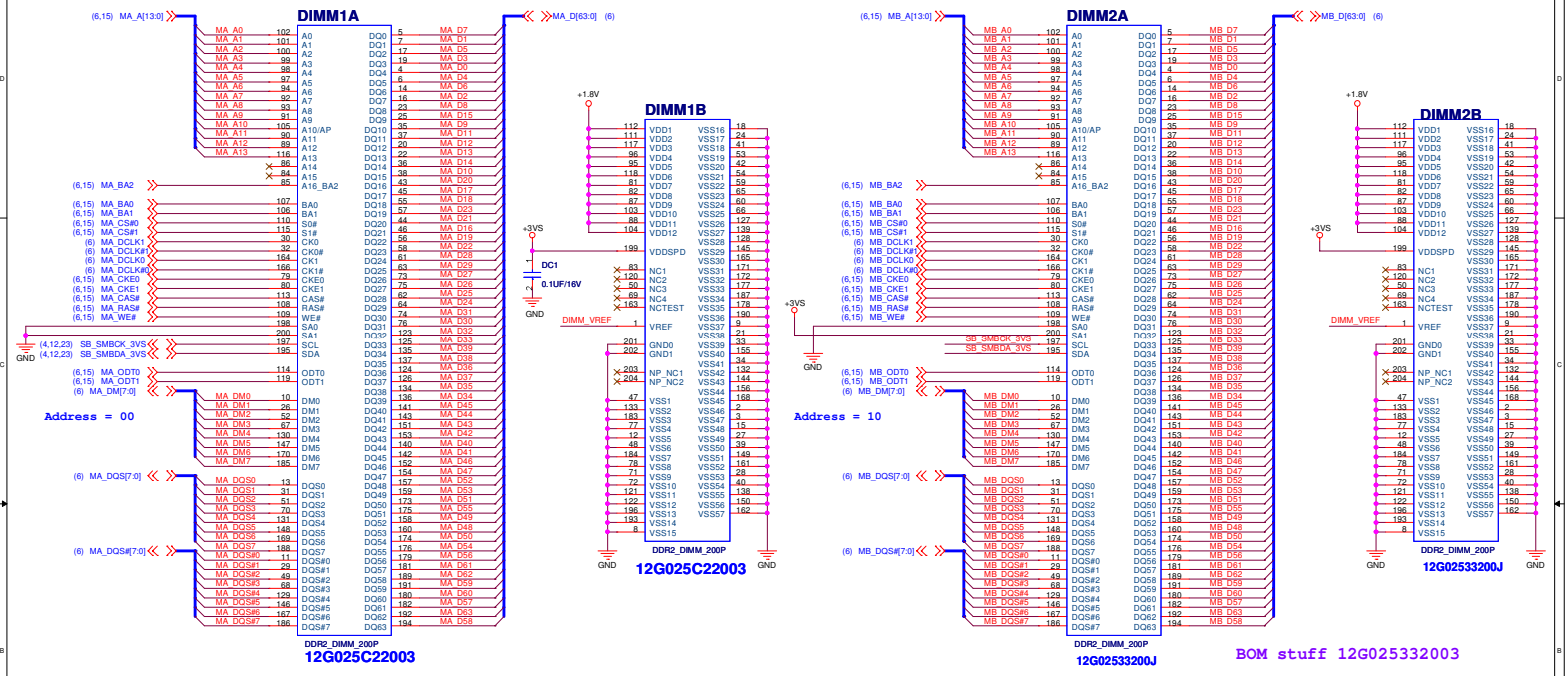
<Variant Name>

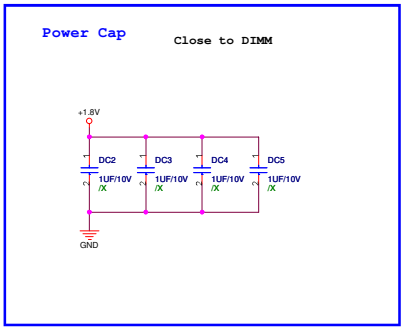
ASUSTek Computer INC.	Title : LGA775-3	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期一, 五月 30, 2007	Sheet 12 of 55	

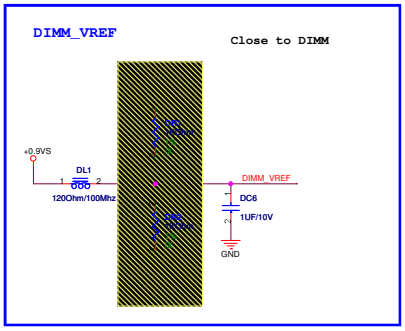


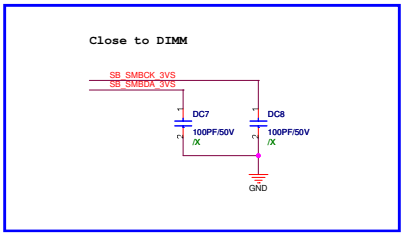
<Variant Name>

ASUSTek Computer INC.	Title : LGA775-4	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期一, 五月 30, 2007	Sheet 13 of 55	



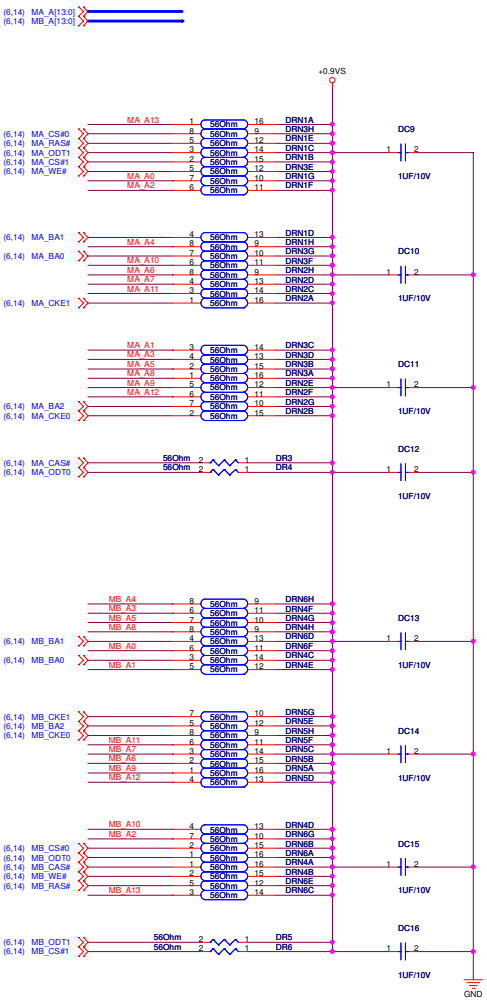






<variant_name>

Title : DDR2 SO-DIMMs
ASUSTek Computer INC.
Engineer: Chad Lai
Size: Custom
Project Name: C90S
Rev: 2.0G
Date: 星期二, 五月 30, 2007
Sheet 14 of 55



<Variant Name>

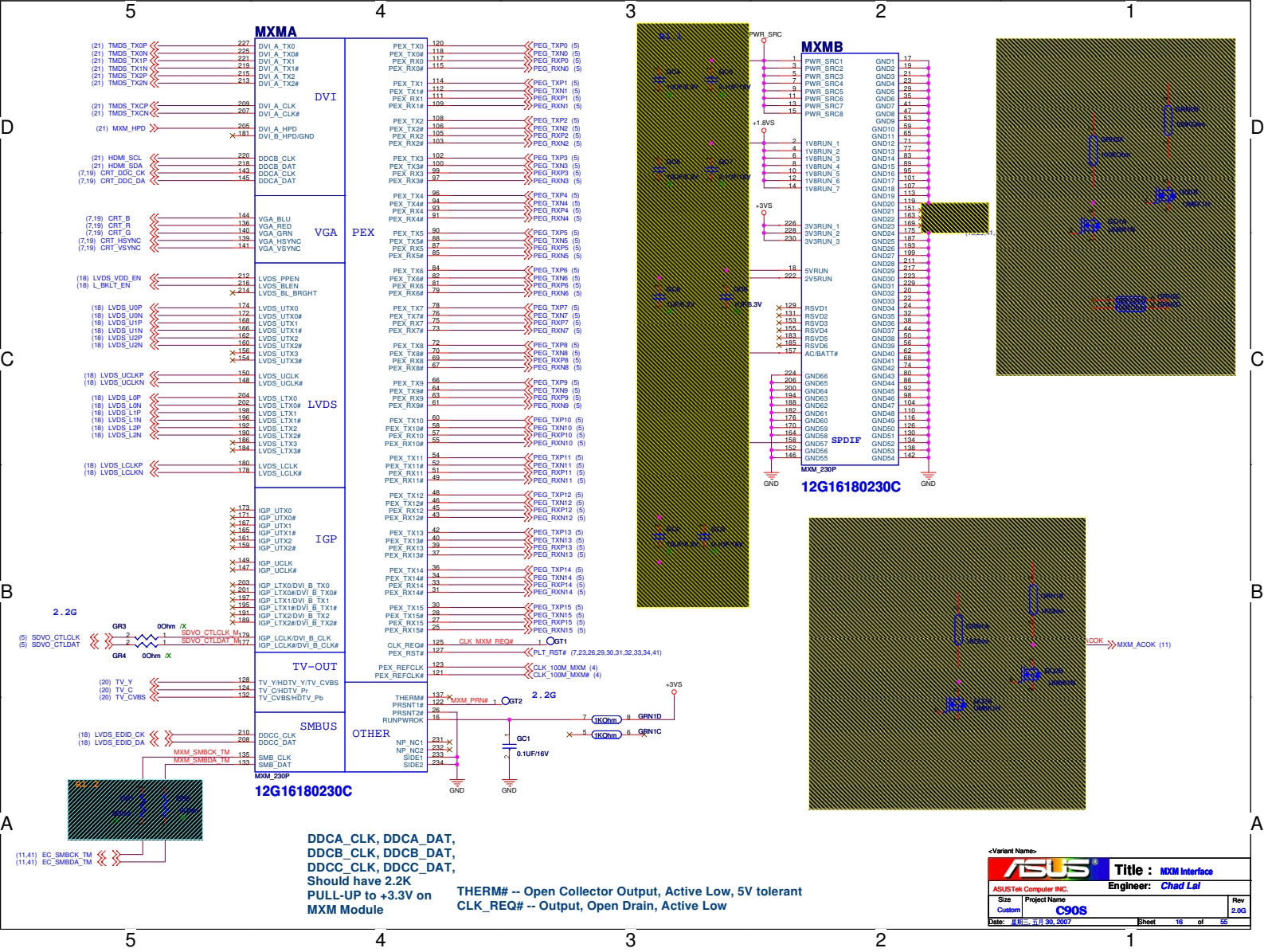
ASUSTek Computer INC.

Title : DDR2 TERMINATION

Engineer: Chad Lai

Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 五月 30, 2007 Sheet 15 of 55


MXMA
DVI
VGA
PEX
LVDS
IGP
TV-OUT
SMBUS
OTHER
MXM_230P
12G16180230C
MXMB
SPDIF
MXM_230P
12G16180230C
2.2G
DDCA_CLK, DDCA_DAT,
DDCB_CLK, DDCB_DAT,
DDCC_CLK, DDCC_DAT,
Should have 2.2K
PULL-UP to +3.3V on
MXM Module
THERM# -- Open Collector Output, Active Low, 5V tolerant
CLK_REQ# -- Output, Open Drain, Active Low
Title : MXM Interface
ASUSTek Computer INC.
Engineer: Chad Lai
C90S
2.0G
Sheet 16 of 55

MXM Connector Pin Definition

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	PWR_SRC	2	1V8RUN	111	PEX_RX1	112	PEX_TX1#	221	DVI_A_TX1	222	2V5RUN
3	PWR_SRC	4	1V8RUN	113	GND	114	PEX_TX1	223	GND	224	GND
5	PWR_SRC	6	1V8RUN	115	PEX_RX0#	116	GND	225	DVI_A_TX0#	226	3V3RUN
7	PWR_SRC	8	1V8RUN	117	PEX_RX0	118	PEX_TX0#	227	DVI_A_TX0	228	3V3RUN
9	PWR_SRC	10	1V8RUN	119	GND	120	PEX_TX0	229	GND	230	3V3RUN
11	PWR_SRC	12	1V8RUN	121	PEX_REFCLK#	122	PRSNT1#				
13	PWR_SRC	14	1V8RUN	123	PEX_REFCLK	124	TV_C/HDTV_Pr				
15	PWR_SRC	16	RUNPWROK	125	CLK_REQ#	126	GND				
17	GND	18	5VRUN	127	PEX_RST#	128	TV_Y/HDTV_Y/TV_CVBS				
19	GND	20	GND	129	RSVD	130	GND				
21	GND	22	GND	131	RSVD	132	TV_CVBS/HDTV_Pb				
23	GND	24	GND	133	SMB_DAT	134	GND				
25	PEX_RX15#	26	PRSNT2#	135	SMB_CLK	136	VGA_RED				
27	PEX_RX15	28	PEX_TX15#	137	THERM#	138	GND				
29	GND	30	PEX_TX15	139	VGA_HSYNC	140	VGA_GRN				
31	PEX_RX14#	32	GND	141	VGA_VSYNC	142	GND				
33	PEX_RX14	34	PEX_TX14#	143	DDCA_CLK	144	VGA_BLU				
35	GND	36	PEX_TX14	145	DDCA_DAT	146	GND				
37	PEX_RX13#	38	GND	147	IGP_RSVD	148	LVDS_UCLK#				
39	PEX_RX13	40	PEX_TX13#	149	IGP_RSVD	150	LVDS_UCLK				
41	GND	42	PEX_TX13	151	IGP_RSVD	152	GND				
43	PEX_RX12#	44	GND	153	IGP_RSVD	154	LVDS_UTX3#				
45	PEX_RX12	46	PEX_TX12#	155	IGP_RSVD	156	LVDS_UTX3				
47	GND	48	PEX_TX12	157	AC/BATT#	158	SPDIF				
49	PEX_RX11#	50	GND	159	IGP_RSVD	160	LVDS_UTX2#/DVI_C_TX5#				
51	PEX_RX11	52	PEX_TX11#	161	IGP_RSVD	162	LVDS_UTX2/DVI_C_TX5				
53	GND	54	PEX_TX11	163	IGP_RSVD	164	GND				
55	PEX_RX10#	56	GND	165	IGP_RSVD	166	LVDS_UTX1#/DVI_C_TX4#				
57	PEX_RX10	58	PEX_TX10#	167	IGP_RSVD	168	LVDS_UTX1//DVI_C_TX4				
59	GND	60	PEX_TX10	169	IGP_RSVD	170	GND				
61	PEX_RX9#	62	GND	171	IGP_RSVD	172	LVDS_UTX0#/DVI_C_TX3#				
63	PEX_RX9	64	PEX_TX9#	173	IGP_RSVD	174	LVDS_UTX0/DVI_C_TX3				
65	GND	66	PEX_TX9	175	GND	176	GND				
67	PEX_RX8#	68	GND	177	IGP/DVI_B_CLK#	178	LVDS_LCLK#//DVI_C_TXC#				
69	PEX_RX8	70	PEX_TX8#	179	IGP/DVI_B_CLK	180	LVDS_LCLK/DVI_C_TXC				
71	GND	72	PEX_TX8	181	DVI_B_HPD/GND	182	GND				
73	PEX_RX7#	74	GND	183	RSVD	184	LVDS_LTX3#				
75	PEX_RX7	76	PEX_TX7#	185	RSVD	186	LVDS_LTX3				
77	GND	78	PEX_TX7	187	GND	188	GND				
79	PEX_RX6#	80	GND	189	IGP/DVI_B_TX2#	190	LVDS_LTX2#/DVI_C_TX2#				
81	PEX_RX6	82	PEX_TX6#	191	IGP/DVI_B_TX2	192	LVDS_LTX2/DVI_C_TX2				
83	GND	84	PEX_TX6	193	GND	194	GND				
85	PEX_RX5#	86	GND	195	IGP/DVI_B_TX1#	196	LVDS_LTX1#/DVI_C_TX1#				
87	PEX_RX5	88	PEX_TX5#	197	IGP/DVI_B_TX1	198	LVDS_LTX1/DVI_C_TX1				
89	GND	90	PEX_TX5	199	GND	200	GND				
91	PEX_RX4#	92	GND	201	IGP/DVI_B_TX0#	202	LVDS_LTX0#/DVI_C_TX0#				
93	PEX_RX4	94	PEX_TX4#	203	IGP/DVI_B_TX0	204	LVDS_LTX0/DVI_C_TX0				
95	GND	96	PEX_TX4	205	DVI_A_HPD	206	GND				
97	PEX_RX3#	98	GND	207	DVI_A_CLK#	208	DDCC_DAT				
99	PEX_RX3	100	PEX_TX3#	209	DVI_A_CLK	210	DDCC_CLK				
101	GND	102	PEX_TX3	211	GND	212	LVDS_PPEN				
103	PEX_RX2#	104	GND	213	DVI_A_TX2#	214	LVDS_BL_BRGHT				
105	PEX_RX2	106	PEX_TX2#	215	DVI_A_TX2	216	LVDS_BLEN				
107	GND	108	PEX_TX2	217	GND	218	DDCB_DAT				
109	PEX_RX1#	110	GND	219	DVI_A_TX1#	220	DDCB_CLK				

<Variant Name>

ASUSTek Computer INC.

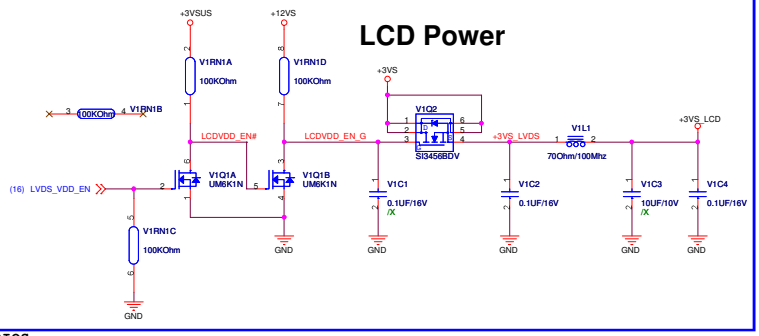
Title : MXM PWR & GND

Engineer: Chad Lai

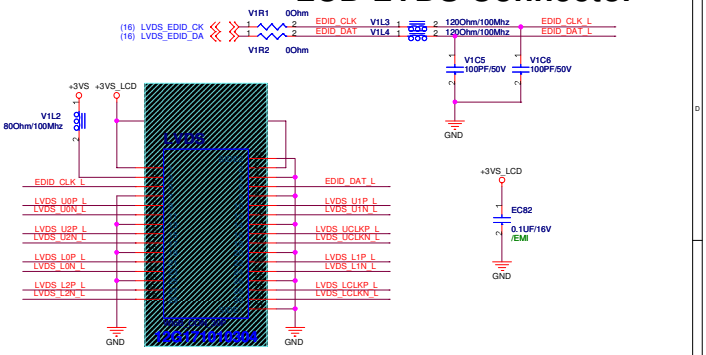
Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 五月 30, 2007 Sheet 17 of 55

LCD Power



LCD LVDS Connector

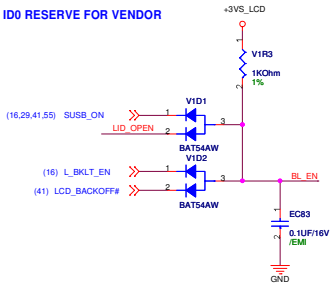


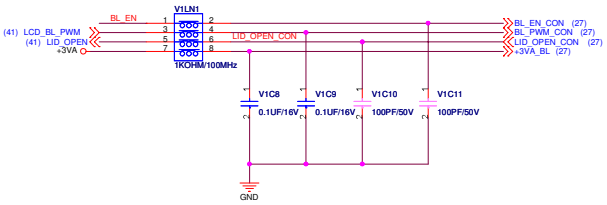
BIOS

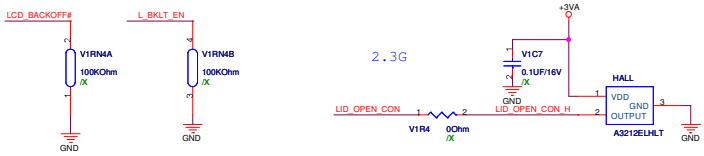
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

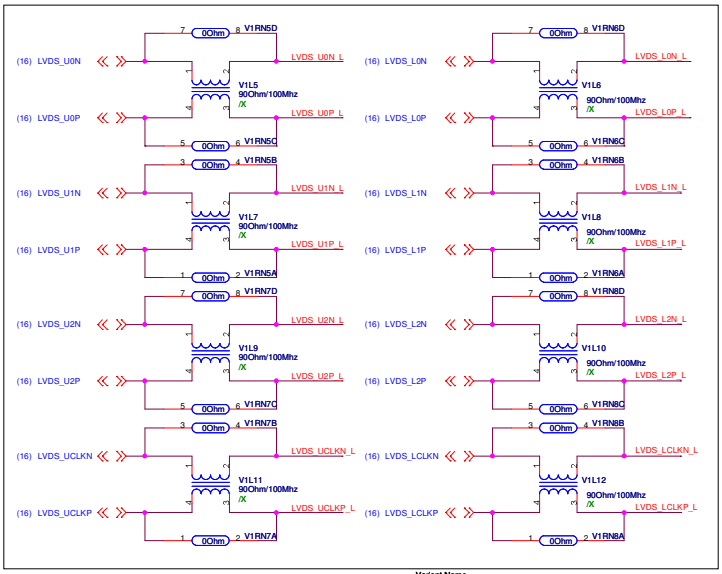
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR



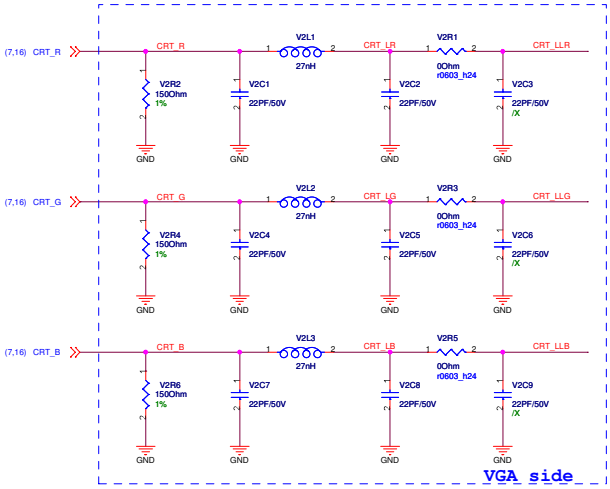


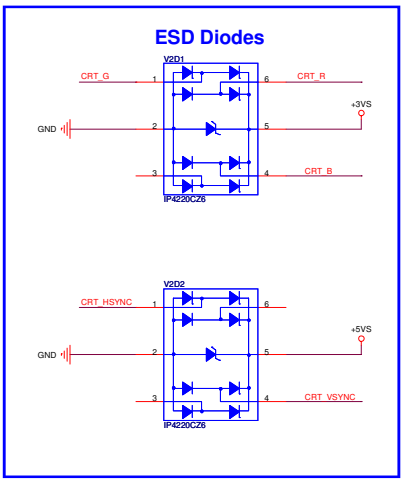


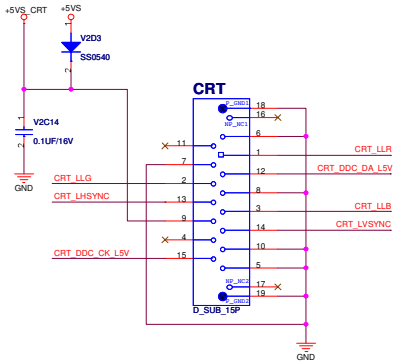


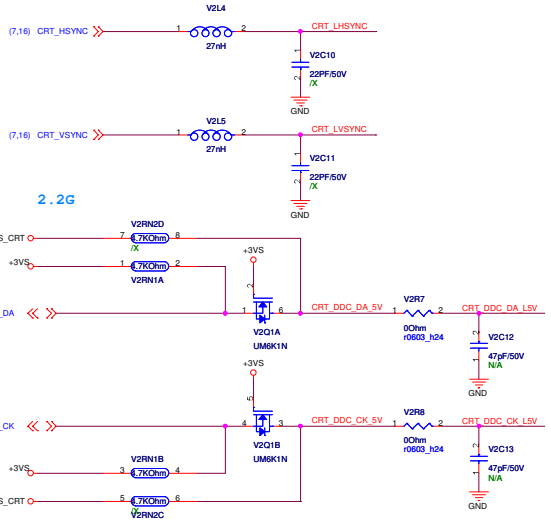
<Variant Name>

ASUSTek Computer INC.	Title : LVDS & INVERTER	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期一, 五月 30, 2007	Sheet 18 of 55	



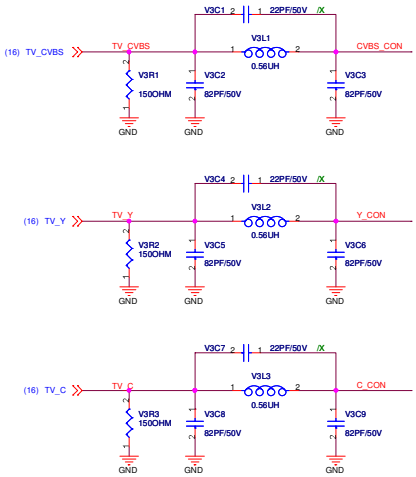


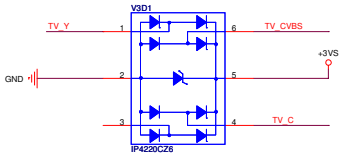




<-Variant Name->

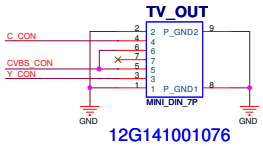
ASUSTek Computer INC.	Title : CRT	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期三, 八月 29, 2007	Sheet 19 of 55	





ESD Diode, Place close to Connector

TV OUT Connector



12G141001076

Check OK

<Variant Name>

Title : TV-OUT Connector

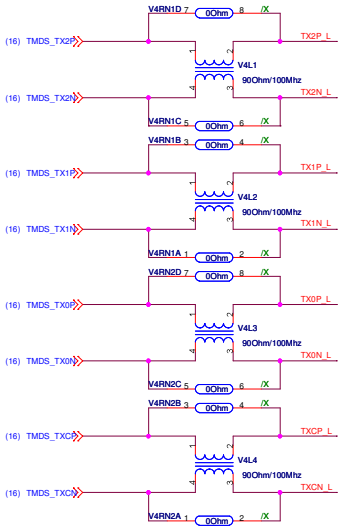
ASUSTek Computer INC.

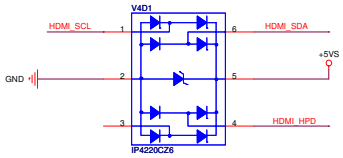
Engineer: Chad Lai

Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 六月 30, 2007 Sheet 20 of 55

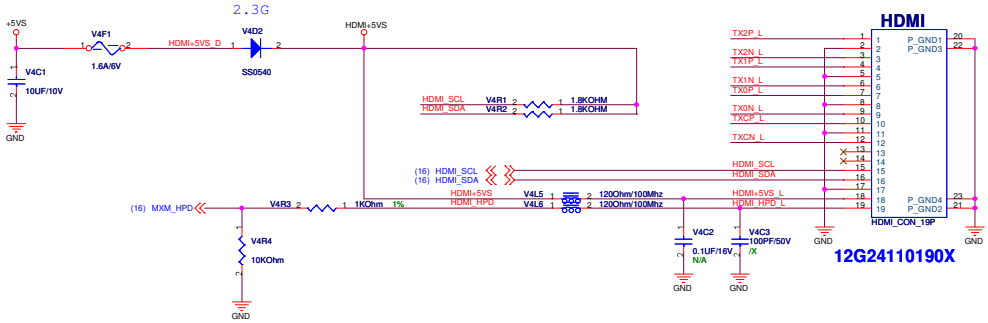
Choke : TDK ACM2012 prefered





ESD Diode, Place close to Connector

HDMI Connector



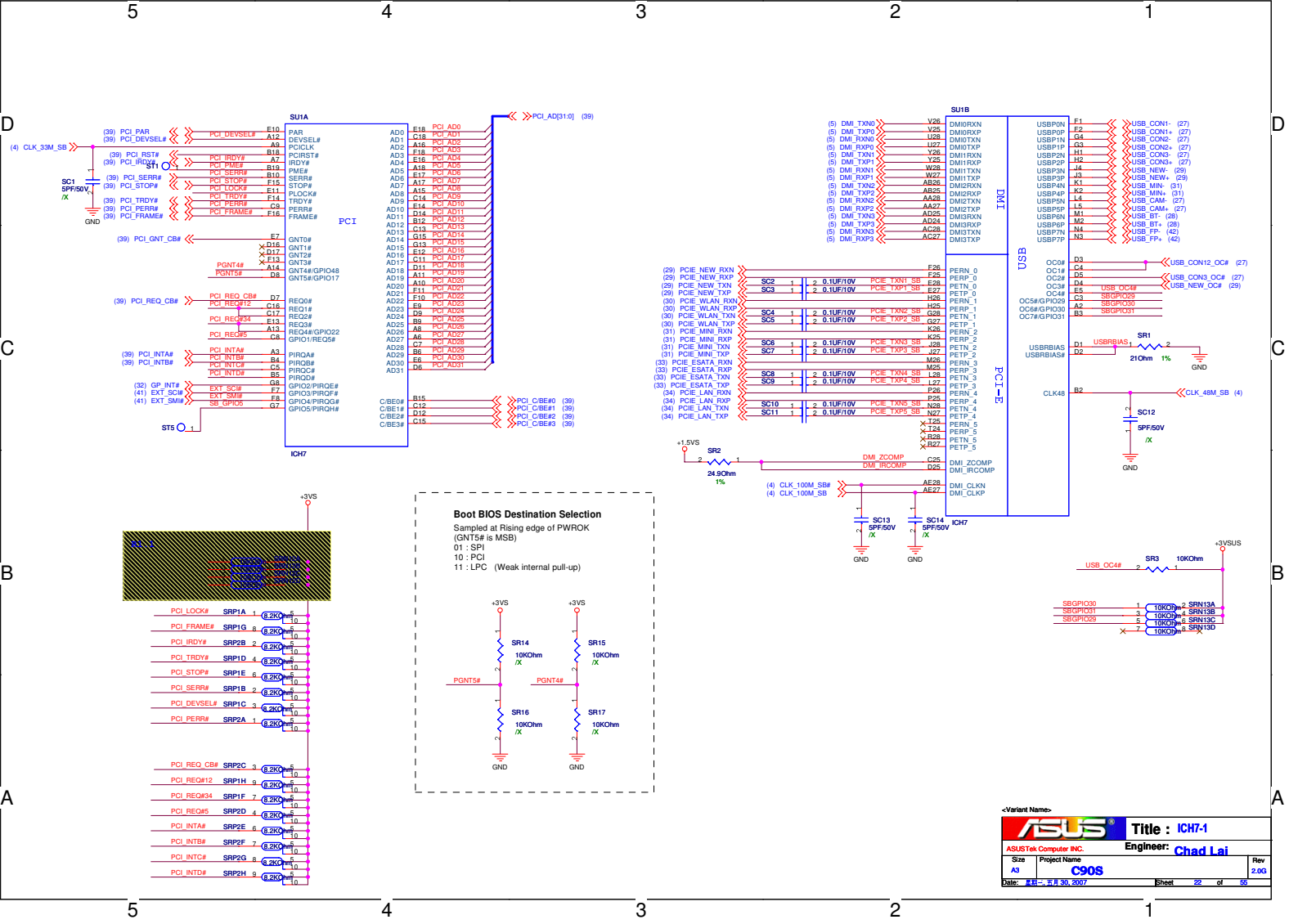
<Variant Name>

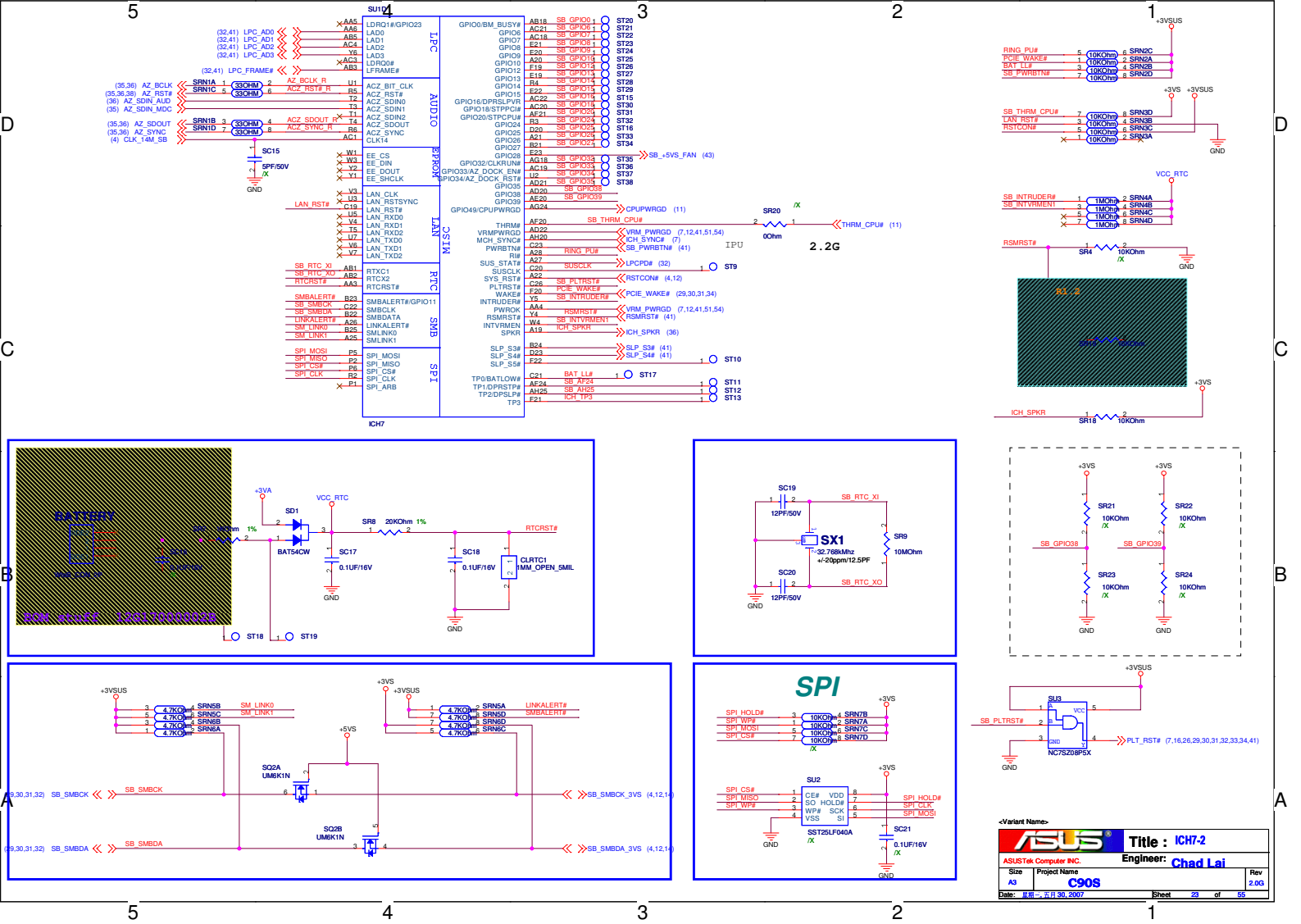
Title : HDMI Connector

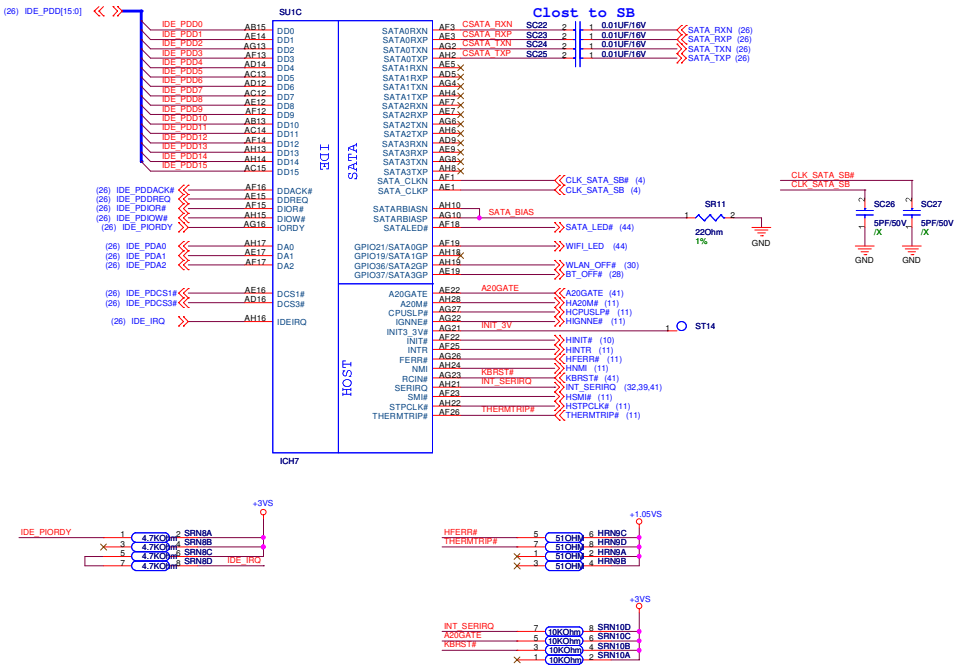
ASUSTek Computer INC. Engineer: Chad Lai

Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 五月 30, 2007 Sheet 21 of 55


SU1A
ICH7
PCI
SU1B
DMI
PCI-E
USB
Boot BIOS Destination Selection
Sampled at Rising edge of PWROK
(GNT5# is MSB)
01 : SPI
10 : PCI
11 : LPC (Weak internal pull-up)
Title : ICH7-1
Engineer: Chad Lai
ASUSTek Computer INC.
C90S
Size A3
Rev 2.0G
Sheet 22 of 55


SU1D
ICH7
LPC
AUDIO
EEPROM
GLAN
RTC
SMB
SPI
SC15
5PF/50V
/X
SR20
0Ohm
2.2G
IPU
SR4
10KOhm
SR18
10KOhm
ICH_SPKR
BATTERY
SD1
BAT54CW
SR8 20KOhm 1%
SC17
0.1UF/16V
SC18
0.1UF/16V
CLRTC1
1MM_OPEN_5MIL
ST18
ST19
SC19
12PF/50V
SX1
32.768kMhz
+/-20ppm/12.5PF
SC20
12PF/50V
SR9
10MOhm
SR21
SR22
SR23
SR24
10KOhm
SPI
SU2
SST25LF040A
SC21
0.1UF/16V
SU3
NC7SZ08P5X
SQ2A
UM6K1N
SQ2B
UM6K1N
SB_SMBCK_3VS
SB_SMBDA_3VS
Title : ICH7-2
ASUSTek Computer INC.
Engineer: Chad Lai
C90S
2.0G
Date: 星期一, 五月 30, 2007
Sheet 23 of 55



(HDA_SDOUT, HDA_SYNC)
(11) = LANE1~4 as a PCIEx4 port
(00) = LANE1~4 as 4 PCIEx1 ports (*) default internal PD
others = reserved
(GNT3#)
1 = Normal (* internal PU)
0 = Top-block swap for FWH

(SB_GPIO20)
1 = reserved
0 = Intel recommend (*
internal PD)
(GNT1#)
1 = Destop/Mobile (* internal PU)
0 = Server

(ICH_TP3)
1 = PCIE Strap (*) default internal PU
0 = XOR chan test mode

(INTVRMEN, LAN100_SLP)
1 = Enabled internal VRMs for VccSus1_05, 1_5 and VccCL1_5, 1_05 and VccLAN1_05 (*)
0 = Disabled internal VRMs

(ICH_SATALED#)
1 = LANE1~4 normal (* internal PU)
0 = LANE1~4 reverse

(SPKR)
1 = Disabled TCO Reboot
0 = Enabled TCO Reboot
(* internal PD)
(TP_GPIO33) : Not used for ICH8M
1 = Enabled Descriptor Security (* internal PU)
0 = Dnabled Descriptor Security

<Variant Name>

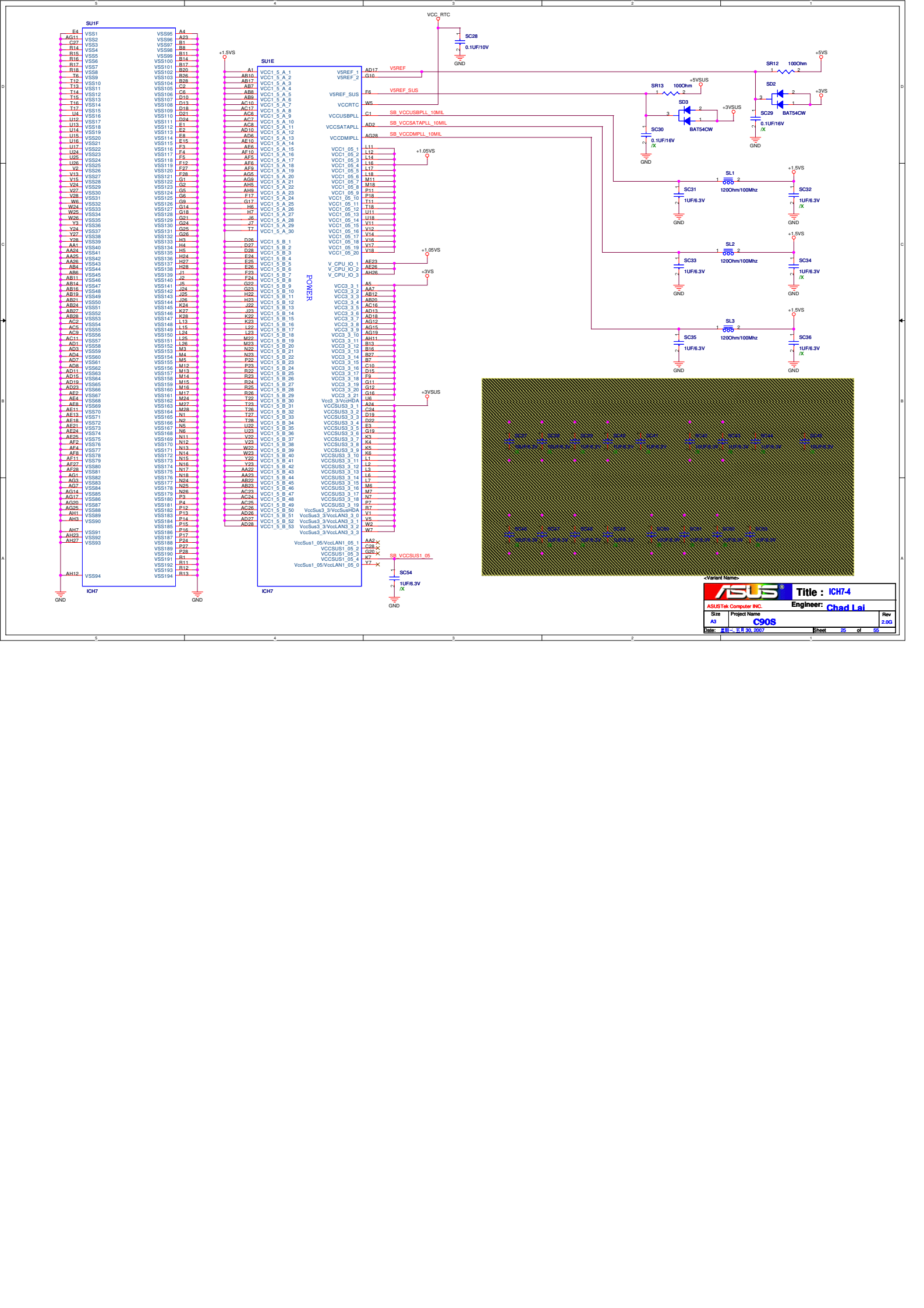
ASUSTek Computer INC.

Title : ICH7-3

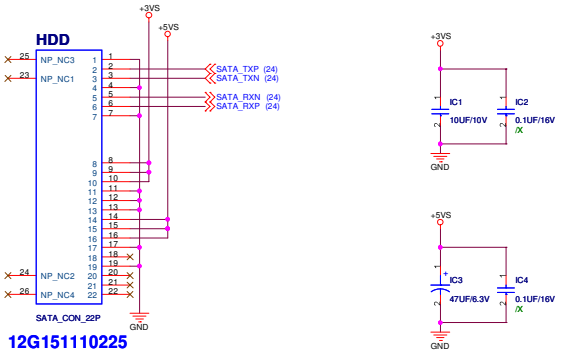
Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

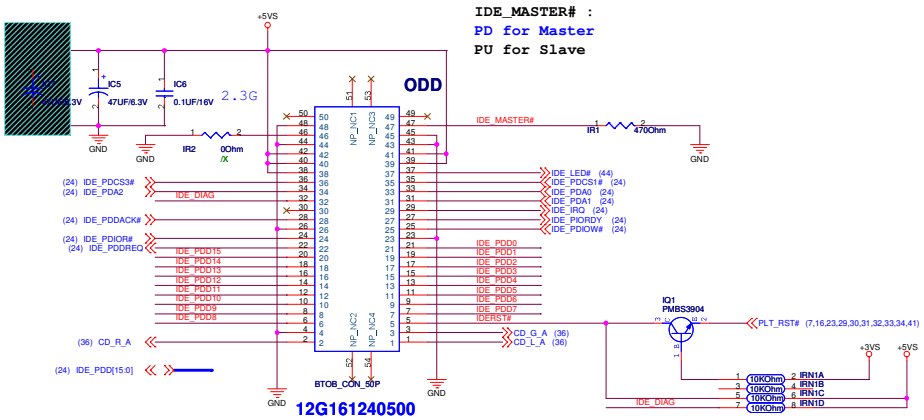
Date: 星期一, 五月 30, 2007 Sheet 24 of 55


SU1F
ICH7
SU1E
ICH7
POWER
VCC_RTC
SC28
0.1UF/10V
GND
+1.5VS
+5VS
+3VS
+5VSUS
+3VSUS
+1.05VS
V5REF
V5REF_SUS
SB_VCCUSBPLL_10MIL
SB_VCCSATAPLL_10MIL
SB_VCCDMIPLL_10MIL
SB_VCCSUS1_05
SR12 100Ohm
SR13 100Ohm
SD2
SD3
BAT54CW
SC29 0.1UF/16V /X
SC30 0.1UF/16V /X
SL1 120Ohm/100Mhz
SL2 120Ohm/100Mhz
SL3 120Ohm/100Mhz
SC31 1UF/6.3V
SC32 1UF/6.3V /X
SC33 1UF/6.3V
SC34 1UF/6.3V /X
SC35 1UF/6.3V
SC36 1UF/6.3V /X
SC54 1UF/6.3V /X
<Variant Name>
Title : ICH7-4
ASUSTek Computer INC.
Engineer: Chad Lai
Size A3
Project Name C90S
Rev 2.0G
Date: 星期一, 五月 30, 2007
Sheet 25 of 55

SATA HDD



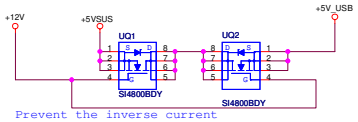
ODD



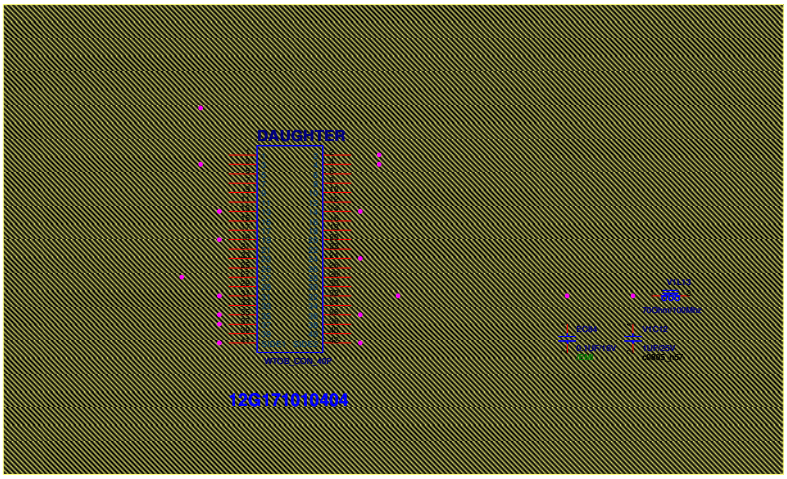
<Variant Name>

ASUSTek Computer INC.	Title : SATA-HDD & ODD	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期二, 五月 30, 2007	Sheet 28 of 55	

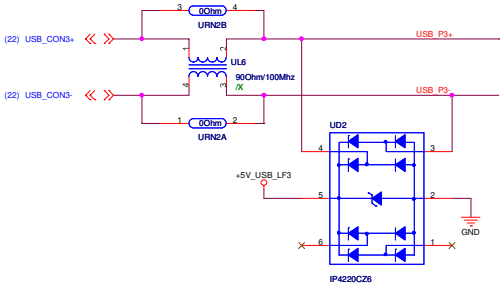
3.0G

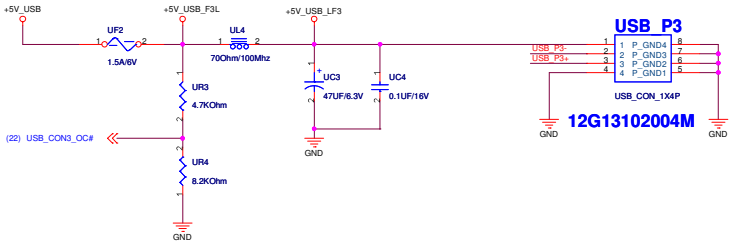


Prevent the inverse current
form external device
with Power



All close to USB connectors





<Variant Name>

ASUSTek Computer INC.

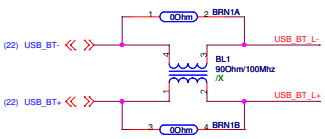
Title : USB CONN

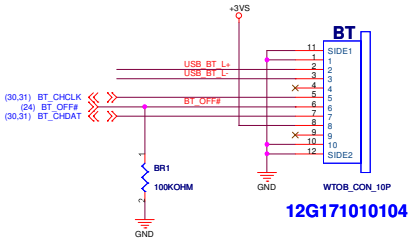
Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期一, 五月 30, 2007 Sheet 27 of 55

Bluetooth Connector





12G171010104

BT_OFF# : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

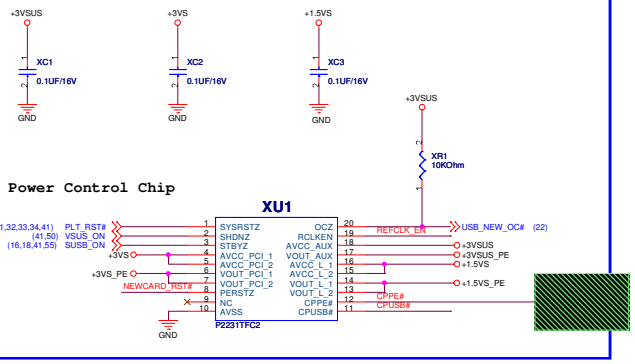
G-Sensor

3.0G

<Variant Name>

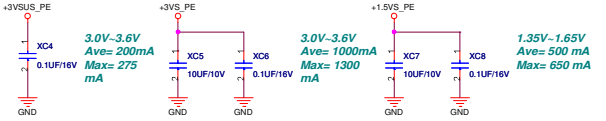
ASUSTek Computer INC.	Title : Blue Tooth & G-Sensor	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期二, 五月 30, 2007	Sheet 28 of 55	

Decouple Cap. (Near XU1)

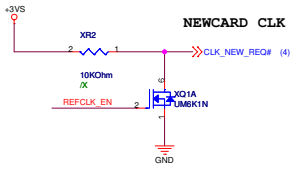


Power Control Chip

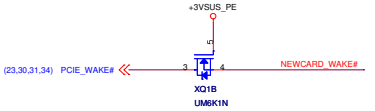
Decouple Cap. (Near Express connector)



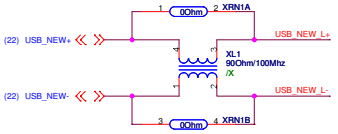
NEWCARD CLK Request



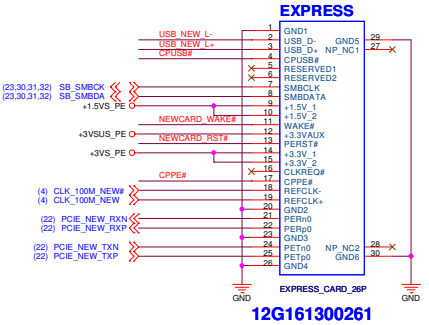
NEWCARD Wake#



USB CHOKE FOR EMI



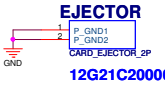
EXPRESS



12G161300261

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

EJECTOR



12G21C20000P

<Variant Name>

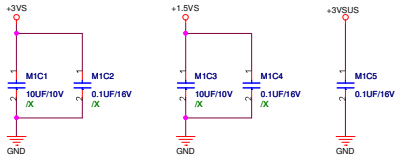
ASUSTeK Computer INC.	Title : NEWCARD	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期一, 十月 30, 2007	Sheet 29 of 55	

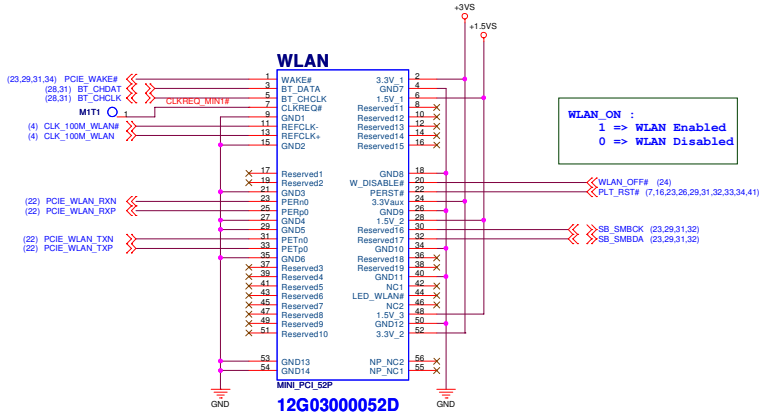
Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA





12G03000052D

<Variant Name>

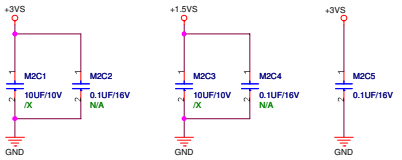
ASUSTek Computer INC.	Title : MINI CARD	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期二, 五月 30, 2007	Sheet 30 of 55	

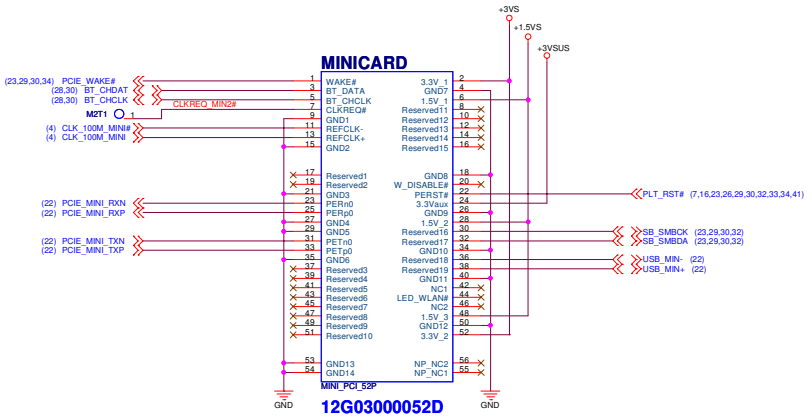
Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA

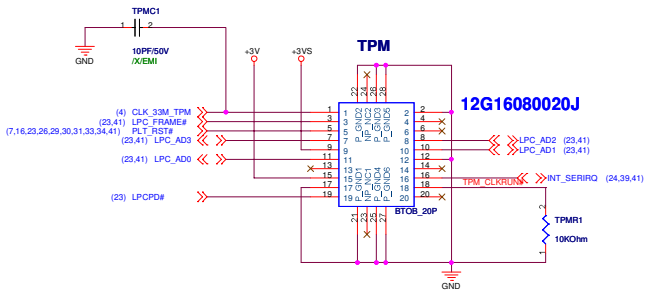




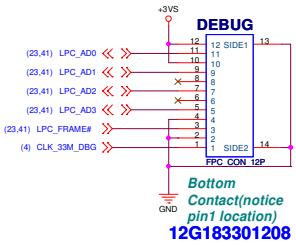
<Variant Name>

ASUSTek Computer INC.	Title : MINI CARD	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期二, 五月 30, 2007	Sheet 31 of 55	

TPM Connector



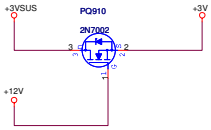
Debug Connector



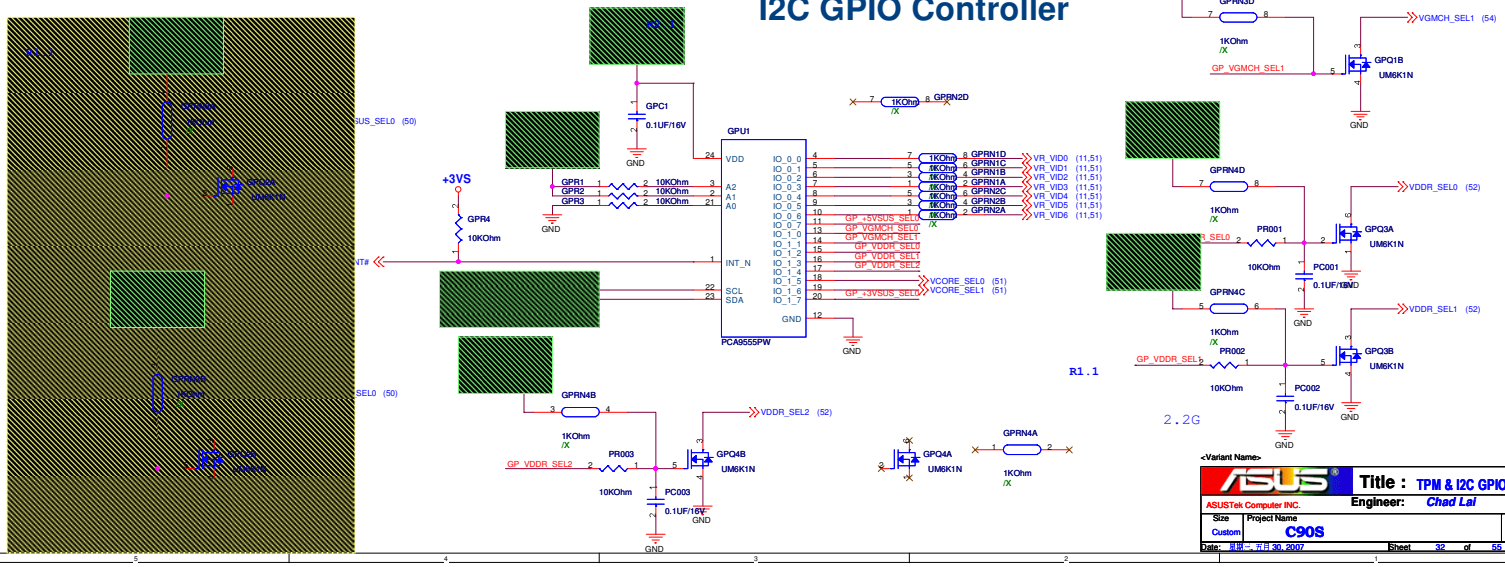
Bottom Contact(notice pin1 location)

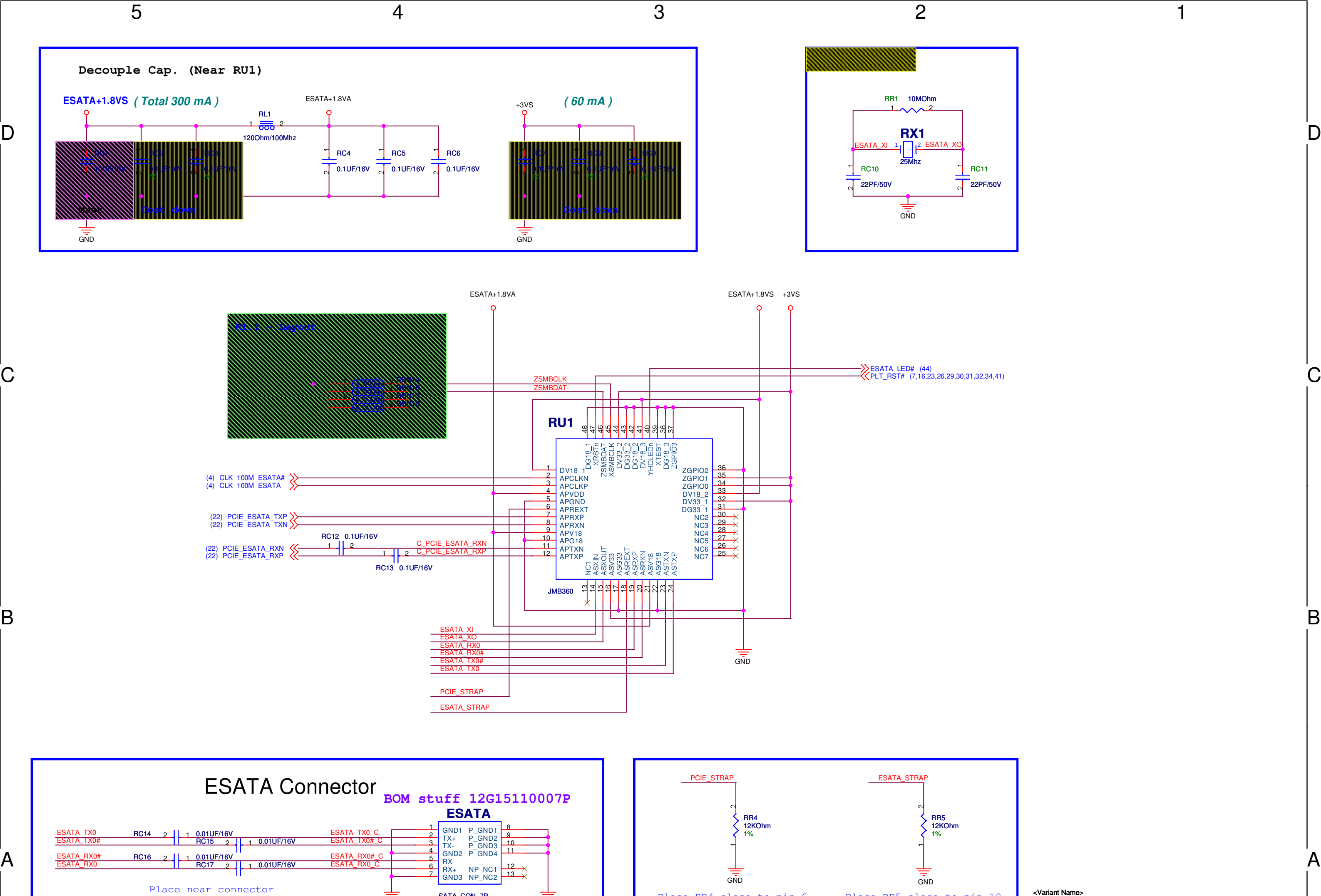
12G183301208

FOR +3V POWER TPM PWR_LED



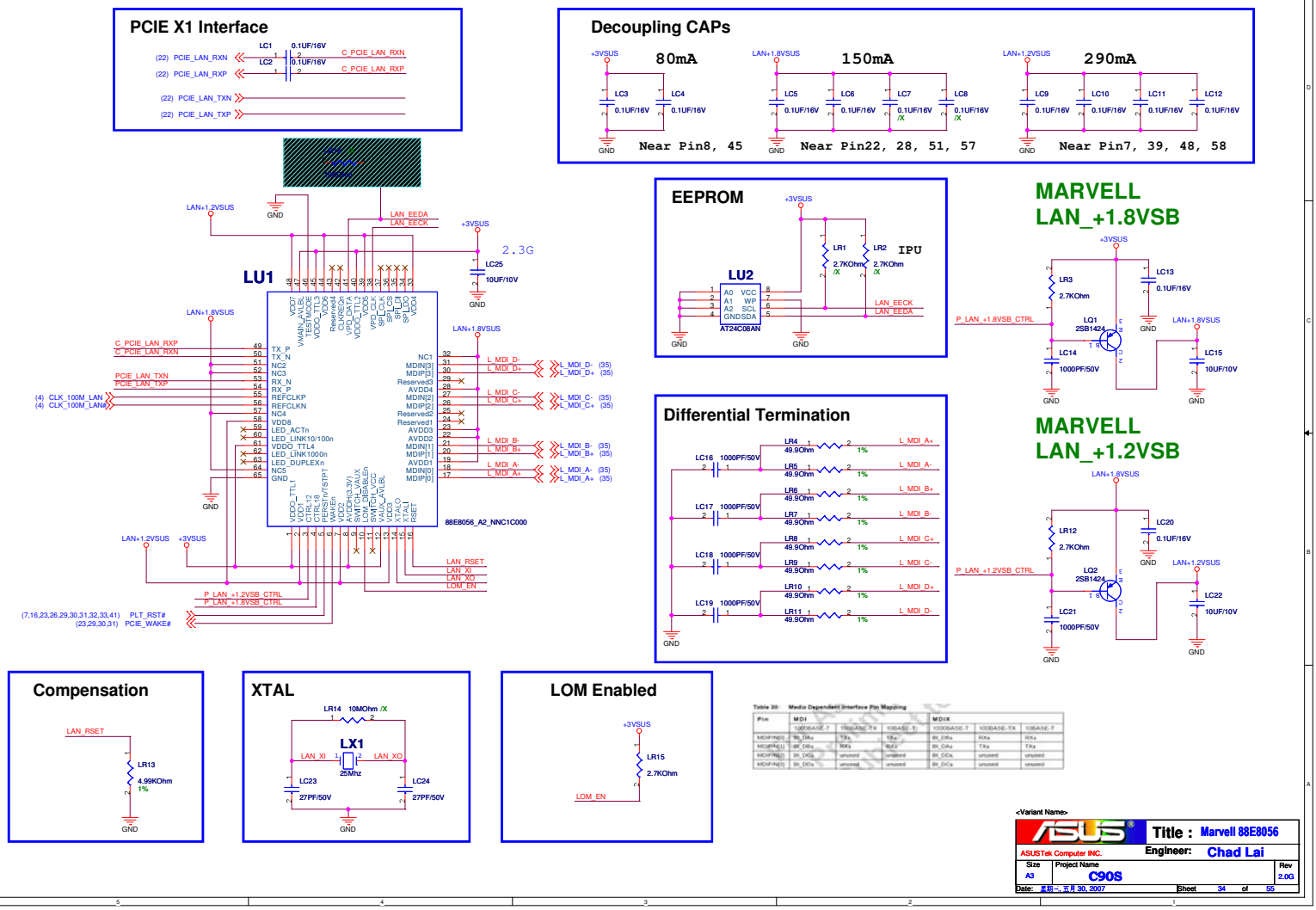
I2C GPIO Controller

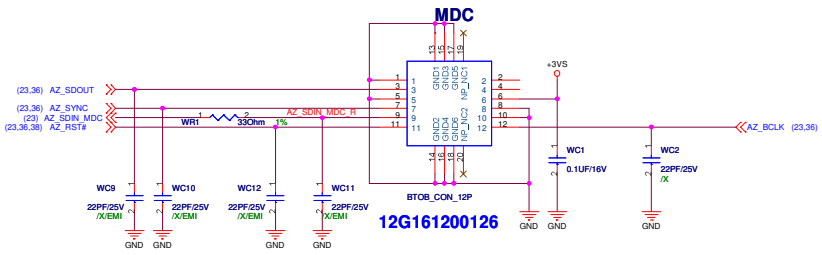


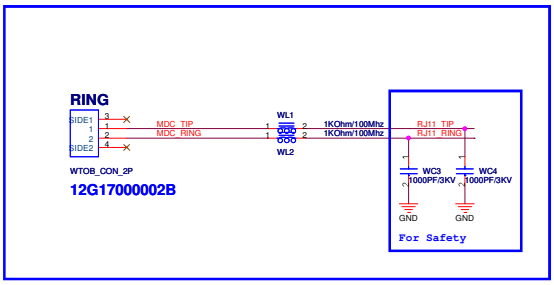


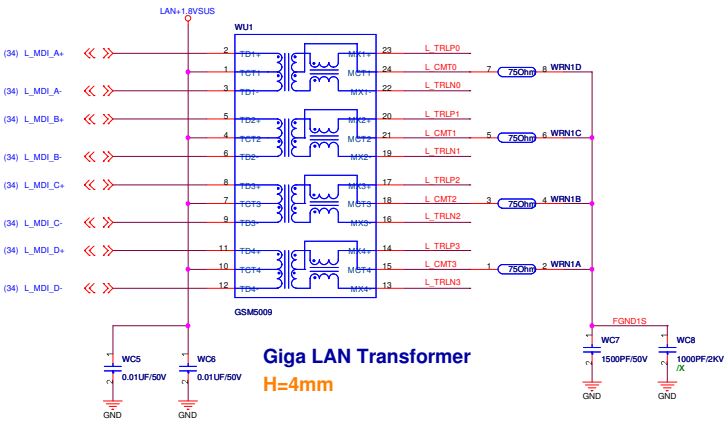
<Variant Name>

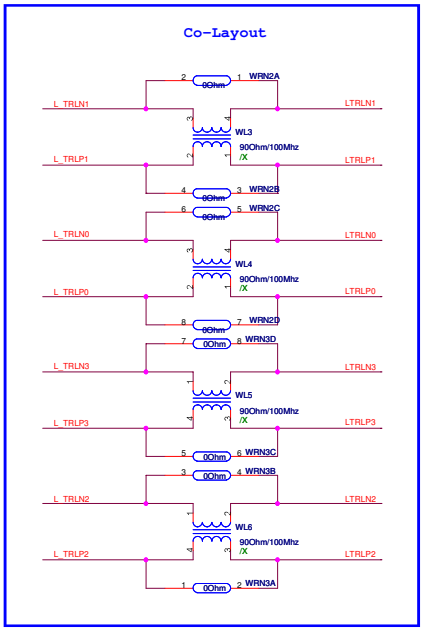
ASUSTek Computer INC.	Title : ESATA-JMB360	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期一, 五月 30, 2007	Sheet 33 of 55	

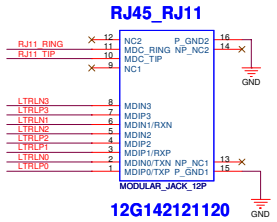

PCIE X1 Interface
LC1 0.1UF/16V
LC2 0.1UF/16V
(22) PCIE_LAN_RXN
(22) PCIE_LAN_RXP
C_PCIE_LAN_RXN
C_PCIE_LAN_RXP
(22) PCIE_LAN_TXN
(22) PCIE_LAN_TXP
Decoupling CAPs
+3VSUS 80mA
LC3 0.1UF/16V
LC4 0.1UF/16V
GND
Near Pin8, 45
LAN+1.8VSUS 150mA
LC5 0.1UF/16V
LC6 0.1UF/16V
LC7 0.1UF/16V /X
LC8 0.1UF/16V /X
GND
Near Pin22, 28, 51, 57
LAN+1.2VSUS 290mA
LC9 0.1UF/16V
LC10 0.1UF/16V
LC11 0.1UF/16V
LC12 0.1UF/16V
GND
Near Pin7, 39, 48, 58
LU1
88E8056_A2_NNC1C000
LAN+1.2VSUS
LAN+1.8VSUS
+3VSUS
GND
LAN_EEDA
LAN_EECK
LC25 10UF/10V
2.3G
C_PCIE_LAN_RXP
C_PCIE_LAN_RXN
PCIE_LAN_TXN
PCIE_LAN_TXP
(4) CLK_100M_LAN
(4) CLK_100M_LAN#
L_MDI_D- (35)
L_MDI_D+ (35)
L_MDI_C- (35)
L_MDI_C+ (35)
L_MDI_B- (35)
L_MDI_B+ (35)
L_MDI_A- (35)
L_MDI_A+ (35)
LAN_RSET
LAN_XI
LAN_XO
LOM_EN
P_LAN_+1.2VSB_CTRL
P_LAN_+1.8VSB_CTRL
(7,16,23,26,29,30,31,32,33,41) PLT_RST#
(23,29,30,31) PCIE_WAKE#
EEPROM
LU2
AT24C08AN
LR1 2.7KOhm /X
LR2 2.7KOhm /X
IPU
LAN_EECK
LAN_EEDA
MARVELL
LAN_+1.8VSB
LR3 2.7KOhm
LC13 0.1UF/16V
LQ1 2SB1424
LC14 1000PF/50V
LC15 10UF/10V
P_LAN_+1.8VSB_CTRL
Differential Termination
LC16 1000PF/50V
LC17 1000PF/50V
LC18 1000PF/50V
LC19 1000PF/50V
LR4 49.9Ohm 1%
LR5 49.9Ohm 1%
LR6 49.9Ohm 1%
LR7 49.9Ohm 1%
LR8 49.9Ohm 1%
LR9 49.9Ohm 1%
LR10 49.9Ohm 1%
LR11 49.9Ohm 1%
L_MDI_A+
L_MDI_A-
L_MDI_B+
L_MDI_B-
L_MDI_C+
L_MDI_C-
L_MDI_D+
L_MDI_D-
MARVELL
LAN_+1.2VSB
LR12 2.7KOhm
LC20 0.1UF/16V
LQ2 2SB1424
LC21 1000PF/50V
LC22 10UF/10V
P_LAN_+1.2VSB_CTRL
Compensation
LAN_RSET
LR13 4.99KOhm 1%
XTAL
LR14 10MOhm /X
LX1 25Mhz
LAN_XI
LAN_XO
LC23 27PF/50V
LC24 27PF/50V
LOM Enabled
+3VSUS
LR15 2.7KOhm
LOM_EN
Table 30 : Media Dependent Interface Pin Mapping
<Variant Name>
Title : Marvell 88E8056
ASUSTek Computer INC.
Engineer: Chad Lai
Size A3
Project Name C90S
Rev 2.0G
Date: 星期一, 五月 30, 2007
Sheet 34 of 55





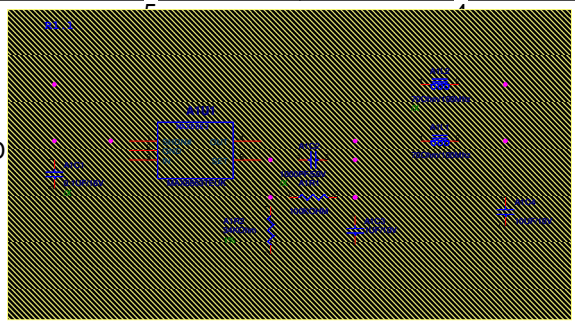


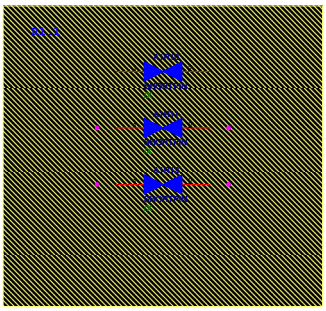


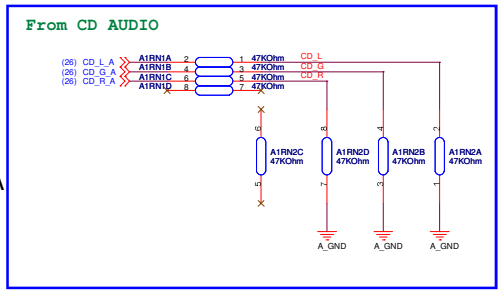


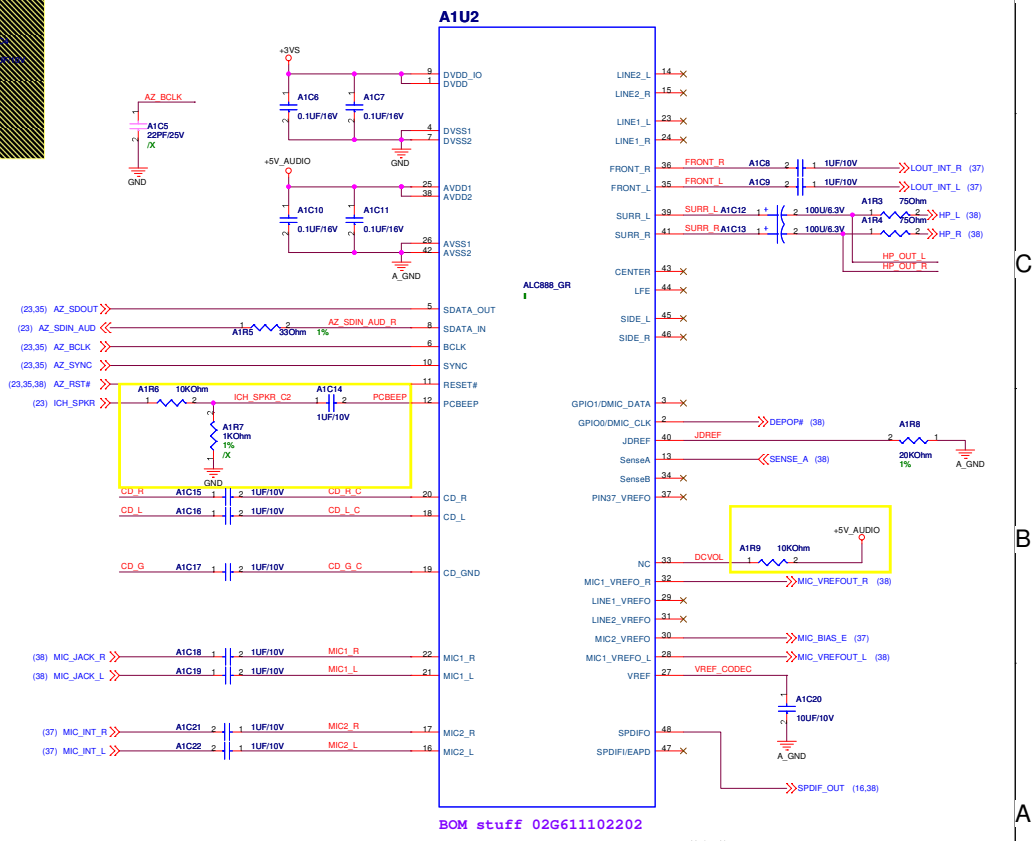
<Variant Name>

ASUSTek Computer INC.	Title : MDC / RJ45	
	Engineer: Chad Lai	
Size: A3	Project Name: C90S	Rev: 2.0G
Date: 星期二, 五月 30, 2007	Sheet 35 of 55	









BOM stuff 02G611102202

<Variant Name>

ASUSTek Computer INC.

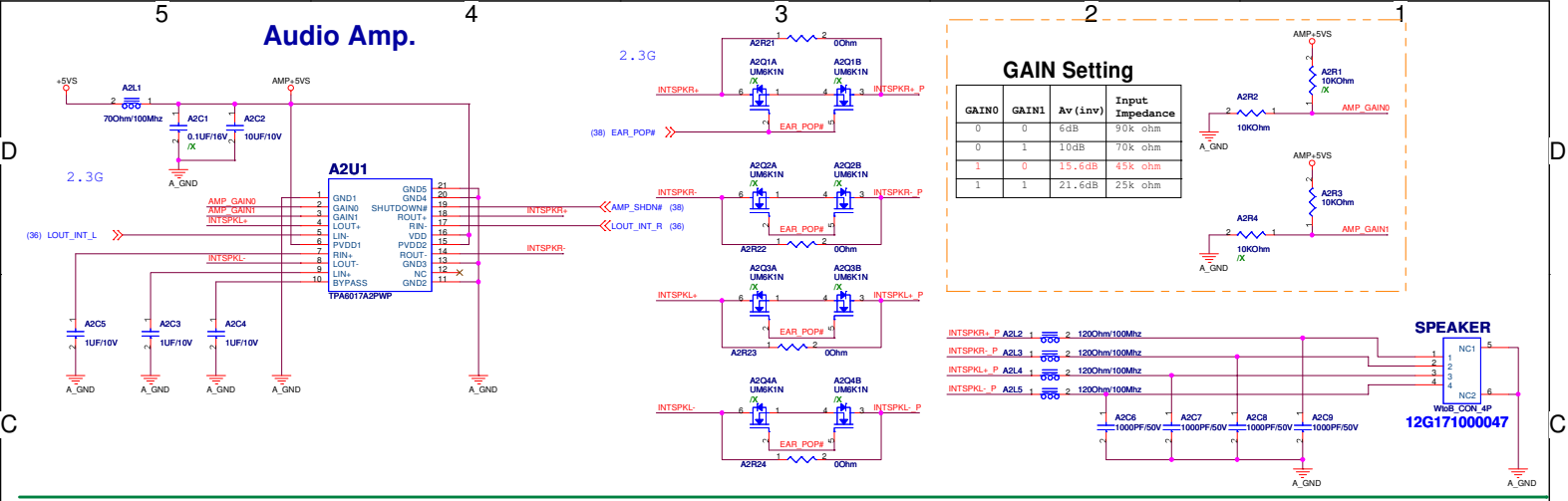
Title : <Title>

Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期一, 五月 30, 2007 Sheet 36 of 55

Audio Amp.



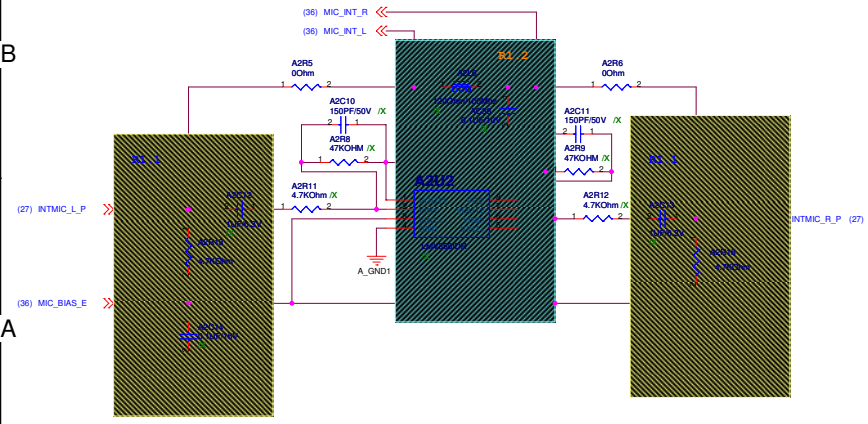
GAIN Setting

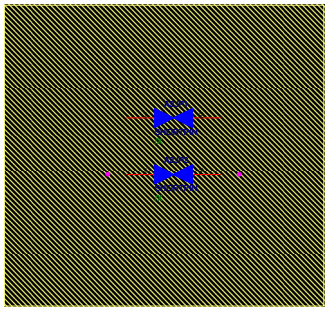
GAIN0	GAIN1	Av(inv)	Input Impedance
0	0	6dB	90k ohm
0	1	10dB	70k ohm
1	0	15.6dB	45k ohm
1	1	21.6dB	25k ohm

Internal MIC Amp.

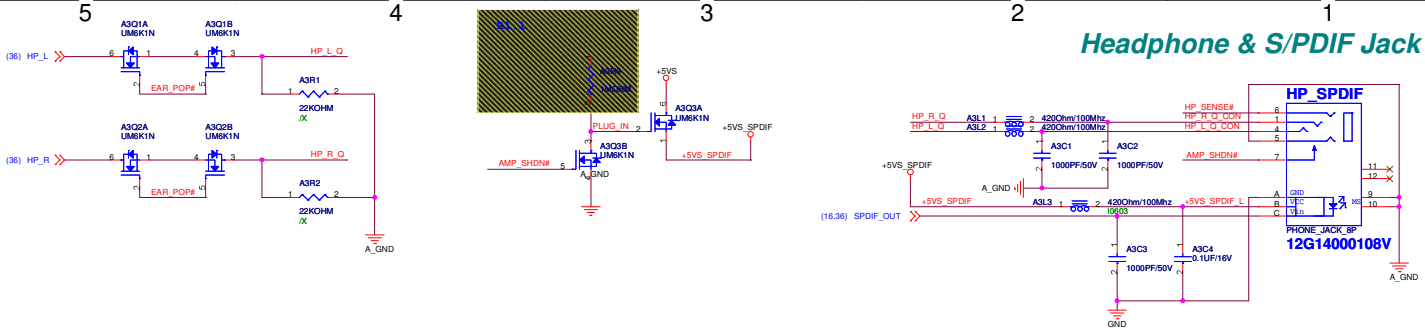
FL = 33.86kHz, FH = 22.5kHz

Place Near INTMIC Connector



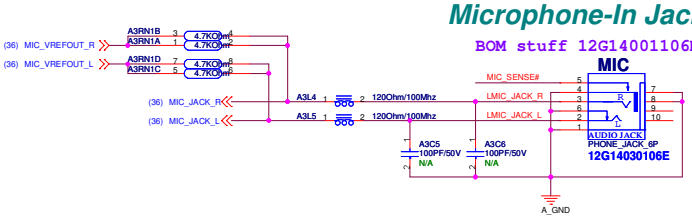


Headphone & S/PDIF Jack

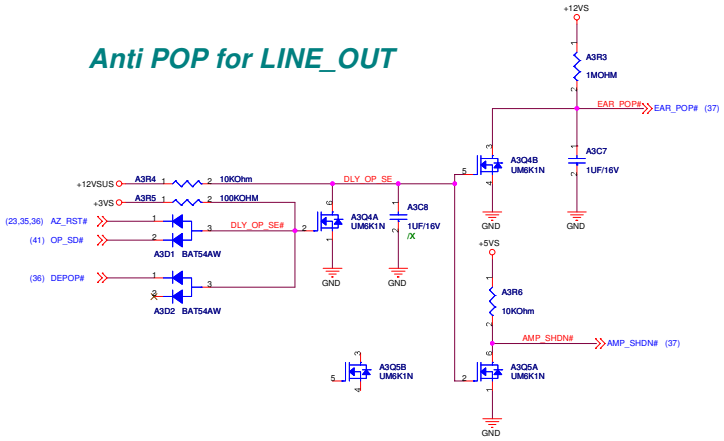


Microphone-In Jack

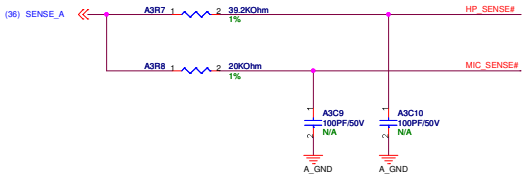
BOM stuff 12G14001106M



Anti POP for LINE_OUT



Jack Plug-in Detection



<Variant Name>

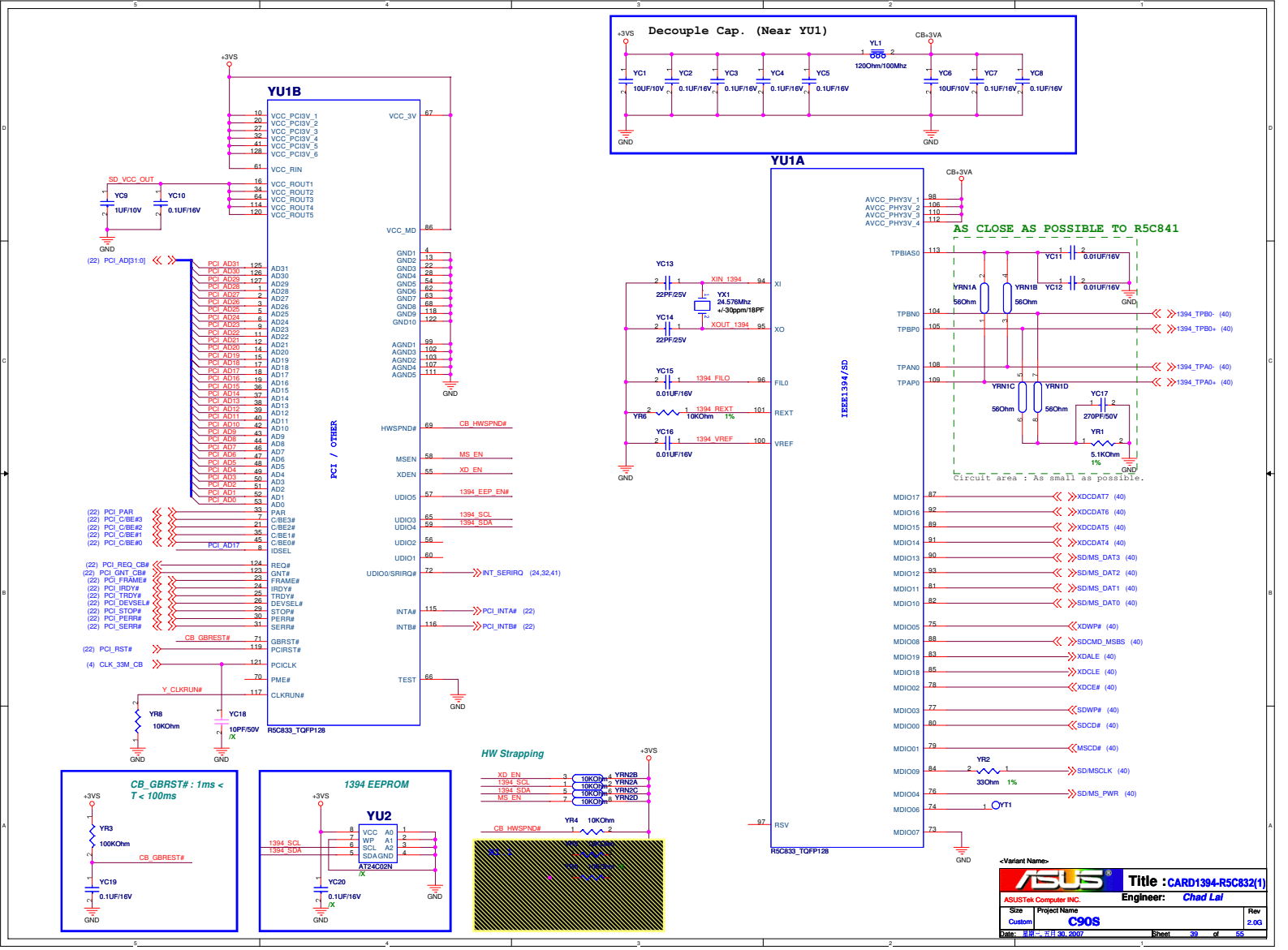
ASUSTek Computer INC.

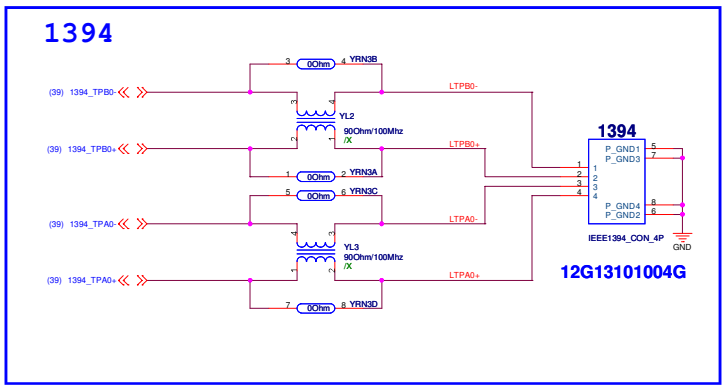
Title : SCH page name

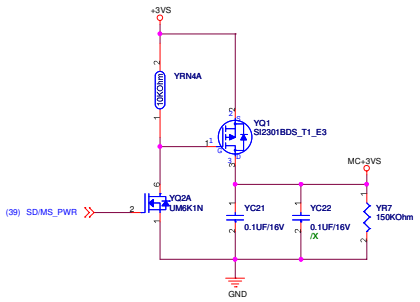
Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

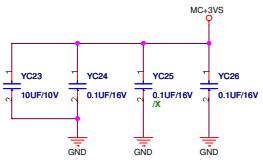
Date: 星期二, 五月 30, 2007 Sheet 38 of 55


Decouple Cap. (Near YU1)
YU1B
YU1A
PCI / OTHER
IEEE1394/SD
AS CLOSE AS POSSIBLE TO R5C841
Circuit area : As small as possible.
HW Strapping
CB_GBRST# : 1ms < T < 100ms
1394 EEPROM
YU2
R5C833_TQFP128
AT24C02N
Title : CARD1394-R5C832(1)
ASUSTek Computer INC.
Engineer: Chad Lai
C90S

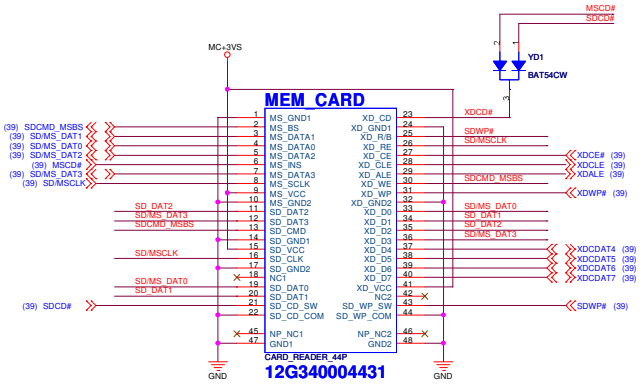




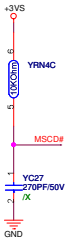
Card Reader Power Switcher

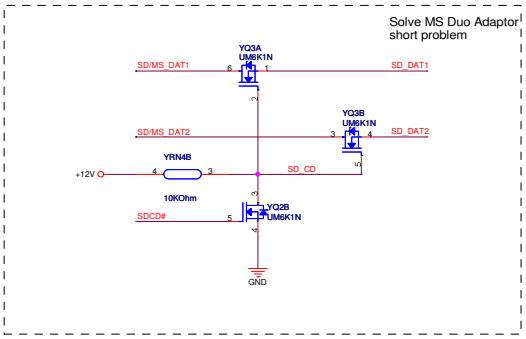


SD_VCC MS_VCC XD_VCC



6 hold change to 4hold





<Variant Name>

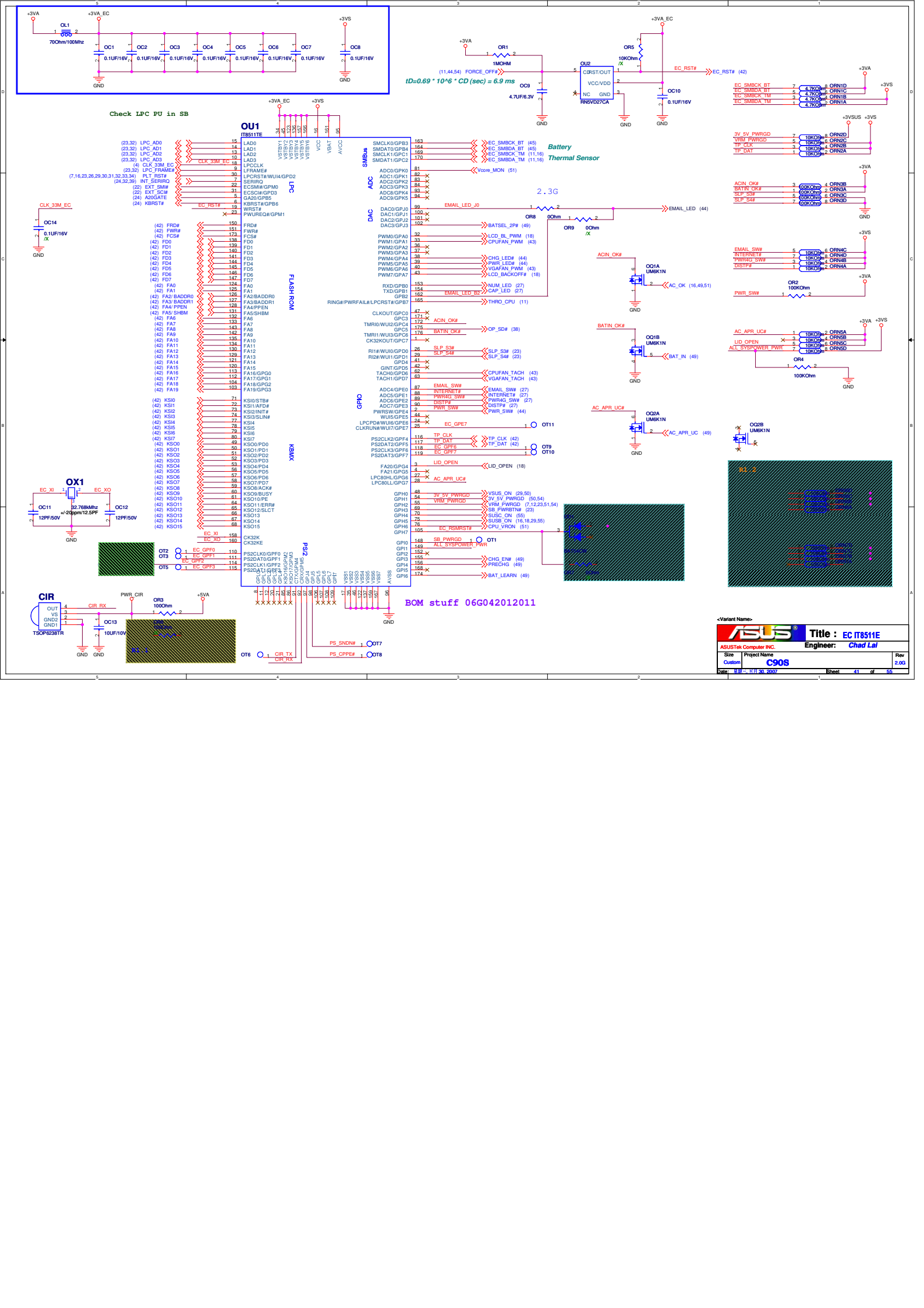
ASUSTek Computer INC.

Title: 1394 CON

Engineer: Chad Lai

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期三, 五月 30, 2007 Sheet 40 of 55


OL1
70Ohm/100Mhz
OC1 0.1UF/16V
OC2 0.1UF/16V
OC3 0.1UF/16V
OC4 0.1UF/16V
OC5 0.1UF/16V
OC6 0.1UF/16V
OC7 0.1UF/16V
OC8 0.1UF/16V
OR1 1MOHM
OR5 10KOhm /X
OU2 RN5VD27CA
OC9 4.7UF/6.3V
OC10 0.1UF/16V
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Check LPC PU in SB
OU1
IT8511TE
Battery
Thermal Sensor
2.3G
OR8 0Ohm
OR9 0Ohm /X
OQ1A UM6K1N
OQ1B UM6K1N
OQ2A UM6K1N
OQ2B UM6K1N
OR2 100KOhm
OR4 100KOhm
OX1
32.768kMhz +/-20ppm/12.5PF
OC11 12PF/50V
OC12 12PF/50V
OT1
OT2
OT3
OT4
OT5
OT6
OT7
OT8
OT9
OT10
OT11
CIR
TSOP6238TR
OR3 100Ohm
OC13 10UF/10V
BOM stuff 06G042012011
Title : EC IT8511E
ASUSTek Computer INC.
Engineer: Chad Lai
C90S
Rev 2.00
Sheet 41 of 55

ISA ROM

EC Hardware Strapping

[FA3/ BADDR1 : FA2/ BADDR0]

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

01: PNPCNG Access Register Pair Are 004Eh and 004Fh

10: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

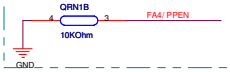
11: Reserved

Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

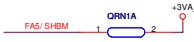
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

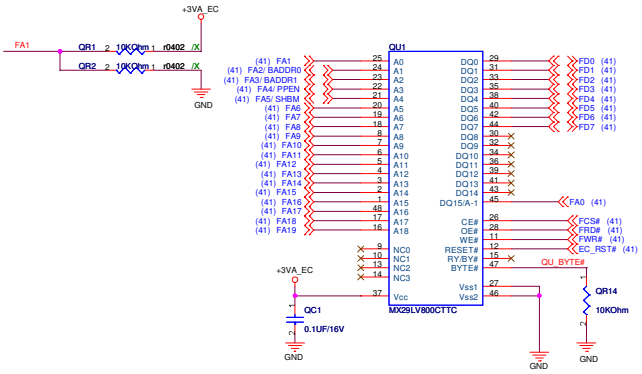


FA5/ SHBM

0: Disable Shared Memory with Host BIOS

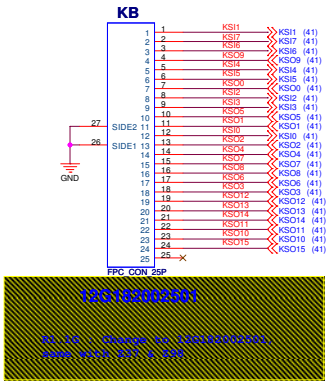
1: Enable Shared Memory with Host BIOS



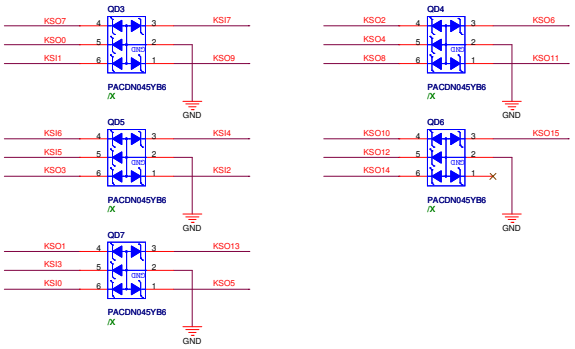


BIOS:05G001204043

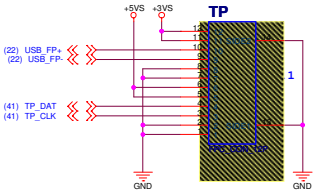
Keyboard Connector



FOR EMI/ESD



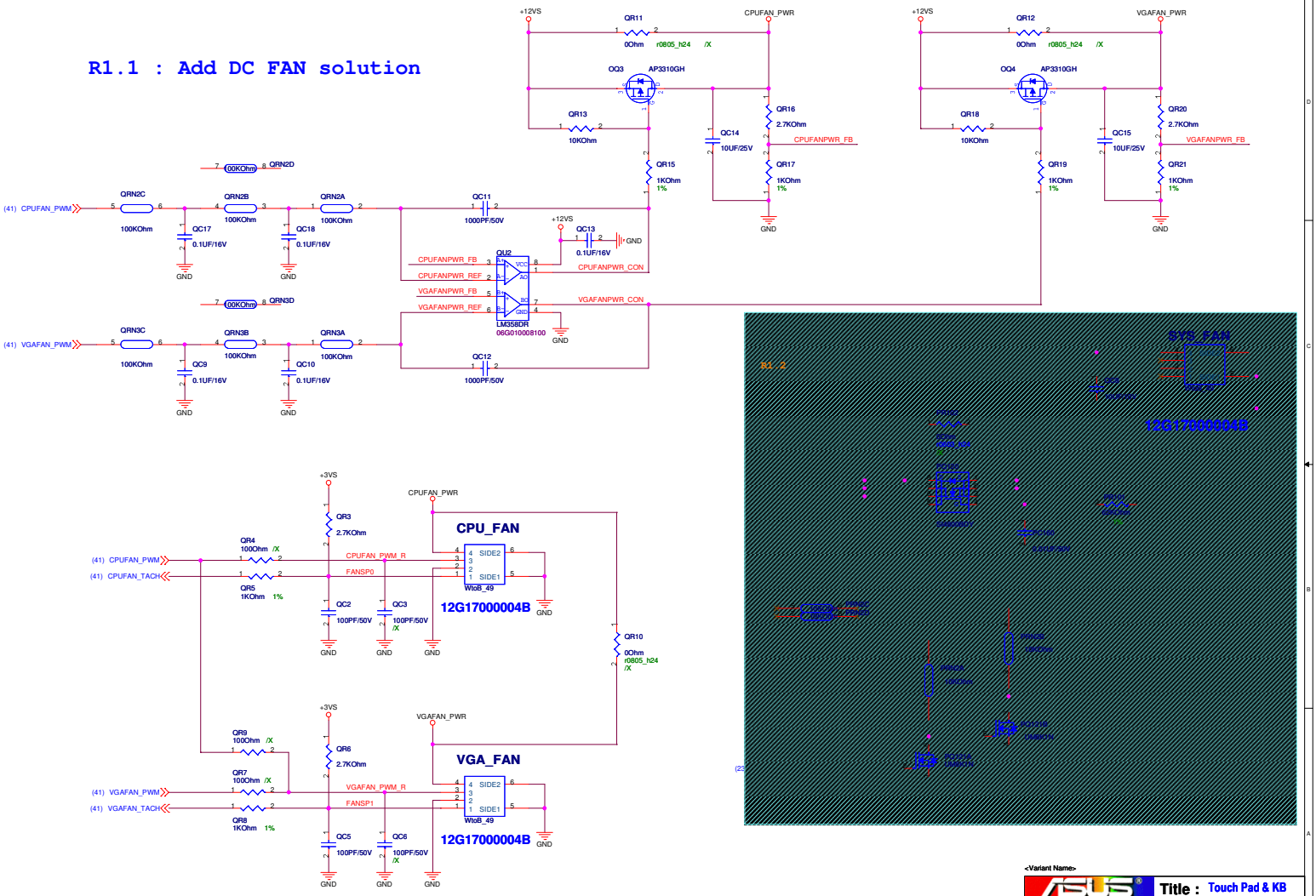
Fingerprint & TouchPad Connector



<Variant Name>

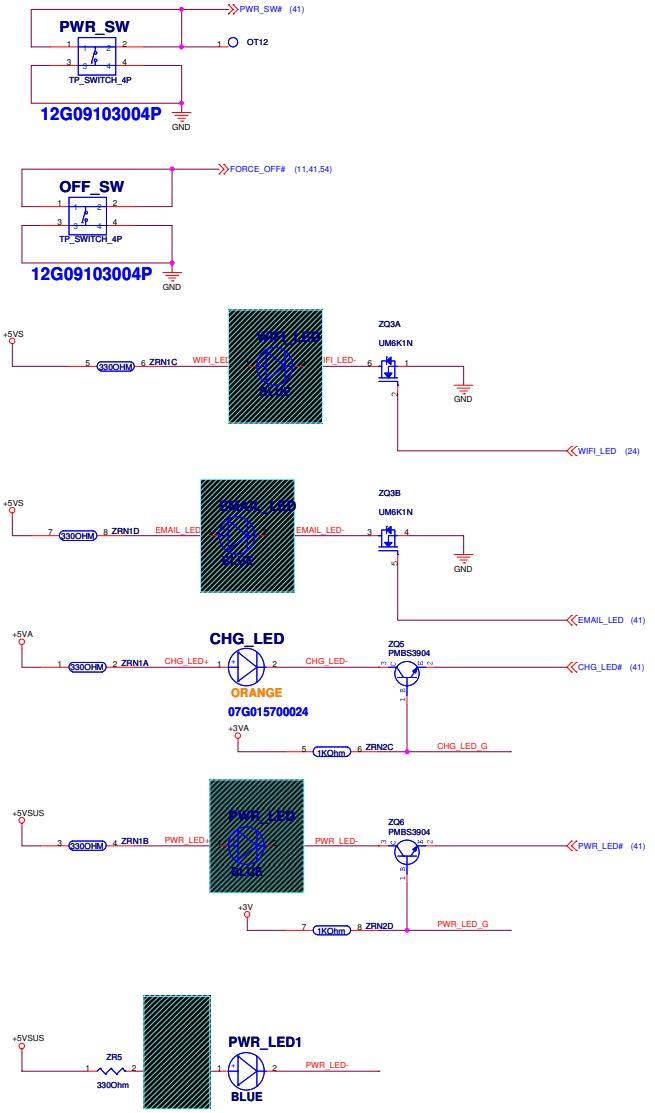
ASUSTek Computer INC.	Title : ISA FLASH ROM	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期二, 六月 30, 2007	Sheet 42 of 55	

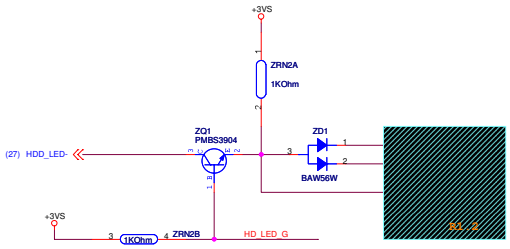
R1.1 : Add DC FAN solution



<Variant Name>

ASUSTek Computer INC.	Title : Touch Pad & KB	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期三, 六月 30, 2007	Sheet 43 of 55	

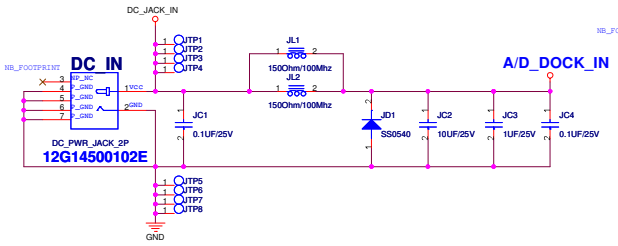




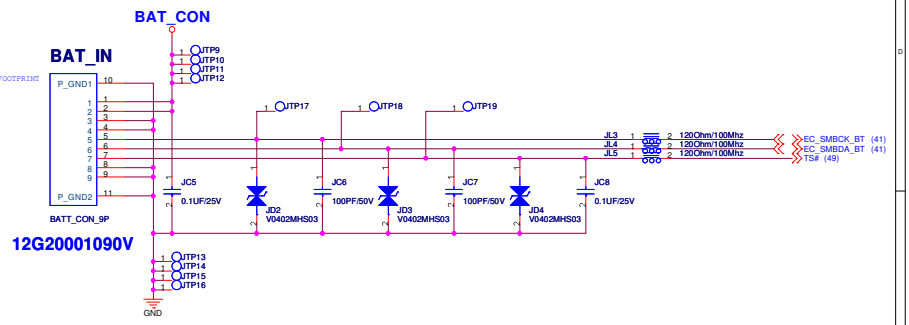
<variant_name>

ASUSTek Computer INC.	Title : LED & SW	
	Engineer: Chad Lai	
Size: Custom	Project Name: C90S	Rev: 2.0G
Date: 星期三, 六月 30, 2007	Sheet 44 of 55	

DC-IN Connector



BAT-IN Connector



<Variant Name>

Title : DC IN & BAT IN

ASUSTek Computer INC.

Engineer: Chad Lai

Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 六月 30, 2007 Sheet 45 of 55

FOR Mini Card_TVTuner (H=7.5mm)

NUT_TV1 — CT217B63D47 — GND
NUT_TV2 — CT217B63D47 — GND

FOR Mini Card_Wireless (H=7.5mm)

NUT_WLS1 — CT217B63D47 — GND
NUT_WLS2 — CT217B63D47 — GND

FOR TPM (H=3mm)

NUT_TPM — L4E_1A — GND

FOR MDC (H=3mm)

NUT_MDC1 — L4E_1A — GND
NUT_MDC2 — L4E_1A — GND

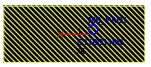
FOR FAN FIXING (H=2.6mm)

NUT_FAN1 — HT-G4034M20TFE — GND
NUT_FAN2 — HT-G4034M20TFE — GND

FOR Power Board (H=4.95mm)

NUT_PWR1 — C236D146 — GND
NUT_PWR2 — C236D146 — GND

M/B PAD (For EMI)



MB_PAD1 — SMD197X197 /X — GND
MB_PAD2 — SMD197X197 /X — GND
MB_PAD3 — SMD197X197 /X — GND
MB_PAD4 — SMD197X197 /X — GND
MB_PAD5 — SMD197X197 /X — GND
MB_PAD6 — SMD197X197 /X — GND
MB_PAD7 — SMD197X197 /X — GND
MB_PAD8 — SMD197X197 /X — GND

SATA HDD PAD

PAD_HDD — 2DRILL_D110N /X — GND

TP PAD (For EMI)

TP_PAD1 — SMD350X118 /X
TP_PAD2 — SMD350X118 /X — GND

Battery PAD (For EMI)

BAT_PAD1 — SMD197X350 /X
BAT_PAD2 — SMD197X350 /X — GND

M/B Screw Hole (Group A)

SCWA1 — S354D110N /X
SCWA2 — S354D110N /X
SCWA3 — S354D110N /X
SCWA4 — S354D110N /X
SCWA5 — S354D110N /X
SCWA6 — S354D110N /X
SCWA7 — S354D110N /X

CPU Heatsink (Group D)

SCWD1 — C315D169 /X
SCWD2 — C315D169 /X — GND
SCWD3 — C315D169 /X
SCWD4 — C315D169 /X — GND

NB Heatsink (Group E)

SCWE1 — C315D161N /X
SCWE2 — C315D161N /X
SCWE3 — C315D161N /X — GND
SCWE4 — C315D161N /X
SCWE5 — C315D161N /X — GND

SH1 — C118D118N /X

M/B Corner Screw Hole (Group B)

SCWB1 — CR354X354D110N /X — GND
SCWB2 — CR354X354D110N /X — GND
SCWB3 — CR354X354D110N /X — GND
SCWB4 — CR354X354D110N /X — GND

Group C

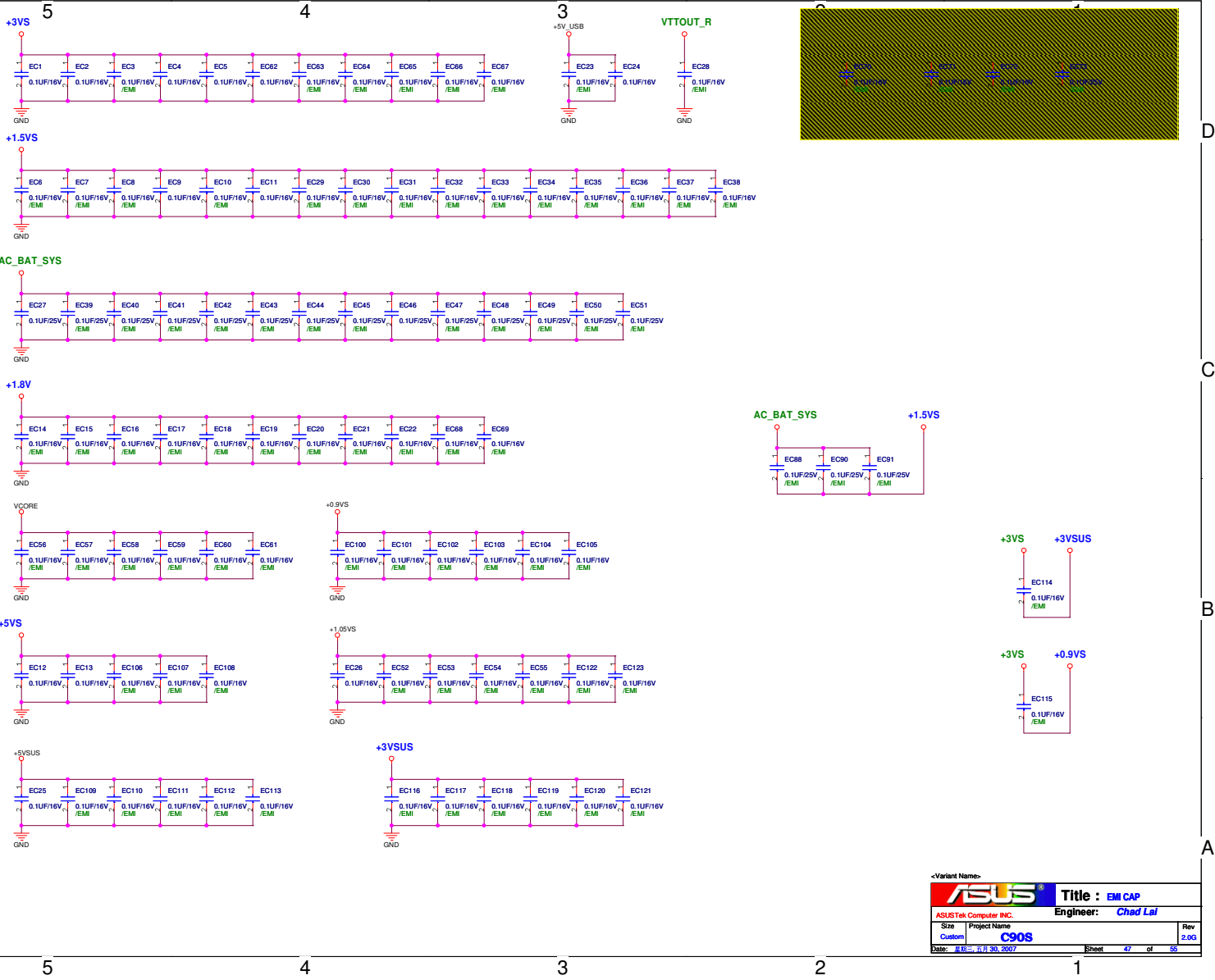
SCWC1 — C276D110N /X — GND

Group F

SCWF1 — RT354X354B236D146 /X — GND

<Variant Name>

Title : Screw Hole
ASUSTek Computer INC.
Engineer: Chad Lai
Size: Custom
Project Name: C90S
Rev: 2.00
Date: 星期二, 六月 30, 2007
Sheet 46 of 55



<Variant Name>

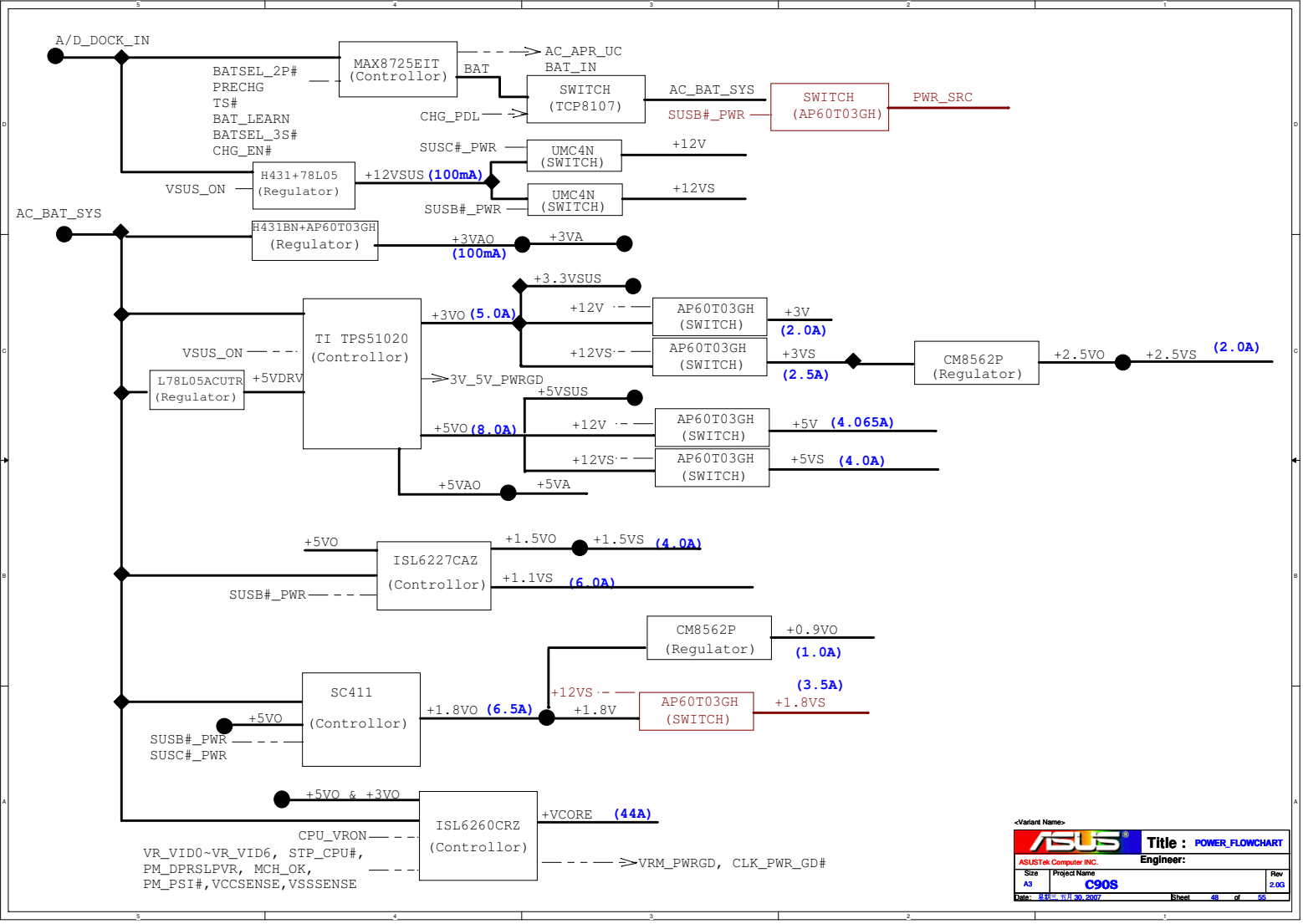
Title : EMI CAP

ASUSTek Computer INC.

Engineer: Chad Lai

Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 五月 30, 2007 Sheet 47 of 55



<Variant Name>

ASUSTek Computer INC.

Title : POWER_FLOWCHART

Engineer:

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期二, 五月 30, 2007 Sheet 48 of 55

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V

Adaptor Max. Current :

PR807=20K PR812 = 178K; Iilimit = 4.5A; 81W
PR807=27K PR812 = 47K; Iilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA
Victl = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Victl = 2.084V
=> Icharge = 1.6933A
BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V
=> Icharge = 2.9329A

PR814=120K PR813 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

BAT — BAT_CON

(41) BATSEL_2P#
BATSEL_2P# = 1, 3 Cells
BATSEL_2P# = 0, 6 or 9 Cells

(41) PRECHG
PRECHG = 1, Pre-Charging Mode
Charging Current = 156mA

(41) CHG_EN#
CHG_EN# = 1, Charger Disabled
CHG_EN# = 0, Charger Enabled

(16,41,51) AC_OK
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent

(41) BAT_LEARN
BAT_LEARN = 1, Battery discharges
BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

AC_APR_UC (41)
AC_APR_UC = 1, Adaptor is present
AC_APR_UC = 0, Adaptor is absent

(45) TS#
TS# = 1; Battery absence
TS# = 0; Battery Plug-in

BAT_IN_OC# = 1; Battery absence
BAT_IN_OC# = 0; Battery Plug-in
BAT_IN (41)

<Variant Name>

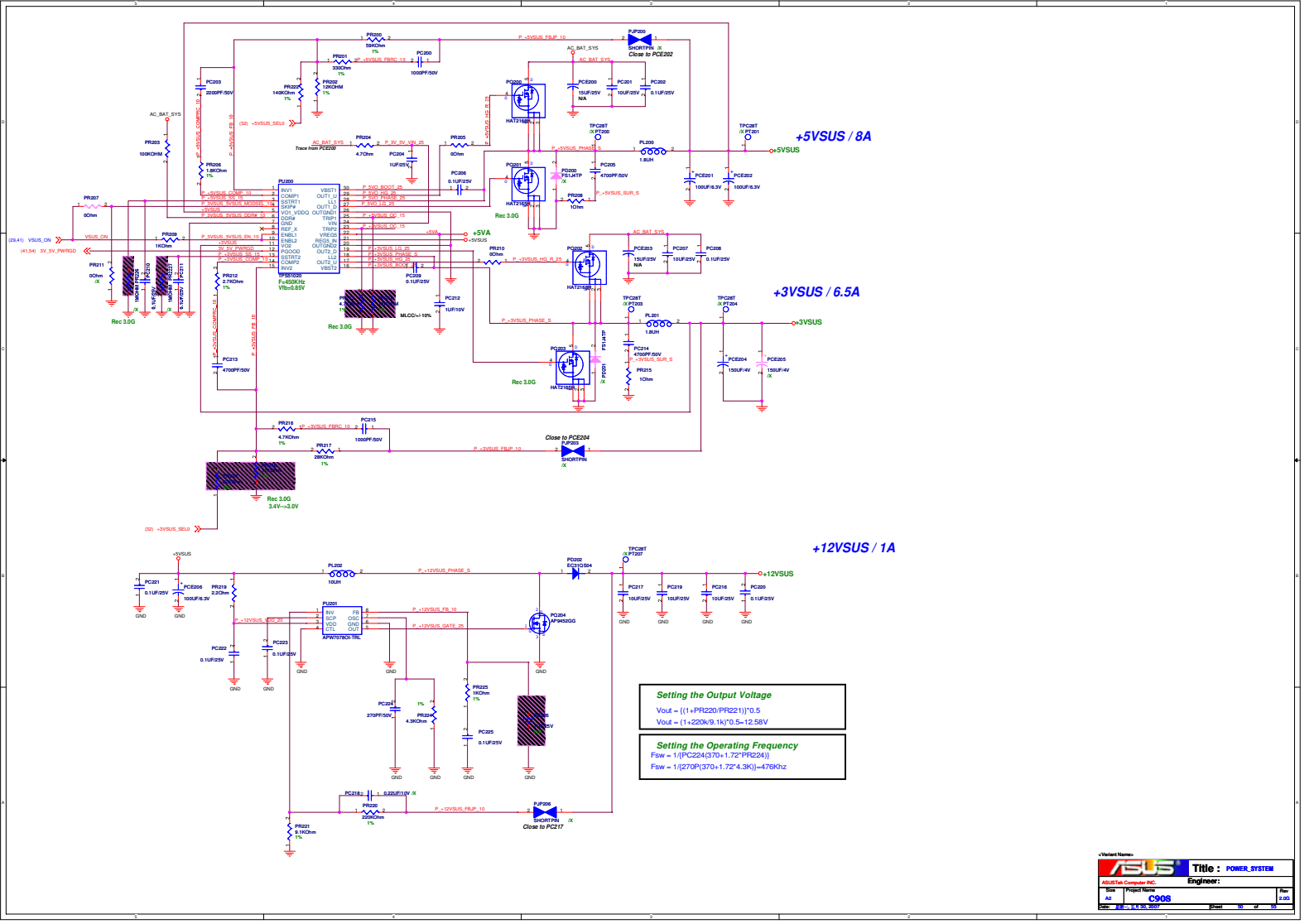
ASUSTeK Computer INC.

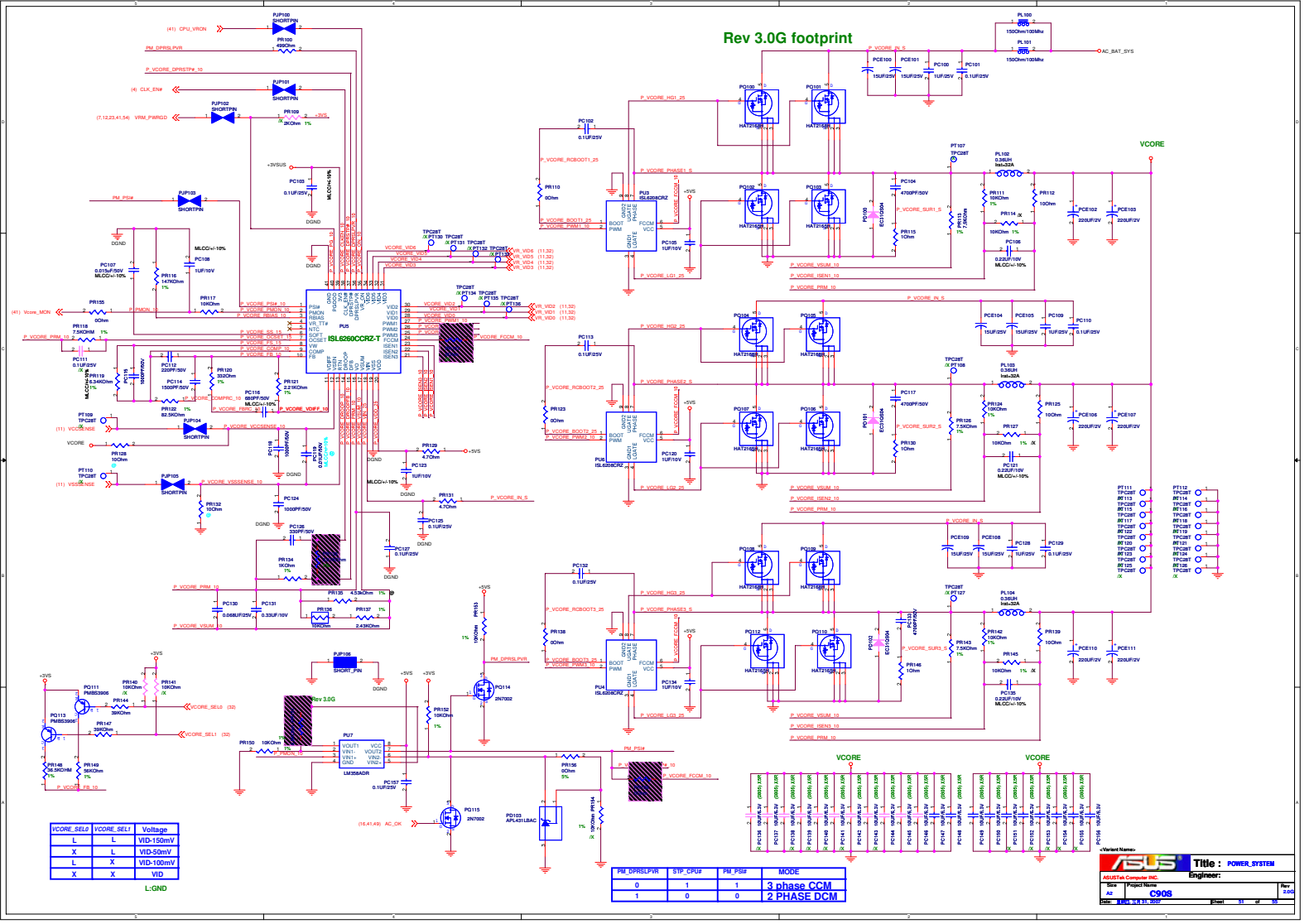
Title : POWER_CHARGER

Engineer:

Size	Project Name	Rev
C	C90S	2.0G

Date: 星期二, 九月 30, 2007 Sheet 49 of 55

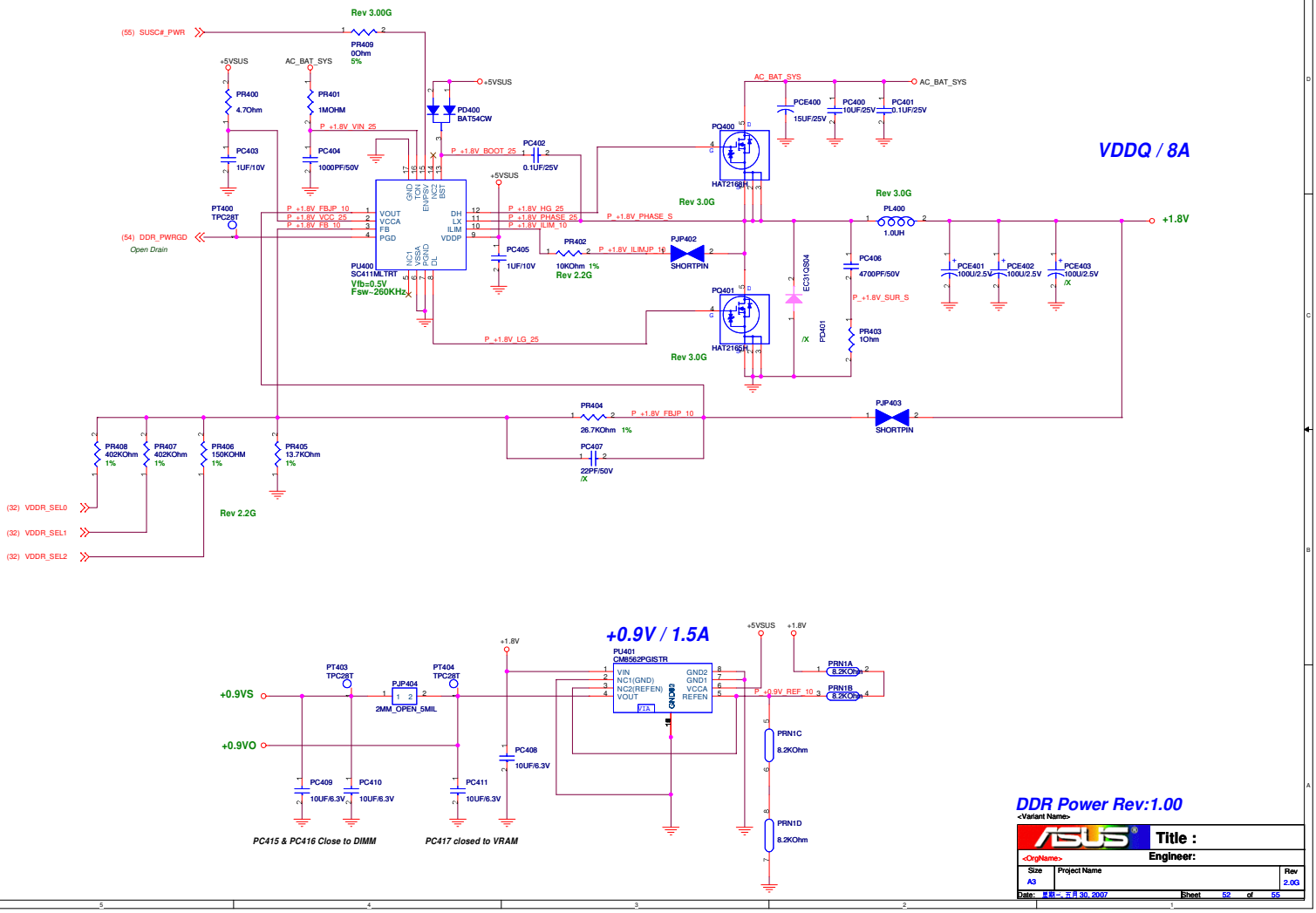

+5VSUS / 8A
+3VSUS / 6.5A
+12VSUS / 1A
Setting the Output Voltage
Vout = (1+PR220/PR221)*0.5
Vout = (1+220k/9.1k)*0.5~12.58V
Setting the Operating Frequency
Fsw = 1/(PC224(370+1.72*PR224))
Fsw = 1/(270P(370+1.72*4.3K))=476Khz
Title : POWER_SYSTEM
ASUSTek Computer INC.
Engineer:
C906



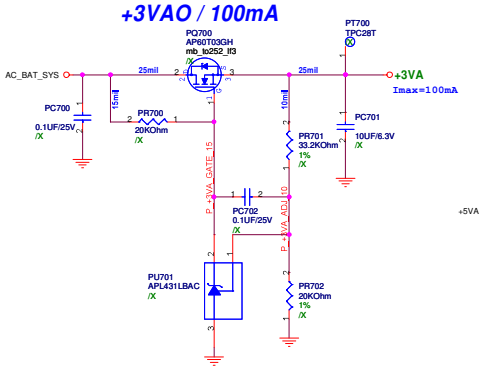
VCORE_SEL0	VCORE_SEL1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID

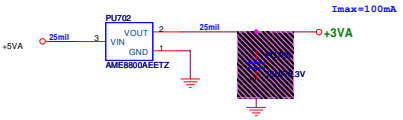
L:GND

PM_DPRSLPVR	STP_CPU#	PM_PSI#	MODE
0	1	1	3 phase CCM
1	0	0	2 PHASE DCM

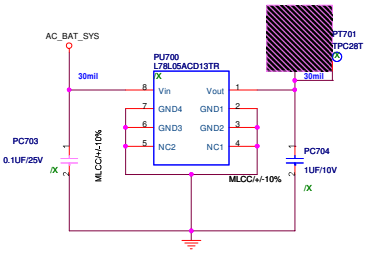

Rev 3.00G
(55) SUSC#_PWR
PR409
0Ohm
5%
+5VSUS
AC_BAT_SYS
PR400
4.7Ohm
PR401
1MOHM
PC403
1UF/10V
PC404
1000PF/50V
P_+1.8V_VIN_25
PD400
BAT54CW
PC402
0.1UF/25V
P_+1.8V_BOOT_25
PT400
TPC28T
(54) DDR_PWRGD
Open Drain
P_+1.8V_FBJP_10
P_+1.8V_VCC_25
P_+1.8V_FB_10
PU400
SC411MLTRT
Vfb=0.5V
Fsw~260KHz
P_+1.8V_HG_25
P_+1.8V_PHASE_25
P_+1.8V_ILIM_10
PC405
1UF/10V
PR402
10KOhm 1%
Rev 2.2G
P_+1.8V_ILIMJP_10
PJP402
SHORTPIN
PC400
HAT2168H
PC401
HAT2165H
PCE400
15UF/25V
PC400
10UF/25V
PC401
0.1UF/25V
VDDQ / 8A
Rev 3.0G
P_+1.8V_PHASE_S
PL400
1.0UH
+1.8V
PC406
4700PF/50V
PCE401
100U/2.5V
PCE402
100U/2.5V
PCE403
100U/2.5V
/X
P_+1.8V_SUR_S
EC31QS04
PD401
PR403
1Ohm
P_+1.8V_LG_25
PR404
26.7KOhm 1%
P_+1.8V_FBJP_10
PJP403
SHORTPIN
PC407
22PF/50V
/X
PR408
402KOhm
1%
PR407
402KOhm
1%
PR406
150KOHM
1%
PR405
13.7KOhm
1%
(32) VDDR_SEL0
(32) VDDR_SEL1
(32) VDDR_SEL2
Rev 2.2G
+0.9V / 1.5A
PU401
CM8562PGISTR
VIN
NC1(GND)
NC2(REFEN)
VOUT
GND2
GND1
VCCA
REFEN
P_+0.9V_REF_10
PRN1A
8.2KOhm
PRN1B
8.2KOhm
PRN1C
8.2KOhm
PRN1D
8.2KOhm
PT403
TPC28T
PT404
TPC28T
PJP404
2MM_OPEN_5MIL
+0.9VS
+0.9VO
PC408
10UF/6.3V
PC409
10UF/6.3V
PC410
10UF/6.3V
PC411
10UF/6.3V
PC415 & PC416 Close to DIMM
PC417 closed to VRAM
DDR Power Rev:1.00
<Variant Name>
Title :
<OrgName>
Engineer:
Size
A3
Project Name
Rev
2.0G
Date: 星期一, 五月 30, 2007
Sheet 52 of 55

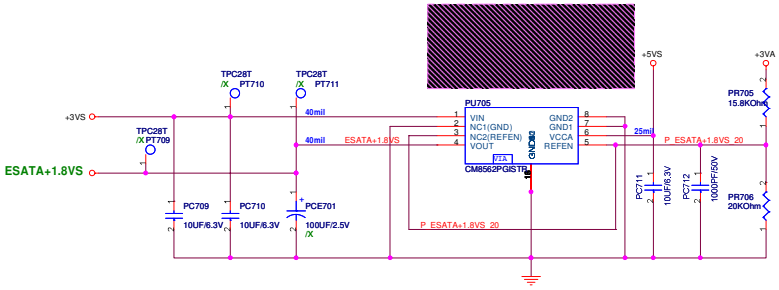
+3VAO / 100mA



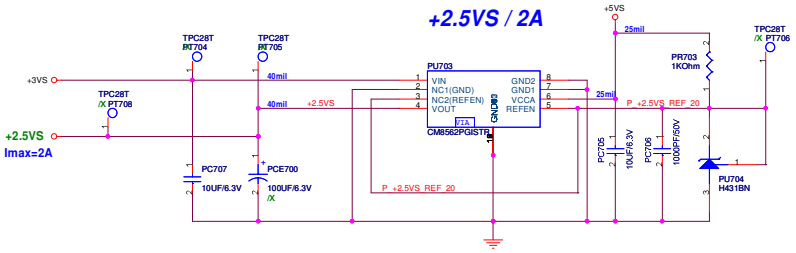


For CIR Power





+2.5VS / 2A



<Variant Name>

ASUSTek Computer INC.

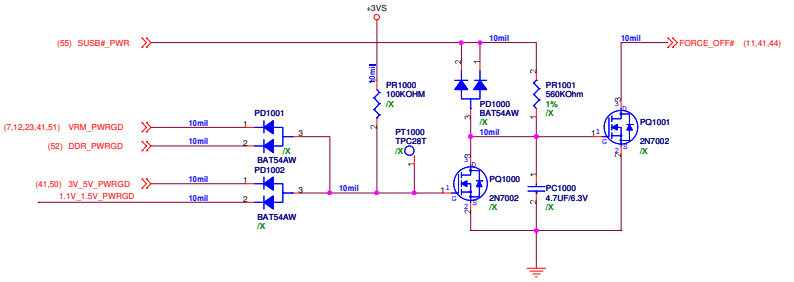
Title : POWER_I/O_+3VA & +2.5V

Engineer:

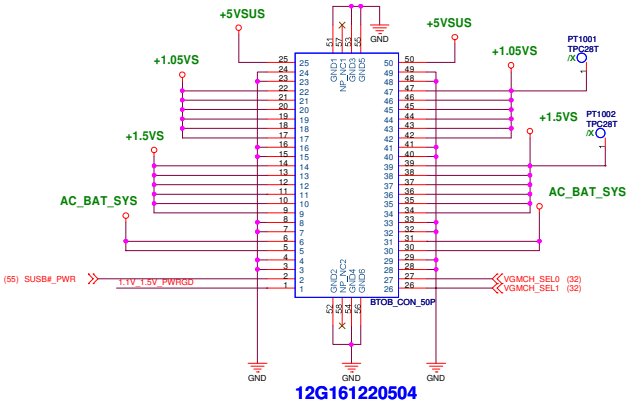
Size	Project Name	Rev
Custom	C90S	2.0G

Date: 星期二, 四月 30, 2007 Sheet 53 of 55

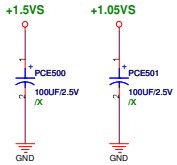
Power Good Detecter



PCON1



12G161220504



Near NB & SB

<Variant Name>

ASUSTek Computer INC.

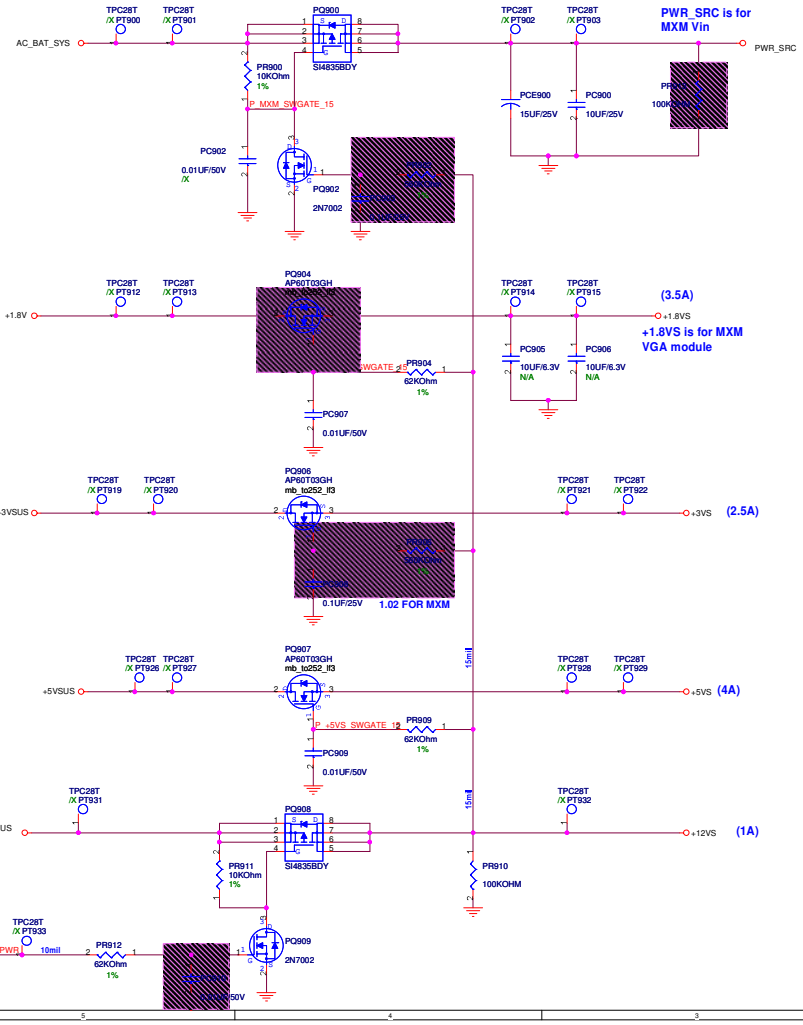
Title : POWER_PROTECT

Engineer:

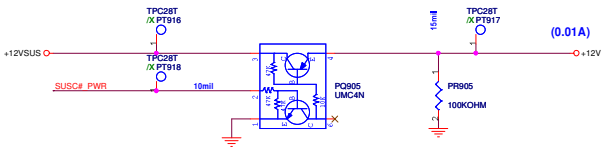
Size	Project Name	Rev
Custom	C90S	2.0G

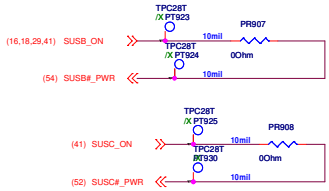
Date: 星期三, 六月 30, 2007 Sheet 54 of 55

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

Title : POWER_LOAD SWITCH

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
A3	C90S	2.0G

Date: 星期三, 五月 30, 2007 Sheet 55 of 55