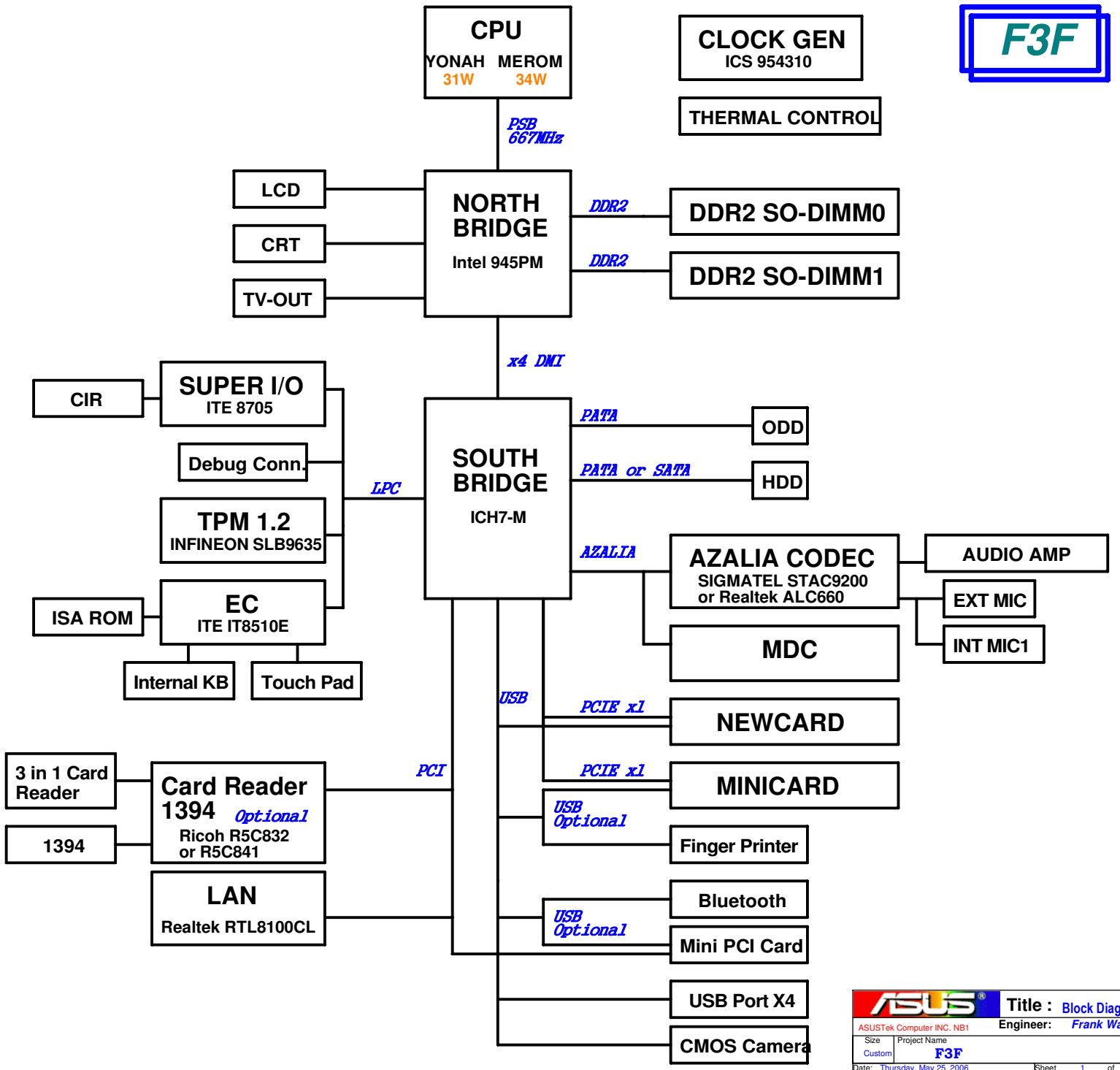


ASUSTek Computer INC. NB1

Title : Block Diagram

Engineer: Frank Wang

Size	Project Name	Rev
Custom	F3F	2.1

Date: Thursday, May 25, 2006 Sheet 1 of 89

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	/	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	BT_ON#	O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BTLED_ON	O
AC18	GPIO07	WLAN_LED_EN	O
E21	GPIO08	EXTSMI#	I
E20	GPIO09	/	
A20	GPIO10	WLAN_ON#	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	CB_SD#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	TP_LEDON	O
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	CPU_SELECT	O
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	/	
A21	GPIO26/EL_RSVD	/	
B21	GPIO27/EL_STATE0	BT_DET#	
E23	GPIO28/EL_STATE1	/	
C3	GPIO29/OC#5	USB_OC#5	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC#7	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	PANEL_ID0	I
AH19	GPIO36/SATA2GP	PANEL_ID1	I
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	C
R5C832 CARD READER	AD17	0	C
R5C832 1394	AD17	0	B
R5C841 CARD READER	AD18	1	C
R5C841 1394	AD18	1	B
Mini PCI Card	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

ASUSTek Computer INC. NB1

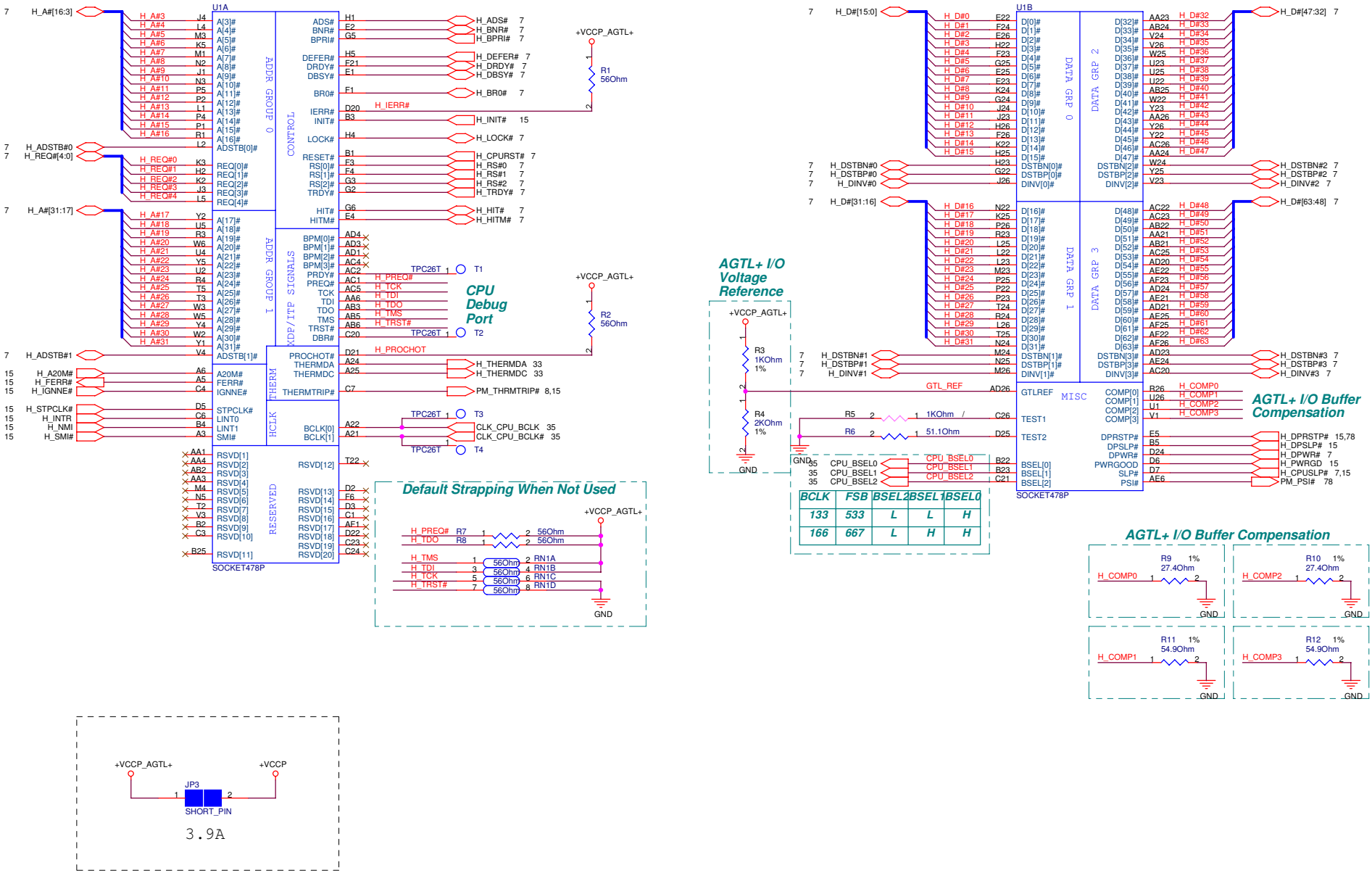
Title : System Setting

Engineer: Frank Wang

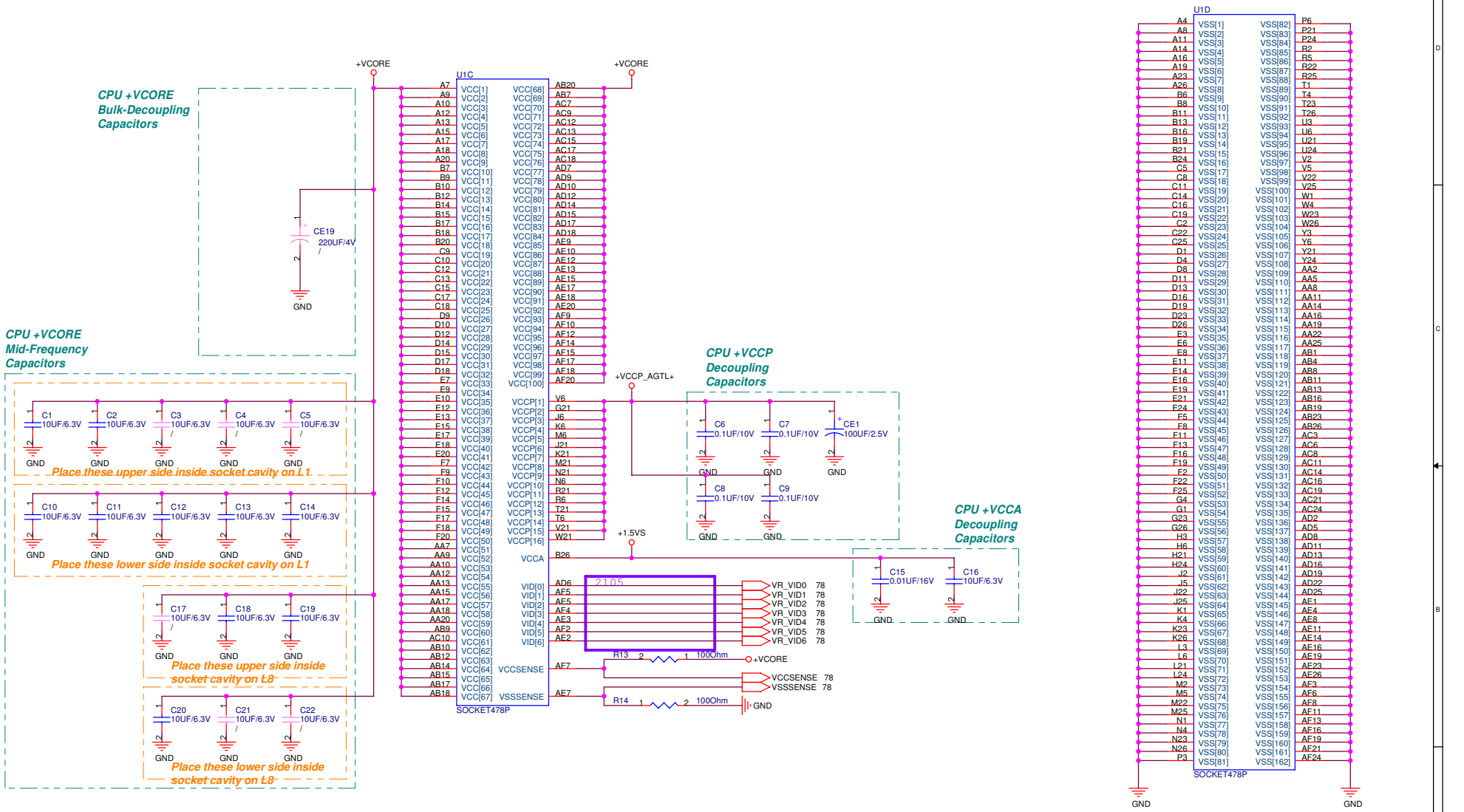
Size	Project Name	Rev
Custom	F3F	2.1

Date: Thursday, May 25, 2006 Sheet 2 of 89

ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 3 of 89	



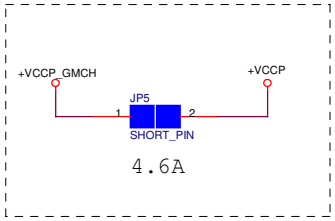
ASUSTeK COMPUTER INC. NB1	Title : CPU-YONAH(HOST)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 4 of 89		



+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

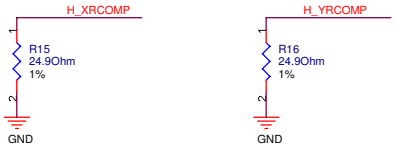
ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 5 of 89	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 6 of 89



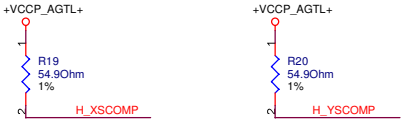
RCOMP

For Calibrating the FSB I/O Buffer



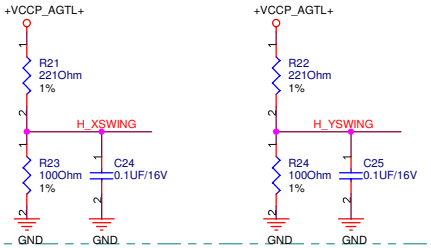
SCOMP

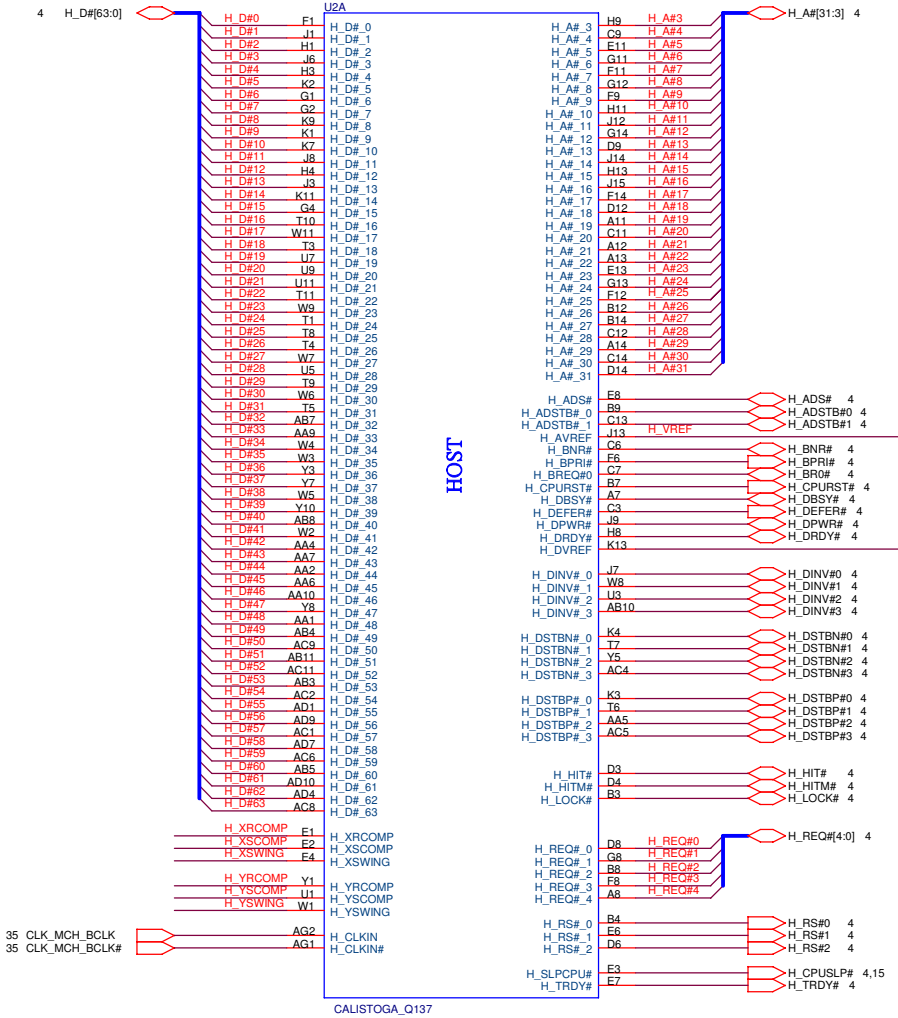
For Slew Rate Compenssation on the FSB



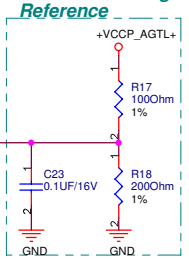
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits





AGTL+ I/O Voltage Reference



ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(HOST)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 7 of 89		

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — R25 1KOhm — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — R26 1KOhm — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable

1 = Normal Operation (D)

MCH_CFG_15 — R27 1KOhm — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — R30 1KOhm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 1KOhm — GND

CFG10 : HOST PLL VCO Select

0 = Reserved

1 = Mobility (D)

MCH_CFG_10 — R34 1KOhm — GND

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

MCH_CFG_18 — R35 1KOhm — +2.5VS

CFG11 : PSB 4x CLK Enable

0 = 4x Enable

1 = 8x Enable (D)

MCH_CFG_11 — R37 1KOhm — GND

CFG19 : DMI Lane Reversal

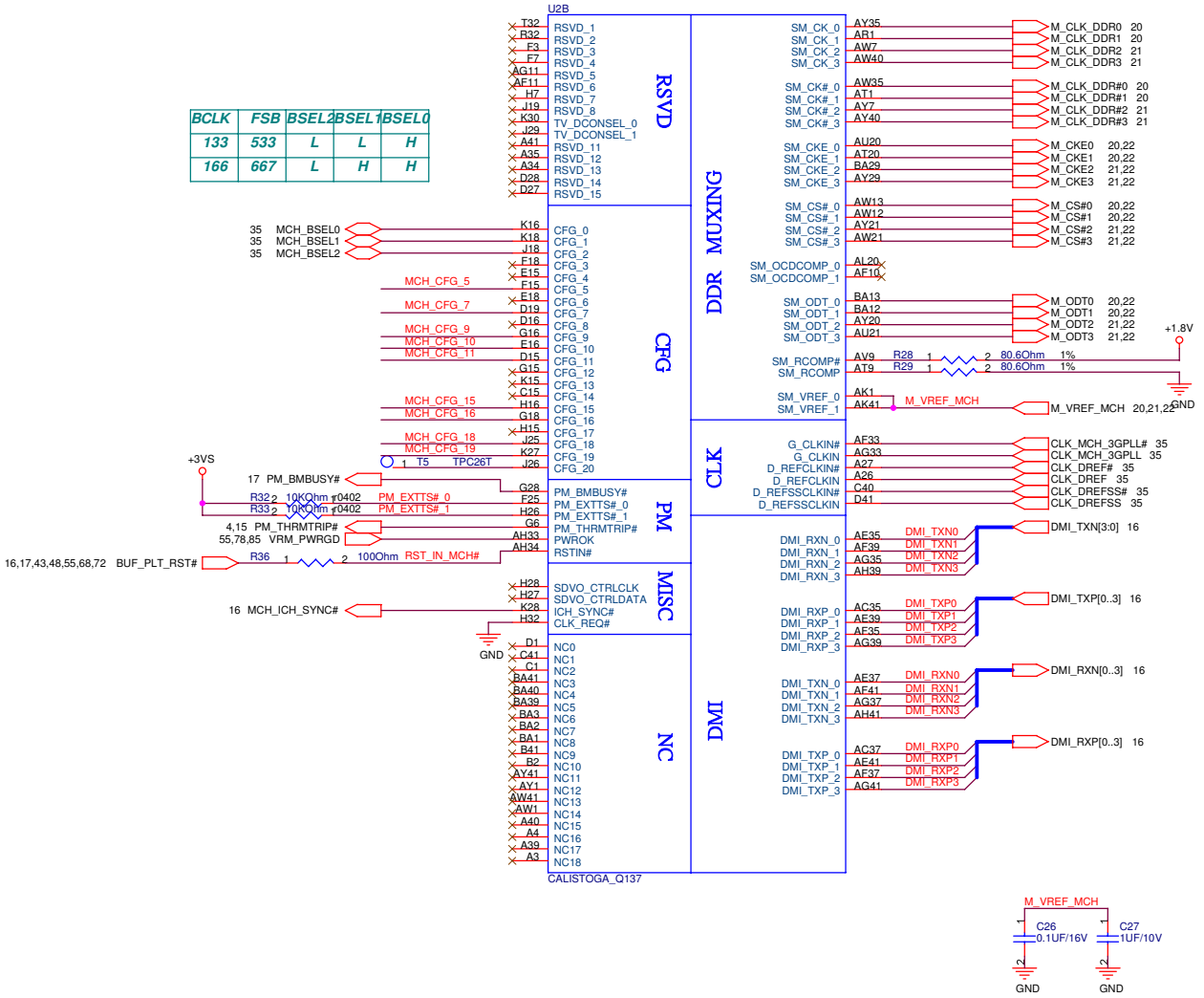
0 = Normal Operation (D)

1 = Lanes Reversed

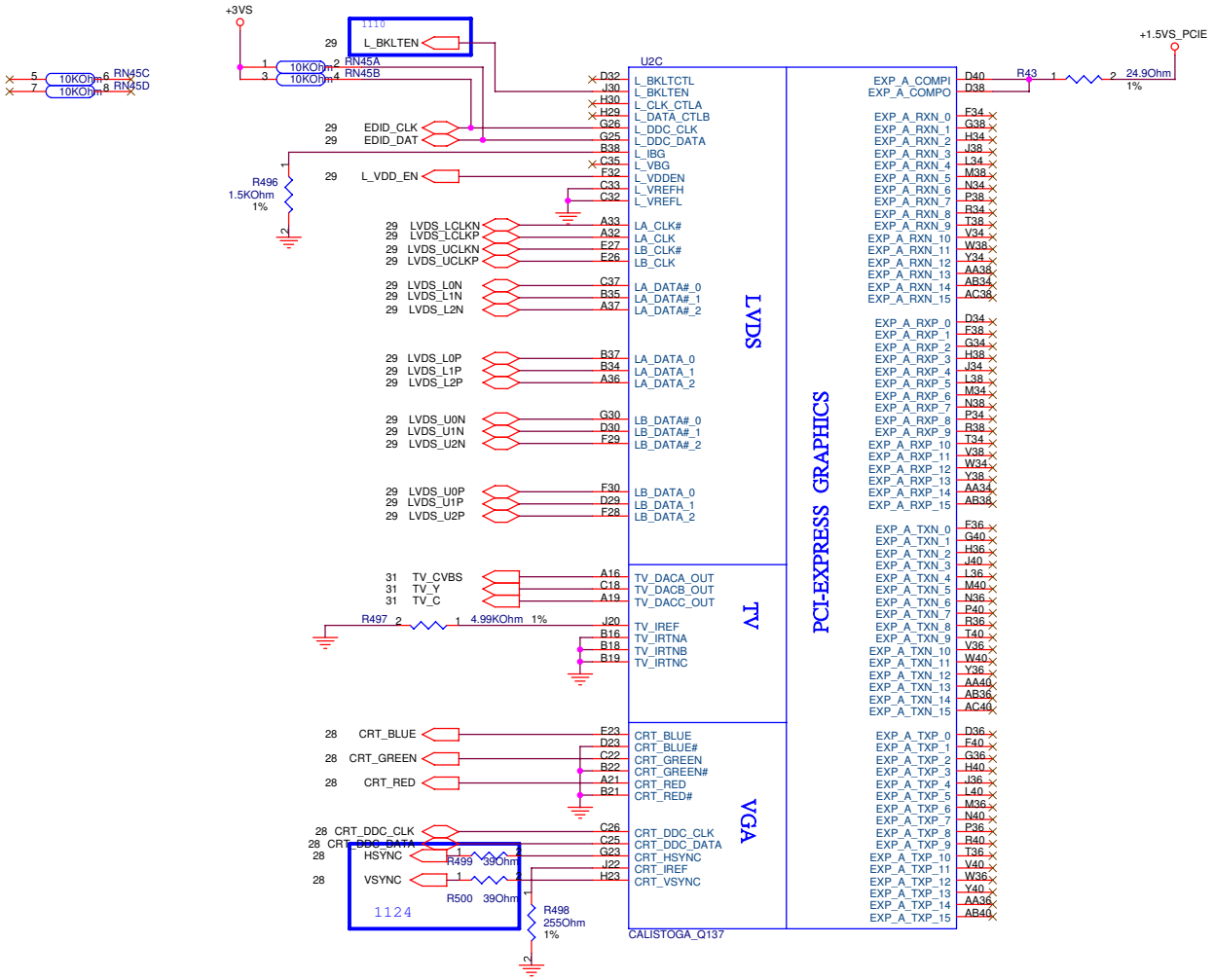
MCH_CFG_19 — R38 1KOhm — +2.5VS

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

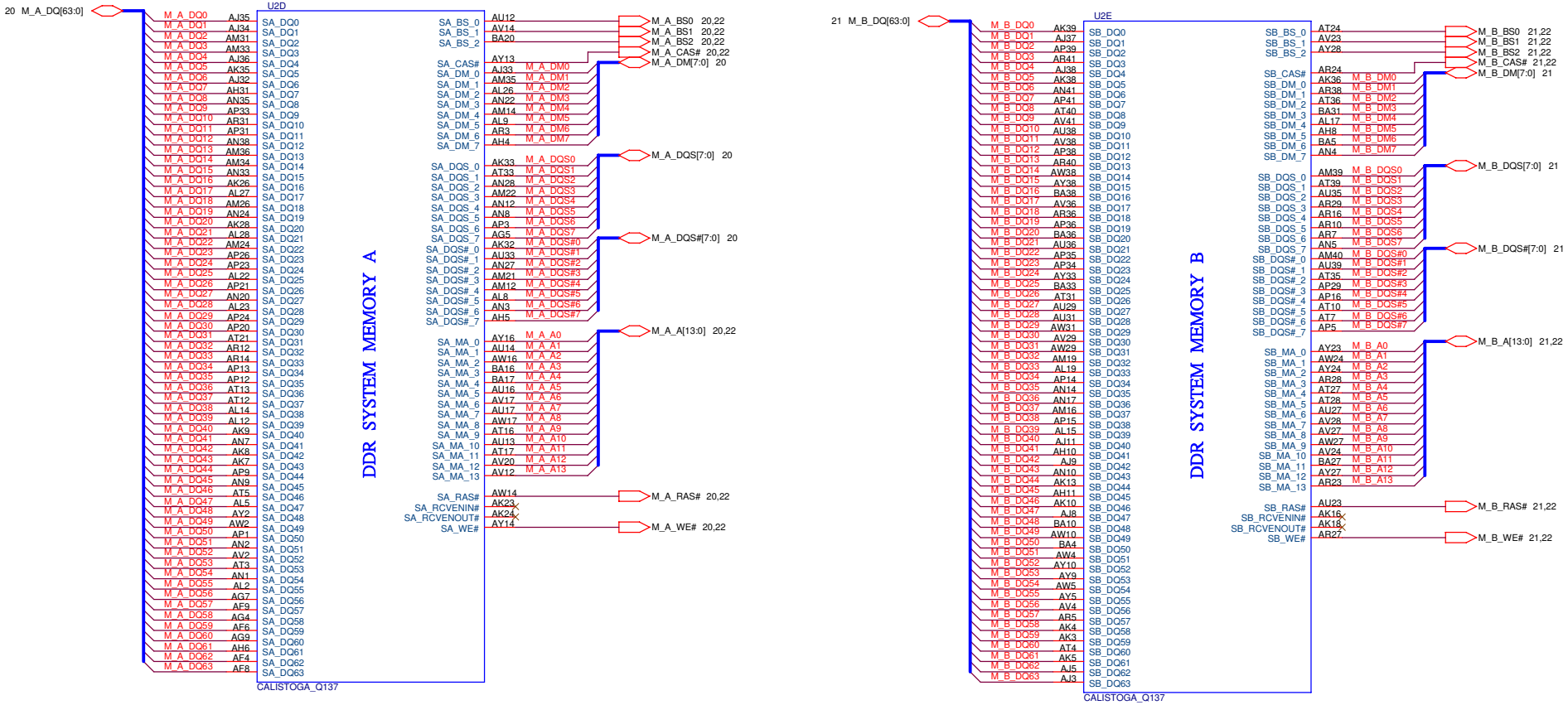
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



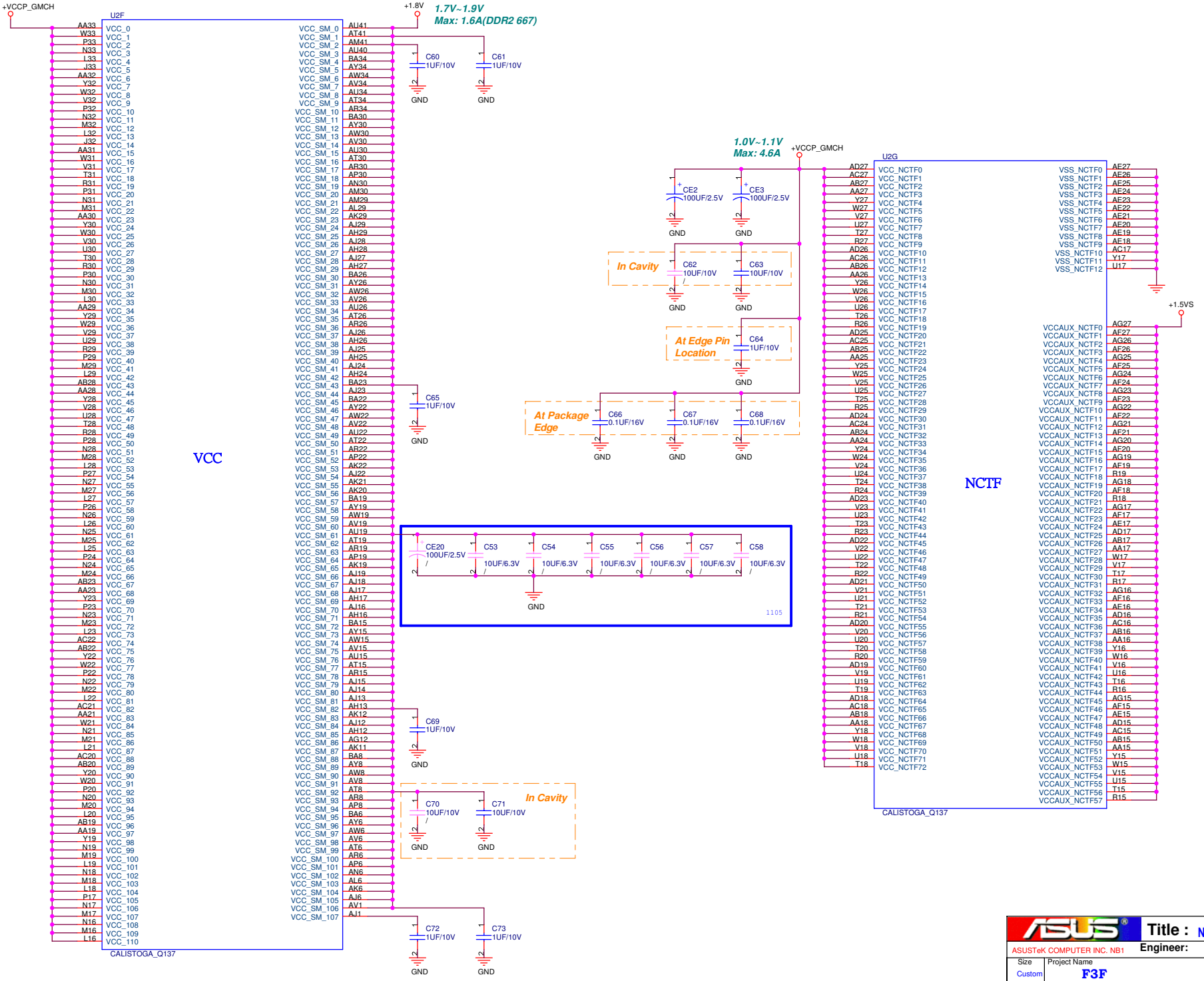
ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(DMI & CFG)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 8 of 89		

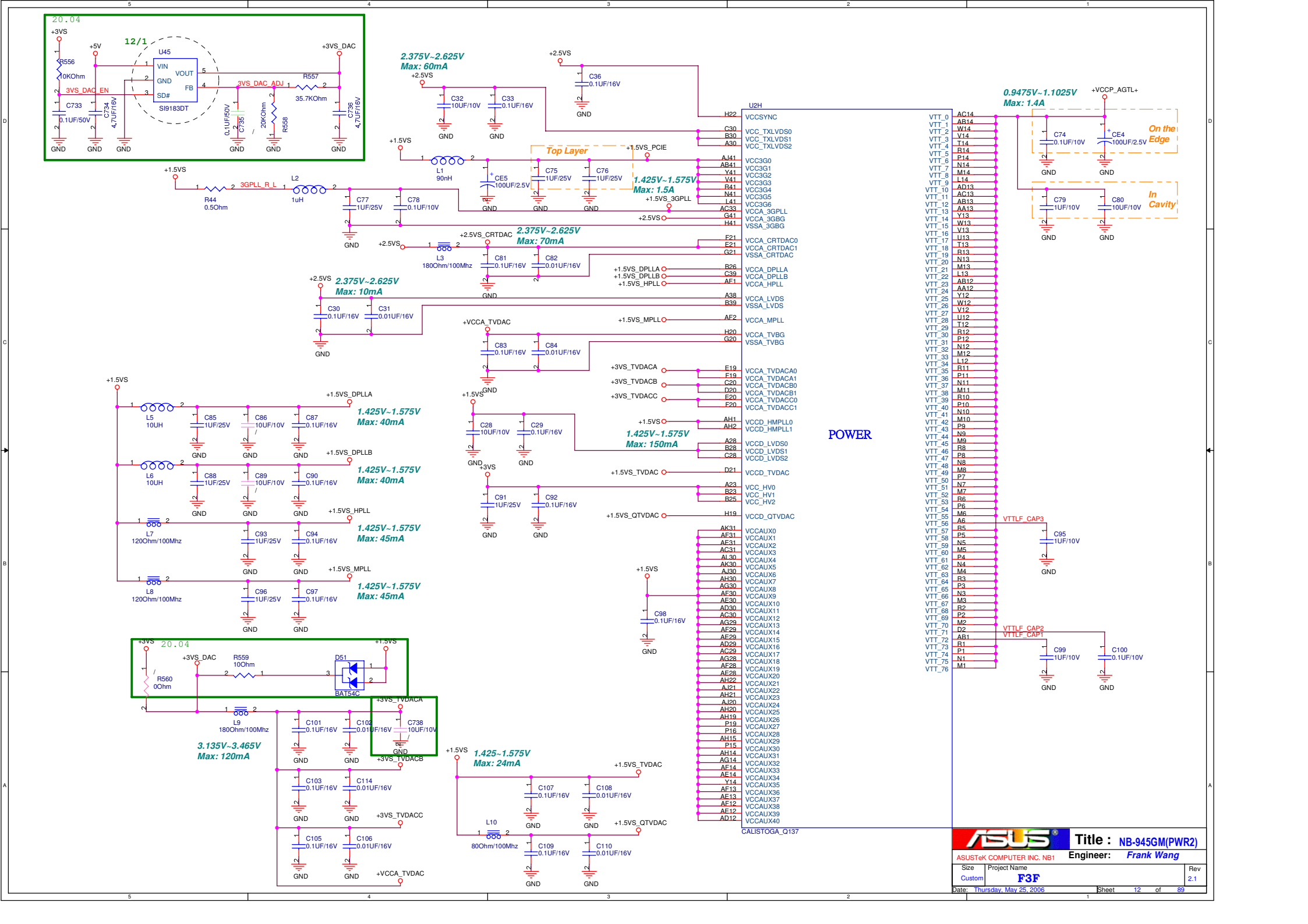


ASUSTeK COMPUTER INC. NB1	Title : NB_945GM(GRAPHIC)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 9 of 89		



ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(DDR2)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 10 of 89		


+VCCP_GMCH
U2F
VCC
CALISTOGA_Q137
+1.8V
1.7V~1.9V
Max: 1.6A(DDR2 667)
C60 1UF/10V
C61 1UF/10V
C65 1UF/10V
C69 1UF/10V
C70 10UF/10V
C71 10UF/10V
In Cavity
C72 1UF/10V
C73 1UF/10V
GND
1.0V~1.1V
Max: 4.6A
CE2 100UF/2.5V
CE3 100UF/2.5V
C62 10UF/10V
C63 10UF/10V
At Edge Pin Location
C64 1UF/10V
At Package Edge
C66 0.1UF/16V
C67 0.1UF/16V
C68 0.1UF/16V
CE20 100UF/2.5V
C53 10UF/6.3V
C54 10UF/6.3V
C55 10UF/6.3V
C56 10UF/6.3V
C57 10UF/6.3V
C58 10UF/6.3V
1105
U2G
NCTF
CALISTOGA_Q137
+1.5VS
Title : NB-945GM(PWR)
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Wang
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
Sheet 11 of 89


20.04
12/1
U45
SI9183DT
3VS_DAC_EN
3VS_DAC_ADJ
R556 10KOhm
R557 35.7KOhm
R558 20KOhm
C733 0.1UF/50V
C734 4.7UF/16V
C735 0.1UF/50V
C736 4.7UF/16V
2.375V~2.625V
Max: 60mA
Top Layer
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
2.375V~2.625V
Max: 10mA
1.425V~1.575V
Max: 150mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
3.135V~3.465V
Max: 120mA
1.425~1.575V
Max: 24mA
0.9475V~1.1025V
Max: 1.4A
On the Edge
In Cavity
POWER
U2H
CALISTOGA_Q137
BAT54C
R559 10Ohm
R560 0Ohm
R44 0.5Ohm
L1 90nH
L2 1uH
L3 180Ohm/100Mhz
L5 10UH
L6 10UH
L7 120Ohm/100Mhz
L8 120Ohm/100Mhz
L9 180Ohm/100Mhz
L10 80Ohm/100Mhz
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
Title : NB-945GM(PWR2)
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Wang
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
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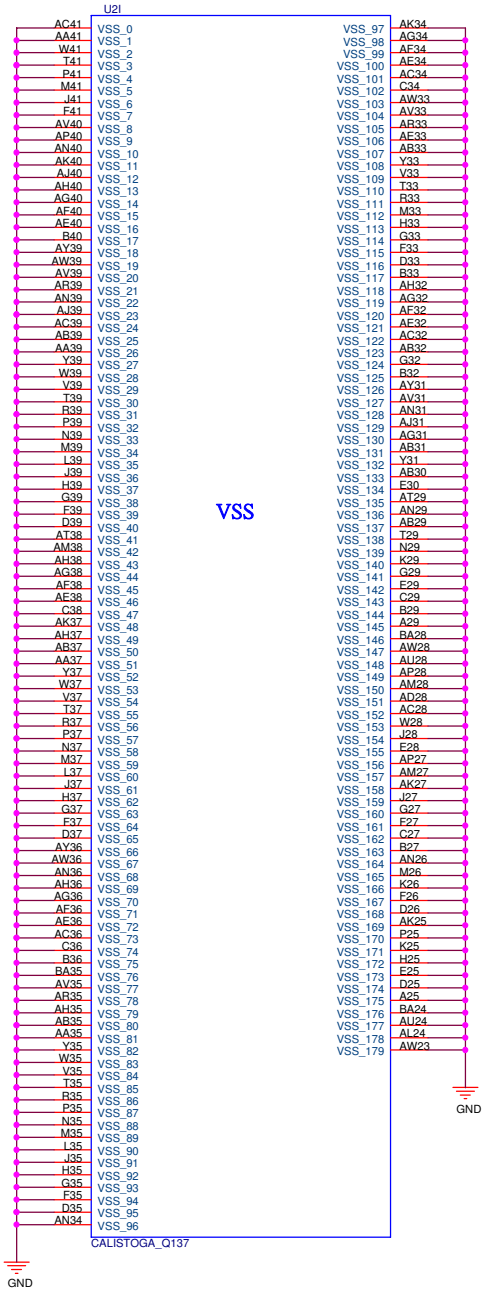
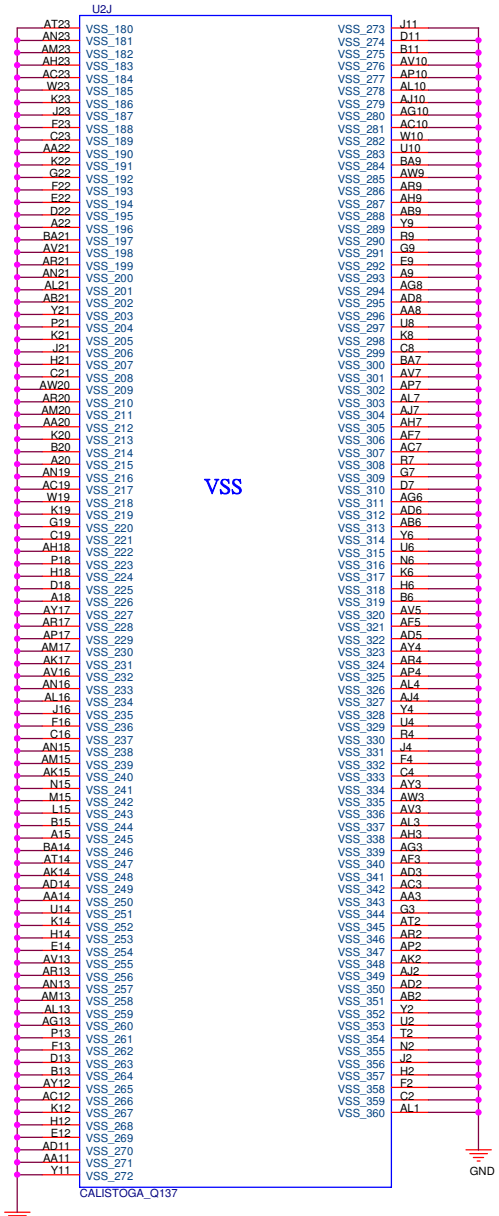
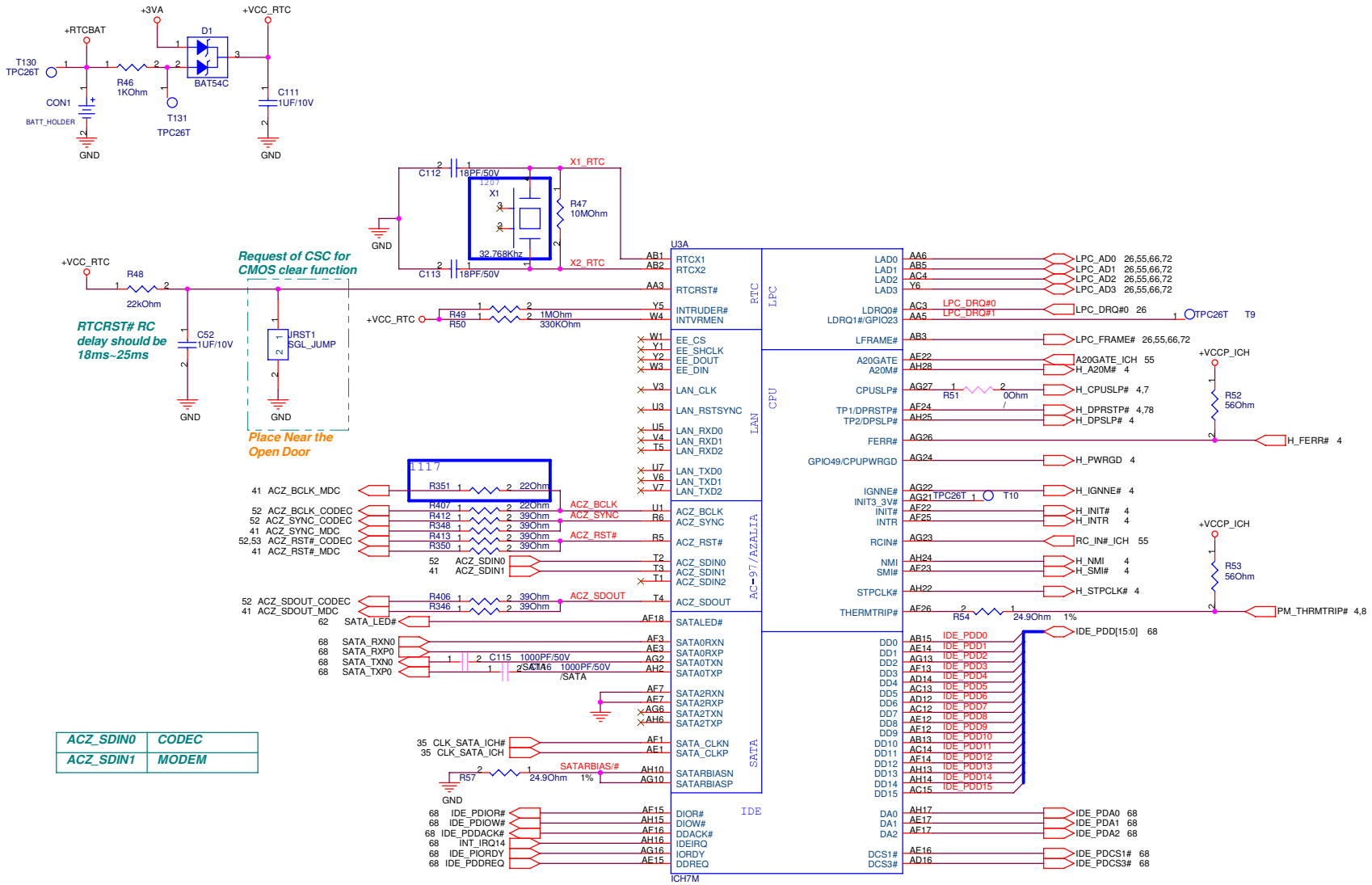


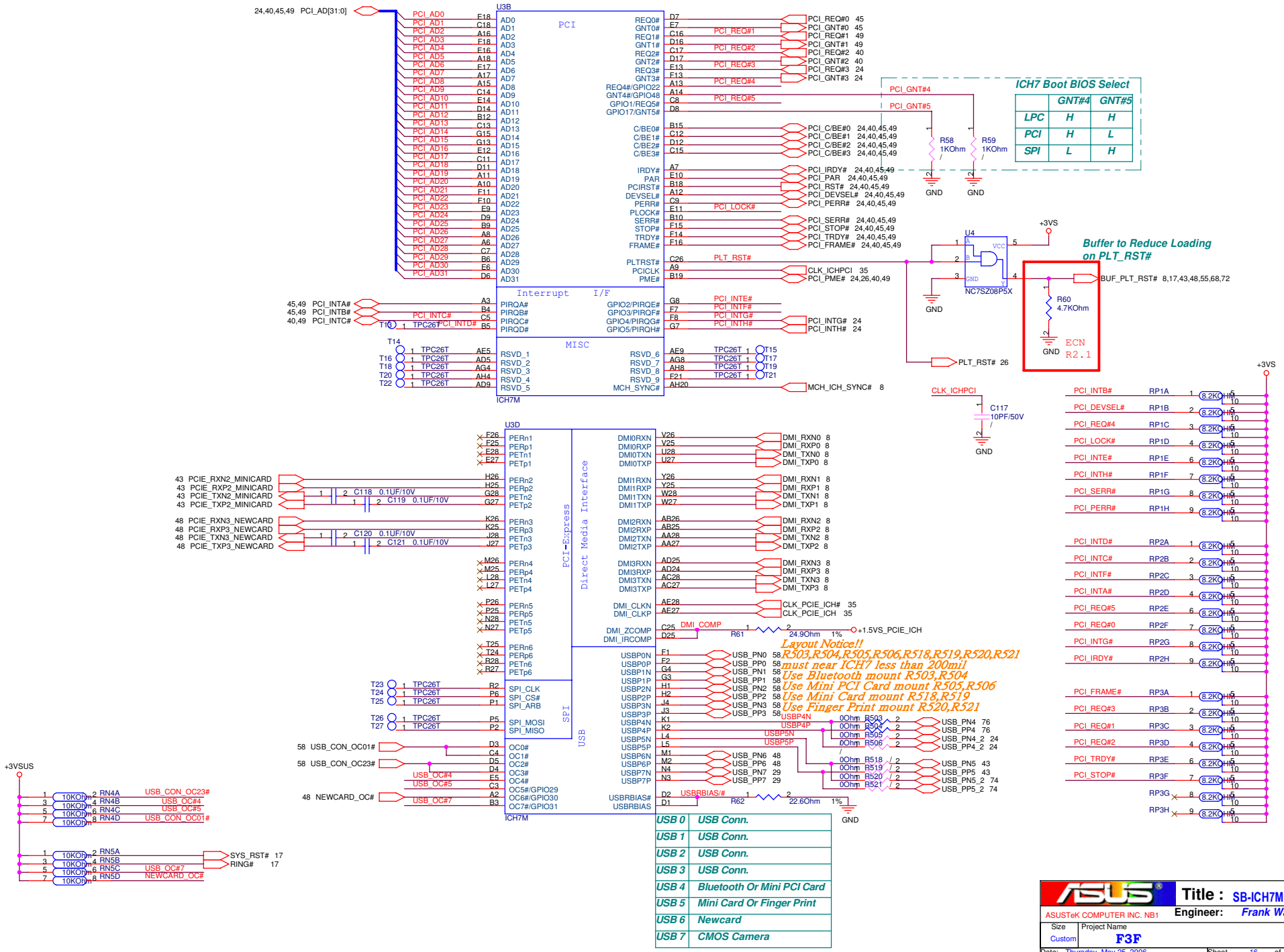


ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(GND)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 13 of 89		

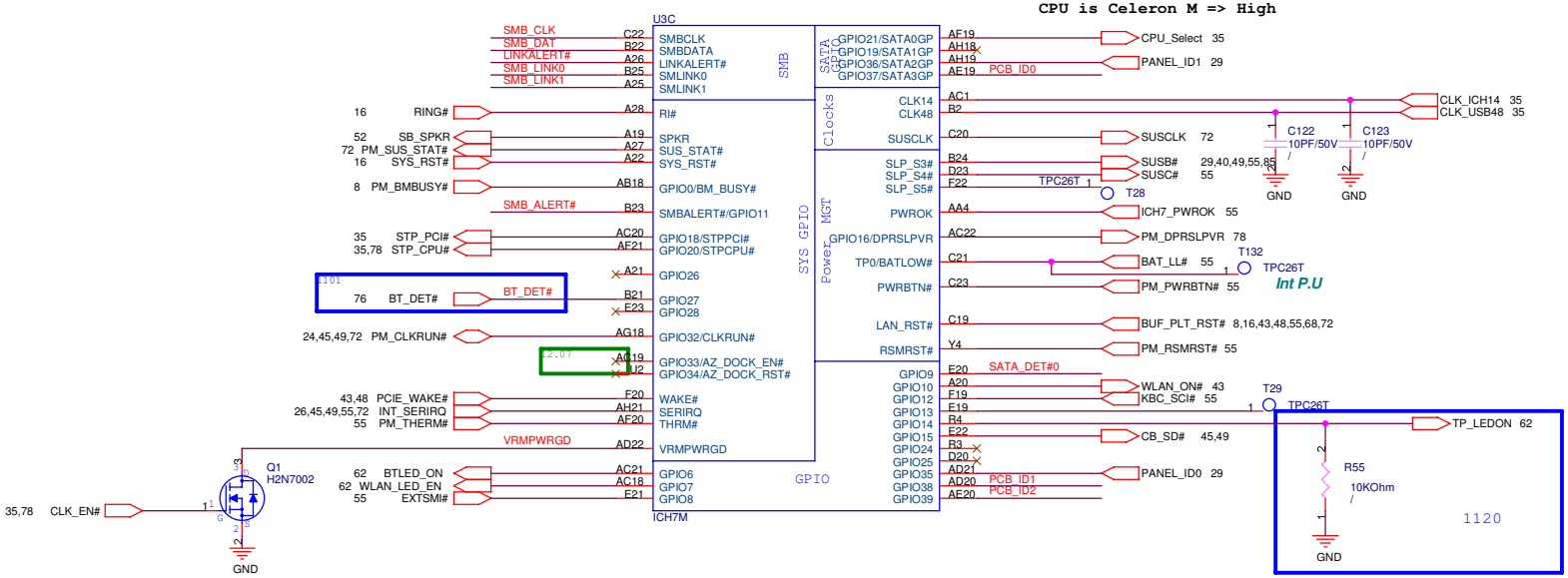
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 14 of 89

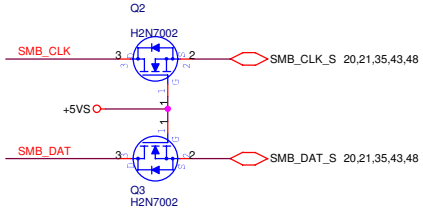


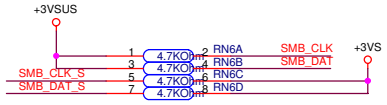
Title :	SB-ICH7-M(1)
ASUSTeK COMPUTER INC. NB1	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 15 of 89

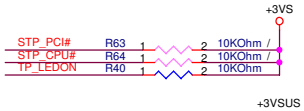

U3B
PCI
Interrupt I/F
MISC
ICH7M
24,40,45,49 PCI_AD[31:0]
PCI_AD0 PCI_AD1 PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 PCI_AD20 PCI_AD21 PCI_AD22 PCI_AD23 PCI_AD24 PCI_AD25 PCI_AD26 PCI_AD27 PCI_AD28 PCI_AD29 PCI_AD30 PCI_AD31
REQ0# REQ1# REQ2# REQ3# REQ4#/GPIO22 GNT0# GNT1# GNT2# GNT3# GNT4#/GPIO48 GPIO1/REQ5# GPIO17/GNT5#
PCI_REQ#1 PCI_REQ#2 PCI_REQ#3 PCI_REQ#4 PCI_REQ#5
PCI_REQ#0 45
PCI_GNT#0 45
PCI_REQ#1 49
PCI_GNT#1 49
PCI_REQ#2 40
PCI_GNT#2 40
PCI_REQ#3 24
PCI_GNT#3 24
PCI_GNT#4
PCI_GNT#5
ICH7 Boot BIOS Select
GNT#4 GNT#5
LPC H H
PCI H L
SPI L H
R58 1KOhm
R59 1KOhm
GND
C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C/BE#0 24,40,45,49
PCI_C/BE#1 24,40,45,49
PCI_C/BE#2 24,40,45,49
PCI_C/BE#3 24,40,45,49
IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PCI_IRDY# 24,40,45,49
PCI_PAR 24,40,45,49
PCI_RST# 24,40,45,49
PCI_DEVSEL# 24,40,45,49
PCI_PERR# 24,40,45,49
PCI_LOCK#
PCI_SERR# 24,40,45,49
PCI_STOP# 24,40,45,49
PCI_TRDY# 24,40,45,49
PCI_FRAME# 24,40,45,49
PLTRST# PCICLK PME#
PLT_RST#
CLK_ICHPCI 35
PCI_PME# 24,26,40,49
+3VS
U4
NC7SZ08P5X
Buffer to Reduce Loading on PLT_RST#
BUF_PLT_RST# 8,17,43,48,55,68,72
R60 4.7KOhm
ECN R2.1
PLT_RST# 26
45,49 PCI_INTA#
45,49 PCI_INTB#
40,49 PCI_INTC#
PCI_INTC# PCI_INTD#
PIRQA# PIRQB# PIRQC# PIRQD#
GPIO2/PIRQE# GPIO3/PIRQF# GPIO4/PIRQG# GPIO5/PIRQH#
PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#
PCI_INTG# 24
PCI_INTH# 24
RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5
RSVD_6 RSVD_7 RSVD_8 RSVD_9 MCH_SYNC#
MCH_ICH_SYNC# 8
CLK_ICHPCI
C117 10PF/50V
U3D
PCI-Express
Direct Media Interface
SPI
USB
PERn1 PERp1 PETn1 PETp1
PERn2 PERp2 PETn2 PETp2
PERn3 PERp3 PETn3 PETp3
PERn4 PERp4 PETn4 PETp4
PERn5 PERp5 PETn5 PETp5
PERn6 PERp6 PETn6 PETp6
43 PCIE_RXN2_MINICARD
43 PCIE_RXP2_MINICARD
43 PCIE_TXN2_MINICARD
43 PCIE_TXP2_MINICARD
C118 0.1UF/10V
C119 0.1UF/10V
48 PCIE_RXN3_NEWCARD
48 PCIE_RXP3_NEWCARD
48 PCIE_TXN3_NEWCARD
48 PCIE_TXP3_NEWCARD
C120 0.1UF/10V
C121 0.1UF/10V
DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI_RXN0 8
DMI_RXP0 8
DMI_TXN0 8
DMI_TXP0 8
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI_RXN1 8
DMI_RXP1 8
DMI_TXN1 8
DMI_TXP1 8
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI_RXN2 8
DMI_RXP2 8
DMI_TXN2 8
DMI_TXP2 8
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_RXN3 8
DMI_RXP3 8
DMI_TXN3 8
DMI_TXP3 8
DMI_CLKN DMI_CLKP
CLK_PCIE_ICH# 35
CLK_PCIE_ICH 35
DMI_ZCOMP DMI_IRCOMP
DMI_COMP
R61 24.9Ohm 1%
+1.5VS_PCIE_ICH
SPI_CLK SPI_CS# SPI_ARB SPI_MOSI SPI_MISO
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P
USB_PN0 58
USB_PP0 58
USB_PN1 58
USB_PP1 58
USB_PN2 58
USB_PP2 58
USB_PN3 58
USB_PP3 58
USBP4N
USBP4P
USBP5N
USBP5P
0Ohm R503
0Ohm R504
0Ohm R505
0Ohm R506
0Ohm R518
0Ohm R519
0Ohm R520
0Ohm R521
USB_PN4 76
USB_PP4 76
USB_PN4_2 24
USB_PP4_2 24
USB_PN5 43
USB_PP5 43
USB_PN5_2 74
USB_PP5_2 74
USB_PN6 48
USB_PP6 48
USB_PN7 29
USB_PP7 29
USBRBIAS/#
R62 22.6Ohm 1%
USBRBIAS# USBRBIAS
GND
Layout Notice!!
R503,R504,R505,R506,R518,R519,R520,R521
must near ICH7 less than 200mil
Use Bluetooth mount R503,R504
Use Mini PCI Card mount R505,R506
Use Mini Card mount R518,R519
Use Finger Print mount R520,R521
T23 T24 T25 T26 T27
SPI_CLK SPI_CS# SPI_ARB SPI_MOSI SPI_MISO
58 USB_CON_OC01#
58 USB_CON_OC23#
48 NEWCARD_OC#
OC0# OC1# OC2# OC3# OC4# OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31
USB_OC#4 USB_OC#5 USB_OC#7
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth Or Mini PCI Card
USB 5 Mini Card Or Finger Print
USB 6 Newcard
USB 7 CMOS Camera
+3VSUS
10KOhm RN4A RN4B RN4C RN4D
USB_CON_OC23# USB_OC#4 USB_OC#5 USB_CON_OC01#
RN5A RN5B RN5C RN5D
SYS_RST# 17
RING# 17
USB_OC#7 NEWCARD_OC#
+3VS
PCI_INTB# RP1A
PCI_DEVSEL# RP1B
PCI_REQ#4 RP1C
PCI_LOCK# RP1D
PCI_INTE# RP1E
PCI_INTH# RP1F
PCI_SERR# RP1G
PCI_PERR# RP1H
PCI_INTD# RP2A
PCI_INTC# RP2B
PCI_INTF# RP2C
PCI_INTA# RP2D
PCI_REQ#5 RP2E
PCI_REQ#0 RP2F
PCI_INTG# RP2G
PCI_IRDY# RP2H
PCI_FRAME# RP3A
PCI_REQ#3 RP3B
PCI_REQ#1 RP3C
PCI_REQ#2 RP3D
PCI_TRDY# RP3E
PCI_STOP# RP3F
RP3G
RP3H
8.2KOhm
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Wang
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
Sheet 16 of 89

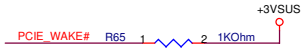
CPU_Select :
CPU is Pentem M => Low
CPU is Celeron M => High

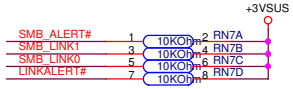


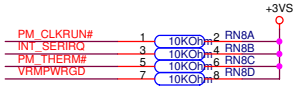


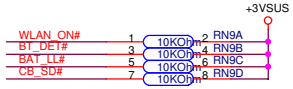


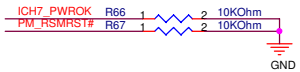


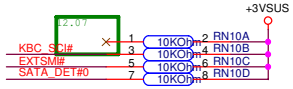


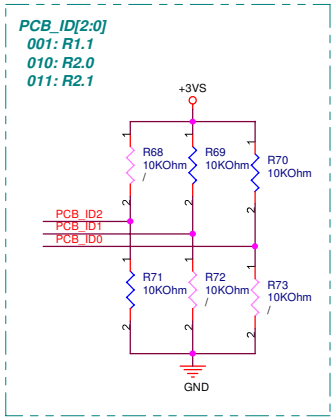




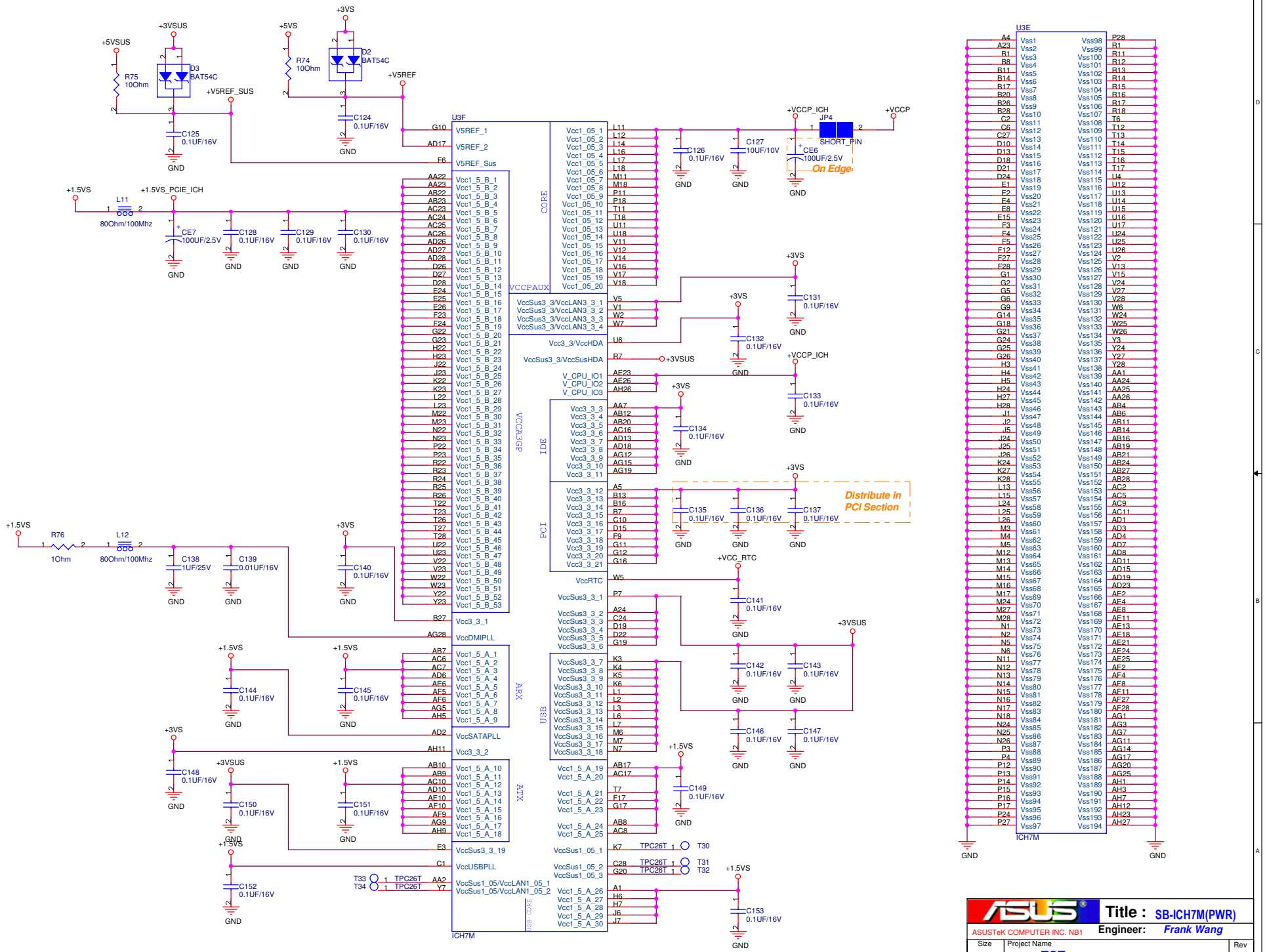






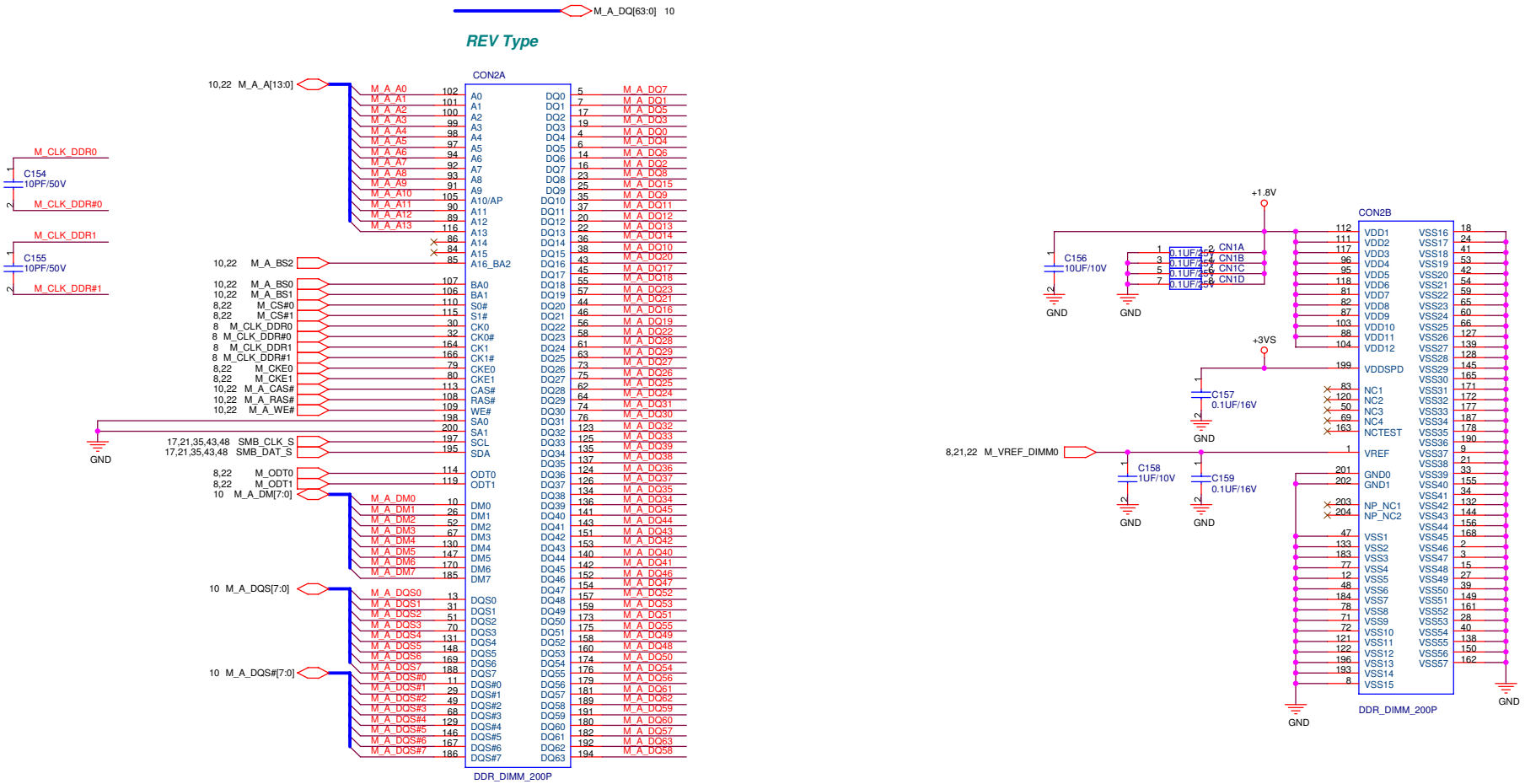


ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(3)	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 17 of 89	



ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(PWR)		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 18 of 89		

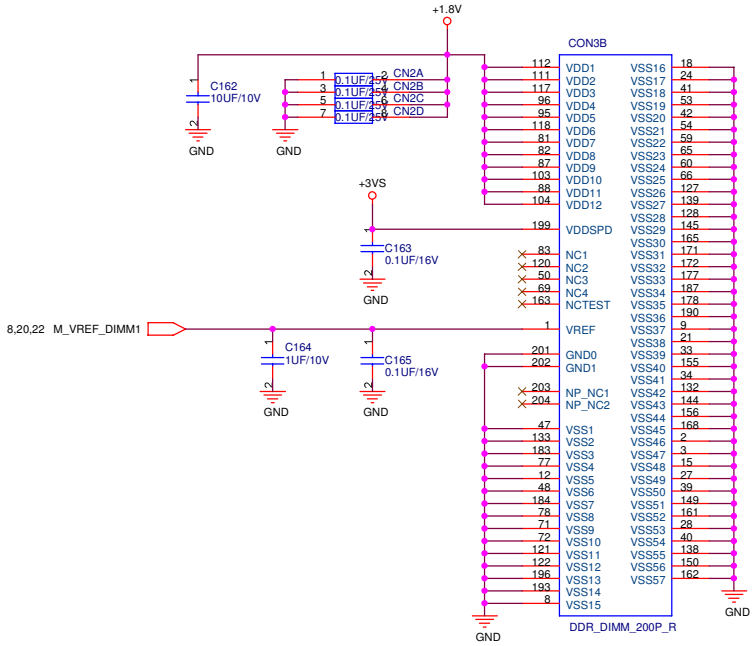
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 19 of 89



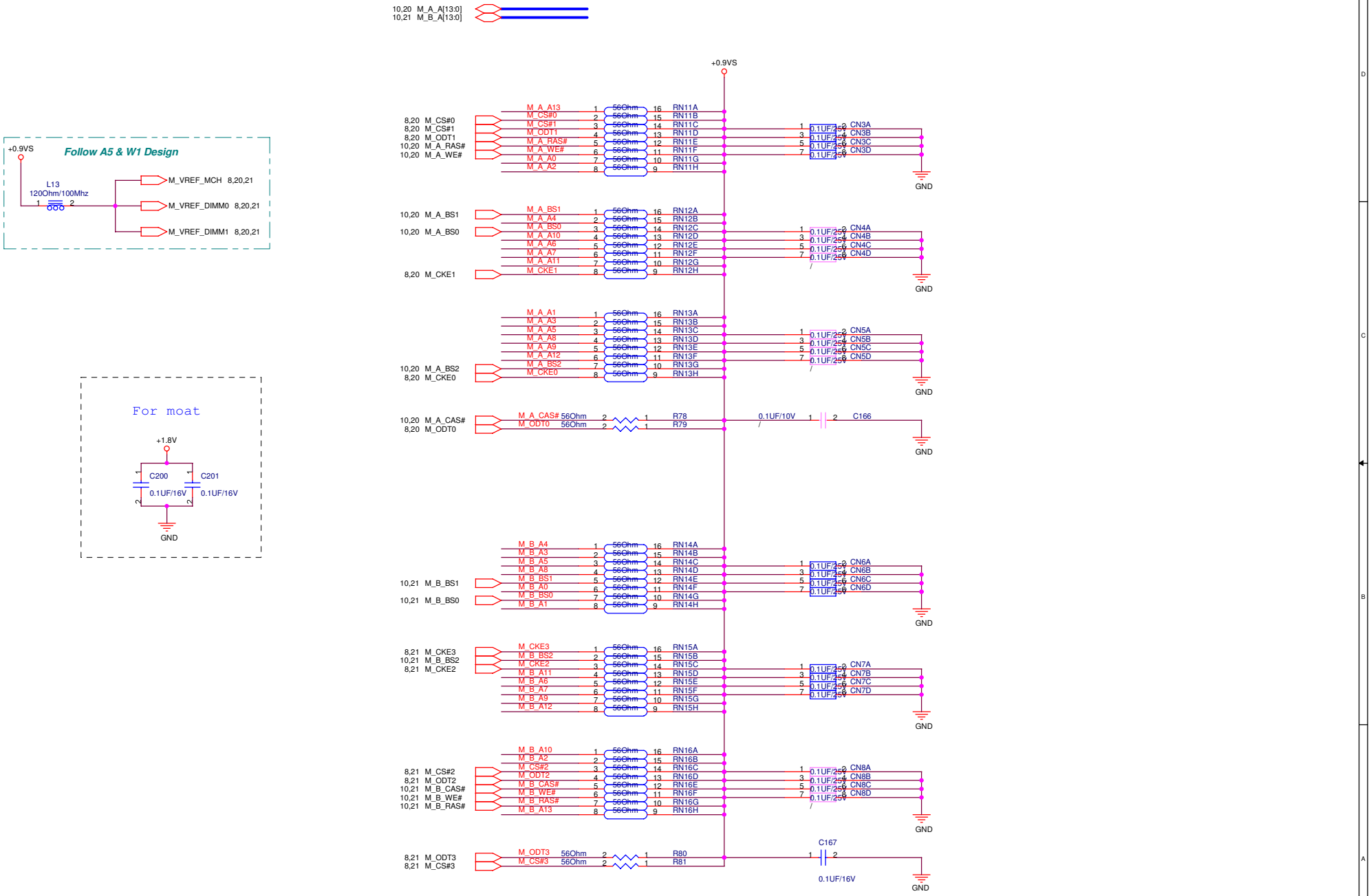
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 20 of 89	

M_B_DQ[63:0] 10

STD Type

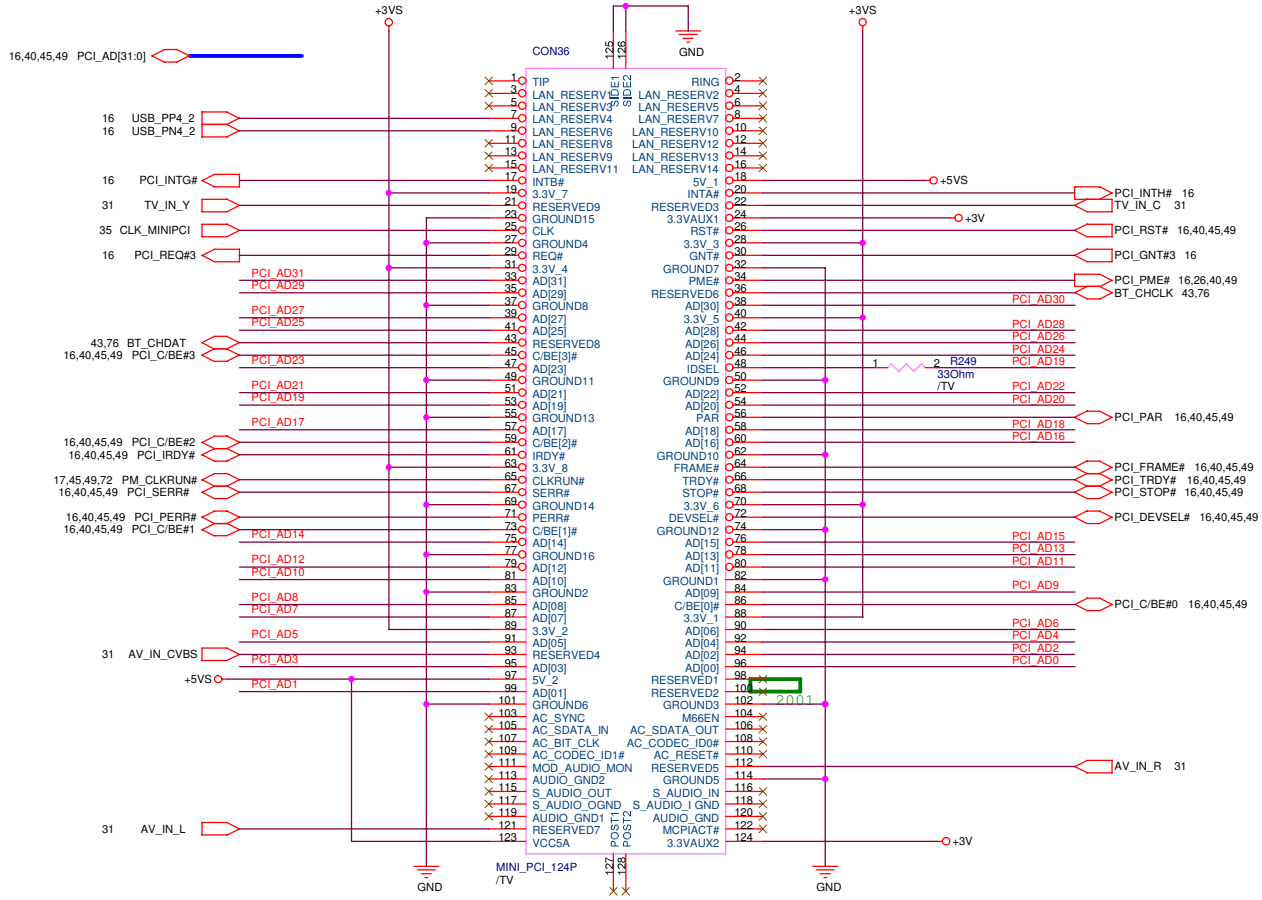


ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 21 of 89		



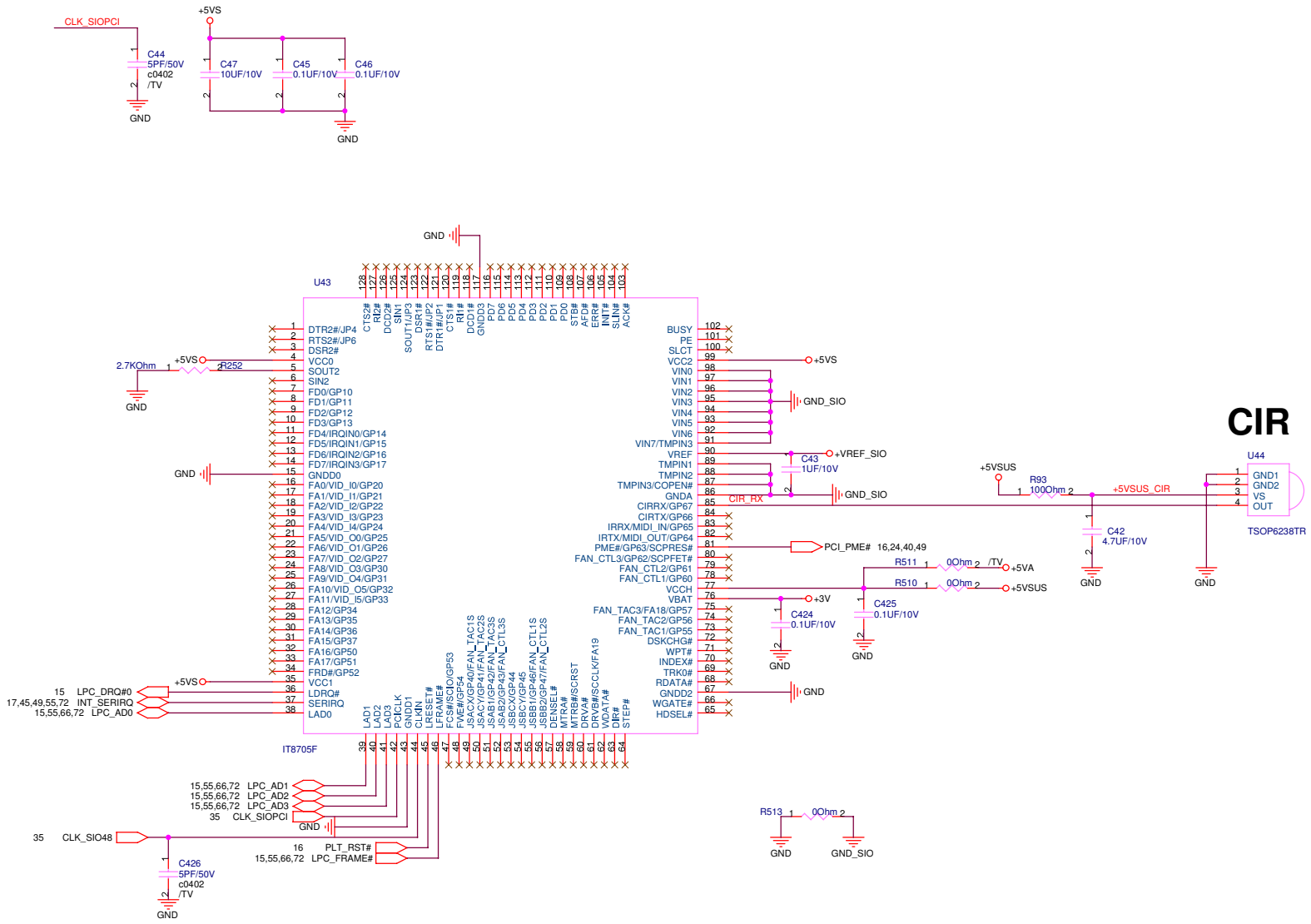
ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 22 of 89	

ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 23 of 89	



ASUSTek COMPUTER INC	Title : MINI PCI CARD	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 24 of 89	

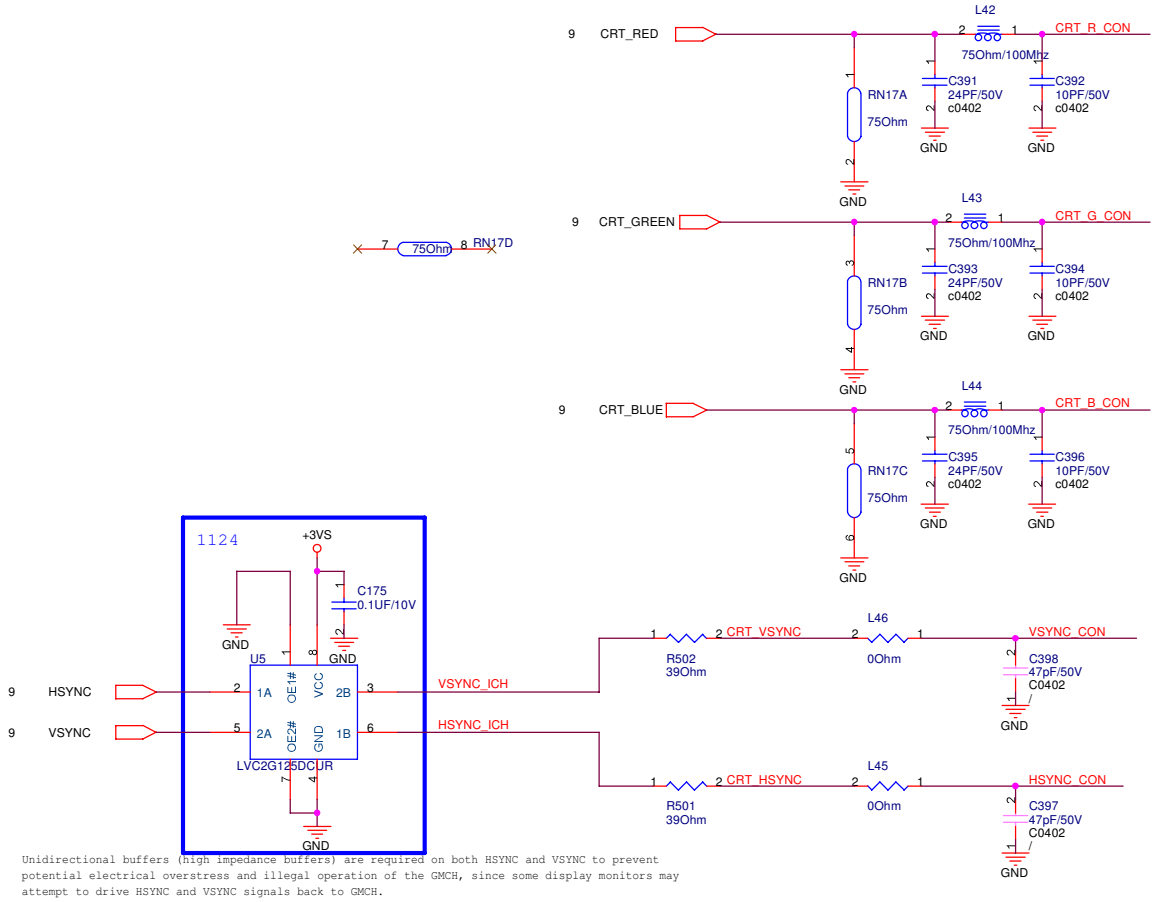
ASUSTek COMPUTER INC	Title: Schematic page name	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 25 of 89	



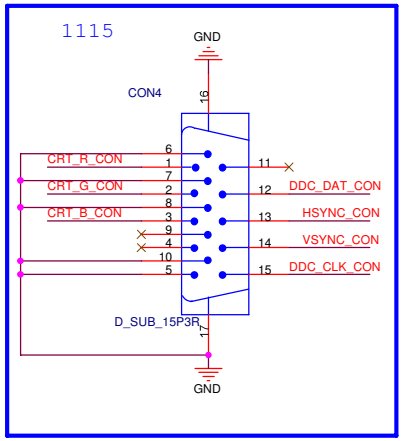
ASUSTeK COMPUTER INC	Title : SIO ITE8705F		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 26 of 89		

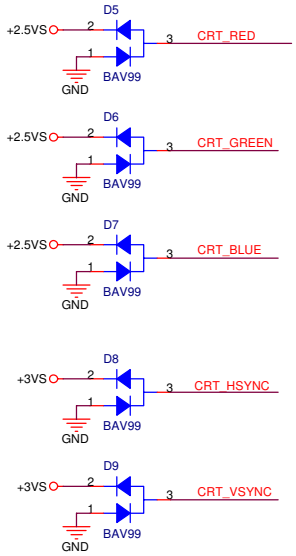
Title :	Schematic page name
ASUSTek COMPUTER INC	Engineer: Frank Wang
Size: C	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 27 of 89

阻抗37.5Ohm <== ==> 阻抗75Ohm OR W= 4 mil

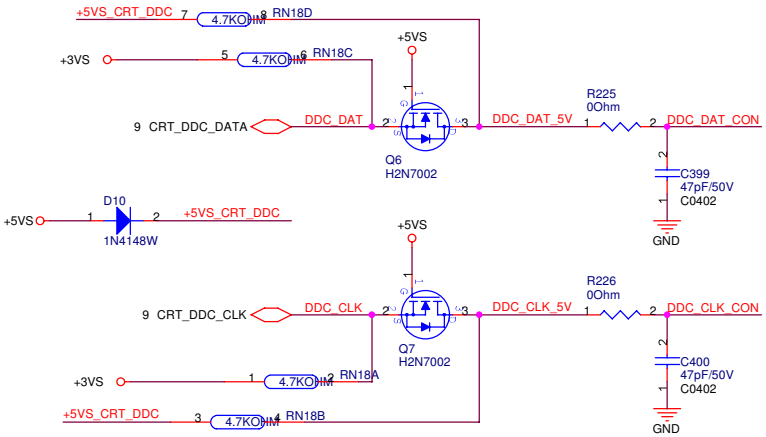


Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.





PLACE ESD Diodes near VGA port

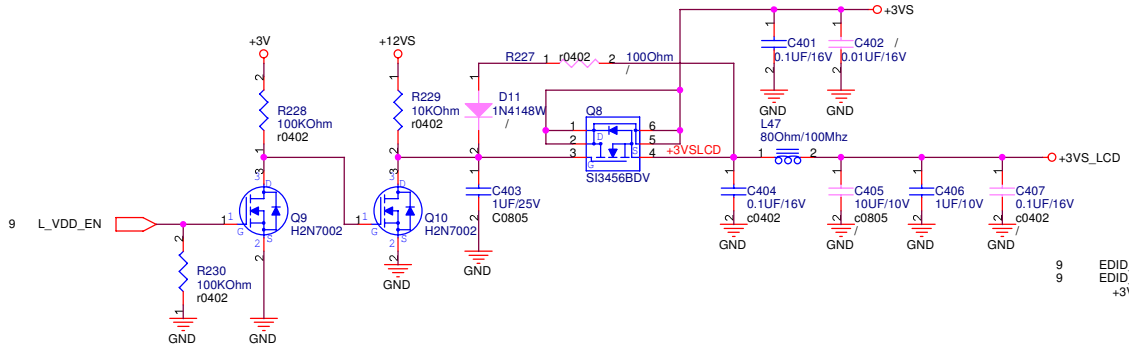


ASUSTeK COMPUTER INC	Title : CRT		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 28 of 89		

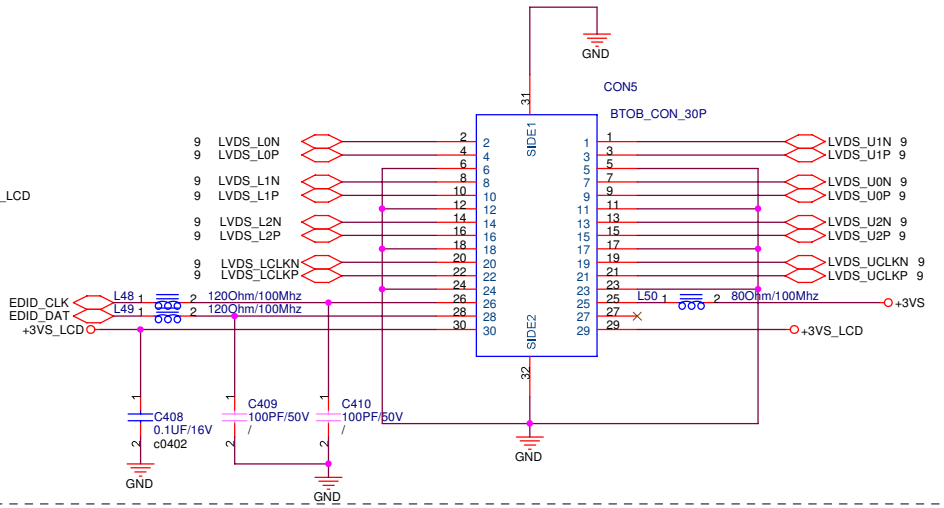
LCD Backlight Control

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Power



LCD LVDS Interface

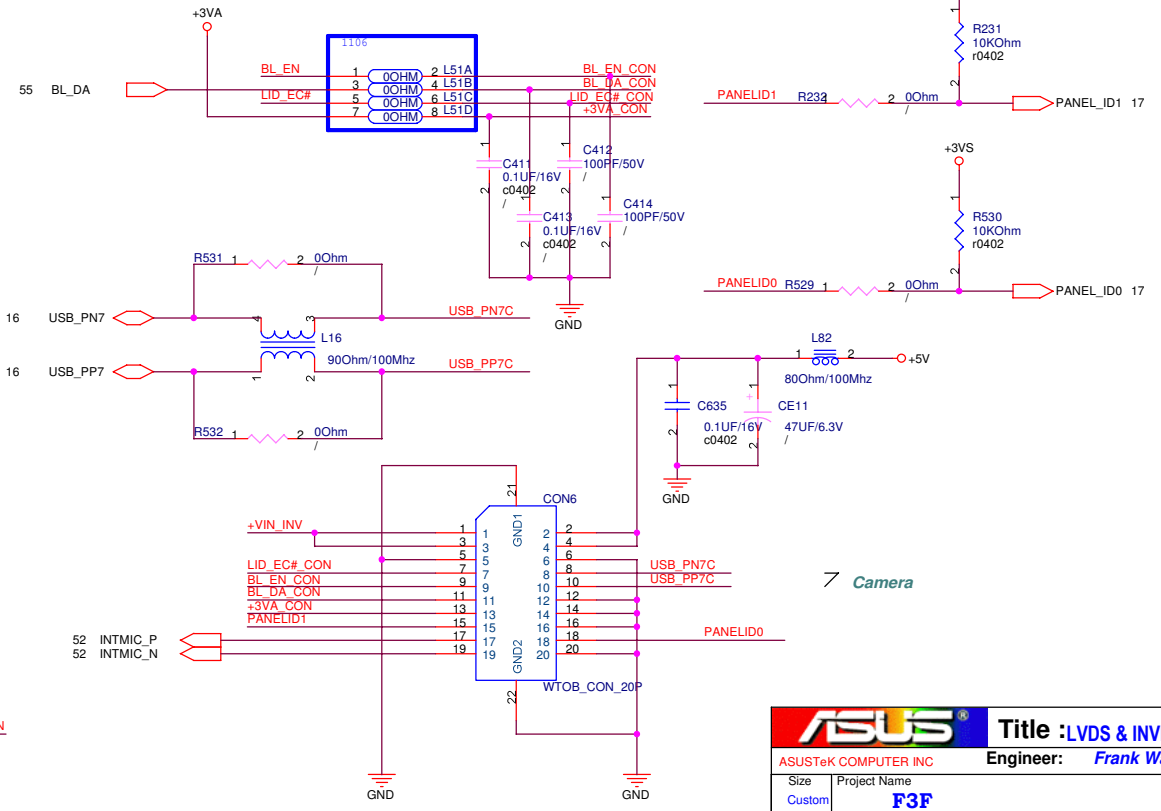


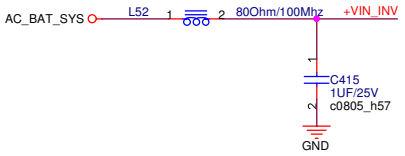
INVERTER
Interface/Speaker
CONN.

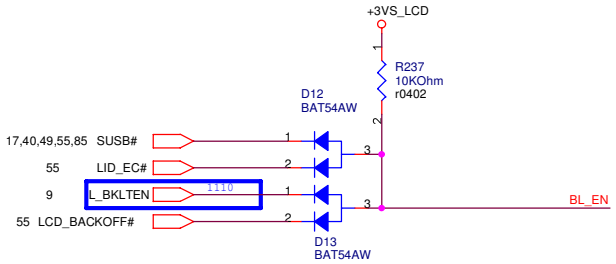
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR







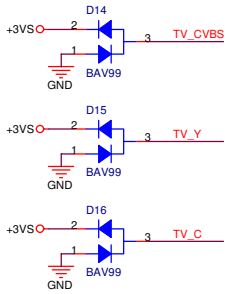
Camera

ASUSTeK COMPUTER INC	Engineer: *Frank Wang*	
Size: Custom	Project Name: **F3F**	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 29 of 89	

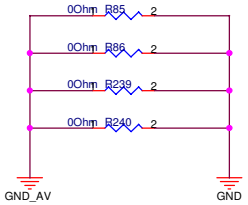
Title : LVDS & INVERTER

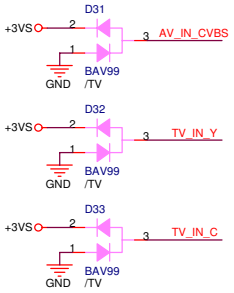
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 30 of 89

TV OUT

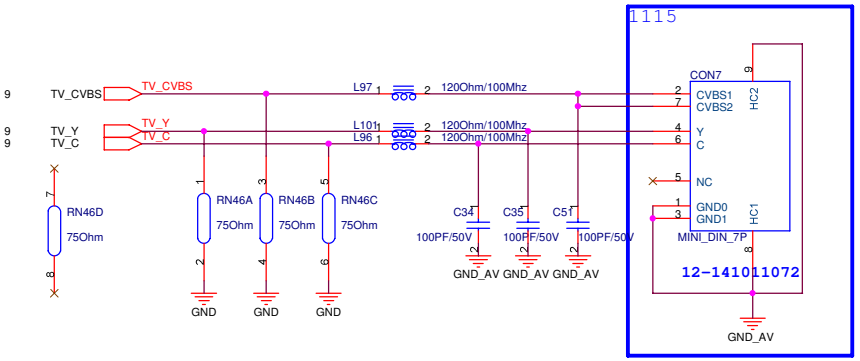


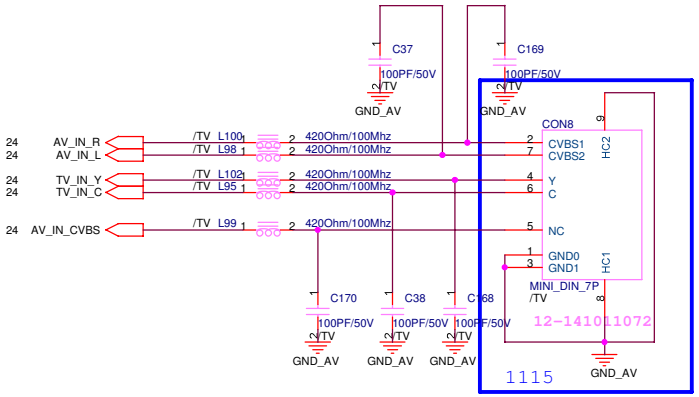
PLACE ESD
Diodes near
TV port

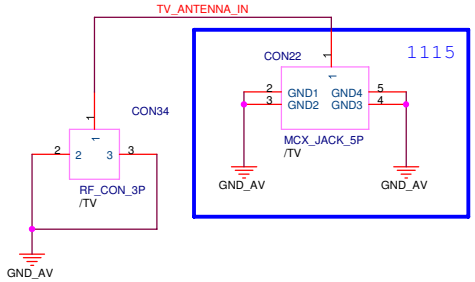




PLACE ESD
Diodes near
AV_IN port



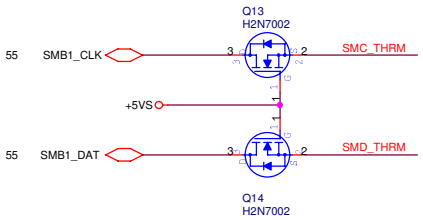


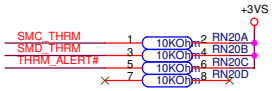


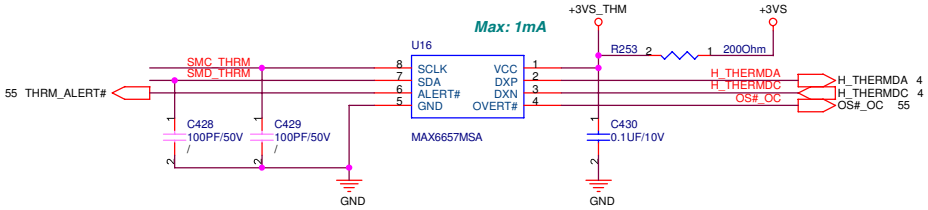
ASUSTeK COMPUTER INC	Title : TV OUT & AV_IN	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 31 of 89	

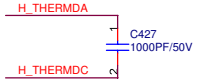
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 32 of 89

Thermal Sensor









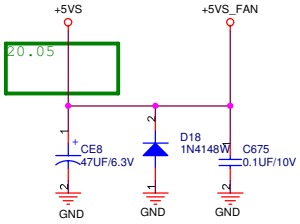
Route H_THERMDA and H_THERMDC on the same layer

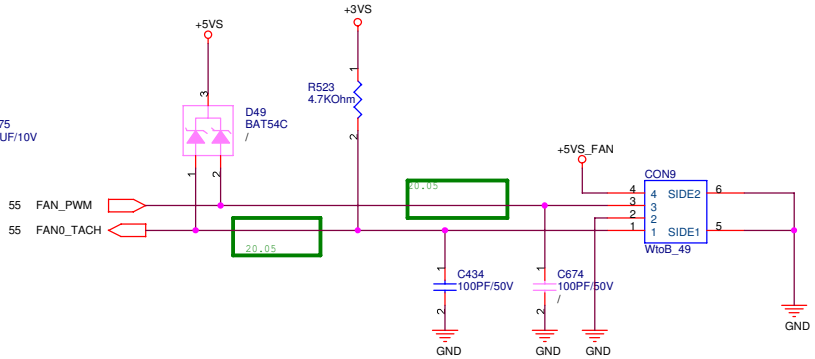
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

1108

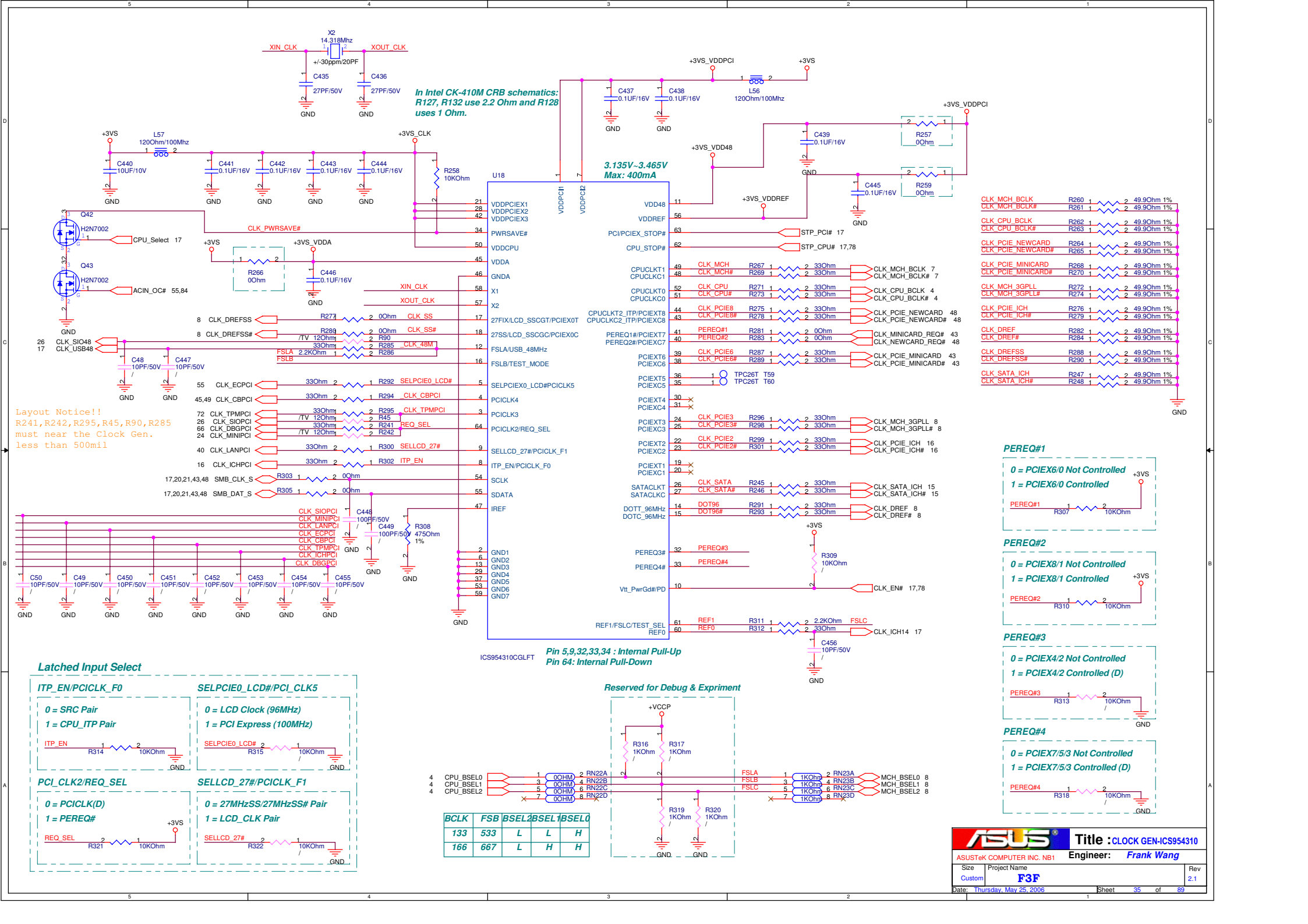
DC FAN Control



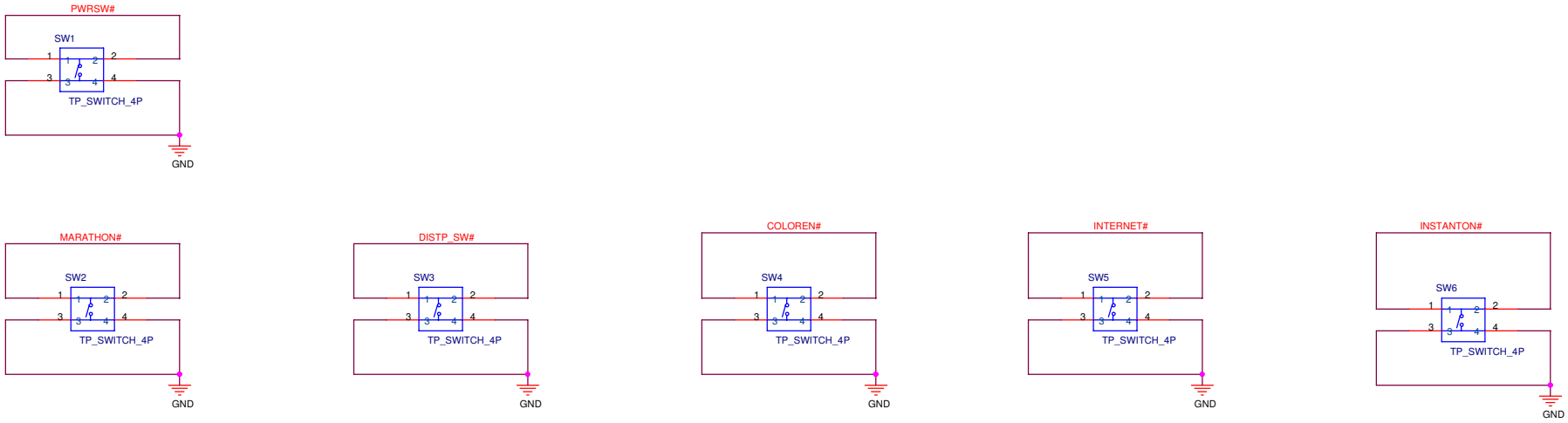


ASUSTeK COMPUTER INC. NB1	Title : THER SENSOR & FAN	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 33 of 89	

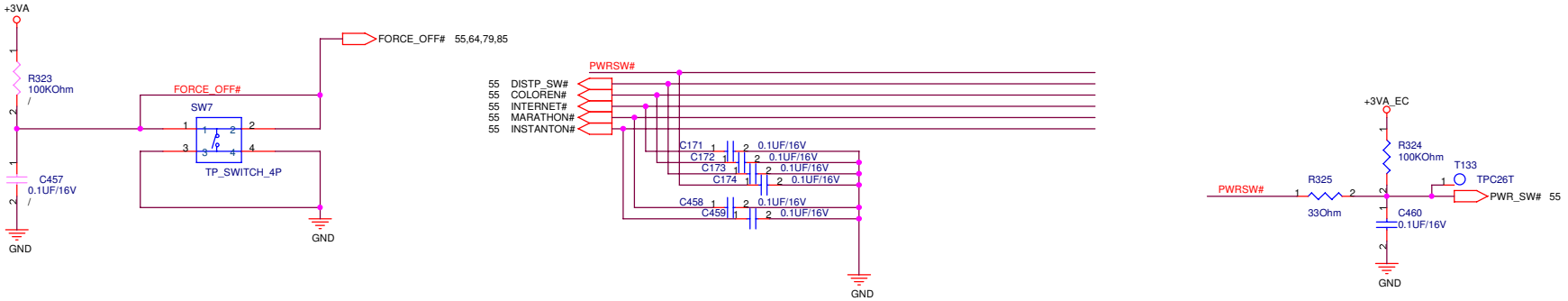
ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 34 of 89	


X2
14.318Mhz
XIN_CLK
XOUT_CLK
+/-30ppm/20PF
C435
27PF/50V
C436
27PF/50V
GND
In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128
uses 1 Ohm.
+3VS_VDDPCI
+3VS
L56
120Ohm/100Mhz
C437
0.1UF/16V
C438
0.1UF/16V
+3VS
L57
120Ohm/100Mhz
+3VS_CLK
C440
10UF/10V
C441
0.1UF/16V
C442
0.1UF/16V
C443
0.1UF/16V
C444
0.1UF/16V
R258
10KOhm
U18
3.135V~3.465V
Max: 400mA
+3VS_VDD48
C439
0.1UF/16V
R257
0Ohm
R259
0Ohm
C445
0.1UF/16V
+3VS_VDDREF
Q42
H2N7002
CPU_Select 17
CLK_PWRSAVE#
Q43
H2N7002
ACIN_OC# 55,84
+3VS
R266
0Ohm
+3VS_VDDA
C446
0.1UF/16V
XIN_CLK
XOUT_CLK
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIEX0T
27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz
FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5
PCICLK4
PCICLK3
PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1
ITP_EN/PCICLK_F0
SCLK
SDATA
IREF
GND1
GND2
GND3
GND4
GND5
GND6
GND7
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
CPUCLKT1
CPUCLKC1
CPUCLKT0
CPUCLKC0
CPUCLKT2_ITP/PCIEXT8
CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7
PEREQ2#/PCIEXC7
PCIEXT6
PCIEXC6
PCIEXT5
PCIEXC5
PCIEXT4
PCIEXC4
PCIEXT3
PCIEXC3
PCIEXT2
PCIEXC2
PCIEXT1
PCIEXC1
SATACLKT
SATACLKC
DOTT_96MHz
DOTC_96MHz
PEREQ3#
PEREQ4#
Vtt_PwrGd#/PD
REF1/FSLC/TEST_SEL
REF0
STP_PCI# 17
STP_CPU# 17,78
CLK_MCH 33Ohm
CLK_MCH# 33Ohm
CLK_CPU 33Ohm
CLK_CPU# 33Ohm
CLK_PCIE8 33Ohm
CLK_PCIE8# 33Ohm
PEREQ#1 0Ohm
PEREQ#2 0Ohm
CLK_PCIE6 33Ohm
CLK_PCIE6# 33Ohm
TPC26T T59
TPC26T T60
CLK_PCIE3 33Ohm
CLK_PCIE3# 33Ohm
CLK_PCIE2 33Ohm
CLK_PCIE2# 33Ohm
CLK_SATA 33Ohm
CLK_SATA# 33Ohm
DOT96 33Ohm
DOT96# 33Ohm
PEREQ#3
PEREQ#4
CLK_EN# 17,78
REF1 2.2KOhm FSLC
REF0 33Ohm
CLK_ICH14 17
C456
10PF/50V
ICS954310CGLFT
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down
CLK_MCH_BCLK R260 49.9Ohm 1%
CLK_MCH_BCLK# R261 49.9Ohm 1%
CLK_CPU_BCLK R262 49.9Ohm 1%
CLK_CPU_BCLK# R263 49.9Ohm 1%
CLK_PCIE_NEWCARD R264 49.9Ohm 1%
CLK_PCIE_NEWCARD# R265 49.9Ohm 1%
CLK_PCIE_MINICARD R268 49.9Ohm 1%
CLK_PCIE_MINICARD# R270 49.9Ohm 1%
CLK_MCH_3GPLL R272 49.9Ohm 1%
CLK_MCH_3GPLL# R274 49.9Ohm 1%
CLK_PCIE_ICH R276 49.9Ohm 1%
CLK_PCIE_ICH# R279 49.9Ohm 1%
CLK_DREF R282 49.9Ohm 1%
CLK_DREF# R284 49.9Ohm 1%
CLK_DREFSS R288 49.9Ohm 1%
CLK_DREFSS# R290 49.9Ohm 1%
CLK_SATA_ICH R247 49.9Ohm 1%
CLK_SATA_ICH# R248 49.9Ohm 1%
CLK_DREFSS 8
CLK_DREFSS# 8
R277 0Ohm CLK_SS
R280 0Ohm CLK_SS#
/TV 12Ohm R90
33Ohm R285 CLK_48M
FSLA 2.2KOhm R286
FSLB
CLK_SIO48 26
CLK_USB48 17
C48 10PF/50V
C447 10PF/50V
CLK_ECPCI 55
CLK_CBPCI 45,49
CLK_TPMPCI 72
CLK_SIOPCI 26
CLK_DBGPCI 66
CLK_MINIPCI 24
CLK_LANPCI 40
CLK_ICHPCI 16
33Ohm R292 SELPCIE0_LCD#
33Ohm R294 CLK_CBPCI
33Ohm R295 CLK_TPMPCI
/TV 12Ohm R45
33Ohm R241 REQ_SEL
/TV 12Ohm R242
33Ohm R300 SELLCD_27#
33Ohm R302 ITP_EN
SMB_CLK_S 17,20,21,43,48
SMB_DAT_S 17,20,21,43,48
R303 0Ohm
R305 0Ohm
C448 100PF/50V
C449 100PF/50V
R308 475Ohm 1%
C50 10PF/50V
C49 10PF/50V
C450 10PF/50V
C451 10PF/50V
C452 10PF/50V
C453 10PF/50V
C454 10PF/50V
C455 10PF/50V
Layout Notice!!
R241,R242,R295,R45,R90,R285
must near the Clock Gen.
less than 500mil
R309
10KOhm
PEREQ#1
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
R307 10KOhm
PEREQ#2
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
R310 10KOhm
PEREQ#3
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
R313 10KOhm
PEREQ#4
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
R318 10KOhm
Latched Input Select
ITP_EN/PCICLK_F0
0 = SRC Pair
1 = CPU_ITP Pair
ITP_EN R314 10KOhm
SELPCIE0_LCD#/PCI_CLK5
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)
SELPCIE0_LCD# R315 10KOhm
PCI_CLK2/REQ_SEL
0 = PCICLK(D)
1 = PEREQ#
REQ_SEL R321 10KOhm
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
SELLCD_27# R322 10KOhm
Reserved for Debug & Expriment
+VCCP
R316 1KOhm
R317 1KOhm
R319 1KOhm
R320 1KOhm
CPU_BSEL0 4
CPU_BSEL1 4
CPU_BSEL2 4
0OHM RN22A
0OHM RN22B
0OHM RN22C
0OHM RN22D
FSLA
FSLB
FSLC
1KOhm RN23A
1KOhm RN23B
1KOhm RN23C
1KOhm RN23D
MCH_BSEL0 8
MCH_BSEL1 8
MCH_BSEL2 8
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN-ICS954310
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Wang
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
Sheet 35 of 89

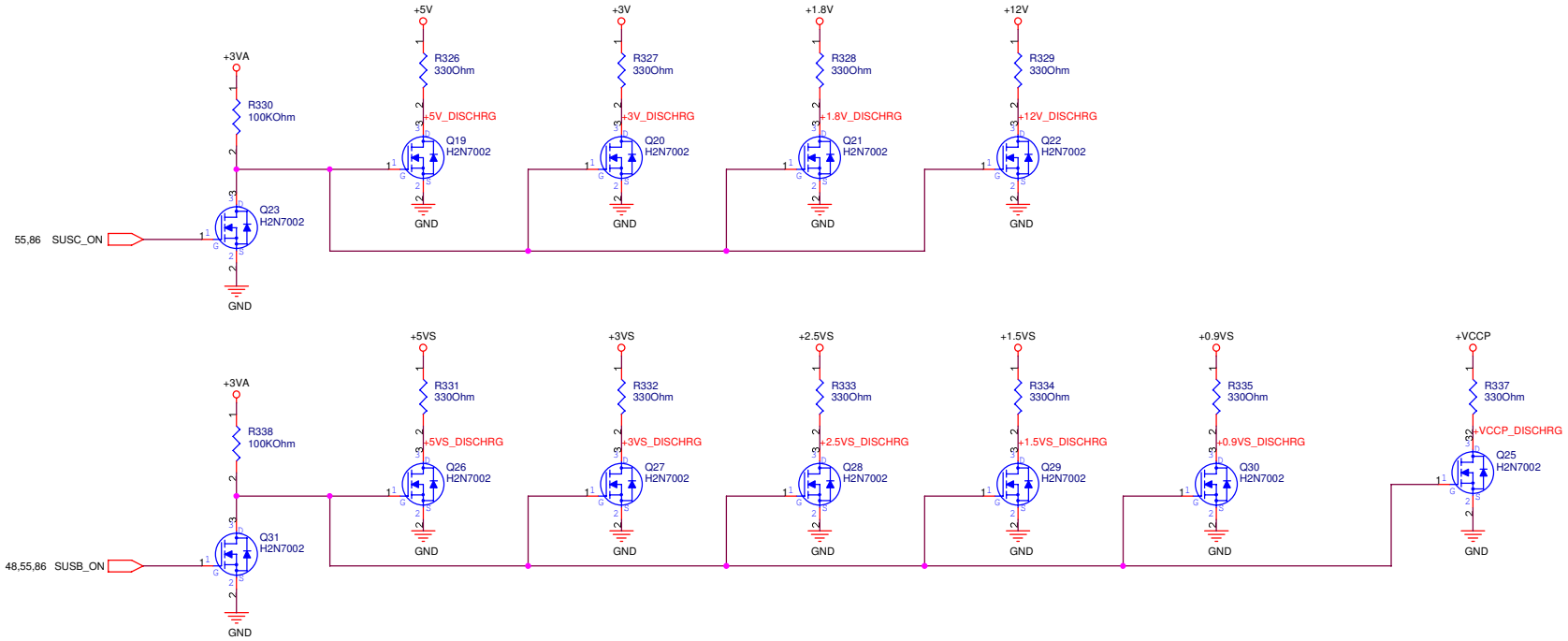
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 36 of 89



SHUT_DOWN#

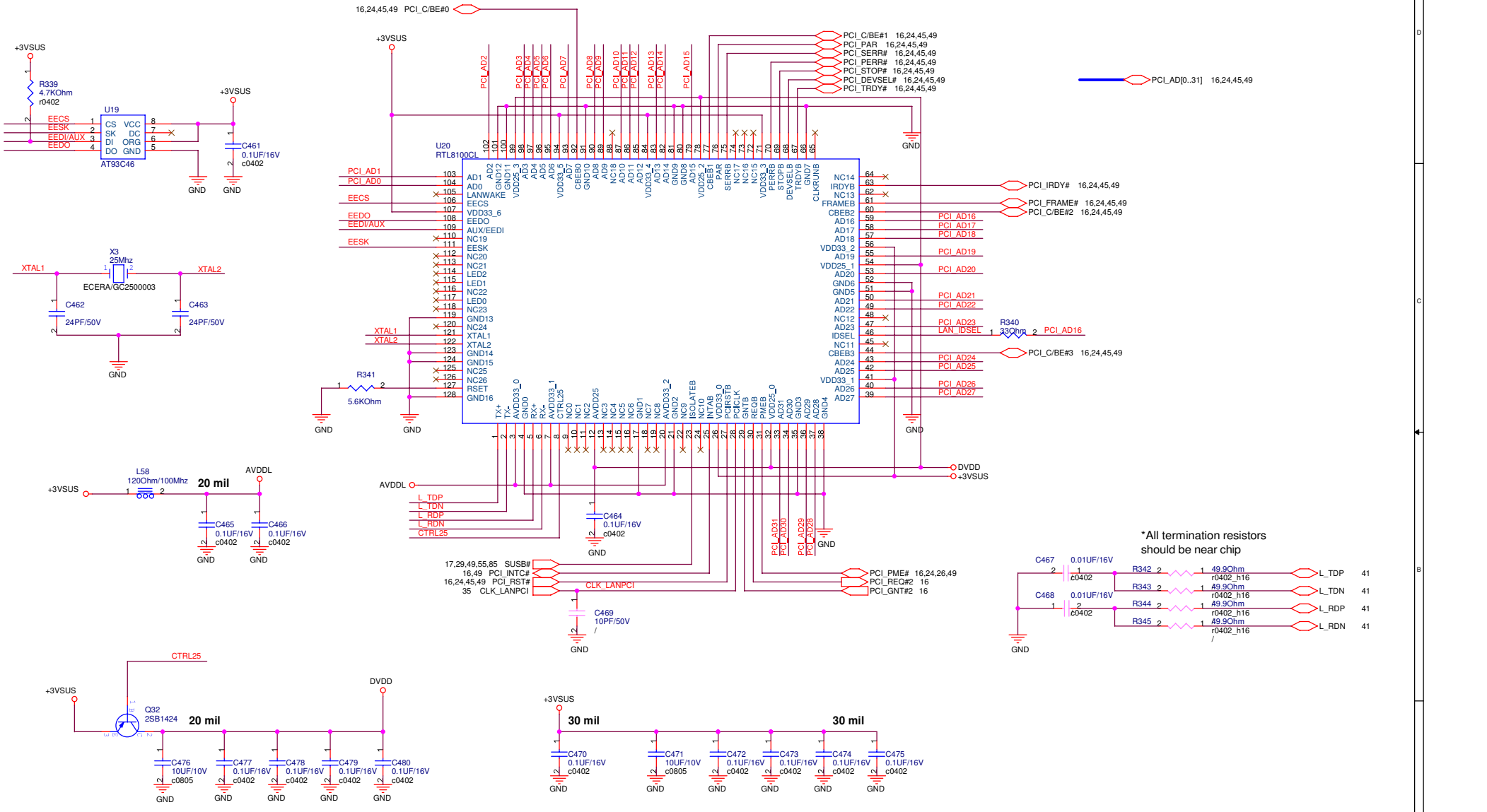


ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 37 of 89	



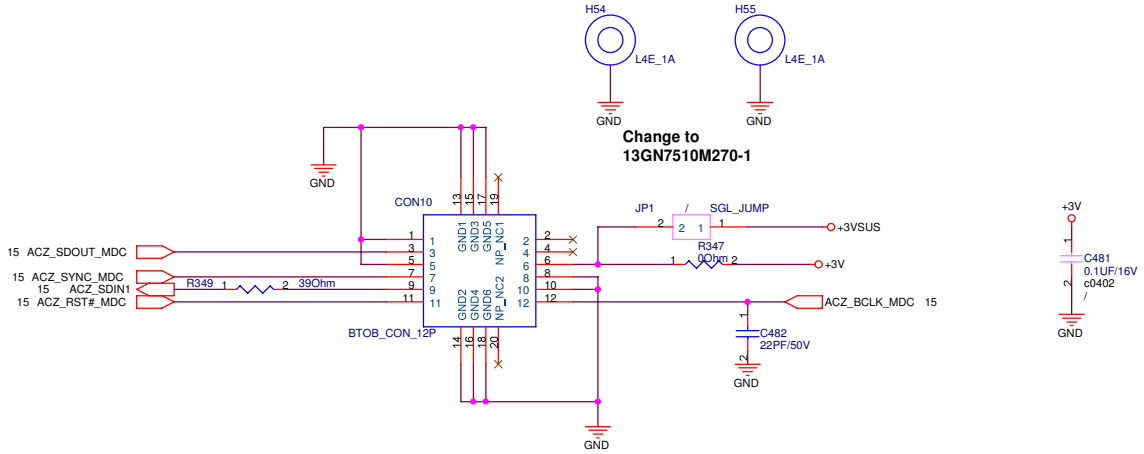
ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 38 of 89	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 39 of 89

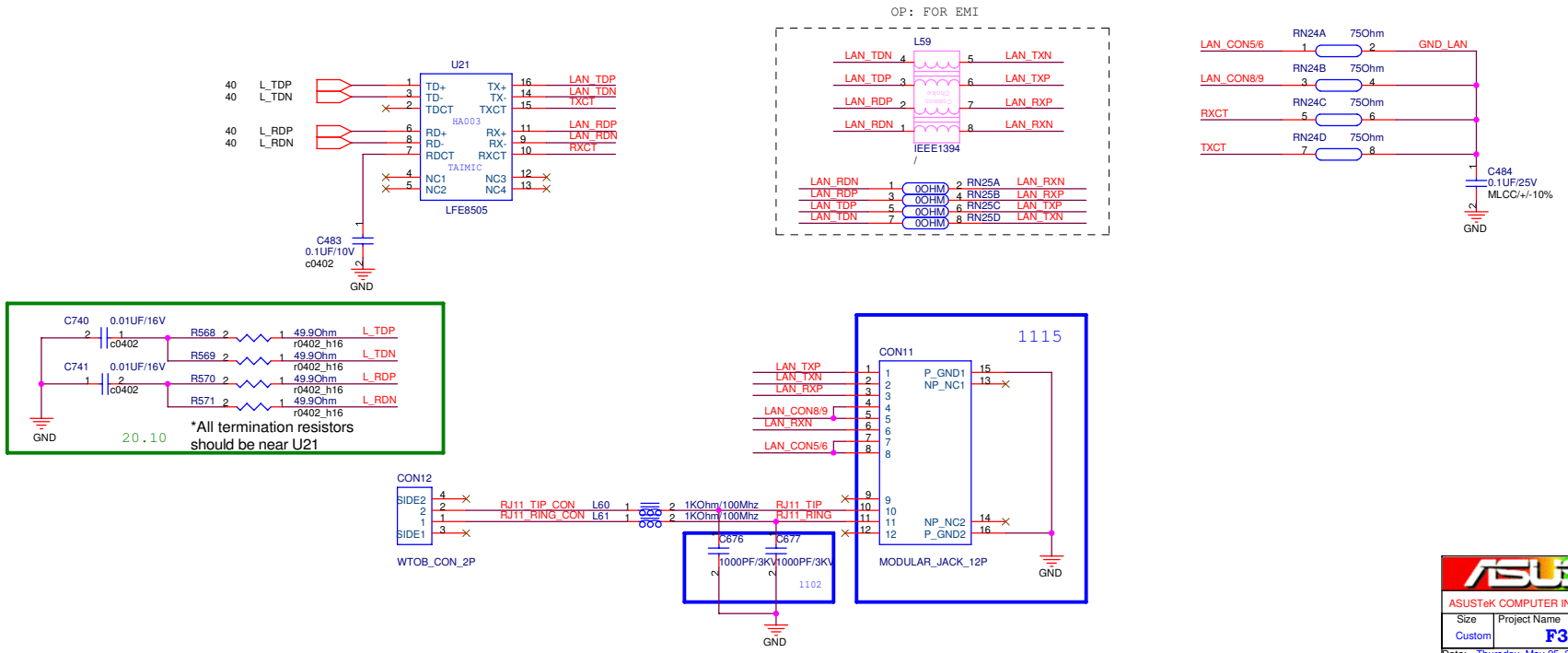


ASUSTeK COMPUTER INC. NB1	Title : LAN-RTL8100CL		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 40 of 89		

MDC CONN.

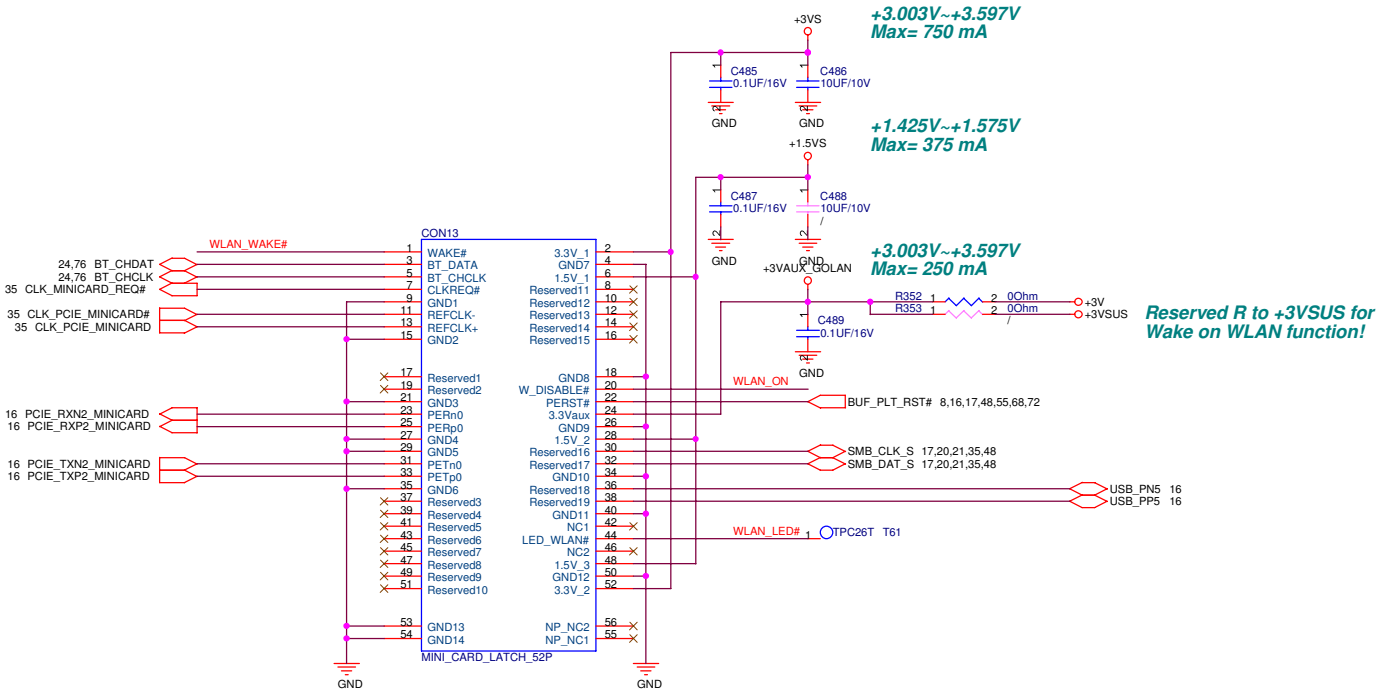


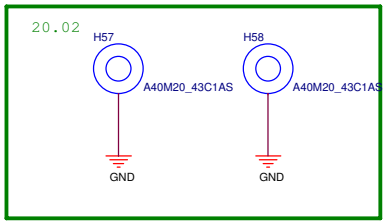
LAN CONN.

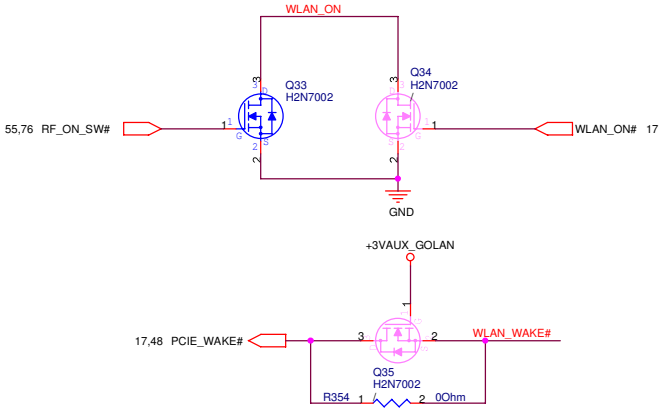


ASUSTeK COMPUTER INC. NB1	Title : MDC & RJ45+11		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 41 of 89		

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 42 of 89

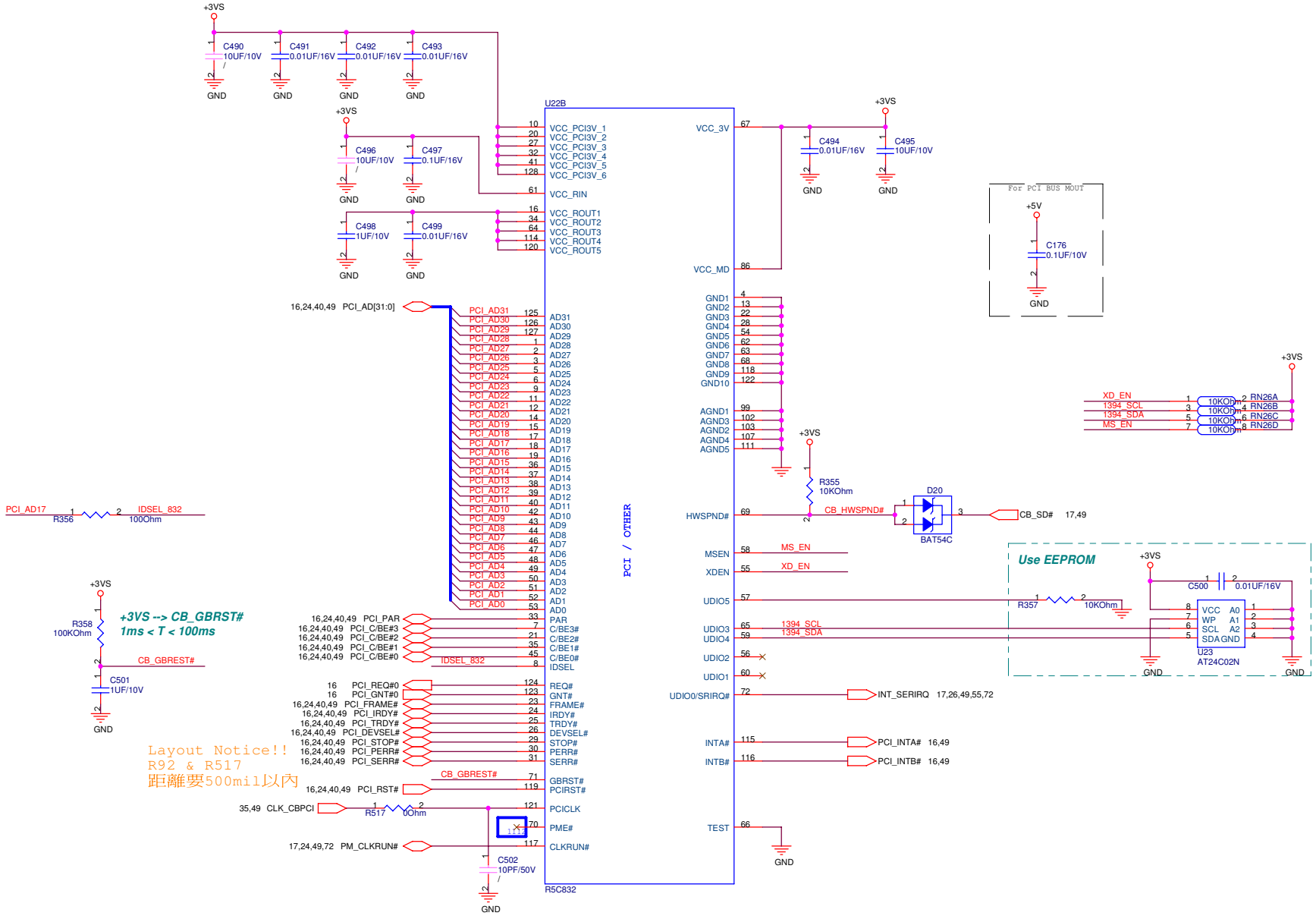




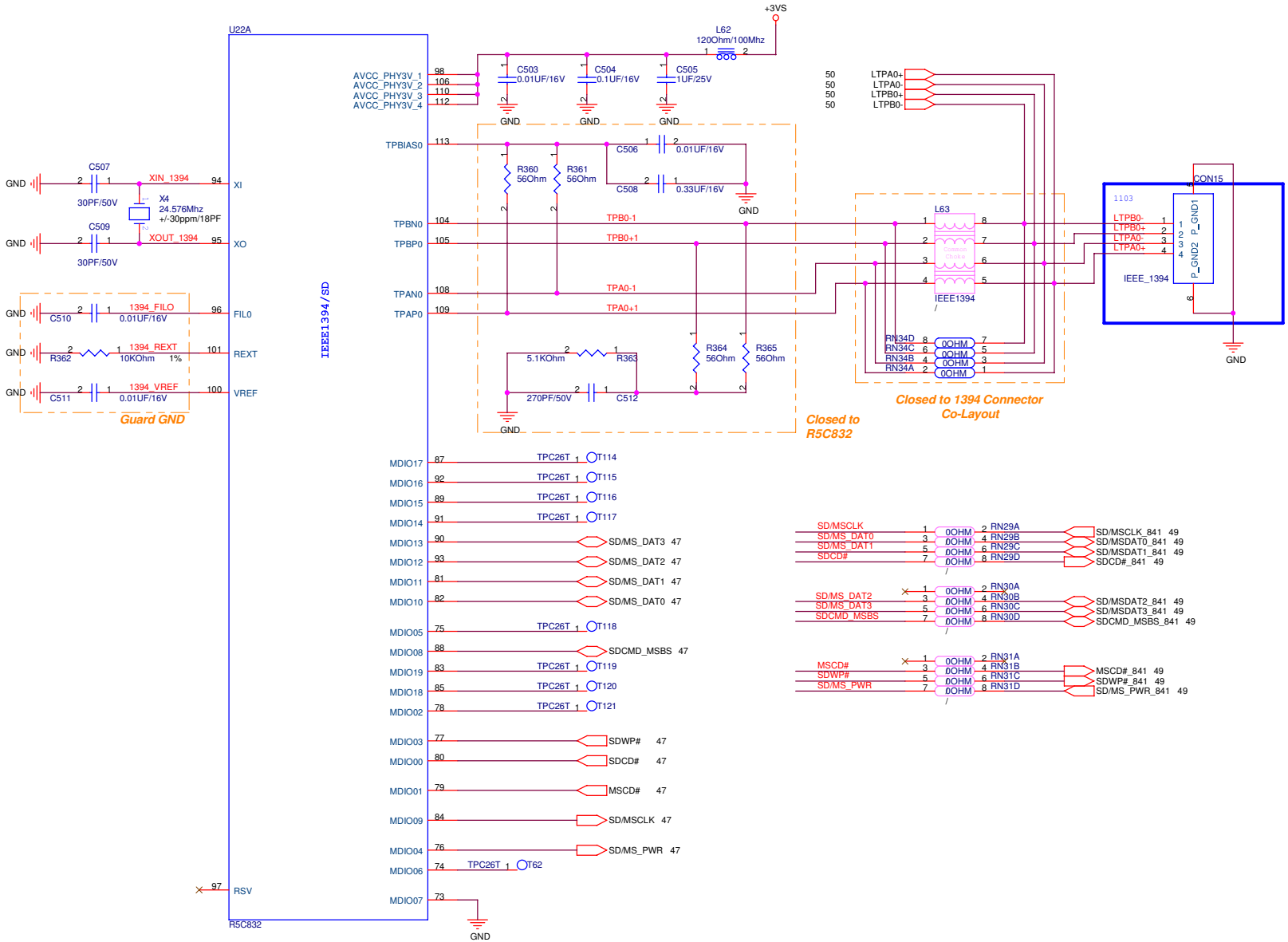


ASUSTeK COMPUTER INC. NB1	Title : MINICARD	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 43 of 89	

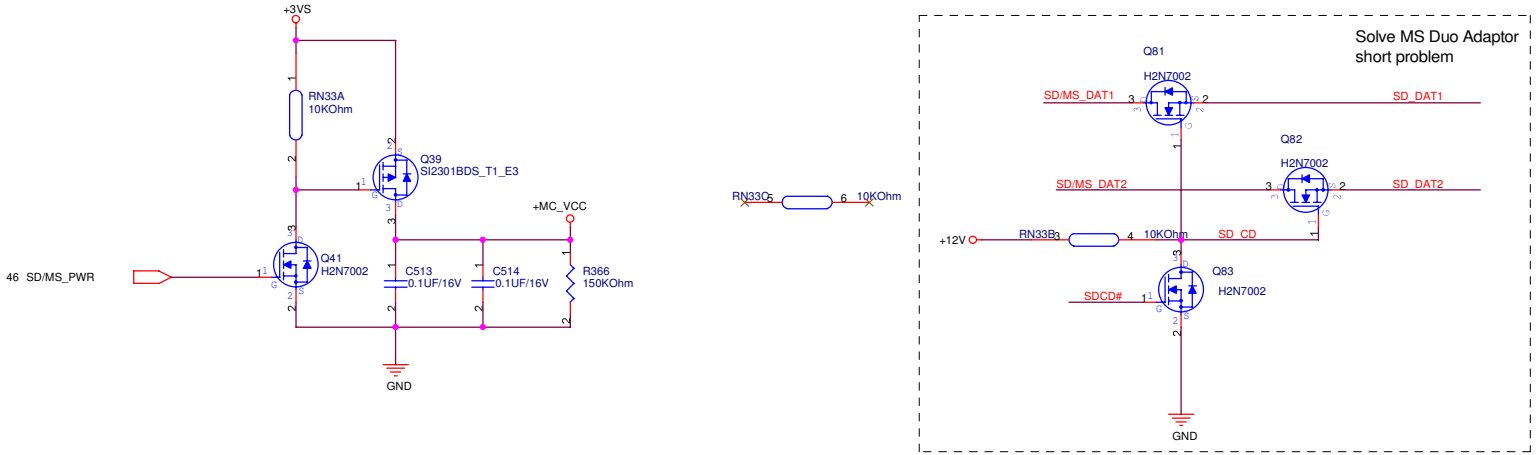
ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: **F3F**	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 44 of 89	

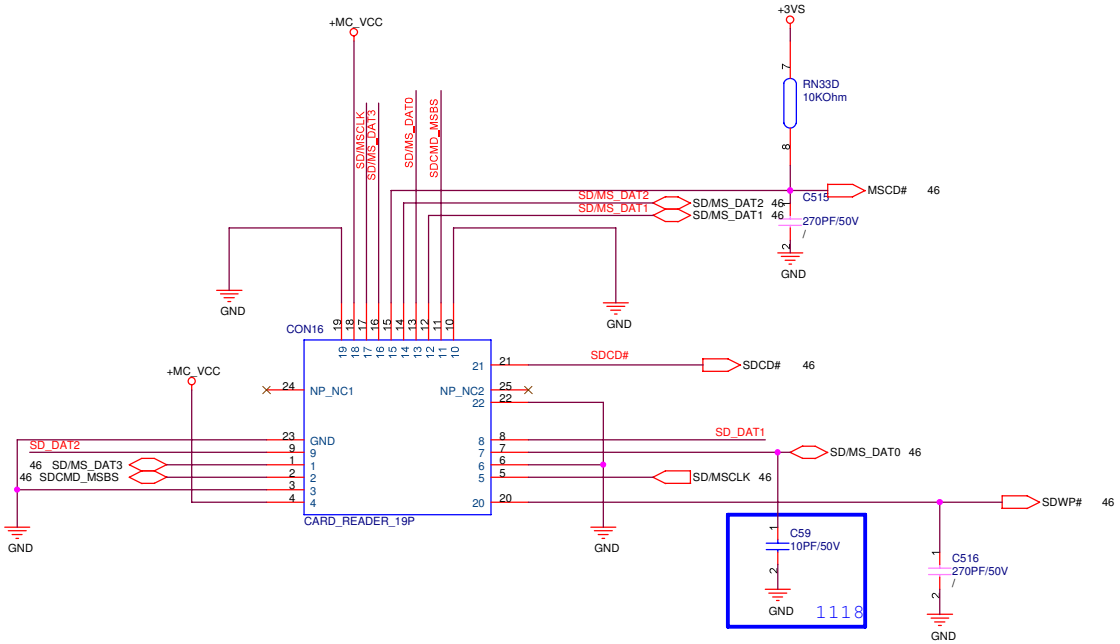


ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(1)	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 45 of 89	

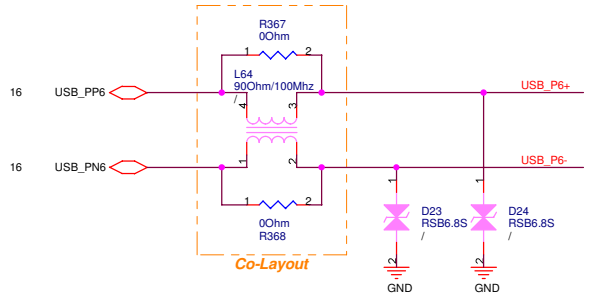


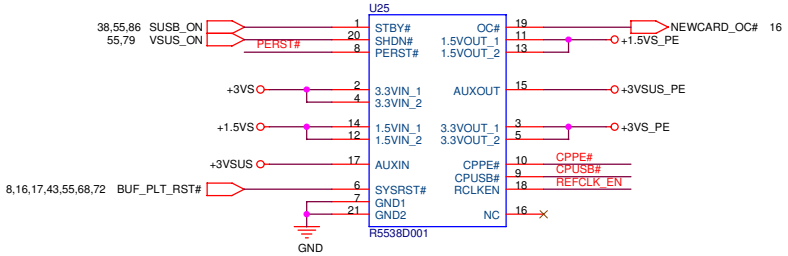
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 46 of 89	

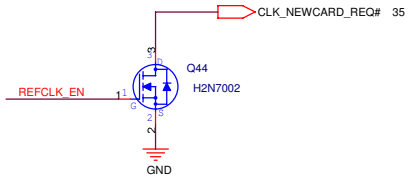


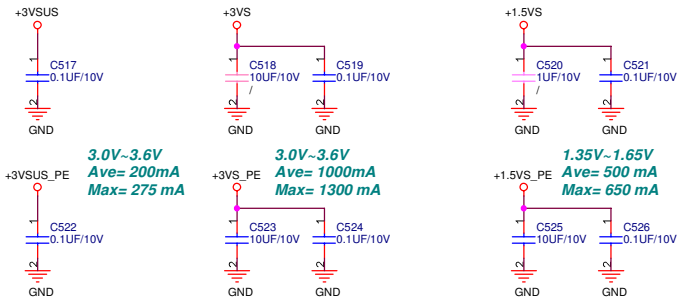


ASUSTeK COMPUTER INC	Title: 3 in 1 CARD READER	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 47 of 89	



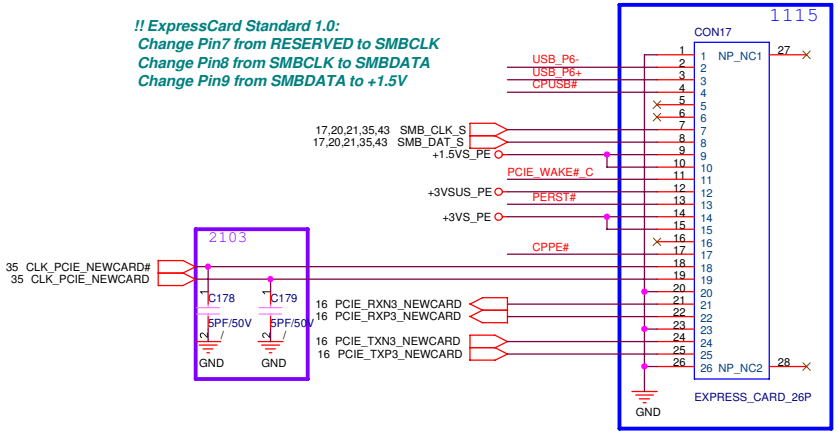




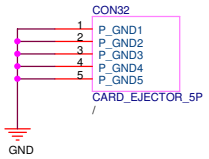


NewCard Header

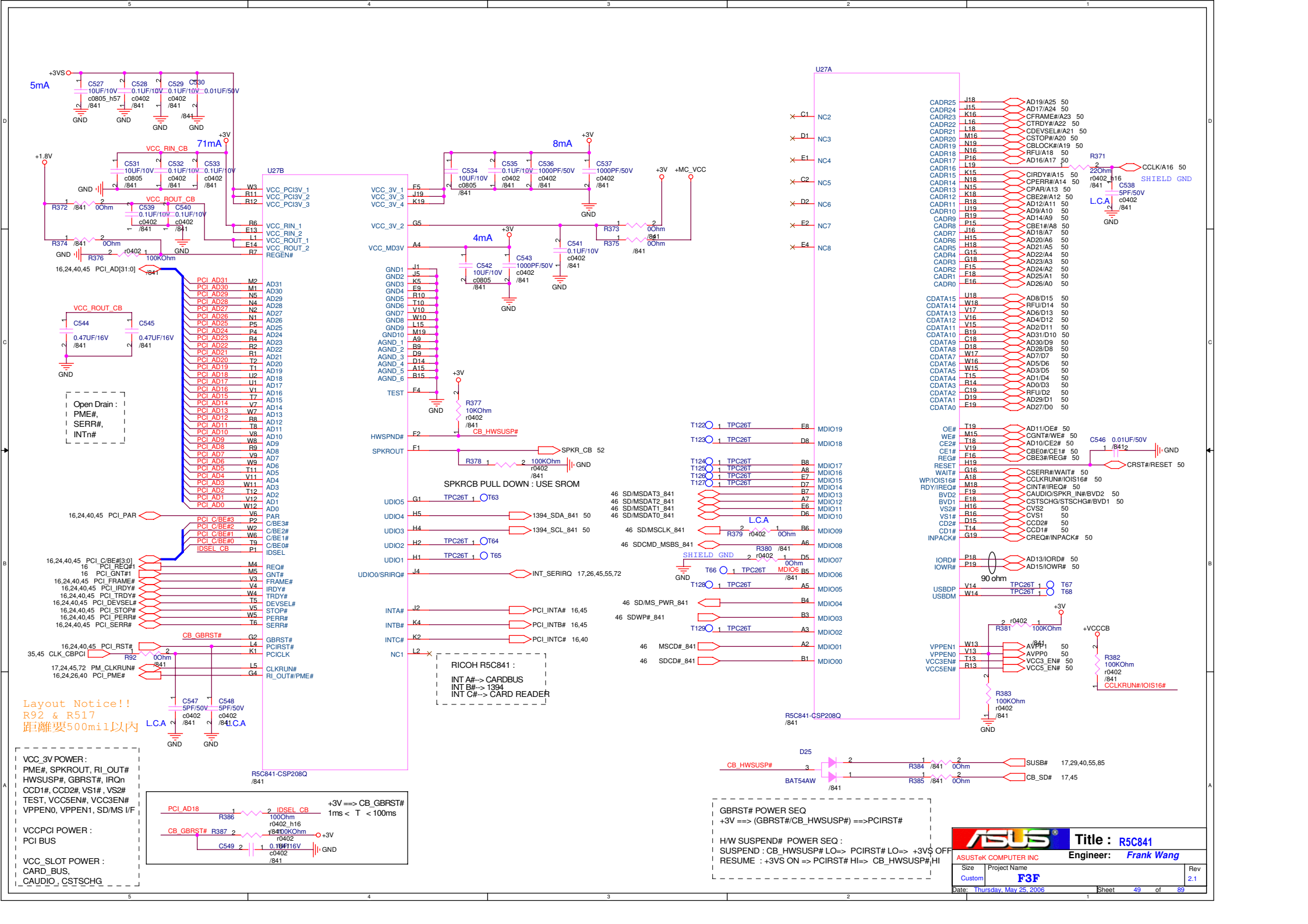
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

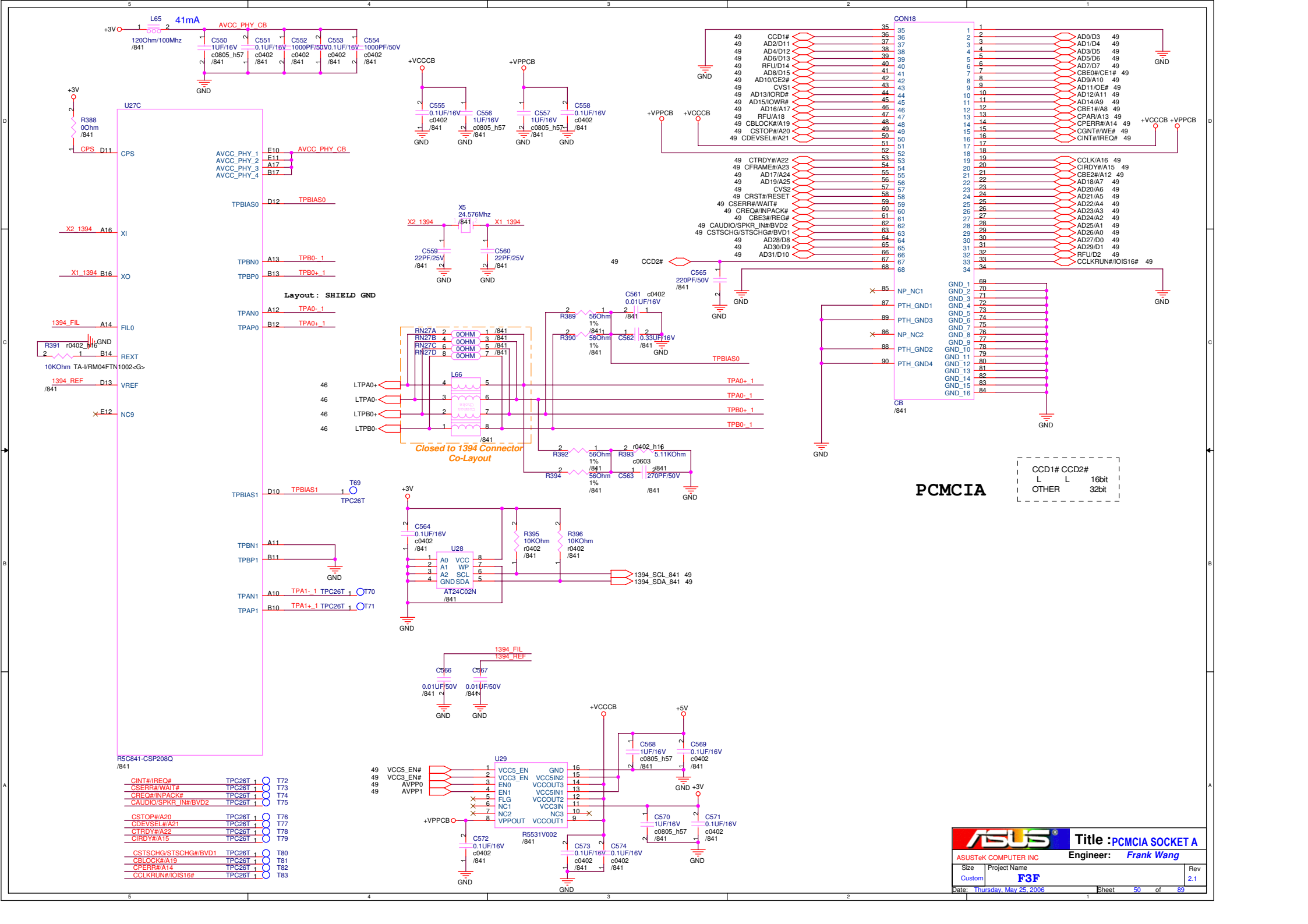


NewCard Ejecter

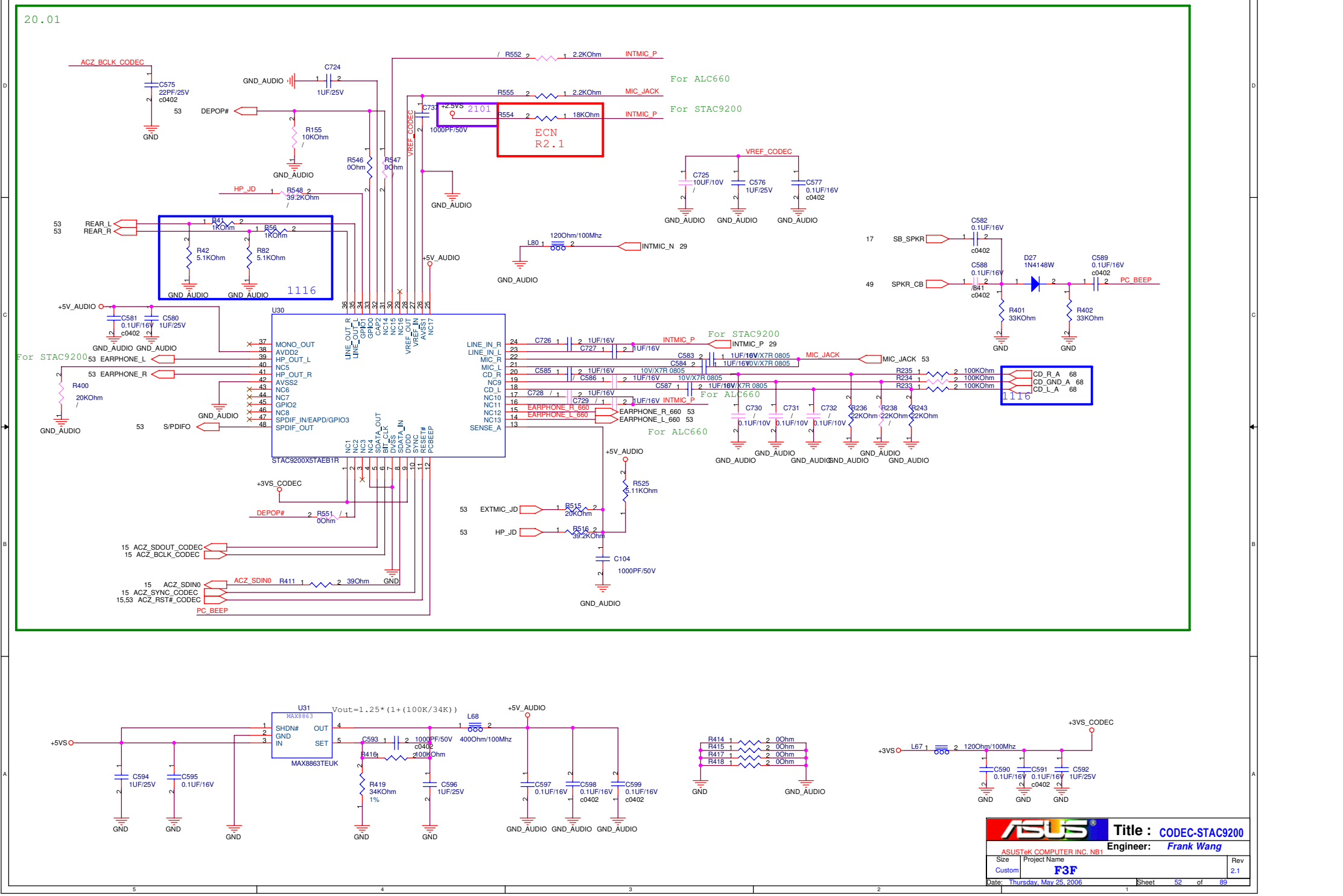


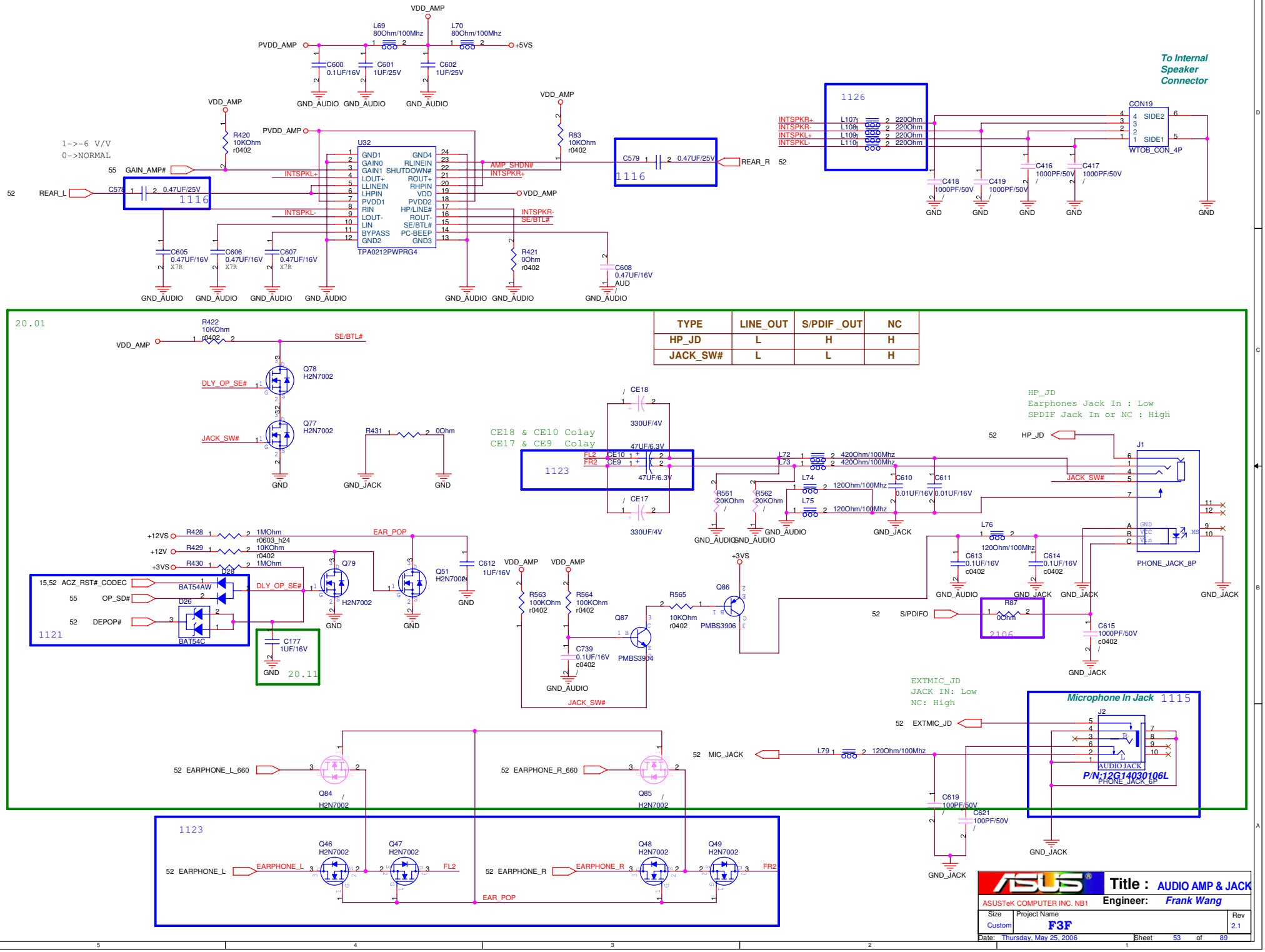
ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 48 of 89	


5mA
71mA
8mA
4mA
U27B
U27A
R5C841-CSP208Q
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
Layout Notice!!
R92 & R517
距離要500mil以內
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP#,HI
SHIELD GND
L.C.A
90 ohm
Title : R5C841
ASUSTeK COMPUTER INC
Engineer: Frank Wang
Size: Custom
Project Name: F3F
Rev: 2.1
Date: Thursday, May 25, 2006
Sheet 49 of 89


L65
41mA
+3V
AVCC_PHY_CB
120Ohm/100Mhz
/841
C550 1UF/16V c0805_h57 /841
C551 0.1UF/16V c0402 /841
C552 1000PF/50V c0402 /841
C553 0.1UF/16V c0402 /841
C554 1000PF/50V c0402 /841
GND
+VCCCB
+VPPCB
C555 0.1UF/16V c0402 /841
C556 1UF/16V c0805_h57 /841
C557 1UF/16V c0805_h57 /841
C558 0.1UF/16V c0402 /841
CON18
CCD1#
AD2/D11
AD4/D12
AD6/D13
RFU/D14
AD8/D15
AD10/CE2#
CVS1
AD13/IORD#
AD15/IOWR#
AD16/A17
RFU/A18
CBLOCK#/A19
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CFRAME#/A23
AD17/A24
AD19/A25
CVS2
CRST#/RESET
CSERR#/WAIT#
CREQ#/INPACK#
CBE3#/REG#
CAUDIO/SPKR_IN#/BVD2
CSTSCHG/STSCHG#/BVD1
AD28/D8
AD30/D9
AD31/D10
AD0/D3
AD1/D4
AD3/D5
AD5/D6
AD7/D7
CBE0#/CE1#
AD9/A10
AD11/OE#
AD12/A11
AD14/A9
CBE1#/A8
CPAR/A13
CPERR#/A14
CGNT#/WE#
CINT#/IREQ#
CCLK/A16
CIRDY#/A15
CBE2#/A12
AD18/A7
AD20/A6
AD21/A5
AD22/A4
AD23/A3
AD24/A2
AD25/A1
AD26/A0
AD27/D0
AD29/D1
RFU/D2
CCLKRUN#/IOIS16#
NP_NC1
PTH_GND1
PTH_GND3
NP_NC2
PTH_GND2
PTH_GND4
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
CB
/841
U27C
R388 0Ohm /841
CPS D11
AVCC_PHY_1 E10
AVCC_PHY_2 E11
AVCC_PHY_3 A17
AVCC_PHY_4 B17
TPBIAS0 D12
X5 24.576Mhz /841
X2_1394 A16
X1_1394 B16
C559 22PF/25V /841
C560 22PF/25V /841
TPBN0 A13
TPBP0 B13
Layout: SHIELD GND
C565 220PF/50V /841
C561 c0402 0.01UF/16V /841
R389 56Ohm 1% /841
R390 56Ohm 1% /841
C562 0.33UF/16V /841
TPAN0 A12
TPAP0 B12
1394_FIL A14
FIL0
R391 r0402_h16
REXT B14
10KOhm TA-I/RM04FTN1002<G>
1394_REF /841 D13
VREF
NC9 E12
RN27A 0OHM /841
RN27B 0OHM /841
RN27C 0OHM /841
RN27D 0OHM /841
L66
LTPA0+
LTPA0-
LTPB0+
LTPB0-
TPA0+_1
TPA0-_1
TPB0+_1
TPB0-_1
Closed to 1394 Connector Co-Layout
R392 56Ohm 1% /841
R393 5.11KOhm c0603 /841
R394 56Ohm 1% /841
C563 270PF/50V /841
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
TPBIAS1 D10
T69
TPC26T
C564 0.1UF/16V c0402 /841
U28
AT24C02N /841
R395 10KOhm r0402 /841
R396 10KOhm r0402 /841
1394_SCL_841
1394_SDA_841
TPBN1 A11
TPBP1 B11
TPAN1 A10
TPAP1 B10
TPA1-_1
TPA1+_1
T70
T71
C566 0.01UF/50V /841
C567 0.01UF/50V /841
U29
VCC5_EN
VCC3_EN
EN0
EN1
FLG
NC1
NC2
VPPOUT
GND
VCC5IN2
VCCOUT3
VCC5IN1
VCCOUT2
VCC3IN
NC3
VCCOUT1
R5531V002 /841
C568 1UF/16V c0805_h57 /841
C569 0.1UF/16V c0402 /841
C570 1UF/16V c0805_h57 /841
C571 0.1UF/16V c0402 /841
C572 0.1UF/16V c0402 /841
C573 0.1UF/16V c0402 /841
C574 0.1UF/16V c0402 /841
R5C841-CSP208Q /841
CINT#/IREQ# T72
CSERR#/WAIT# T73
CREQ#/INPACK# T74
CAUDIO/SPKR_IN#/BVD2 T75
CSTOP#/A20 T76
CDEVSEL#/A21 T77
CTRDY#/A22 T78
CIRDY#/A15 T79
CSTSCHG/STSCHG#/BVD1 T80
CBLOCK#/A19 T81
CPERR#/A14 T82
CCLKRUN#/IOIS16# T83
TPC26T
ASUSTeK COMPUTER INC
Title : PCMCIA SOCKET A
Engineer: Frank Wang
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
Sheet 50 of 89

ASUSTeK COMPUTER INC	Title : F3J	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 51 of 89	


20.01
ACZ_BCLK_CODEC
C575 22PF/25V c0402
GND
C724 1UF/25V
GND_AUDIO
53 DEPOP#
R155 10KOhm /
R546 0Ohm
R547 0Ohm /
VREF_CODEC
C731 1000PF/50V
+2.5VS
2101
R552 2.2KOhm INTMIC_P
For ALC660
R555 2.2KOhm MIC_JACK
For STAC9200
R554 18KOhm INTMIC_P
ECN R2.1
HP_JD
R548 39.2KOhm /
C725 10UF/10V /
C576 1UF/25V
C577 0.1UF/16V c0402
53 REAR_L
53 REAR_R
R41 1KOhm
R56 1KOhm
R42 5.1KOhm
R82 5.1KOhm
1116
L80 120Ohm/100Mhz
INTMIC_N 29
+5V_AUDIO
17 SB_SPKR
C582 0.1UF/16V c0402
49 SPKR_CB
C588 0.1UF/16V /841 c0402
D27 1N4148W
C589 0.1UF/16V c0402
PC_BEEP
R401 33KOhm
R402 33KOhm
C581 0.1UF/16V c0402
C580 1UF/25V
U30
MONO_OUT
AVDD2
HP_OUT_L
NC5
HP_OUT_R
AVSS2
NC6
NC7
GPIO2
NC8
SPDIF_IN/EAPD/GPIO3
SPDIF_OUT
LINE_OUT_R
LINE_OUT_L
GPIO1
GPIO0
CAP2
NC14
NC15
NC16
VREF_OUT
VREF_IN
AVSS1
NC17
LINE_IN_R
LINE_IN_L
MIC_R
MIC_L
CD_R
NC9
CD_L
NC10
NC11
NC12
NC13
SENSE_A
NC1
NC2
NC3
NC4
SDATA_OUT
BIT_CLK
DVSS
SDATA_IN
DVDD
SYNC
RESET#
PCBEEP
STAC9200X5TAEB1R
53 EARPHONE_L
53 EARPHONE_R
R400 20KOhm /
53 S/PDIFO
C726 1UF/16V
C727 1UF/16V
INTMIC_P
INTMIC_P 29
C583 1UF/16V/X7R 0805
C584 1UF/16V/X7R 0805
MIC_JACK
MIC_JACK 53
C585 1UF/16V 10V/X7R 0805
C586 1UF/16V 10V/X7R 0805
C587 1UF/16V/X7R 0805
C728 / 1UF/16V
C729 / 1UF/16V INTMIC_P
EARPHONE_R_660
EARPHONE_L_660
EARPHONE_R_660 53
EARPHONE_L_660 53
For ALC660
C730 / 0.1UF/10V
C731 / 0.1UF/10V
C732 / 0.1UF/10V
R235 100KOhm
R234 100KOhm
R233 100KOhm
CD_R_A 68
CD_GND_A 68
CD_L_A 68
1116
R236 22KOhm
R238 22KOhm /
R243 22KOhm
+3VS_CODEC
DEPOP# 2 R551 0Ohm /
+5V_AUDIO
R525 5.11KOhm
53 EXTMIC_JD
R515 20KOhm
53 HP_JD
R516 39.2KOhm
C104 1000PF/50V
15 ACZ_SDOUT_CODEC
15 ACZ_BCLK_CODEC
15 ACZ_SDIN0
15 ACZ_SYNC_CODEC
15,53 ACZ_RST#_CODEC
ACZ_SDIN0 R411 39Ohm GND
PC_BEEP
U31
MAX8863
Vout=1.25*(1+(100K/34K))
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
L68 400Ohm/100Mhz
C593 1000PF/50V c0402
R416 100KOhm
R419 34KOhm 1%
C596 1UF/25V
C594 1UF/25V
C595 0.1UF/16V
+5VS
C597 0.1UF/16V
C598 0.1UF/16V c0402
C599 0.1UF/16V c0402
R414 0Ohm
R415 0Ohm
R417 0Ohm
R418 0Ohm
+3VS
L67 120Ohm/100Mhz
C590 0.1UF/16V
C591 0.1UF/16V c0402
C592 1UF/25V
Title : CODEC-STAC9200
Engineer: Frank Wang
ASUSTeK COMPUTER INC. NB1
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
Sheet 52 of 89


VDD_AMP
L69 80Ohm/100Mhz
L70 80Ohm/100Mhz
PVDD_AMP
+5VS
C600 0.1UF/16V
C601 1UF/25V
C602 1UF/25V
GND_AUDIO
To Internal Speaker Connector
1126
CON19
SIDE2
SIDE1
WTOB_CON_4P
INTSPKR+
INTSPKR-
INTSPKL+
INTSPKL-
L107 220Ohm
L108 220Ohm
L109 220Ohm
L110 220Ohm
C416 1000PF/50V
C417 1000PF/50V
C418 1000PF/50V
C419 1000PF/50V
GND
1->-6 V/V
0->NORMAL
R420 10KOhm r0402
R83 10KOhm r0402
55 GAIN_AMP#
52 REAR_L
C578 0.47UF/25V
1116
U32
GND1 GND4
GAIN0 RLINEIN
GAIN1 SHUTDOWN#
LOUT+ ROUT+
LLINEIN RHPIN
LHPIN VDD
PVDD1 PVDD2
RIN HP/LINE#
LOUT- ROUT-
LIN SE/BTL#
BYPASS PC-BEEP
GND2 GND3
TPA0212PWPRG4
AMP_SHDN#
INTSPKR+
INTSPKR-
SE/BTL#
C579 0.47UF/25V
REAR_R 52
C605 0.47UF/16V X7R
C606 0.47UF/16V X7R
C607 0.47UF/16V X7R
C608 0.47UF/16V AUD
R421 0Ohm r0402
20.01
R422 10KOhm r0402
SE/BTL#
Q78 H2N7002
Q77 H2N7002
DLY_OP_SE#
JACK_SW#
R431 0Ohm
GND_JACK
TYPE | LINE_OUT | S/PDIF _OUT | NC
HP_JD | L | H | H
JACK_SW# | L | L | H
CE18 & CE10 Colay
CE17 & CE9 Colay
CE18 330UF/4V
CE10 47UF/6.3V
CE9 47UF/6.3V
CE17 330UF/4V
FL2
FR2
1123
HP_JD
Earphones Jack In : Low
SPDIF Jack In or NC : High
52 HP_JD
J1
L72 420Ohm/100Mhz
L73 420Ohm/100Mhz
L74 120Ohm/100Mhz
L75 120Ohm/100Mhz
L76 120Ohm/100Mhz
R561 20KOhm
R562 20KOhm
C610 0.01UF/16V
C611 0.01UF/16V
C613 0.1UF/16V c0402
C614 0.1UF/16V c0402
C615 1000PF/50V c0402
R87 0Ohm
2106
52 S/PDIFO
PHONE_JACK_8P
+12VS
+12V
+3VS
R428 1MOhm r0603_h24
R429 10KOhm r0402
R430 1MOhm r0402
D28 BAT54AW
D26 BAT54C
15,52 ACZ_RST#_CODEC
55 OP_SD#
52 DEPOP#
1121
Q79 H2N7002
Q51 H2N7002
EAR_POP
C612 1UF/16V
C177 1UF/16V
20.11
R563 100KOhm r0402
R564 100KOhm r0402
R565 10KOhm r0402
Q86 PMBS3904
Q87 PMBS3904
C739 0.1UF/16V c0402
EXTMIC_JD
JACK IN: Low
NC: High
Microphone In Jack 1115
J2
52 EXTMIC_JD
52 MIC_JACK
L79 120Ohm/100Mhz
AUDIO JACK
P/N:12G14030106L
PHONE_JACK_6P
C619 100PF/50V
C621 100PF/50V
52 EARPHONE_L_660
52 EARPHONE_R_660
Q84 H2N7002
Q85 H2N7002
1123
Q46 H2N7002
Q47 H2N7002
Q48 H2N7002
Q49 H2N7002
52 EARPHONE_L
52 EARPHONE_R
EARPHONE_L
EARPHONE_R
EAR_POP
Title : AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Wang
Size Custom
Project Name F3F
Rev 2.1
Date: Thursday, May 25, 2006
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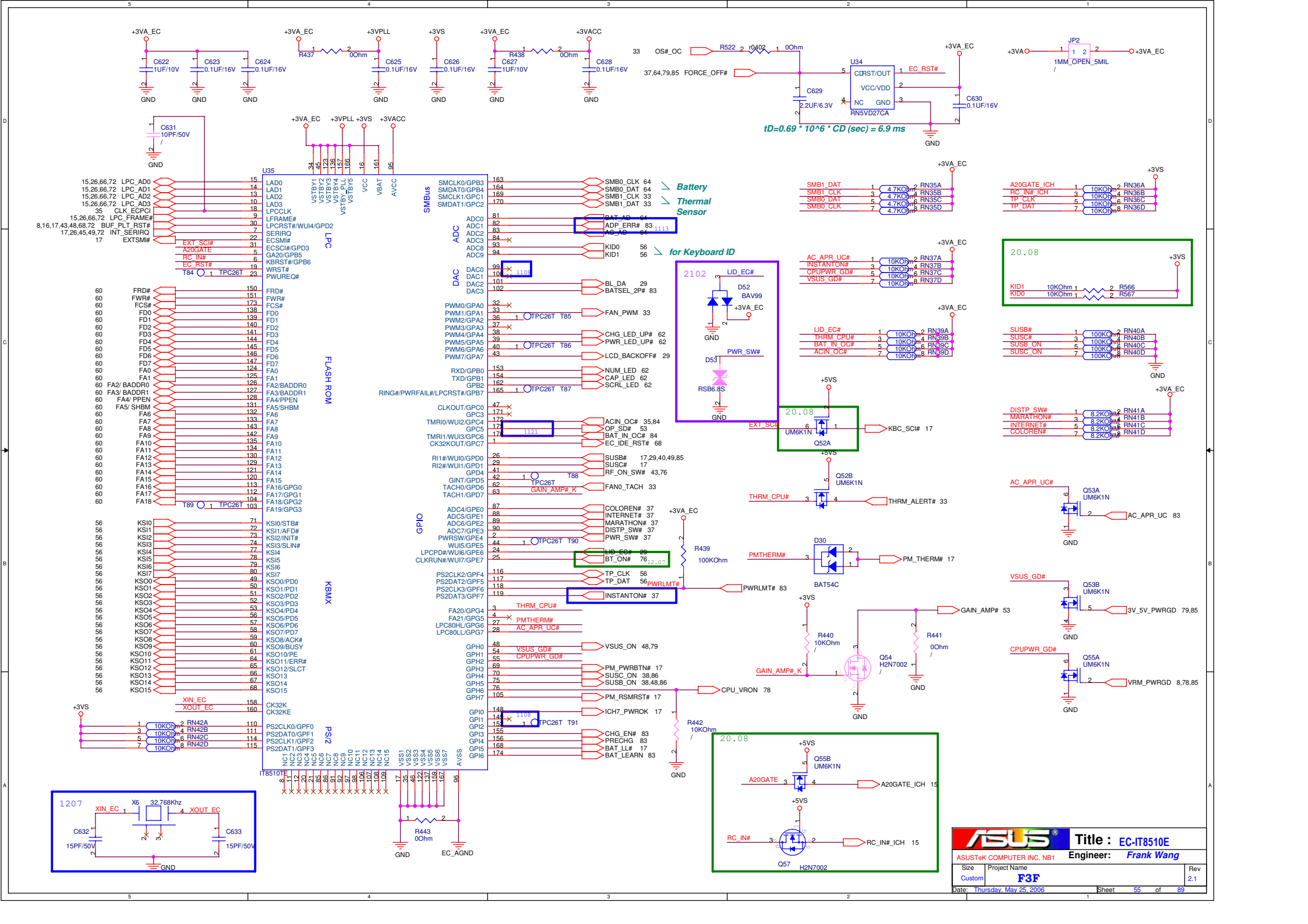
ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: **F3F**	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 54 of 89	


U35
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
SMBus
ADC
DAC
Battery
Thermal Sensor
for Keyboard ID
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
20.08
2102
1207
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Frank Wang
Project Name F3F
Size Custom
Rev 2.1
Date: Thursday, May 25, 2006
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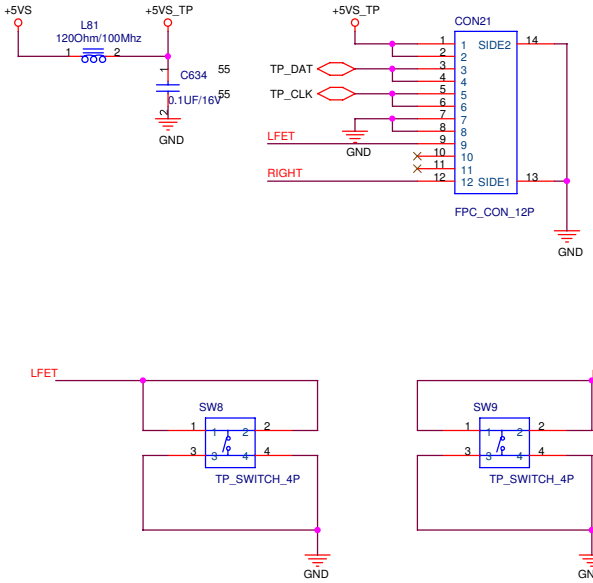
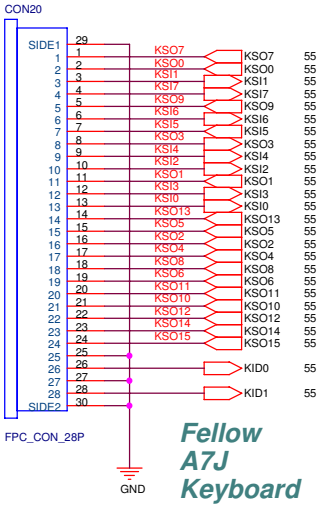
For Touch-Pad



For Keyboard



Fellow A7J Keyboard

ASUSTeK COMPUTER INC. NB1		Title :	Touch Pad & KB
		Engineer:	Frank Wang
Size: Custom	Project Name: F3F		Rev: 2.1
Date: Thursday, May 25, 2006		Sheet 56 of 89	

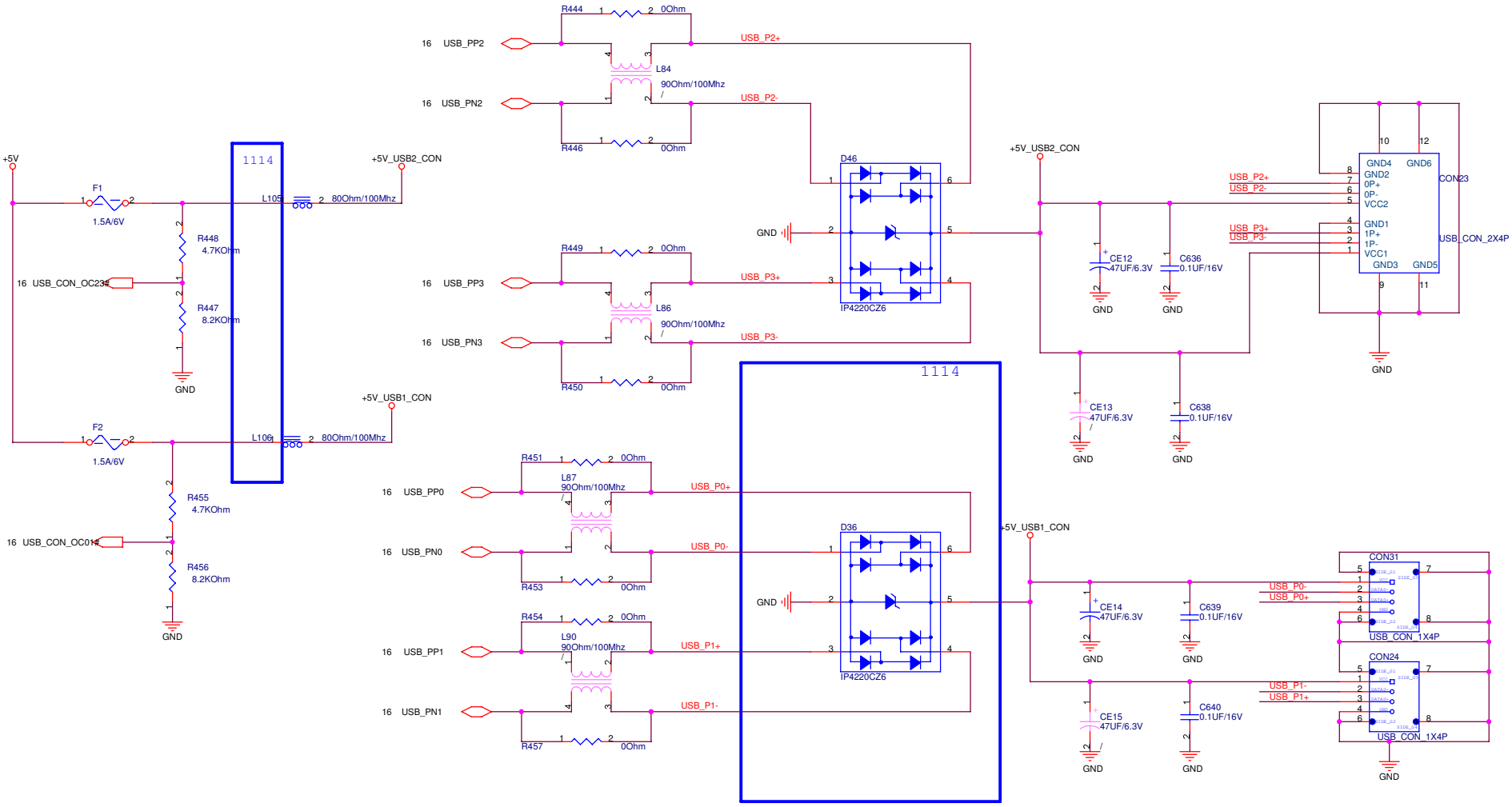
Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: Frank Wang

Size	Project Name	Rev
Custom	F3F	2.1

Date: Thursday, May 25, 2006 Sheet 57 of 89



ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 58 of 89	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 59 of 89

ISA ROM

EC Hardware Strapping

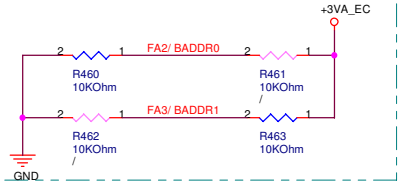
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

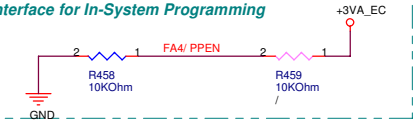


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

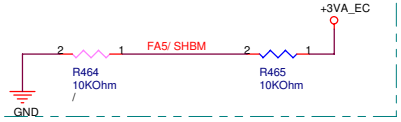
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

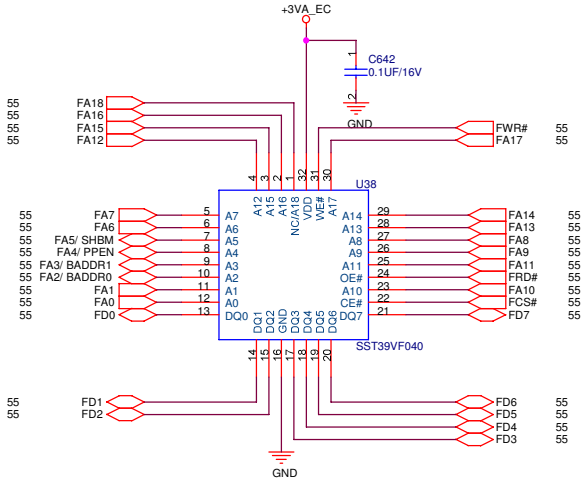


FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



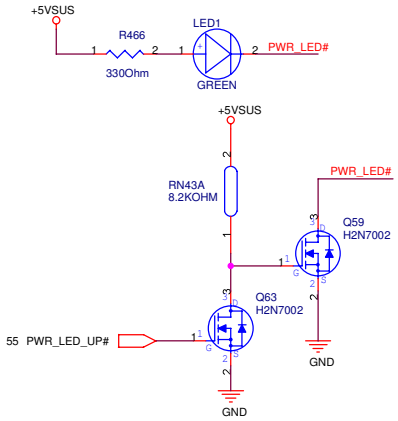


ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 60 of 89	

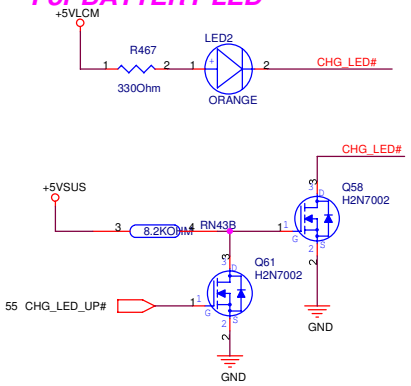
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 61 of 89

For LED

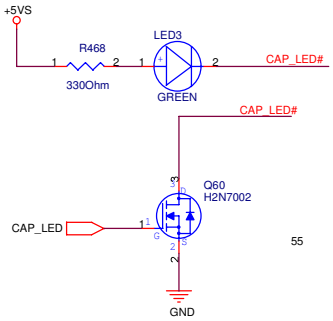
For POWER LED



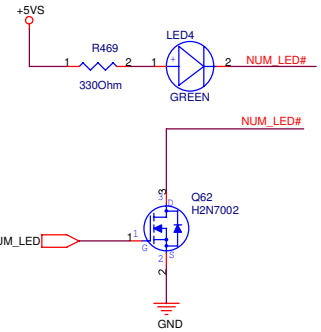
For BATTERY LED



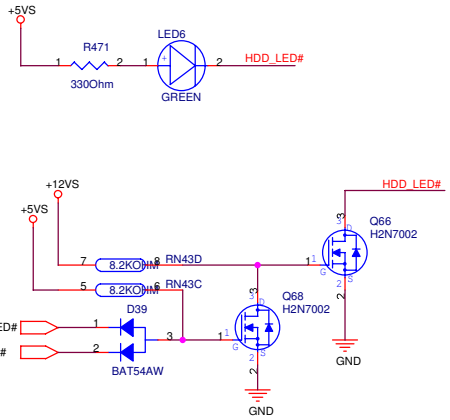
for Cap. Lock



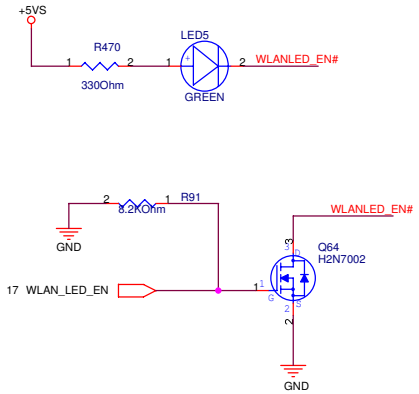
for Num Lock



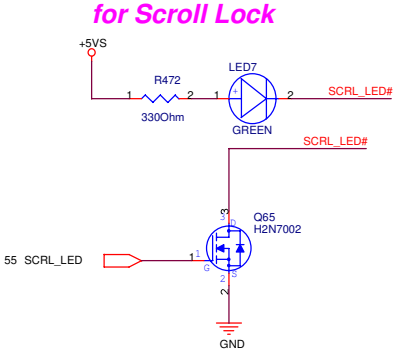
For SATA/IDE LED



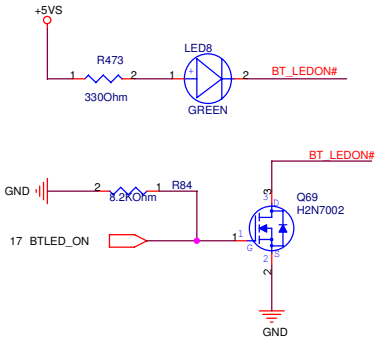
For WireLess LED



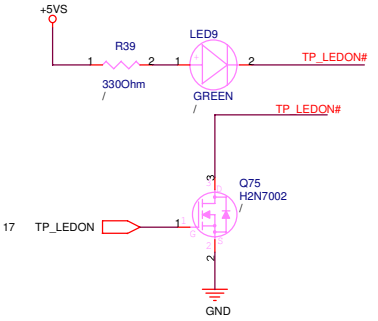
for Scroll Lock



For BT LED



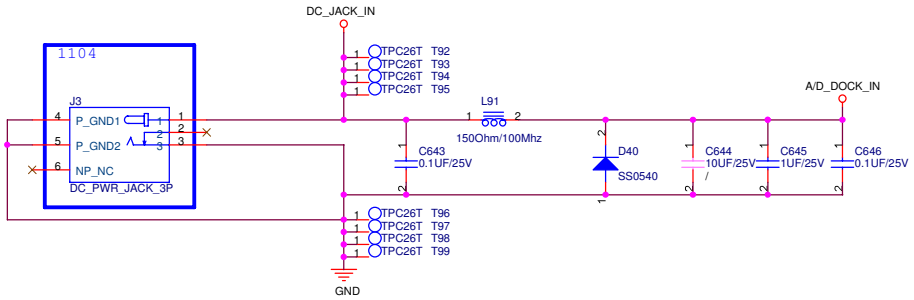
for Touch Pad



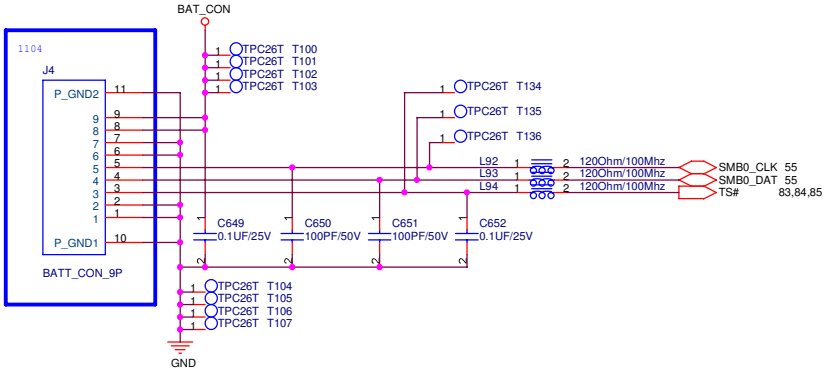
ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 62 of 89	

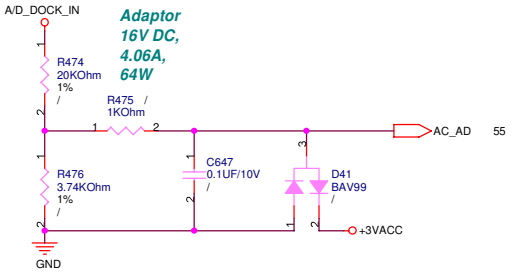
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 63 of 89

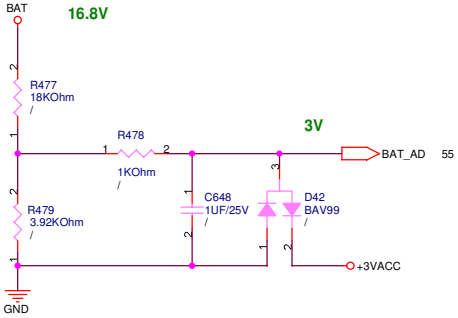
DC IN



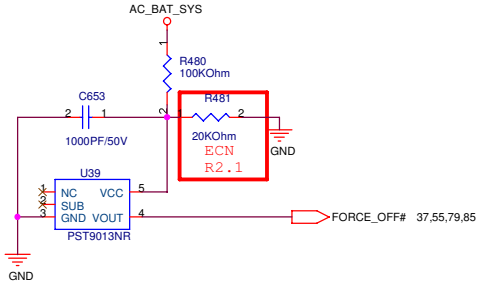
BAT IN







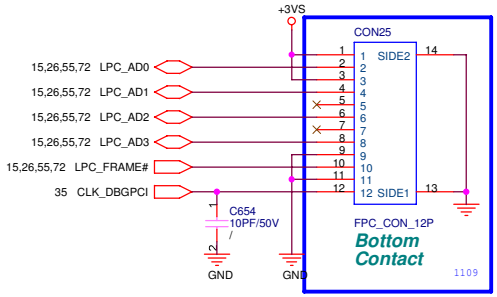
Without Battery & Pull out Adapter

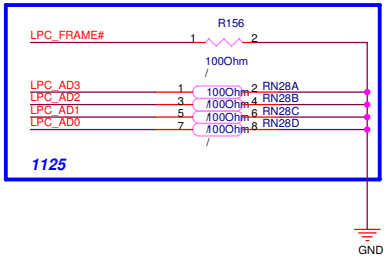


ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 64 of 89	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 65 of 89

For Debug





ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 66 of 89	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
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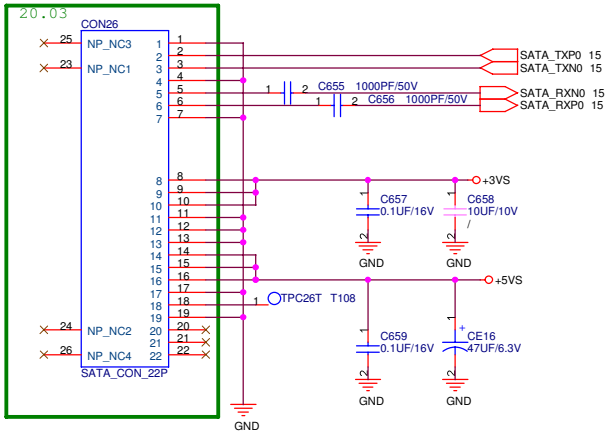
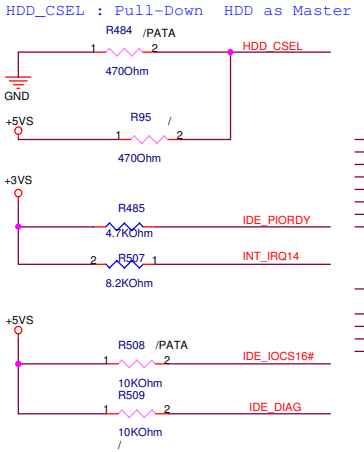
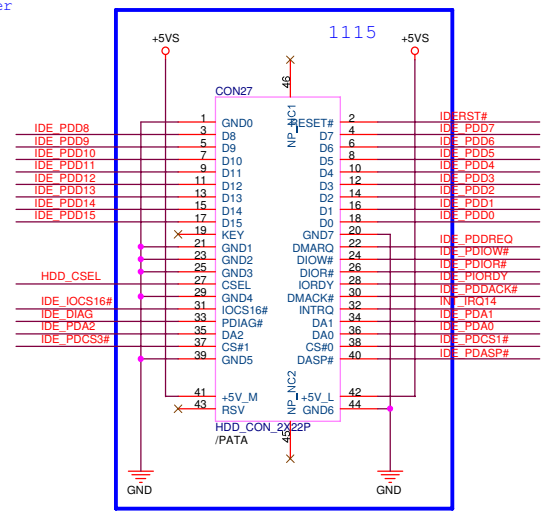


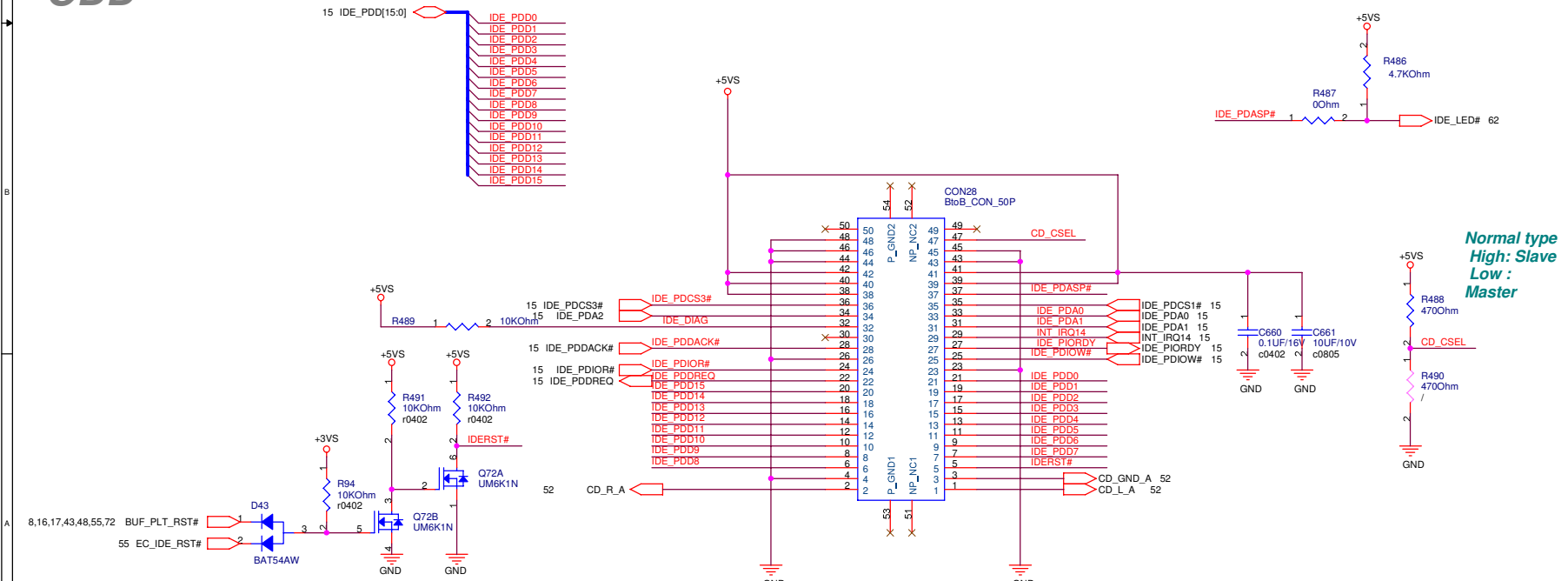




SATA HDD

PATA HDD

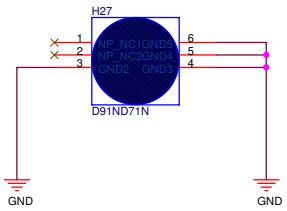
ODD



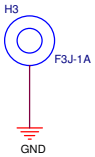
ASUSTeK COMPUTER INC. NB1	Title : HDD & ODD	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 68 of 89	

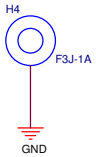
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 69 of 89

FOR LEFT UNDER

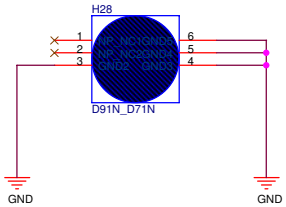


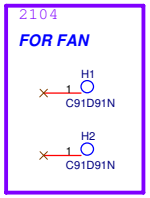
FOR FAN

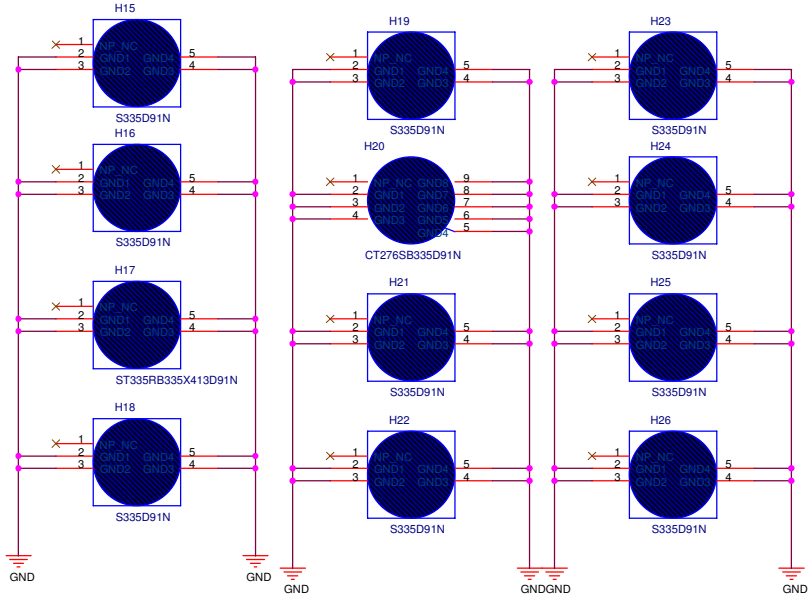




FOR RIGHT UP

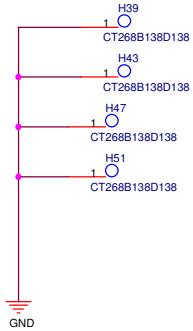






FOR SCREW HOLE

FOR CPU



ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
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ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Frank Wang*	
Size: Custom	Project Name: F3F	Rev: 2.1
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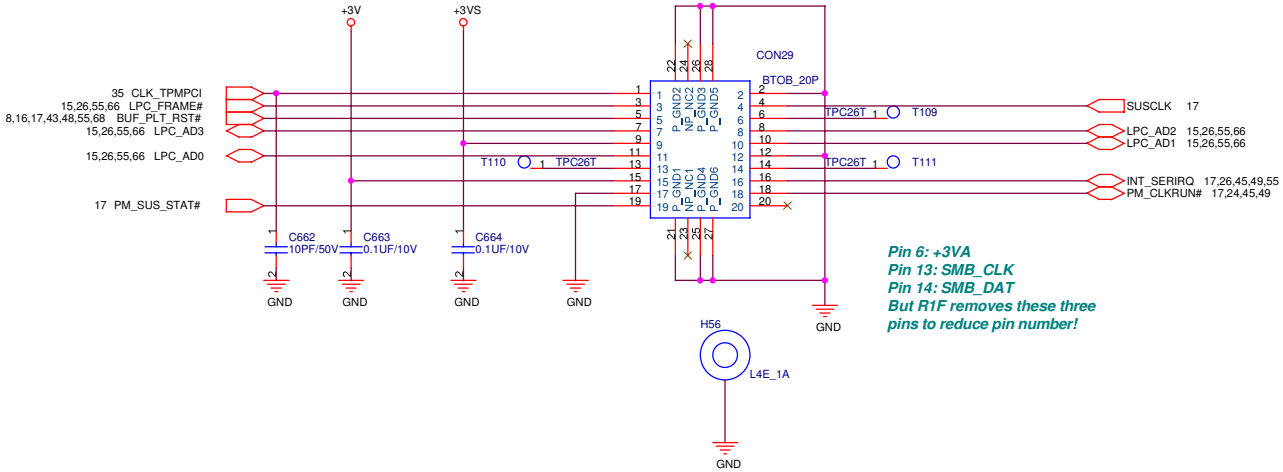
For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
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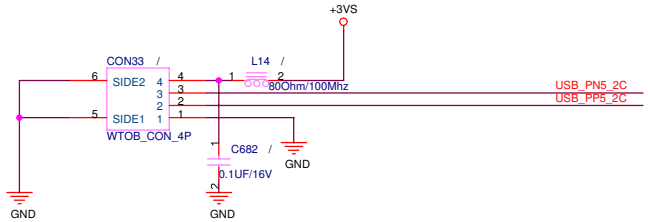
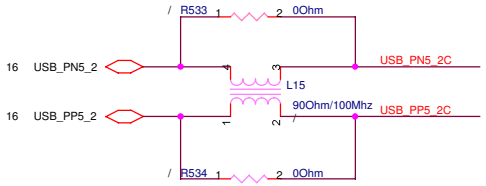
Title :	
<OrgName>	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 73 of 89





ASUSTeK COMPUTER INC	Title : FINGER PRINT	
	Engineer: Frank Wang	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 74 of 89	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: *Frank Wang*
Size: Custom	Project Name: **F3F**
Rev: 2.1	
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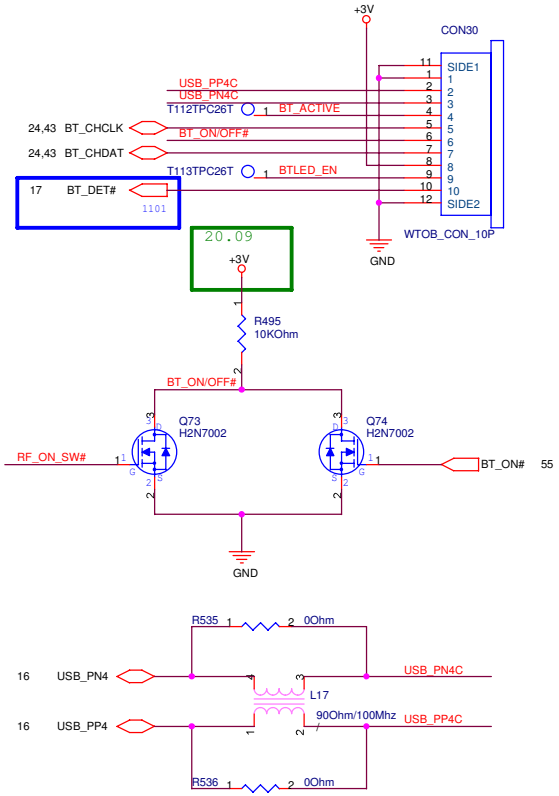
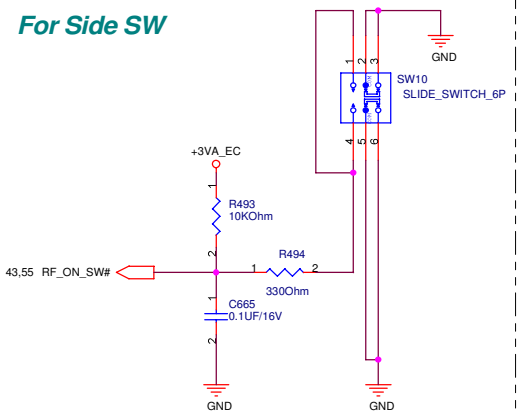
For Bluetooth



For Side SW



ASUSTeK COMPUTER INC	Title : Blue Tooth		
	Engineer: Frank Wang		
Size: Custom	Project Name: F3F		Rev: 2.1
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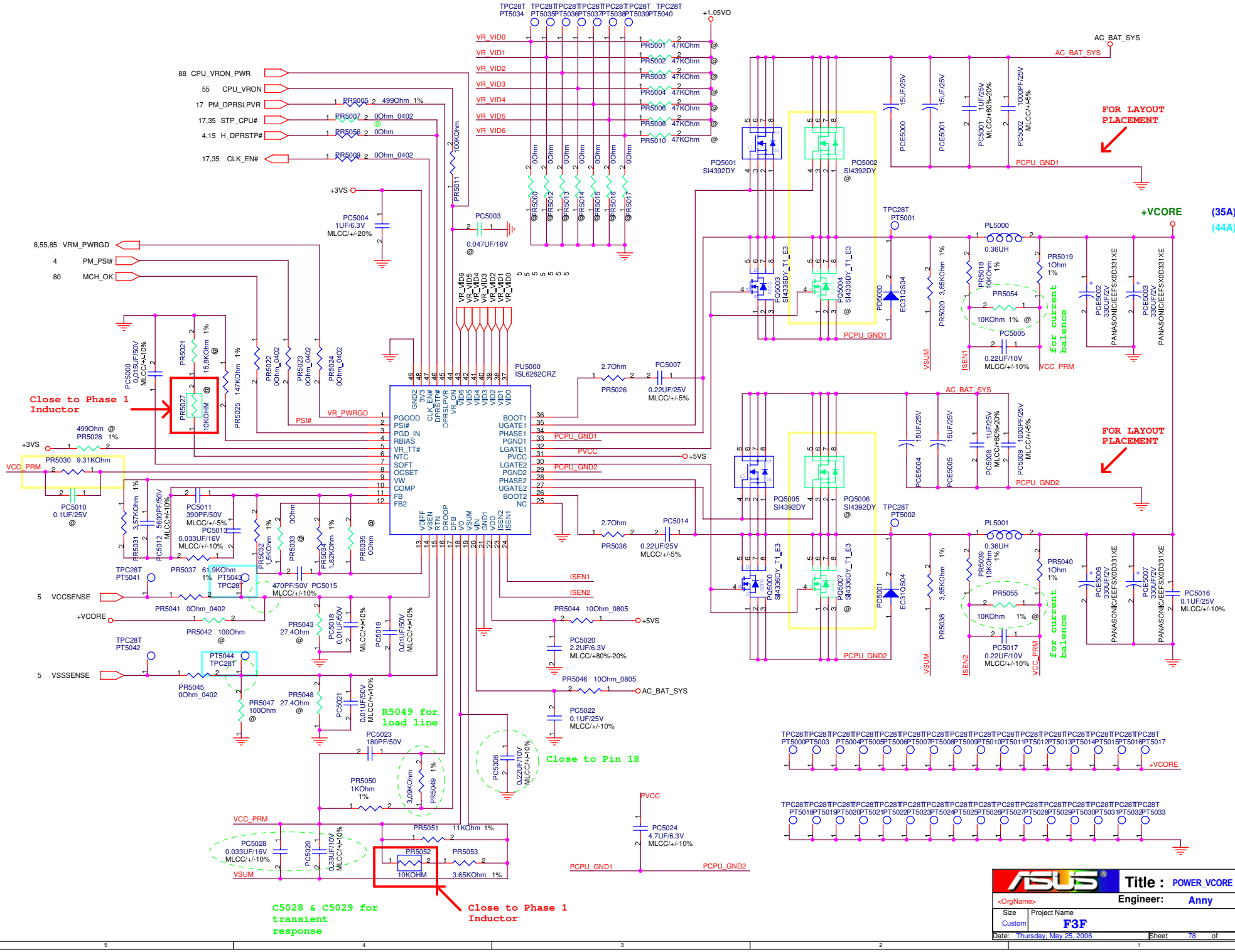
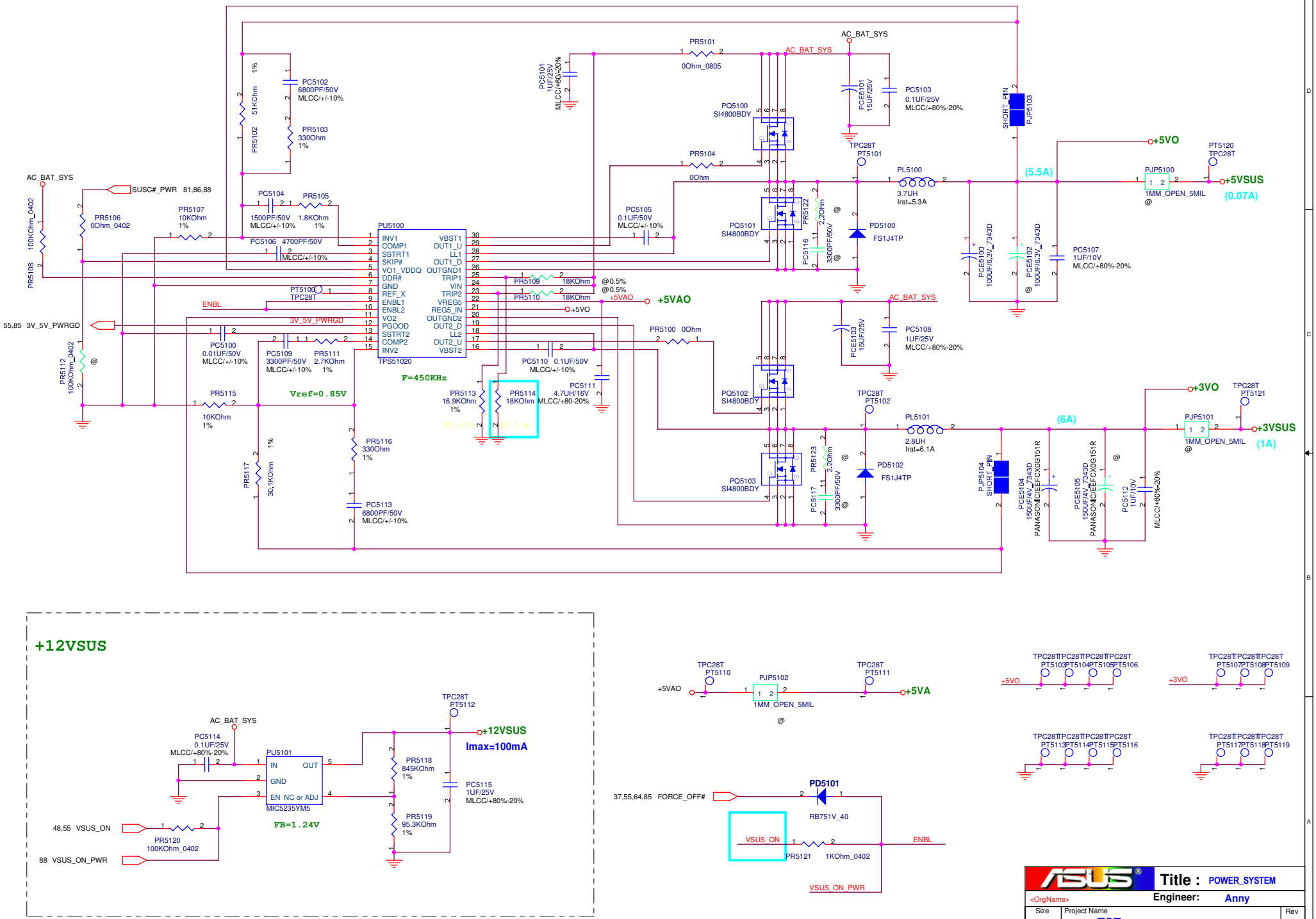
Title :	
<OrgName>	Engineer: Frank Wang
Size: Custom	Project Name: F3F
Rev: 2.1	
Date: Thursday, May 25, 2006	Sheet 77 of 89


+VCORE (35A) (44A)
Close to Phase 1 Inductor
FOR LAYOUT PLACEMENT
for current balence
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
PU5000 ISL6262CRZ
PQ5001 SI4392DY
PQ5002 SI4392DY
PQ5005 SI4392DY
PQ5006 SI4392DY
PL5000 0.36UH
PL5001 0.36UH
AC_BAT_SYS
+5VS
+3VS
PCPU_GND1
PCPU_GND2
PVCC
VCC_PRM
VSUM
ISEN1
ISEN2
Title : POWER_VCORE
Engineer: Anny
Project Name F3F
Rev 2.1
Sheet 78 of 89
Date: Thursday, May 25, 2006



ASUS

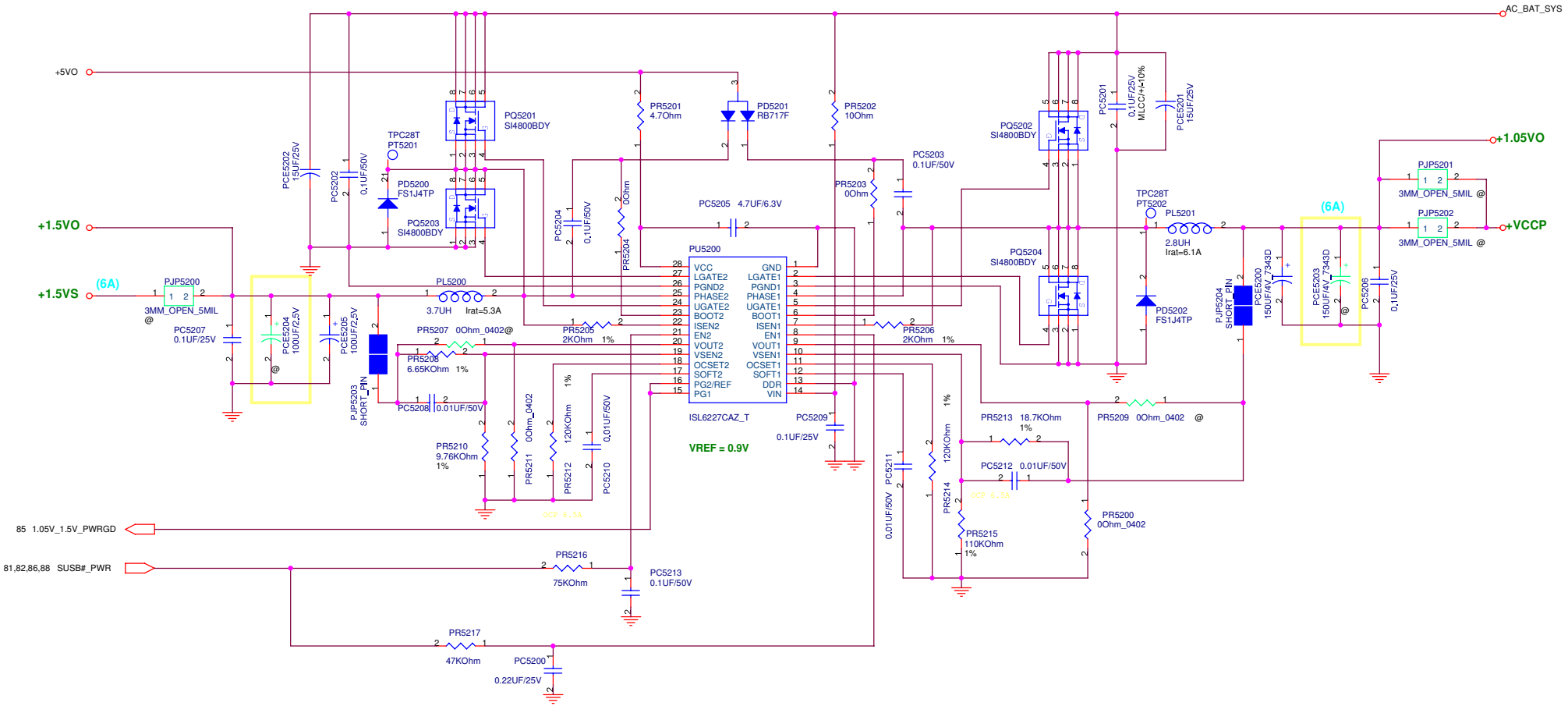
Title : POWER_SYSTEM

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	F3F	2.1

Date: Thursday, May 25, 2006 Sheet 79 of 89



ASUS

Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	F3F	2.1

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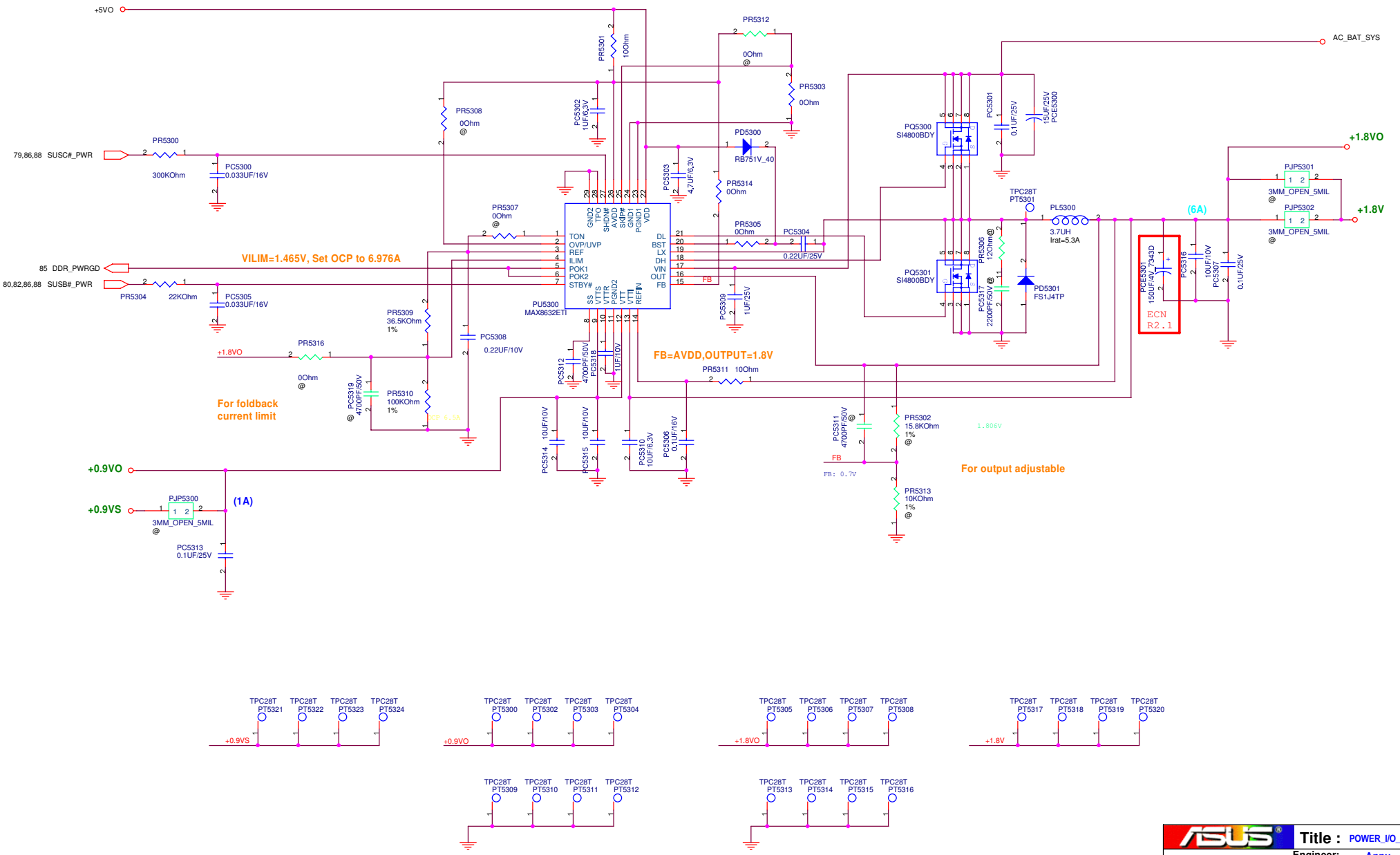

Title :	POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	Anny
Size: Custom	Project Name: F3F	Rev: 2.1
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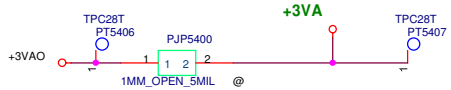
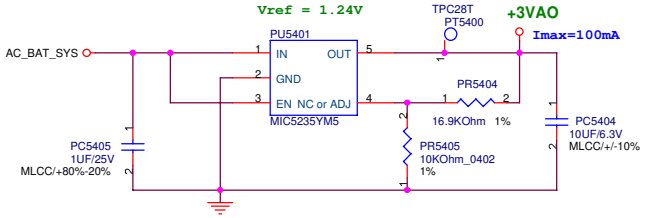
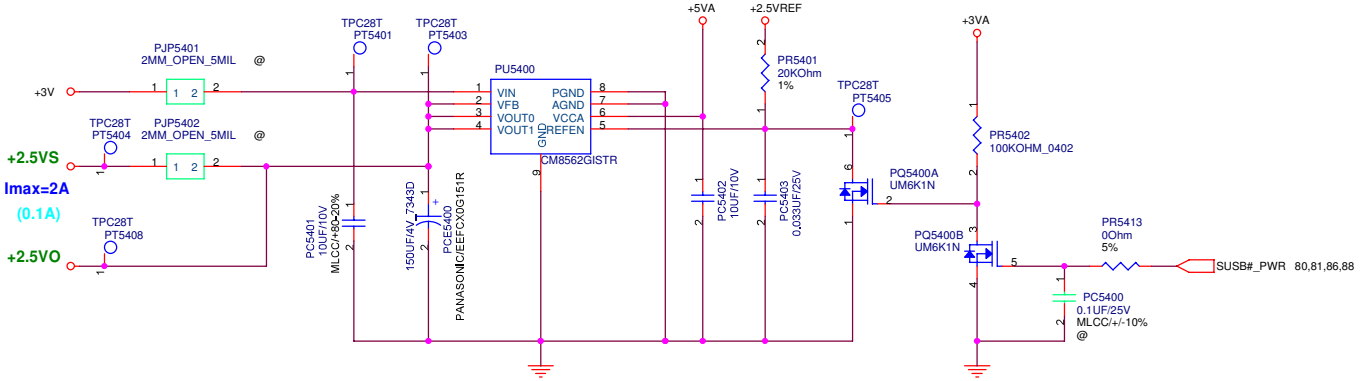
+3VAO





+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: F3F	Rev: 2.1
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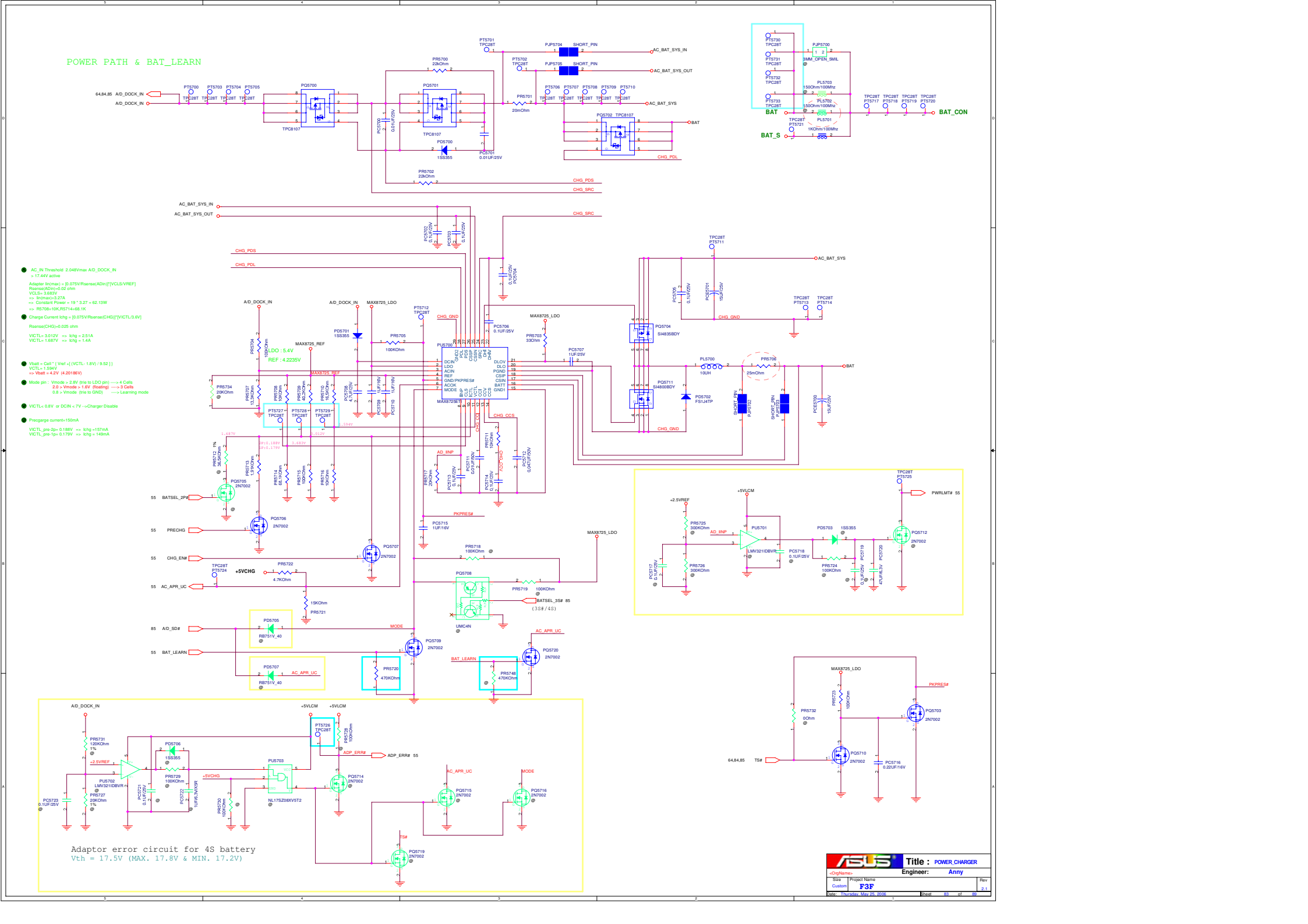
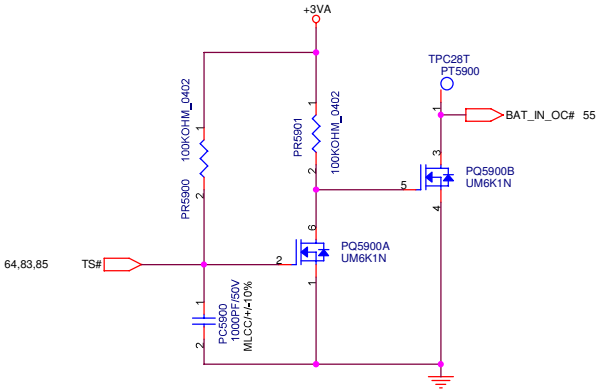
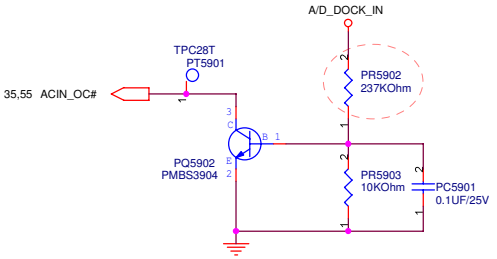
POWER PATH & BAT_LEARN



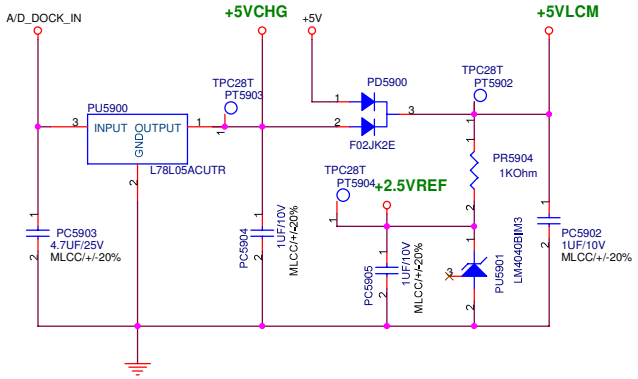
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: F3F	Rev: 2.1
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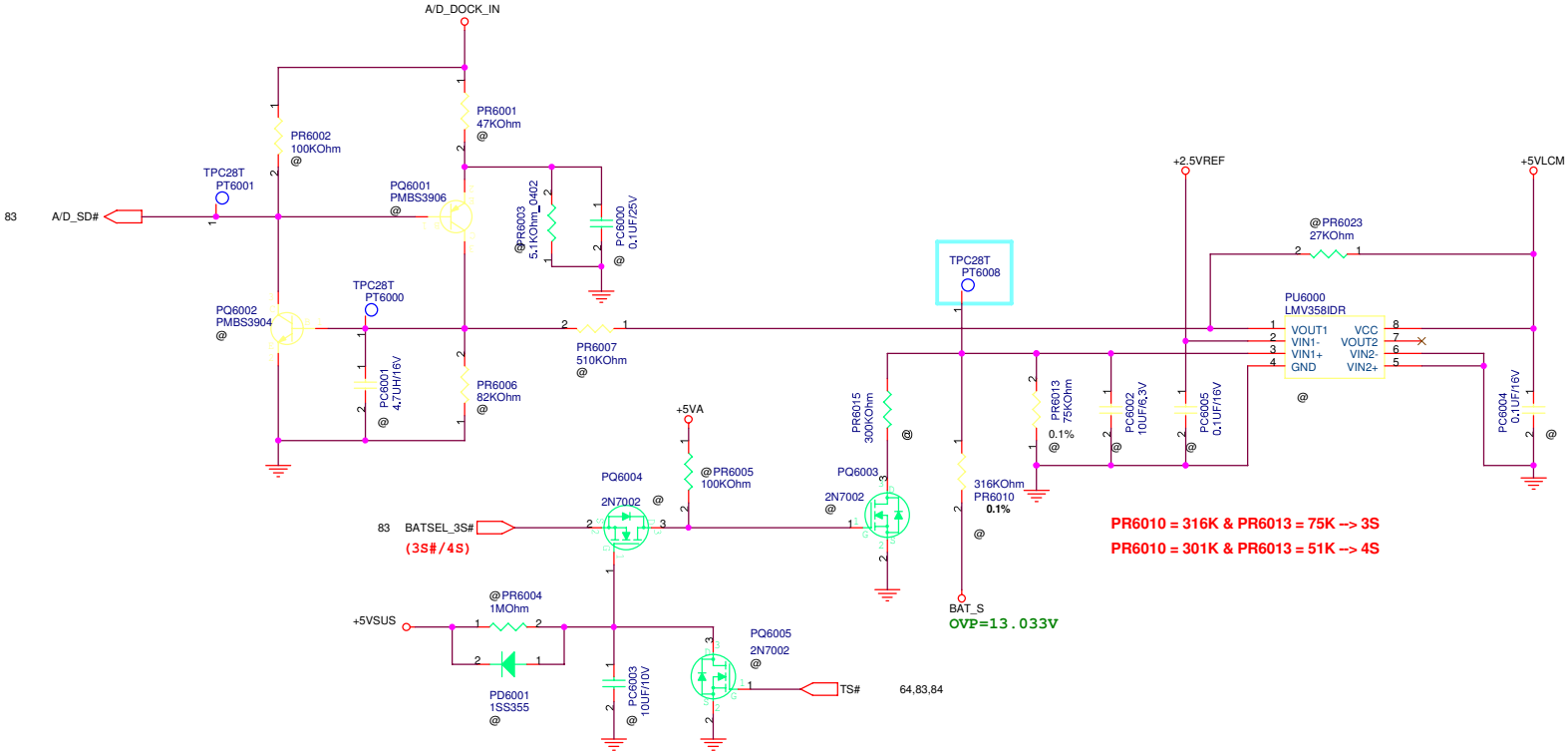
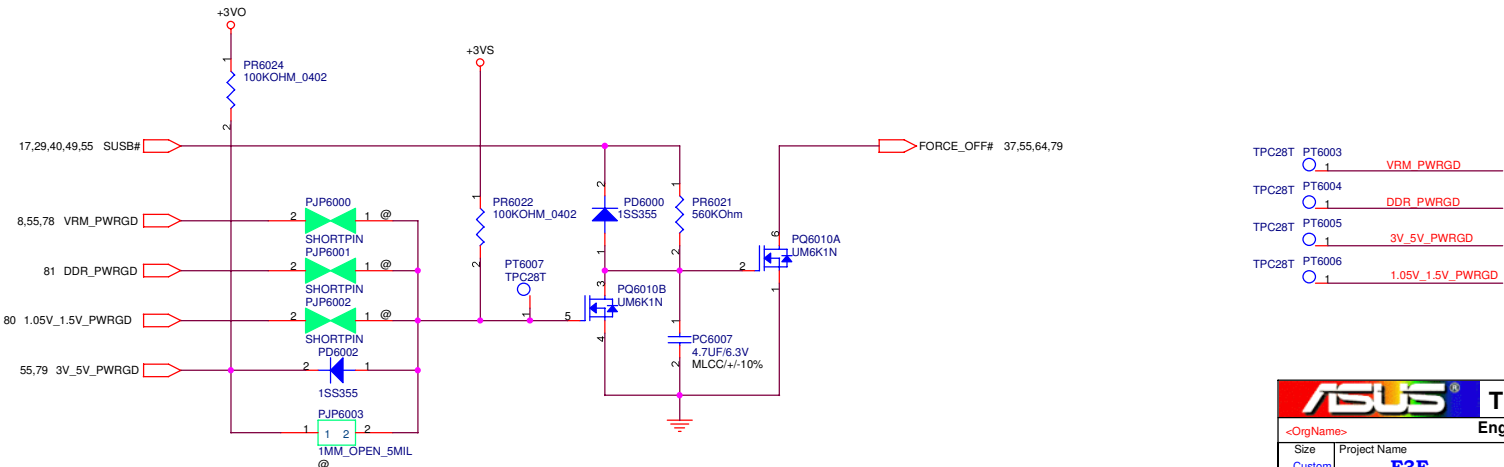
BATTERY A/D_SD# (OVP)

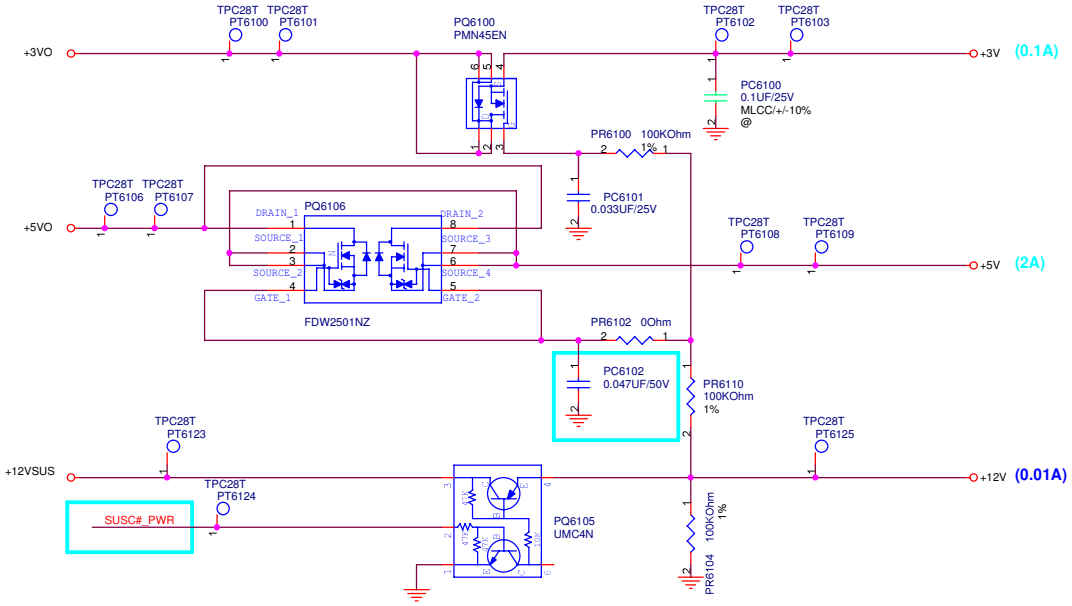


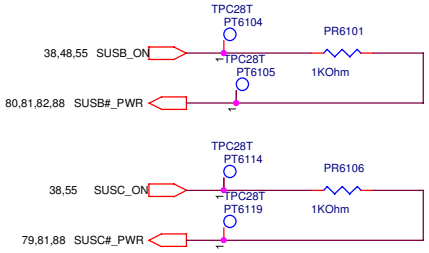
POWER GOOD DETECTER



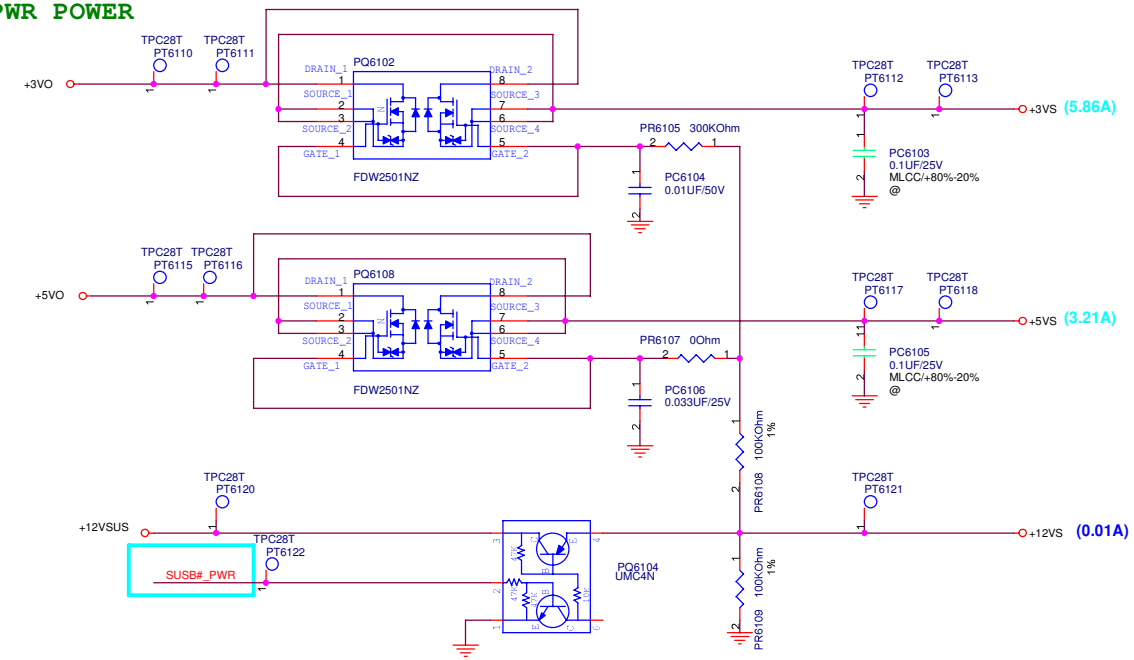
Title : POWER_PROTECT		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 85 of 89	

SUSC#_PWR POWER

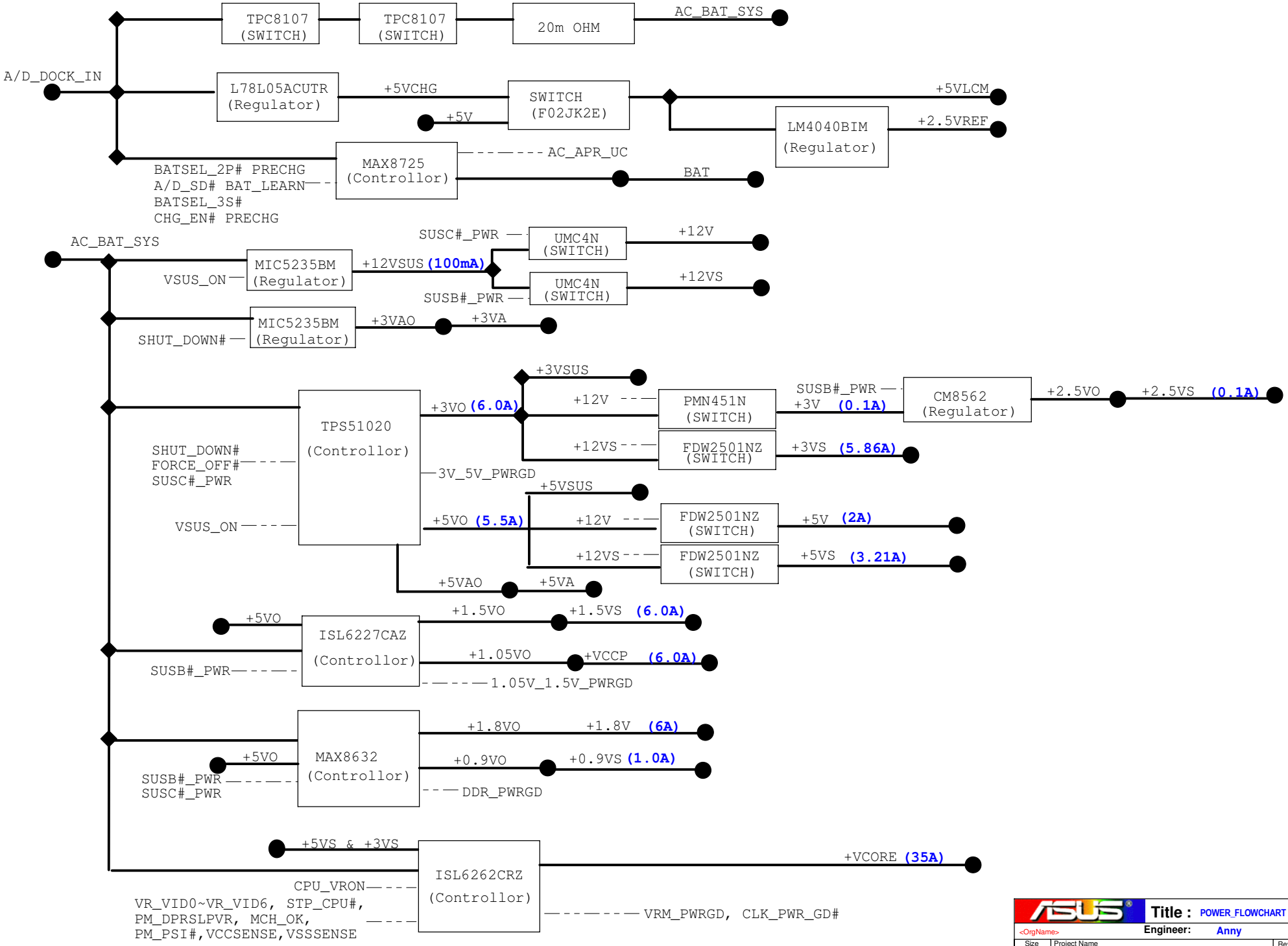




SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 86 of 89	



ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 87 of 89	

AC_BAT_SYS → AC_BAT_SYS 29,64,78,79,80,81,82,83

+3VA → +3VA 15,29,37,38,55,82,84

+5VA → +5VA 26,79,82,85

+5VO → +5VO 79,80,81,86

+3VO → +3VO 79,80,85,86

+3VSUS → +3VSUS 16,17,18,40,41,43,48,79

+5VSUS → +5VSUS 18,26,62,79,85

+3V → +3V 24,26,29,38,41,43,49,50,72,76,82,86

+3VS → +3VS 8,9,12,16,17,18,20,21,24,28,29,31,33,35,38,43,45,46,47,48,49,52,53,55,66,68,72,74,78,80,85,86

+12VSUS → +12VSUS 79,86

+12V → +12V 38,47,53,86

+12VS → +12VS 29,53,62,86

+5V → +5V 12,29,38,45,50,58,84,86

+5VS → +5VS 17,18,24,26,28,33,38,52,53,55,56,62,68,78,86

+2.5VO → +2.5VO 82

+2.5VS → +2.5VS 8,12,28,38,52,82

+1.8VO → +1.8VO 81

+1.8V → +1.8V 8,11,20,21,22,38,49,81

+VCCP → +VCCP 4,7,18,35,38,80

+VCCP_AGTL+ → +VCCP_AGTL+ 4,5,7,12

+VCCP_GMCH → +VCCP_GMCH 7,11

+VCCP_ICH → +VCCP_ICH 15,18

+0.9VS → +0.9VS 22,38,81

BAT → BAT 64,83

+5VCHG → +5VCHG 83,84

+5VLCM → +5VLCM 62,83,84,85

+2.5VREF → +2.5VREF 82,83,84,85

+VCORE → +VCORE 5,78

BAT_CON → BAT_CON 64,83

FOR POWER TEST

+3VA

PJP6300 (SGL_JUMP @) → CPU_VRON_PWR 78

PJP6301 (SGL_JUMP @) → SUSB#_PWR → SUSB#_PWR 80,81,82,86

PJP6302 (SGL_JUMP @) → SUSC#_PWR → SUSC#_PWR 79,81,86

PJP6303 (SGL_JUMP @) → VSUS_ON_PWR → VSUS_ON_PWR 79

1111

Title : POWER_SIGNAL		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: F3F	Rev: 2.1
Date: Thursday, May 25, 2006	Sheet 88 of 89	

Rev	Date	Description
1.0	11/28/2005	1. Initial release.
1.1	01/13/2006	1. For RF Switch disable, BT can't detect by Wireless console issue, add BT detect pin. Page 17,74. 2. Change C676,C677 Package size. Page 41. 3. Fix 1394 connector pin reverse issue. Page 46. 4. Fix Battery connector ping reverse issue. Page 64. 5. Add Capacity CE20, C53, C54, C55, C56, C57, C58, for 3DMark screen become to one color and hang issue. Page 11. 6. Change L51 Package size. Page 29. 7. Change X1 & X6 for cost down. Page 15,55. 8. Remove Fan 3 pin design circuit. Page 33,55. 9. Fix debug connector pin reverse issue. Page 66. 10. Fix LID Switch can't disable backlight issue, change NB BL_EN net name to BKLTEN. Page 9,29. 11. Fix VSUS_ON_PWR and SUSC#PWR Net connect issue. Page 88. 12. Remove Cardbus PME signal for R5C832. Page 45. 13. Add AC Adaptor Voltage Error Signal to EC, and EC will show the abnormal by LED. Page 55. 14. Remove L107,D37,CE17,CE18 for cost down. Page 58. 15. Change Connector CON15,J2,CON11,CON17,CON27,CON22&CON7&CON8,J3&J4. Page 28,53,41,48,68,31,22,64. 16. Modify Audio schematic Change C578,C579 to 0.47UF and remove R403,R404,R405,R398,R399,R408,R409,R410,C603,C604. Page 52,53. 17. Change R351 to 22 ohm. Page 15. 18. Add C59 for EMI. Page 47. 19. Charger circuit add component. Page 83. 20. Change TPLED_ON GPIO pin from GPIO19 to GPIO14 and R55 10K ohm pull low. Page 17. 21. Depop circuit remove OP_SD# control function. Page 53,55. 22. Add Mic. Preamplifer circuit. Page 52. 23. Change CE9,CE10 position for pop noise. Page 53. 24. Add buffer U5 for HSYNC and VSYNC of CRT signal. Page 9,28. 25. Add RN28,R156 near debug connector to be LPC terminal resistor. Page 66. 26. Change R233,R234,R235,R236 to L107,L108,L109,L110 for EMI. Page 53.
2.0		1. Colay Audio circuit for STAC9200 and ALC660. Remove Mic. Pre-Amplifer circuit. Page 52,53. 2. Modify minicard latch connector to nut.(H57,H58) Page 43. 3. Change SATA Connector. Page 68. 4. Add +3V LDO circuit for TV_DAC Power. Page 12.

Rev	Date	Description
		5. Remove R96,R97,R524 for Fan circuit. Page 33. 6.Add some test point for factory request. 7.Change BT_ON# from SB GPIO to EC GPIOE7. Page 17,55. 8.Add MOS for EC leakage of electricity issue.Page 55. 9.Change BT logic power from +3VS to +3V for WHQL S3 test .Page 76. 10.For Lan -ve test issue,add terminal resistor near the transformer .Page 41. 11.For ACZ RST will let Sigmatel codec GPIO0 high issue, add C177 to deplay depop time to avoid pop from speaker .Page 53.
2.1	04/24/2006	1.Change internal Mic. bias voltage from +5V_AUDIO to +2.5VS. Page 52. 2.Add D52,D53 to protect EC. Page 55. 3.Add C178,C179 for new card clock. Page 48. 4.Add H1,H2 for Fan. Page 70. 5.Remove RN2,RN3 for Vcore VID. ESD Request. Page 5. 6.Add R87 for moat issue. Page 53.

ASUSTek COMPUTER INC

Title : History

Engineer: Frank Wang

Size	Project Name	Rev
Custom	F3F	2.1

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