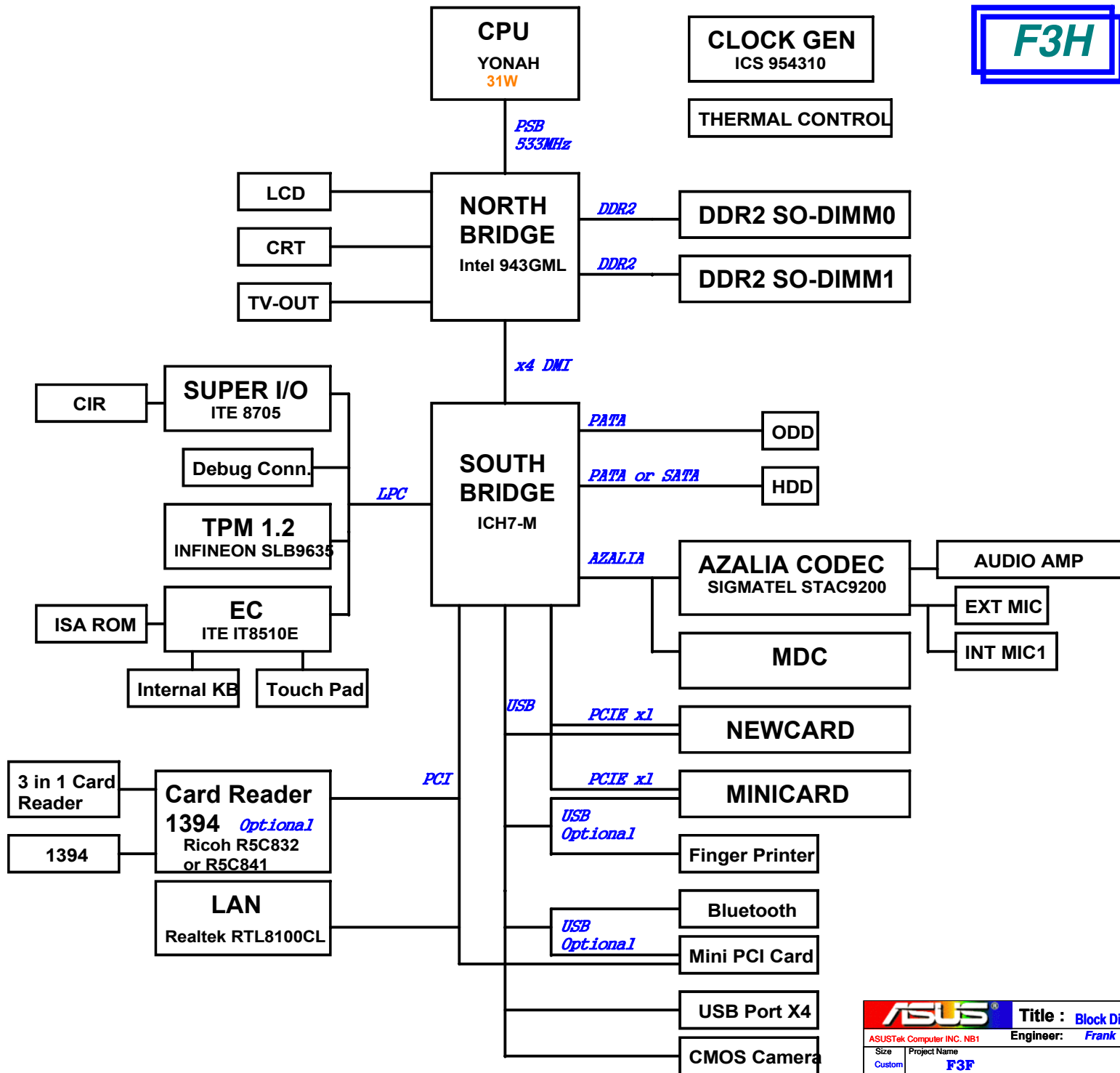


		Title : <u>Block Diagram</u>	
ASUSTek Computer INC. NB1		Engineer: <u>Frank Wang</u>	
Size <u>Custom</u>	Project Name F3F	Rev 2.3	
Date: 星期日 一月 04, 2007		Sheet	1 of 89



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	/	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSC#//GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	BT_ON#	O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

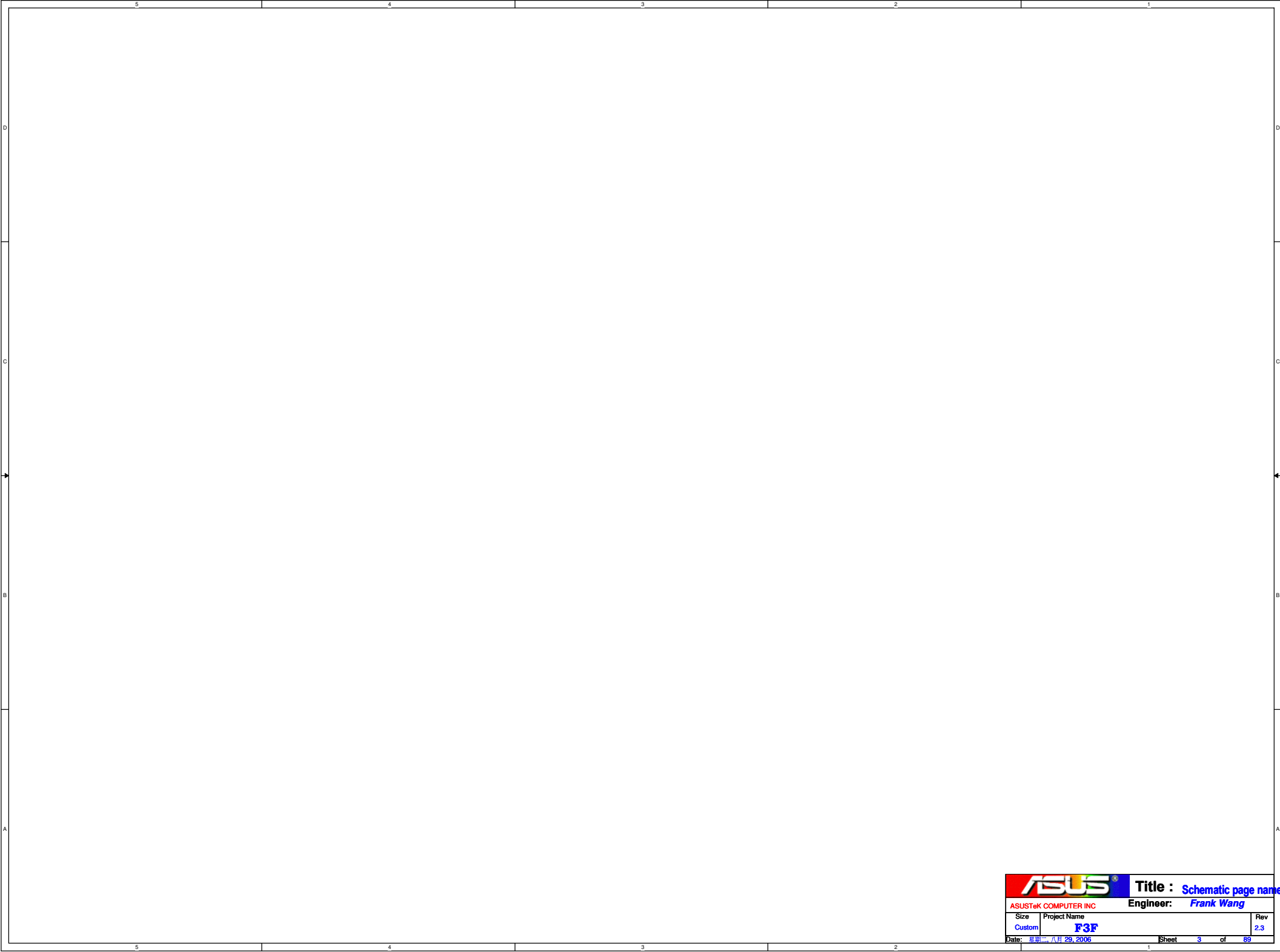
Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

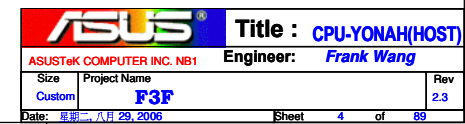
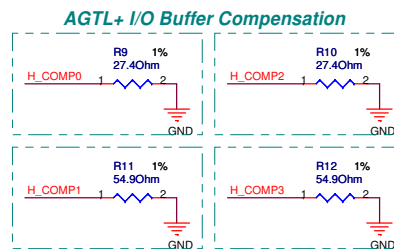
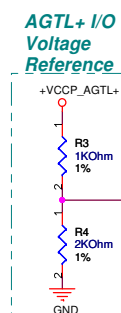
ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BTLED_ON	O
AC18	GPIO07	WLAN_LED_EN	O
E21	GPIO08	EXTSMI#	I
E20	GPIO09	/	
A20	GPIO10	WLAN_ON#	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	CB_SD#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	TP_LEDON	O
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	CPU_SELECT	O
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	/	
A21	GPIO26/EL_RSVD	/	
B21	GPIO27/EL_STATE0	BT_DET#	
E23	GPIO28/EL_STATE1	/	
C3	GPIO29/OC#5	USB_OC#5	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC#7	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	PANEL_ID0	I
AH19	GPIO36/SATA2GP	PANEL_ID1	I
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	C
R5C832 CARD READER	AD17	0	C
R5C832 1394	AD17	0	B
R5C841 CARD READER	AD18	1	C
R5C841 1394	AD18	1	B
Mini PCI Card	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)



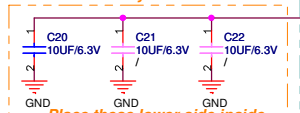
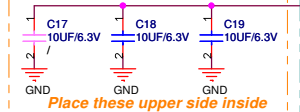
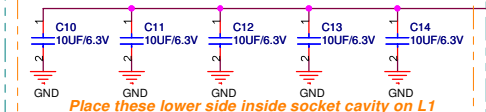
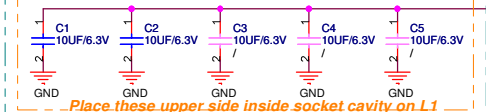


**CPU +VCCORE
Bulk-Decoupling
Capacitors**

+VCCORE

CE19
220UF/4V

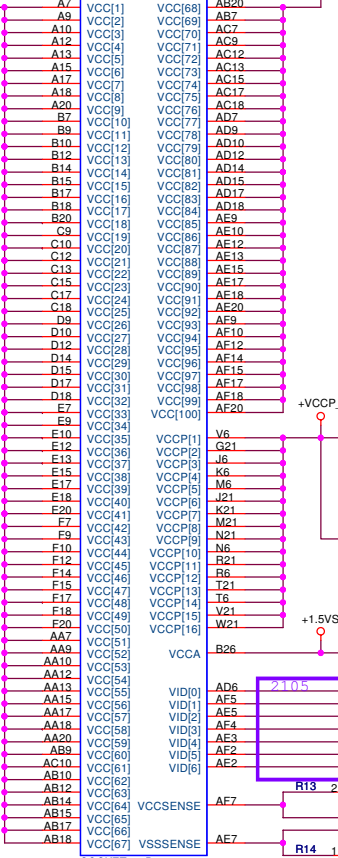
**CPU +VCCORE
Mid-Frequency
Capacitors**



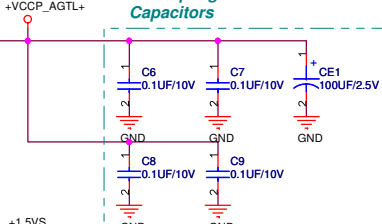
+VCCORE Mid-Frequency Capacitor
Intel: 22UF *32
R1F: 10UF *16

+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4

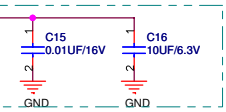
U1C



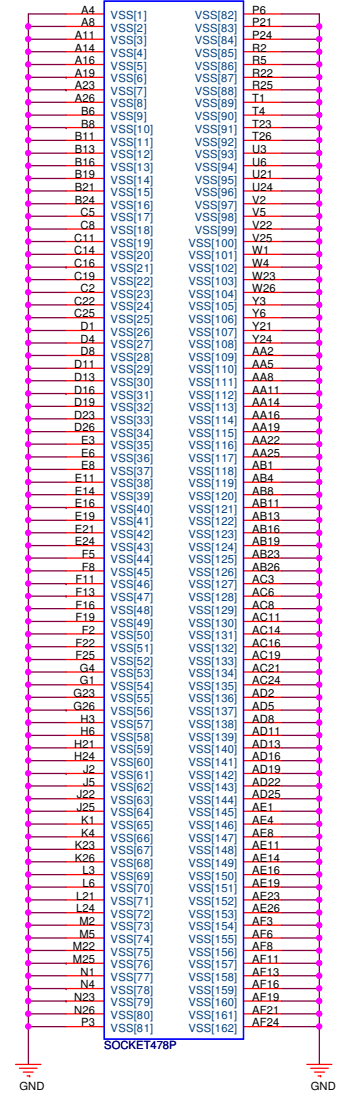
**CPU +VCCP
Decoupling
Capacitors**

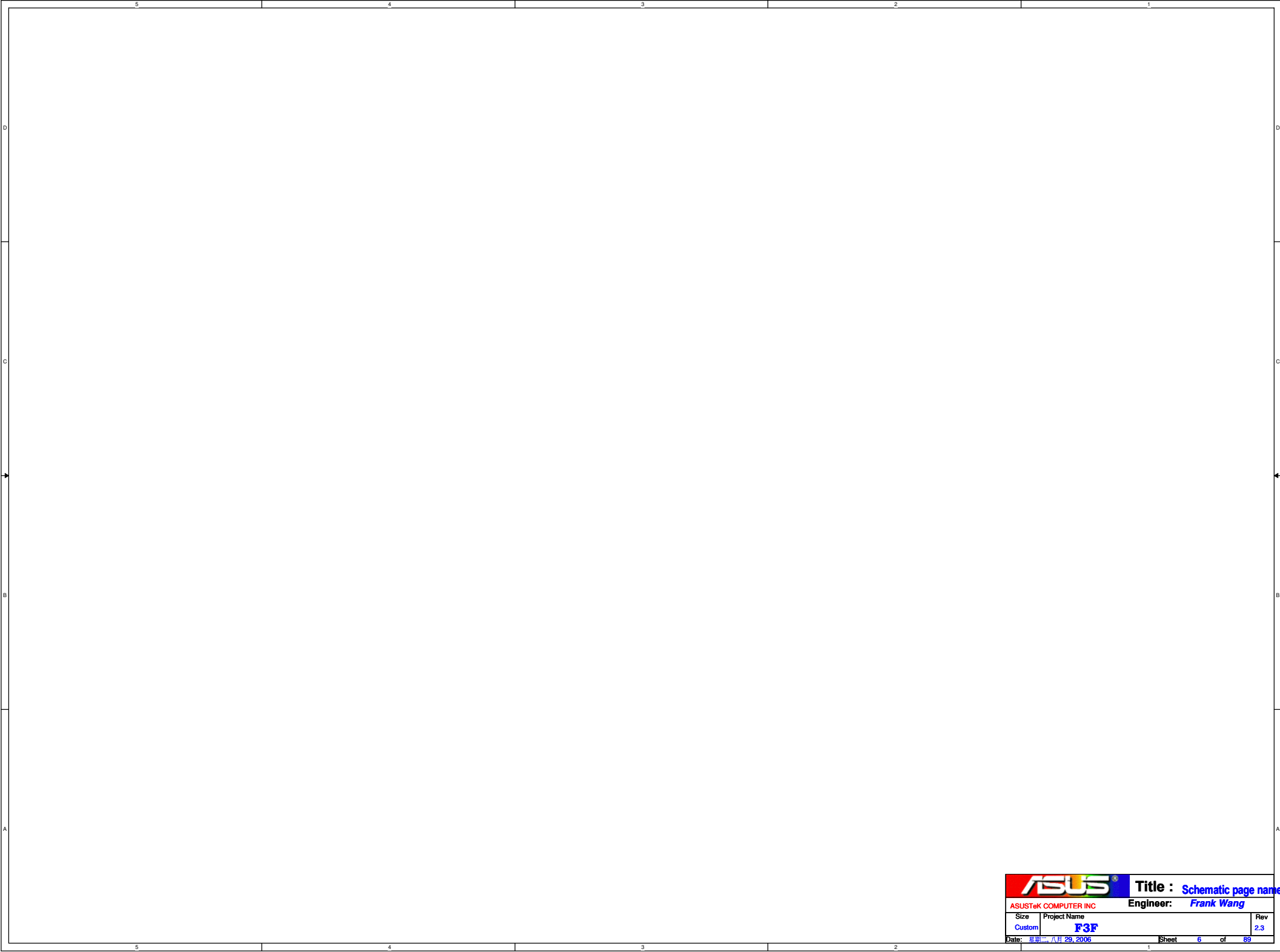


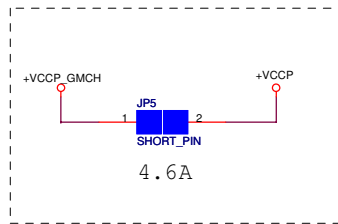
**CPU +VCCA
Decoupling
Capacitors**



U1D







RCOMP

For Calibrating the FSB I/O Buffer



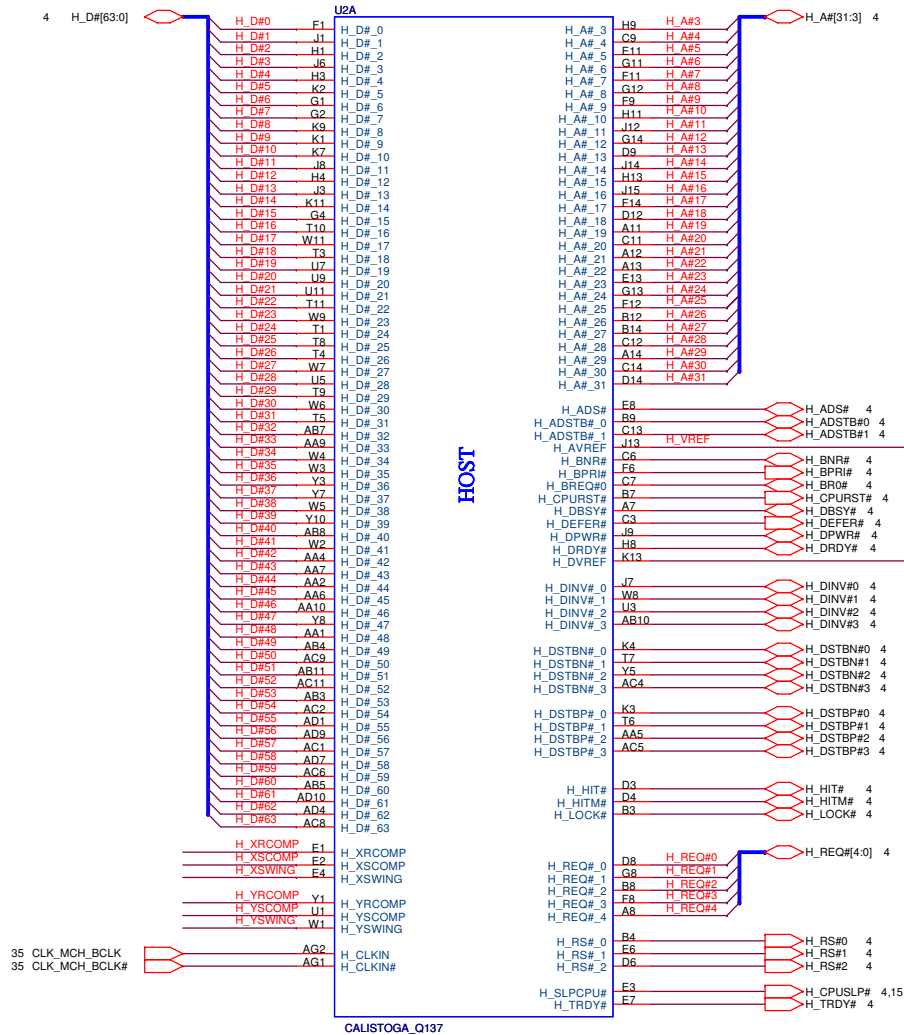
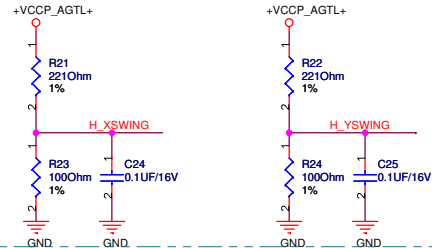
SCOMP

For Slew Rate Compensation on the FSB

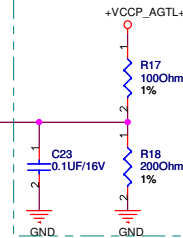


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



AGTL+ I/O Voltage Reference



GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)



CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU
1 = Mobile CPU (D)



CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)



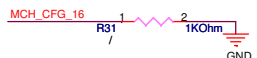
CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)



CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)



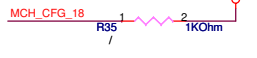
CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)



CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V



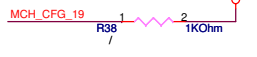
CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)



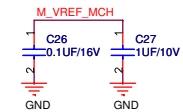
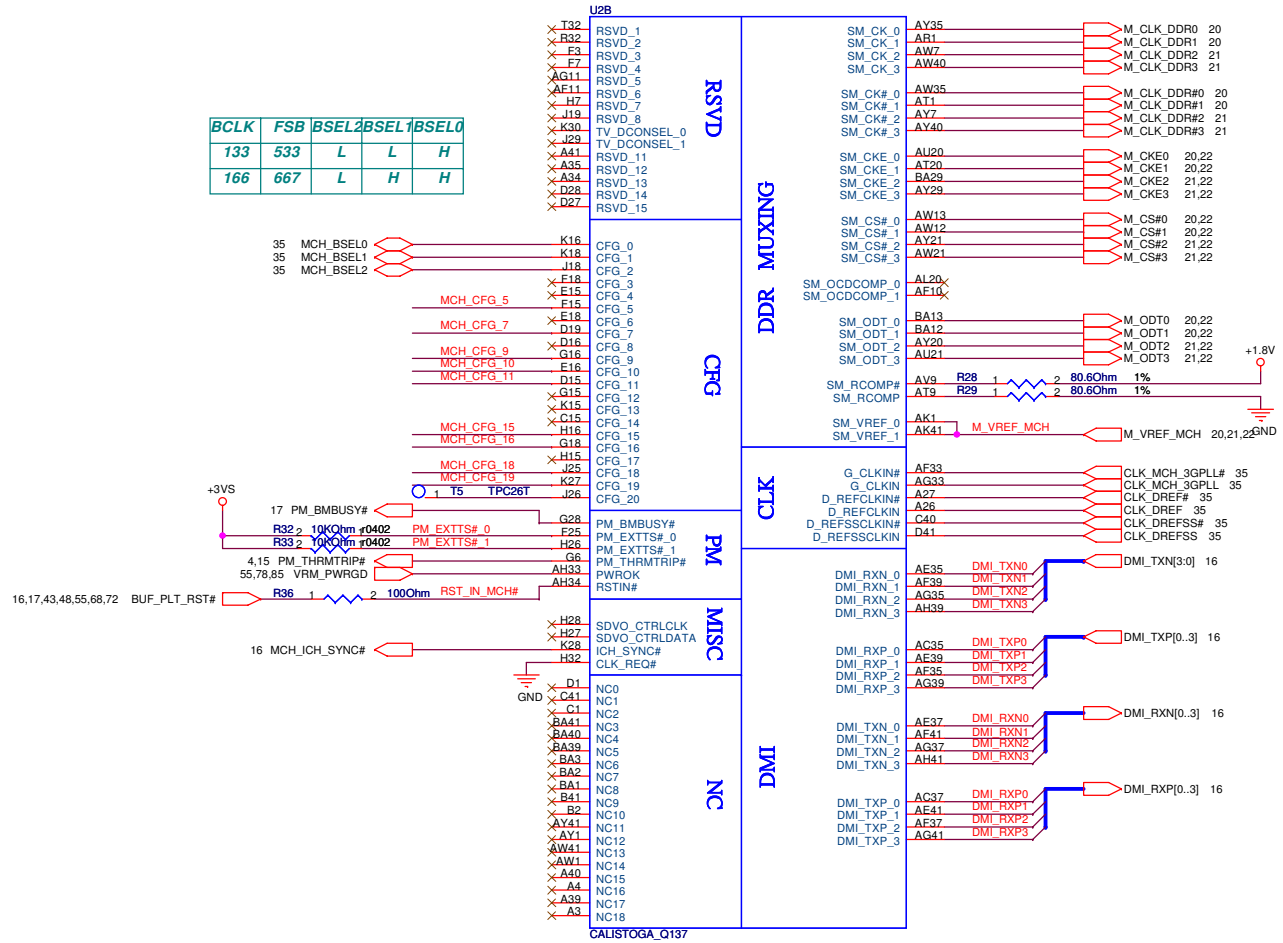
CFG19 : DMI Lane Reversal

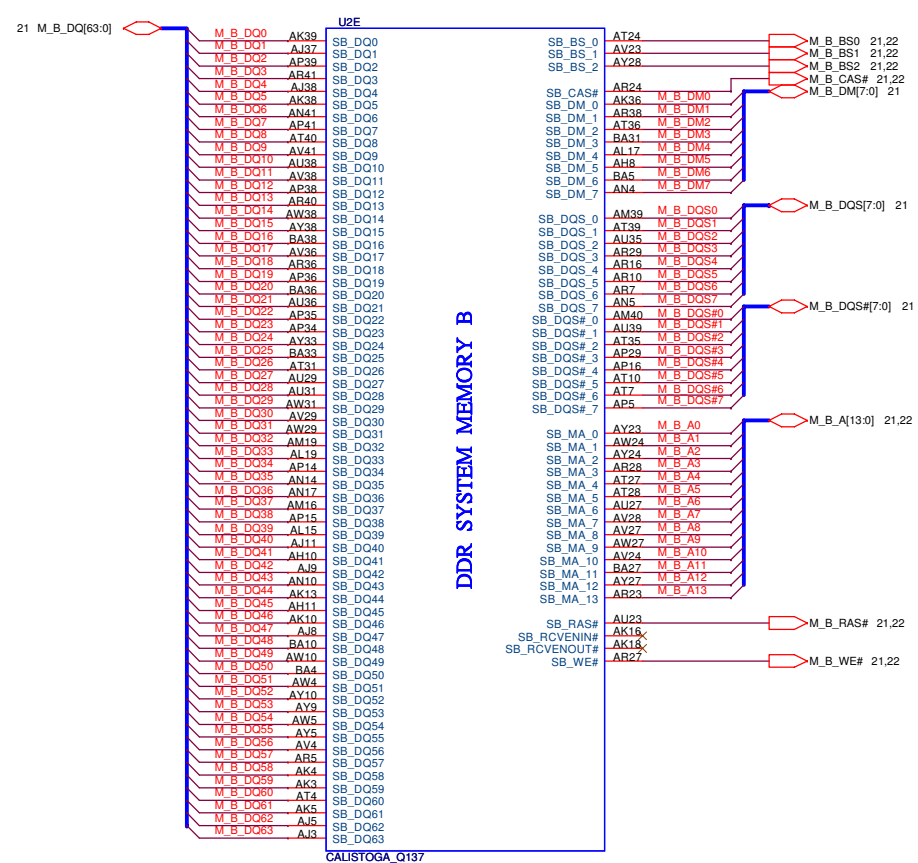
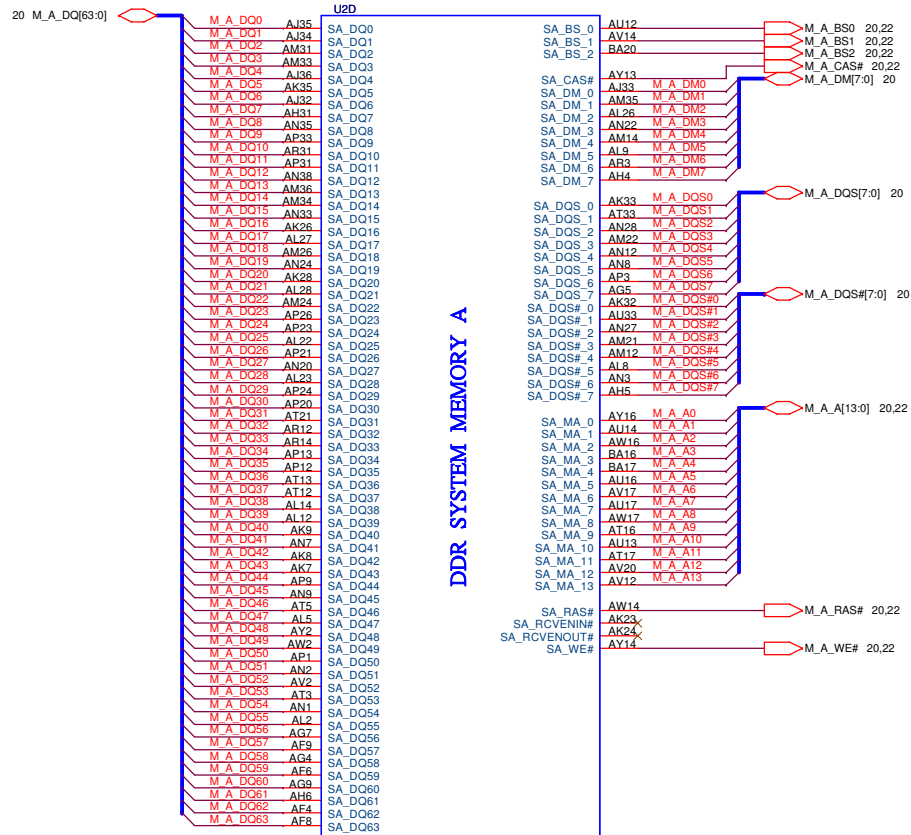
0 = Normal Operation (D)
1 = Lanes Reversed

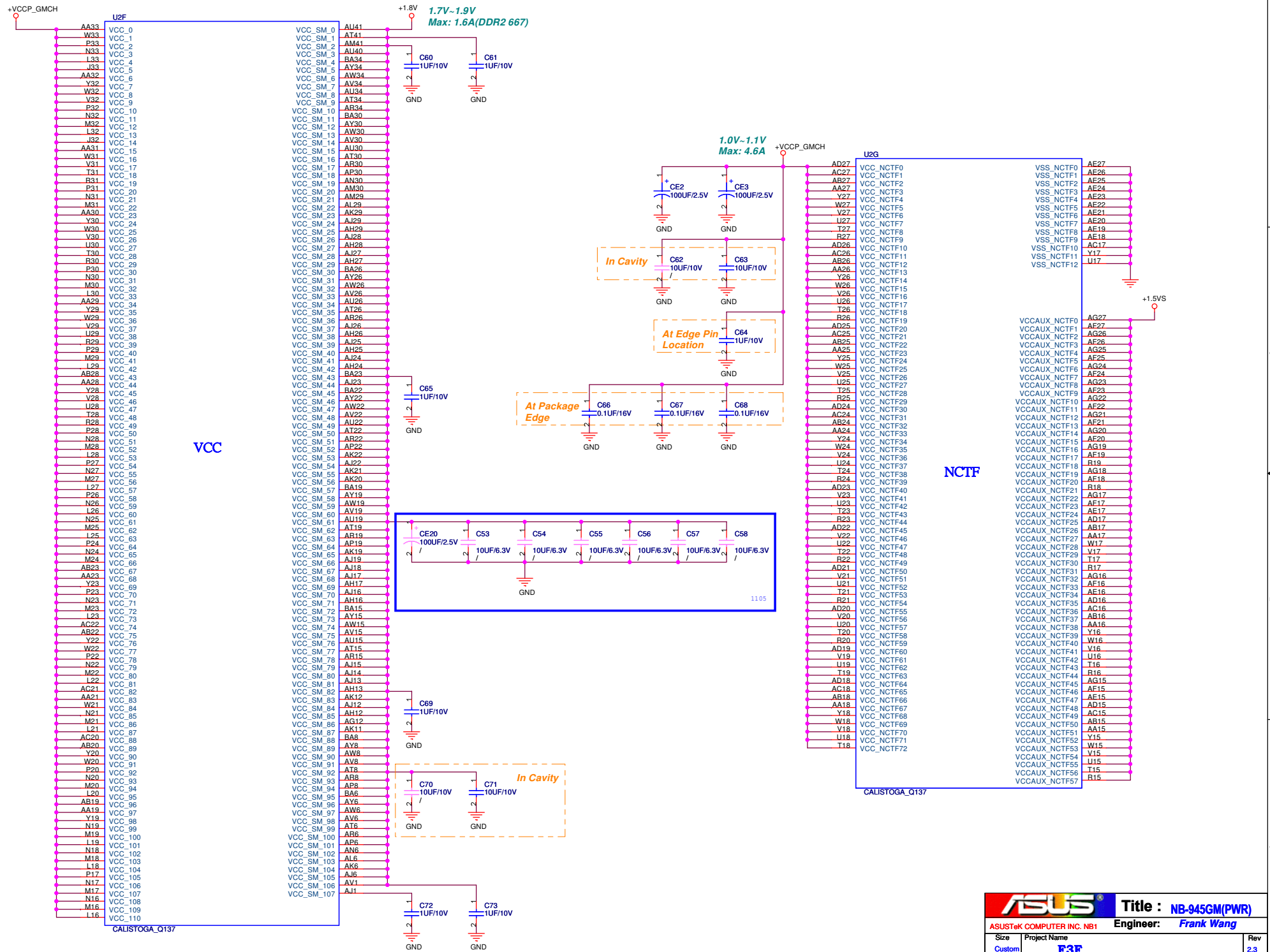


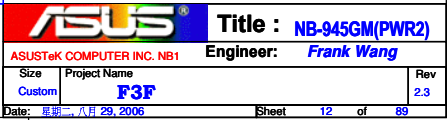
Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

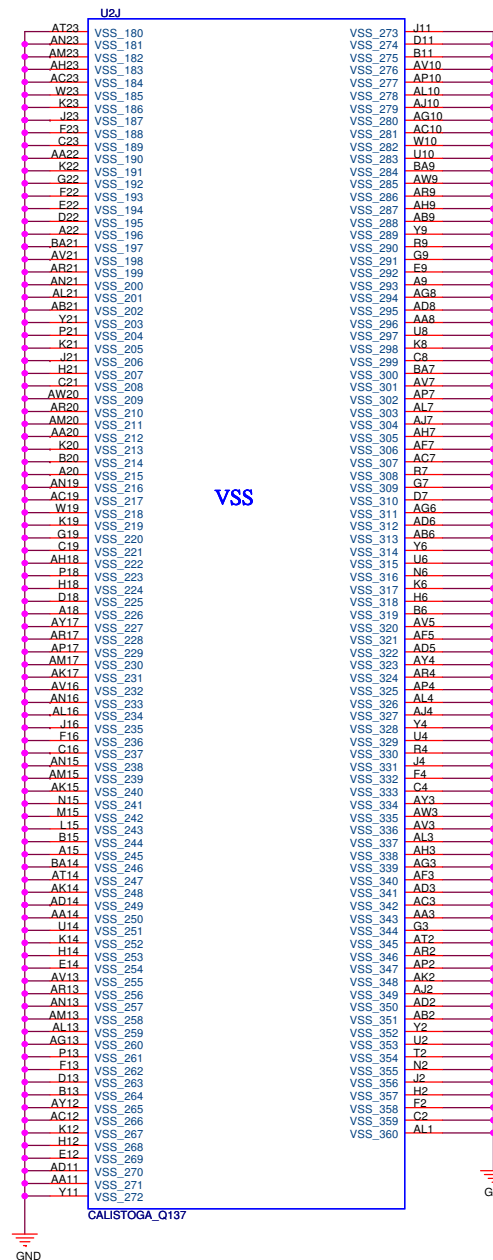
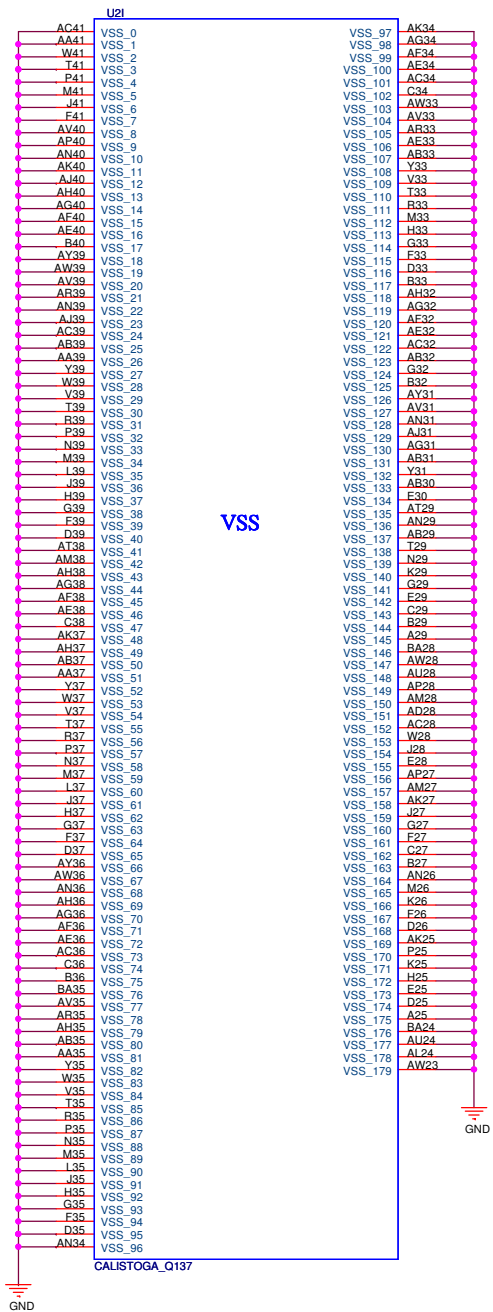
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

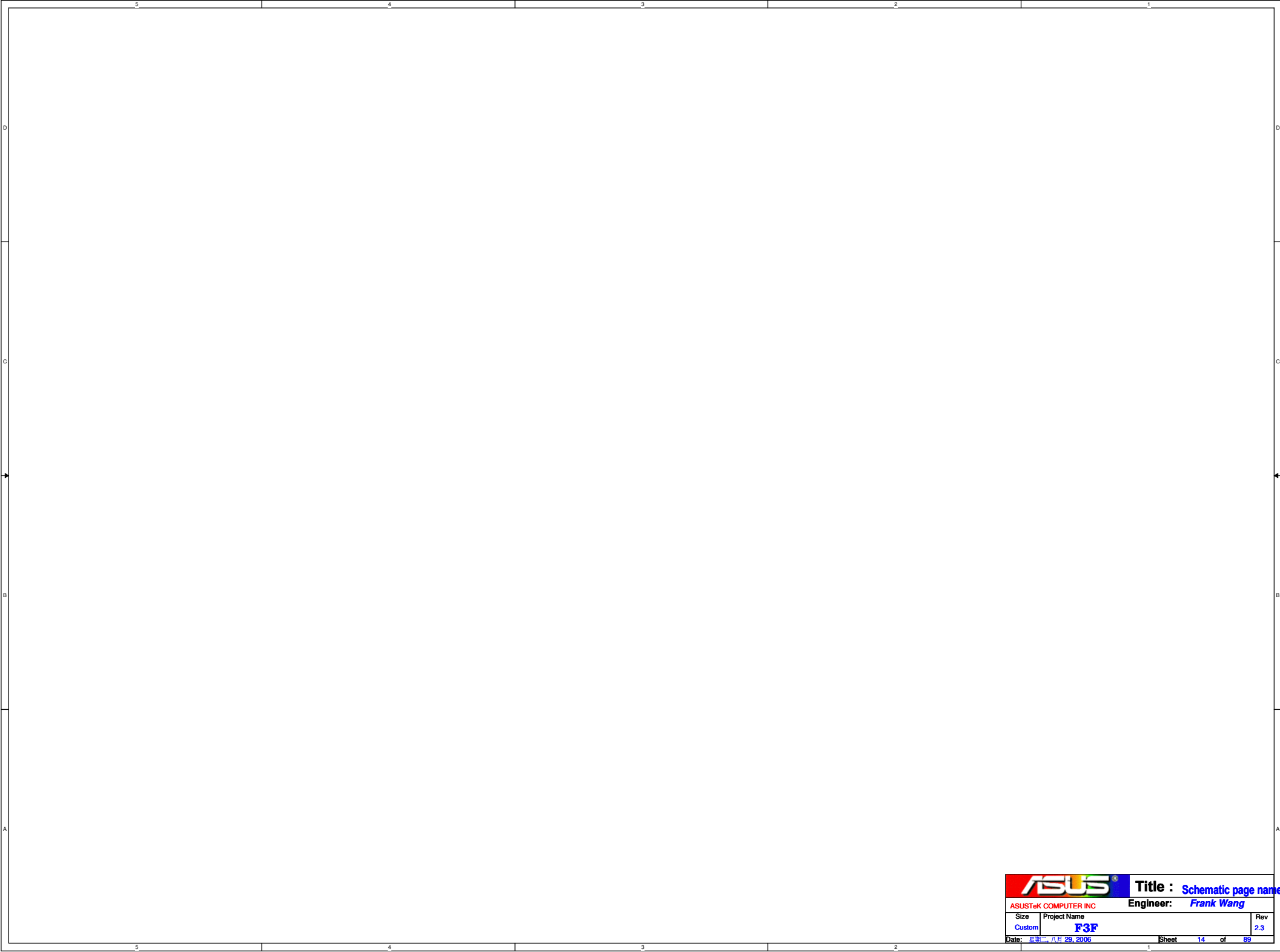


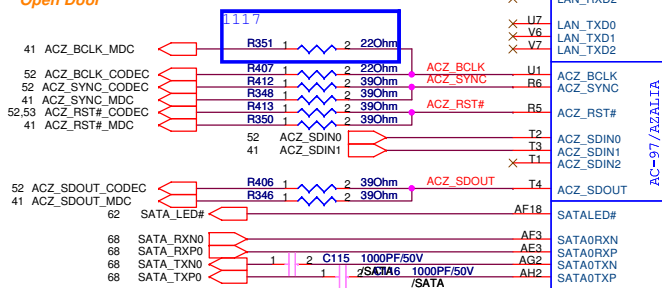
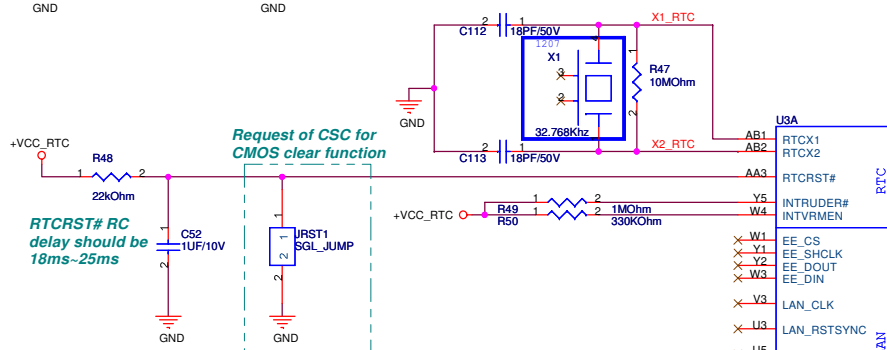
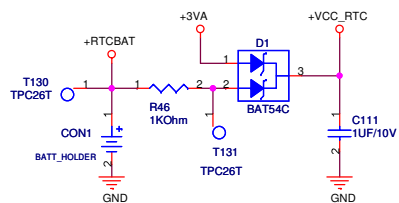




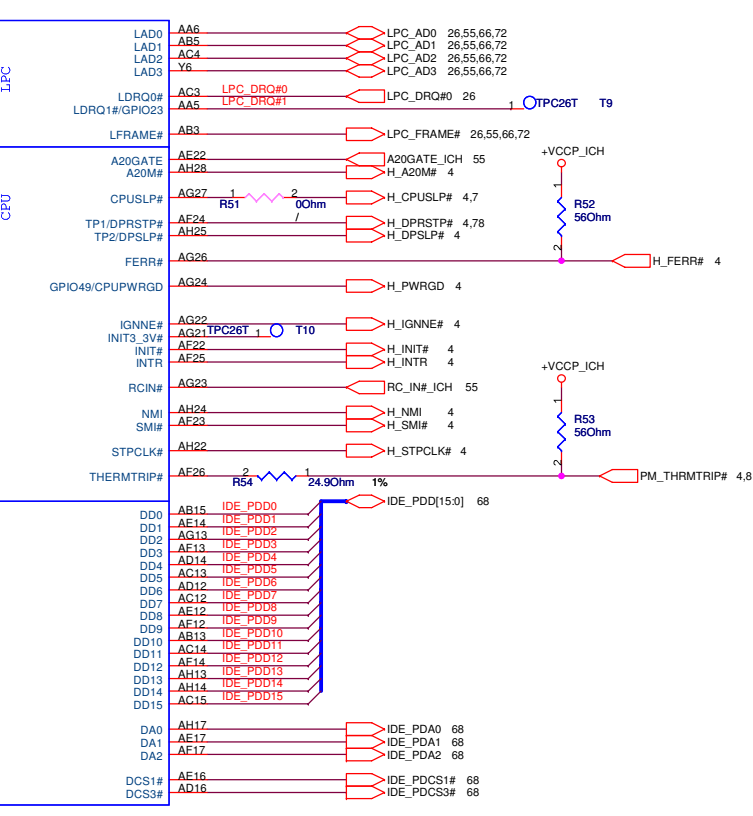
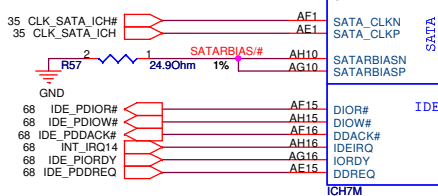


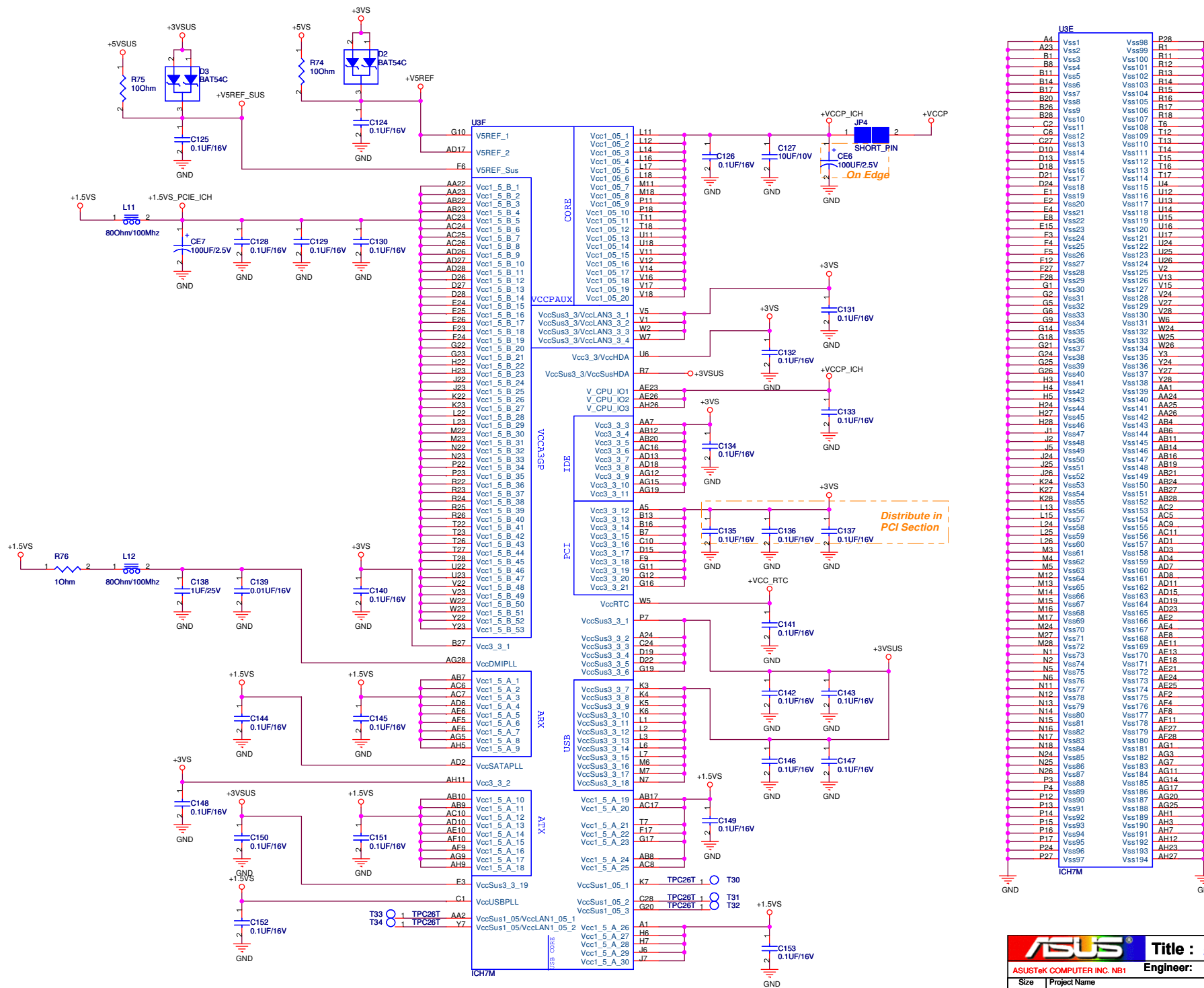


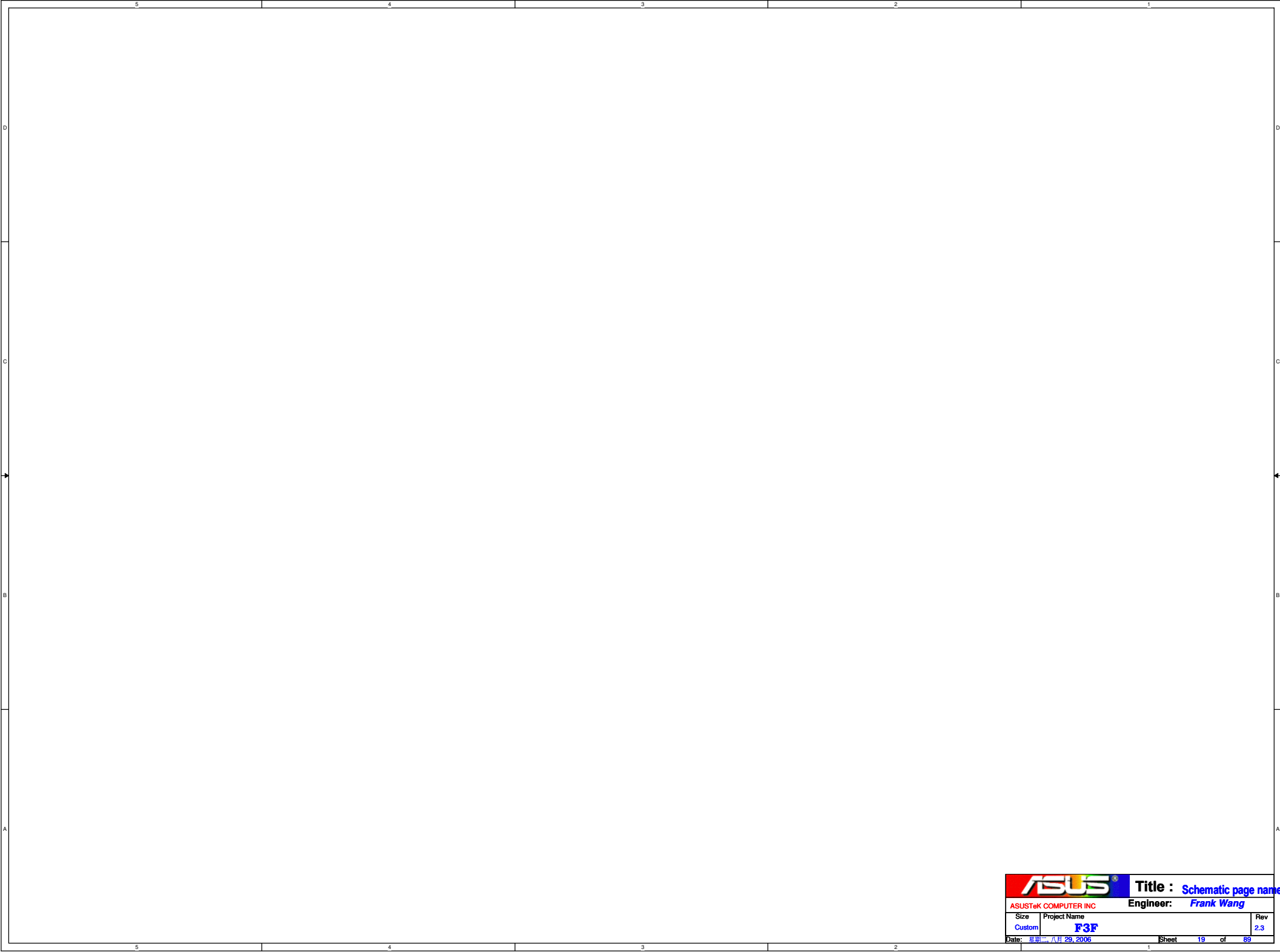




ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM



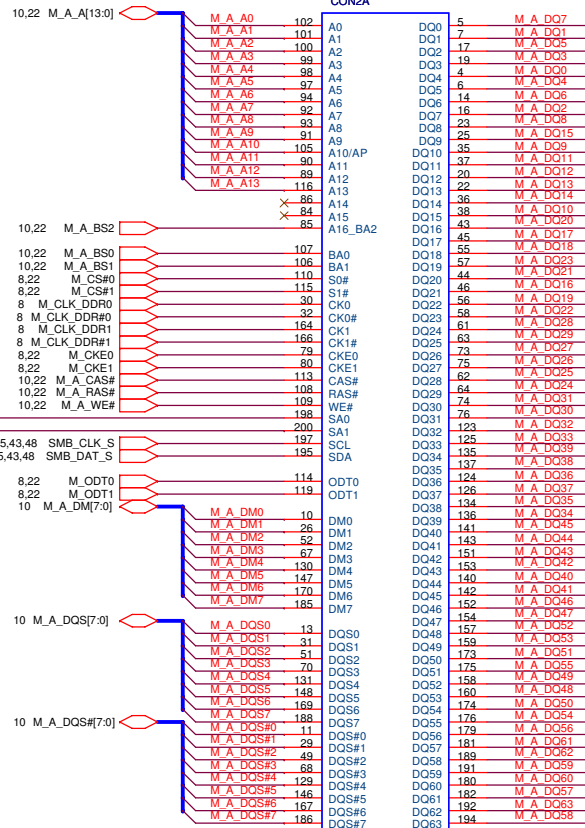




REV Type

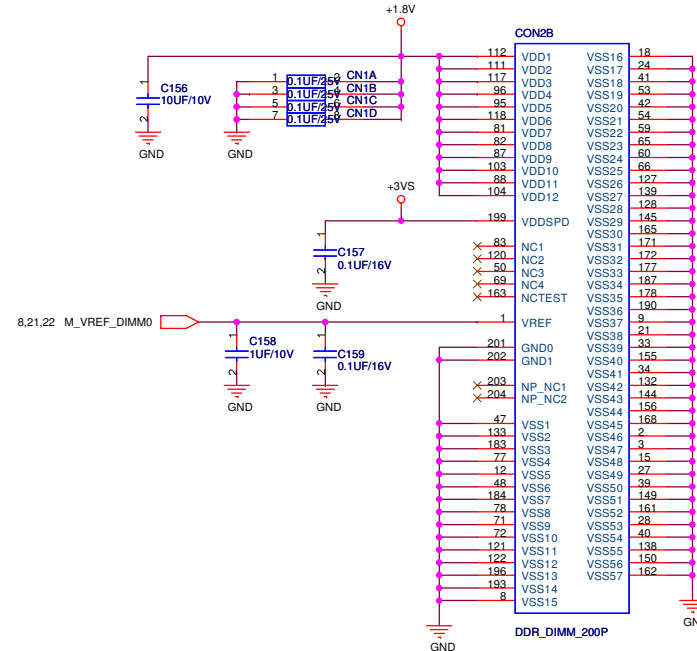
M_A_DQ[63:0] 10

CON2A

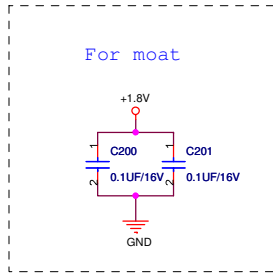
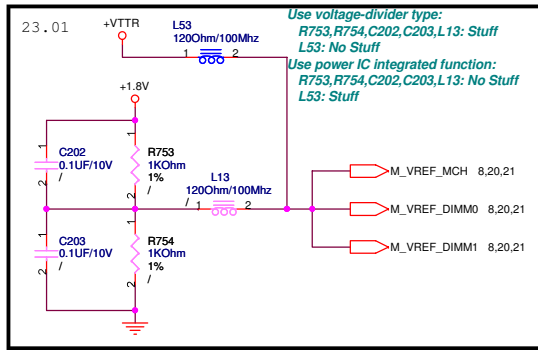


DDR_DIMM_200P

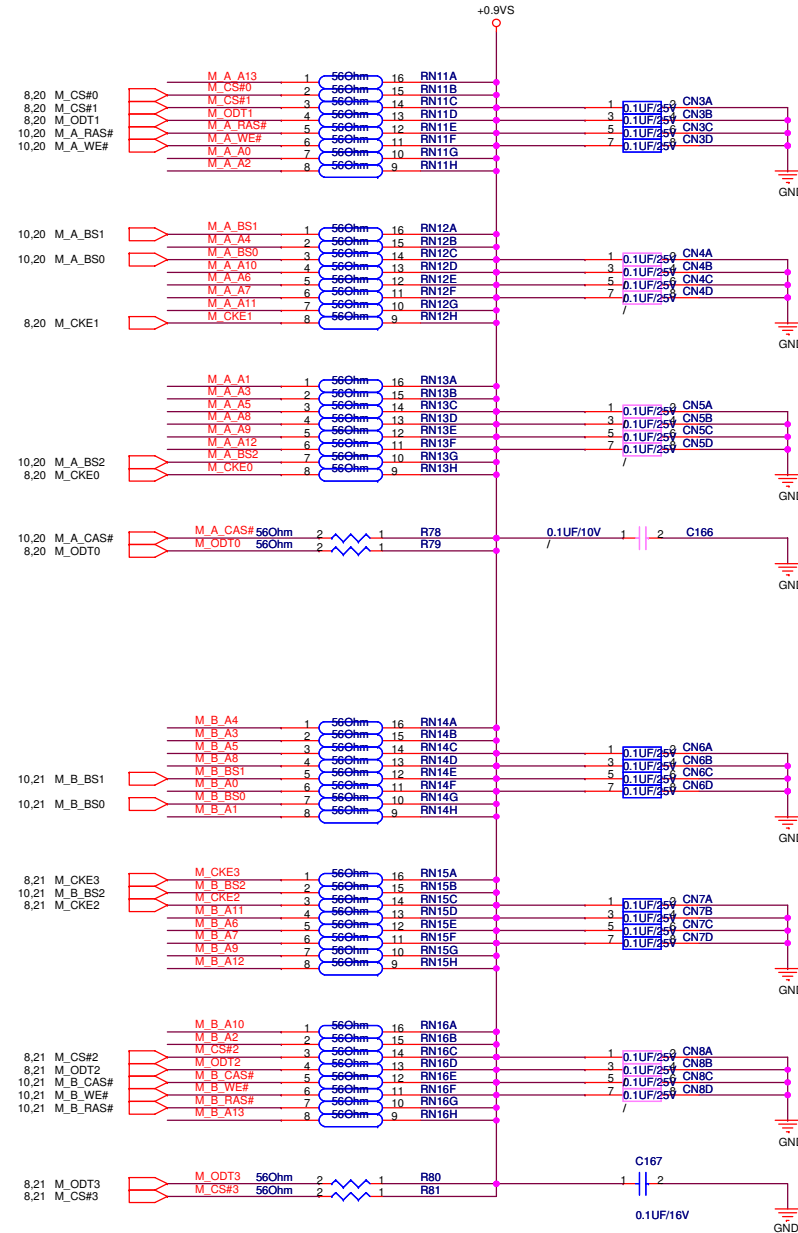
CON2B

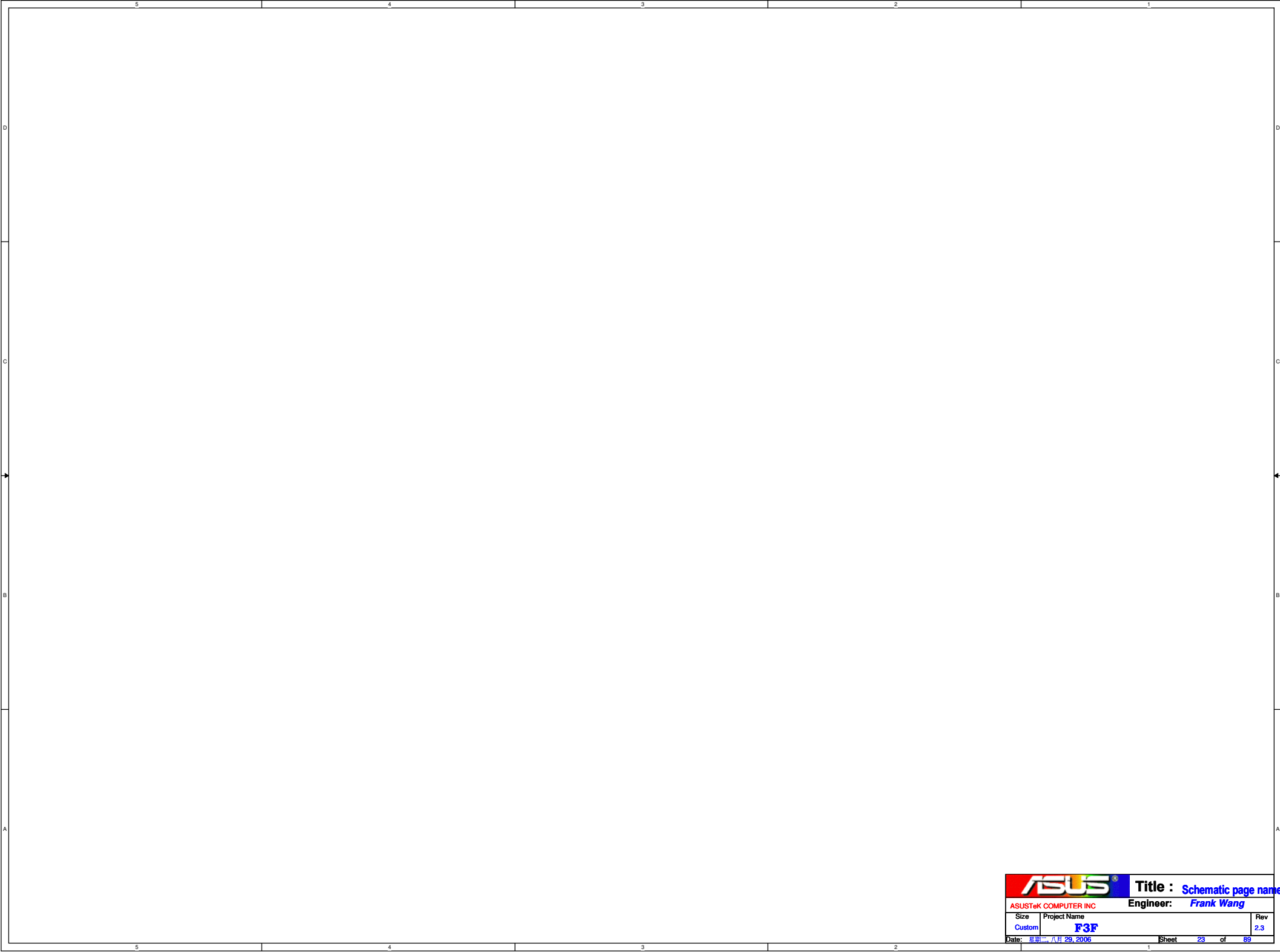


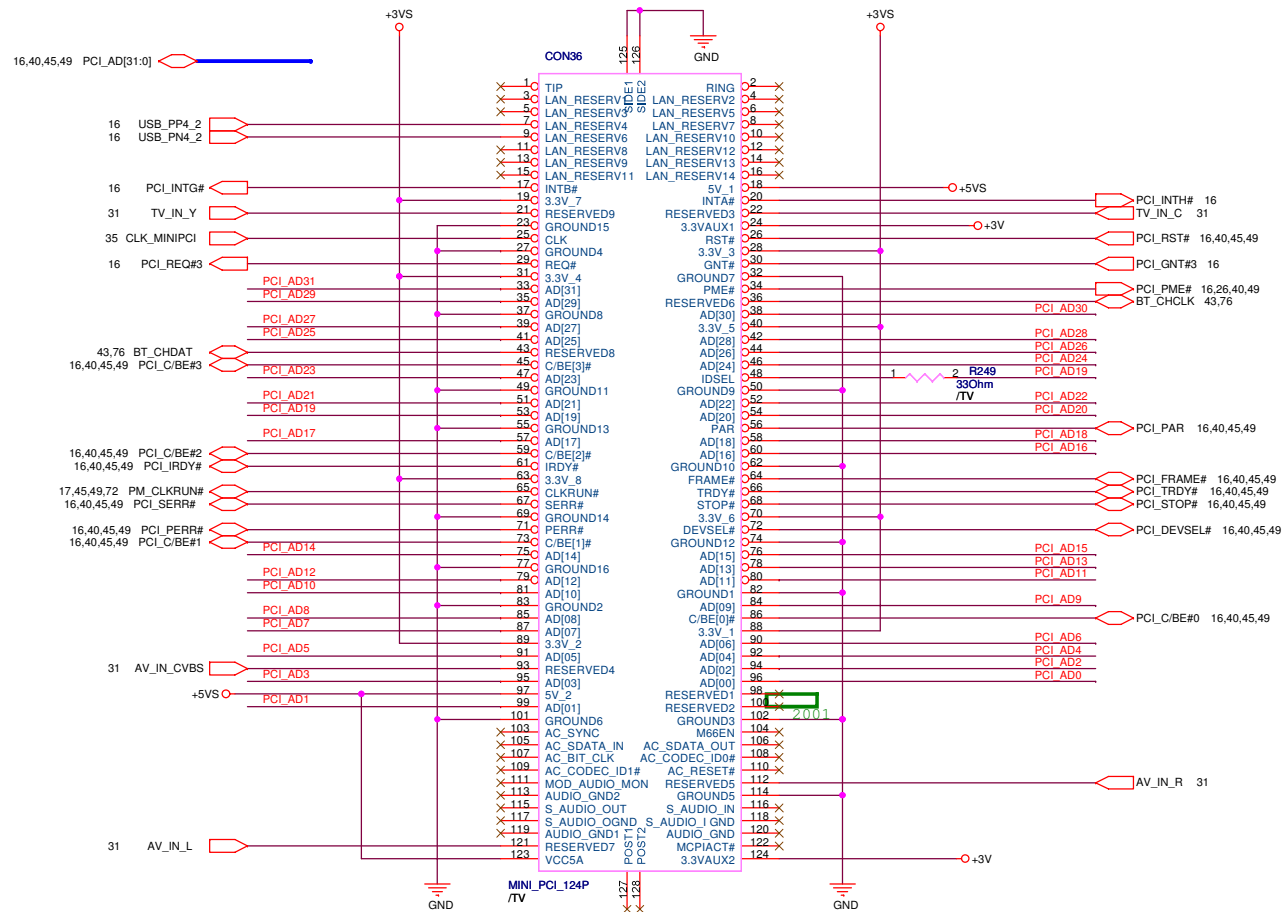
DDR_DIMM_200P



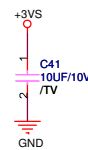
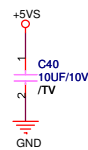
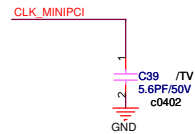
10,20 M_A_A[13:0]
10,21 M_B_A[13:0]



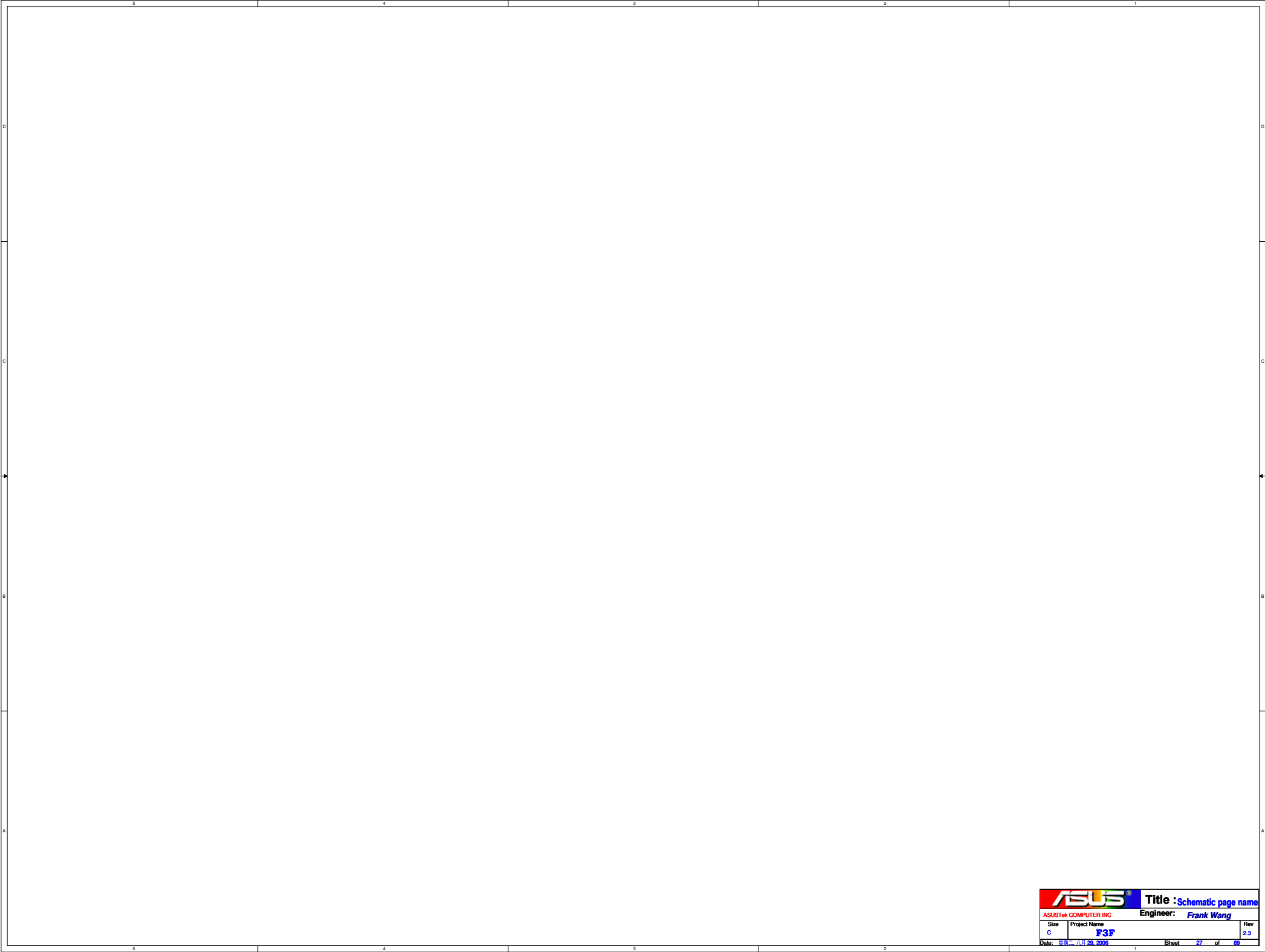




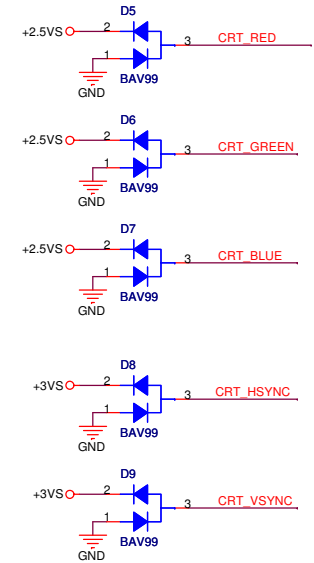
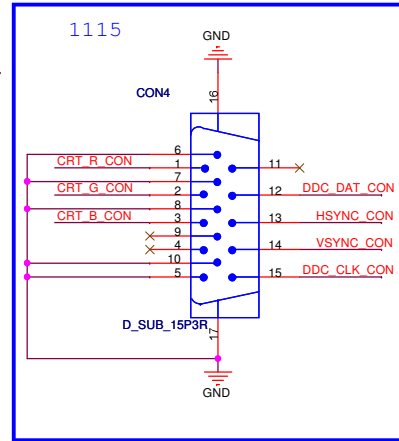
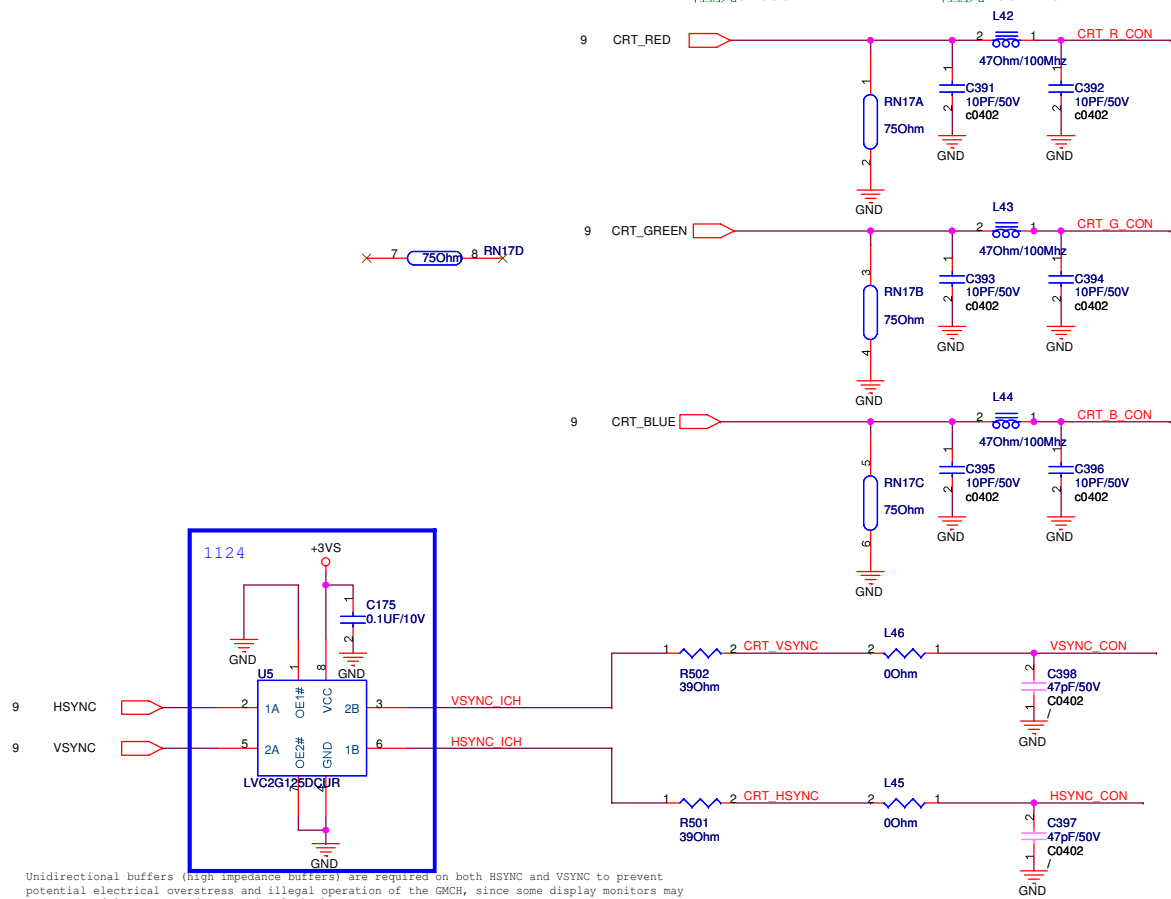
FOR TV TUNER



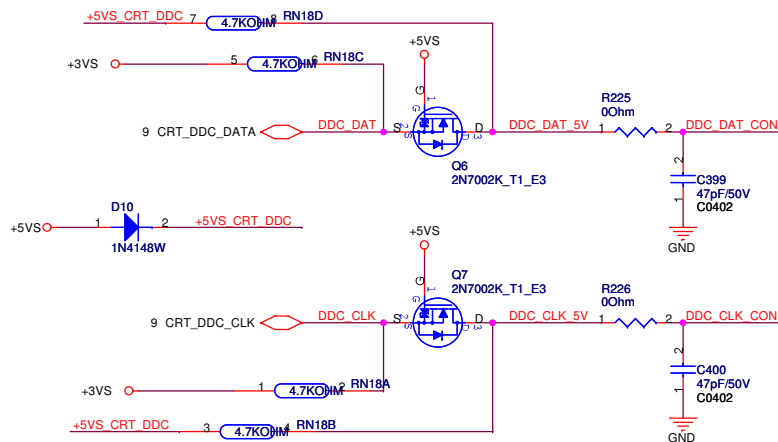
E	D	C	B	A
D				D
C				C
B				B
A				A
E	D	C	B	A



阻抗37.5Ohm <== ==> 阻抗75Ohm OR W= 4 mil

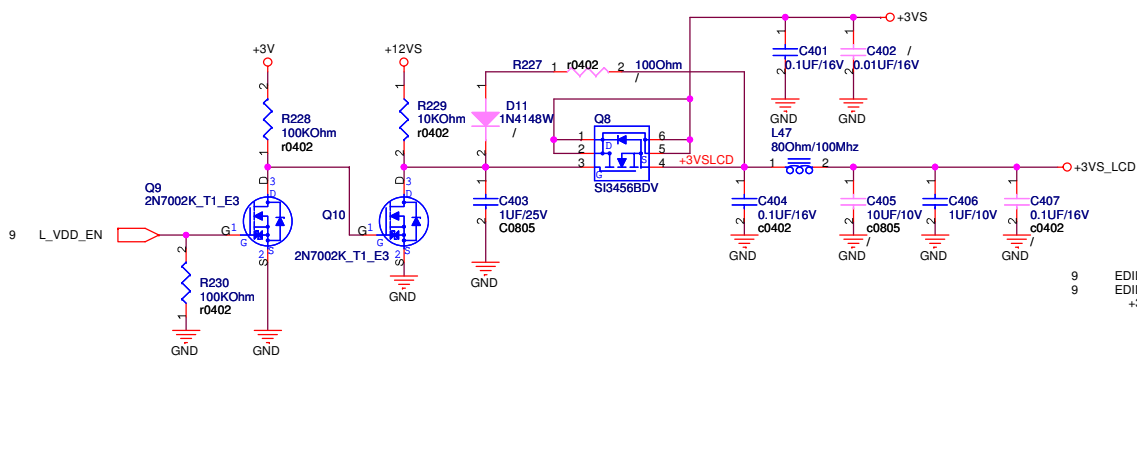


PLACE ESD Diodes near VGA port



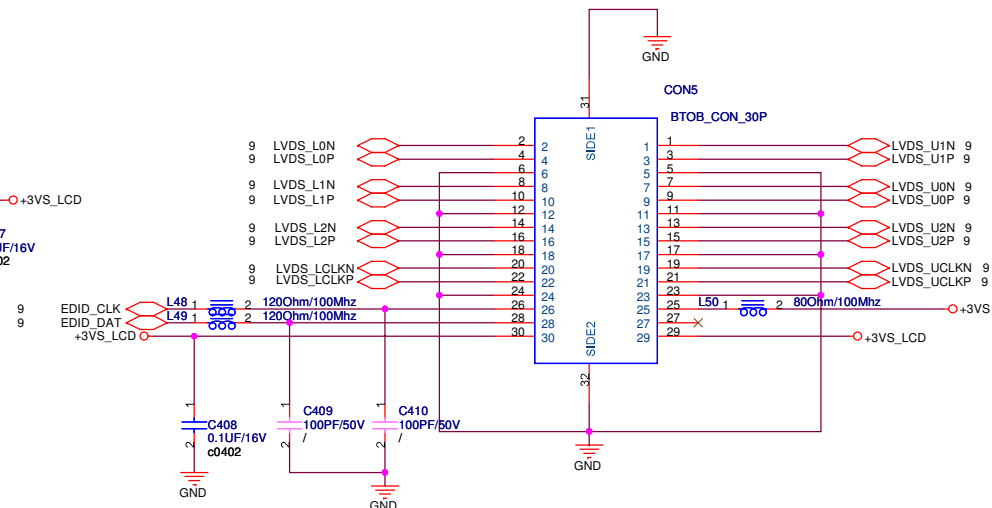
LCD Backlight Control

LCD Power



LCD LVDS Interface

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



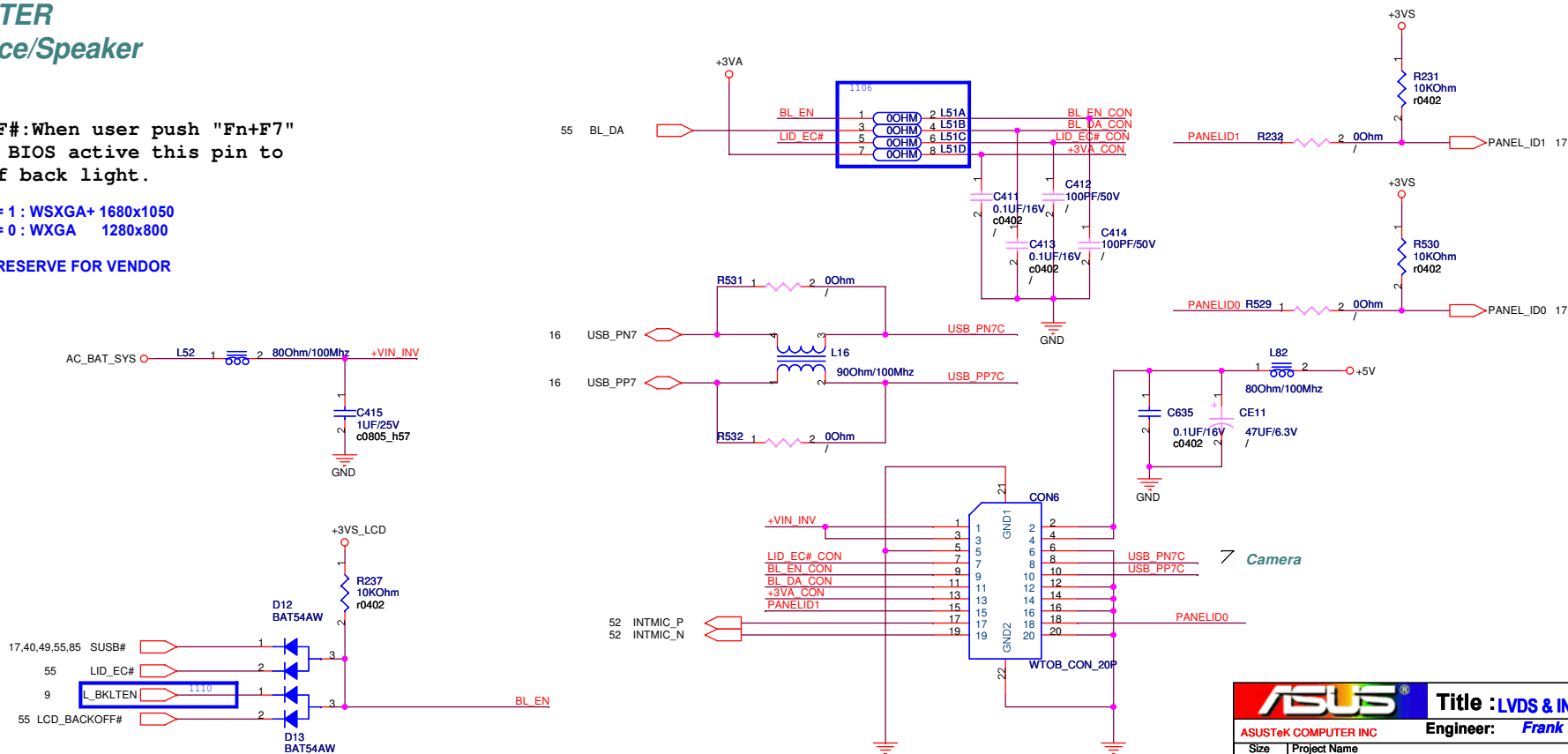
INVERTER
Interface/Speaker
CONN.

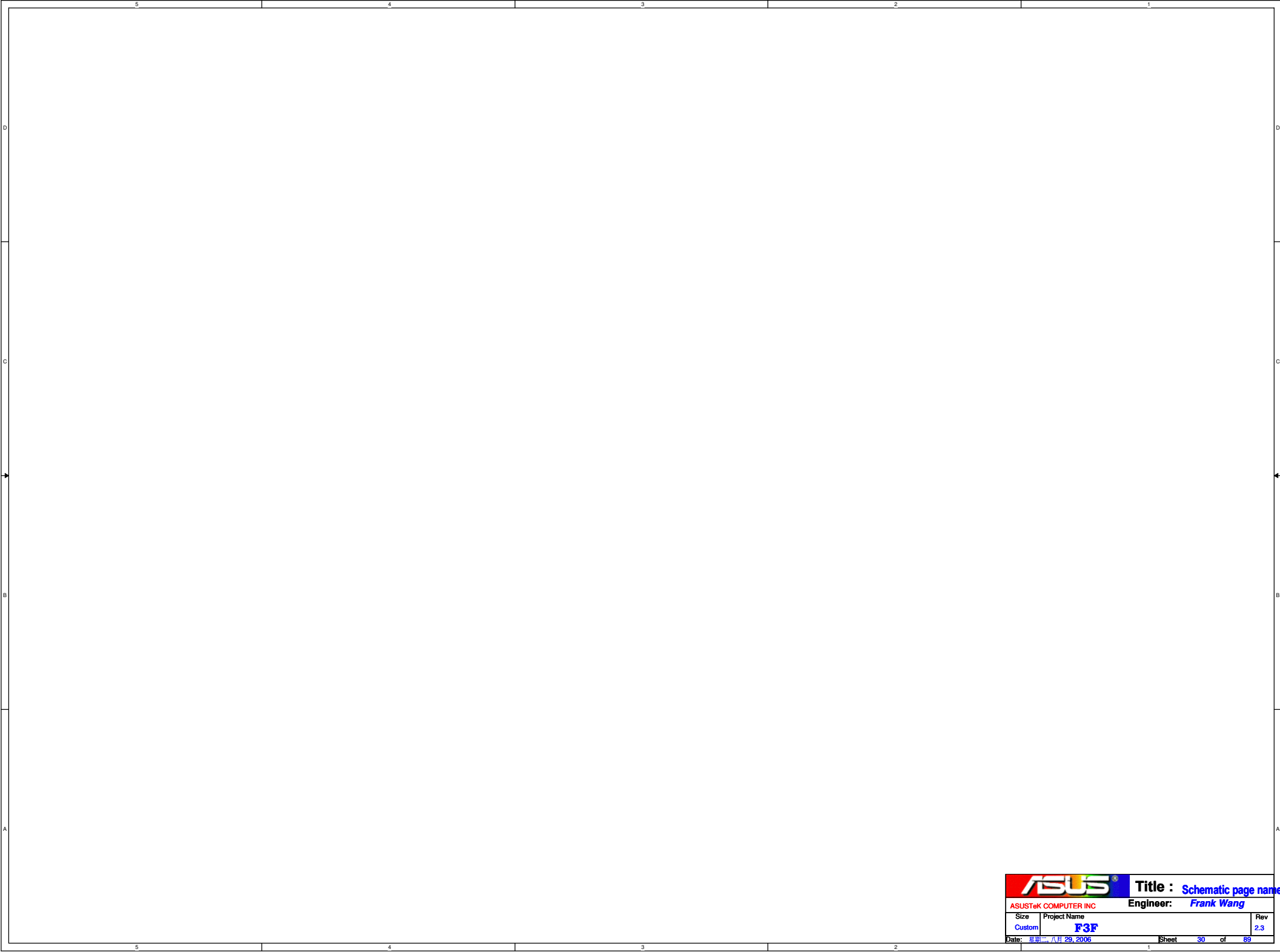
BIOS

BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

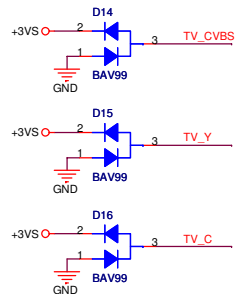
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR

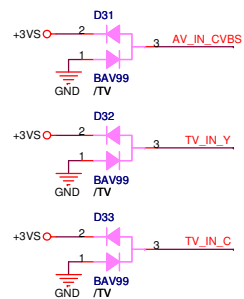
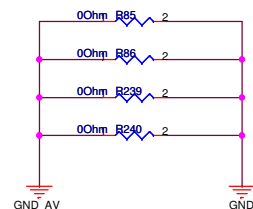




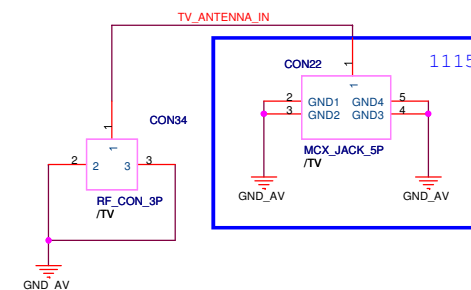
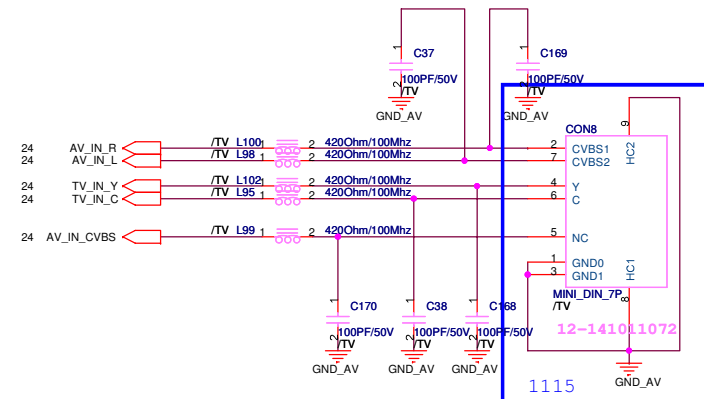
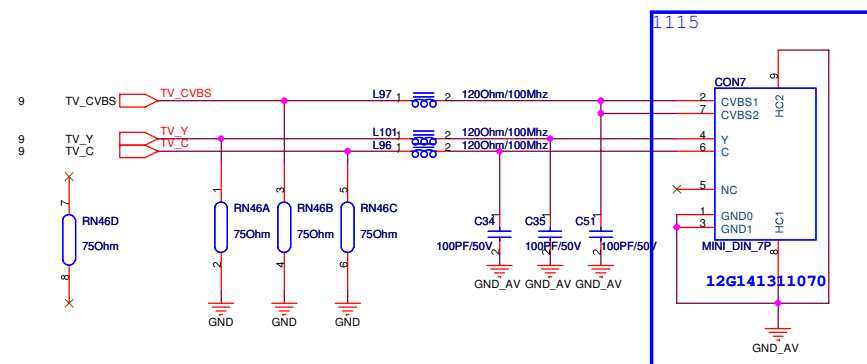
TV OUT

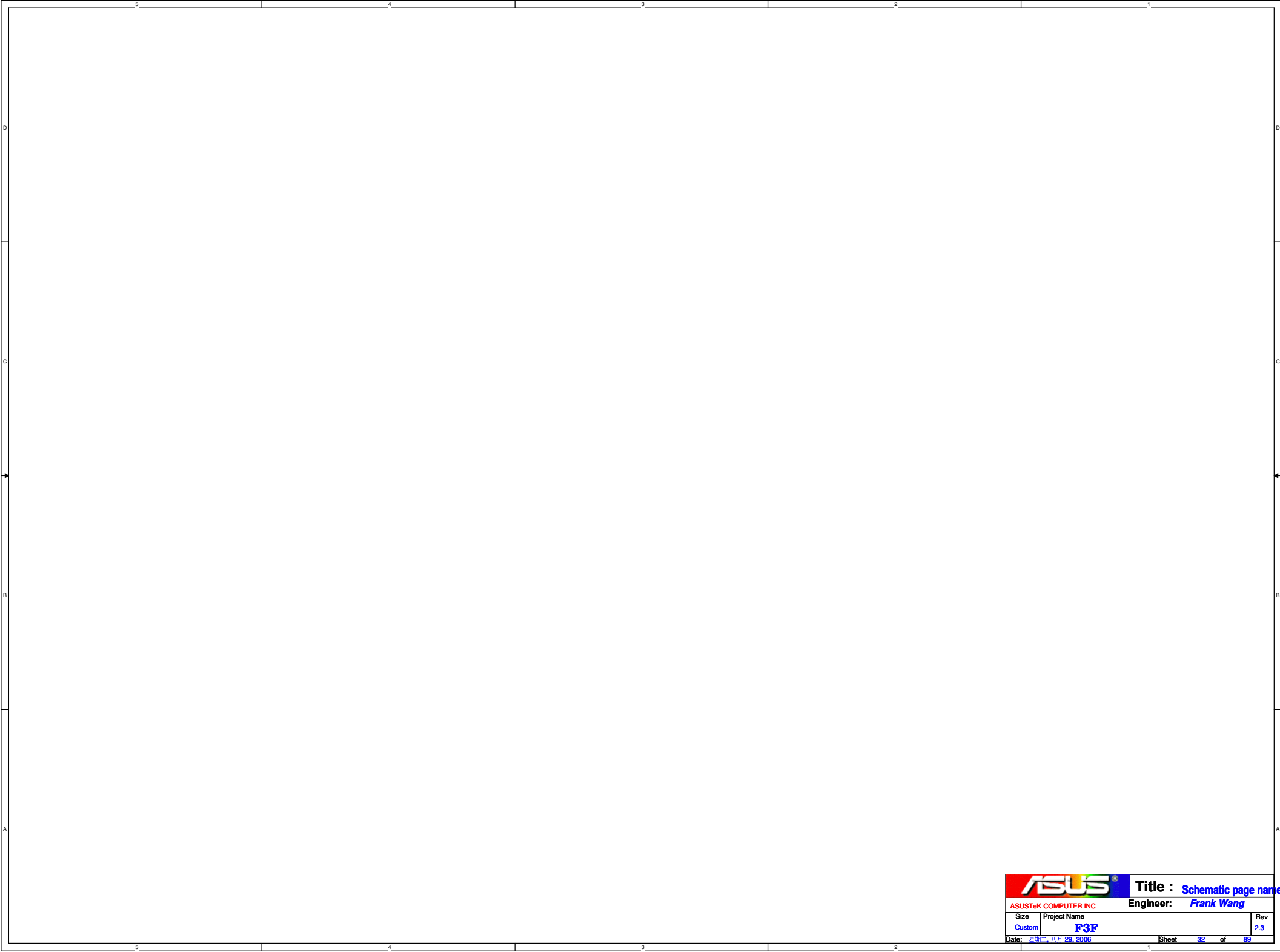


PLACE ESD
Diodes near
TV port

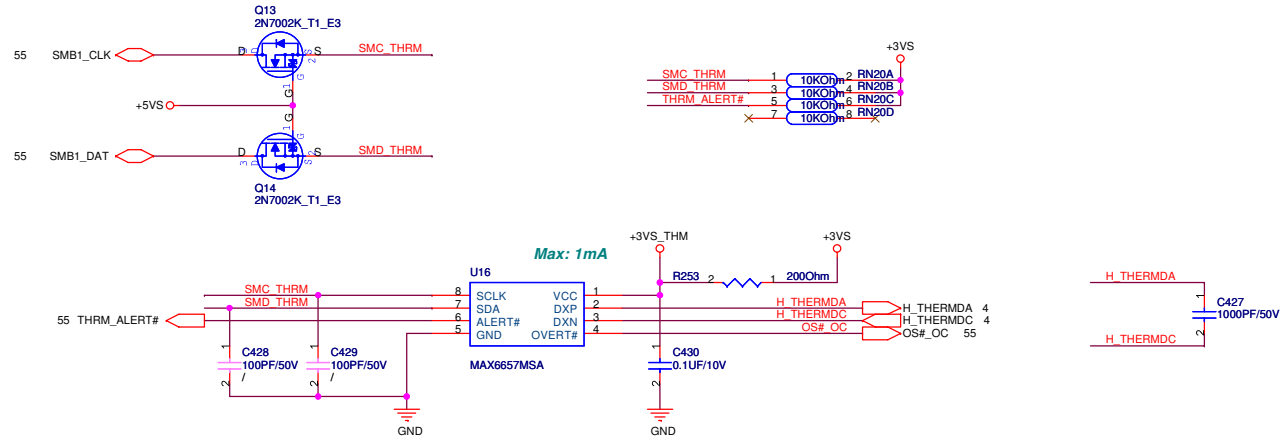


PLACE ESD
Diodes near
AV_IN port





Thermal Sensor

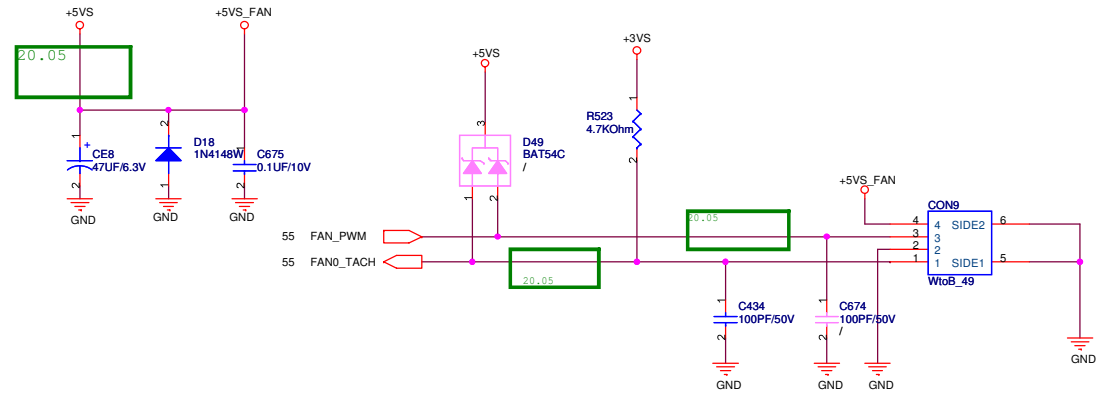


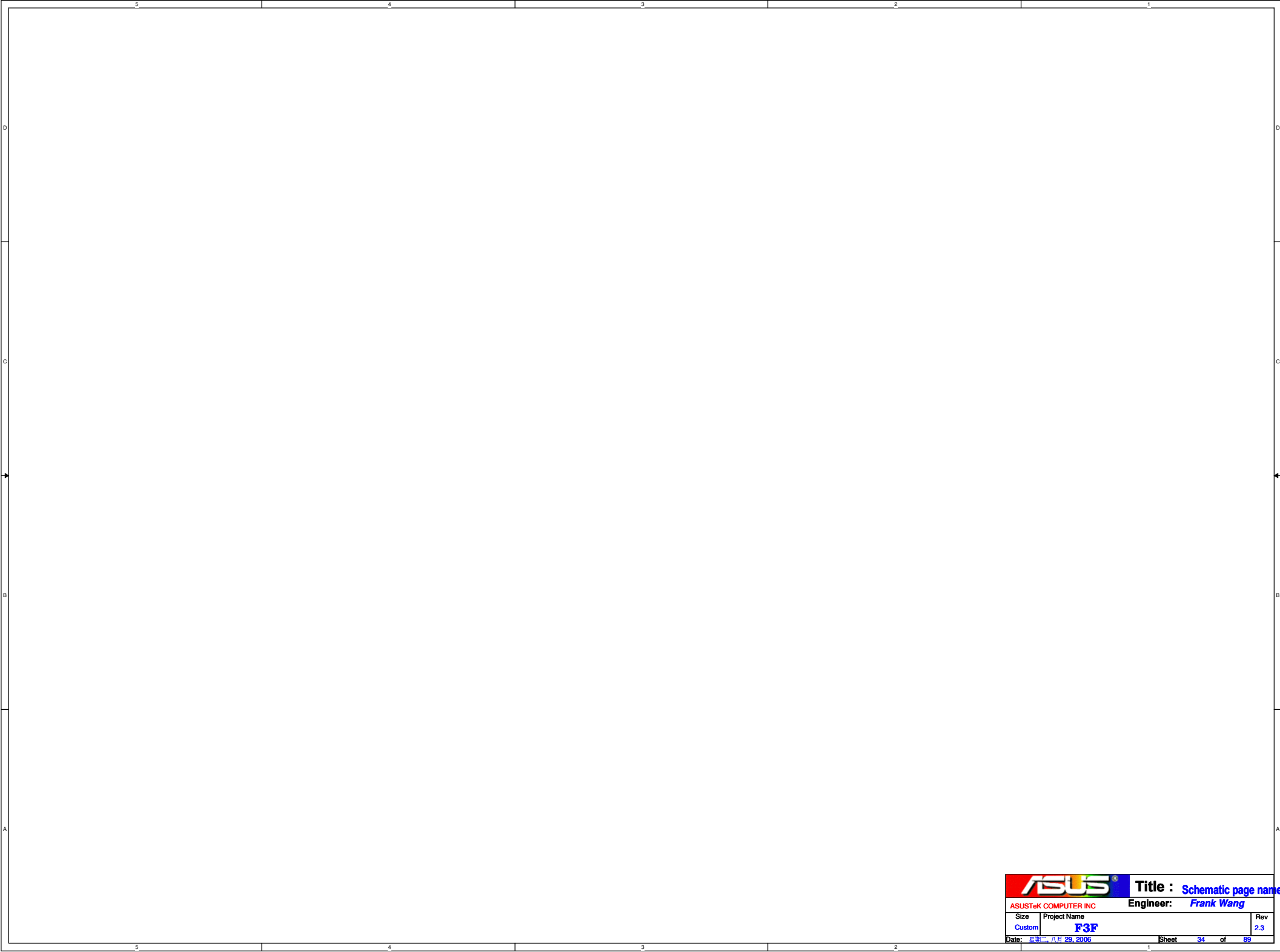
Route H_THERMDA and H_THERMDC on the same layer

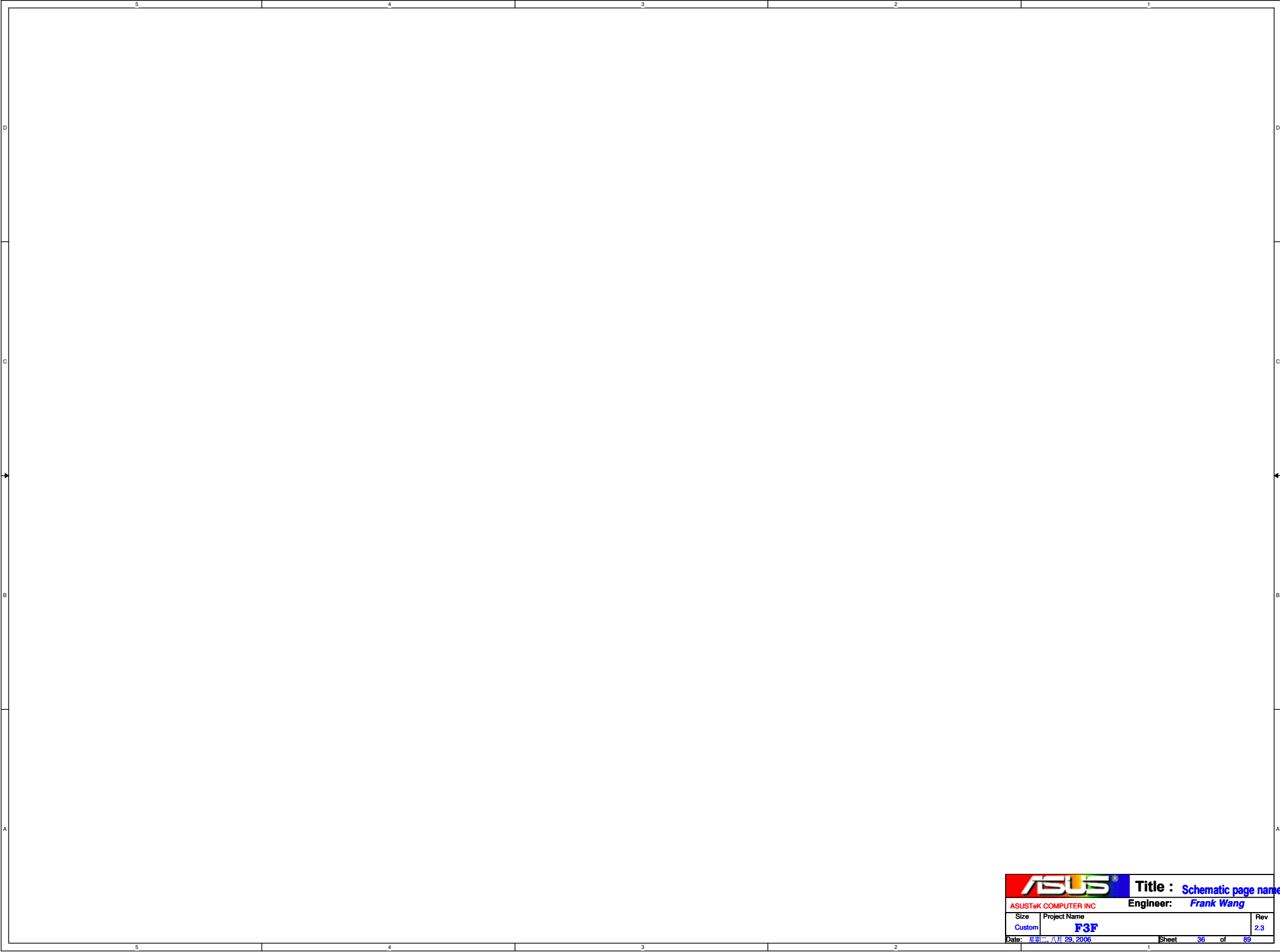
-----OTHER SIGNALS
15 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
15 mils
-----OTHER SIGNALS
Avoid FSB,Power

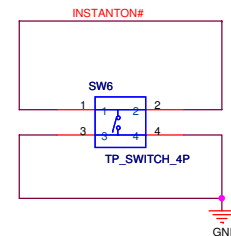
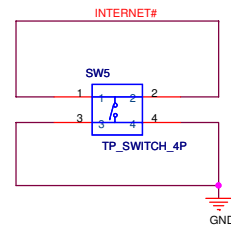
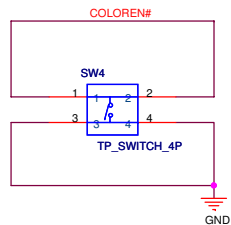
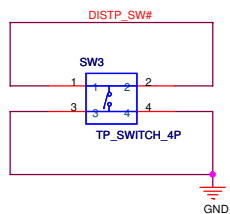
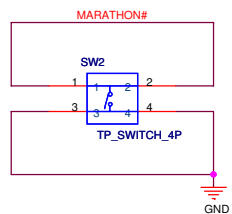
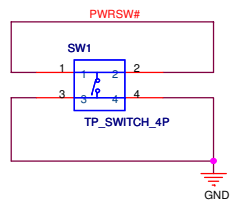
1108

DC FAN Control

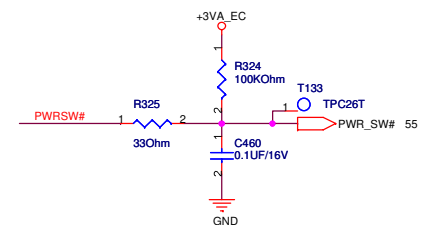
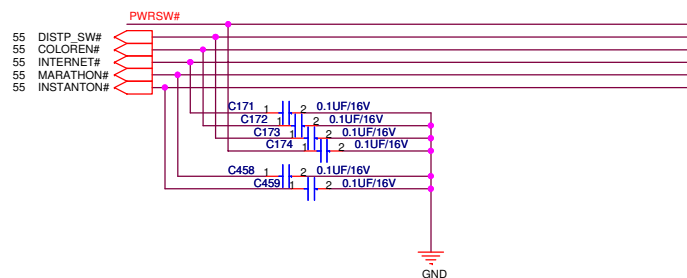
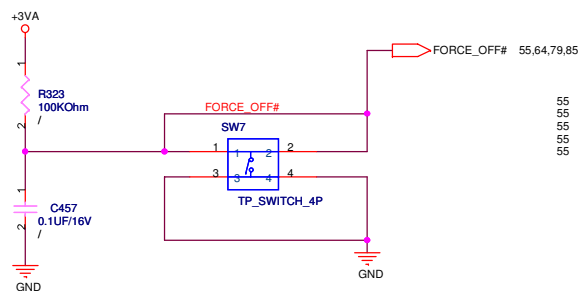


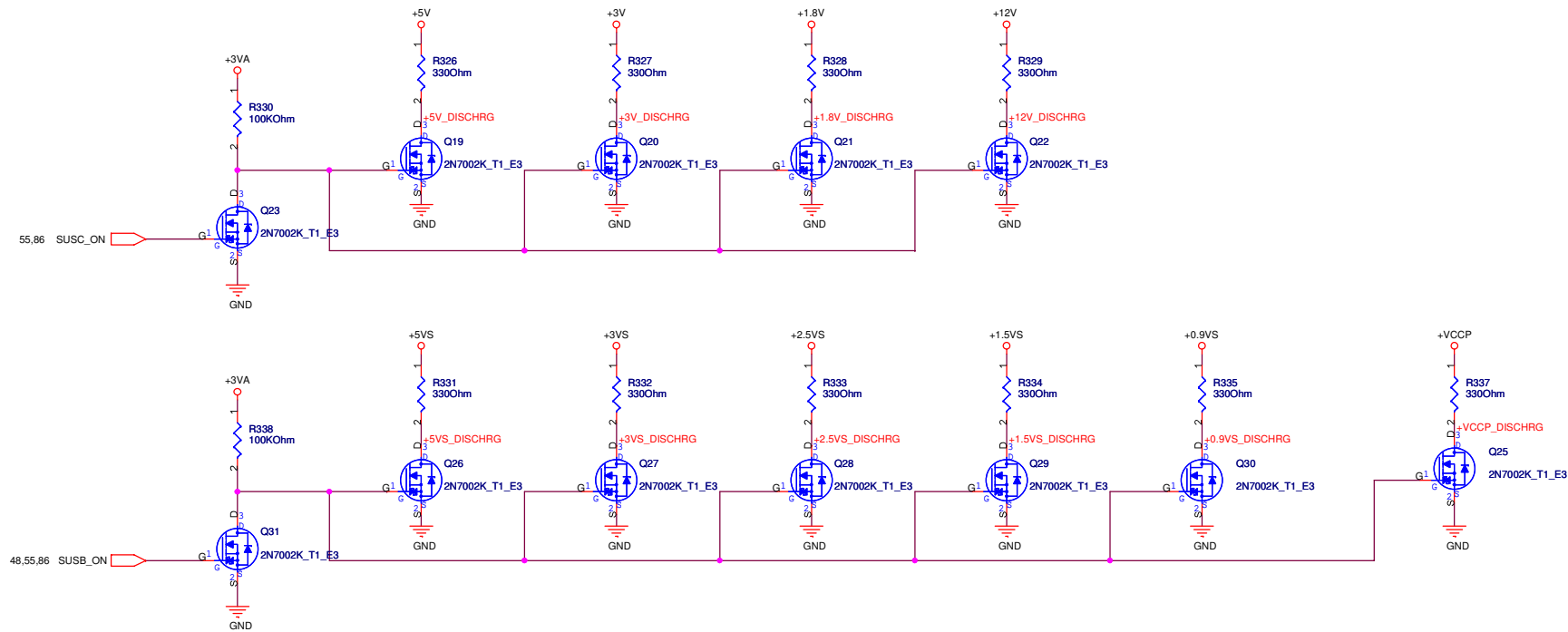


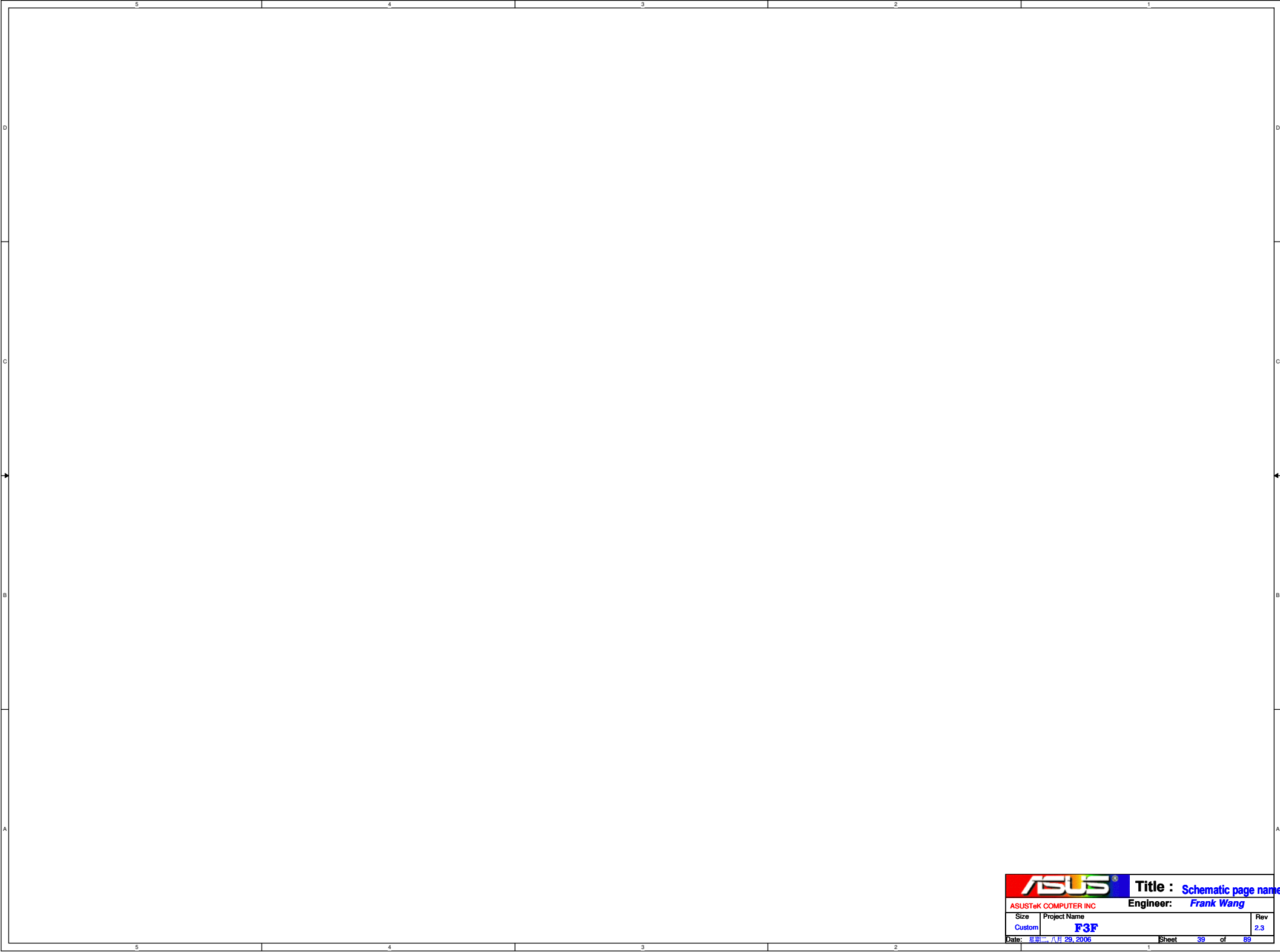




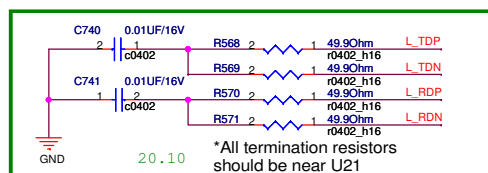
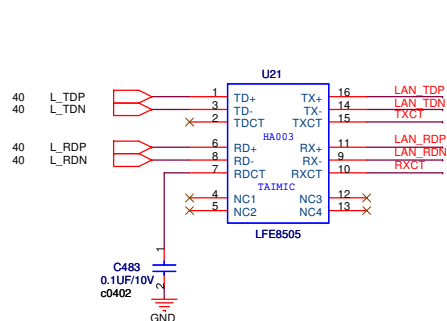
SHUT_DOWN#



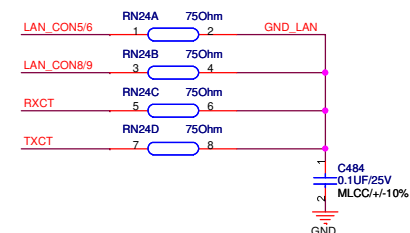
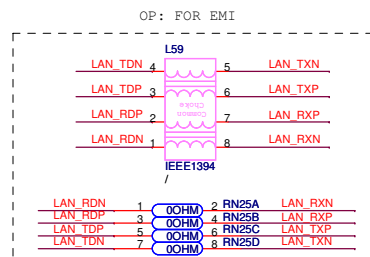


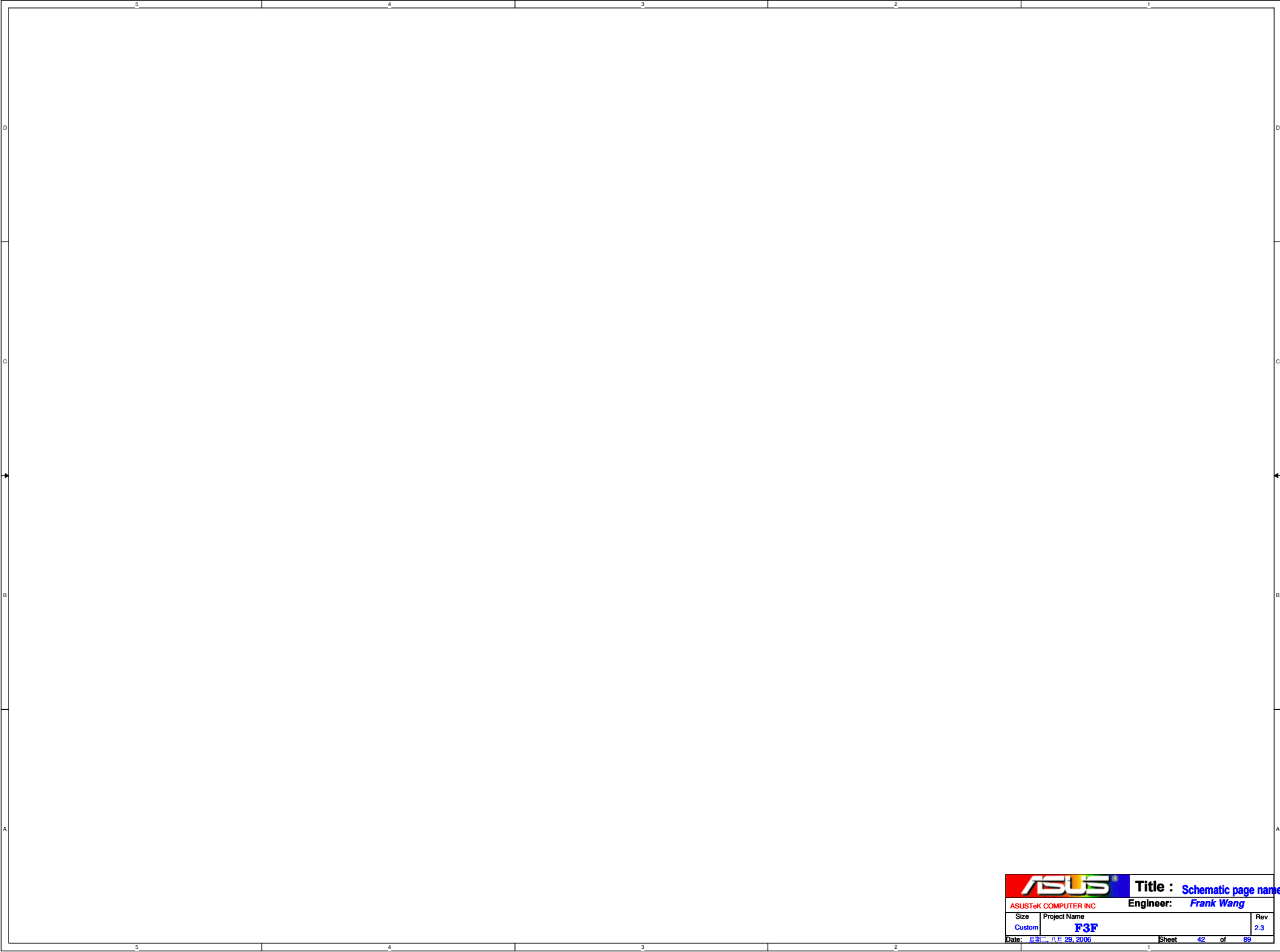


LAN CONN.



*All termination resistors should be near U21







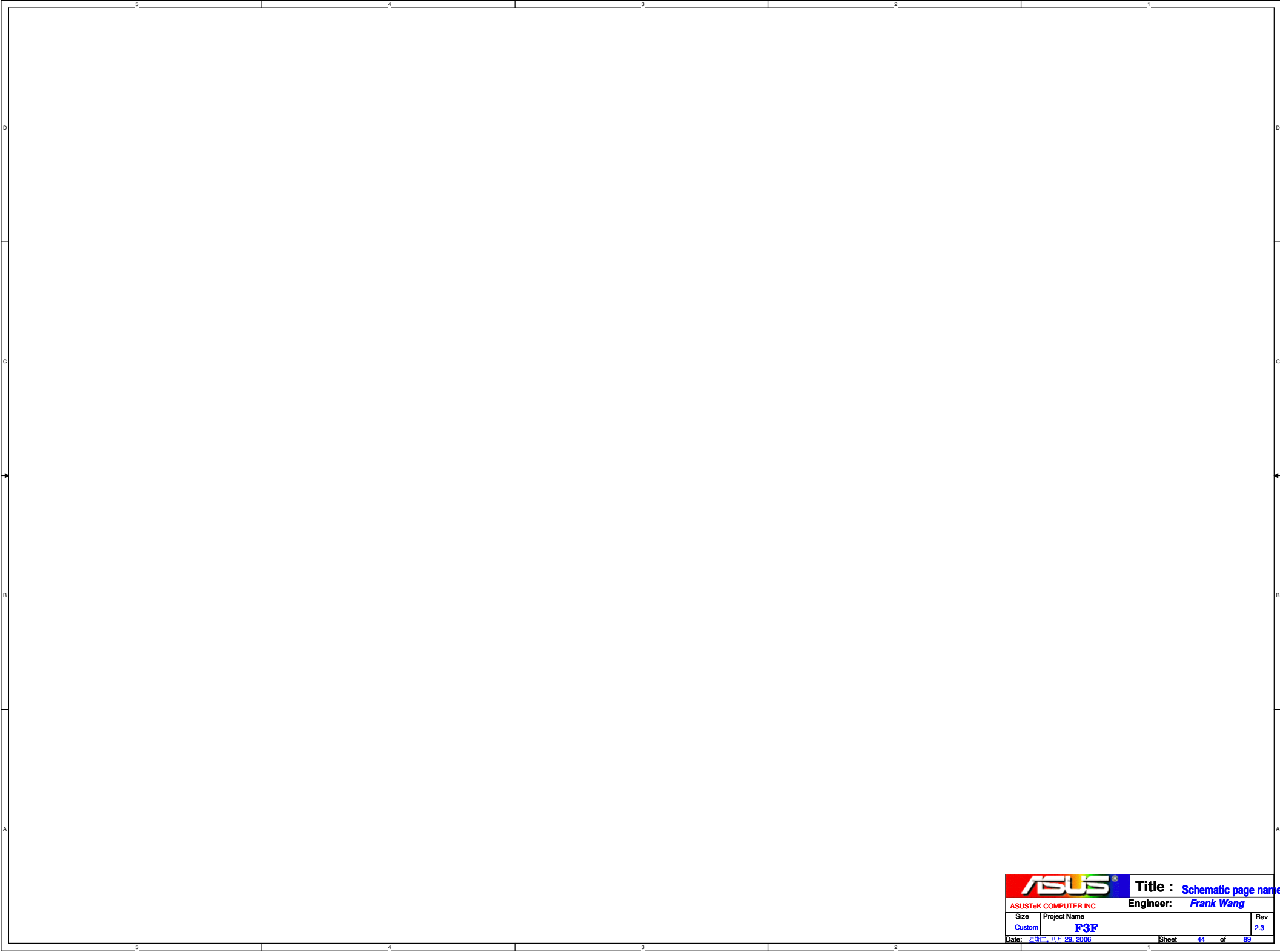
Title : Schematic page name

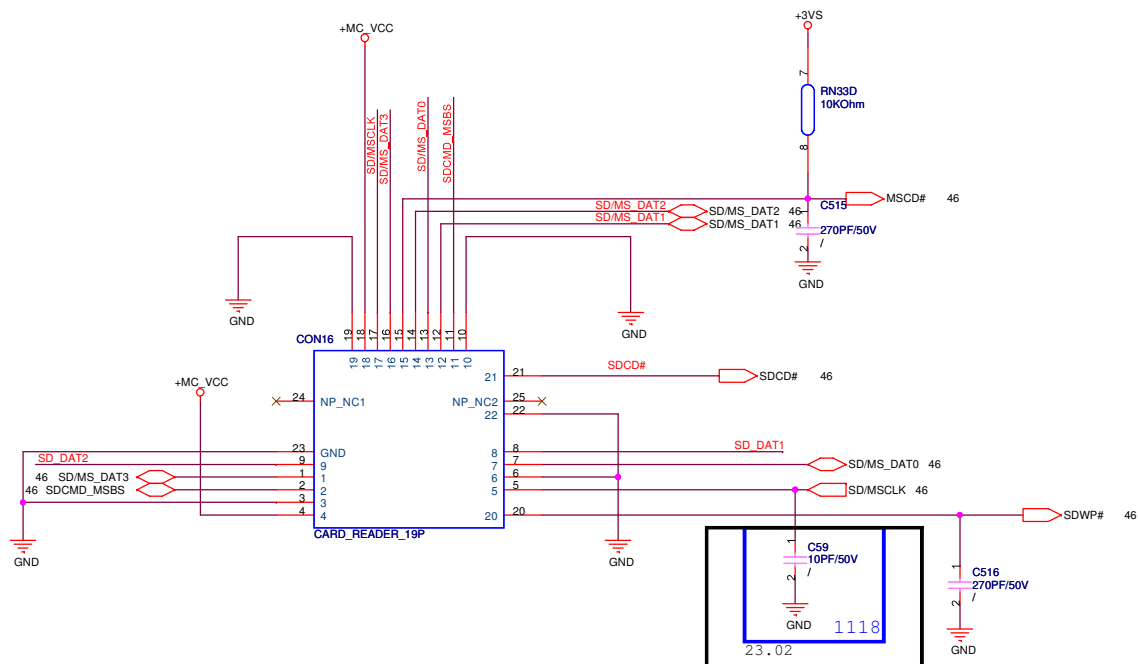
ASUSTeK COMPUTER INC

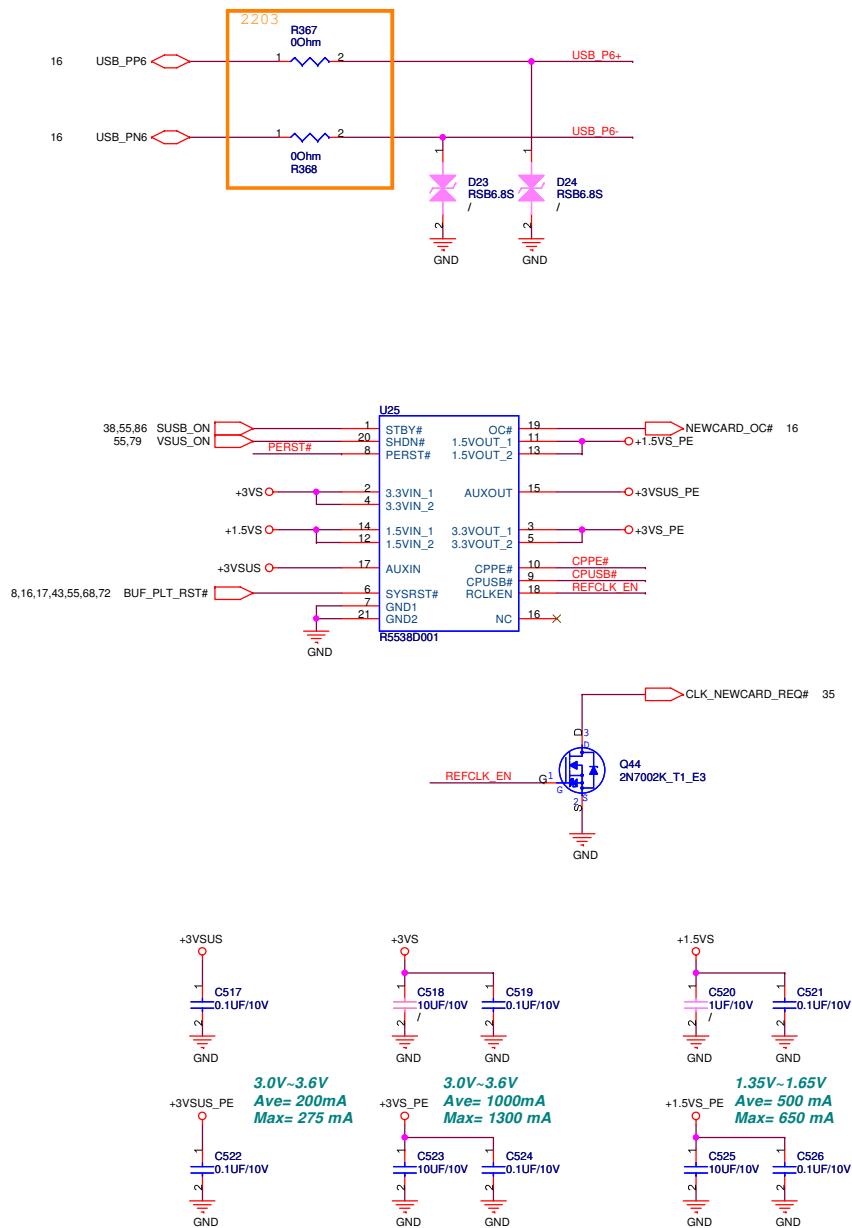
Engineer: Frank Wang

Size	Project Name	Rev
Custom	F3F	2.3

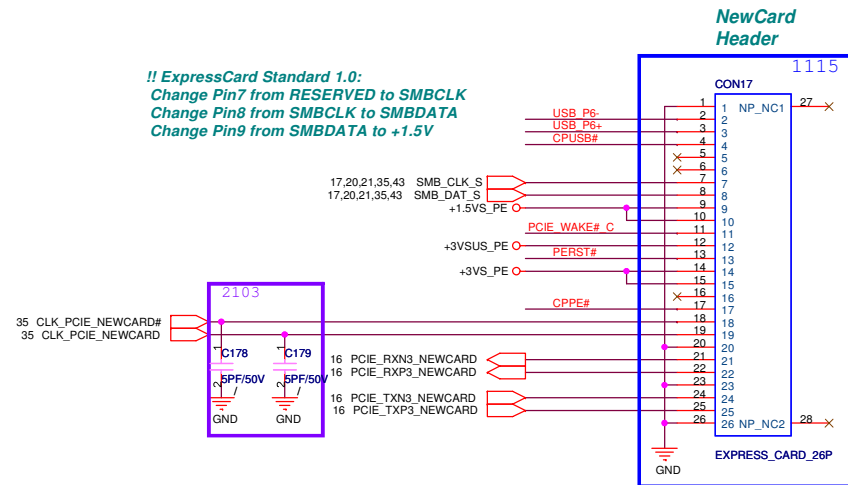
Date: 星期二, 八月 29, 2006Sheet 42 of 89



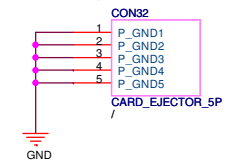


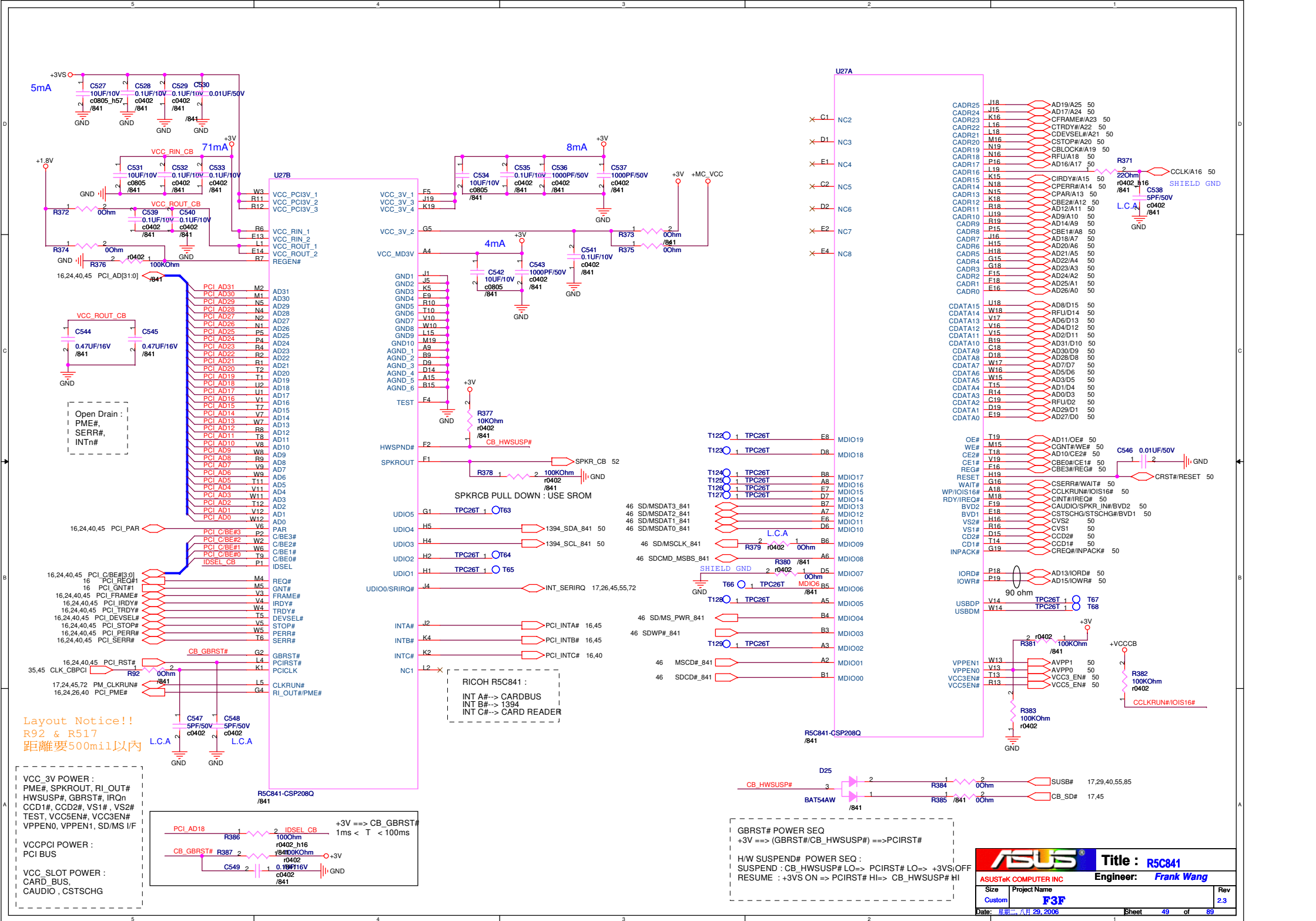


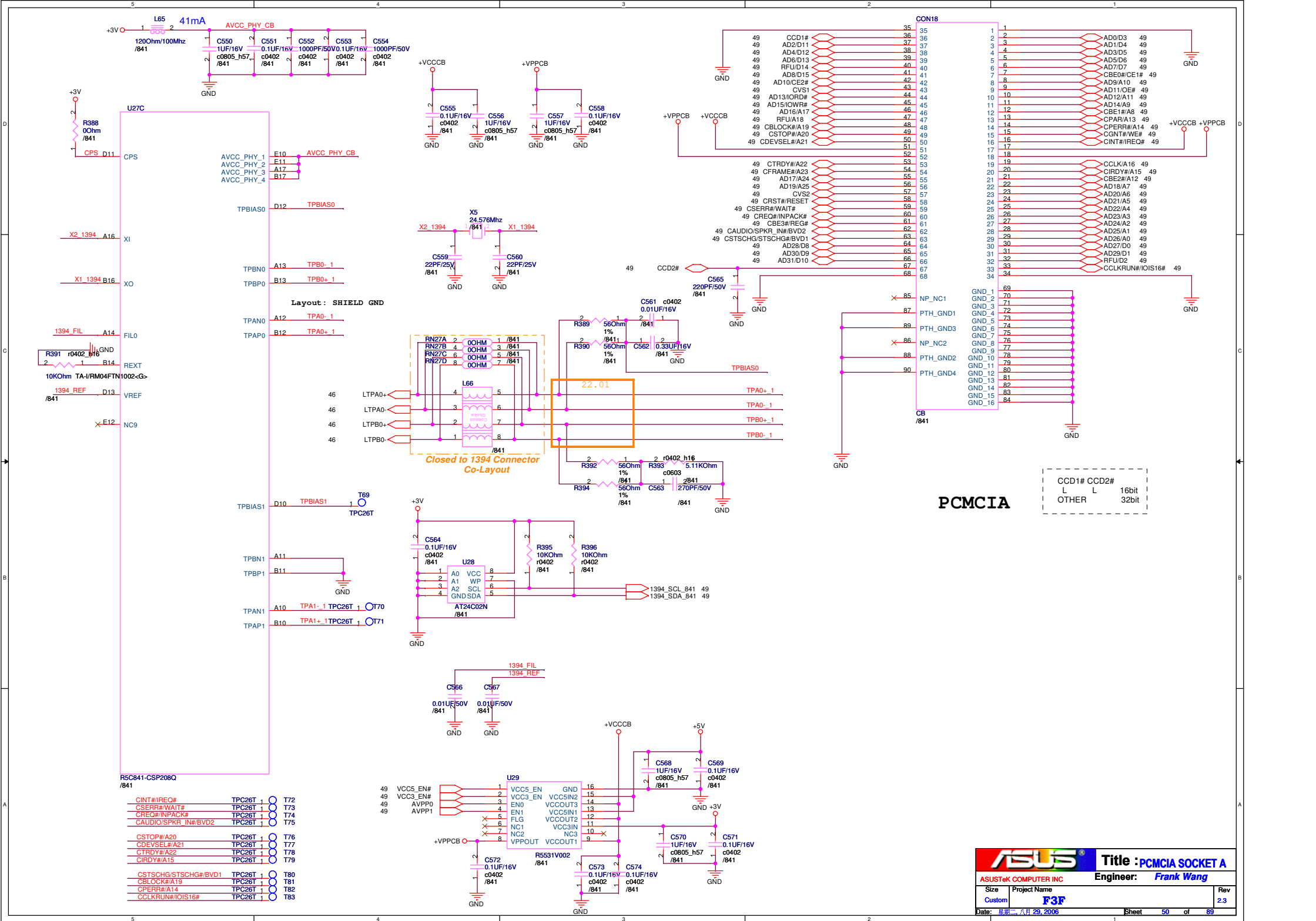
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

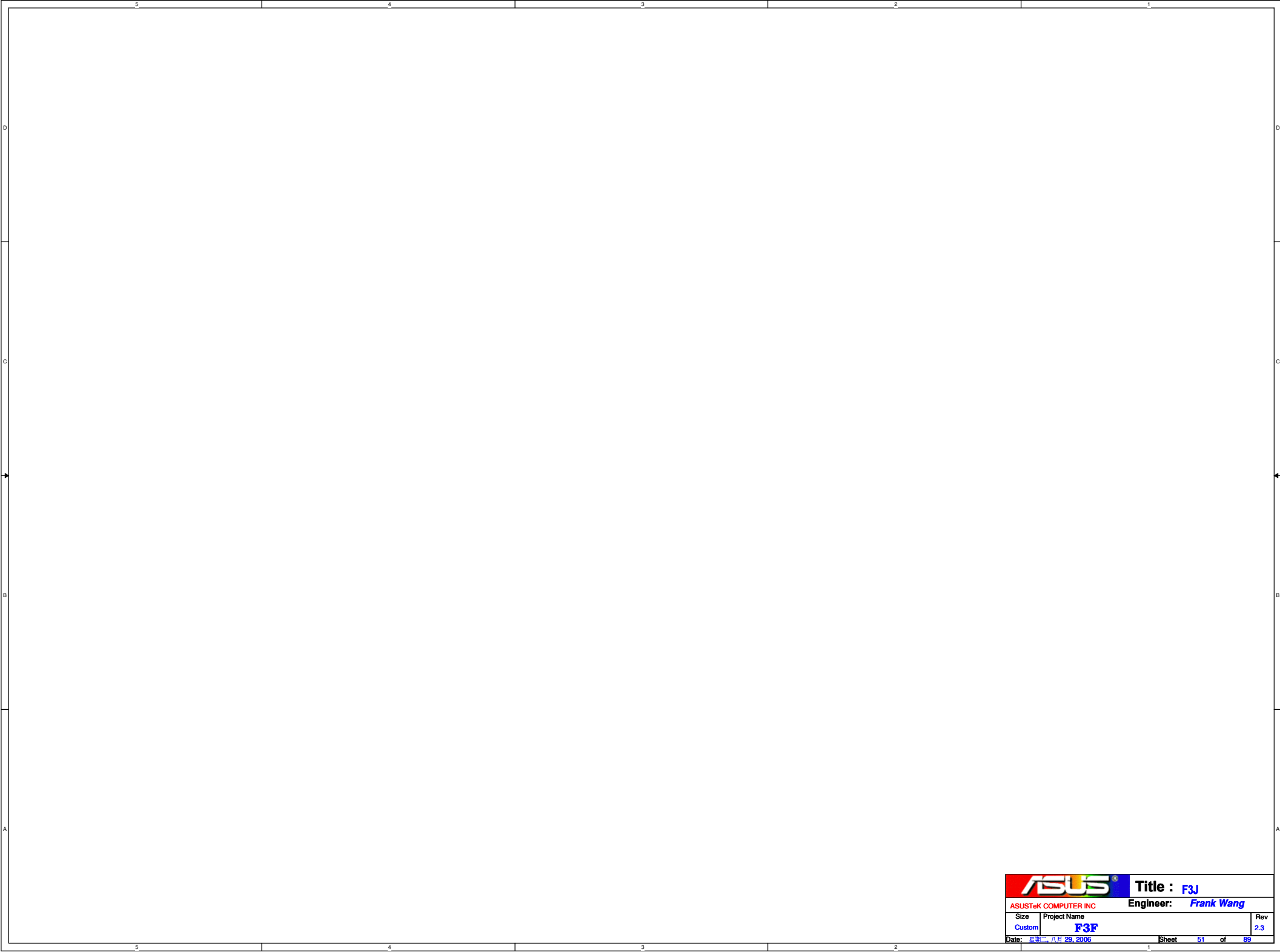


NewCard Ejecter

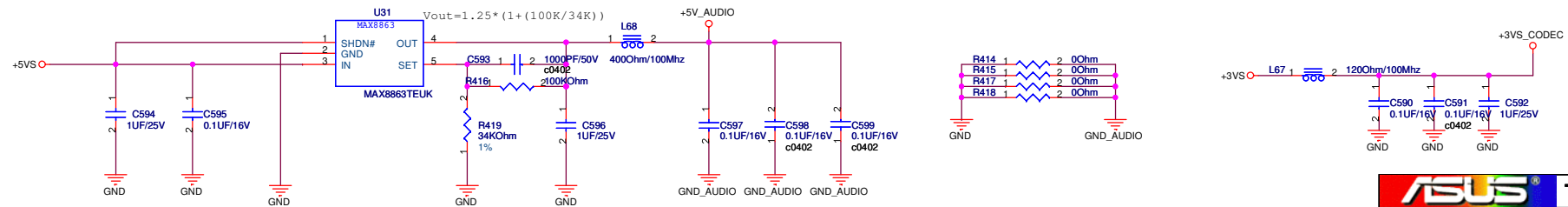
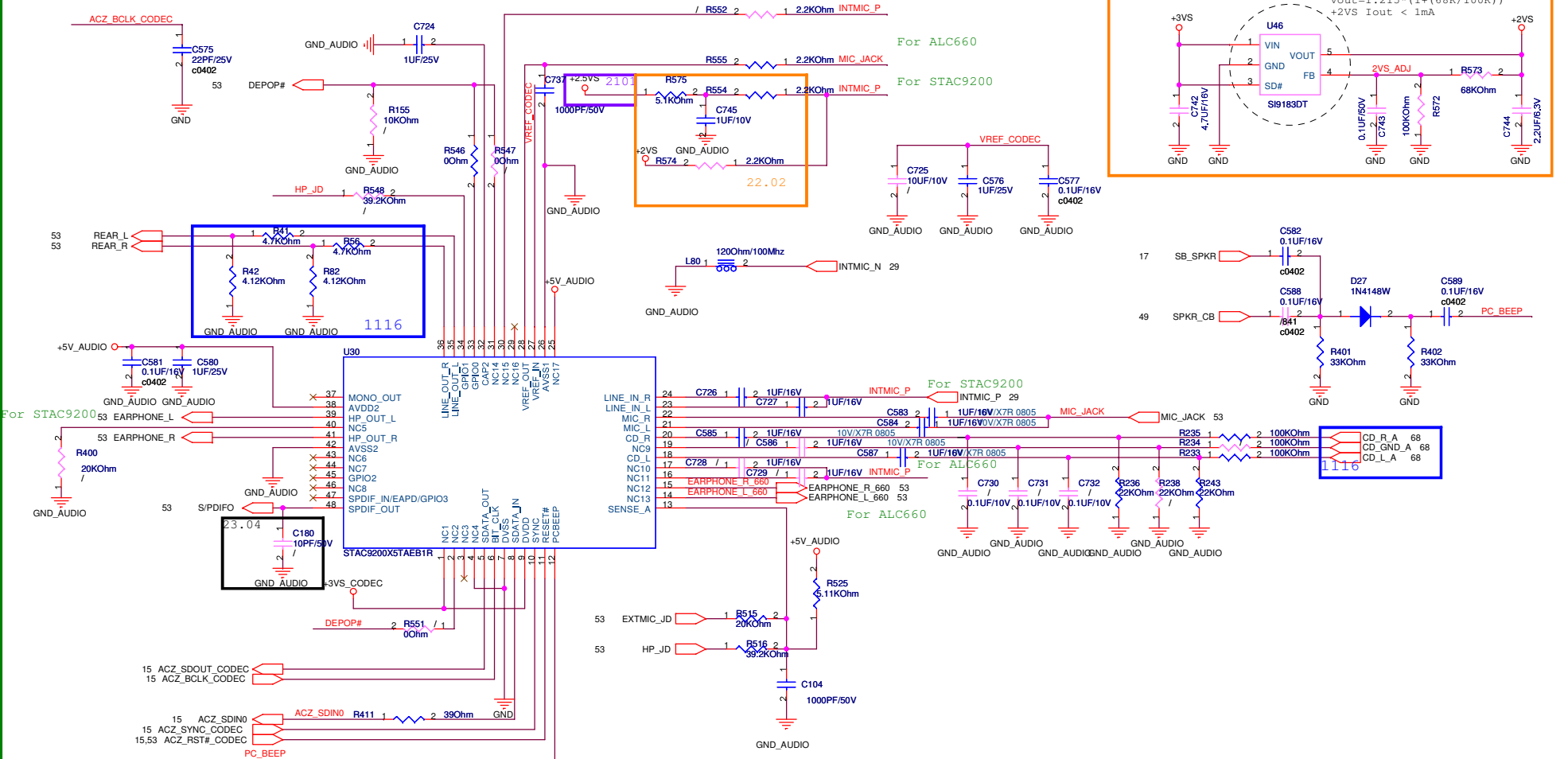


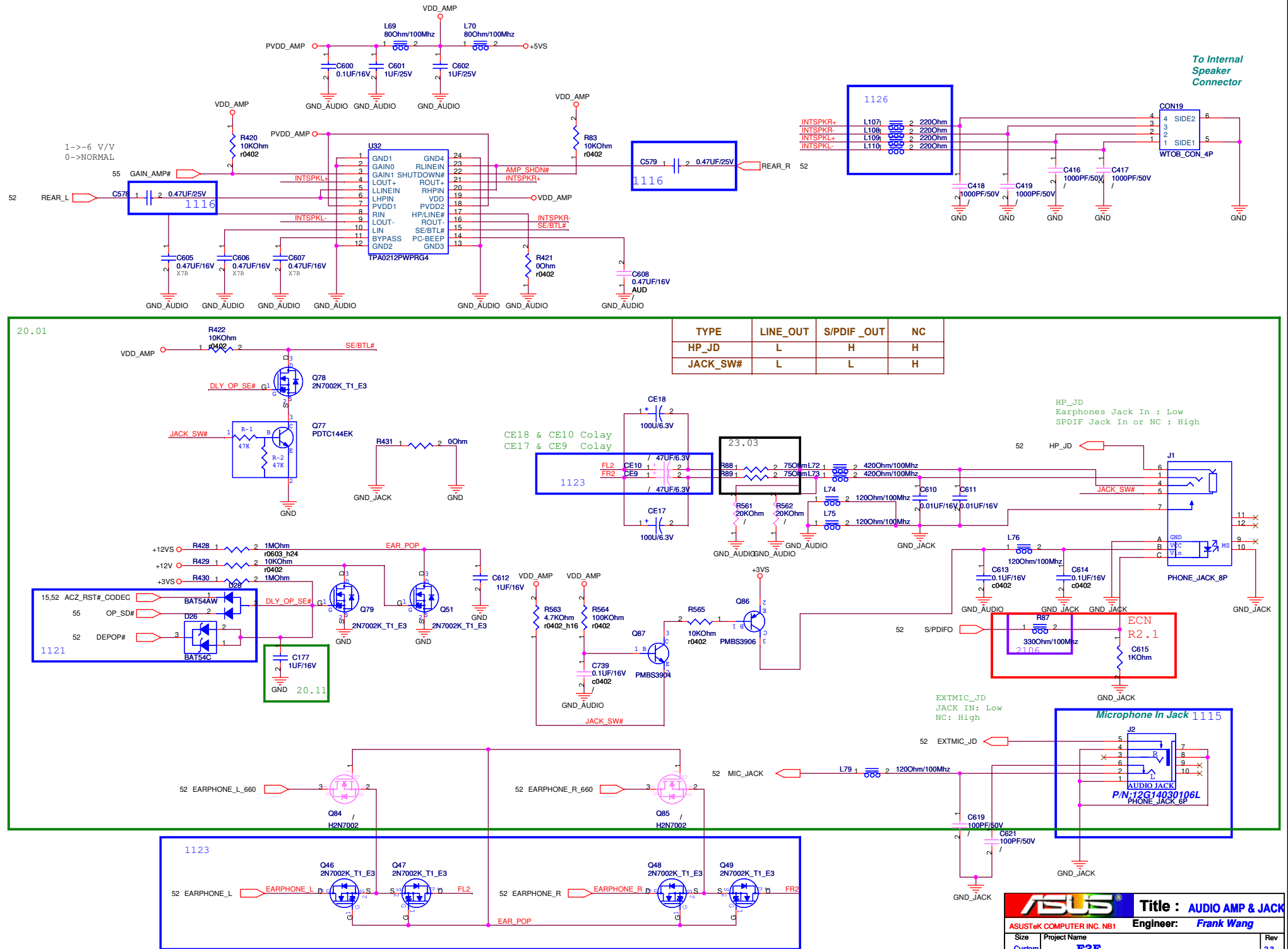


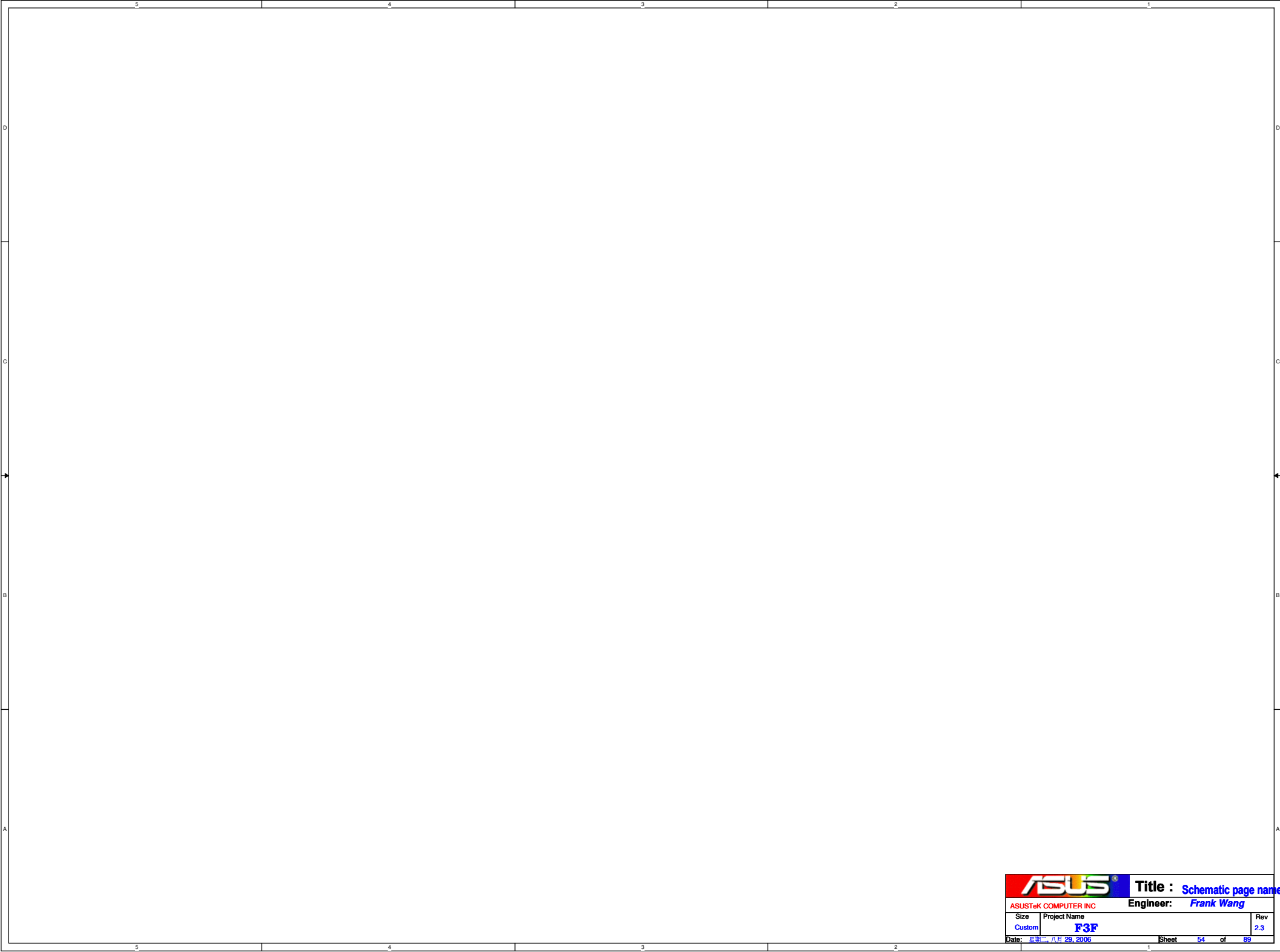


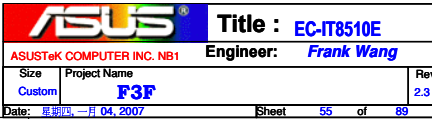


20.01

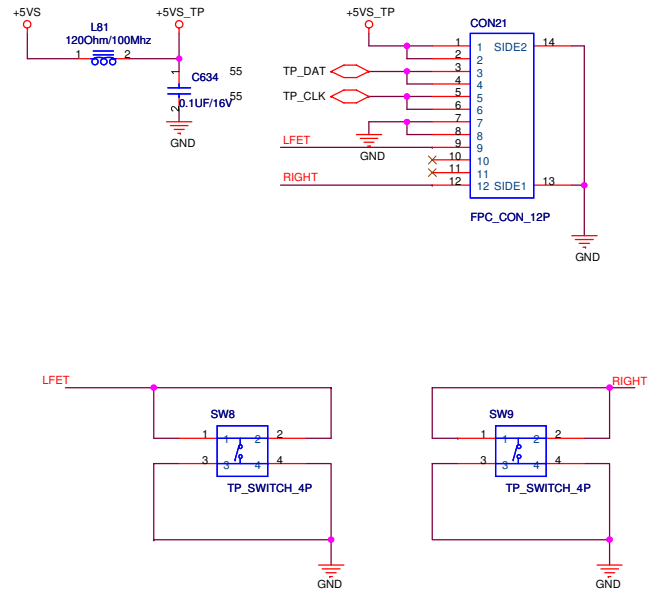




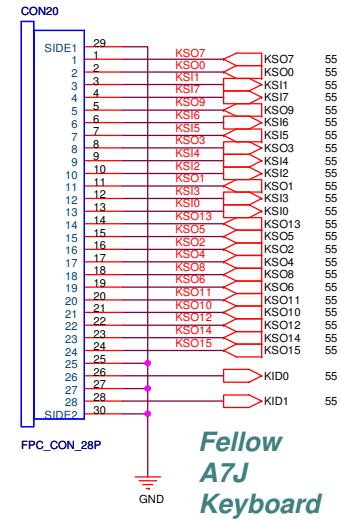




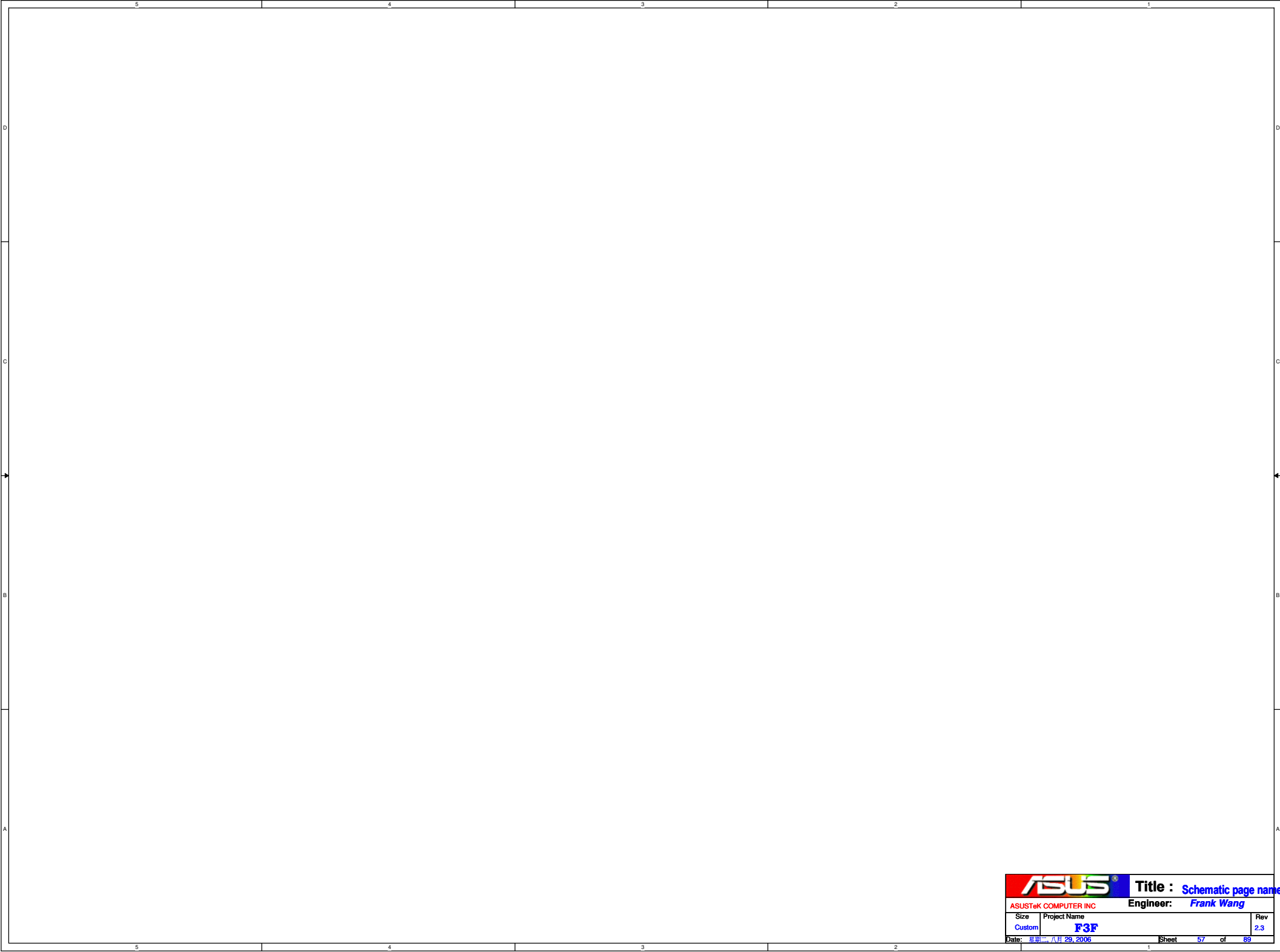
For Touch-Pad

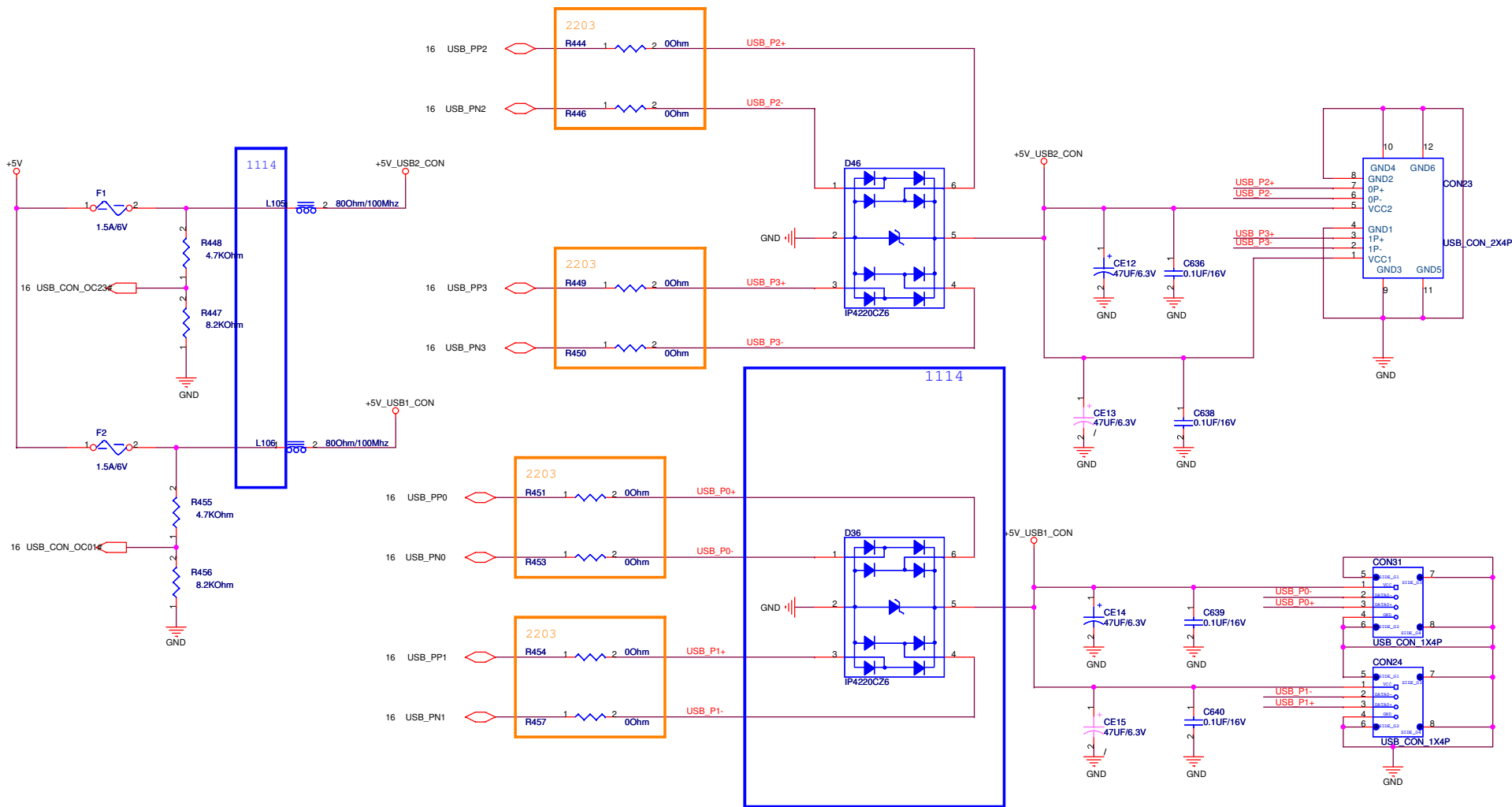


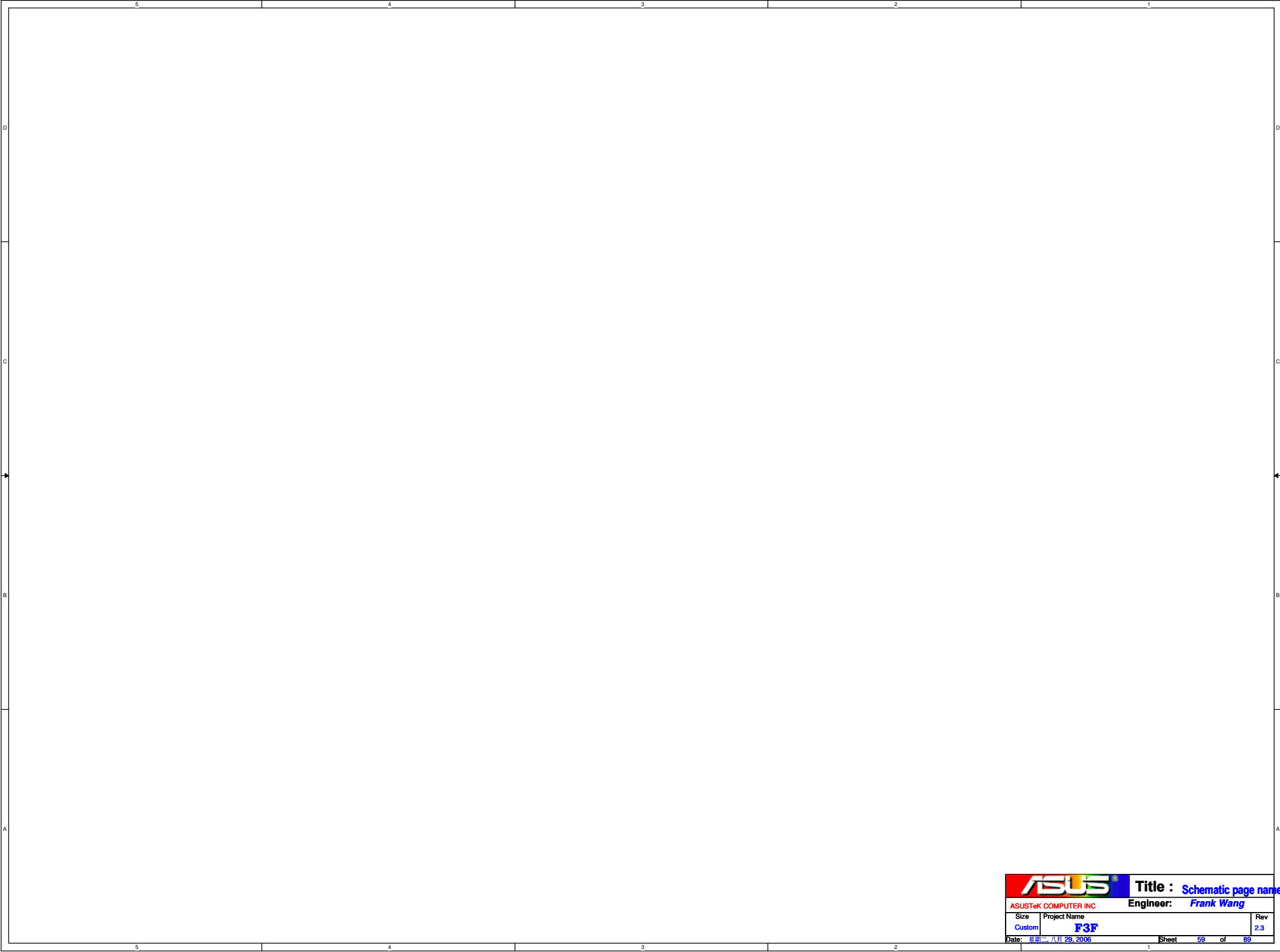
For Keyboard



**Fellow
A7J
Keyboard**





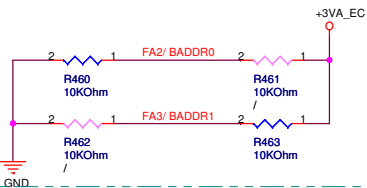


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

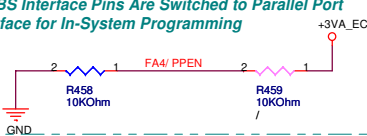
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by
EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

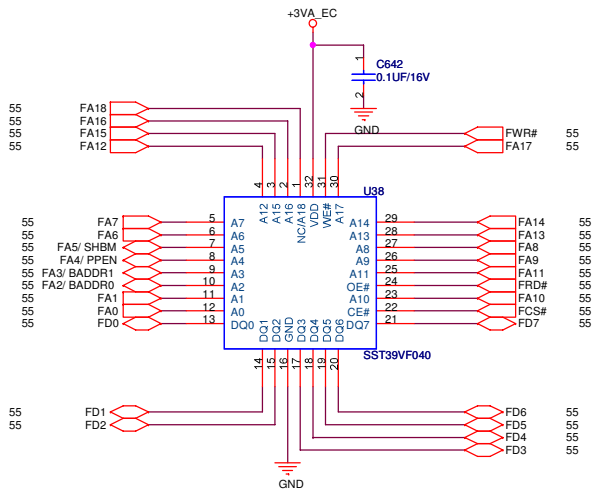
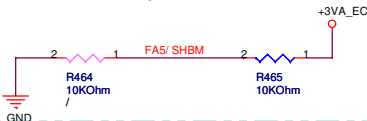
FA4/ PPEN

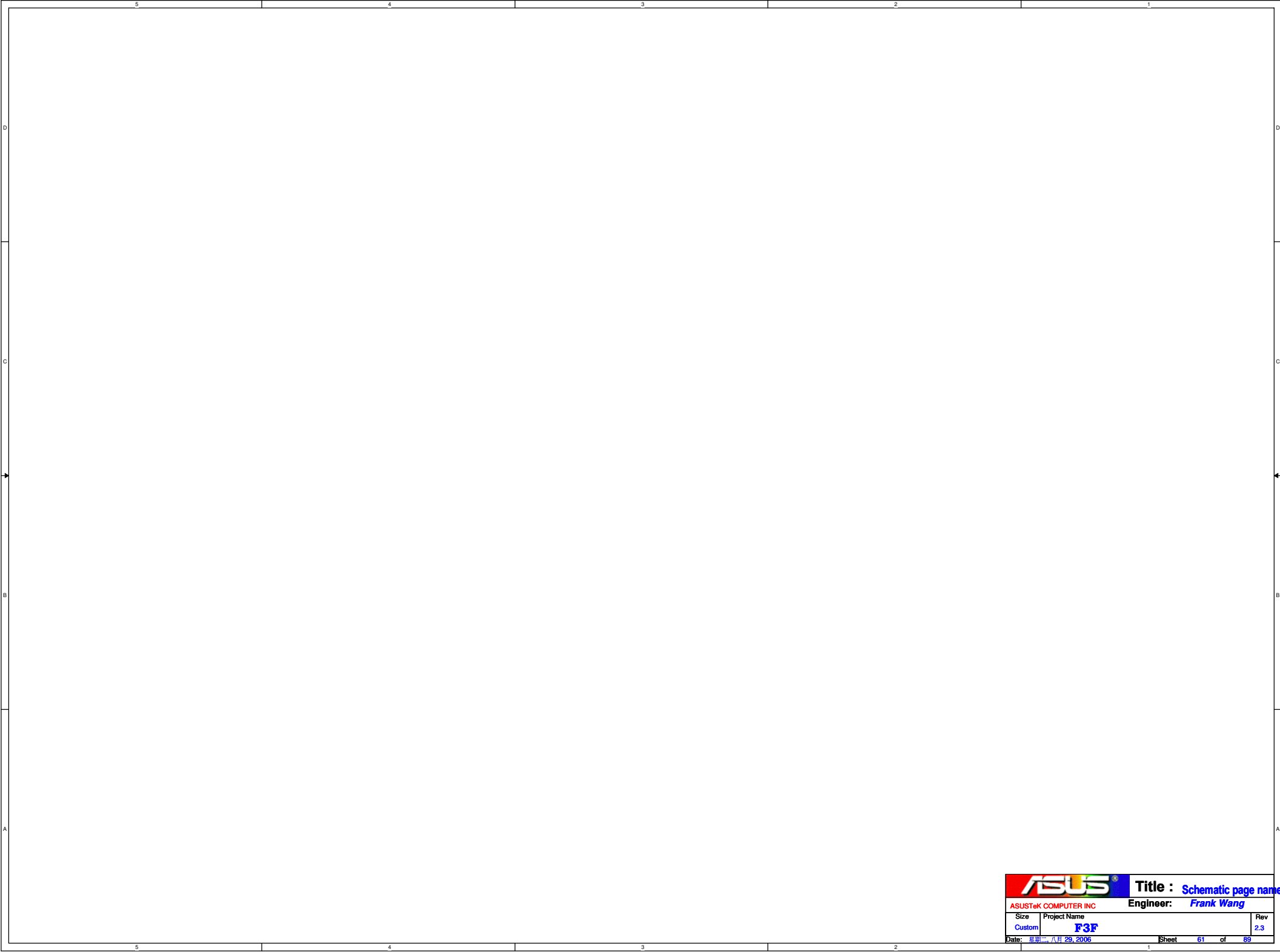
0: Normal
1: KBS Interface Pins Are Switched to Parallel Port
Interface for In-System Programming



FA5/ SHBM

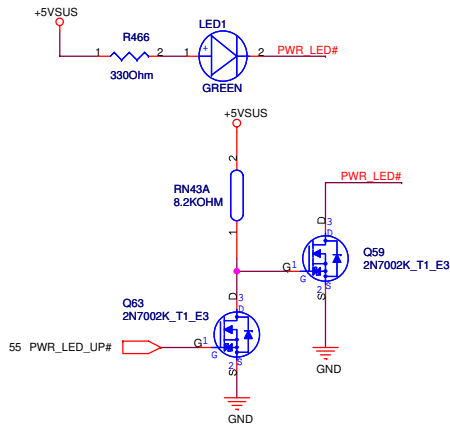
0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS



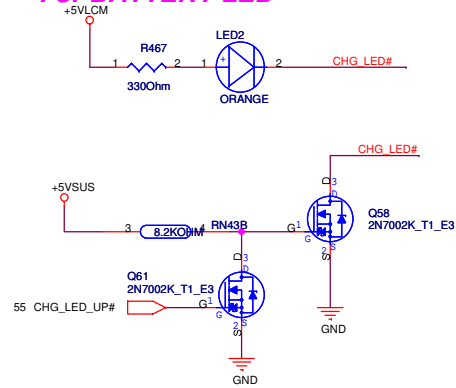


For LED

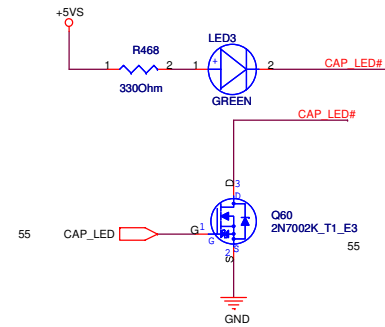
For POWER LED



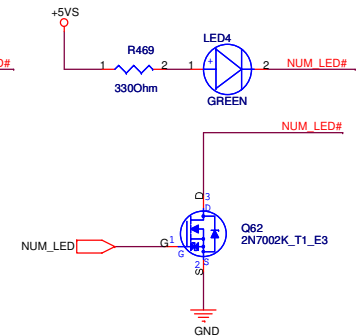
For BATTERY LED



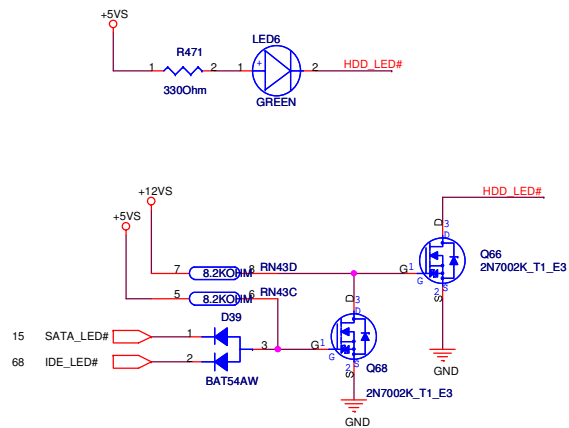
for Cap. Lock



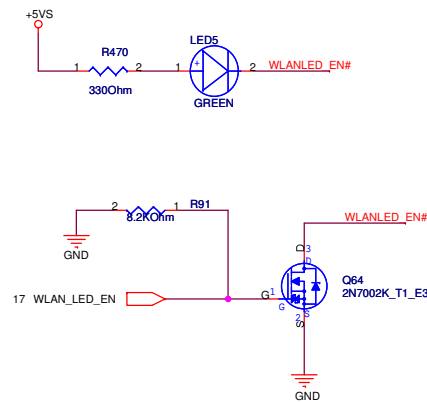
for Num Lock



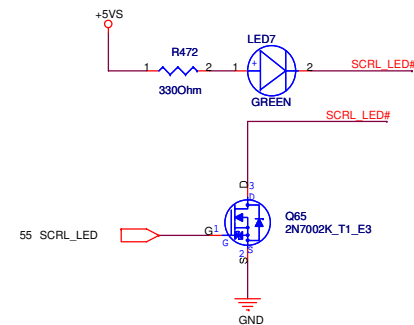
For SATA/IDE LED



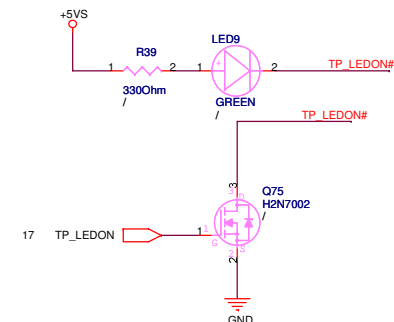
For WireLess LED



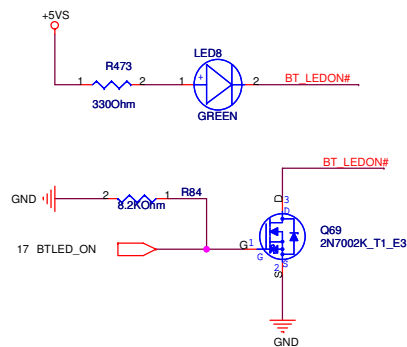
for Scroll Lock

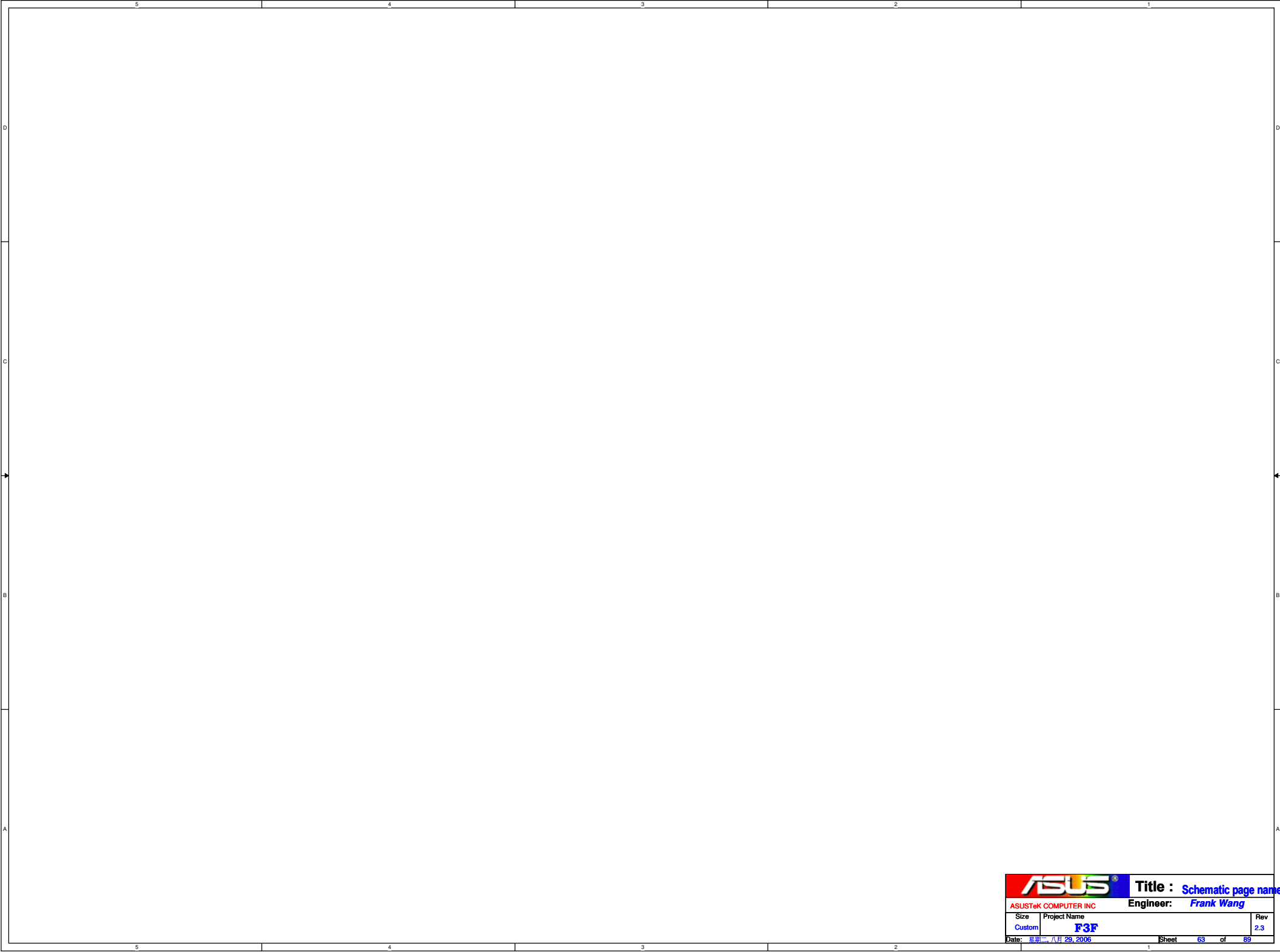


for Touch Pad

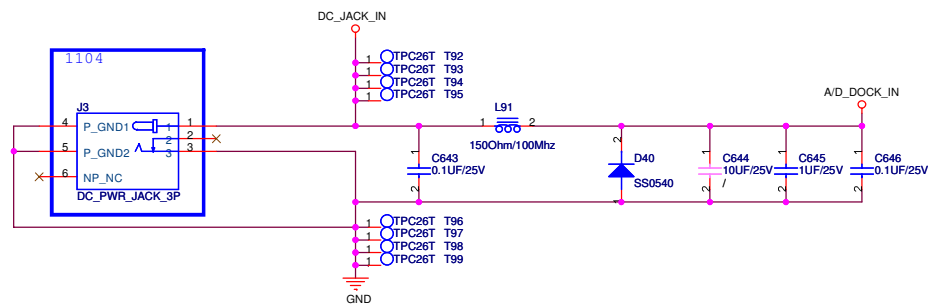


For BT LED

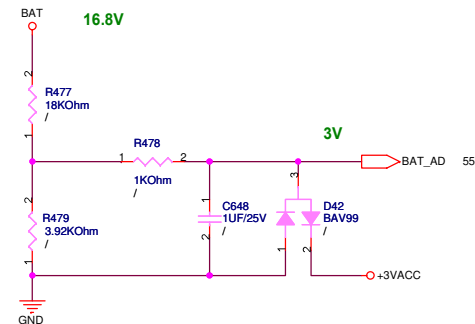
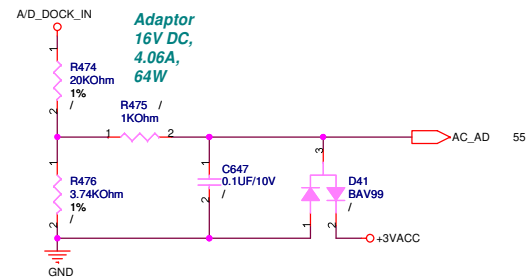
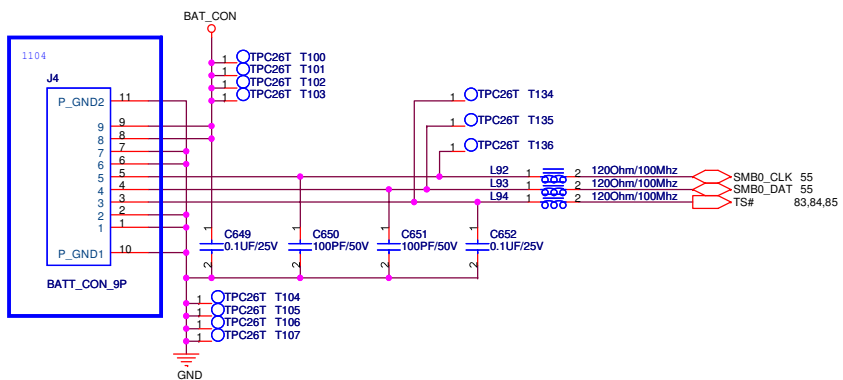




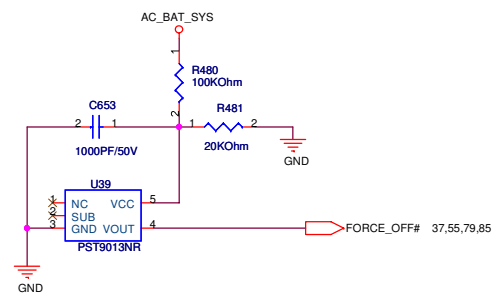
DC IN

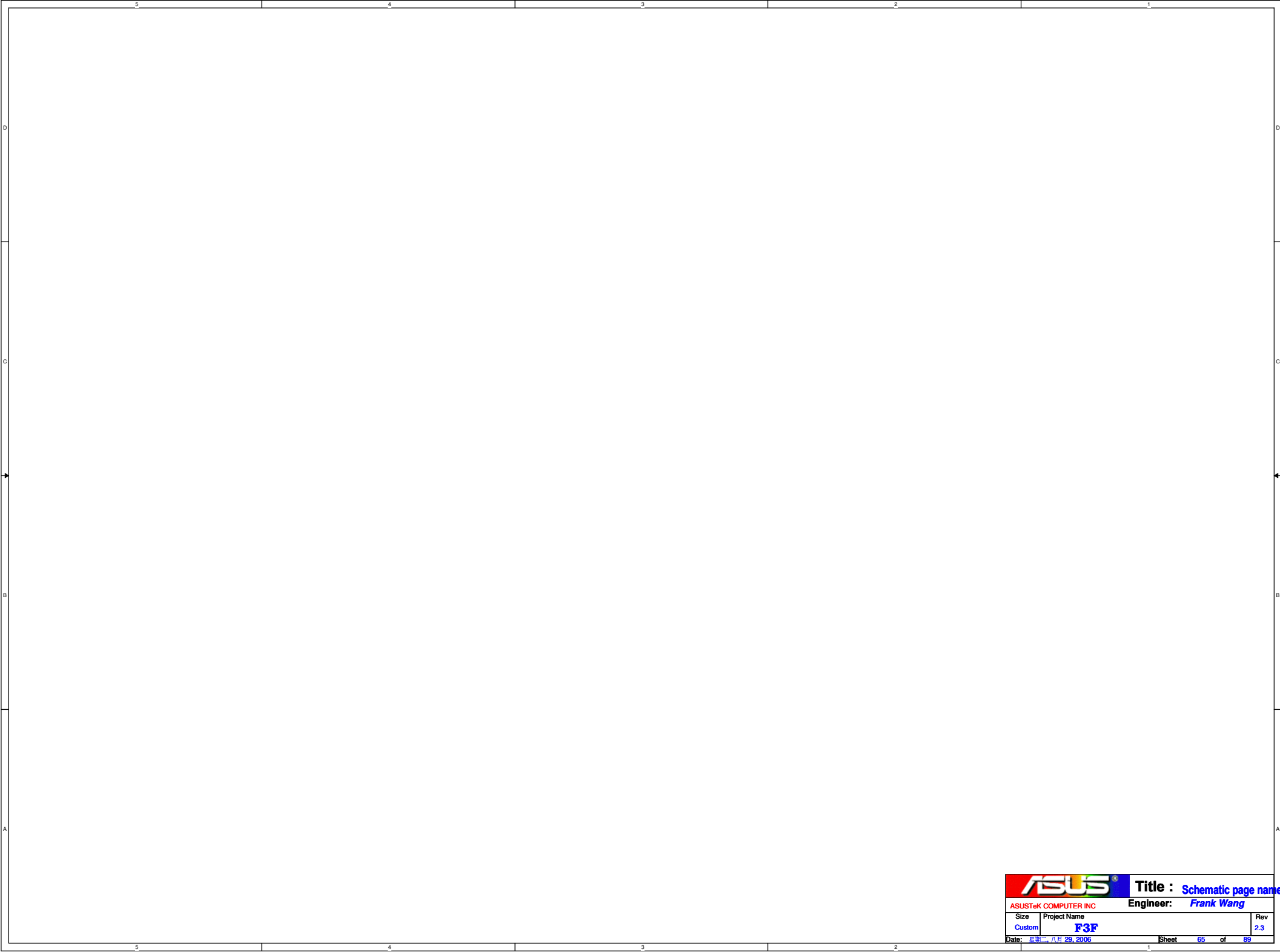


BAT IN

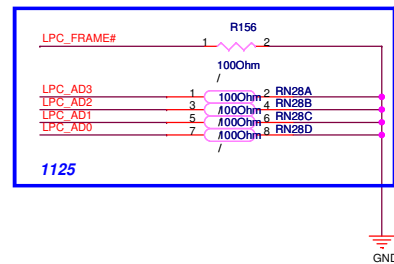
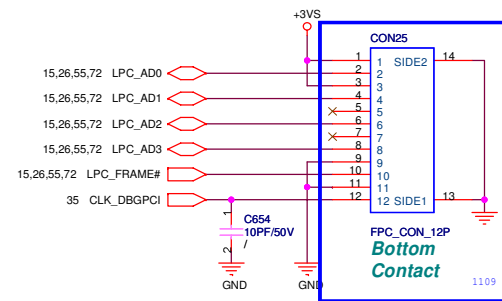


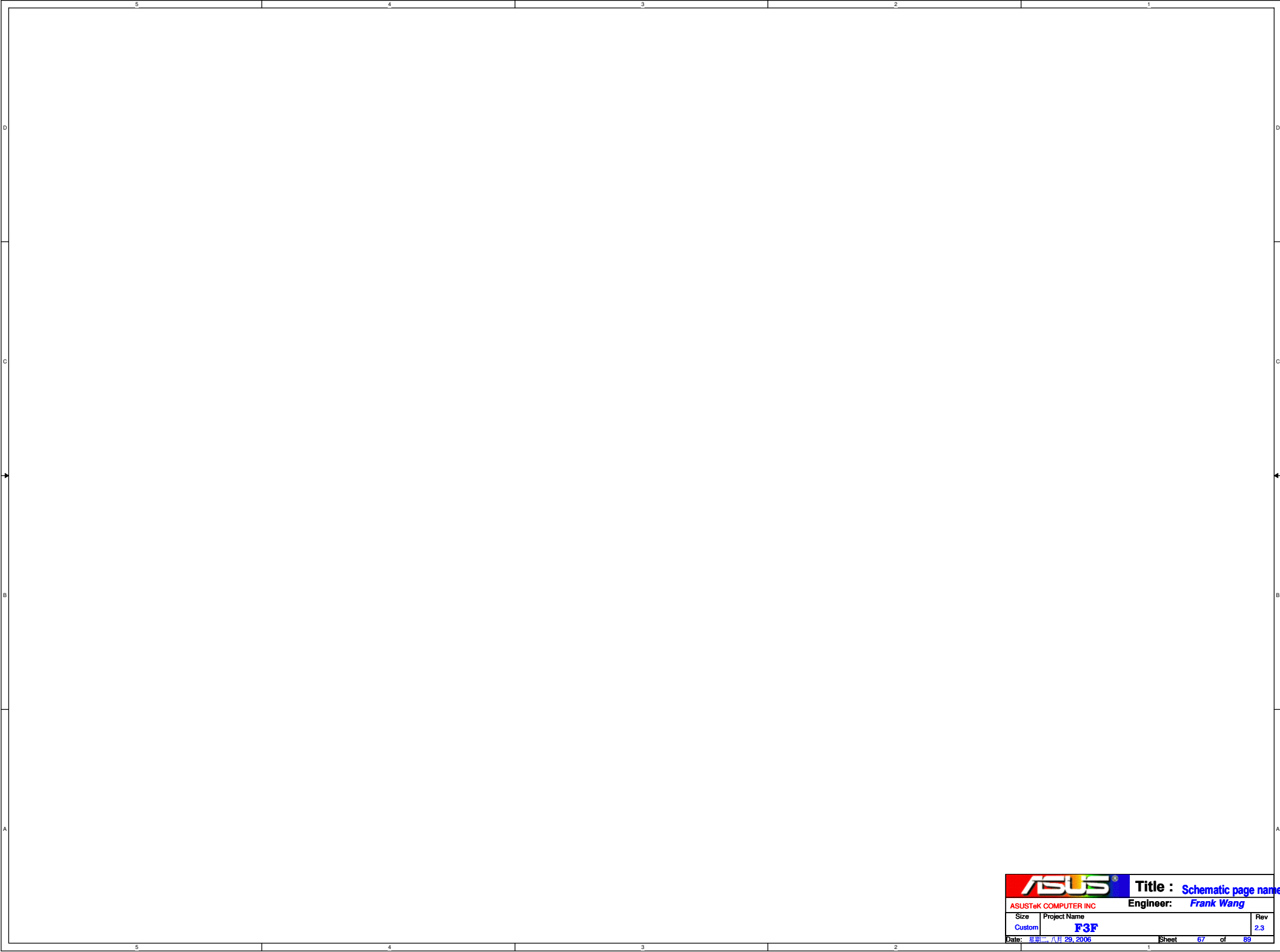
Without Battery & Pull out Adaptor

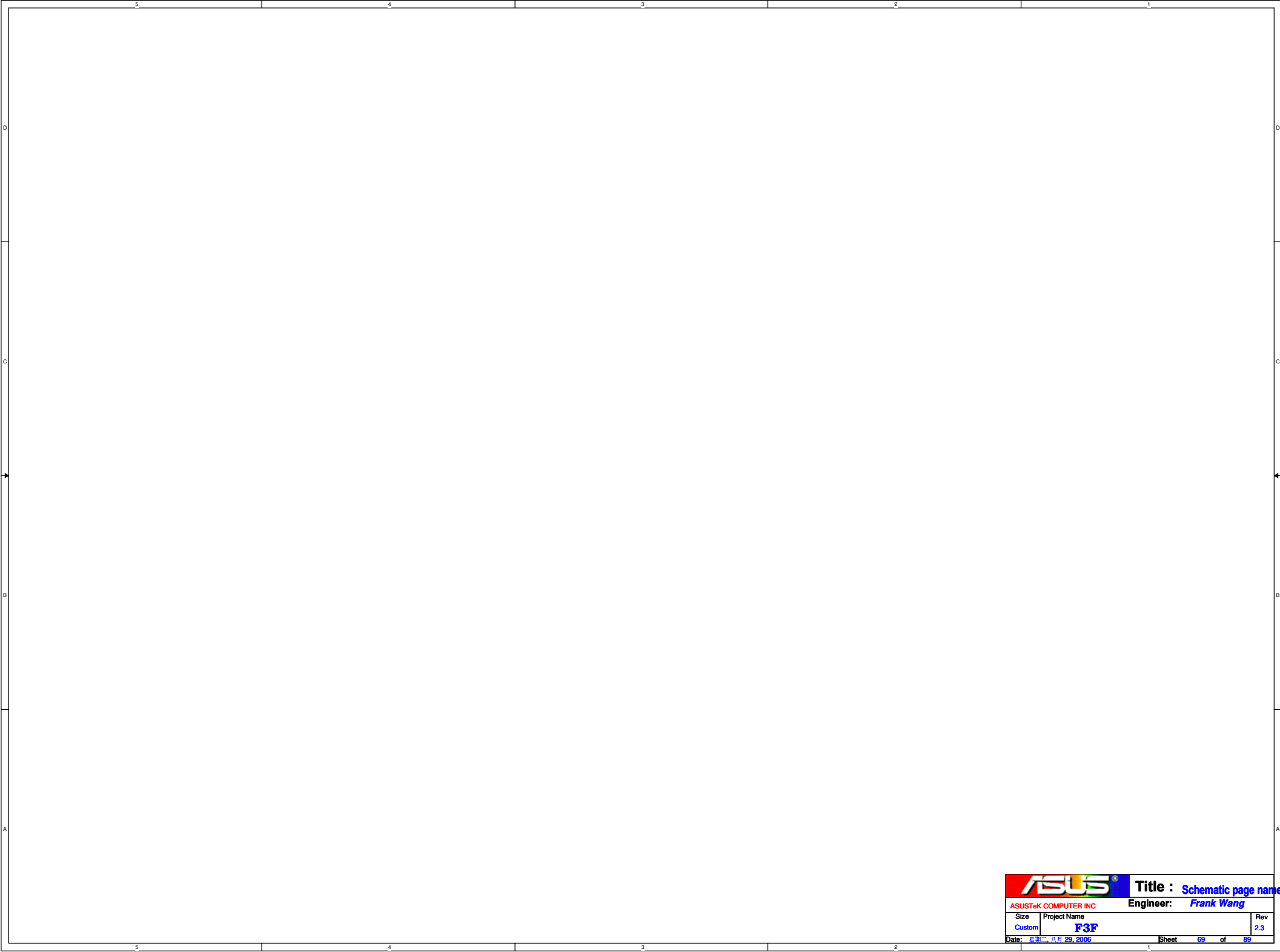


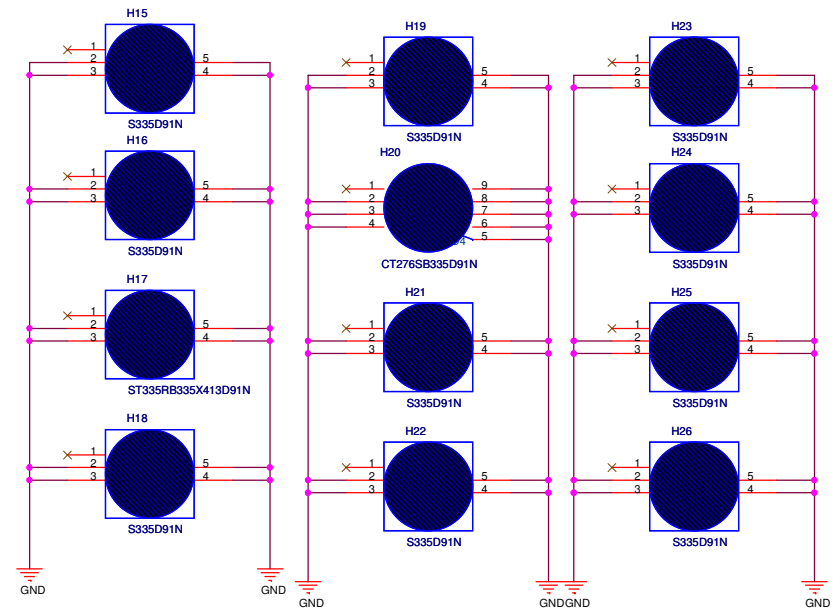
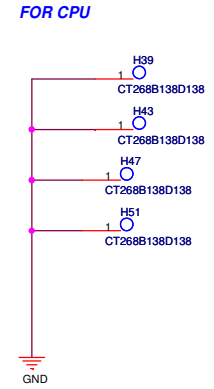
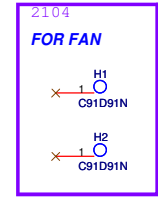
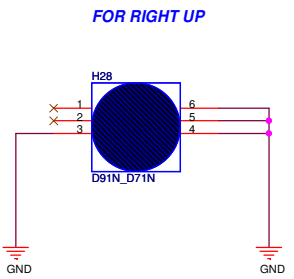
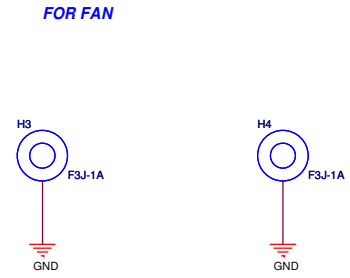
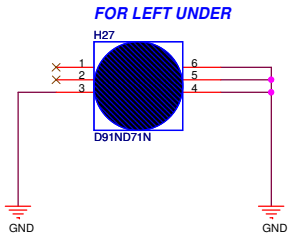


For Debug

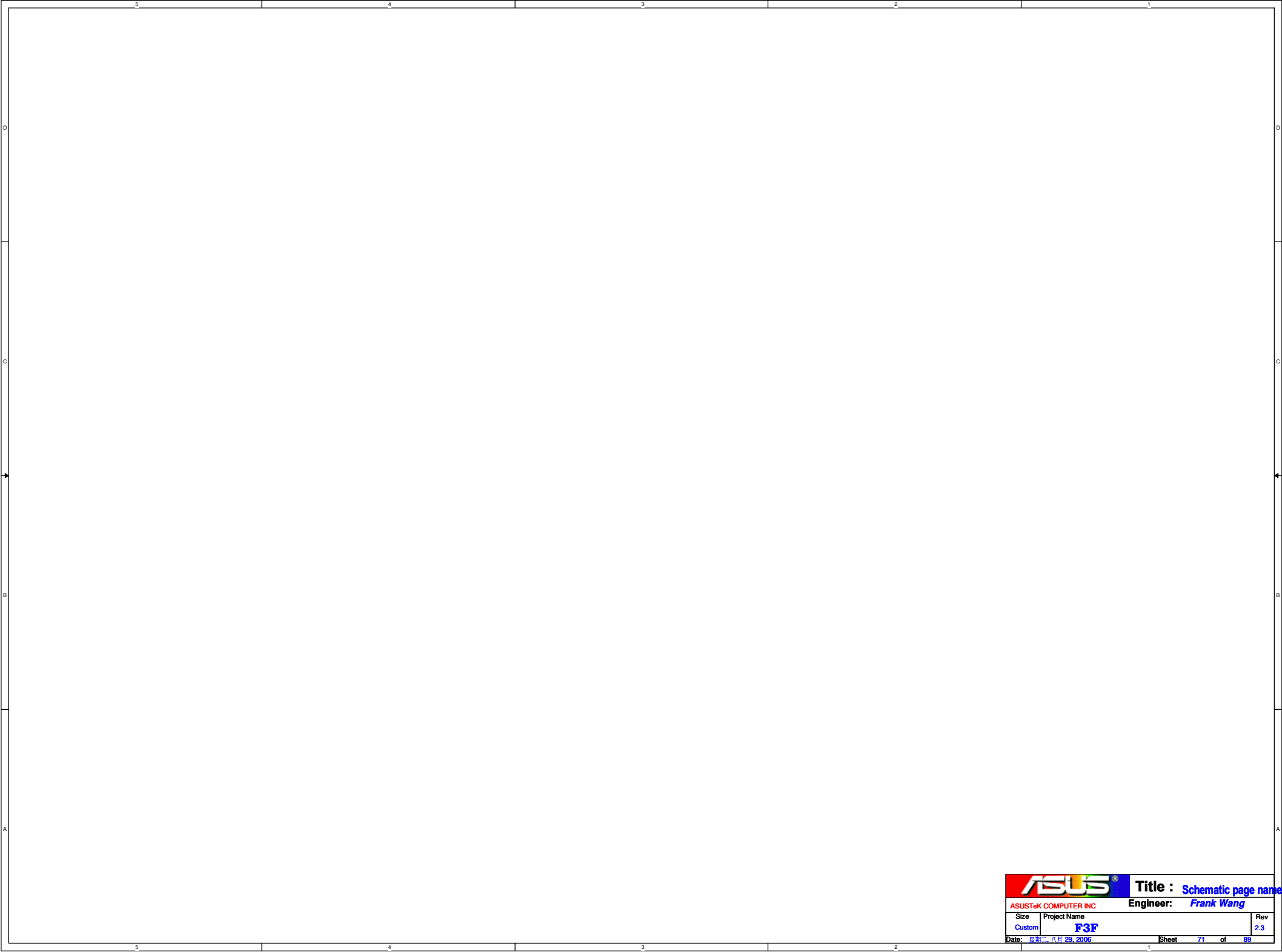




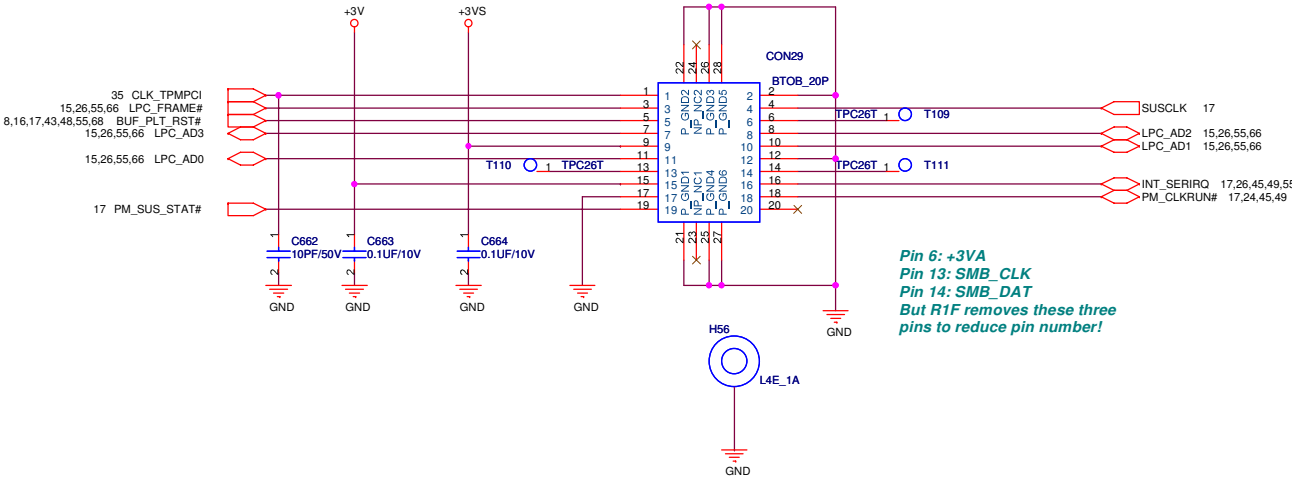


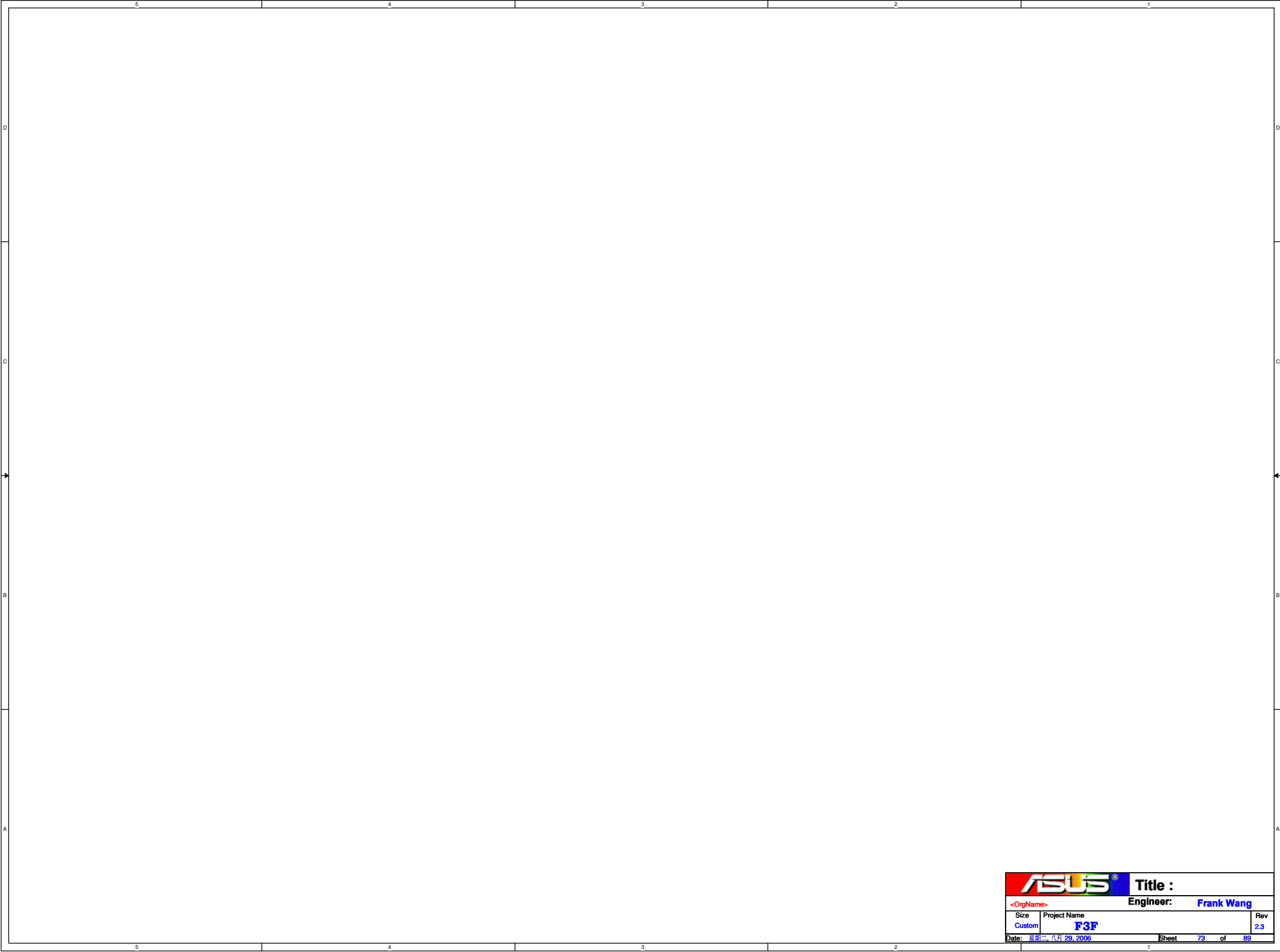


FOR SCREW HOLE

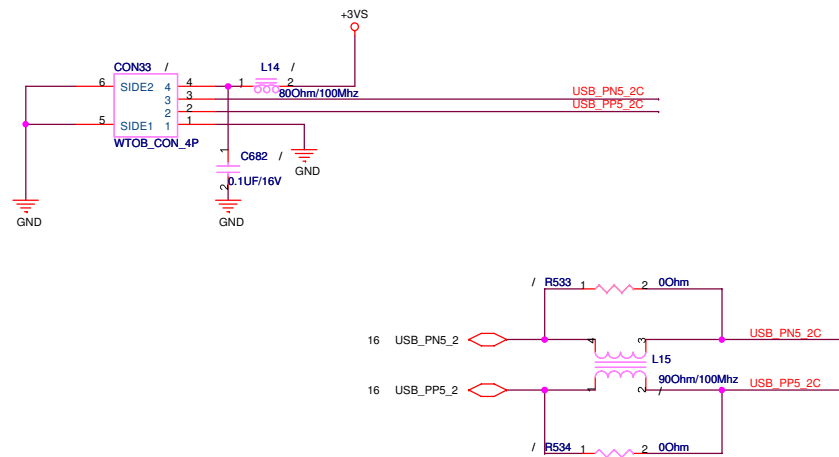


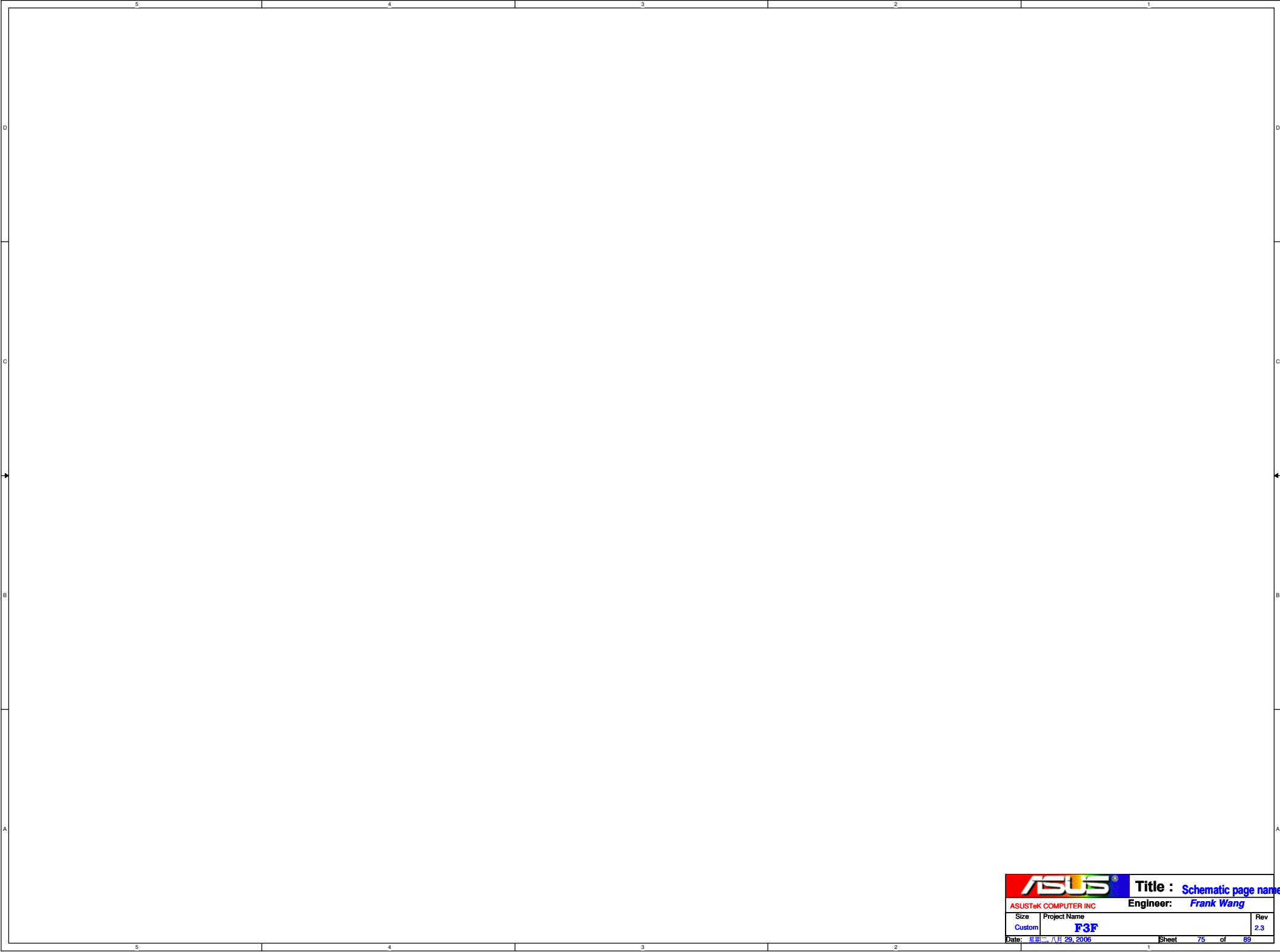
For TPM Module



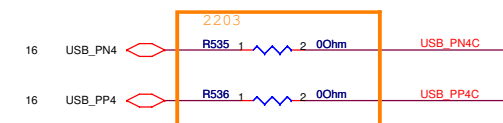
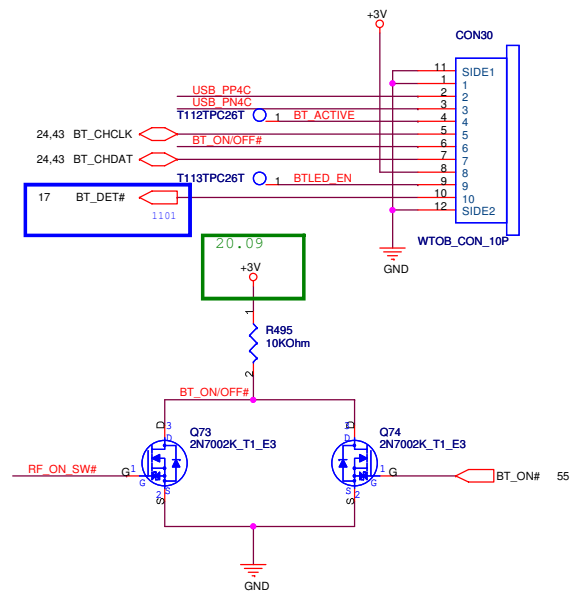


		Title :	
<OrigName>		Engineer: Frank Wang	
Size	Project Name		Rev
Custom	F3F		2.3
Date: 星期二, 八月 29, 2006		Sheet	73 of 89

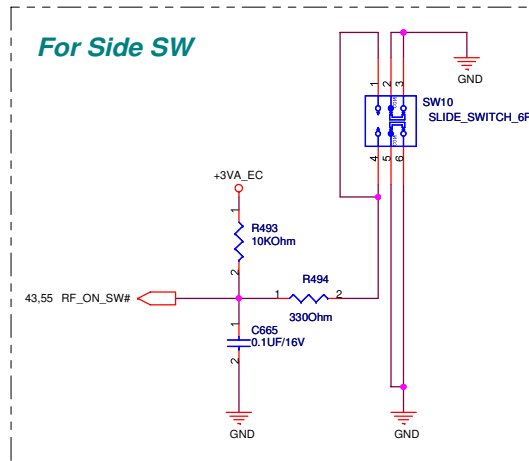


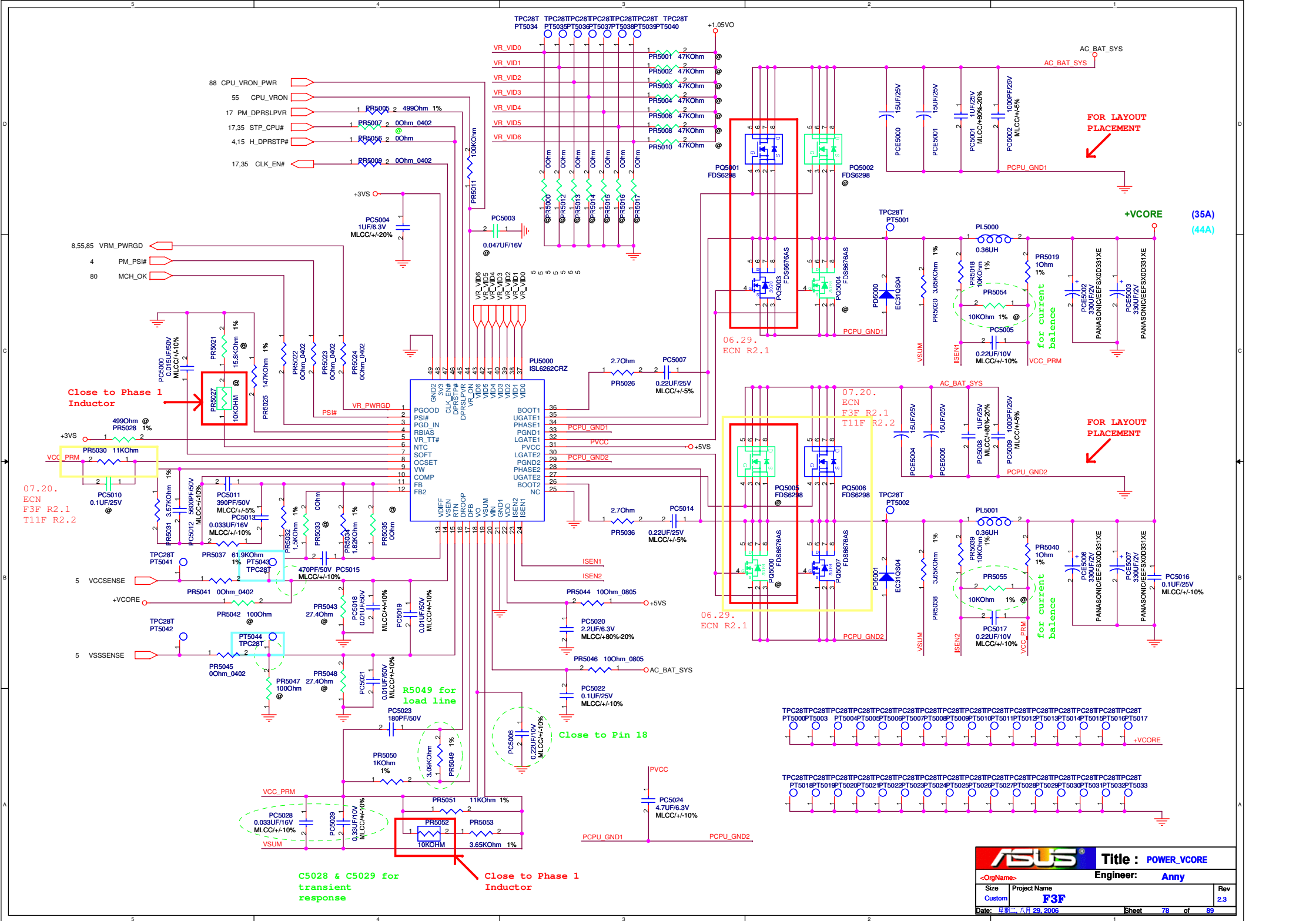


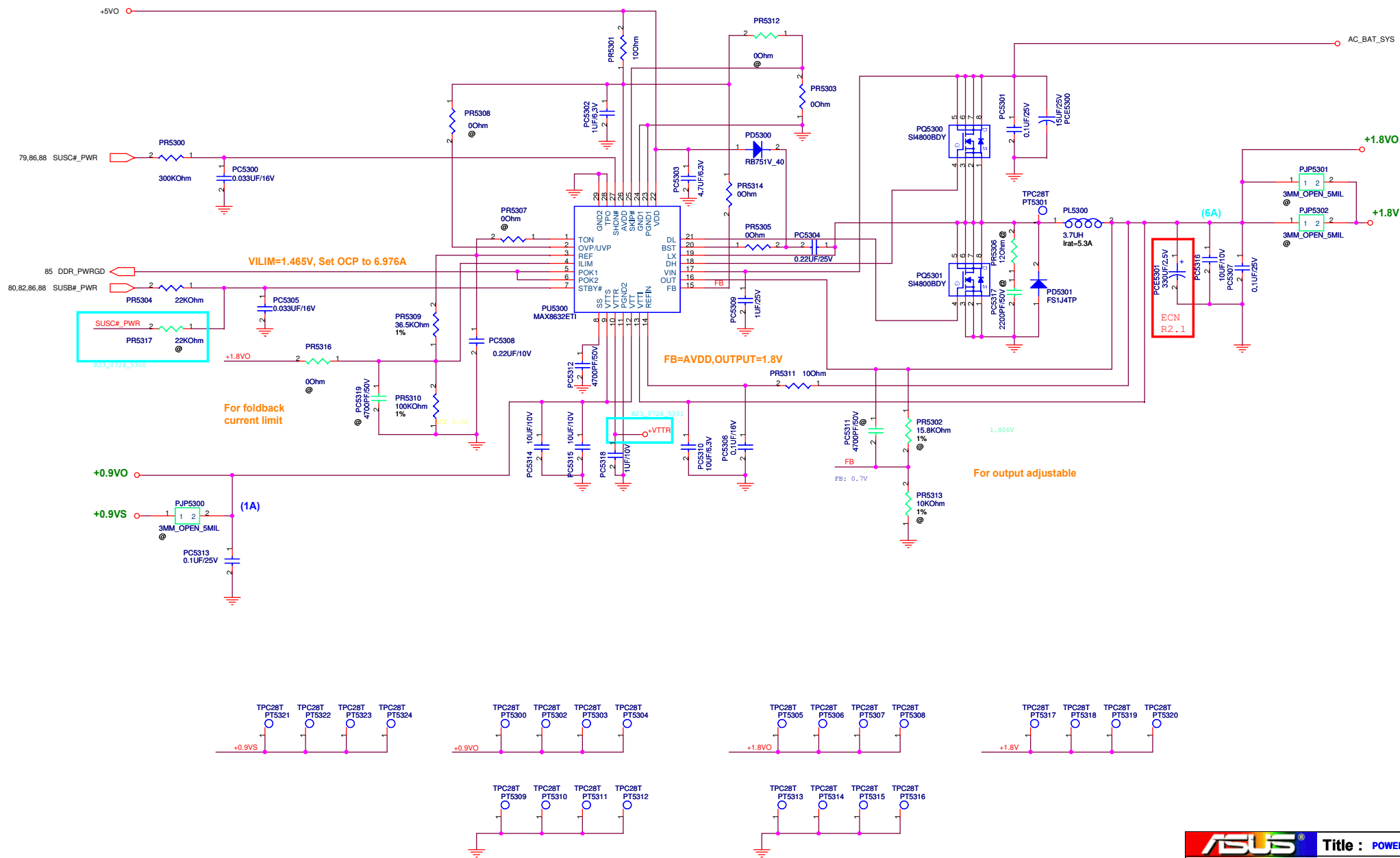
For Bluetooth



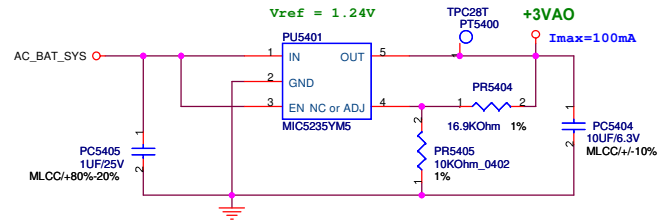
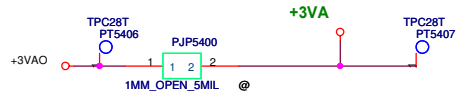
For Side SW



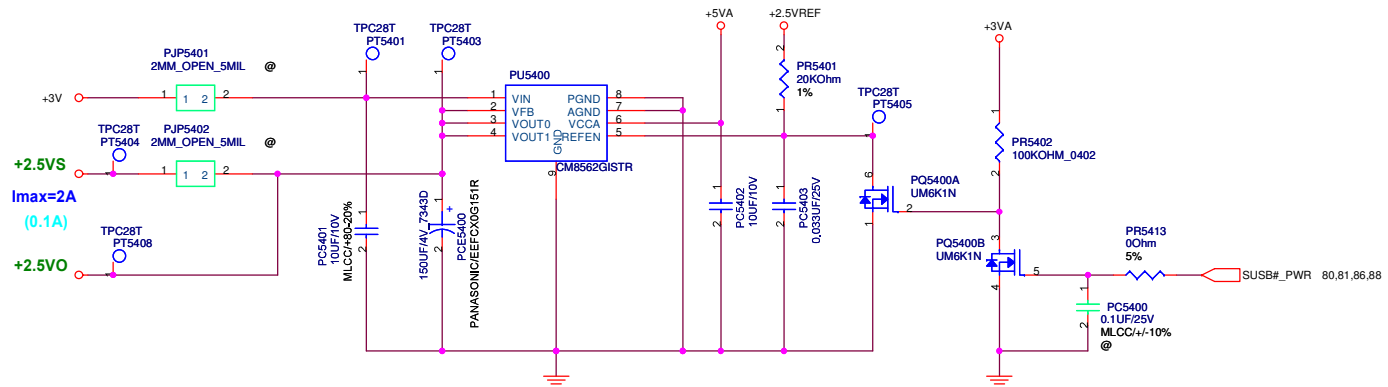




+3VAO

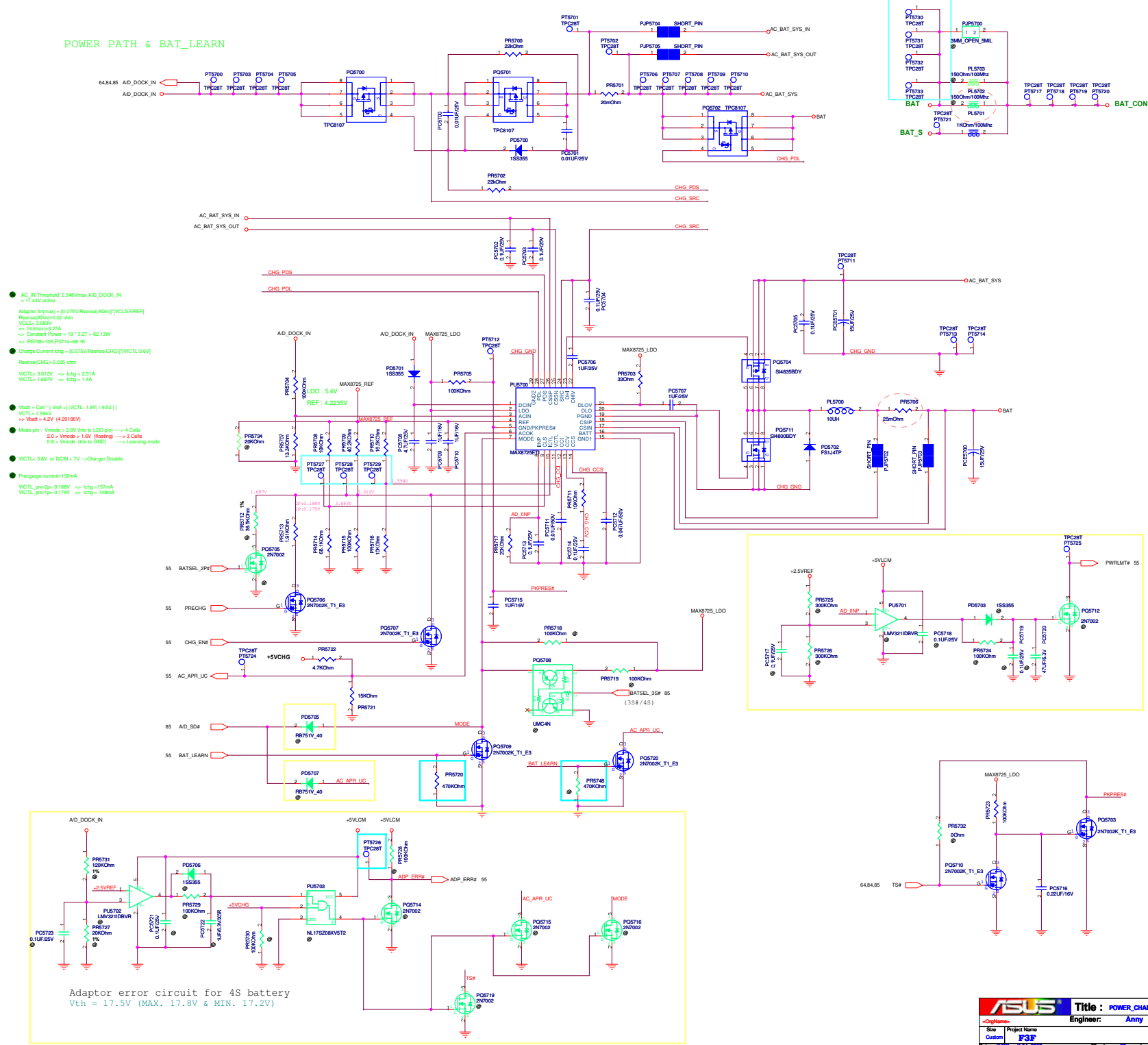


+2.5VS



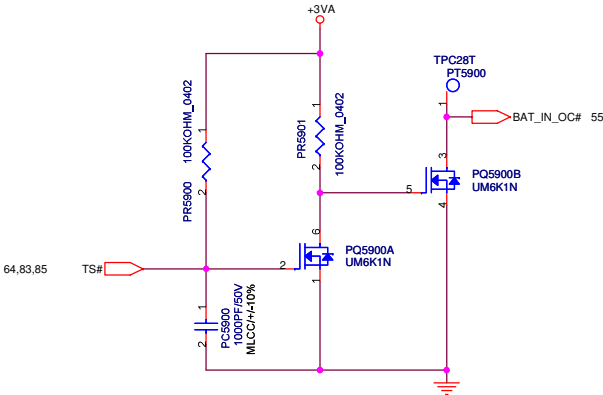
POWER PATH & BAT_LEARN

- AC_IN Threshold 2.048Vmax AD_DOCK_IN
> 17.44V active
Adapter In(max) = $[0.075V/Rsense/Adm][TVOL5-VREF]$
Resense(42m)/0.022 ohm
VOL5= 5.683V
=> In(max)= 2.27A
=> Constant Power = $19 \times 3.27 = 62.13W$
=> RS708=10K,RS714=68.1K
- Charge Current Ichg = $[0.075V/Rsense/CHG][TVICTL/3.6V]$
Resense(42m)/0.022 ohm
VICTL= 3.012V => Ichg = 251A
VICTL= 1.687V => Ichg = 1.4A
- Vbat = Cell * Vref * (VICTL - 1.8V) / 9.521
VICTL= 1.594V
=> Vbat = 4.2V (4.20188V)
- Mode pin : Vmode > 2.8V (tied to LDO pin) => 4 Cells
2.8 > Vmode > 1.6V (floating) => 3 Cells
0.8 > Vmode (tied to GND) => Learning mode
- VICTL< 0.8V or DCIN < 7V => Charger Disable
- Precharge current=150mA
VICTL_pre-2p= 0.188V => Ichg =157mA
VICTL_pre-1p= 0.179V => Ichg = 149mA

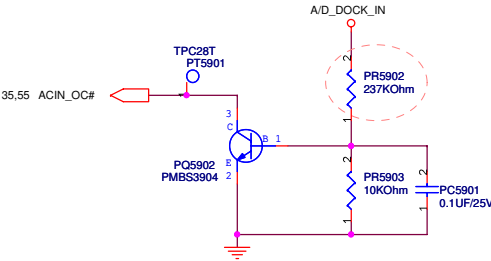


Adaptor error circuit for 4S battery
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

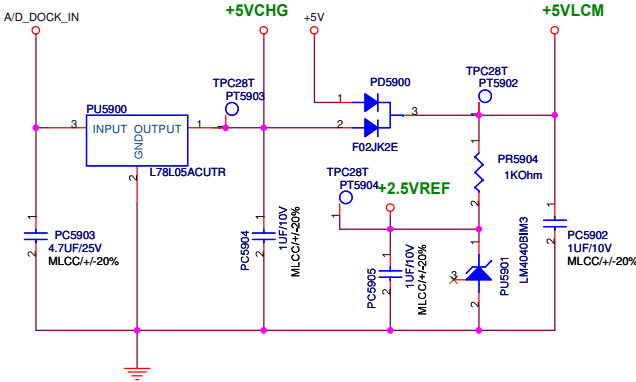
BATTERY IN DETECT



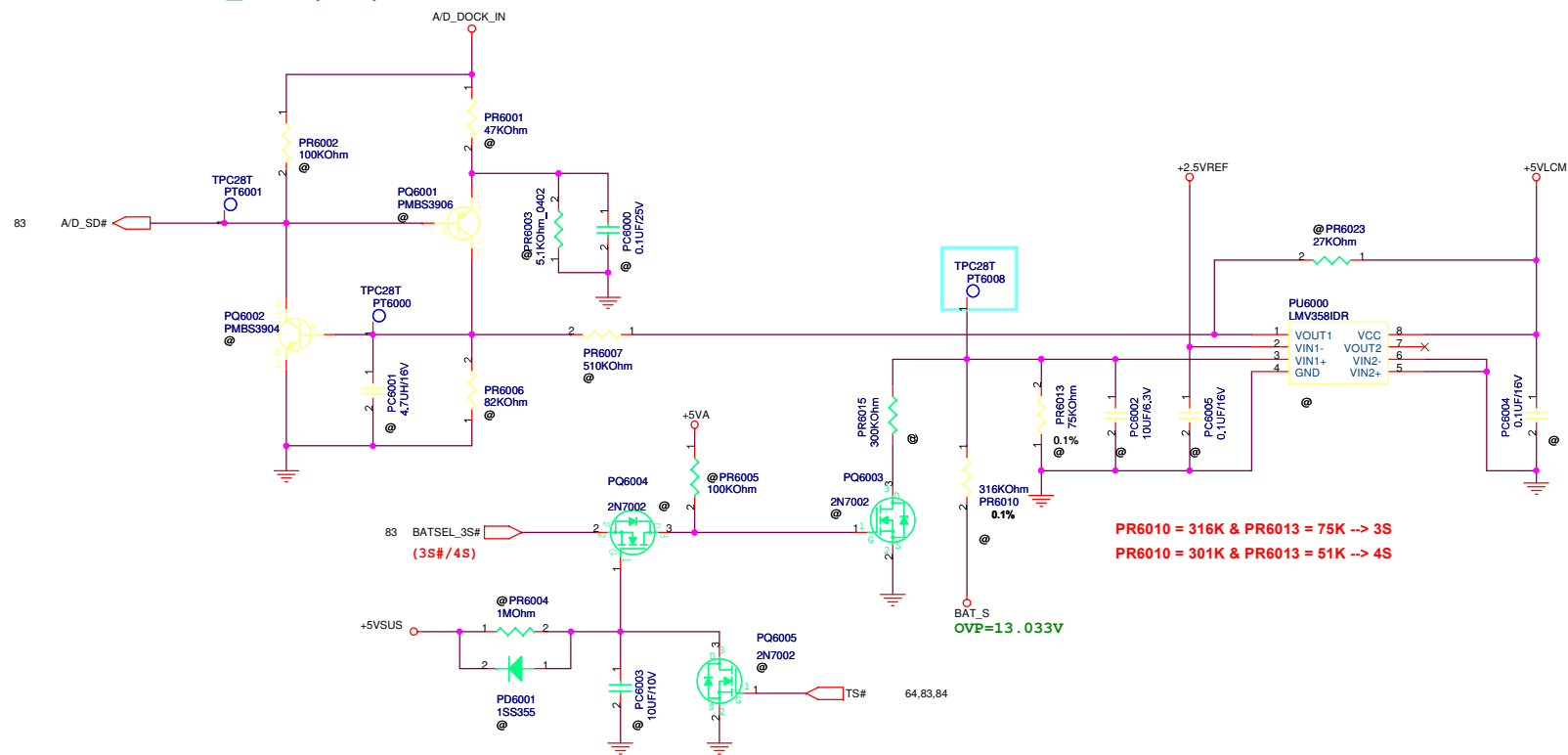
ADAPTER IN DETECT



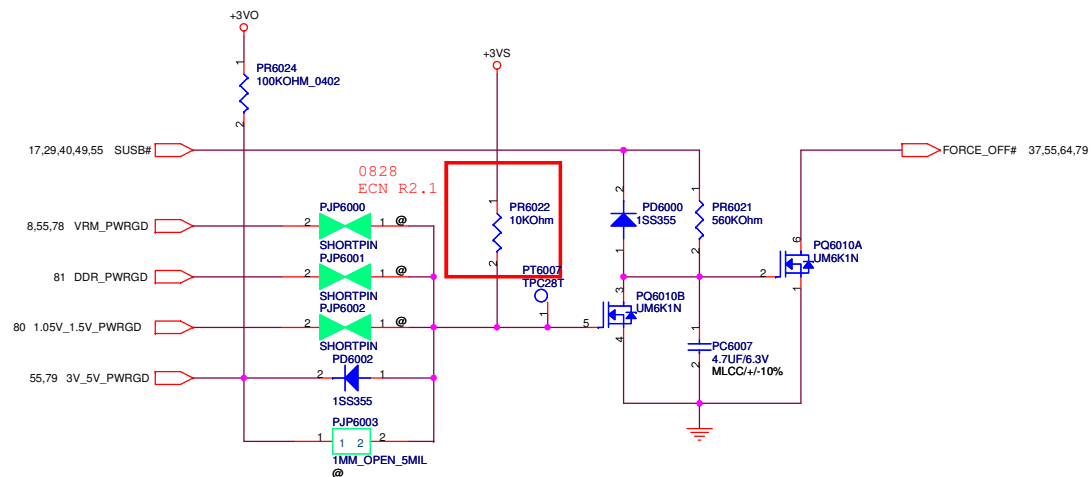
+5VLCM, +5VCHG & +2.5VREF



BATTERY A/D_SD# (OVP)



POWER GOOD DETECTOR



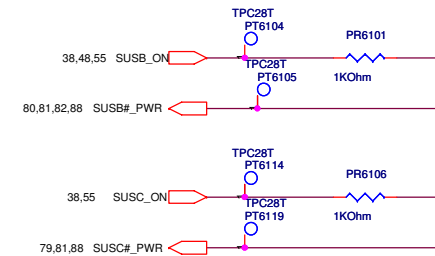
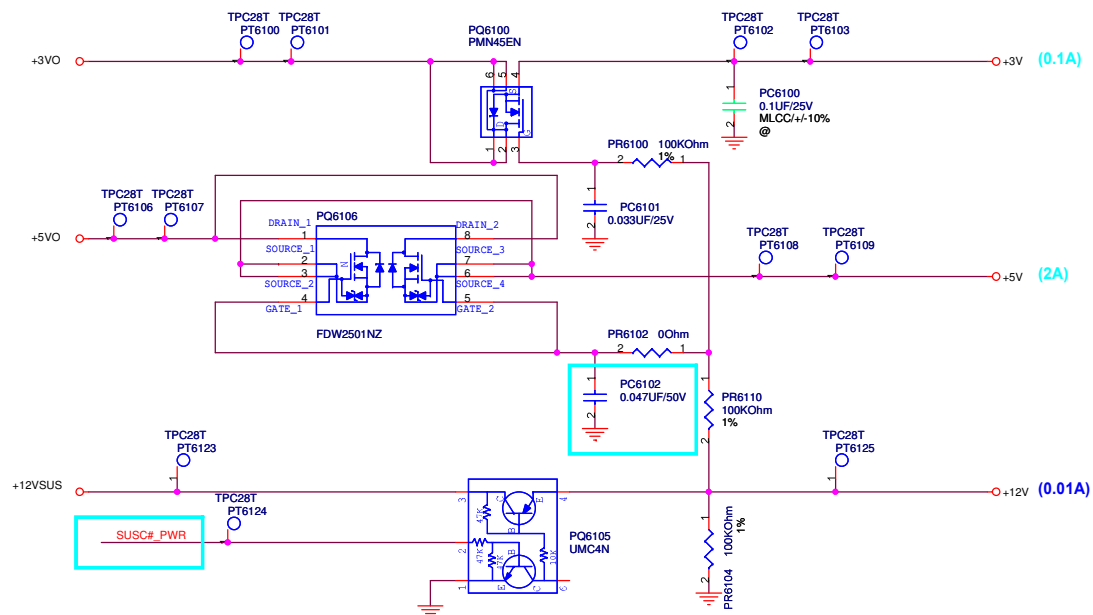
TPC28T PT6003 1 VRM_PWRGD

TPC28T PT6004 1 DDR_PWRGD

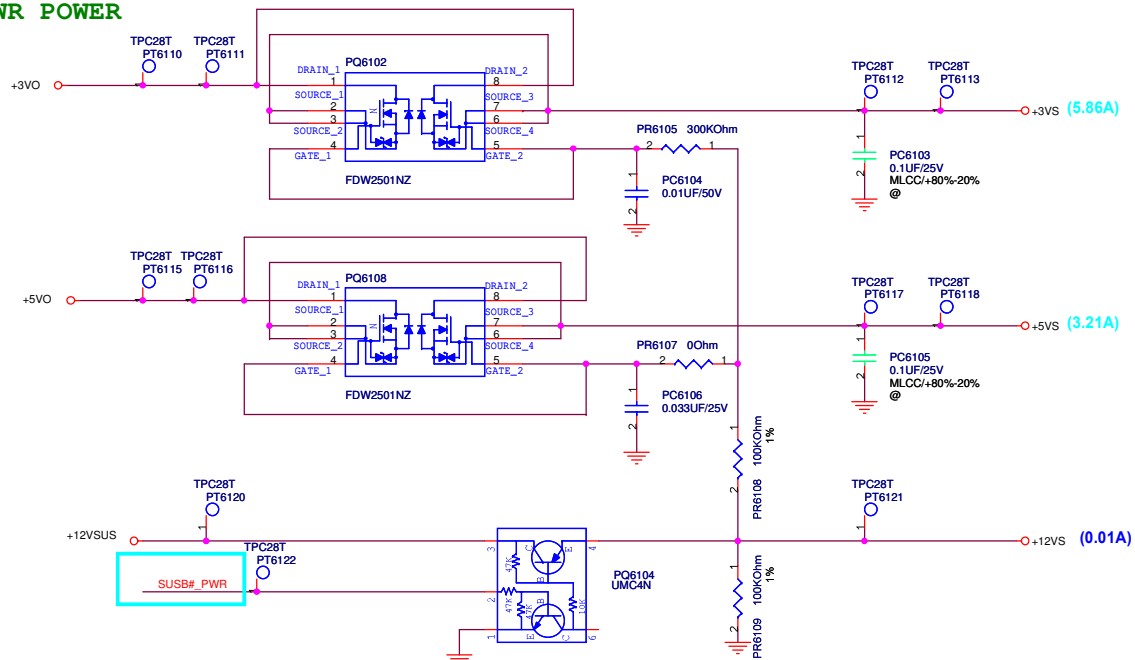
TPC28T PT6005 1 3V_5V_PWRGD

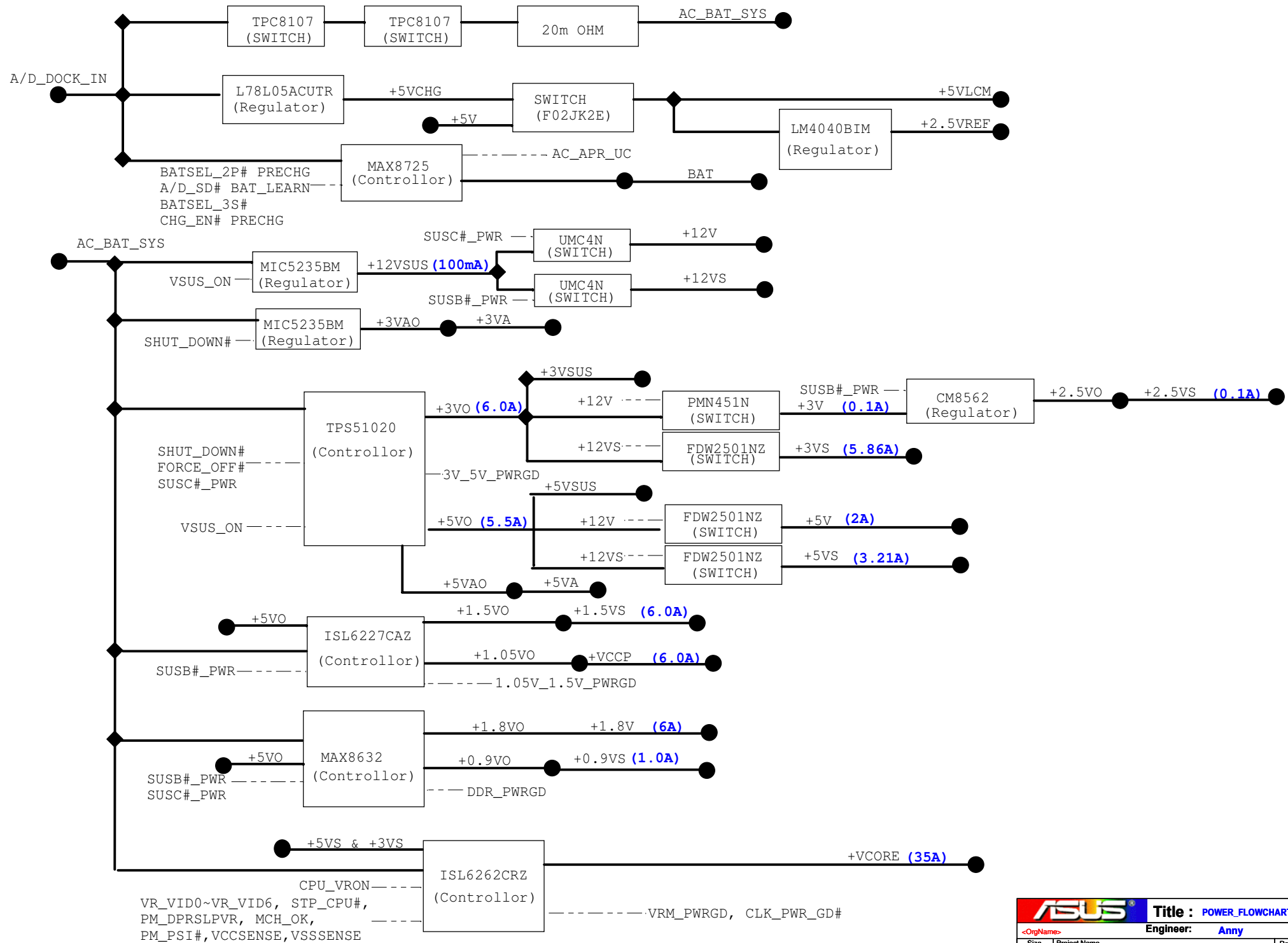
TPC28T PT6006 1 1.05V_1.5V_PWRGD

SUSC#_PWR POWER



SUSB#_PWR POWER





AC_BAT_SYS ○ → AC_BAT_SYS 29,64,78,79,80,81,82,83

+3VA ○ → +3VA 15,29,37,38,55,82,84

+5VA ○ → +5VA 26,79,82,85

+5VO ○ → +5VO 79,80,81,86

+3VO ○ → +3VO 79,80,85,86

+3VSUS ○ → +3VSUS 16,17,18,40,41,43,48,79

+5VSUS ○ → +5VSUS 18,26,62,79,85

+3V ○ → +3V 24,26,29,38,41,43,49,50,72,76,82,86

+3VS ○ → +3VS 8,9,12,16,17,18,20,21,24,28,29,31,33,35,38,43,45,46,47,48,49,52,53,55,66,68,72,74,78,80,85,86

+12VSUS ○ → +12VSUS 79,86

+12V ○ → +12V 38,47,53,86

+12VS ○ → +12VS 29,53,62,86

+5V ○ → +5V 12,29,38,45,50,58,84,86

+5VS ○ → +5VS 17,18,24,26,28,33,38,52,53,55,56,62,68,78,86

+2.5VO ○ → +2.5VO 82

+2.5VS ○ → +2.5VS 8,12,28,38,52,82

+1.8VO ○ → +1.8VO 81

+1.8V ○ → +1.8V 8,11,20,21,22,38,49,81

+VCCP ○ → +VCCP 4,7,18,35,38,80

+VCCP_AGTL+ ○ → +VCCP_AGTL+ 4,5,7,12

+VCCP_GMCH ○ → +VCCP_GMCH 7,11

+VCCP_ICH ○ → +VCCP_ICH 15,18

+0.9VS ○ → +0.9VS 22,38,81

BAT ○ → BAT 64,83

+5VCHG ○ → +5VCHG 83,84

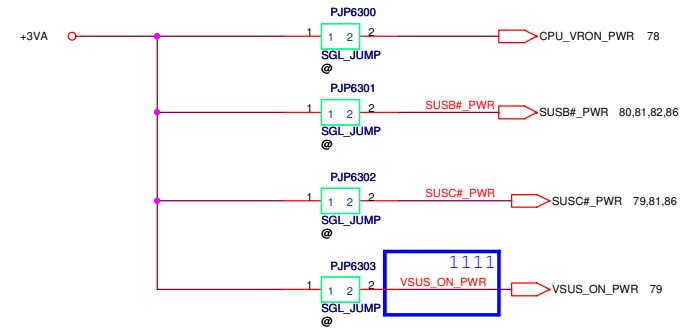
+5VLCM ○ → +5VLCM 62,83,84,85

+2.5VREF ○ → +2.5VREF 82,83,84,85

+VCORE ○ → +VCORE 5,78

BAT_CON ○ → BAT_CON 64,83

FOR POWER TEST



Rev	Date	Description
1.0	11/28/2005	1. Initial release.
1.1	01/13/2006	1. For RF Switch disable, BT can't detect by Wireless console issue, add BT detect pin. Page 17,74. 2. Change C676,C677 Package size. Page 41. 3. Fix 1394 connector pin reverse issue. Page 46. 4. Fix Battery connector ping reverse issue. Page 64. 5. Add Capacity CE20, C53, C54, C55, C56, C57, C58, for 3DMark screen become to one color and hang issue. Page 11. 6. Change L51 Package size. Page 29. 7. Change X1 & X6 for cost down. Page 15,55. 8. Remove Fan 3 pin design circuit. Page 33,55. 9. Fix debug connector pin reverse issue. Page 66. 10. Fix LID Switch can't disable backlight issue, change NB BL_EN net name to BKLTEN. Page 9,29. 11. Fix VSUS_ON_PWR and SUSC#PWR Net connect issue. Page 88. 12. Remove Cardbus PME signal for R5C832. Page 45. 13. Add AC Adaptor Voltage Error Signal to EC, and EC will show the abnormal by LED. Page 55. 14. Remove L107,D37,CE17,CE18 for cost down. Page 58. 15. Change Connector CON15,J2,CON11,CON17,CON27,CON22&CON7&CON8,J3&J4. Page 28,53,41,48,68,31,22,64. 16. Modify Audio schematic Change C578,C579 to 0.47UF and remove R403,R404,R405,R398,R399,R408,R409,R410,C603,C604. Page 52,53. 17. Change R351 to 22 ohm. Page 15. 18. Add C59 for EMI. Page 47. 19. Charger circuit add component. Page 83. 20. Change TPLED_ON GPIO pin from GPIO19 to GPIO14 and R55 10K ohm pull low. Page 17. 21. Depop circuit remove OP_SD# control function. Page 53,55. 22. Add Mic. Preamplifer circuit. Page 52. 23. Change CE9,CE10 position for pop noise. Page 53. 24. Add buffer U5 for HSYNC and VSYNC of CRT signal. Page 9,28. 25. Add RN28,R156 near debug connector to be LPC terminal resistor. Page 66. 26. Change R233,R234,R235,R236 to L107,L108,L109,L110 for EMI. Page 53.
2.0		1. Colay Audio circuit for STAC9200 and ALC660. Remove Mic. Pre-Amplifer circuit. Page 52,53. 2. Modify minicard latch connector to nut.(H57,H58) Page 43. 3. Change SATA Connector. Page 68. 4. Add +3V LDO circuit for TV_DAC Power. Page 12.

Rev	Date	Description
		5. Remove R96,R97,R524 for Fan circuit. Page 33. 6.Add some test point for factory request. 7.Change BT_ON# from SB GPIO to EC GPIOE7. Page 17,55. 8.Add MOS for EC leakage of electricity issue.Page 55. 9.Change BT logic power from +3VS to +3V for WHQL S3 test .Page 76. 10.For Lan -ve test issue,add terminal resistor near the transformer .Page 41. 11.For ACZ RST will let Sigmatel codec GPIO0 high issue, add C177 to deploy depop time to avoid pop from speaker .Page 53.
2.1	04/24/2006	1.Change internal Mic. bias voltage from +5V_AUDIO to +2.5VS. Page 52. 2.Add D52,D53 to protect EC. Page 55. 3.Add C178,C179 for new card clock. Page 48. 4.Add H1,H2 for Fan. Page 70. 5.Remove RN2,RN3 for Vcore VID. ESD Request. Page 5. 6.Add R87 for moat issue. Page 53.
2.2	05/25/2006	1.Change CarBus R5C841 1394 Pull High from TPB to TPA. Page 50. 2.Add U46,C742,C743,R572,R573,R574 LDO circuit for internal Mic. Pull high +2VS. Add R575,C745 for +2.5VS Low Pass Filter. Page 52. 3.Remove L17,L64,L84,L86,L87,L90 Co-Lay circuit. Page 76,48,58.
2.3	07/24/2006	1.Change DDR2 VREF Voltage from 0.9VS to 0.9V. Add L53,PR5317 from Power IC and R753,R754,C202,C203 from 1.8V. Page 22,81. 2.Change C59 connect from MS_DAT0 to MSCLK. Page 47. 3.Add R88,R89 for VISTA cost down with 100uF. Page 53. 4.For EMI Request, add C180 to SPDIF signal and near the codec. Page 52.
F3F ↓ F3H	01/04/2007	1. Page28 : Change CRT filter from 24p-75-10p to 10p-47-10p. 2. Page53 : Change Q77 from 2N7002 to DTC144EK , R563 from 100K to 4.7K for ESD issue 3. Change all 2N7002 to 2N7002K for ESD issue. 4. Change PC5706 from 0.1uF to 1uF to reduce MAX8725 Vref shift.