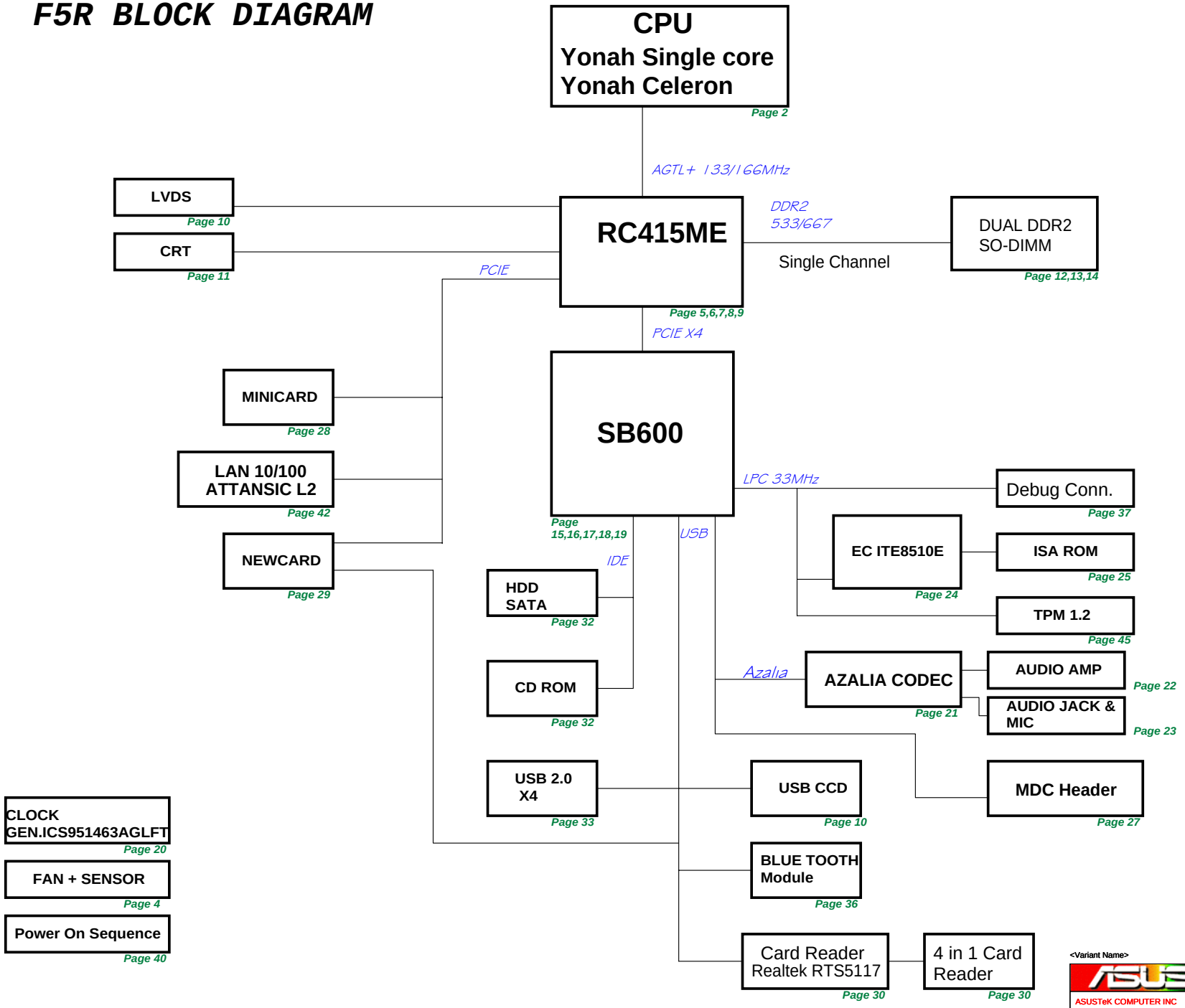
F5R BLOCK DIAGRAM



<Variant Name>

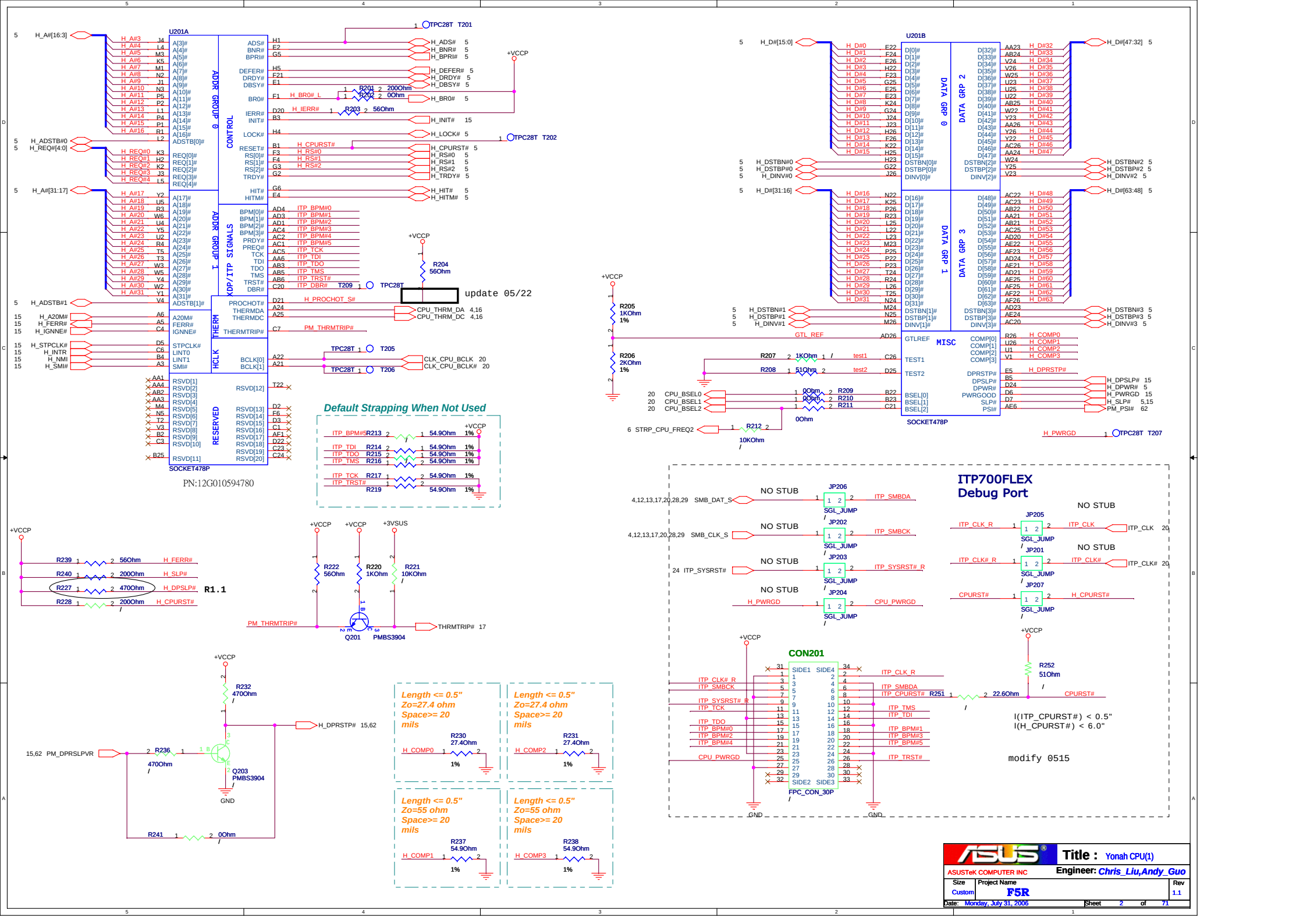
Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

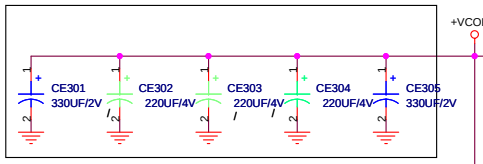
Engineer: Chris Liu,Andy Guo

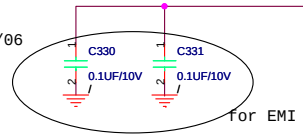
Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 1 of 71

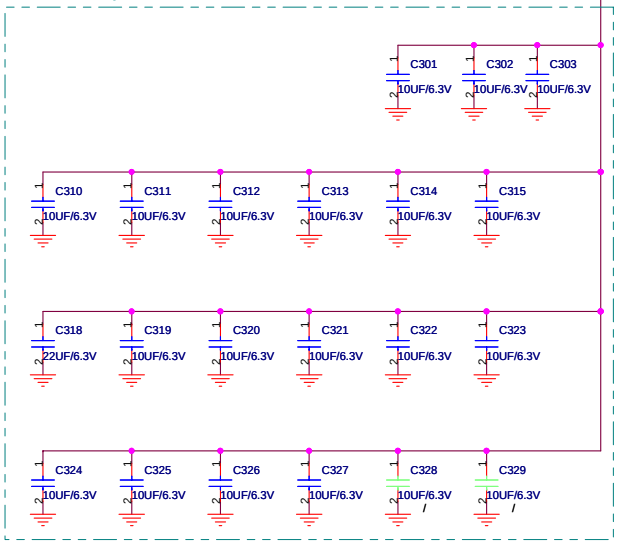

U201A
U201B
SOCKET478P
PN:12G010594780
update 05/22
Default Strapping When Not Used
R1.1
ITP700FLEX
Debug Port
NO STUB
CON201
FPC_CON_30P
I(ITP_CPURST#) < 0.5"
I(H_CPURST#) < 6.0"
modify 0515
Length <= 0.5" Zo=27.4 ohm Space>= 20 mils
Length <= 0.5" Zo=55 ohm Space>= 20 mils
Title : Yonah CPU(1)
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 2 of 71

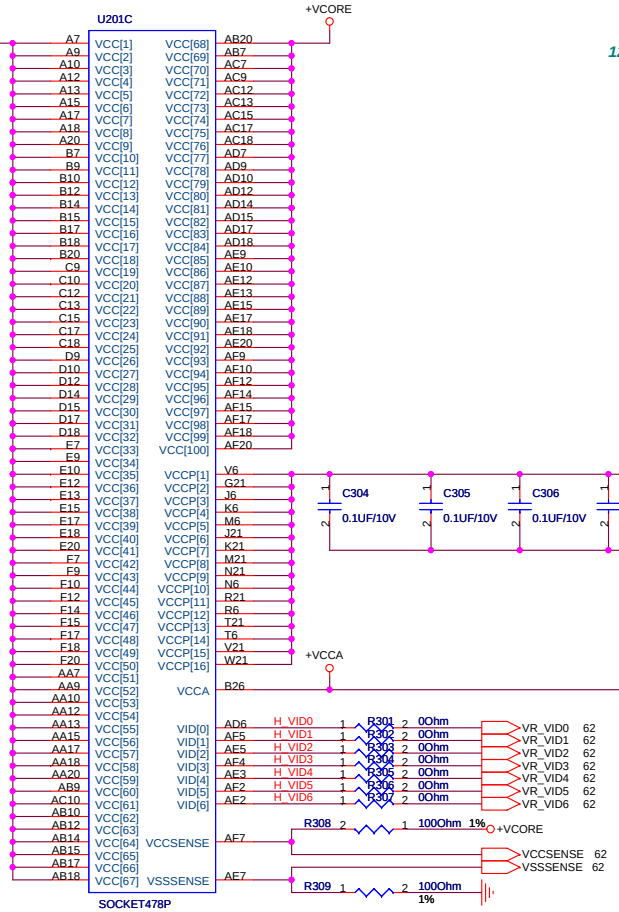
R1.1

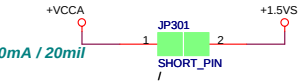




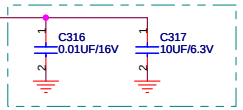
CPU +VCORE
Mid-Frequency
Capacitors

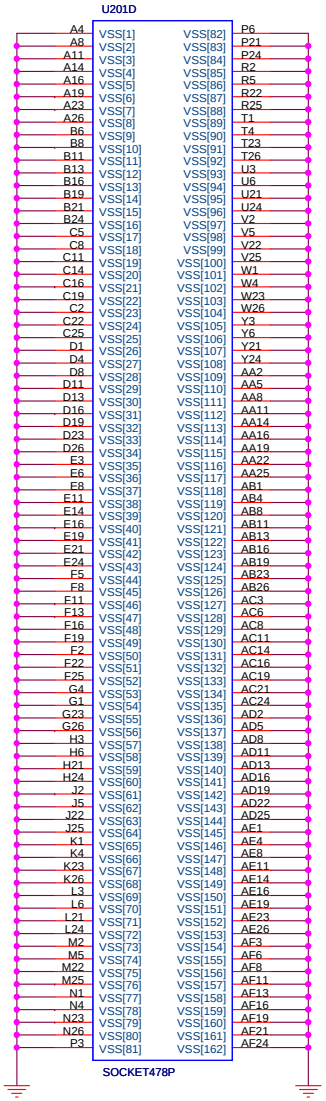






+VCCA
Decoupling
Capacitors

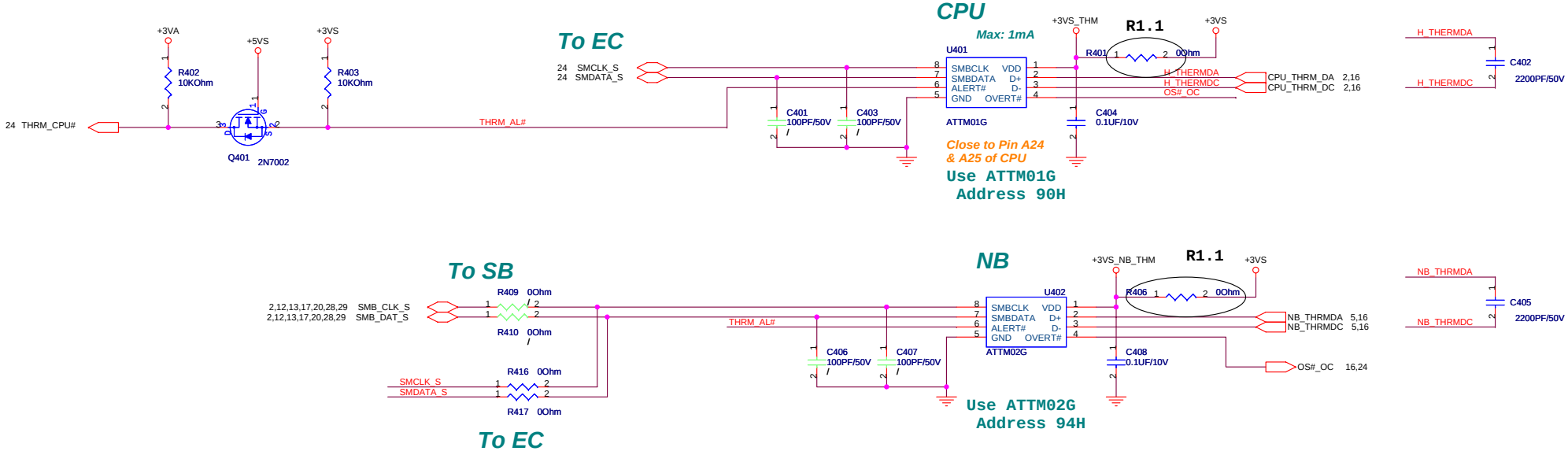




+VCORE Low-Freq Capacitor
*Intel: 330UF *6*
*ATI: 330UF *6*
*R1F: 330UF *4*
*A7J: 330UF *5*
*F5X: 330UF *5*
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*ATI: 10UF *26*
*R1F: 22UF *16*
*A7J: 22UF*29 use 19*
*A6RF: 22UF*21 use 21*
*F5X: 10UF *21 use 19*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*
*A7J: 220UF *1, 0,1UF *6*
*A6RF: 220UF *1, 0,1UF *6*
*F5X: 220UF *1, 0.1UF *6*

ASUSTeK COMPUTER INC	Title : Yonah CPU(2)	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 3 of 71	

Thermal Sensor

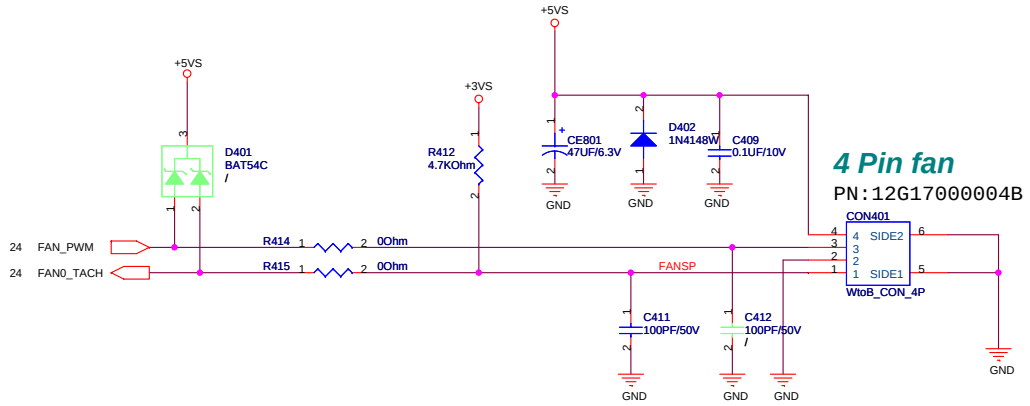


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



<Variant Name>

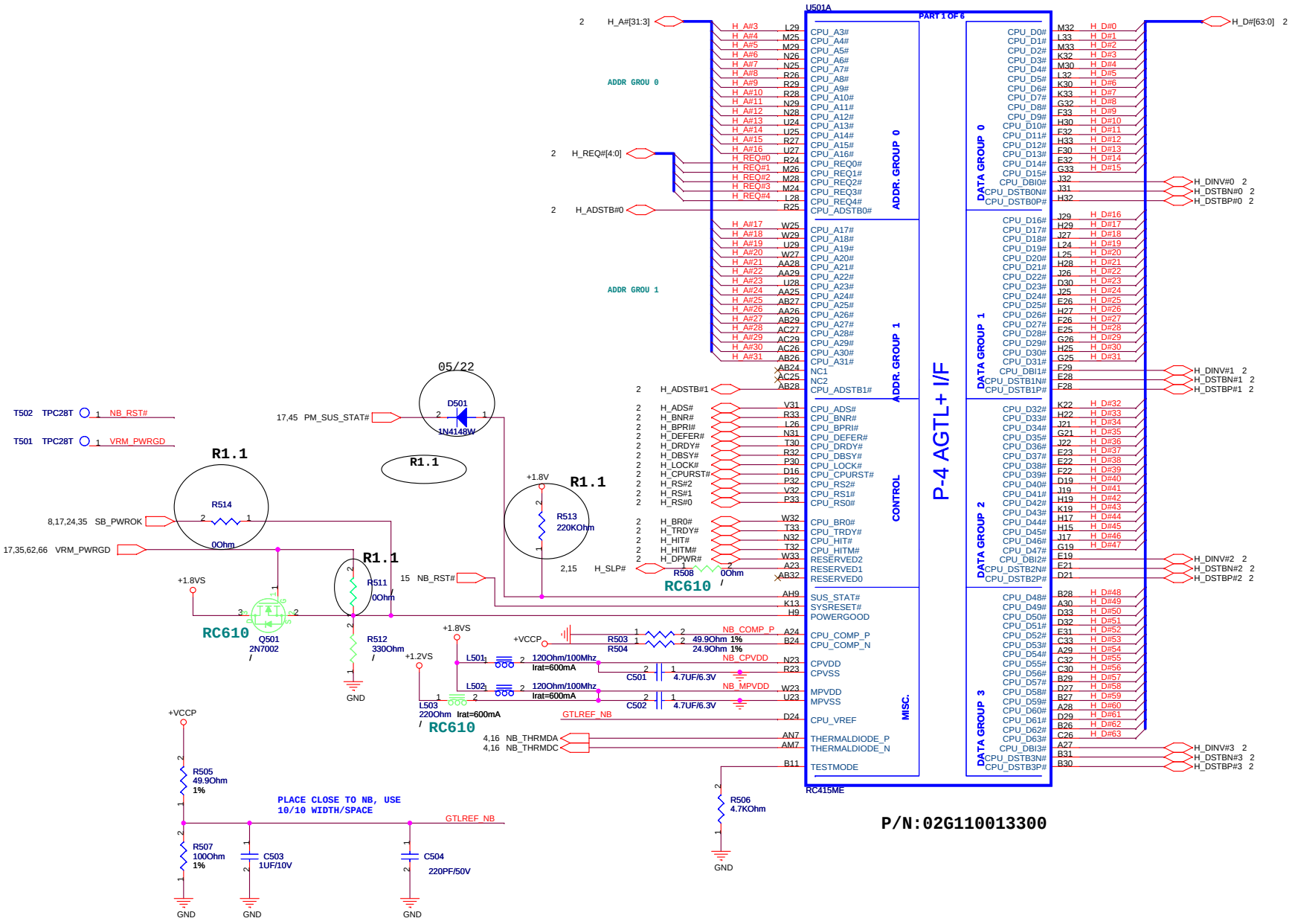
Title : THER SENSOR & FAN

ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 4 of 71



<Variant Name>

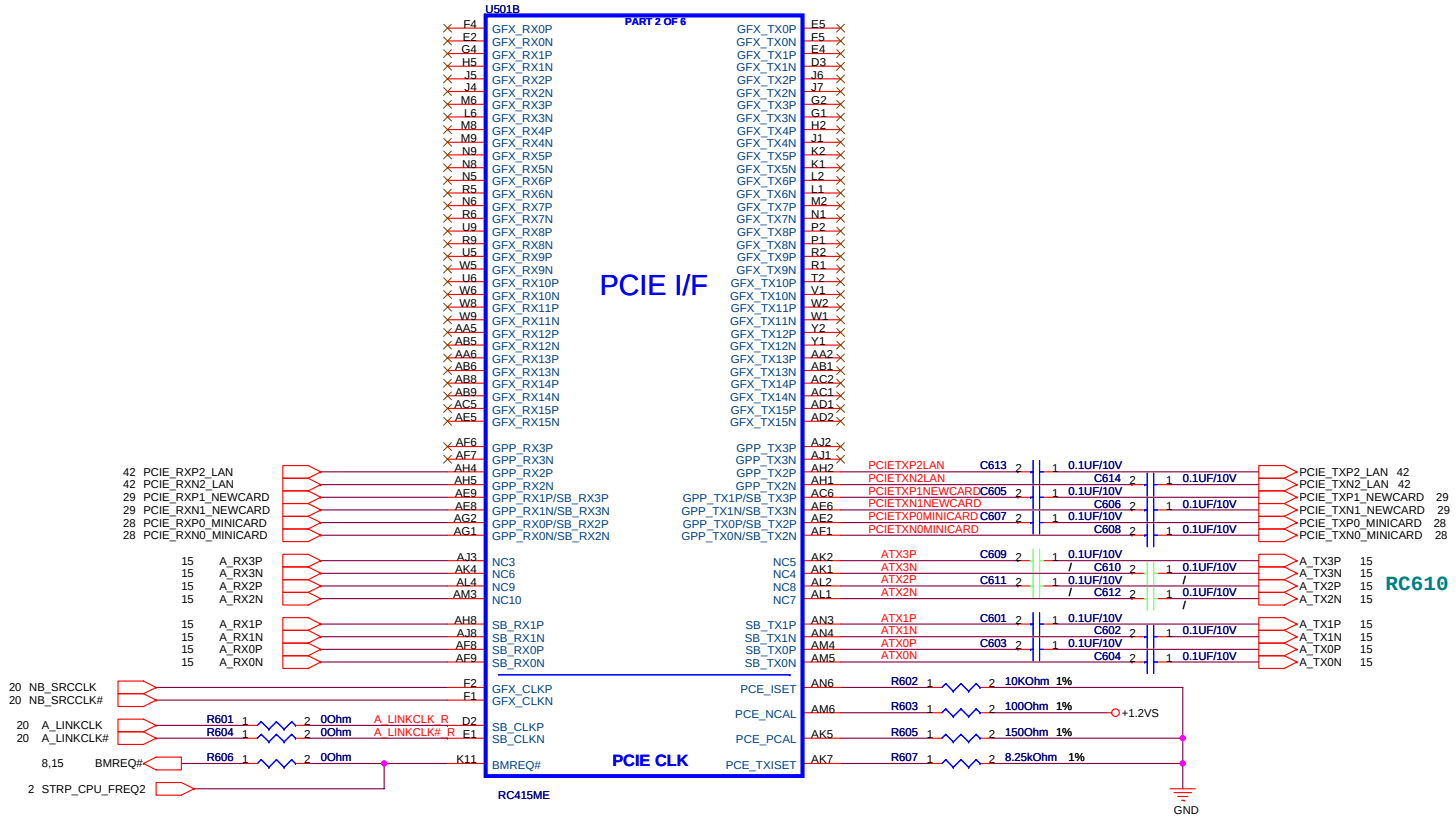
ASUSTeK COMPUTER INC

Title : RC415M(HOST)

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 5 of 71



<Variant Name>

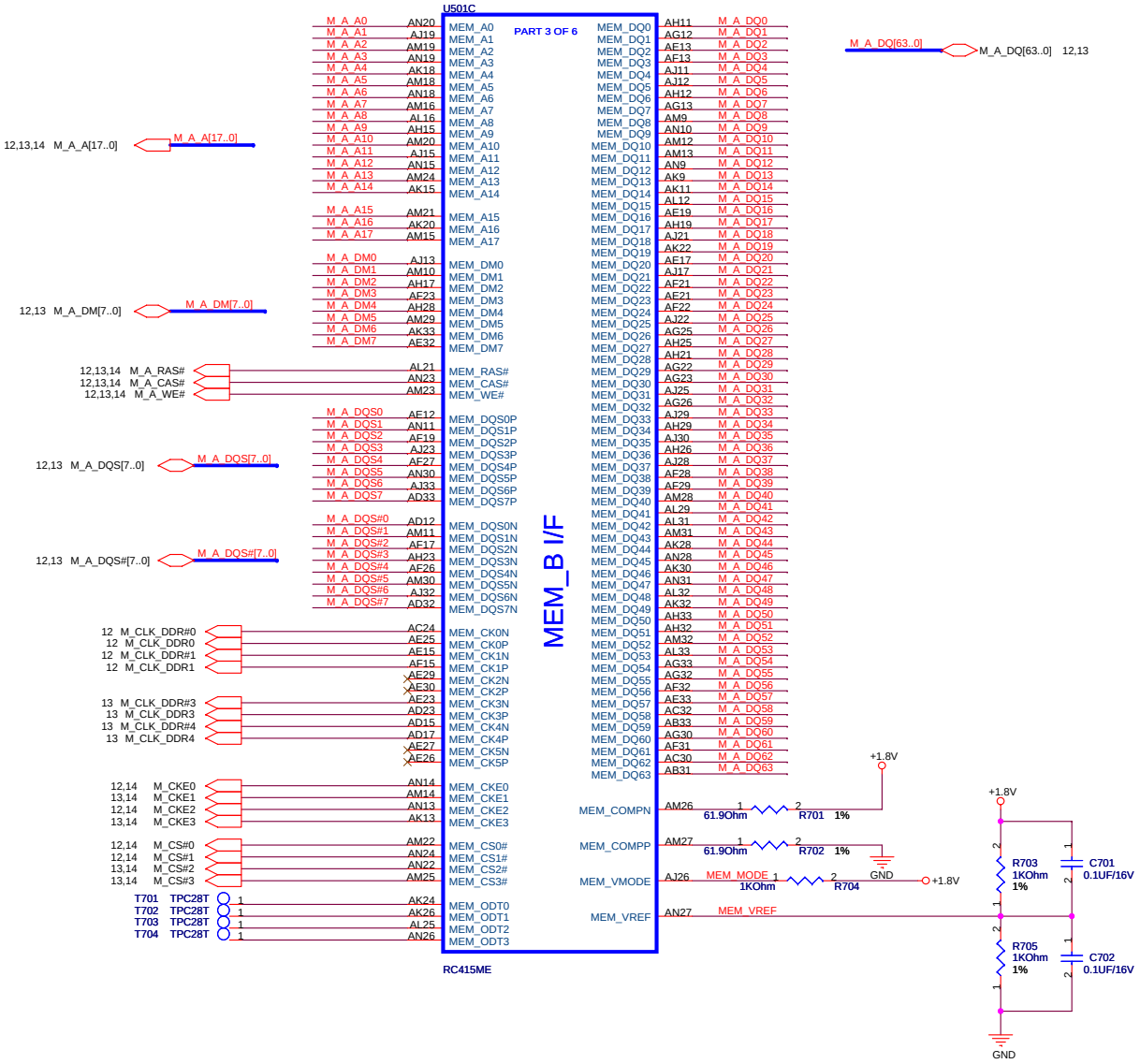
Title : RC415M(2)

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 6 of 71



<Variant Name>

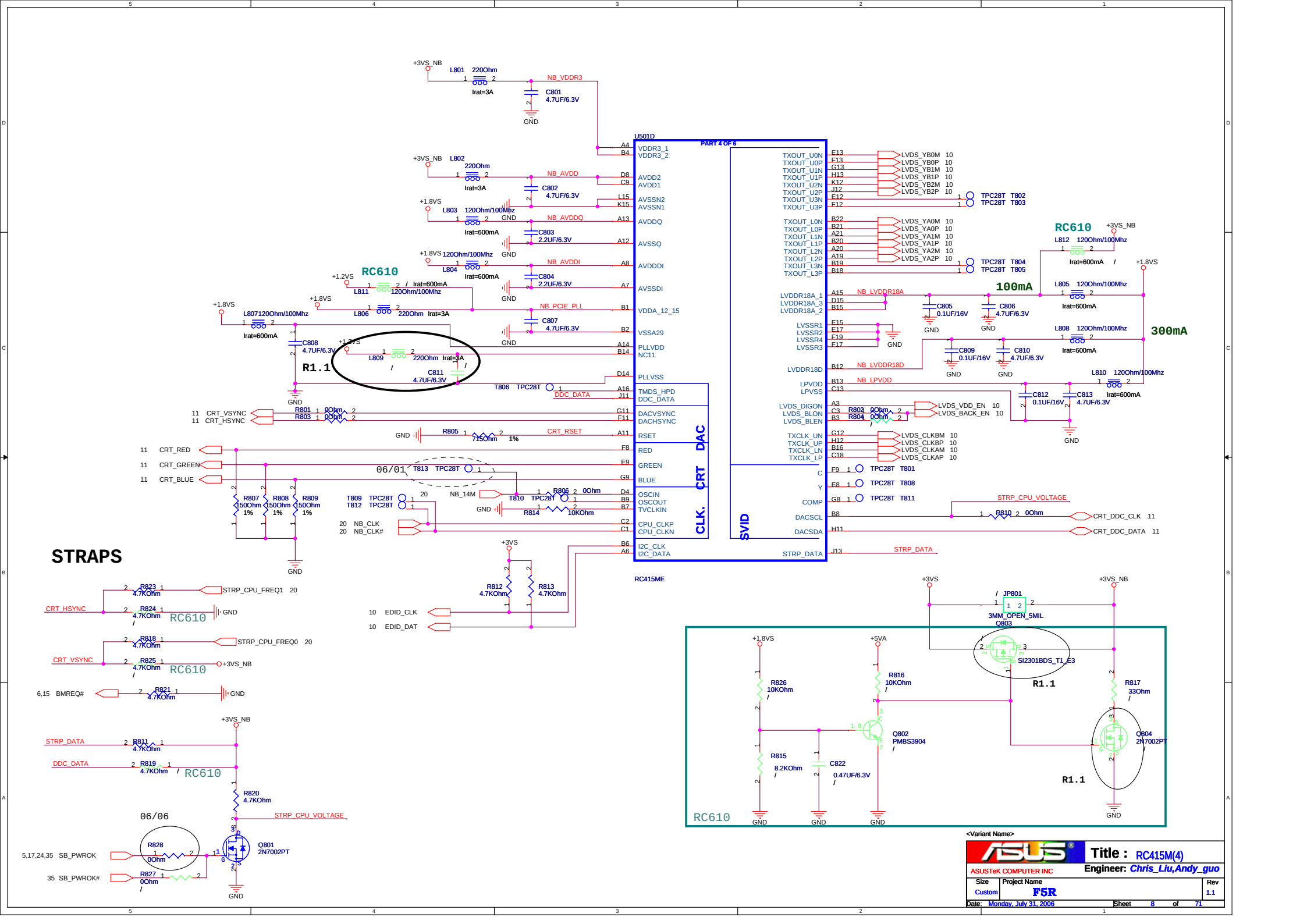
Title : RC415M(3)

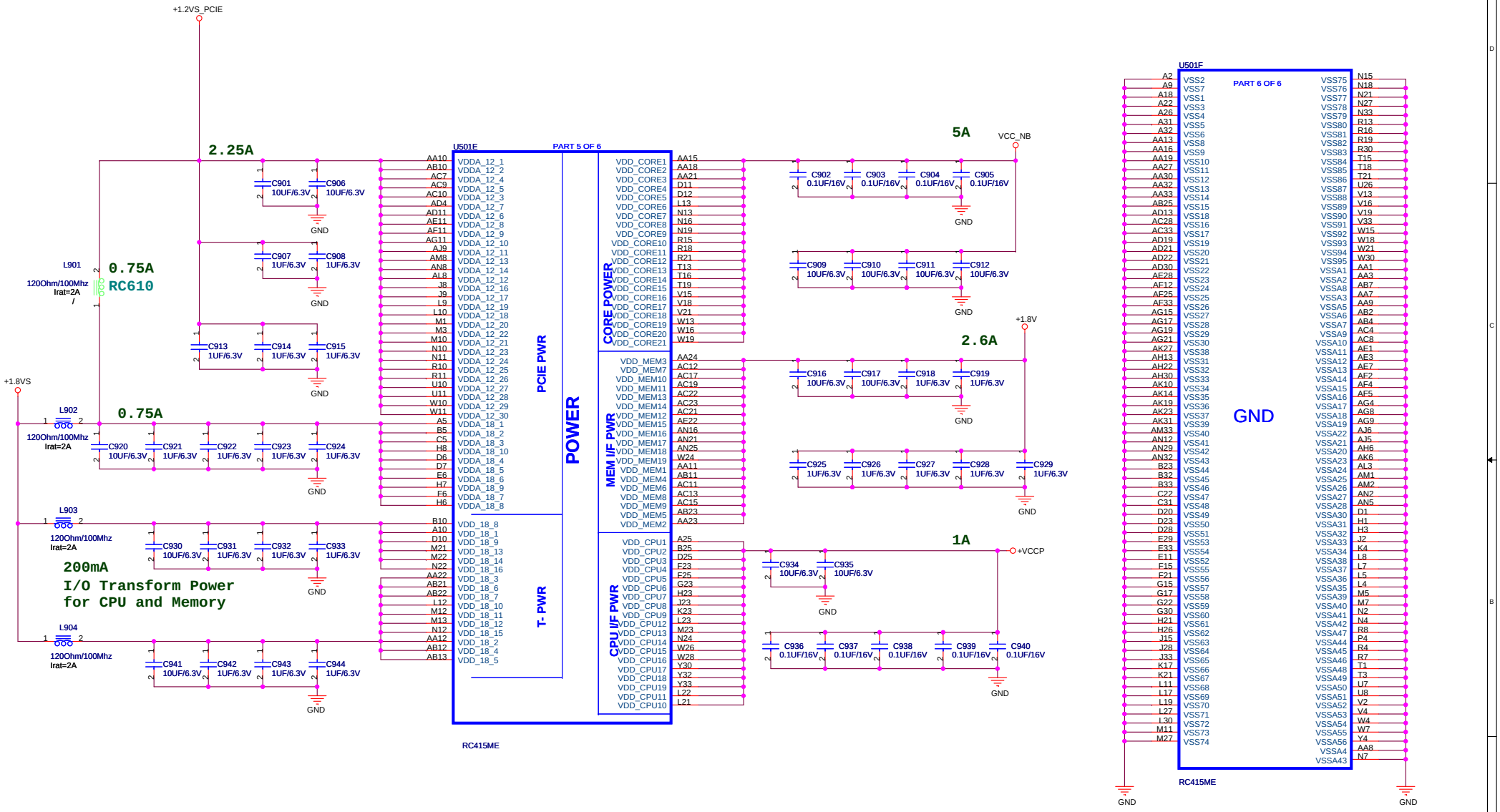
ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 7 of 71


STRAPS
U501D
PART 4 OF 6
RC415ME
RC610
100mA
300mA
R1.1
SVID
DAC
CRT
CLK.
+3VS_NB
+1.8VS
+1.2VS
+3VS
+5VA
GND
L801 220Ohm Irat=3A
L802 220Ohm Irat=3A
L803 120Ohm/100Mhz Irat=600mA
L804 120Ohm/100Mhz Irat=600mA
L806 220Ohm Irat=3A
L807 120Ohm/100Mhz Irat=600mA
L808 120Ohm/100Mhz Irat=600mA
L809 220Ohm Irat=3A
L810 120Ohm/100Mhz Irat=600mA
L811 120Ohm/100Mhz Irat=600mA
L812 120Ohm/100Mhz Irat=600mA
C801 4.7UF/6.3V
C802 4.7UF/6.3V
C803 2.2UF/6.3V
C804 2.2UF/6.3V
C805 0.1UF/16V
C806 4.7UF/6.3V
C807 4.7UF/6.3V
C808 4.7UF/6.3V
C809 0.1UF/16V
C810 4.7UF/6.3V
C811 4.7UF/6.3V
C812 0.1UF/16V
C813 4.7UF/6.3V
NB_VDDR3
NB_AVDD
NB_AVDDQ
NB_AVDDI
NB_PCIE_PLL
NB_LVDDR18A
NB_LVDDR18D
NB_LPVDD
DDC_DATA
CRT_RSET
CRT_VSYNC
CRT_HSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
NB_14M
NB_CLK
NB_CLK#
EDID_CLK
EDID_DAT
STRP_CPU_VOLTAGE
STRP_DATA
STRP_CPU_FREQ1
STRP_CPU_FREQ0
BMREQ#
SB_PWROK
SB_PWROK#
LVDS_VDD_EN
LVDS_BACK_EN
R801 0Ohm
R803 0Ohm
R805 715Ohm 1%
R806 0Ohm
R807 150Ohm 1%
R808 150Ohm 1%
R809 150Ohm 1%
R810 0Ohm
R812 4.7KOhm
R813 4.7KOhm
R814 10KOhm
R816 10KOhm
R817 33Ohm
R820 4.7KOhm
R821 4.7KOhm
R823 4.7KOhm
R824 4.7KOhm
R825 4.7KOhm
R826 10KOhm
R828 0Ohm
R827 0Ohm
R811 4.7KOhm
R818 4.7KOhm
R819 4.7KOhm
R815 8.2KOhm
C822 0.47UF/6.3V
Q801 2N7002PT
Q802 PMBS3904
Q803 SI2301BDS_T1_E3
Q804 2N7002PT
JP801 3MM_OPEN_5MIL
TPC28T T801
TPC28T T802
TPC28T T803
TPC28T T804
TPC28T T805
TPC28T T806
TPC28T T808
TPC28T T809
TPC28T T810
TPC28T T811
TPC28T T812
TPC28T T813
06/01
06/06
LVDS_YB0M 10
LVDS_YB0P 10
LVDS_YB1M 10
LVDS_YB1P 10
LVDS_YB2M 10
LVDS_YB2P 10
LVDS_YA0M 10
LVDS_YA0P 10
LVDS_YA1M 10
LVDS_YA1P 10
LVDS_YA2M 10
LVDS_YA2P 10
LVDS_CLKBM 10
LVDS_CLKBP 10
LVDS_CLKAM 10
LVDS_CLKAP 10
<Variant Name>
Title : RC415M(4)
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_guo
Size Custom
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 8 of 71



<Variant Name>

ASUSTeK COMPUTER INC

Title : RC415M(5)

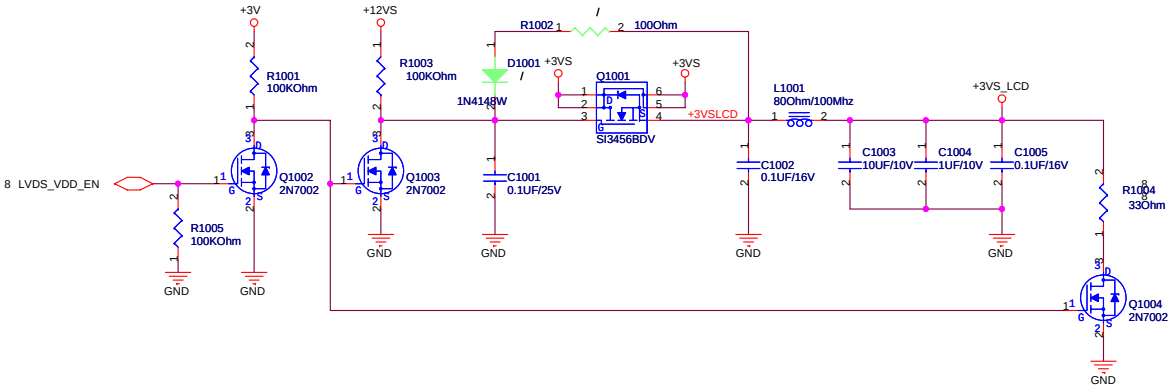
Engineer: Chris_liu,Andy_guo

Size	Project Name	Rev
Custom	F5X	1.1

Date: Monday, July 31, 2006 Sheet 9 of 71

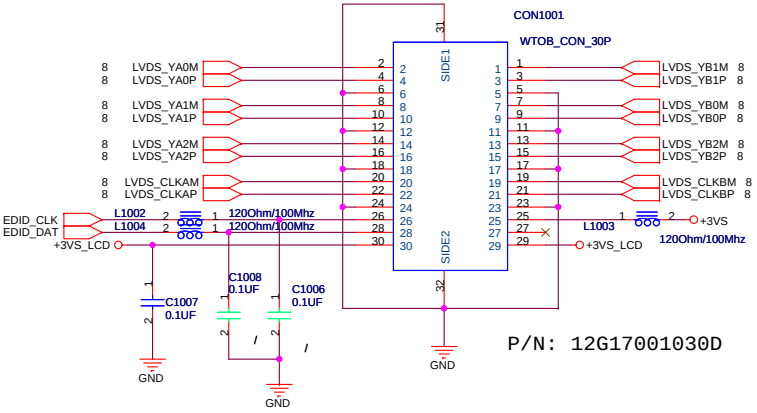
LCD Backlight Control

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

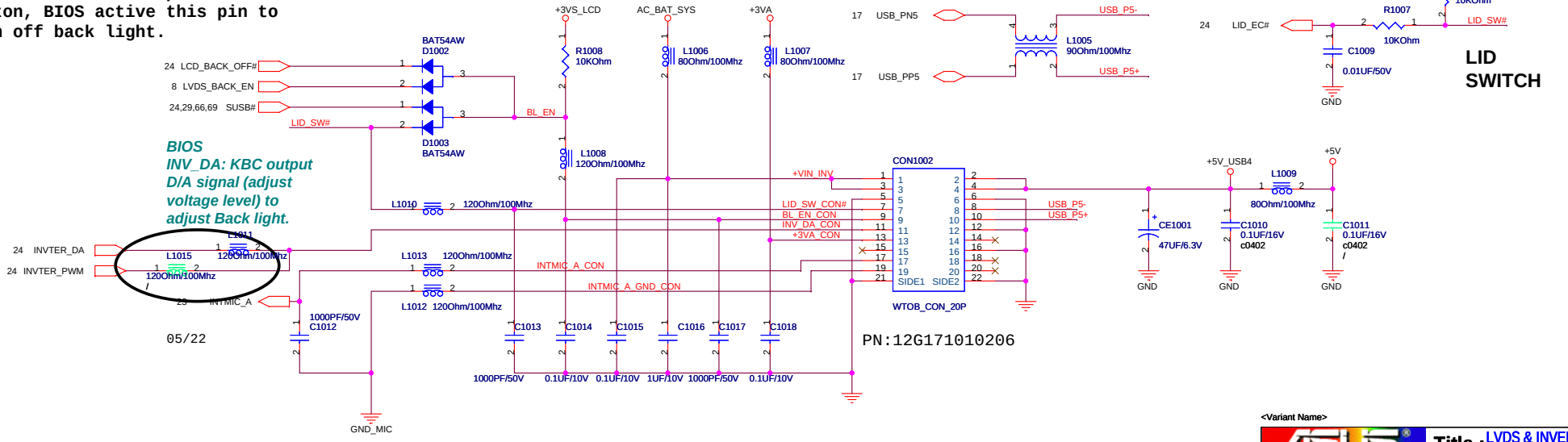
LCD LVDS Interface



P/N: 12G17001030D

INVERTER Interface

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



05/22

PN:12G171010206

<Variant Name>

ASUSTeK COMPUTER INC

Title : LVDS & INVERTER

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 10 of 71

PLACE ESD Diodes near
VGA port

R1.1

D1105 BAV99 — +5VS — HSYNC
D1106 BAV99 — +5VS — VSYNC
D1101 BAV99 — +3VS — CRT_RED
D1102 BAV99 — +3VS — CRT_GREEN
D1104 BAV99 — +3VS — CRT_BLUE

8 CRT_RED → L1101 60Ohm/100Mhz → CRT_R_CON
R1101 150Ohm r0402, C1101 15PF/50V c0402, C1102 22PF/25V c0402

8 CRT_GREEN → L1102 60Ohm/100Mhz → CRT_G_CON
R1106 150Ohm r0402, C1103 15PF/50V c0402, C1104 22PF/25V c0402

8 CRT_BLUE → L1103 60Ohm/100Mhz → CRT_B_CON
R1107 150Ohm r0402, C1105 15PF/50V c0402, C1106 22PF/25V c0402

8 CRT_HSYNC → U1101 74LVC1G17GW → HSYNC → L1104 120Ohm/100Mhz → HSYNC_CON
R1114 0Ohm, C1107 47PF/50V c0402

8 CRT_VSYNC → U1102 74LVC1G17GW → VSYNC → L1105 120Ohm/100Mhz → VSYNC_CON
R1115 0Ohm, C1109 47PF/50V c0402

8 CRT_DDC_DATA → DDC_DAT → Q1101 2N7002 → DDC_DAT_5V → R1110 0Ohm → DDC_DAT_CON
C1110 47PF/50V c0402
+5VS_CRT_DDC: R1102 6.8KOhm, R1103 4.7KOhm
D1109 SS0540

8 CRT_DDC_CLK → DDC_CLK → Q1104 2N7002 → DDC_CLK_5V → R1111 0Ohm → DDC_CLK_CON
C1111 47PF/50V c0402
R1104 4.7KOhm, R1105 6.8KOhm

CON1101 D_SUB_15P3R
CRT_R_CON, CRT_G_CON, CRT_B_CON
DDC_DAT_CON, HSYNC_CON, VSYNC_CON, DDC_CLK_CON

PN: 12G101102155

<Variant Name>

ASUSTeK COMPUTER INC

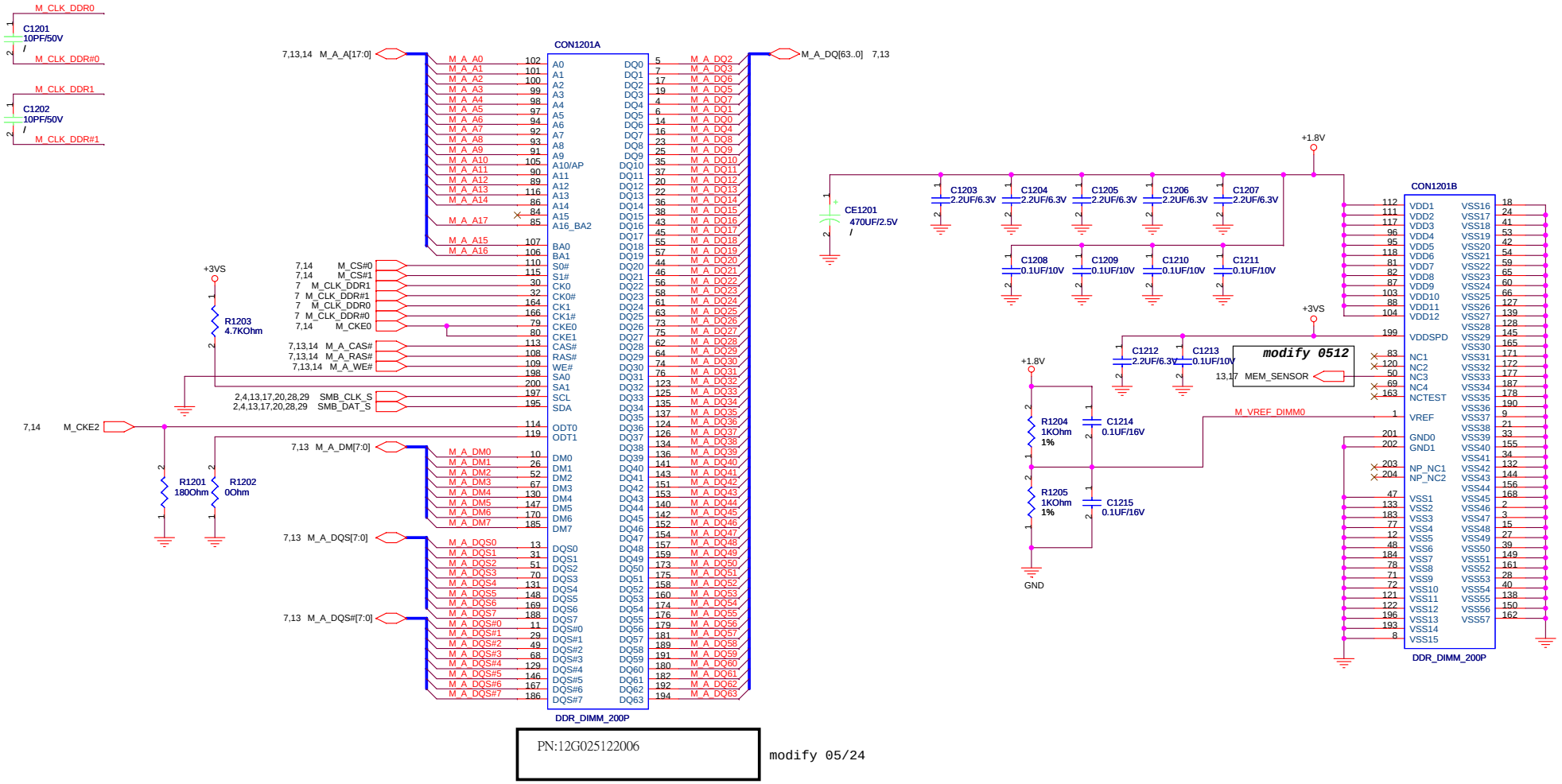
Title : CRT

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 11 of 71

TOP



PN:12G025122006

modify 05/24

<Variant Name>

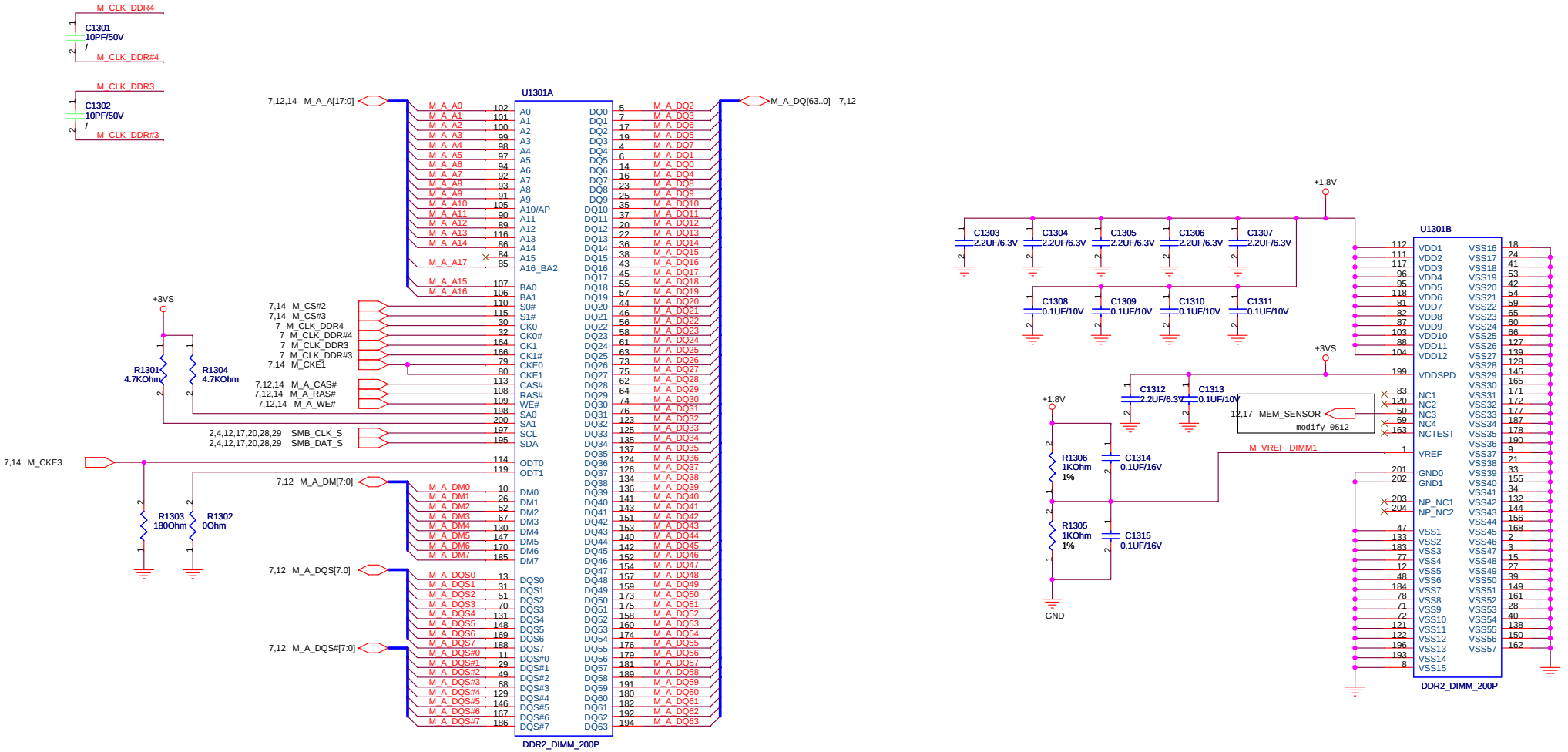
ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM1

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 12 of 71



PN:12G025C22002 REV.

<Variant Name>

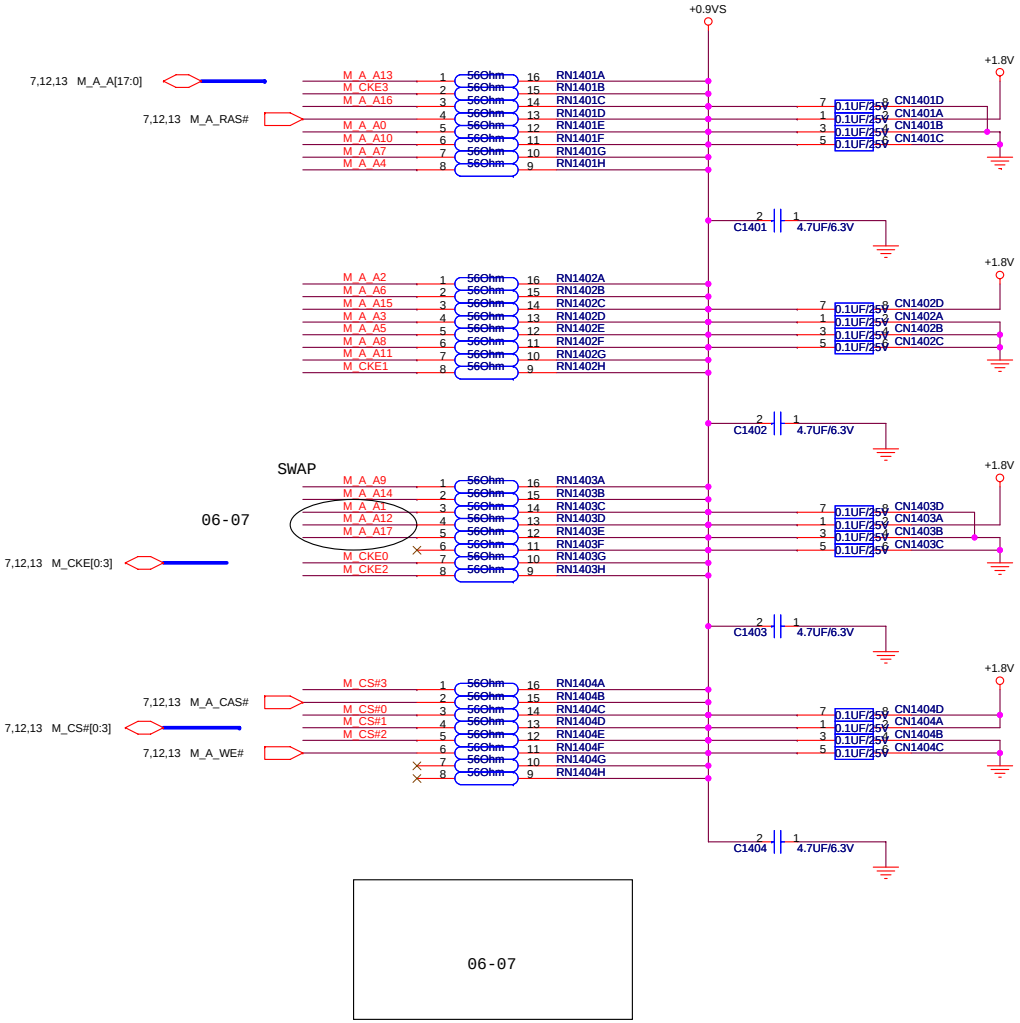
ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM1

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 13 of 71



<Variant Name>

Title : DDR2 TERMINATION

ASUSTeK COMPUTER INC

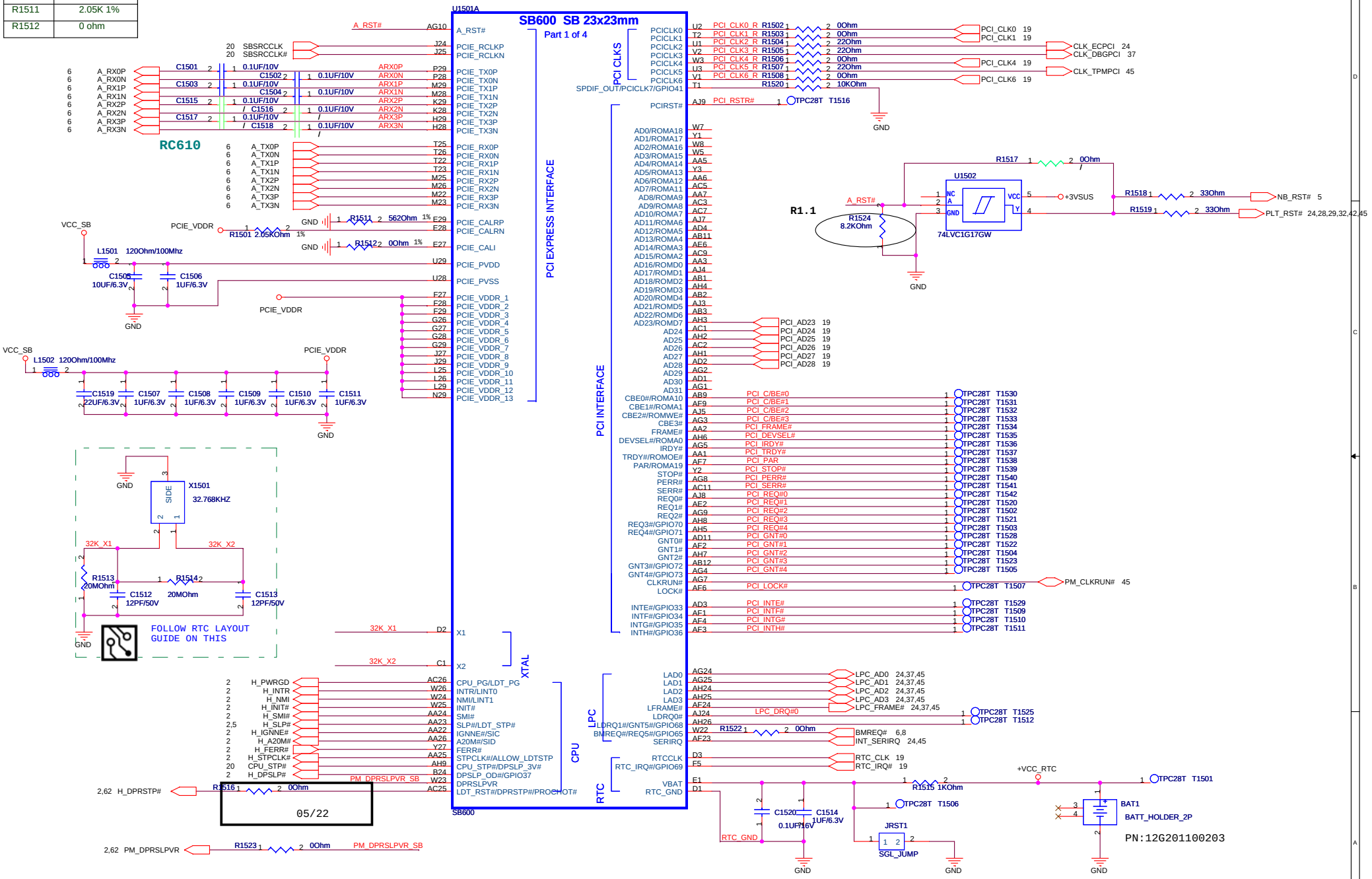
Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

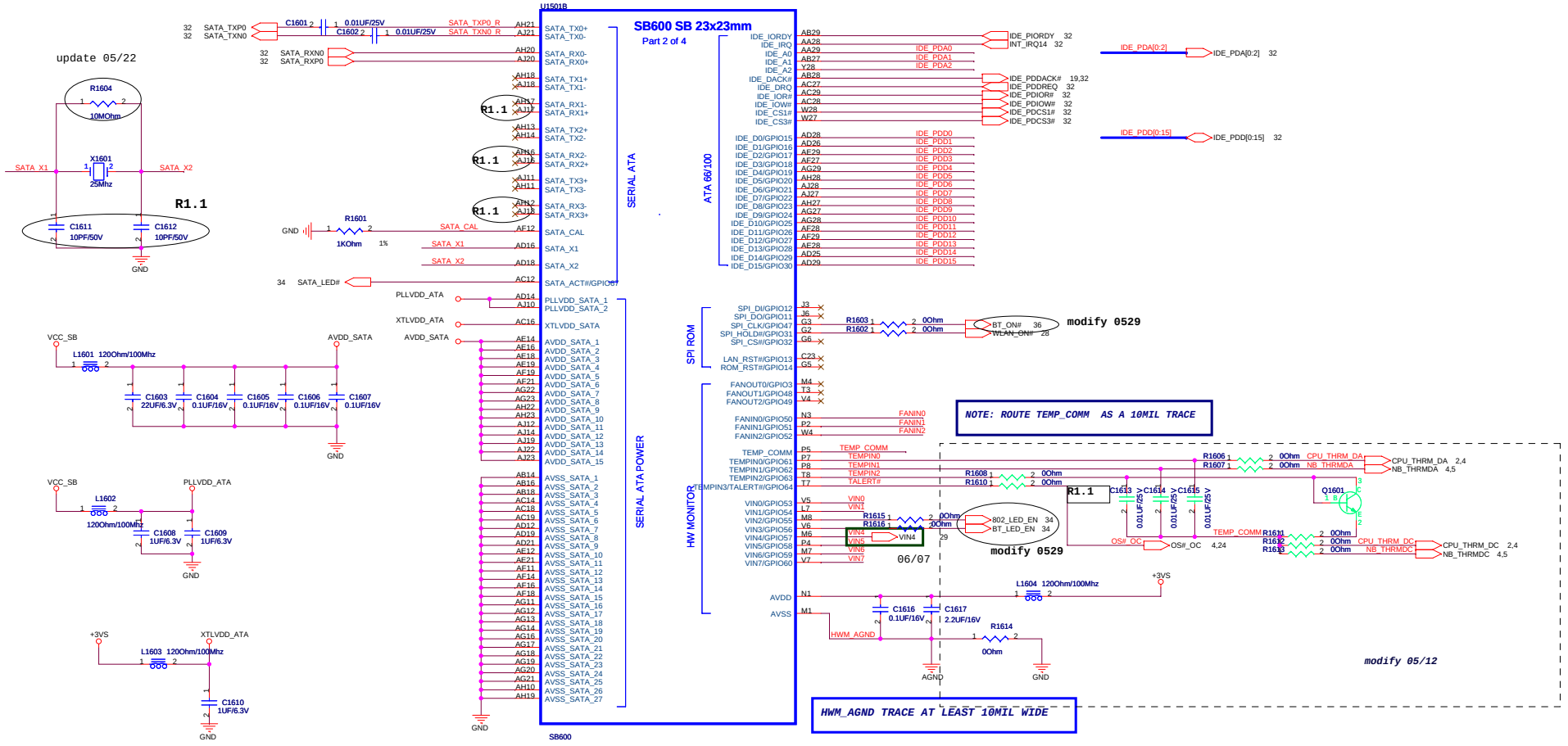
Date: Monday, July 31, 2006 Sheet 14 of 71

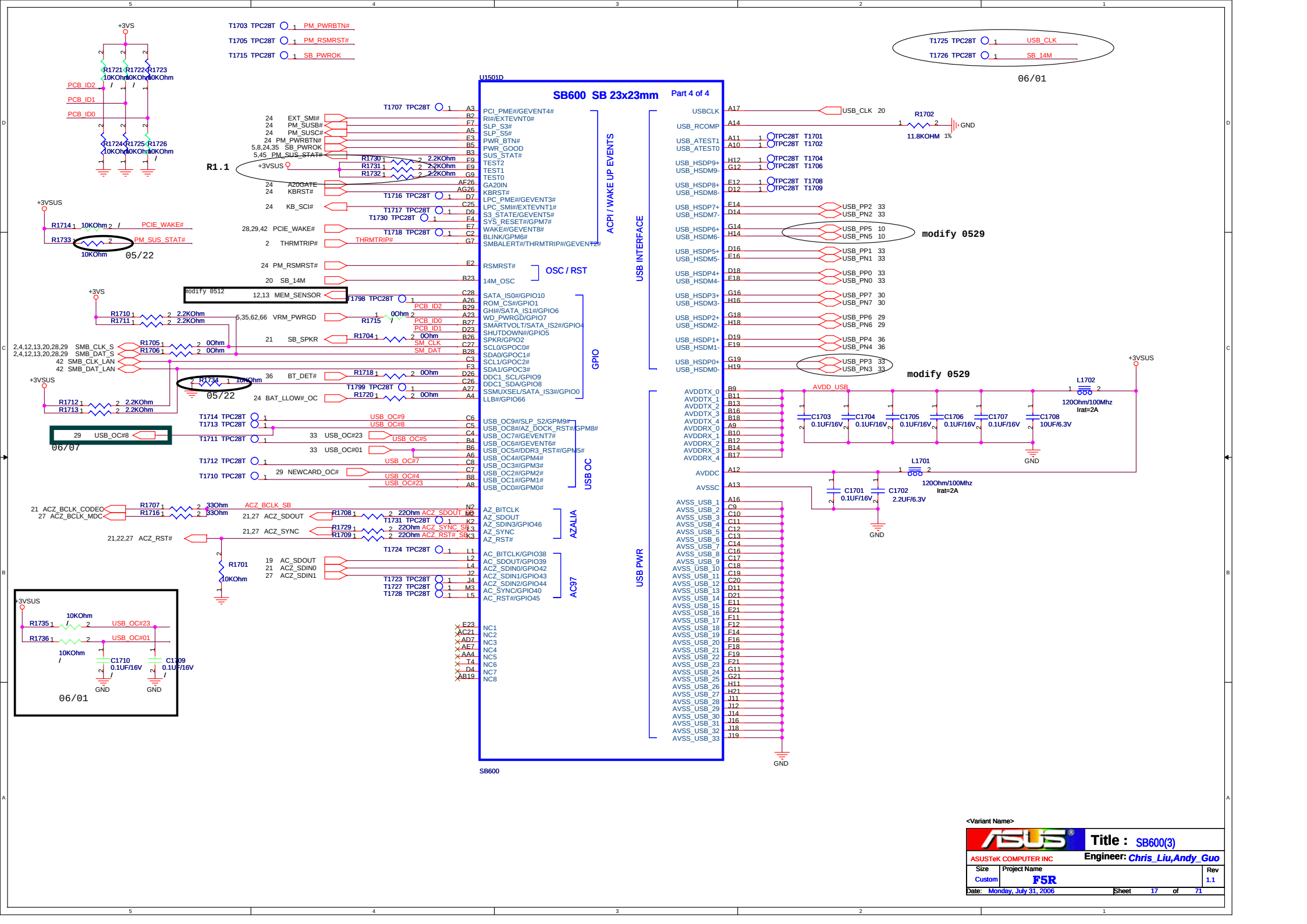
SB CALIBRATION RESISITOR VALUE

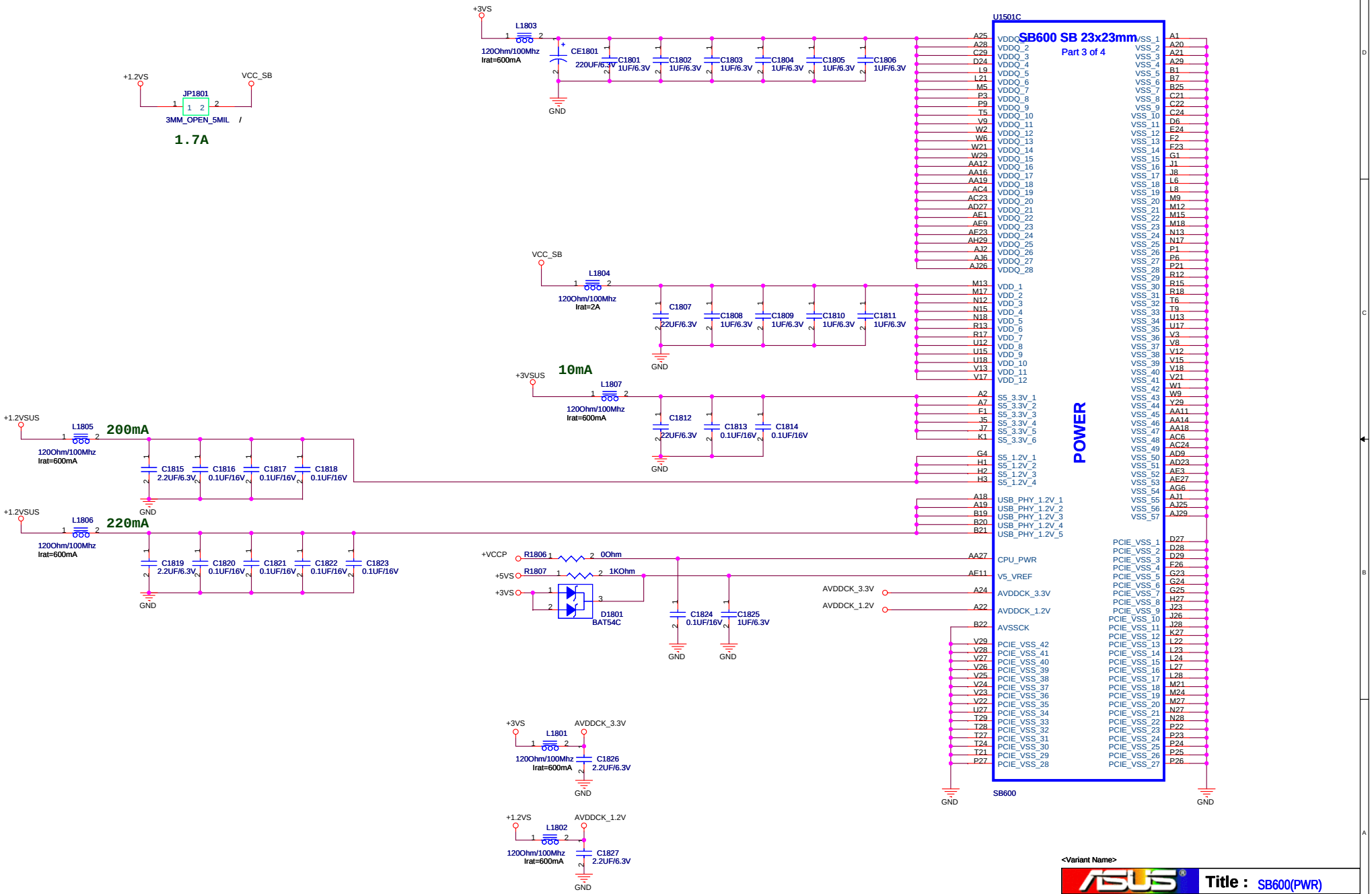
	SB600
R1501	562 OHM 1%
R1511	2.05K 1%
R1512	0 ohm



Title :	SB600(1)
ASUSTeK COMPUTER INC	Engineer: Chris_Liu,Andy_Guo
Size: Custom	Project Name: F5R
Rev: 1.1	
Date: Monday, July 31, 2006	Sheet 15 of 71


update 05/22
SB600 SB 23x23mm
Part 2 of 4
U1501B
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SB600
modify 0529
modify 05/12
NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE
HWM_AGND TRACE AT LEAST 10MIL WIDE
R1.1
06/07


SB600 SB 23x23mm
Part 4 of 4
U1501D
SB600
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
modify 0529
modify 0512
R1.1
05/22
06/07
06/01
Title : SB600(3)
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 17 of 71



<Variant Name>

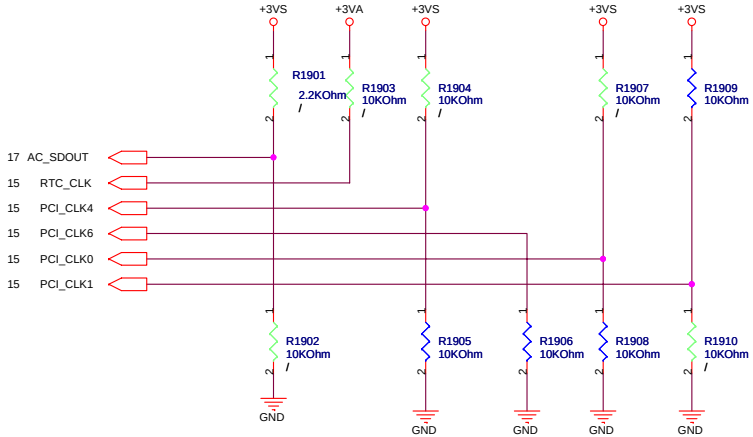
Title : SB600(PWR)

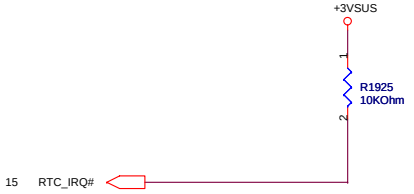
ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 18 of 71

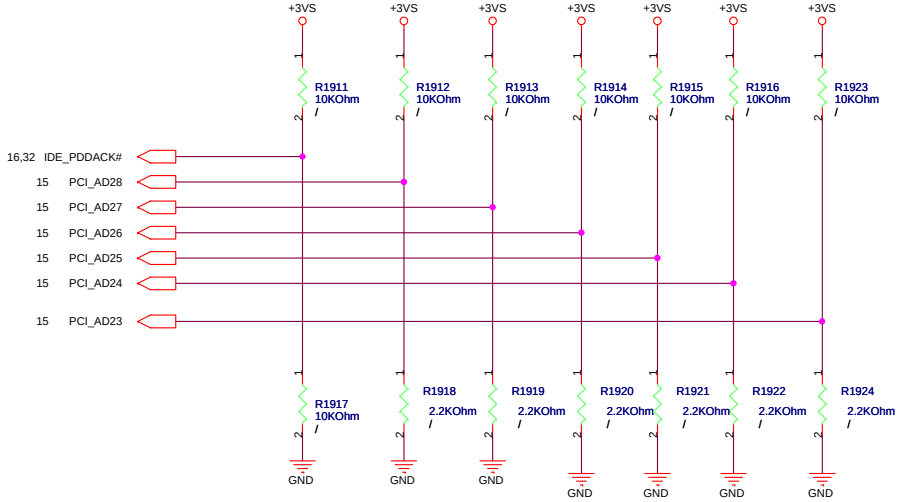




NOTE: R1925 PU RESISTOR FOR RTC_IRQ# IS REQUIRED FOR SB600 TOKEEP THE INPUT FROM FLOATING.

REQUIRED STRAPS

					SB600		SB460	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM		ROM TYPE: H, H = PCI ROM H, L = LPC I ROM DEFAULT L, H = LPC II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT				



DEBUG STRAPS

	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB460 ONLY SB600 ONLY

SB600 ONLY

NOTE: FOR SB460, PCI_AD23 IS RESERVED

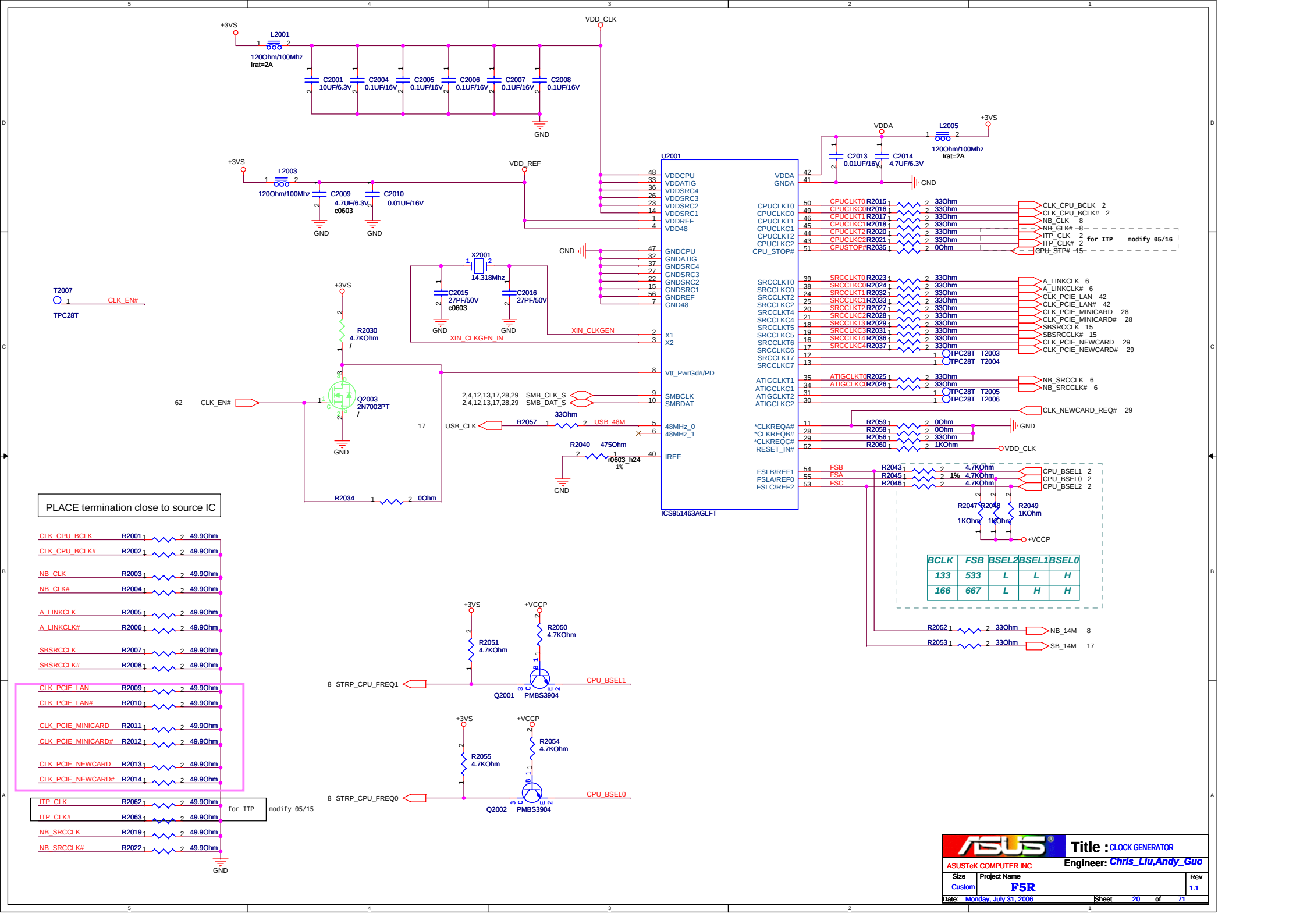
ASUSTeK COMPUTER INC

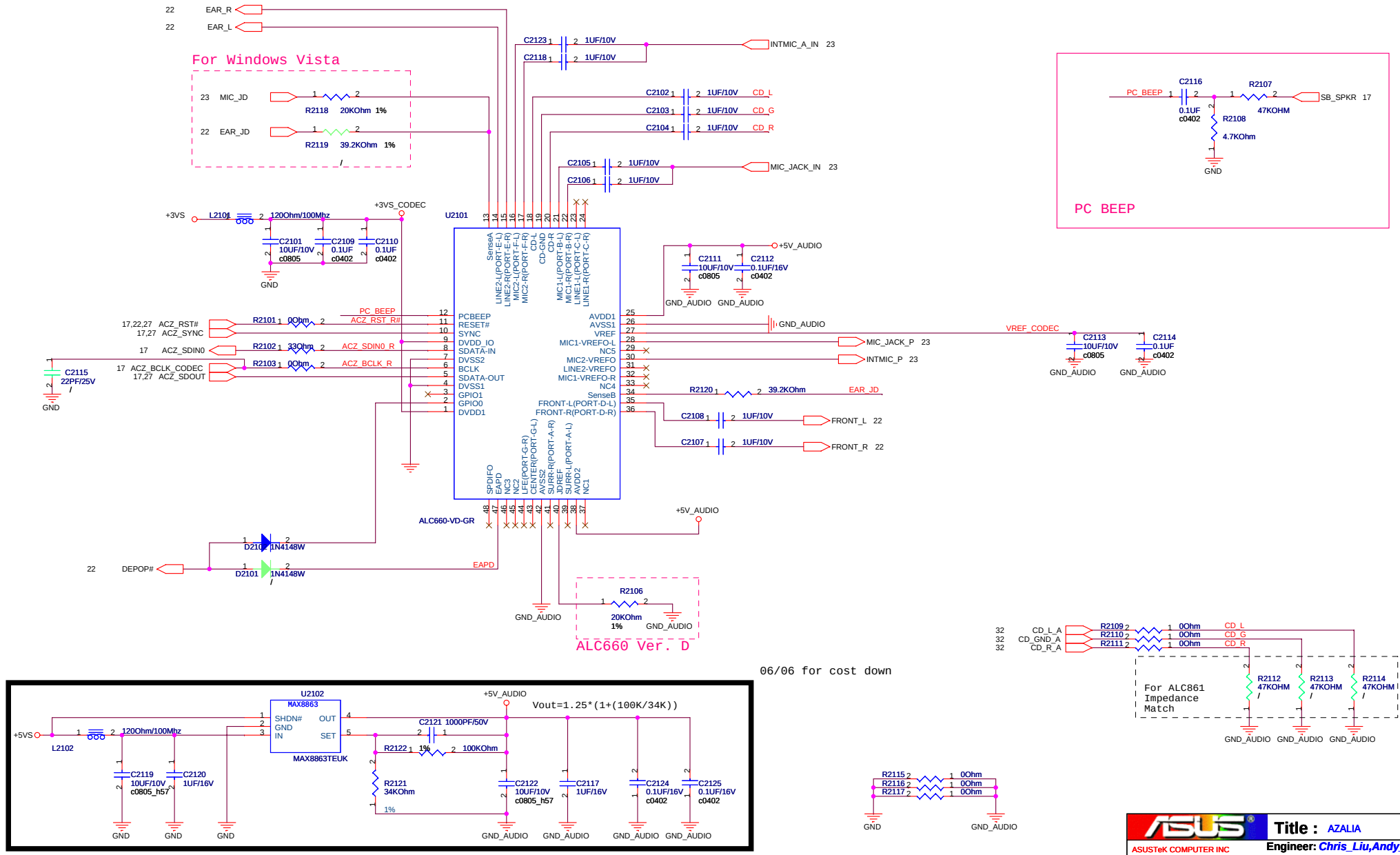
Title : SB600(5)

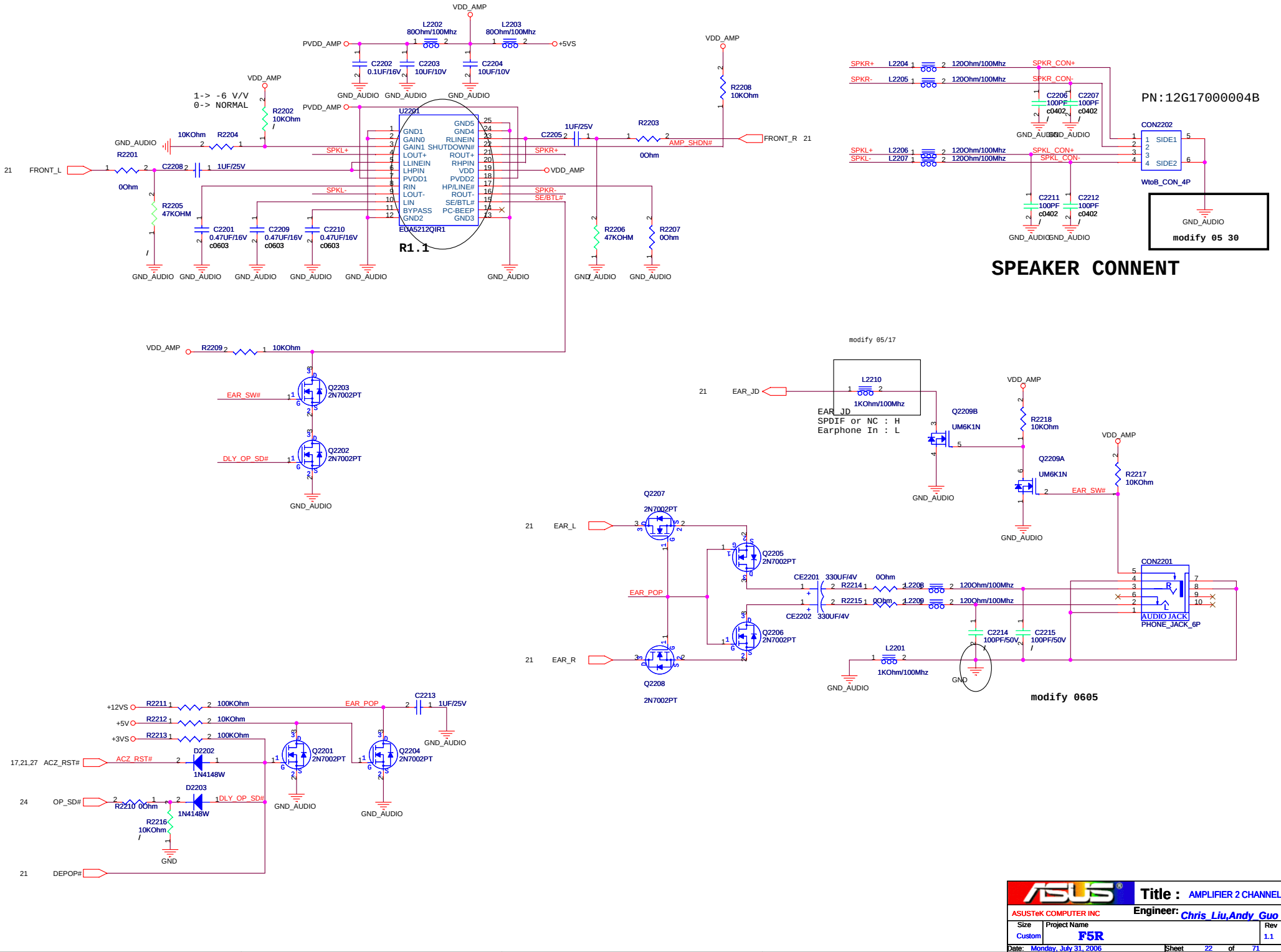
Engineer: <Enginner Name>

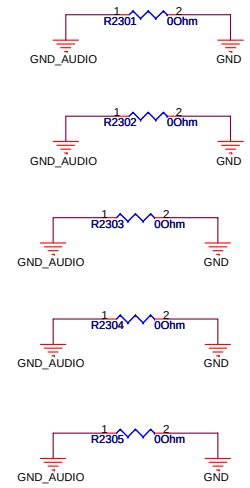
Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 19 of 71

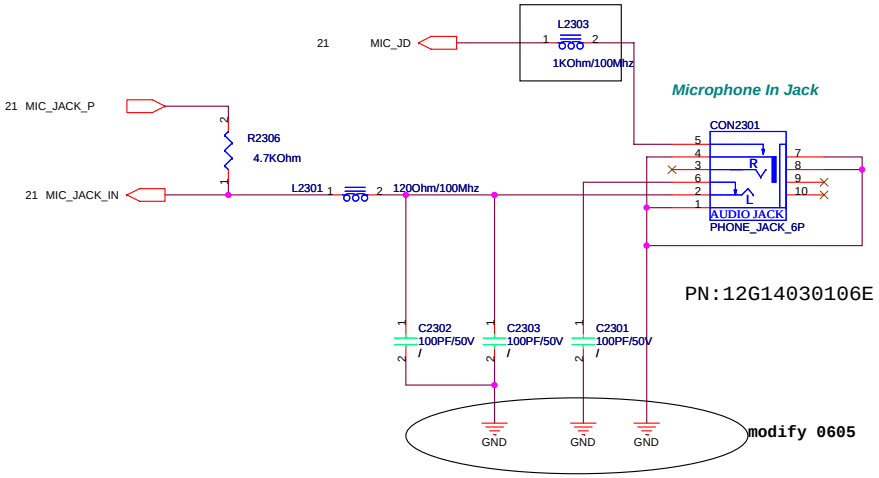

+3VS
L2001
120Ohm/100Mhz
Irat=2A
C2001 10UF/6.3V
C2004 0.1UF/16V
C2005 0.1UF/16V
C2006 0.1UF/16V
C2007 0.1UF/16V
C2008 0.1UF/16V
GND
VDD_CLK
+3VS
L2003
120Ohm/100Mhz
C2009 4.7UF/6.3V c0603
C2010 0.01UF/16V
GND
GND
VDD_REF
U2001
VDDCPU
VDDATIG
VDDSRC4
VDDSRC3
VDDSRC2
VDDSRC1
VDDREF
VDD48
GNDCPU
GNDATIG
GNDSRC4
GNDSRC3
GNDSRC2
GNDSRC1
GNDREF
GND48
X2001
14.318Mhz
C2015 27PF/50V c0603
C2016 27PF/50V
XIN_CLKGEN
XIN_CLKGEN_IN
X1
X2
Vtt_PwrGd#/PD
SMBCLK
SMBDAT
48MHz_0
48MHz_1
IREF
R2040 475Ohm r0603_h24 1%
R2034 0Ohm
R2030 4.7KOhm
Q2003 2N7002PT
CLK_EN#
T2007
TPC28T
SMB_CLK_S
SMB_DAT_S
USB_CLK
R2057 33Ohm
USB_48M
ICS951463AGLFT
VDDA
L2005
120Ohm/100Mhz
Irat=2A
C2013 0.01UF/16V
C2014 4.7UF/6.3V
CPUCLKT0
CPUCLKC0
CPUCLKT1
CPUCLKC1
CPUCLKT2
CPUCLKC2
CPU_STOP#
SRCCLKT0
SRCCLKC0
SRCCLKT2
SRCCLKC1
SRCCLKT2
SRCCLKC2
SRCCLKT3
SRCCLKC3
SRCCLKT4
SRCCLKC4
ATIGCLKT0
ATIGCLKC0
*CLKREQA#
*CLKREQB#
*CLKREQC#
RESET_IN#
FSB
FSA
FSC
FSLB/REF1
FSLA/REF0
FSLC/REF2
R2043 4.7KOhm
R2045 4.7KOhm
R2046 4.7KOhm
1% 4.7KOhm
R2047 1KOhm
R2048 1KOhm
R2049 1KOhm
+VCCP
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
CLK_CPU_BCLK
CLK_CPU_BCLK#
NB_CLK
NB_CLK#
A_LINKCLK
A_LINKCLK#
SBSRCCLK
SBSRCCLK#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_MINICARD
CLK_PCIE_MINICARD#
CLK_PCIE_NEWCARD
CLK_PCIE_NEWCARD#
CLK_NEWCARD_REQ#
NB_SRCCLK
NB_SRCCLK#
SB_14M
NB_14M
CPU_BSEL1
CPU_BSEL0
PLACE termination close to source IC
49.9Ohm
ITP_CLK
ITP_CLK#
for ITP
modify 05/15
STRP_CPU_FREQ1
STRP_CPU_FREQ0
Q2001 PMBS3904
Q2002 PMBS3904
R2050 4.7KOhm
R2051 4.7KOhm
R2054 4.7KOhm
R2055 4.7KOhm
ASUSTeK COMPUTER INC
Title : CLOCK GENERATOR
Engineer: Chris_Liu,Andy_Guo
Size Custom
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 20 of 71


For Windows Vista
PC BEEP
ALC660 Ver. D
06/06 for cost down
For ALC861 Impedance Match
ALC660-VD-GR
MAX8863
MAX8863TEUK
Vout=1.25*(1+(100K/34K))
Title : AZALIA
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Size: Custom
Project Name: F5R
Rev: 1.1
Date: Monday, July 31, 2006
Sheet 21 of 71


VDD_AMP
L2202 80Ohm/100Mhz
L2203 80Ohm/100Mhz
PVDD_AMP
+5VS
C2202 0.1UF/16V
C2203 10UF/10V
C2204 10UF/10V
GND_AUDIO
1-> -6 V/V
0-> NORMAL
R2202 10KOhm
R2208 10KOhm
U2201
EUA5212QIR1
R1.1
GND1
GAIN0
GAIN1
LOUT+
LLINEIN
LHPIN
PVDD1
RIN
LOUT-
LIN
BYPASS
GND2
GND5
GND4
RLINEIN
SHUTDOWN#
ROUT+
RHPIN
VDD
PVDD2
HP/LINE#
ROUT-
SE/BTL#
PC-BEEP
GND3
10KOhm R2204
R2201 0Ohm
21 FRONT_L
C2208 1UF/25V
R2205 47KOHM
C2201 0.47UF/16V c0603
C2209 0.47UF/16V c0603
C2210 0.47UF/16V c0603
SPKL+
SPKL-
SPKR+
SPKR-
SE/BTL#
C2205 1UF/25V
R2203 0Ohm
AMP_SHDN#
FRONT_R 21
R2206 47KOHM
R2207 0Ohm
SPKR+ L2204 120Ohm/100Mhz
SPKR- L2205 120Ohm/100Mhz
SPKR_CON+
SPKR_CON-
C2206 100PF c0402
C2207 100PF c0402
SPKL+ L2206 120Ohm/100Mhz
SPKL- L2207 120Ohm/100Mhz
SPKL_CON+
SPKL_CON-
C2211 100PF c0402
C2212 100PF c0402
CON2202
SIDE1
SIDE2
WtoB_CON_4P
PN:12G17000004B
modify 05 30
SPEAKER CONNENT
R2209 10KOhm
EAR_SW#
DLY_OP_SD#
Q2203 2N7002PT
Q2202 2N7002PT
modify 05/17
21 EAR_JD
L2210 1KOhm/100Mhz
EAR_JD
SPDIF or NC : H
Earphone In : L
Q2209B UM6K1N
Q2209A UM6K1N
R2218 10KOhm
R2217 10KOhm
Q2207 2N7002PT
Q2208 2N7002PT
Q2205 2N7002PT
Q2206 2N7002PT
21 EAR_L
21 EAR_R
EAR_POP
CE2201 330UF/4V
CE2202 330UF/4V
R2214 0Ohm
R2215 0Ohm
L2208 120Ohm/100Mhz
L2209 120Ohm/100Mhz
L2201 1KOhm/100Mhz
C2214 100PF/50V
C2215 100PF/50V
CON2201
AUDIO JACK
PHONE_JACK_6P
modify 0605
+12VS
+5VS
+3VS
R2211 100KOhm
R2212 10KOhm
R2213 100KOhm
C2213 1UF/25V
17,21,27 ACZ_RST#
D2202 1N4148W
Q2201 2N7002PT
Q2204 2N7002PT
24 OP_SD#
D2203 1N4148W
R2210 0Ohm
R2216 10KOhm
21 DEPOP#
GND
ASUSTeK COMPUTER INC
Engineer: Chris_Liu,Andy_Guo
Title : AMPLIFIER 2 CHANNEL
Size Custom
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 22 of 71



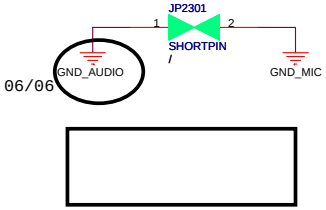
modify 05/17



PN:12G14030106E

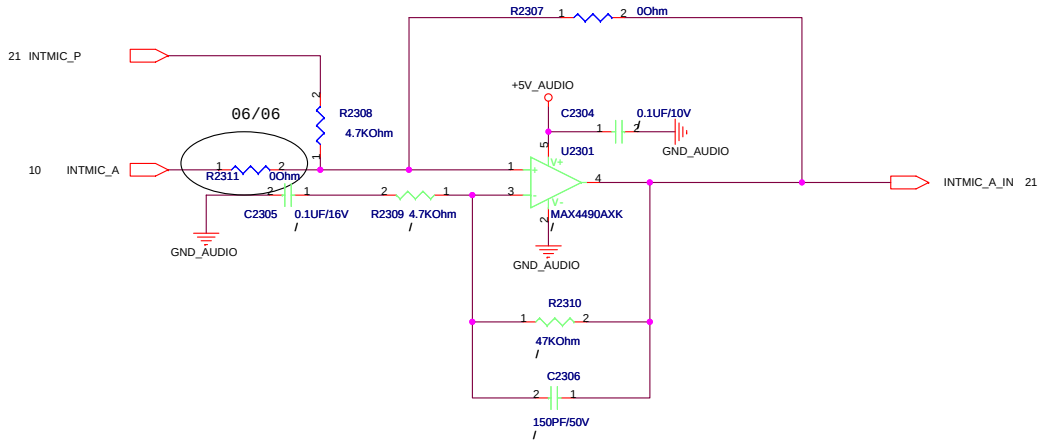
modify 0605

INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



modify 0605

Pre-AMP For Test Function



ASUSTeK COMPUTER INC	Title : MIC JACK	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 23 of 71	

For Keyboard

Close to Switch

to Battery

to Thermal

U2401

IT8510TE

R1.1

CON2401

FPC_CON_28P

PN:12G182402806

KID0 : 0 1 1

KID1 : 0 1 0

Mode : US UK JP

Layout Note: close to CON6600

Layout Note: close to CON1002

modify 0529

modify 0515

06/06

Cload=12.5PF

close to EC

start up time : 750ms

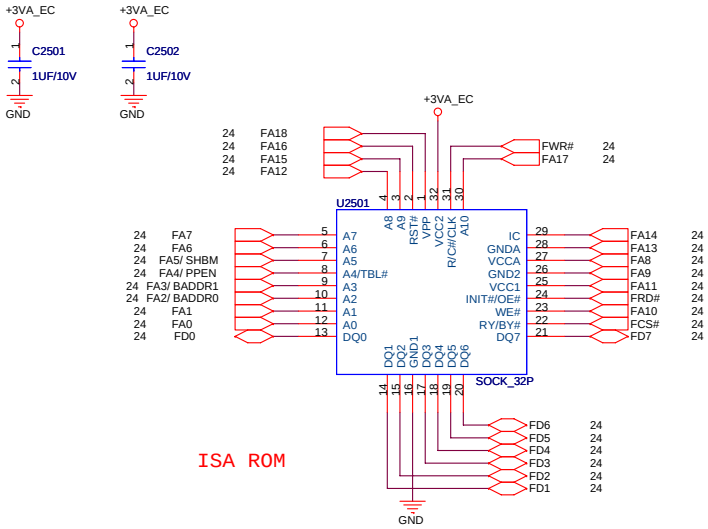
for ITP modify 05/15

Title :	EC ITE8510
ASUSTeK COMPUTER INC	Engineer: Chris_Liu,Andy_Guo
Size: Custom	Project Name: F5R
Rev: 1.1	
Date: Wednesday, August 02, 2006	Sheet 24 of 71

EC Hardware Strapping

PLCC32 Socket **PN:12G04300032F**

SST-PLCC32 4Mbits Flash ROM **PN:05G001027221**



ISA ROM

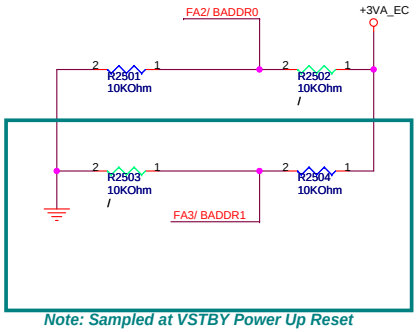
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

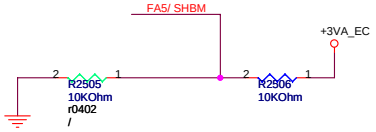


Note: Sampled at VSTBY Power Up Reset

FA5/ SHBM

0: Disable Shared Memory with Host BIOS

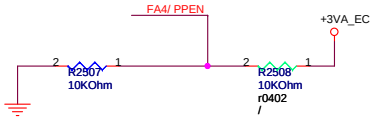
1: Enable Shared Memory with Host BIOS



FA4/ PPEN

0: Normal

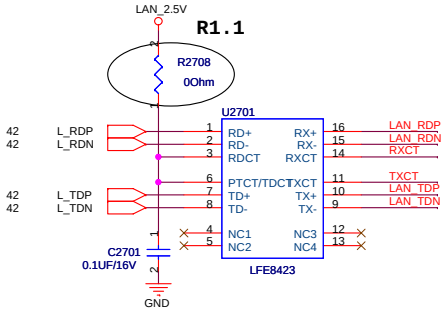
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

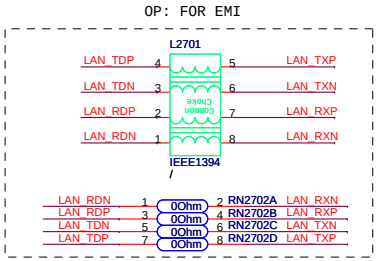


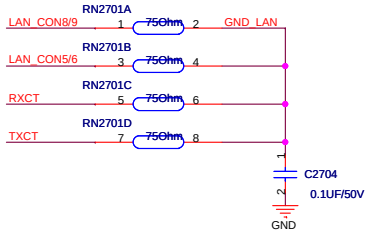
ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: Chris_Liu,Andy_Guo	
Size: Custom	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 25 of 71	

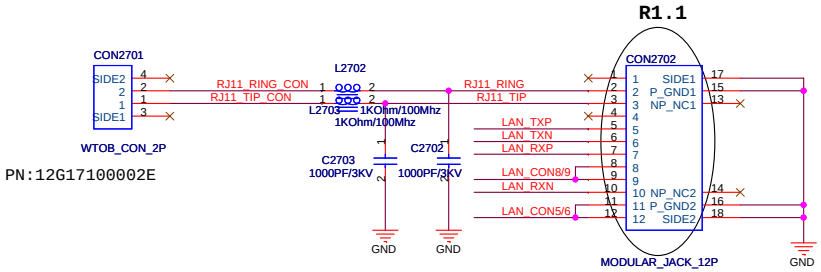
Title :	*
ASUSTeK COMPUTER INC	Engineer: Chris_Liu,Andy_Guo
Size: Custom	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 26 of 71

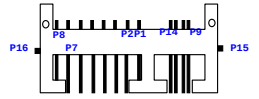
LAN PORT





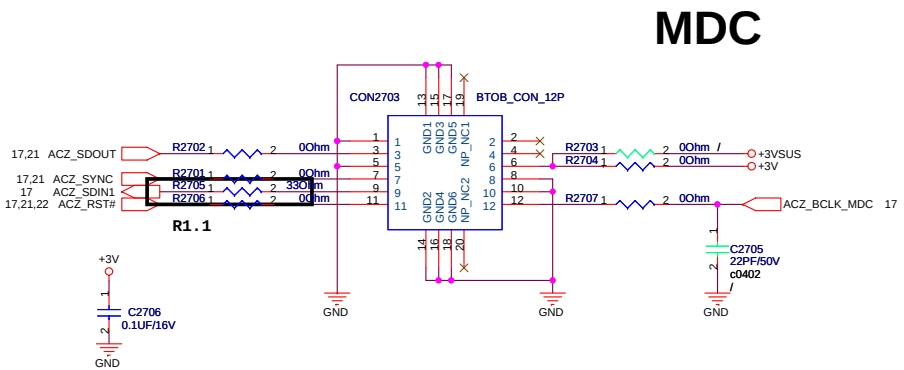




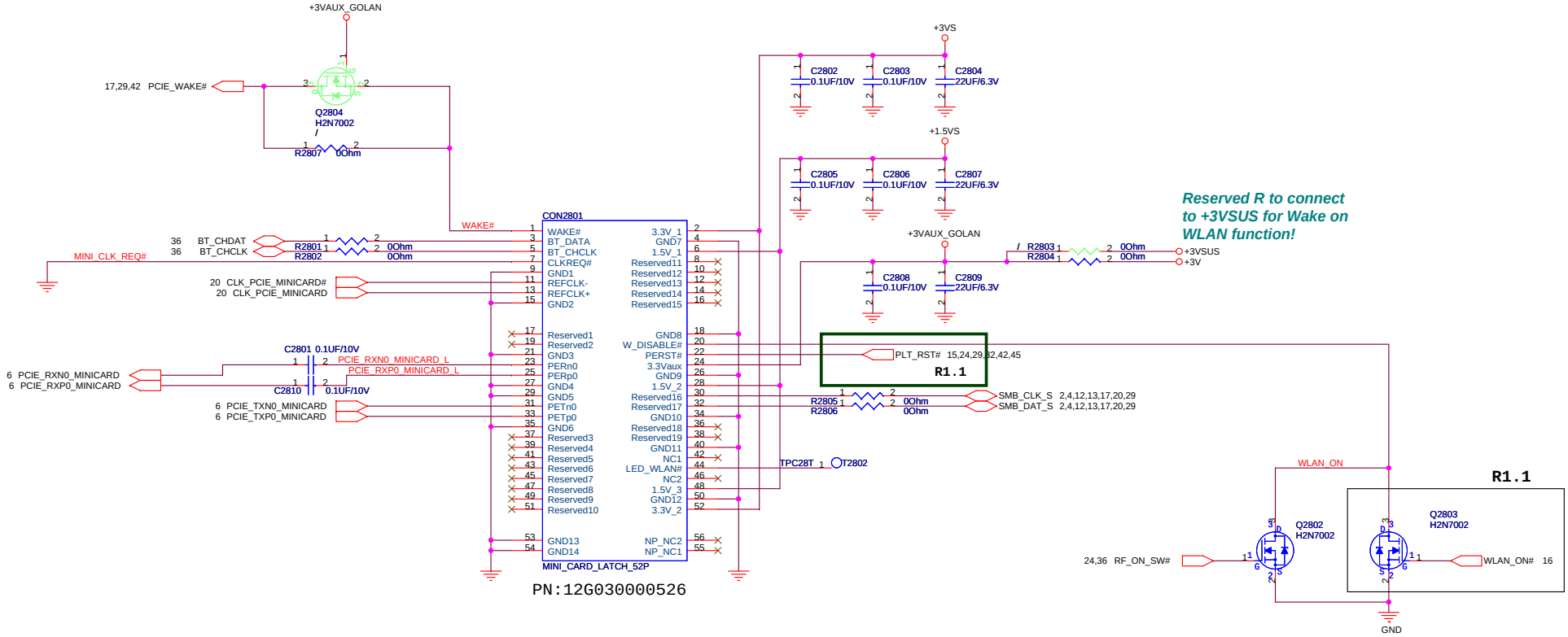


RJ 45 & RJ 11
BOTTOM VIEW

MDC



ASUSTeK COMPUTER INC	Title : RJ11+45 & MDC		
	Engineer: Chris_Liu,Andy_Guo		
Size: Custom	Project Name: F5R		Rev: 1.1
Date: Monday, July 31, 2006	Sheet 27 of 71		



PN:12G030000526

<Variant Name>

Title : MINICARD

ASUSTeK COMPUTER INC

Engineer: Chris Liu,Andy Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 28 of 71

FOR SWAP

modify 0607

17 USB_PP6 — L2901 90Ohm/100Mhz — USB_P6+

17 USB_PN6 — USB_P6-

D2902 RSB6.8S / D2903 RSB6.8S /

06/07

SB600 GPO57

SB600 GPM8

16 VIN4 — R2902 0Ohm

10,24,66,69 SUSB#

17 USB_OC#8 — D2904 1N4148W D2905 1N4148W — CPUSB#

24,63,64,69 VSUS_ON — D2901 1N4148W — 0Ohm R2905 — NEWCARDS_RST

06/06

U2901 R5538D001

STBY# SHDN# PERST# 3.3VIN_1 3.3VIN_2 1.5VIN_1 1.5VIN_2 AUXIN SYSRST# GND1 GND2

OC# 1.5VOUT_1 1.5VOUT_2 AUXOUT 3.3VOUT_1 3.3VOUT_2 CPPE# CPUSB# RCLKEN NC

NEWCARD_OC# 17 — +1.5VS_PE — +3VSUS_PE — +3VS_PE — CPUSB# — REFCLK_EN

+3VSUS — +1.5VS — +3VS

15,24,28,32,42,45 PLT_RST# — R1.1

!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

CON2901 EXPRESS_CARD_26P

GND1 USB_D- USB_D+ CPUSB# RESERVED1 RESERVED2 SMBCLK SMBDATA +1.5V_1 +1.5V_2 WAKE# +3.3VAUX PERST# +3.3V_1 +3.3V_2 CLKREQ# CPPE# REFCLK- REFCLK+ GND2 PERn0 PERp0 GND3 PETn0 PETp0 GND4 GND5 NP_NC1 NP_NC2 GND6

USB_P6- USB_P6+ CPUSB#

2,4,12,13,17,20,28 SMB_CLK_S

2,4,12,13,17,20,28 SMB_DAT_S

+1.5VS_PE — PCIE_WAKE# C — +3VSUS_PE — PERST# — +3VS_PE

NEWCARS_RST — R2901 0Ohm

20 CLK_PCIE_NEWCARD#

20 CLK_PCIE_NEWCARD

6 PCIE_RXN1_NEWCARD — C2902 0.1UF/10V — PCIE_RXN1_NEWCARD_L

6 PCIE_RXP1_NEWCARD — C2903 0.1UF/10V — PCIE_RXP1_NEWCARD_L

6 PCIE_TXN1_NEWCARD

6 PCIE_TXP1_NEWCARD

06/07

PN:12G161300261

CLK_NEWCARD_REQ# 20 — Q2901 2N7002 — REFCLK_EN

+3VSUS_PE — R2904 10KOhm

17,28,42 PCIE_WAKE# — Q2902 H2N7002 — PCIE_WAKE# C

R2903 0Ohm

U2902 CARD_EJECTOR_2P

P_GND1 P_GND2

PN:12G21C102604

+3VSUS: C2901 2.2UF/6.3V — C2904 0.1UF/10V

+3VS: C2905 4.7UF/10V — C2906 0.1UF/10V

+1.5VS: C2907 2.2UF/6.3V — C2908 0.1UF/10V

+3VSUS_PE: C2909 10UF/10V — C2910 0.01UF/16V

+3VS_PE: C2911 10UF/10V — C2912 10UF/10V — C2913 0.01UF/16V

+1.5VS_PE: C2914 10UF/10V — C2915 0.01UF/16V

<Variant Name>

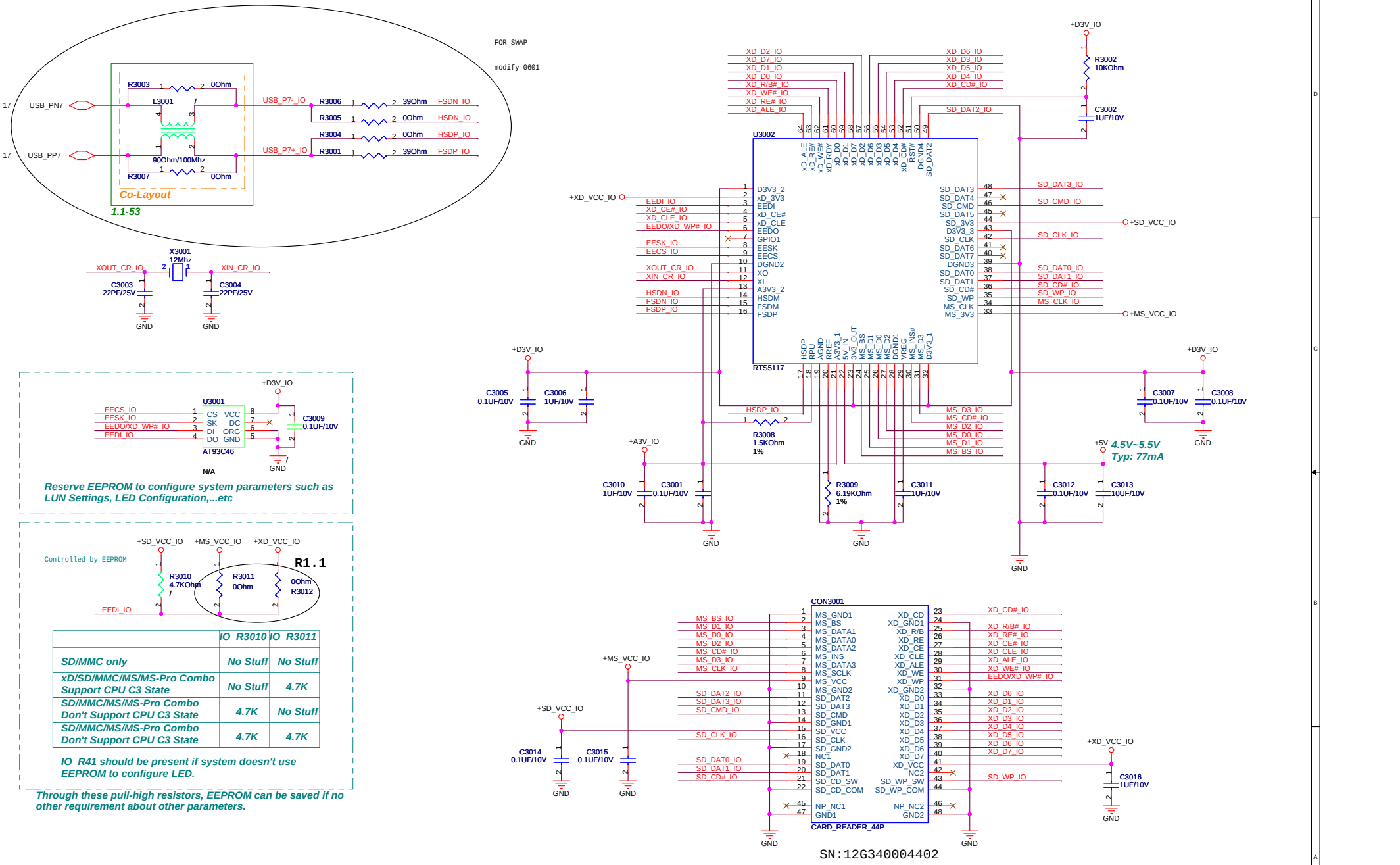
Title : NEWCARD

ASUSTeK COMPUTER INC

Engineer: Chris Liu,Andy Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 29 of 71



<Variant Name>

ASUSTeK COMPUTER INC

Title : CARD READER

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 30 of 71

<Variant Name>

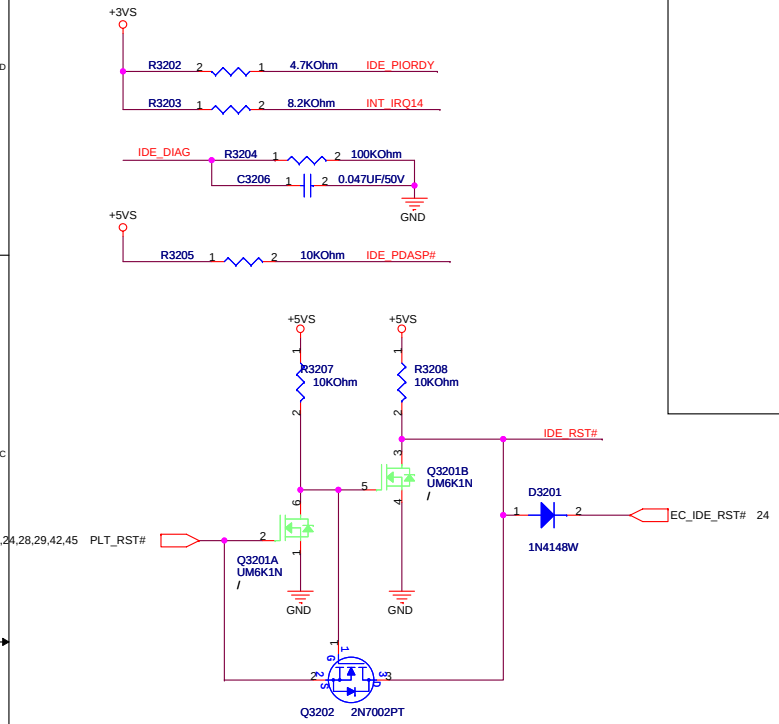
Title : *

ASUSTeK COMPUTER INC

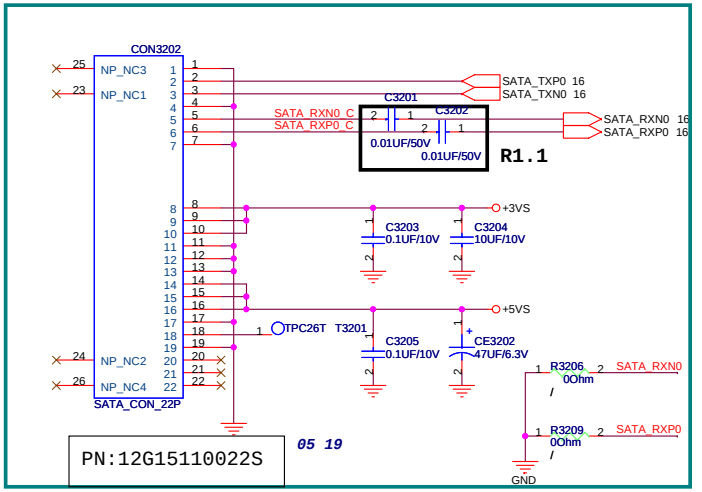
Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 31 of 71



modify 0512

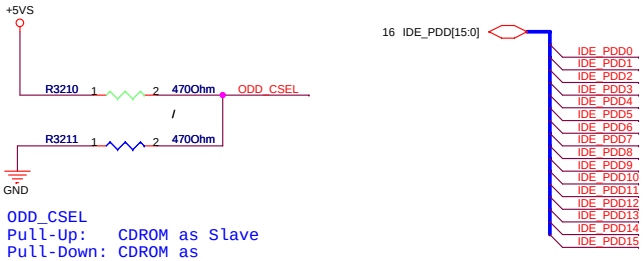


Dafult

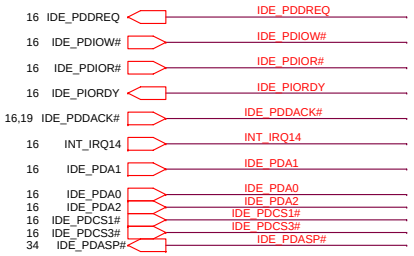
PATA

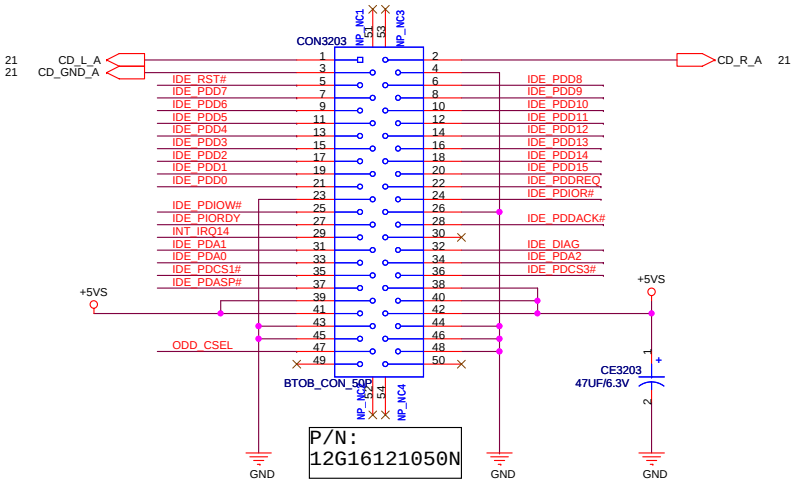
SATA

CD-ROM



ODD_CSEL
Pull-Up: CDROM as Slave
Pull-Down: CDROM as Master





update 05 18

<Variant Name>

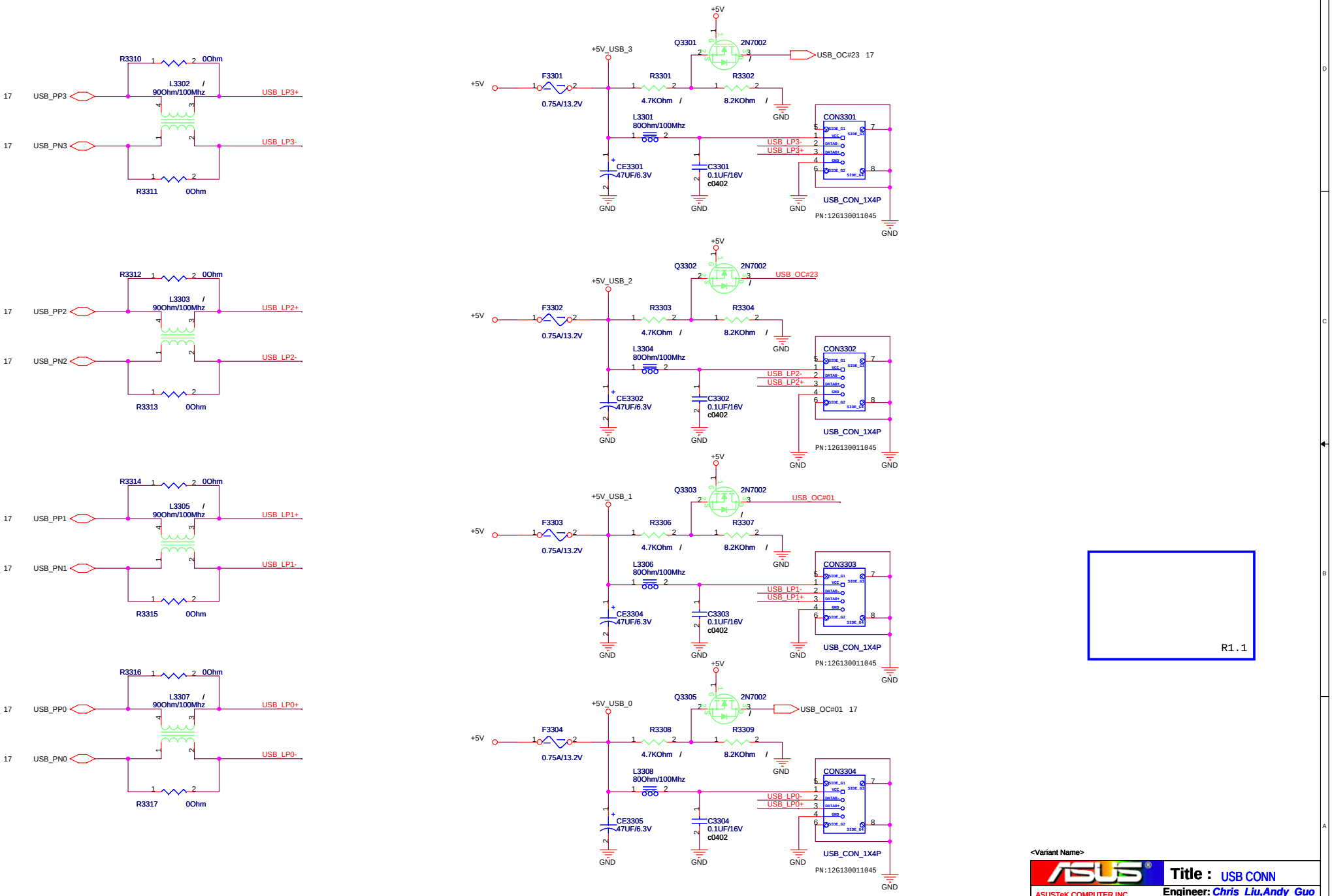
ASUSTeK COMPUTER INC

Title : HDD & CD-ROM

Engineer: Chris Liu,Andy Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 32 of 71



<Variant Name>

ASUSTeK COMPUTER INC

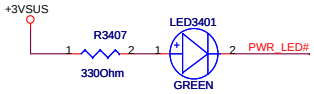
Title : USB CONN

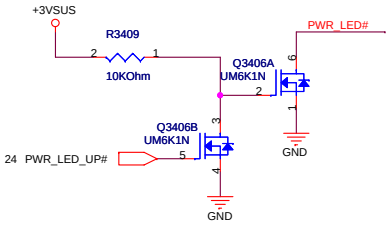
Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

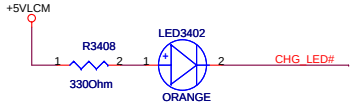
Date: Monday, July 31, 2006 Sheet 33 of 71

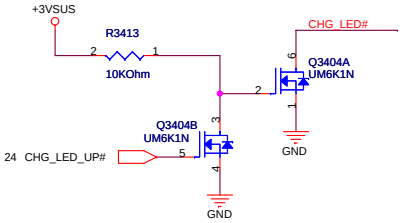
For POWER LED



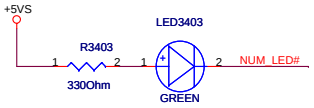


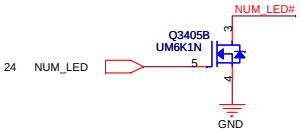
BATTERY LED



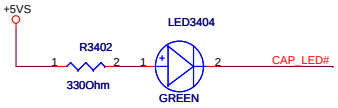


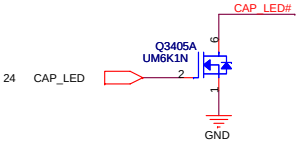
Num Lock



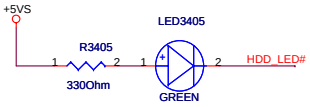


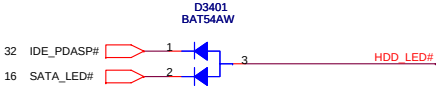
Cap Lock



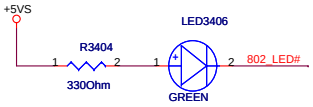


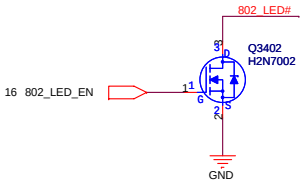
SATA/IDE LED



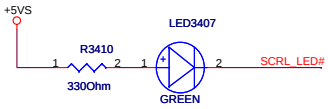


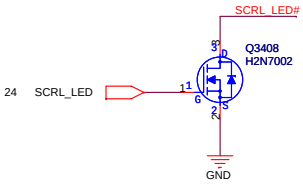
WireLess LED



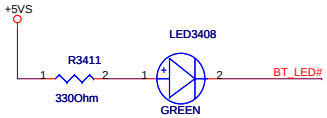


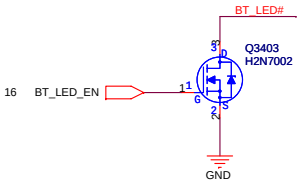
Scroll Lock





BT LED





<Variant Name>

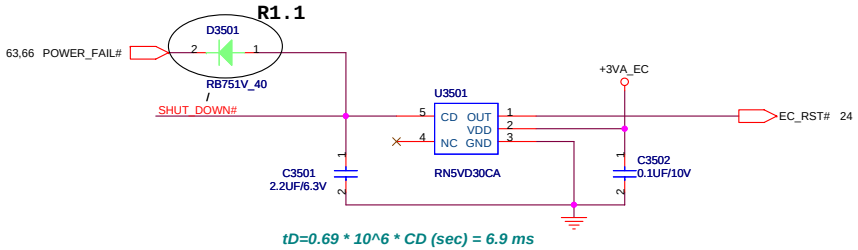
ASUSTeK COMPUTER INC

Title : LED

Engineer: Chris Liu,Andy Guo

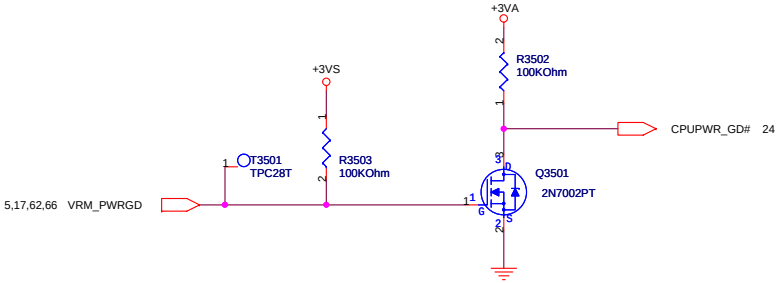
Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 34 of 71

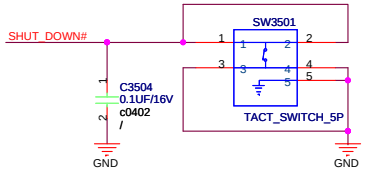


*tD=0.69 * 10^6 * CD (sec) = 6.9 ms*

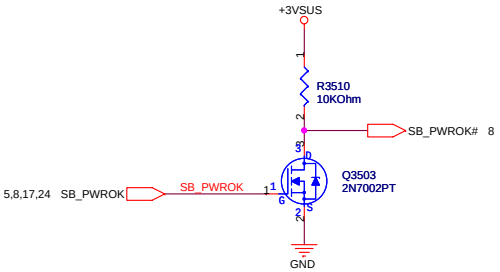
tD=0.69*10^6*CD pin sec **Change threshold = 2.9V**



RESET SW.



P/N: 12G091030050



<Variant Name>

ASUSTeK COMPUTER INC

Title : RST

Engineer: Chris_Liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

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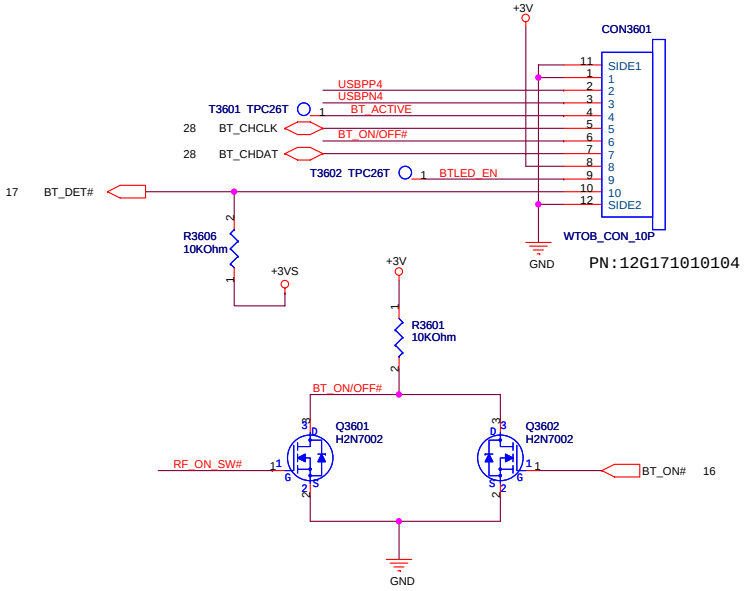
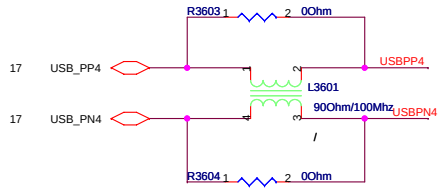
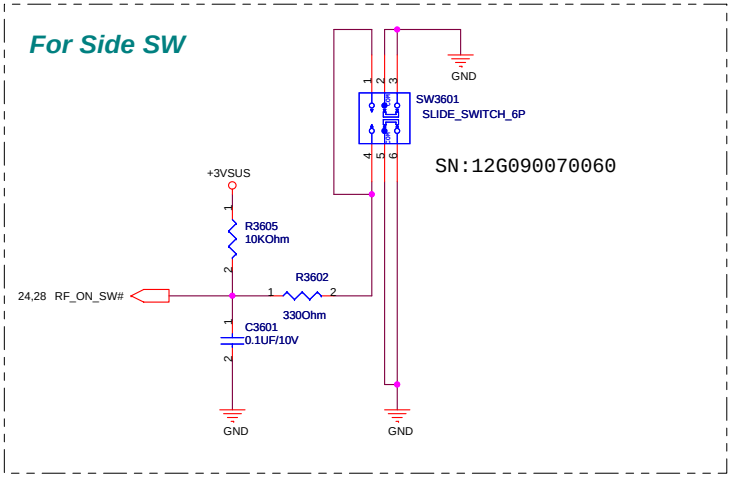
For Bluetooth





For Side SW



<Variant Name>

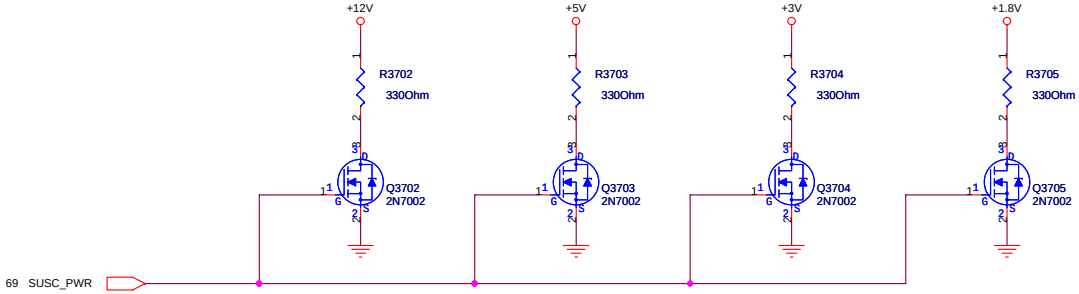
Title : BlueTooth

ASUSTeK COMPUTER INC

Engineer: Chris_Liu,Andy_Guo

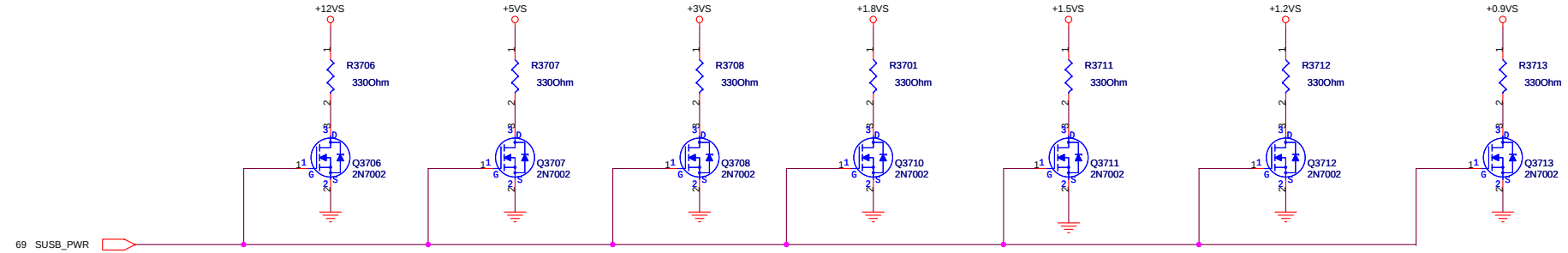
Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 36 of 71

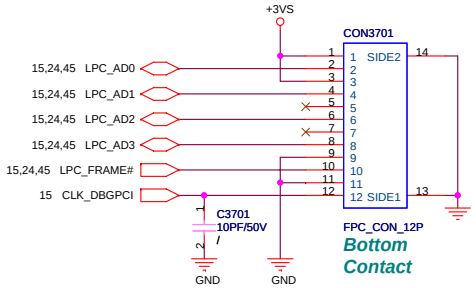


System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#

CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.2VS, +2.5V, +VCCP
SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS



Debug Port



<Variant Name>

Title : DISCHARGE CKT

ASUSTeK COMPUTER INC

Engineer: Chris Liu,Andy Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 37 of 71

above ODD connector

near cpu

near NB

D

pad3805 C138 GND
pad3806 C138 GND
pad3802 C138 GND
pad3808 C138 GND
pad3812 C138 GND
pad3811 C138 GND
pad3803 C138 GND
pad3809 C138 GND
pad3810 C138 GND
pad3801 C138 GND
pad3807 C138 GND
pad3804 C138 GND
pad3820 C138 GND
pad3821 C138 GND

K

pad3813 SMD98X315 GND

H

pad3822 SMD276x472 GND
pad3814 SMD276x472 GND

I

pad3815 SMD236X1181 GND

O

H3807 S315D91N GND GND

P R1.1

H3829 C256D98N GND GND

Q R1.1

H3830 CR315D91N GND GND

A

H3828 D91N&D87N GND GND

H near NEWCARD

pad3816 SMD276x472 GND
pad3818 SMD276x472 GND
pad3819 SMD276x472 GND
pad3835 SMD276x472 R1.1 GND

N

H3815 2DRILL_D91N_D71N GND GND

X R1.1

H3816 2DRILL_D91N_D87N GND GND

R R1.1

pad1822 C165 GND
pad3823 C165 GND
pad3824 C165 GND
pad3825 C165 GND

S R1.1

pad3826 C112 GND
pad3833 C112 GND

H3806 R335X335D91N GND GND
H3808 R335X335D91N GND GND
H3809 R335X335D91N GND GND
H3810 R335X335D91N GND GND
H3811 R335X335D91N GND GND
H3812 R335X335D91N GND GND
H3813 R335X335D91N GND GND

B

H3814 R335X335D91N GND GND

T R1.1

pad3828 SMD591x118 GND
pad3829 SMD591x118 GND

U R1.1

pad3831 SMD106x315 GND
pad3832 SMD106x315 GND

For EMI

pad3834 EMI_SPRING_PAD R1.1 GND

FOR CPU

H3817 CT268B138D138
H3819 CT268B138D138
H3821 CT268B138D138
H3823 CT268B138D138
GND

FOR Mini card

H3824 A40M20-64AS GND
H3825 A40M20-64AS GND

FOR MDC

H3801 L5-1A GND
H3802 L5-1A GND

FOR FAN

H3826 F5 R1.1 GND

<Variant Name>

ASUSTeK COMPUTER INC

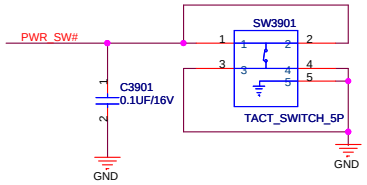
Title : Screw Hole

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

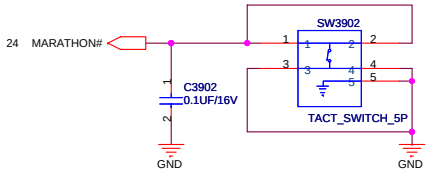
Date: Monday, July 31, 2006 Sheet 38 of 71

Power SW.

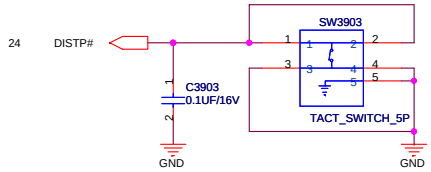


P/N: 12G091030050

Marathon SW.

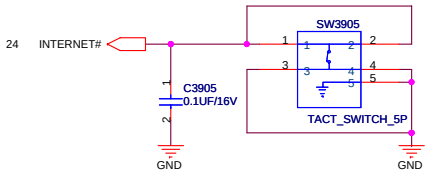


Disable Touch Pad SW.

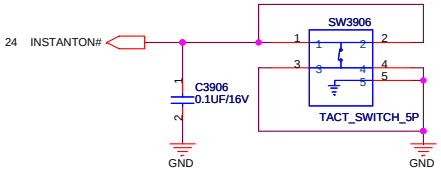


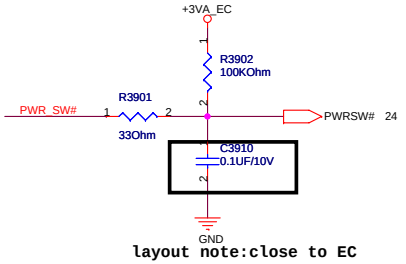
modify 05/17

Internet SW.



IstantON SW.

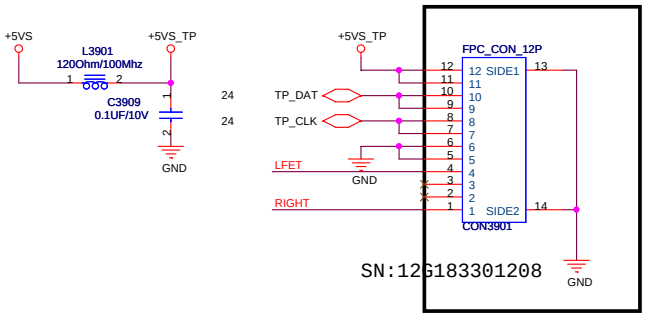


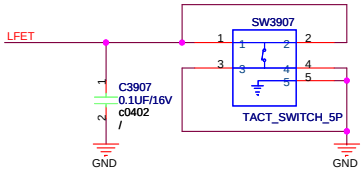


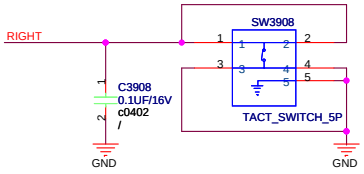
layout note:close to EC

Touch-Pad

R1.1







<Variant Name>

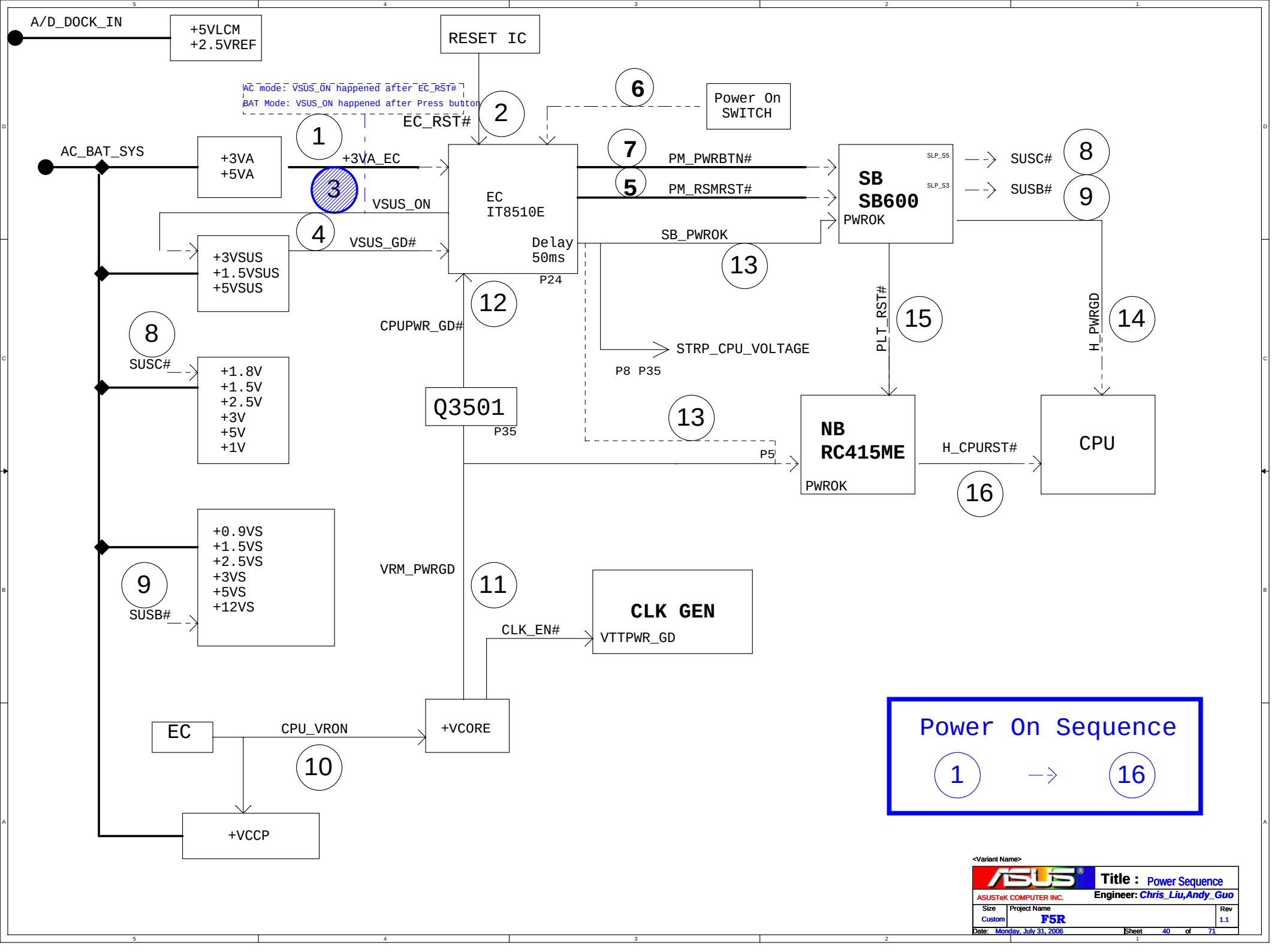
Title : SWITCH & TP

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 39 of 71


A/D_DOCK_IN
+5VLCM
+2.5VREF
RESET IC
AC mode: VSUS_ON happened after EC_RST#
BAT Mode: VSUS_ON happened after Press button
EC_RST#
2
6
Power On
SWITCH
AC_BAT_SYS
+3VA
+5VA
1
+3VA_EC
3
VSUS_ON
4
VSUS_GD#
EC
IT8510E
Delay
50ms
P24
7
PM_PWRBTN#
5
PM_RSMRST#
SB_PWROK
SB
SB600
PWROK
SLP_S5
SLP_S3
SUSC#
SUSB#
8
9
13
+3VSUS
+1.5VSUS
+5VSUS
12
CPUPWR_GD#
8
SUSC#
+1.8V
+1.5V
+2.5V
+3V
+5V
+1V
STRP_CPU_VOLTAGE
P8 P35
PLT_RST#
15
H_PWRGD
14
Q3501
P35
13
P5
NB
RC415ME
PWROK
H_CPURST#
CPU
16
+0.9VS
+1.5VS
+2.5VS
+3VS
+5VS
+12VS
9
SUSB#
VRM_PWRGD
11
CLK_EN#
CLK GEN
VTTPWR_GD
EC
CPU_VRON
10
+VCORE
+VCCP
Power On Sequence
1
16
<Variant Name>
Title : Power Sequence
ASUSTeK COMPUTER INC.
Engineer: Chris_Liu,Andy_Guo
Size
Custom
Project Name
F5R
Rev
1.1
Date: Monday, July 31, 2006
Sheet 40 of 71

<Variant Name>

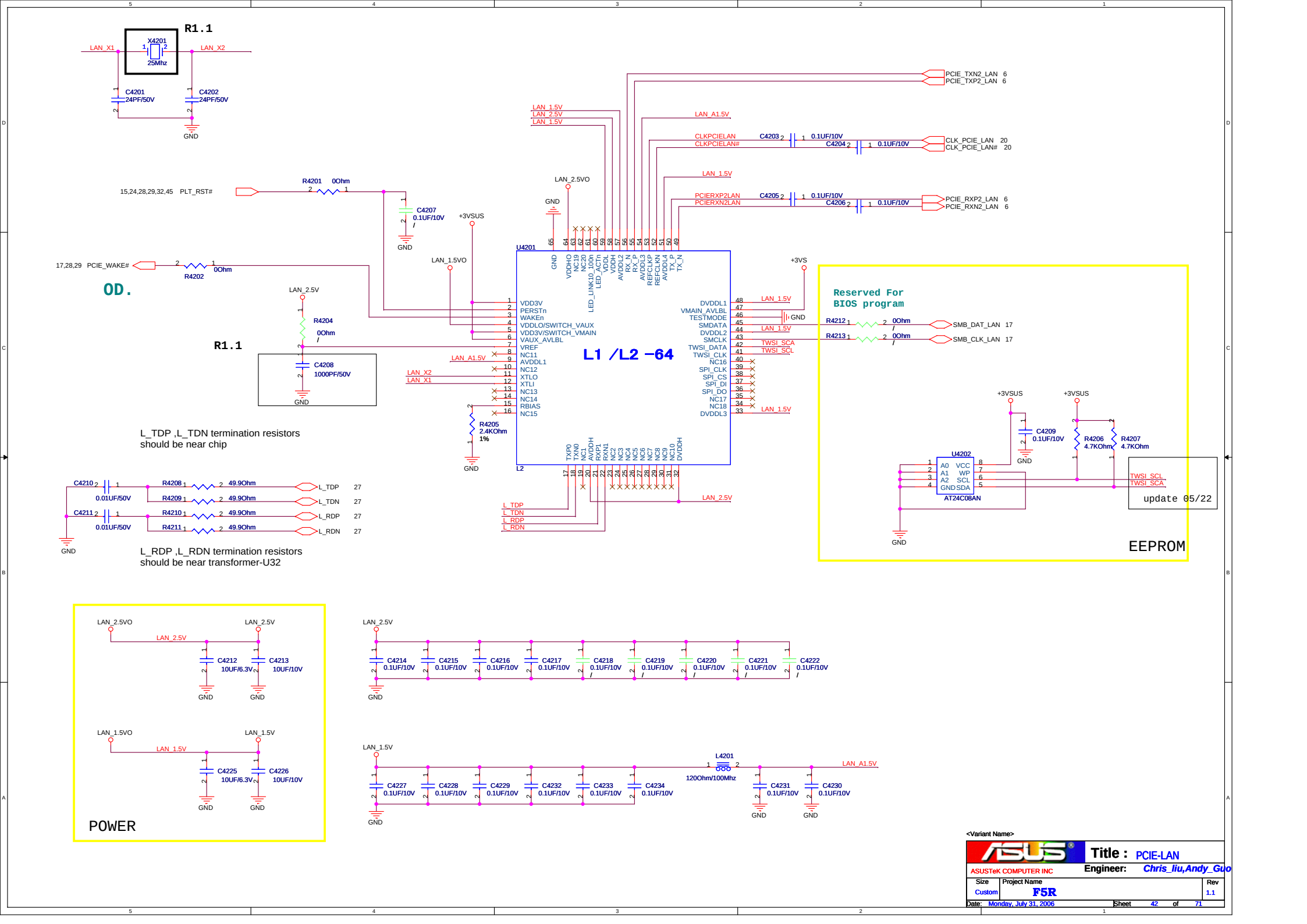
Title : *

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 41 of 71



<Variant Name>

Title : PCIE-LAN

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 42 of 71

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 43 of 71

<Variant Name>

Title : *

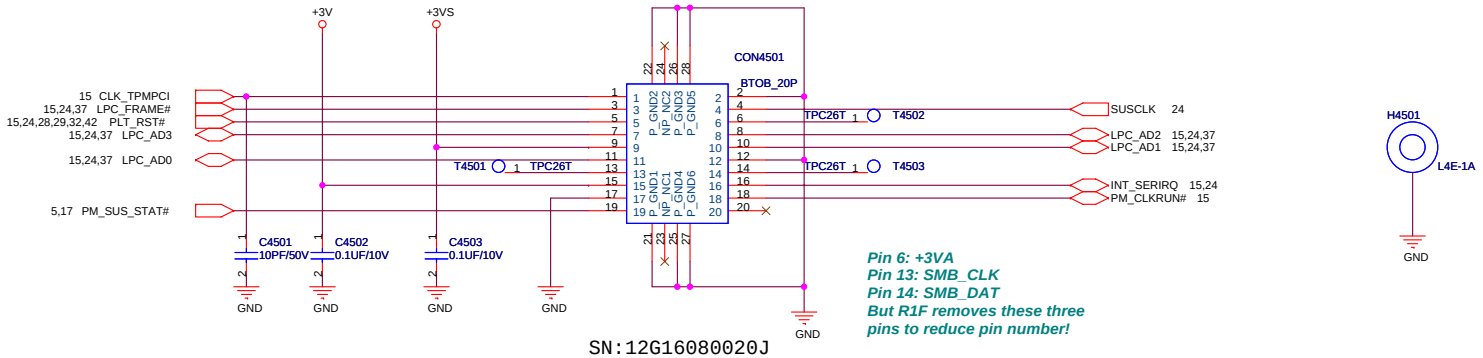
ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 44 of 71

For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

SN:12G16080020J

<Variant Name>

ASUSTeK COMPUTER INC

Title : TPM

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 45 of 71

change list:

06-05-12

1. page16, add another thermal sensor schematic according to ATI demo schematic.
2. page32. delete PATA HDD connector according to ME request
3. page 12.13.17.add mem_sensor according to ATI demo schematic

06-05-15

1. Add the ITP function on page 2,20,24.
2. Page 24 delete the PWRLIMIT# net (power part has delete the power limit function)

06-05-16

1. connect BATSEL_3S# to EC pin 40

05-06-17

1. pag39 delete sw3904 according to markeeting spec
2. page 22 add L2210 for layout request
3. add L2303 for layout request

06-05-18

1. page 32 update ODD connector CON3203 P/N
2. PAGE 29 modify NEWCARD connector U2902 P/N

06-05-19

1. page 32 update SATA connector CON3202 P/N

06-05-22

1. page 5 change R510 to D501 according to F5X
2. page5 ADD R513 according to F5X
3. page 8 Remove L809,C811 according to ATI demo schematic
4. page10 mount L1011,unmount L1015 due to using the D/A inverter
5. page 15 remove R1524 due to SB600 (for Yonah)do not support H_PROCHOT
6. page 16 mount R1604 according to ATI suggestion
7. Page 17 add R1733,R1733 according to ATI suggestion
8. Page 30mount U3001,C3009 according to F5X
9. Page 38 add screw hole and pad
10. Page 42 exchange TWSI_SCA and TWSI_SCL

06-05-23

1. Page27 Add R2708 pull up resistor for Attansic request
2. Page27 change C2702,C2703 to close to CON2702

06-05-24

1. page12 modify CON1201 P/N

06-05-25

1. Page38 add H3826 for lock fan
2. delete some screw hole and add pad3820,pad3821

06-05-26

1. page 38 add screw hole H3815 H3816

06-05-29

1. page 17 exchange net USB_PP5 and USB_PP3,exchange net USB_PN5 and USB_PN3
2. page 24 connect RF_ON_SW# to EC pin 25
3. page16 connect net BT_ON# to SB600 GPIO47
4. page 16connect net 802_LED_EN to GPIO55
5. page 16 connect net BT_LED_EN to GPIO56

06-05-30

1. page 22 connect con2202 pin 5,pin6 to GND_AUDIO

06-06-01

1. Page 29 swap USB_PP6 and USB_PN6
2. Page 30 swap USB_PP7 and USB_PN7
3. Page 17 add pull up resistor R1735 and R1736,decoupling capacitor C1709 and C1710 on the USB_OC#01,USB_OC#23
4. Page17 add test point T1725,T1726
5. Page8 add test point T813

06-06-05

1. page38 change H3807 P/N
2. page22 delete net GND JACK
3. page23 delete net GND JACK and JP2302

06-06-06

Page 5 Add resistor R514 accordintg to Frank's suggestion
Page 8 Add resistor R828 accordintg to Frank's suggestion
Page 23 Add resistor R2311 for EMI request
Page 23 change GND to GND_AUDIO for EMI request
Page 3 Add C330 and C331 for EMI suggestion
Page 65 connect PR6507 pin 2 to +12VS
Page 24 delete Q2407 for repeat
Page 29 Add R2905,unmout d2901 for cost down
Page 21 change U2102 for cost down
Page 20 change U2001 for thermal request

06-06-07

Page 29 Modify the CON2901 schematic
Page 14 delete RN1405,CN1405
Page 16 connect VIN4 to R2902 for newcard shut down
Page 17 connect USB_OC#8 to D2904,D2905 FOR NEW CARD DETECT
Page 29 ADD R2902, D2904,D2905
page 38 change pad3819 connect to GND for EMI request
Page 29 swap USB_PP6 and USB_PN6

06-08

page4 change CE401 P/N for hight limit

R1.1

Page3 DNI CE301,CE302,CE303,CE304,CE305
Page4 R401,R406 change to 0 ohm
Page5 R513 cahnge to 220K ohm,Mount R514, DNI R511
Page8 add (L809 and C811)DNI for RC610
Page16 X1601 change to PN:07G010Q02501 for cost
Page22 R2201,R2203 change to 0ohm DNI R2205,R2206 chenge U2201 P/N for cost down
page 24 R2404 change to 4.7Kohm
Page27 R2708 change to 0 ohm,change CON2702 P/N
Page28 Mount Q2803 for BIOS request
Page30 R3011,R3012 change to 0 ohm according to attansic demo schematic
Page32 C3201,C3202 change to 0.01u
Page39 Reverse CON3901 pin definition for ME request
Page42 X4201 change to PN:07G010Q02501 for cost down
Page 2 change R227 pull-up resistor from 200 ohm resistor to 470 ohm resistor according ATI suggestion
Page 5 remove D502 (for SB600,it is no need)
Page 8 chang Q803 from N-MOS to P-MOS,add Q804 for correction
Page11 correct HSYNC YSYNC the ESD prodection diodes connect to +5VS instead of +3vs.
page 15 add 8.2Kohm 5% pull-down resistor on A_RST# to ensure a logic low at initial power-on.
Page 16 Please leave pin SATA_RX1/2/3+/- unconnected, do not connected them to ground according to ATI suggestion
Page 16 remove R1609,RN1601according to ATI suggestion
Page 17 change R1730,R1731,R1732 pull-up resistor to +3.3VSUS
page 38 add EMI finger
page 16 change C1611,C1612 from 24pf to 10pf

<Variant Name>

ASUSTeK COMPUTER INC

Title : change list

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 46 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 47 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 48 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 49 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 50 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 51 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 52 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 53 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 54 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 55 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 56 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 57 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 58 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 59 of 71

<Variant Name>

Title : GPIO SETTING

ASUSTeK COMPUTER INC

Engineer: Chris_liu,Andy_Guo

Size	Project Name	Rev
Custom	F5R	1.1

Date: Monday, July 31, 2006 Sheet 60 of 71

<Variant Name>

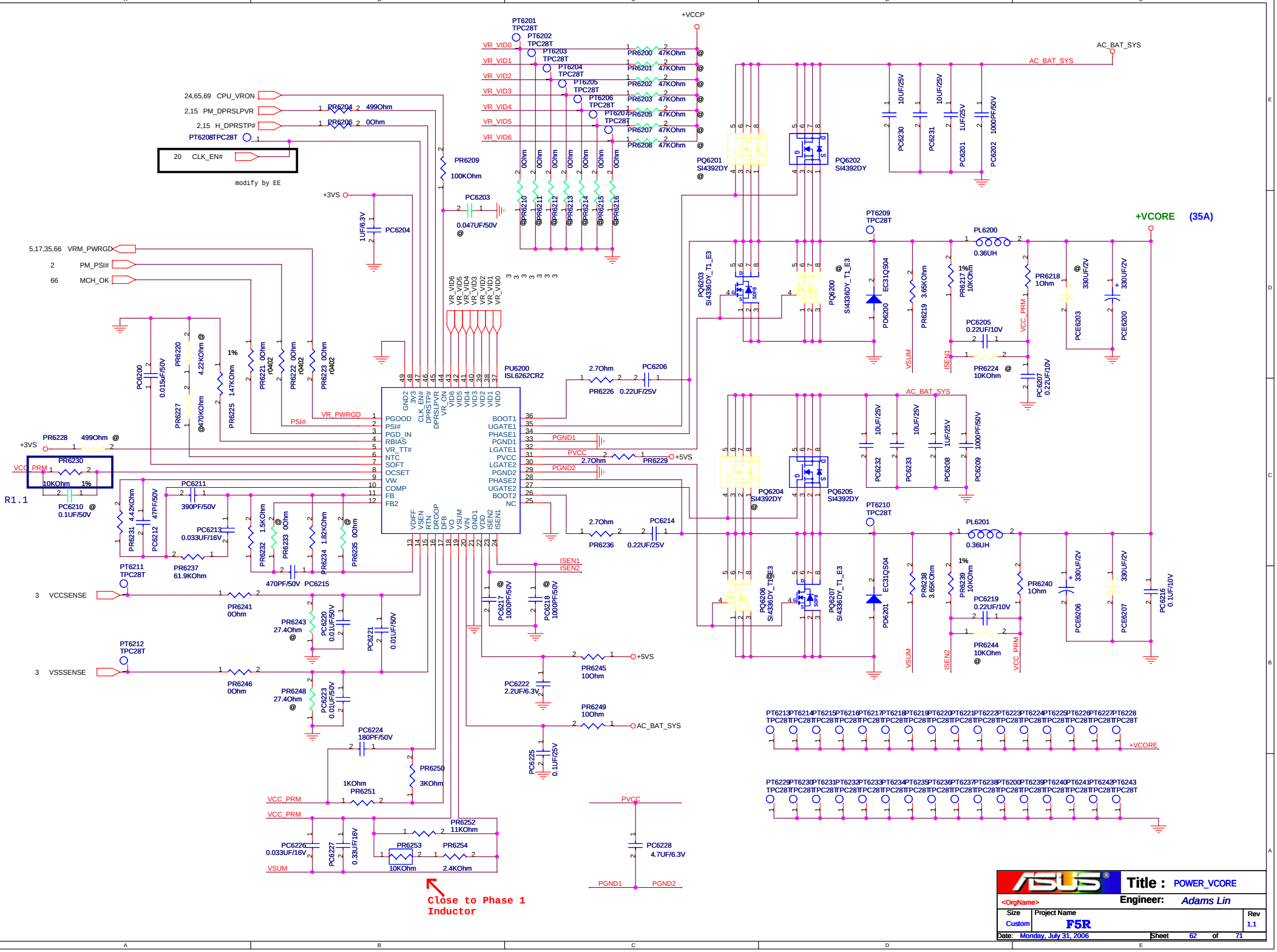
Title : GPIO SETTING

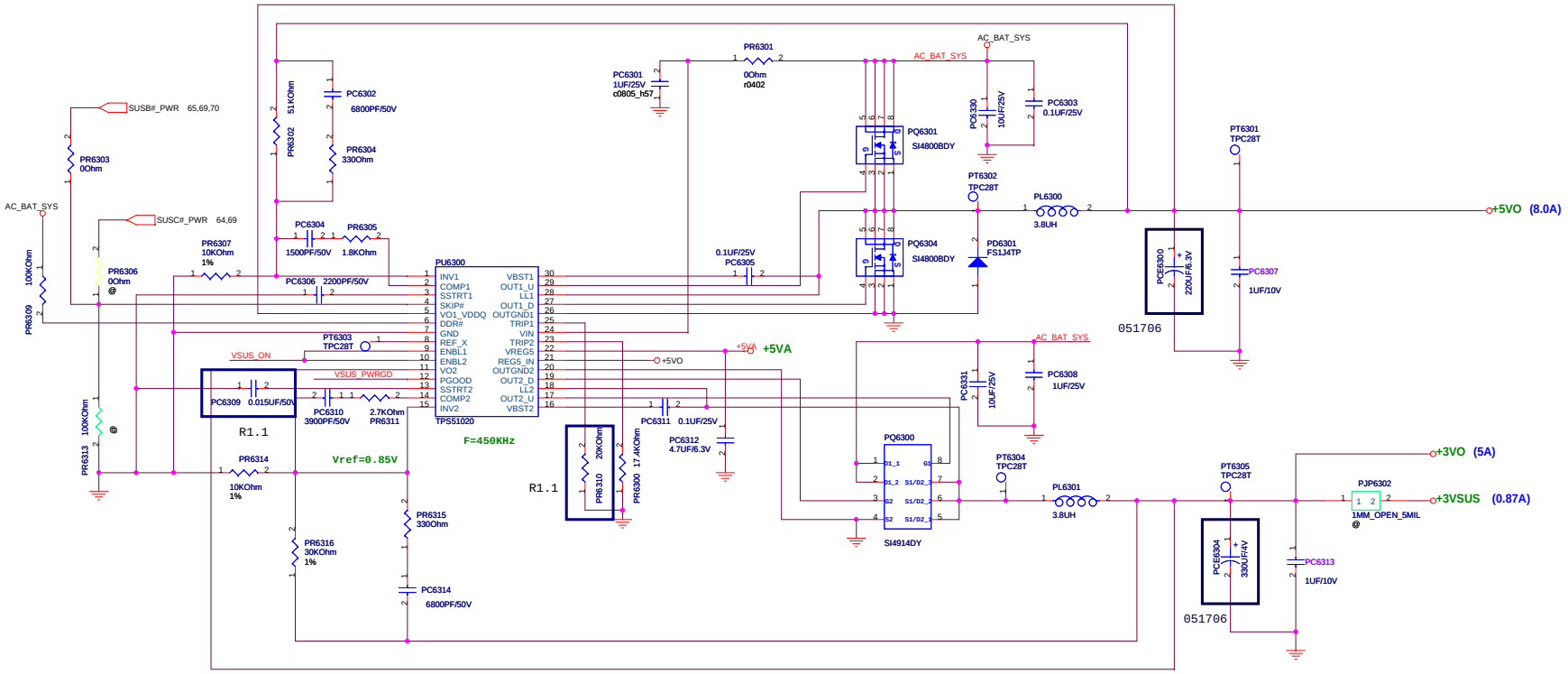
ASUSTeK COMPUTER INC

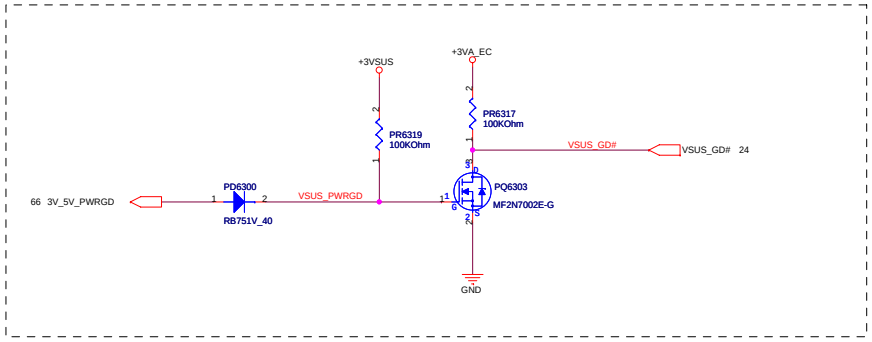
Engineer: Chris_liu,Andy_Guo

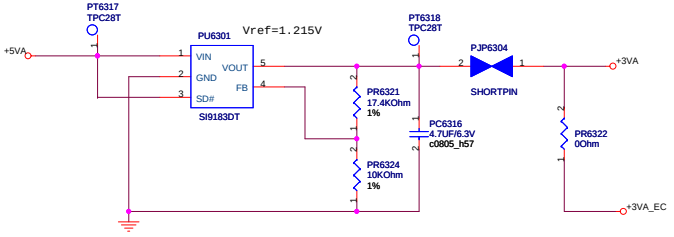
Size	Project Name	Rev
Custom	F5R	1.1

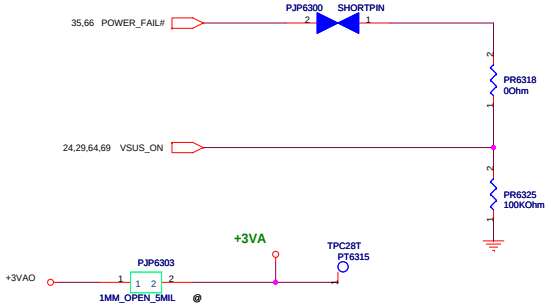
Date: Monday, July 31, 2006 Sheet 61 of 71

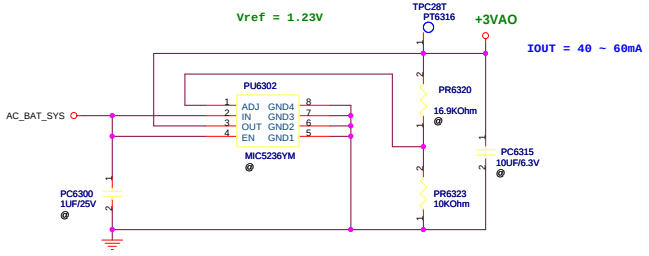

+VCCP
AC_BAT_SYS
+VCORE (35A)
PU6200 ISL6262CRZ
PQ6201 SI4392DY
PQ6202 SI4392DY
PQ6204 SI4392DY
PQ6205 SI4392DY
PQ6200 SI4336DY_T1_E3
PQ6203 SI4336DY_T1_E3
PQ6206 SI4336DY_T1_E3
PQ6207 SI4336DY_T1_E3
PD6200 EC31QS04
PD6201 EC31QS04
PL6200 0.36UH
PL6201 0.36UH
PR6200 47KOhm
PR6201 47KOhm
PR6202 47KOhm
PR6203 47KOhm
PR6204 499Ohm
PR6205 47KOhm
PR6206 0Ohm
PR6207 47KOhm
PR6208 47KOhm
PR6209 100KOhm
PR6210 0Ohm
PR6211 0Ohm
PR6212 0Ohm
PR6213 0Ohm
PR6214 0Ohm
PR6215 0Ohm
PR6216 0Ohm
PR6217 10KOhm
PR6218 1Ohm
PR6219 3.65KOhm
PR6224 10KOhm
PR6225 147KOhm
PR6226 0.22UF/25V
PR6227 @470KOhm
PR6228 499Ohm @
PR6229 +5VS
PR6230 10KOhm 1%
PR6231 4.42KOhm
PR6232 1.5KOhm
PR6233 0Ohm
PR6234 1.82KOhm
PR6235 0Ohm
PR6236 0.22UF/25V
PR6237 61.9KOhm
PR6238 3.65KOhm
PR6239 10KOhm
PR6240 1Ohm
PR6241 0Ohm
PR6243 27.4Ohm @
PR6244 10KOhm @
PR6245 10Ohm
PR6246 0Ohm
PR6248 27.4Ohm @
PR6249 10Ohm
PR6250 3KOhm
PR6251 1KOhm
PR6252 11KOhm
PR6253 10KOhm
PR6254 2.4KOhm
PC6200 0.015UF/50V
PC6201 1UF/25V
PC6202 1000PF/50V
PC6203 0.047UF/50V @
PC6204 1UF/6.3V
PC6205 0.22UF/10V
PC6206 0.22UF/25V
PC6207 0.22UF/10V
PC6208 1UF/25V
PC6209 1000PF/50V
PC6210 0.1UF/50V @
PC6211 390PF/50V
PC6212 47PF/50V
PC6213 0.033UF/16V
PC6214 0.22UF/25V
PC6215 470PF/50V
PC6216 0.1UF/10V
PC6217 1000PF/50V @
PC6218 1000PF/50V @
PC6220 0.01UF/50V
PC6221 0.01UF/50V
PC6222 2.2UF/6.3V
PC6223 0.01UF/50V
PC6224 180PF/50V
PC6225 0.1UF/25V
PC6226 0.033UF/16V
PC6227 0.33UF/16V
PC6228 4.7UF/6.3V
PC6230 10UF/25V
PC6231 10UF/25V
PC6232 10UF/25V
PC6233 10UF/25V
PC6208 1UF/25V
PC6209 1000PF/50V
PCE6200 330UF/2V
PCE6203 330UF/2V @
PCE6205 330UF/2V
PCE6206 330UF/2V
PCE6207 330UF/2V
PT6201 TPC28T
PT6202 TPC28T
PT6203 TPC28T
PT6204 TPC28T
PT6205 TPC28T
PT6206 TPC28T
PT6207 TPC28T
PT6208TPC28T
PT6209 TPC28T
PT6210 TPC28T
PT6211 TPC28T
PT6212 TPC28T
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
24,65,69 CPU_VRON
2,15 PM_DPRSLPVR
2,15 H_DPRSTP#
20 CLK_EN#
modify by EE
5,17,35,66 VRM_PWRGD
2 PM_PSI#
66 MCH_OK
VR_PWRGD
PSI#
+3VS
+5VS
VCC_PRM
R1.1
3 VCCSENSE
3 VSSSENSE
VSUM
ISEN1
ISEN2
PVCC
PGND1
PGND2
PT6213PT6214PT6215PT6216PT6217PT6218PT6219PT6220PT6221PT6222PT6223PT6224PT6225PT6226PT6227PT6228
TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28T
PT6229PT6230PT6231PT6232PT6233PT6234PT6235PT6236PT6237PT6238PT6200PT6239PT6240PT6241PT6242PT6243
TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28T
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer: Adams Lin
<OrgName>
Size Custom
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 62 of 71

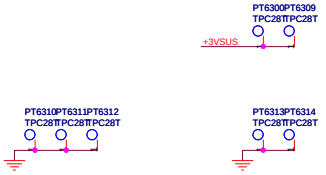




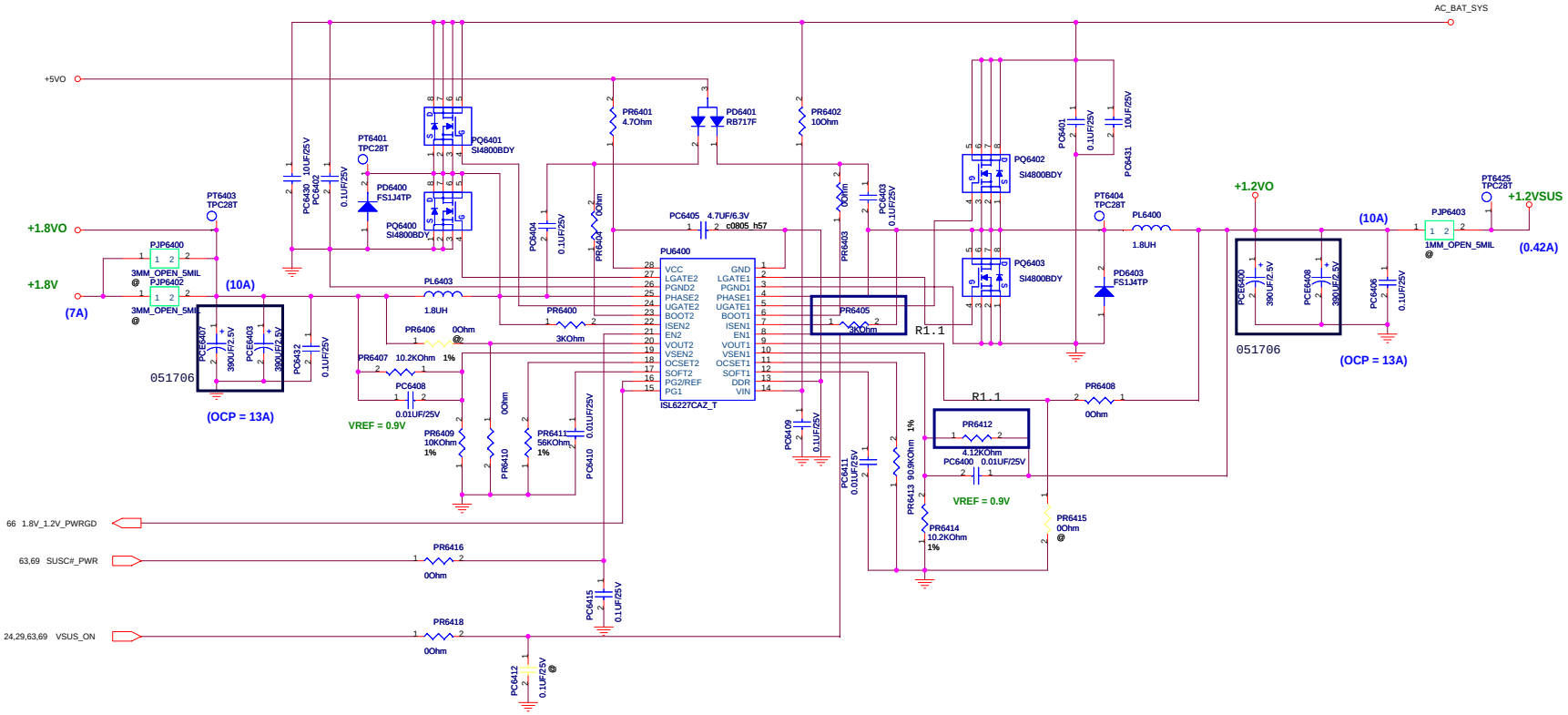


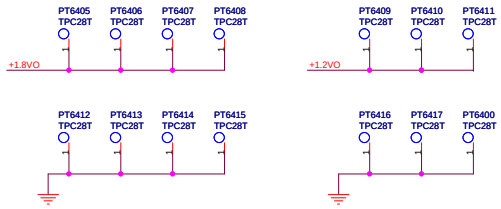


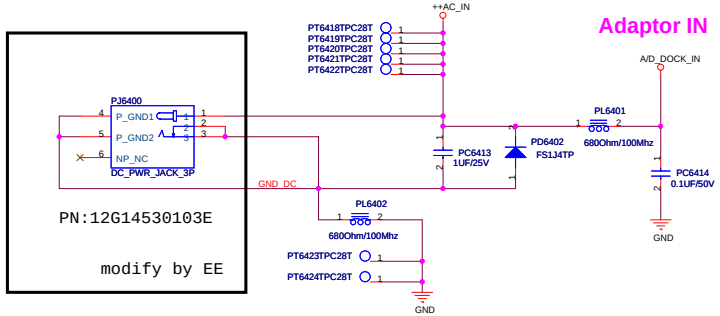




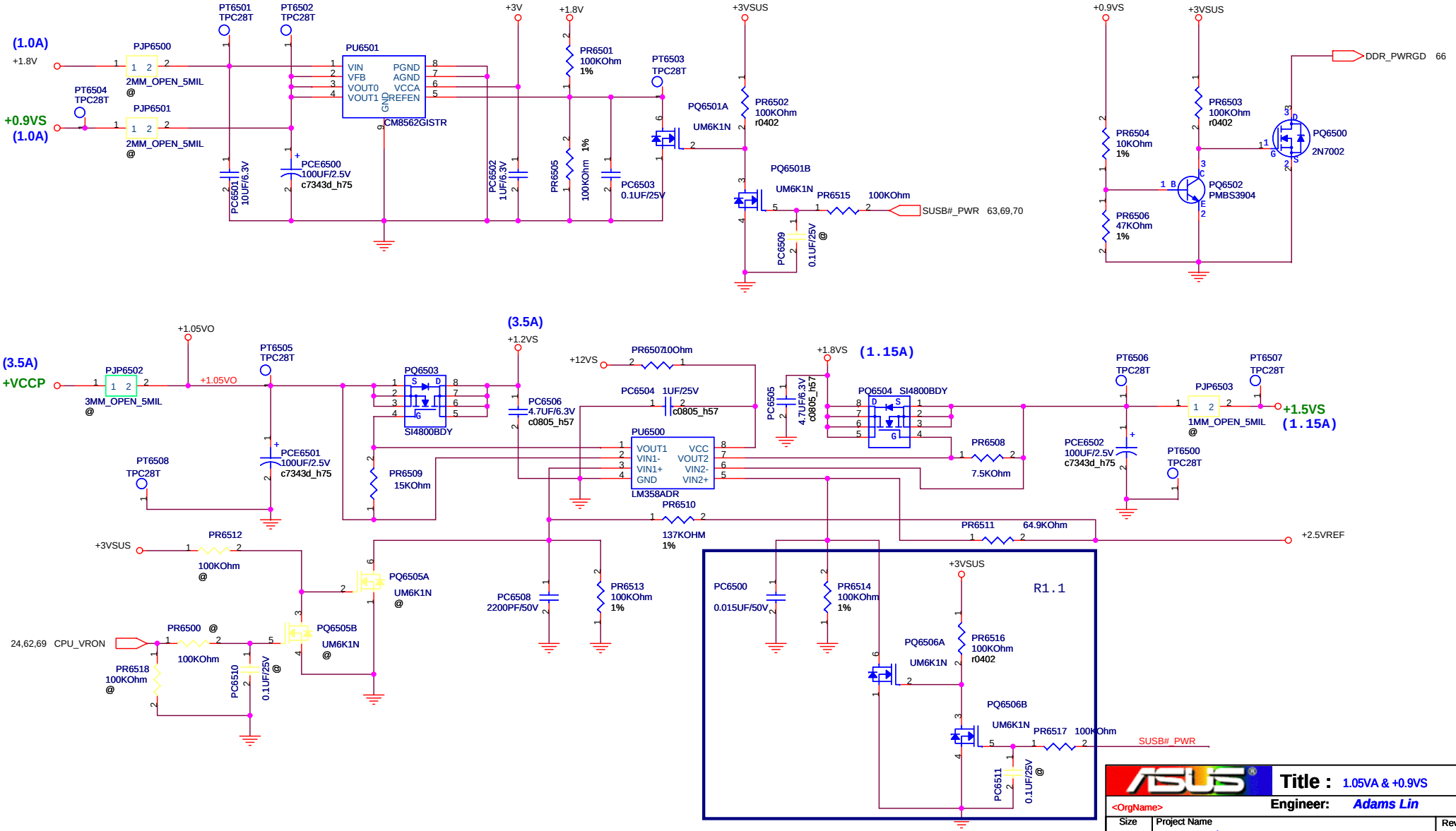
ASUS	Title :	SYSTEM_+5VA & +3VA
<OrgName>	Engineer:	Adams Lin
Size: C	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 63 of 71	



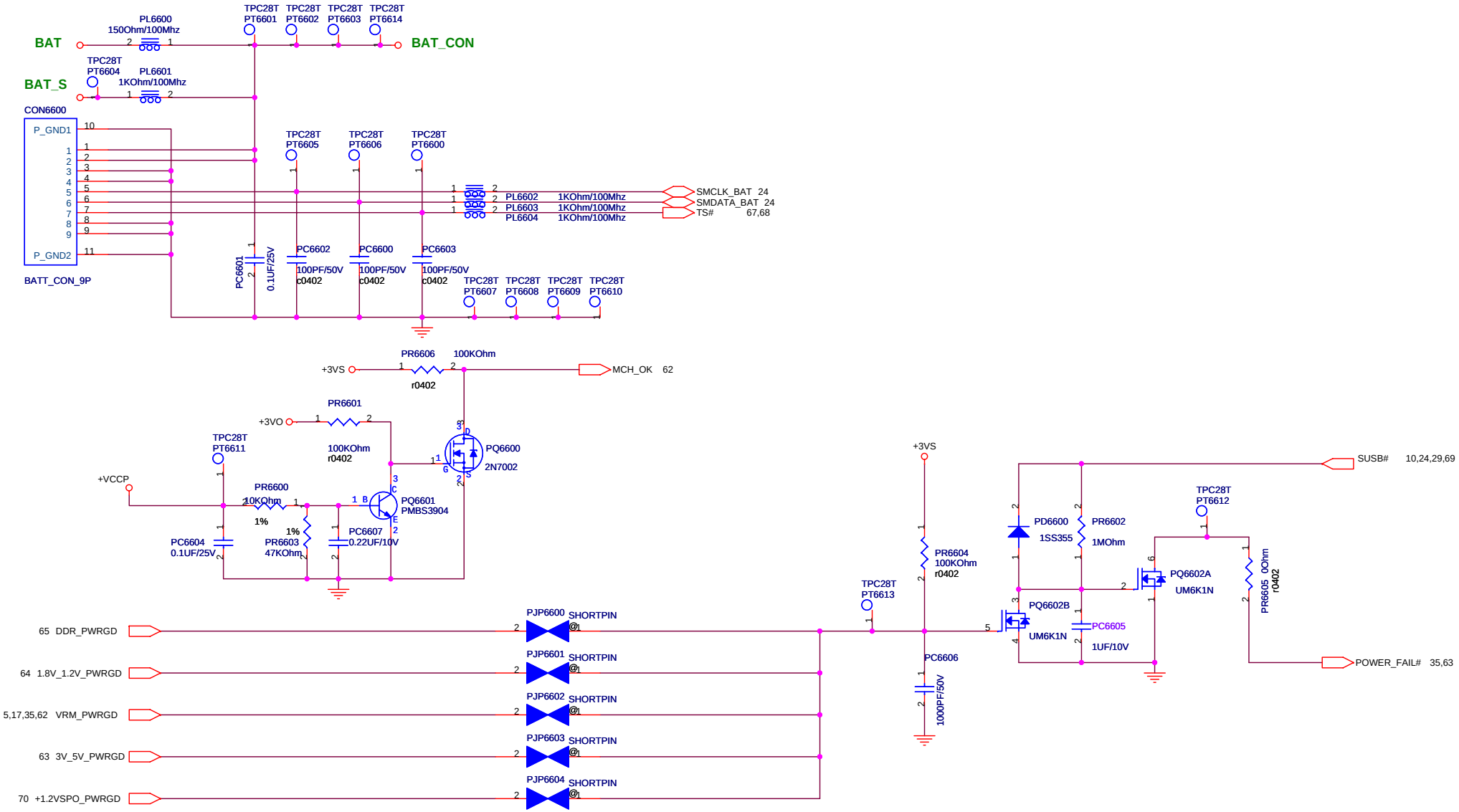




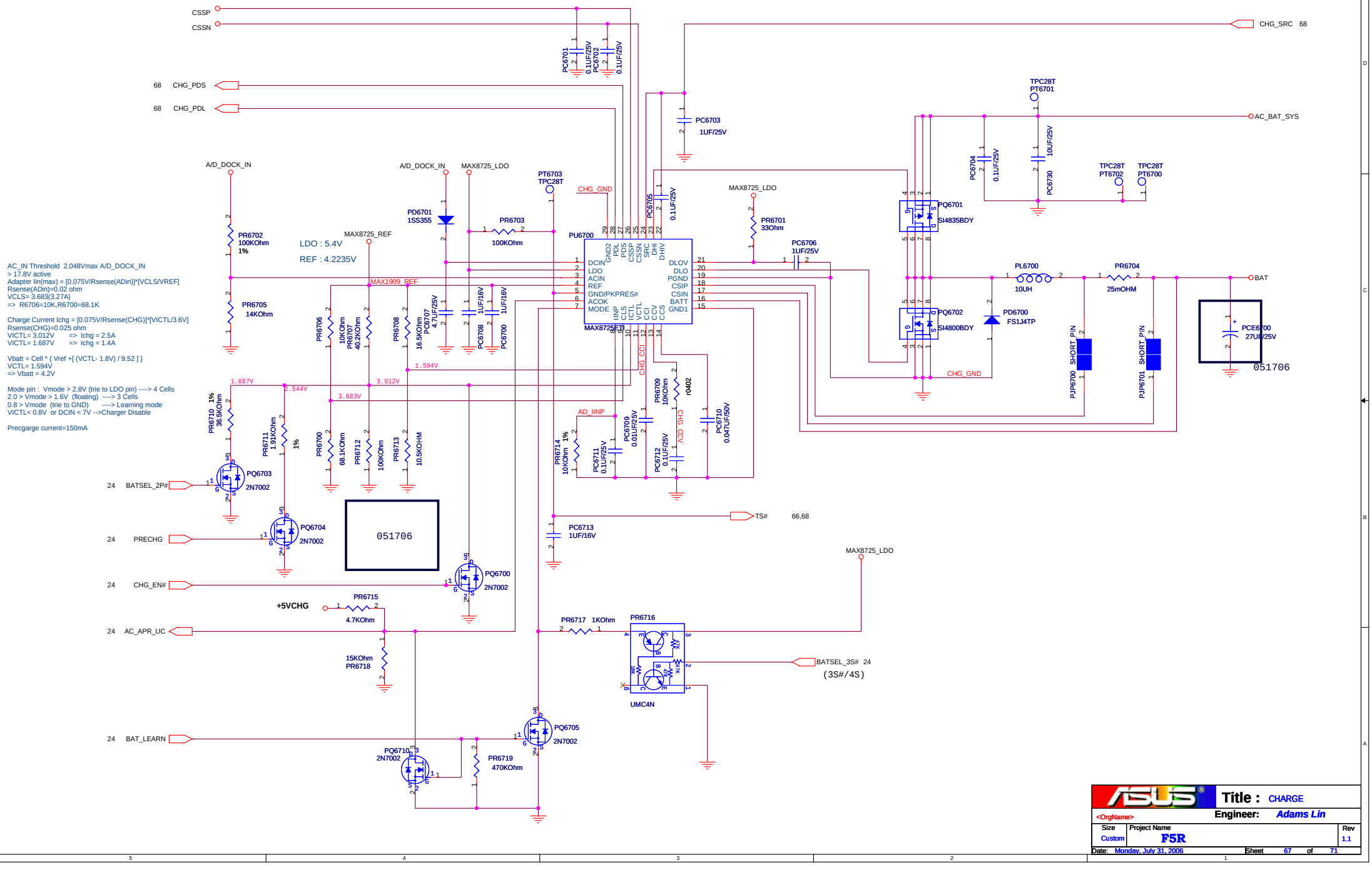
ASUS	Title : 1.8V&1.2VS	
<OrgName>	Engineer: Adams Lin	
Size: C	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 64 of 71	



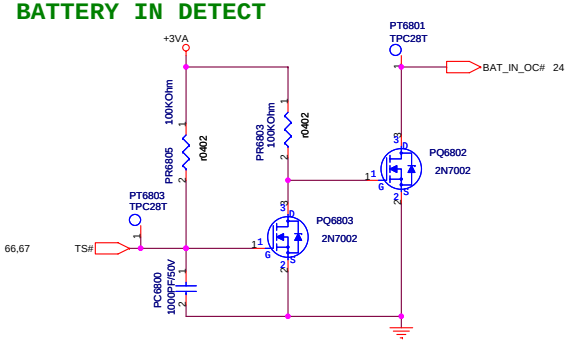
Title : 1.05VA & +0.9VS		
<OrgName>	Engineer: Adams Lin	
Size: B	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 65 of 71	

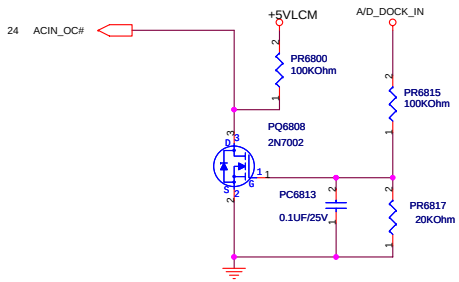


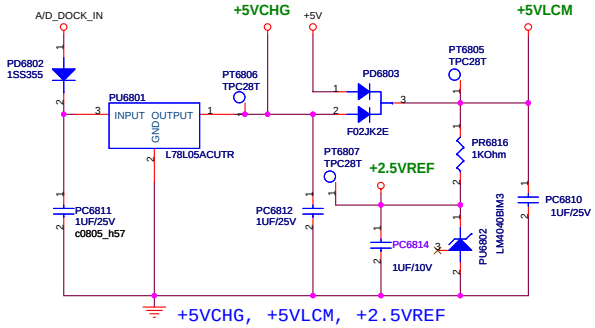
Title : BAT CON/PWOK		
<OrgName>	Engineer: Adams Lin	
Size: B	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 66 of 71	

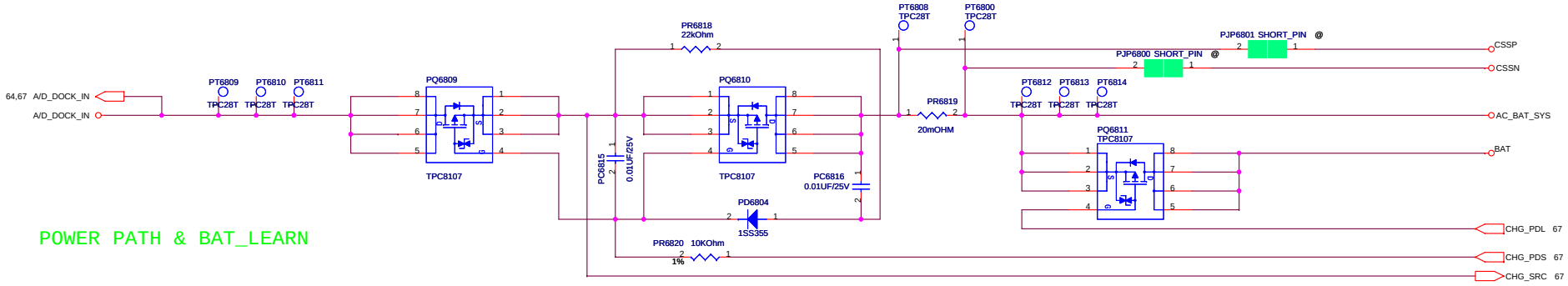

CSSP
CSSN
CHG_SRC 68
68 CHG_PDS
68 CHG_PDL
AC_BAT_SYS
BAT
A/D_DOCK_IN
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
MAX1909_REF
PU6700
MAX8725ETJ
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
CHG_GND
CHG_CCI
CHG_CCV
AD_IINP
PD6701 1SS355
PR6703 100KOhm
PR6701 33Ohm
PR6702 100KOhm 1%
PR6705 14KOhm
PC6703 1UF/25V
PC6706 1UF/25V
PC6705 0.1UF/25V
PC6701 0.1UF/25V
PC6702 0.1UF/25V
PC6704 0.1UF/25V
PC6730 10UF/25V
PQ6701 SI4835BDY
PQ6702 SI4800BDY
PD6700 FS1J4TP
PL6700 10UH
PR6704 25mOHM
PJP6700 SHORT_PIN
PJP6701 SHORT_PIN
PCE6700 27UF/25V
TPC28T PT6701
TPC28T PT6702
TPC28T PT6700
PR6706 10KOhm
PR6707 40.2KOhm
PR6708 16.5KOhm
PC6707 4.7UF/25V
PC6708 1UF/16V
PC6700 1UF/16V
PR6709 10KOhm
PC6709 0.01UF/25V
PC6710 0.047UF/50V
PR6714 10KOhm 1%
PC6711 0.1UF/25V
PC6712 0.1UF/25V
PC6713 1UF/16V
PR6710 1% 36.5KOhm
PR6711 1.91KOhm 1%
PR6700 68.1KOhm
PR6712 100KOhm
PR6713 10.5KOHM
1.687V
2.544V
3.683V
3.612V
1.594V
PQ6703 2N7002
PQ6704 2N7002
PQ6700 2N7002
PQ6705 2N7002
PQ6710 2N7002
051706
24 BATSEL_2P#
24 PRECHG
24 CHG_EN#
24 AC_APR_UC
24 BAT_LEARN
TS# 66,68
+5VCHG
PR6715 4.7KOhm
15KOhm PR6718
PR6717 1KOhm
PR6716
UMC4N
BATSEL_3S# 24
(3S#/4S)
PR6719 470KOhm
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.8V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.683(3.27A)
=> R6706=10K,R6700=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.012V => Ichg = 2.5A
VICTL= 1.687V => Ichg = 1.4A
Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.594V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
Title : CHARGE
Engineer: Adams Lin
<OrgName>
Size Custom
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 67 of 71

BATTERY IN DETECT



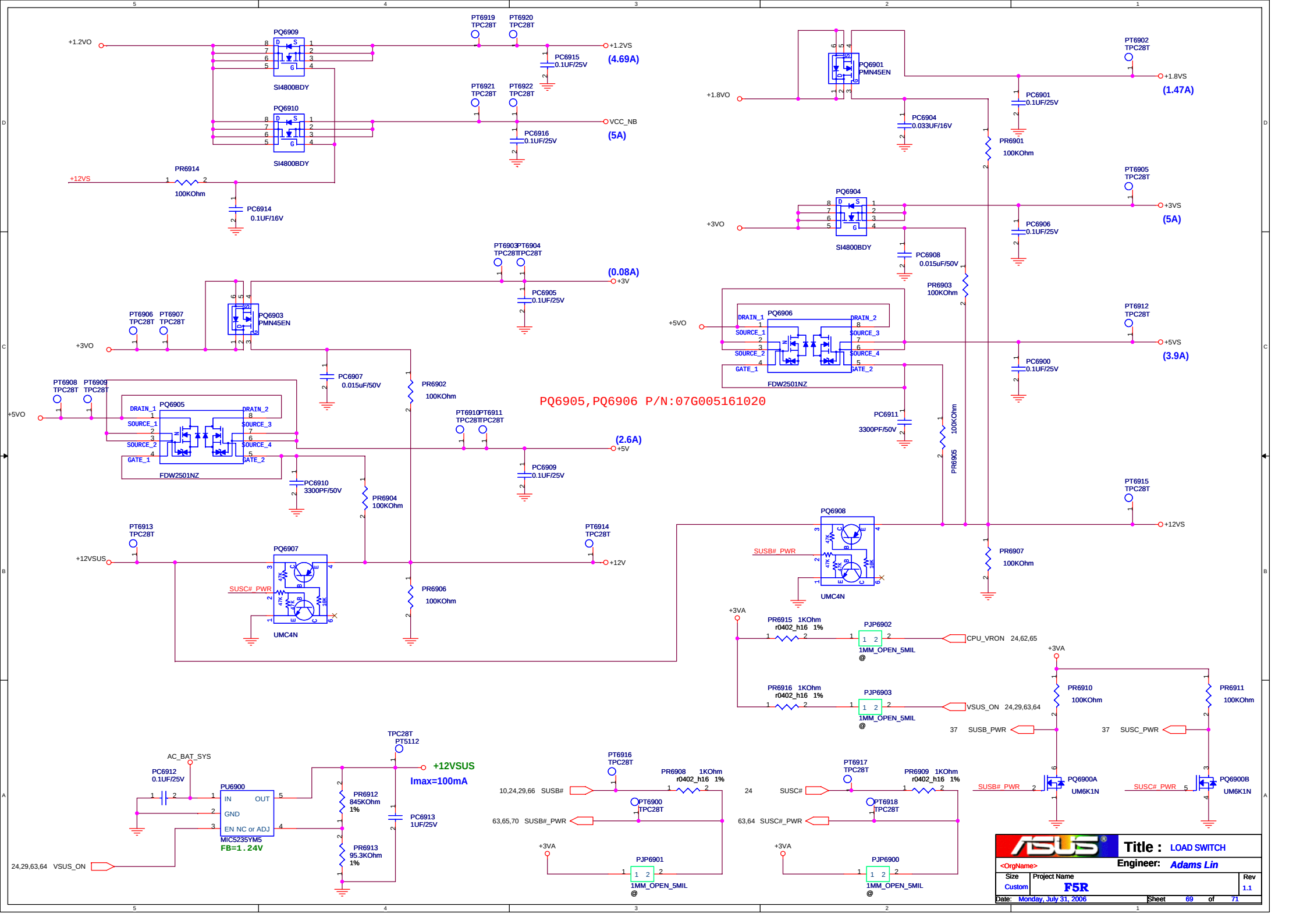


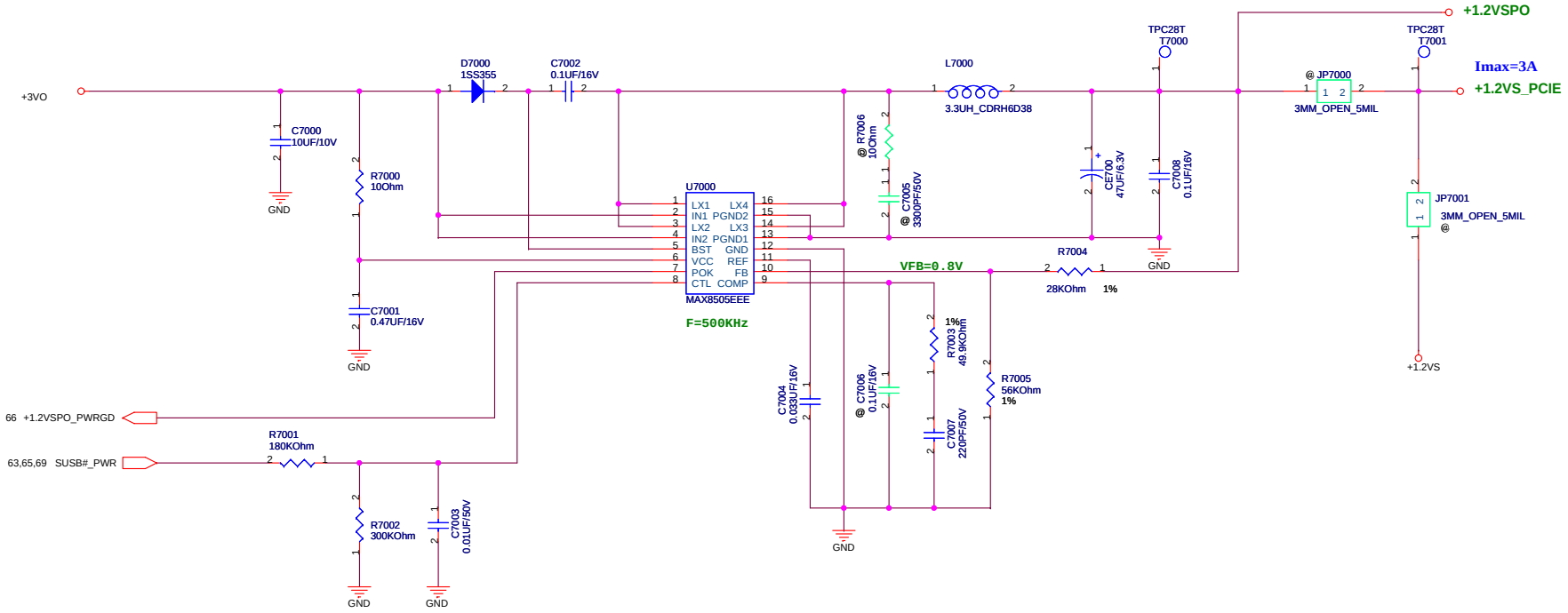




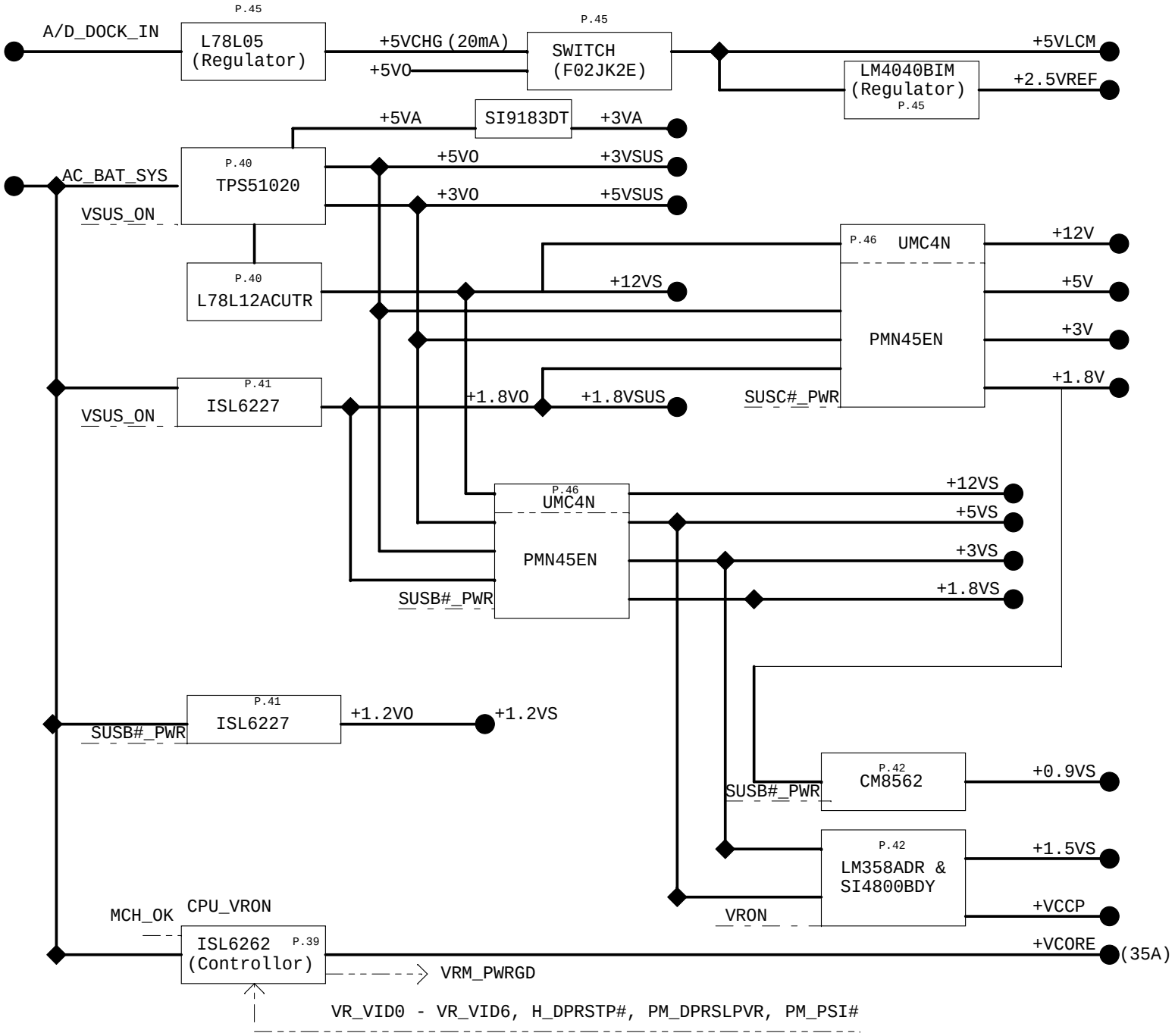
POWER PATH & BAT_LEARN

ASUS	Title :	PROTECTION/SD#	
<OrgName>	Engineer:	Adams Lin	
Size: Custom	Project Name: F5R		Rev: 1.1
Date: Monday, July 31, 2006	Sheet 68 of 71		


+1.2VO
PQ6909
SI4800BDY
PQ6910
SI4800BDY
PT6919 TPC28T
PT6920 TPC28T
PT6921 TPC28T
PT6922 TPC28T
+1.2VS
(4.69A)
VCC_NB
(5A)
PC6915 0.1UF/25V
PC6916 0.1UF/25V
+12VS
PR6914
100KOhm
PC6914 0.1UF/16V
PQ6901 PMN45EN
+1.8VO
PC6904 0.033UF/16V
PT6902 TPC28T
+1.8VS
(1.47A)
PC6901 0.1UF/25V
PR6901 100KOhm
PQ6904
SI4800BDY
+3VO
PC6908 0.015uF/50V
PT6905 TPC28T
+3VS
(5A)
PC6906 0.1UF/25V
PR6903 100KOhm
PQ6906
FDW2501NZ
+5VO
PT6912 TPC28T
+5VS
(3.9A)
PC6900 0.1UF/25V
PC6911 3300PF/50V
PR6905 100KOhm
PT6903 TPC28T
PT6904 TPC28T
(0.08A)
+3V
PC6905 0.1UF/25V
PQ6903 PMN45EN
PT6906 TPC28T
PT6907 TPC28T
+3VO
PC6907 0.015uF/50V
PR6902 100KOhm
PT6908 TPC28T
PT6909 TPC28T
+5VO
PQ6905
FDW2501NZ
PT6910 TPC28T
PT6911 TPC28T
(2.6A)
+5V
PC6909 0.1UF/25V
PC6910 3300PF/50V
PR6904 100KOhm
PT6913 TPC28T
+12VSUS
PQ6907
SUSC#_PWR
UMC4N
PT6914 TPC28T
+12V
PR6906 100KOhm
PQ6905,PQ6906 P/N:07G005161020
PQ6908
SUSB#_PWR
UMC4N
PT6915 TPC28T
+12VS
PR6907 100KOhm
+3VA
PR6915 1KOhm r0402_h16 1%
PJP6902
1MM_OPEN_5MIL
@
CPU_VRON 24,62,65
PR6916 1KOhm r0402_h16 1%
PJP6903
1MM_OPEN_5MIL
@
VSUS_ON 24,29,63,64
37 SUSB_PWR
37 SUSC_PWR
PR6910 100KOhm
PR6911 100KOhm
PQ6900A UM6K1N
PQ6900B UM6K1N
SUSB#_PWR
SUSC#_PWR
AC_BAT_SYS
PC6912 0.1UF/25V
PU6900
IN
OUT
GND
EN NC or ADJ
MIC5235YM5
FB=1.24V
PR6912 845KOhm 1%
PR6913 95.3KOhm 1%
PC6913 1UF/25V
TPC28T PT5112
+12VSUS
Imax=100mA
24,29,63,64 VSUS_ON
PT6916 TPC28T
PR6908 1KOhm r0402_h16 1%
10,24,29,66 SUSB#
PT6900 TPC28T
63,65,70 SUSB#_PWR
+3VA
PJP6901
1MM_OPEN_5MIL
@
PT6917 TPC28T
PR6909 1KOhm r0402_h16 1%
24 SUSC#
PT6918 TPC28T
63,64 SUSC#_PWR
+3VA
PJP6900
1MM_OPEN_5MIL
@
Title : LOAD SWITCH
<OrgName>
Engineer: Adams Lin
Size Custom
Project Name F5R
Rev 1.1
Date: Monday, July 31, 2006
Sheet 69 of 71



ASUS	Title : POWER_1.2VS_PCIE	
<OrgName>	Engineer:	
Size: Custom	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 70 of 71	



ASUS	Title : POWER BLOCK DIAGRAM	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: F5R	Rev: 1.1
Date: Monday, July 31, 2006	Sheet 71 of 71	