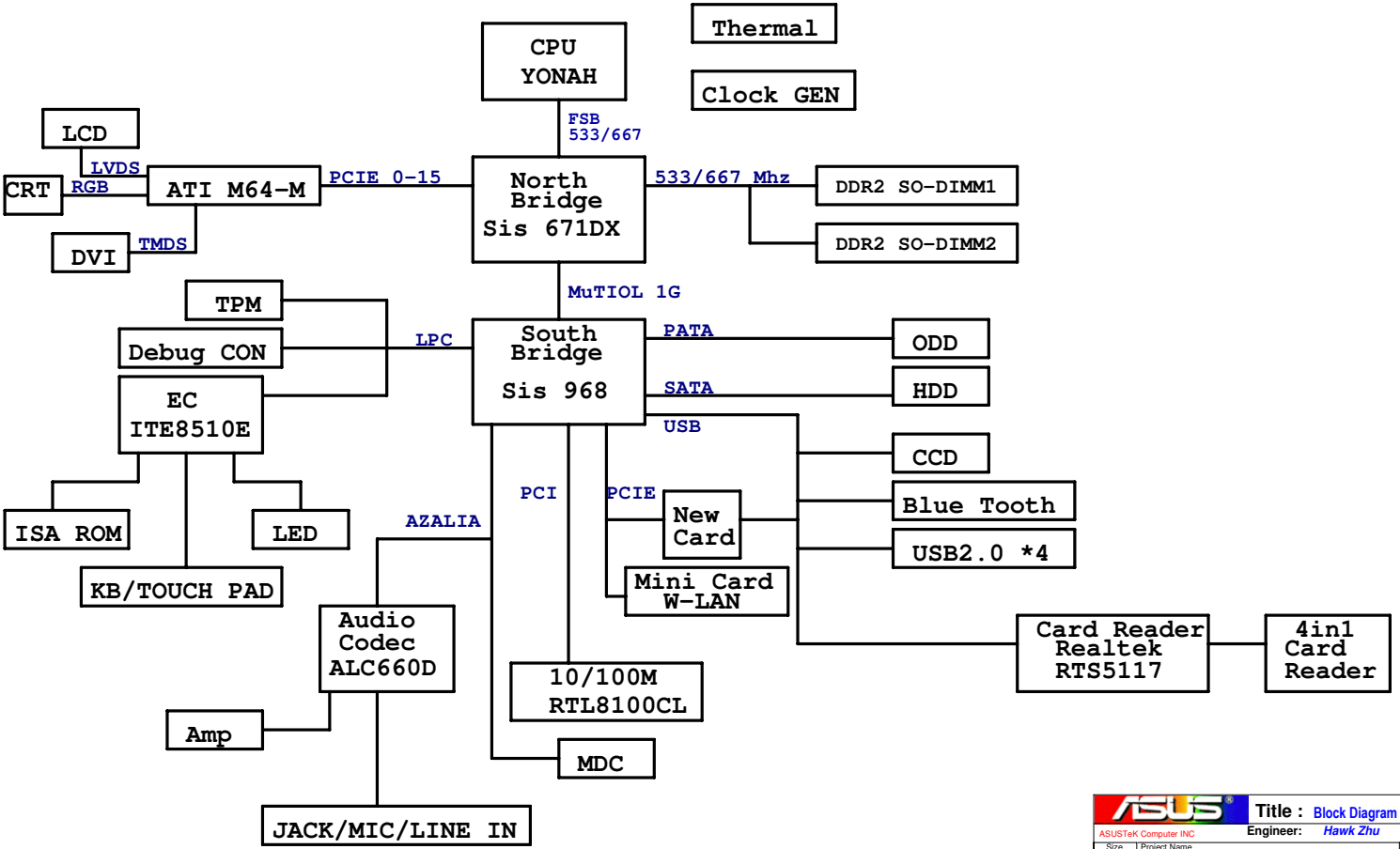


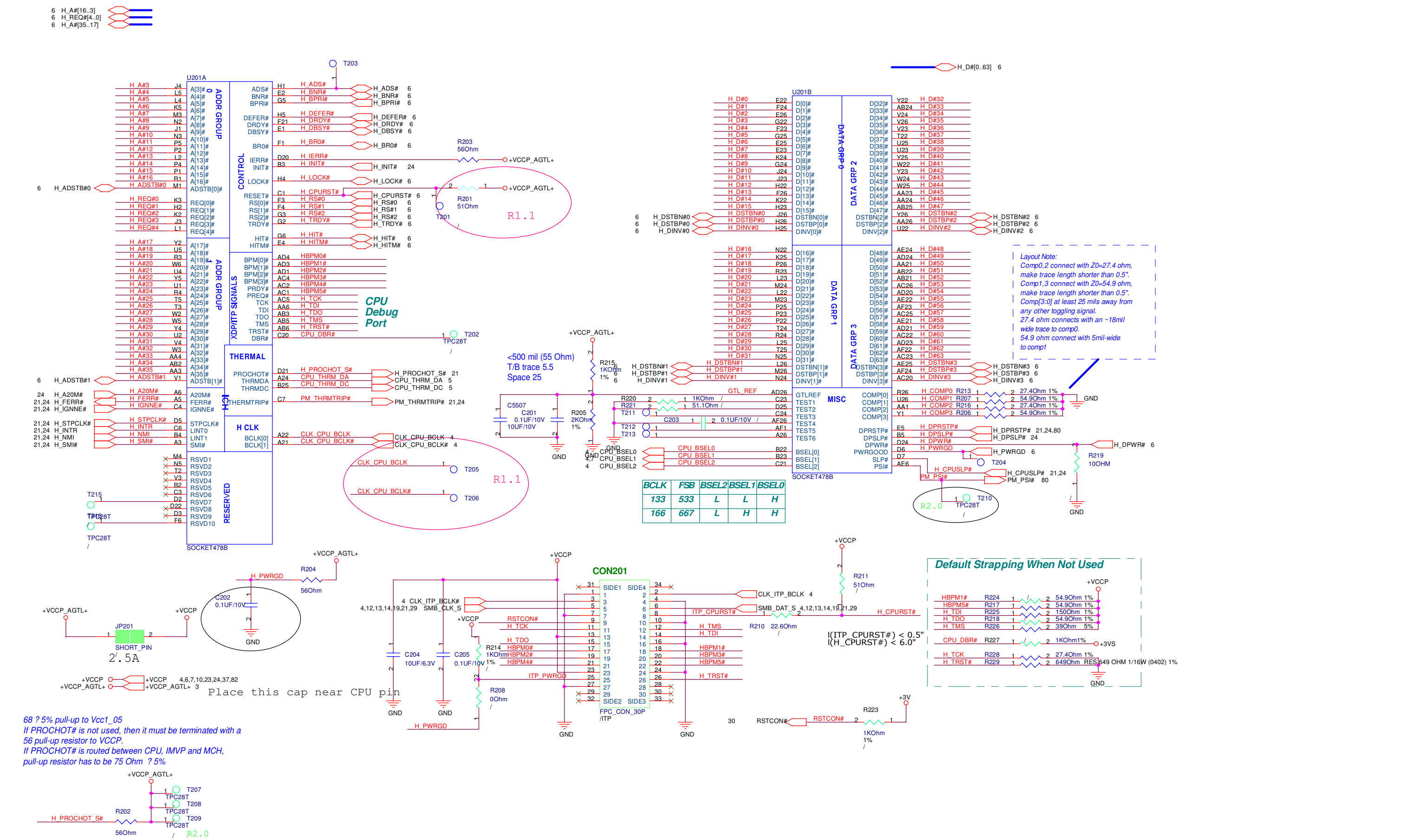
ASUSTeK Computer INC

Title : Block Diagram

Engineer: Hawk Zhu

Size	Project Name	Rev
B	F5V	1.0

Date: 星期 一, 四月 23, 2007 Sheet 1 of 94



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

68 ? 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ? 5%

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer: Hawk Zhu

Size: C

Project Name: F5V

Rev: 1.0

Date: 星期一, 四月 23, 2007

Sheet 2 of 94

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

U201C

SOCKET478B

12G04600479A

U201D

SOCKET478B

12G04600479A

R2.0

T301 T302 T303

JP301 SHORT_PIN

CE302 220UF/4V

Place these caps on North of Secondary side

C322 C309 C321 C310 C334 C318 C317 C324 22UF/6.3V 0805

Place these caps on North of Primary side

C320 C302 C303 C326 C301 22UF/6.3V 0805

Place these caps on South of Primary side

C308 C325 C316 C329 C314 22UF/6.3V 0805

Place these caps on South of Secondary side

C304 C305 C332 C331 C312 C323 C333 C313 22UF/6.3V 0805

+1.05V Decoupling Capacitor
Place near CPU

C311 C330 C328 C307 C327 C319 CE301 c0402 0.1UF/10V 470UF/2.5V c7343d_h75

120mA / 20mil
Close to Pin B26

C306 10UF/10V C315 0.01UF/16V

checklist suggests
10uF POSCAP

RN301B 0Ohm

RN302C RN302B RN302D RN302A RN301C RN301D 0Ohm

R302 100Ohm

R301 100Ohm

VR_VID0 VR_VID1 VR_VID2 VR_VID3 VR_VID4 VR_VID5 VR_VID6 VCCSENSE VSSSENSE

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

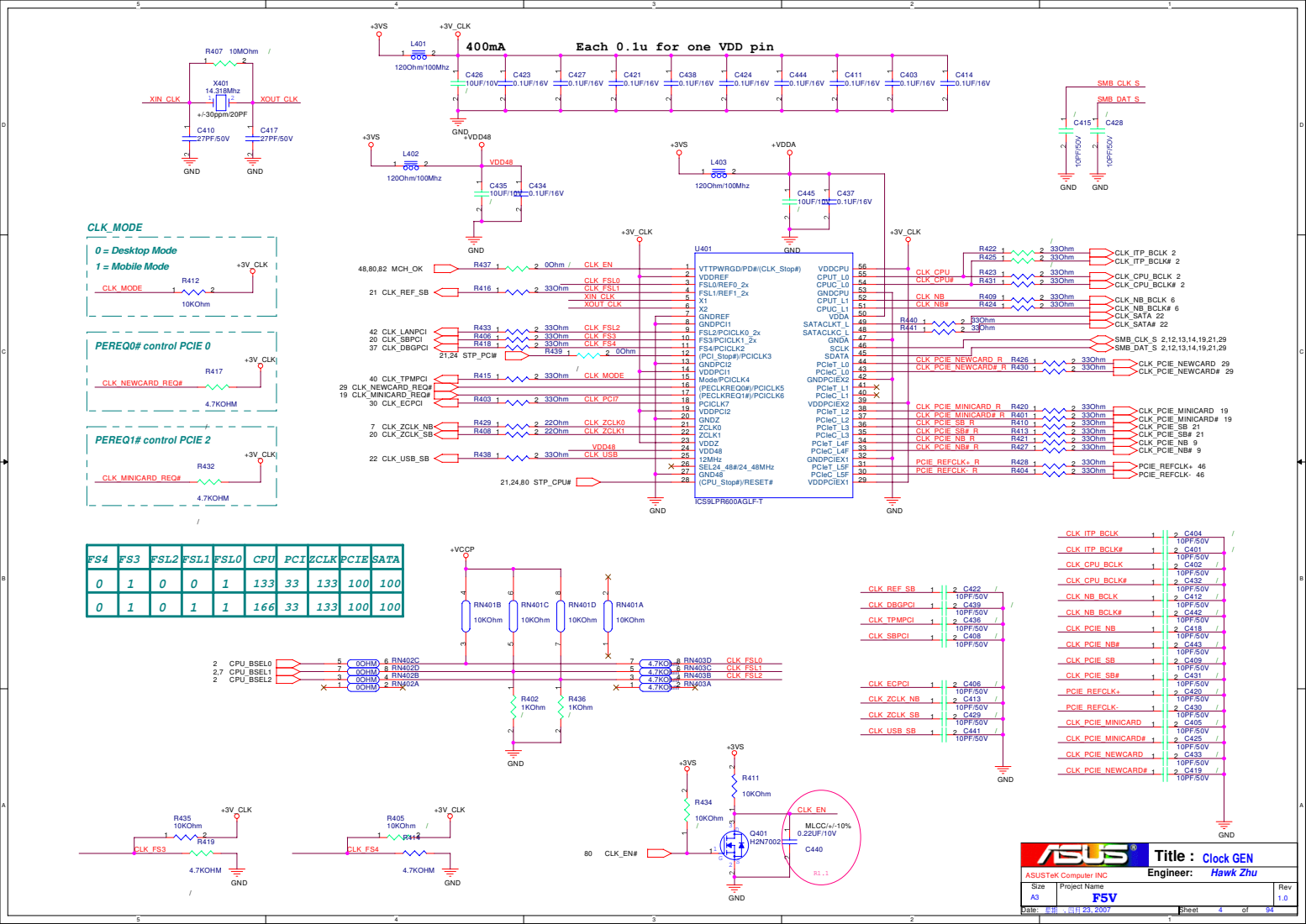
ASUSTeK COMPUTER INC

Title : Yonah CPU (2)

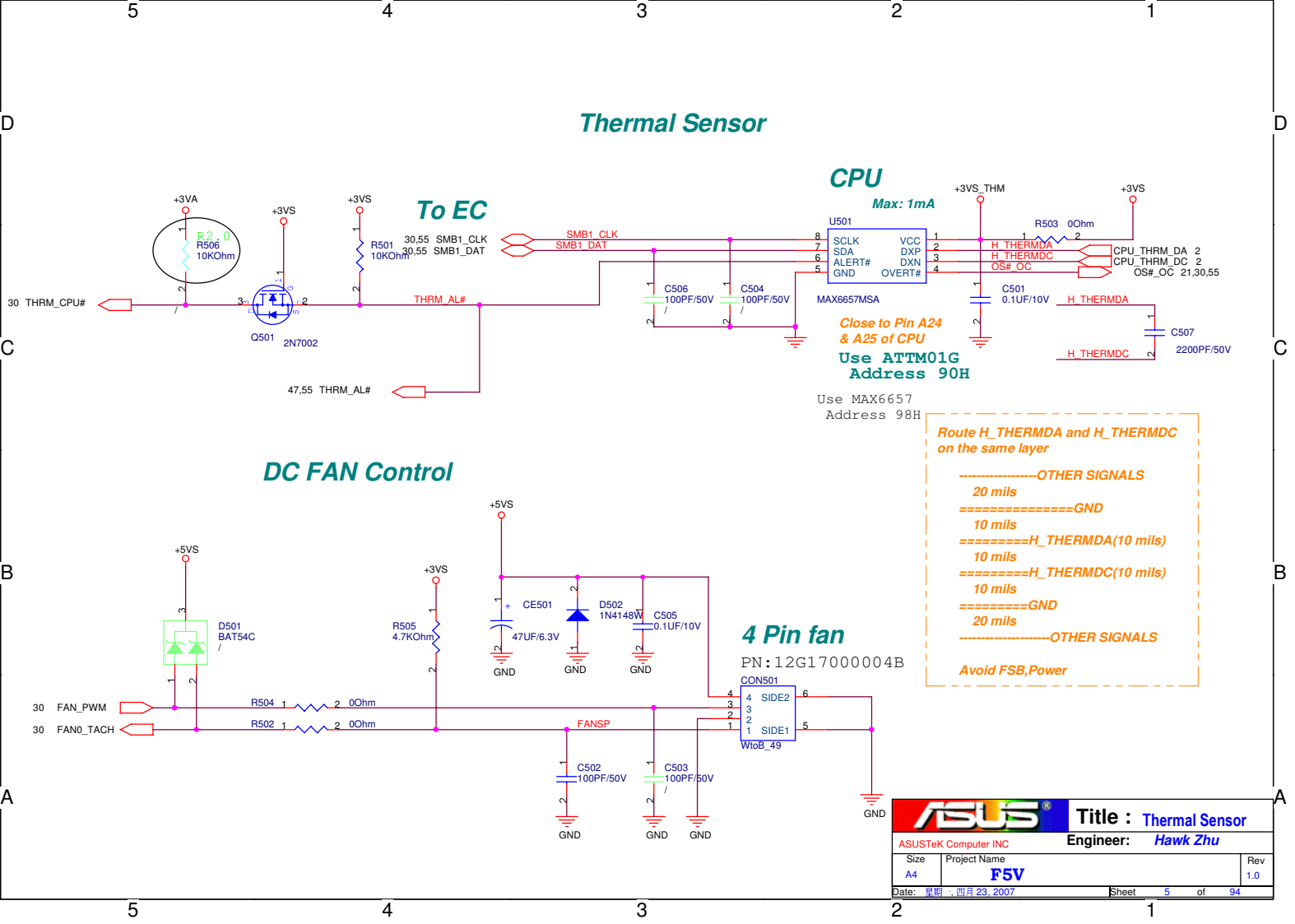
Engineer: Hawk Zhu

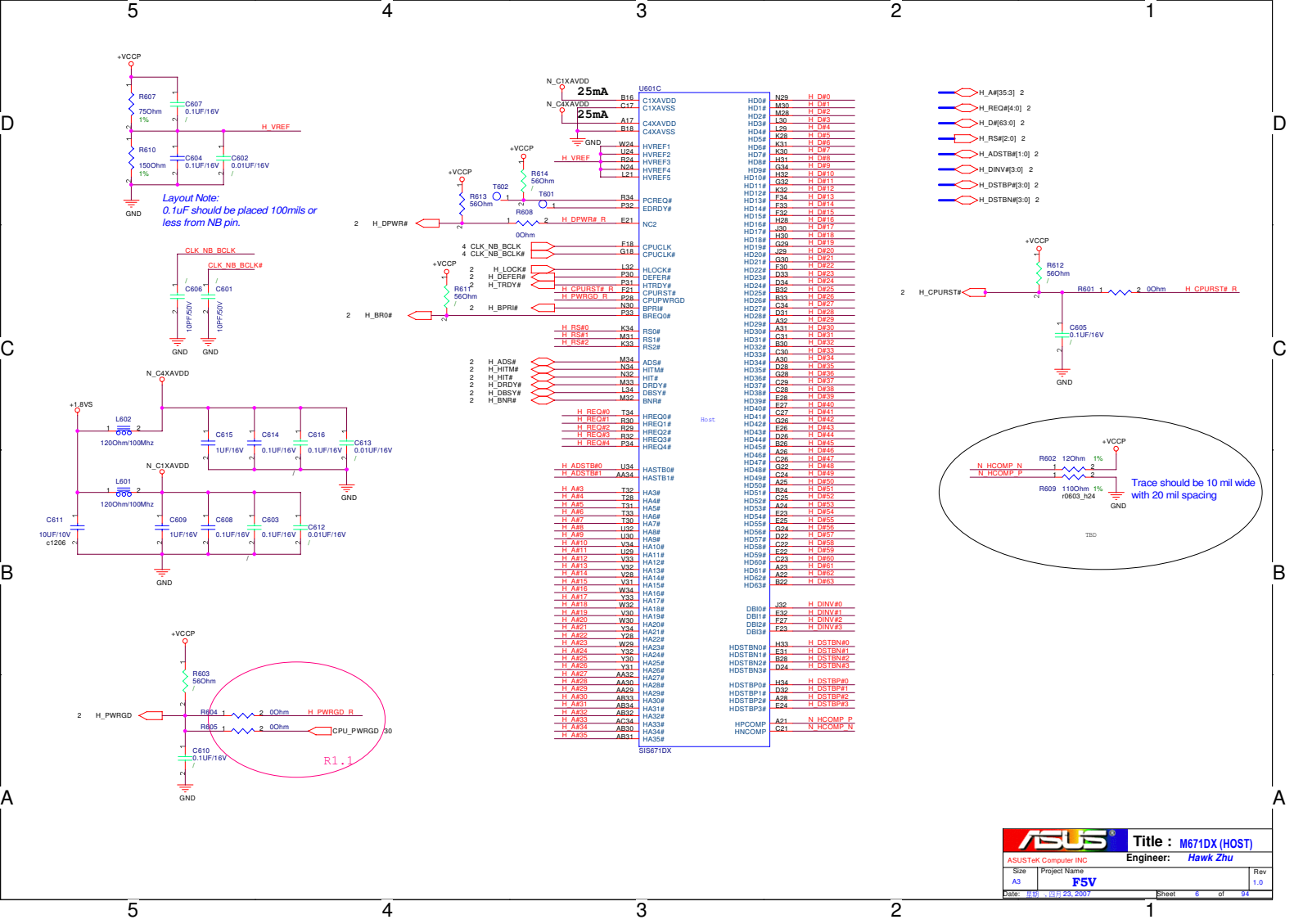
Size	Project Name	Rev
A3	F5V	1.0

Date: 星期 一, 四月 23, 2007 Sheet 3 of 94

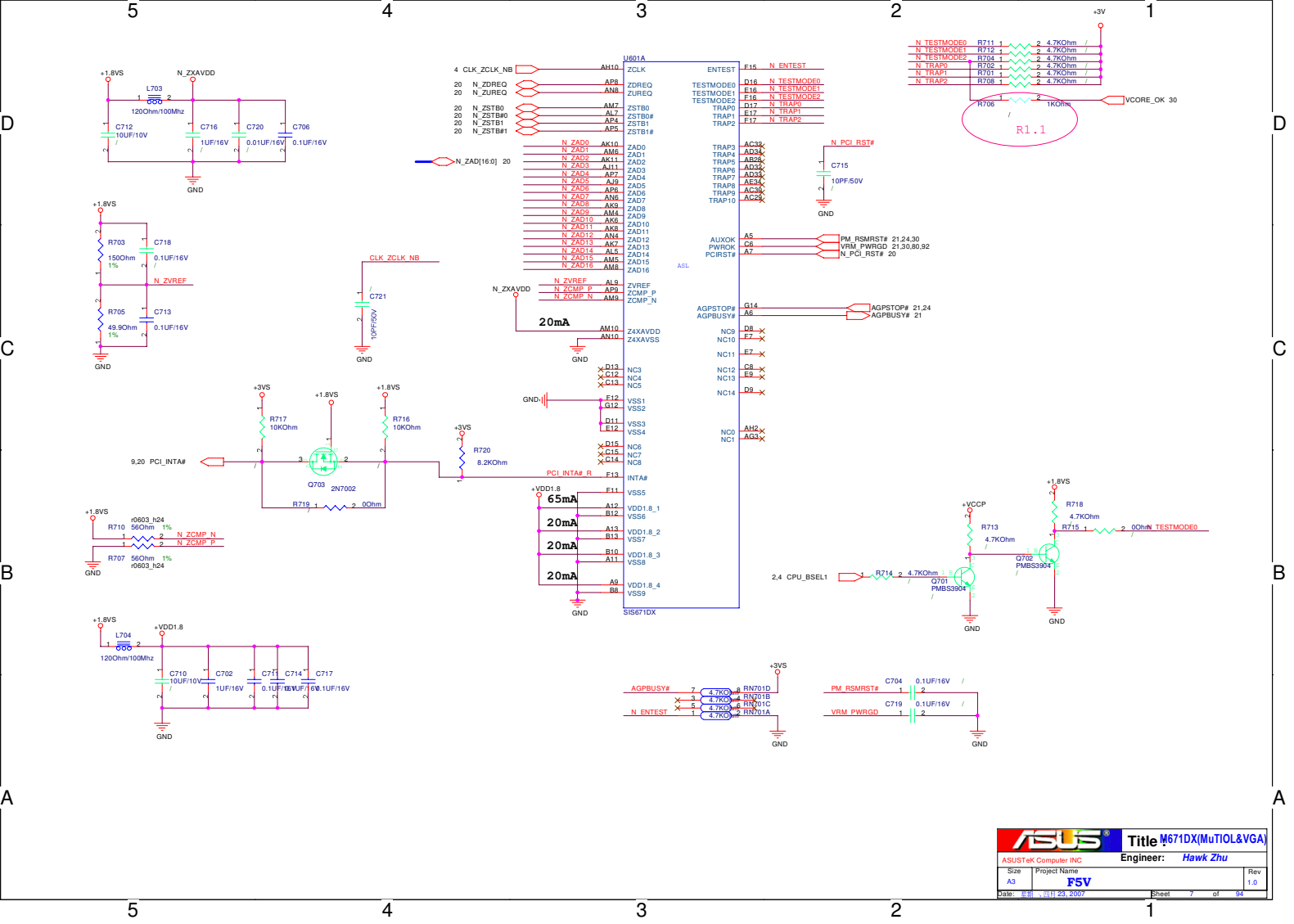


FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100

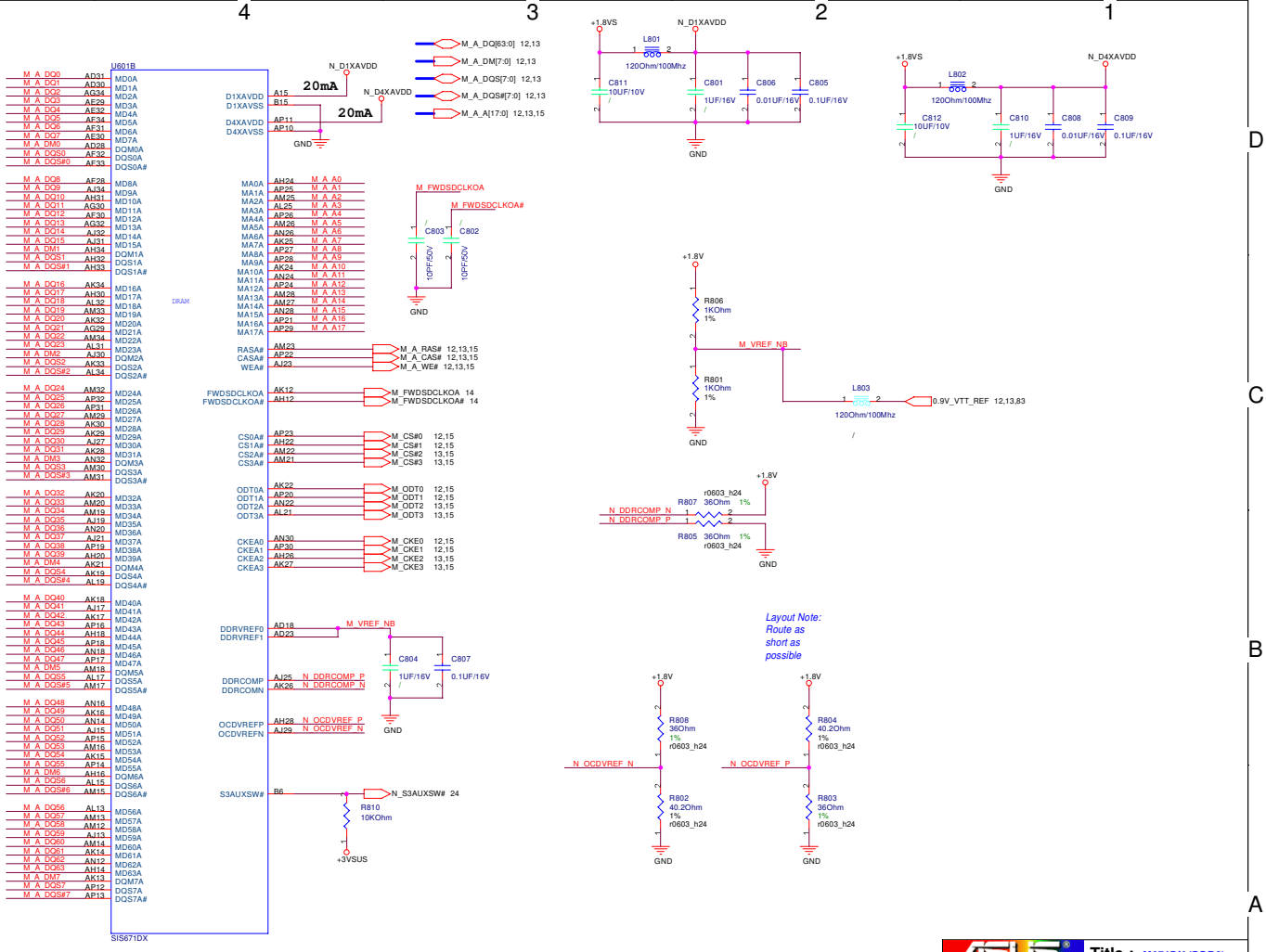

Thermal Sensor
To EC
CPU
Max: 1mA
+3VA
+3VS
+3VS_THM
R506 10KOhm
R501 10KOhm
30,55 SMB1_CLK
30,55 SMB1_DAT
SMB1_CLK
SMB1_DAT
30 THRM_CPU#
THRM_AL#
Q501 2N7002
47,55 THRM_AL#
U501
SCLK
SDA
ALERT#
GND
VCC
DXP
DXN
OVERT#
MAX6657MSA
R503 0Ohm
H_THERMDA
H_THERMDC
OS#_OC
CPU_THRM_DA 2
CPU_THRM_DC 2
OS#_OC 21,30,55
C506 100PF/50V
C504 100PF/50V
C501 0.1UF/10V
C507 2200PF/50V
Close to Pin A24
& A25 of CPU
Use ATTM01G
Address 90H
Use MAX6657
Address 98H
Route H_THERMDA and H_THERMDC
on the same layer
----------OTHER SIGNALS
20 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
20 mils
----------OTHER SIGNALS
Avoid FSB,Power
DC FAN Control
+5VS
+3VS
D501 BAT54C
R505 4.7KOhm
CE501 47UF/6.3V
D502 1N4148W
C505 0.1UF/10V
4 Pin fan
PN:12G17000004B
CON501
SIDE2
SIDE1
WtoB_49
30 FAN_PWM
30 FAN0_TACH
R504 0Ohm
R502 0Ohm
FANSP
C502 100PF/50V
C503 100PF/50V
GND
Title : Thermal Sensor
ASUSTeK Computer INC
Engineer: Hawk Zhu
Size A4
Project Name F5V
Rev 1.0
Date: 星期 , 四月 23, 2007
Sheet 5 of 94



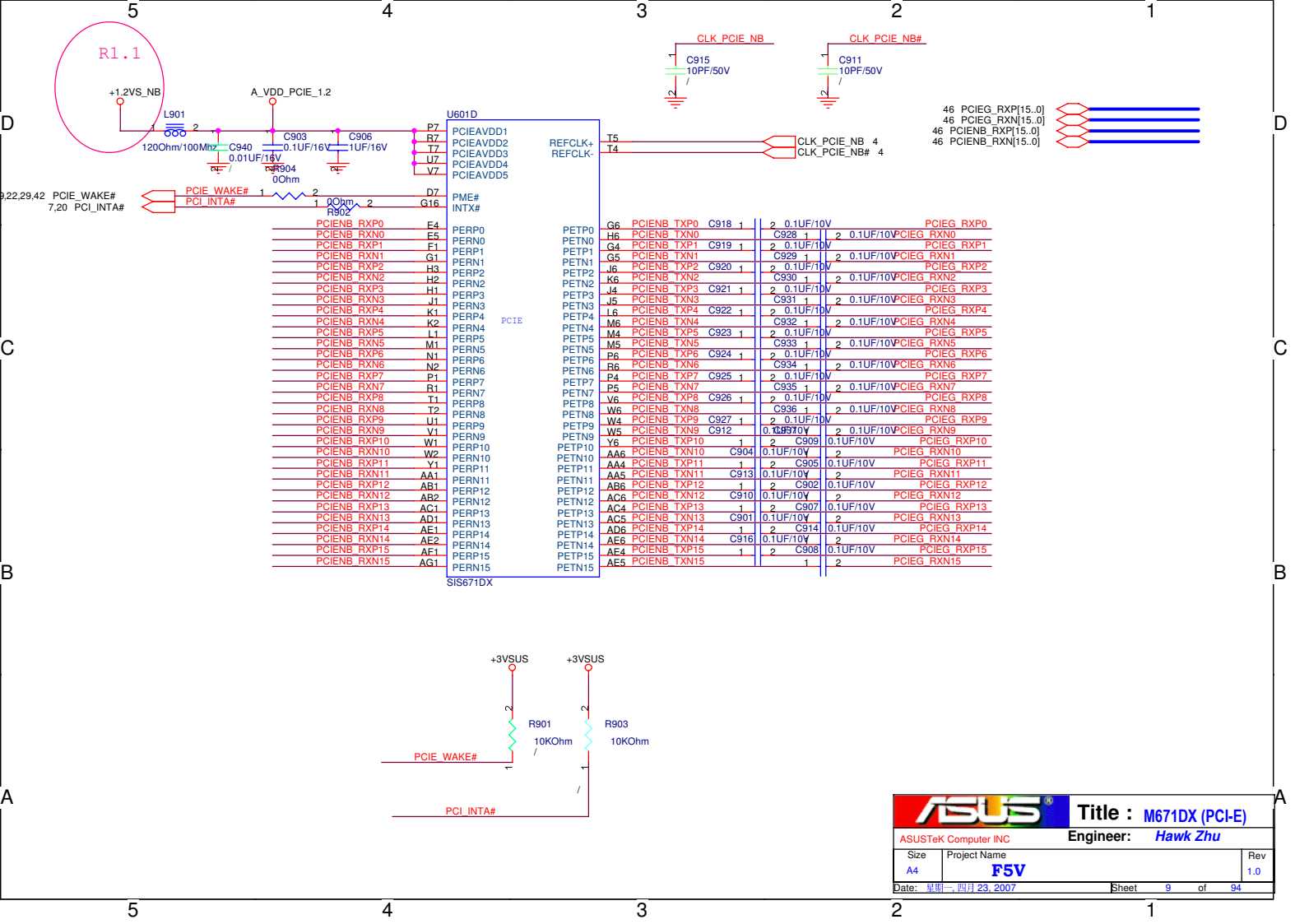
Title :	M671DX (HOST)
ASUSTeK Computer INC	Engineer: Hawk Zhu
Size: A3	Project Name: F5V
Rev: 1.0	
Date: 星期 , 四月 23, 2007	Sheet 6 of 94



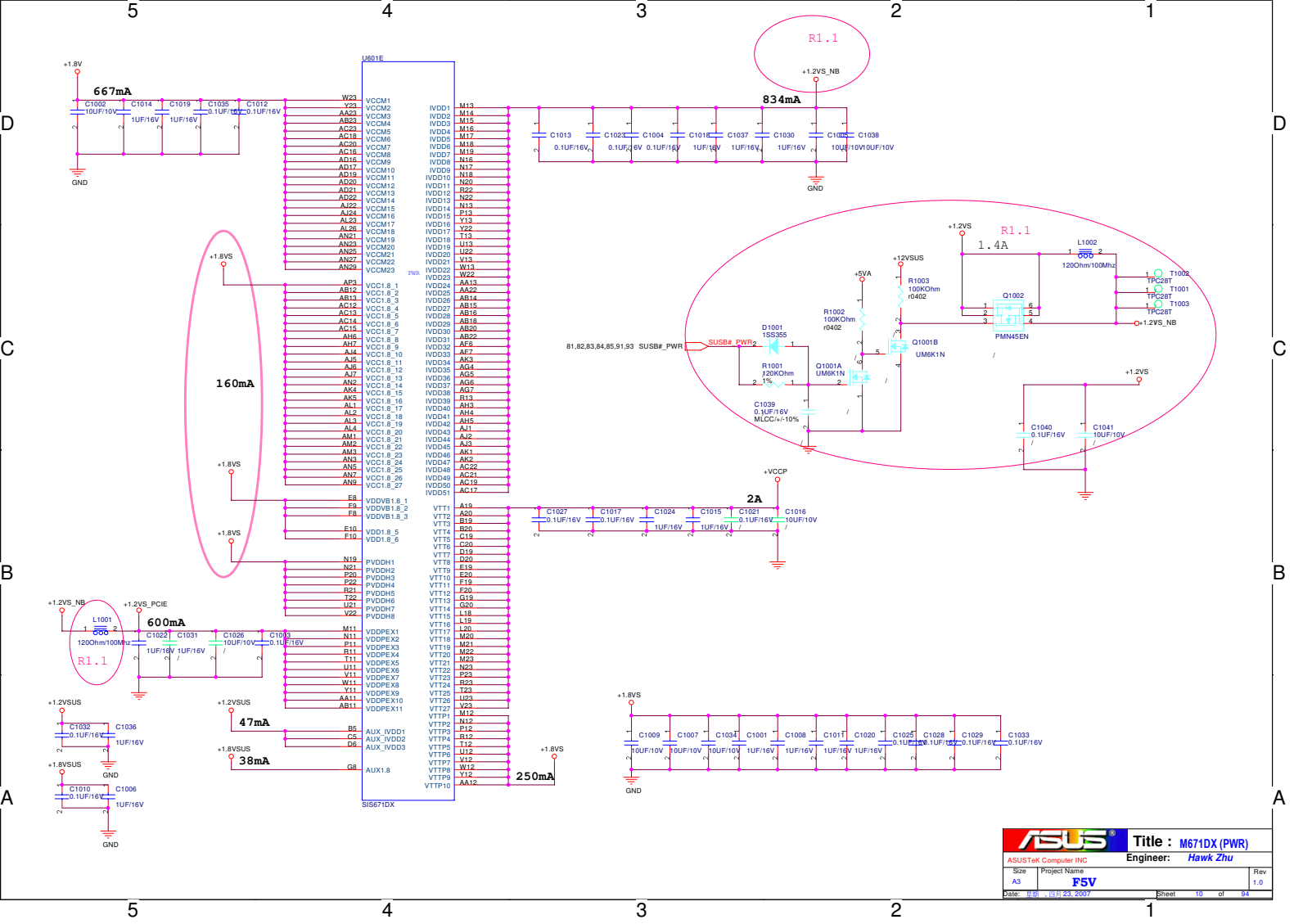
ASUSTeK Computer INC	Title: M671DX(MuTIOL&VGA)	
	Engineer: Hawk Zhu	
Size: A3	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 7 of 94	

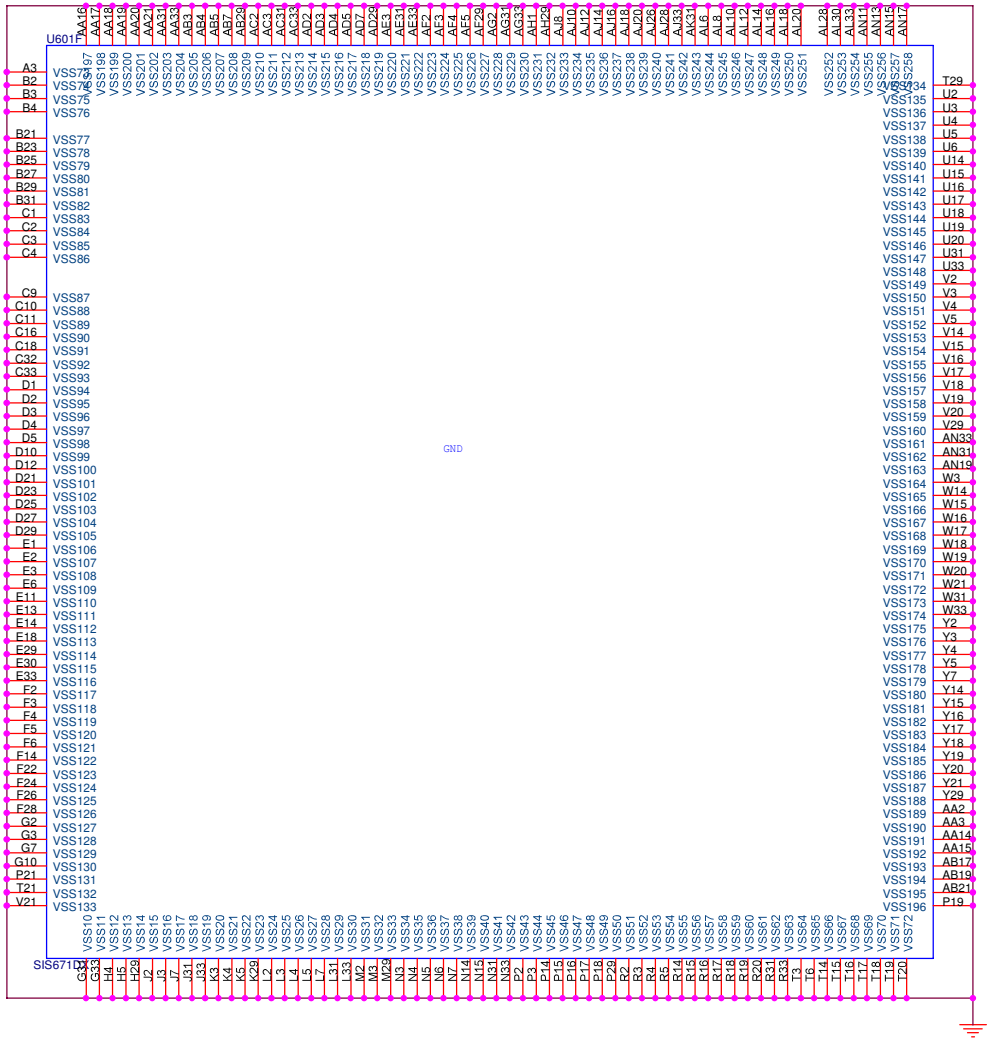


Title :	M671DX (DDR2)
ASUSTeK Computer INC	Engineer: Hawk Zhu
Size: A3	Project Name: F5V
Rev: 1.0	
Date: 星期 一, 四月 23, 2007	Sheet 8 of 94



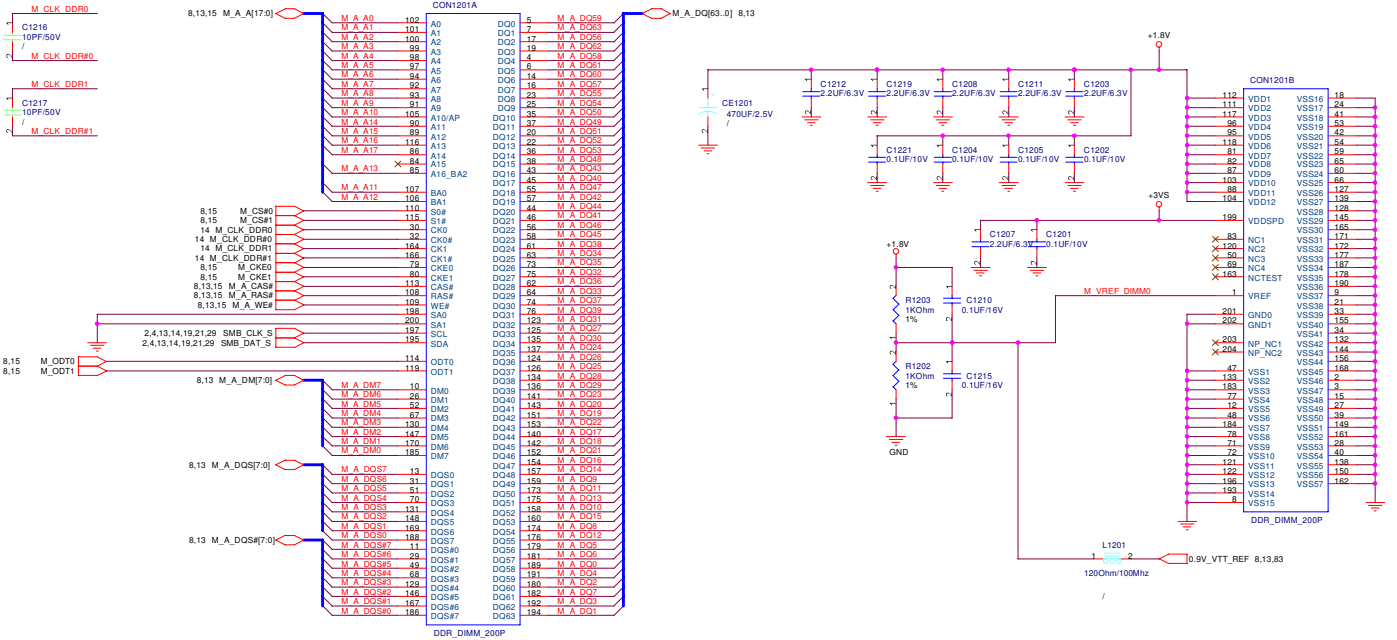
Title :	M671DX (PCI-E)
ASUSTeK Computer INC	Engineer: Hawk Zhu
Size: A4	Project Name: F5V
Rev: 1.0	
Date: 星期一, 四月 23, 2007	Sheet 9 of 94


U601E
SIS671DX
667mA
160mA
600mA
47mA
38mA
834mA
2A
250mA
1.4A
R1.1
+1.8V
+1.2VS_NB
+1.2VS_PCIE
+1.2VS
+1.8VS
+1.2VSUS
+1.8VSUS
+5VA
+12VSUS
+VCCP
GND
SUSB#_PWR
81,82,83,84,85,91,93 SUSB#_PWR
PMN45EN
UM6K1N
120Ohm/100Mhz
Title : M671DX (PWR)
ASUSTeK Computer INC
Engineer: Hawk Zhu
Project Name
F5V
Rev 1.0
Sheet 10 of 94



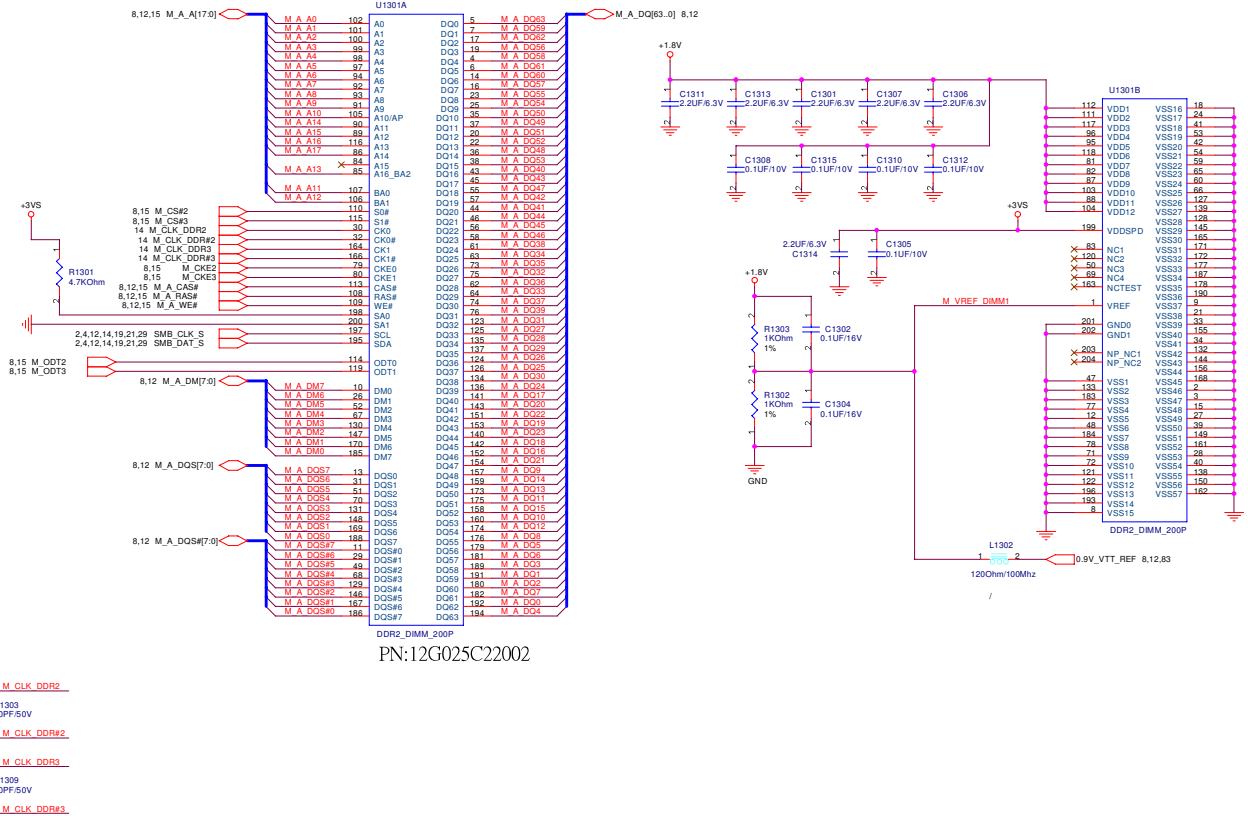
ASUSTeK Computer INC	Title : M671DX (GND)		
	Engineer: Hawk Zhu		
Size: A4	Project Name: F5V		Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 11 of 94		

TOP



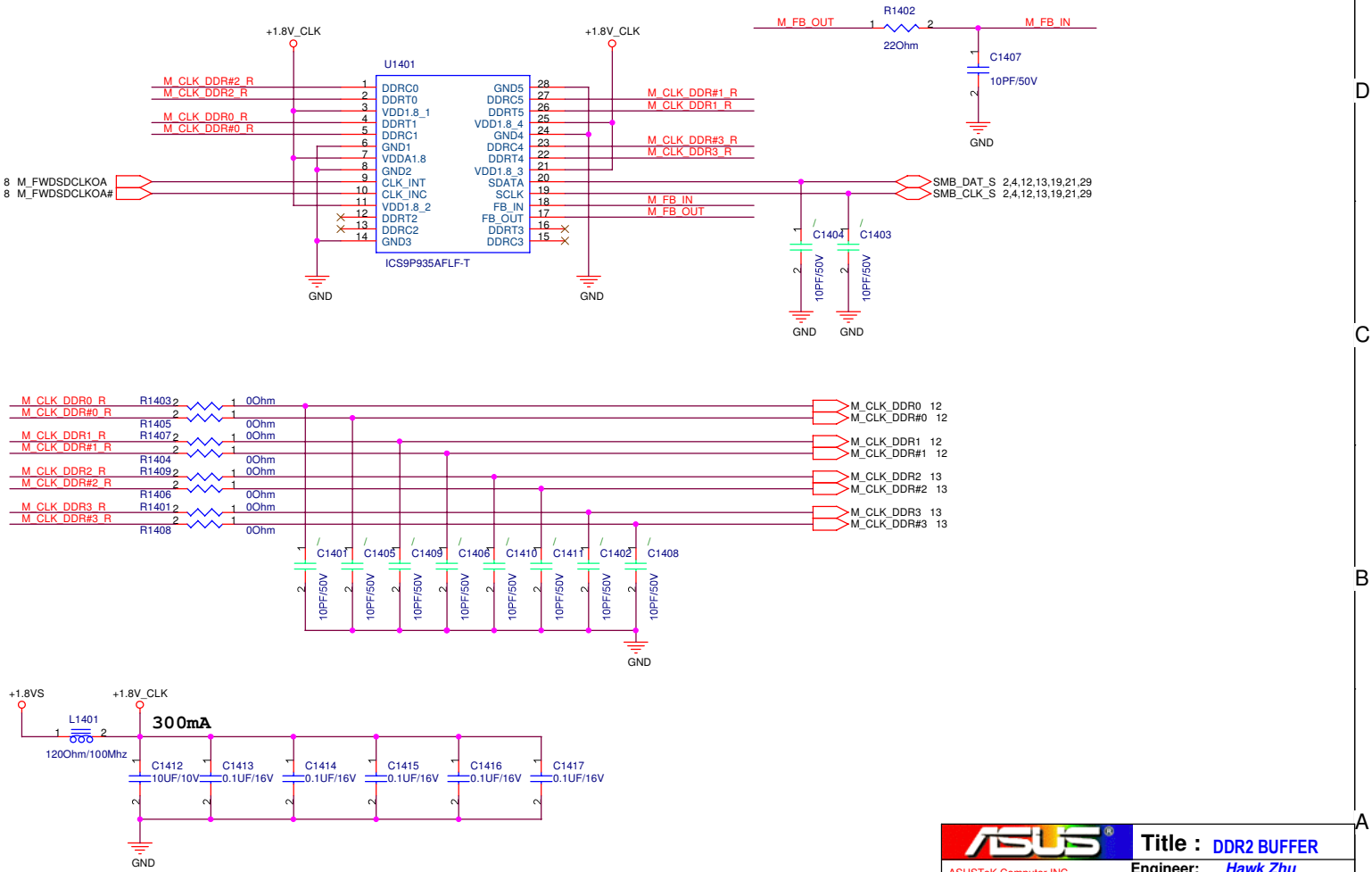
PN:12G025122006

ASUSTeK Computer INC	Title : DDR2 SO-DIMM1		
	Engineer: Hawk Zhu		
Size: A3	Project Name: F5V		Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 12 of 94		

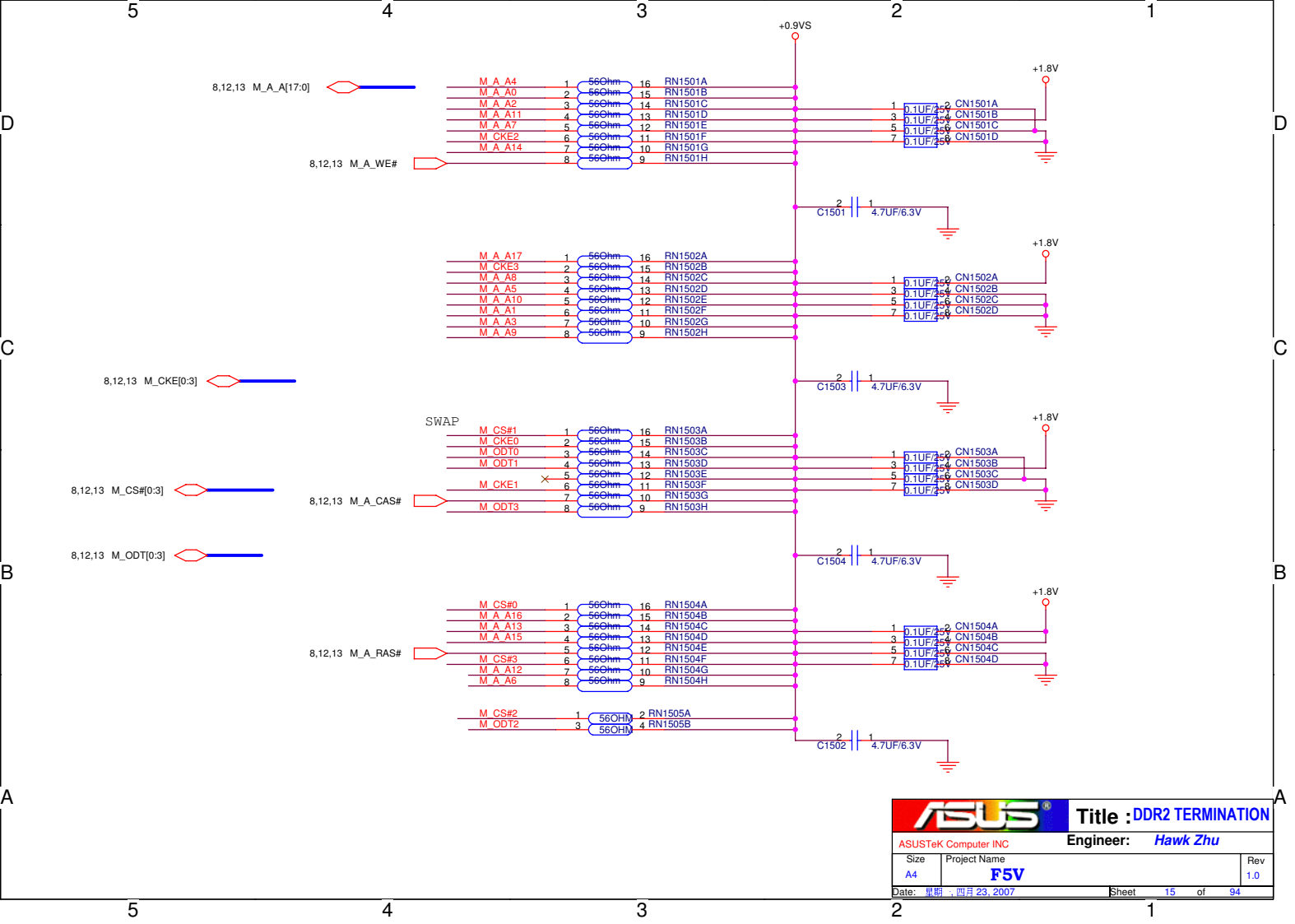


PN:12G025C22002

ASUSTeK Computer INC	Title : DDR2 SO-DIMM2		
	Engineer: Hawk Zhu		
Size: A3	Project Name: F5V		Rev: 1.0
Date: 星期 一, 四月 23, 2007	Sheet 13 of 94		



ASUSTeK Computer INC	Title : DDR2 BUFFER	
	Engineer: Hawk Zhu	
Size: A4	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 14 of 94	



ASUSTeK Computer INC	Title : DDR2 TERMINATION		
	Engineer: Hawk Zhu		
Size: A4	Project Name: F5V		Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 15 of 94		

Title : SIS

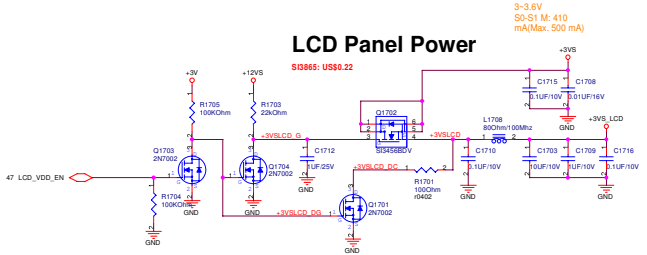
ASUSTeK Computer INC

Engineer: Hawk Zhu

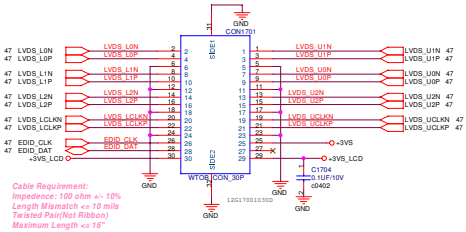
Size	Project Name	Rev
C	F5V	1.0

Date: 星期一, 五月 23, 2007 Sheet 16 of 94

LCD Panel Power

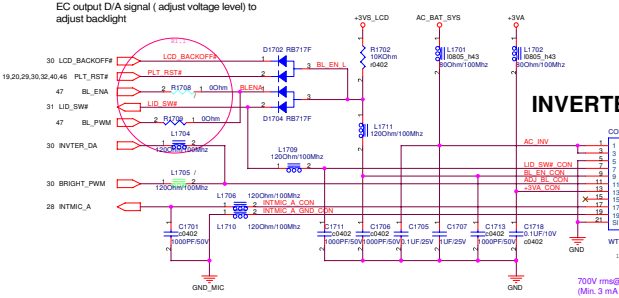


LCD LVDS Interface

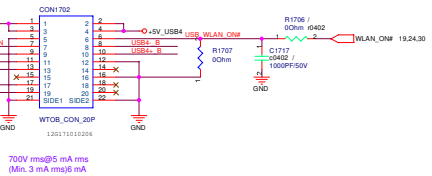


LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn
On/Off backlight
EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

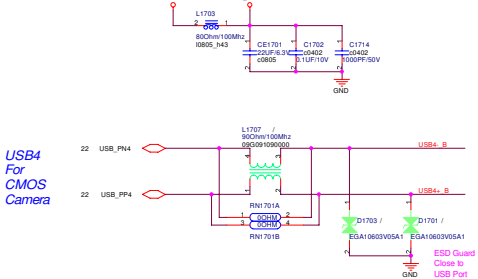


INVERTER Interface

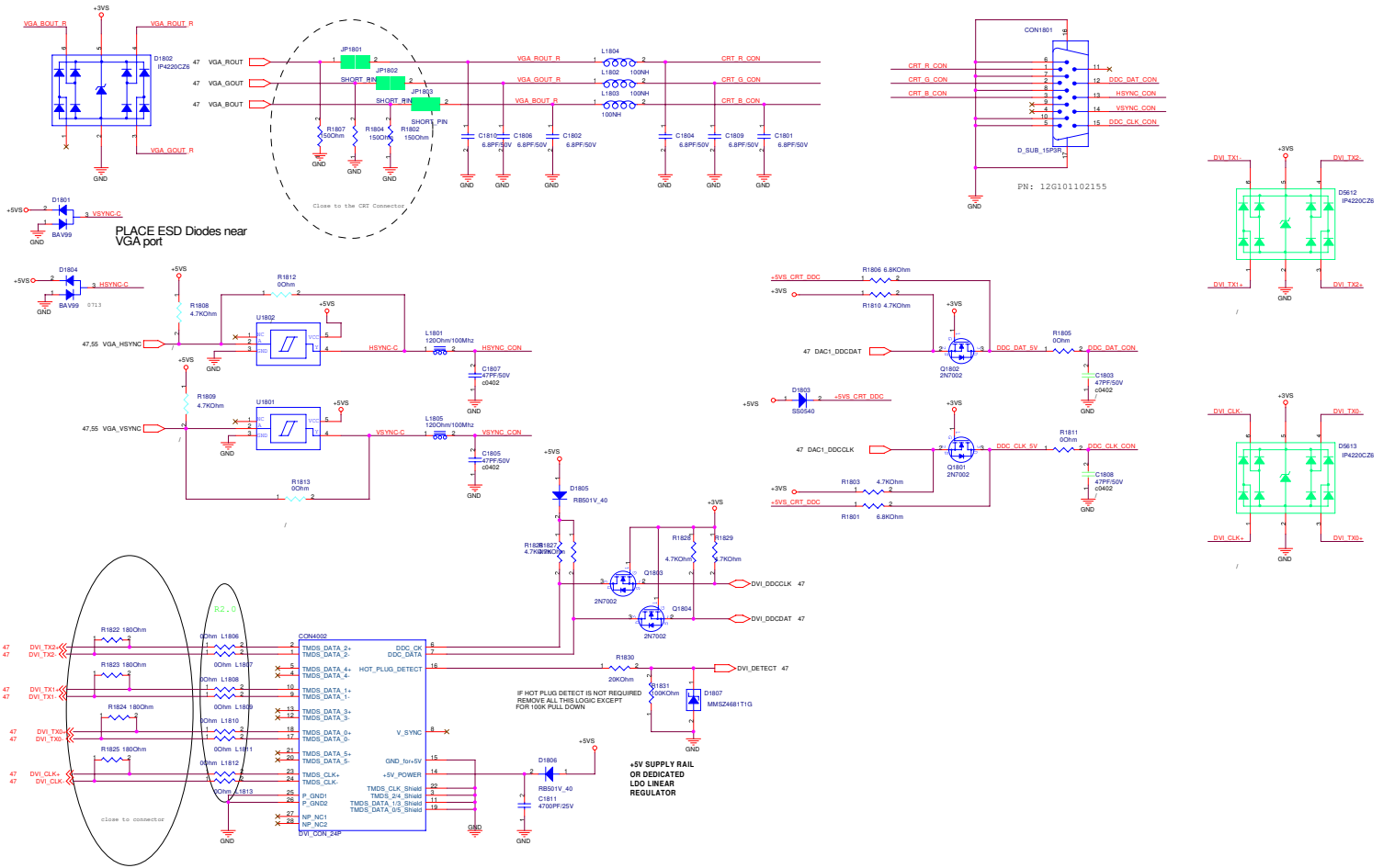


700V rms@5 mA rms
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

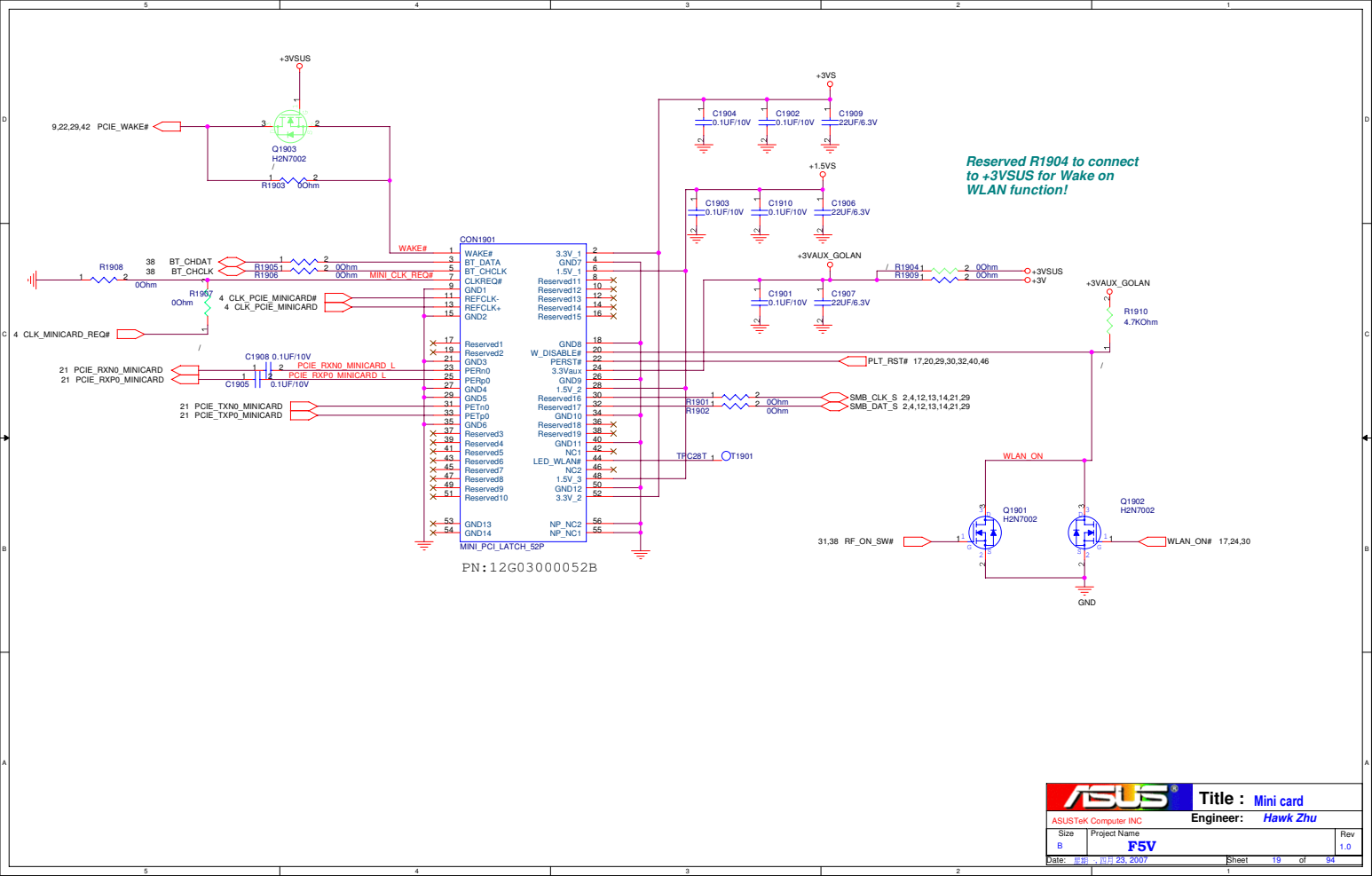
USB4 For CMOS Camera



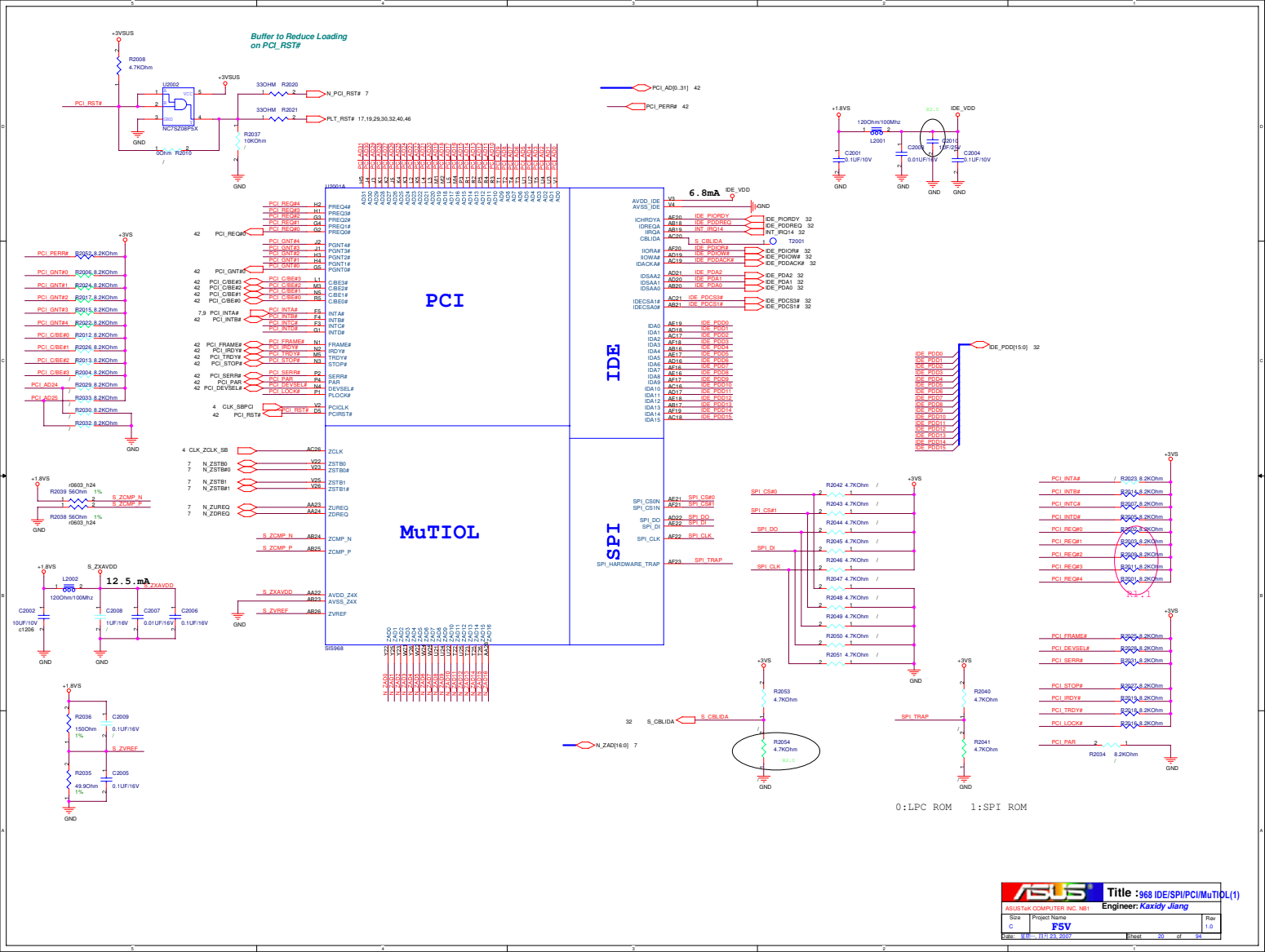
ASUSTeK Computer INC	Title : LVDS		
	Engineer: Hawk Zhu		
Size: C	Project Name: F5V		Rev: 1.0
Date: 星期二, 五月 23, 2007	Sheet 17 of 94		

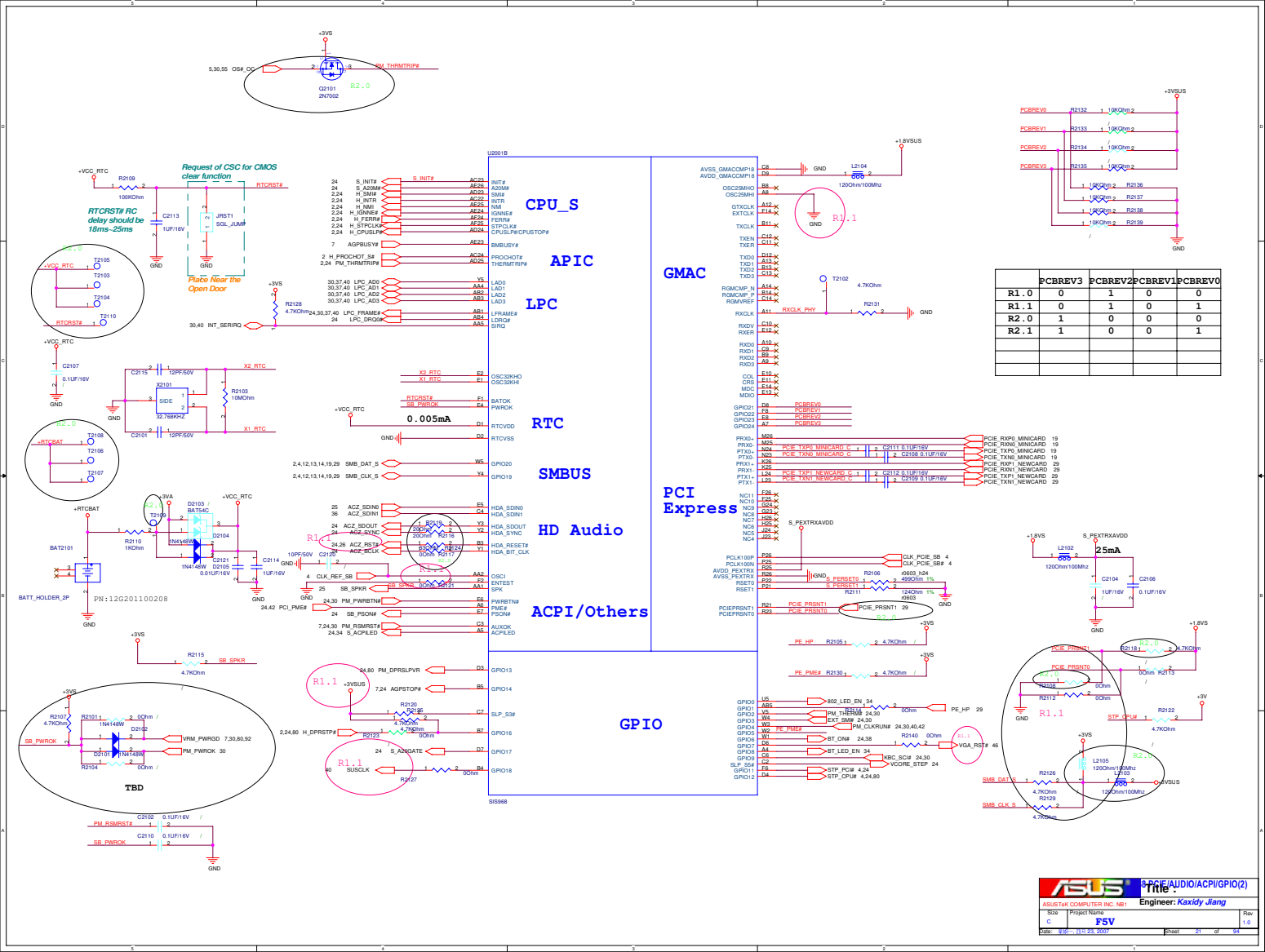


ASUSTeK Computer INC	Title : CRT&DVI		
	Engineer: Hawk Zhu		
Size: C	Project Name: F5V		Rev: 1.0
Date: 星期一, 五月 23, 2007	Sheet 18 of 94		

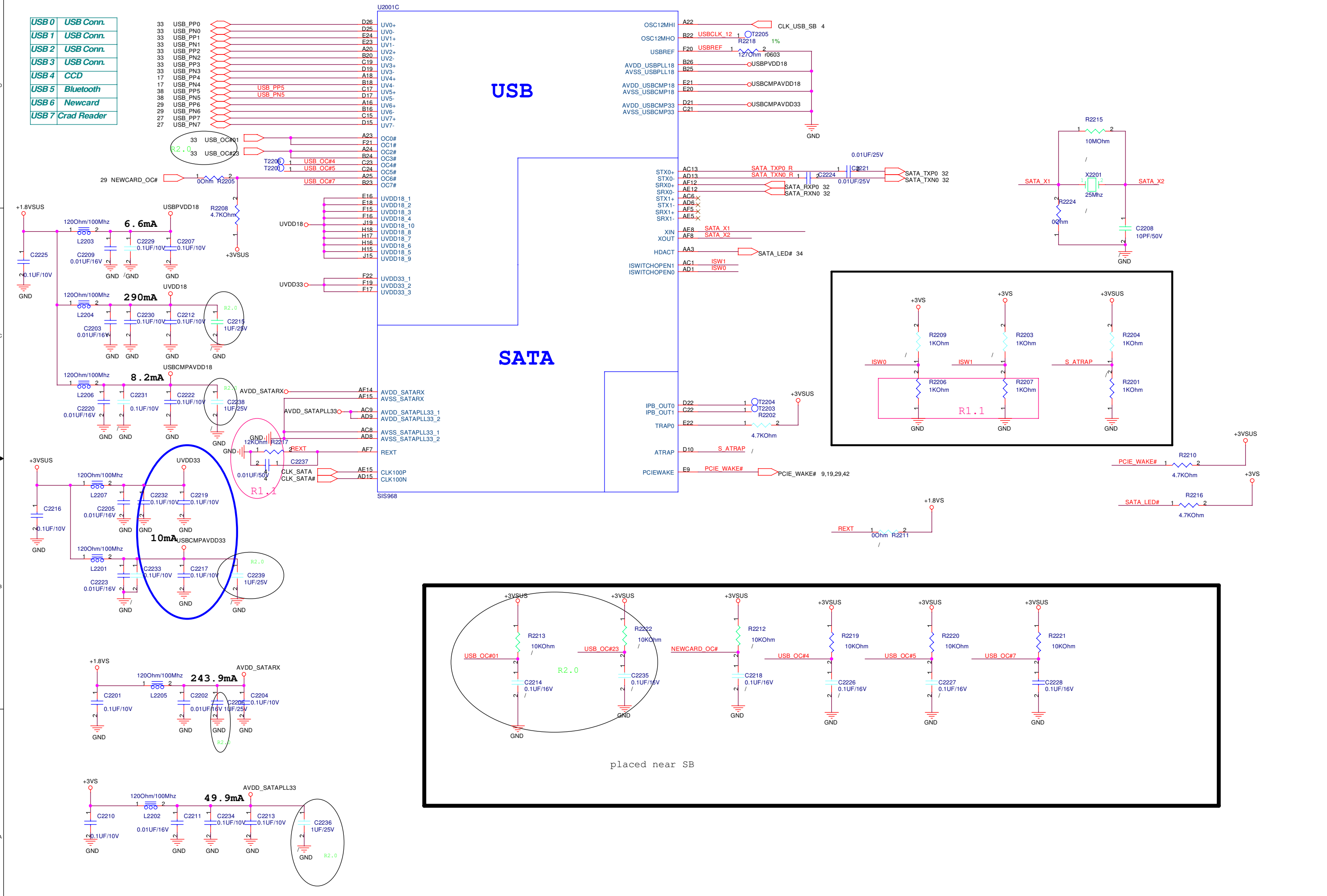


ASUSTeK Computer INC	Title : Mini card	
	Engineer: Hawk Zhu	
Size: B	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 19 of 94	


Buffer to Reduce Loading on PCI_RST#
PCI
IDE
SPI
MuTIOL
SIS968
6.8mA
12.5mA
0:LPC ROM 1:SPI ROM
Title :968 IDE/SPI/PCI/MuTIOL(1)
ASUSTeK COMPUTER INC. NB1
Engineer: Kaxidy Jiang
Project Name
FSV
Rev
1.0
Sheet 20 of 84



	PCBREV3	PCBREV2	PCBREV1	PCBREV0
R1.0	0	1	0	0
R1.1	0	1	0	1
R2.0	1	0	0	0
R2.1	1	0	0	1



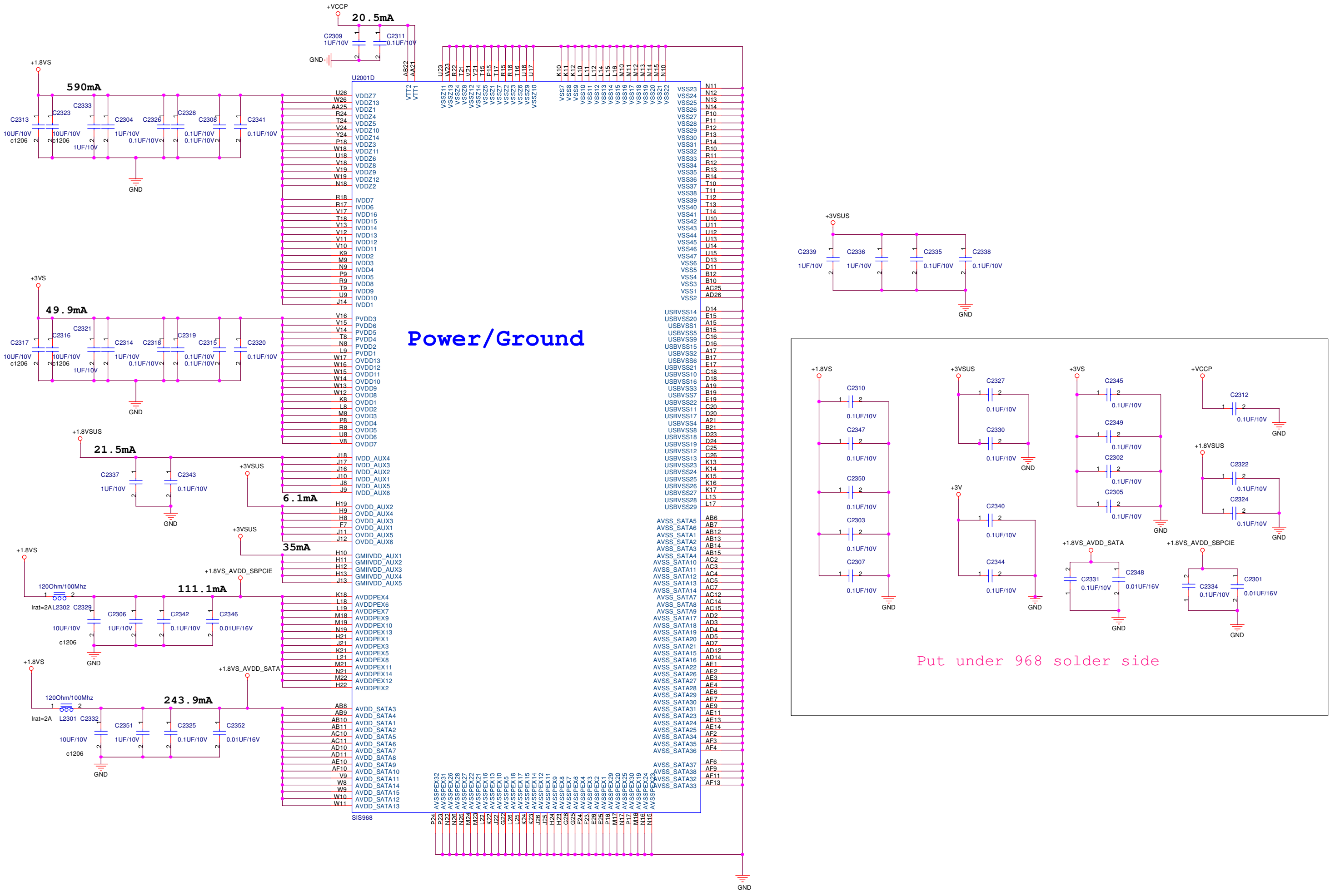
Title : 968 USB/SATA(3)

Engineer: Kaxidy Jiang

ASUSTeK COMPUTER INC. NB1

Size	Project Name	Rev
C	F5V	1.0

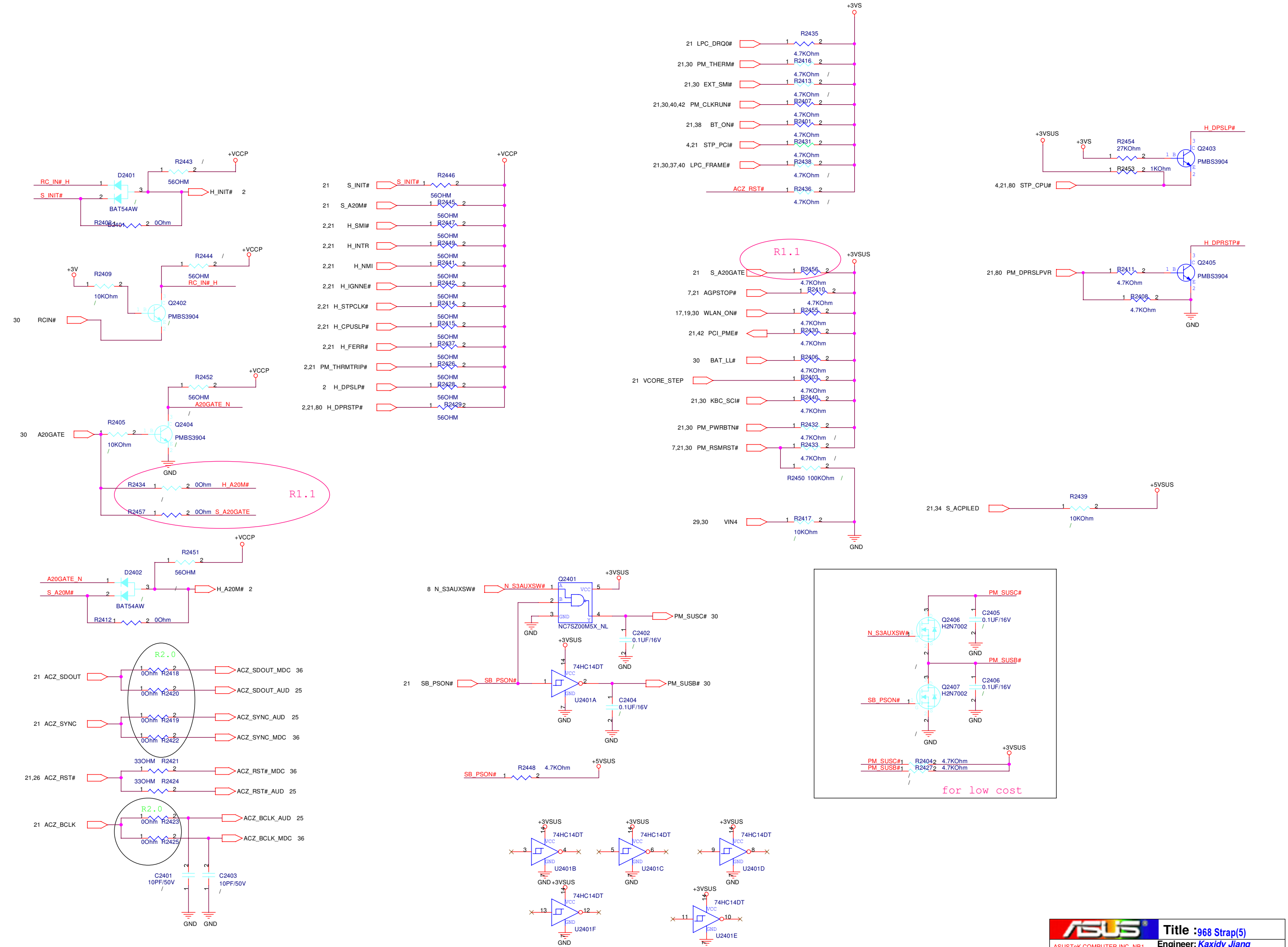
Date: 星期一, 四月 23, 2007 Sheet 22 of 94



Title : 968 Power(4)
Engineer: Kaxidy Jiang
ASUSTeK COMPUTER INC. NB1

Size	Project Name	Rev
C	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 23 of 94



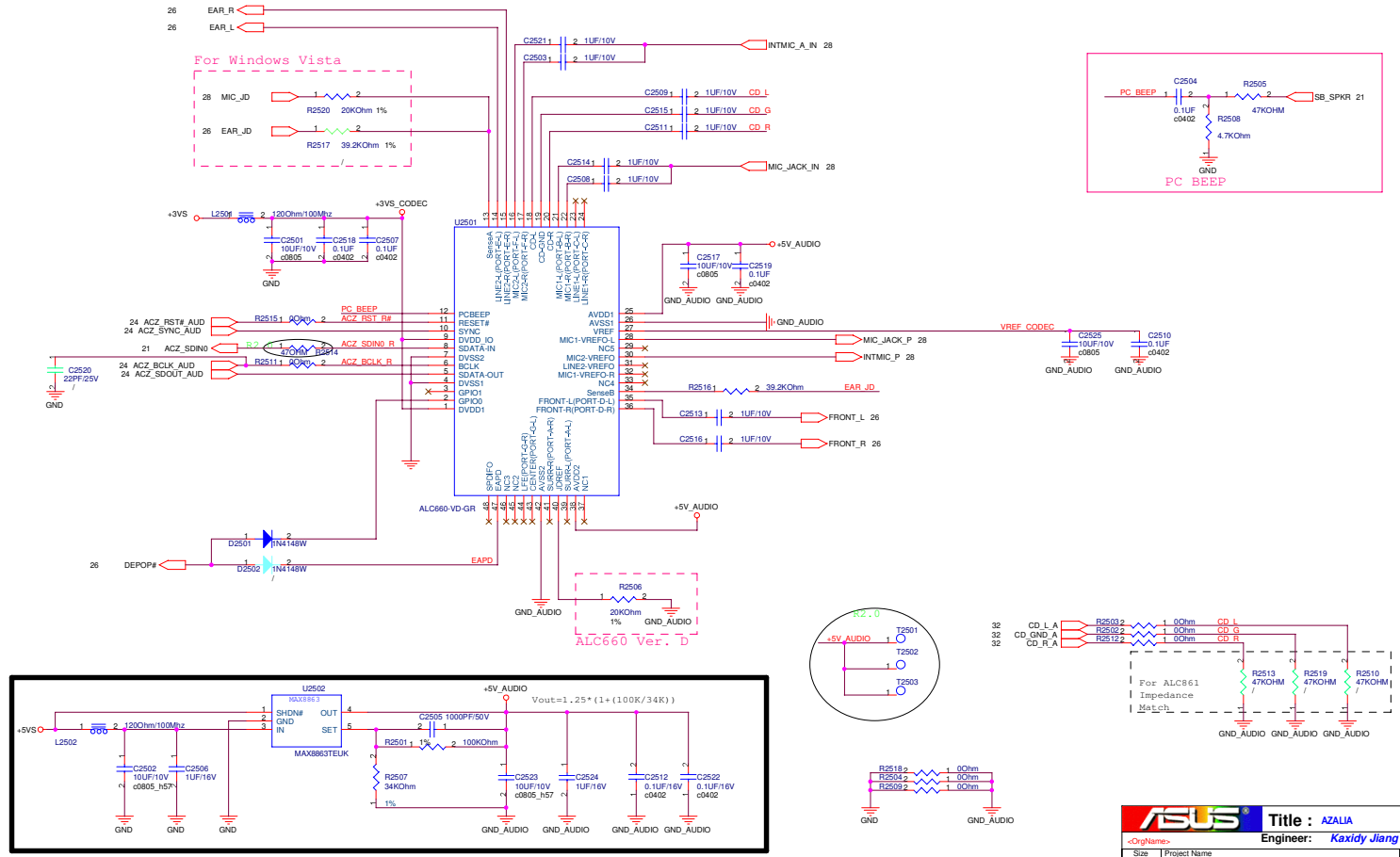
Title : 968 Strap(5)

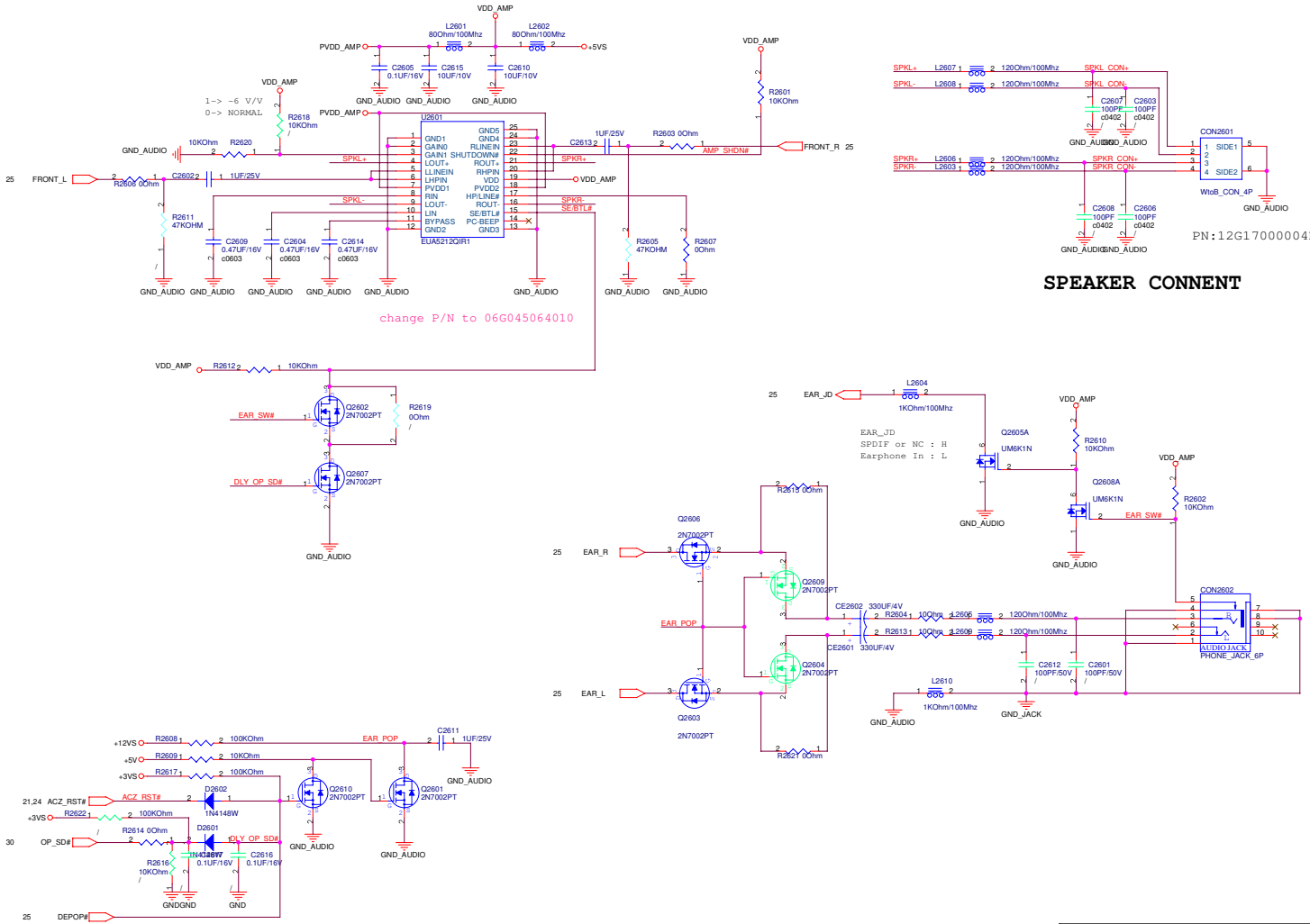
ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy Jiang

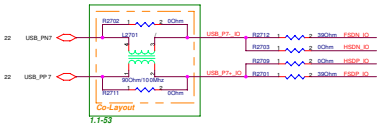
Size	Project Name	Rev
C	F5V	1.0

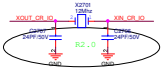
Date: 星期一, 四月 23, 2007 Sheet 24 of 94

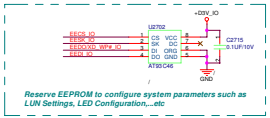

For Windows Vista
PC BEEP
ALC660 Ver. D
For ALC861 Impedance Match
U2501
ALC660-VD-GR
U2502
MAX8863
MAX8863TEUK
Vout=1.25*(1+(100K/34K))
Title : AZALIA
Engineer: Kaxidy Jiang
Project Name F5V
Sheet 25 of 94

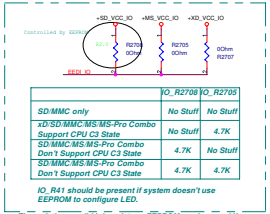


Title : AMPLIFIER 2 CHANNEL			
<OrgName>	Engineer: Kaxidy Jiang		
Size: Custom	Project Name: F5V		Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 26 of 94		





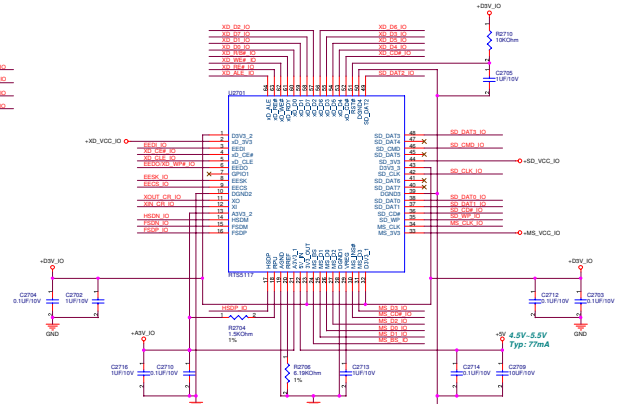


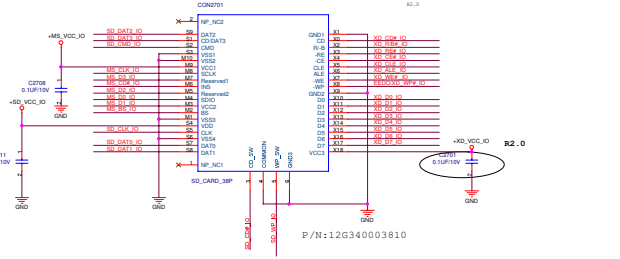


	IO_R2708	IO_R2705
SD/MMC only	No Stuff	No Stuff
xD/SD/MMC/MS/MS-Pro Combo Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	No Stuff
SD/MMC/MS/MS-Pro Combo Don't Support CPU C3 State	4.7K	4.7K

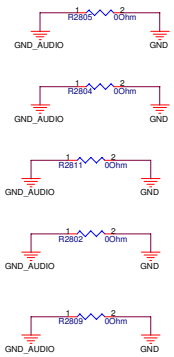
IO_R41 should be present if system doesn't use EEPROM to configure LED.

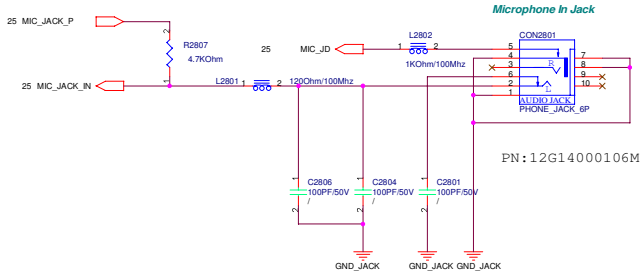
Through these pull-high resistors, EEPROM can be saved if no other requirement about other parameters.





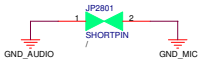
P/N:12G340003810



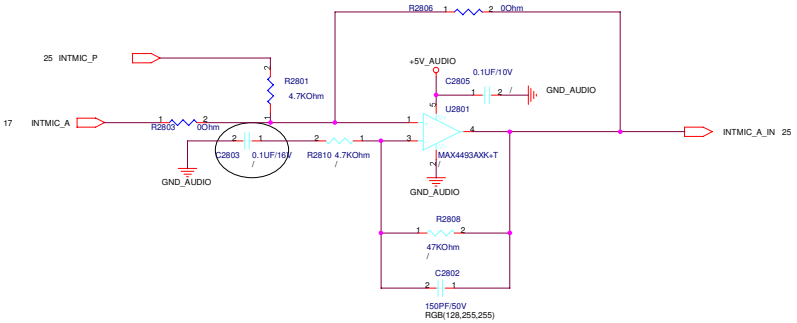


PN:12G14000106M

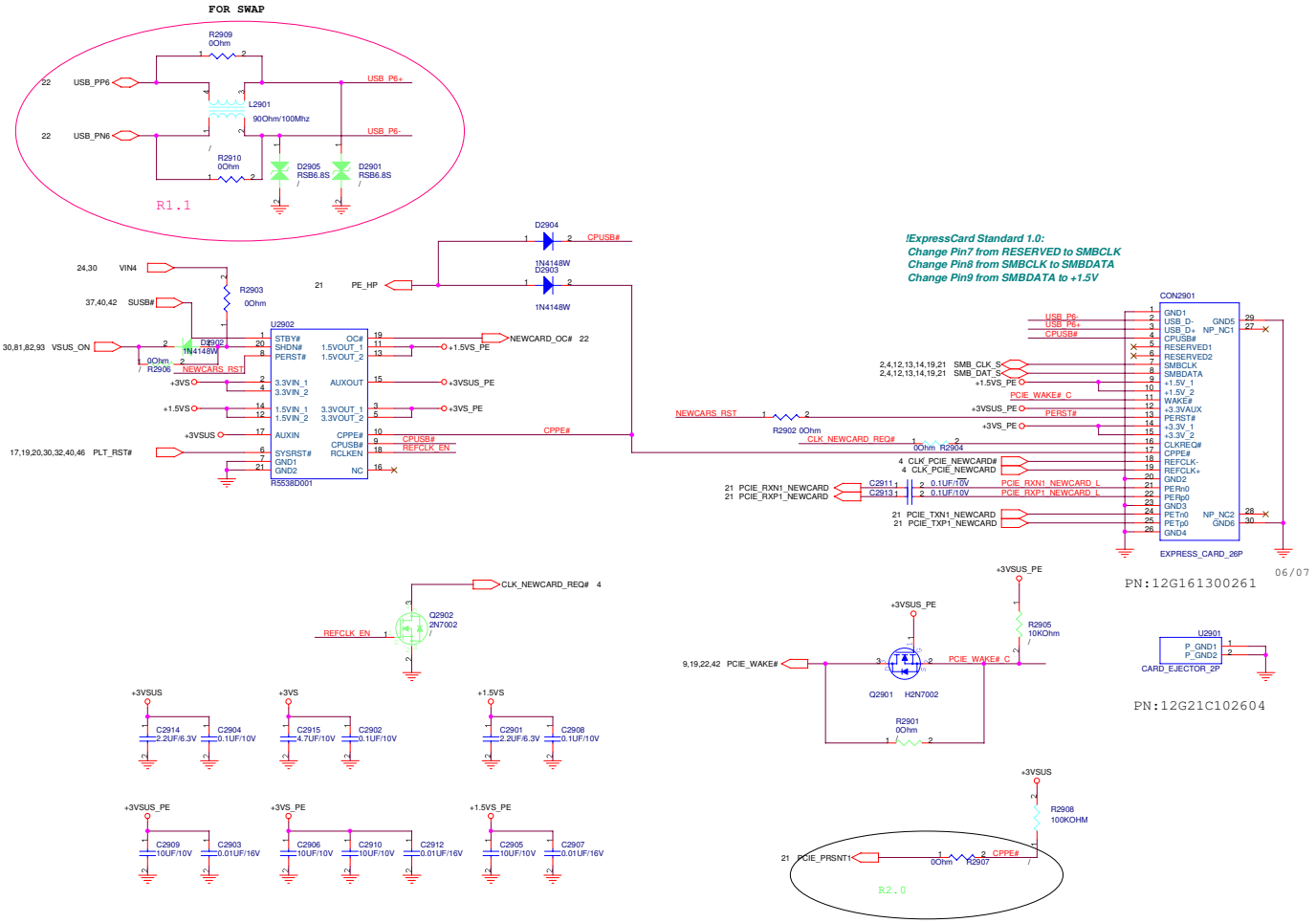
INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



Pre-AMP **For Test Function**



Title : MIC,LINE-IN JACK			
<OrgName>	Engineer: Kaxidy Jiang		
Size: Custom	Project Name: F5V		Rev: 1.0
Date: 星期一, 四月 23, 2007		Sheet 28 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

Title : NEWCARD

Engineer: Kaxidy Jiang

Size	Project Name	Rev
Custom	F5V	1.0

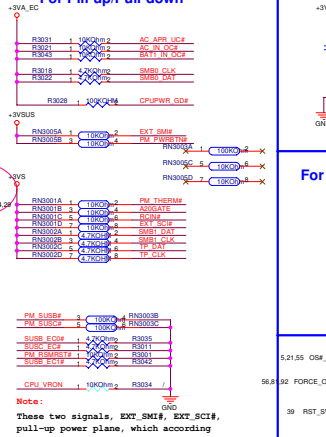
Date: 星期一, 四月 23, 2007 Sheet 29 of 94

For IT8510 Core IC

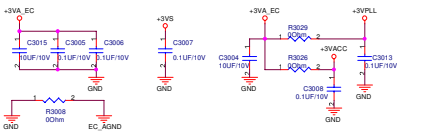
TQFP Package PN:06G042003021

TFBGA Package PN:06G042003030

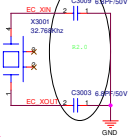
For Pill-up/Pull-down



For IT8510 Power

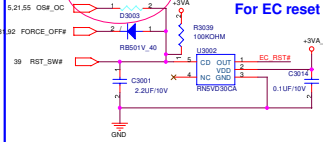


For Xtal



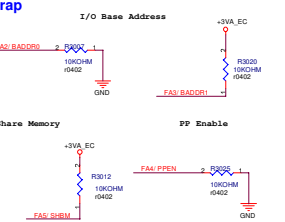
Note:
Cload=12.5PF
close to EC
start up time : 750ms

For EC reset

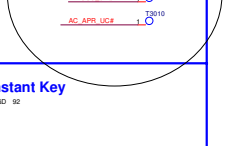


Note:
The reset timing of IT8510 : Refer to IT8510 Hardware Common Pin Assignment section 2.4.

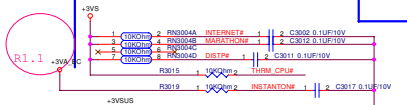
For EC Hardware Strap

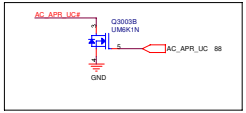


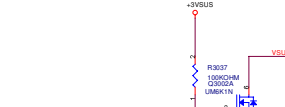
For Instant Key



Note:
Close to EC







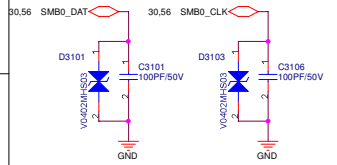
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# don't connect to Battery Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# must connect to Battery Connector.

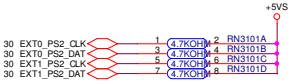


Note:

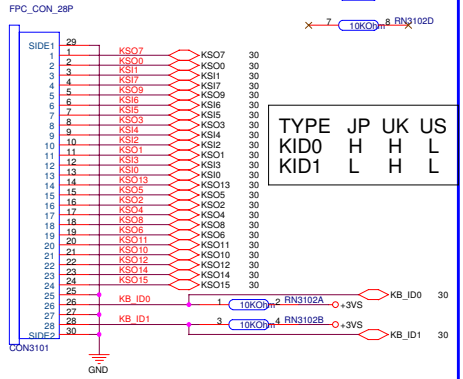
When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

For External PS/2 I/F

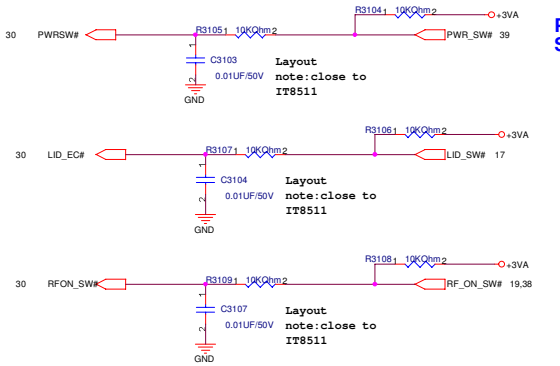


For Keyboard



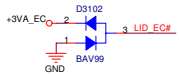
TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

For Switch



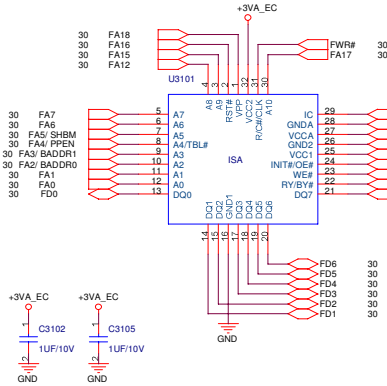
Note:

This LID_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.



Layout note:close to connector

For 4M bits ISA ROM



Note:

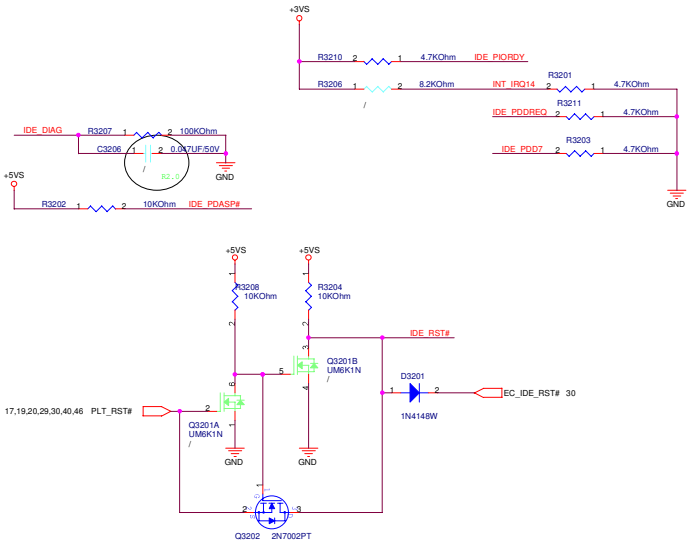
If you use 8M bits ROM, you need to connect FA19 to EC side.

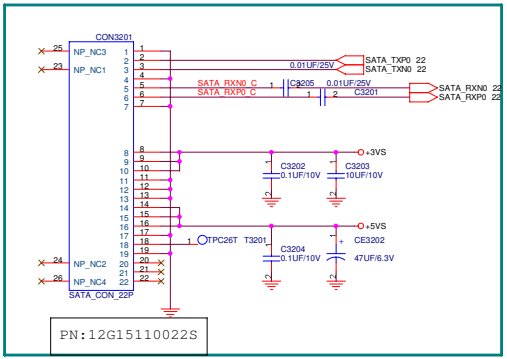
PLCC32 Socket
PN:12G04300032F

SST-PLCC32 4Mbits Flash ROM
PN:05G001027221

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : KB&ISA ROM	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 31 of 94	

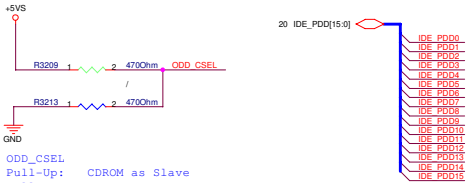




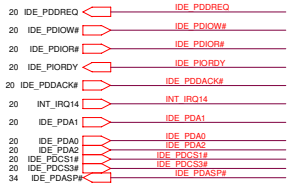
Dafult

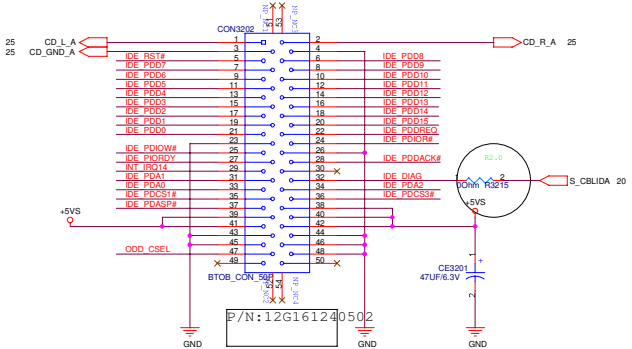
SATA

CD-ROM

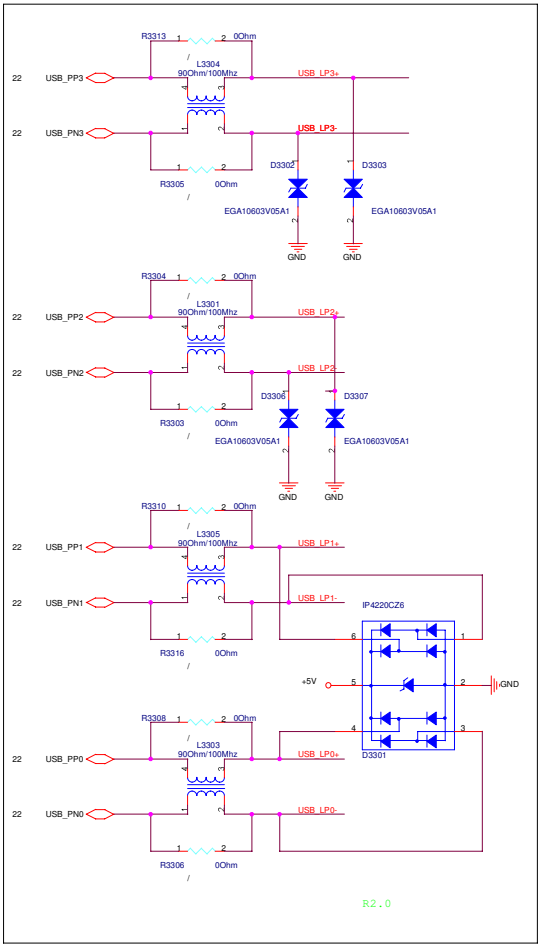


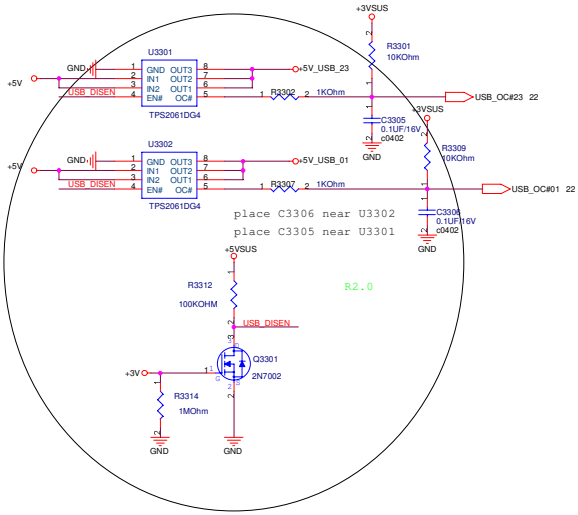
ODD_CSEL
Pull-Up: CDROM as Slave
Pull-Down: CDROM as Master

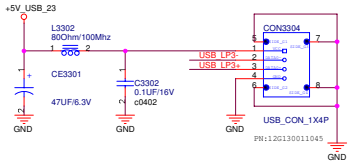


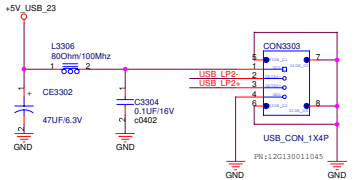


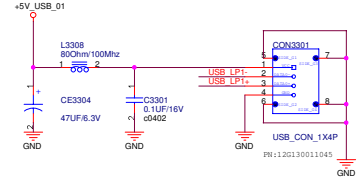
<Variant Name>
ASUSTeK COMPUTER INC
Title : HDD & CD-ROM
Engineer: Kaxidy Jiang
Size: Custom
Project Name: F5V
Rev: 1.0
Date: 星期一, 四月 23, 2007
Sheet 32 of 94

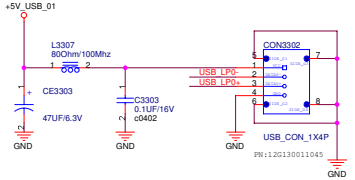








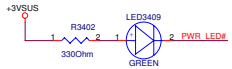


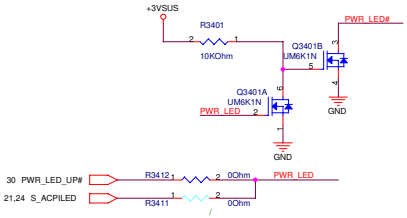


<variant_name>

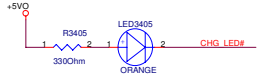
ASUSTeK COMPUTER INC. NB1	Title : USB CONN	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 33 of 94	
</variant_name>

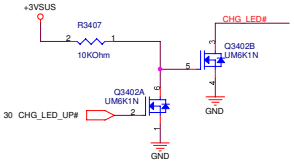
For POWER LED



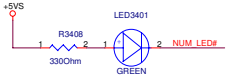


BATTERY LED

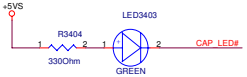


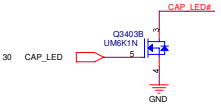


Num Lock

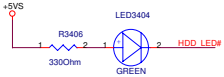


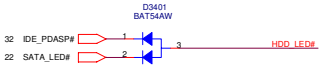
Cap Lock



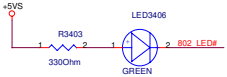


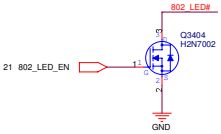
SATA/IDE LED



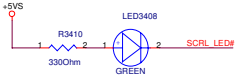


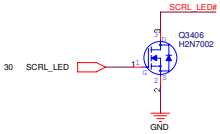
WireLess LED



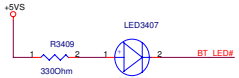


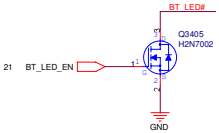
Scroll Lock

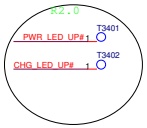




BT LED







ASUSTeK Computer INC

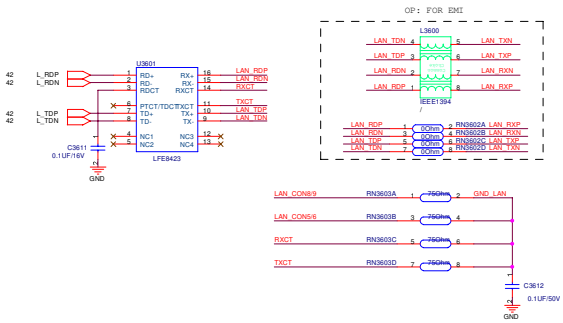
Title : BLANK

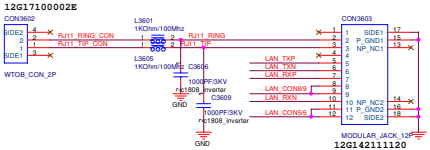
Engineer: Hawk Zhu

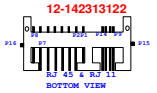
Size	Project Name	Rev
B	F5V	1.0

Date: 星期 一, 四月 23, 2007 Sheet 35 of 94

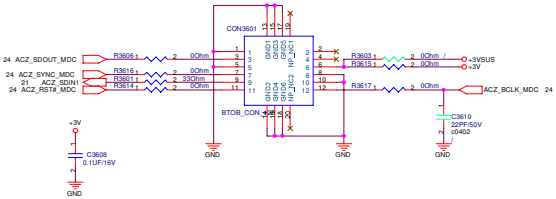
LAN PORT







MDC



ASUSTeK COMPUTER INC	Title : RJ11+45 & MDC		
	Engineer: Kaxidy Jiang		
Size: C	Project Name: F5V		Rev: 1.0
Date: 日期-, 月1 23, 2007	Sheet 36 of 94		

System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.2VS, +2.5V, +VCCP
SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS

+12V
R3701
330Ohm
Q3707
2N7002
+5V
R3706
330Ohm
Q3701
2N7002
+3V
R3709
330Ohm
Q3706
2N7002
+1.8V
R3703
330Ohm
Q3710
2N7002
+3VA
100KOHM
R3713
Q3712
2N7002
30,91 SUSC_EC#
+12VS
R3702
330Ohm
Q3702
2N7002
+5VS
R3710
330Ohm
Q3704
2N7002
+3VS
R3707
330Ohm
Q3705
2N7002
+2.5VS
R3714
330Ohm
Q3714
2N7002
+1.8VS
R3704
330Ohm
Q3709
2N7002
+1.5VS
R3708
330Ohm
Q3711
2N7002
+1.2VS
R3711
330Ohm
Q3703
2N7002
+VCCP
R3716
330Ohm
Q3715
2N7002
+0.9VS
R3705
330Ohm
Q3708
2N7002
R1.1
+3VA
100KOHM
R3712
Q3713
2N7002
30,91,92 SUSB_EC1#
R3715
0Ohm
SUSB# 29,40,42

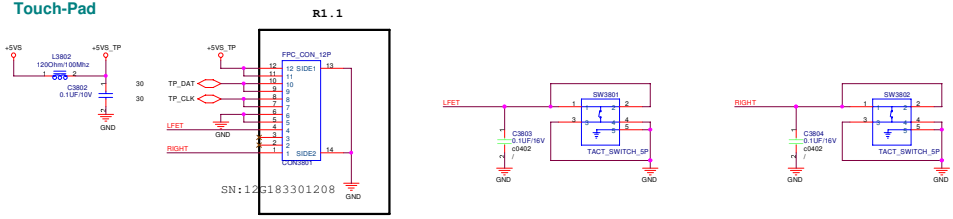
Debug Port

+3VS
CON3701
21,30,40 LPC_AD0
21,30,40 LPC_AD1
21,30,40 LPC_AD2
21,30,40 LPC_AD3
21,24,30,40 LPC_FRAME#
4 CLK_DBGPCI
SIDE2
SIDE1
C3701
10PF/50V
GND
GND
FPC_CON_12P
Bottom Contact

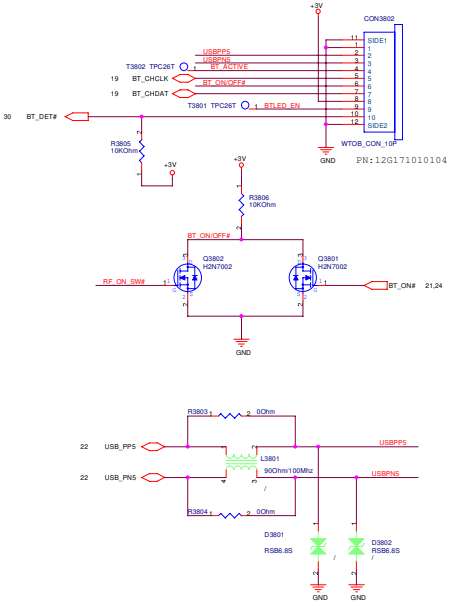
<Variant Name>

ASUSTeK COMPUTER INC	Title : DISCHARGE CKT	
	Engineer: Kaxidy Jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 37 of 94	

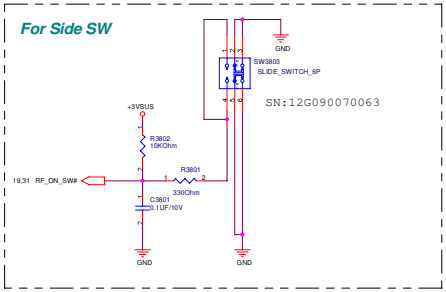
Touch-Pad



For Bluetooth



For Side SW



<Variant Name>

ASUSTeK COMPUTER INC. NB1

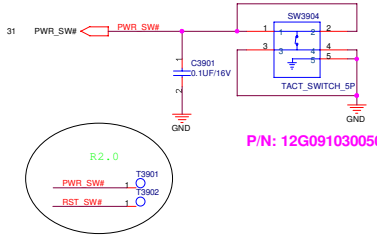
Title : BT&TP

Engineer: Kaxidy Jiang

Size	Project Name	Rev
C	F5V	1.0

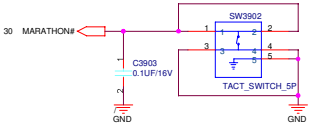
Date: 星期一, 四月 23, 2007 Sheet 38 of 84

Power SW.

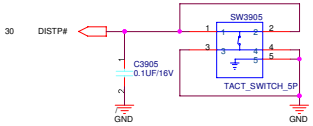


P/N: 12G091030050

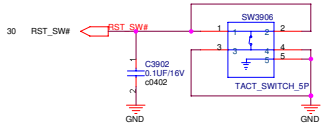
Marathon SW.



Disable Touch Pad SW.

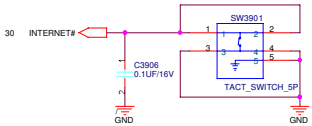


RESET SW.

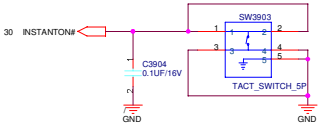


P/N: 12G091030050

Internet SW.



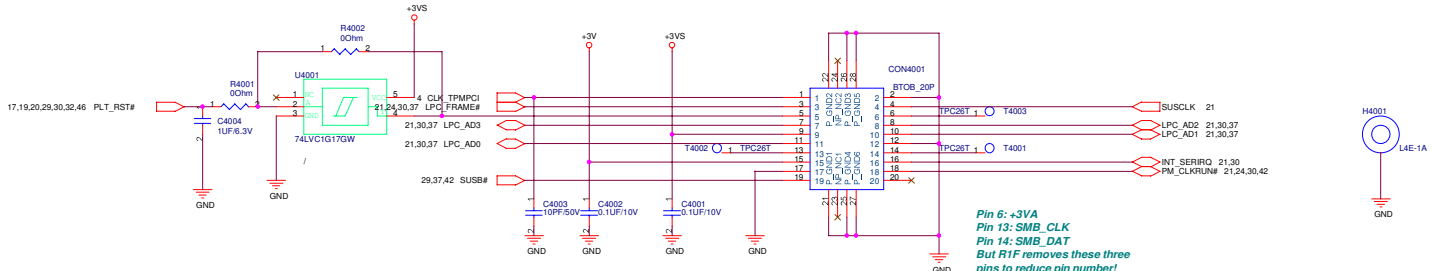
IstantON SW.



<Variant Name>

ASUSTeK COMPUTER INC	Title : SWITCH	
	Engineer: Kaxidy jiang	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 39 of 94	

For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

SN:12G16080020J

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : TPM

Engineer: Kaxidy Jiang

Size	Project Name	Rev
Custom	F5V	1.0

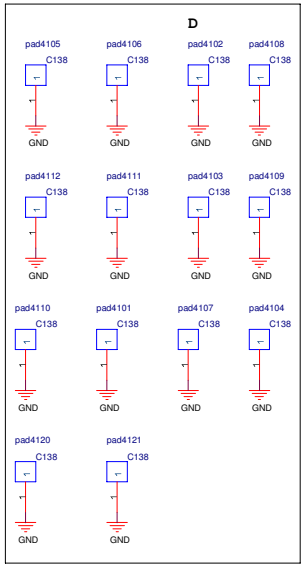
Date: 星期一, 四月 23, 2007 Sheet 40 of 94

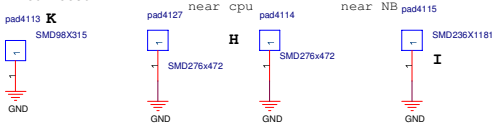
above ODD connector

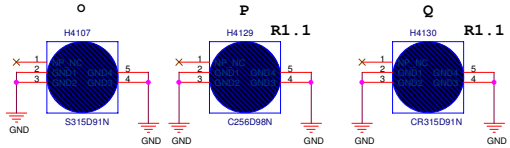
near cpu

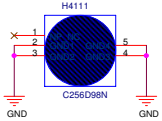
near NB

near NEWCARD

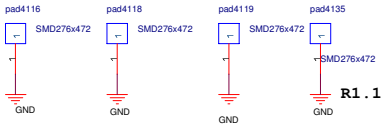


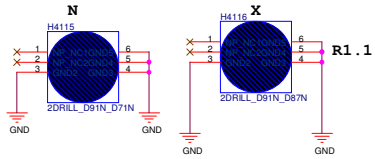


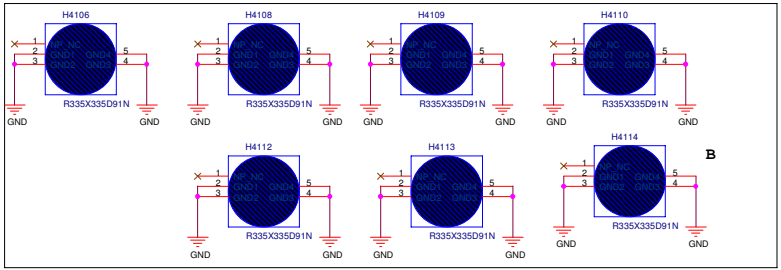


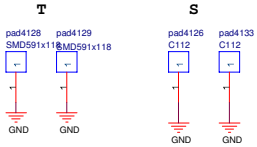


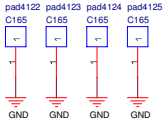
H



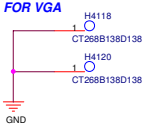




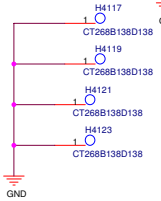




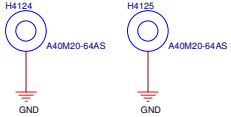
FOR VGA



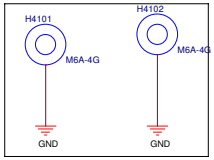
FOR CPU



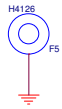
FOR Mini card



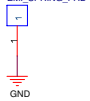
FOR MDC



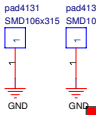
FOR FAN



For EMI

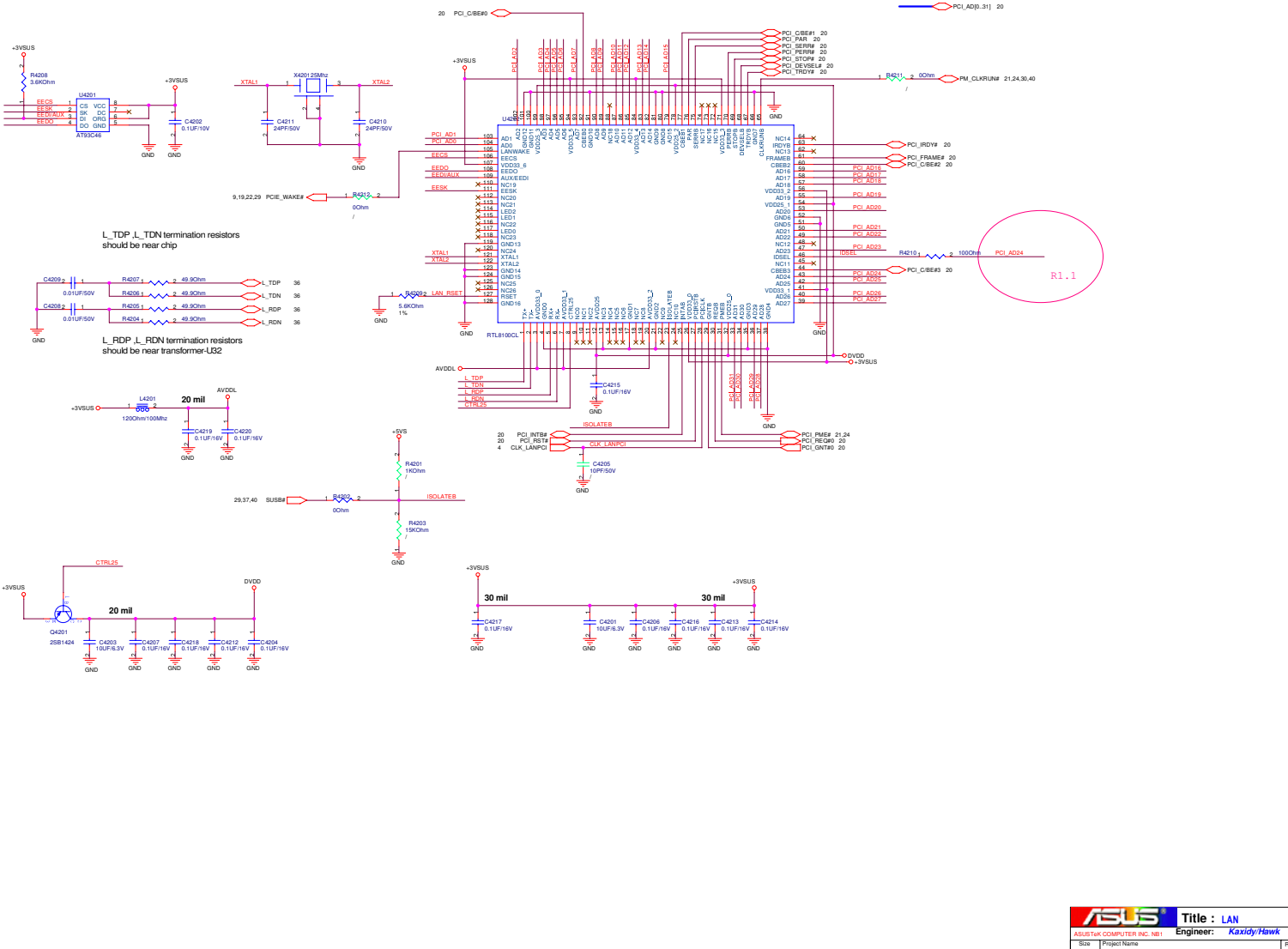


U



R2.0 change to P/N:13GN9980M090-1 for high limit

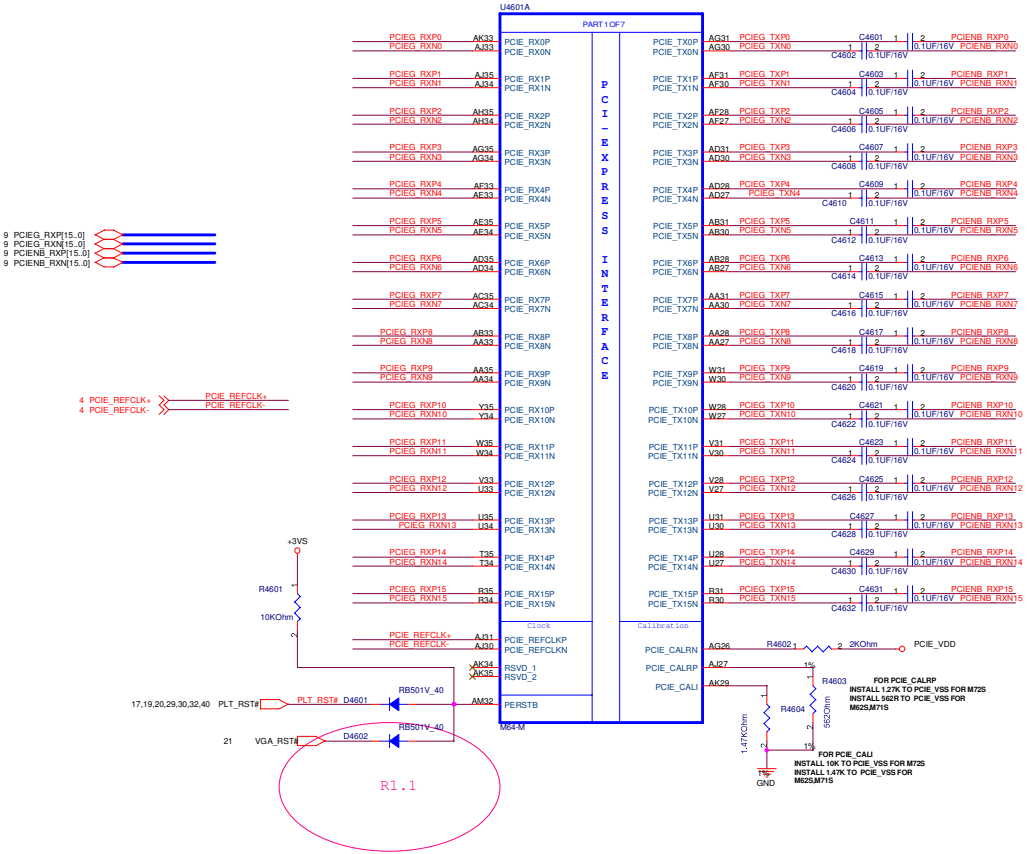
ASUSTeK COMPUTER INC. NB1	Title : Screw hole	
	Engineer: Kaxidy/Hawk	
Size: B	Project Name: F5V	Rev: 1.0
Date: 星期 , 四月 23, 2007	Sheet 41 of 94	


L_TDP /L_TDN termination resistors
should be near chip
L_RDP /L_RDN termination resistors
should be near transformer-U32
20 mil
30 mil
30 mil
RTL8100CL
AT93C46
X4201 25MHz
R1.1
Title : LAN
ASUSTeK COMPUTER INC. NB1
Engineer: Kaxidy/Hawk
Size: C
Project Name: F5V
Rev: 1.0
Date: 星期一, 五月 23, 2007
Sheet 42 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 43 of 94	

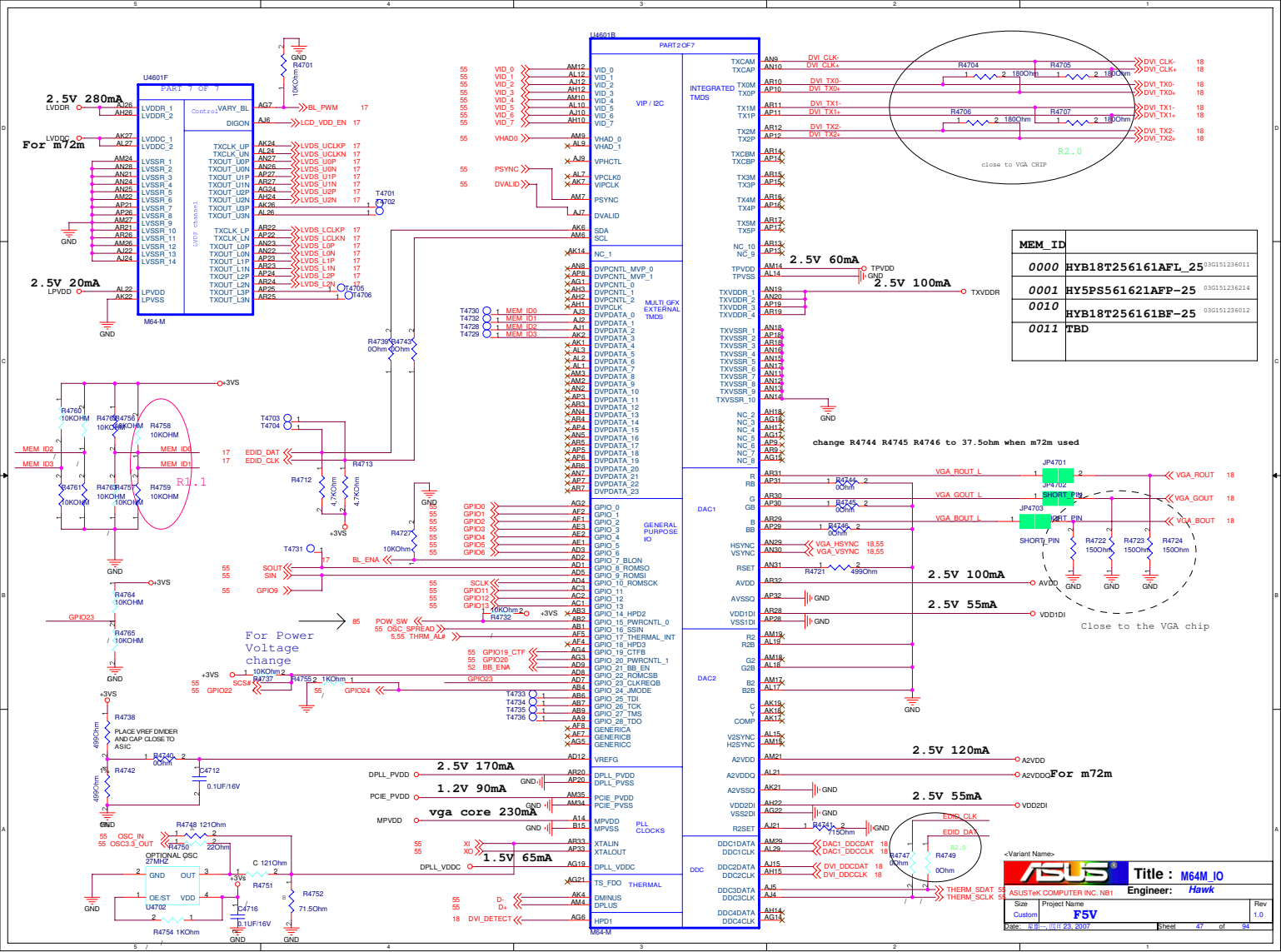
ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 44 of 94	

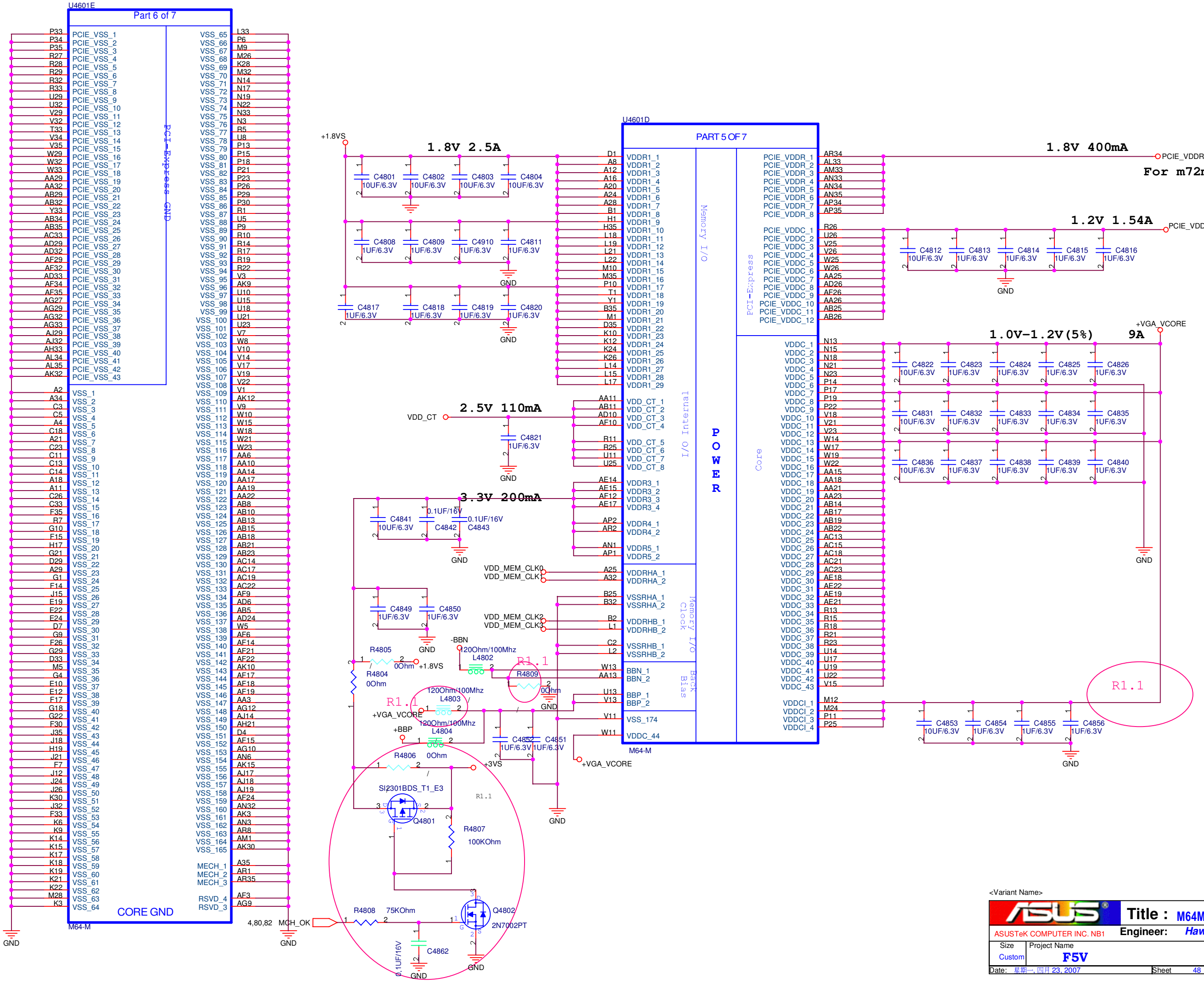
ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 45 of 94	



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : M64M PCIE	
	Engineer: Hawk	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 46 of 94	


U4601F
PART 7 OF 7
2.5V 280mA
LVDDR
For m72m
LVDDC
2.5V 20mA
LPVDD
M64-M
U4601B
PART 2 OF 7
VIP / I2C
INTEGRATED TMDS
MULTI GFX EXTERNAL TMDS
GENERAL PURPOSE IO
DAC1
DAC2
DDC
PLL CLOCKS
THERMAL
2.5V 60mA
2.5V 100mA
TPVDD
TXVDDR
change R4744 R4745 R4746 to 37.5ohm when m72m used
2.5V 100mA
AVDD
2.5V 55mA
VDD1DI
Close to the VGA chip
2.5V 120mA
A2VDD
A2VDDQ
For m72m
VDD2DI
2.5V 55mA
2.5V 170mA
DPLL_PVDD
1.2V 90mA
PCIE_PVDD
vga core 230mA
MPVDD
1.5V 65mA
DPLL_VDDC
For Power Voltage change
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC
OPTIONAL OSC 27MHZ
close to VGA CHIP
R2.0
MEM_ID
0000 HYB18T256161AFL_25
0001 HY5PS561621AFP-25
0010 HYB18T256161BF-25
0011 TBD
Title : M64M_IO
ASUSTeK COMPUTER INC. NB1
Engineer: Hawk
Project Name F5V
Date: 星期一, 四月 23, 2007
Sheet 47 of 94



<Variant Name>

ASUS

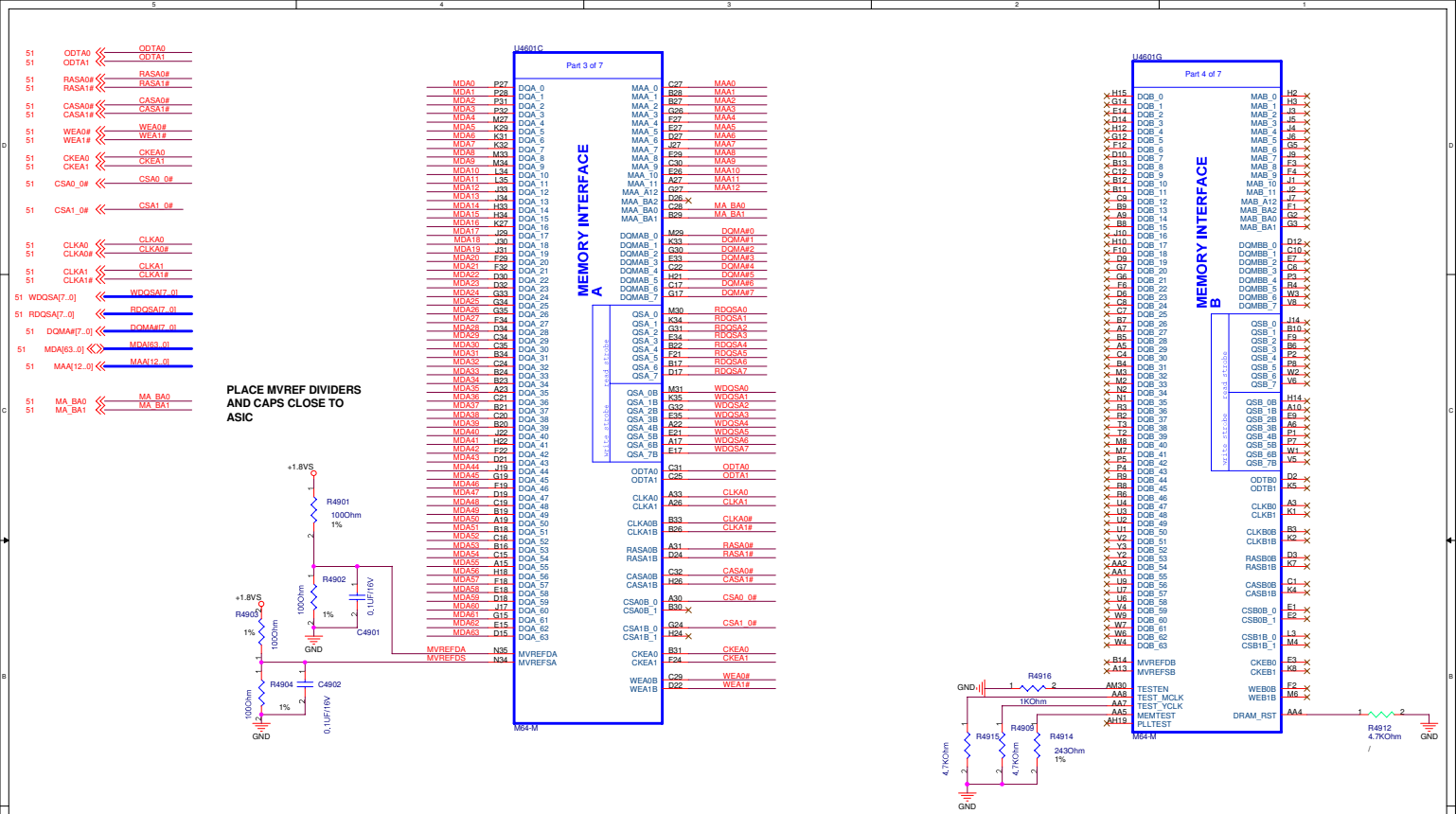
Title : M64M POWER

Engineer: Hawk

ASUSTeK COMPUTER INC. NB1

Size	Project Name	Rev
Custom	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 48 of 94


ODTA0
ODTA1
RASA0#
RASA1#
CASA0#
CASA1#
WEA0#
WEA1#
CKEA0
CKEA1
CSA0_0#
CSA1_0#
CLKA0
CLKA0#
CLKA1
CLKA1#
WDQSA[7..0]
RDQSA[7..0]
DQMA#[7..0]
MDA[63..0]
MAA[12..0]
MA_BA0
MA_BA1
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
+1.8VS
R4901
100Ohm
1%
R4902
100Ohm
1%
C4901
0.1UF/16V
GND
R4903
100Ohm
1%
R4904
100Ohm
1%
C4902
0.1UF/16V
MVREFDA
MVREFDS
U4601C
Part 3 of 7
MEMORY INTERFACE A
DQA_0
DQA_1
DQA_2
DQA_3
DQA_4
DQA_5
DQA_6
DQA_7
DQA_8
DQA_9
DQA_10
DQA_11
DQA_12
DQA_13
DQA_14
DQA_15
DQA_16
DQA_17
DQA_18
DQA_19
DQA_20
DQA_21
DQA_22
DQA_23
DQA_24
DQA_25
DQA_26
DQA_27
DQA_28
DQA_29
DQA_30
DQA_31
DQA_32
DQA_33
DQA_34
DQA_35
DQA_36
DQA_37
DQA_38
DQA_39
DQA_40
DQA_41
DQA_42
DQA_43
DQA_44
DQA_45
DQA_46
DQA_47
DQA_48
DQA_49
DQA_50
DQA_51
DQA_52
DQA_53
DQA_54
DQA_55
DQA_56
DQA_57
DQA_58
DQA_59
DQA_60
DQA_61
DQA_62
DQA_63
MVREFDA
MVREFSA
MAA_0
MAA_1
MAA_2
MAA_3
MAA_4
MAA_5
MAA_6
MAA_7
MAA_8
MAA_9
MAA_10
MAA_11
MAA_A12
MAA_BA2
MAA_BA0
MAA_BA1
MA_BA0
MA_BA1
DQMA#0
DQMA#1
DQMA#2
DQMA#3
DQMA#4
DQMA#5
DQMA#6
DQMA#7
DQMAB_0
DQMAB_1
DQMAB_2
DQMAB_3
DQMAB_4
DQMAB_5
DQMAB_6
DQMAB_7
read strobe
write strobe
QSA_0
QSA_1
QSA_2
QSA_3
QSA_4
QSA_5
QSA_6
QSA_7
QSA_0B
QSA_1B
QSA_2B
QSA_3B
QSA_4B
QSA_5B
QSA_6B
QSA_7B
RDQSA0
RDQSA1
RDQSA2
RDQSA3
RDQSA4
RDQSA5
RDQSA6
RDQSA7
WDQSA0
WDQSA1
WDQSA2
WDQSA3
WDQSA4
WDQSA5
WDQSA6
WDQSA7
ODTA0
CLKA0
CLKA1
CLKA0B
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
CSA0_0#
CSA1_0#
CKEA0
CKEA1
WEA0#
WEA1#
M64-M
U4601G
Part 4 of 7
MEMORY INTERFACE B
DQB_0
DQB_1
DQB_2
DQB_3
DQB_4
DQB_5
DQB_6
DQB_7
DQB_8
DQB_9
DQB_10
DQB_11
DQB_12
DQB_13
DQB_14
DQB_15
DQB_16
DQB_17
DQB_18
DQB_19
DQB_20
DQB_21
DQB_22
DQB_23
DQB_24
DQB_25
DQB_26
DQB_27
DQB_28
DQB_29
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DQB_33
DQB_34
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DQB_37
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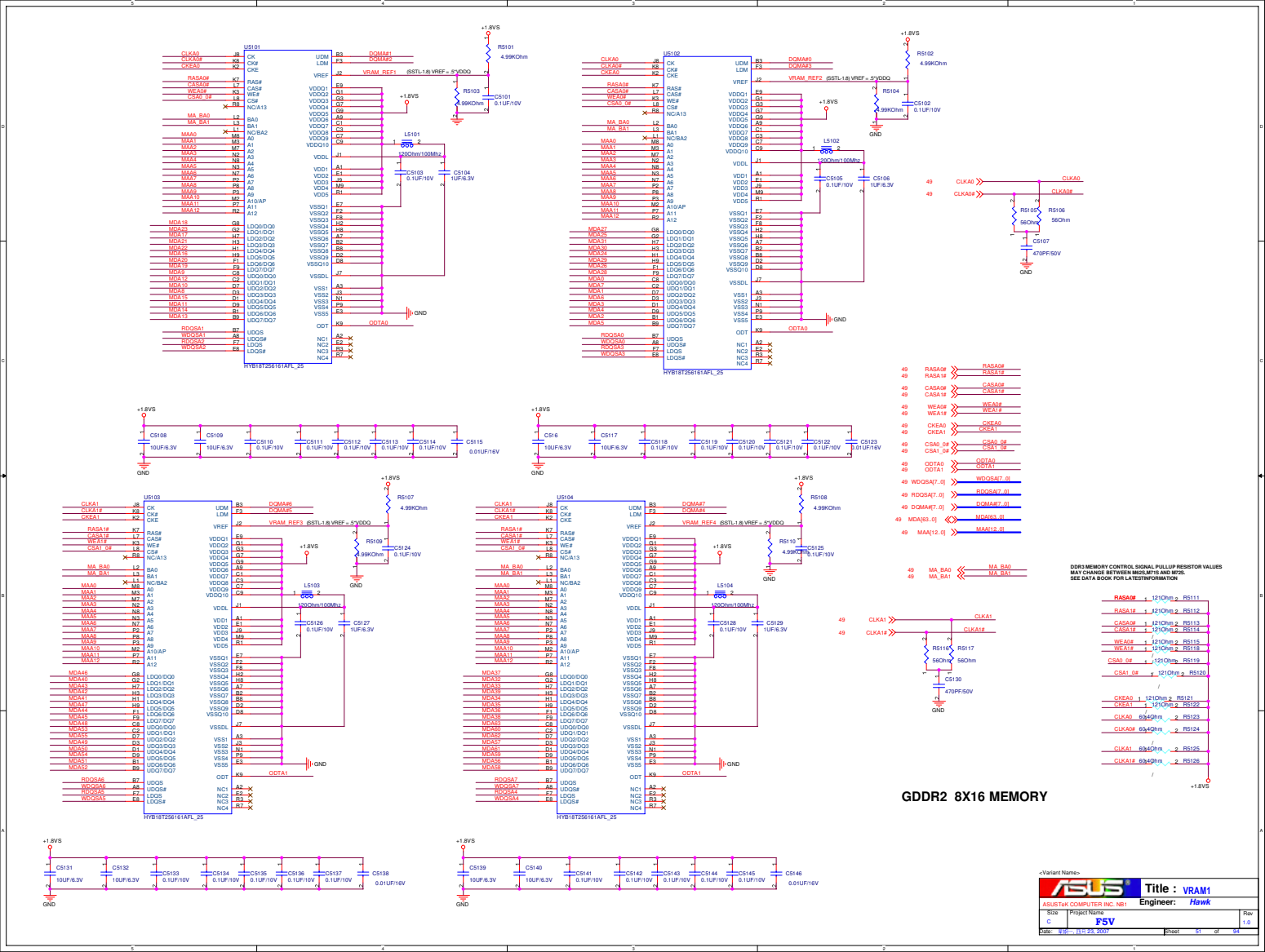
DQB_44
DQB_45
DQB_46
DQB_47
DQB_48
DQB_49
DQB_50
DQB_51
DQB_52
DQB_53
DQB_54
DQB_55
DQB_56
DQB_57
DQB_58
DQB_59
DQB_60
DQB_61
DQB_62
DQB_63
MAB_0
MAB_1
MAB_2
MAB_3
MAB_4
MAB_5
MAB_6
MAB_7
MAB_8
MAB_9
MAB_10
MAB_11
MAB_A12
MAB_BA2
MAB_BA0
MAB_BA1
DQMBB_0
DQMBB_1
DQMBB_2
DQMBB_3
DQMBB_4
DQMBB_5
DQMBB_6
DQMBB_7
QSB_0
QSB_1
QSB_2
QSB_3
QSB_4
QSB_5
QSB_6
QSB_7
QSB_0B
QSB_1B
QSB_2B
QSB_3B
QSB_4B
QSB_5B
QSB_6B
QSB_7B
ODTB0
CLKB0
CLKB1
CLKB0B
CLKB1B
RASB0B
RASB1B
CASB0B
CASB1B
CSB0B_0
CSB0B_1
CSB1B_0
CSB1B_1
CKEB0
CKEB1
WEB0B
WEB1B
MVREFDB
MVREFSB
TESTEN
TEST_MCLK
TEST_YCLK
MEMTEST
PLLTEST
DRAM_RST
M64-M
R4916
1KOhm
R4915
4.7KOhm
R4905
4.7KOhm
R4914
243Ohm
1%
R4912
4.7KOhm
GND
<Variant Name>
Title : M64M MEMORY
ASUSTeK COMPUTER INC. NB1
Engineer: Hawk
Size
Custom
Project Name
F5V
Rev
1.0
Date: 星期一, 四月 23, 2007
Sheet 49 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 50 of 94	

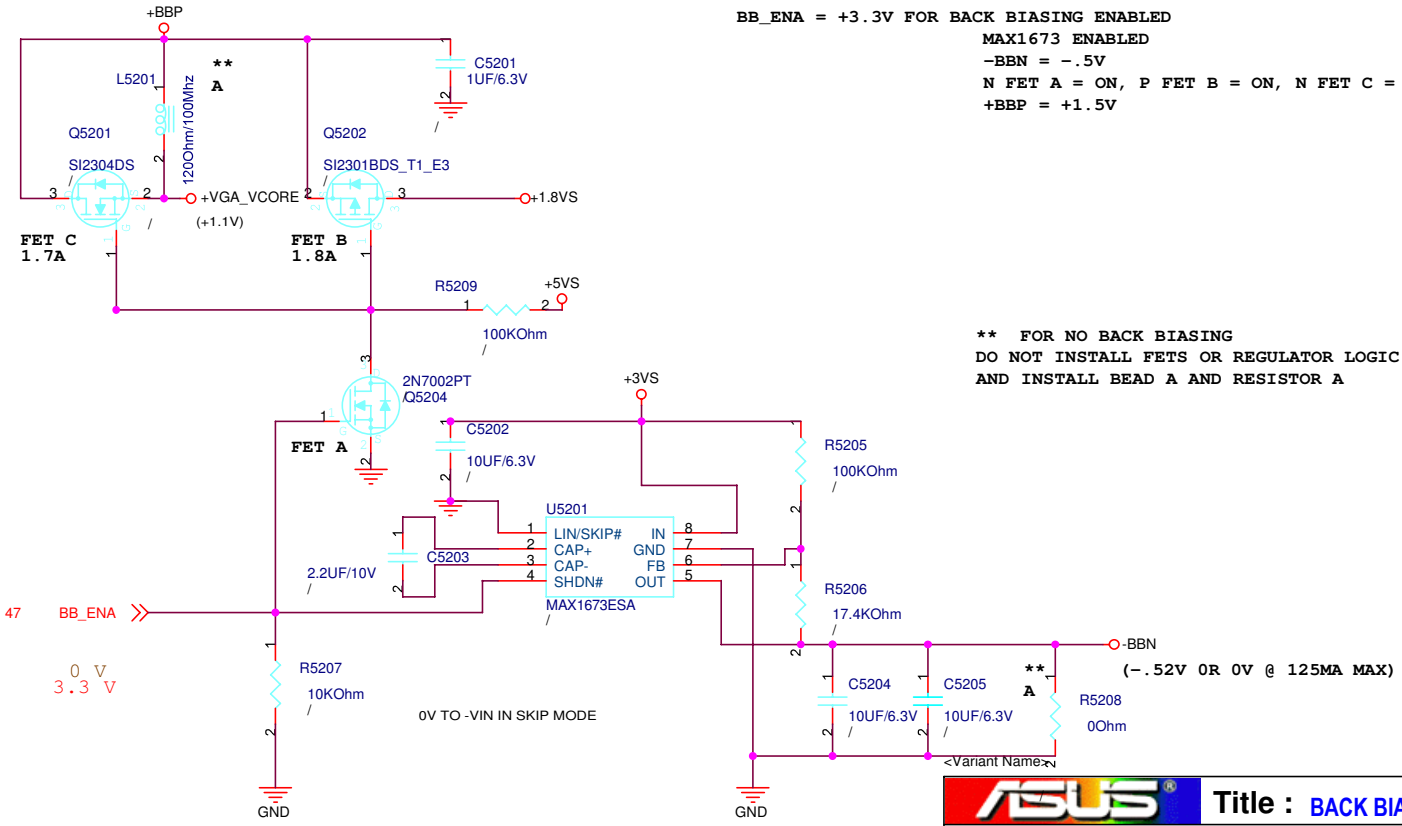

GDDR2 8X16 MEMORY
DDR3 MEMORY CONTROL SIGNAL PULL UP RESISTOR VALUES MAY CHANGE BETWEEN M62S,M71S AND M72S. SEE DATA BOOK FOR LATEST INFORMATION
HYB18T256161AFL_25
Title : VRAM1
Engineer: Hawk
ASUSTeK COMPUTER INC. NB1
F5V

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V

** FOR NO BACK BIASING
DO NOT INSTALL FETS OR REGULATOR LOGIC
AND INSTALL BEAD A AND RESISTOR A



ASUSTeK COMPUTER INC. NB1	Title : BACK BIAS	
	Engineer: Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 52 of 94	

COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

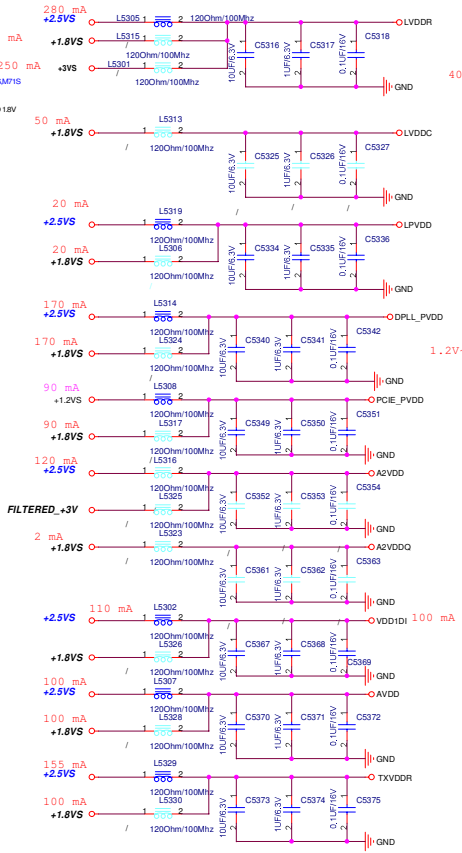
LTPVSS18 DVSSDI TPVSS MPVSS
PCIE_PVSS PVSS A2VSSQ AVSSQ
*****

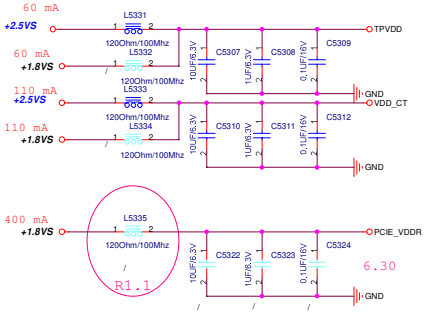
PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACES
FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP

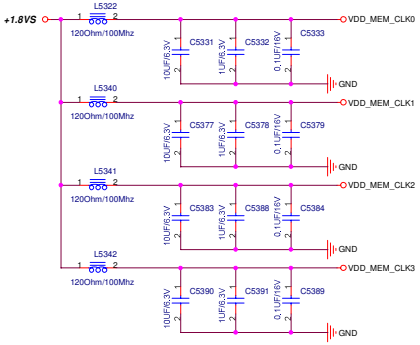
INSTALL LTDDR TO +1.8V OR 3.3V FOR M72S

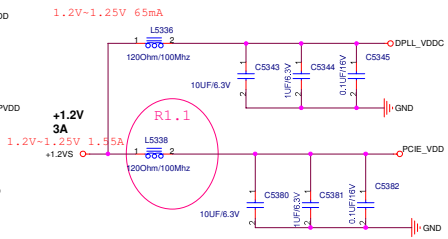
INSTALL LVDDR TO +2.5V FOR M62S,M71S

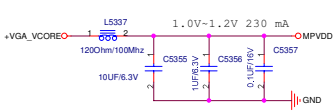
FOR M72S INSTALL LVDDC TO 1.8V
FOR M62S,M71S LVDDC IS NO CONNECTION

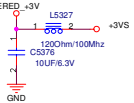












55 mA

ASUSTeK COMPUTER INC. NB1		Title : IO capacitor	
		Engineer: Hawk	
Size: Custom	Project Name: F5V		Rev: 1.0
Date: 星期一, 四月 23, 2007		Sheet 53 of 94	

<Variant Name>

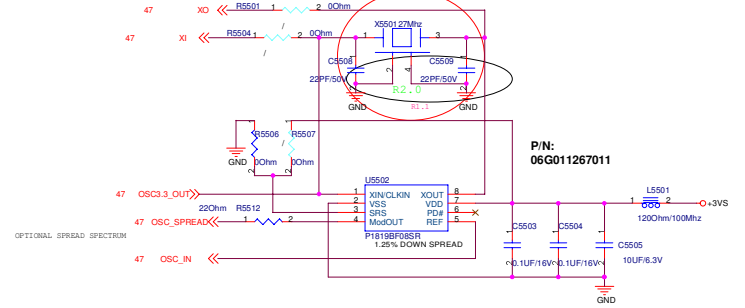
Title : VRAM2

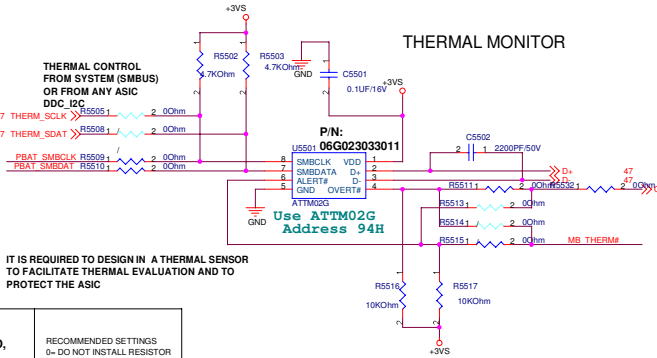
ASUSTeK COMPUTER INC. NB1

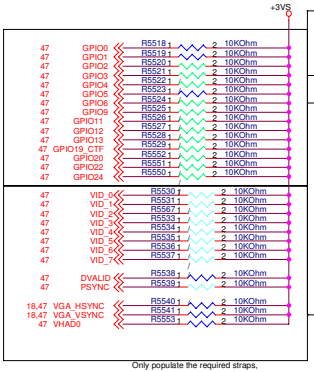
Engineer: Hawk

Size	Project Name	Rev
C	F5V	1.0

Date: 星期一, 月 23, 2007 Sheet 54 of 94







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M62S,M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1:0	GPIO[6:5]	BIAS CURRENT FOR PCIE PHY PLL	0 1	X X
BIOS_ROM_EN	GPIO19_CTF	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERATURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0	O
BIF_VGA DIS	PSYNC	VGA ENABLED	NA	O
MEM_TYPE	UNUSED GPIO	MEMORY TYPE,MAKE AND SIZE INFO	X X X	X X X

ATI RESERVED CONFIGURATION STRAPS

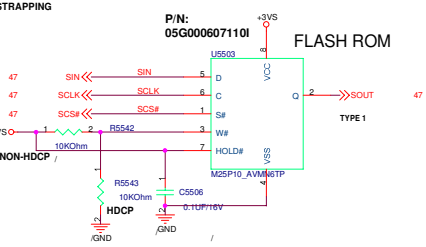
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VID0 VID2 VID3 VID4 VID6 VID7 HSYNC GPIO8 DVALID GPIO2 GPIO3

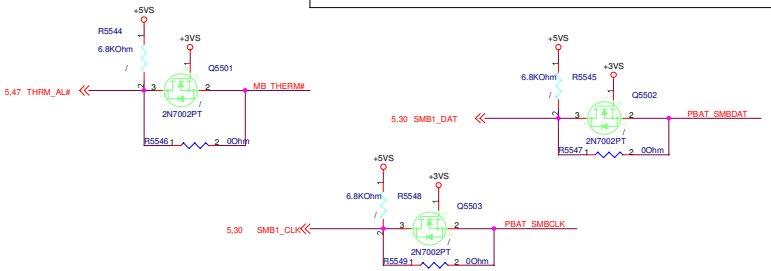
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GENERICC GPIO18_HPD3 GPIO23_CLKREQB

A 256MB MEMORY APERTURE SIZE CAN BE DEFINED USING A SEPARATE ROM OR STRAPPING

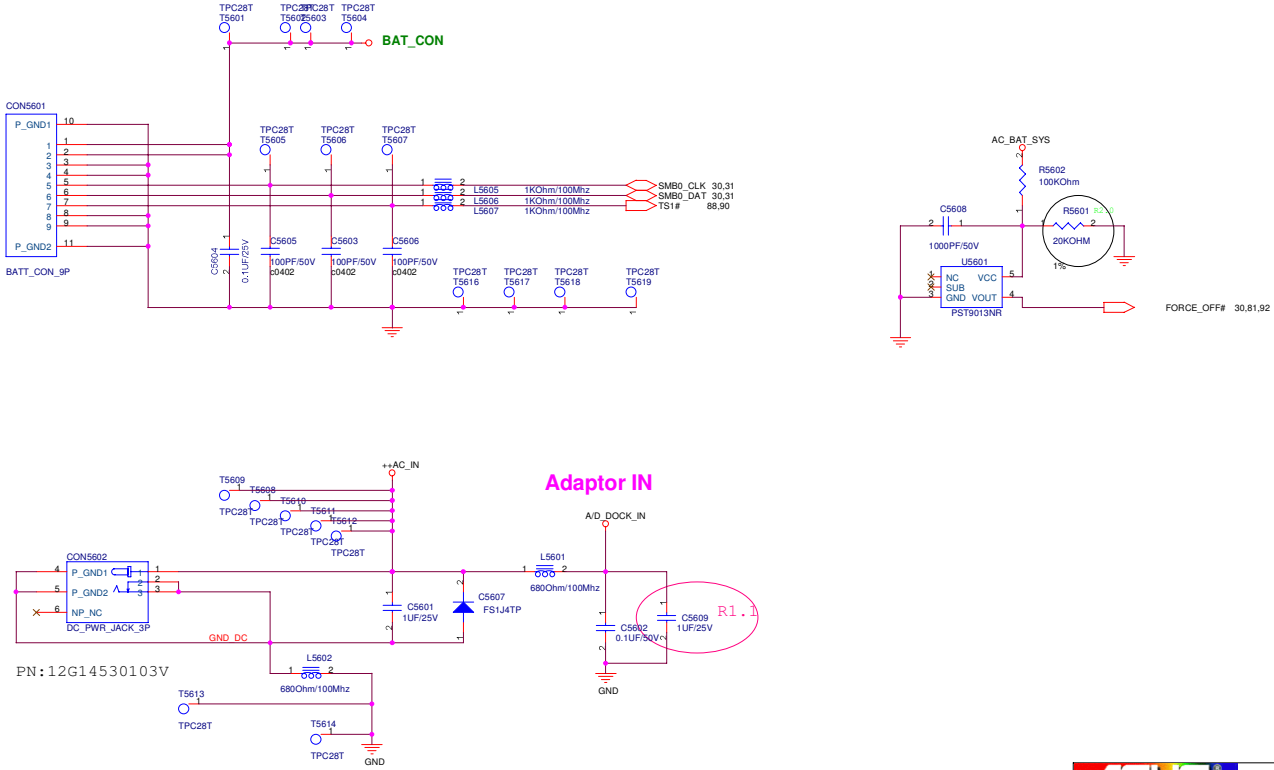


FOR M62S,M71S
A SPECIAL EXTERNAL EEPROM WITH THE WP PIN PULLED DOWN IS MANDATORY FOR HDCP SUPPORT
CONSULT HDCP APPLICATION NOTES FOR ADDITIONAL INFORMATION
M72S DOES NOT REQUIRE AN EXTERNAL ROM FOR HDCP SUPPORT

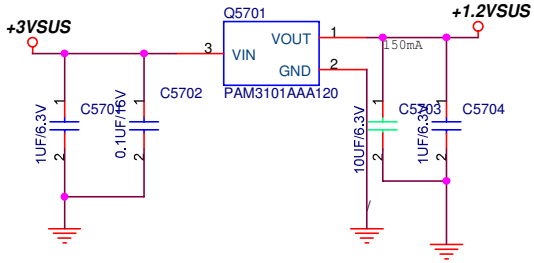


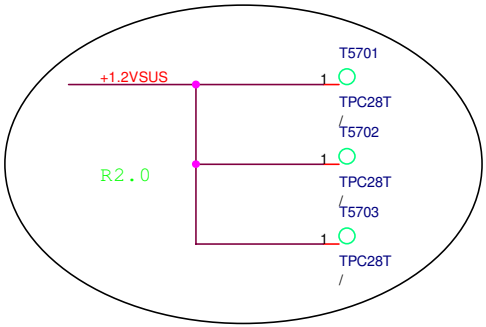
COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

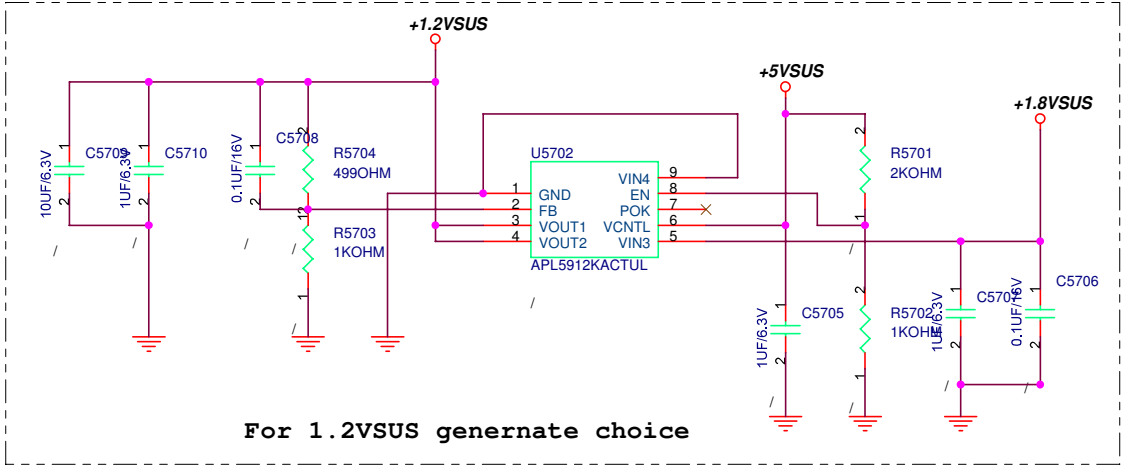
ASUSTeK COMPUTER INC. NB1	Title : SS STRAPS	
	Engineer: Hawk Kaxidy	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 55 of 94	



ASUSTeK COMPUTER INC. NB1	Title : AC/BAT JACK	
	Engineer: Hawk	
Size: B	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 56 of 94	

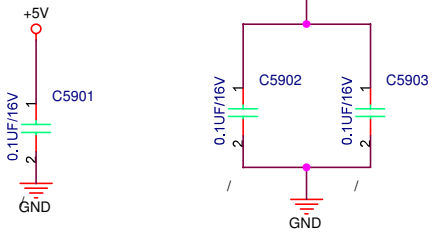






ASUSTeK COMPUTER INC. NB1	Title : +1.2VSUS	
	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 57 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 58 of 94	



ASUSTeK COMPUTER INC. NB1	Title : EMI	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 59 of 94	

1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.

2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#.

3. P7 unmount R706

4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]

5. P21 change R2121 to 0Ohm
   add R2124(33Ohm) for ACZ_RST# according to 968 ACT.
   add R2108/R2112(0Ohm) for PCIEPRSNT0/1 according to sis ACT
   ADD GMAC OSC25MHI to GND according to sis ACT.
   unmount L2103,mount L2105 according to spec.
   unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
   change GPIO17 from VIN4 to S_A20GATE, add R2127(0Ohm) for reserve SUSCLK

6.P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage

7. P22 change R2217 to 12KOhm, add C2237(22pF) for SATA REXT according to 968 ACT.

8. P24 add R2434 for A20GATE to H_A20M#,add R2457 for A20GATE to S_A20GATE,add R2456 to PU S_A20GATE

9. P29 add R2909/R2910(0Ohm), unmount L2901 for EMI.

10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .

    delete D3004 for DDR power are not SUS power,

    add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,

    Add R3019 for INSTANTON#

11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost

12. P37 mount R3716/Q3715 for +VCCP discharge

13. P42 change IDSEL to PCI_AD24

14.P46 add D4602 for VGA_RST#

15. P48 unmount L4803/R4809, delete L4801
    unmount R4806,mountQ4801/R4807/Q4802/R4808

16. P53 change L5335/L5338 to match the current.

17.P55 change X5501 to +-10ppm to follow spec,add C5508/C5509 to match X5501

18. P56 add C5609 for over current damaging charge IC.

19. P4 Change C440 from 0.1UF to 0.22UF

20. P10 change L1001 to 2A to match the current,, Add +1.2VS delay circuit.

21.P21 Add VGA_RST# to GPIO7, add R2140 for VGA_RST#.

22.P47 Unmount R4759,mount R4758 for Vram changed from 03G151236011 to 03G151236012.

F5VL

1. P2/3 change CPU socket to P
2. P32 delete R3205/R3212
3. P59 add C5902/C5903 for EMI

R2.0

1.P29 mount R2907, connect PCIE_PRSNT1 to CPPE#
  P21 unmount R2108, mount R2118, change R2118 from 0Ohm to 4.7KOhm but unmount R2118
2.P27 change R2708 to 0Ohm and mount it to not support C3 mode
3.P33&22 add two TPS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply
4.P21 add R2141 to connect OS#_OC to PM_THRMTRIP#, change R2141 to Q2101
5.P30 change C3009/C3003 to 6.8pF
6.P27 change C2706/C2707 to 24pF
7.P55 change C5508/C5509 to 22pF
8.P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301
9.P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3
10.P30 change Q3003 PU from +5V to +5VS
11.P5 unmount R506
12.P56 change R5601 to 20KOhm
13.P20 unmount R2054,add and mount C2010
  P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
  P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206
14.P27 change 4in1 cardreader
15.P47 mount R4704/R4705/R4706/R4707
  P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839,change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813
16.P21 Unmount L2105, mount L2103
17.P21 change R2116 from 330hm to 200hm, change R2117 from 330hm to 00hm, change R2119 from 330hm to 200hm
   P24 change R2418 from 330hm to 00hm, change R2420 from 330hm to 00hm, change R2419 from 330hm to 00hm, change R2422 from 330hm to 00hm, change R2423 from 330hm to 00hm, change R2425 from 330hm to 00hm
   P25 change R2514 from 330hm to 470hm

ASUSTeK COMPUTER INC. NB1

Title : BLANK

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
C	F5V	1.0

Date: 星期一, 八月 23, 2007 Sheet 60 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 61 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 62 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 63 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 64 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 65 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 66 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 67 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 68 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 69 of 94	

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 70 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 71 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 72 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 73 of 94	

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Kaxidy/Hawk

Size	Project Name	Rev
A	F5V	1.0

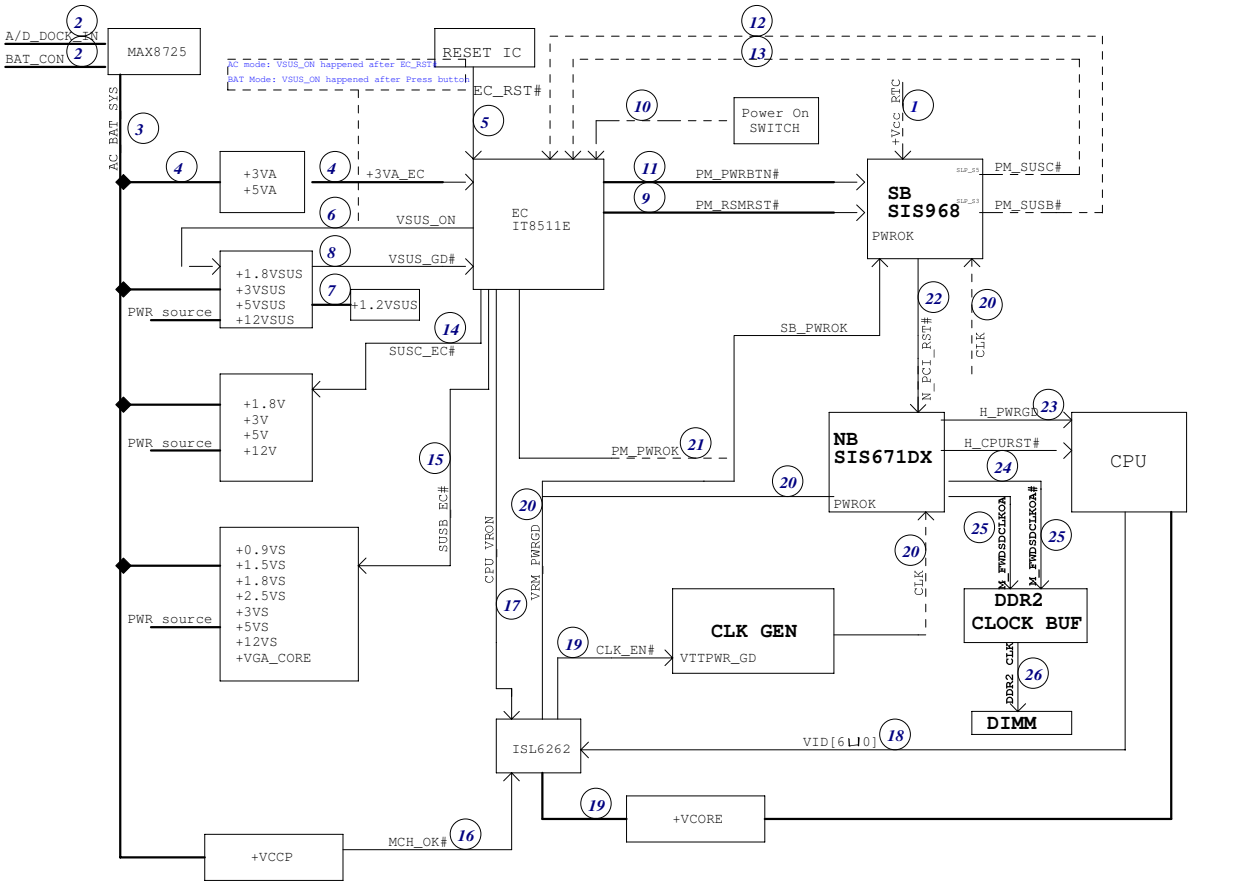
Date: 星期一, 四月 23, 2007 Sheet 74 of 94

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 75 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 76 of 94	

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: *Kaxidy/Hawk*	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 77 of 94	

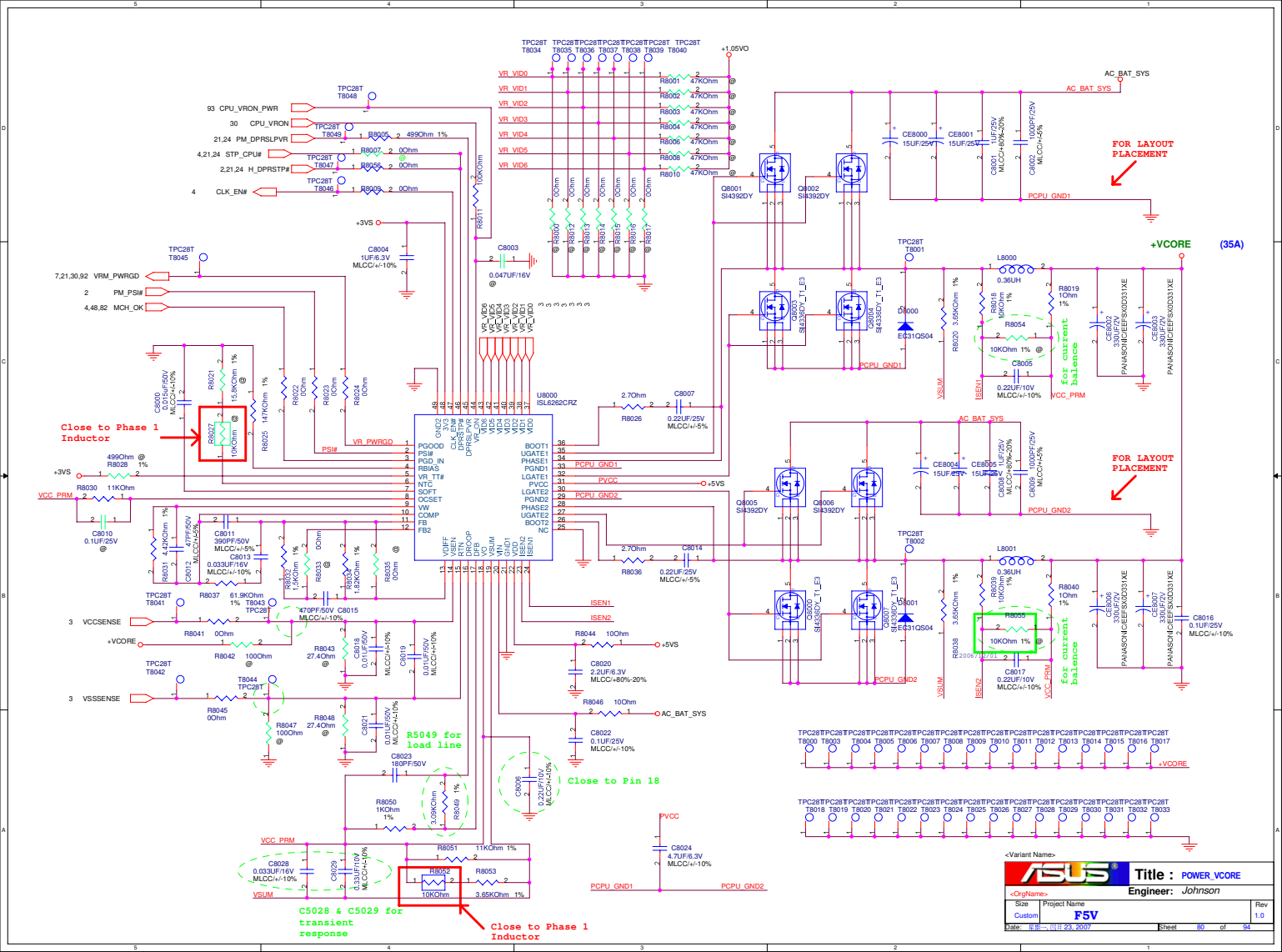
Title : BLANK		
ASUSTeK COMPUTER INC. NB1	Engineer: Kaxidy/Hawk	
Size: A	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 78 of 94	



Power On Sequence

1 — - - - — 26

ASUSTeK COMPUTER INC. NB1	Title : Power sequence		
	Engineer: Kaxidy/Hawk		
Size: C	Project Name: F5V		Rev: 1.0
Date: 星期一, 五月 23, 2007	Sheet 79 of 84		


+VCORE
(35A)
FOR LAYOUT PLACEMENT
for current balence
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
U8000 ISL6262CRZ
Q8001 SI4392DY
Q8002 SI4392DY
Q8003 SI4336DY_T1_E3
Q8004 SI4336DY_T1_E3
Q8005 SI4392DY
Q8006 SI4392DY
Q8007 SI4336DY_T1_E3
Q8008 SI4336DY_T1_E3
L8000 0.36UH
L8001 0.36UH
D8000 EG31QS04
D8001 EG31QS04
PCPU_GND1
PCPU_GND2
VCC_PRM
VSUM
ISEN1
ISEN2
PVCC
AC_BAT_SYS
+5VS
+3VS
+1.05VO
VR_PWRGD
PSI#
VCCSENSE
VSSSENSE
Title : POWER_VCORE
Engineer: Johnson
Project Name F5V
Rev 1.0
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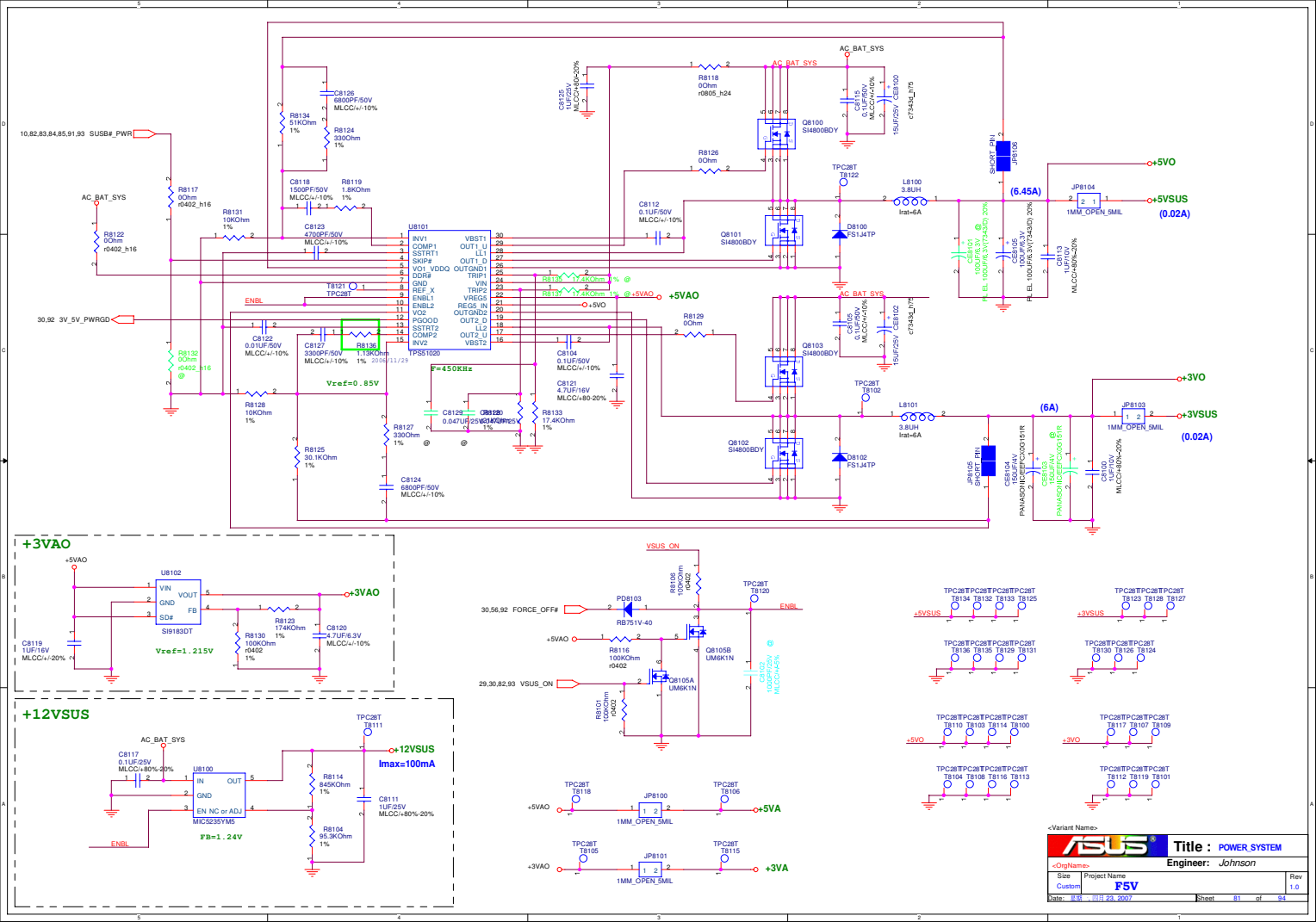
10,82,83,84,85,91,93 SUSB#_PWR
AC_BAT_SYS
30,92 3V_5V_PWRGD
ENBL
U8101
TPS51020
Vref=0.85V
F=450KHz
+5VAO
+5VO
+5VSUS
(0.02A)
(6.45A)
+3VO
+3VSUS
(0.02A)
(6A)
+3VAO
U8102
SI9183DT
Vref=1.215V
+12VSUS
Imax=100mA
U8100
MIC5235YM5
FB=1.24V
VSUS_ON
30,56,92 FORCE_OFF#
29,30,82,93 VSUS_ON
+5VA
+3VA
1MM_OPEN_5MIL
<Variant Name>
Title : POWER_SYSTEM
Engineer: Johnson
<OrgName>
Size Custom
Project Name F5V
Rev 1.0
Date: 星期一 四月 23, 2007
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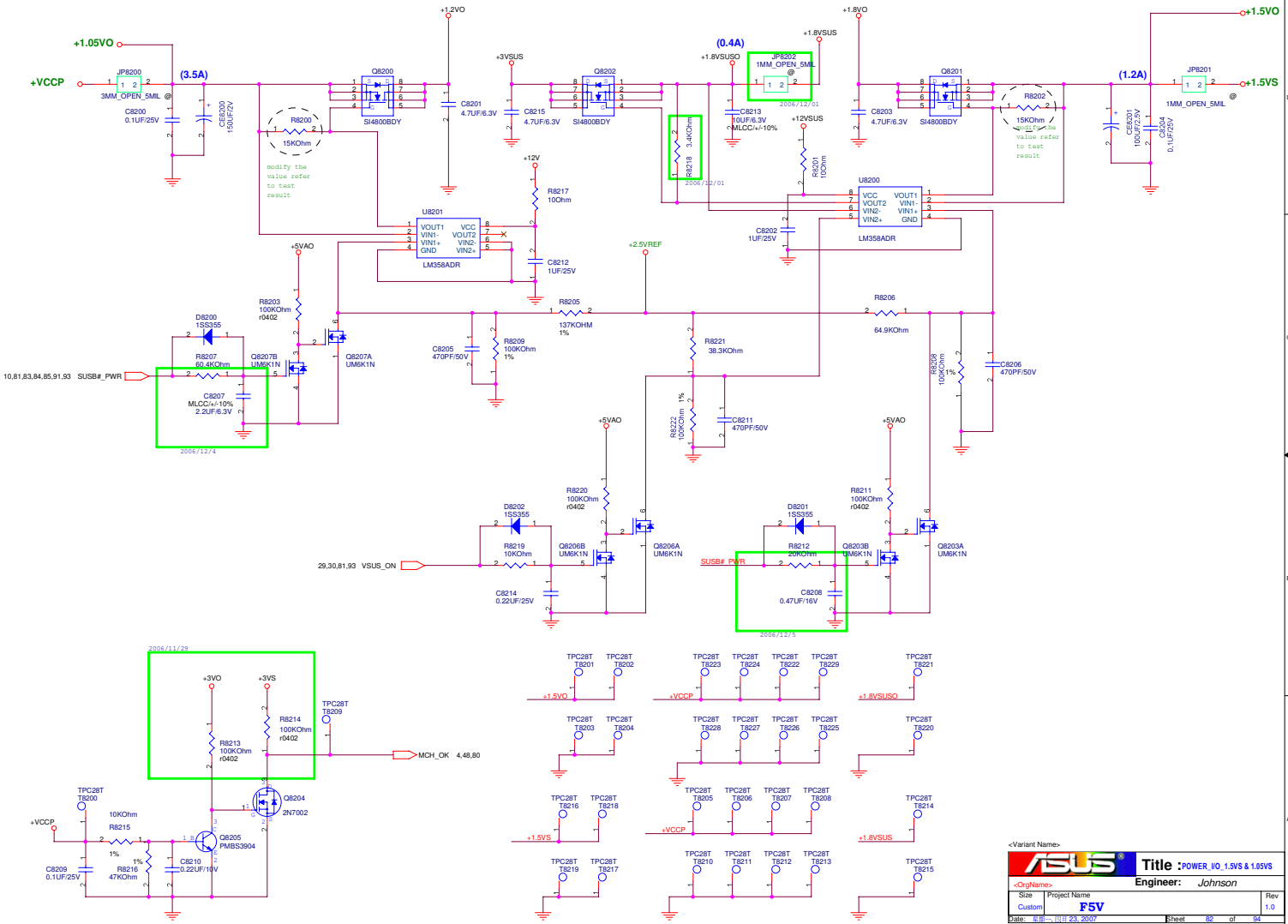
+1.05VO
+VCCP
JP8200
3MM_OPEN_5MIL
(3.5A)
C8200
0.1UF/25V
CE8200
150UF/2V
R8200
15KOhm
modify the value refer to test result
Q8200
SI4800BDY
+1.2VO
C8201
4.7UF/6.3V
+3VSUS
C8215
4.7UF/6.3V
Q8202
SI4800BDY
(0.4A)
+1.8VSUSO
JP8202
1MM_OPEN_5MIL
2006/12/01
+1.8VSUS
C8213
10UF/6.3V
MLCC/+/-10%
R8218
3.4KOhm
2006/12/01
+12VSUS
R8201
10Ohm
+1.8VO
C8203
4.7UF/6.3V
Q8201
SI4800BDY
R8202
15KOhm
modify the value refer to test result
(1.2A)
CE8230
100UF/6.3V
C8204
0.1UF/25V
JP8201
1MM_OPEN_5MIL
+1.5VO
+1.5VS
+12V
R8217
10Ohm
U8201
VOUT1
VIN1-
VIN1+
GND
VCC
VOUT2
VIN2-
VIN2+
LM358ADR
C8212
1UF/25V
U8200
LM358ADR
C8202
1UF/25V
+5VAO
+2.5VREF
R8203
100KOhm
r0402
D8200
1SS355
R8207
60.4KOhm
Q8207B
UM6K1N
Q8207A
UM6K1N
10,81,83,84,85,91,93 SUSB#_PWR
C8207
MLCC/+/-10%
2.2UF/6.3V
2006/12/4
C8205
470PF/50V
R8209
100KOhm
1%
R8805
137KOHM
1%
R8206
64.9KOhm
R8221
38.3KOhm
R8208
100KOhm
1%
C8206
470PF/50V
R8222
105KOhm
1%
C8211
470PF/50V
R8220
100KOhm
r0402
D8202
1SS355
R8219
10KOhm
Q8206B
UM6K1N
Q8206A
UM6K1N
29,30,81,93 VSUS_ON
C8214
0.22UF/25V
R8211
100KOhm
r0402
D8201
1SS355
R8212
20KOhm
Q8203B
UM6K1N
Q8203A
UM6K1N
SUSB# PWR
C8208
0.47UF/16V
2006/12/5
2006/11/29
+3VO
+3VS
R8214
100KOhm
r0402
R8213
100KOhm
r0402
TPC28T
T8209
MCH_OK 4,48,80
Q8204
2N7002
TPC28T
T8200
+VCCP
10KOhm
R8215
1%
C8209
0.1UF/25V
R8216
47KOhm
C8210
0.22UF/10V
Q8205
PMBS3904
TPC28T T8201 T8202 +1.5VO
TPC28T T8223 T8224 T8222 T8229 +VCCP
TPC28T T8221 +1.8VSUSO
TPC28T T8203 T8204
TPC28T T8228 T8227 T8226 T8225
TPC28T T8220
TPC28T T8216 T8218 +1.5VS
TPC28T T8205 T8206 T8207 T8208 +VCCP
TPC28T T8214 +1.8VSUS
TPC28T T8219 T8217
TPC28T T8210 T8211 T8212 T8213
TPC28T T8215
<Variant Name>
<OrgName>
Title : POWER_I/O_1.5VS & 1.05VS
Engineer: Johnson
Size Custom
Project Name F5V
Rev 1.0
Date: 星期一, 四月 23, 2007
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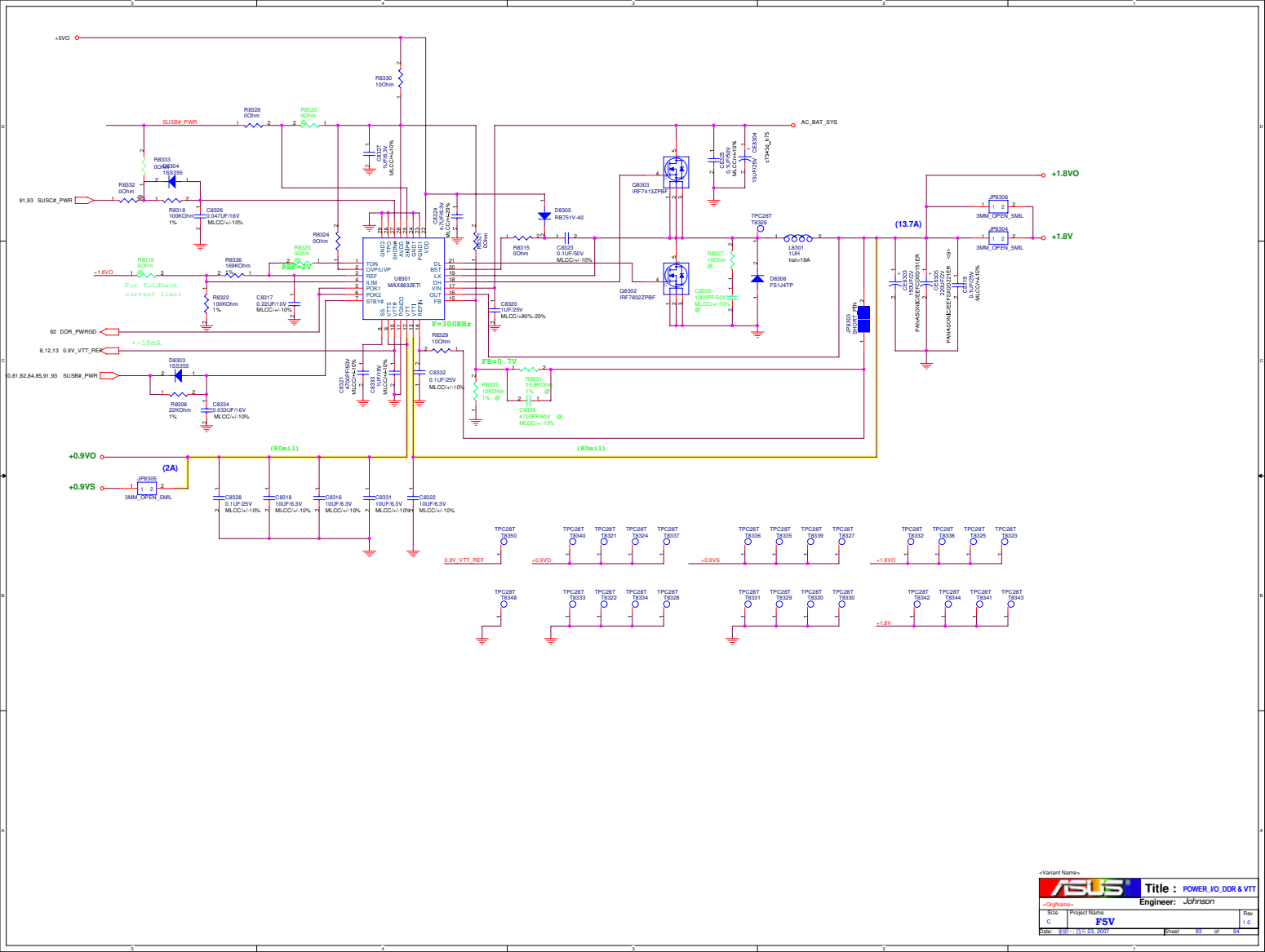
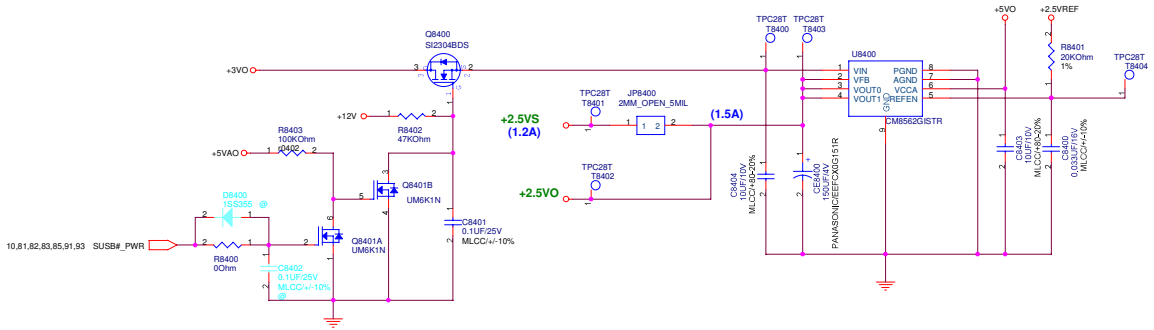


<Variant Name>

Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer: Johnson	
Size: C	Project Name: F5V	Rev: 1.0
Date: 월 6, 11 H 23, 2007	Sheet: 83 of 94	

+2.5VS



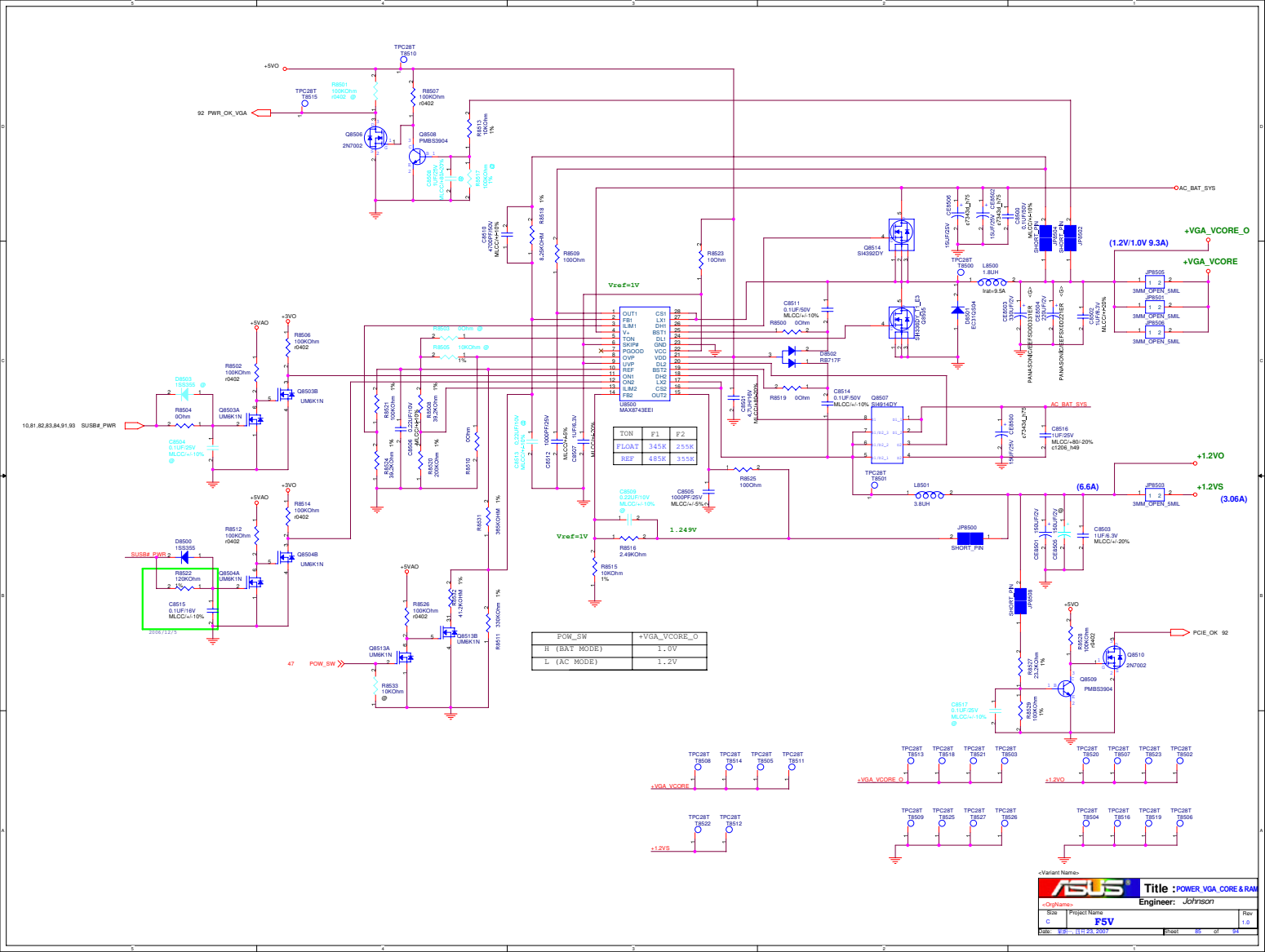
<Variant Name>

<OrgName>
Engineer: Johnson

Title : POWER_I/O_+3VA & +2.5V

Size	Project Name	Rev
Custom	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 84 of 94



<Variant Name>

ASUS

Title : POWER_VGA_CORE & RAM

Engineer: Johnson

<OrgName>

Size	Project Name	Rev
C	F5V	1.0

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<Variant Name>

Title : N/A

<OrgName>

Engineer: Johnson

Size	Project Name	Rev
B	F5V	1.0

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<Variant Name>

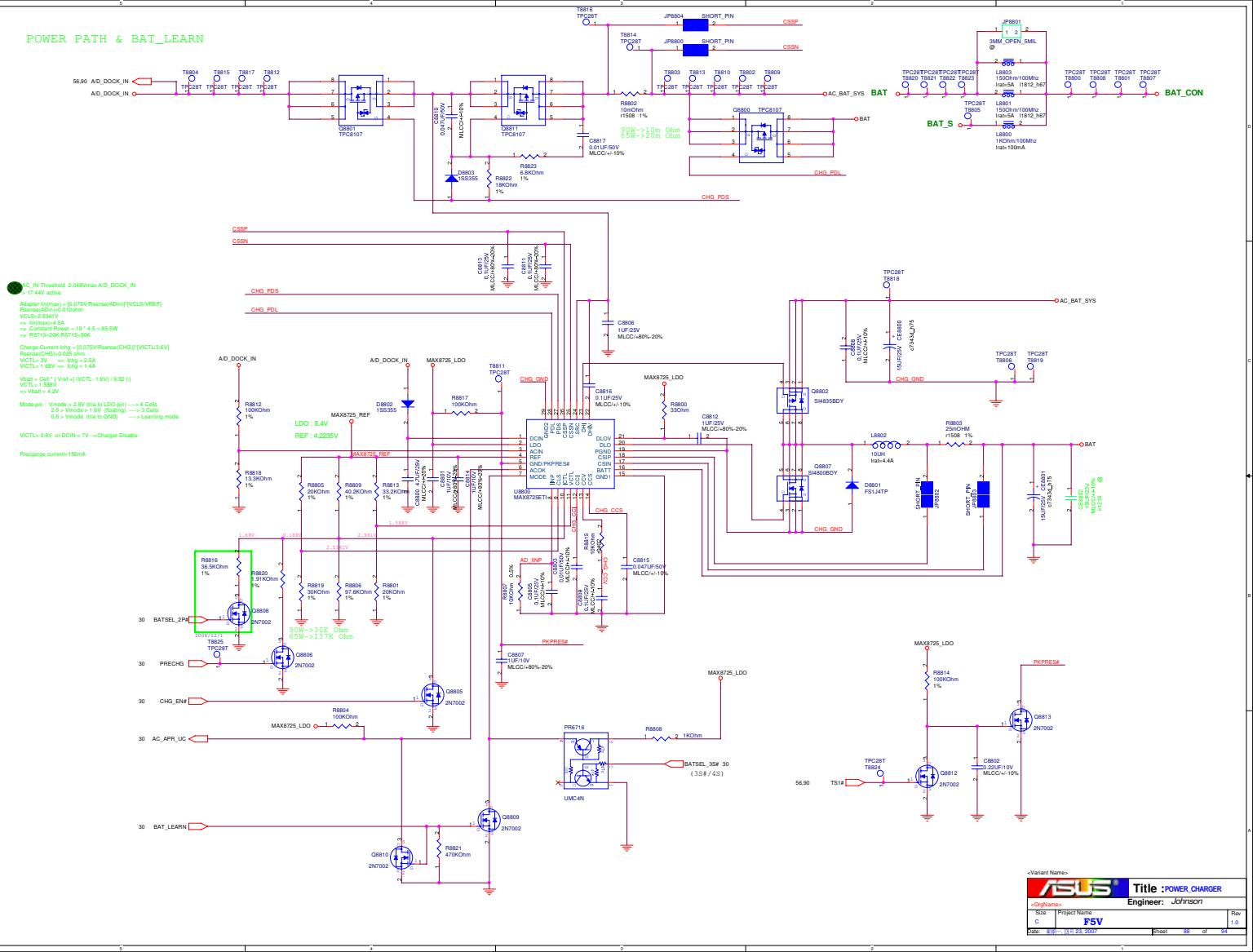
Title : N/A

<OrgName>

Engineer: Johnson

Size	Project Name	Rev
Custom	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 87 of 94


POWER PATH & BAT_LEARN
AC_IN Threshold 2.048V/max A/D_DOCK_IN > 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01ohm
VCLS=2.534V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R5710=20K,R5715=30K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTU/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VCTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
A/D_DOCK_IN
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
CHG_PDS
CHG_PDL
CHG_GND
CSSP
CSSN
AC_BAT_SYS
BAT
BAT_CON
BAT_S
PKPRES#
AD_INP
CHG_CCS
BATSEL_2S#
PRECHG
CHG_EN#
AC_APR_UC
BAT_LEARN
BATSEL_3S# 30
(3S#/4S)
TS1#
90W->10m Ohm
65W->20m Ohm
90W->30K Ohm
65W->137K Ohm
<Variant Name>
Title : POWER_CHARGER
Engineer: Johnson
<OrgName>
Size C
Project Name F5V
Rev 1.0
Date 年6月 11日 23, 2007
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<Variant Name>

Title : N/A

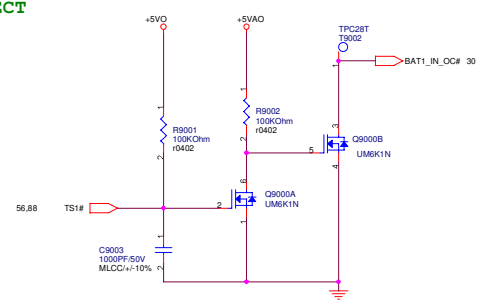
<OrgName>

Engineer: Johnson

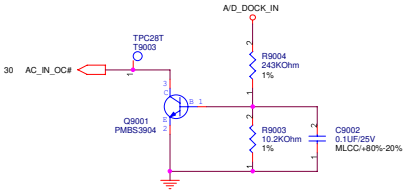
Size	Project Name	Rev
Custom	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 89 of 94

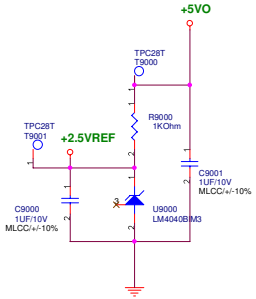
BATTERY IN DETECT



ADAPTER IN DETECT



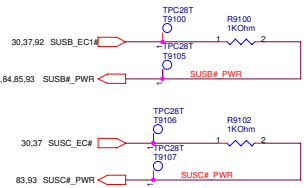
+2.5VREF

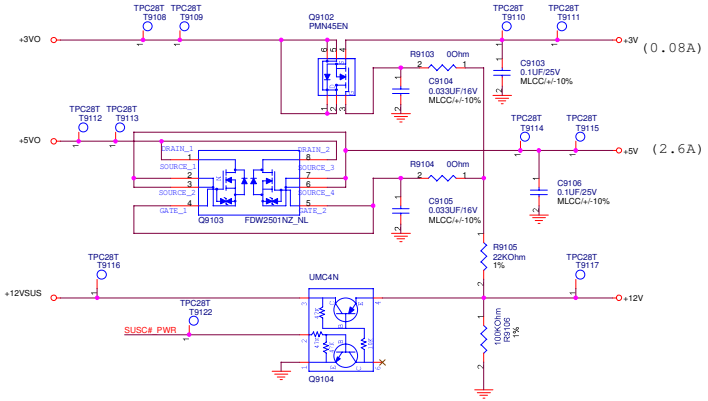


<Variant Name>

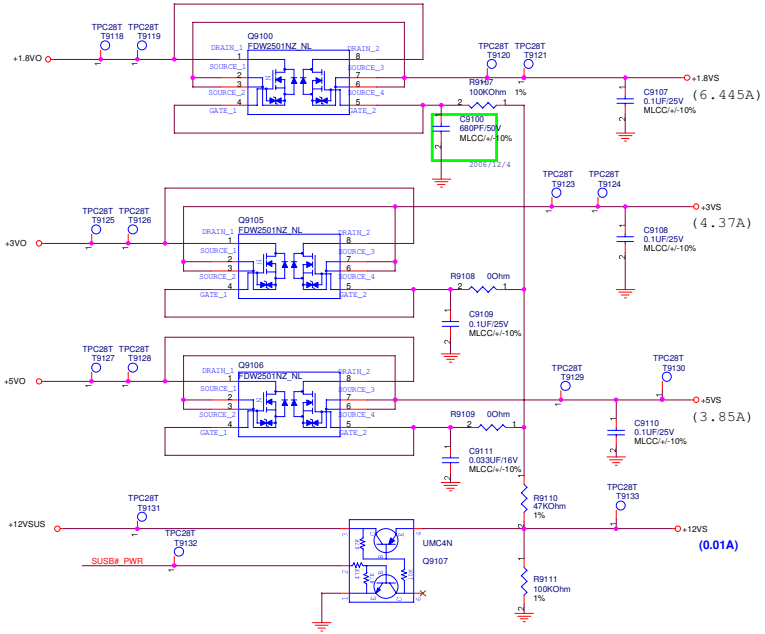
<OrgName>	Title : POWER_DETECT	
	Engineer: Johnson	
Size: Custom	Project Name: F5V	Rev: 1.0
Date: 星期一, 四月 23, 2007	Sheet 90 of 94	

SUSC#_STAGE POWER





SUSB#_PWR POWER



<Variant Name>

Title : POWER_LOAD SWITCH

<OrgName>

Engineer: Johnson

Size	Project Name	Rev
Custom	F5V	1.0

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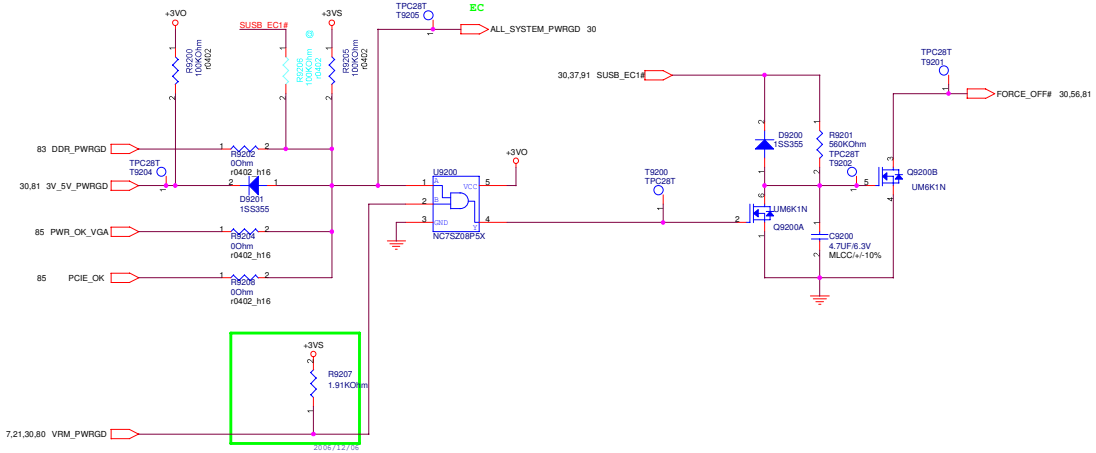
POWER GOOD DETECTER



<Variant Name>

<OrgName>

Title : POWER_PROTECT

Engineer: Johnson

Size	Project Name	Rev
Custom	F5V	1.0

Date: 星期一, 四月 23, 2007 Sheet 92 of 94

AC_BAT_SYS → AC_BAT_SYS 17,56,80,81,83,85,88

+3VA → +3VA 5,17,21,30,31,37,81

+5VA → +5VA 10,81

+5VO → +5VO 34,81,83,84,85,90,91

+3VO → +3VO 81,82,84,85,91,92

+3VSUS → +3VSUS 8,9,19,20,21,22,23,24,29,30,33,34,36,38,42,57,81,82

+5VSUS → +5VSUS 24,33,57,81

+3V → +3V 2,7,17,19,21,23,24,33,36,37,38,40,91

+3VS → +3VS 2,4,5,7,12,13,17,18,19,20,21,22,23,24,25,26,29,30,31,32,37,40,46,47,48,52,53,55,80,82,91,92

+12VSUS → +12VSUS 10,81,82,91

+12V → +12V 37,82,84,91

+12VS → +12VS 17,26,37,91

+5V → +5V 17,26,27,33,37,59,91

+5VS → +5VS 5,18,25,26,30,31,32,34,37,38,42,52,55,80,91

+2.5VO → +2.5VO 84

+2.5VS → +2.5VS 37,53,84

+1.8VO → +1.8VO 82,83,91

+1.8VSUS → +1.8VSUS 10,21,22,23,57,82

+1.8V → +1.8V 8,10,12,13,15,37,83

+1.8VS → +1.8VS 6,7,8,10,14,20,21,22,23,37,48,49,51,52,53,91

+1.5VS → +1.5VS 3,19,29,37,82

+VCCP → +VCCP 2,4,6,7,10,23,24,37,82

+0.9VS → +0.9VS 15,37,83

BAT → BAT 88

+2.5VREF → +2.5VREF 82,84,90

+VCORE → +VCORE 3,80

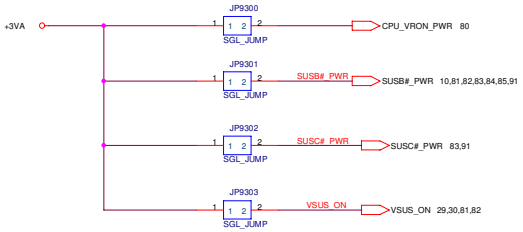
+VGA_VCORE → +VGA_VCORE 48,52,53,85

+1.2VO → +1.2VO 82,85

+1.2VS → +1.2VS 10,37,53,85

BAT_CON → BAT_CON 56,88

FOR POWER TEST



CHANGE LIST

2006/11/29	1. Pull high R8213 to +3VO , 2. change C8334 to 0.1uF, 3.change R8136 to 1.13KOhm
2006/12/01	1. change R8218 to 3.4KOhm, 2. add JP8202, 3. delete R8055, 4.add Q8808 & R8816
2006/12/04	1. change C8207 to 2.2uF & R8207 to 60.4KOhm , 2. delete R8055, 3.change C9910 to 680pF
2006/12/05	1. change C8208 to 0.47uF & R8212 to 20KOhm. 2. change C8515 to 0.1uF & R8522 to 120KOhm.
2006/12/05	1.change R9207 to 1.91KOhm
2007/01/12	1. change input cap footprint. 2. add necessary TP.
2007/01/30	1. C8207 to 2.2uF/6.3V

<Variant Name>

<OrgName>
Engineer: Johnson

Title : POWER_SIGNAL

Size	Project Name	Rev
Custom	P5V	1.0

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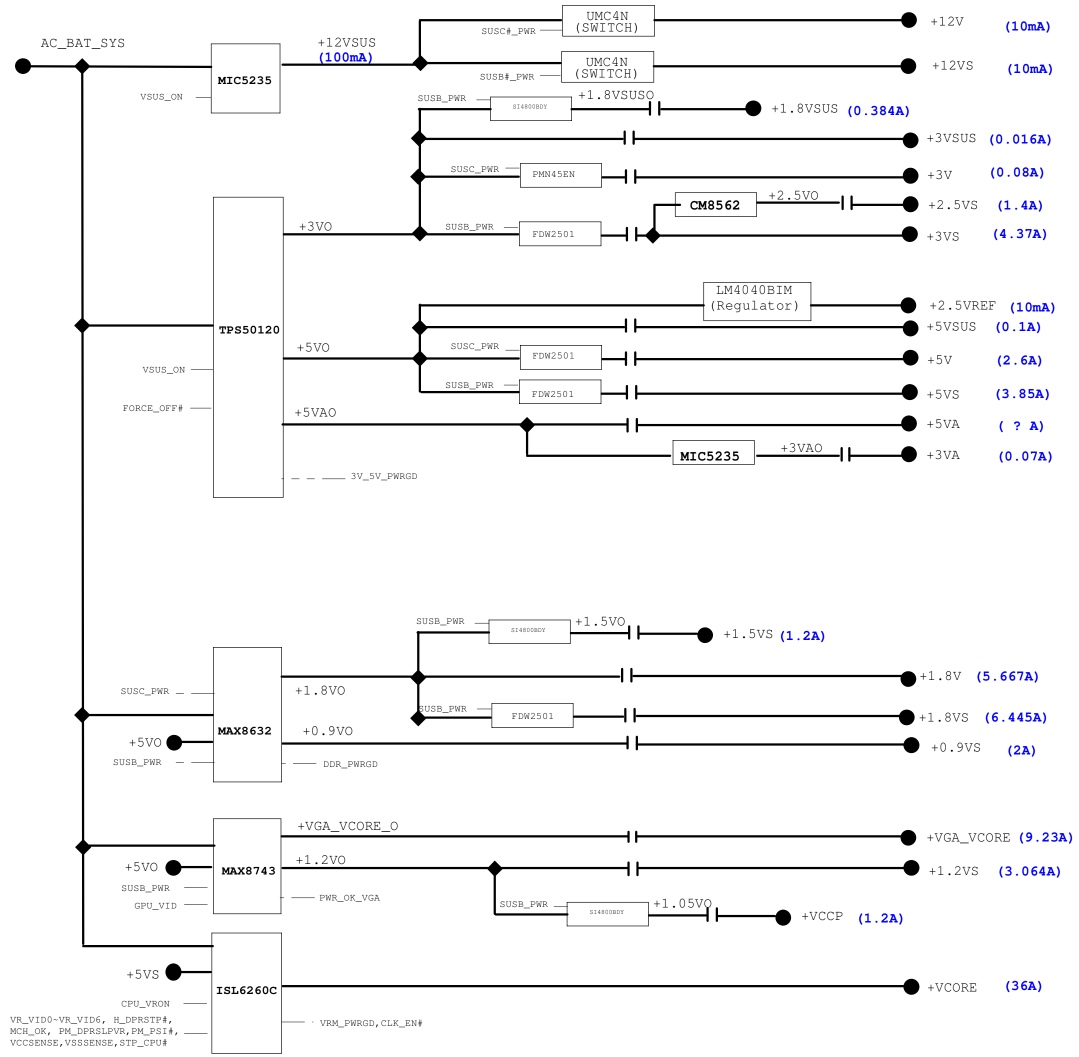

<Variant Name>

Title : POWER_FLOWCHART

<OrgName>

Engineer: *Johnson*

Size	Project Name	Rev
Custom	F5V	1.0

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