F6E SCHEMATIC Revision 1.10

SYSTEM PAGE REF.

POWER PAGE REF.

<Variant Name>

ASUSTeK COMPUTER INC

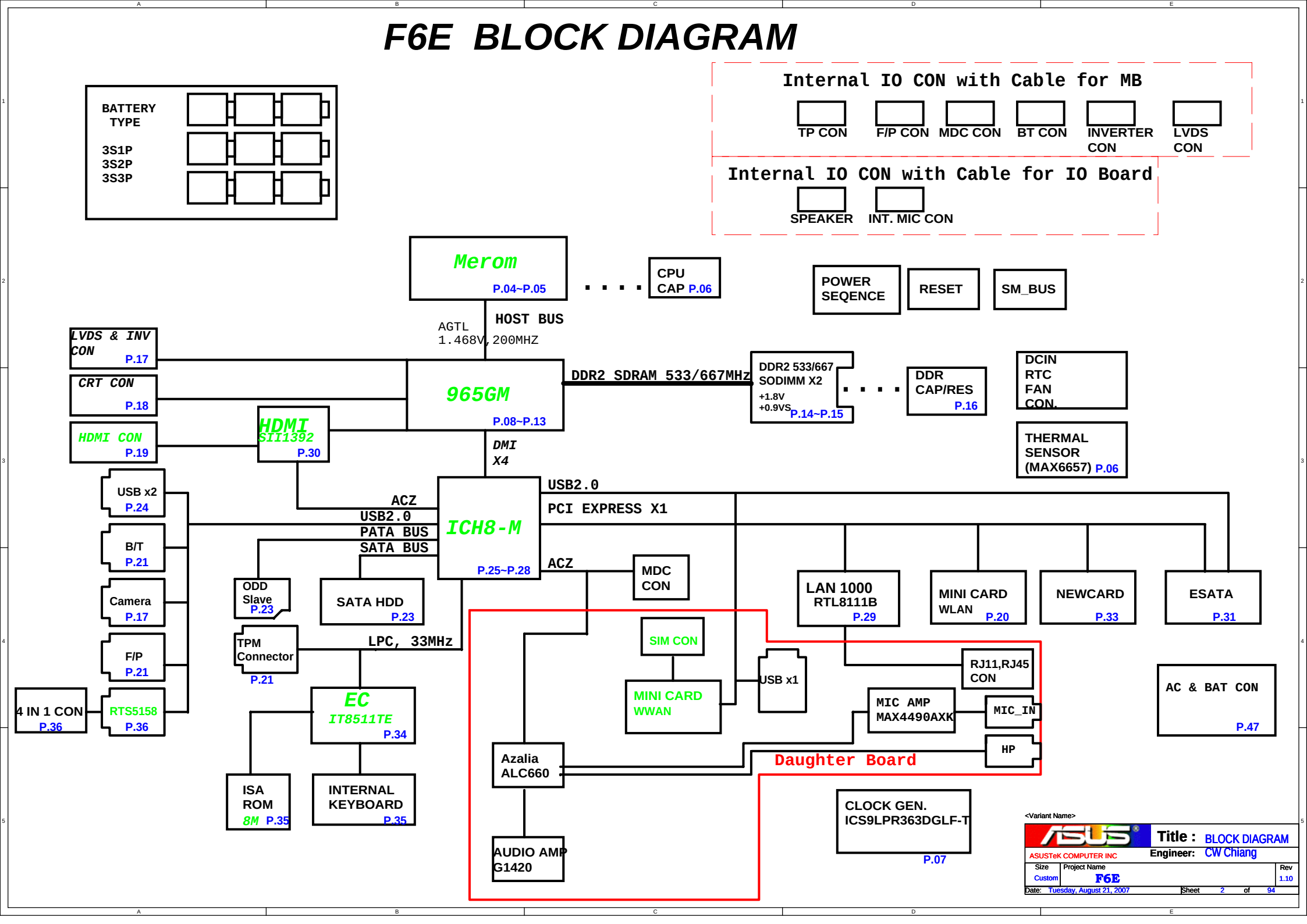
Title : PAGE REF.

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 1 of 94

F6E BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 2 of 94

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	PWRLIMIT#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/0
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

ICH8M_GPIO

Pin.	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 00	i		GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	0	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i	H-Z	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	0	GPO	BIOS_REC_?_(TP)	+3VS	TACH2
GPIO 07	i	0	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i		GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i	H-Z	GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i	H-Z	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat.	H-Z	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i		GPI	KBC_SCI#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat.		GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	H-Z	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat.	1	Native	STP_PCI#	+3VSUS	STP_PCI# , No-GPIO, in Mobile
GPIO 16	Nat.	0	Native	PM_DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	1	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O	freq 1K	GPO	N/A	+3VS	N/A
GPIO 19	i		GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i		GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i		GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat.		Native	N/A	+3VS	LDRQ1#
GPIO 24	O	H-Z	GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED) , Not Cleared by CF9h RST event.
GPIO 25	Nat.	1	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO, in Mobile
GPIO 26	Nat.		GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	0	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	0	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat.		Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat.		Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat.		Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	0	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO, in Mobile
GPIO 33	O	1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	0	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i		GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i	0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i		GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 39	i		GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat.		Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a		N/A	N/A	N/A	No implement
GPIO 48	i	1	Native		+3VS	SDATAOUT1
GPIO 49	Nat.		Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat.		Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat.	1	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat.		Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat.	1	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat.		Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat.	1	Native	PCI_GNT3#	+3VS	GNT3#

<Variant Name>

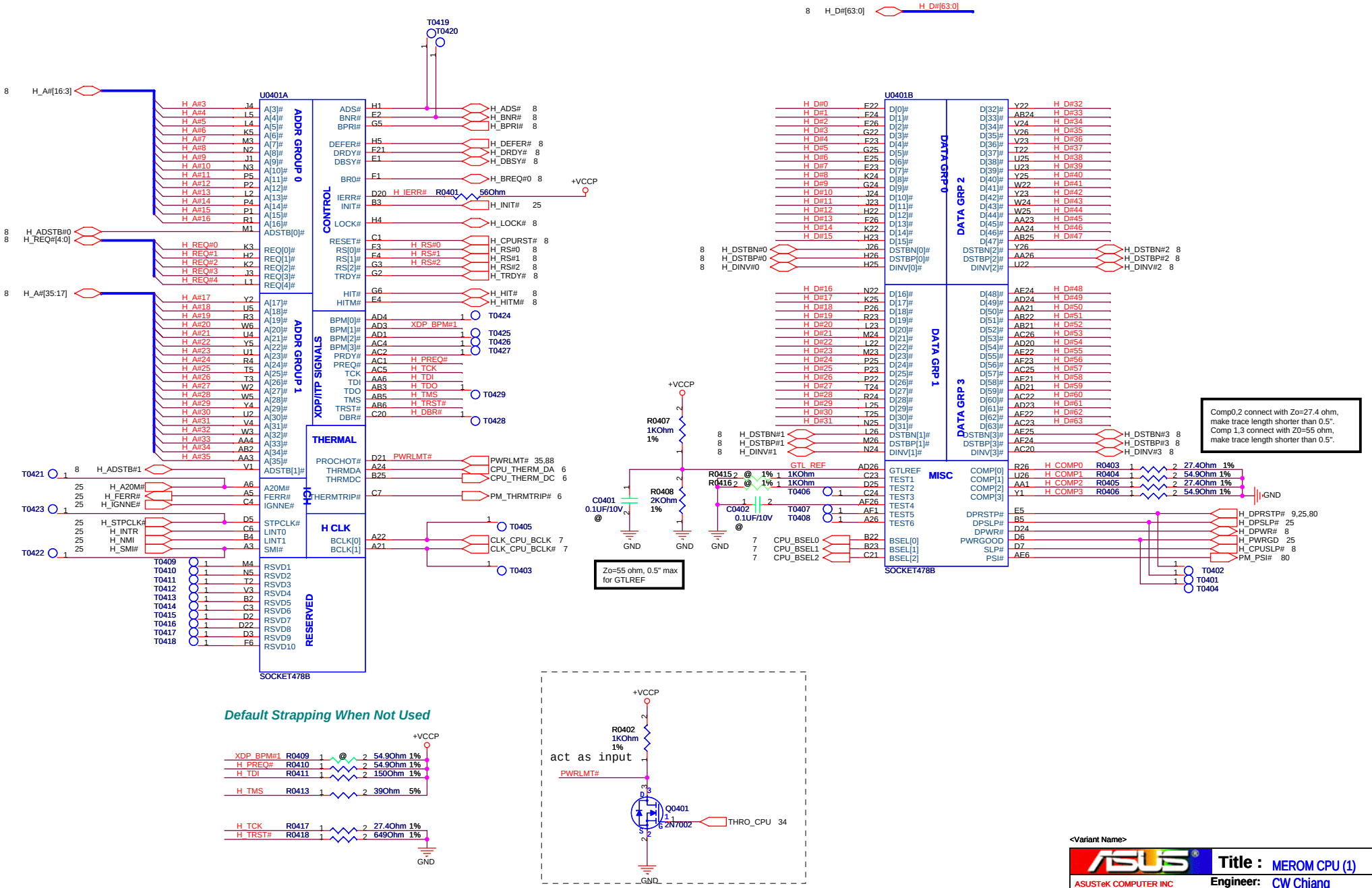
ASUSTeK COMPUTER INC

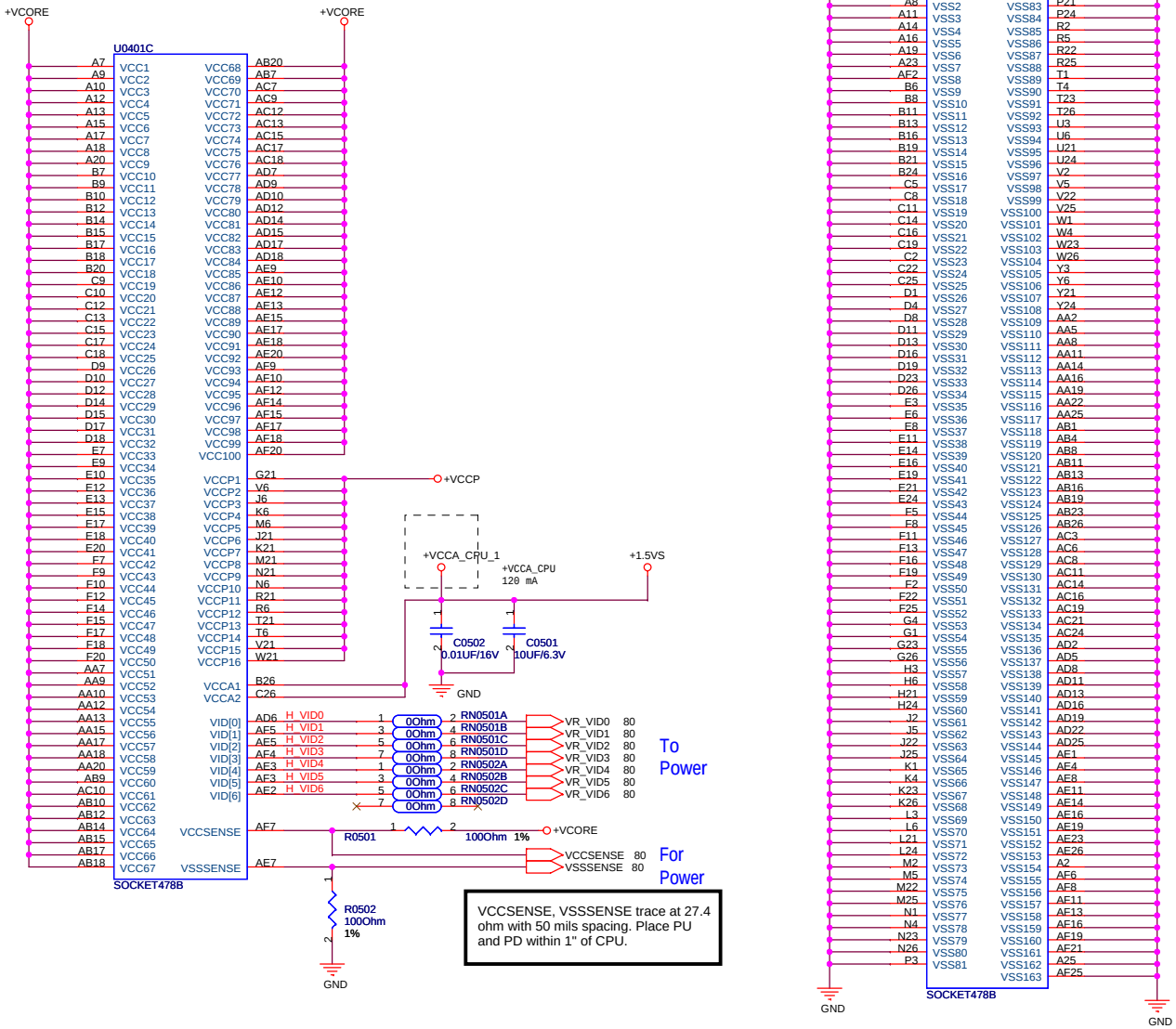
Title : Schematic Info.

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 3 of 94


U0401A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
SOCKET478B
U0401B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
SOCKET478B
H_A#[16:3]
H_A#[35:17]
H_ADSTB#0
H_REQ#[4:0]
H_ADSTB#1
H_D#[63:0]
T0419
T0420
H_ADS# 8
H_BNR# 8
H_BPRI# 8
H_DEFER# 8
H_DRDY# 8
H_DBSY# 8
H_BREQ#0 8
H_IERR# R0401 56Ohm +VCCP
H_INIT# 25
H_LOCK# 8
H_CPURST# 8
H_RS#0 8
H_RS#1 8
H_RS#2 8
H_TRDY# 8
H_HIT# 8
H_HITM# 8
XDP_BPM#1
H_PREQ#
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#
H_DBR#
T0424
T0425
T0426
T0427
T0429
T0428
PWRLMT# 35,88
CPU_THERM_DA 6
CPU_THERM_DC 6
PM_THRMTRIP# 6
T0405
CLK_CPU_BCLK 7
CLK_CPU_BCLK# 7
T0403
T0421
T0423
T0422
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
T0409
T0410
T0411
T0412
T0413
T0414
T0415
T0416
T0417
T0418
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2 8
H_DSTBP#2 8
H_DINV#2 8
H_DSTBN#3 8
H_DSTBP#3 8
H_DINV#3 8
R0407 1KOhm 1%
R0408 2KOhm 1%
C0401 0.1UF/10V @
C0402 0.1UF/10V @
GTL_REF
R0415 1KOhm 1%
R0416 1KOhm 1%
T0406
T0407
T0408
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
Zo=55 ohm, 0.5" max for GTLREF
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".
R0403 27.4Ohm 1%
R0404 54.9Ohm 1%
R0405 27.4Ohm 1%
R0406 54.9Ohm 1%
H_DPRSTP# 9,25,80
H_DPSLP# 25
H_DPWR# 8
H_PWRGD 25
H_CPUSLP# 8
PM_PSI# 80
T0402
T0401
T0404
Default Strapping When Not Used
XDP_BPM#1 R0409 54.9Ohm 1%
H_PREQ# R0410 54.9Ohm 1%
H_TDI R0411 150Ohm 1%
H_TMS R0413 39Ohm 5%
H_TCK R0417 27.4Ohm 1%
H_TRST# R0418 649Ohm 1%
act as input
PWRLMT#
R0402 1KOhm 1%
Q0401 2N7002
THRO_CPU 34
<Variant Name>
Title : MEROM CPU (1)
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 4 of 94



<variant_name>

ASUSTeK COMPUTER INC	Title : MEROM CPU (2)	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 5 of 94	

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom

+VCORE

C0614 10UF/6.3V, C0632 10UF/6.3V, C0621 10UF/6.3V, C0603 10UF/6.3V, C0625 10UF/6.3V, C0609 10UF/6.3V, C0631 10UF/6.3V, C0604 10UF/6.3V, C0622 10UF/6.3V, C0629 10UF/6.3V

C0627 10UF/6.3V, C0620 10UF/6.3V, C0626 10UF/6.3V, C0607 10UF/6.3V, C0624 10UF/6.3V, C0605 10UF/6.3V, C0623 10UF/6.3V, C0601 10UF/6.3V, C0615 10UF/6.3V, C0602 10UF/6.3V

C0616 10UF/6.3V, C0639 10UF/6.3V, C0619 10UF/6.3V, C0610 10UF/6.3V, C0613 10UF/6.3V, C0608 10UF/6.3V, C0612 10UF/6.3V, C0617 10UF/6.3V, C0628 10UF/6.3V, C0630 10UF/6.3V

C0611 10UF/6.3V, C0633 10UF/6.3V

GND

+VCCP Decoupling Capacitor (Place near CPU)

+VCCP

CE0601 150UF/4V, C0618 0.1UF/16V X7R, C0606 0.1UF/16V X7R, C0636 0.1UF/16V X7R, C0635 0.1UF/16V X7R, C0638 0.1UF/16V X7R, C0637 0.1UF/16V X7R

GND

Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it !_0907

Thermal Sensor

+3VS

SMB1_CLK 1 R0658 2 4.7KOhm

SMB1_DAT 1 R0657 2 4.7KOhm

THRM_ALERT#_CPU 1 R0650 2 10KOhm

+3VS_THM

R0656 200 +3VS

C0652 0.1U

Max: 1mA

U0650 MAX6657MSA

VCC, DXP, DXN, OVERT#, SCLK, SMB1_CLK, SMB1_DAT, ALERT#, THRM_ALERT#_CPU, GND

4 CPU_THERM_DA

4 CPU_THERM_DC

SMB1_CLK 34

SMB1_DAT 34

T0601

CPU_THERM_DA

CPU_THERM_DC

C0651 1000P

OS#_OC

OS#_OC 34

+3VS R617 10KOhm

Q0605 PMBS3904

OS#OC

Max6657: 0.26(USD)

ADT7401ARMZ: 0.28(USD)

Close to Pin A24 & A25 of CPU

Enable: Turn OFF system

Slave address: 98h

H/W Thermal Protect

+5VA

(94~98'C protect)

R0670 22.1K 1%

RT0671 100K

C0670 0.1U

U0670 PST9013NR

NC, SUB, GND, VCC, VOUT

+5VA R0660 4.7KOhm

FORCE_OFF# 34,81,92

Enable: Turn OFF system

OPEN Collect

Sub-SYS=CPU

34 FAN_PWM

+3VS R0602 100KOhm

Q0653B UM6K1N

Sub-SYS=FAN

+3VS R0601 100KOhm @

+5VSFAN R0603 10KOhm @

Q0653A UM6K1N

C0654 100PF/50V @

+3VS R0659 10KOhm

D0602 1N4148WS

34 FAN0_TACH

C0653 100PF/50V @

+5VS_FAN

D0603 BAT54C @

R6005 0Ohm

C0671 0.1UF/10V

CE0602 47UF/6.3V

+5VSFAN D0601 1N4148WS @

P/N:12G17000004B

CON601 WtoB_49

SIDE1, SIDE2

R0651 @ 0Ohm ICH_THRMTRIP# 25

+VCCP R0671 56Ohm

+VCCP R0652 330

+3VS R0654 10KOhm

C0650 0.1U

Enable: Turn OFF system

To EC(Internal Pull Hi)

4 PM_THRMTRIP#

9 GMCH_THRMTRIP#

9,23,26 PLT_RST#

R0655 0Ohm

Q0650 PMBS3904

Q0651 H2N7002

THRMTRIP# 34

To EC

<Variant Name>

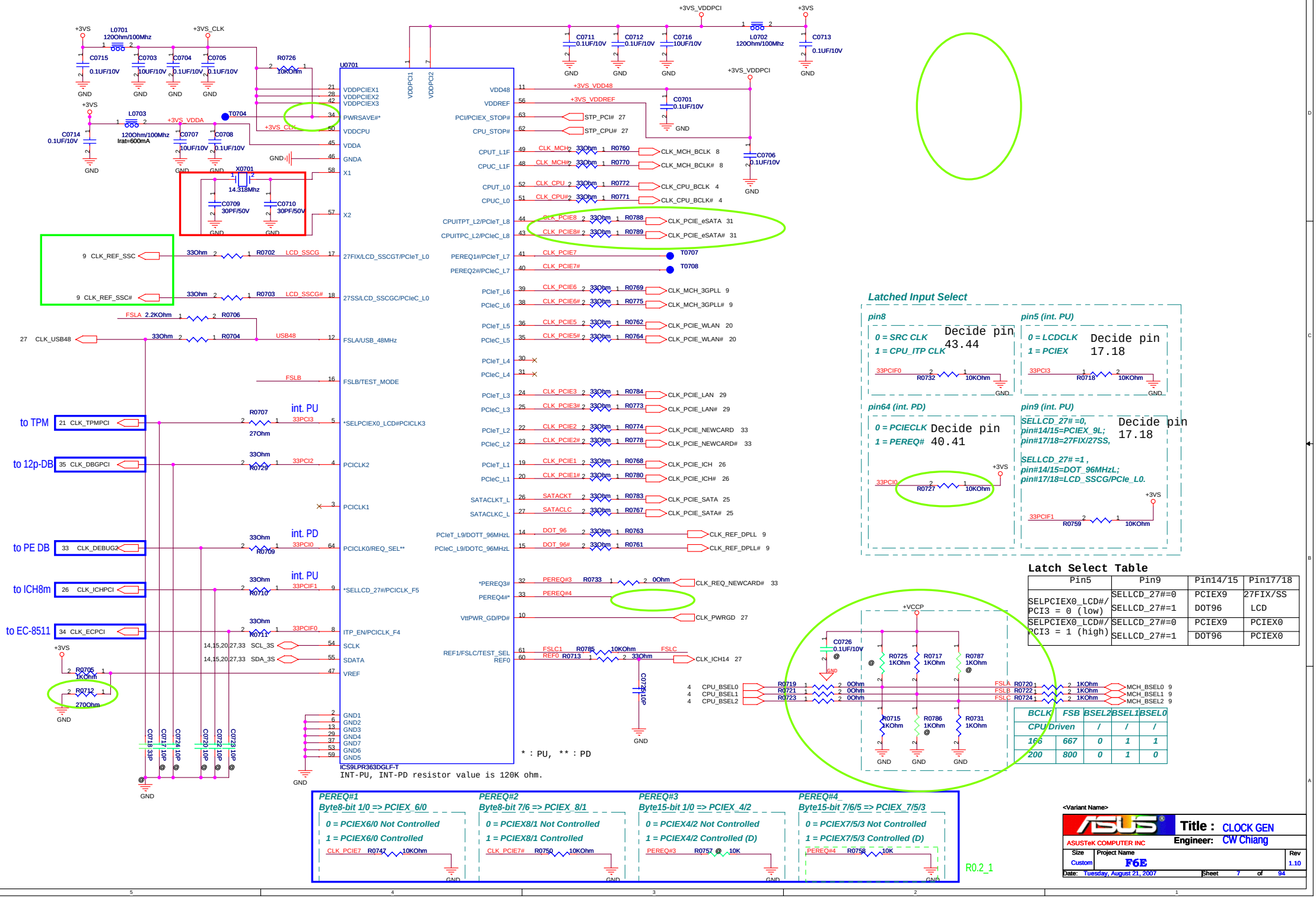
ASUSTeK COMPUTER INC

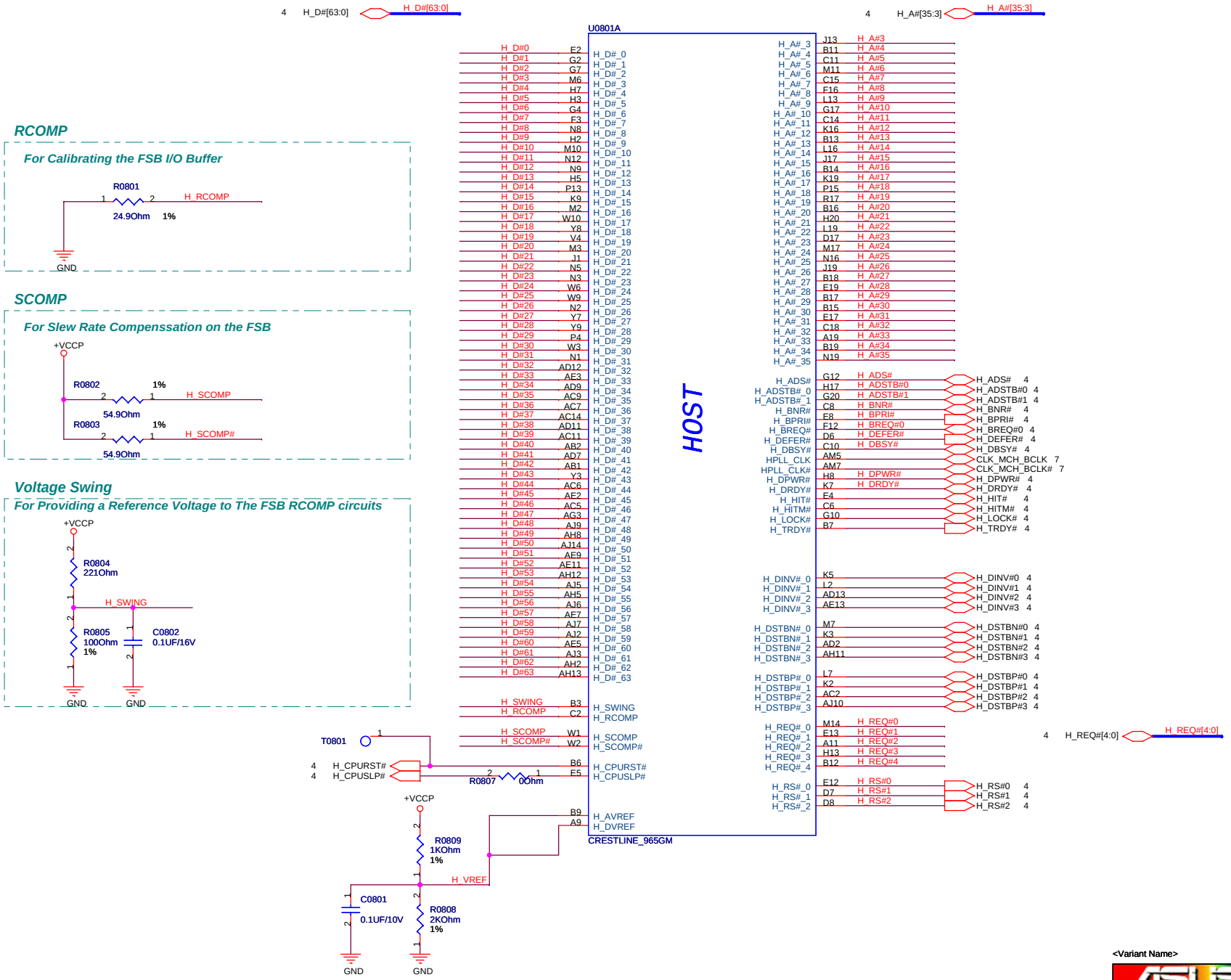
Title : CPU CAP, Thermal Senor

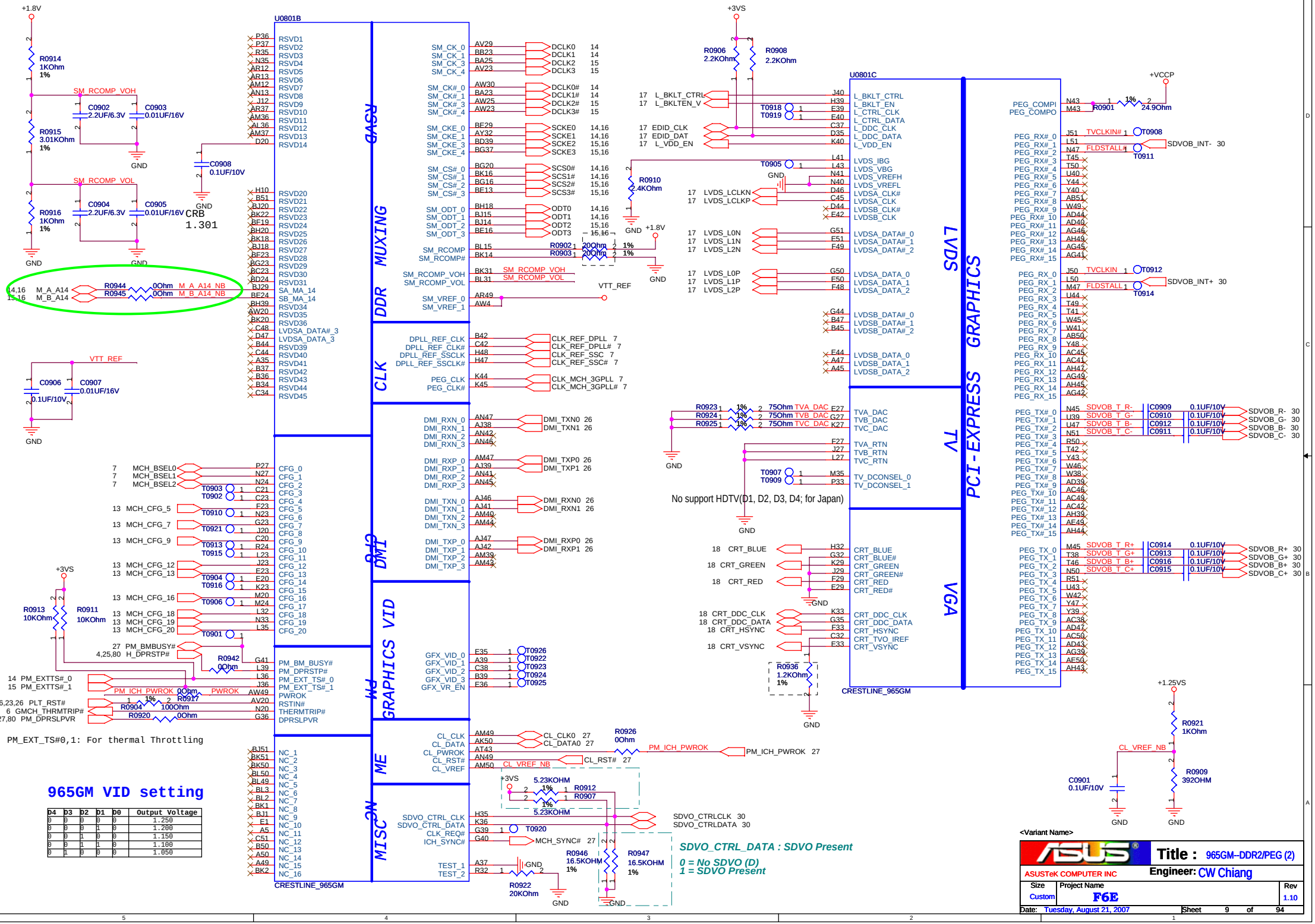
Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

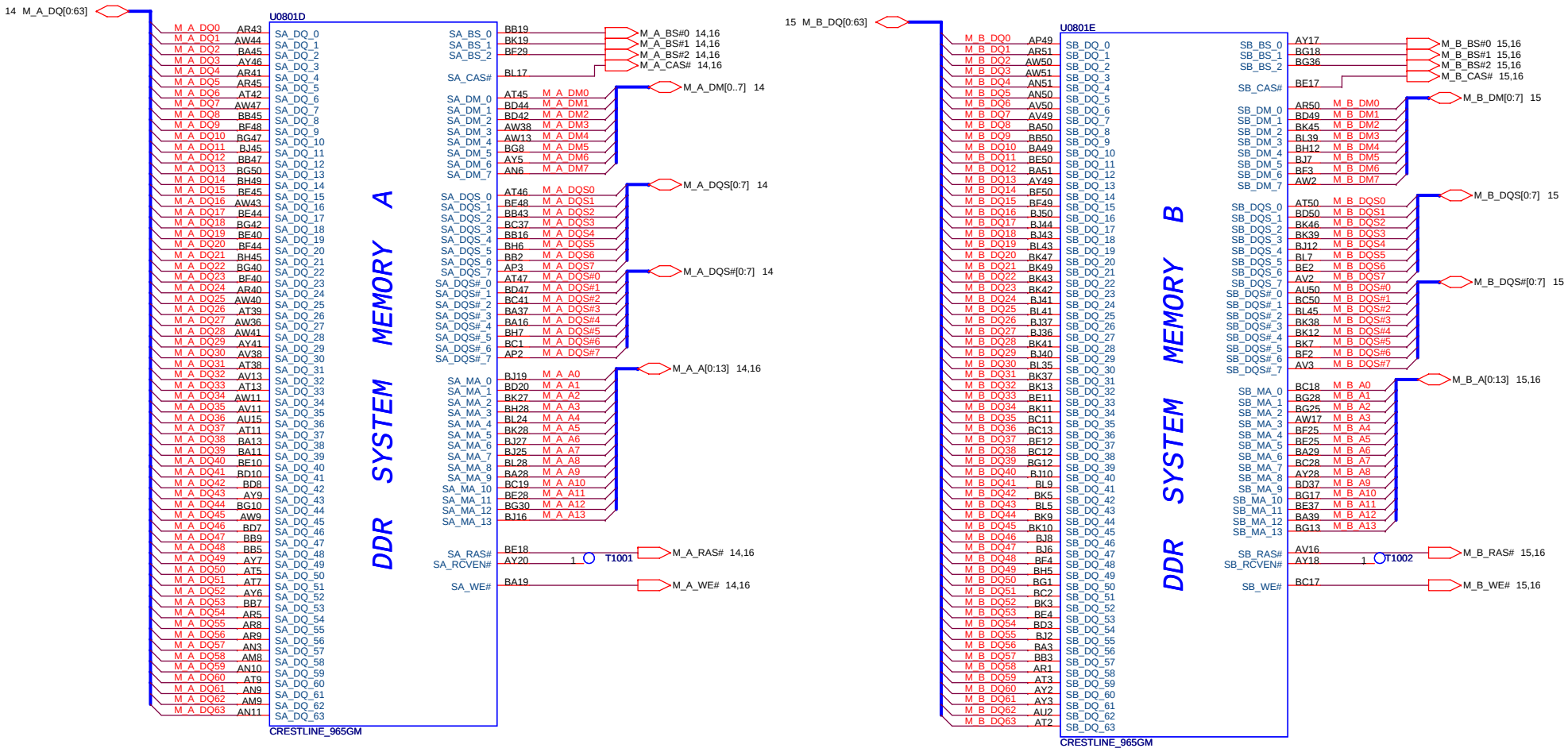
Date: Tuesday, August 21, 2007 Sheet 6 of 94


U0701
ICS9LPR363DGLF-T
X0701
14.318Mhz
to TPM
to 12p-DB
to PE DB
to ICH8m
to EC-8511
int. PU
int. PU
int. PD
int. PU
* : PU, ** : PD
INT-PU, INT-PD resistor value is 120K ohm.
Latched Input Select
pin8
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
pin5 (int. PU)
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
pin64 (int. PD)
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
pin9 (int. PU)
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
Latch Select Table
Pin5 | Pin9 | Pin14/15 | Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low) | SELLCD_27#=0 | PCIEX9 | 27FIX/SS
SELLCD_27#=1 | DOT96 | LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high) | SELLCD_27#=0 | PCIEX9 | PCIEX0
SELLCD_27#=1 | DOT96 | PCIEX0
BCLK | FSB | BSEL2 | BSEL1 | BSEL0
CPU Driven | / | / | /
166 | 667 | 0 | 1 | 1
200 | 800 | 0 | 1 | 0
PEREQ#1
Byte8-bit 1/0 => PCIEX_6/0
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#2
Byte8-bit 7/6 => PCIEX_8/1
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#3
Byte15-bit 1/0 => PCIEX_4/2
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#4_
Byte15-bit 7/6/5 => PCIEX_7/5/3
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
R0.2_1
<Variant Name>
ASUSTeK COMPUTER INC
Title : CLOCK GEN
Engineer: CW Chiang
Size: Custom
Project Name: F6E
Rev: 1.10
Date: Tuesday, August 21, 2007
Sheet 7 of 94


RCOMP
For Calibrating the FSB I/O Buffer
R0801
24.9Ohm 1%
H_RCOMP
GND
SCOMP
For Slew Rate Compenssation on the FSB
+VCCP
R0802
54.9Ohm
1%
H_SCOMP
R0803
54.9Ohm
1%
H_SCOMP#
Voltage Swing
For Providing a Reference Voltage to The FSB RCOMP circuits
+VCCP
R0804
221Ohm
H_SWING
R0805
100Ohm
1%
C0802
0.1UF/16V
GND
GND
4 H_D#[63:0]
H_D#[63:0]
4 H_A#[35:3]
H_A#[35:3]
U0801A
HOST
CRESTLINE_965GM
H_D#0 E2
H_D#1 G2
H_D#2 G7
H_D#3 M6
H_D#4 H7
H_D#5 H3
H_D#6 G4
H_D#7 F3
H_D#8 N8
H_D#9 H2
H_D#10 M10
H_D#11 N12
H_D#12 N9
H_D#13 H5
H_D#14 P13
H_D#15 K9
H_D#16 M2
H_D#17 W10
H_D#18 Y8
H_D#19 V4
H_D#20 M3
H_D#21 J1
H_D#22 N5
H_D#23 N3
H_D#24 W6
H_D#25 W9
H_D#26 N2
H_D#27 Y7
H_D#28 Y9
H_D#29 P4
H_D#30 W3
H_D#31 N1
H_D#32 AD12
H_D#33 AE3
H_D#34 AD9
H_D#35 AC9
H_D#36 AC7
H_D#37 AC14
H_D#38 AD11
H_D#39 AC11
H_D#40 AB2
H_D#41 AD7
H_D#42 AB1
H_D#43 Y3
H_D#44 AC6
H_D#45 AE2
H_D#46 AC5
H_D#47 AG3
H_D#48 AJ9
H_D#49 AH8
H_D#50 AJ14
H_D#51 AE9
H_D#52 AE11
H_D#53 AH12
H_D#54 AJ5
H_D#55 AH5
H_D#56 AJ6
H_D#57 AE7
H_D#58 AJ7
H_D#59 AJ2
H_D#60 AE5
H_D#61 AJ3
H_D#62 AH2
H_D#63 AH13
H_A#3 J13
H_A#4 B11
H_A#5 C11
H_A#6 M11
H_A#7 C15
H_A#8 F16
H_A#9 L13
H_A#10 G17
H_A#11 C14
H_A#12 K16
H_A#13 B13
H_A#14 L16
H_A#15 J17
H_A#16 B14
H_A#17 K19
H_A#18 P15
H_A#19 R17
H_A#20 B16
H_A#21 H20
H_A#22 L19
H_A#23 D17
H_A#24 M17
H_A#25 N16
H_A#26 J19
H_A#27 B18
H_A#28 E19
H_A#29 B17
H_A#30 B15
H_A#31 E17
H_A#32 C18
H_A#33 A19
H_A#34 B19
H_A#35 N19
H_ADS# G12
H_ADSTB#_0 H17
H_ADSTB#_1 G20
H_BNR# C8
H_BPRI# E8
H_BREQ# F12
H_DEFER# D6
H_DBSY# C10
HPLL_CLK AM5
HPLL_CLK# AM7
H_DPWR# H8
H_DRDY# K7
H_HIT# E4
H_HITM# C6
H_LOCK# G10
H_TRDY# B7
H_ADS# 4
H_ADSTB#0 4
H_ADSTB#1 4
H_BNR# 4
H_BPRI# 4
H_BREQ#0 4
H_DEFER# 4
H_DBSY# 4
CLK_MCH_BCLK 7
CLK_MCH_BCLK# 7
H_DPWR# 4
H_DRDY# 4
H_HIT# 4
H_HITM# 4
H_LOCK# 4
H_TRDY# 4
H_DINV#_0 K5
H_DINV#_1 L2
H_DINV#_2 AD13
H_DINV#_3 AE13
H_DINV#0 4
H_DINV#1 4
H_DINV#2 4
H_DINV#3 4
H_DSTBN#_0 M7
H_DSTBN#_1 K3
H_DSTBN#_2 AD2
H_DSTBN#_3 AH11
H_DSTBN#0 4
H_DSTBN#1 4
H_DSTBN#2 4
H_DSTBN#3 4
H_DSTBP#_0 L7
H_DSTBP#_1 K2
H_DSTBP#_2 AC2
H_DSTBP#_3 AJ10
H_DSTBP#0 4
H_DSTBP#1 4
H_DSTBP#2 4
H_DSTBP#3 4
H_REQ#_0 M14
H_REQ#_1 E13
H_REQ#_2 A11
H_REQ#_3 H13
H_REQ#_4 B12
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
4 H_REQ#[4:0]
H_REQ#[4:0]
H_RS#_0 E12
H_RS#_1 D7
H_RS#_2 D8
H_RS#0
H_RS#1
H_RS#2
H_RS#0 4
H_RS#1 4
H_RS#2 4
H_SWING B3
H_RCOMP C2
H_SCOMP W1
H_SCOMP# W2
H_CPURST# B6
H_CPUSLP# E5
H_AVREF B9
H_DVREF A9
H_SWING
H_RCOMP
H_SCOMP
H_SCOMP#
H_CPURST#
H_CPUSLP#
T0801
4 H_CPURST#
4 H_CPUSLP#
R0807 0Ohm
+VCCP
R0809
1KOhm
1%
H_VREF
C0801
0.1UF/10V
R0808
2KOhm
1%
GND
GND
<Variant Name>
Title : 965GM -- CPU (1)
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 8 of 94



D4	D3	D2	D1	D0	Output Voltage
0	0	0	0	0	1.250
0	0	0	1	0	1.200
0	0	1	0	0	1.150
0	0	1	1	0	1.100
0	1	0	0	0	1.050



<Variant Name>

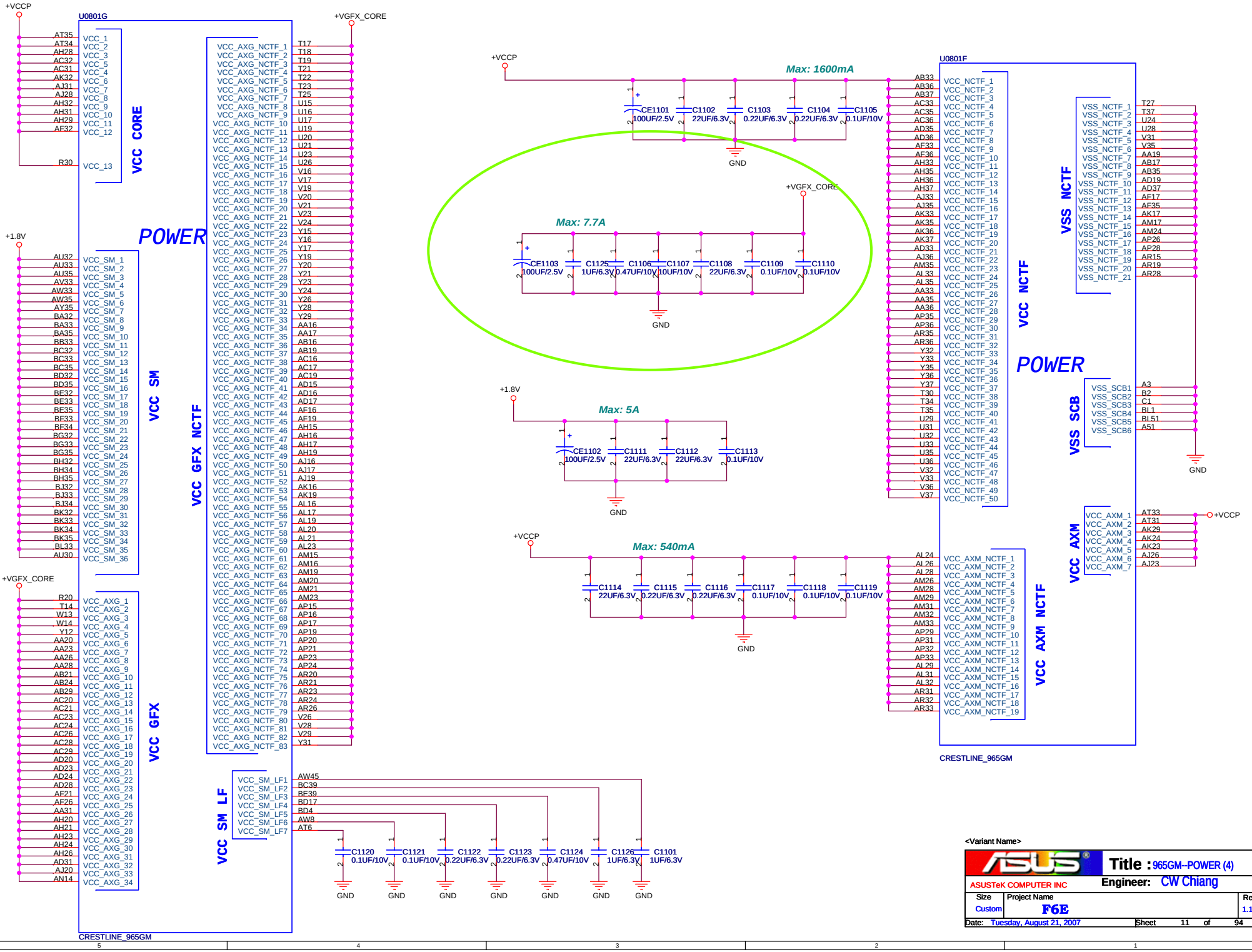
ASUSTeK COMPUTER INC

Title : 965GM--DDR2 bus (3)

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 10 of 94



<Variant Name>

ASUSTeK COMPUTER INC

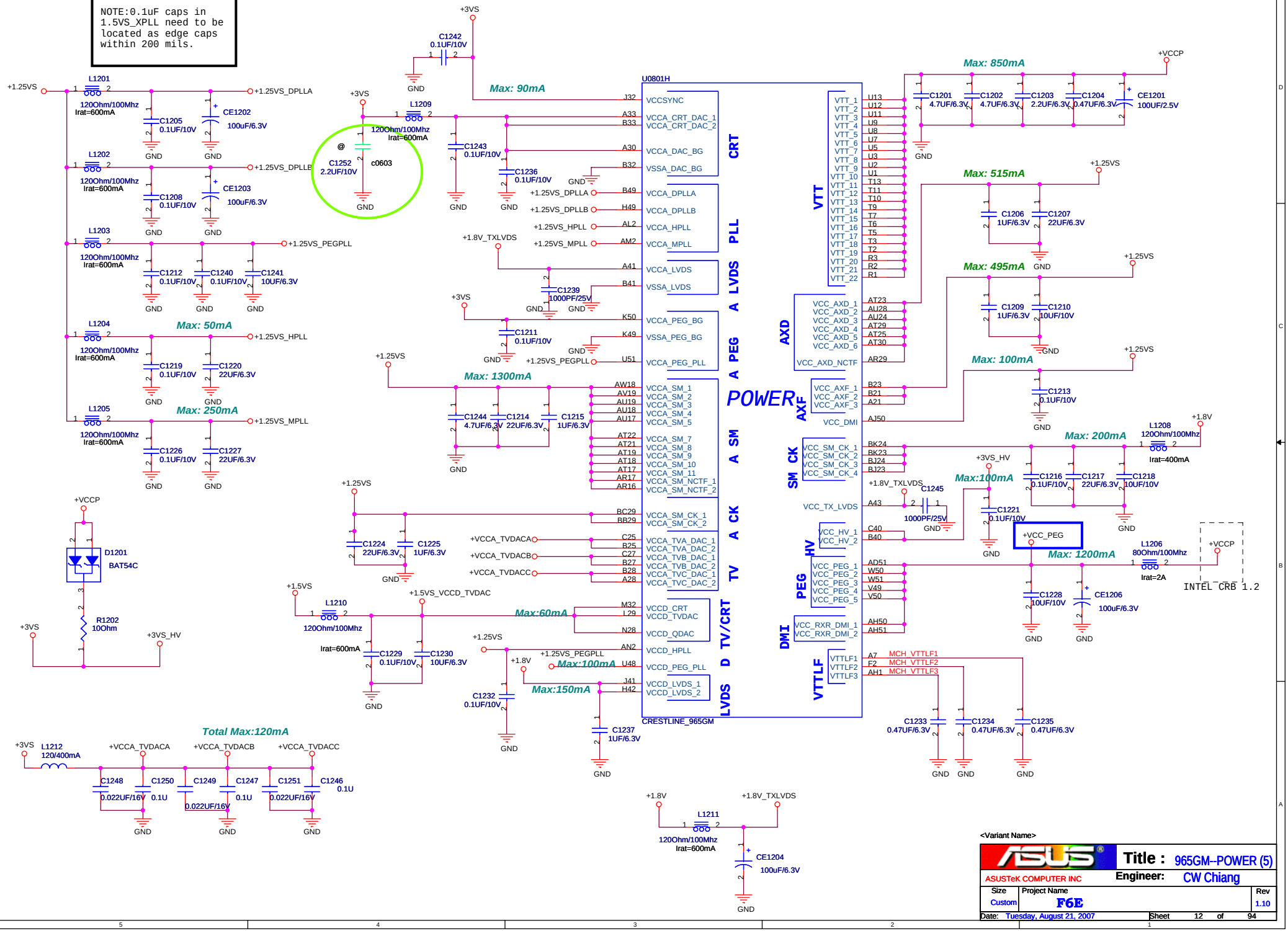
Title : 965GM--POWER (4)

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 11 of 94

NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.

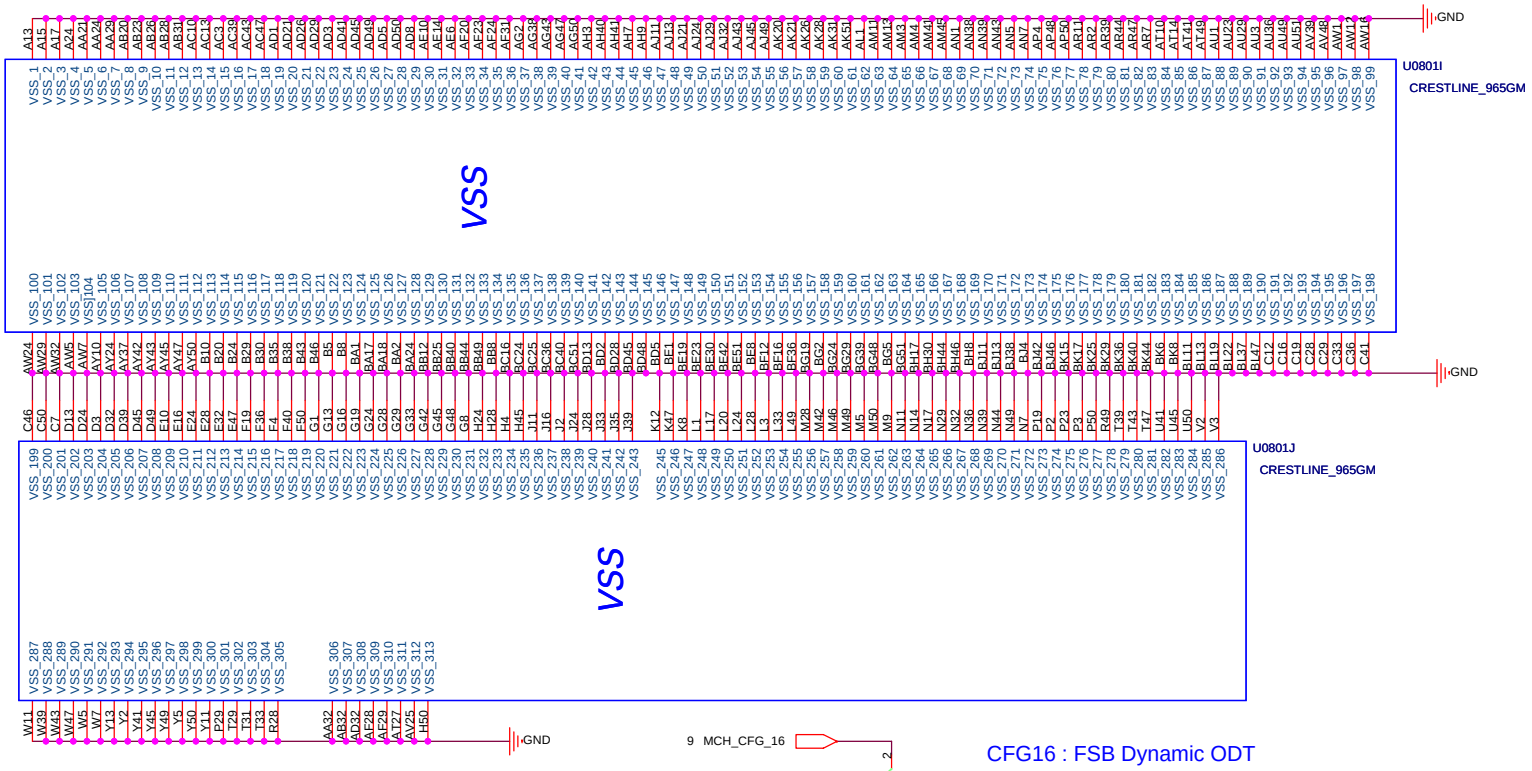


<Variant Name>

ASUSTeK COMPUTER INC

Engineer: CW Chiang

Title : 965GM--POWER (5)		
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 12 of 94	



9 MCH_CFG_5 — R1301 4.02KOHM — GND

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

9 MCH_CFG_7 — R1304 4.02KOHM @ — GND

CFG7 : Intel Management Engine Crypto strap
HIGH = TLS cipher suite with confidentiality (Default)
LOW = TLS cipher suite with no confidentiality

9 MCH_CFG_9 — R1302 4.02KOHM @ — GND

CFG9 : PCI Express Graphics Lane Reversal
LOW = Lane Reversed
HIGH = Normal mode (Default; lanes numbered in order)
CHECK detail...

9 MCH_CFG_13 — R1308 4.02KOHM @ — GND
9 MCH_CFG_12 — R1309 4.02KOHM @ — GND

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

9 MCH_CFG_16 — R1305 4.02KOHM @ — GND

CFG16 : FSB Dynamic ODT
Low = Dynamic ODT Disabled
HIGH = Dyanamic ODT Enabled (default)

+3VS — R1310 4.02KOHM @ — 9 MCH_CFG_18

CFG18 : VCC Select
LOW = 1.05V (default)
HIGH = 1.5V

DG1.5a(22244): CFG18: reserved.

+3VS — R1303 4.02KOHM @ — 9 MCH_CFG_19

CFG19 : DMI Lane Reversal
LOW = Normal (default)
HIGH = LANES REVERSED

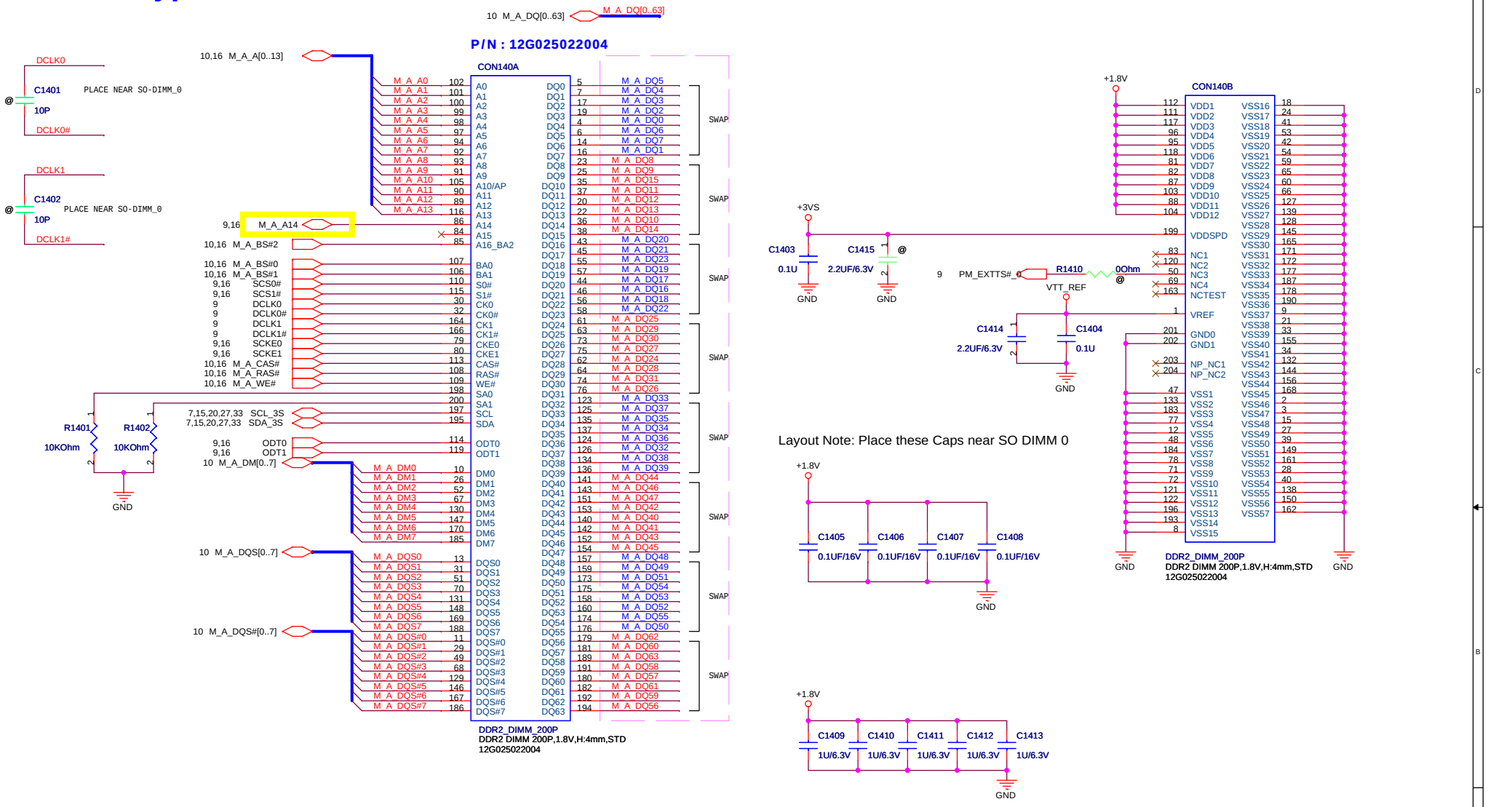
+3VS — R1307 4.02KOHM @ — 9 MCH_CFG_20

CFG20 : Concurrent SDVO / PCIe
LOW = Only SDVO or PCIE is operational (default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port
CHECK detail...

<Variant Name>

ASUSTeK COMPUTER INC	Title : GND/Strapping (6)	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 13 of 94	

Standard Type



<Variant Name>

ASUSTeK COMPUTER INC

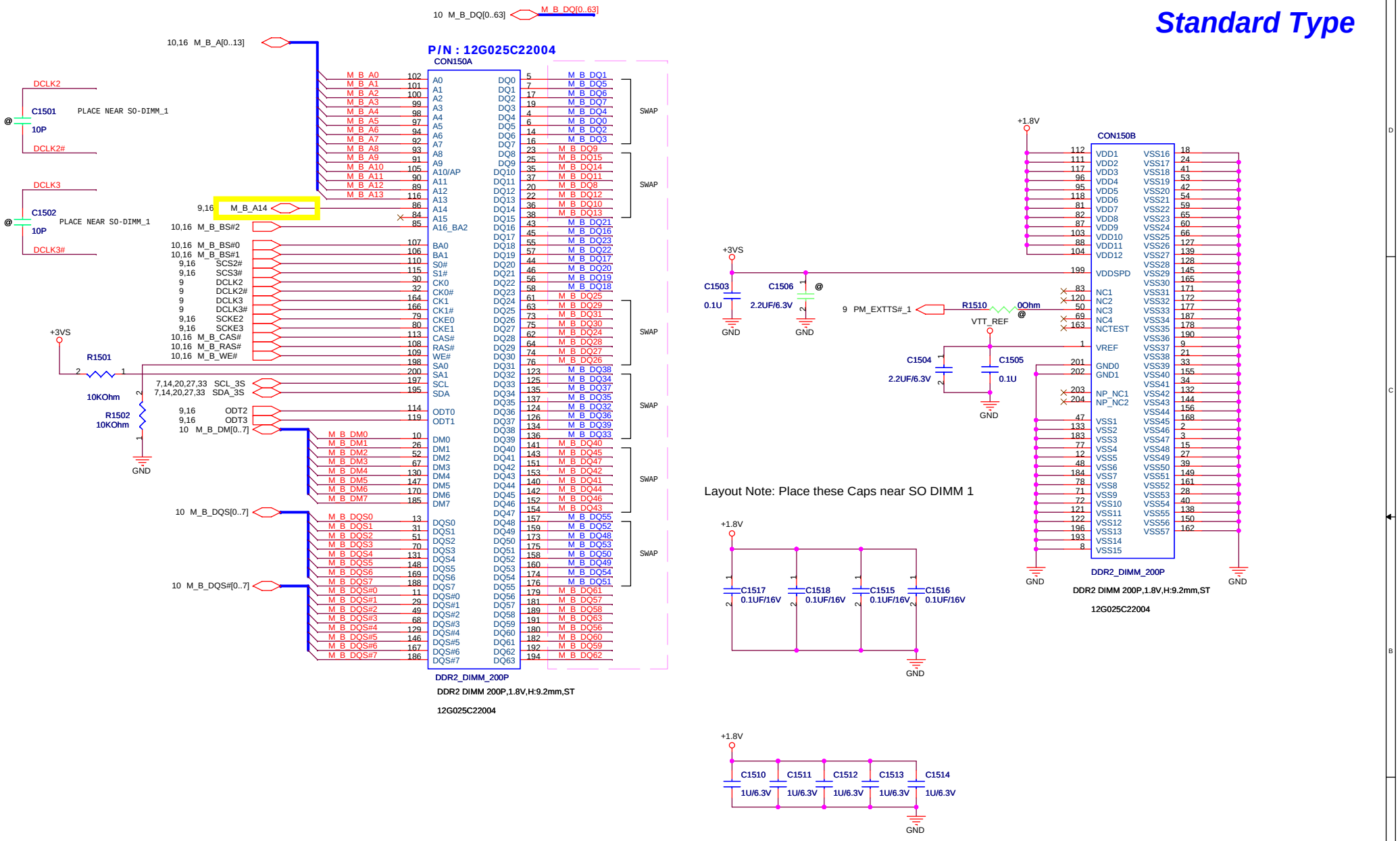
Title : DDR SO-DIMM 0

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 14 of 94

Standard Type



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR SO-DIMM_1

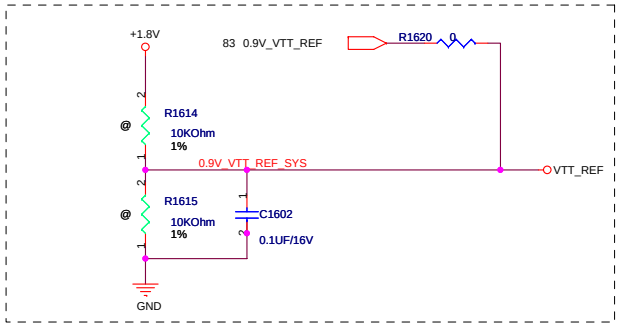
Engineer: CW Chiang

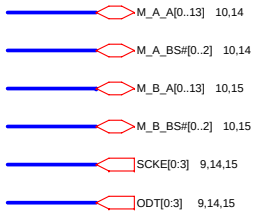
Size	Project Name	Rev
Custom	F6E	1.10

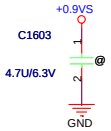
Date: Tuesday, August 21, 2007 Sheet 15 of 94

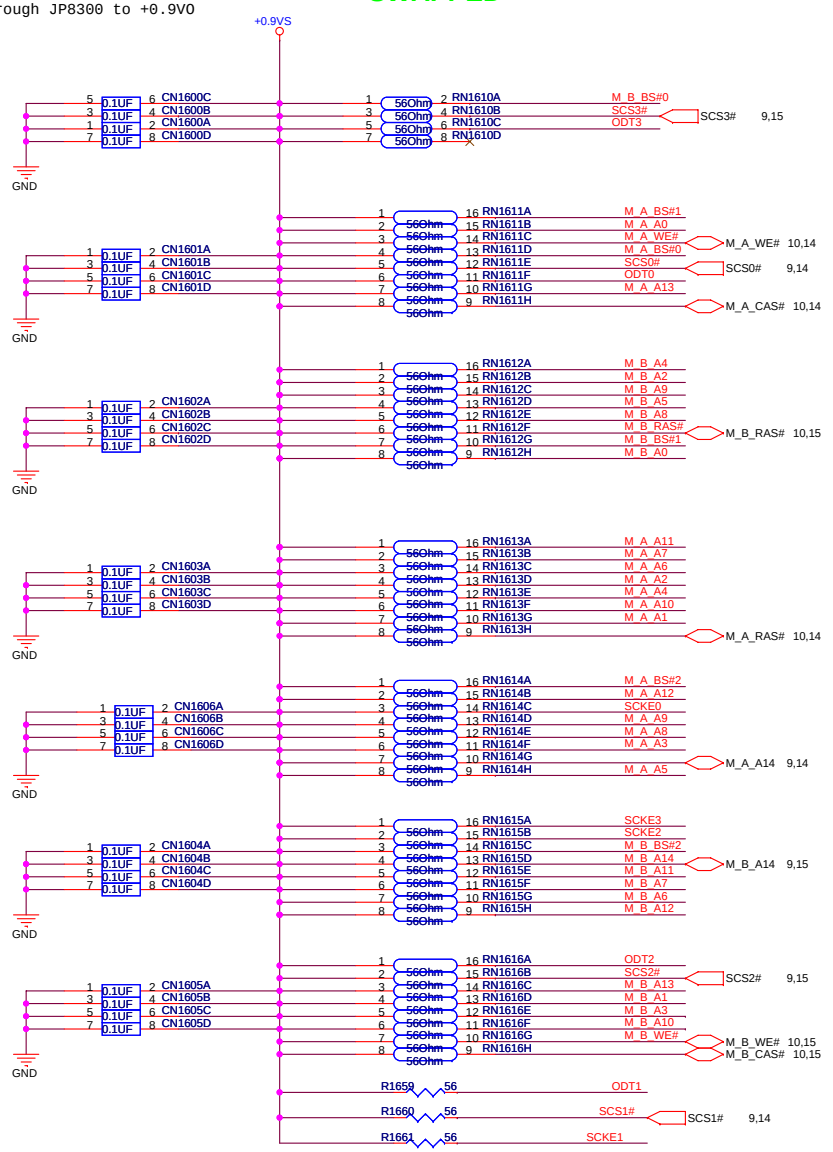
SWAPPED

+0.9VS through JP8300 to +0.9VO







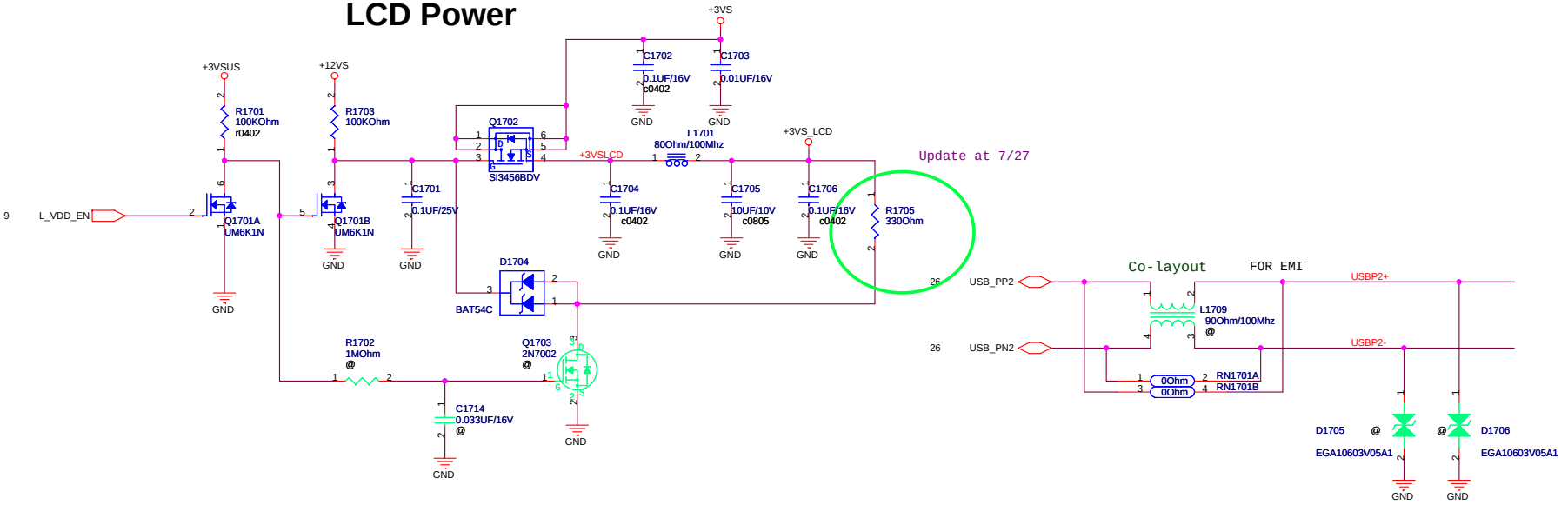


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

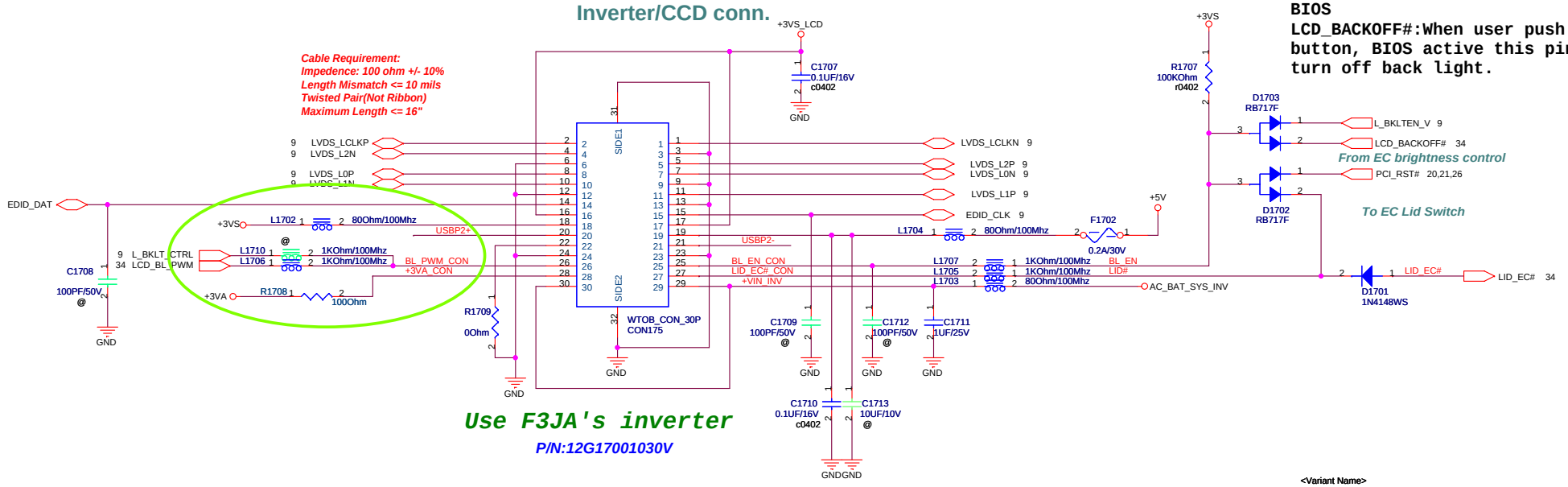
ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 16 of 94	

LCD Power



Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



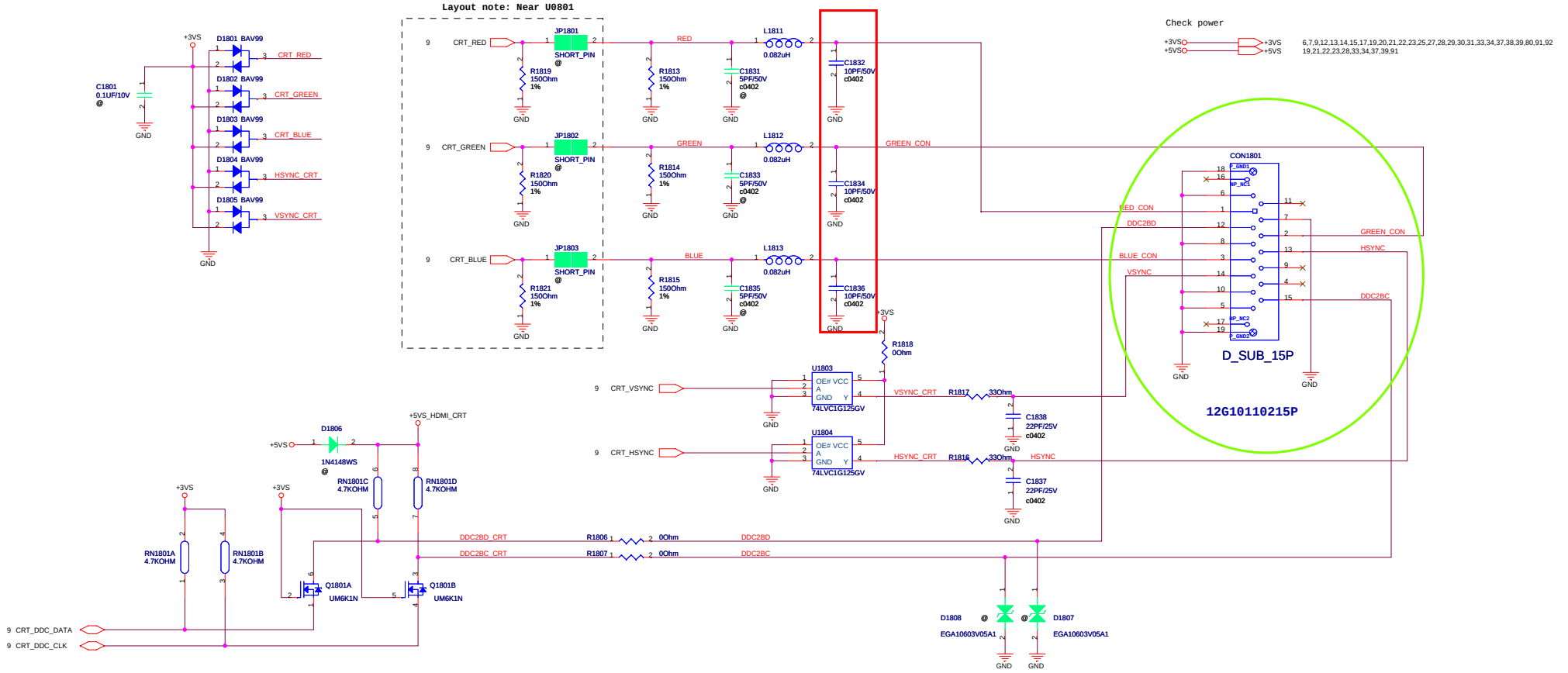
Use F3JA's inverter

P/N:12G17001030V

BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 17 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

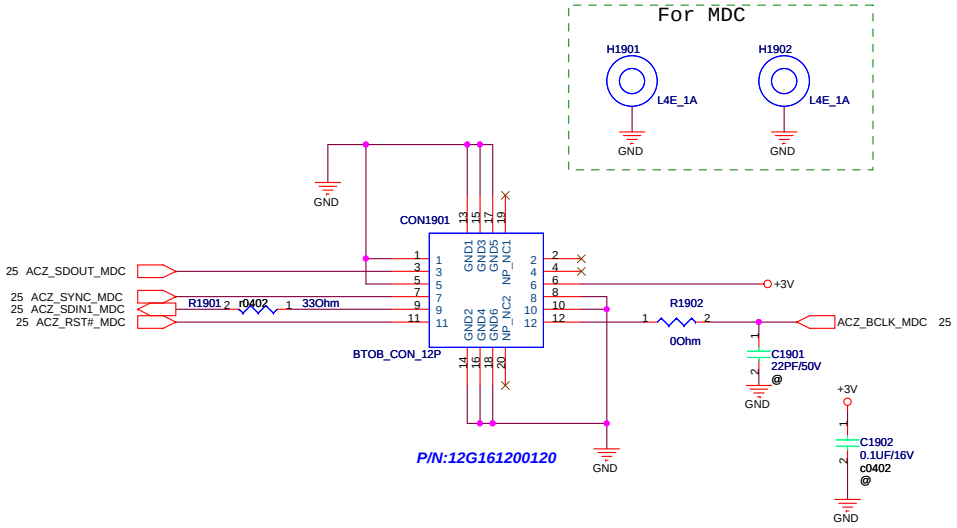
Title : CRT

Engineer: CW Chiang

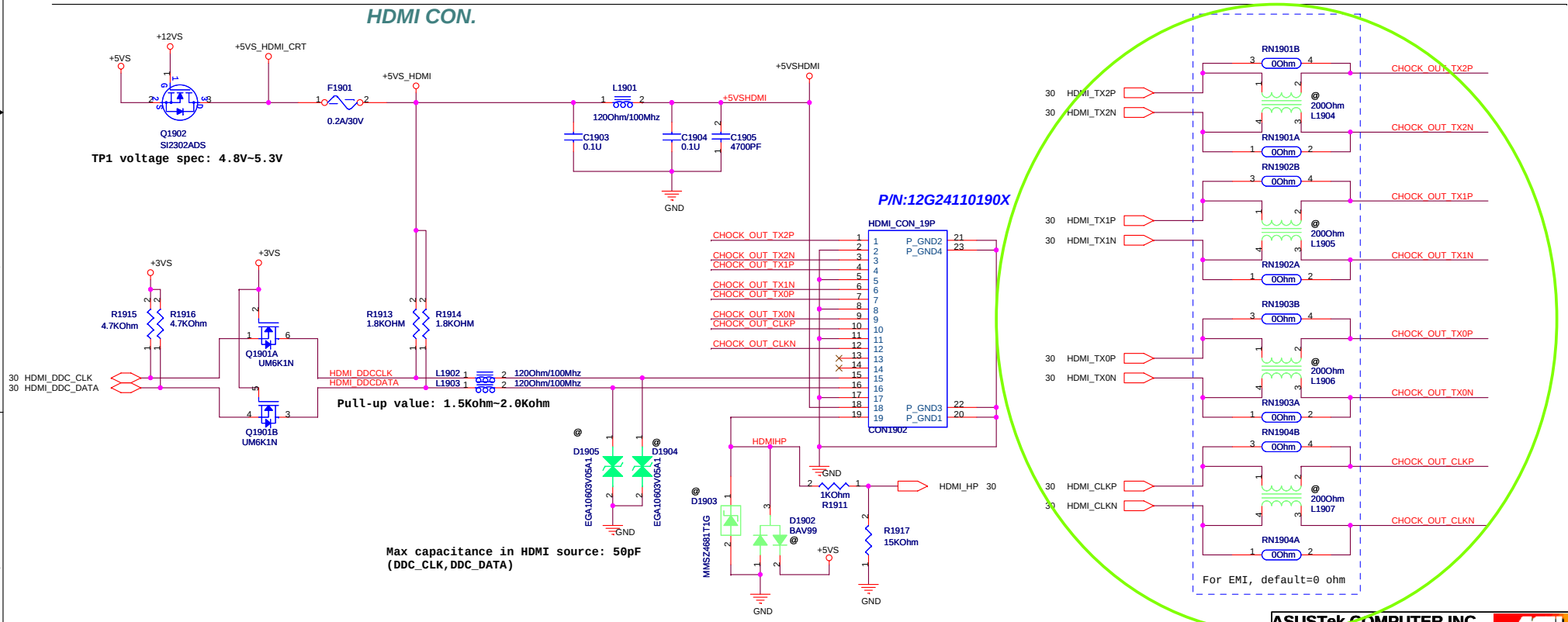
Size	Project Name	Rev
C	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 18 of 94

MDC CON.



HDMI CON.



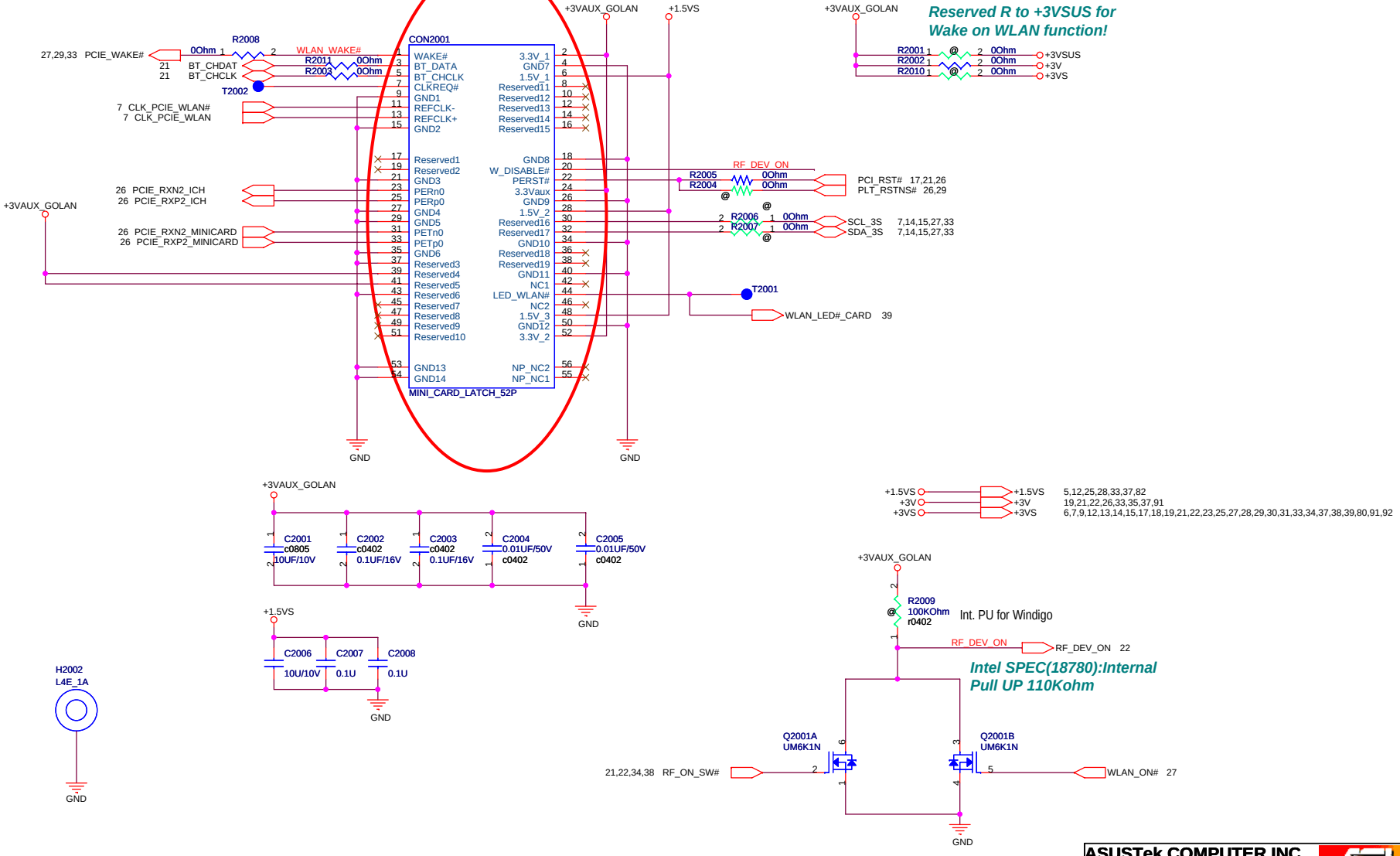
Note:
1. L1901,L1902,L1903: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant pins of SII1392.

ASUSTek COMPUTER INC.	Li-Te Rd.,Peitou, Taipei,Taiwan, ROC	
Title: MDC,HDMI CON		CW Chiang
Size: Custom	Document Number: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 19 of 94	

+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

P/N : 12G030000523

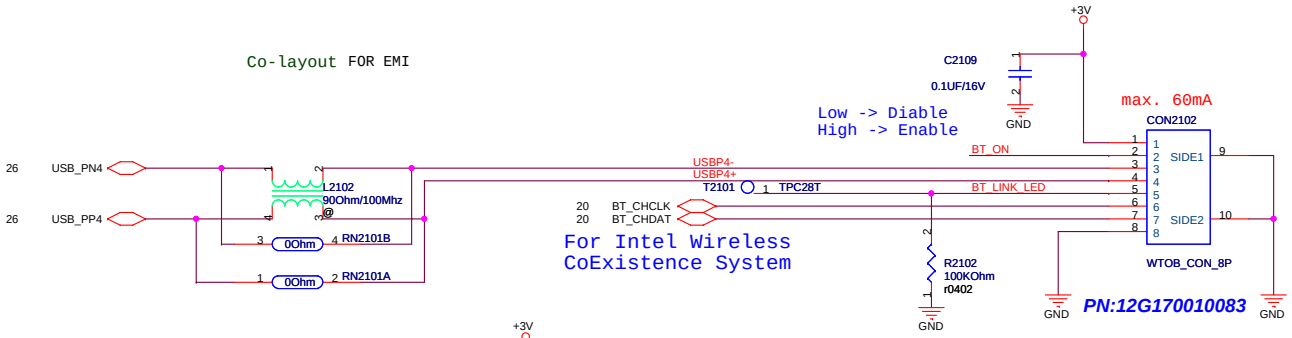
WLAN

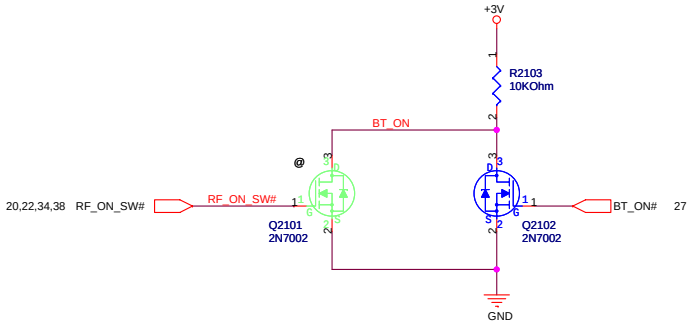


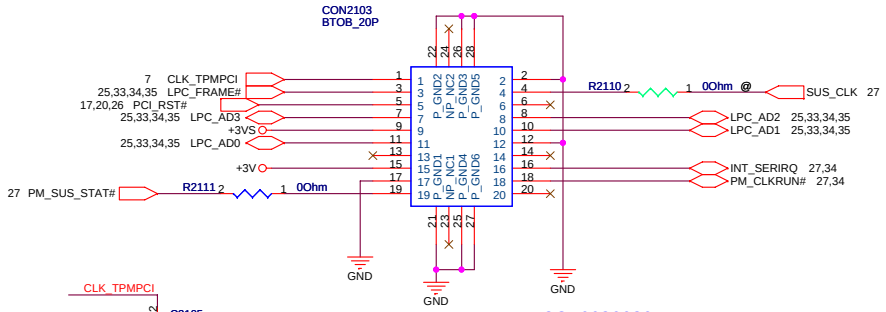
Reserved R to +3VSUS for Wake on WLAN function!

ASUSTek COMPUTER INC.		
Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: MINI CARD--(1)	CW Chiang	
Size: Custom	Document Number: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 20 of 94	

Co-layout FOR EMI

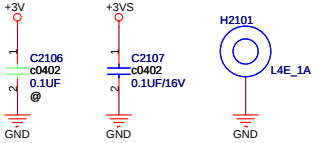




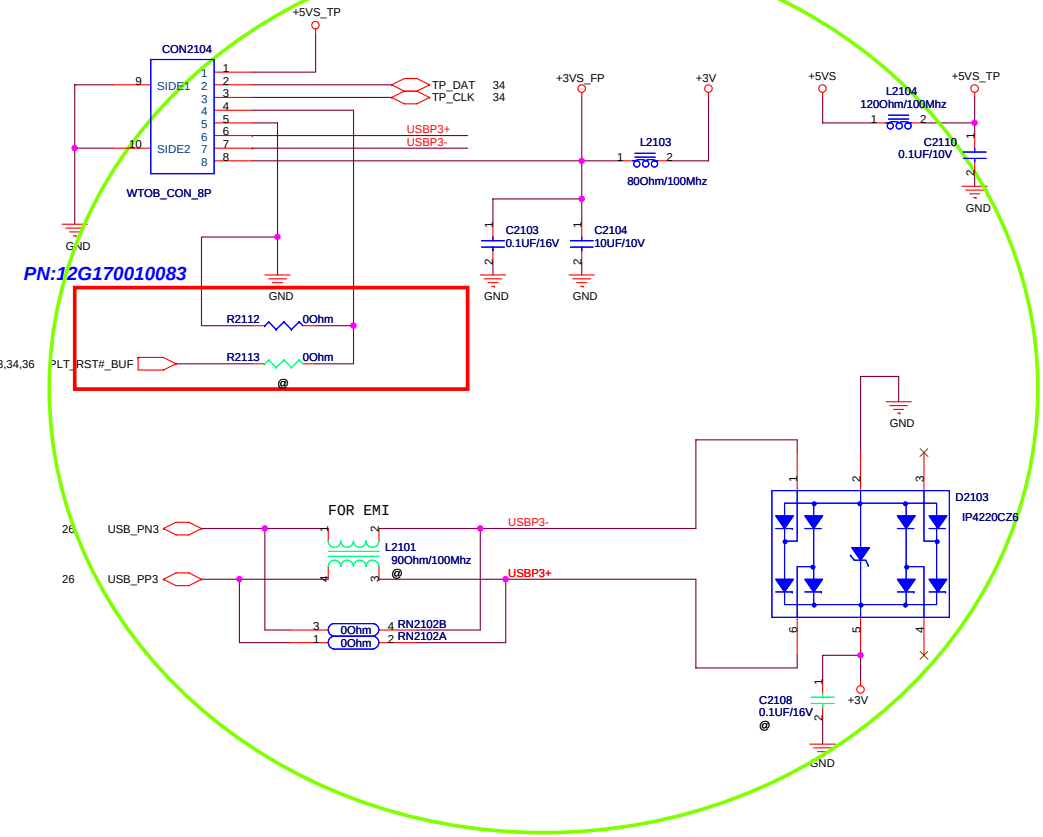


PN:12G16080020J

TPM Module CON

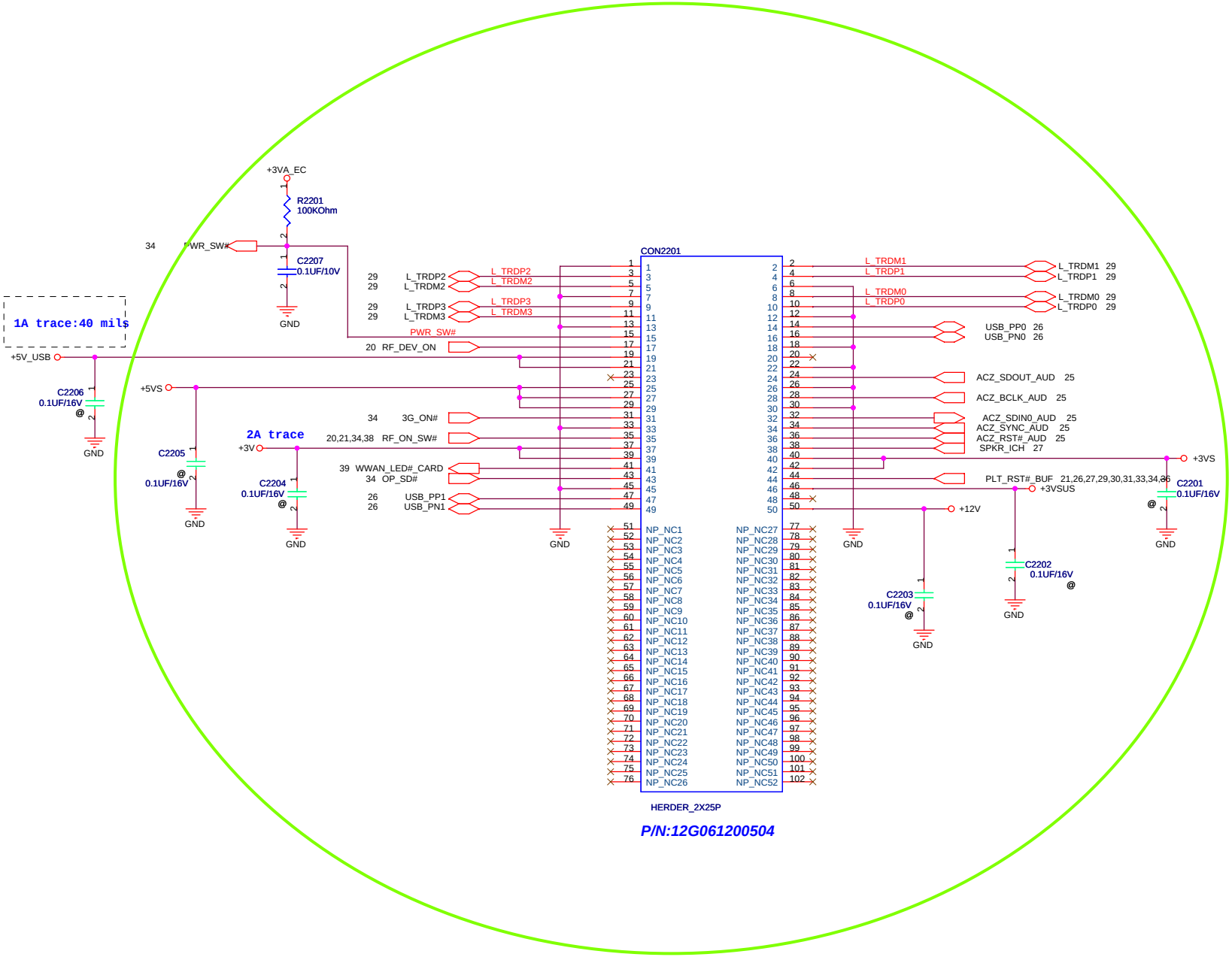


For Finger Printer and Touch-Pad



<Variant Name>

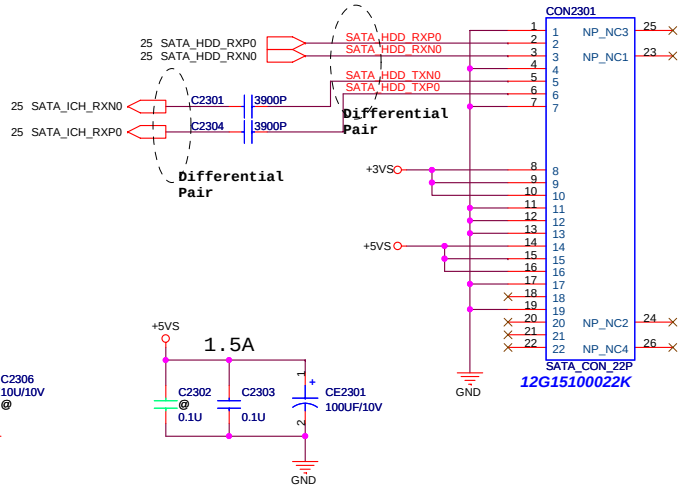
ASUSTeK COMPUTER INC	Title : B/T,F/P& TPM	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 21 of 94	



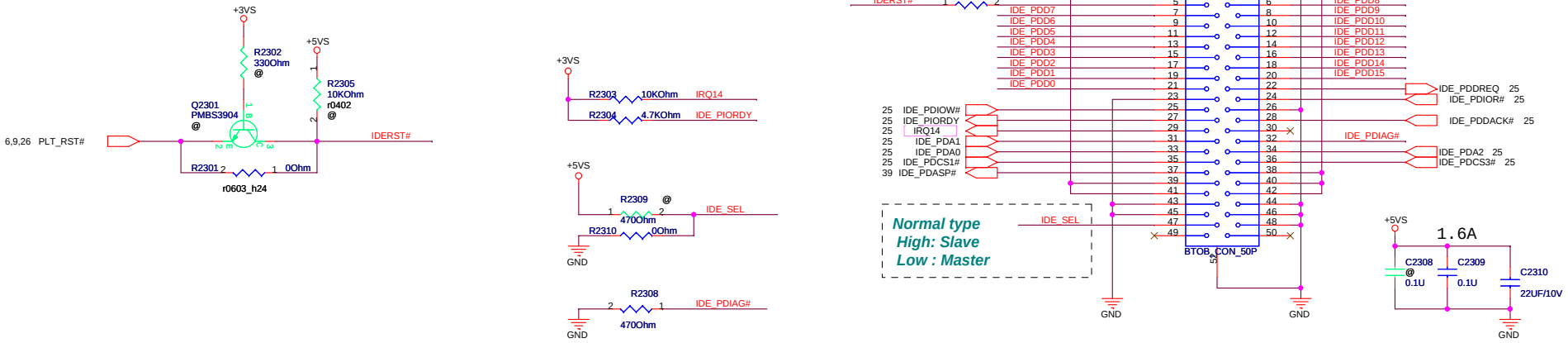
<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 22 of 94	

SATA HDD CON



PATA CD-ROM CON



<Variant Name>

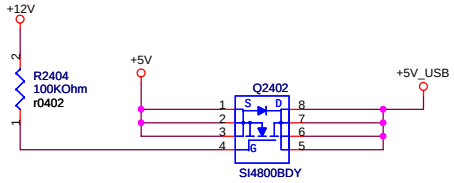
ASUSTeK COMPUTER INC

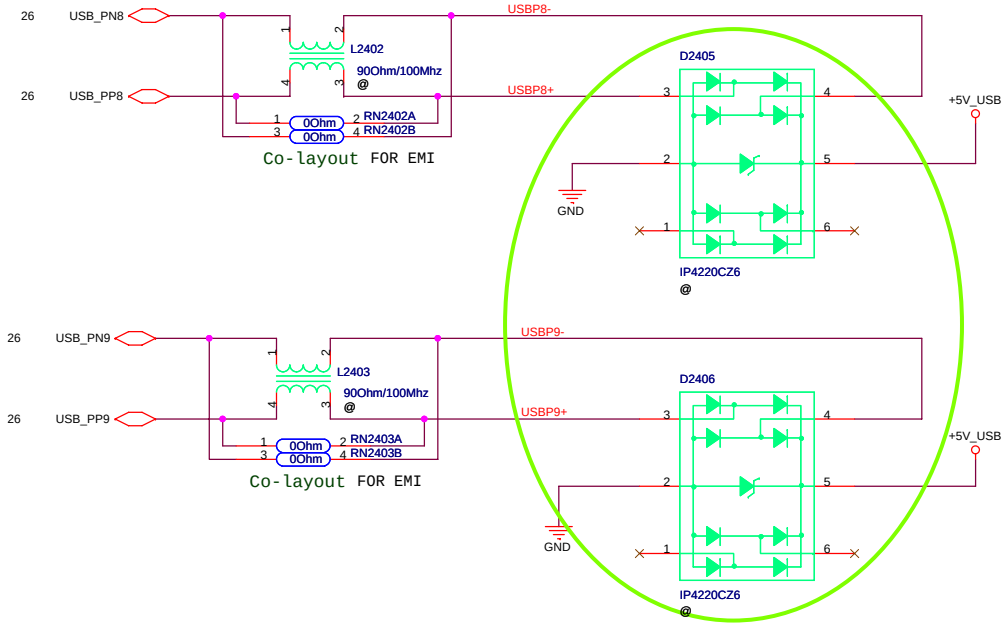
Title : HDD & CDROM

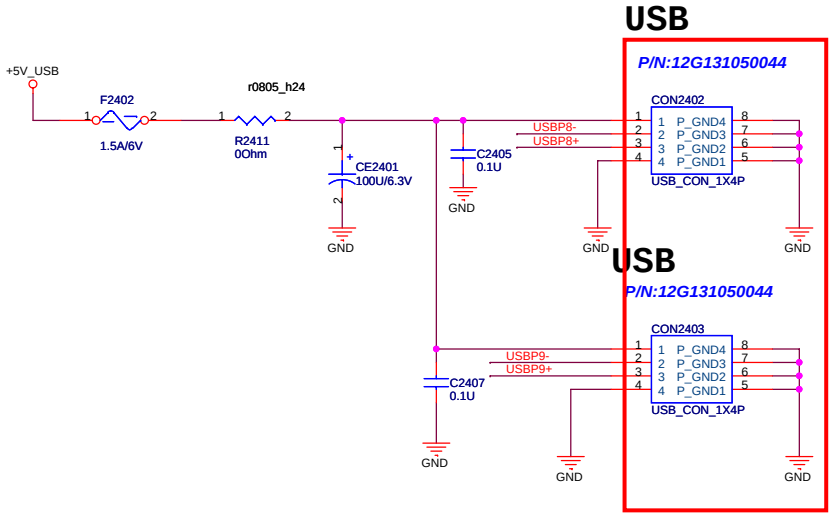
Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 23 of 94

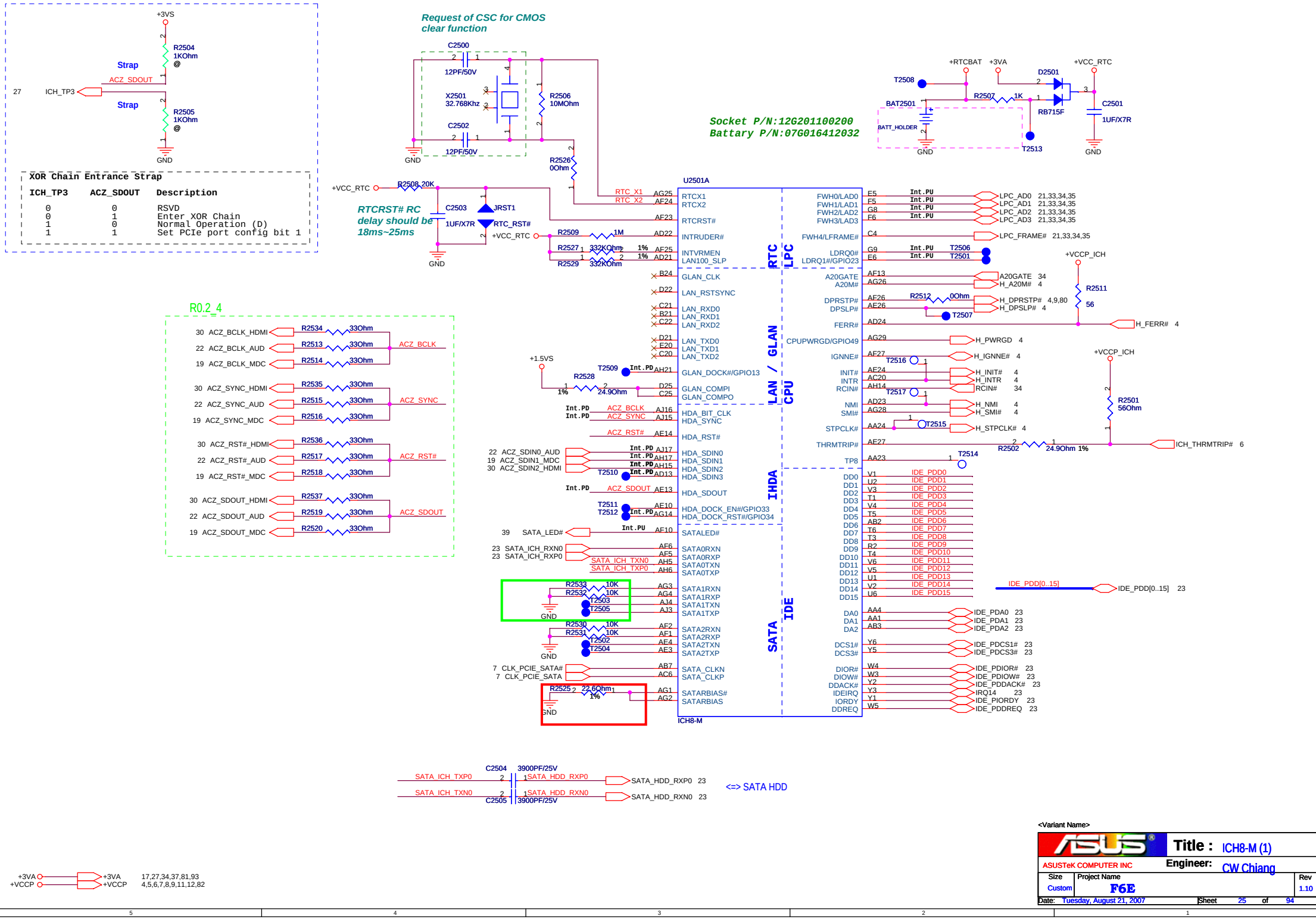


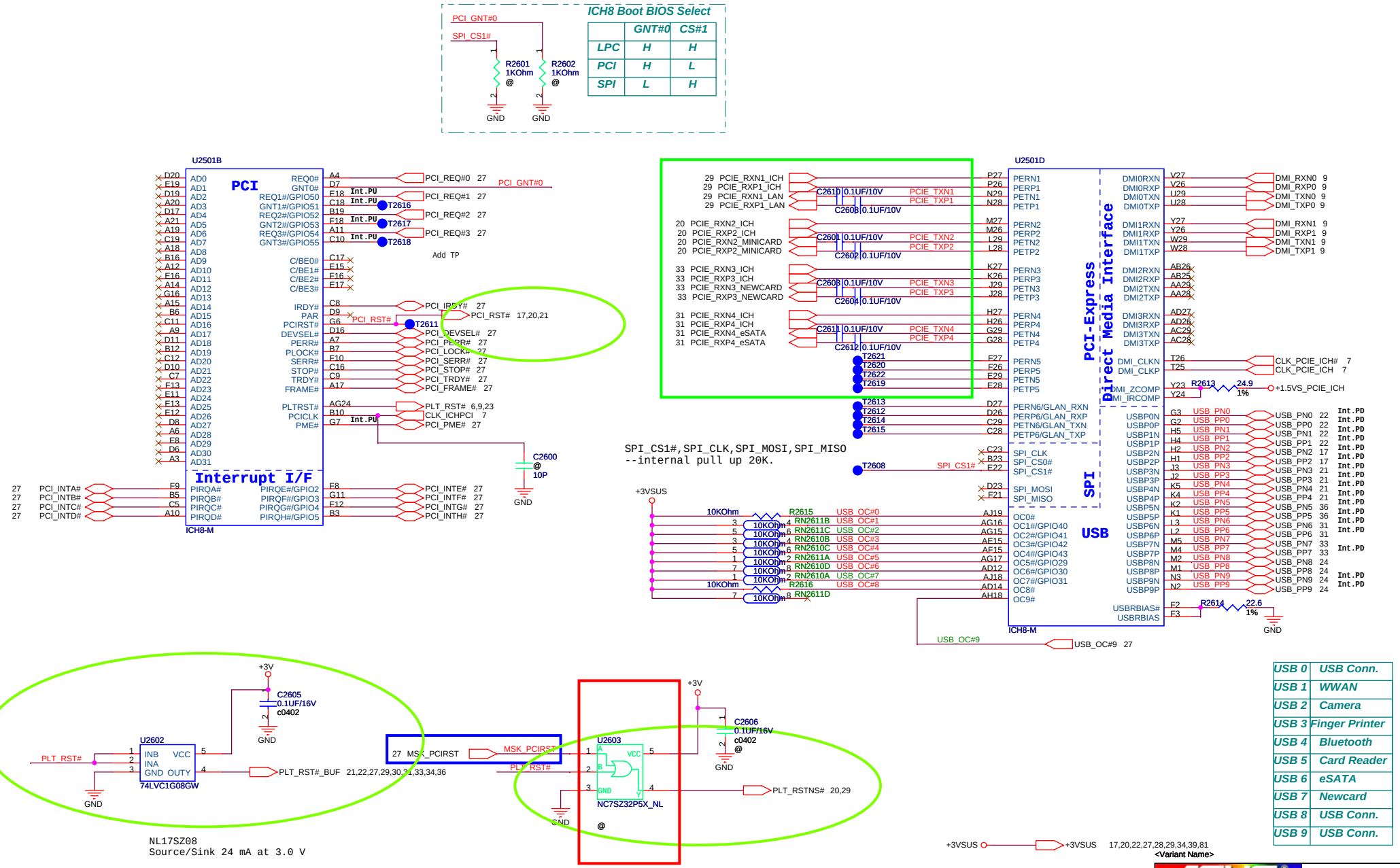


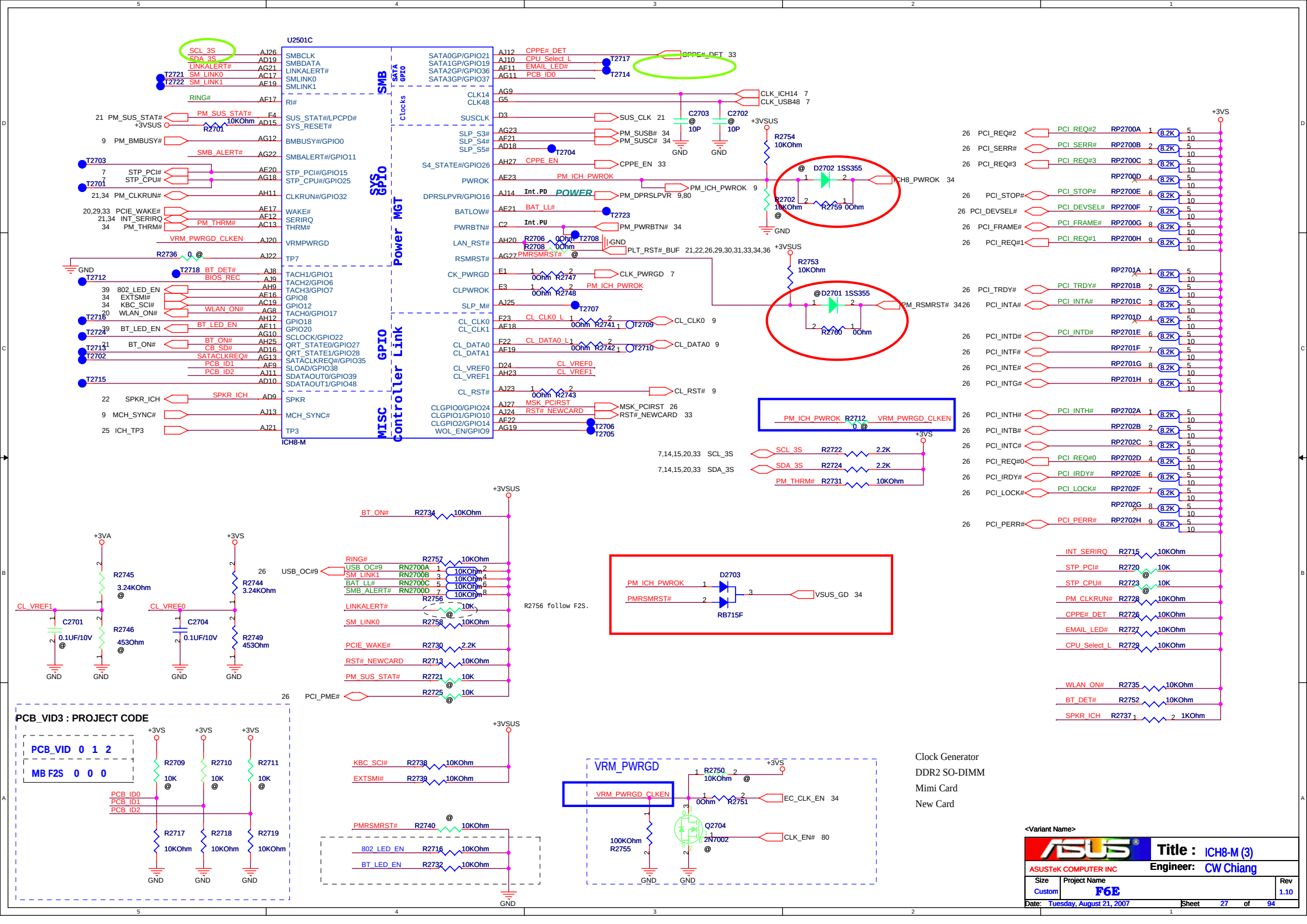


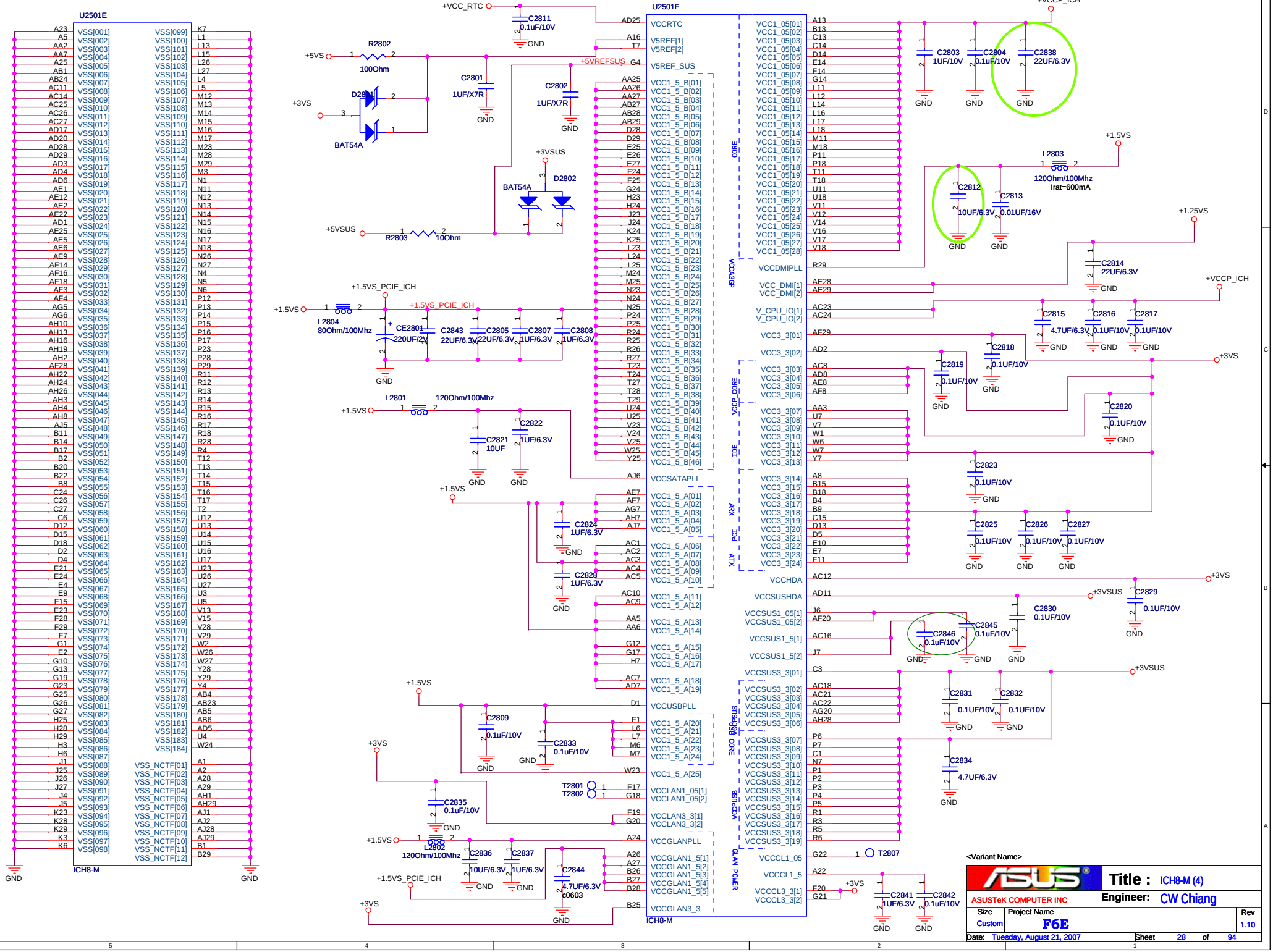
<Variant Name>

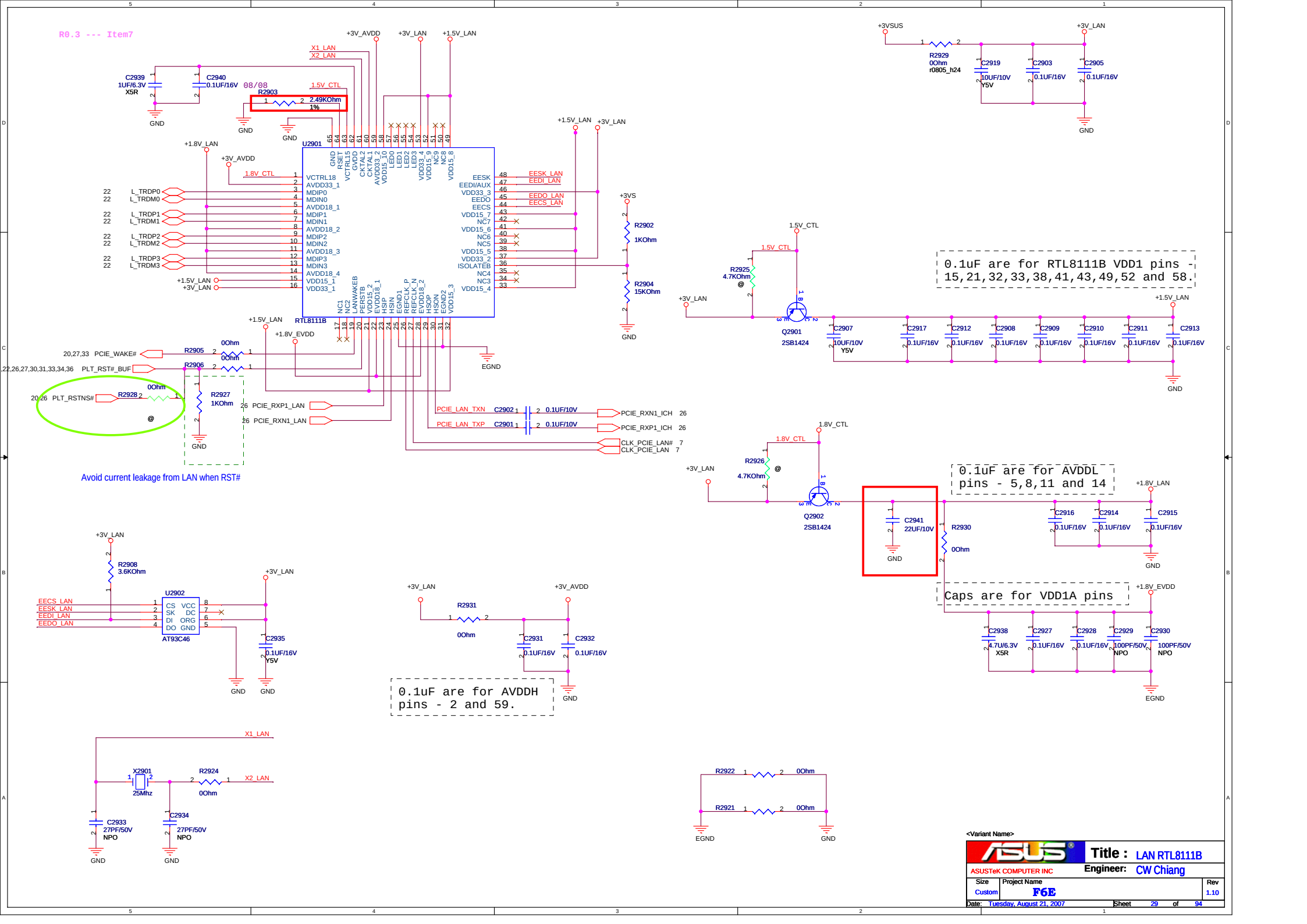
ASUSTeK COMPUTER INC	Title : USB PORTS	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 24 of 94	

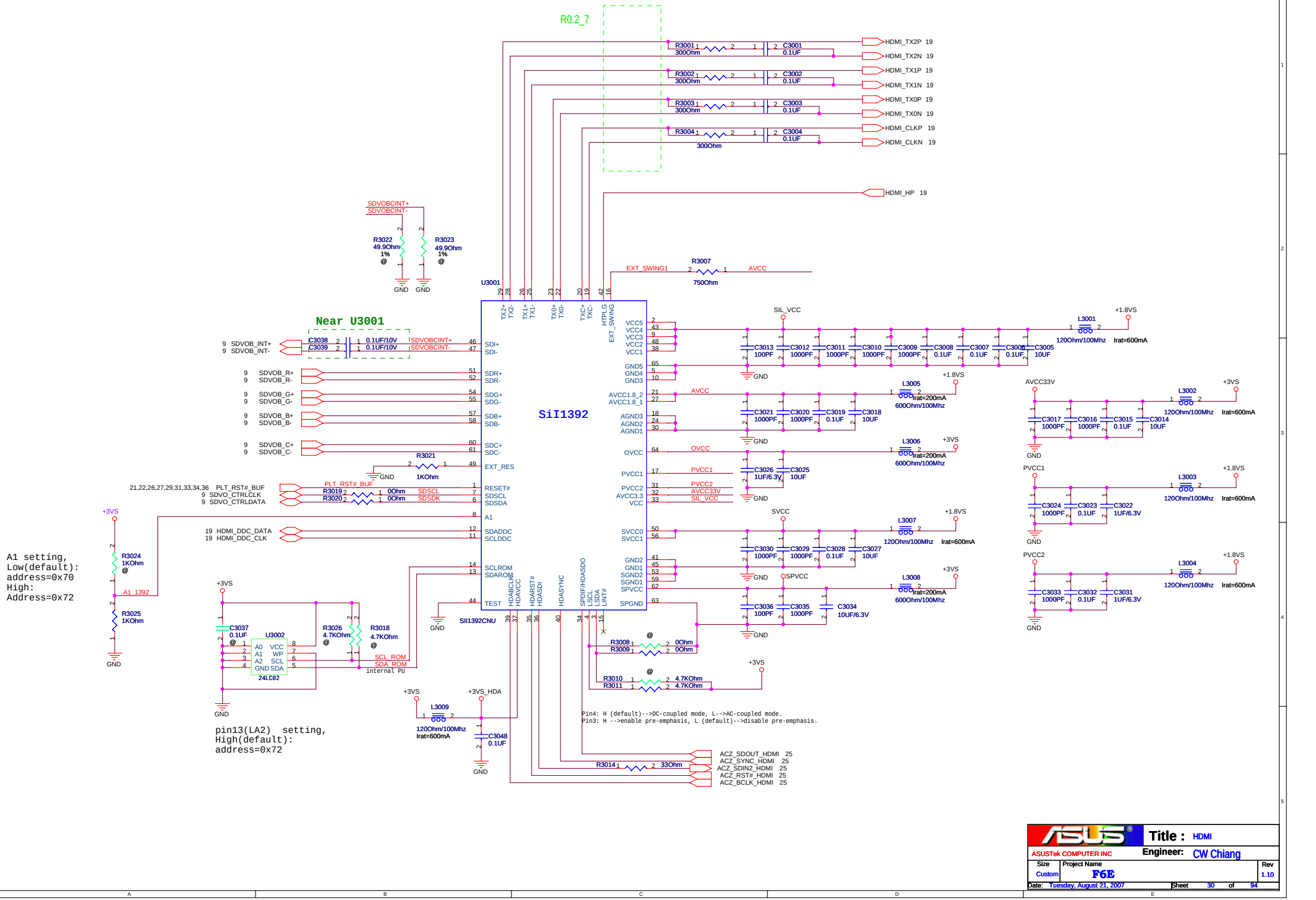

Strap
ACZ_SDOUT
27 ICH_TP3
Strap
R2504 1KOhm @
R2505 1KOhm @
GND
XOR Chain Entrance Strap
ICH_TP3 ACZ_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (D)
1 1 Set PCIe port config bit 1
Request of CSC for CMOS clear function
C2500 12PF/50V
X2501 32.768Khz
C2502 12PF/50V
R2506 10MOhm
R2526 0Ohm
Socket P/N:12G201100200
Battary P/N:07G016412032
+RTCBAT +3VA +VCC_RTC
T2508 BAT2501 BATT_HOLDER
R2507 1K
D2501 RB715F
C2501 1UF/X7R
T2513
RTCRST# RC delay should be 18ms~25ms
+VCC_RTC R2508 20K
C2503 1UF/X7R
JRST1
RTC_RST#
R2509 1M
R2527 332KOhm 1%
R2529 332KOhm 1%
U2501A
RTC_X1 AG25 RTCX1
RTC_X2 AF24 RTCX2
AF23 RTCRST#
AD22 INTRUDER#
AE25 INTVRMEN
AD21 LAN100_SLP
RTC
B24 GLAN_CLK
D22 LAN_RSTSYNC
C21 LAN_RXD0
B21 LAN_RXD1
C22 LAN_RXD2
D21 LAN_TXD0
E20 LAN_TXD1
C20 LAN_TXD2
LAN / GLAN
+1.5VS R2528 24.9Ohm 1%
T2509 Int.PD
AH21 GLAN_DOCK#/GPIO13
D25 GLAN_COMPI
C25 GLAN_COMPO
CPU
Int.PD ACZ_BCLK AJ16 HDA_BIT_CLK
Int.PD ACZ_SYNC AJ15 HDA_SYNC
ACZ_RST# AE14 HDA_RST#
22 ACZ_SDIN0_AUD
19 ACZ_SDIN1_MDC
30 ACZ_SDIN2_HDMI
T2510
AJ17 HDA_SDIN0
AH17 HDA_SDIN1
AH15 HDA_SDIN2
AD13 HDA_SDIN3
Int.PD ACZ_SDOUT AE13 HDA_SDOUT
T2511 T2512
AE10 HDA_DOCK_EN#/GPIO33
AG14 HDA_DOCK_RST#/GPIO34
IHDA
39 SATA_LED# Int.PU AE10 SATALED#
23 SATA_ICH_RXN0 AE6 SATA0RXN
23 SATA_ICH_RXP0 AE5 SATA0RXP
SATA_ICH_TXN0 AH5 SATA0TXN
SATA_ICH_TXP0 AH6 SATA0TXP
R2533 10K
R2532 10K
T2503
T2505
AG3 SATA1RXN
AG4 SATA1RXP
AJ4 SATA1TXN
AJ3 SATA1TXP
R2530 10K
R2531 10K
T2502
T2504
AF2 SATA2RXN
AF1 SATA2RXP
AE4 SATA2TXN
AE3 SATA2TXP
7 CLK_PCIE_SATA#
7 CLK_PCIE_SATA
AB7 SATA_CLKN
AC6 SATA_CLKP
R2525 22.6Ohm 1%
AG1 SATARBIAS#
AG2 SATARBIAS
SATA
IDE
ICH8-M
FWH0/LAD0 E5 Int.PU LPC_AD0 21,33,34,35
FWH1/LAD1 F5 Int.PU LPC_AD1 21,33,34,35
FWH2/LAD2 G8 Int.PU LPC_AD2 21,33,34,35
FWH3/LAD3 F6 Int.PU LPC_AD3 21,33,34,35
FWH4/LFRAME# C4 LPC_FRAME# 21,33,34,35
LDRQ0# G9 Int.PU T2506
LDRQ1#/GPIO23 E6 Int.PU T2501
A20GATE AF13 A20GATE 34
A20M# AG26 H_A20M# 4
DPRSTP# AF26 R2512 0Ohm H_DPRSTP# 4,9,80
DPSLP# AE26 T2507 H_DPSLP# 4
FERR# AD24 H_FERR# 4
CPUPWRGD/GPIO49 AG29 H_PWRGD 4
IGNNE# AF27 T2516 H_IGNNE# 4
INIT# AE24 H_INIT# 4
INTR AC20 H_INTR 4
RCIN# AH14 T2517 RCIN# 34
NMI AD23 H_NMI 4
SMI# AG28 H_SMI# 4
STPCLK# AA24 T2515 H_STPCLK# 4
THRMTRIP# AE27 R2502 24.9Ohm 1% ICH_THRMTRIP# 6
TP8 AA23 T2514
+VCCP_ICH R2511 56
+VCCP_ICH R2501 56Ohm
DD0 V1 IDE_PDD0
DD1 U2 IDE_PDD1
DD2 V3 IDE_PDD2
DD3 T1 IDE_PDD3
DD4 V4 IDE_PDD4
DD5 T5 IDE_PDD5
DD6 AB2 IDE_PDD6
DD7 T6 IDE_PDD7
DD8 T3 IDE_PDD8
DD9 R2 IDE_PDD9
DD10 T4 IDE_PDD10
DD11 V6 IDE_PDD11
DD12 V5 IDE_PDD12
DD13 U1 IDE_PDD13
DD14 V2 IDE_PDD14
DD15 U6 IDE_PDD15
IDE_PDD[0..15] IDE_PDD[0..15] 23
DA0 AA4 IDE_PDA0 23
DA1 AA1 IDE_PDA1 23
DA2 AB3 IDE_PDA2 23
DCS1# Y6 IDE_PDCS1# 23
DCS3# Y5 IDE_PDCS3# 23
DIOR# W4 IDE_PDIOR# 23
DIOW# W3 IDE_PDIOW# 23
DDACK# Y2 IDE_PDDACK# 23
IDEIRQ Y3 IRQ14 23
IORDY Y1 IDE_PIORDY 23
DDREQ W5 IDE_PDDREQ 23
R0.2_4
30 ACZ_BCLK_HDMI R2534 33Ohm
22 ACZ_BCLK_AUD R2513 33Ohm
19 ACZ_BCLK_MDC R2514 33Ohm
ACZ_BCLK
30 ACZ_SYNC_HDMI R2535 33Ohm
22 ACZ_SYNC_AUD R2515 33Ohm
19 ACZ_SYNC_MDC R2516 33Ohm
ACZ_SYNC
30 ACZ_RST#_HDMI R2536 33Ohm
22 ACZ_RST#_AUD R2517 33Ohm
19 ACZ_RST#_MDC R2518 33Ohm
ACZ_RST#
30 ACZ_SDOUT_HDMI R2537 33Ohm
22 ACZ_SDOUT_AUD R2519 33Ohm
19 ACZ_SDOUT_MDC R2520 33Ohm
ACZ_SDOUT
SATA_ICH_TXP0 C2504 3900PF/25V SATA_HDD_RXP0 SATA_HDD_RXP0 23
SATA_ICH_TXN0 C2505 3900PF/25V SATA_HDD_RXN0 SATA_HDD_RXN0 23
<=> SATA HDD
+3VA +VCCP +3VA +VCCP 17,27,34,37,81,93 4,5,6,7,8,9,11,12,82
<Variant Name>
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 25 of 94


ICH8 Boot BIOS Select
GNT#0 CS#1
LPC H H
PCI H L
SPI L H
PCI_GNT#0
SPI_CS1#
R2601 1KOhm @
R2602 1KOhm @
GND
U2501B
PCI
Interrupt I/F
ICH8-M
PCI_REQ#0 27
PCI_REQ#1 27
PCI_REQ#2 27
PCI_REQ#3 27
Add TP
PCI_IRDY# 27
PCI_RST# 17,20,21
PCI_DEVSEL# 27
PCI_PERR# 27
PCI_LOCK# 27
PCI_SERR# 27
PCI_STOP# 27
PCI_TRDY# 27
PCI_FRAME# 27
PLT_RST# 6,9,23
CLK_ICHPCI 7
PCI_PME# 27
C2600 @ 10P
PCI_INTA#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_INTE# 27
PCI_INTF# 27
PCI_INTG# 27
PCI_INTH# 27
U2501D
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M
SPI_CS1#,SPI_CLK,SPI_MOSI,SPI_MISO
--internal pull up 20K.
+3VSUS
R2615
R2616
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9 27
R2613 24.9 1%
+1.5VS_PCIE_ICH
R2614 22.6 1%
U2602
74LVC1G08GW
PLT_RST#_BUF 21,22,27,29,30,31,33,34,36
C2605 0.1UF/16V c0402
U2603
NC7SZ32P5X_NL
MSK_PCIRST 27
PLT_RSTNS# 20,29
C2606 0.1UF/16V c0402
NL17SZ08
Source/Sink 24 mA at 3.0 V
+3VSUS 17,20,22,27,28,29,34,39,81
<Variant Name>
USB 0 USB Conn.
USB 1 WWAN
USB 2 Camera
USB 3 Finger Printer
USB 4 Bluetooth
USB 5 Card Reader
USB 6 eSATA
USB 7 Newcard
USB 8 USB Conn.
USB 9 USB Conn.
Title : ICH8-M (2)
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 26 of 94

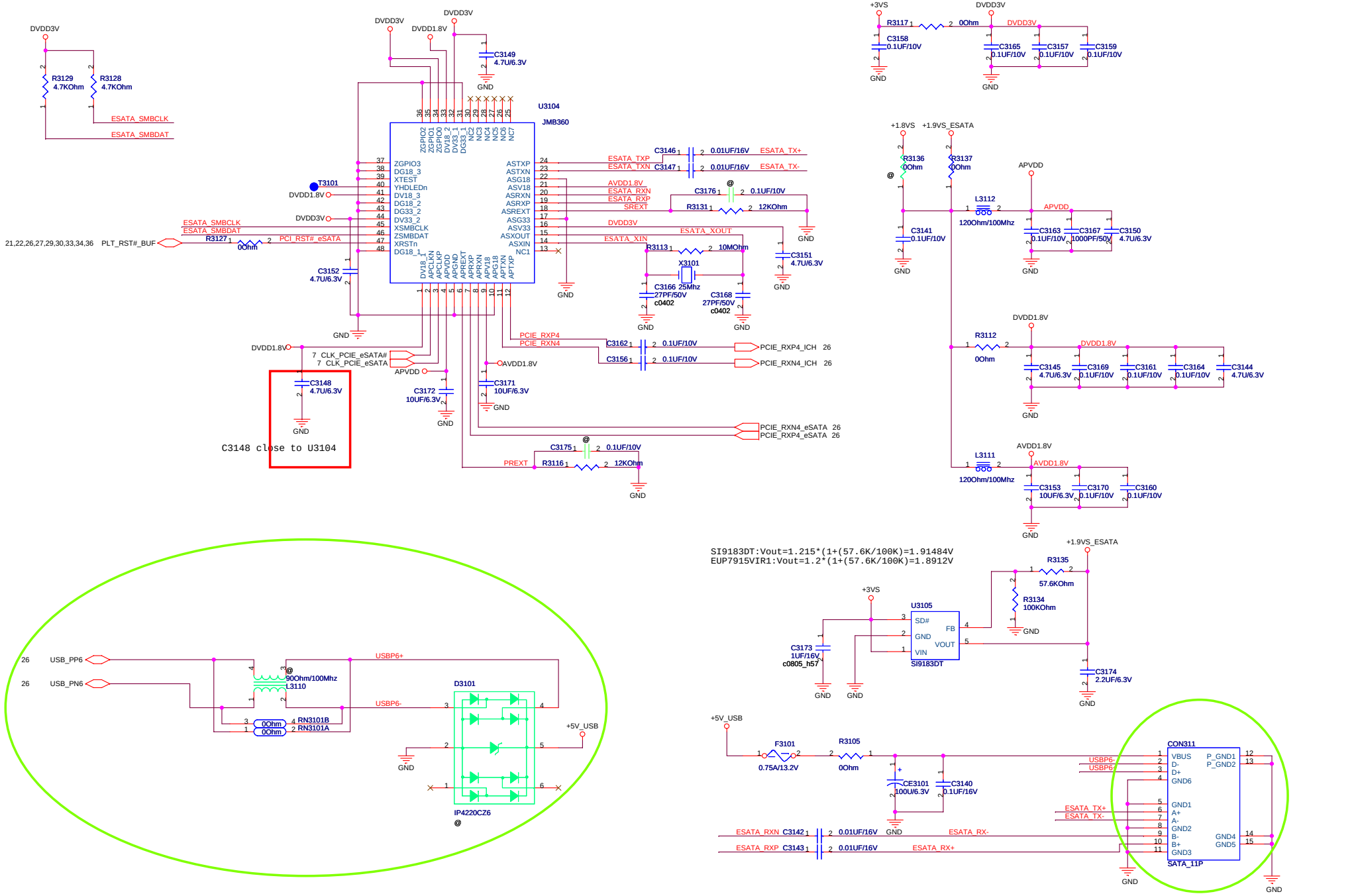

U2501C
ICH8-M
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SCL_3S
SDA_3S
LINKALERT#
SM_LINK0
SM_LINK1
RING#
PM_SUS_STAT#
PM_BMBUSY#
SMB_ALERT#
STP_PCI#
STP_CPU#
CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THRM#
VRM_PWRGD_CLKEN
SPKR_ICH
MCH_SYNC#
ICH_TP3
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CPPE# DET
CPU_Select_L
EMAIL_LED#
PCB_ID0
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
CLK_ICH14
CLK_USB48
SUS_CLK
PM_SUSB#
PM_SUSC#
CPPE_EN
PM_ICH_PWROK
PM_DPRSLPVR
BAT_LL#
PM_PWRBTN#
PLT_RST#_BUF
PMRSMRST#
CL_CLK0_L
CL_DATA0_L
MSK_PCIRST
RST#_NEWCARD
PCI_REQ#2
PCI_SERR#
PCI_REQ#3
PCI_STOP#
PCI_DEVSEL#
PCI_FRAME#
PCI_REQ#1
PCI_TRDY#
PCI_INTA#
PCI_INTD#
PCI_INTF#
PCI_INTE#
PCI_INTG#
PCI_INTH#
PCI_INTB#
PCI_INTC#
PCI_REQ#0
PCI_IRDY#
PCI_LOCK#
PCI_PERR#
D2702 1SS355
D2701 1SS355
D2703
RB715F
PM_ICH_PWROK
PMRSMRST#
VSUS_GD
R2712
VRM_PWRGD_CLKEN
SCL_3S
SDA_3S
PM_THRM#
BT_ON#
USB_OC#9
LINKALERT#
SM_LINK0
PCIE_WAKE#
RST#_NEWCARD
PM_SUS_STAT#
PCI_PME#
R2756 follow F2S.
INT_SERIRQ
STP_PCI#
STP_CPU#
PM_CLKRUN#
CPPE# DET
EMAIL_LED#
CPU_Select_L
WLAN_ON#
BT_DET#
SPKR_ICH
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB F2S 0 0 0
PCB_ID0
PCB_ID1
PCB_ID2
KBC_SCI#
EXTSMI#
802_LED_EN
BT_LED_EN
VRM_PWRGD
VRM_PWRGD_CLKEN
EC_CLK_EN
CLK_EN#
Clock Generator
DDR2 SO-DIMM
Mimi Card
New Card
<Variant Name>
Title : ICH8-M (3)
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 27 of 94


U2501E
ICH8-M
U2501F
ICH8-M
R2802
100Ohm
D2801
BAT54A
C2801
1UF/X7R
C2802
1UF/X7R
D2802
BAT54A
R2803
10Ohm
L2804
80Ohm/100Mhz
CE2801
220UF/2V
L2801
120Ohm/100Mhz
L2802
120Ohm/100Mhz
L2803
120Ohm/100Mhz
Irat=600mA
T2801
T2802
T2807
+VCC_RTC
+5VS
+3VS
+5VSUS
+5VREFSUS
+3VSUS
+1.5VS
+1.5VS_PCIE_ICH
+VCCP_ICH
+1.25VS
+3VSUS
GND
<Variant Name>
Title : ICH8-M (4)
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size: Custom
Project Name: F6E
Rev: 1.10
Date: Tuesday, August 21, 2007
Sheet 28 of 94


R0.3 --- Item7
U2901
RTL8111B
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
MDIP2
MDIN2
AVDD18_3
MDIP3
MDIN3
AVDD18_4
VDD15_1
VDD33_1
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
VDD15_7
NC7
VDD15_6
NC6
NC5
VDD15_5
VDD33_2
ISOLATEB
NC4
NC3
VDD15_4
EESK_LAN
EEDI_LAN
EEDO_LAN
EECS_LAN
L_TRDP0
L_TRDM0
L_TRDP1
L_TRDM1
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
1.8V_CTL
1.5V_CTL
X1_LAN
X2_LAN
R2903 2.49KOhm 1%
08/08
C2939 1UF/6.3V X5R
C2940 0.1UF/16V
R2902 1KOhm
R2904 15KOhm
R2905 0Ohm
R2906 0Ohm
R2927 1KOhm
R2928 0Ohm
20,27,33 PCIE_WAKE#
22,26,27,30,31,33,34,36 PLT_RST#_BUF
20,26 PLT_RSTNS#
26 PCIE_RXP1_LAN
26 PCIE_RXN1_LAN
PCIE_LAN_TXN C2902 0.1UF/10V
PCIE_LAN_TXP C2901 0.1UF/10V
PCIE_RXN1_ICH 26
PCIE_RXP1_ICH 26
CLK_PCIE_LAN# 7
CLK_PCIE_LAN 7
Avoid current leakage from LAN when RST#
+3V_AVDD
+3V_LAN
+1.5V_LAN
+1.8V_LAN
+1.8V_EVDD
+3VS
+3VSUS
EGND
GND
R2929 0Ohm r0805_h24
C2919 10UF/10V Y5V
C2903 0.1UF/16V
C2905 0.1UF/16V
R2925 4.7KOhm @
Q2901 2SB1424
C2907 10UF/10V Y5V
C2917 0.1UF/16V
C2912 0.1UF/16V
C2908 0.1UF/16V
C2909 0.1UF/16V
C2910 0.1UF/16V
C2911 0.1UF/16V
C2913 0.1UF/16V
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
R2926 4.7KOhm @
Q2902 2SB1424
C2941 22UF/10V
R2930 0Ohm
C2916 0.1UF/16V
C2914 0.1UF/16V
C2915 0.1UF/16V
0.1uF are for AVDDL pins - 5,8,11 and 14
Caps are for VDD1A pins
C2938 4.7U/6.3V X5R
C2927 0.1UF/16V
C2928 0.1UF/16V
C2929 100PF/50V NPO
C2930 100PF/50V NPO
R2908 3.6KOhm
U2902
AT93C46
EECS_LAN
EESK_LAN
EEDI_LAN
EEDO_LAN
C2935 0.1UF/16V Y5V
R2931 0Ohm
C2931 0.1UF/16V
C2932 0.1UF/16V
0.1uF are for AVDDH pins - 2 and 59.
X2901 25Mhz
R2924 0Ohm
C2933 27PF/50V NPO
C2934 27PF/50V NPO
R2922 0Ohm
R2921 0Ohm
<Variant Name>
Title : LAN RTL8111B
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 29 of 94



ASUSTek COMPUTER INC	Title : HDMI	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 30 of 94	



ASUSTek COMPUTER INC

Title : 31_ESATA-JMB360

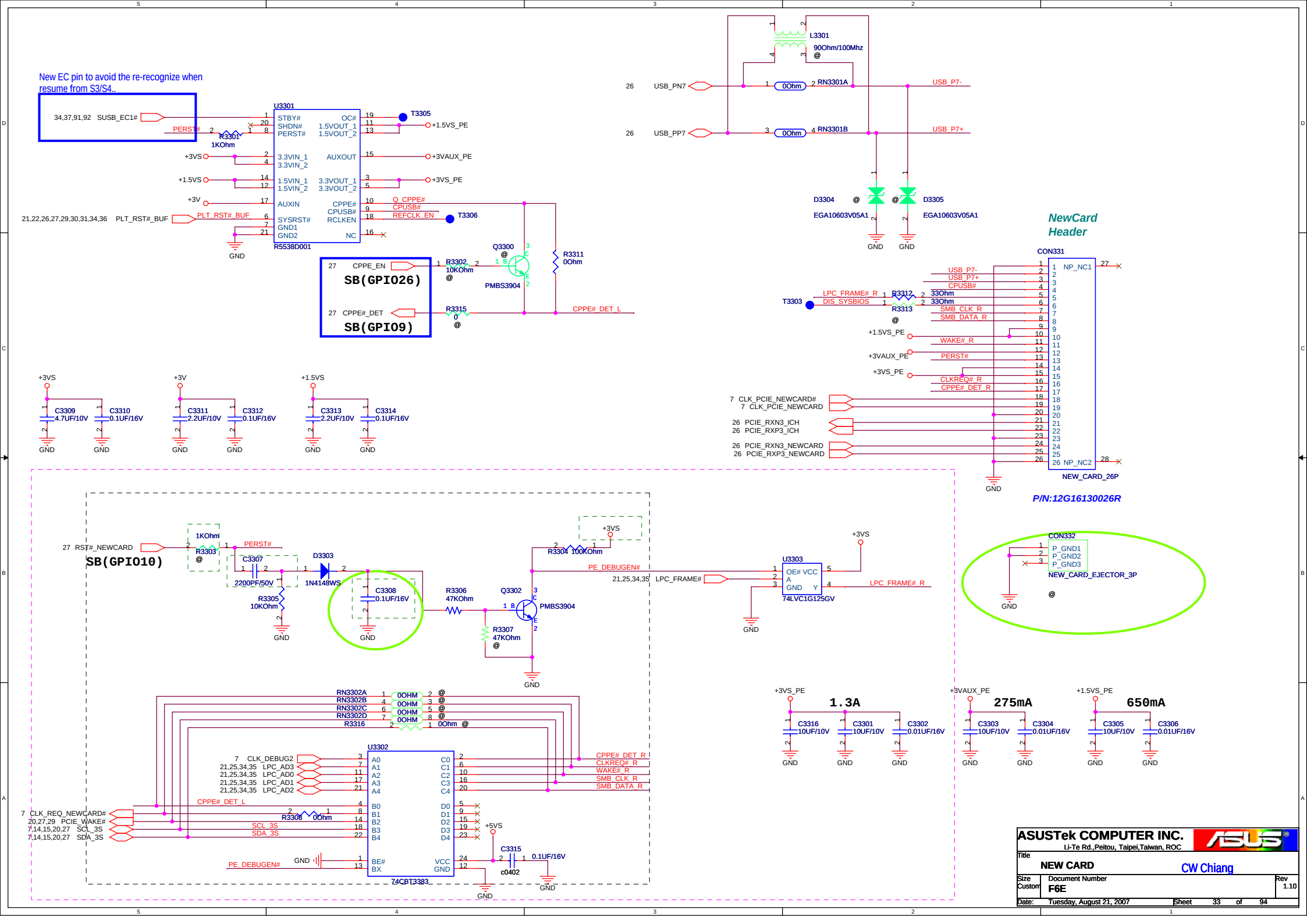
Engineer: CW Chiang

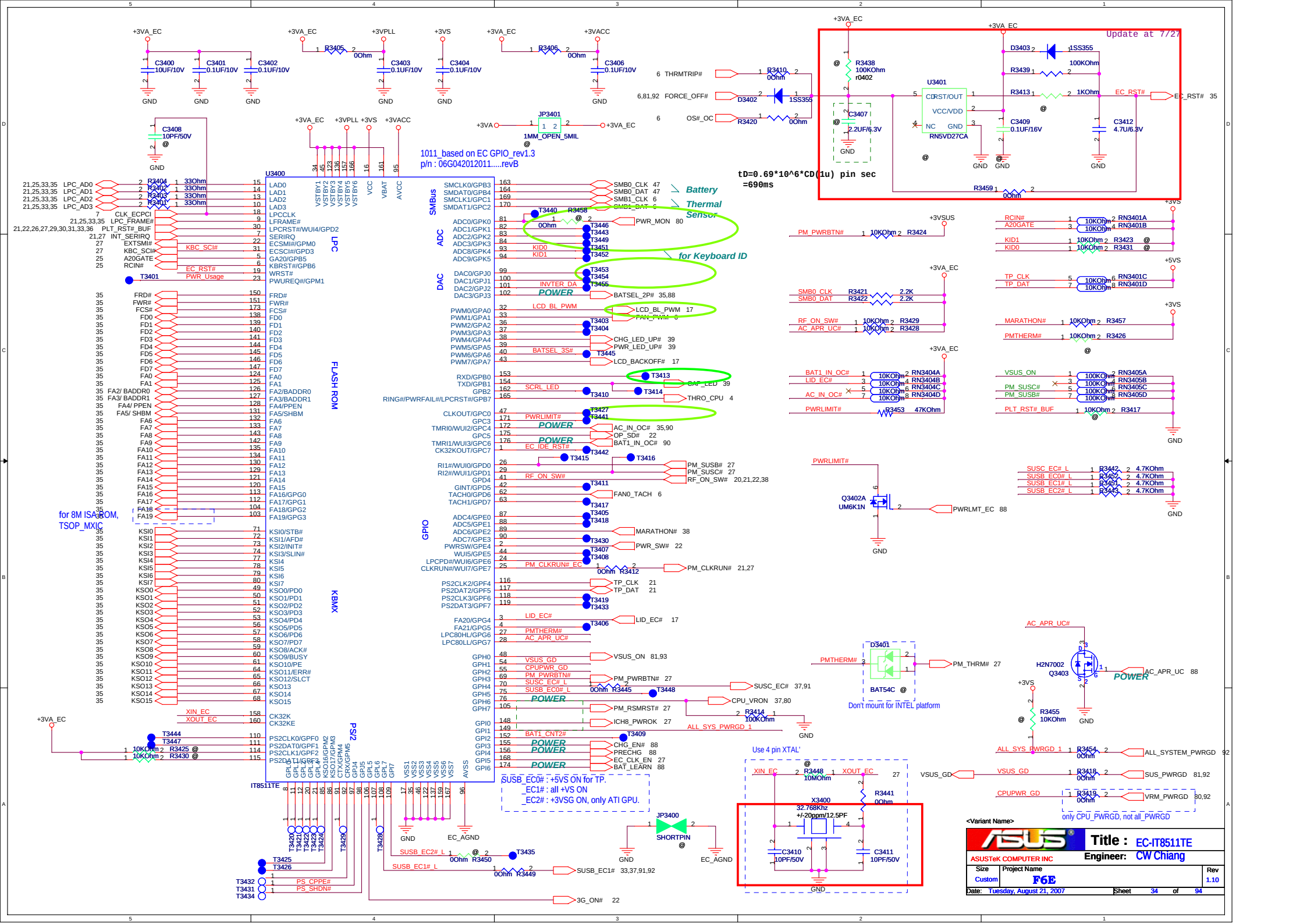
Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 31 of 94

<Variant Name>

ASUSTeK COMPUTER INC	Title : EMPTY Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 32 of 94	


New EC pin to avoid the re-recognize when resume from S3/S4..
34,37,91,92 SUSB_EC1#
U3301
PERST#
R3301 1KOhm
STBY# SHDN# PERST#
OC# 1.5VOUT_1 1.5VOUT_2
3.3VIN_1 3.3VIN_2
AUXOUT
1.5VIN_1 1.5VIN_2
3.3VOUT_1 3.3VOUT_2
AUXIN
SYSRST# GND1 GND2
CPPE# CPUSB# RCLKEN
NC
R5538D001
T3305
+1.5VS_PE
+3VAUX_PE
+3VS_PE
Q_CPPE#
CPUSB#
REFCLK_EN
T3306
+3VS
+1.5VS
+3V
21,22,26,27,29,30,31,34,36 PLT_RST#_BUF
GND
27 CPPE_EN
SB(GPIO26)
27 CPPE#_DET
SB(GPIO9)
R3302 10KOhm @
Q3300 @
PMBS3904
R3311 0Ohm
R3315 0 @
CPPE# DET L
L3301
90Ohm/100Mhz @
26 USB_PN7
26 USB_PP7
0Ohm
RN3301A
RN3301B
USB_P7-
USB_P7+
D3304 @
D3305 @
EGA10603V05A1
NewCard Header
CON331
NP_NC1
NP_NC2
NEW_CARD_26P
T3303
LPC_FRAME# R
DIS_SYSBIOS
R3312 33Ohm
R3313 33Ohm @
SMB_CLK_R
SMB_DATA_R
WAKE# R
PERST#
CLKREQ# R
CPPE# DET R
7 CLK_PCIE_NEWCARD#
7 CLK_PCIE_NEWCARD
26 PCIE_RXN3_ICH
26 PCIE_RXP3_ICH
26 PCIE_RXN3_NEWCARD
26 PCIE_RXP3_NEWCARD
P/N:12G16130026R
C3309 4.7UF/10V
C3310 0.1UF/16V
C3311 2.2UF/10V
C3312 0.1UF/16V
C3313 2.2UF/10V
C3314 0.1UF/16V
27 RST#_NEWCARD
SB(GPIO10)
R3303 1KOhm @
C3307 2200PF/50V
R3305 10KOhm
D3303 1N4148WS
C3308 0.1UF/16V
R3306 47KOhm
Q3302 PMBS3904
R3307 47KOhm @
R3304 100KOhm
PE_DEBUGEN#
21,25,34,35 LPC_FRAME#
U3303
74LVC1G125GV
CON332
P_GND1
P_GND2
P_GND3
NEW_CARD_EJECTOR_3P
RN3302A 0OHM @
RN3302B 0OHM @
RN3302C 0OHM @
RN3302D 0OHM @
R3316 0Ohm @
U3302
74CBT3383
7 CLK_DEBUG2
21,25,34,35 LPC_AD3
21,25,34,35 LPC_AD0
21,25,34,35 LPC_AD1
21,25,34,35 LPC_AD2
CPPE# DET R
CLKREQ# R
WAKE# R
SMB_CLK_R
SMB_DATA_R
7 CLK_REQ_NEWCARD#
20,27,29 PCIE_WAKE#
7,14,15,20,27 SCL_3S
7,14,15,20,27 SDA_3S
SCL_3S
SDA_3S
R3308 0Ohm
PE_DEBUGEN#
+5VS
C3315 0.1UF/16V c0402
+3VS_PE 1.3A
C3316 10UF/10V
C3301 10UF/10V
C3302 0.01UF/16V
+3VAUX_PE 275mA
C3303 10UF/10V
C3304 0.01UF/16V
+1.5VS_PE 650mA
C3305 10UF/10V
C3306 0.01UF/16V
ASUSTek COMPUTER INC.
Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
NEW CARD
CW Chiang
Size Custom
Document Number F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 33 of 94


Update at 7/27
1011_based on EC GPIO_rev1.3
p/n : 06G042012011.....revB
tD=0.69*10^6*CD(1u) pin sec
=690ms
Battery
Thermal
Sensor
for Keyboard ID
POWER
for 8M ISA ROM,
TSOP_MXIC
Don't mount for INTEL platform
Use 4 pin XTAL'
SUSB_EC0# : +5VS ON for TP.
_EC1# : all +VS ON
_EC2# : +3VSG ON, only ATI GPU.
only CPU_PWRGD, not all_PWRGD
U3400
IT8511TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
Title : EC-IT8511TE
ASUSTeK COMPUTER INC
Engineer: CW Chiang
Size: Custom
Project Name: F6E
Rev: 1.10
Date: Tuesday, August 21, 2007
Sheet 34 of 94

EC Hardware Strapping

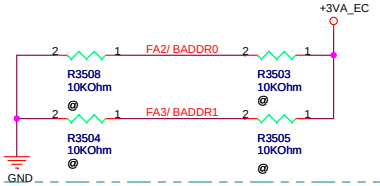
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

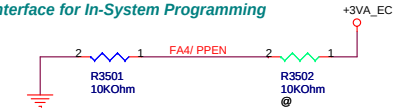


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

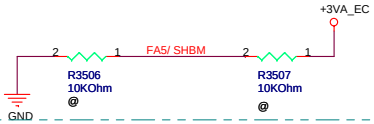
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

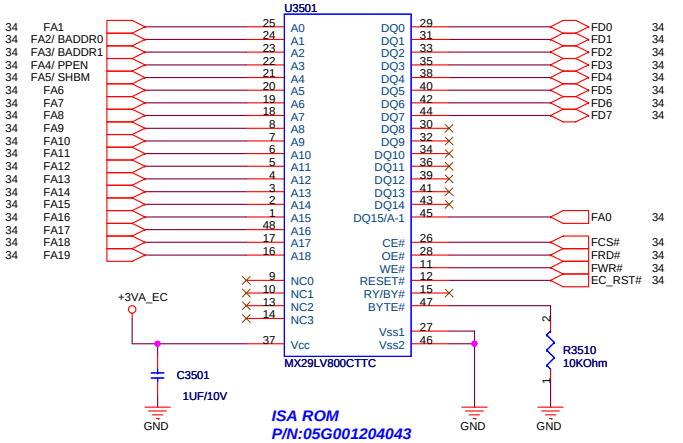
0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



ISA ROM_TSOP

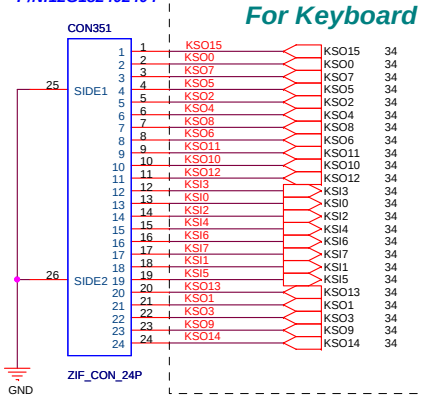
8M TSOP _ MXIC

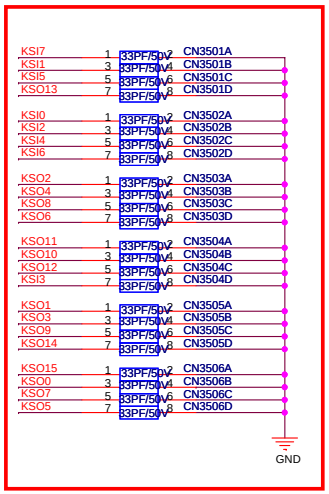


ISA ROM
P/N:05G001204043

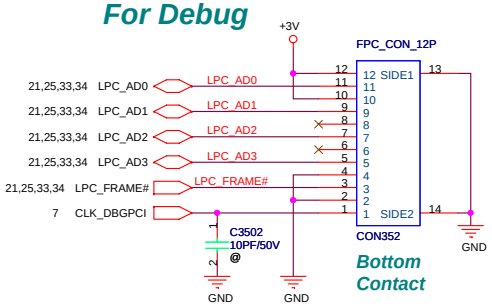
For Keyboard

P/N:12G182402404

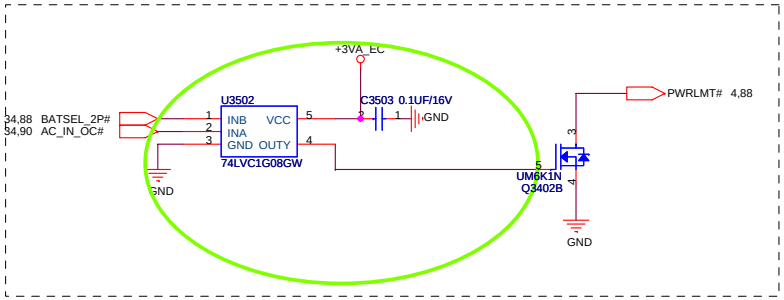




For Debug



PWRLMT Circuit: For 65W adaptor.



<Variant Name>

ASUSTeK COMPUTER INC

Title : ISA_ROM&KB conn

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 35 of 94

Update at 7/27

PLT_RST#_BUF 21,22,26,27,29,30,31,33,34

Pull down 10K: 3 in 1 mode
Stuff 47P: Support suspend mode in CPU's C3

C-L-C Filter

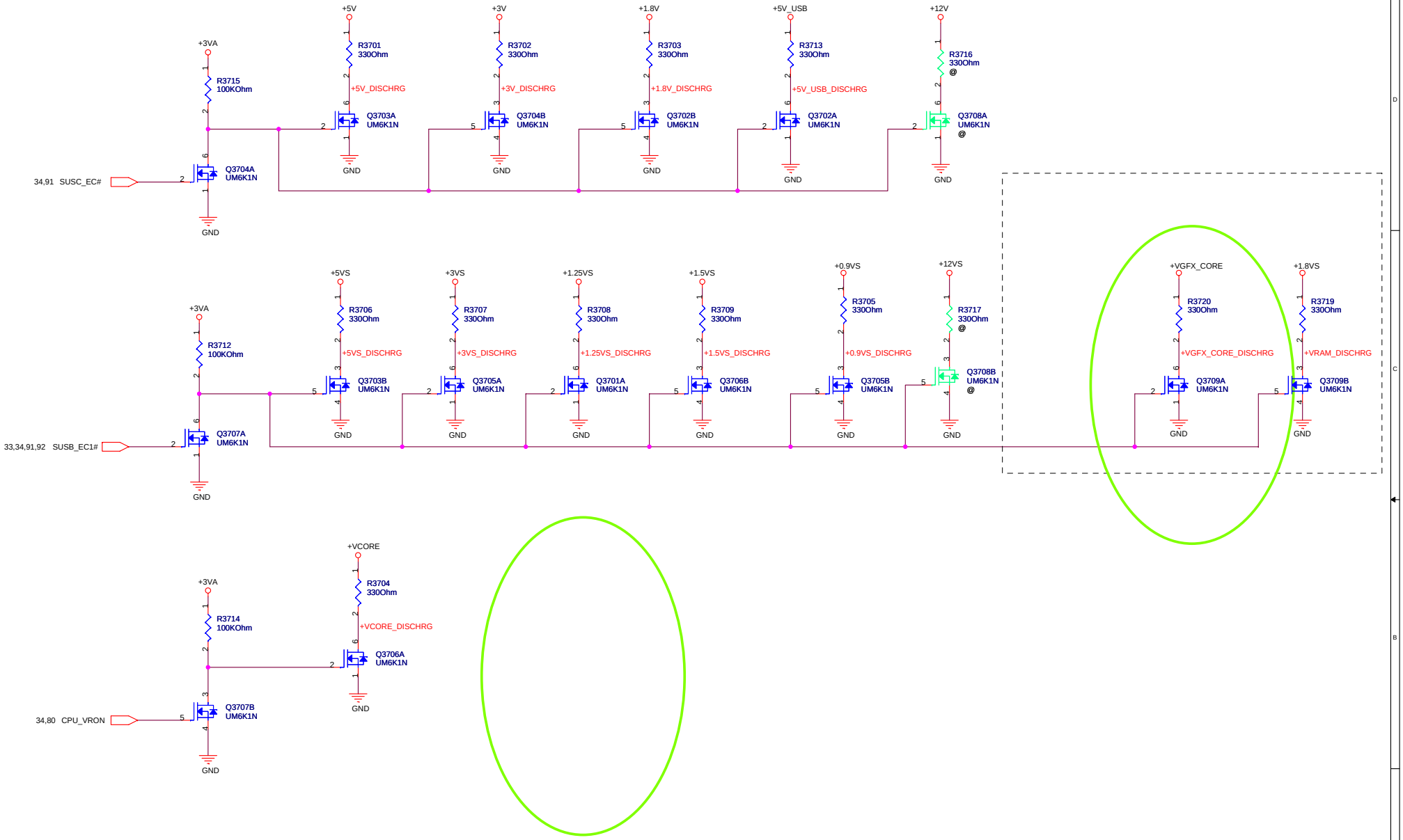
Reserve R for Eye Diagram

P/N:12G340003810

Max: 250mA Max: 220mA

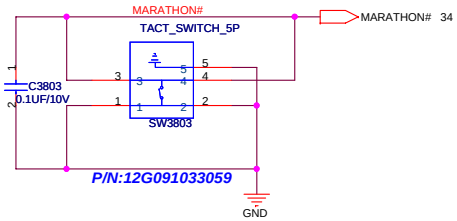
Max: 120mA

Title :	CR RTS-5158 & 4-in-1 CON		
ASUSTeK COMPUTER INC		Engineer:	CW Chiang
Size	Project Name		Rev
Custom	F6E		1.10
Date:	Tuesday, August 21, 2007	Sheet	36 of 94



<Variant Name>

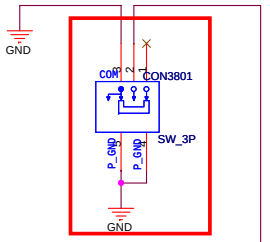
ASUSTeK COMPUTER INC	Title : DISCHARGE	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 37 of 94	



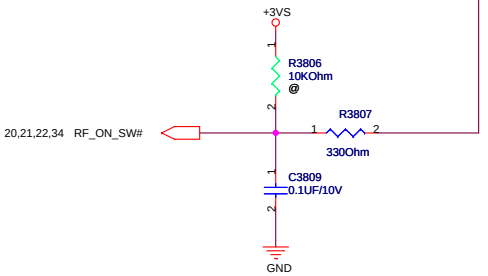
P/N:12G091033059

MARATHON#

P/N:12G09107003M



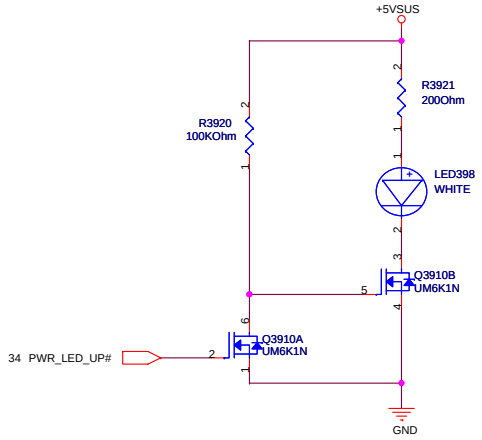
BT/WLAN SW



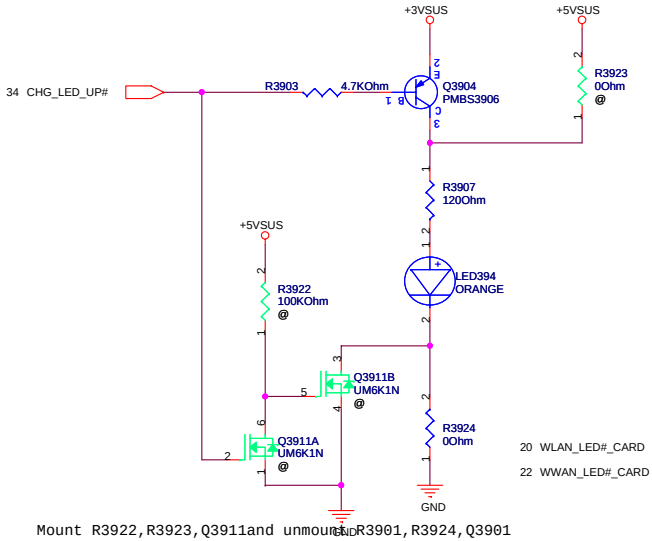
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 38 of 94	

PWR LED

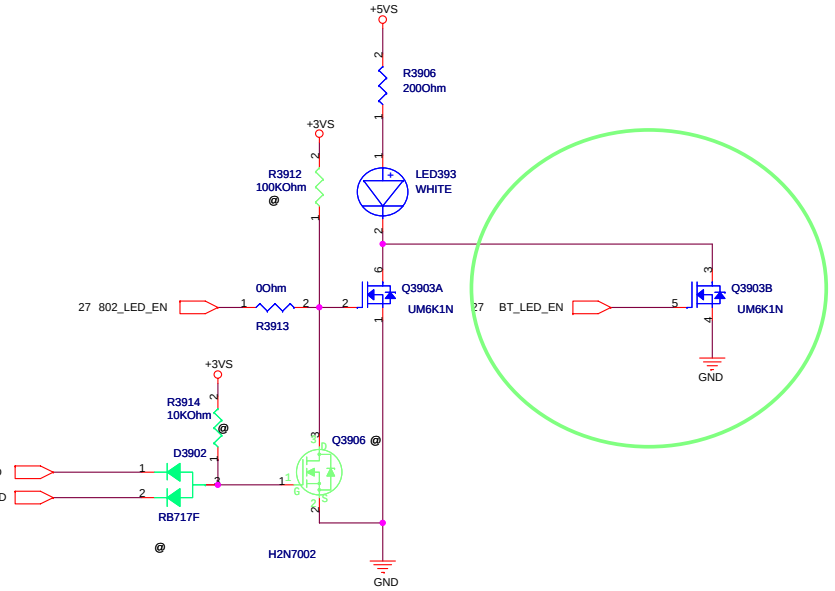


For BATTERY LED

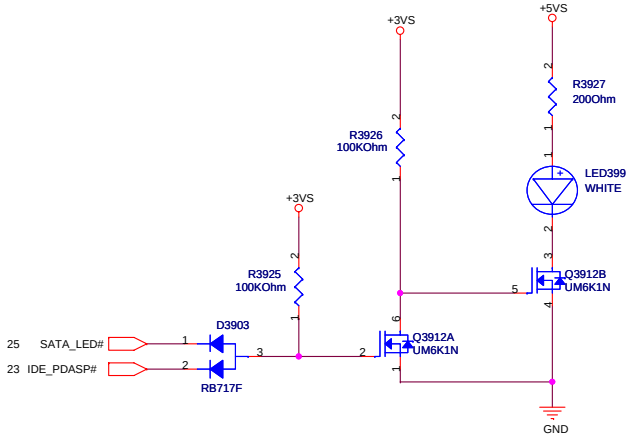


Mount R3922,R3923,Q3911and unmount R3901,R3924,Q3901 for white LED test.

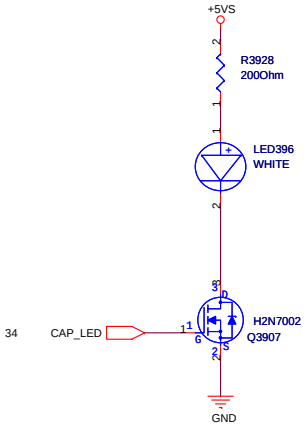
For WireLess & BT LED



SATA/IDE LED



For Cap. Lock



<Variant Name>

ASUSTeK COMPUTER INC

Title : LEDs

Engineer: CW Chiang

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 39 of 94

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 40 of 94

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC.

Engineer:

Size	Project Name	Rev
C	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 41 of 94

<variant_name><Variant Name></variant_name>

ASUSTeK COMPUTER INC

Title : EMPTY

Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 42 of 94

<variant_name><Variant Name></variant_name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 43 of 94

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 44 of 94

<Variant Name>

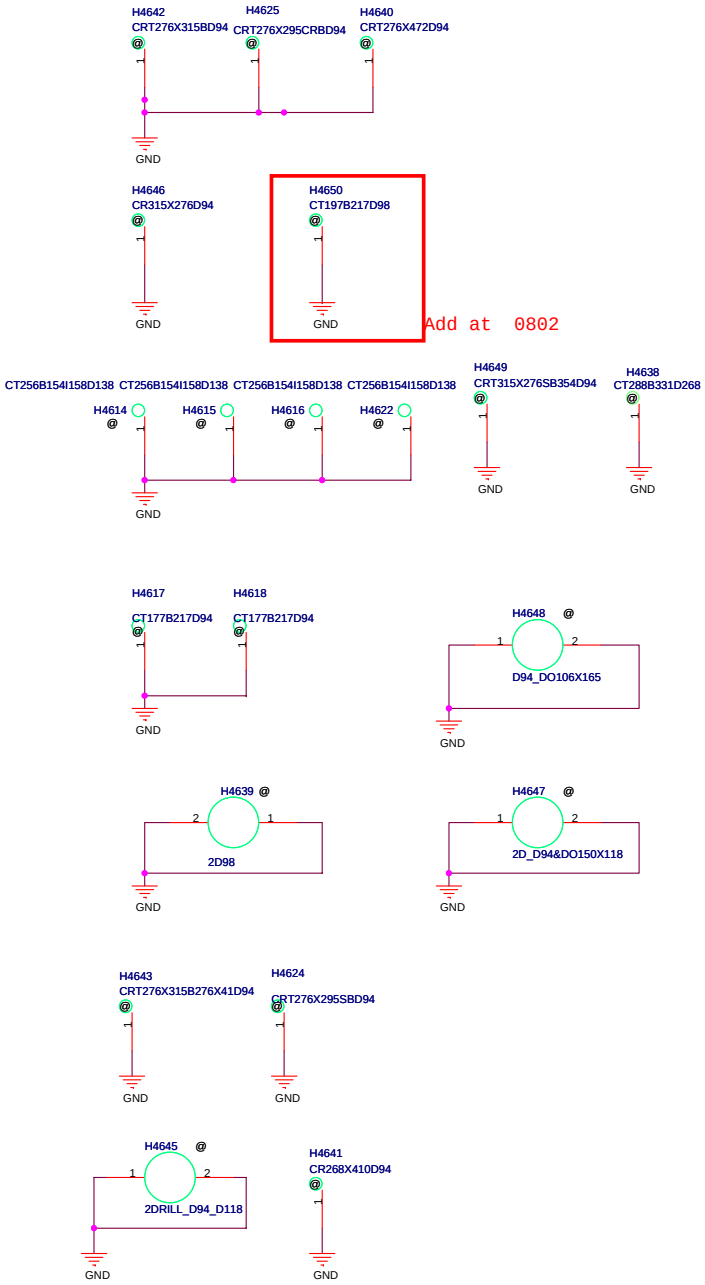
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

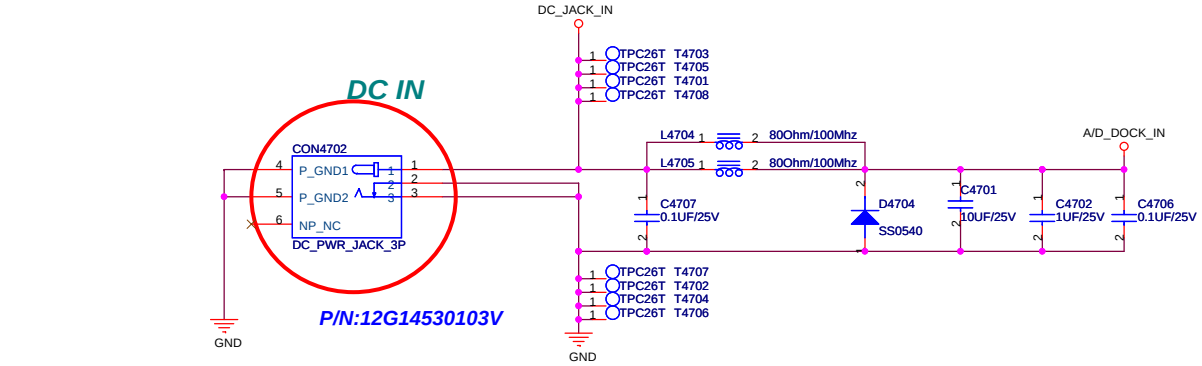
Size	Project Name	Rev
Custom	F6E	1.10

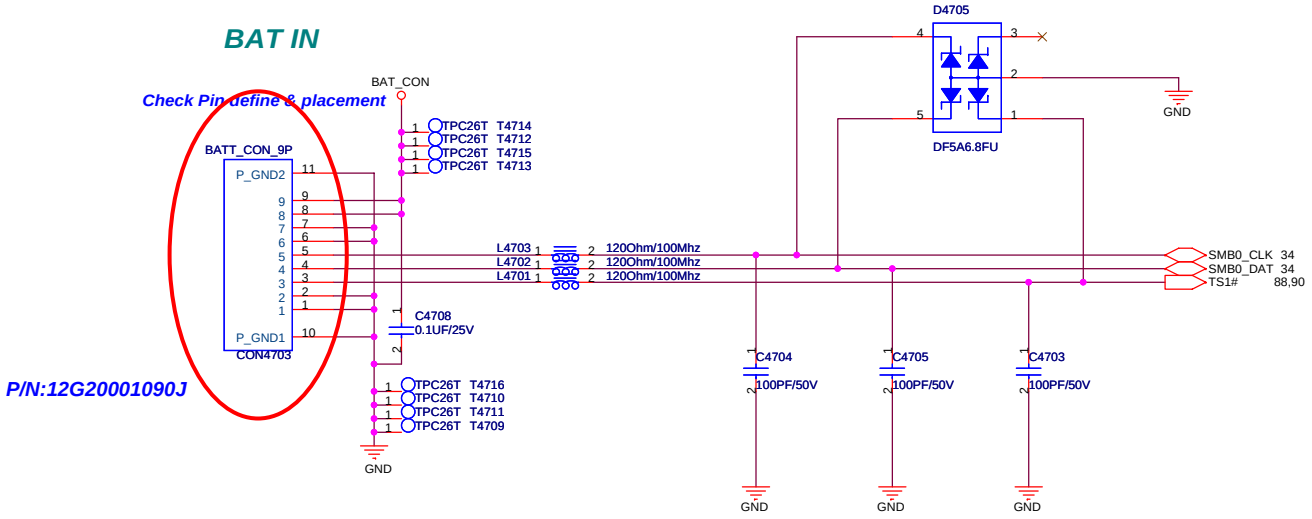
Date: Tuesday, August 21, 2007 Sheet 45 of 94



<Variant Name>

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 46 of 94	





<Variant Name>

ASUSTeK COMPUTER INC	Title : DC & BAT IN	
	Engineer: CW Chiang	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 47 of 94	

Rev0.3(Change List from R0.2 to R0.3)

1.Page 35: Add C3504-C3527 for EMI Requirement
2.Page 29 and 36: Add PLT_RSTNS# Connect to Lan and Card Reader Reset Pin
3.Page 34: Add EC Reset Circuit
4.Page 81: Change L8100 and L8101 from height = 4.5mm to 4.0mm
5.Page 46: Add H4638 for Antenna
6.Page 22: Change CON2201(BtoB Conn) Pin Define(Follow IO Board)
7.Page 19: Swap Signal Between CON1902 (HDMI Connector) and CHOKE
8.Page 86: Remove VGA Vcore Circuit
9.Page 11: Remove JP1102 and JP1103
10.Page 31: Swap D3101
11.Page 34: Add R3458
12.Page 11: Add CE1103 for VGFX_CORE

Rev0.4(Change List from R0.3 to R0.4)

13.Page 36: Remove C3619
14.Page 31: Swap L3110 RN3101 D3101
15.Page 38: Change SW3803 to 12G091033059
16.Page 92 Page 93: Remove GFX_PWRGD, +VCCFX_CORE
17.Page 27: Modify SM BUS Signal
18.Page 06: Remove Q9201
19.Page 22: R3803 rename to R2201,C3805 rename to C2207
20.Page 38: CON4707 rename to CON3801
21.Page 35: Change C3504 - C3527 to CN3501 - CN3506
22.Page 47: Change Batt Connector From 12G200010901 to 12G20001090J
23.Page 81 Page82: Power remove CE8101 CE8103 CE8204

Rev0.5(Change List from R0.4 to R0.5)

24.Page 07: Remove Q0701
25.Page 38: CON3801 Pin1 Pin2 swap
26.Page 17: Change L1708 to R1708 (0603 100ohm)
27.Page 82: Remove JP8202 JP8206
28.Page 26: Change U2603 to 06G004603219 for cost down
29.Page 26 35: Change U2602 U3502 to 06G004092010 for cost down
30.Page 07 20: Remove CLK_REQ_MINICARD and R0734
31.Page 28: Change C2812 to 11G235210615320 for cost down
32.Page 28: Add C2838 for VCCP_ICH
33.Page 06: Add R0671 for PM_THRMTRIP# Pull Up.
34.Page 16: Add C1602 C1603 for VTT_REF +0.9VS
35.Page 27: Modify ICH8_PWROK circuit for Leakage issue(ADD R2754 D2702)
36.Page 24: Change R2411 from 0603 to 0805
37.Page 17: Add R1709 for CCD
38.Page 26 27: Change USB_OC# Pull High Circuit and Add R2615 R2616 R2757 R2758
39.Page 31: Add C3175 C3176 for eSATA(JMicron suggested)
40.Page 35: Remove R3509
41.Page 34: Add T3449
42.Page 19: Change R1903~R1910 to RN1901~RN1904
43.Page 37: Remove +VCCP Discharge Circuit
44.Page 34: Remove R3432 R3433
45.Page 27: Add D2703 for Leakage Issue
46.Page 24: Change ESD Diode D2401 D2402 to D2405, D2403 D2404 to D2406 for cost
47.Page 33: Change C3308 from 0603 to 0402

Rev0.6(Change List from R0.5 to R1.0)

48.Page 39: Remove R3907 R3909 LED394 LED395 Q3905 Add Q3907 for 5 LED Lights
49.Page 47: Change ESD Diode D4701 D4702 D4703 to D4705
50.Page 31: Change eSATA Connector to 12G142001110
51.Page 35: Change Debug Connector to 12G183301208
52.Page 28: Change JP2802
53.Page 39: Modify LED Circuits for White LED
54.Page 46: Update Screw Hold
55.Page 17 19 24 31 33: Change Co-lay resistance from 0402 to 0603
56.Page 6 Rename +5VS to +5VS_FAN for FAN Power(Power request)
57.Page 28: Change C2801 C2802 0.1uF (0402) to 1uF (0603)
58.Page 46: Remove JP4601
59.Page 39: Change R3926 connect to +3VS
60.Page 36: Change RST5158 Reset Pin Connect to PLT_RST#_BUF
61.Page 27: Remove D2702 D2701 due to the ITE 8511 set the GPIO to OPEN-DRAIN
62.Page 34: Remove D3404 and Unmount Reset IC (EC_RST# By RC)
63.Page 29: Add C2941 for +1.8V_LAN
64.Page 17: Change R1705 to 330 ohm for LCD Power Sequence
65.Page 29: Change R2903 from 2.49K ohm to 2.21K ohm for GigaLan eye patterm
66.Page 24: Change USB Connector CON2402 CON2403 to 12G131050044
67.Page38: Change Slide Switch CON3801 to 12G09107003M
68.Page17: Change LVDS Connector CON175 to 12G17001030V
69.Page 29: Change R2903 from 2.21K ohm to 2.49K ohm
70.Page 25: Change R2525 from 24.9 ohm to 22.6 ohm for SATA
71.Page 21: Add R2111 R2112 (PLT_RST#_BUF) Connected to CON2104 for Finger Printer Issue
72.Page 29: Del C2924 Change C2841 to 22UF/10V
73.Page 28: Change JP2802 to 2MM size
74.Page 27: Add D2701 D2702 R2759 R2760 for ICH8_PWROK PM_RSMRST# Leakage Issue.
75.Page 31: Add C3148 4.7uF/6.3V for DVDD1.8V
76.Page 31: Remove Extra eSATA Reset Circuit (Remove U3103 R3115 C3155 C3154)
77.Page 34: Add R3459 for EC_RST#
78.Page 28: Change JP2802 to JP8206(+VCCP change to +1.05VO)
79.Page 29: Change L2903 L2905 L2906 to R2929 R2930 R2931
80.Page 31: Change R3135 to 57.6K ohm

<Variant Name>

ASUSTeK COMPUTER INC

Title : History(1)

Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 48 of 94

<Variant Name>

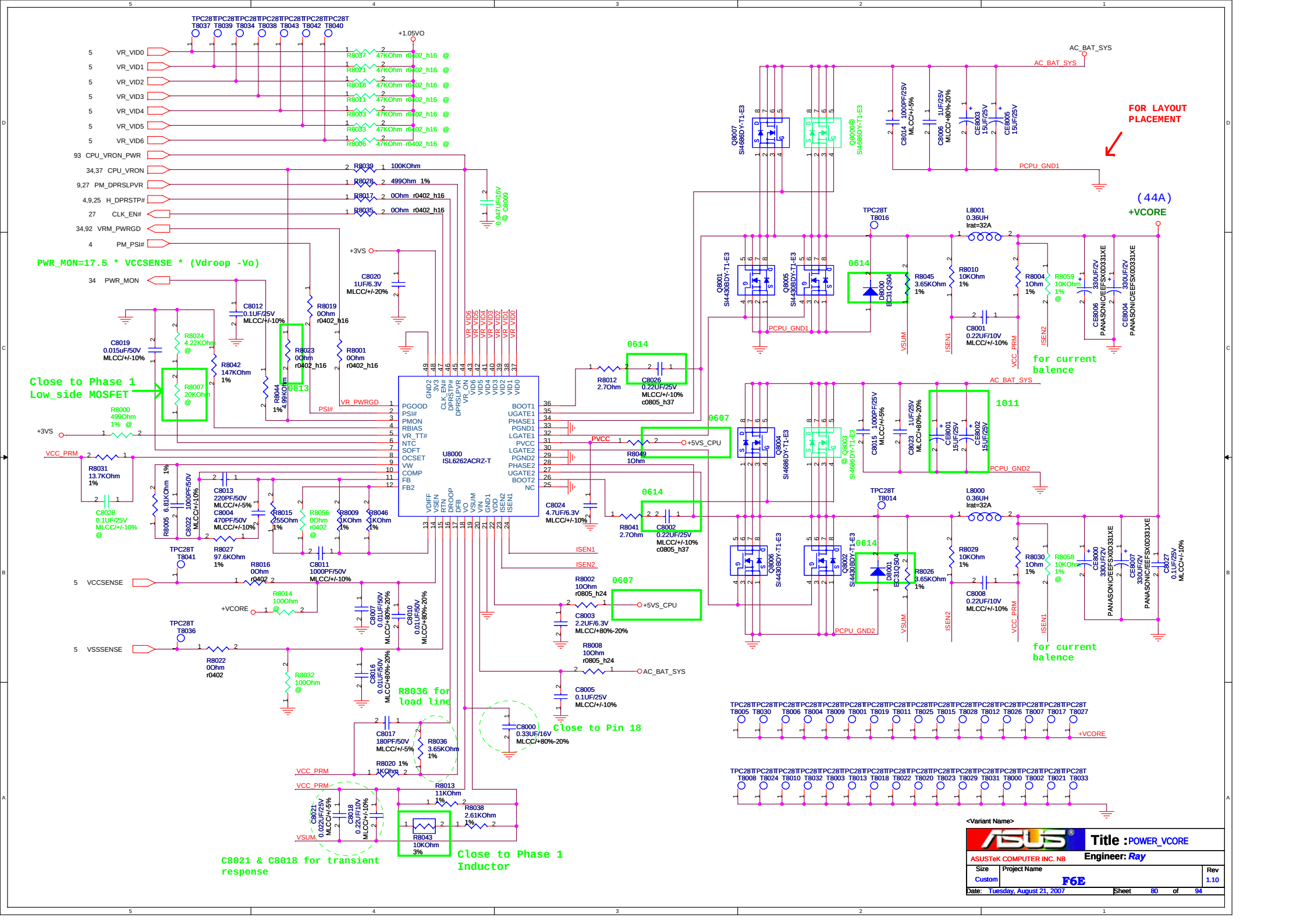
Title : History(2)

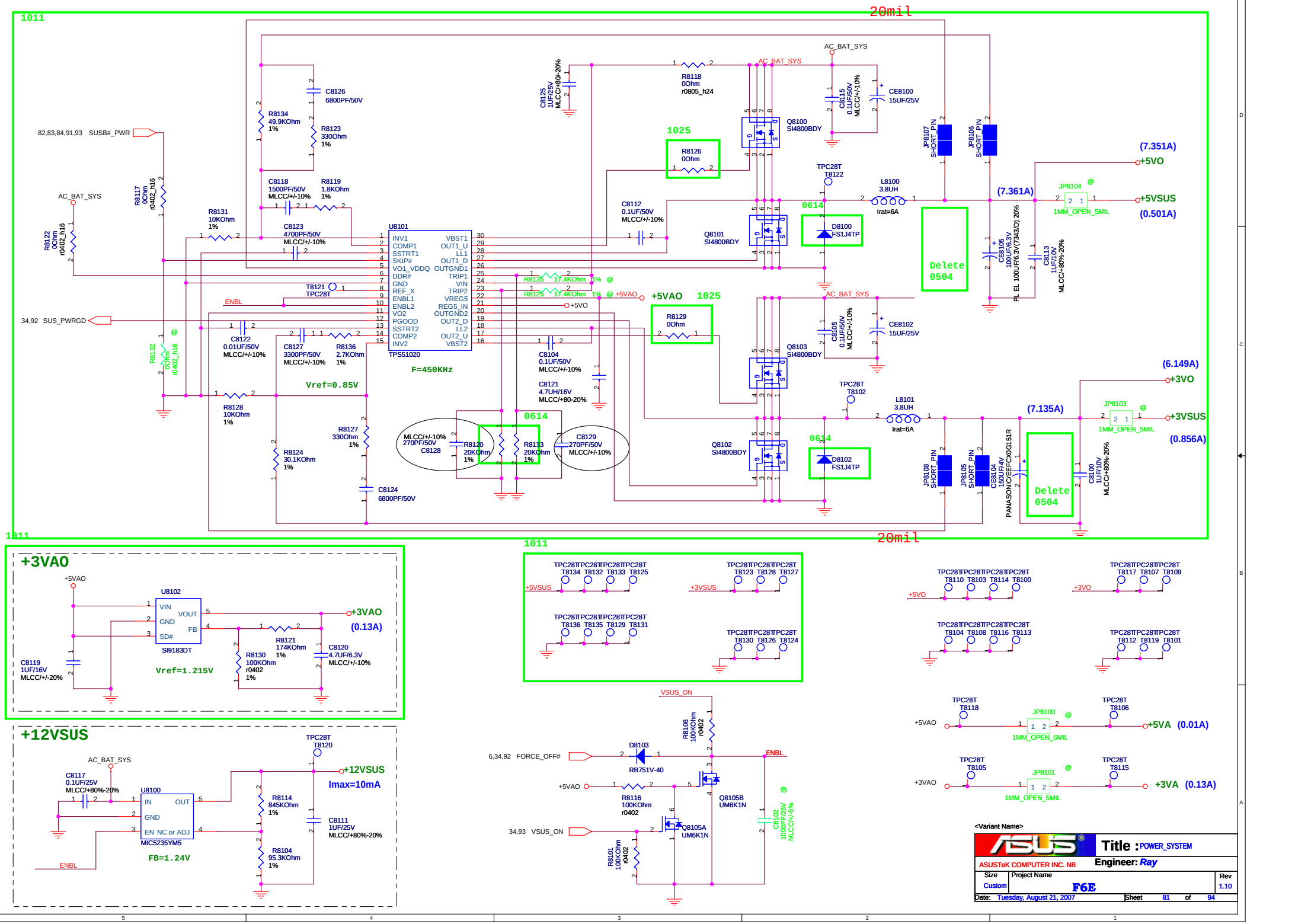
ASUSTeK COMPUTER INC

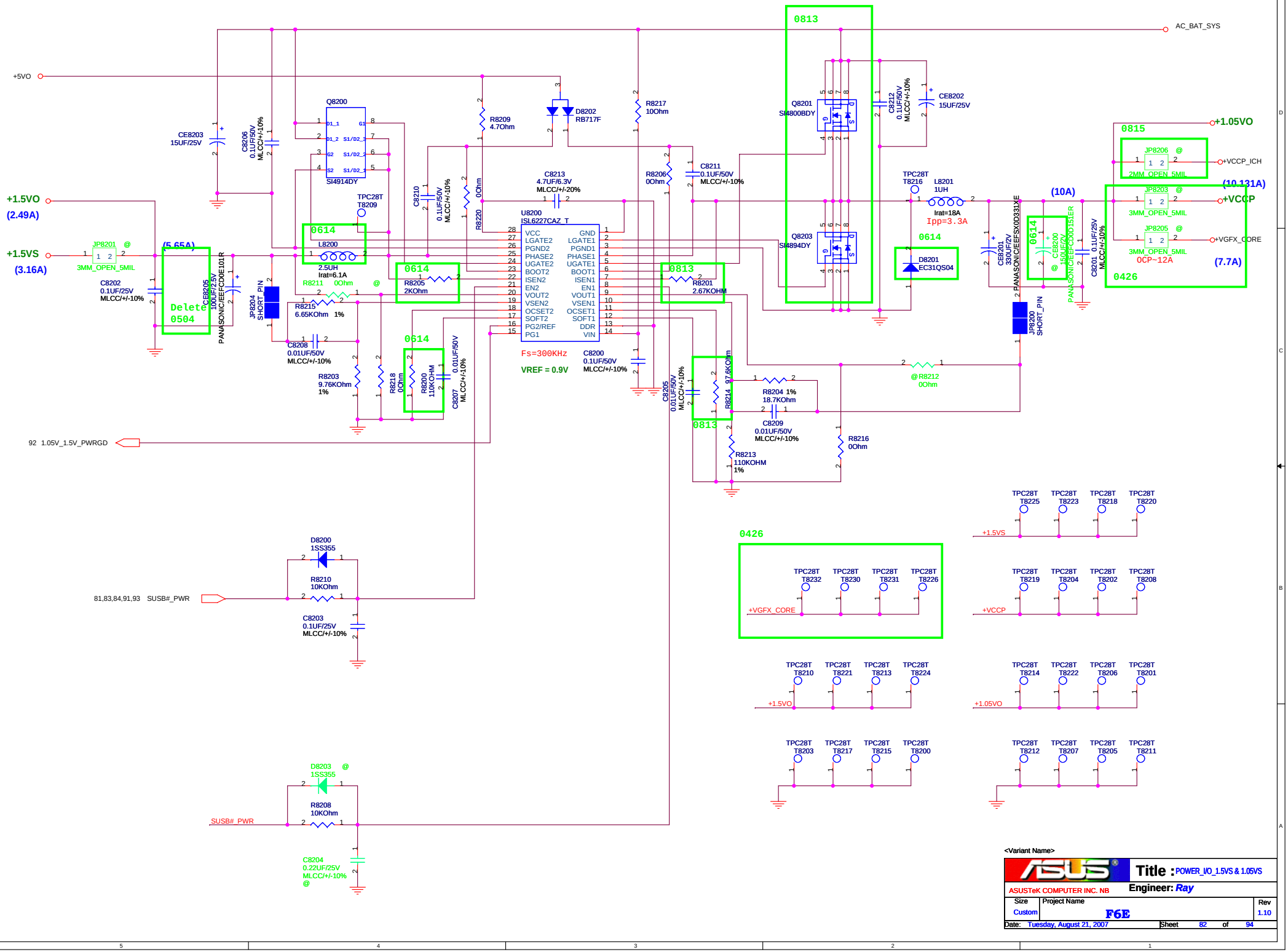
Engineer:

Size	Project Name	Rev
Custom	F6E	1.10

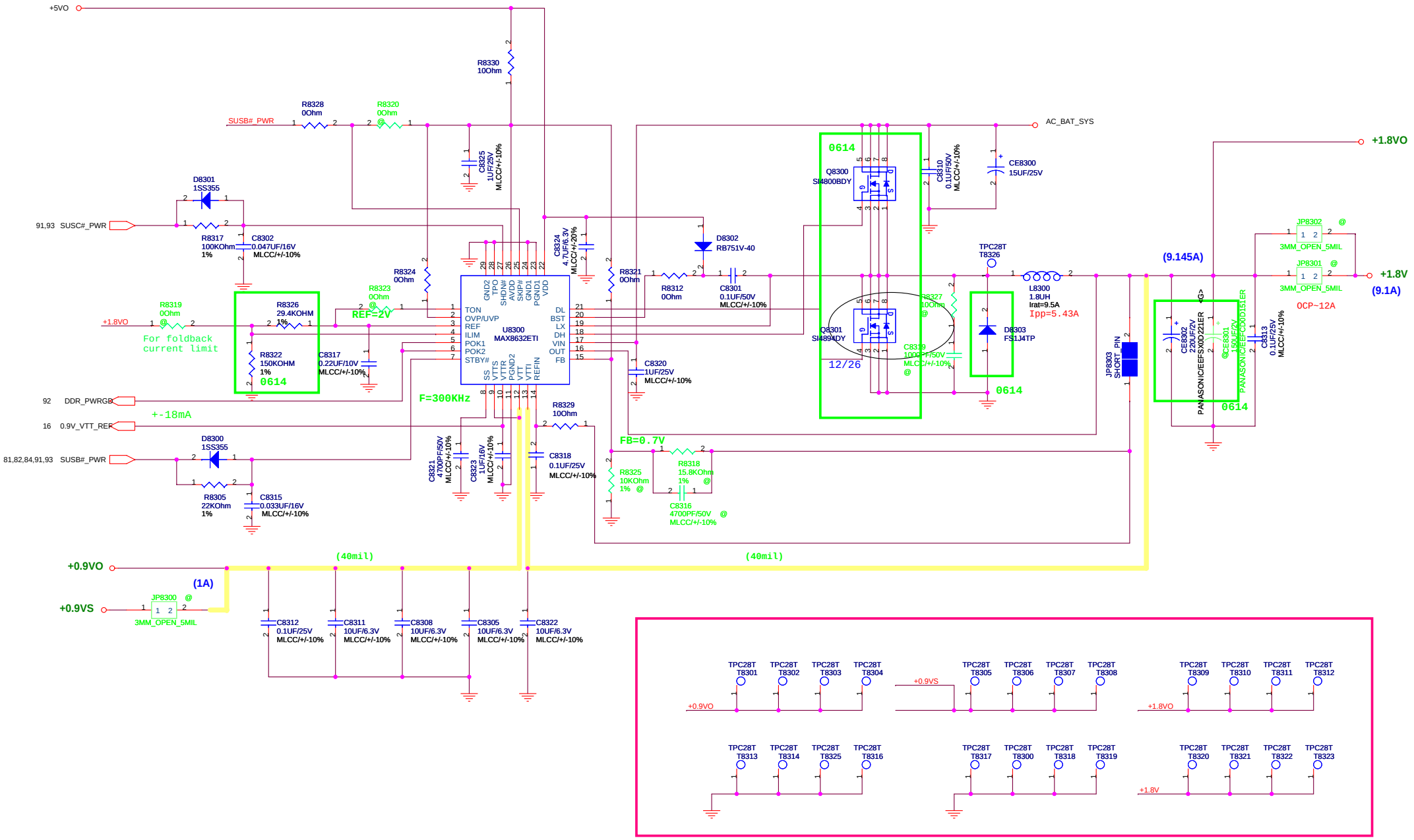
Date: Tuesday, August 21, 2007 Sheet 49 of 94


PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to Phase 1 Low_side MOSFET
U8000 ISL6262ACRZ-T
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND1
VDD
ISEN2
ISEN1
R8036 for load line
Close to Pin 18
C8021 & C8018 for transient response
Close to Phase 1 Inductor
FOR LAYOUT PLACEMENT
(44A)
+VCORE
for current balence
for current balence
AC_BAT_SYS
PCPU_GND1
PCPU_GND2
+5VS_CPU
+1.05VO
+3VS
VCC_PRM
PVCC
PSI#
ISEN1
ISEN2
VSUM
VCCSENSE
VSSSENSE
+VCORE
0614
0607
0813
1011
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Ray
Size: Custom
Project Name: F6E
Rev: 1.10
Date: Tuesday, August 21, 2007
Sheet 80 of 94


1011
20mil
82,83,84,91,93 SUSB#_PWR
AC_BAT_SYS
34,92 SUS_PWRGD
ENBL
U8101
TPS51020
F=450KHz
Vref=0.85V
+5VAO
+5VO
1025
0614
Delete 0504
(7.351A)
+5VO
(7.361A)
+5VSUS
(0.501A)
(6.149A)
+3VO
(7.135A)
+3VSUS
(0.856A)
+3VA0
U8102
SI9183DT
Vref=1.215V
+3VAO
(0.13A)
+12VSUS
Imax=10mA
U8100
MIC5235YM5
FB=1.24V
6,34,92 FORCE_OFF#
34,93 VSUS_ON
D8103
RB751V-40
Q8105B UM6K1N
Q8105A UM6K1N
+5VA (0.01A)
+5VA (0.13A)
<Variant Name>
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Ray
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 81 of 94


AC_BAT_SYS
+5VO
+1.5VO
(2.49A)
+1.5VS
(3.16A)
+1.05VO
(10.131A)
+VCCP
(10A)
+VGFX_CORE
(7.7A)
0813
0614
0815
0426
0504
Delete
U8200
ISL6227CAZ_T
Fs=300KHz
VREF = 0.9V
Q8200
SI4914DY
Q8201
SI4800BDY
Q8203
SI4894DY
D8202
RB717F
D8201
EC31QS04
L8200
2.5UH
Irat=6.1A
L8201
1UH
Irat=18A
Ipp=3.3A
OCP~12A
JP8201
JP8204
JP8205
JP8206
JP8207
JP8200
3MM_OPEN_5MIL
2MM_OPEN_5MIL
SHORT_PIN
92 1.05V_1.5V_PWRGD
81,83,84,91,93 SUSB#_PWR
SUSB#_PWR
D8200
1SS355
D8203
1SS355
R8209 4.7Ohm
R8217 10Ohm
R8206 0Ohm
R8220 0Ohm
R8210 10KOhm
R8208 10KOhm
R8215 6.65KOhm 1%
R8203 9.76KOhm 1%
R8218 0Ohm
R8200 110KOHM
R8205 2KOhm
R8201 2.67KOHM
R8214 97.6KOhm
R8204 1% 18.7KOhm
R8213 110KOHM 1%
R8216 0Ohm
R8211 0Ohm
@R8212 0Ohm
C8213 4.7UF/6.3V MLCC/+/-20%
C8211 0.1UF/50V MLCC/+/-10%
C8212 0.1UF/50V MLCC/+/-10%
C8210 0.1UF/50V MLCC/+/-10%
C8200 0.1UF/50V MLCC/+/-10%
C8205 0.01UF/50V MLCC/+/-10%
C8207 0.01UF/50V MLCC/+/-10%
C8208 0.01UF/50V MLCC/+/-10%
C8209 0.01UF/50V MLCC/+/-10%
C8203 0.1UF/25V MLCC/+/-10%
C8204 0.22UF/25V MLCC/+/-10% @
C8202 0.1UF/25V MLCC/+/-10%
C8206 0.1UF/50V MLCC/+/-10%
CE8203 15UF/25V
CE8202 15UF/25V
C8201 0.1UF/25V MLCC/+/-10%
CE8201 330UF/2V PANASONIC/EEFSX0D331XE
CE8200 150UF/2V @ PANASONIC/EEFCD0D151ER
C8205 100UF/2.5V PANASONIC/EEFCD0E101R
TPC28T T8209
TPC28T T8216
TPC28T T8225 TPC28T T8223 TPC28T T8218 TPC28T T8220
TPC28T T8232 TPC28T T8230 TPC28T T8231 TPC28T T8226
TPC28T T8219 TPC28T T8204 TPC28T T8202 TPC28T T8208
TPC28T T8210 TPC28T T8221 TPC28T T8213 TPC28T T8224
TPC28T T8214 TPC28T T8222 TPC28T T8206 TPC28T T8201
TPC28T T8203 TPC28T T8217 TPC28T T8215 TPC28T T8200
TPC28T T8212 TPC28T T8207 TPC28T T8205 TPC28T T8211
+1.5VS
+VCCP
+1.05VO
+VCCP_ICH
+VGFX_CORE
<Variant Name>
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC. NB
Engineer: Ray
Size Custom
Project Name F6E
Rev 1.10
Date: Tuesday, August 21, 2007
Sheet 82 of 94

1011



<Variant Name>

Title : POWER_I/O_DDR & VTT

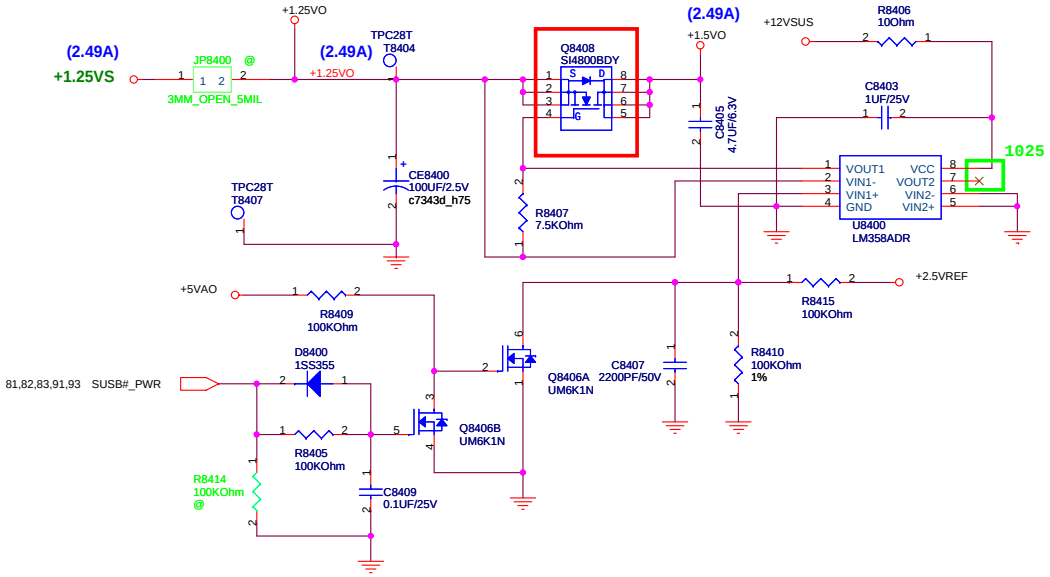
ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 83 of 94

+1.25VS



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_ +1.25VS

Engineer: Ray

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 84 of 94

```
delete +VRAM &VGA_core
```

<Variant Name>

Title : POWER_VGA_CORE & RAM

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
C	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 85 of 94

<Variant Name>

Title : POWER_+VCCFX_CORE

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
B	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 86 of 94

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_SHUTDOWN#	
	Engineer: Ray	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 87 of 94	

POWER PATH & BAT_LEARN

65 WATT

070115

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

AC_IN Threshold: 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R5710=20K,R5715=30K

VCLS=3.6855V
=> Iin(max)=3.272A
=> Constant Power = 19 * 4.5 = 62.2W
=> R5710=20K,R5715=137K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA

90W->10m Ohm
65W->20m Ohm

90W->30K Ohm
65W->137K Ohm

mount: 4S
unmount: 3S

Iin=3.28A

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_CHARGER

Engineer: Ray

Size	Project Name	Rev
C	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 88 of 94

<Variant Name>

Title : N/A

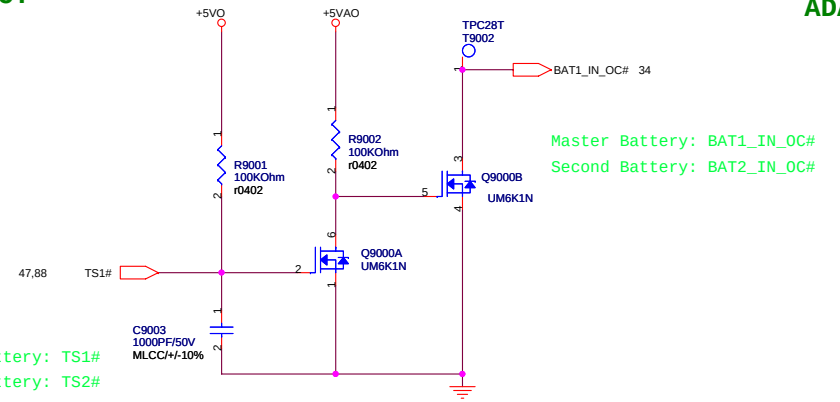
ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 89 of 94

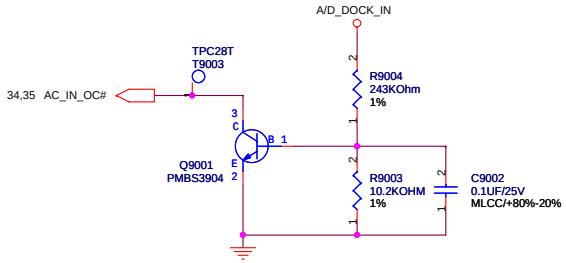
BATTERY IN DETECT



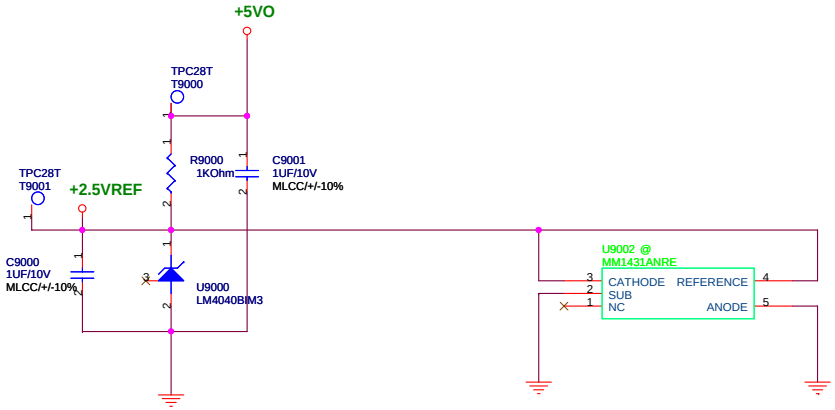
Master Battery: TS1#
Second Battery: TS2#

Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

ADAPTER IN DETECT



+2.5VREF



U9000 & U9002 colay

<Variant Name>

Title : POWER_DETECT

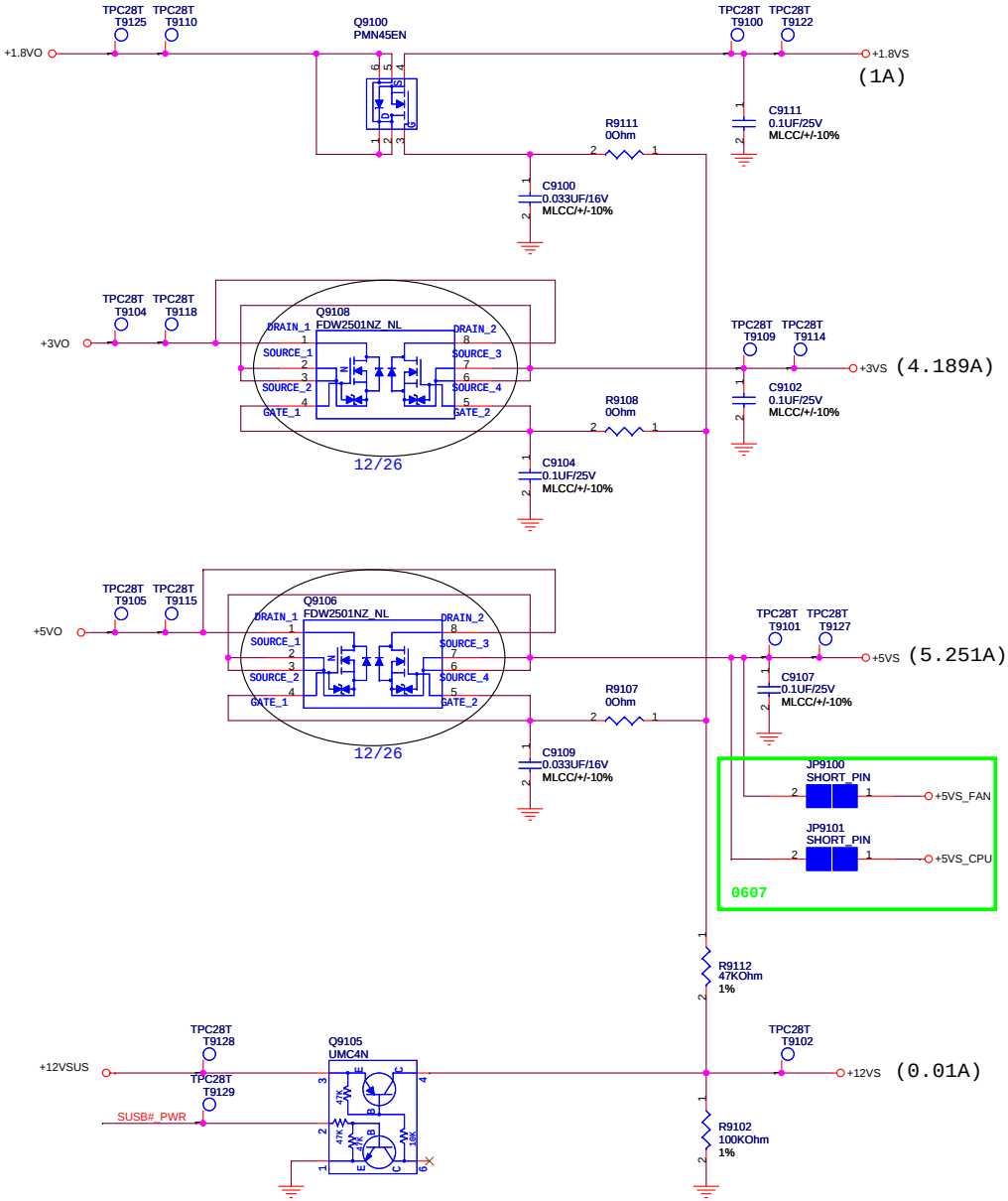
ASUSTeK COMPUTER INC. NB

Engineer: Ray

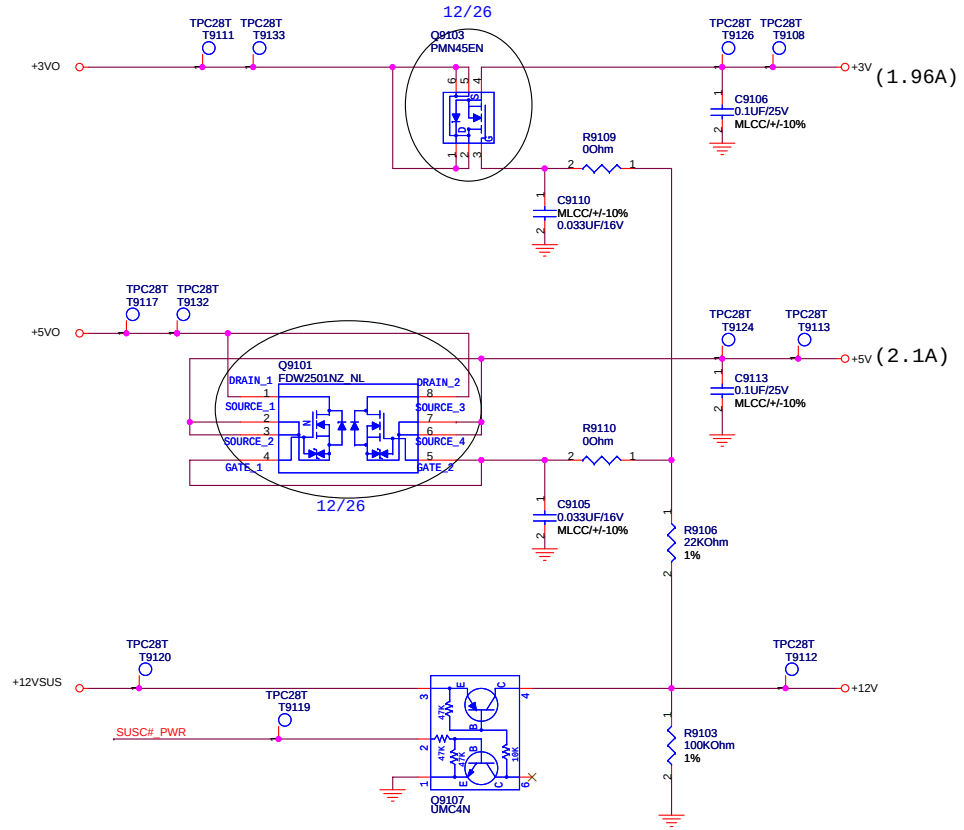
Size	Project Name	Rev
Custom	F6E	1.10

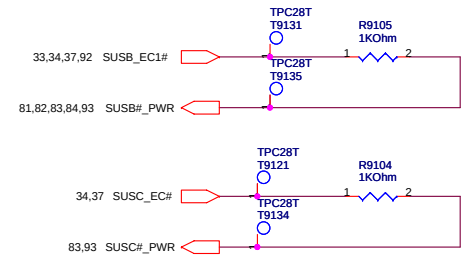
Date: Tuesday, August 21, 2007 Sheet 90 of 94

SUSB#_PWR POWER



SUSC#_PWR POWER





ASUSTeK COMPUTER INC. NB

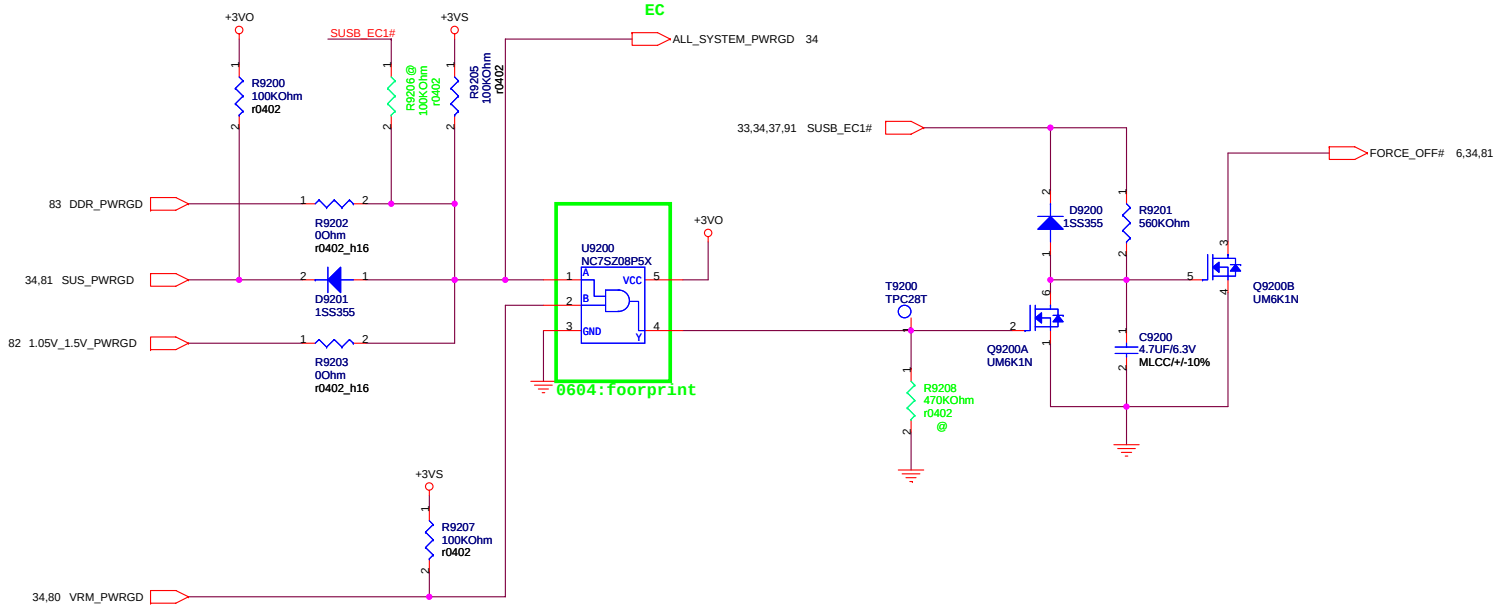
Title : POWER_LOAD SWITCH

Engineer: Ray

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Ray	
Size: Custom	Project Name: F6E	Rev: 1.10
Date: Tuesday, August 21, 2007	Sheet 92 of 94	

AC_BAT_SYS → AC_BAT_SYS 80,81,82,83,88

BAT → BAT 88

BAT_CON → BAT_CON 47,88

+2.5VREF → +2.5VREF 84,88,90

+3VA → +3VA 17,25,27,34,37,81

+5VAO → +5VAO 81,84,90

+5VO → +5VO 81,82,83,90,91

+5VSUS → +5VSUS 28,39,81,88

+5V → +5V 17,24,36,37,91

+5VS → +5VS 18,19,21,22,23,28,33,34,37,39,91

+3VO → +3VO 81,91,92

+3VSUS → +3VSUS 17,20,22,26,27,28,29,34,39,81

+3V → +3V 19,20,21,22,26,33,35,37,91

+3VS → +3VS 6,7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,30,31,33,34,37,38,39,80,91,92

+12VSUS → +12VSUS 81,84,91

+12V → +12V 22,24,36,37,91

+12VS → +12VS 17,19,37,91

+1.8VO → +1.8VO 83,91

+1.8V → +1.8V 9,11,12,14,15,16,37,83

+1.8VS → +1.8VS 30,31,37,91

+0.9VS → +0.9VS 16,37,83

+0.9VO → +0.9VO 83

+1.05VO → +1.05VO 80,82

+VCCP → +VCCP 4,5,6,7,8,9,11,12,82

+1.5VO → +1.5VO 82,84

+1.5VS → +1.5VS 5,12,20,25,28,33,37,82

1023

delete +2.5VO

+VCORE → +VCORE 5,6,37,80

delete VRAM 1.2VSP VGA

+1.25VS → +1.25VS 9,12,28,37,84

0502

delete +VCCFX_CORE

FOR POWER TEST

+3VA

JP9300 @ 1 2 2 SGL_JUMP → CPU_VRON_PWR 80

JP9301 @ 1 2 2 SGL_JUMP → SUSB#_PWR → SUSB#_PWR 81,82,83,84,91

JP9302 @ 1 2 2 SGL_JUMP → SUSC#_PWR → SUSC#_PWR 83,91

JP9303 @ 1 2 2 SGL_JUMP → VSUS_ON → VSUS_ON 34,81

<Variant Name>

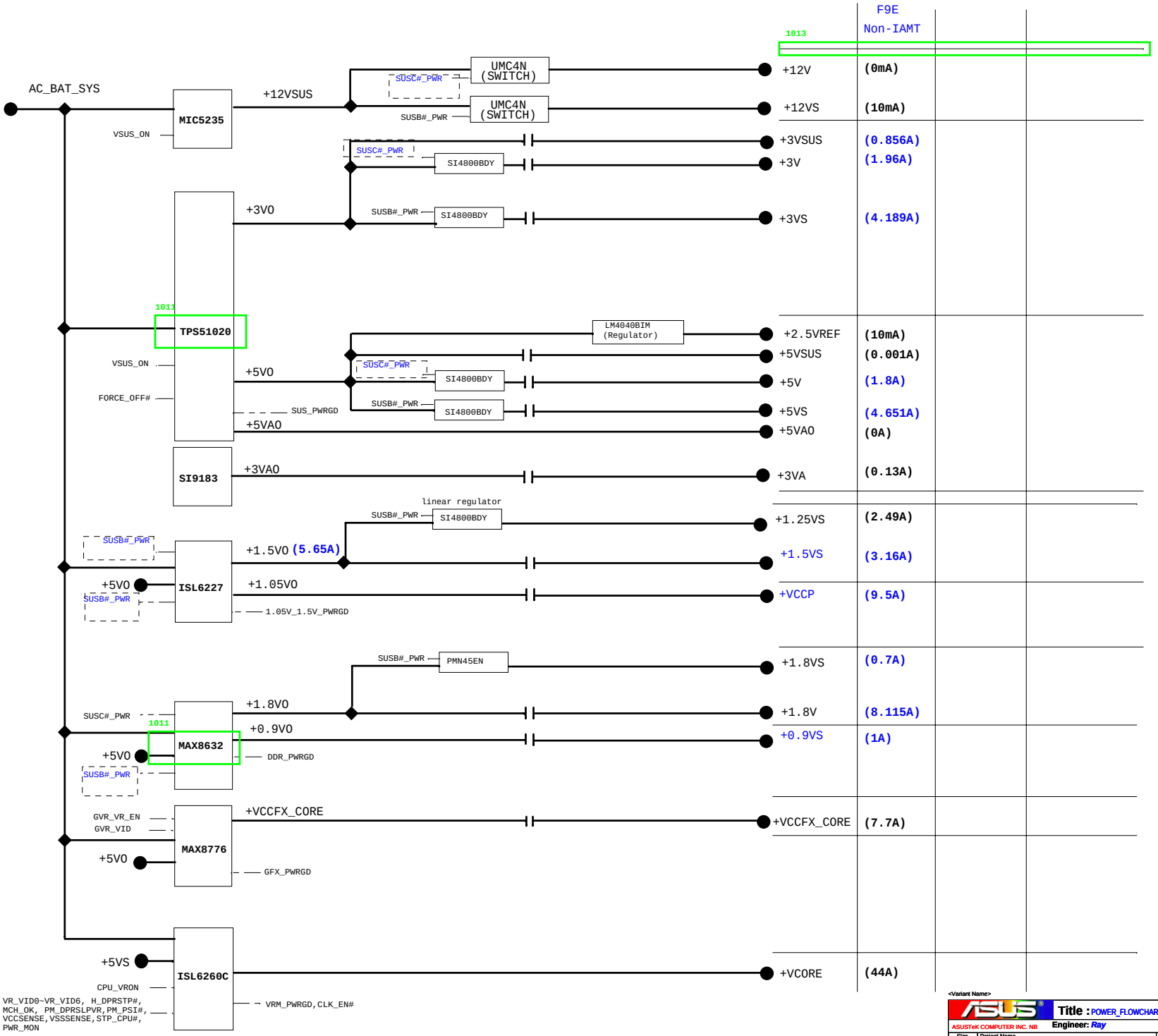
Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 93 of 94



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Ray

Size	Project Name	Rev
Custom	F6E	1.10

Date: Tuesday, August 21, 2007 Sheet 94 of 94