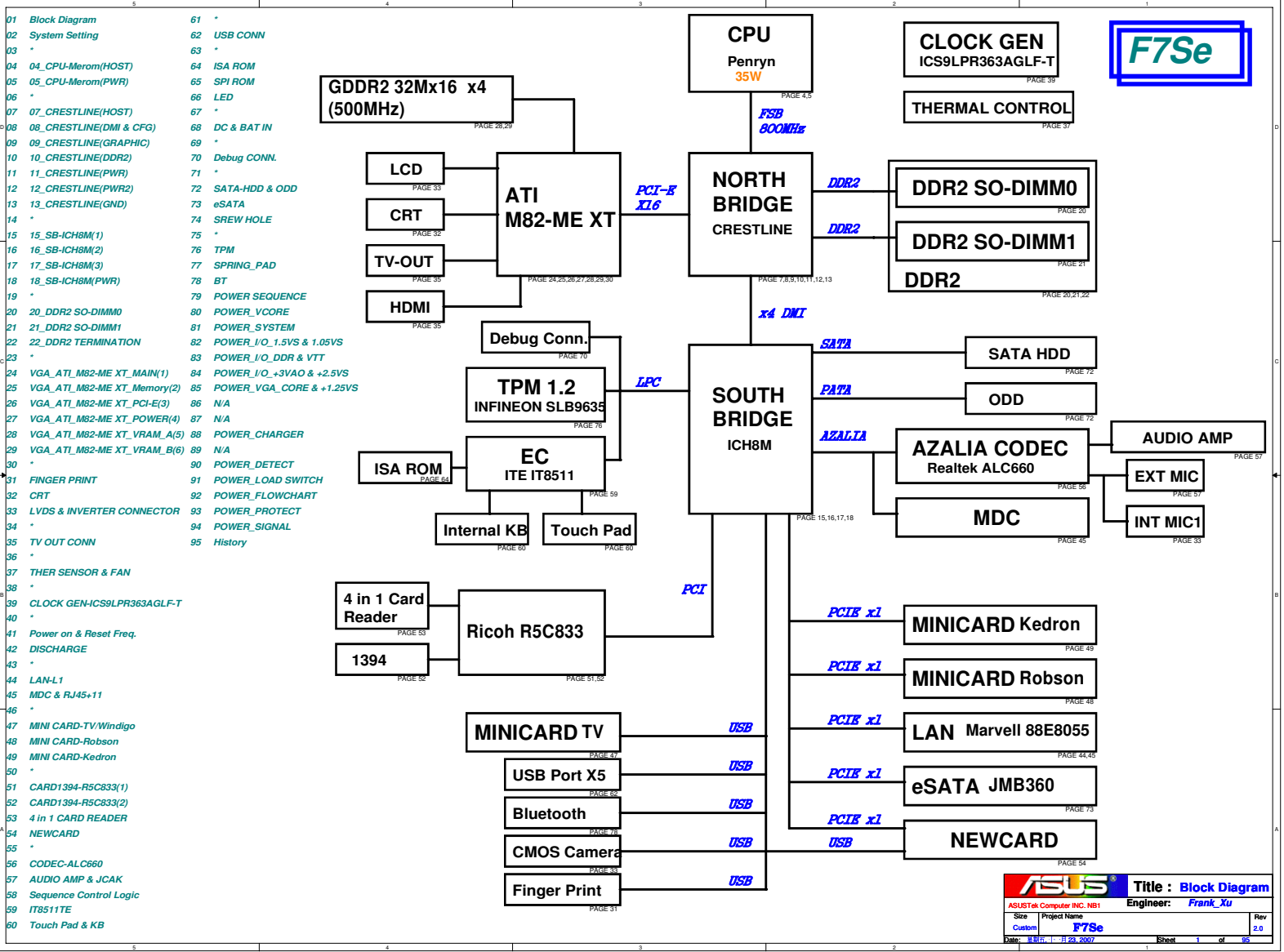




EC_IT8511TE SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	/	
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	O
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	BUF_PLT_RST#	I
31	ECSC1#/GPD3	EXT_SCH#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	PM_SLP_M#	O
110	PS2CLK0/GPF0	WALN_SW#	O
111	PS2DAT0/GPF1	ME_ALERT#	O
114	PS2CLK1/GPF2	/	I/O
115	PS2DAT1/GPF3	/	I/O
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19	O
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80HL/GPG7	AC_APPR_UC#	I

Pin	Pin Name	Signal Name	Type
8	GPL0	PM_S4_STATE#	I
11	GPL1	S4_STATE_ON	O
12	GPL2	SLP_M_ON	O
20	GPL3	EC_WLAN_PWR	O
21	GPL4	MP_PWRGD	I
48	GPH0	VSUS_ON	I
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSN_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYSTEM_PWRGD	I

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	GPI0/BM_BUSY#	PM_BMBUSY#	I
AJ8	GPI01/TACH1	EXTSMI#	I
F8	GPI02/PIRQE#	PCL_INT#	I
G11	GPI03/PIRQF#	PCL_INTF#	I
F12	GPI04/PIRQG#	PCL_INTG#	I
B3	GPI05/PIRQH#	PCL_INT#	I
AJ9	GPI06/TACH2	BIOS_REC	I/O
AH9	GPI07/TACH3	WLAN_LED_EN	I
AE16	GPI08	BT_ON#	I
AG19	GPI09/WOL_EN	LAN_WOL_EN	I
AJ24	GPI010/CLGPIO1	ME_ALERT#	O
AG22	GPI011/SMBALERT#	SMB_ALERT#	I
AC19	GPI012	KBC_SC#	I
AH21	GPI013/GLAN_DOCK#	/	
AF22	GPI014/CLGPIO2	NETDETECT	I
AE20	GPI015/STP_PC#	STP_PC#	I/O
AJ14	GPI016/DPRSPLVR	PM_DPRSPLVR	O
AG8	GPI017/TACH0	WLAN_ON#	O
AH12	GPI018	TP_LEDON	O
AJ10	GPI019/SATA1GP	PCB_ID0	I
AE11	GPI020	BTLED_ON	O
AJ12	GPI021/SATA0GP	CPU_Select	I
AG10	GPI022/SCLOCK	3G_ON#	I
E6	GPI023/LDRQ1#	LPC_DRQ#1	I/O
AJ27	GPI024/CLGPIO0	/	
AG18	GPI025/STP_CPU#	STP_CPU#	O
AH27	GPI026/S4_STATE#	PM_S4_STATE#	O
AH25	GPI027/QRT_STATE0	BT_DET#	I
AD16	GPI028/QRT_STATE1	CB_SD#	O
AG17	GPI029/OC#5	USB_CON_OCS#	I
AD12	GPI030/OC#6	USB_OC#6	I
AJ18	GPI031/OC#7	USB_OC#7	I
AH11	GPI032/CLKRUN#	PM_CLKRUN#	O
AE10	GPI033/AZ_DOCK_EN#	/	O
AG14	GPI034/AZ_DOCK_RST#	/	O
AG13	GPI035/SATACLKREQ#	GPO35	O
AF11	GPI036/SATA2GP	PCB_ID1	O
AG11	GPI037/SATA3GP	PCB_ID2	I/O
AF9	GPI038/SLOAD	GPI38	I
AJ11	GPI039/SDATAOUT0	GPI39	I
AD10	GPI048/SDATAOUT1	PCL_GNT#4	O
AG29	GPI049/CPUPWRGD	H_PWRGD	O

Pin	Pin Name	Signal Name	Type
152	GPI2	/	
155	GPI3	CHG_EN#	O
168	GPI5	EC_CLK_EN	O
85	KS016/GPM2	NETDETECT	O

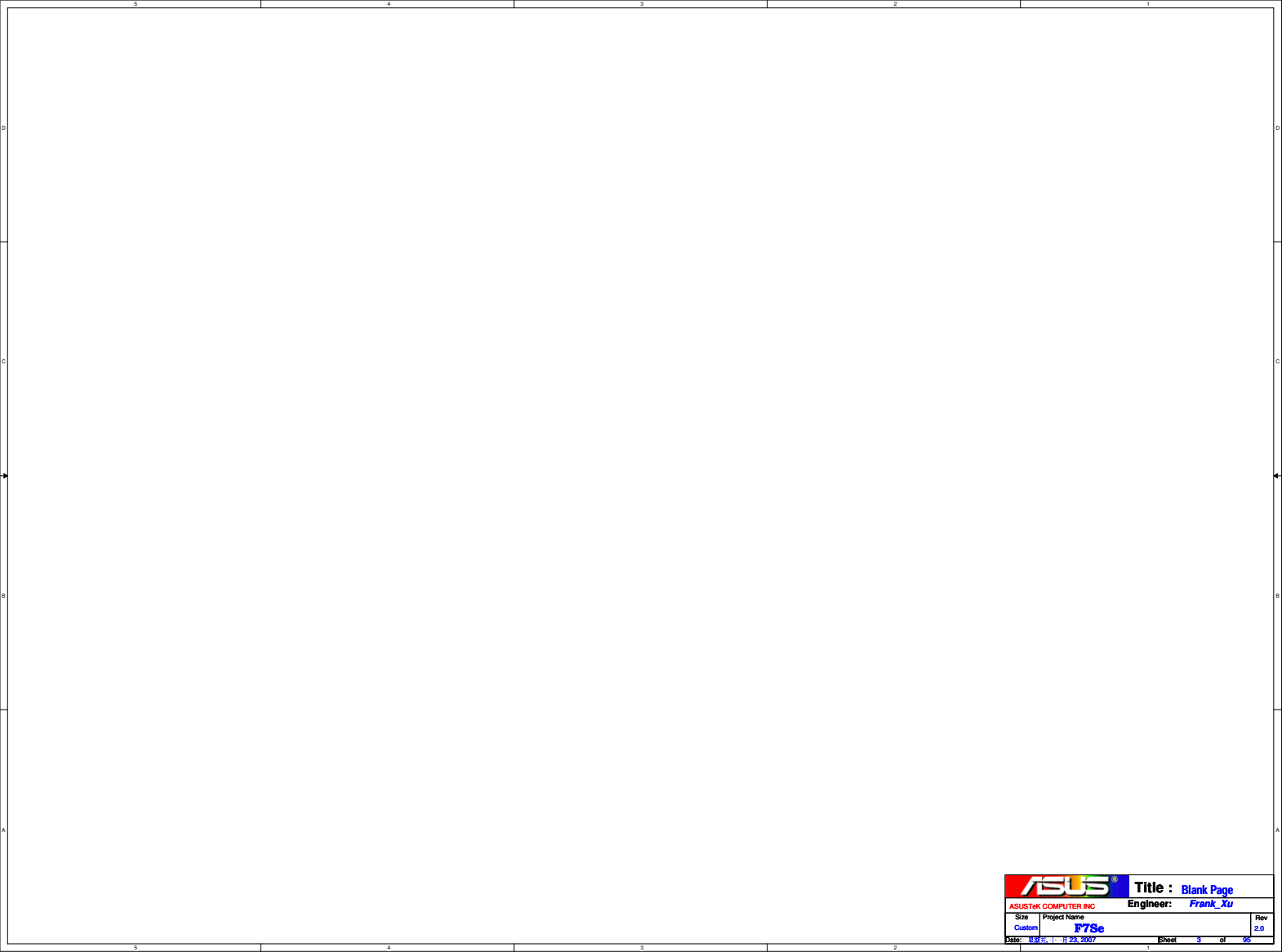
PC1 Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

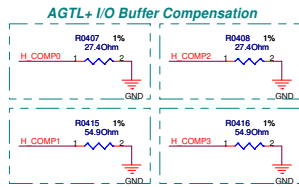
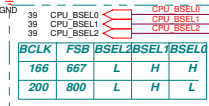
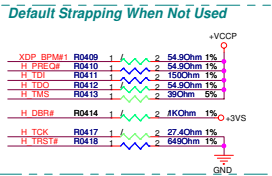
PCIe Device	Bus	PCIe Device	Bus
LAN	PE(T/R)(p/n)1	Robson	PE(T/R)(p/n)4
Kedron	PE(T/R)(p/n)2	NEWCARD	PE(T/R)(p/n)5
eSATA	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)6

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(MAX6657)	0100110x (4C)
VGA Thermal Sensor(MAX6657)	0100110x (4C)

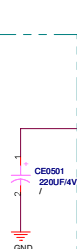
ICS9LPR363AGLF-T SETTING

Pin	Pin Name	Device
3	PCICLK1	TPMPC1
4	PCICLK2	CardBus R5C832
5	SELPCIEX0_LCD#PCICLK3	EC IT8511E
8	ITP_EN/PCICLK_F0	ICH8
15	DOTC_96MHzL	X
14	DOTT_96MHzL	X
12	FSLA/USB_48MHz	ICH8
19	PCleT_L1	eSATA
20	PCleC_L1	eSATA
36	PCleT_L5	M82-M XT
35	PCleC_L5	M82-M XT
39	PCleT_L6	MiniCard(Rob)
38	PCleC_L6	MiniCard(Rob)
22	PCleT_L2	ICH8
23	PCleC_L2	ICH8
24	PCleT_L3	MCH
25	PCleC_L3	MCH
26	SATACLKT_L	ICH8
27	SATACLKC_L	ICH8
44	CPUI1TP_L2 / PCleT_L8	LAN
43	CPUI1TPC_L2 / PCleC_L8	LAN
14	27FIX/LCD_SSCST/PCleT_L0M72M	
15	DOTC_96MHzL	M72M
41	PEREQ1# / PCleT_L7	MiniCard
40	PEREQ2# / PCleC_L7	MiniCard
32	PEREQ3#	NewCard
33	PEREQ4#	MiniCard
30	PCleT_L4	NewCard
31	PCleC_L4	NewCard
49	CPUT_L1F	MCH
48	CPUC_L1F	MCH
52	CPUT_L0	CPU
51	CPUC_L0	CPU
57	X2	14.318MHz
58	X1	14.318MHz
60	REF0	ICH8
61	REF1/FSLC/TEST_SEL	X

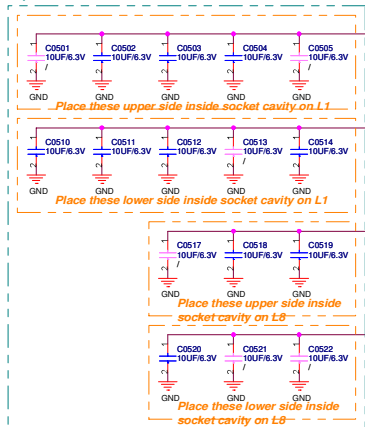




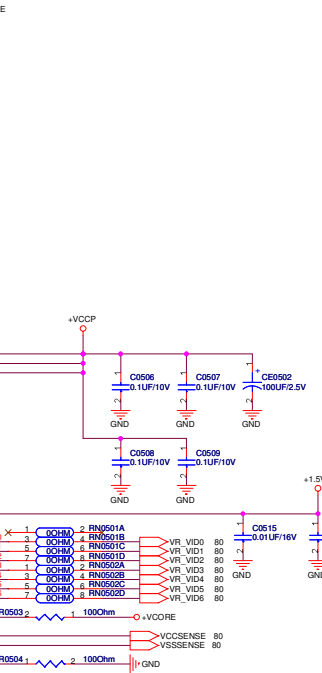
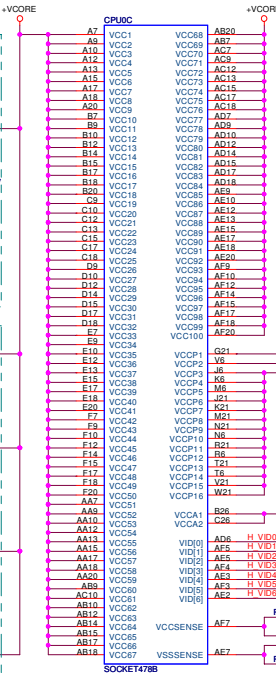
CPU + VCORE
Bulk-Decoupling
Capacitors



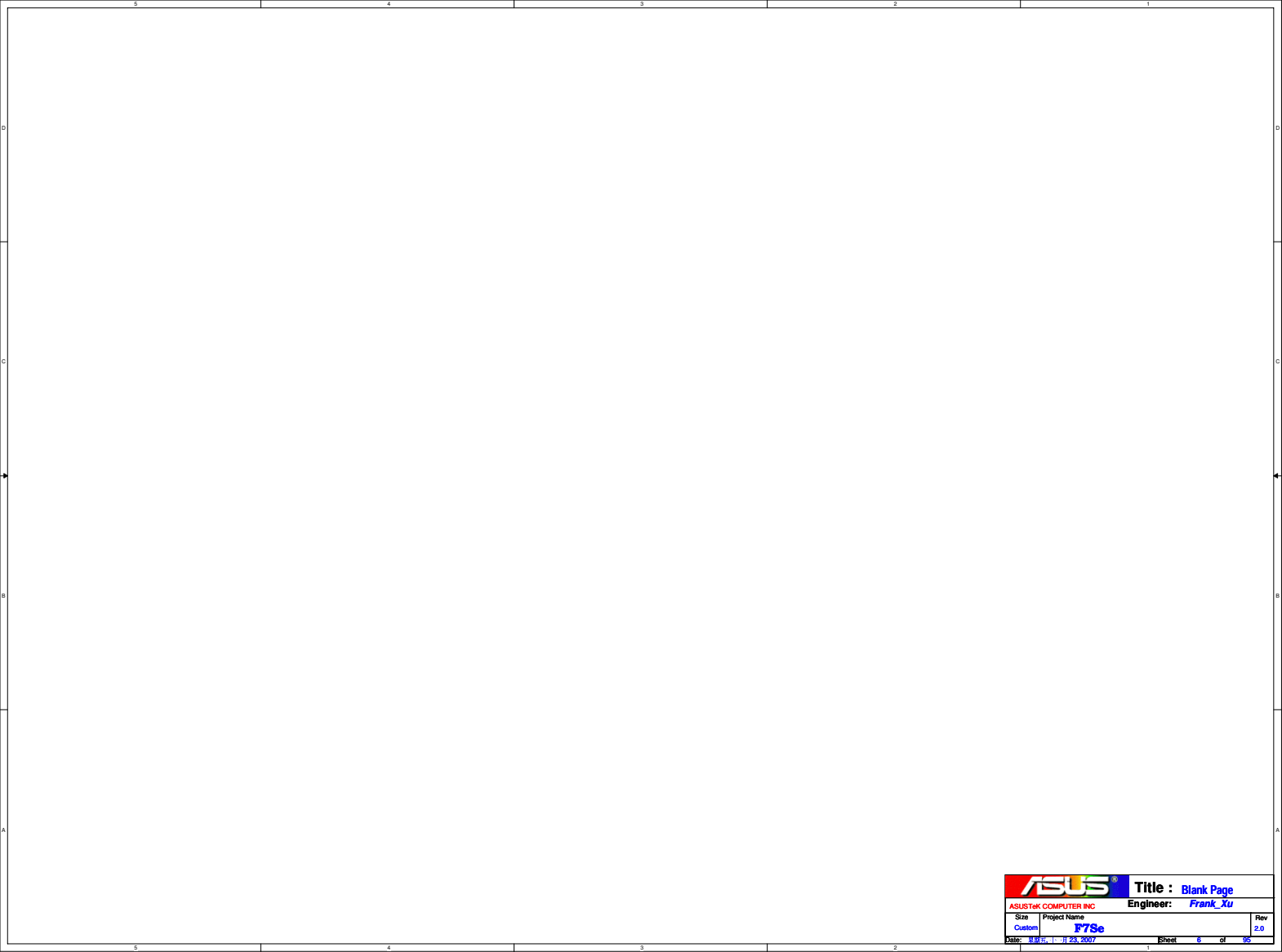
CPU + VCORE
Mid-Frequency
Capacitors



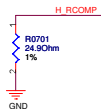
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
F3S: 10UF *16
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
F3S: 100UF *1, 0.1UF *4



A4	VS51	VS52	VS53	P6
A5	VS52	VS53	VS54	P24
A6	VS53	VS54	VS55	P2
A14	VS55	VS56	VS57	P2
A15	VS56	VS57	VS58	P24
A16	VS57	VS58	VS59	P2
A23	VS59	VS60	VS61	P24
B6	VS59	VS60	P25	
B7	VS59	VS60	P25	
B11	VS59	VS60	P25	
B13	VS60	VS61	P25	
B14	VS61	VS62	P25	
B15	VS62	VS63	P25	
B19	VS63	VS64	P25	
B21	VS64	VS65	P25	
B24	VS65	VS66	P25	
C16	VS66	VS67	P25	
C17	VS67	VS68	P25	
C18	VS68	VS69	P25	
C2	VS69	VS70	P25	
C22	VS70	VS71	P25	
C23	VS71	VS72	P25	
C25	VS72	VS73	P25	
D1	VS73	VS74	P25	
D6	VS74	VS75	P25	
D8	VS75	VS76	P25	
D13	VS76	VS77	P25	
D16	VS77	VS78	P25	
D19	VS78	VS79	P25	
D23	VS79	VS80	P25	
E3	VS80	VS81	P25	
E4	VS81	VS82	P25	
E8	VS82	VS83	P25	
E11	VS83	VS84	P25	
E16	VS84	VS85	P25	
E19	VS85	VS86	P25	
E21	VS86	VS87	P25	
E24	VS87	VS88	P25	
E3	VS88	VS89	P25	
F8	VS89	VS90	P25	
F13	VS90	VS91	P25	
F14	VS91	VS92	P25	
F15	VS92	VS93	P25	
F22	VS93	VS94	P25	
F25	VS94	VS95	P25	
G1	VS95	VS96	P25	
G2	VS96	VS97	P25	
G26	VS97	VS98	P25	
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H83	VS162	VS163	P25	
H84	VS163	VS164	P25	
H85	VS164	VS165	P25	
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H256	VS335	VS336	P25	
H257	VS336	VS337	P25	
H258	VS337	VS338	P25	
H259	VS338	VS339	P25	
H260	VS339	VS340	P25	
H261	VS340	VS341	P25	
H262	VS341	VS342	P25	
H263	VS342	VS343	P25	
H264	VS343	VS344	P25	
H265	VS344	VS345	P25	
H266	VS345	VS346	P25	
H267	VS346	VS347	P25	
H268	VS347	VS348	P25	
H269	VS348	VS349	P25	
H270	VS349	VS350	P25	
H271	VS350	VS351	P25	
H272	VS351	VS352	P25	
H273	VS352	VS353	P25	
H274	VS353	VS354	P25	
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H276	VS355	VS356	P25	
H277	VS356	VS357	P25	
H278	VS357</			



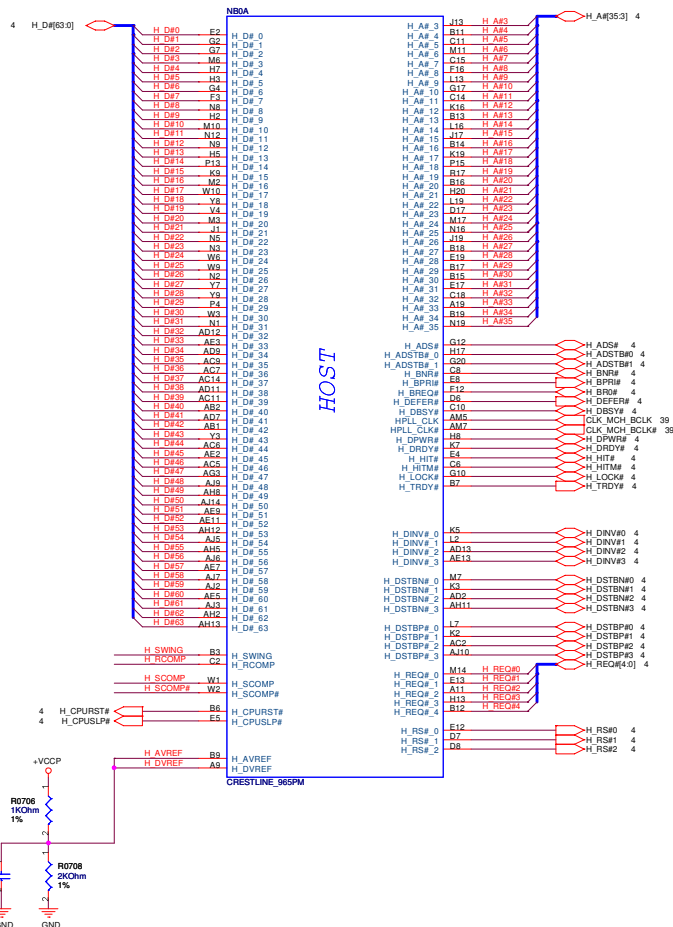
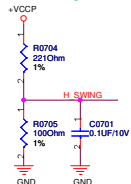
For Calibrating the FSB I/O Buffer

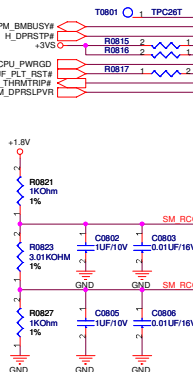
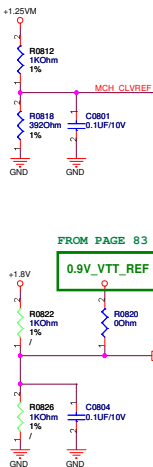


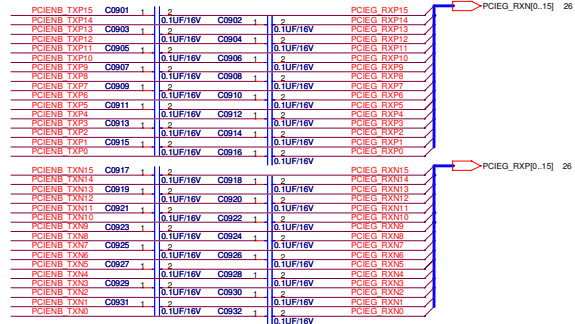
For Slew Rate Compensation on the FSB



For Providing a Reference Voltage to The FSB RCOMP circuits







		Title : NB_965PM(GRAPHIC)	
ASUSTek COMPUTER INC. NBI		Engineer: Frank_Xu	
Size Custom	Project Name F7Se	Re 2.0	
Date: 2007年08月26日		Sheet 9 of 95	

20 M_A_DQ[8:30]

M_A_DQ0 AR441 SA_DQ_0
 M_A_DQ1 AW44 SA_DQ_1
 M_A_DQ2 RA45 SA_DQ_2
 M_A_DQ3 AV46 SA_DQ_3
 M_A_DQ4 AR41 SA_DQ_4
 M_A_DQ5 AT42 SA_DQ_5
 M_A_DQ6 AR45 SA_DQ_6
 M_A_DQ7 AW47 SA_DQ_7
 M_A_DQ8 BR45 SA_DQ_8
 M_A_DQ9 BF48 SA_DQ_9
 M_A_DQ10 BG47 SA_DQ_10
 M_A_DQ11 BA45 SA_DQ_11
 M_A_DQ12 BA47 SA_DQ_12
 M_A_DQ13 BG50 SA_DQ_13
 M_A_DQ14 BH49 SA_DQ_14
 M_A_DQ15 BE45 SA_DQ_15
 M_A_DQ16 BA43 SA_DQ_16
 M_A_DQ17 BE44 SA_DQ_17
 M_A_DQ18 BR42 SA_DQ_18
 M_A_DQ19 BE40 SA_DQ_19
 M_A_DQ20 BF44 SA_DQ_20
 M_A_DQ21 BH45 SA_DQ_21
 M_A_DQ22 BG40 SA_DQ_22
 M_A_DQ23 BR40 SA_DQ_23
 M_A_DQ24 AR40 SA_DQ_24
 M_A_DQ25 AT38 SA_DQ_25
 M_A_DQ26 AW36 SA_DQ_26
 M_A_DQ27 AW34 SA_DQ_27
 M_A_DQ28 AW41 SA_DQ_28
 M_A_DQ29 AV41 SA_DQ_29
 M_A_DQ30 AV38 SA_DQ_30
 M_A_DQ31 AT38 SA_DQ_31
 M_A_DQ32 AV13 SA_DQ_32
 M_A_DQ33 AT10 SA_DQ_33
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 M_A_DQ35 AV11 SA_DQ_35
 M_A_DQ36 AU15 SA_DQ_36
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 M_A_DQ40 BG10 SA_DQ_40
 M_A_DQ41 BD10 SA_DQ_41
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 M_A_DQ59 AN10 SA_DQ_59
 M_A_DQ60 AT9 SA_DQ_60
 M_A_DQ61 AN9 SA_DQ_61
 M_A_DQ62 AM9 SA_DQ_62
 M_A_DQ63 AN11 SA_DQ_63

CRESTLINE_965PM

DDR SYSTEM MEMORY A

SA_BS_0 BE18
 SA_BS_1 BK19
 SA_BS_2 BF29
 SA_CAS# JBL17
 SA_DM_0 AT45 M_A_DM0
 SA_DM_1 BR44 M_A_DM1
 SA_DM_2 BR42 M_A_DM2
 SA_DM_3 AW38 M_A_DM3
 SA_DM_4 AW13 M_A_DM4
 SA_DM_5 BG8 M_A_DM5
 SA_DM_6 AV8 M_A_DM6
 SA_DM_7 AN8 M_A_DM7
 SA_DQS_0 AT46 M_A_DQS0
 SA_DQS_1 BE48 M_A_DQS1
 SA_DQS_2 BR43 M_A_DQS2
 SA_DQS_3 BC37 M_A_DQS3
 SA_DQS_4 BR16 M_A_DQS4
 SA_DQS_5 BR6 M_A_DQS5
 SA_DQS_6 BR2 M_A_DQS6
 SA_DQS_7 AP3 M_A_DQS7
 SA_DQS8_0 AT47 M_A_DQS8_0
 SA_DQS8_1 BR47 M_A_DQS8_1
 SA_DQS8_2 BC41 M_A_DQS8_2
 SA_DQS8_3 BA37 M_A_DQS8_3
 SA_DQS8_4 BA16 M_A_DQS8_4
 SA_DQS8_5 BR7 M_A_DQS8_5
 SA_DQS8_6 BC1 M_A_DQS8_6
 SA_DQS8_7 AP2 M_A_DQS8_7
 SA_MA_0 B119
 SA_MA_1 BR27 M_A_A1
 SA_MA_2 BR28 M_A_A2
 SA_MA_3 BR28 M_A_A3
 SA_MA_4 BR28 M_A_A4
 SA_MA_5 BR28 M_A_A5
 SA_MA_6 B127 M_A_A6
 SA_MA_7 B125 M_A_A7
 SA_MA_8 BR28 M_A_A8
 SA_MA_9 BA28 M_A_A9
 SA_MA_10 BC19 M_A_A10
 SA_MA_11 BR28 M_A_A11
 SA_MA_12 BG30 M_A_A12
 SA_MA_13 B119 M_A_A13
 SA_RAS# BE18
 SA_RCVEN# AY29
 SA_WE# BA19

M_A_BS0 20:22
 M_A_BS1 20:22
 M_A_BS2 20:22
 M_A_CAS# 20:22
 M_A_DM[7:0] 20
 M_A_DQS[7:0] 20
 M_A_DQS[7:0] 20
 M_A_A[13:0] 20:22
 M_A_RAS# 20:22
 M_A_WE# 20:22

21 M_B_DQ[8:30]

M_B_DQ0 AP49 SB_DQ_0
 M_B_DQ1 AR51 SB_DQ_1
 M_B_DQ2 AW50 SB_DQ_2
 M_B_DQ3 AW51 SB_DQ_3
 M_B_DQ4 AN51 SB_DQ_4
 M_B_DQ5 AN50 SB_DQ_5
 M_B_DQ6 AV50 SB_DQ_6
 M_B_DQ7 BA50 SB_DQ_7
 M_B_DQ8 BR50 SB_DQ_8
 M_B_DQ9 BG50 SB_DQ_9
 M_B_DQ10 BA49 SB_DQ_10
 M_B_DQ11 BE50 SB_DQ_11
 M_B_DQ12 BA51 SB_DQ_12
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 M_B_DQ14 BF50 SB_DQ_14
 M_B_DQ15 BR50 SB_DQ_15
 M_B_DQ16 BR50 SB_DQ_16
 M_B_DQ17 BA44 SB_DQ_17
 M_B_DQ18 BA43 SB_DQ_18
 M_B_DQ19 BR42 SB_DQ_19
 M_B_DQ20 BR47 SB_DQ_20
 M_B_DQ21 BR49 SB_DQ_21
 M_B_DQ22 BR43 SB_DQ_22
 M_B_DQ23 BR42 SB_DQ_23
 M_B_DQ24 BA41 SB_DQ_24
 M_B_DQ25 BR41 SB_DQ_25
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 M_B_DQ28 BR41 SB_DQ_28
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 M_B_DQ30 BR35 SB_DQ_30
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 M_B_DQ32 BK13 SB_DQ_32
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 M_B_DQ34 BK11 SB_DQ_34
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 M_B_DQ43 BL5 SB_DQ_43
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 M_B_DQ58 AR1 SB_DQ_58
 M_B_DQ59 AT3 SB_DQ_59
 M_B_DQ60 AV2 SB_DQ_60
 M_B_DQ61 AN1 SB_DQ_61
 M_B_DQ62 AU2 SB_DQ_62
 M_B_DQ63 AT2 SB_DQ_63

CRESTLINE_965PM

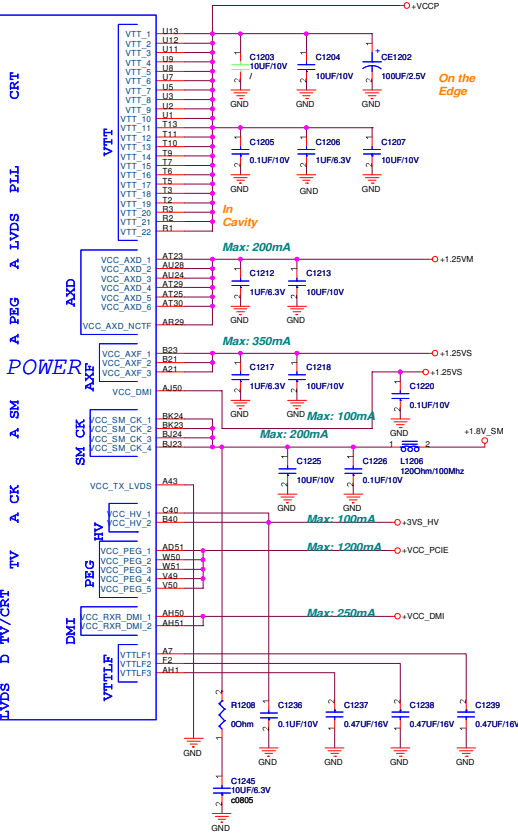
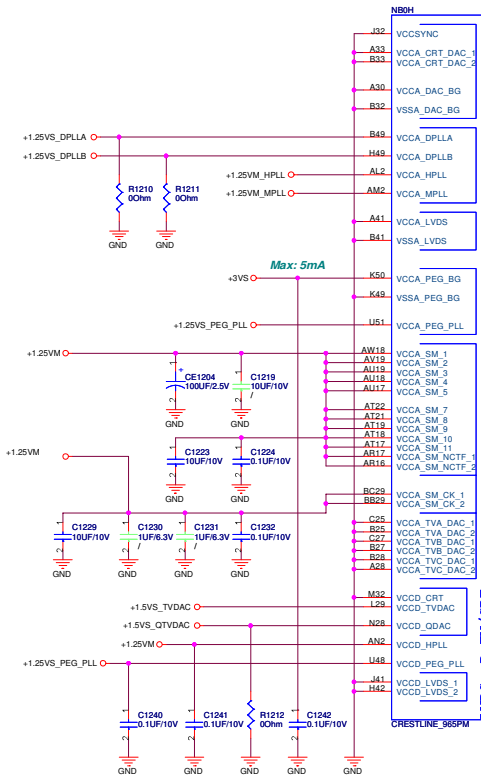
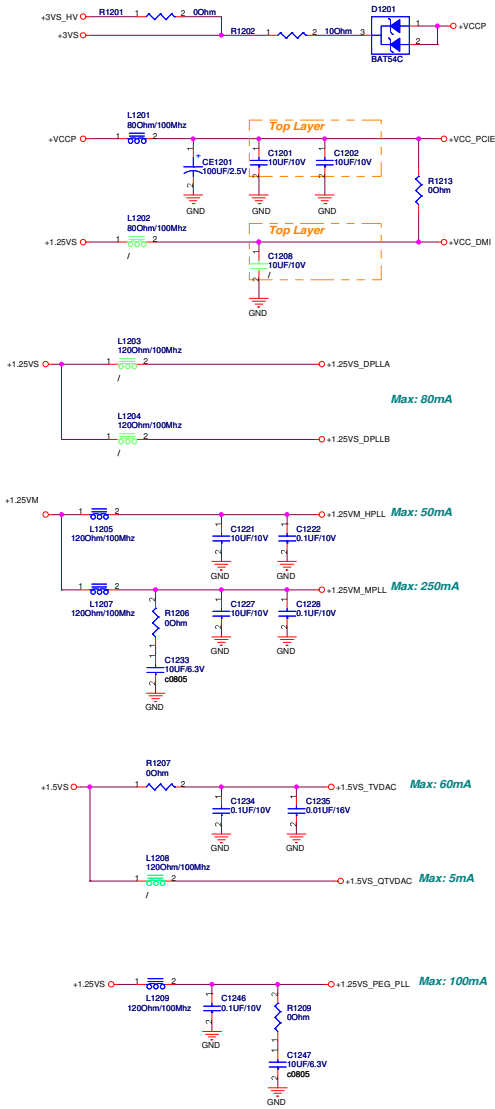
DDR SYSTEM MEMORY B

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 SB_BS_1 BG18
 SB_BS_2 BK36
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 SB_DM_1 BR49 M_B_DM1
 SB_DM_2 BR45 M_B_DM2
 SB_DM_3 BL39 M_B_DM3
 SB_DM_4 BR12 M_B_DM4
 SB_DM_5 BA7 M_B_DM5
 SB_DM_6 BR3 M_B_DM6
 SB_DM_7 AW2 M_B_DM7
 SB_DQS_0 AT50 M_B_DQS0
 SB_DQS_1 BR50 M_B_DQS1
 SB_DQS_2 BR46 M_B_DQS2
 SB_DQS_3 BK39 M_B_DQS3
 SB_DQS_4 BL12 M_B_DQS4
 SB_DQS_5 BL7 M_B_DQS5
 SB_DQS_6 BE2 M_B_DQS6
 SB_DQS_7 AV2 M_B_DQS7
 SB_DQS8_0 AU50 M_B_DQS8_0
 SB_DQS8_1 BC36 M_B_DQS8_1
 SB_DQS8_2 BL45 M_B_DQS8_2
 SB_DQS8_3 BK38 M_B_DQS8_3
 SB_DQS8_4 BK12 M_B_DQS8_4
 SB_DQS8_5 BK7 M_B_DQS8_5
 SB_DQS8_6 BE2 M_B_DQS8_6
 SB_DQS8_7 AV3 M_B_DQS8_7
 SB_MA_0 BC18 M_B_A0
 SB_MA_1 BQ28 M_B_A1
 SB_MA_2 BG28 M_B_A2
 SB_MA_3 AW17 M_B_A3
 SB_MA_4 BR25 M_B_A4
 SB_MA_5 BR25 M_B_A5
 SB_MA_6 BA29 M_B_A6
 SB_MA_7 BC28 M_B_A7
 SB_MA_8 AY28 M_B_A8
 SB_MA_9 BQ37 M_B_A9
 SB_MA_10 BR17 M_B_A10
 SB_MA_11 BE37 M_B_A11
 SB_MA_12 BA30 M_B_A12
 SB_MA_13 BG13 M_B_A13
 SB_RAS# AV18
 SB_RCVEN# AY18
 SB_WE# BC17

M_B_BS0 21:22
 M_B_BS1 21:22
 M_B_BS2 21:22
 M_B_CAS# 21:22
 M_B_DM[7:0] 21
 M_B_DQS[7:0] 21
 M_B_DQS[7:0] 21
 M_B_A[13:0] 21:22
 M_B_RAS# 21:22
 M_B_WE# 21:22

-Variant Name-





NB01		
A13	VSS_1	VSS_100
A15	VSS_2	VSS_101
A17	VSS_3	VSS_102
A24	VSS_4	VSS_103
AA21	VSS_5	VSS_104
AA24	VSS_6	VSS_105
AA29	VSS_7	VSS_106
AB20	VSS_8	VSS_107
AB23	VSS_9	VSS_108
AB26	VSS_10	VSS_109
AB28	VSS_11	VSS_110
AB31	VSS_12	VSS_111
AC10	VSS_13	VSS_112
AC13	VSS_14	VSS_113
AC3	VSS_15	VSS_114
AC38	VSS_16	VSS_115
AC43	VSS_17	VSS_116
AC47	VSS_18	VSS_117
AD1	VSS_19	VSS_118
AD21	VSS_20	VSS_119
AD26	VSS_21	VSS_120
AD29	VSS_22	VSS_121
AD3	VSS_23	VSS_122
AD41	VSS_24	VSS_123
AD45	VSS_25	VSS_124
AD48	VSS_26	VSS_125
AD5	VSS_27	VSS_126
AD50	VSS_28	VSS_127
AD8	VSS_29	VSS_128
AE10	VSS_30	VSS_129
AE14	VSS_31	VSS_130
AE6	VSS_32	VSS_131
AF20	VSS_33	VSS_132
AF23	VSS_34	VSS_133
AF24	VSS_35	VSS_134
AF31	VSS_36	VSS_135
AG2	VSS_37	VSS_136
AG38	VSS_38	VSS_137
AG43	VSS_39	VSS_138
AG47	VSS_40	VSS_139
AG50	VSS_41	VSS_140
AH3	VSS_42	VSS_141
AH40	VSS_43	VSS_142
AH41	VSS_44	VSS_143
AH7	VSS_45	VSS_144
AH9	VSS_46	VSS_145
AH11	VSS_47	VSS_146
AH13	VSS_48	VSS_147
AJ21	VSS_49	VSS_148
AJ24	VSS_50	VSS_149
AJ29	VSS_51	VSS_150
AJ32	VSS_52	VSS_151
AJ43	VSS_53	VSS_152
AJ45	VSS_54	VSS_153
AJ49	VSS_55	VSS_154
AK20	VSS_56	VSS_155
AK21	VSS_57	VSS_156
AK26	VSS_58	VSS_157
AK28	VSS_59	VSS_158
AK31	VSS_60	VSS_159
AK51	VSS_61	VSS_160
AL1	VSS_62	VSS_161
AM11	VSS_63	VSS_162
AM13	VSS_64	VSS_163
AM3	VSS_65	VSS_164
AM4	VSS_66	VSS_165
AM41	VSS_67	VSS_166
AM45	VSS_68	VSS_167
AN1	VSS_69	VSS_168
AN38	VSS_70	VSS_169
AN39	VSS_71	VSS_170
AN63	VSS_72	VSS_171
AN6	VSS_73	VSS_172
AN7	VSS_74	VSS_173
AP4	VSS_75	VSS_174
AP48	VSS_76	VSS_175
AP50	VSS_77	VSS_176
AP11	VSS_78	VSS_177
AP2	VSS_79	VSS_178
AP39	VSS_80	VSS_179
AR44	VSS_81	VSS_180
AR47	VSS_82	VSS_181
AT7	VSS_83	VSS_182
AT10	VSS_84	VSS_183
AT14	VSS_85	VSS_184
AT41	VSS_86	VSS_185
AT49	VSS_87	VSS_186
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AU23	VSS_89	VSS_188
AU29	VSS_90	VSS_189
AU3	VSS_91	VSS_190
AU36	VSS_92	VSS_191
AU49	VSS_93	VSS_192
AU51	VSS_94	VSS_193
AV38	VSS_95	VSS_194
AV48	VSS_96	VSS_195
AW1	VSS_97	VSS_196
AW12	VSS_98	VSS_197
AW16	VSS_99	VSS_198

GND

CRESTLINE 965PM

GND

NB01		
C46	VSS_199	VSS_287
C50	VSS_200	VSS_288
C67	VSS_201	VSS_289
D13	VSS_202	VSS_290
D24	VSS_203	VSS_291
D33	VSS_204	VSS_292
D32	VSS_205	VSS_293
D45	VSS_206	VSS_294
D49	VSS_207	VSS_295
D45	VSS_208	VSS_296
E16	VSS_209	VSS_297
E16	VSS_210	VSS_298
E24	VSS_211	VSS_299
E38	VSS_212	VSS_300
E32	VSS_213	VSS_301
E47	VSS_214	VSS_302
F19	VSS_215	VSS_303
F36	VSS_216	VSS_304
F4	VSS_217	VSS_305
F40	VSS_218	
F50	VSS_219	
G1	VSS_220	
G13	VSS_221	
G16	VSS_222	VSS_306
G19	VSS_223	VSS_307
G24	VSS_224	VSS_308
G28	VSS_225	VSS_309
G29	VSS_226	VSS_310
G33	VSS_227	VSS_311
G42	VSS_228	VSS_312
G45	VSS_229	VSS_313
G48	VSS_230	
G8	VSS_231	
H24	VSS_232	
H28	VSS_233	
H4	VSS_234	
H45	VSS_235	
J11	VSS_236	
J16	VSS_237	
J2	VSS_238	
J24	VSS_239	
J28	VSS_240	
J33	VSS_241	
J35	VSS_242	
J39	VSS_243	
K12	VSS_245	
K47	VSS_246	
K8	VSS_247	
L1	VSS_248	
L17	VSS_249	
L20	VSS_250	
L24	VSS_251	
L28	VSS_252	
L3	VSS_253	
L33	VSS_254	
L49	VSS_255	
M28	VSS_256	
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M49	VSS_259	
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M50	VSS_261	
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N17	VSS_264	
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N36	VSS_266	
N39	VSS_267	
N36	VSS_268	
N44	VSS_269	
N49	VSS_270	
N49	VSS_271	
N7	VSS_272	
P2	VSS_273	
P23	VSS_274	
P4	VSS_275	
P4	VSS_276	
P50	VSS_277	
R49	VSS_278	
T38	VSS_279	
T43	VSS_280	
U47	VSS_281	
U41	VSS_282	
U45	VSS_283	
U50	VSS_284	
V2	VSS_285	
V3	VSS_286	

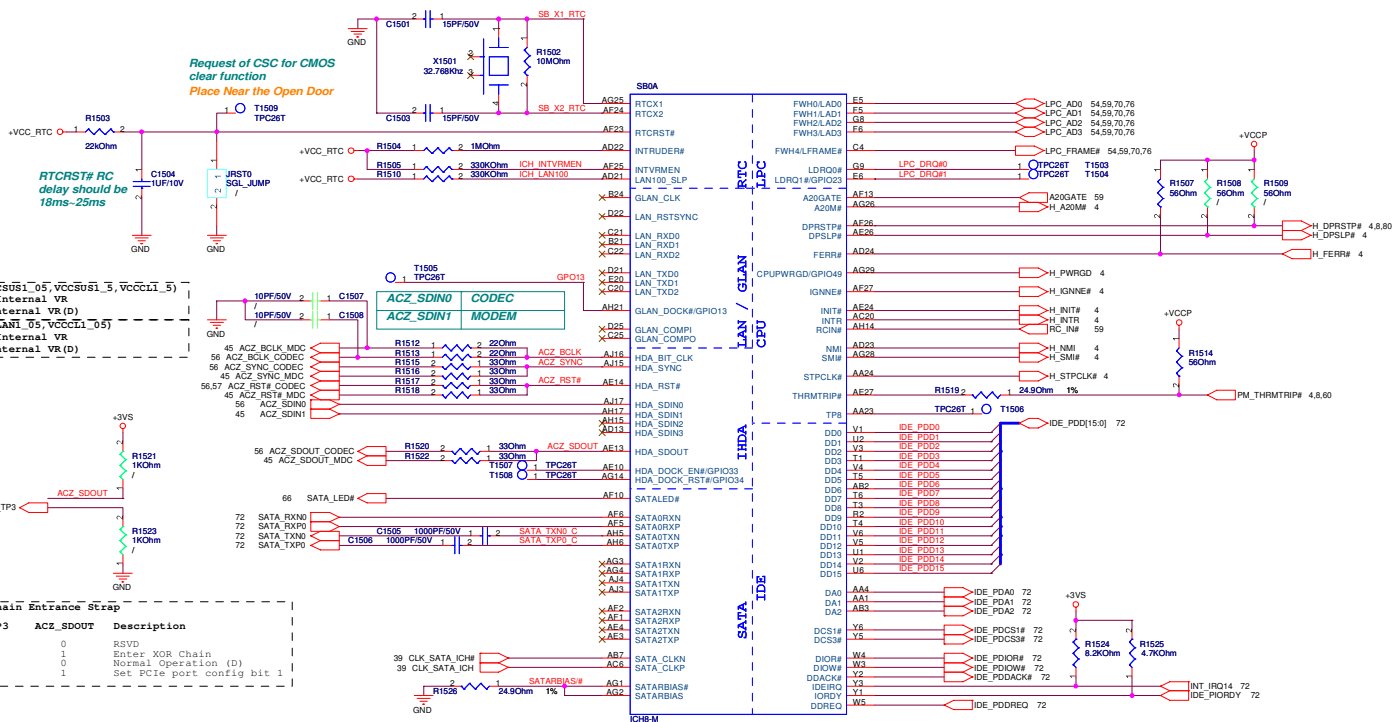
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CRESTLINE 965PM

GND

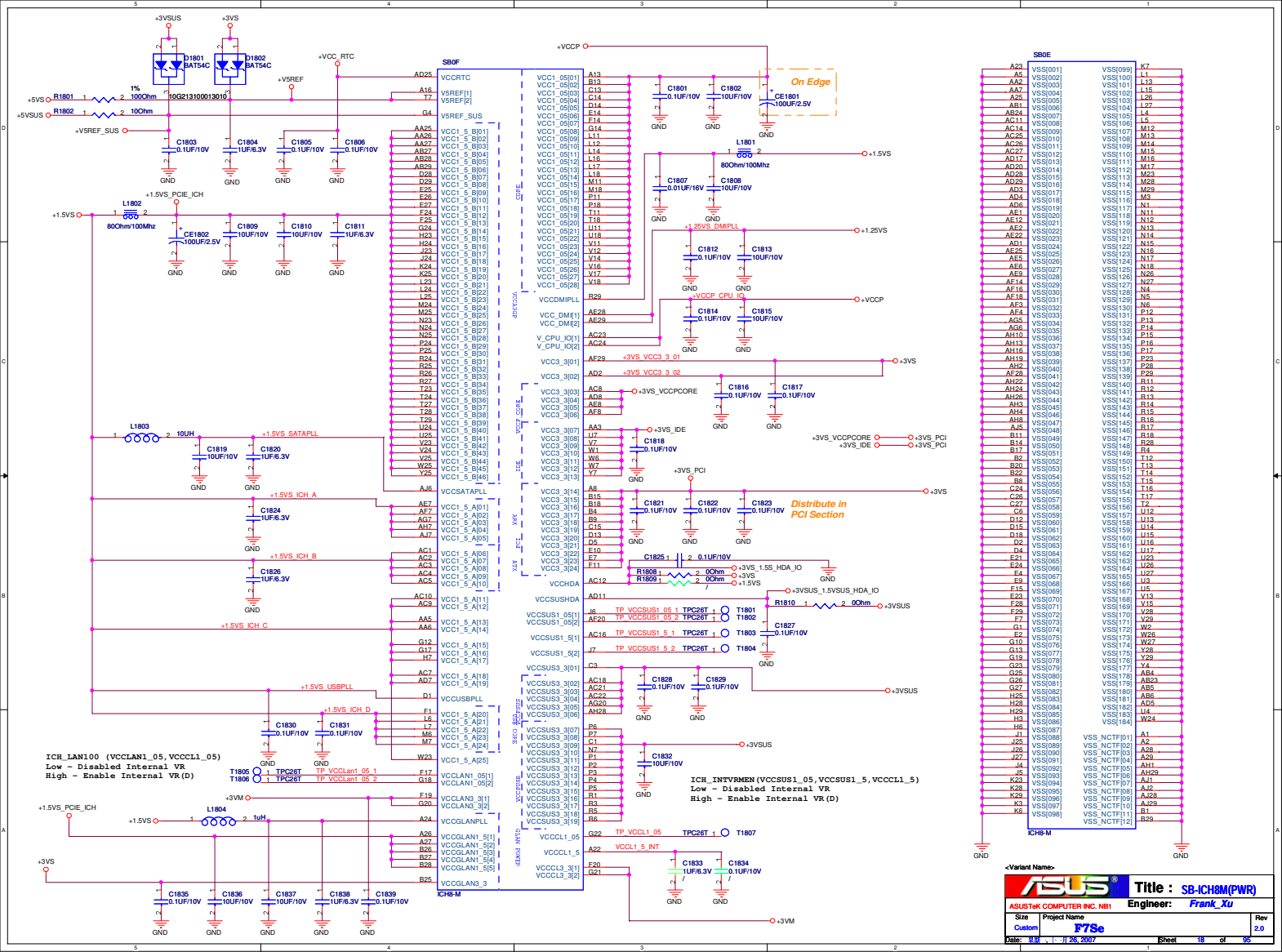
VSS

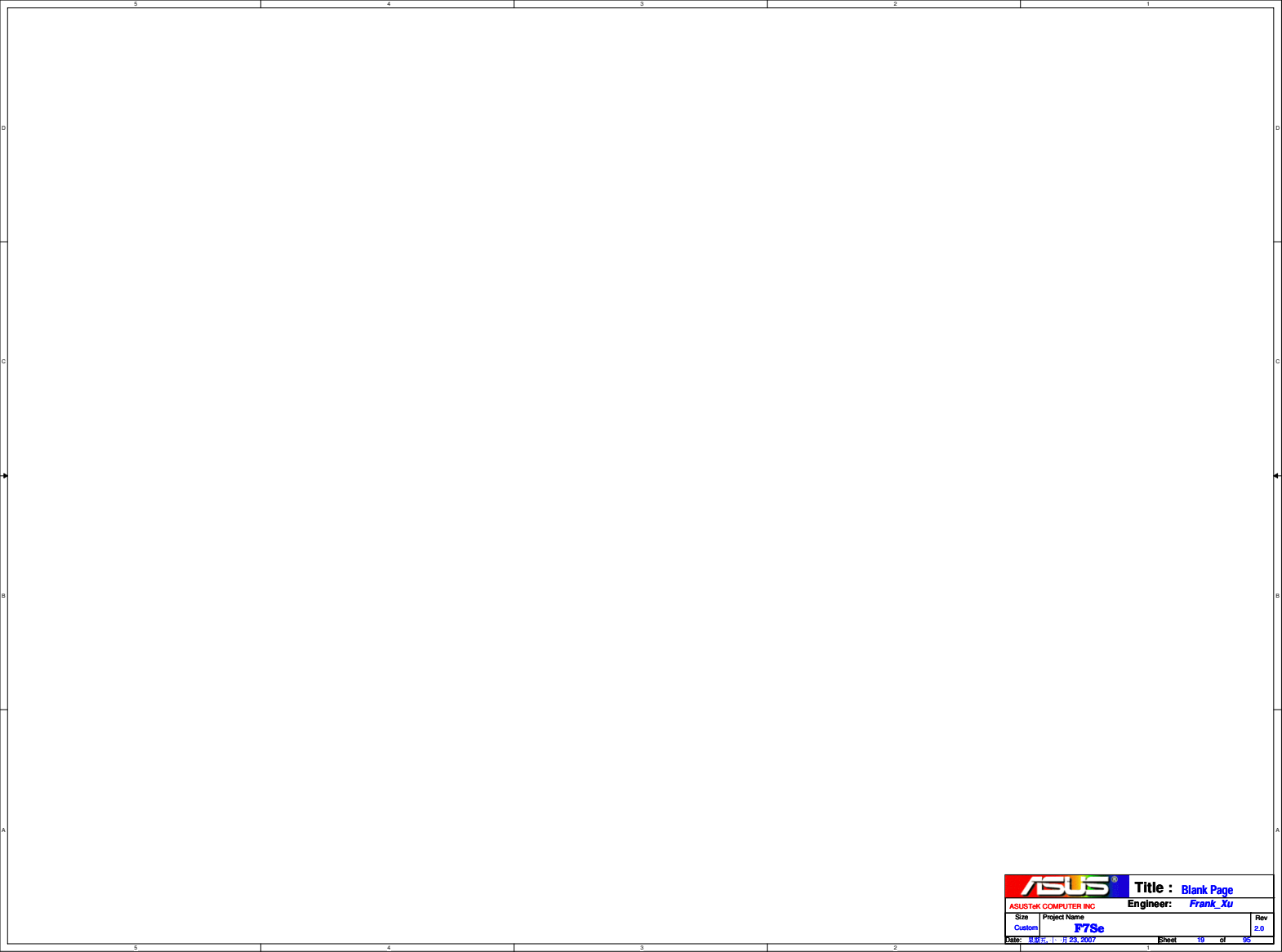
VSS



<Variant Name>





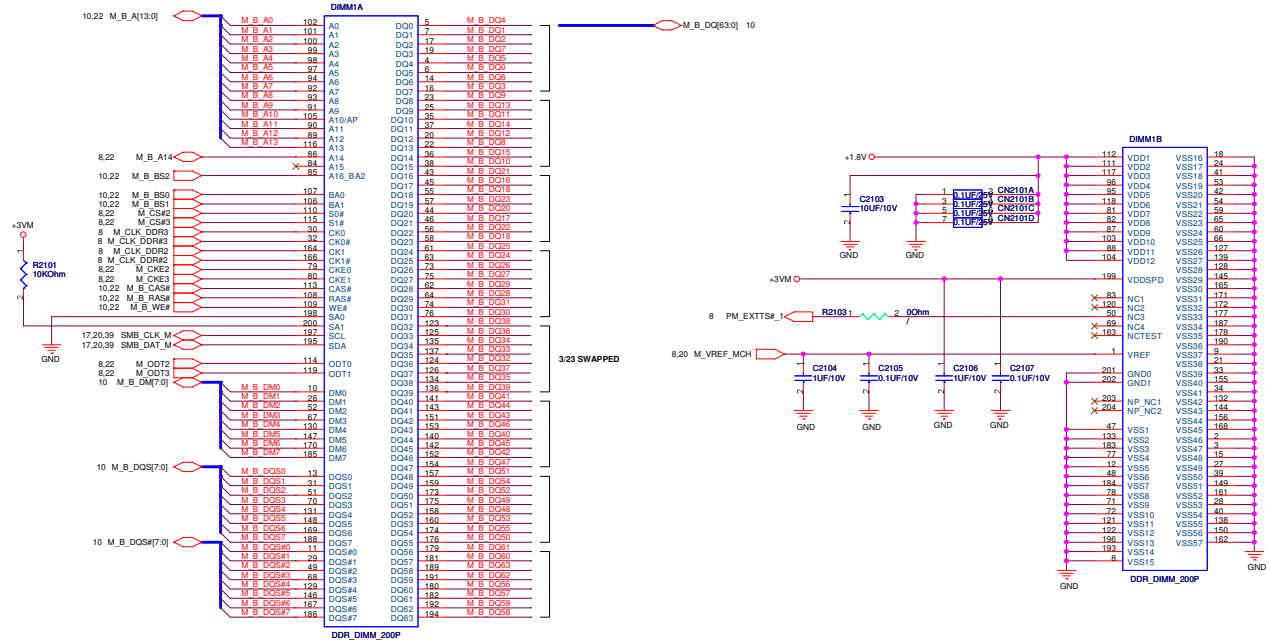


<Variant Name>



Title : DDR2 SO-DIMM0
Engineer: *Frank_Xu*

STD Type - 12G025122000

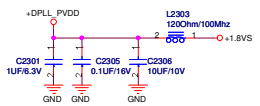


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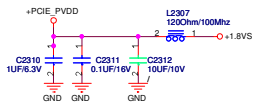


M82/M86ME Power

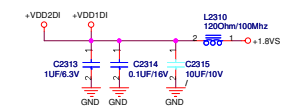
1.8V (? %) @ 120MA DPLL_PVDD M8X-M



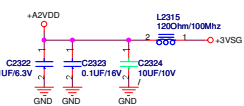
1.8V @ 40mA PCIE_PVDD M8X-M



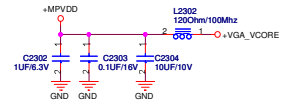
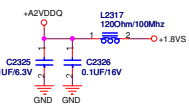
1.8V @ 121MA VDD1DI+VDD2DI FOR M8XM



3.3V @ 135MA A2VDD FOR M8XM

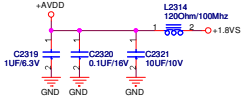


1.8V @ 2MA A2VDDQ FOR M8XM

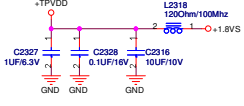


(0.95V-1.1V @ 414MA MPVDD)

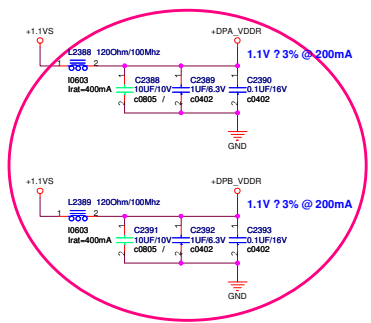
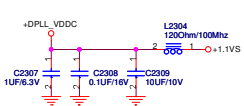
1.8V @ 100MA AVDD FOR M8XM



1.8V ? 3% @ 40 mA for M8XM



1.1V @ 300MA DPLL_VDDC FOR M8XM



<Variant Name>

ASUS®		Title : VGA M82-M XT POWER	
ASUSTek COMPUTER INC		Engineer: Frank_Xu	
Size	Project Name		Rev
Custom	F7Se		2.0
Date: 8/23/2007		Sheet 29	of 95

[illegible]

GPIO[11:13] = 001, 256M memory aperture
 GPIO[11:13] = 001, 512M memory aperture

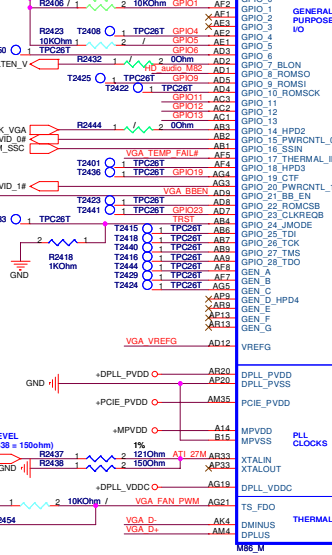
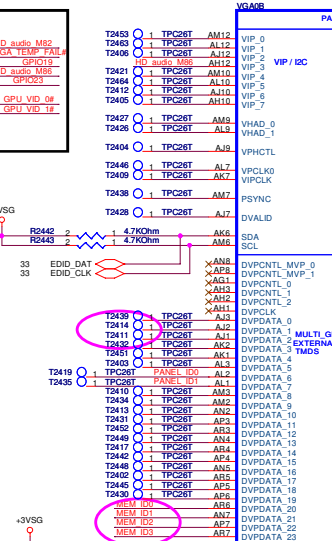
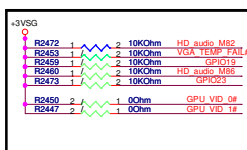
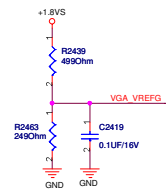
Memory ID: (Only Channel A)
256M
ID3 ID2 ID1 ID0
Samsung MID 0 0 0 1 =>ID1

PU_VID_0#	GPU_VID_1#	+VGA_VCORE
L	L	1.2V
H	L	0.9V
H	H	1.1V

A detailed pinout diagram for the MAX6675 module. The module is shown as a black PCB with components labeled: RN2401A, RN2401B, RN2401C, RN2401D, U2402, MAX6675, and GND. The pin headers are color-coded: red for power (VCC, GND), green for data (SCL, SDA, DXP, DNX, D-), and blue for control (VGA_THERM#, SCL, SDA, ALARM#). The diagram shows the following connections:

- Power:** +3VSG connects to VCC (pin 1) and GND (pin 5).
- Data:** SCL (pin 8) connects to SCL (pin 2), SDA (pin 7) connects to SDA (pin 3), DXP (pin 4) connects to DXP (pin 6), and DNX (pin 9) connects to DNX (pin 7).
- Control:** VGA_THERM# (pin 10) connects to D- (pin 8) and VGA_THERM# (pin 9).
- Other:** The module also has pins for SCL (pin 1), SDA (pin 2), ALARM# (pin 3), and GND (pin 4).

FOR M8XM
VREFG VOLTAGE DIVIDER IS $VREFG = VDDR_{4,5} = 1.8V / 3 = 0.6V$
 $R_{2463} = 249\Omega$



PART 2 OF 7		
16	VP_0	
17	VP_1	
18	VP_2	VP / BC
19	VP_3	
20	VP_4	
21	VP_5	
22	VP_6	
23	VP_7	
24	VHAD_0	
25	VHAD_1	
26	VHCTL	
27	VPCLOCK	
28	VPCLOCK	
29	PSYNC	
30	DVALD	
31	SDA	
32	SCL	
33	DVPCTRL_VMF_0	
34	DVPCTRL_VMF_1	
35	DVPCTRL_0	
36	DVPCTRL_1	
37	DVPCTRL_2	
38	DVPCTRL_3	
39	DVPCTRL_4	MULTI_GFX
40	DVPCTRL_5	EXTERNAL
41	DVPCTRL_6	INCH
42	DVPCTRL_7	
43	DVPCTRL_8	
44	DVPCTRL_9	
45	DVPCTRL_10	
46	DVPCTRL_11	
47	DVPCTRL_12	
48	DVPCTRL_13	
49	DVPCTRL_14	
50	DVPCTRL_15	
51	DVPCTRL_16	
52	DVPCTRL_17	
53	DVPCTRL_18	
54	DVPCTRL_19	
55	DVPCTRL_20	
56	DVPCTRL_21	
57	DVPCTRL_22	
58	DVPCTRL_23	

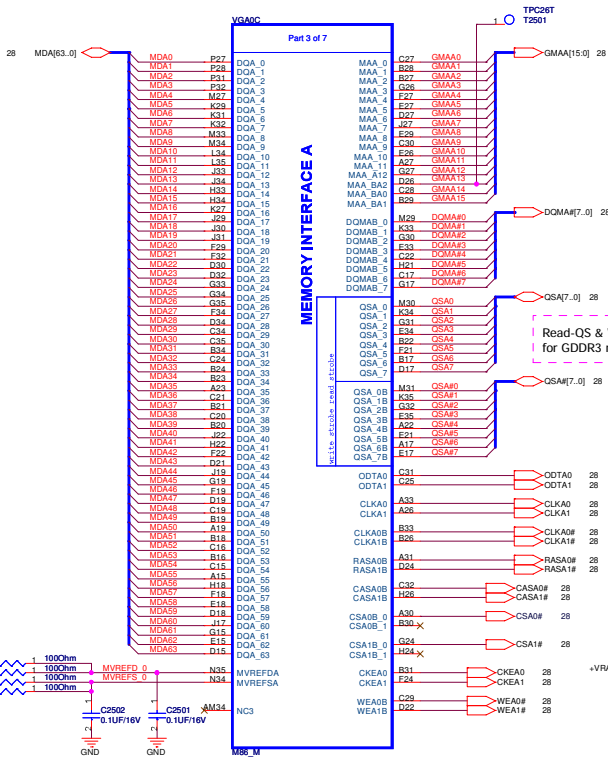


TABLE 1

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

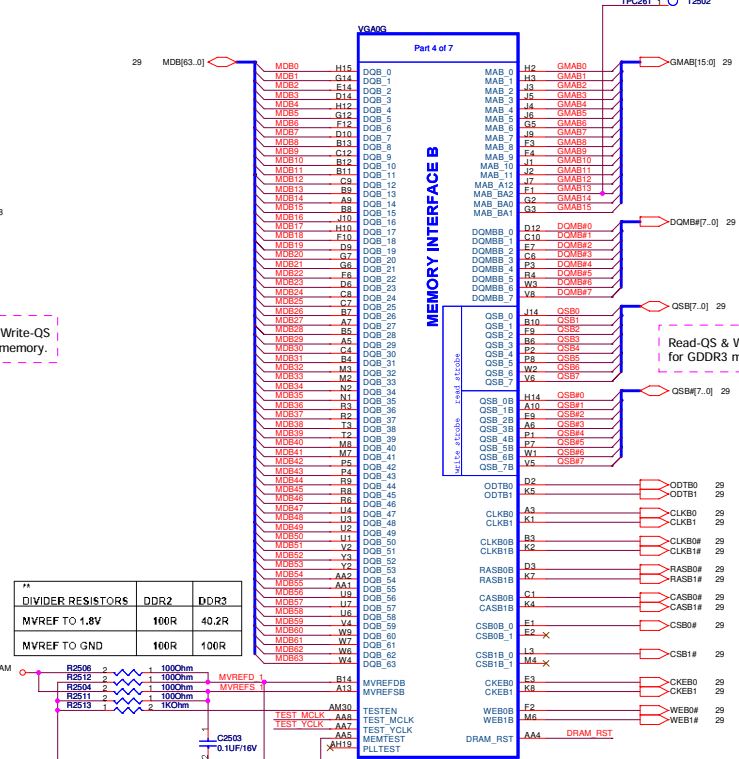
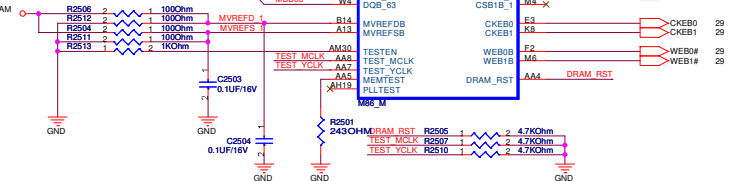
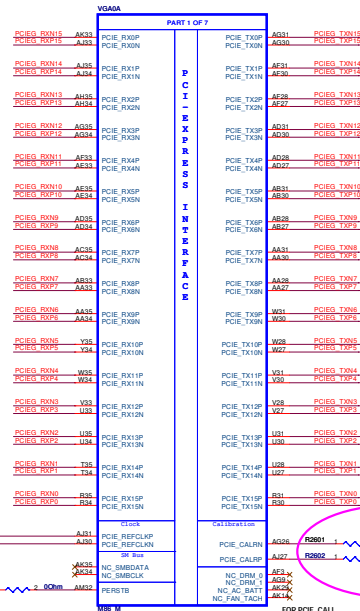
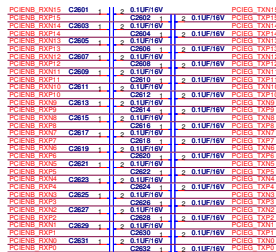


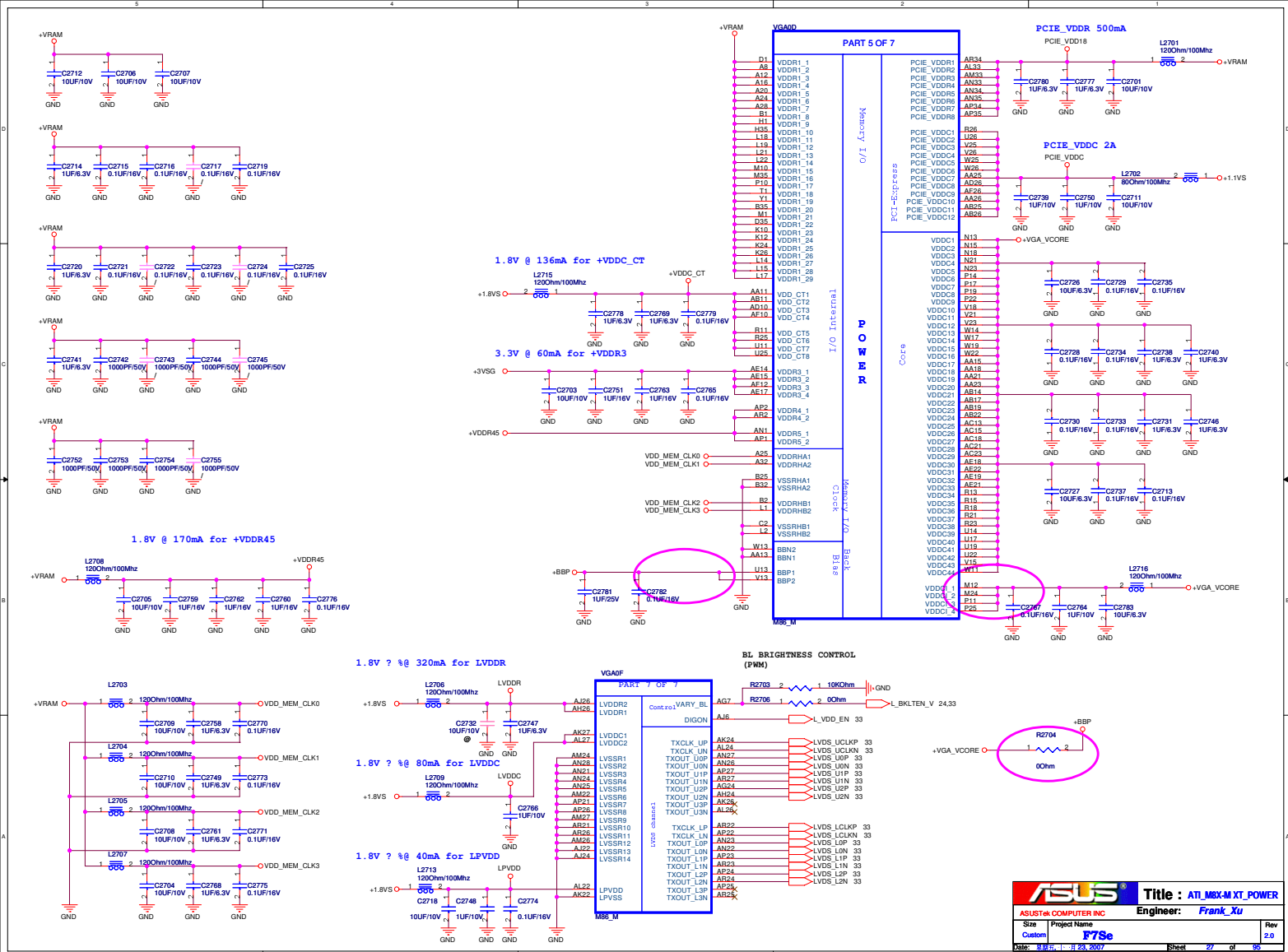
TABLE 2

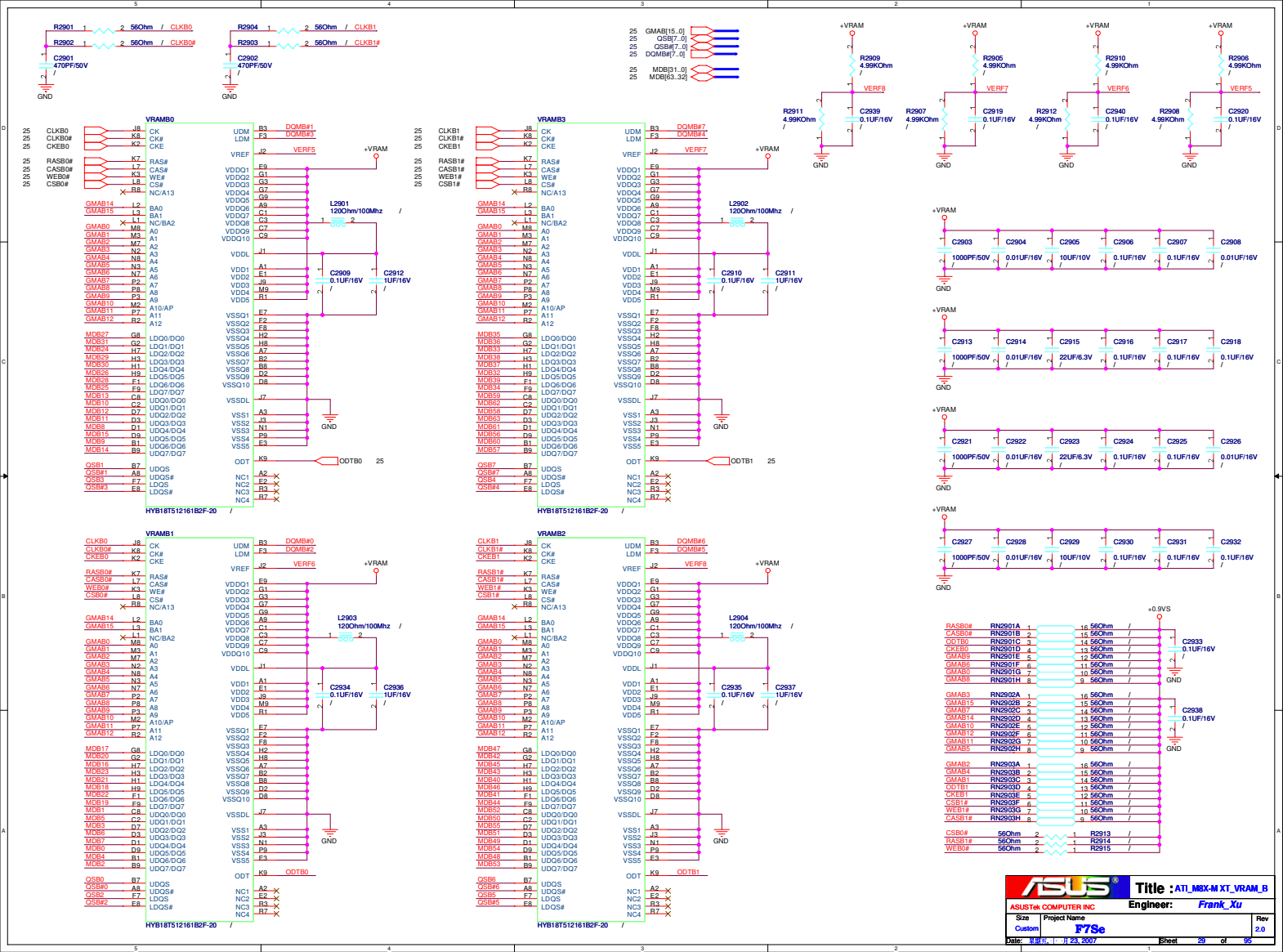
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

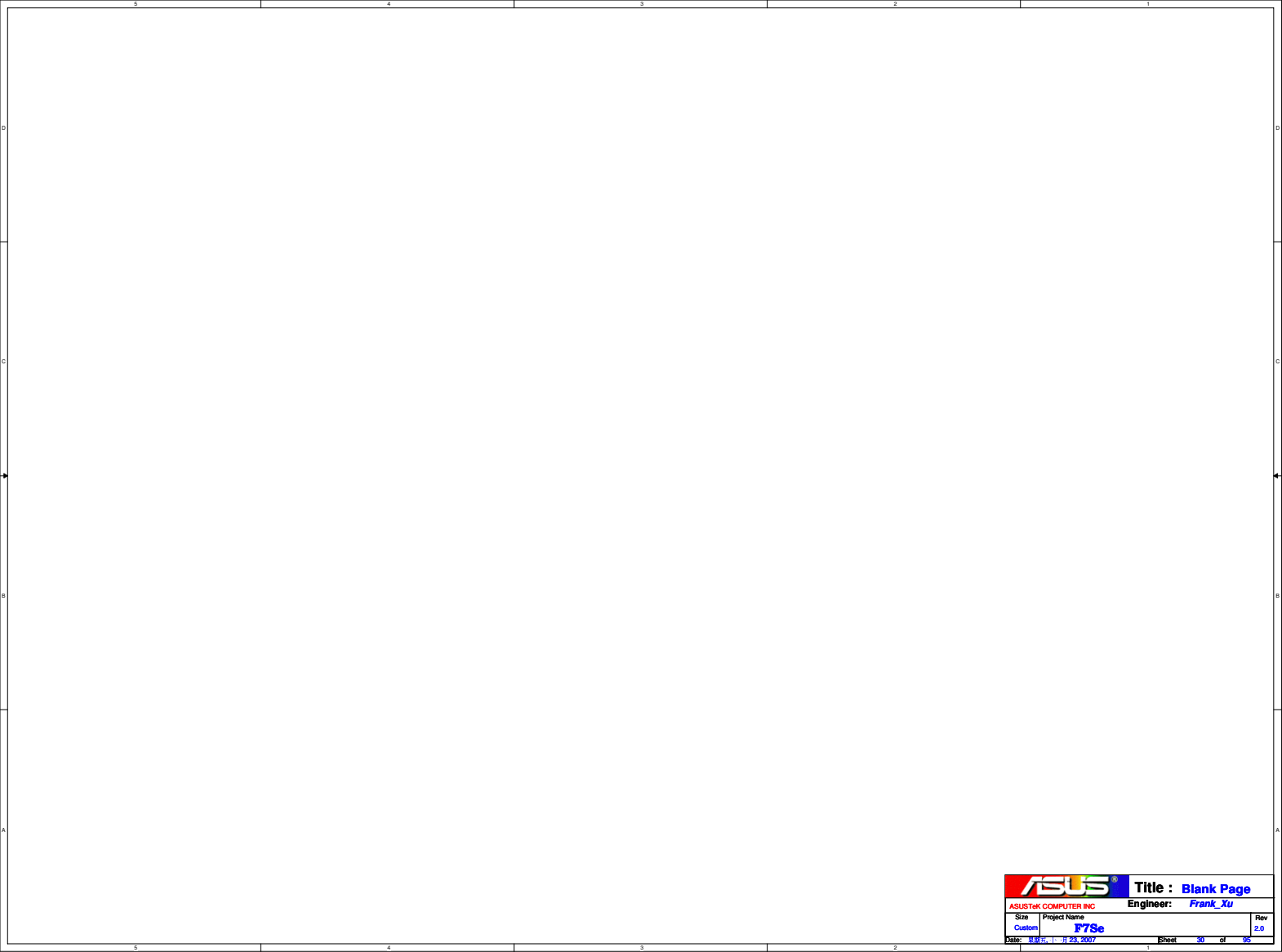




FOR PCIE_CALRP
INSTALL 1.27K TO PCIE_VSS FOR M76
INSTALL 562R TO PCIE_VSS FOR M66



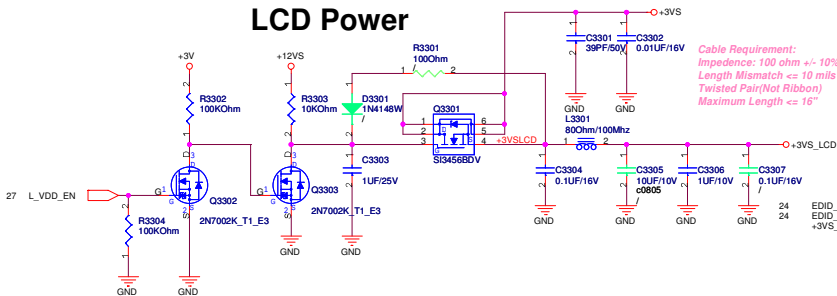




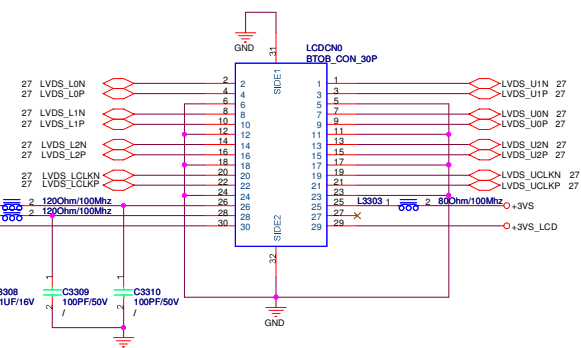


LCD Backlight Control

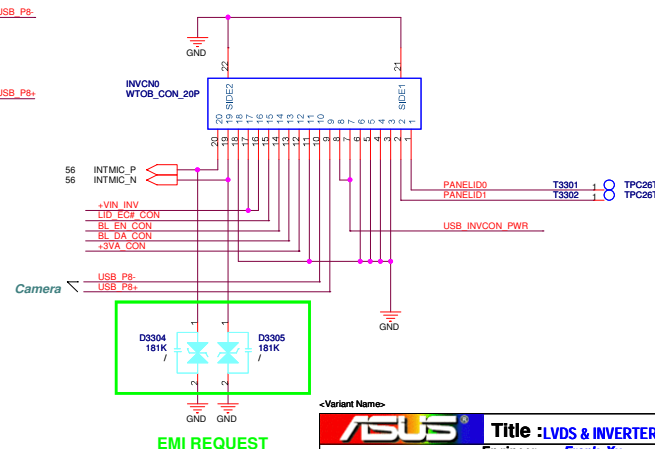
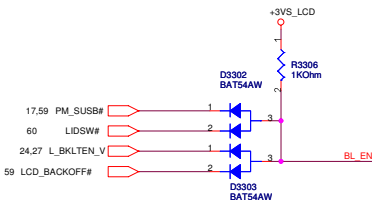
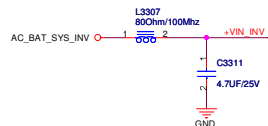
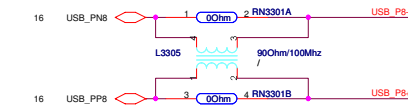
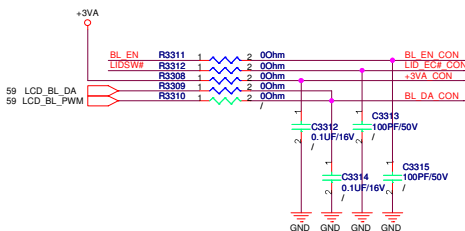
LCD Power

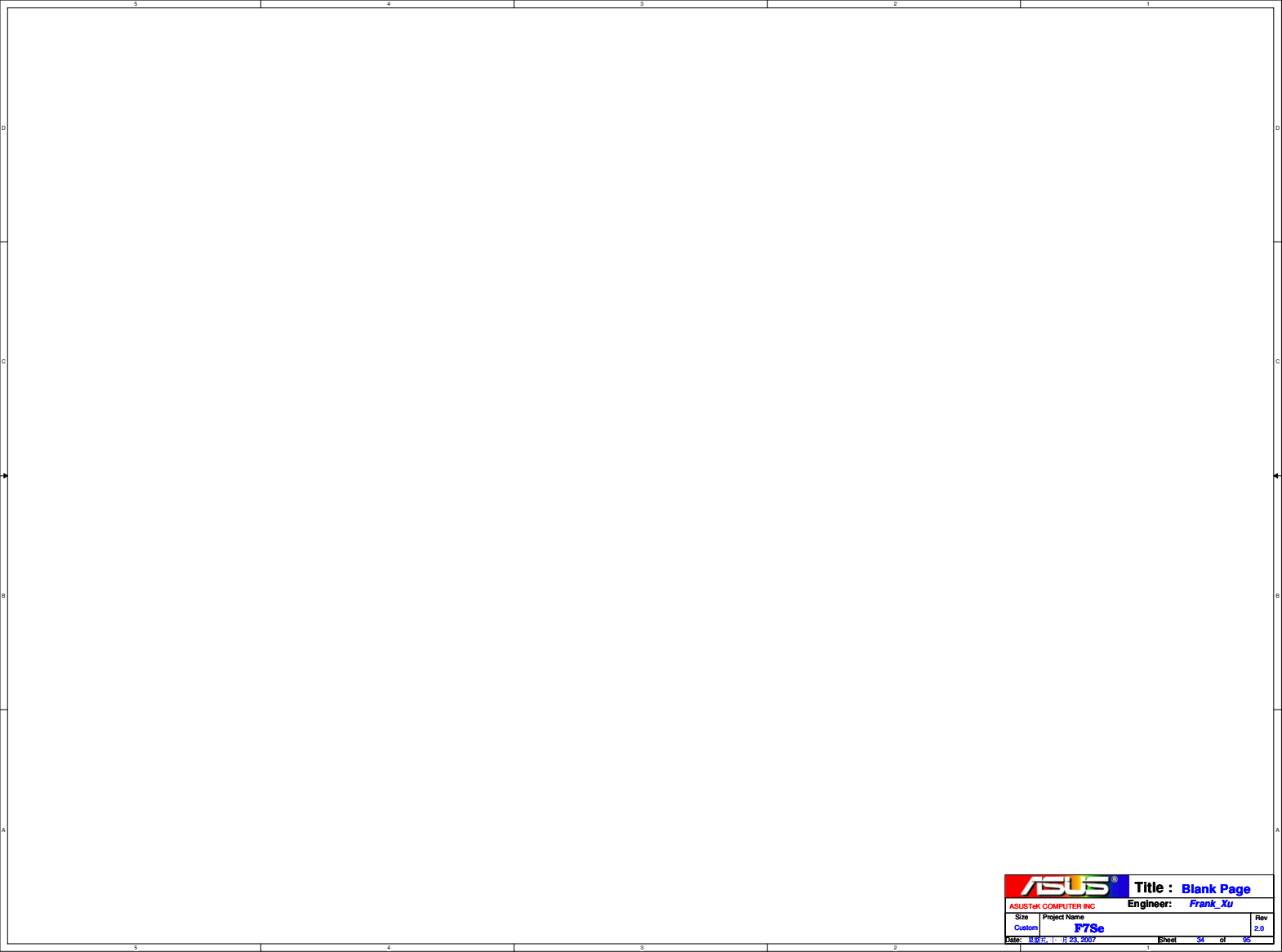


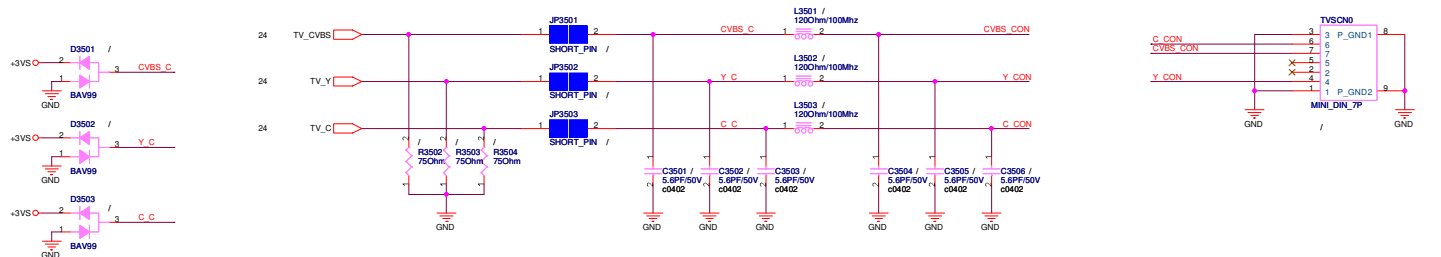
LCD LVDS Interface



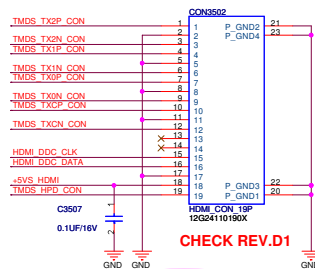
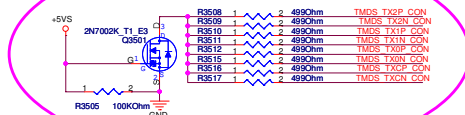
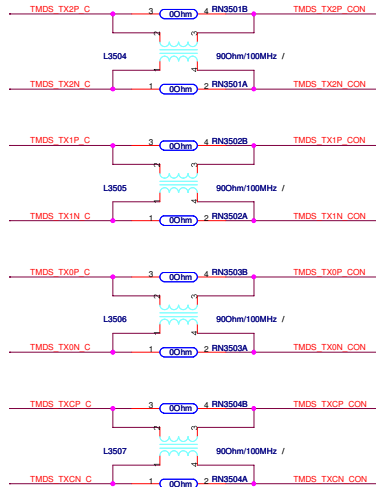
INVERTER Interface/Speaker CONN.





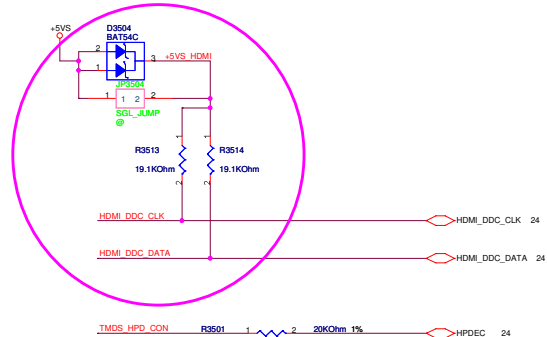
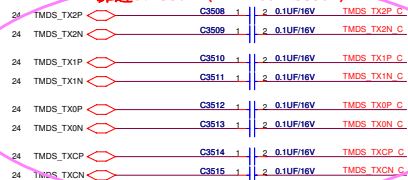


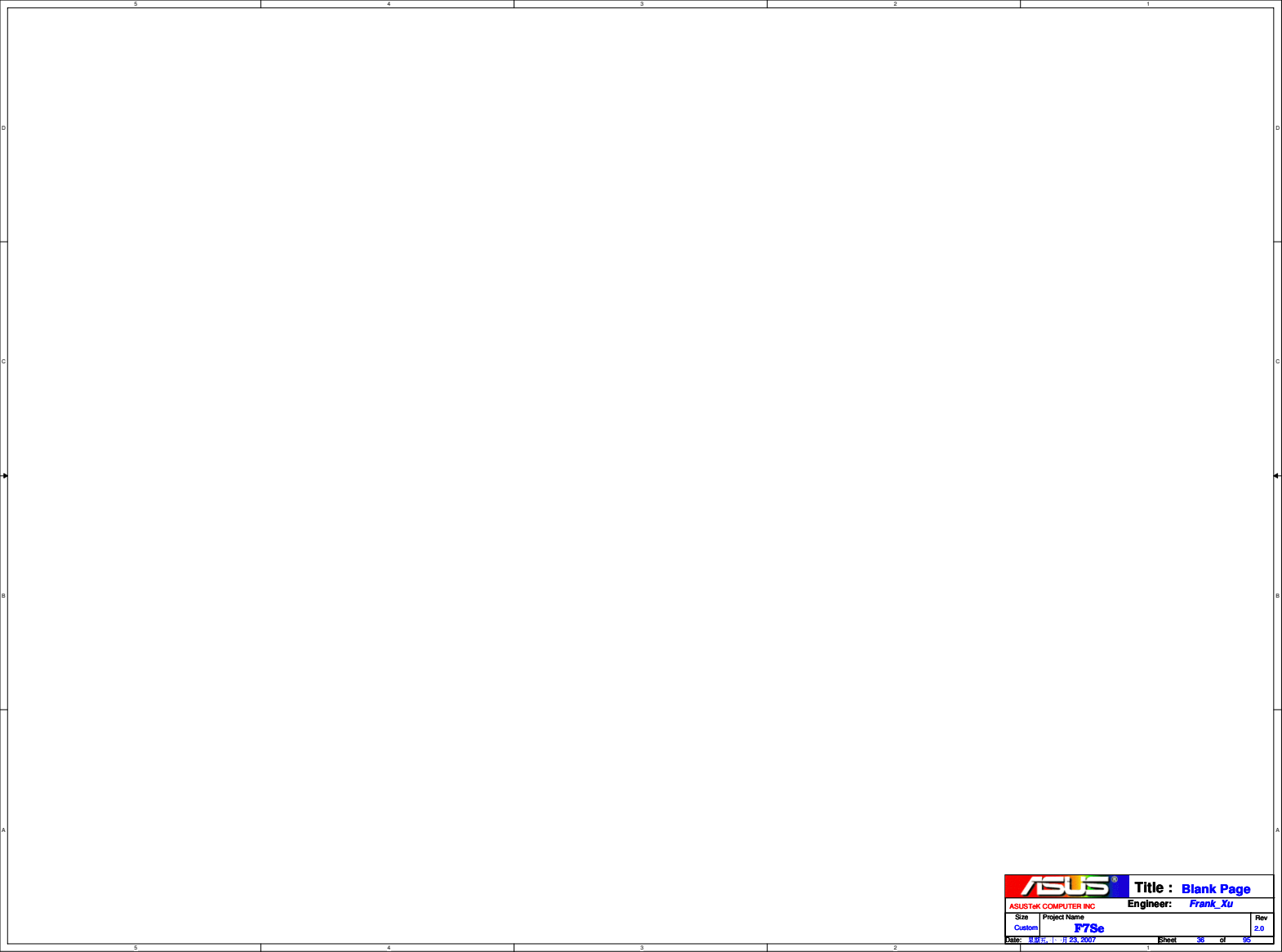
HDMI



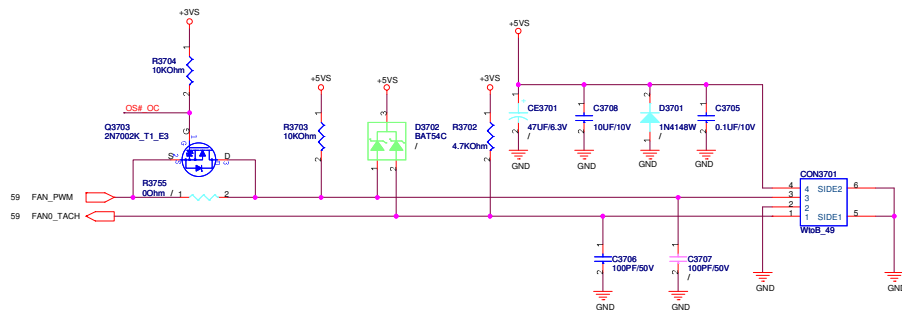
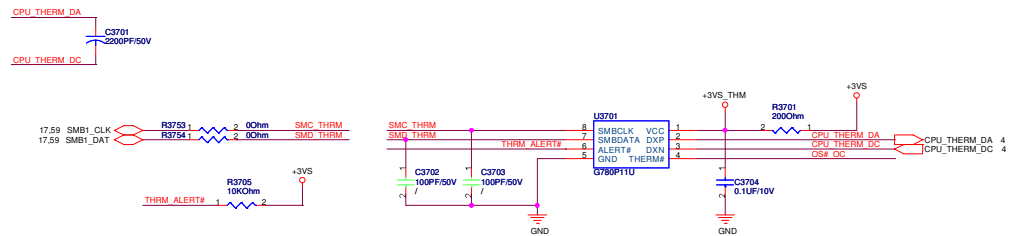
CHECK REV.D1

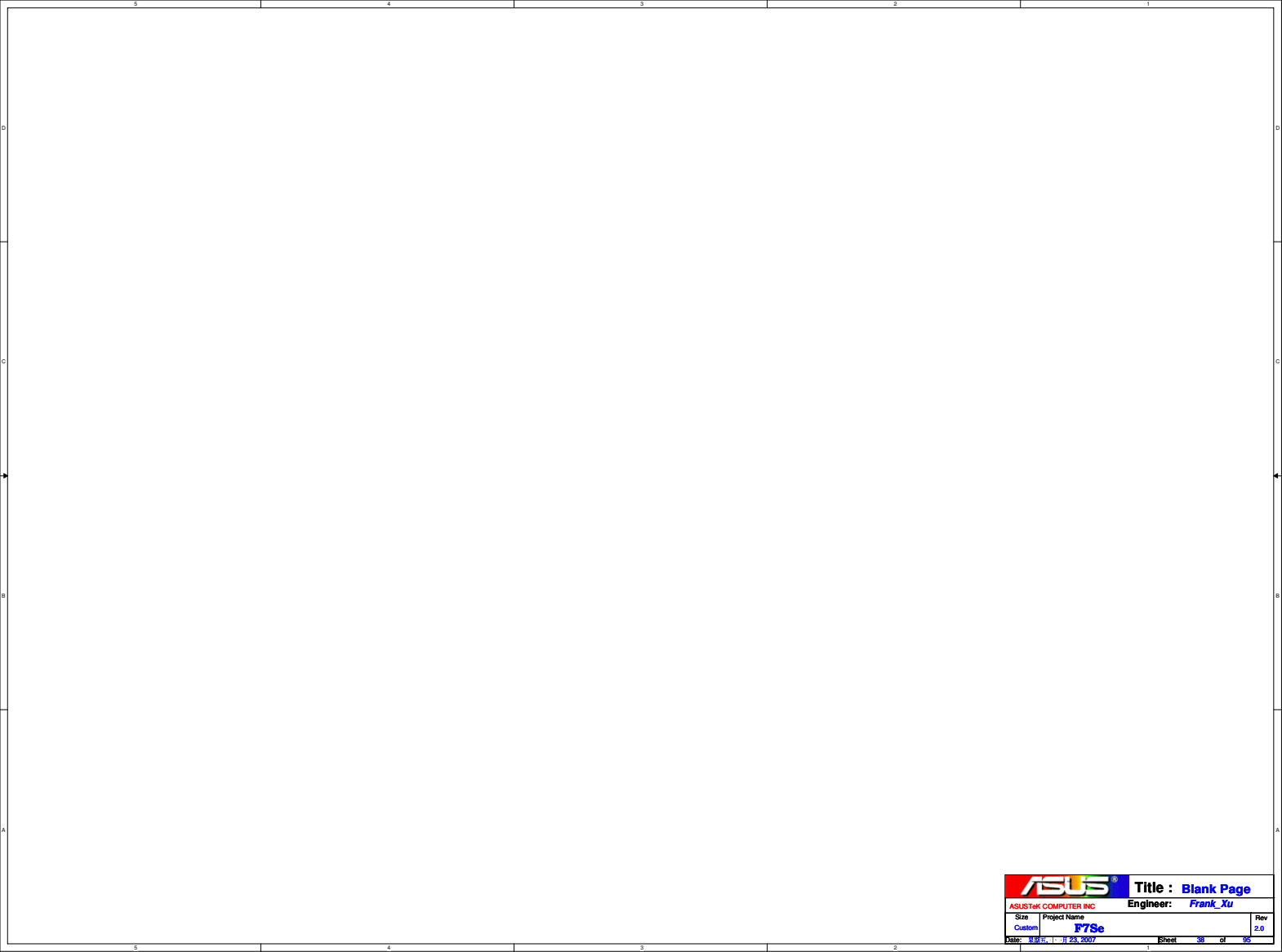
靠近CON3502 (HDMI Connector)

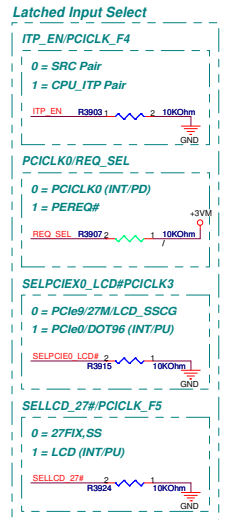
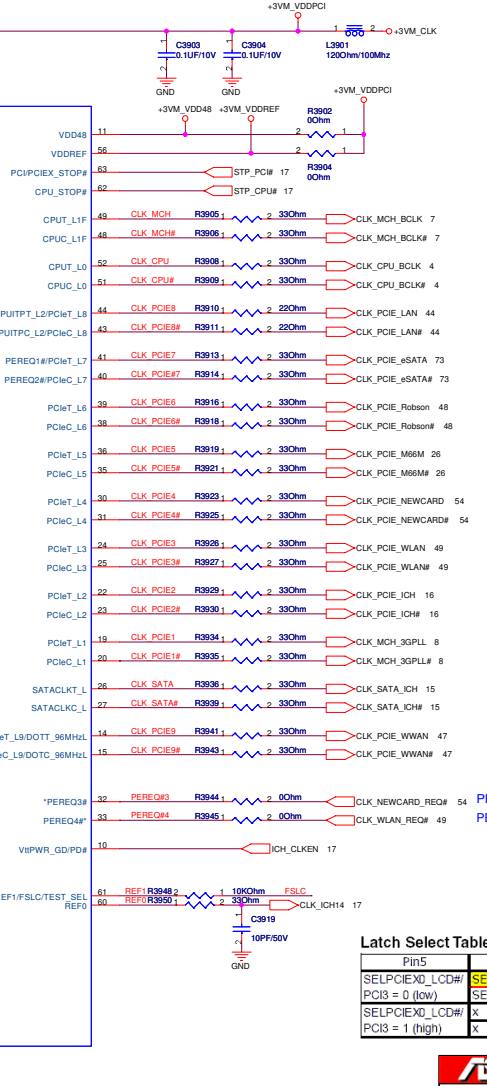
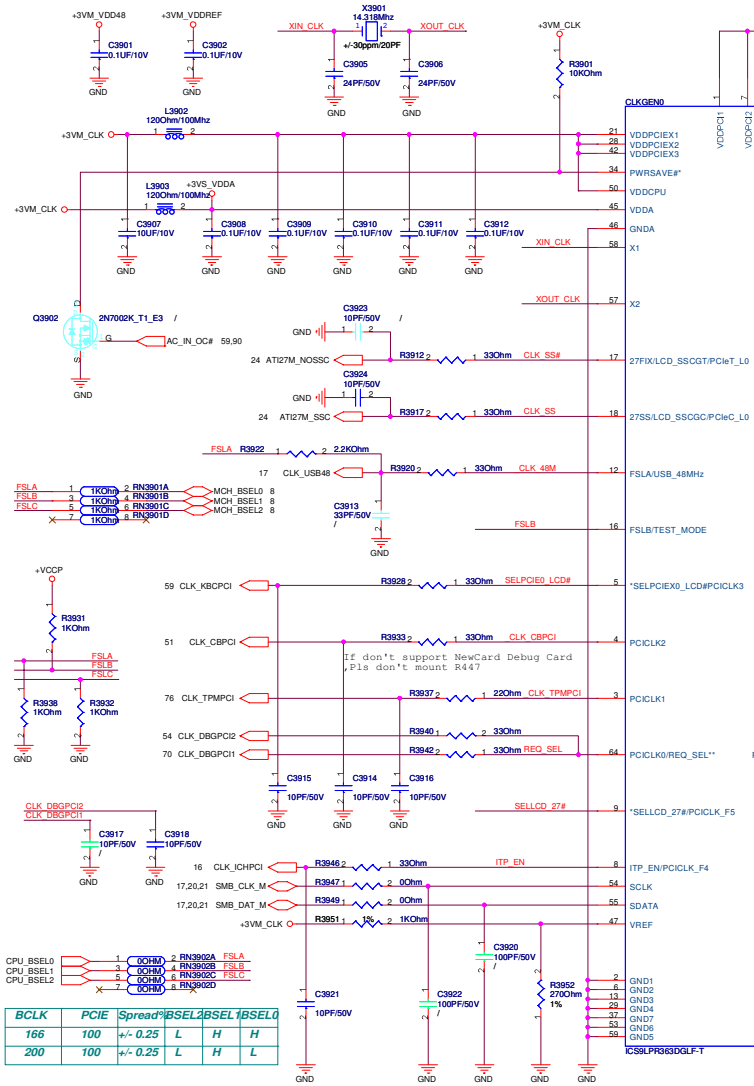




DC FAN Control

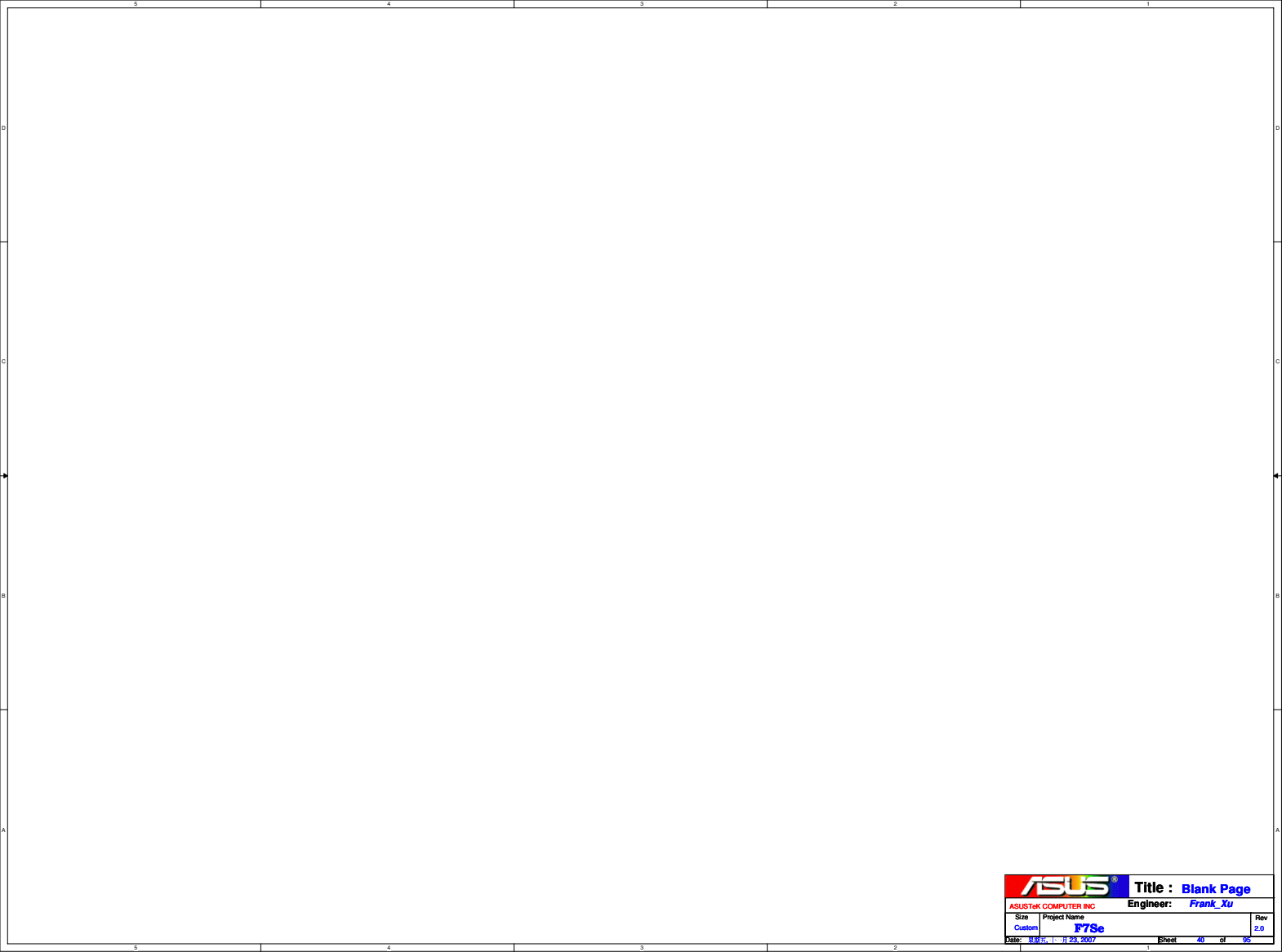


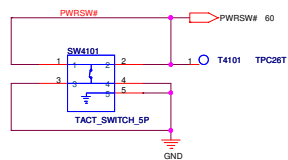
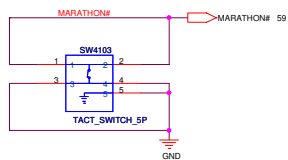




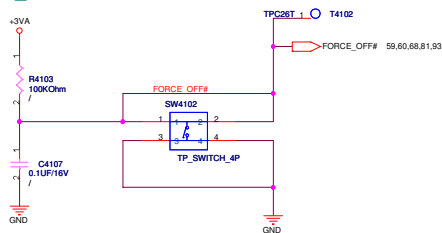
Latch Select Table

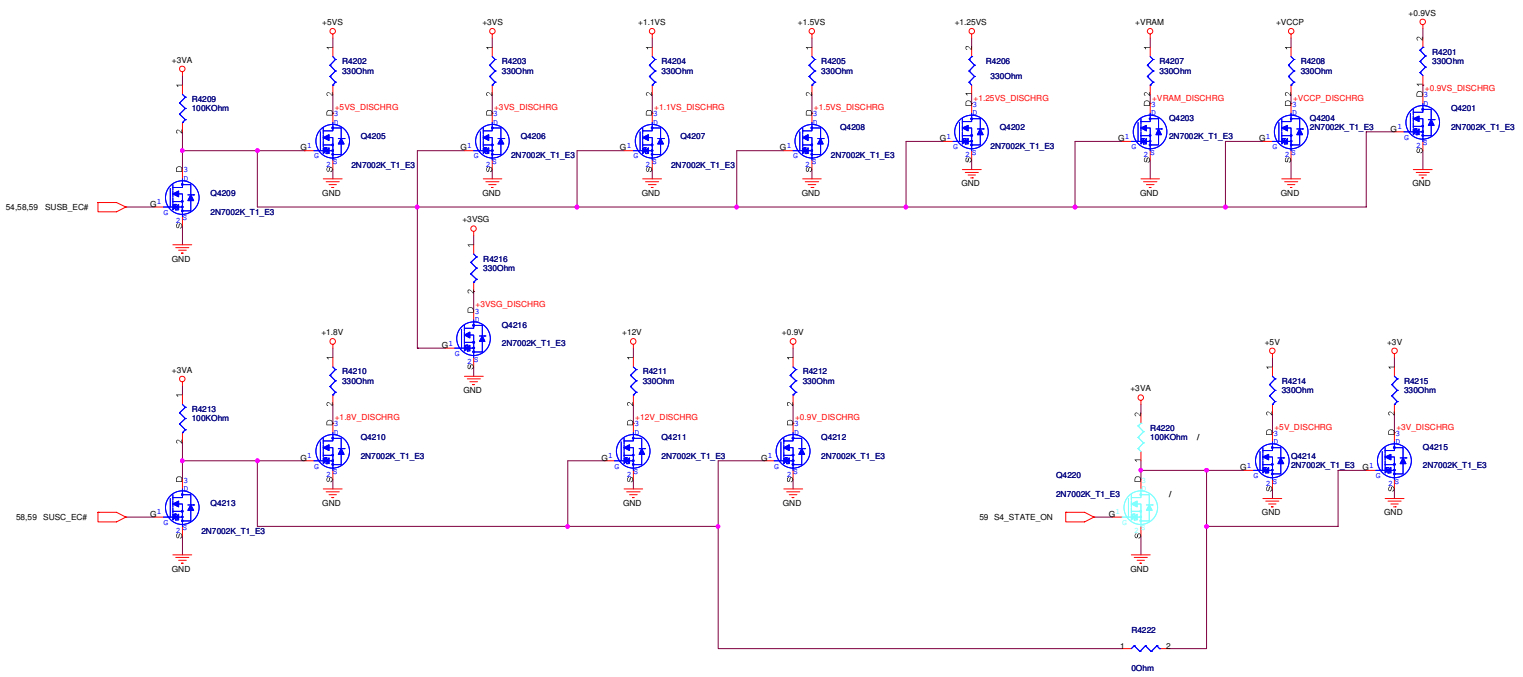
Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD#	SELLCD_27# = 0	PCIE0	27FXSS
PCICLK0 = 0 (low)	SELLCD_27# = 1	PCIE0	LCD
SELPCIE0_LCD#	x	PCIE0	PCIE0
PCICLK0 = 1 (high)	x	PCIE0	PCIE0

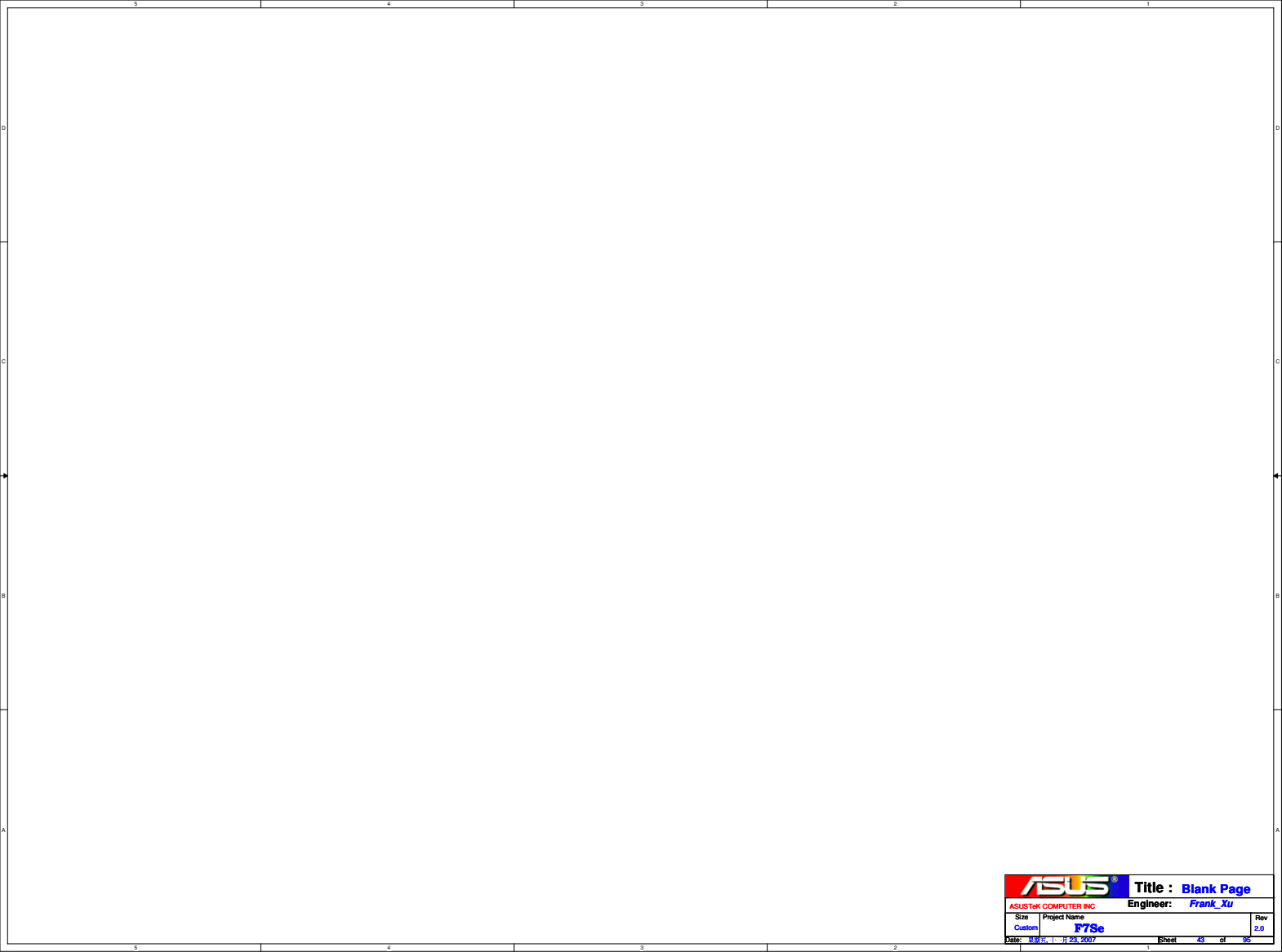




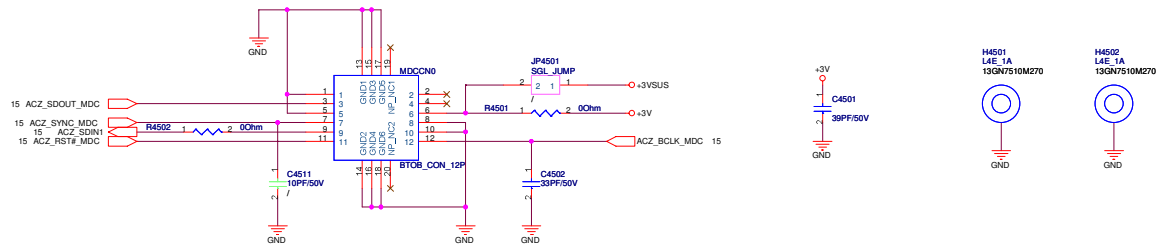
SHUT_DOWN#



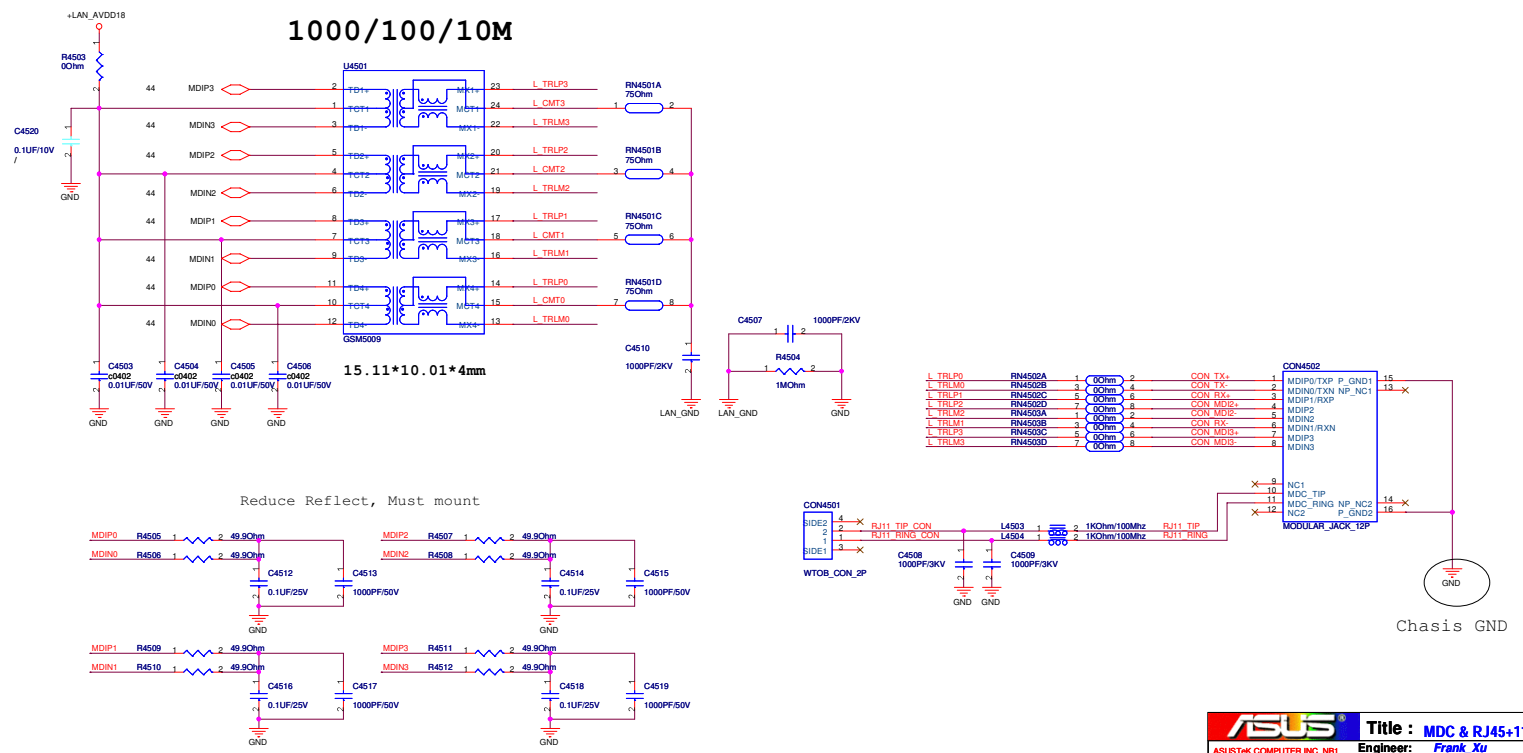


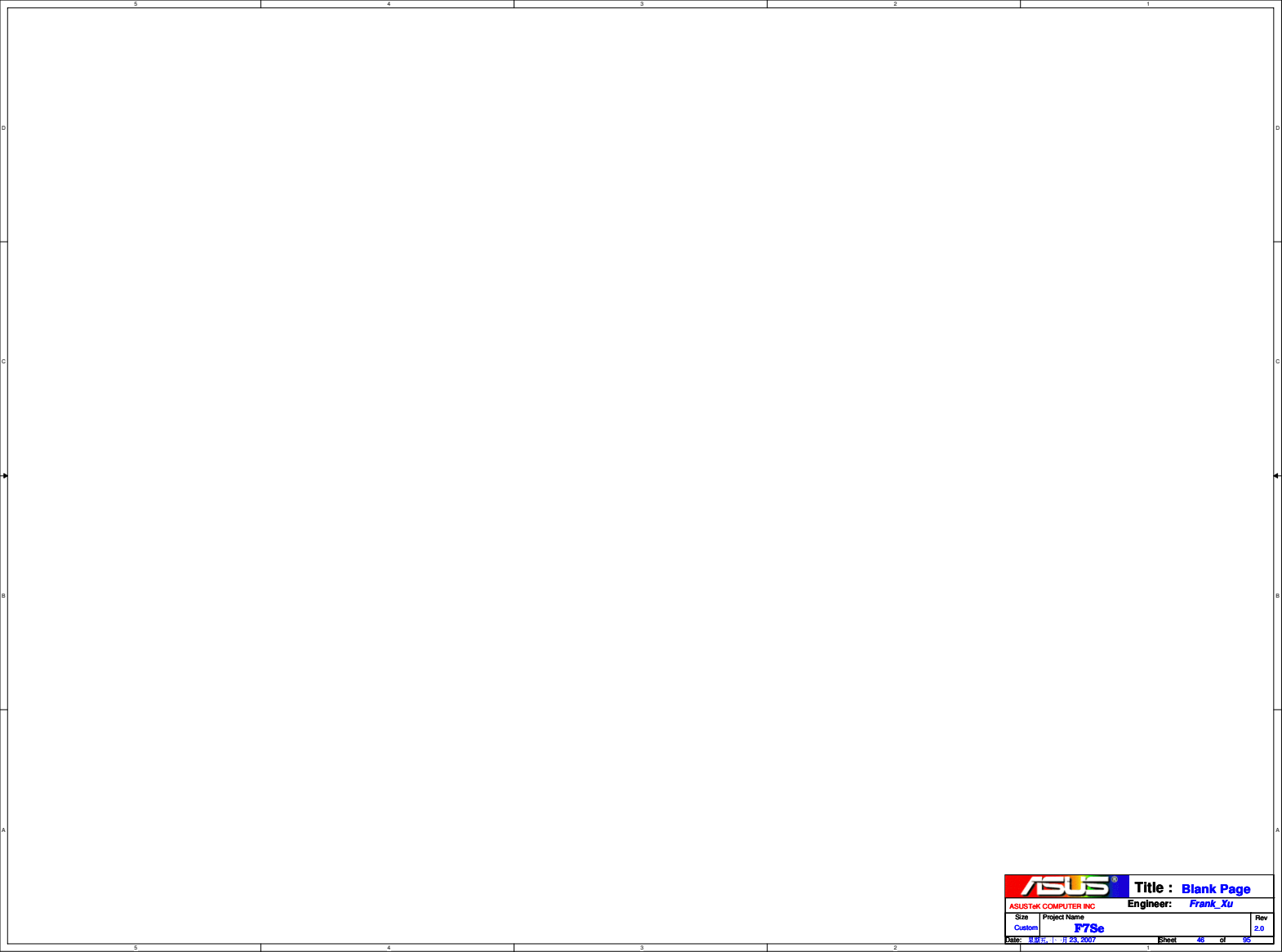


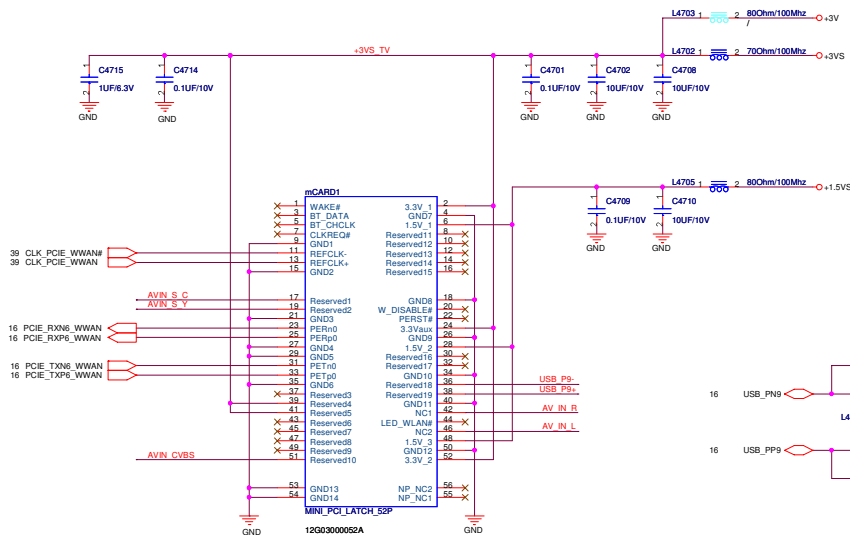
MDC CONN.



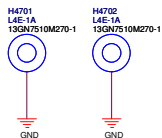
LAN CONN.



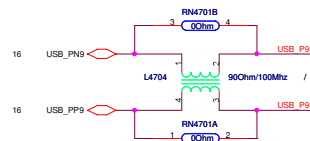




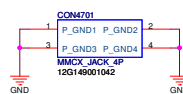
H = 5.2mm
FOR TV TUNER
(UWB OPTION)



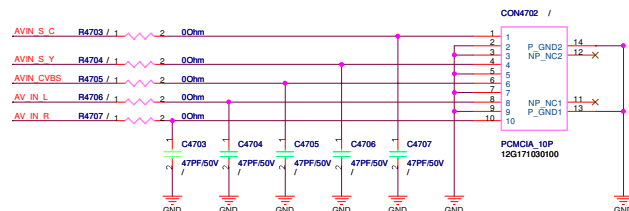
H = 3.0mm



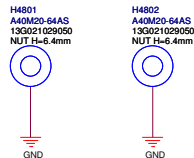
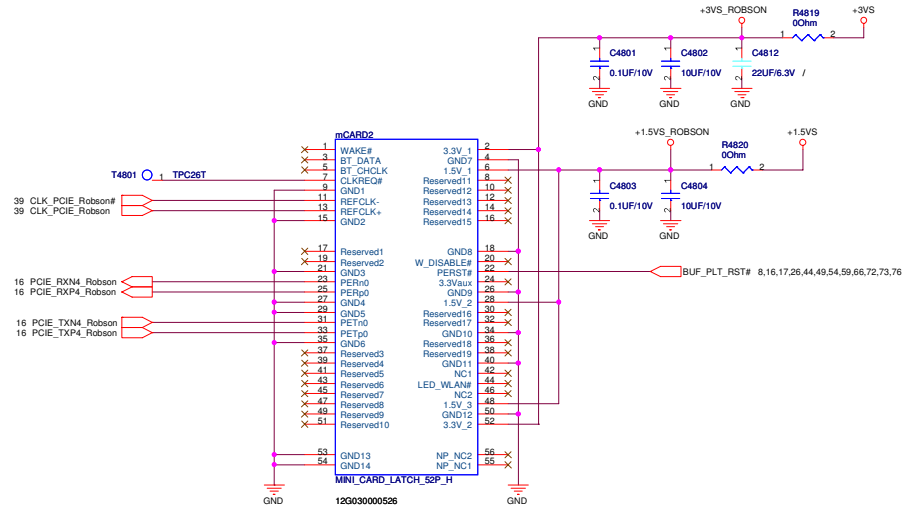
TV Conn.

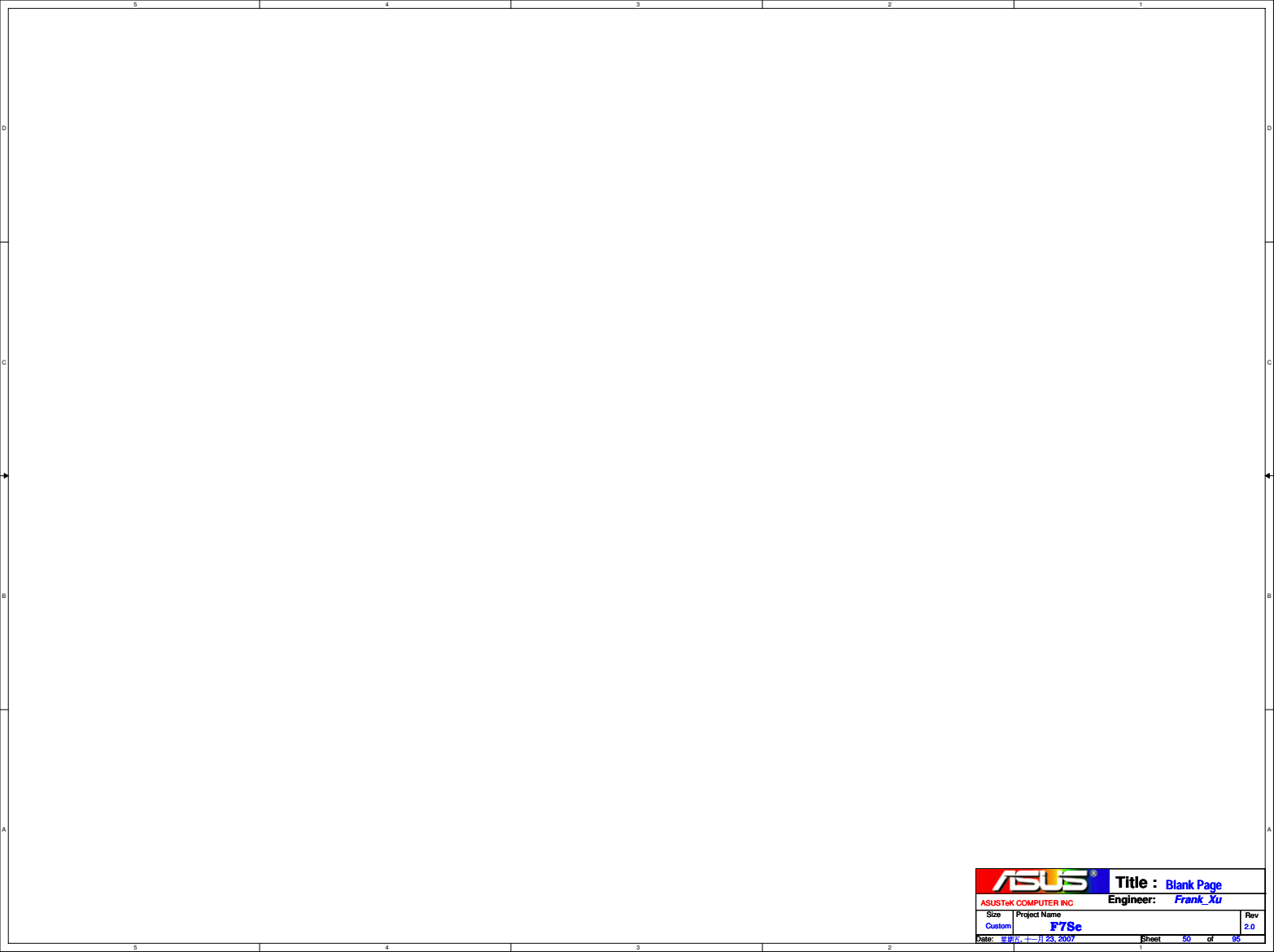


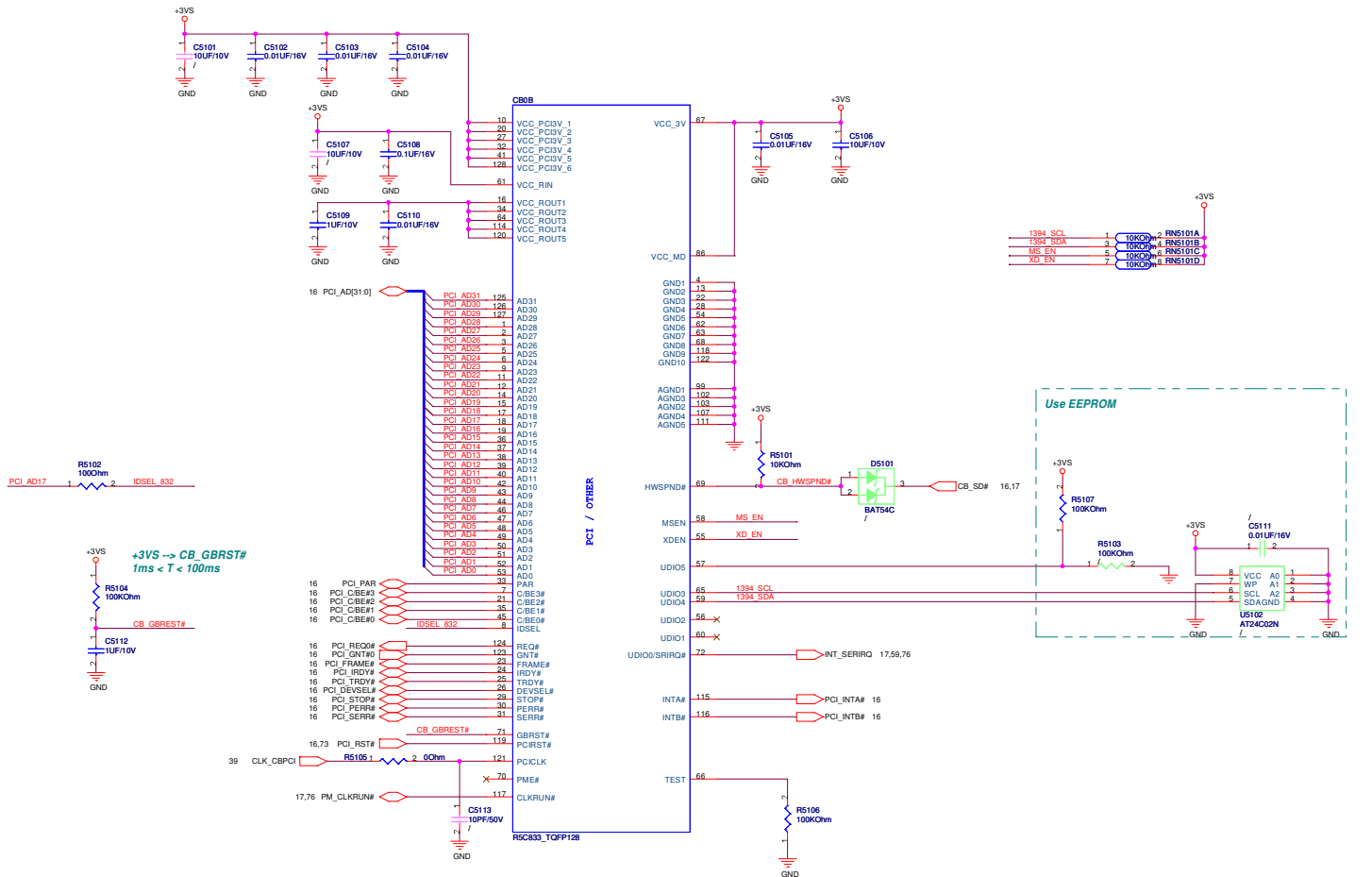
ME P/N : 14G152075000



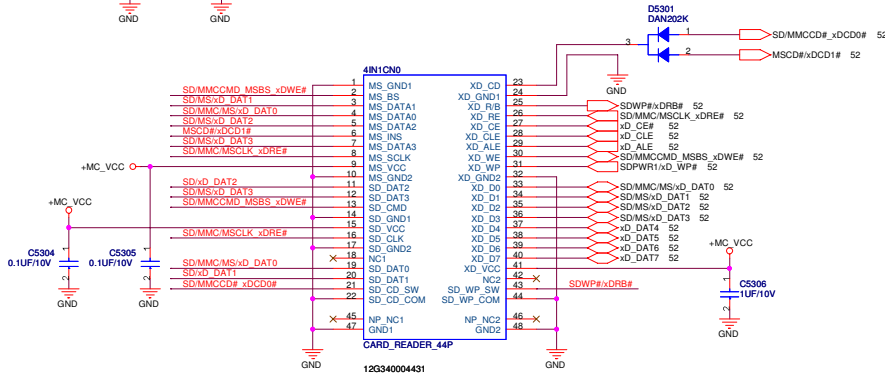
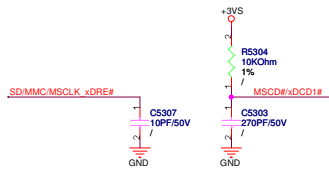
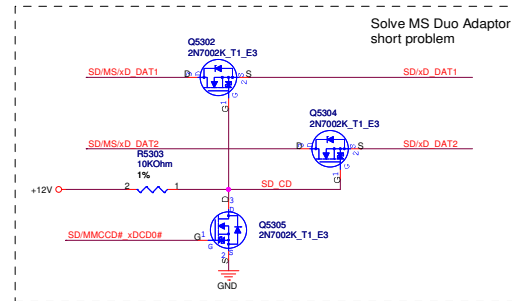
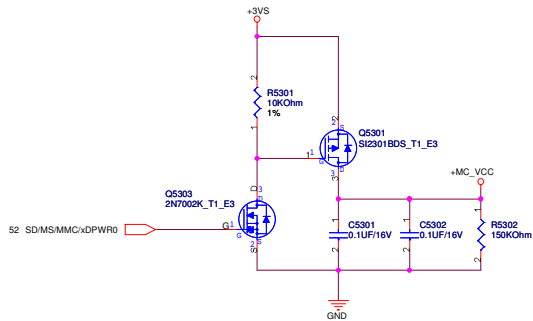
-Variant Name-

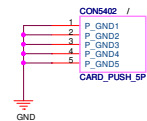
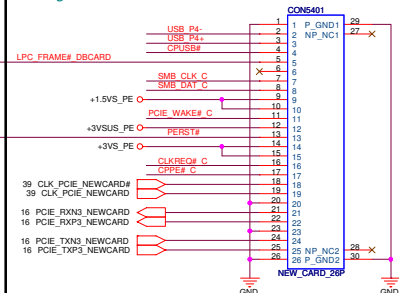
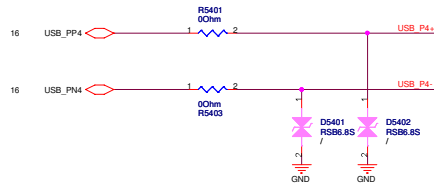




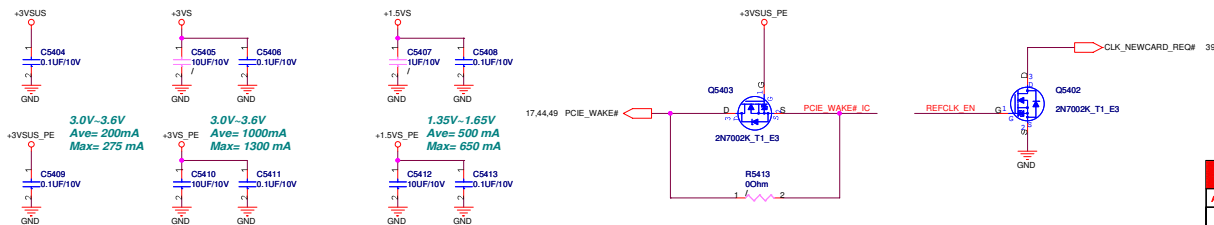


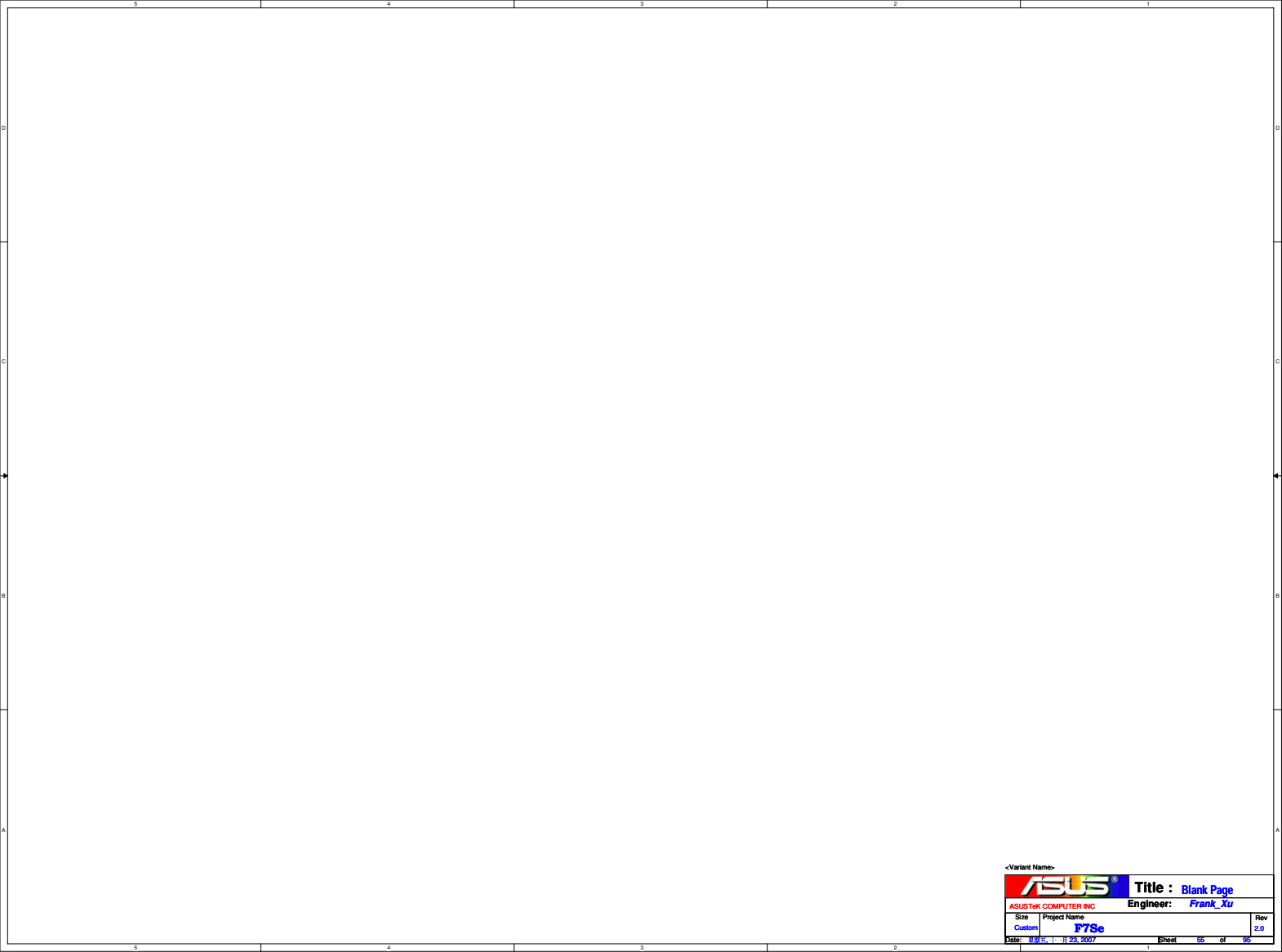
<-Variant Name>





If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN1,R445)



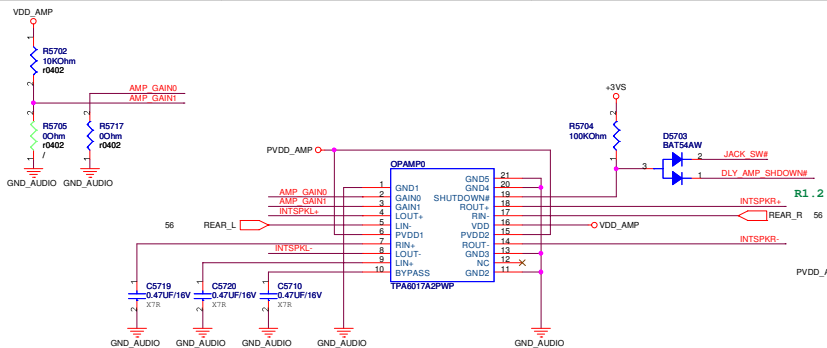


-Variant Name-

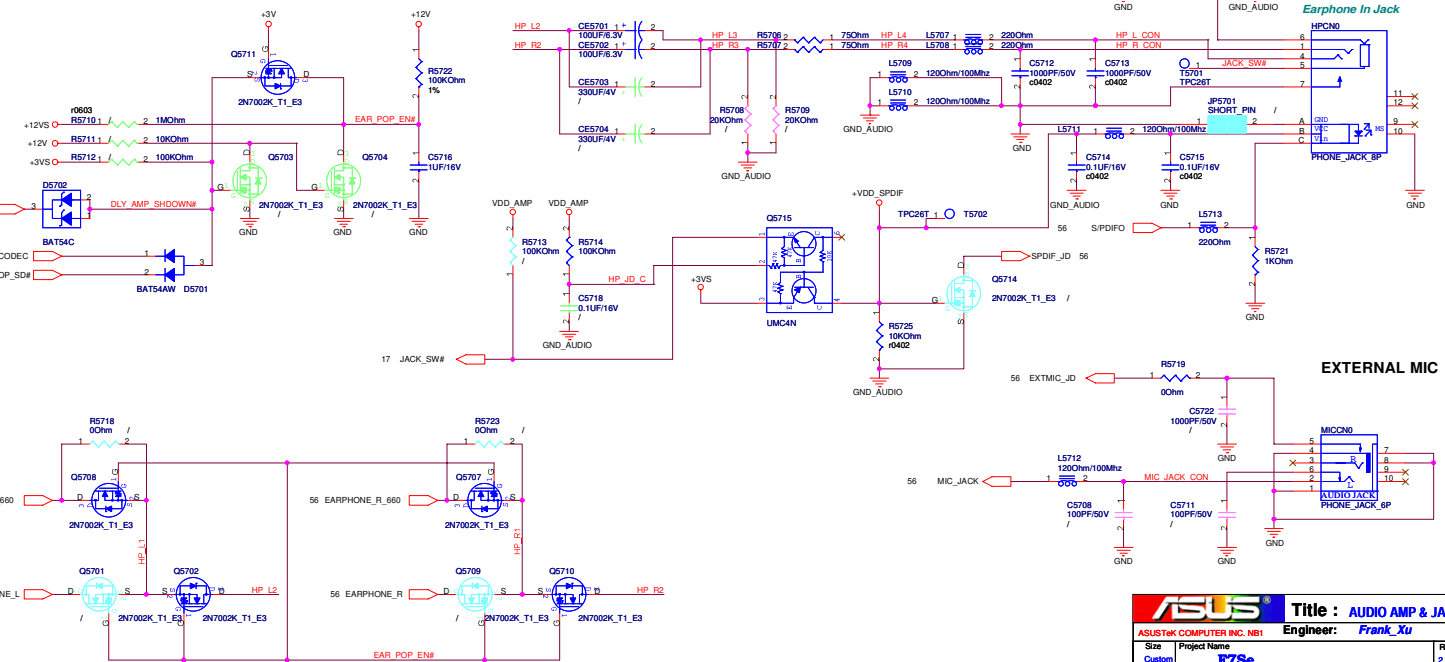
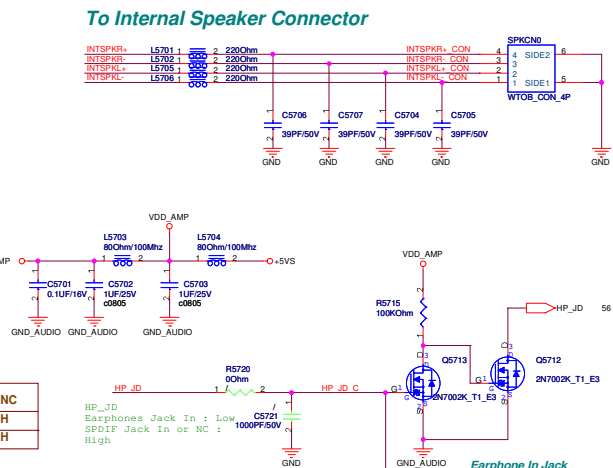
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ASUSTek COMPUTER INC		Engineer: Frank_Xu	
Size	Project Name		Rev
Custom	F7Se		2.0
Date:	2007.11.23	Sheet	55 of 95

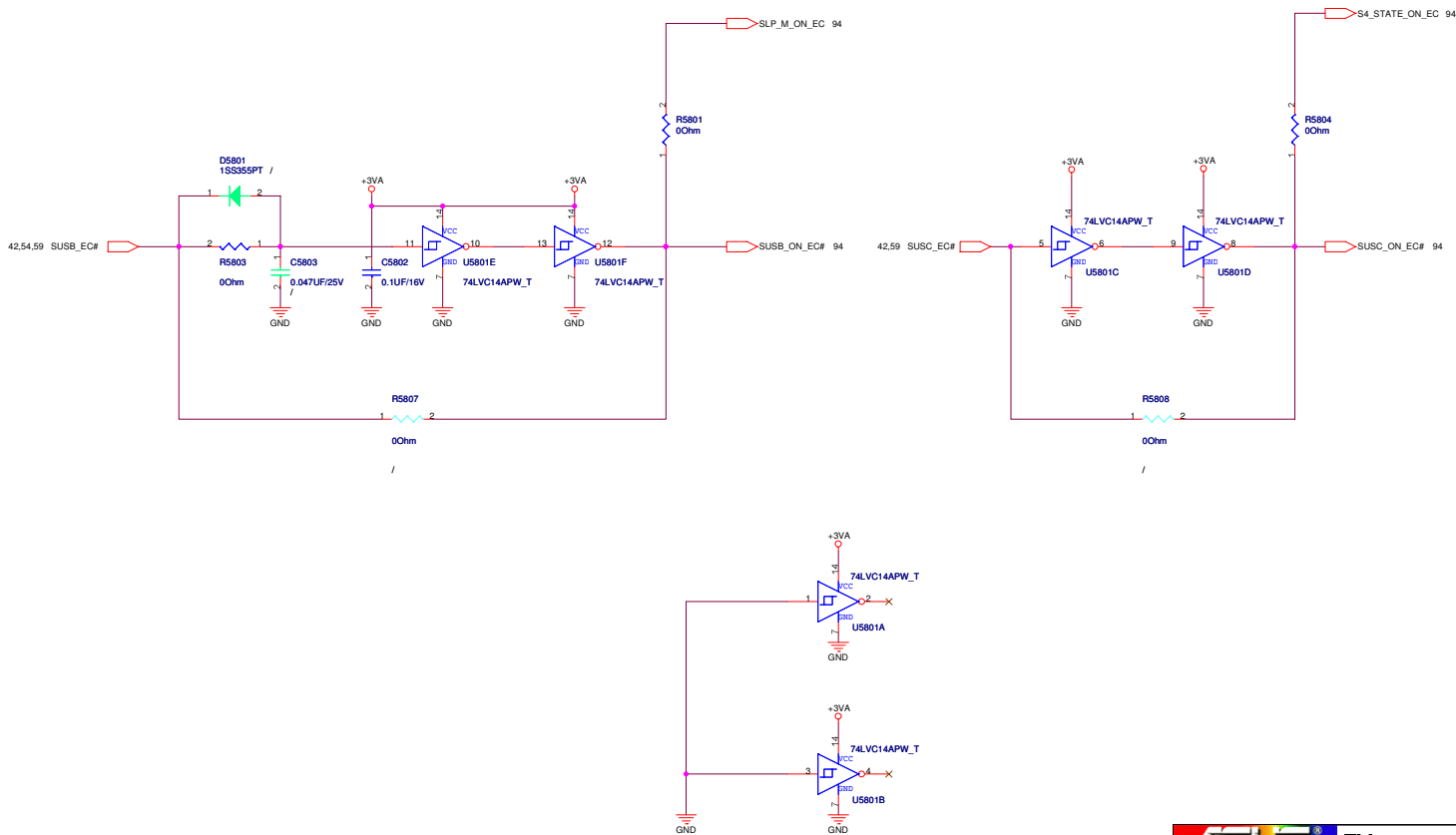


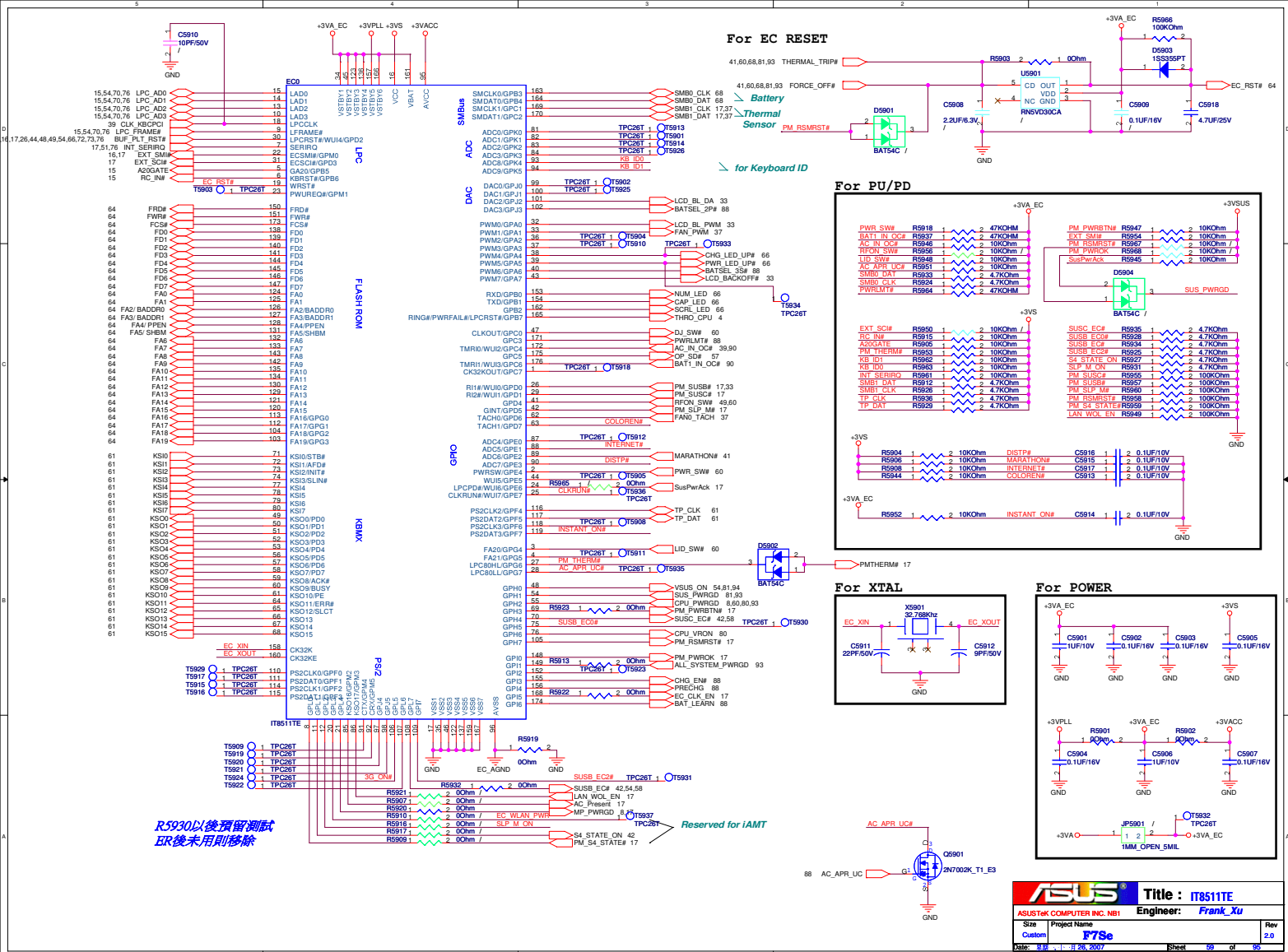
```
1->-6 V/V
0->NORMAL
```



TYPE	LINE_OUT	S/PDIF_OUT	NC
HP_JD	L	H	H
JACK_SW#	L	L	H

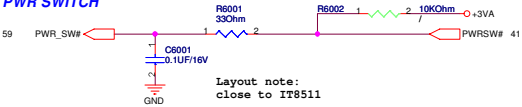




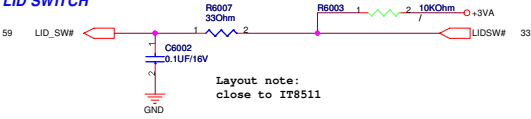


For Switch

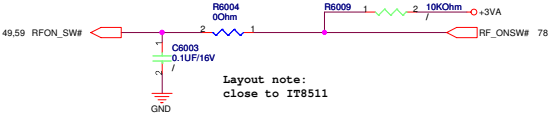
PWR SWITCH



LID SWITCH

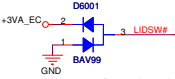


RF ON SWITCH



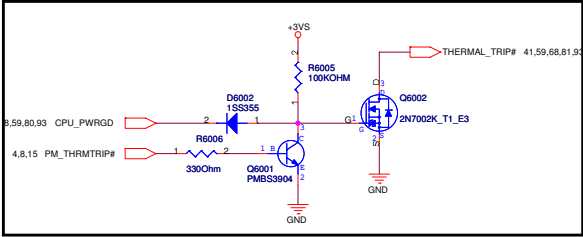
If you don't use Audio DJ function, please use this schematics

Note:
This LID_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.

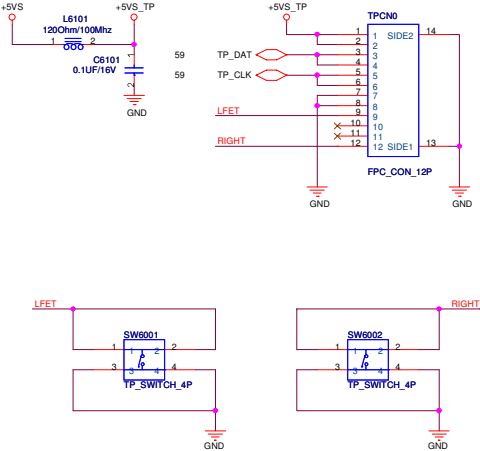


Layout note:
close to connector

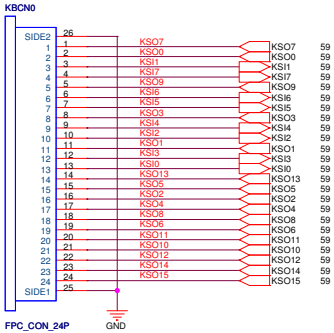
For Thermal Control Method

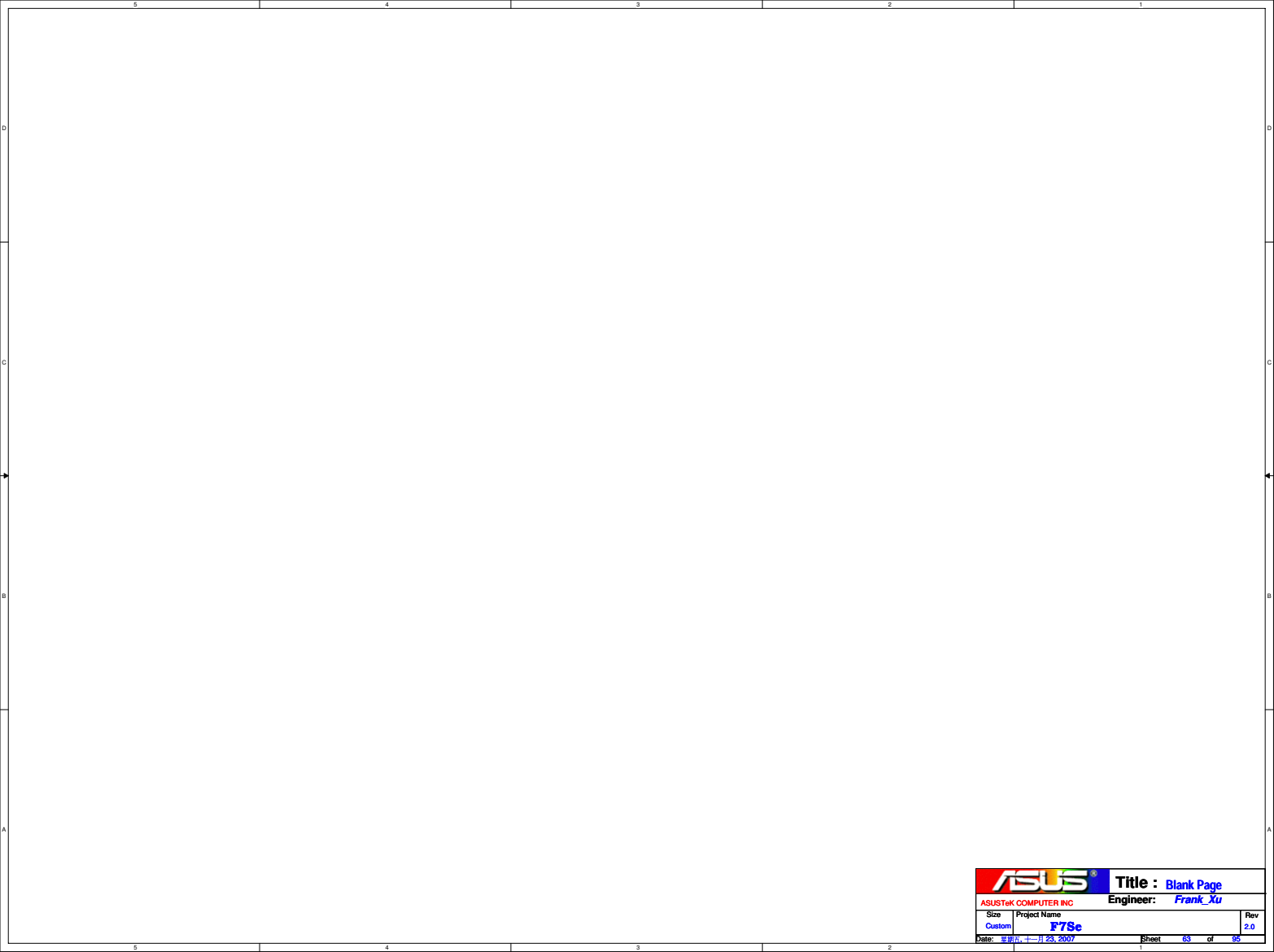


For Touch-Pad



FOR A7 K/B , Matrix B



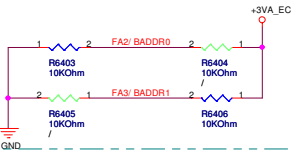


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

- 00: PNPENG Access Register Pair Are 002Eh and 002Fh
10: PNPENG Access Register Pair Are 004Eh and 004Fh
01: PNPENG Access Register Pair Are Determined by
EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

- 0: Normal
1: KBS Interface Pins are Switched to Parallel Port
Interface for In-System Programming

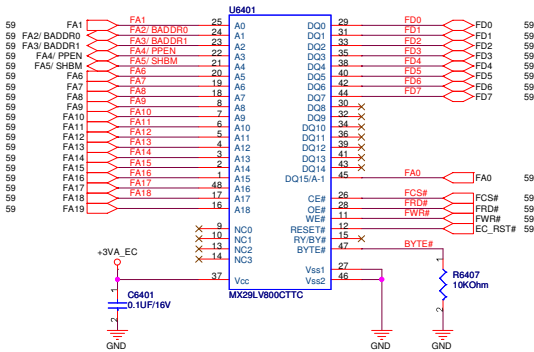


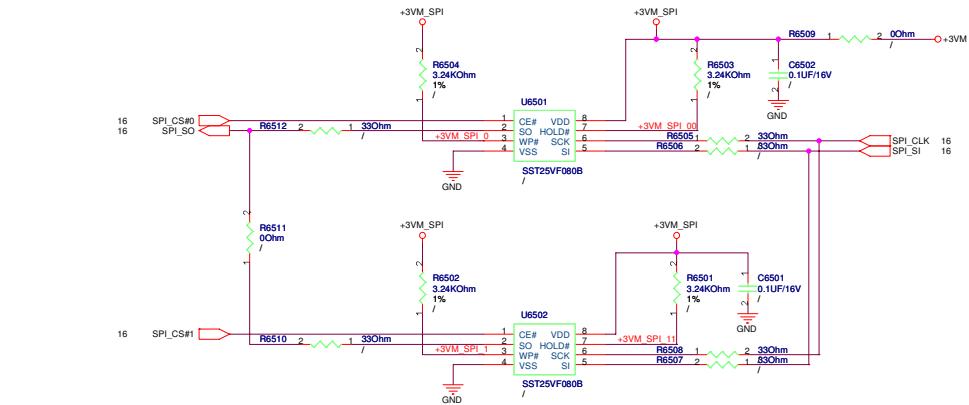
FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

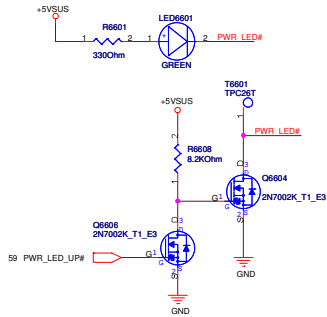


8M TSOP

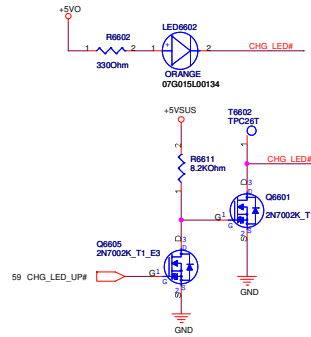




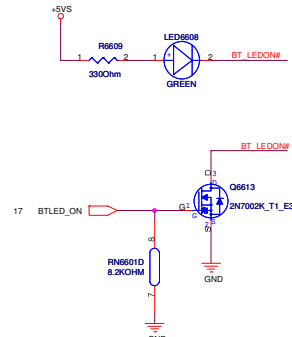
For Power LED



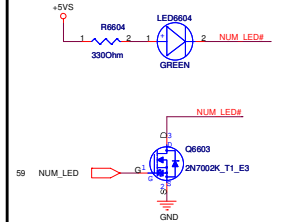
For Battery LED



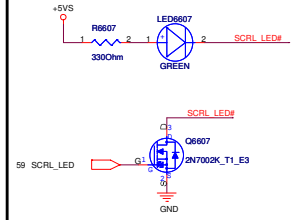
For BT LED



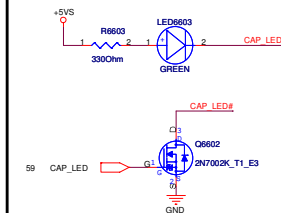
For Number Lock



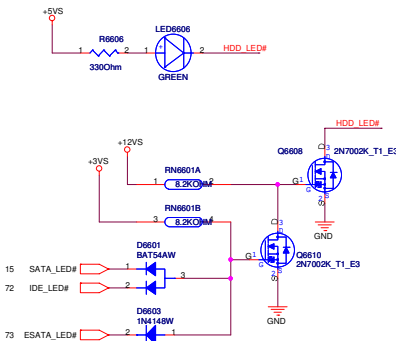
For Scroll Lock



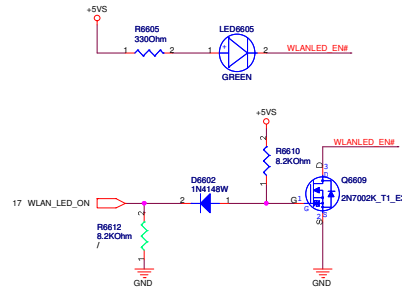
For Caps. Lock



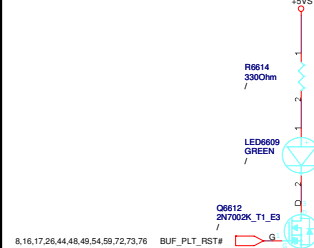
For SATA/IDE LED



For WireLess LED

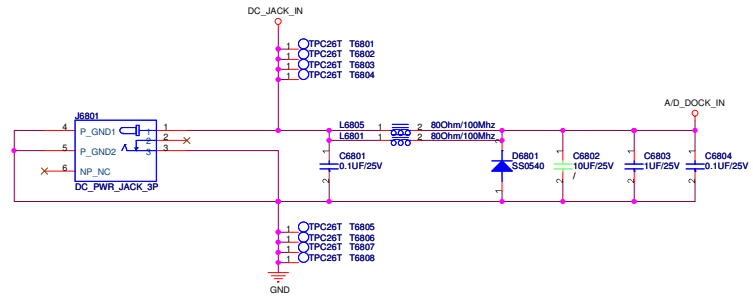


Reserved LED

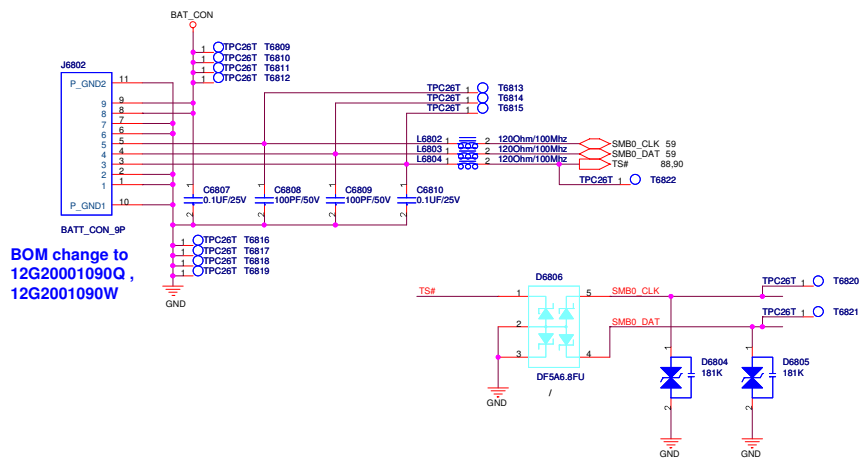


RN6601C
5 8.2KOhm

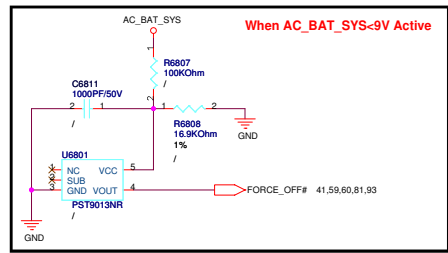
DC IN

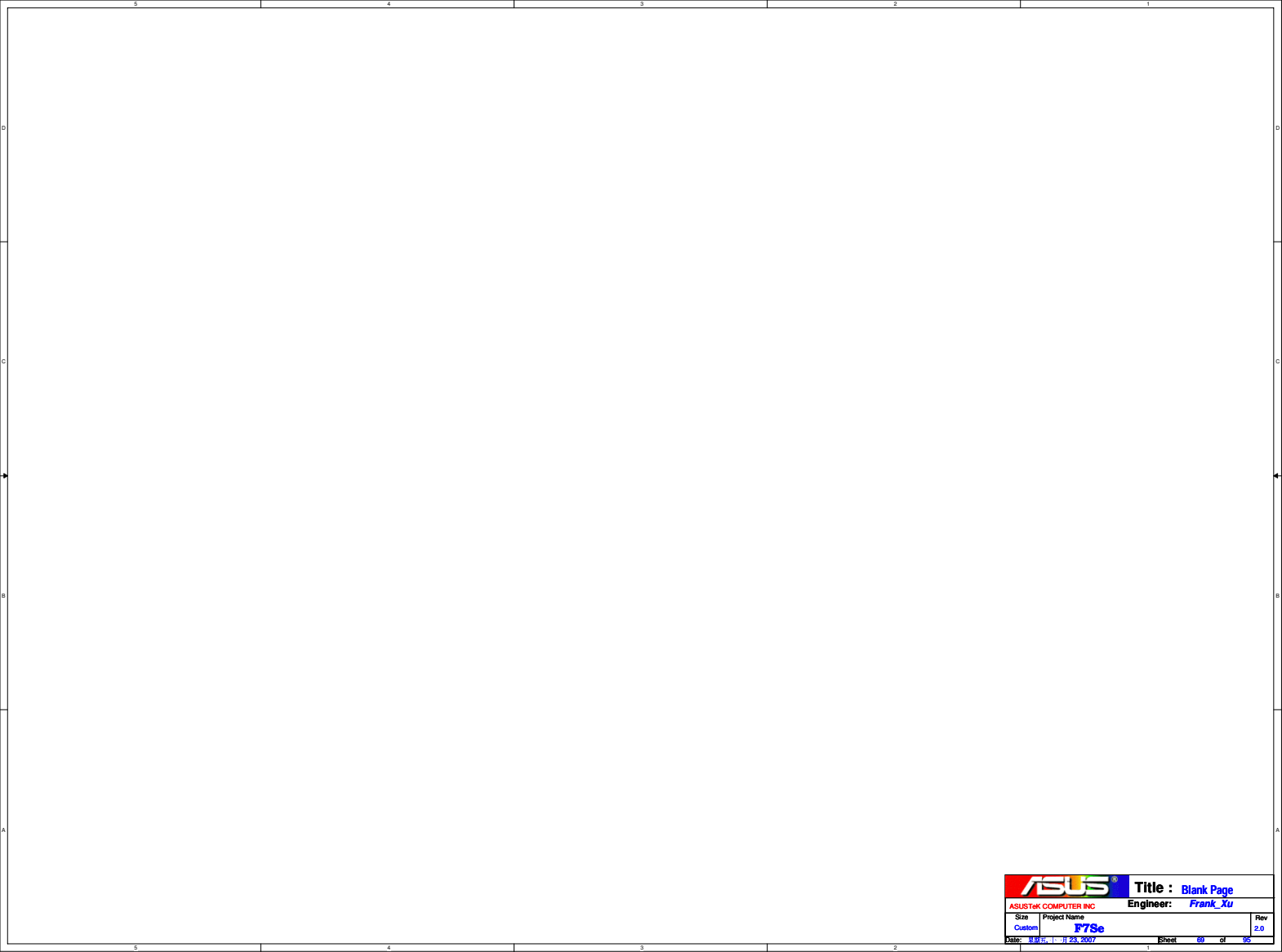


BAT IN



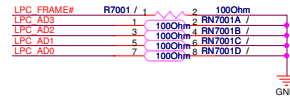
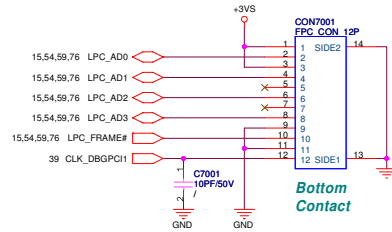
Without Battery & Pull out Adapter

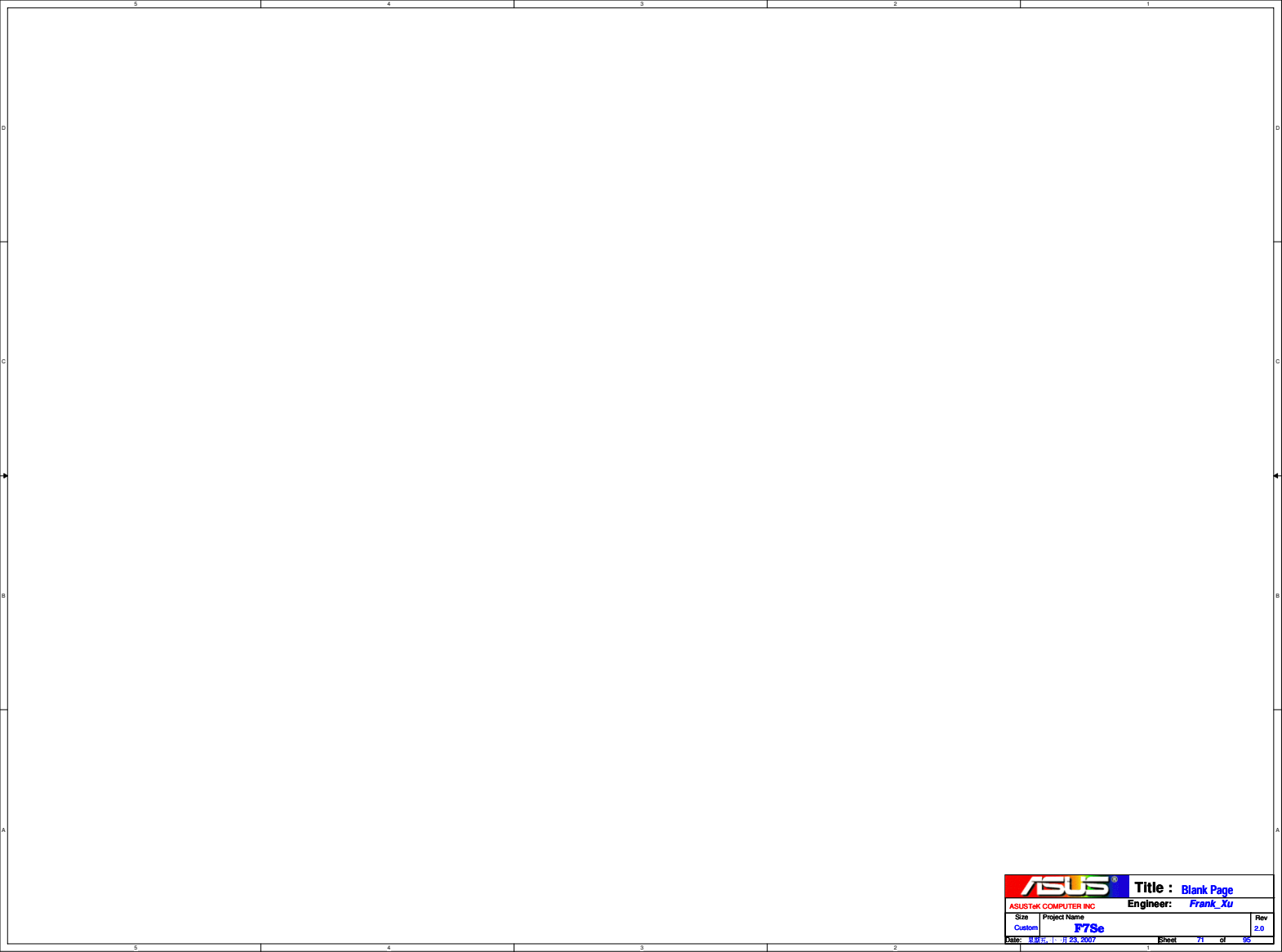




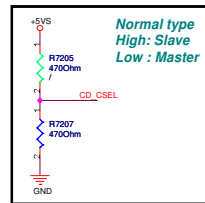
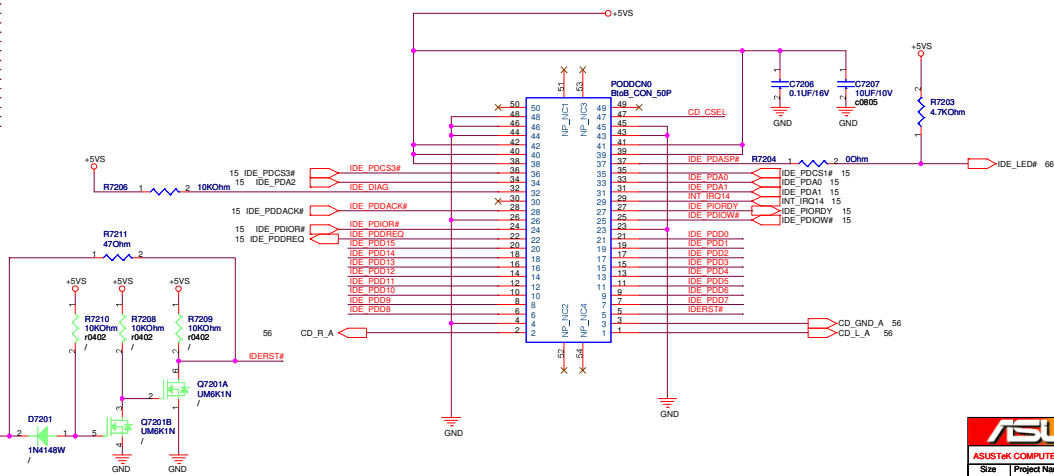
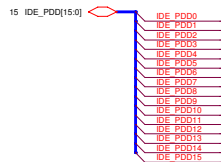
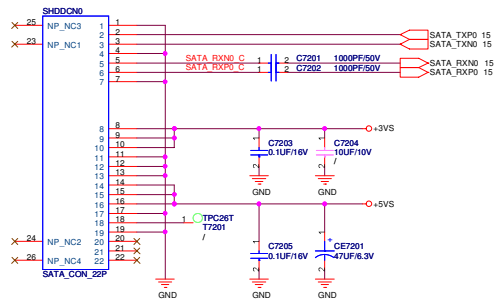
For Debug

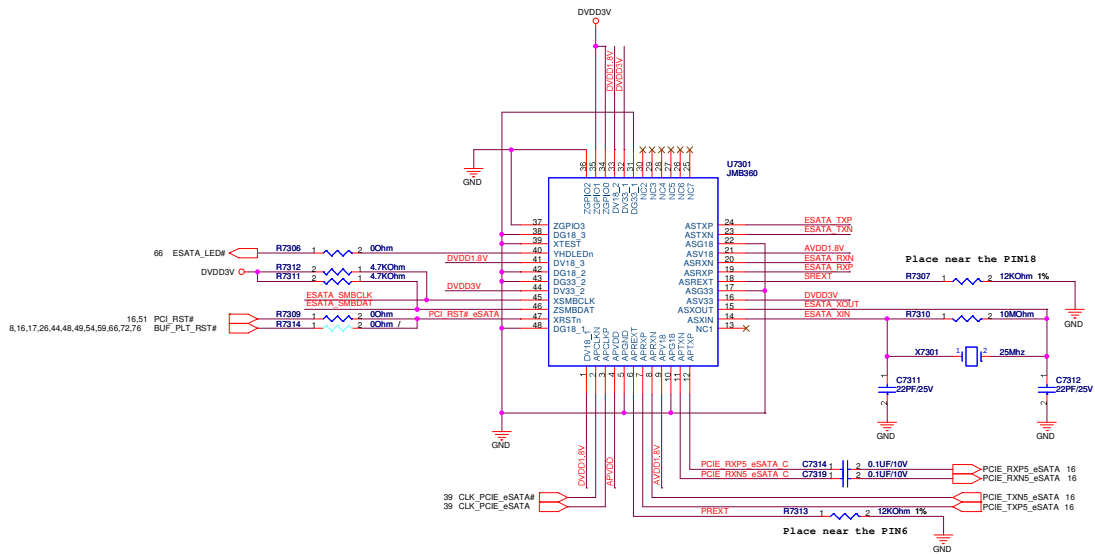
If support NewCard Debug Card,
Pls don't mount all components.



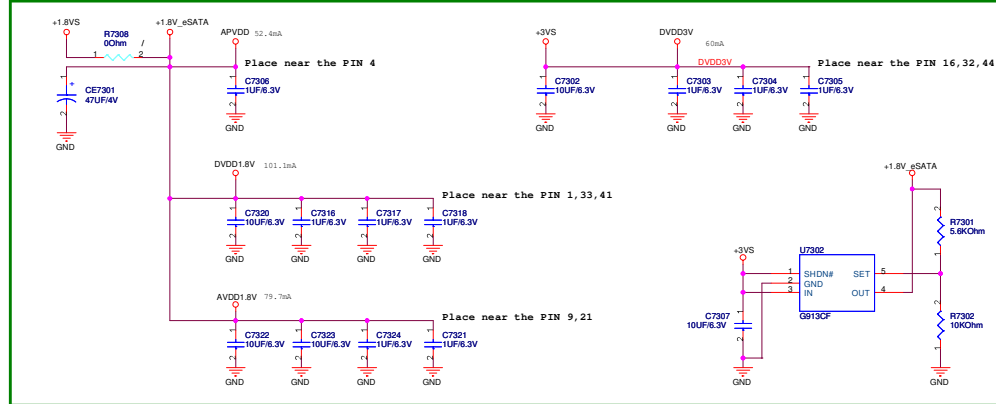


ODD

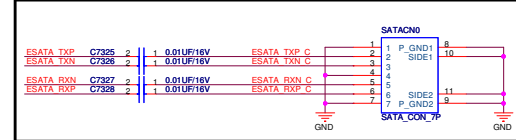


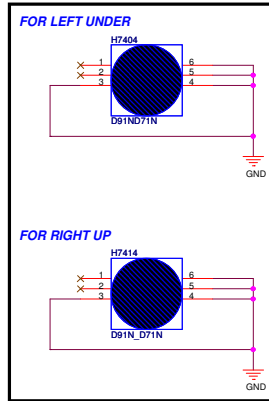


eSATA Power

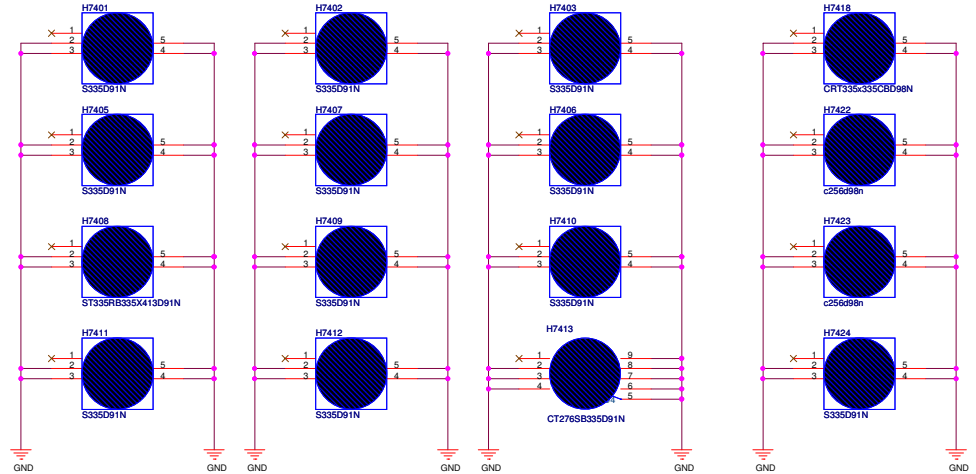


eSATA Connector

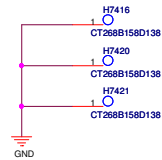




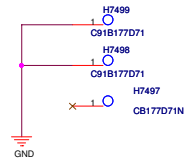
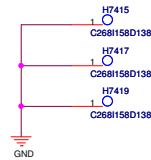
FOR SCREW HOLE

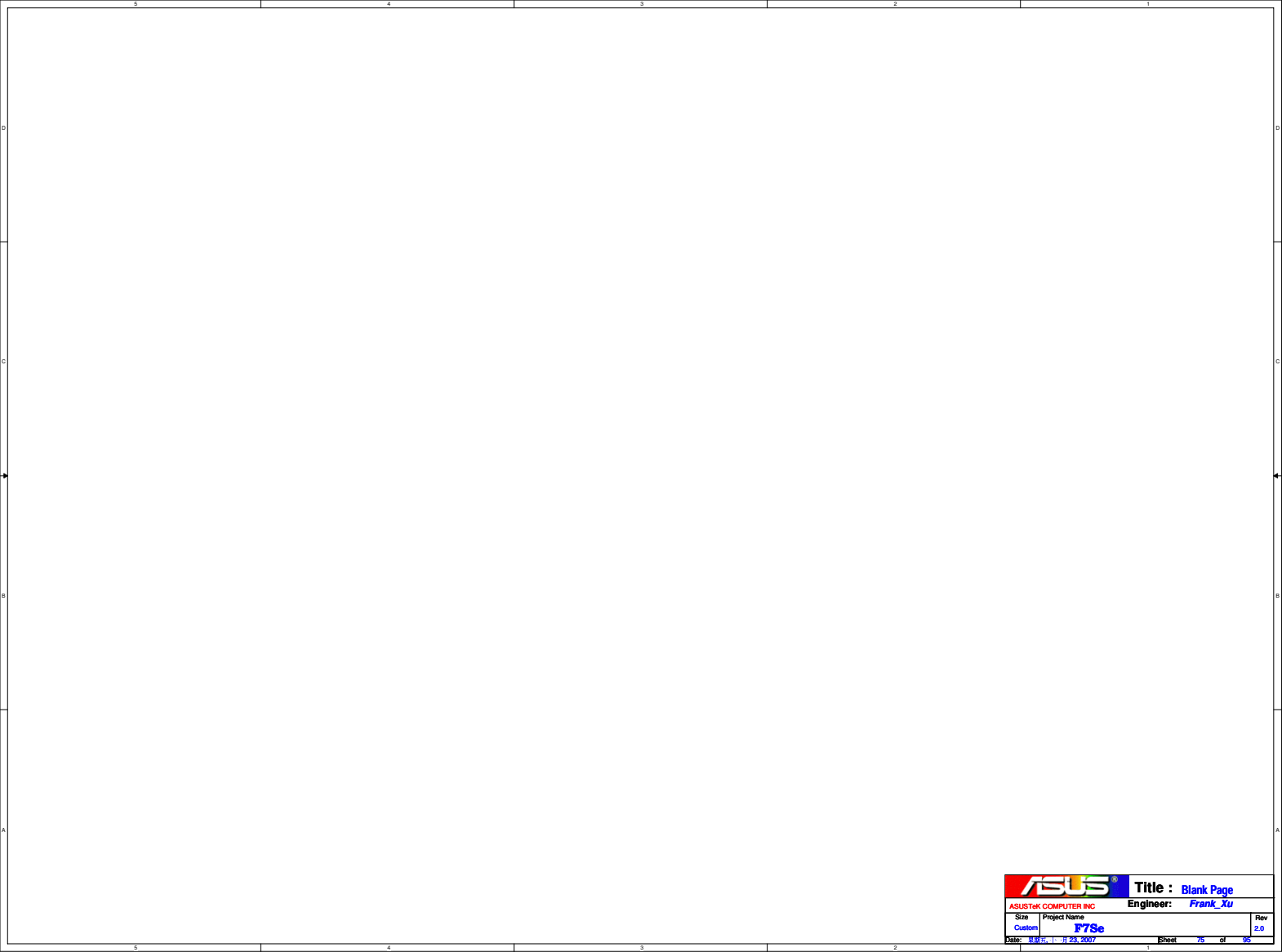


FOR CPU

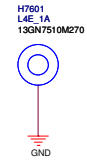
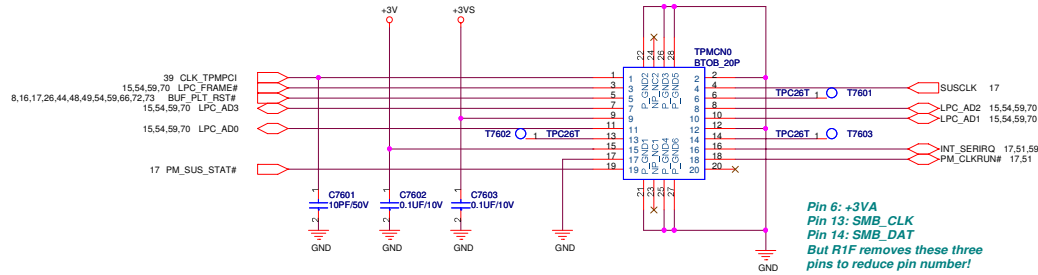


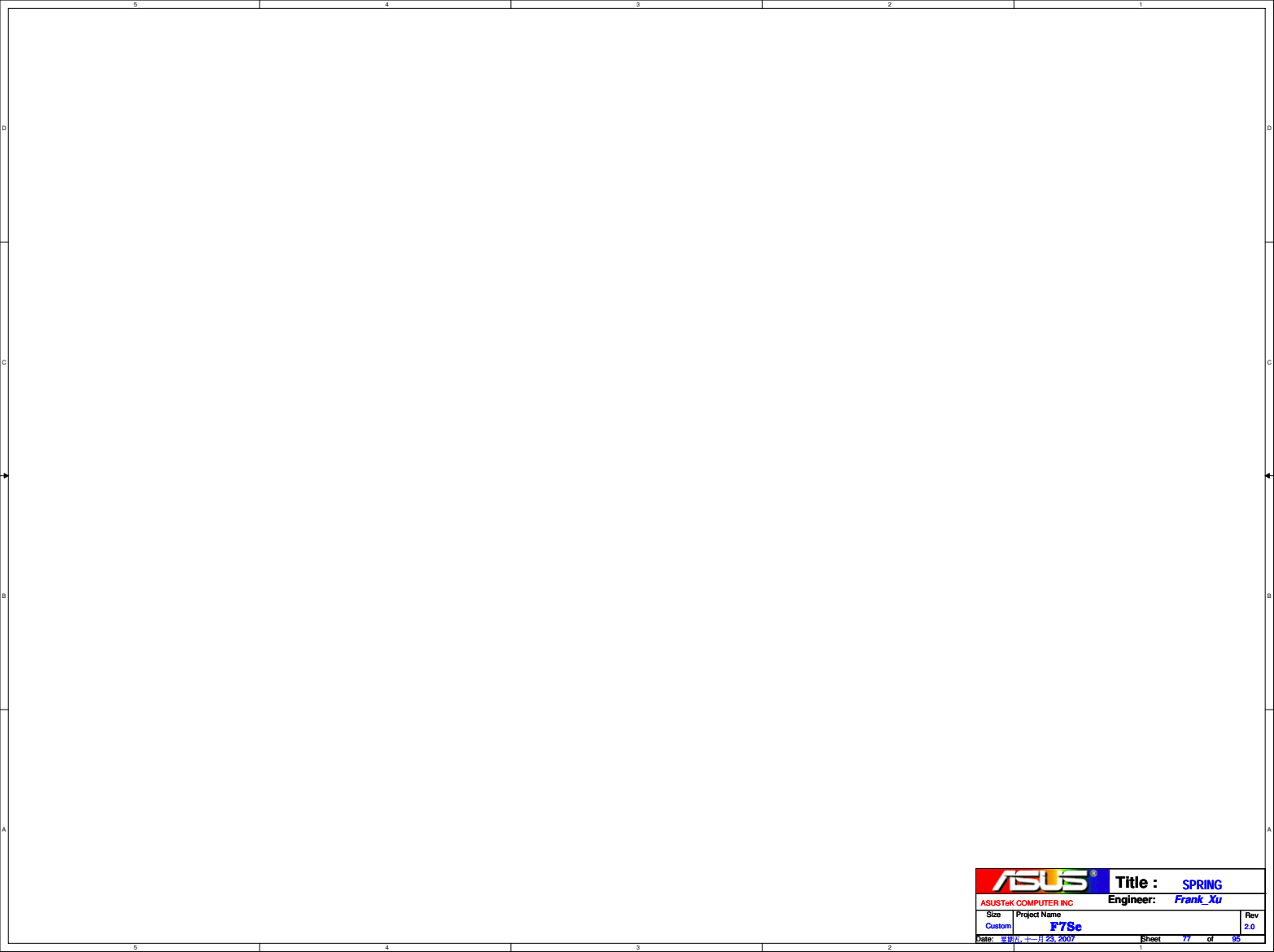
FOR VGA





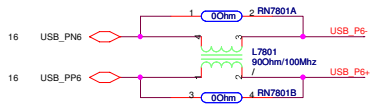
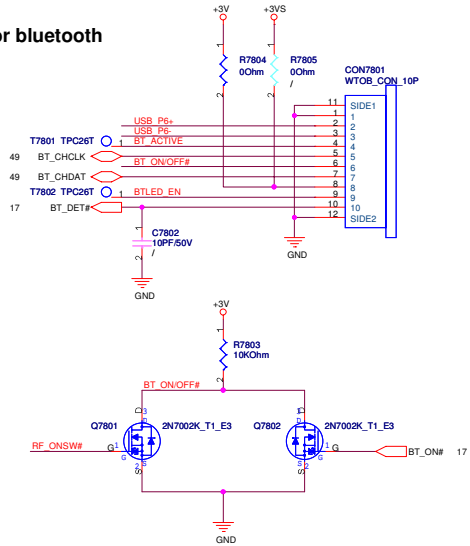
For TPM module



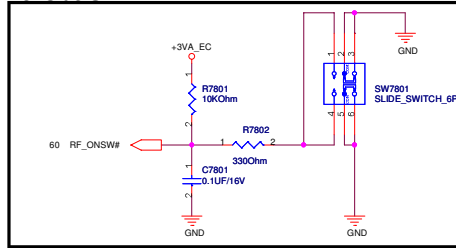


		Title : <i>SPRING</i>	
ASUSTek COMPUTER INC		Engineer: <i>Frank_Xu</i>	
Size	Project Name		Rev
Custom	<i>F78c</i>		2.0
Date: <i>2007-11-23, 2007</i>		Sheet <i>17</i> of <i>50</i>	

For bluetooth

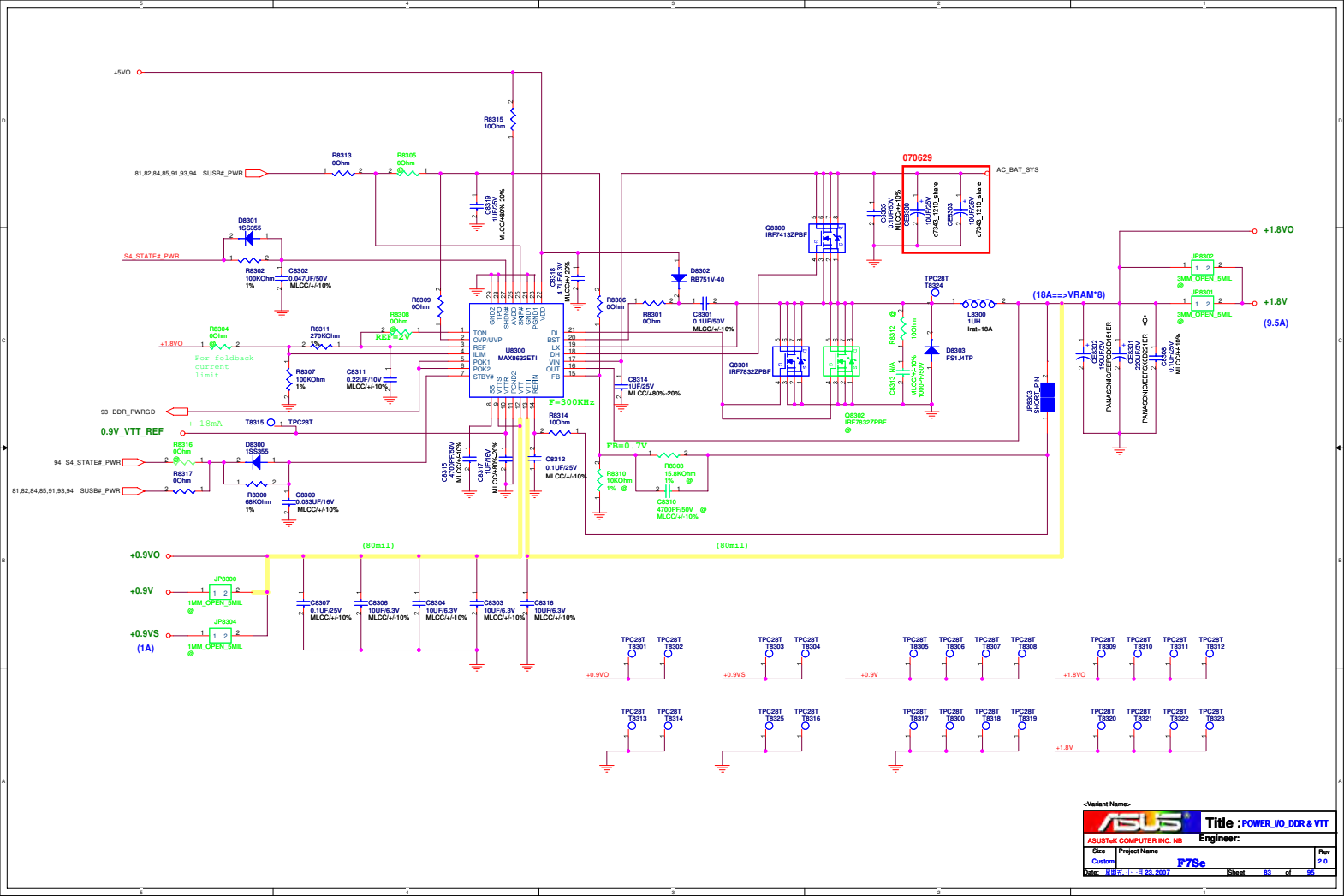


For side SW

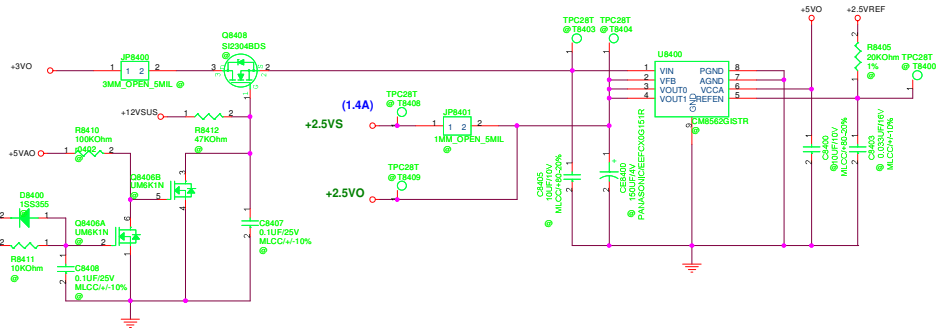




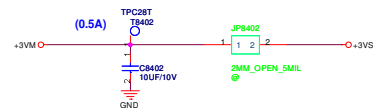




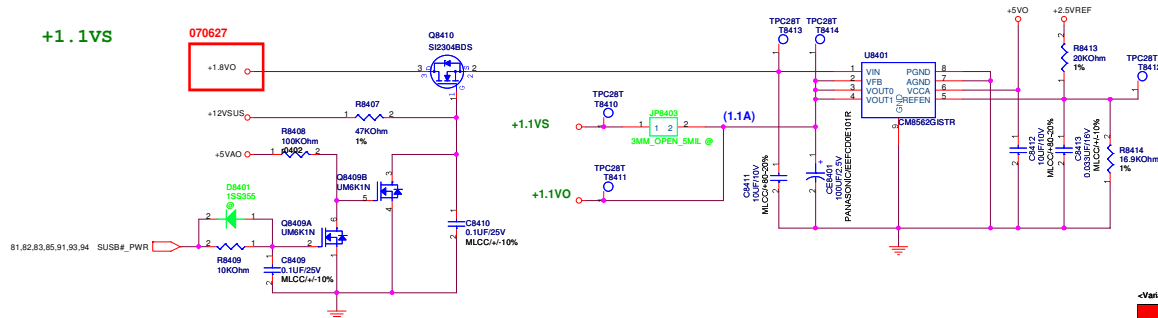
+2.5VS



+3VM

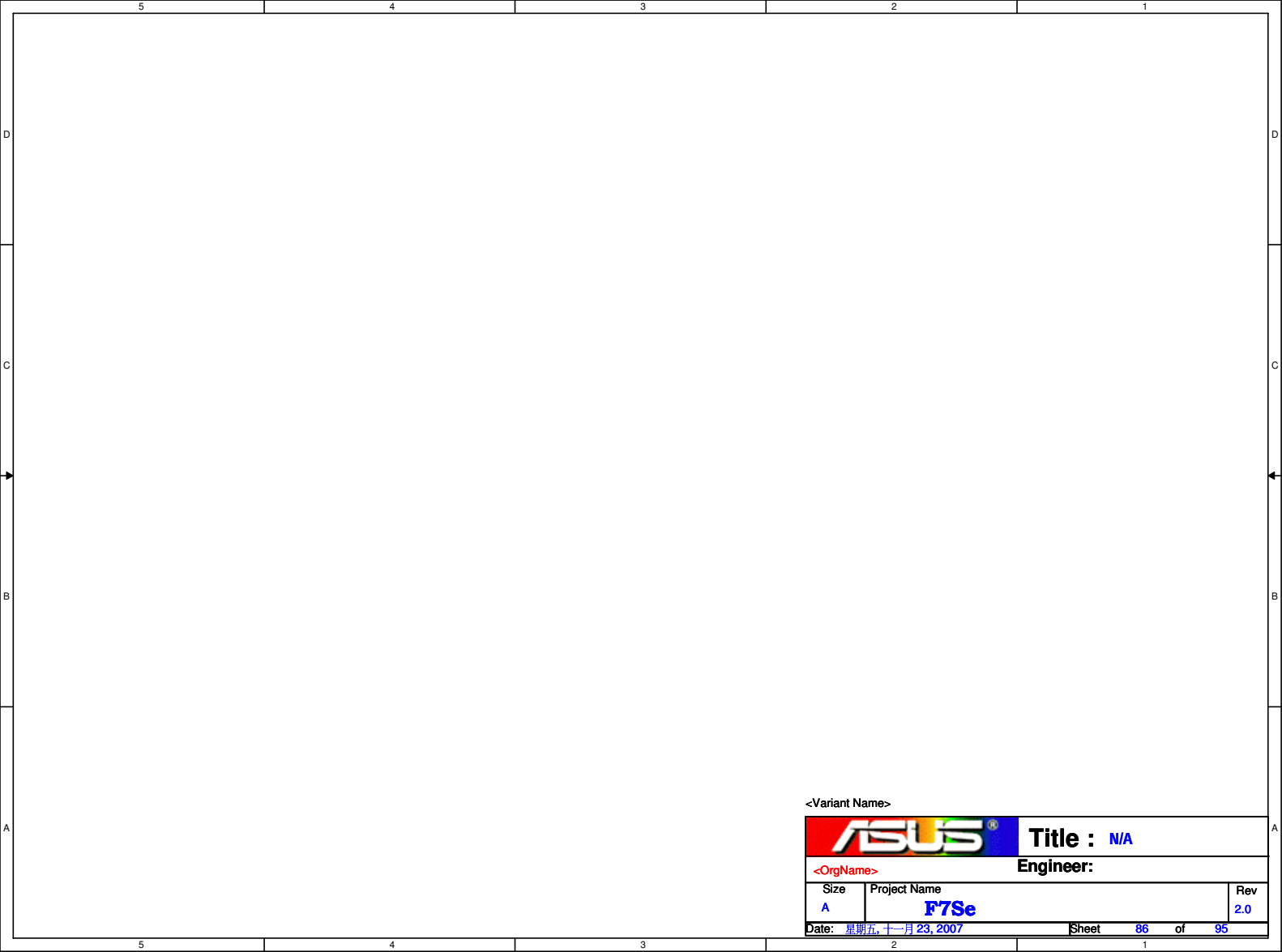


+1.1VS



<Variant Name>

ASUS		Title POWER_0_+3VM & +2.5VS	
<OrigName>		Engineer:	
Size	Project Name	Rev	
Custom	F7Se	2.0	
Date: 2007.11.25		Sheet 84 of 95	

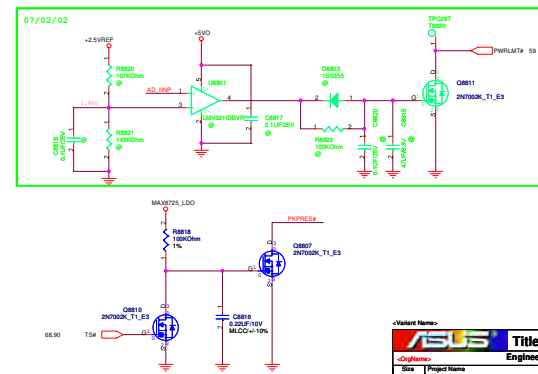
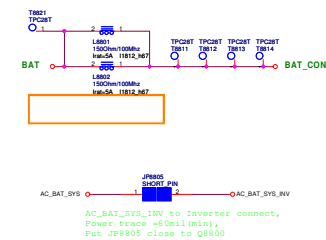
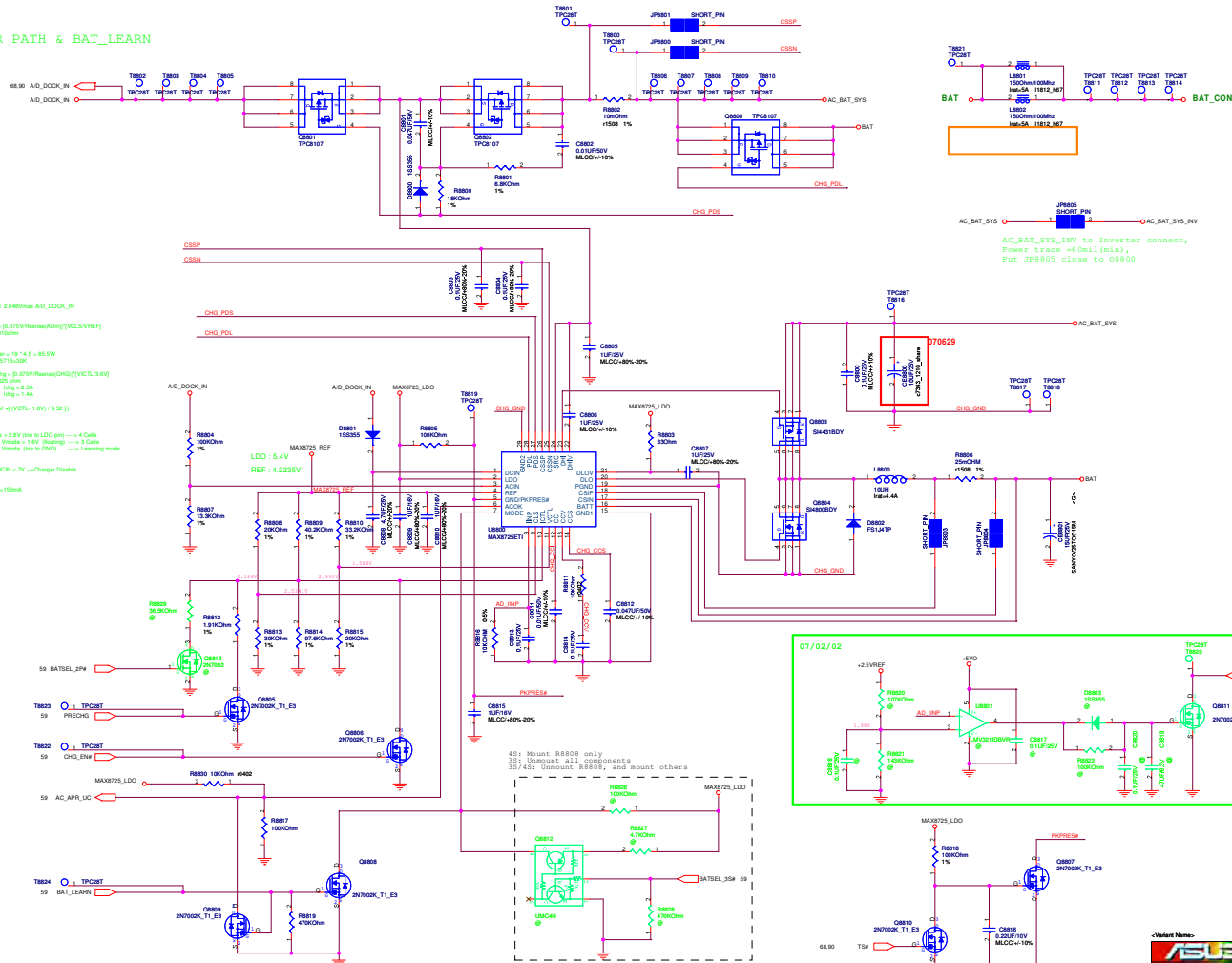


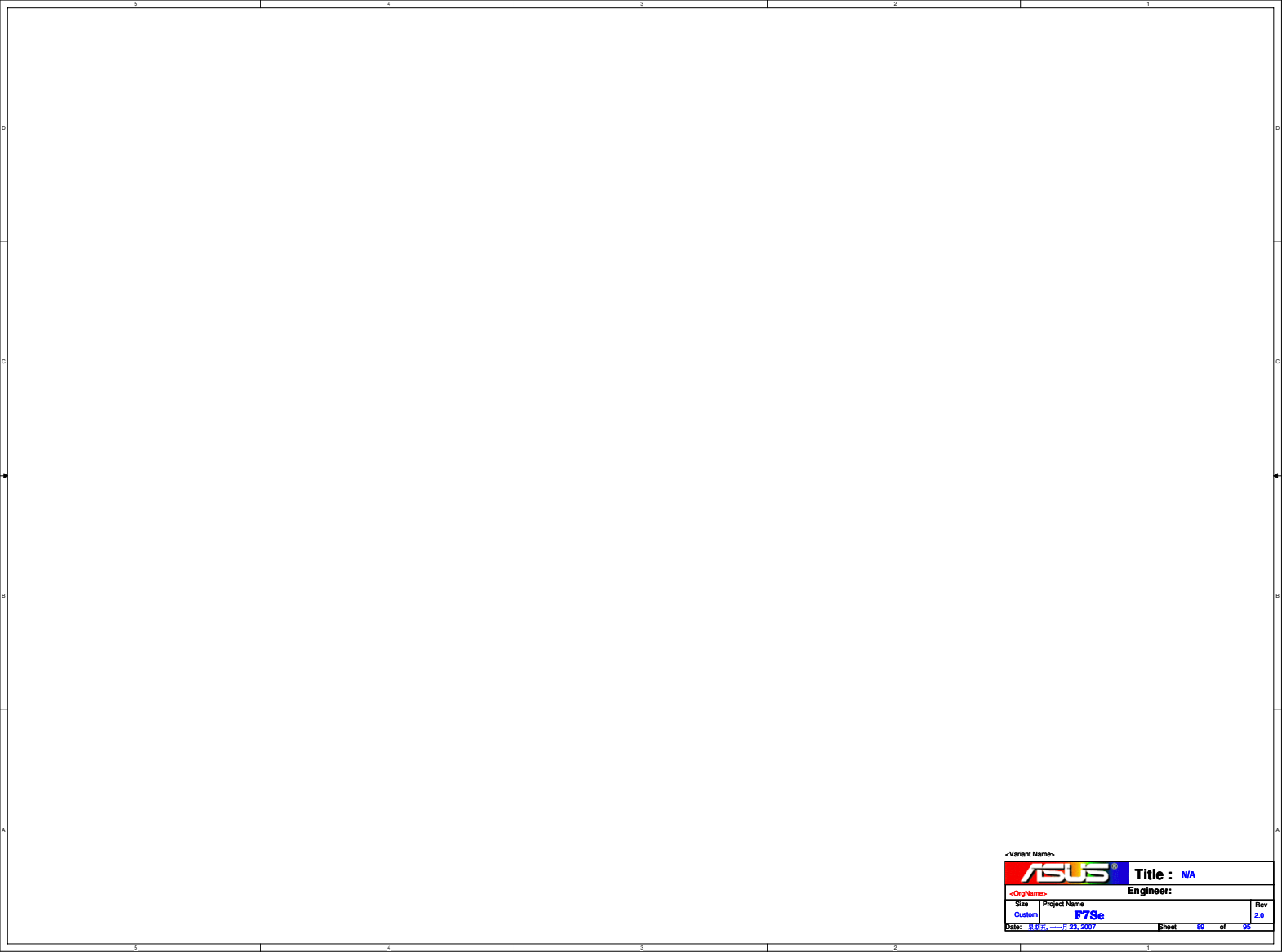
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		Title : N/A	
<OrgName>		Engineer:	
Size	Project Name		Rev
A	F7Se		2.0
Date: 星期五, 十一月 23, 2007		Sheet 86 of 95	

«Variant Name»		Title : N/A	
«Original»		Engineer:	
Size	Project Name	Rev	
C	F78c	2.0	
Date	15.05.2007	Sheet	67 of 65

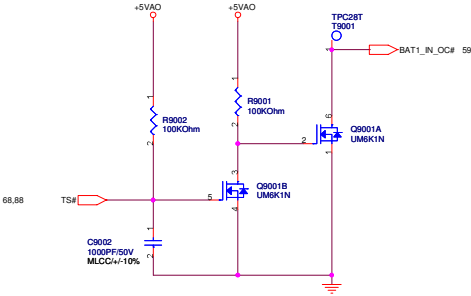
POWER PATH & BAT_LEARN



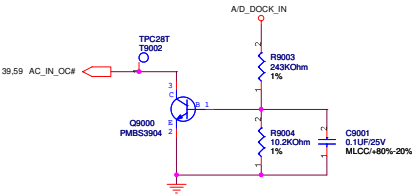


-<Variant Name>		 Title : N/A	
-<OrigName>		Engineer:	
Size	Project Name		Rev
Custom	F7Se		2.0
Date: 2007-11-23, 2007		Sheet	69 of 95

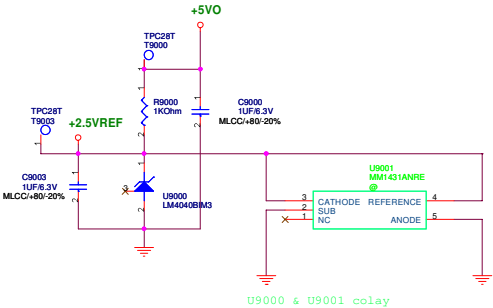
BATTERY IN DETECT



ADAPTER IN DETECT

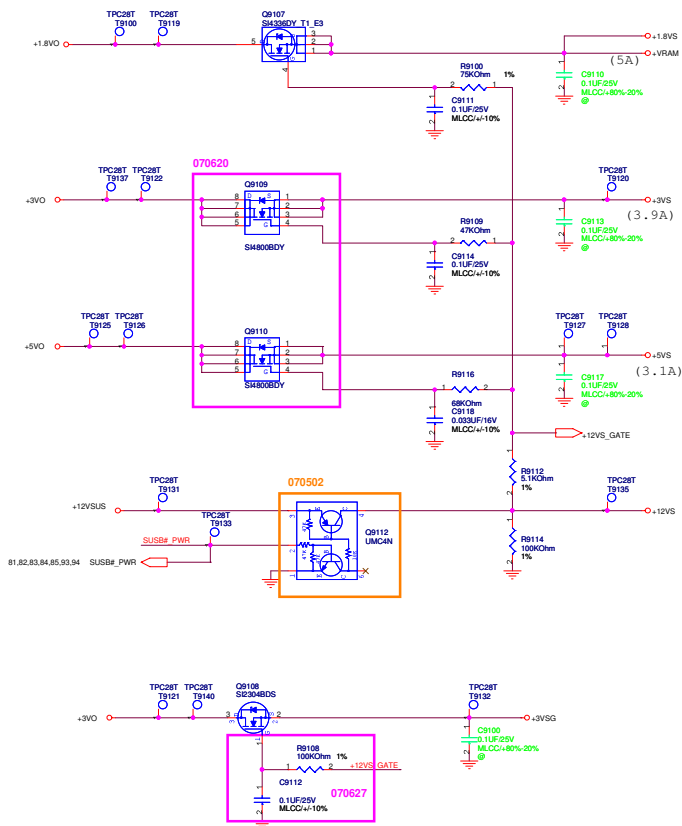


+2.5VREF

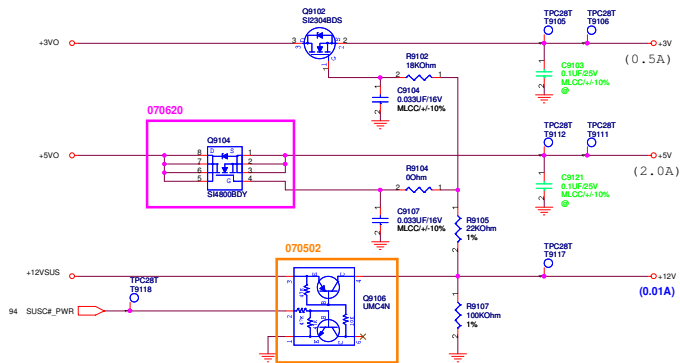


U9000 & U9001 colay

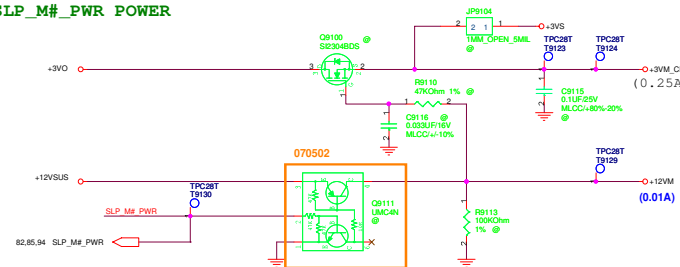
SUSB#_PWR POWER



SUSC#_PWR POWER



SLP_M#_PWR POWER



Variant Name:

ASUS		Title : POWER_LOAD SWITCH	
Design Name		Engineer:	
Size	Project Name		Rev
Custom	F7Se		2.0
Date: 11/23/2007		Sheet 91 of 95	

A/D_DOCK_IN

AC_BAT_SYS

VSUS_ON

MIC5235

+12VSUS
(100mA)

SLP_M#_PWR

UMC4N
(SWITCH)

+12VM

(10mA)

S4_STATE#_PWR

UMC4N
(SWITCH)

+12V

(10mA)

SUSB#_PWR

UMC4N
(SWITCH)

+12VS

(10mA)

VSUS_ON

FORCE_OFF#

TPS51120

+3VO

SUSC_STATE

ND5351AN

+3VSUS (3.9A)

SUSB#_PWR

FDW2501

CM8562

+2.5VO

+3V

(0.08A)

+2.5VS

(1A)

+3VS

(3.9A)

SUSB#_PWR

ND5351AN

+3VAUX_GOLAN

(0.5A)

SC_WLAN_PWR

SLP_M#_PWR

ND5351AN

+3VM

(0.5A)

LAN_WOL_EN

SUSB#_PWR

ND5351AN

+3VSG

(0.1A)

SLP_M#_PWR

ND5351AN

+3VM_CLK

(0.25A)

SUSC_STATE

FDW2501

+5VSUS (0.06A)

SUSB#_PWR

FDW2501

+5V

(2.0A)

+5VS

(3.1A)

+5VAO

+3VAO

-- SUS_FWRGD

+3VA

(0.01A)

+5VO

SUSB#_PWR

ISL6227

+1.5VO

+1.05VO

1.05V-1.5V_PWRGD

SLP_M#_PWR

ND5351AN

+1.5VS

(4A)

+VCCP

(11A)

+1.05VM

(0.54A)

SUSC#_PWR

+1.8VO

SUSB#_PWR

PWR45EN

+1.8V

(5A)

+1.8VS

(0.2A)

+5VO

SUSB#_PWR

TPS51116

+0.9VO

DDR_PWRGD

+0.9V

(1A)

+5VO

SUSB#_PWR

GPU_VID

MAX8743

+VGA_VCORE_O

+1.25VO

PWR_OK_VGA

SLP_M#_PWR

ND5351AN

+VGA_VCORE (19A)

+1.25VS

(4A)

+1.25VM

(0.75A)

+5VS

CPU_VRON

ISL6260C

+VCORE

(44A)

VR_VID0-VR_VID6, R_DPRSTP#,
MCH_OK, PM_DPRSLPVR, PM_PS1#,
VCCSENSE, VSSSENSE, STP_CPU#

* VRM_PWRGD, CLK_EN#

+5VO

LM4040BIM
(Regulator)

+2.5VREF

(10mA)

<Variant Name>

<Chipset>

Size

Custom

Date

Rev

2.0

Project Name

F78c

Sheet

55

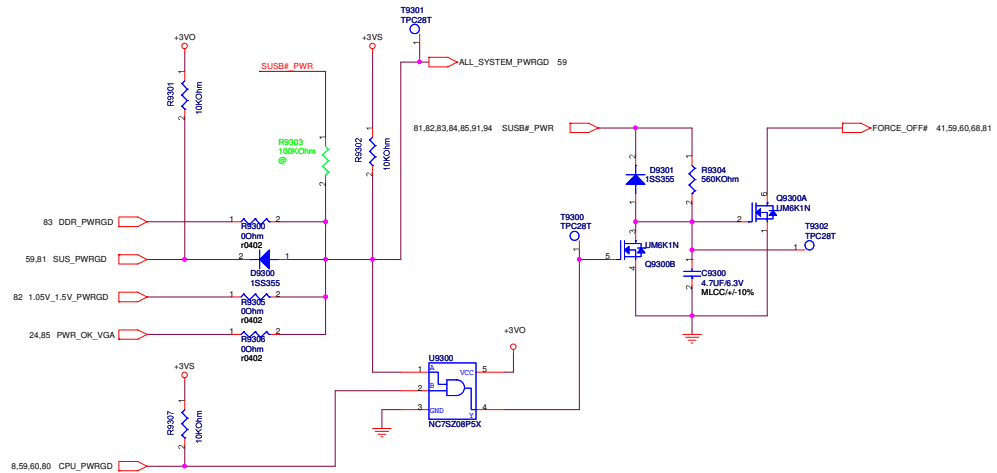
of

55

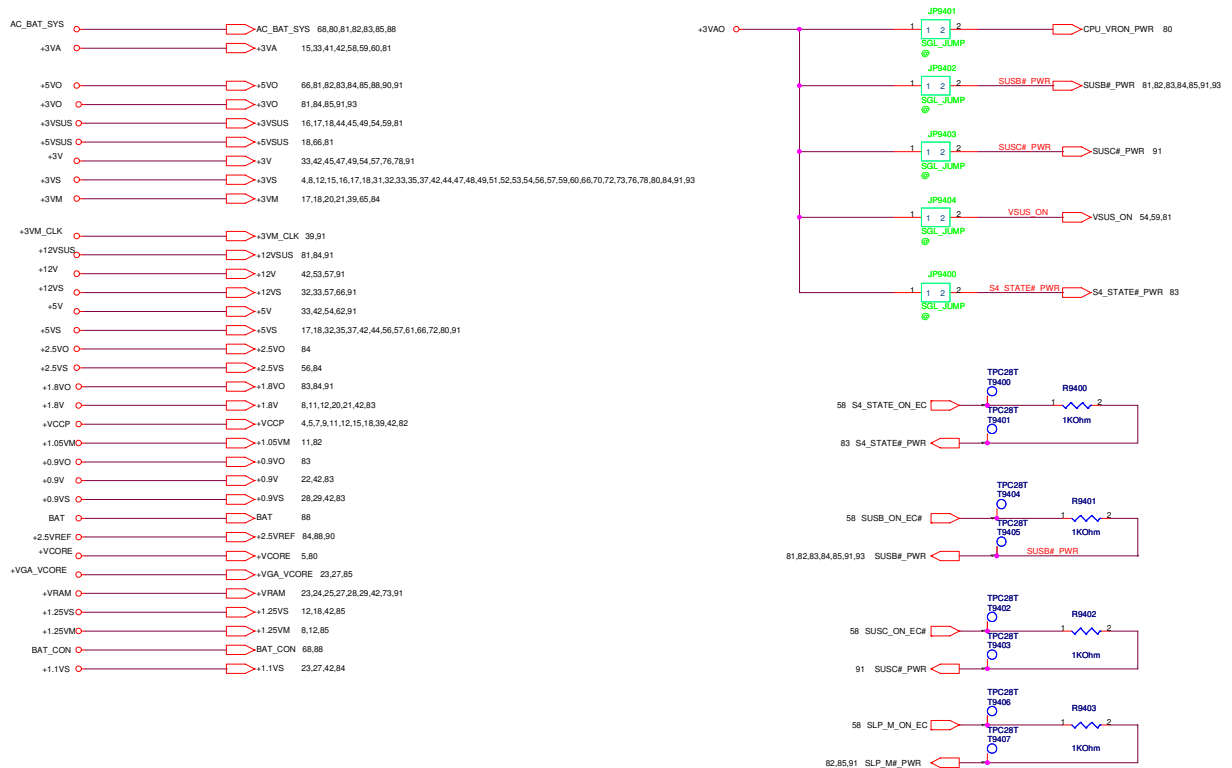
Title : POWER_VCORE

Engineer:

POWER GOOD DETECTOR



FOR POWER TEST



~Variant Name~

ASUS		Title : POWER_SIGNAL	
~OrigName~		Engineer:	
Size	Project Name	Rev	
Custom	P7S	E.0	
Date	2007.03.23	Sheet	94 of 95

Sub system	Reference Circuit	Reason for Change if Any	Page	BOM change		
				Description	Add	Delete
CPU	F7SR.R1.1		4-5			
FAN	F7SR.R1.1	1. Change Q3701, Q3702 to K3753, R3754 for cost down 2. Change RN3701 to R3705 for unnecessary pull-ups 3. Modify FAN circuit for cost down	37	1. Change Q3701, Q3702 to K3753, R3754 2. Change RN3701 to R3705 3. DNI CE3701, D3701, add C3708, R3703, R3704, Q3703	R3753 K3754 R3705 R3704 Q3703 R3703 C3708	Q3701 Q3702 RN3701 CE3701 D3701
NB	F7SR.R1.1		7-13			
SB_	F7SR.R1.1	P15: change C1501, C1503 value for XTAL accuracy P16: exchange USB port 4 & port 6 connection for bluetooth and USB wake-up device issue. P17: change PCB_ID P17: Delete SM-Bus related components which is not used any more P18: change V5REF bypass	15-18	P15: change C1501, C1503 from 12pF to 15pF. P17: change PCB_ID from 001 to 011 P17: delete Q1704, Q1706, R1728, R1729, R1730 P18: change C1004 from 0.1uF to 1uF	C1501 C1503 R1728 R1729 R1730 C1004	C1501 C1503 R1745 R1728 R1729 R1730 C1004
TV_	F7SR.R1.1	Change USB 0 ohm resistor to 2R4P	35	Change R3505-R3512 to RN3501-RN3504	RH3501 RH3502 RH3503 RH3504	RN3505 RN3506 RN3507 RN3508 RN3509 RN3510 RN3511 RN3512
LVDS	F7SR.R1.1	1. Change LVDS connector 2. Change USB 0 ohm resistor to 2R4P	33	1. Change LVDS connector 2. Change R3313, R3314 to RN3301	LCDCN0 RH3301	LCDCN0 R3313 R3314
MEM	F7SR.R1.1		20-22			
CLK	F7SR.R1.1	1. Change C3905, C3906 to 24pF for XTAL accuracy 2. DNI Q3902 for cost down	39	1. Change C3905, C3906 from 22pF to 24pF 2. DNI Q3902	C3905 C3906	C3905 C3906 Q3902
KBC	F7SR.R1.1	1. Add R5957, R5960, D5904 (reserved) to follow ASUS IT8511 EC Common Pin Assignment V2.03 2. Change C5911, C5912 value for XTAL accuracy 3. Rename Q3001 to Q5901 for design rule	59	1. Change C5911, C5912 from 5pF to 15pF 2. Delete Q3001 and add Q5901	C5911 C5912 Q5901	C5911 C5912 Q3001
ROM	F7SR.R1.1		64			
AUD	F7SR.R1.1	1. DNI R5718, R5723, Q5701, Q5709, mount Q5708, Q5707 for POP noise 2. Change L5713 from 330 to 220 ohm for single source issue	56-57	1. DNI R5718, R5723, Q5701, Q5709, mount Q5708, Q5707 2. Change L5713 from 330 to 220 ohm	Q5708 Q5707 L5713	R5718 R5723 Q5701 Q5709
LAN_SIO	F7SR.R1.1	1. Change C4403, C4404 value for XTAL accuracy 2. Change R4504 to 1% for single source issue 3. Change CON4502 P/N for manufacture request	44-45	1. Change C4403, C4404 from 27pF to 22pF 2. Change R4504 from 5% to 1% 3. Change CON4502 P/N to 12G142121120	C4403 C4404 R4504 CON4502	C4403 C4404 R4504 CON4502
HUB	F7SR.R1.1					
CB_	F7SR.R1.1	Page 52: Change C5205, C5207 for XTAL accuracy Page 64: DNI all debug card related components	64 64	Page 52: Change C5205, C5207 from 30pF to 27pF Page 64: DNI RS406, C5401, RS408, RS403, C5402, RS407, RS409, RS404, Q5401, U5402, RS414, RS405, U5403, C5403	C5205 C5207 RS406 C5401 RS408 D5403 C5402 RS407 RS403 RS409 Q5401 U5402 RS414 RS405 U5403 C5403	
XDD	F7SR.R1.1		72			

USB	1. Change USB 0 ohm resistors to 2R4P 2. Change polyswitch for droop fail 3. Change CE6205 to 3528 type for cost down.	62	1. Change R6211, R6214, R6212, R6213, R6201, R6202, R6205, R6207, R6215, R6218 to RN6201-RN6205 2. Change F6201-F6203 to 1012 type (3A3V1) 3. Change CE6205 to 3528 type.	RN6201 RN6202 RN6203 RN6204 RN6205 F6201 F6202 F6203 CE6205	R6211 R6212 R6213 R6201 R6202 R6205 R6207 R6215 R6218 F6201 F6202 F6203 CE6205
SW		41			
DSG					
TP		61			
LED	Change LED6602 P/N for light issue	66	Change LED6602 P/N	LED6602	LED6602
OTH	Page 48: DNI R4817, R4818 for cost down Page 49: mount R4931 for WLAN wake-up function Page 74: change H7499, H7498 to PTH	48 49 74	Page 48: DNI R4817, R4818 Page 49: mount R4931	R4931	R4817 R4818
PB					
CRT	Modify CRT DDC pull-up values for ATI suggestion (M72 Revision A13 Errata)	32	Change RN3201 to R3217, R3218, R3219, R3220	R3217 R3218 R3219 R3220	RN3201
DC_	1. Remove I 6806, I 6807, C6805, C6806 for mechanical issue and cost down 2. Change J6802 P/N for manufacture request 3. Add D6806 (reserved) to follow ASUS IT8511 EC Common Pin Assignment V2.03 4. DNI U6801 related components for cost down	68	1. Delete L6806, L6807, C6805, C6806 2. Change J6802 P/N 3. DNI R6807, C6811, R6808, U6801	J6802	I 6806 L6807 C6805 C6806 J6802 R6807 C6811 R6808 U6801
BT_	Change USB 0 ohm resistor to 2R4P	78	Change R7804, R7805 to RN7801	RN7801	R7804 R7805
TPM		76			
FP_					
TUN	Change USB 0 ohm resistor to 2R4P	47	Change R4729, R4720 to RN4701	RN4701	R4729 R4720
ME					
ESA		73			
VGA	P23: add C2306, C2304, C2309 back for ATI suggestion P23: change L2302 from 400mA to 600mA rating for ATI suggestion P23: add C2321 back for CRT NIR fail P24: change memory ID to 0000 for 32M*16 500MHz VRAM P24: add R2469 for VGA BBEN option	23-24	P23: add C2306, C2304, C2309 P23: change L2302 from 400mA to 600mA P23: add C2321 P24: DNI R2408, mount R2415	C2306 C2304 C2309 L2302 C2321 R2415	L2302 R2408 R2803
VGA	DNI PCIE_CALI pull-down resistor for ATI suggestion	25-26	DNI R2603		R2603
VGA	P27: mount 5 capacitors for +VRAM power P27: add two 1uF capacitors for +VGA_VCORE power P27: add 10uF on LPVDD power for ATI suggestion P27: connect +3VSG and +3VSG_DELAY with 0 ohm, DNI +3VSG_DELAY related components	27-30	1. Mount C2715, C2721, C2723, C2742, C2753 2. Add C2740, C2746 3. Add C2718 4. Add R2709, DNI Q2705, D2701, R2705, R2710, Q2704, C2772	C2715 C2721 C2723 C2304 C2309 L2302 C2321 R2415	Q2705 D2701 R2705 R2710 Q2704 C2718 C2772

ECN : 730 - Remove RS914 to solve system can not power on

ECN : 82 - Add U5403, C5403, RS404 back to solve new card didn't work

ECN : 109 - change main source of CPU and VGA core power.

1. H-side s48326 change to IRF7413
2. L-side s48336 change to IRF7832
3. Change R8518 form 49.9K to 62K

<-Variant Name>

ASUS		Title : History	
ASUSTeK COMPUTER INC		Engineer: Frank_Xu	
Size	Project Name		Rev
Custom	F7Se		2.0
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