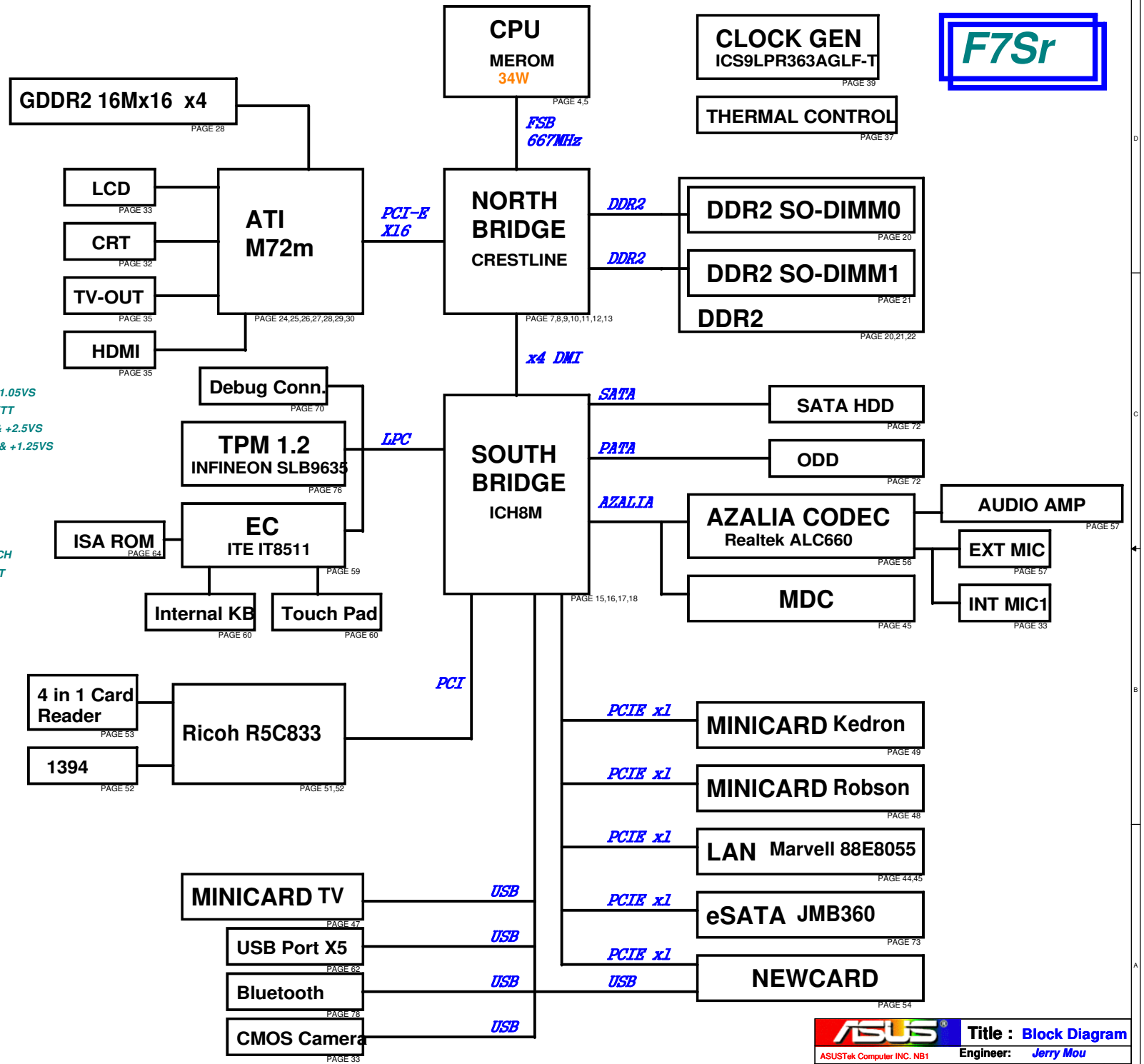


ASUSTek Computer INC. NB1	Title : Block Diagram	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 1 of 95	

EC_IT8511TE SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	PM_SLP_M#	
110	PS2CLK0/GPF0	WALN_SW#	
111	PS2DAT0/GPF1	ME_ALERT#	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	FA19	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80HL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
8	GPL0	PM_S4_STATE#	I
11	GPL1	S4_STATE_ON	O
12	GPL2	SLP_M_ON	O
20	GPL3	EC_WLAN_PWR	O
21	GPL4	MP_PWRGD	I
48	GPH0	VSUS_ON	I
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYSTEM_PWRGD	I

Pin	Pin Name	Signal Name	Type
152	GPI2	/	
155	GPI3	CHG_EN#	O
168	GPI5	EC_CLK_EN	O
85	KS016/GPM2	NETDETECT	O

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	GPIO0/BM_BUSY#	PM_BMBUSY#	I
AJ8	GPIO1/TACH1	EXTSMI#	I
F8	GPIO2/PIRQE#	PCI_INTE#	I
G11	GPIO3/PIRQF#	PCI_INTF#	I
F12	GPIO4/PIRQG#	PCI_INTG#	I
B3	GPIO5/PIRQH#	PCI_INTH#	I
AJ9	GPIO6/TACH2	BIOS_REC	I/O
AH9	GPIO7/TACH3	WLAN_LED_EN	I
AE16	GPIO8	BT_ON#	I
AG19	GPIO9/WOL_EN	LAN_WOL_EN	I
AJ24	GPIO10/CLGPIO1	ME_ALERT#	O
AG22	GPIO11/SMBALERT#	SMB_ALERT#	I
AC19	GPIO12	KBC_SCI#	I
AH21	GPIO13/GLAN_DOCK#		
AF22	GPIO14/CLGPIO2	NETDETECT	
AE20	GPIO15/STP_PCI#	STP_PCI#	I/O
AJ14	GPIO16/DPRSLPVR	PM_DPRSLPVR	O
AG8	GPIO17/TACH0	WLAN_ON#	O
AH12	GPIO18	TP_LEDON	O
AJ10	GPIO19/SATA1GP	PCB_ID0	I
AE11	GPIO20	BTLED_ON	O
AJ12	GPIO21/SATA0GP	CPU_Select	I
AG10	GPIO22/SCLOCK	3G_ON#	I
E6	GPIO23/LDRQ1#	LPC_DRQ#1	I/O
AJ27	GPIO24/CLGPIO0		
AG18	GPIO25/STP_CPU#	STP_CPU#	
AH27	GPIO26/S4_STATE#	PM_S4_STATE#	
AH25	GPIO27/QRT_STATE0	BT_DET#	I
AD16	GPIO28/QRT_STATE1	CB_SD#	
AG17	GPIO29/OC#5	USB_CON_OC5#	I
AD12	GPIO30/OC#6	NEWCARD_OC#	I
AJ18	GPIO31/OC#7	USB_OC#7	I
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	O
AE10	GPIO33/AZ_DOCK_EN#		O
AG14	GPIO34/AZ_DOCK_RST#		
AG13	GPIO35/SATACLKREQ#	GPO35	O
AF11	GPIO36/SATA2GP	PCB_ID1	
AG11	GPIO37/SATA3GP	PCB_ID2	I/O
AF9	GPIO38/SLOAD	GPI38	I
AJ11	GPIO39/SDATAOUT0	GPI39	I
AD10	GPIO48/SDATAOUT1	PCI_GNT#4	O
AG29	GPIO49/CPUPWRGD	H_PWRGD	O

Pin	Pin Name	Signal Name	Type
AG16	GPIO40/OC#1	USB_CON_OC01#	I
AG15	GPIO41/OC#2	USB_CON_OC23#	I
AE15	GPIO42/OC#3	USB_CON_OC23#	I
E18	GPIO50/REQ1#	PCI_REQ#1	
C18	GPIO51/GNT1#	PCI_GNT#1	
B19	GPIO52/REQ2#	PCI_REQ#2	
F18	GPIO53/GNT2#	PCI_GNT#2	
A11	GPIO54/REQ3#	PCI_REQ#3	
C10	GPIO55/GNT3#	PCI_GNT#3	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

PCIE Device	Bus	PCIE Device	Bus
LAN	PE(T/R)(p/n)1	Robson	PE(T/R)(p/n)4
Kedron	PE(T/R)(p/n)2	NEWCARD	PE(T/R)(p/n)5
eSATA	PE(T/R)(p/n)3	GLAN	PE(T/R)(p/n)6

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(MAX6657)	0100110x (4C)
VGA Thermal Sensor(MAX6657)	0100110x (4C)

ICS9LPR363AGLF-T SETTING

Pins	Pin Name	Device
3	PCICLK1	TPMPCI
4	PCICLK2	CardBus R5C832
5	SELPCIEX0_LCD#PCICLK3	EC IT8511E
8	ITP_EN/PCICLK_F0	ICH8
15	DOTC_96MHzL	X
14	DOTT_96MHzL	X
12	FSLA/USB_48MHz	ICH8
19	PCIeT_L1	eSATA
20	PCIeC_L1	eSATA
36	PCIeT_L5	M66M
35	PCIeC_L5	M66M
39	PCIeT_L6	MiniCard(Rob)
38	PCIeC_L6	MiniCard(Rob)
22	PCIeT_L2	ICH8
23	PCIeC_L2	ICH8
24	PCIeT_L3	MCH
25	PCIeC_L3	MCH
26	SATACLKT_L	ICH8
27	SATACLKC_L	ICH8
44	CPUITPT_L2 / PCIeT_L8	LAN
43	CPUITPC_L2 / PCIeC_L8	LAN
14	27FIX/LCD_SSCGT/PCIeT_L0	M72M
15	DOTC_96MHzL	M72M
41	PEREQ1# / PCIeT_L7	MiniCard
40	PEREQ2# / PCIeC_L7	MiniCard
32	PEREQ3#	NewCard
33	PEREQ4#	MiniCard
30	PCIeT_L4	NewCard
31	PCIeC_L4	NewCard
49	CPUT_L1F	MCH
48	CPUC_L1F	MCH
52	CPUT_L0	CPU
51	CPUC_L0	CPU
57	X2	14.318MHz
58	X1	14.318MHz
60	REF0	ICH8
61	REF1/FSLC/TEST_SEL	X

ASUSTek Computer INC. NB1

Title : GPIO setting

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 2 of 95

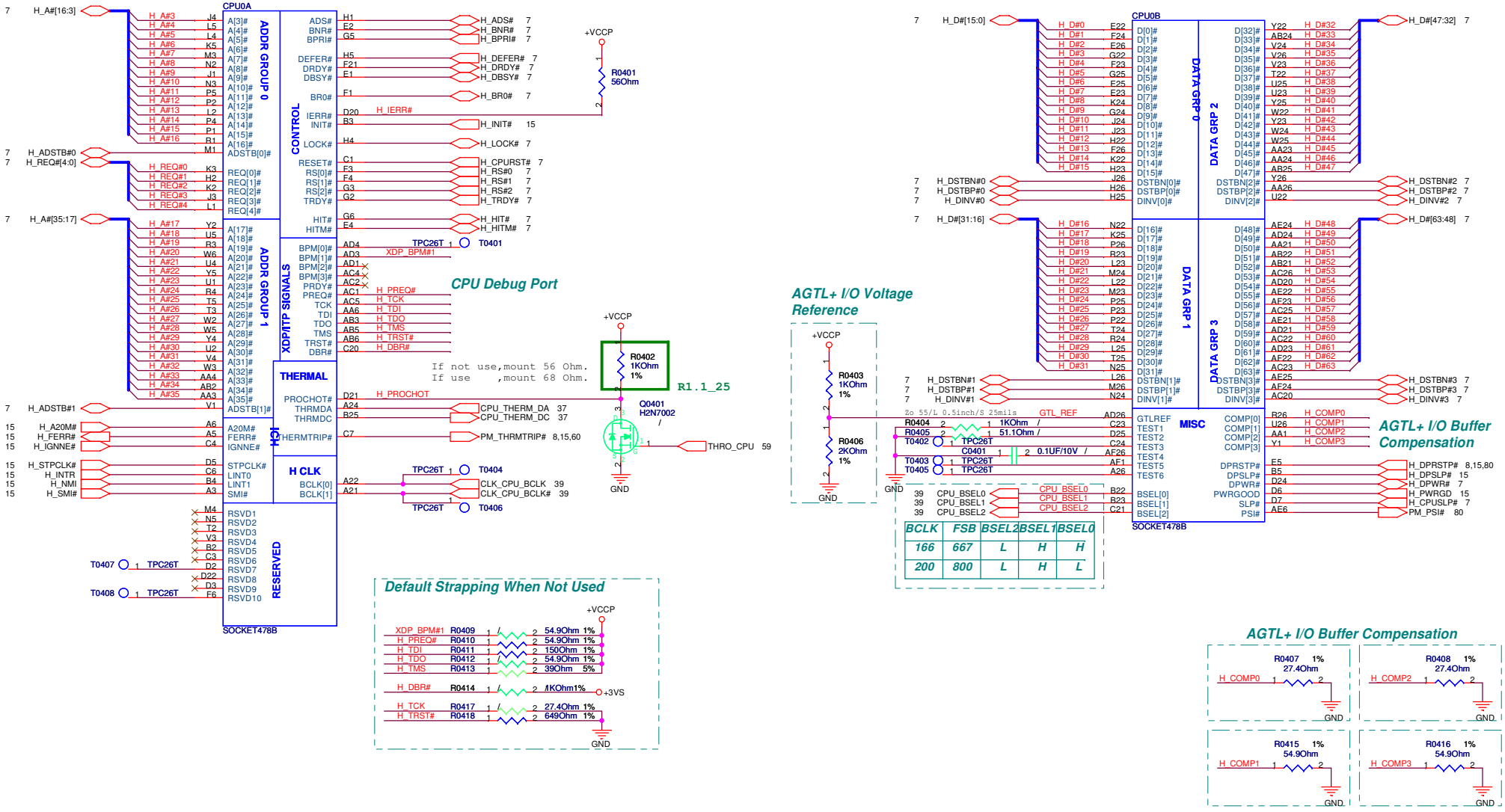
Title : Blank Page

ASUSTeK COMPUTER INC

Engineer: Jerry Mou

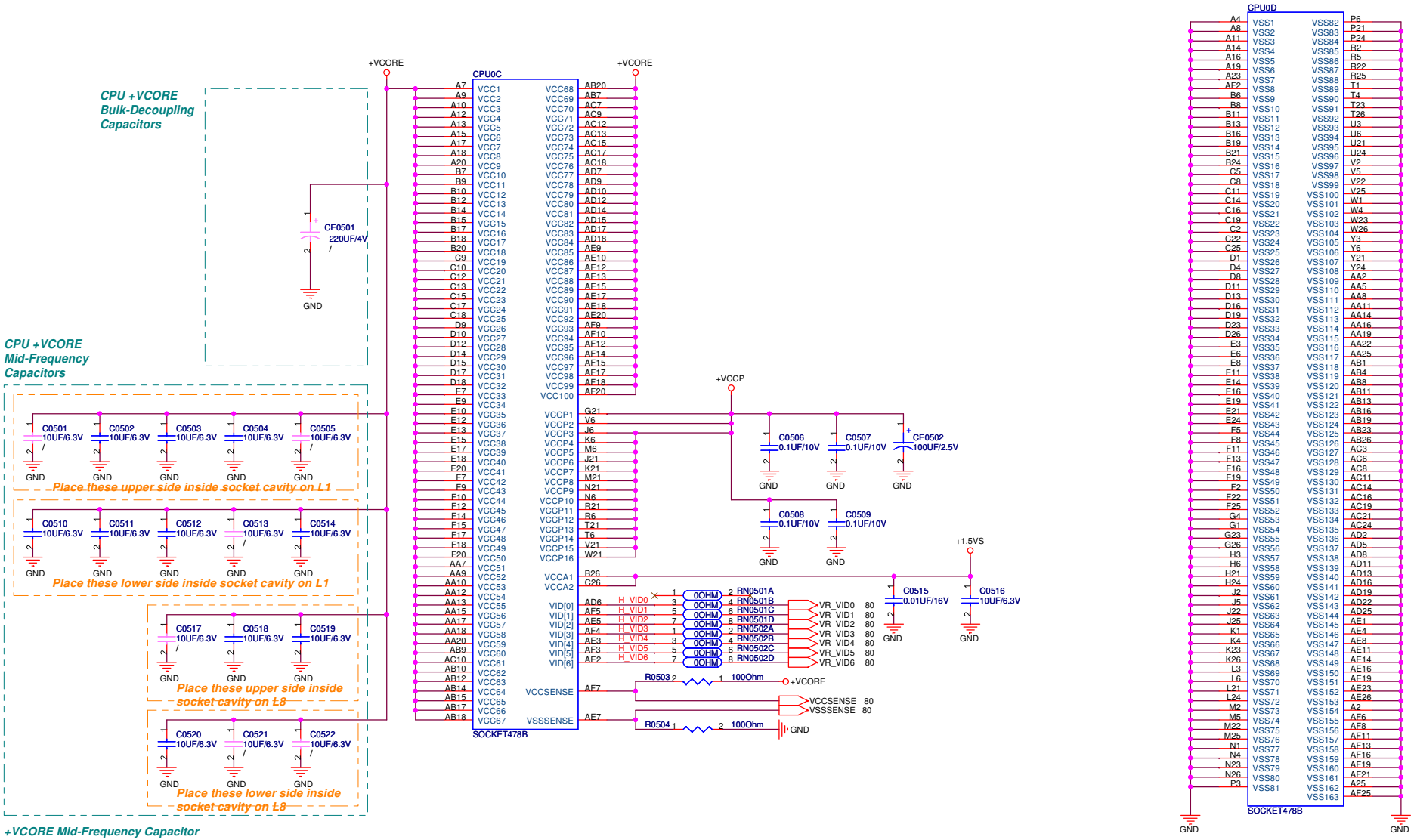
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 3 of 95



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L

ASUSTeK COMPUTER INC. NB1	Title : CPU-Merom(HOST)		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 4 of 95		



ASUSTeK COMPUTER INC. NB1	Title : CPU_Merom(PWR)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 5 of 95	

Title : Blank Page

ASUSTeK COMPUTER INC

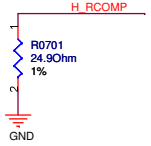
Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 6 of 95

RCOMP

For Calibrating the FSB I/O Buffer

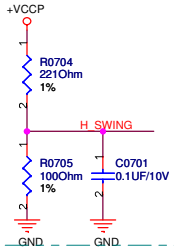


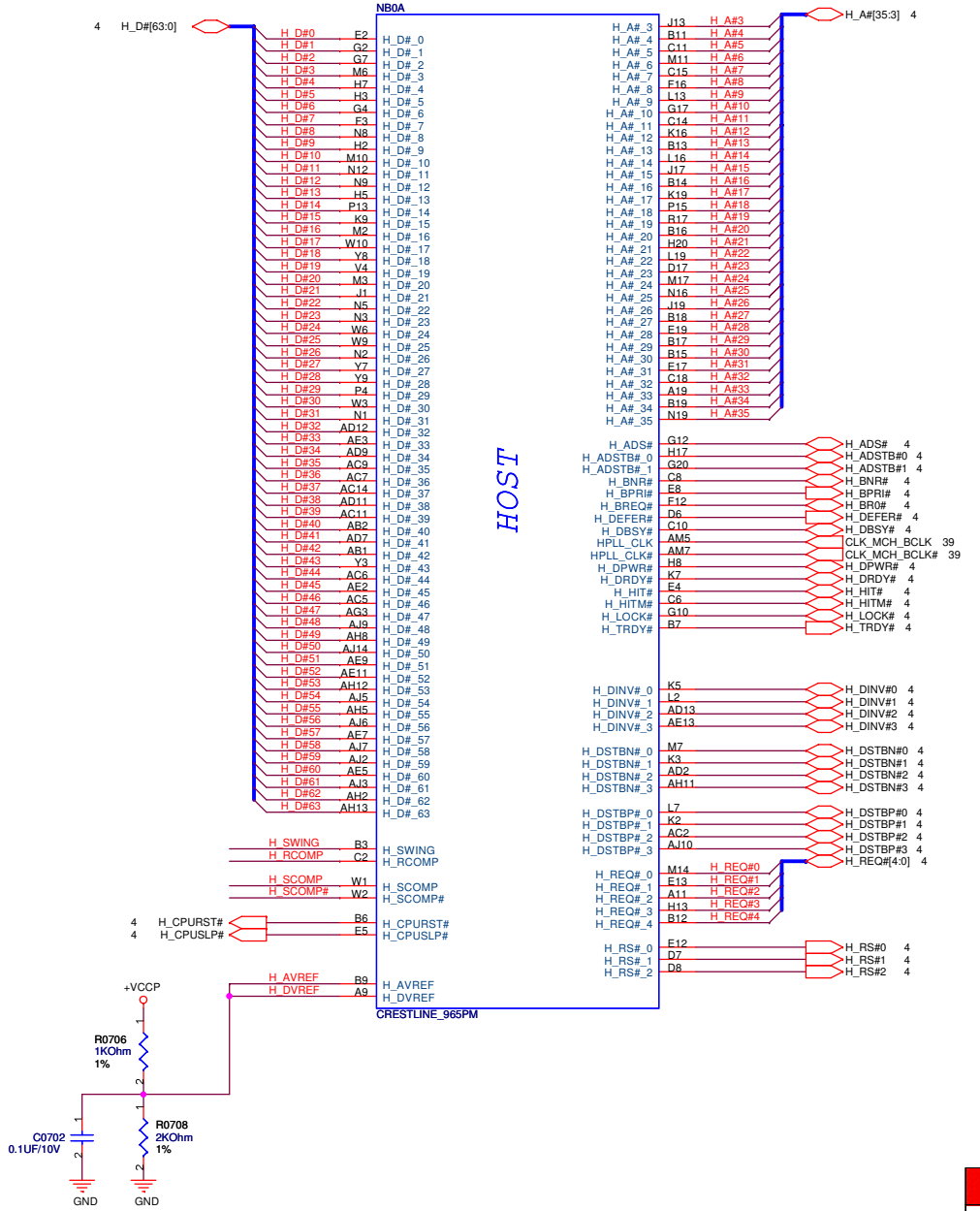
SCOMP

For Slew Rate Compenssation on the FSB

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits





ASUSTeK COMPUTER INC. NB1	Title : NB-965PM(HOST)		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 7 of 95		

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

MCH_CFG_5 — T0803 TPC26T

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed

MCH_CFG_19 — R0802 4.02KOHM — +3VS

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

MCH_CFG_12 — T0805 TPC26T
MCH_CFG_13 — T0806 TPC26T

CFG8 : Low Power PCI-E

0 = Normal mode
1 = Low Power Mode (D)

MCH_CFG_8 — T0804 TPC26T

CFG20 : Concurrent SDVO / PCIe

0 = Only one is operational (D)
1 = operate simultaneous

MCH_CFG_20 — R0808 4.02KOHM — +3VS

CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)

MCH_CFG_9 — R0809 4.02KOHM — GND
R1.1_3

SDVO_CTRL_DATA : SDVO Present

0 = No SDVO (D)
1 = SDVO Present

SDVO_CTRL_DATA — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R0811 4.02KOHM — GND

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L

39 MCH_BSEL0
39 MCH_BSEL1
39 MCH_BSEL2

+1.25VM — R0812 1KOhm 1% — MCH_CLVREF — R0818 392Ohm 1% — C0801 0.1UF/10V — GND

FROM PAGE 83 — 0.9V_VTT_REF

+1.8V — R0822 1KOhm 1% — R0820 0Ohm — M_VREF_MCH 20,21 — R0826 1KOhm 1% — C0804 0.1UF/10V — GND

+1.8V — R0821 1KOhm 1% — SM_RCOMP_VOH — R0823 3.01KOHM 1% — C0802 1UF/10V — C0803 0.01UF/16V — SM_RCOMP_VOL — R0827 1KOhm 1% — C0805 1UF/10V — C0806 0.01UF/16V — GND

NB0B

P36 RSVD1, P37 RSVD2, R35 RSVD3, N35 RSVD4, AR12 RSVD5, AR13 RSVD6, AM12 RSVD7, AN13 RSVD8, J12 RSVD9, AR37 RSVD10, AM36 RSVD11, AL36 RSVD12, AM37 RSVD13, D20 RSVD14 — C0807 0.1UF/10V — GND

H10 RSVD20, B51 RSVD21, BJ20 RSVD22, BK22 RSVD23, BF19 RSVD24, BH20 RSVD25, BK18 RSVD26, BJ18 RSVD27, BF23 RSVD28, BG23 RSVD29, BC23 RSVD30, BD24 RSVD31

20,22 M_A_A14 — M_A_A14 — BJ29 SA_MA_14
21,22 M_B_A14 — M_B_A14 — BF24 SB_MA_14

BH39 RSVD34, AW20 RSVD35, BK20 RSVD36, C48 LVDSA_DATA#_3, D47 LVDSA_DATA_3, B44 RSVD39, C44 RSVD40, A35 RSVD41, B37 RSVD42, B36 RSVD43, B34 RSVD44, C34 RSVD45

39 MCH_BSEL0 — P27 CFG_0
39 MCH_BSEL1 — N27 CFG_1
39 MCH_BSEL2 — N24 CFG_2
C21 CFG_3
C23 CFG_4
MCH_CFG_5 — F23 CFG_5
N23 CFG_6
MCH_CFG_8 — G23 CFG_7
MCH_CFG_9 — J20 CFG_8
C20 CFG_9
R24 CFG_10
L23 CFG_11
MCH_CFG_12 — J23 CFG_12
MCH_CFG_13 — E23 CFG_13
E20 CFG_14
K23 CFG_15
MCH_CFG_16 — M20 CFG_16
M24 CFG_17
L32 CFG_18
MCH_CFG_19 — N33 CFG_19
MCH_CFG_20 — L35 CFG_20

20 PM_EXTTS#_0 — PM_EXTTS#_0
21 PM_EXTTS#_1 — PM_EXTTS#_1

T0801 TPC26T
17 PM_BMBUSY# — G41 PM_BM_BUSY#
4,15,80 H_DPRSTP# — L39 PM_DPRSTP#
+3VS — R0815 10KOhm — R0816 10KOhm 0402 — PM_EXTTS#_0 — L36 PM_EXT_TS#_0 — PM_EXTTS#_1 — J36 PM_EXT_TS#_1
59,60,80,93 CPU_PWRGD — AW49 PWROK
16,17,26,44,48,49,54,59,66,72,73,76 BUF_PLT_RST# — R0817 100Ohm — RST_IN_MCH# — AV20 RSTIN#
4,15,60 PM_THRMTRIP# — N20 THERMTRIP#
17,80 PM_DPRSLPVR — G36 DPRSLPVR

BJ51 NC_1, BK51 NC_2, BK50 NC_3, BL50 NC_4, BL49 NC_5, BL3 NC_6, BL2 NC_7, BK1 NC_8, BJ1 NC_9, E1 NC_10, A5 NC_11, C51 NC_12, B50 NC_13, A50 NC_14, A49 NC_15, BK2 NC_16

CRESTLINE_965PM

DDR MUXING

SM_CK_0 AV29 M_CLK_DDR0 20
SM_CK_1 BB23 M_CLK_DDR1 20
SM_CK_3 BA25 M_CLK_DDR2 21
SM_CK_4 AV23 M_CLK_DDR3 21

SM_CK#_0 AW30 M_CLK_DDR#0 20
SM_CK#_1 BA23 M_CLK_DDR#1 20
SM_CK#_3 AW25 M_CLK_DDR#2 21
SM_CK#_4 AW23 M_CLK_DDR#3 21

SM_CKE_0 BE29 M_CKE0 20,22
SM_CKE_1 AY32 M_CKE1 20,22
SM_CKE_3 BD39 M_CKE2 21,22
SM_CKE_4 BG37 M_CKE3 21,22

SM_CS#_0 BG20 M_CS#0 20,22
SM_CS#_1 BK16 M_CS#1 20,22
SM_CS#_2 BG16 M_CS#2 21,22
SM_CS#_3 BE13 M_CS#3 21,22

SM_ODT_0 BH18 M_ODT0 20,22
SM_ODT_1 BJ15 M_ODT1 20,22
SM_ODT_2 BJ14 M_ODT2 21,22
SM_ODT_3 BE16 M_ODT3 21,22

SM_RCOMP BL15 — R0803 20Ohm 1% — +1.8V
SM_RCOMP# BK14 — R0804 20Ohm 1% — GND
R1.1_2
SM_RCOMP_VOH BK31
SM_RCOMP_VOL BL31
SM_VREF_0 AR49
SM_VREF_1 AW4 — M_VREF_MCH
For Calero 20 Ohm
For Crestline 80.6 Ohm

CLK

DPLL_REF_CLK B42
DPLL_REF_CLK# C42
DPLL_REF_SSCLK H48
DPLL_REF_SSCLK# H47 — GND
PEG_CLK K44 — CLK_MCH_3GPLL 39
PEG_CLK# K45 — CLK_MCH_3GPLL# 39

DMI

DMI_RXN_0 AN47 DMI_TXN0
DMI_RXN_1 AJ38 DMI_TXN1
DMI_RXN_2 AN42 DMI_TXN2
DMI_RXN_3 AN46 DMI_TXN3 — DMI_TXN[3:0] 16

DMI_RXP_0 AM47 DMI_TXP0
DMI_RXP_1 AJ39 DMI_TXP1
DMI_RXP_2 AN41 DMI_TXP2
DMI_RXP_3 AN45 DMI_TXP3 — DMI_TXP[0..3] 16

DMI_TXN_0 AJ46 DMI_RXN0
DMI_TXN_1 AJ41 DMI_RXN1
DMI_TXN_2 AM40 DMI_RXN2
DMI_TXN_3 AM44 DMI_RXN3 — DMI_RXN[0..3] 16

DMI_TXP_0 AJ47 DMI_RXP0
DMI_TXP_1 AJ42 DMI_RXP1
DMI_TXP_2 AM39 DMI_RXP2
DMI_TXP_3 AM43 DMI_RXP3 — DMI_RXP[0..3] 16

GRAPHICS VID

GFX_VID_0 E35
GFX_VID_1 A39
GFX_VID_2 C38
GFX_VID_3 B39
GFX_VR_EN E36

ME

CL_CLK AM49 — CL_CLK0 17
CL_DATA AK50 — CL_DATA0 17
CL_PWROK AT43 — MP_PWRGD 17,59
CL_RST# AN49 — CL_RST#0 17
CL_VREF AM50 — MCH_CLVREF

MISC

SDVO_CTRL_CLK H35 — T0802 TPC26T (INT PD)
SDVO_CTRL_DATA K36 — SDVO_CTRL_DATA (INT PD)
CLK_REQ# G39 — CLK_MCH_OE#
ICH_SYNC# G40 — MCH_ICH_SYNC# 17
+3VS — R0813 10KOhm
TEST_1 A37
TEST_2 R32 — R0825 22kOhm — GND

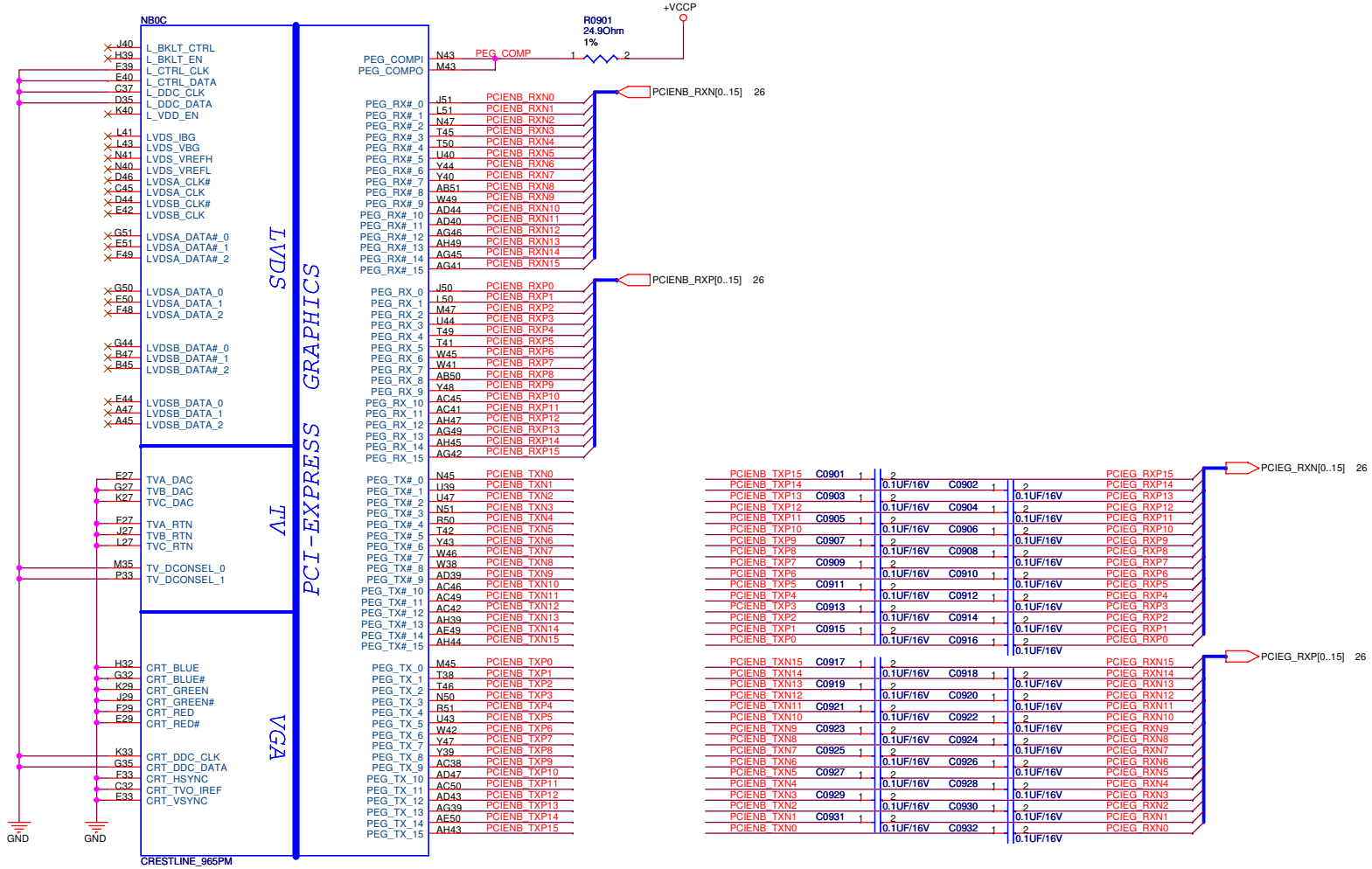
<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : NB-965PM(DMI & CFG)
Engineer: Jerry Mou

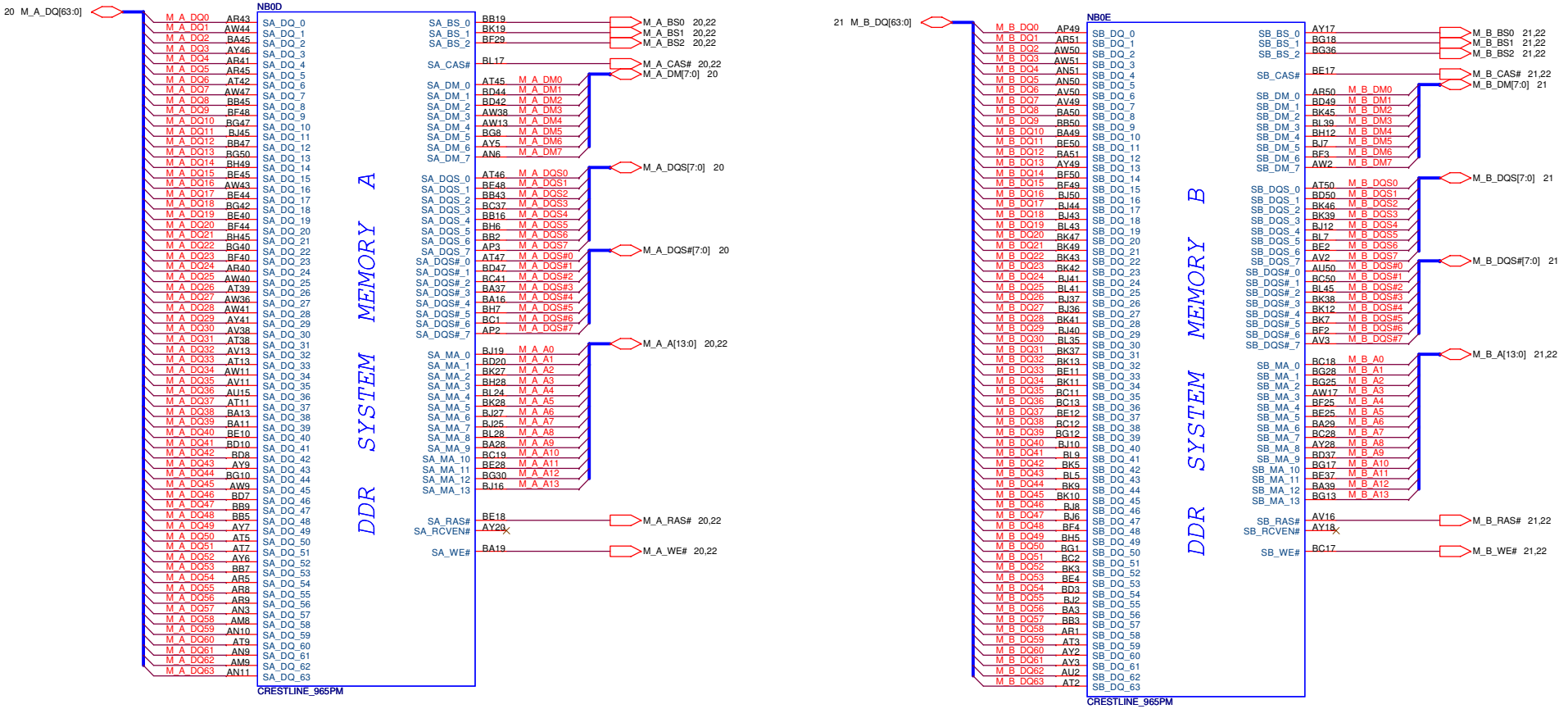
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 8 of 95



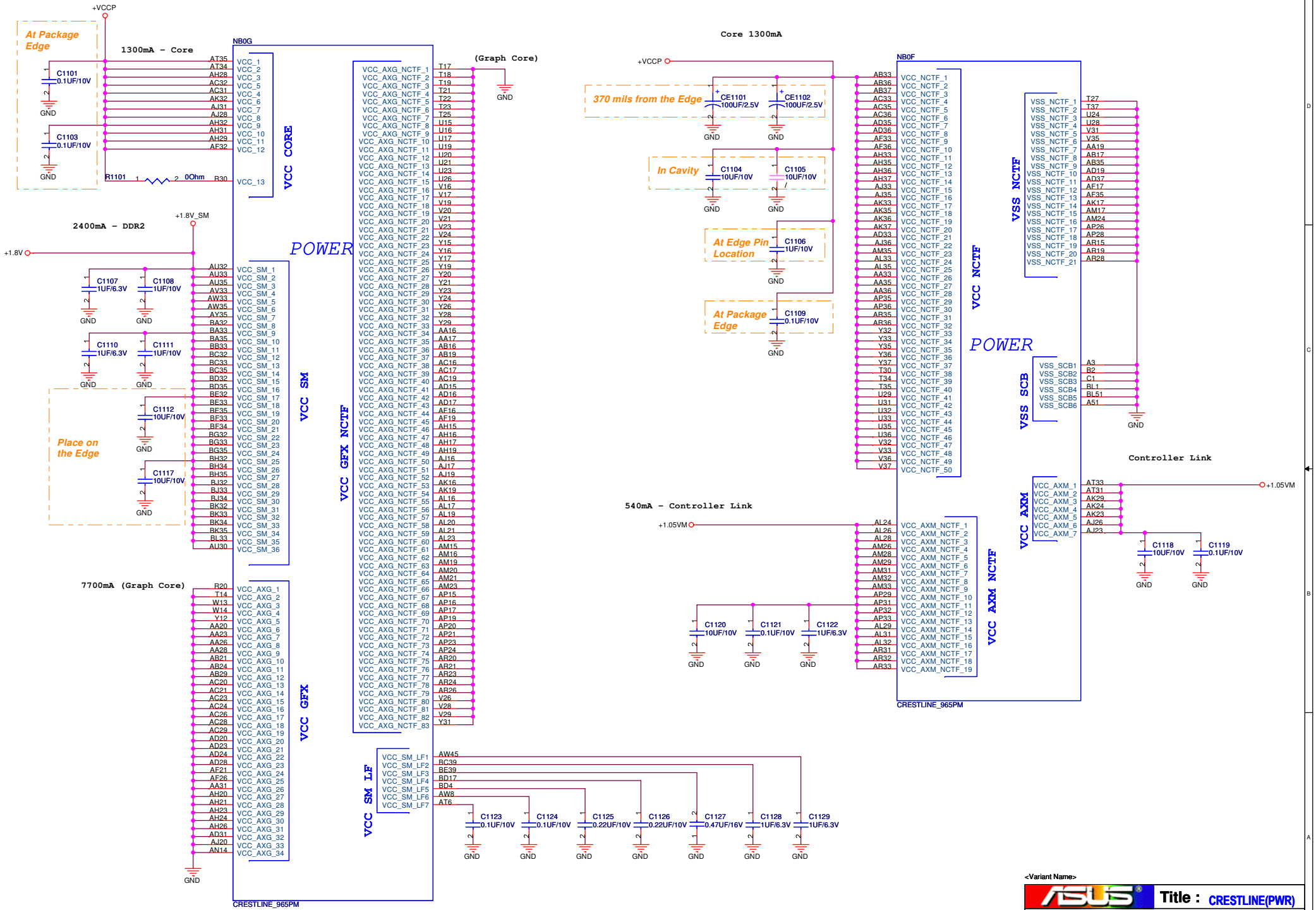
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(GRAPHIC)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 9 of 95	



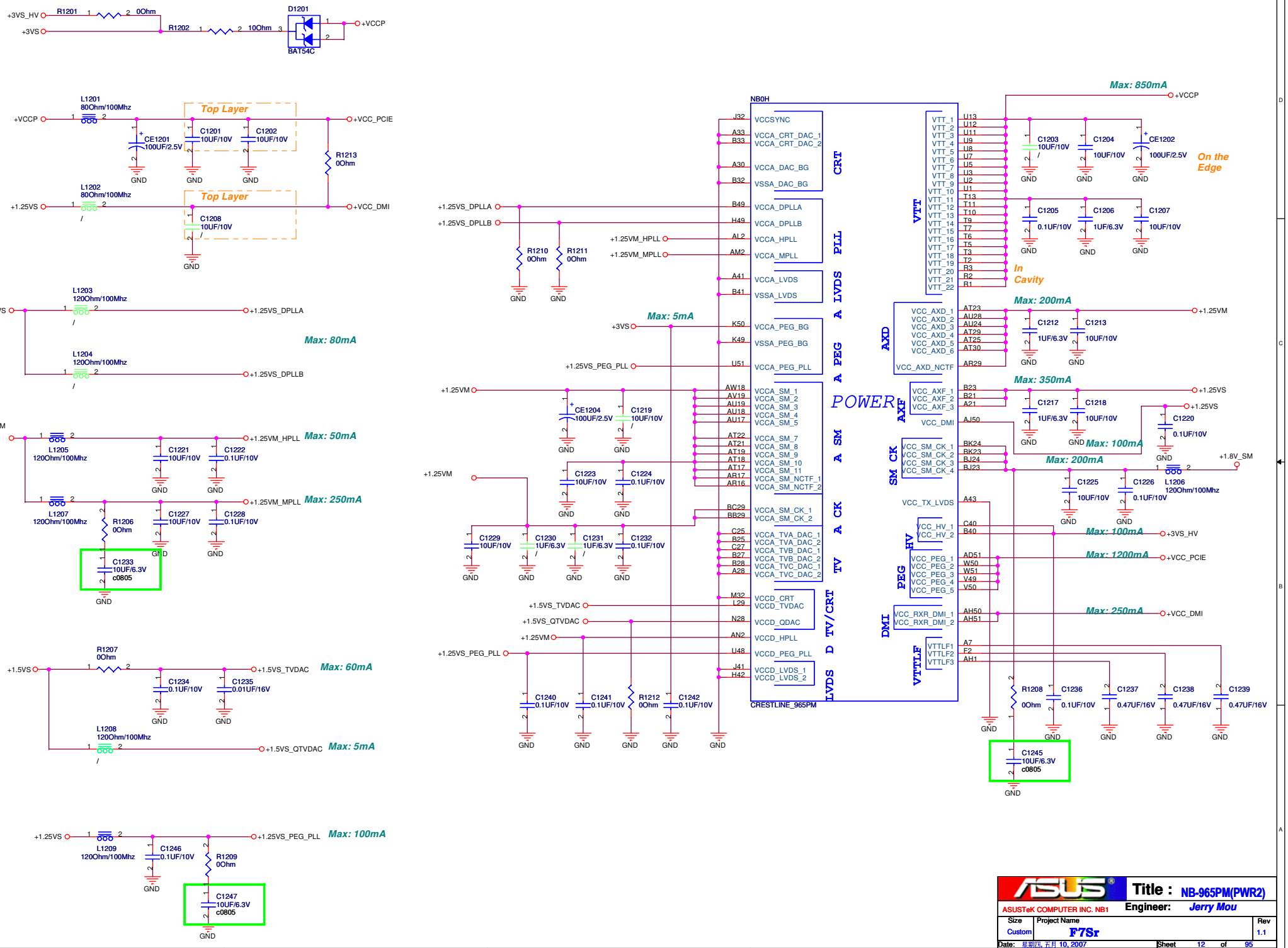
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB-965PM(DDR2)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 10 of 95	

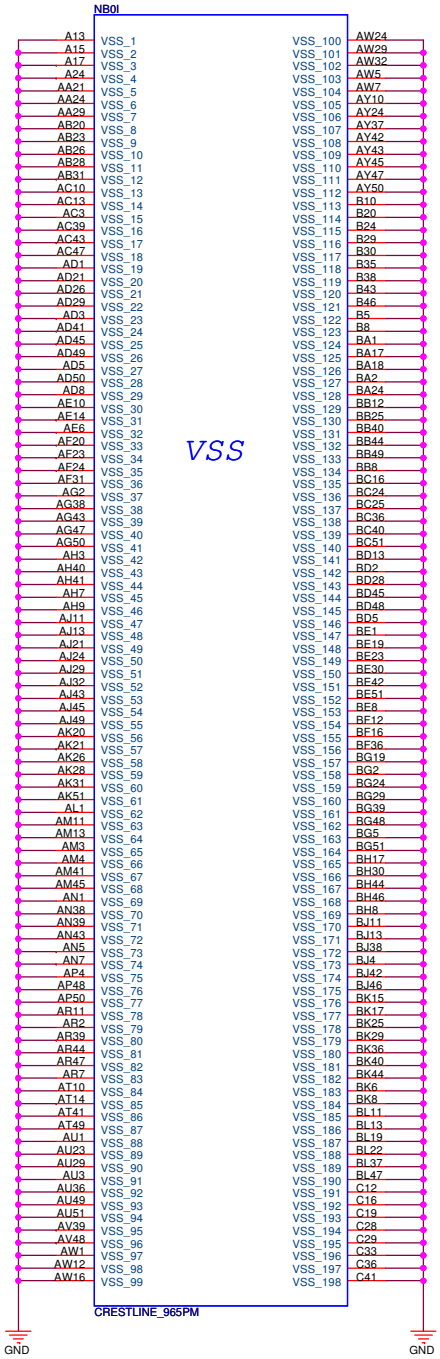


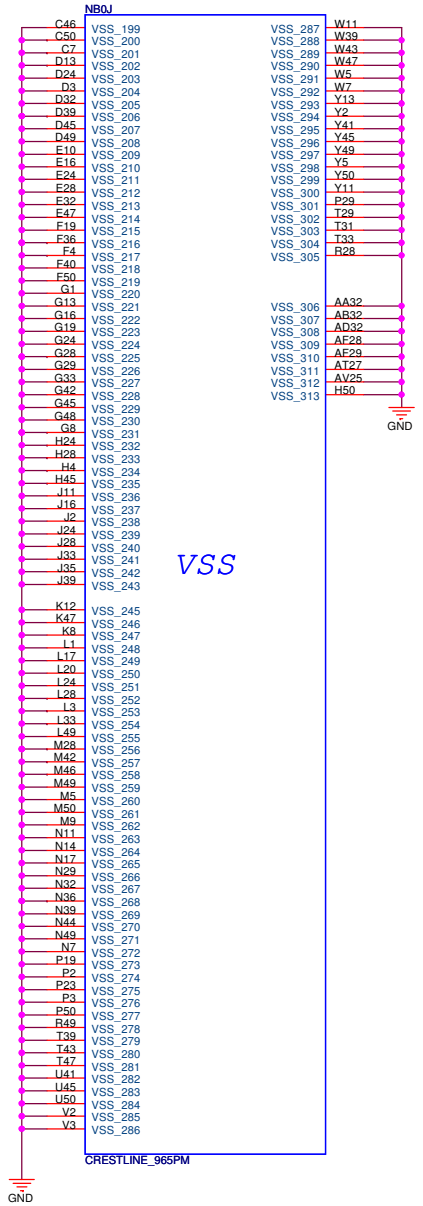
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CRESTLINE(PWR)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 11 of 95	



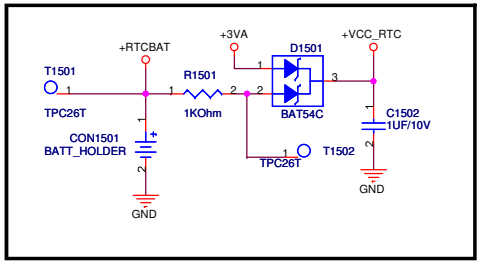
Title :	NB-965PM(PWR2)	
ASUSTeK COMPUTER INC. NB1	Engineer:	Jerry Mou
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 12 of 95	

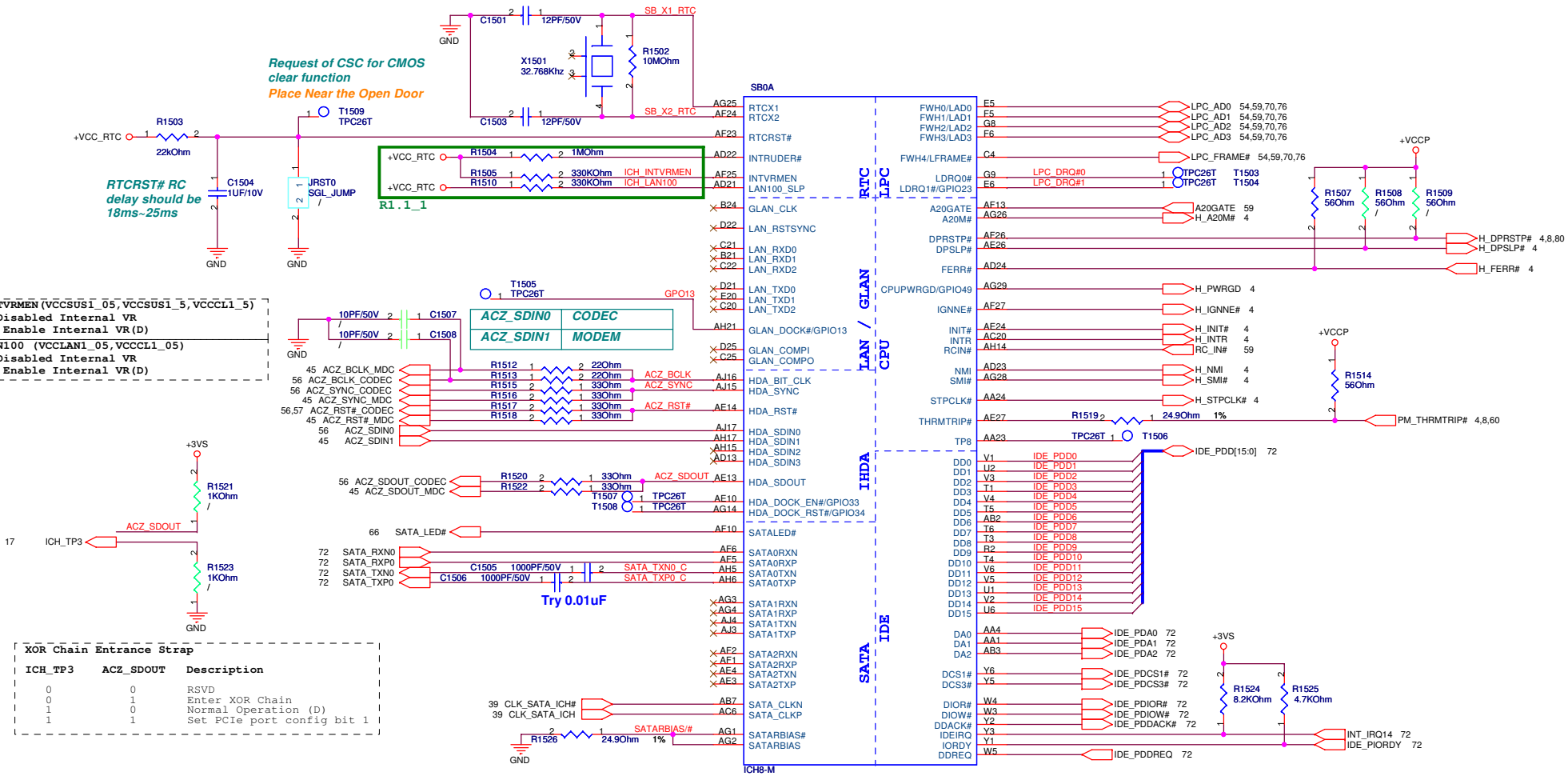




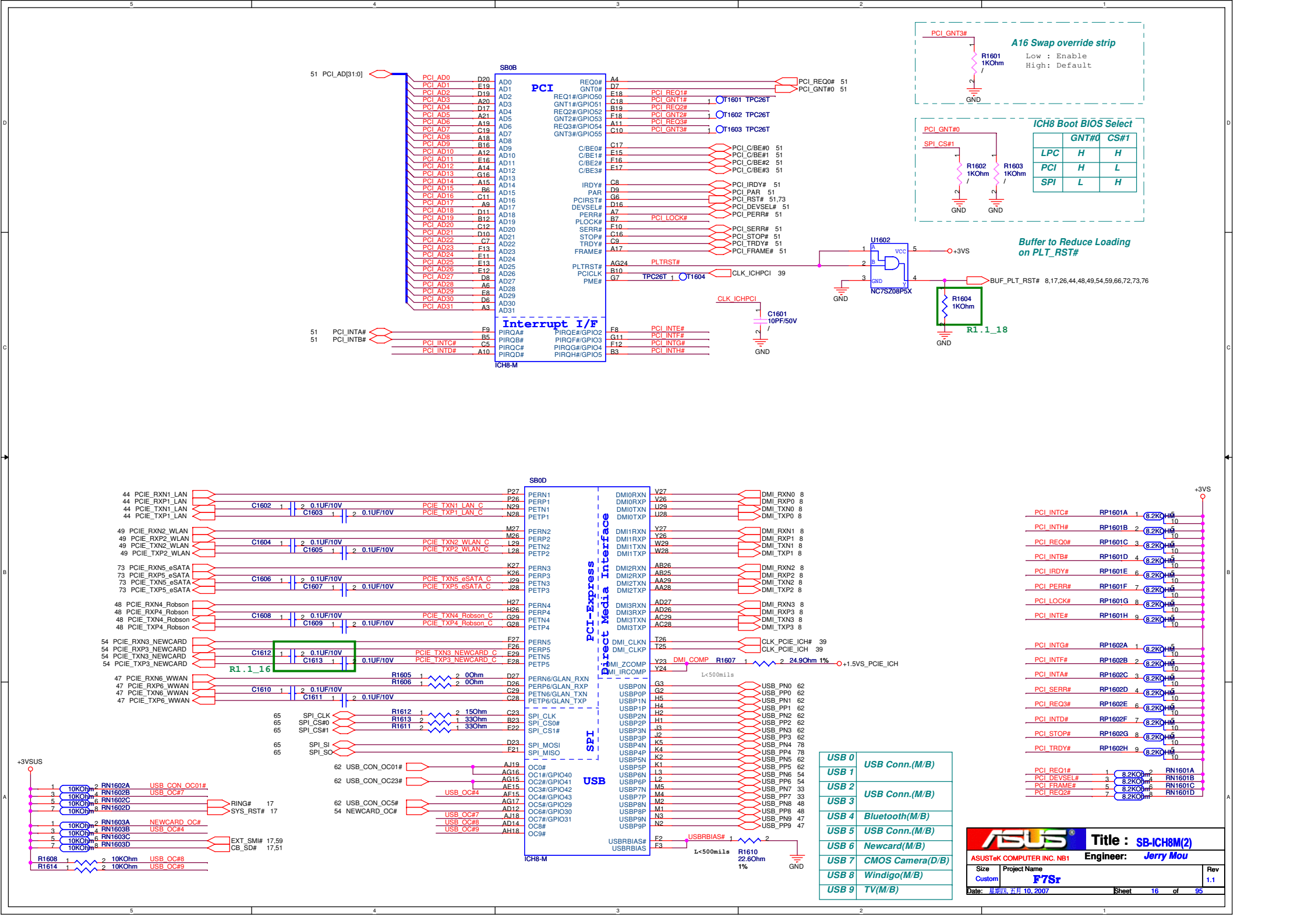
ASUSTeK COMPUTER INC. NB1	Title : CRESTLINE(GND)		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007		Sheet 13 of 95	

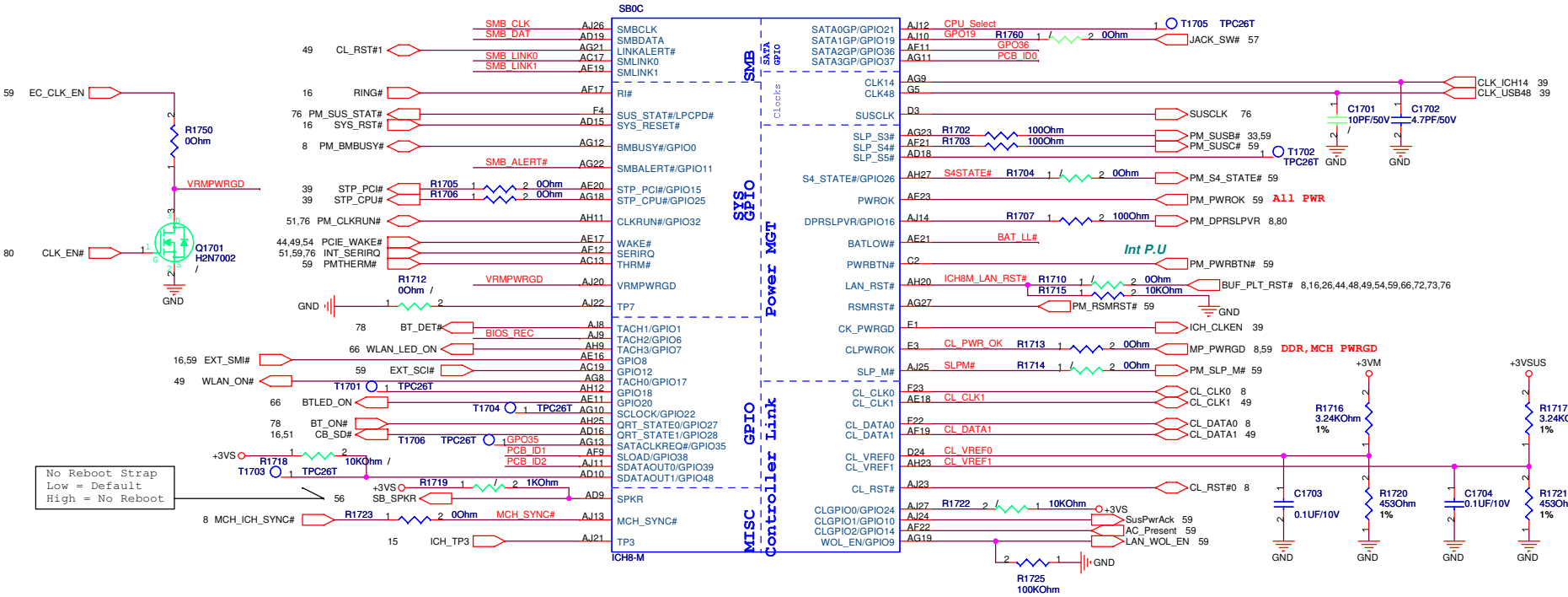
ASUSTeK COMPUTER INC	Title : Blank Page		
	Engineer: Jerry Mou		
Size: C	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 14 of 95		


+RTCBAT
+3VA
+VCC_RTC
T1501
R1501
D1501
TPC26T
1KOhm
BAT54C
C1502
1UF/10V
CON1501
BATT_HOLDER
TPC26T
T1502
GND
GND


Request of CSC for CMOS clear function
Place Near the Open Door
RTCRST# RC delay should be 18ms~25ms
R1.1_1
SB0A
RTC
LPC
GLAN
LAN / CPU
IHDA
SATA
IDE
ICH8-M
ICH_INTVRMEN(VCCSUS1_05,VCCSUS1_5,VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR(D)
ICH_LAN100 (VCCLAN1_05,VCCCL1_05)
Low - Disabled Internal VR
High - Enable Internal VR(D)
ACZ_SDIN0 CODEC
ACZ_SDIN1 MODEM
Try 0.01uF
XOR Chain Entrance Strap
ICH_TP3 ACZ_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (D)
1 1 Set PCIe port config bit 1

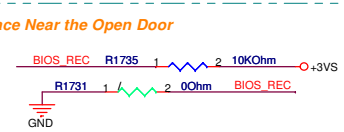
Variant Name
Title : SB-ICH8M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: Jerry Mou
Size Custom
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 15 of 95


A16 Swap override strip
Low : Enable
High: Default
ICH8 Boot BIOS Select
GNT#0 CS#1
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
SB0B
PCI
Interrupt I/F
ICH8-M
SB0D
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M
USB 0 USB Conn.(M/B)
USB 1
USB 2 USB Conn.(M/B)
USB 3
USB 4 Bluetooth(M/B)
USB 5 USB Conn.(M/B)
USB 6 Newcard(M/B)
USB 7 CMOS Camera(D/B)
USB 8 Windigo(M/B)
USB 9 TV(M/B)
Title : SB-ICH8M(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Jerry Mou
Size Custom
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 16 of 95



Mount for BIOS Recovery

Place Near the Open Door



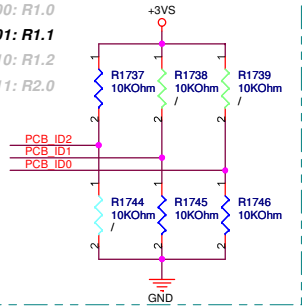
PCB_ID[0:2]

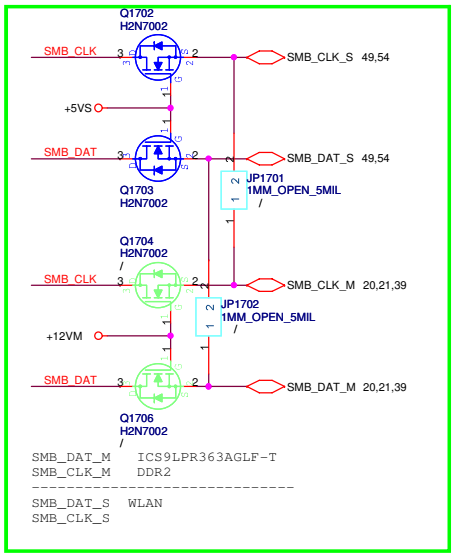
000: R1.0

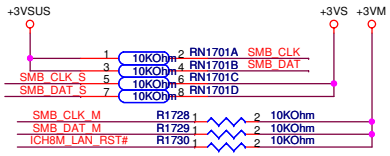
001: R1.1

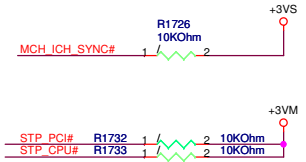
010: R1.2

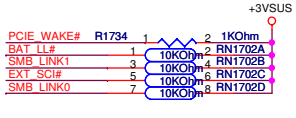
011: R2.0

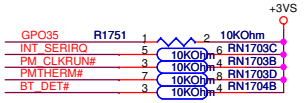


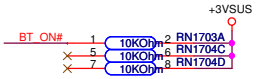


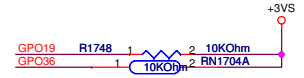


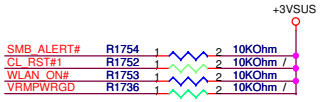


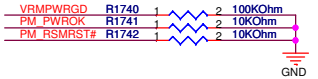


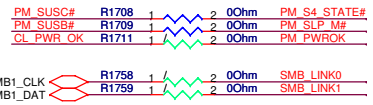






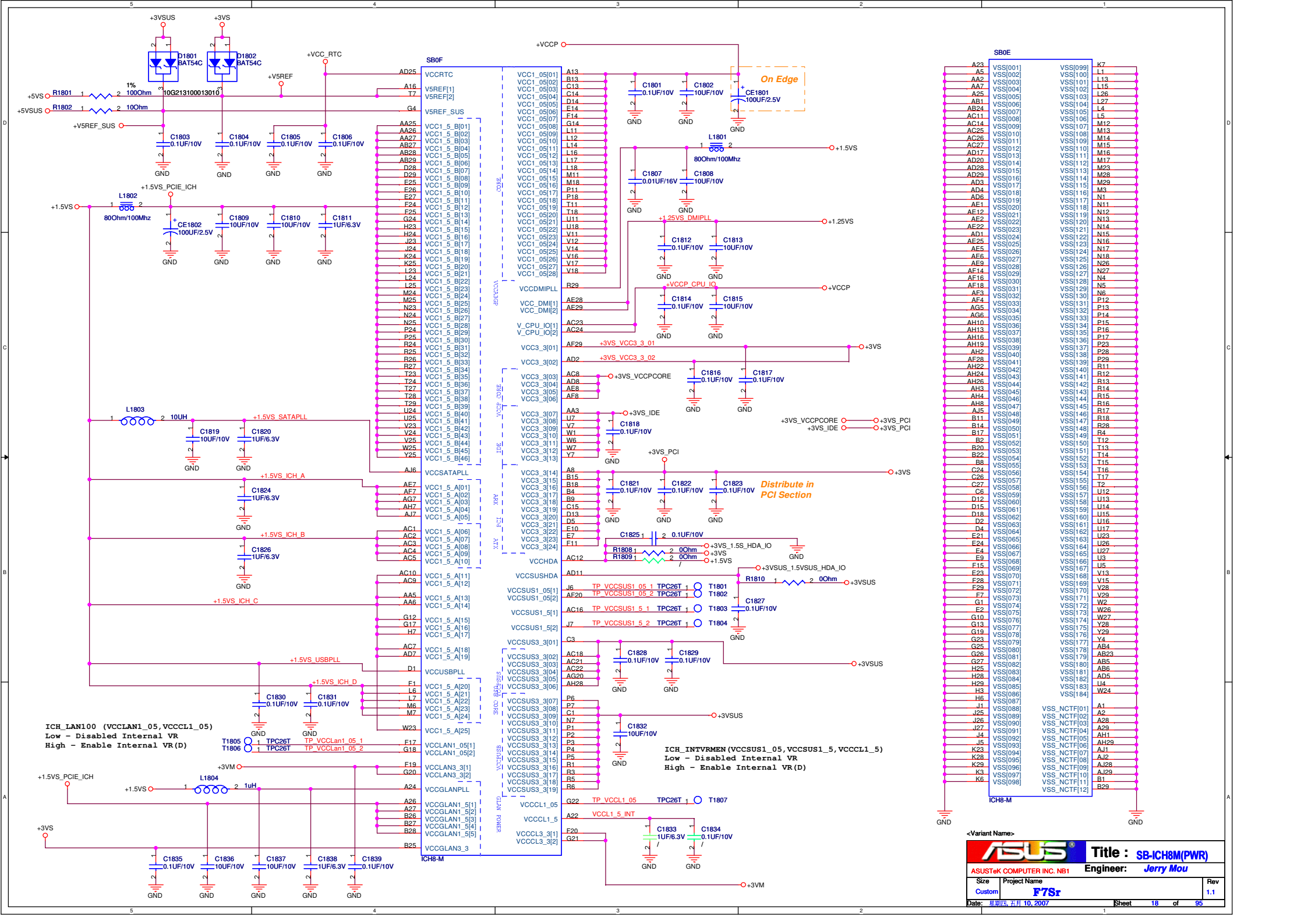






<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH8M(3)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 17 of 95	


SB0F
SB0E
ICH8-M
D1801 BAT54C
D1802 BAT54C
L1801 80Ohm/100Mhz
L1802 80Ohm/100Mhz
L1803 10UH
L1804 1uH
On Edge
CE1801 100UF/2.5V
CE1802 100UF/2.5V
Distribute in PCI Section
ICH_LAN100 (VCCLAN1_05,VCCCL1_05)
Low - Disabled Internal VR
High - Enable Internal VR(D)
ICH_INTVRMEN(VCCSUS1_05,VCCSUS1_5,VCCCL1_5)
Low - Disabled Internal VR
High - Enable Internal VR(D)
Title : SB-ICH8M(PWR)
ASUSTeK COMPUTER INC. NB1
Engineer: Jerry Mou
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 18 of 95

Title : Blank Page

ASUSTeK COMPUTER INC

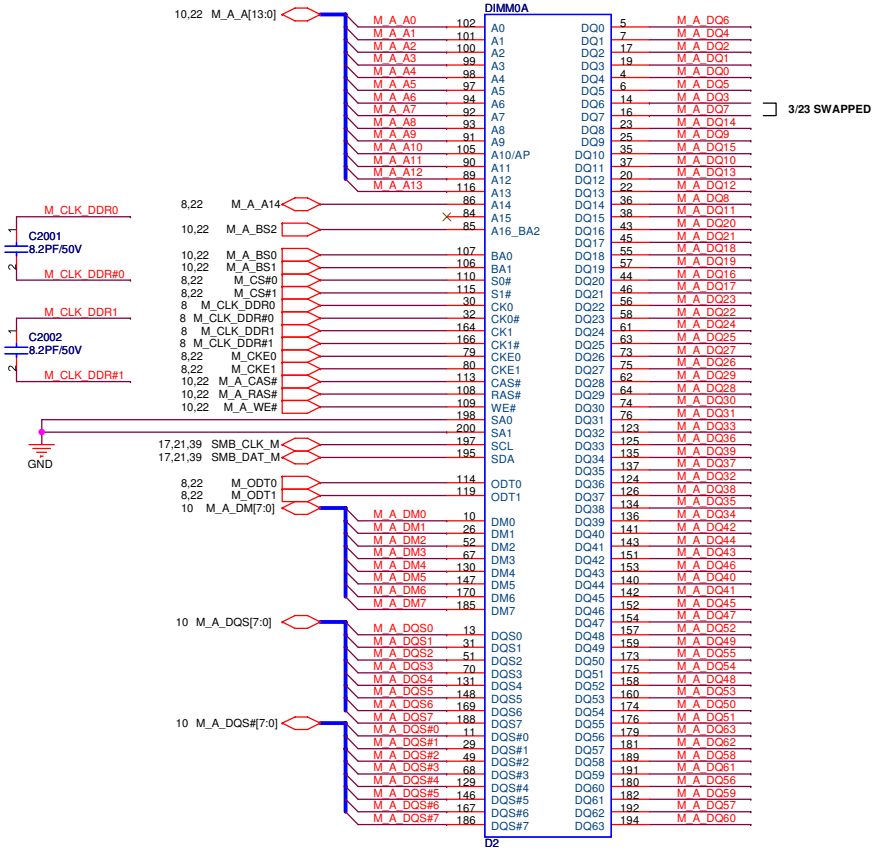
Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

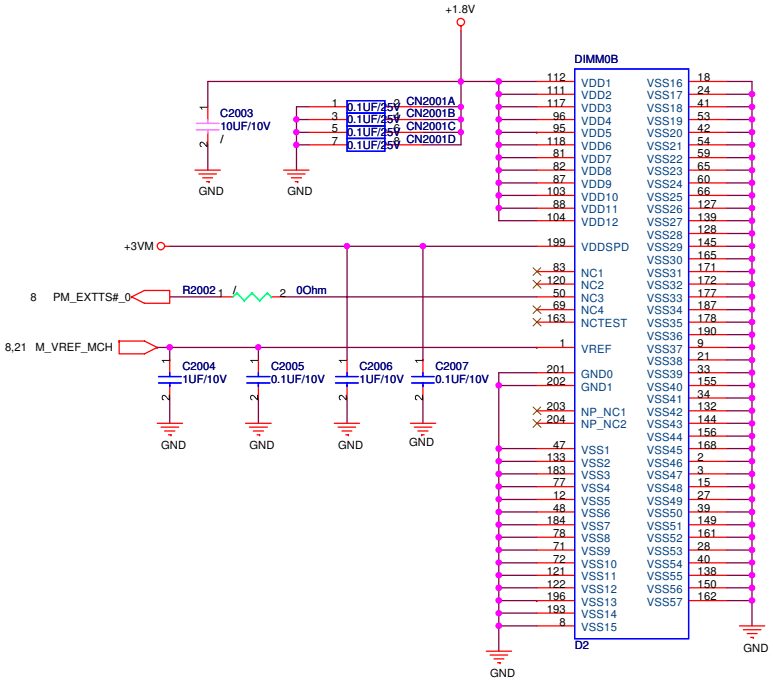
Date: 星期四, 五月 10, 2007 Sheet 19 of 95

M_A_DQ[63:0] 10

REV Type - 12G025122006
ME - 12G025332003



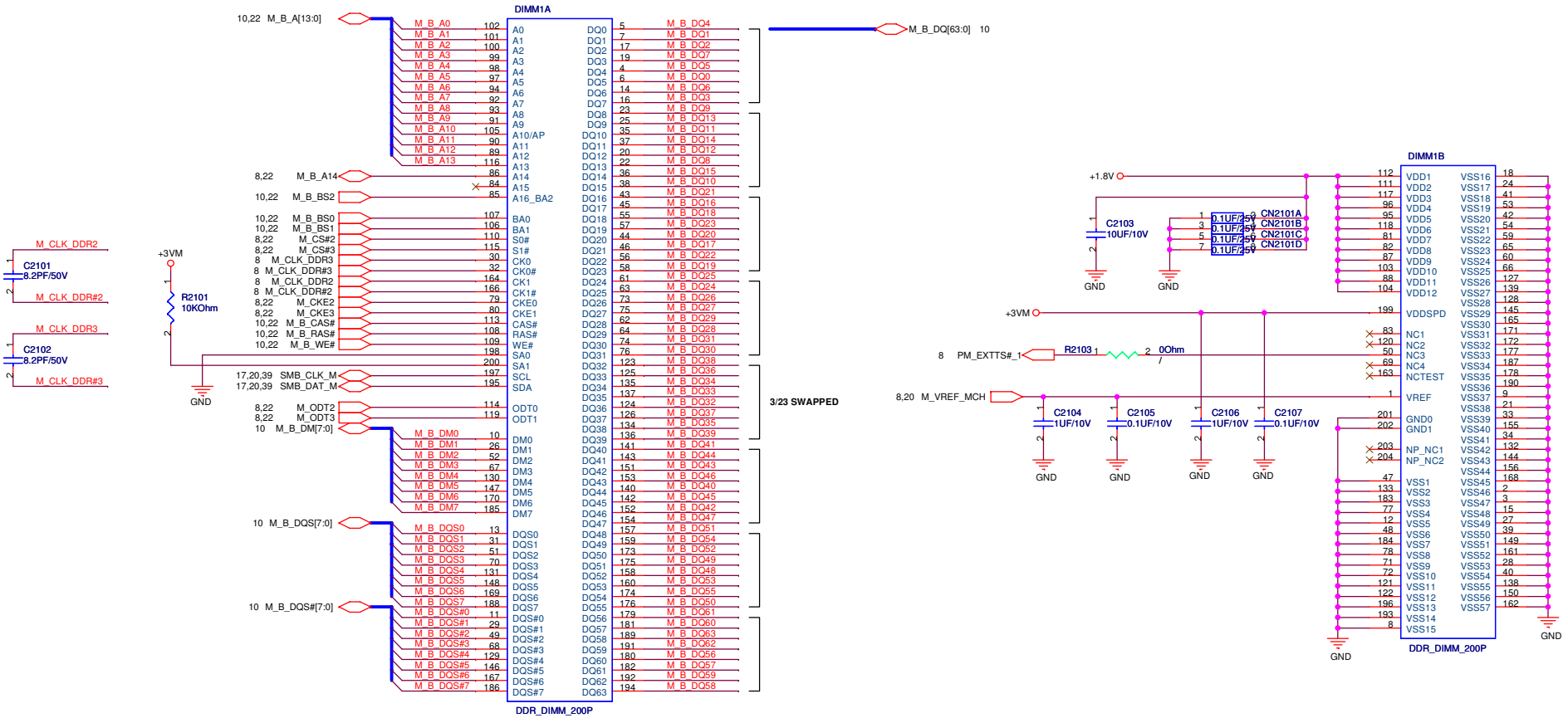
3/23 SWAPPED



<Variant Name>

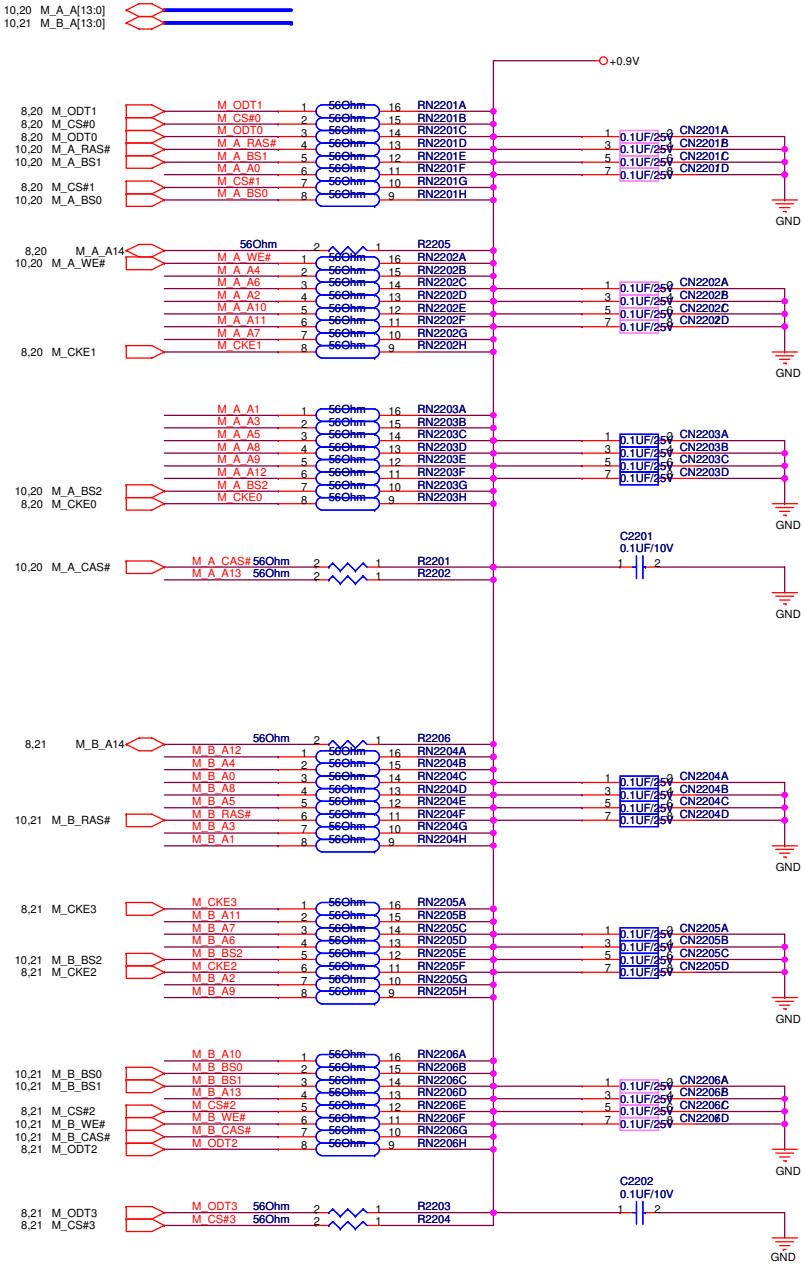
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 20 of 95	

STD Type - 12G025122000



<Variant Name>

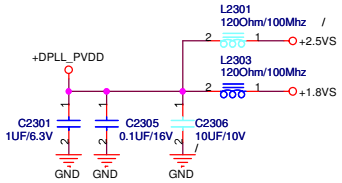
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 21 of 95	



<Variant Name>

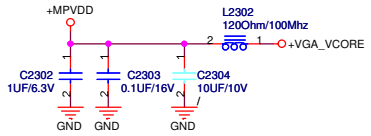
ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 22 of 95	

M66/M76M Power

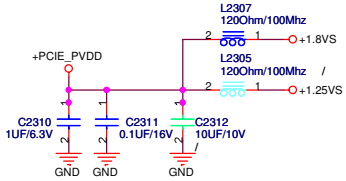


(2.5V @ 170MA DPLL_PVDD) INSTALL DPLL_PVDD TO +2.5V FOR M66M

(1.8V @ 40MA DPLL_PVDD) INSTALL DPLL_PVDD TO +1.8V FOR M76M

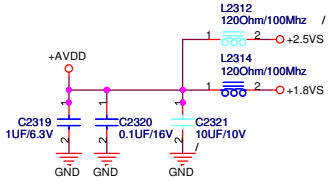


(0.95V~1.1V @ 345MA MPVDD)



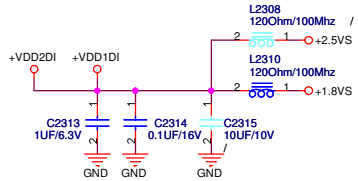
(1.8V @ 40mA PCIE_PVDD) INSTALL PCIE_PVDD TO +1.8V FOR M76M

(1.2V @ 90mA PCIE_PVDD) INSTALL PCIE_PVDD TO +1.2V FOR M66M



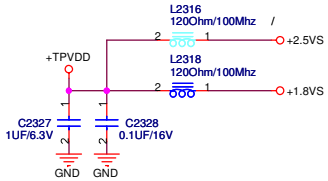
(2.5V @ 100MA AVDD) INSTALL AVDD TO +2.5V FOR M66M

(1.8V @ 100MA AVDD) INSTALL AVDD TO +1.8V FOR M76M



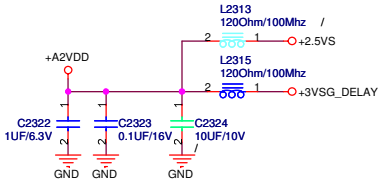
(2.5V @ 110 MA VDD1DI) INSTALL VDD1DI,VDD2DI TO +2.5V FOR M66M

(1.8V @ 100MA VDD1DI) INSTALL VDD1DI,VDD2DI TO +1.8V FOR M76M



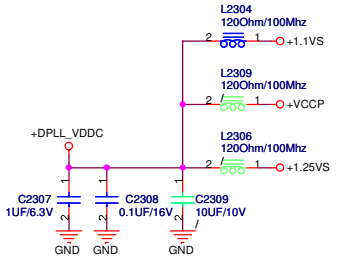
(2.5V @ 60MA TPVDD) INSTALL TPVDD TO +2.5V FOR M66M

(1.8V @ 20MA TPVDD) INSTALL TPVDD TO +1.8V FOR M76M



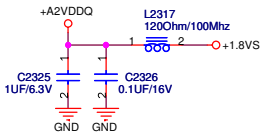
(2.5V @ 120MA A2VDD) INSTALL A2VDD TO +2.5V FOR M66M

(3.3V @ 135MA A2VDD) INSTALL A2VDD TO +3.3V FOR M76M



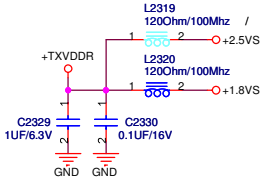
(1.25V @ 100MA AVDD) INSTALL +DPLL_VDDC TO +1.25V FOR M66M

(1.1V @ 100MA AVDD) INSTALL +DPLL_VDDC TO +1.1V FOR M76M



(1.8V @ 2MA A2VDDQ) INSTALL A2VDDQ TO +1.8V FOR M76M

DO NOT INSTALL A2VDDQ FOR M66M



(2.5V @ 155MA TXVDDR) INSTALL TXVDDR TO +2.5V FOR M66M

(1.8V @ 200mA TXVDDR) INSTALL TXVDDR TO +1.8V FOR M76M

<Variant Name>

ASUSTeK COMPUTER INC	Title : VGA M72M POWER	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 23 of 95	

Spread Spectrum

	SRS		NC.
P1819B	-1.25	-1.75	x.
MK1726	-1.8	-2.5	-0.6.

ROM Strap

Primary Memory Aperture size requested at PCI Configuration

	GPIO_13	GPIO_12	GPIO_11
1GB	1	0	1
512MB	1	0	0
256MB	0	0	1
128MB	0	0	0
64MB	0	1	0
32MB	0	1	1

Memory ID

*Infineon (DDR2 16M*16 for A Channel 1.8V 128M)*
MEM ID[0:3] = 0100

*Hynix (DDR2 16M*16 for A Channel 1.8V 128M)*
MEM ID[0:3] = 1100

Thermal

MAX6657MSA

R1.3

FOR M76M
VREFG VOLTAGE DIVIDER IS VREFG = VDDR4,5 = 1.8V / 3 = 0.6V
R2463=249ohm

FOR M66M
VREFG VOLTAGE DIVIDER IS VREFG = 3.3V / 2 = 1.65V
R2463=499ohm

XTALIN VOLTAGE LEVEL
1.2V FOR M66M (R2438 = 71.5ohm)
1.8V FOR M76M (R2438 = 150ohm)

MOUNT R2449 FOR M7x

INSTALL TERMINATION RESISTORS CLOSE TO ASIC

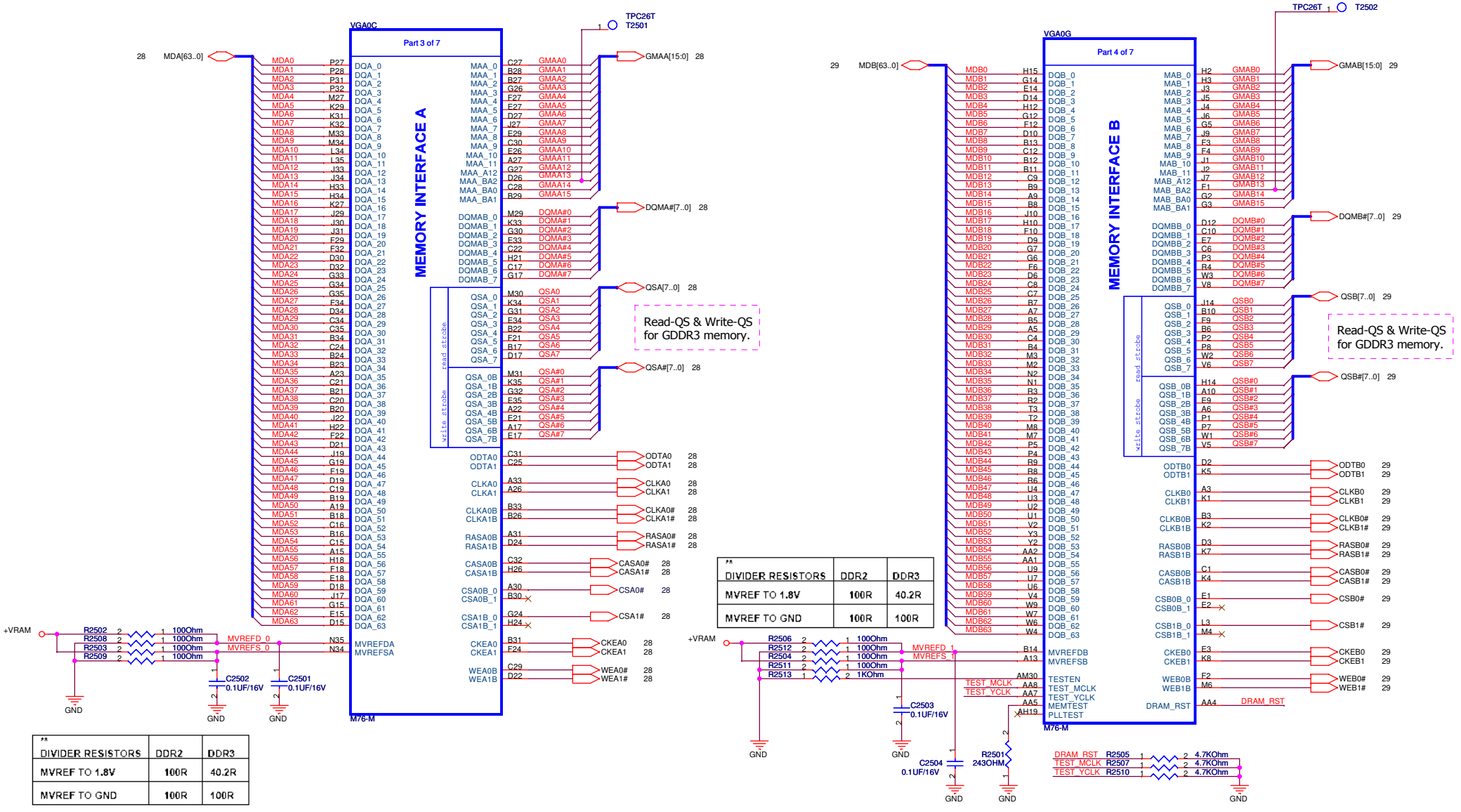
M72 - Close to GPU
M76 - All mount 0 ohm

HDMI_EN

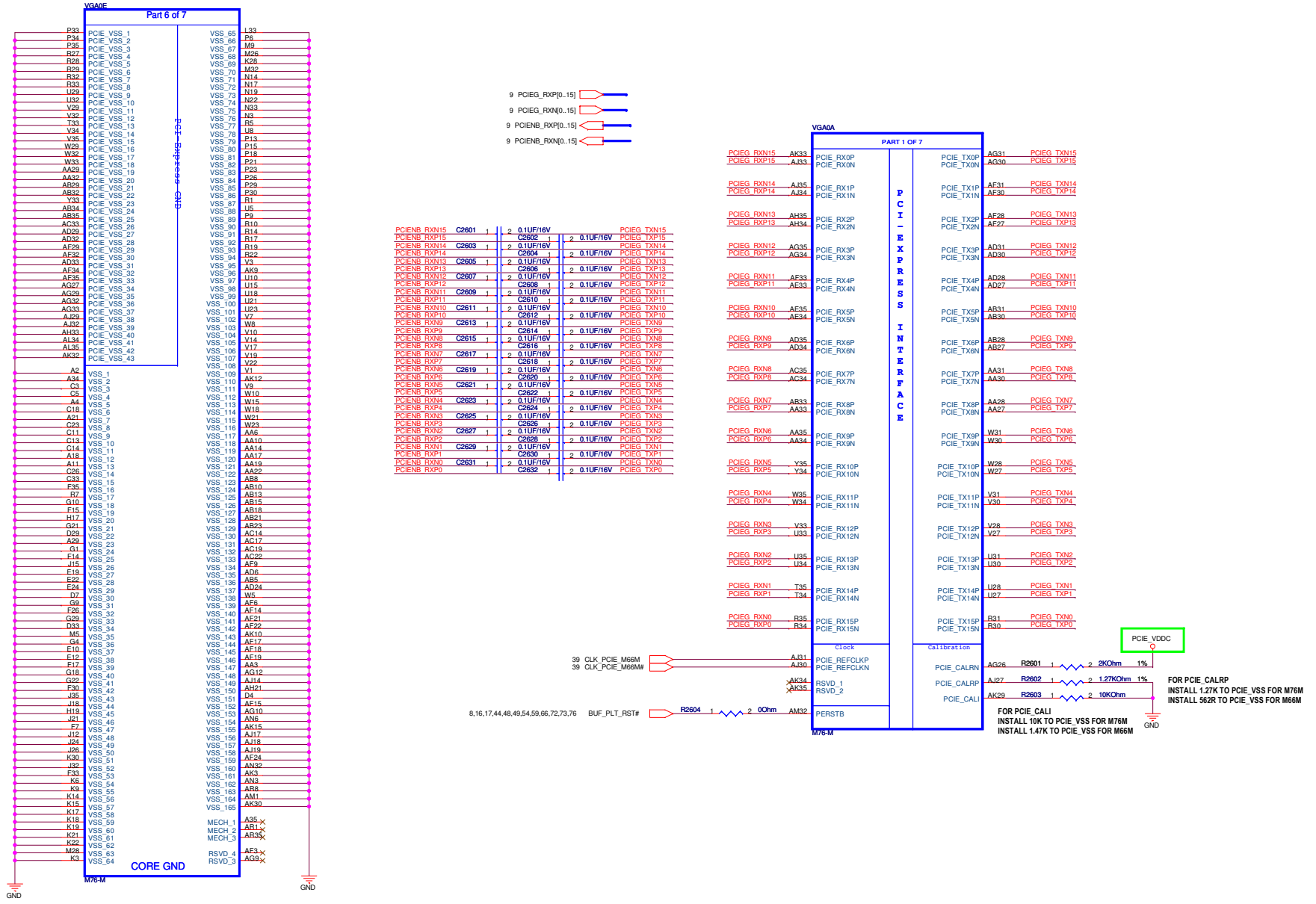
CHANGE BOM P/N TO M72

M76-M

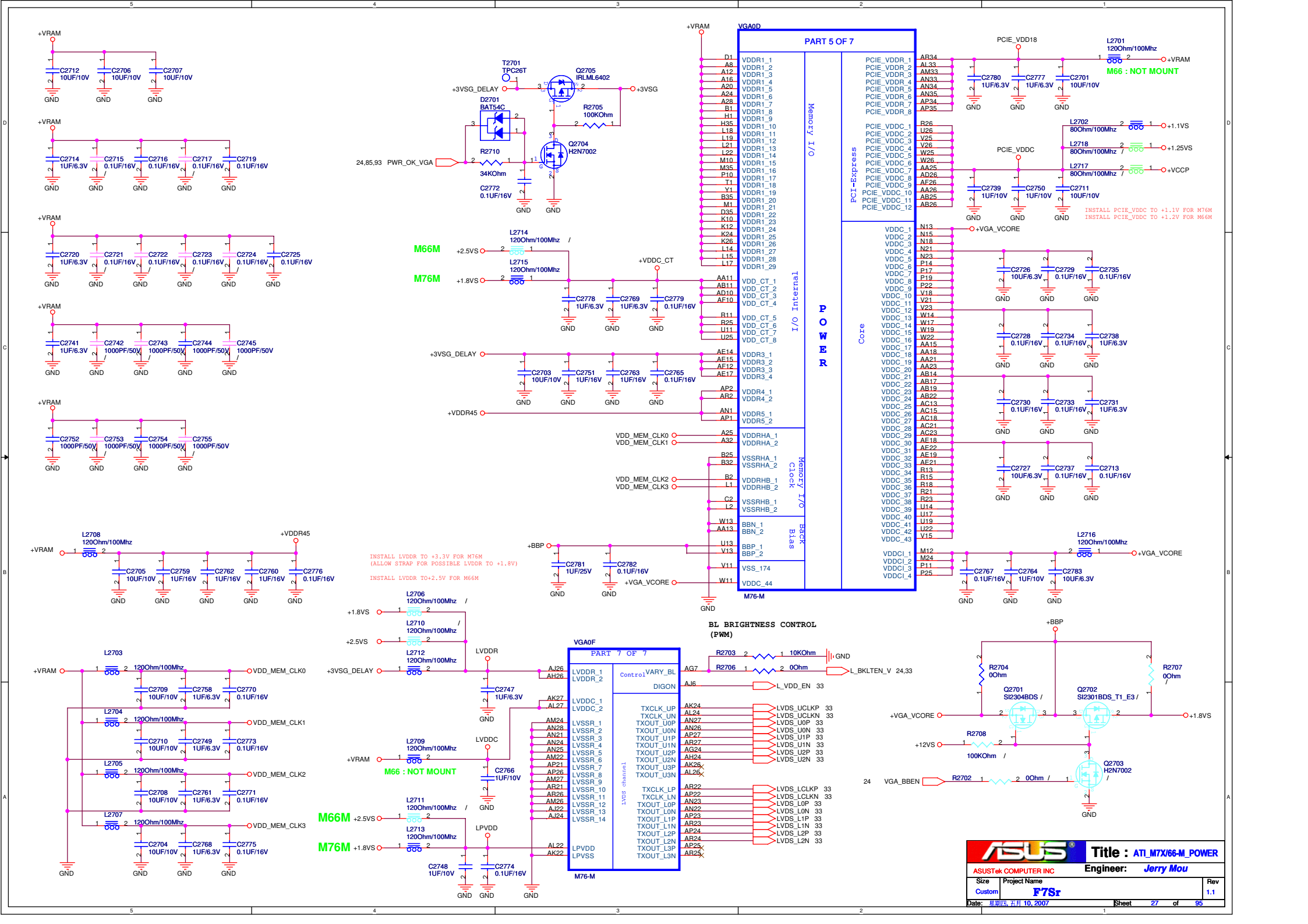
Title	ATI_M7X/66-M_MAIN
ASUSTek COMPUTER INC	Engineer: Jerry Mou
Size: Custom	Project Name: F7Sr
Rev	1.1
Date: 星期四, 五月 10, 2007	Sheet 24 of 95

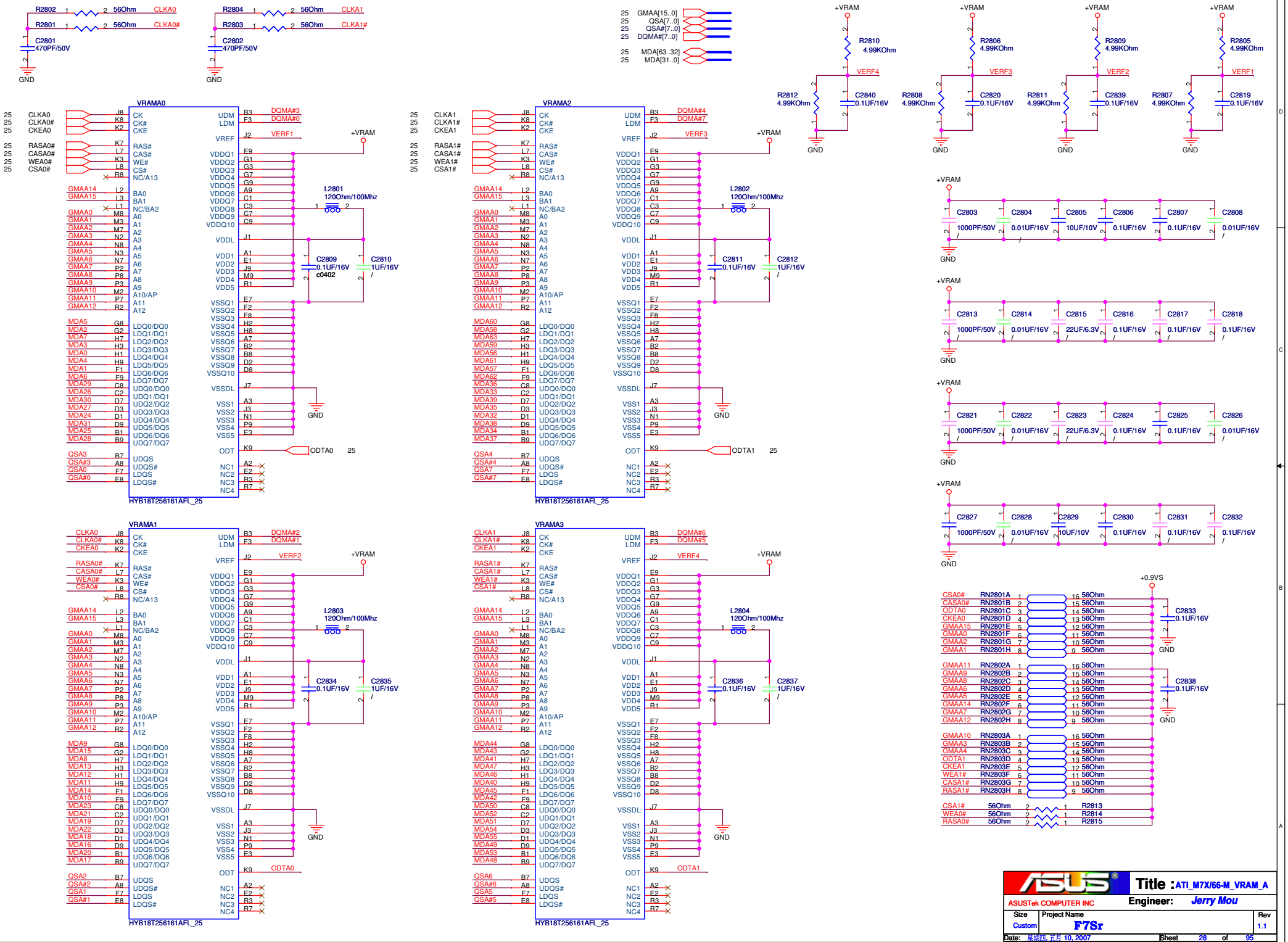


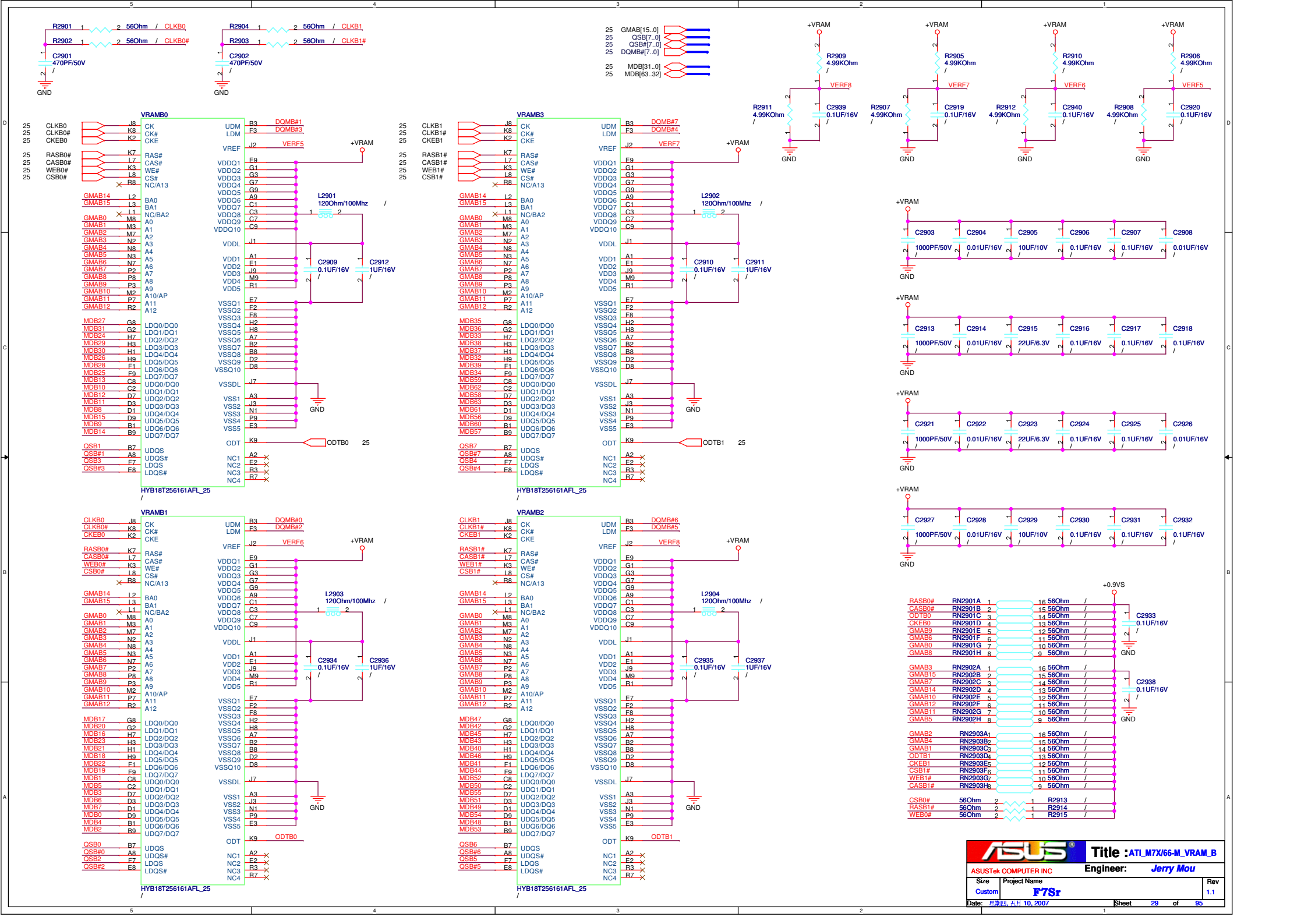
Title :	ATI_M7X/66-M_Memory	
ASUSTek COMPUTER INC	Engineer:	Jerry Mou
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 25 of 95	

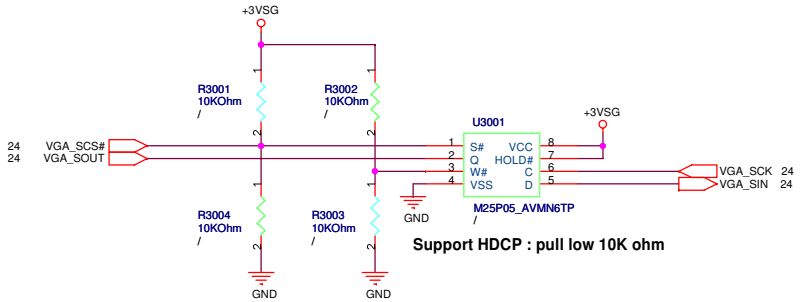


ASUSTek COMPUTER INC	Title : ATI_M7X/66-M_PCI-E	
	Engineer: Jerry Mou	
Size: C	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 26 of 95	


PART 5 OF 7
VGA0D
M76-M
Memory I/O
I/O Internal
Memory Clock I/O
Misc Bus
PCI-Express
Core
POWER
PART 7 OF 7
VGA0F
LVDS channel
M66 : NOT MOUNT
M66M
M76M
BL BRIGHTNESS CONTROL (PWM)
INSTALL LVDDR TO +3.3V FOR M76M (ALLOW STRAP FOR POSSIBLE LVDDR TO +1.8V)
INSTALL LVDDR TO+2.5V FOR M66M
INSTALL PCIE_VDDC TO +1.1V FOR M76M
INSTALL PCIE_VDDC TO +1.2V FOR M66M
ASUSTek COMPUTER INC
Title : ATI_M7X/66-M_POWER
Engineer: Jerry Mou
Project Name F7Sr
Rev 1.1
Size Custom
Date: 星期四, 五月 10, 2007
Sheet 27 of 95


R2802 56Ohm CLKA0
R2801 56Ohm CLKA0#
C2801 470PF/50V
GND
R2804 56Ohm CLKA1
R2803 56Ohm CLKA1#
C2802 470PF/50V
GND
25 GMA[15..0]
25 QSA[7..0]
25 QSA#[7..0]
25 DQMA#[7..0]
25 MDA[63..32]
25 MDA[31..0]
+VRAM
R2810 4.99KOhm
VERF4
C2840 0.1UF/16V
R2812 4.99KOhm
R2806 4.99KOhm
VERF3
C2820 0.1UF/16V
R2808 4.99KOhm
R2809 4.99KOhm
VERF2
C2839 0.1UF/16V
R2811 4.99KOhm
R2805 4.99KOhm
VERF1
C2819 0.1UF/16V
R2807 4.99KOhm
VRAMA0
25 CLKA0
25 CLKA0#
25 CKEA0
25 RASA0#
25 CASA0#
25 WEA0#
25 CSA0#
HYB18T256161AFL_25
L2801 120Ohm/100Mhz
C2809 0.1UF/16V c0402
C2810 1UF/16V
ODTA0 25
VRAMA2
25 CLKA1
25 CLKA1#
25 CKEA1
25 RASA1#
25 CASA1#
25 WEA1#
25 CSA1#
L2802 120Ohm/100Mhz
C2811 0.1UF/16V
C2812 1UF/16V
ODTA1 25
C2803 1000PF/50V
C2804 0.01UF/16V
C2805 10UF/10V
C2806 0.1UF/16V
C2807 0.1UF/16V
C2808 0.01UF/16V
C2813 1000PF/50V
C2814 0.01UF/16V
C2815 22UF/6.3V
C2816 0.1UF/16V
C2817 0.1UF/16V
C2818 0.1UF/16V
C2821 1000PF/50V
C2822 0.01UF/16V
C2823 22UF/6.3V
C2824 0.1UF/16V
C2825 0.1UF/16V
C2826 0.01UF/16V
C2827 1000PF/50V
C2828 0.01UF/16V
C2829 10UF/10V
C2830 0.1UF/16V
C2831 0.1UF/16V
C2832 0.1UF/16V
VRAMA1
L2803 120Ohm/100Mhz
C2834 0.1UF/16V
C2835 1UF/16V
ODTA0
VRAMA3
L2804 120Ohm/100Mhz
C2836 0.1UF/16V
C2837 1UF/16V
ODTA1
+0.9VS
RN2801A 56Ohm
RN2801B 56Ohm
RN2801C 56Ohm
RN2801D 56Ohm
RN2801E 56Ohm
RN2801F 56Ohm
RN2801G 56Ohm
RN2801H 56Ohm
C2833 0.1UF/16V
RN2802A 56Ohm
RN2802B 56Ohm
RN2802C 56Ohm
RN2802D 56Ohm
RN2802E 56Ohm
RN2802F 56Ohm
RN2802G 56Ohm
RN2802H 56Ohm
C2838 0.1UF/16V
RN2803A 56Ohm
RN2803B 56Ohm
RN2803C 56Ohm
RN2803D 56Ohm
RN2803E 56Ohm
RN2803F 56Ohm
RN2803G 56Ohm
RN2803H 56Ohm
CSA1# 56Ohm R2813
WEA0# 56Ohm R2814
RASA0# 56Ohm R2815
ASUSTek COMPUTER INC
Title : ATI_M7X/66-M_VRAM_A
Engineer: Jerry Mou
Size Custom
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 28 of 95


R2901 56Ohm / CLKB0
R2902 56Ohm / CLKB0#
C2901 470PF/50V
GND
R2904 56Ohm / CLKB1
R2903 56Ohm / CLKB1#
C2902 470PF/50V
GND
25 GMAB[15..0]
25 QSB[7..0]
25 QSB#[7..0]
25 DQMB#[7..0]
25 MDB[31..0]
25 MDB[63..32]
+VRAM
R2909 4.99KOhm
R2911 4.99KOhm
VERF8
C2939 0.1UF/16V
R2905 4.99KOhm
R2907 4.99KOhm
VERF7
C2919 0.1UF/16V
R2910 4.99KOhm
R2912 4.99KOhm
VERF6
C2940 0.1UF/16V
R2906 4.99KOhm
R2908 4.99KOhm
VERF5
C2920 0.1UF/16V
VRAMB0
25 CLKB0
25 CLKB0#
25 CKEB0
25 RASB0#
25 CASB0#
25 WEB0#
25 CSB0#
CK
CK#
CKE
RAS#
CAS#
WE#
CS#
NC/A13
BA0
BA1
NC/BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
LDQ0/DQ0
LDQ1/DQ1
LDQ2/DQ2
LDQ3/DQ3
LDQ4/DQ4
LDQ5/DQ5
LDQ6/DQ6
LDQ7/DQ7
UDQ0/DQ0
UDQ1/DQ1
UDQ2/DQ2
UDQ3/DQ3
UDQ4/DQ4
UDQ5/DQ5
UDQ6/DQ6
UDQ7/DQ7
UDQS
UDQS#
LDQS
LDQS#
UDM
LDM
VREF
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDL
VDD1
VDD2
VDD3
VDD4
VDD5
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSSQ9
VSSQ10
VSSDL
VSS1
VSS2
VSS3
VSS4
VSS5
ODT
NC1
NC2
NC3
NC4
DQMB#1
DQMB#3
VERF5
+VRAM
L2901 120Ohm/100Mhz
C2909 0.1UF/16V
C2912 1UF/16V
GND
ODTB0 25
GMAB14
GMAB15
GMAB0
GMAB1
GMAB2
GMAB3
GMAB4
GMAB5
GMAB6
GMAB7
GMAB8
GMAB9
GMAB10
GMAB11
GMAB12
MDB27
MDB31
MDB24
MDB29
MDB30
MDB26
MDB28
MDB25
MDB13
MDB10
MDB12
MDB11
MDB8
MDB15
MDB9
MDB14
QSB1
QSB#1
QSB3
QSB#3
HYB18T256161AFL_25
VRAMB3
25 CLKB1
25 CLKB1#
25 CKEB1
25 RASB1#
25 CASB1#
25 WEB1#
25 CSB1#
DQMB#7
DQMB#4
VERF7
L2902 120Ohm/100Mhz
C2910 0.1UF/16V
C2911 1UF/16V
ODTB1 25
MDB35
MDB36
MDB33
MDB38
MDB37
MDB32
MDB39
MDB34
MDB59
MDB62
MDB58
MDB63
MDB61
MDB56
MDB60
MDB57
QSB7
QSB#7
QSB4
QSB#4
VRAMB1
DQMB#0
DQMB#2
VERF6
L2903 120Ohm/100Mhz
C2934 0.1UF/16V
C2936 1UF/16V
ODTB0
MDB17
MDB20
MDB16
MDB23
MDB21
MDB18
MDB22
MDB19
MDB1
MDB5
MDB3
MDB6
MDB7
MDB0
MDB4
MDB2
QSB0
QSB#0
QSB2
QSB#2
VRAMB2
DQMB#6
DQMB#5
VERF8
L2904 120Ohm/100Mhz
C2935 0.1UF/16V
C2937 1UF/16V
ODTB1
MDB47
MDB42
MDB45
MDB43
MDB40
MDB46
MDB41
MDB44
MDB52
MDB50
MDB55
MDB51
MDB49
MDB54
MDB48
MDB53
QSB6
QSB#6
QSB5
QSB#5
C2903 1000PF/50V
C2904 0.01UF/16V
C2905 10UF/10V
C2906 0.1UF/16V
C2907 0.1UF/16V
C2908 0.01UF/16V
C2913 1000PF/50V
C2914 0.01UF/16V
C2915 22UF/6.3V
C2916 0.1UF/16V
C2917 0.1UF/16V
C2918 0.1UF/16V
C2921 1000PF/50V
C2922 0.01UF/16V
C2923 22UF/6.3V
C2924 0.1UF/16V
C2925 0.1UF/16V
C2926 0.01UF/16V
C2927 1000PF/50V
C2928 0.01UF/16V
C2929 10UF/10V
C2930 0.1UF/16V
C2931 0.1UF/16V
C2932 0.1UF/16V
+0.9VS
RASB0# RN2901A 56Ohm
CASB0# RN2901B 56Ohm
ODTB0 RN2901C 56Ohm
CKEB0 RN2901D 56Ohm
GMAB9 RN2901E 56Ohm
GMAB6 RN2901F 56Ohm
GMAB0 RN2901G 56Ohm
GMAB8 RN2901H 56Ohm
C2933 0.1UF/16V
GMAB3 RN2902A 56Ohm
GMAB15 RN2902B 56Ohm
GMAB7 RN2902C 56Ohm
GMAB14 RN2902D 56Ohm
GMAB10 RN2902E 56Ohm
GMAB12 RN2902F 56Ohm
GMAB11 RN2902G 56Ohm
GMAB5 RN2902H 56Ohm
C2938 0.1UF/16V
GMAB2 RN2903A 56Ohm
GMAB4 RN2903B 56Ohm
GMAB1 RN2903C 56Ohm
ODTB1 RN2903D 56Ohm
CKEB1 RN2903E 56Ohm
CSB1# RN2903F 56Ohm
WEB1# RN2903G 56Ohm
CASB1# RN2903H 56Ohm
CSB0# 56Ohm R2913
RASB1# 56Ohm R2914
WEB0# 56Ohm R2915
ASUSTek COMPUTER INC
Title : ATI_M7X/66-M_VRAM_B
Engineer: Jerry Mou
Size Custom
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 29 of 95



ASUSTeK COMPUTER INC	Title : Blank Page	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 30 of 95	

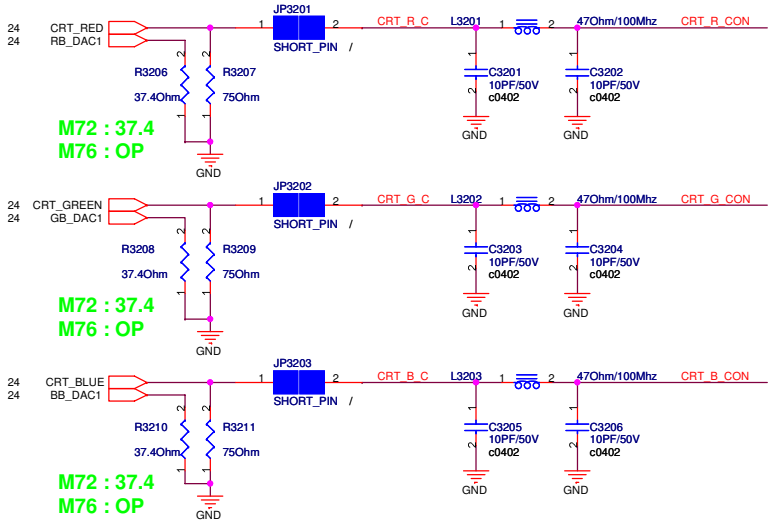
Title : Blank Page

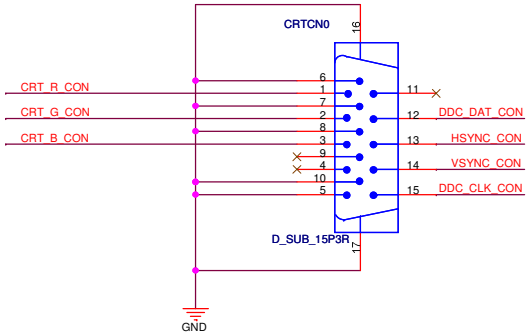
ASUSTeK COMPUTER INC

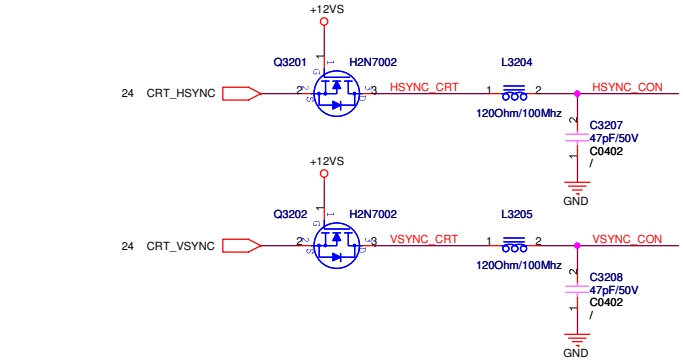
Engineer: Jerry Mou

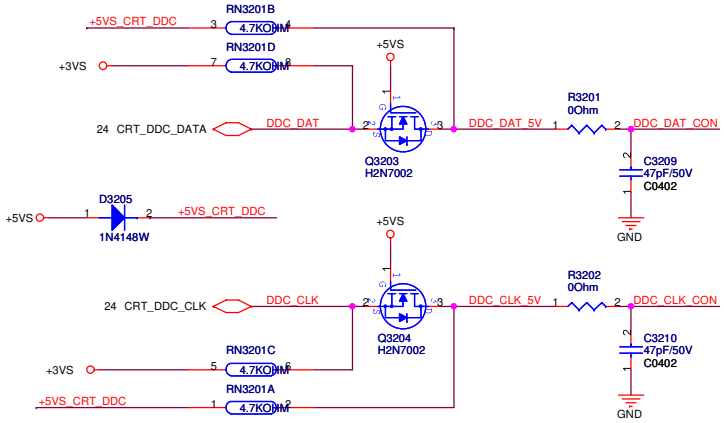
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 31 of 95

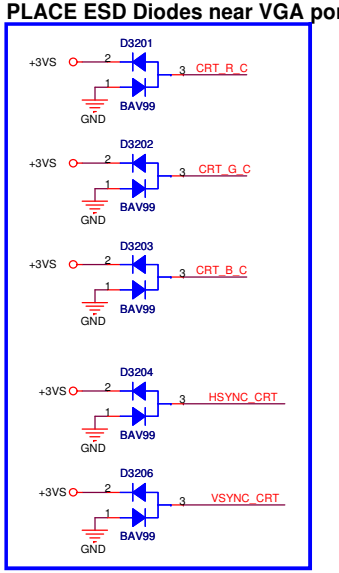








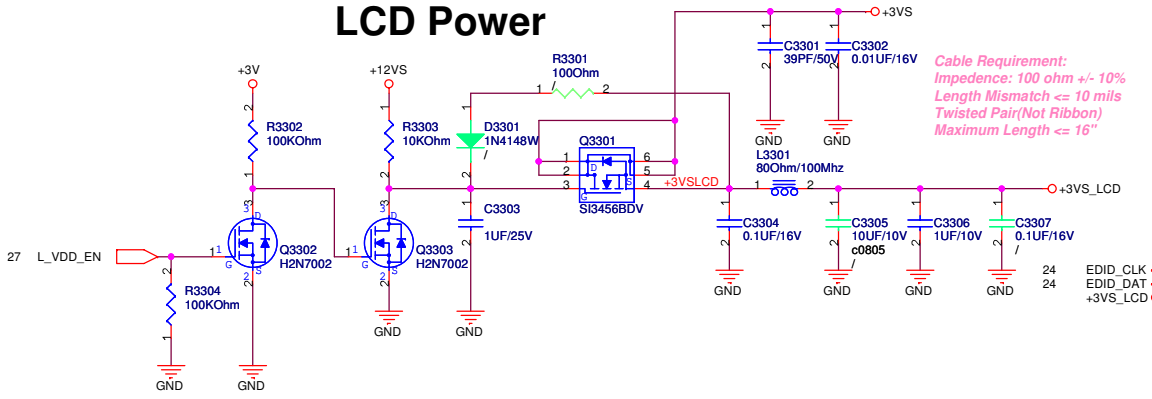
PLACE ESD Diodes near VGA port



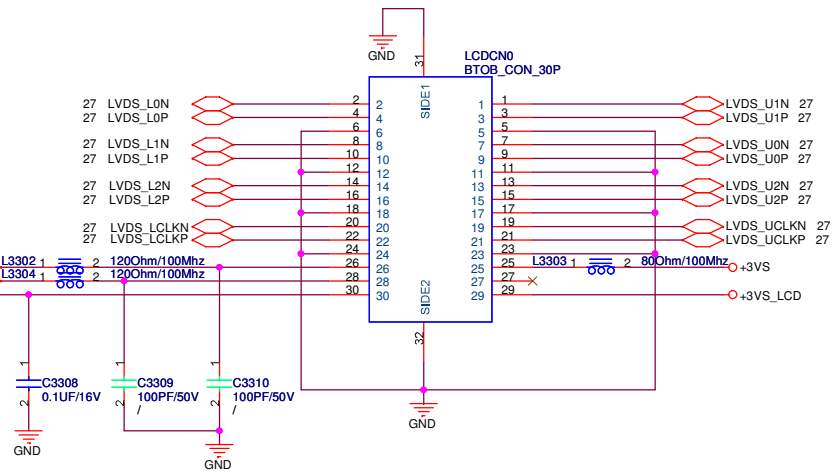
ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 32 of 95	

LCD Backlight Control

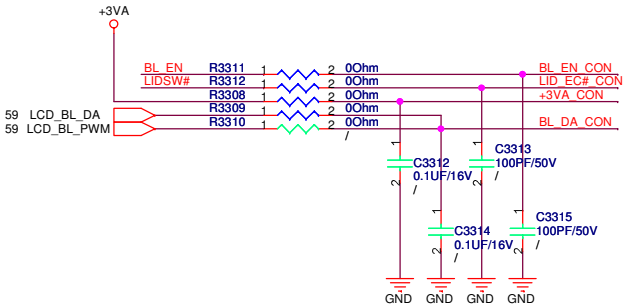
LCD Power

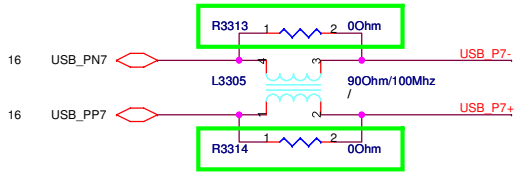


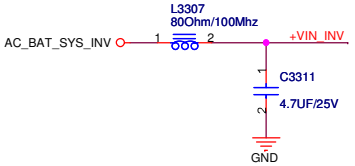
LCD LVDS Interface

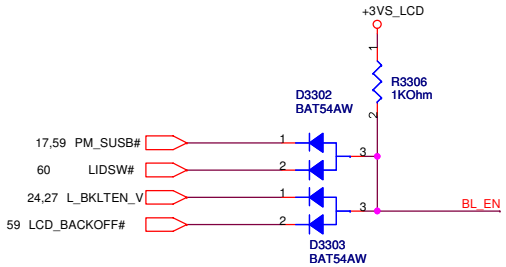


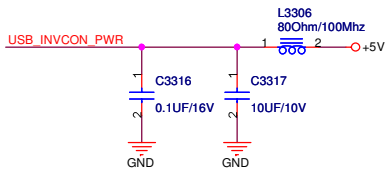
INVERTER
Interface/Speaker CONN.

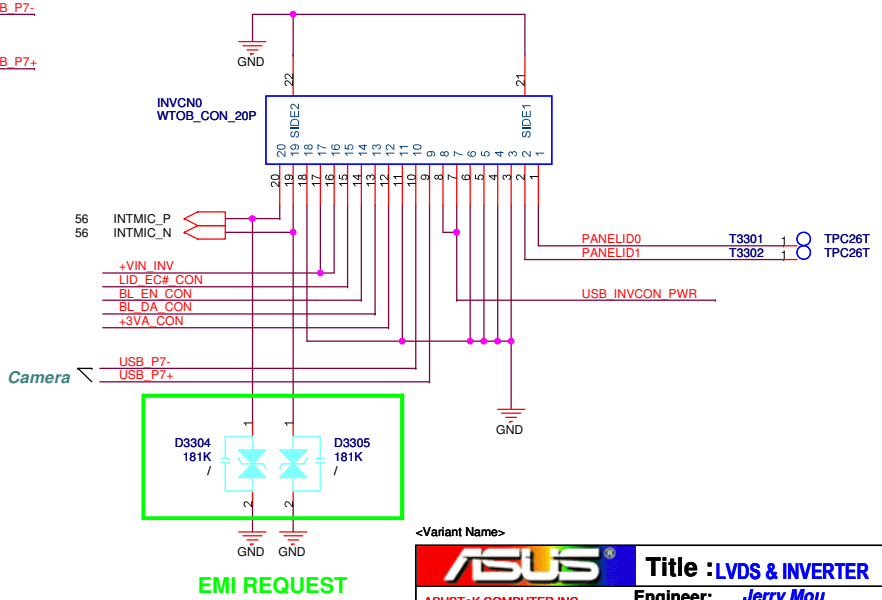












<Variant Name>

ASUSTeK COMPUTER INC

Title : LVDS & INVERTER

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 33 of 95

Title : Blank Page

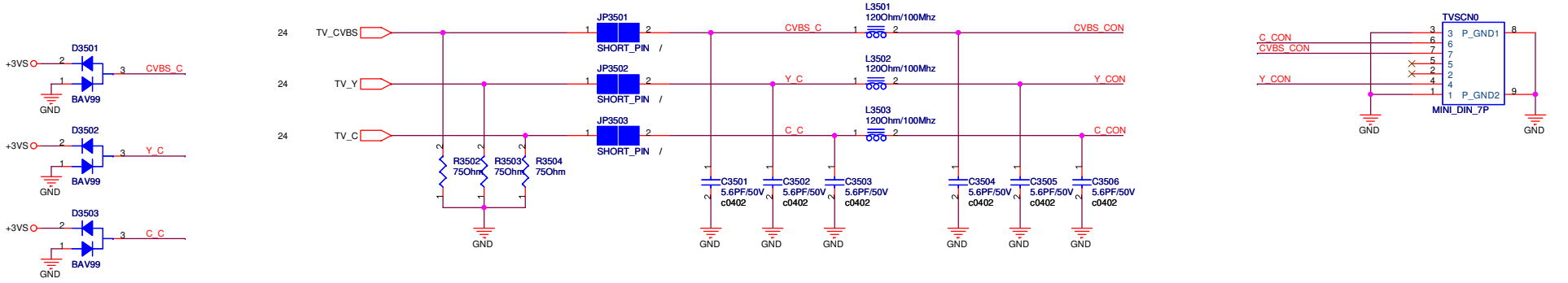
ASUSTeK COMPUTER INC

Engineer: Jerry Mou

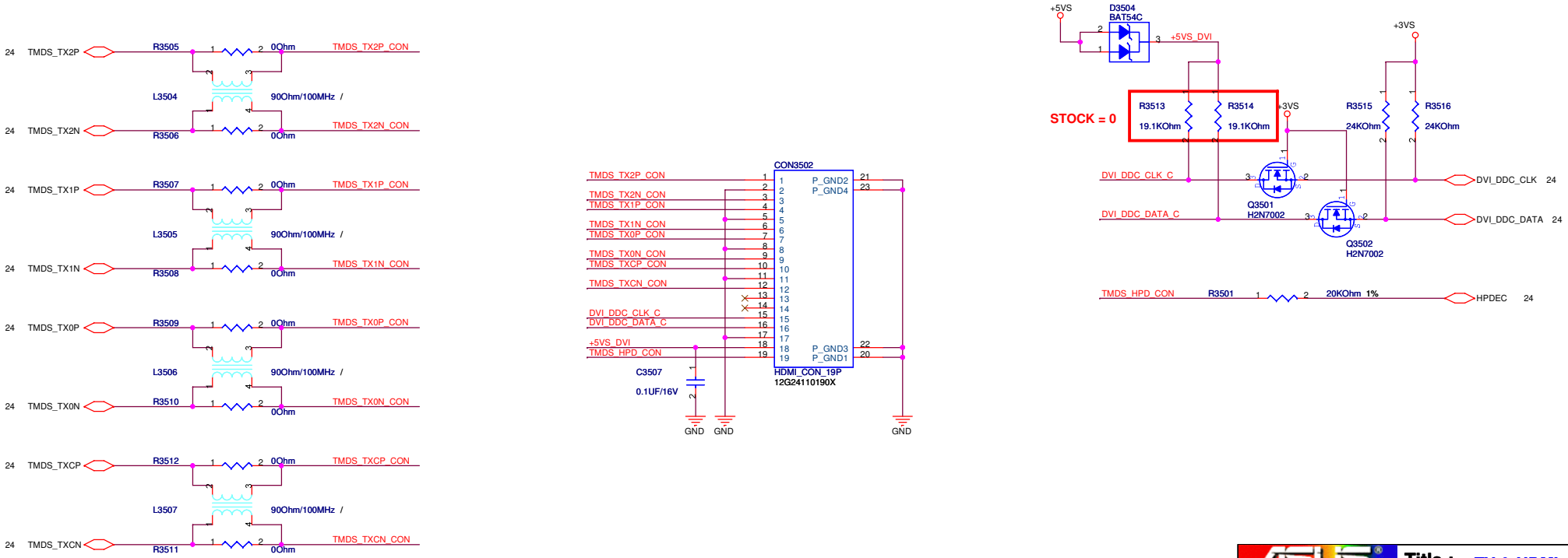
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 34 of 95

TV OUT



HDMI



ASUSTeK COMPUTER INC	Title : TV & HDMI	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 35 of 95	

Title : Blank Page

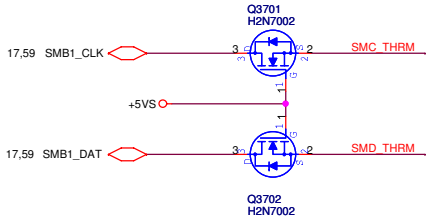
ASUSTeK COMPUTER INC

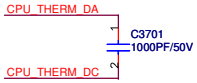
Engineer: Jerry Mou

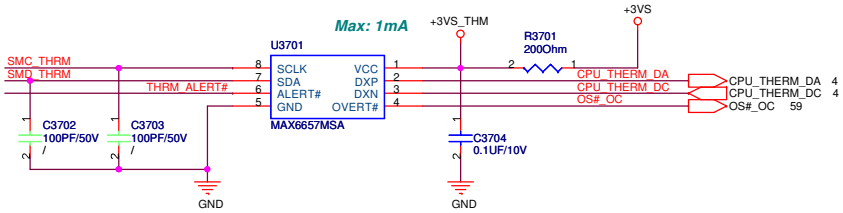
Size	Project Name	Rev
Custom	F7Sr	1.1

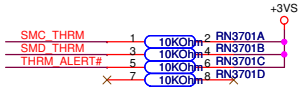
Date: 星期四, 五月 10, 2007

Thermal Sensor

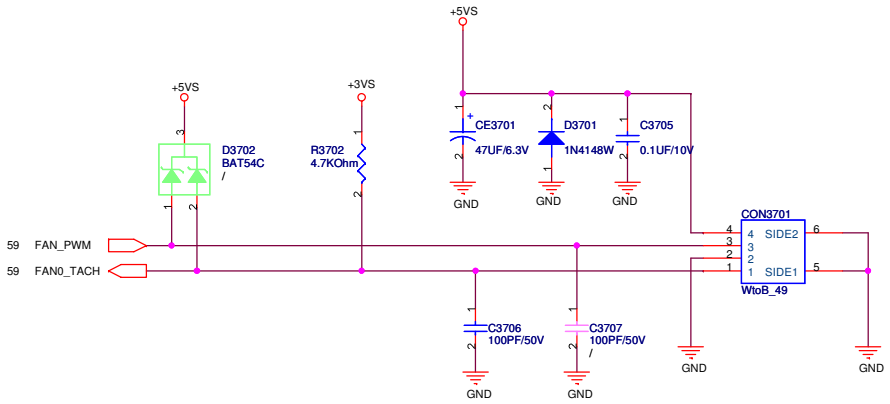








DC FAN Control



ASUSTeK COMPUTER INC. NB1	Title : THER SENSOR & FAN	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 37 of 95	

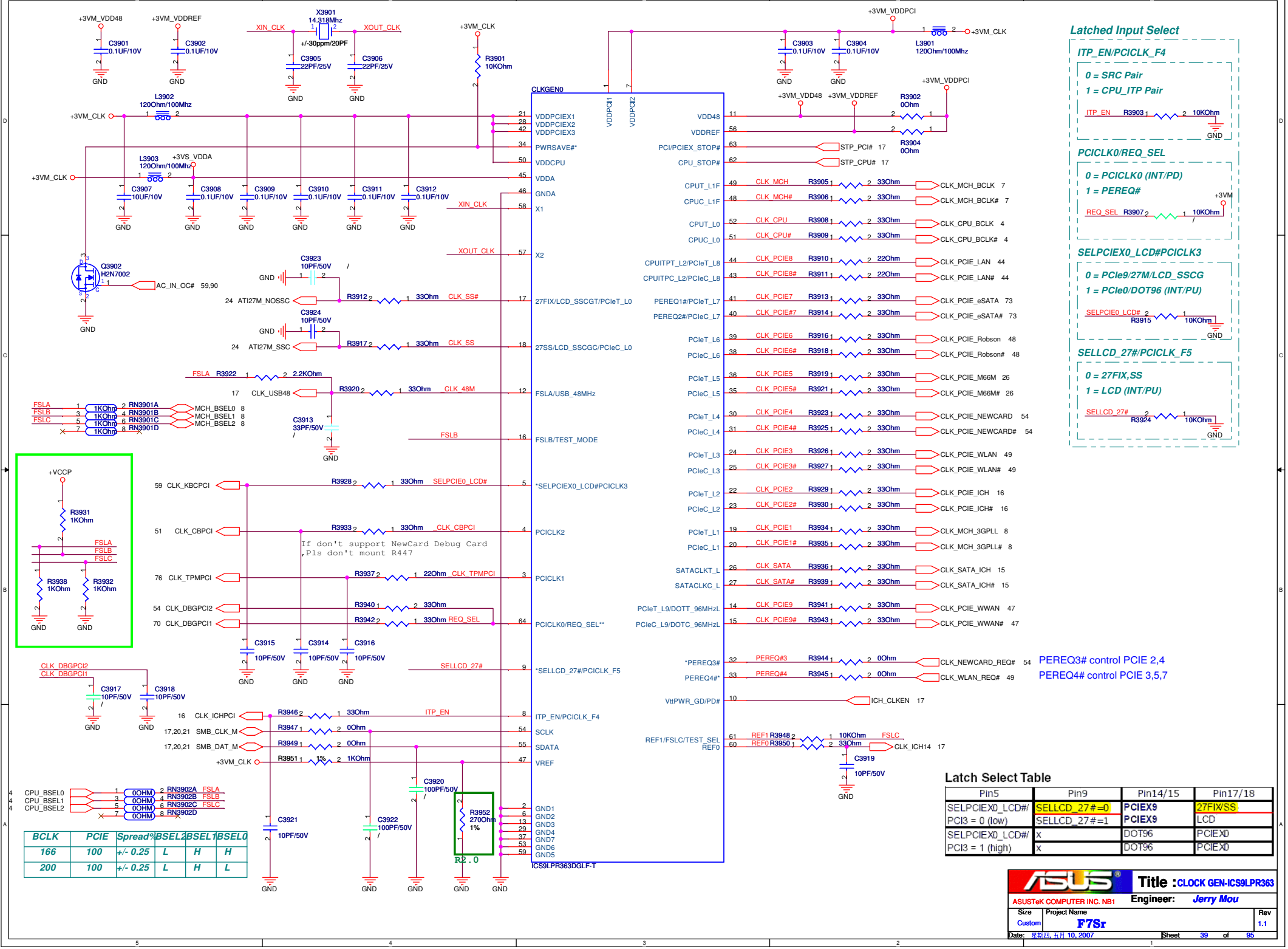
Title : Blank Page

ASUSTeK COMPUTER INC

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 38 of 95


CLKGEN0
ICS9LPR363DGLF-T
X3901 14.318Mhz
+/-30ppm/20PF
XIN_CLK
XOUT_CLK
+3VM_CLK
+3VM_VDD48
+3VM_VDDREF
+3VM_VDDPCI
+3VS_VDDA
C3901 0.1UF/10V
C3902 0.1UF/10V
C3903 0.1UF/10V
C3904 0.1UF/10V
C3905 22PF/25V
C3906 22PF/25V
L3901 120Ohm/100Mhz
L3902 120Ohm/100Mhz
L3903 120Ohm/100Mhz
R3901 10KOhm
R3902 0Ohm
R3903 10KOhm
R3904 0Ohm
C3907 10UF/10V
C3908 0.1UF/10V
C3909 0.1UF/10V
C3910 0.1UF/10V
C3911 0.1UF/10V
C3912 0.1UF/10V
Q3902 H2N7002
AC_IN_OC# 59,90
C3923 10PF/50V
C3924 10PF/50V
R3912 33Ohm CLK_SS#
R3917 33Ohm CLK_SS
R3922 2.2KOhm
R3920 33Ohm CLK_48M
C3913 33PF/50V
FSLA R3901A 1KOhm
FSLB R3901B 1KOhm
FSLC R3901C 1KOhm
R3901D 1KOhm
MCH_BSEL0 8
MCH_BSEL1 8
MCH_BSEL2 8
+VCCP
R3931 1KOhm
R3938 1KOhm
R3932 1KOhm
R3928 33Ohm SELPCIE0_LCD#
R3933 33Ohm CLK_CBPCI
If don't support NewCard Debug Card
,Pls don't mount R447
R3937 22Ohm CLK_TPMPCI
R3940 33Ohm
R3942 33Ohm REQ_SEL
C3915 10PF/50V
C3914 10PF/50V
C3916 10PF/50V
C3917 10PF/50V
C3918 10PF/50V
R3946 33Ohm ITP_EN
R3947 0Ohm
R3949 0Ohm
R3951 1% 1KOhm
C3920 100PF/50V
C3921 10PF/50V
C3922 100PF/50V
R3952 270Ohm 1%
R2.0
CPU_BSEL0 0OHM RN3902A FSLA
CPU_BSEL1 0OHM RN3902B FSLB
CPU_BSEL2 0OHM RN3902C FSLC
0OHM RN3902D
BCLK PCIE Spread% BSEL2 BSEL1 BSEL0
166 100 +/- 0.25 L H H
200 100 +/- 0.25 L H L
R3905 33Ohm CLK_MCH_BCLK
R3906 33Ohm CLK_MCH_BCLK#
R3908 33Ohm CLK_CPU_BCLK
R3909 33Ohm CLK_CPU_BCLK#
R3910 22Ohm CLK_PCIE_LAN
R3911 22Ohm CLK_PCIE_LAN#
R3913 33Ohm CLK_PCIE_eSATA
R3914 33Ohm CLK_PCIE_eSATA#
R3916 33Ohm CLK_PCIE_Robson
R3918 33Ohm CLK_PCIE_Robson#
R3919 33Ohm CLK_PCIE_M66M
R3921 33Ohm CLK_PCIE_M66M#
R3923 33Ohm CLK_PCIE_NEWCARD
R3925 33Ohm CLK_PCIE_NEWCARD#
R3926 33Ohm CLK_PCIE_WLAN
R3927 33Ohm CLK_PCIE_WLAN#
R3929 33Ohm CLK_PCIE_ICH
R3930 33Ohm CLK_PCIE_ICH#
R3934 33Ohm CLK_MCH_3GPLL
R3935 33Ohm CLK_MCH_3GPLL#
R3936 33Ohm CLK_SATA_ICH
R3939 33Ohm CLK_SATA_ICH#
R3941 33Ohm CLK_PCIE_WWAN
R3943 33Ohm CLK_PCIE_WWAN#
R3944 0Ohm CLK_NEWCARD_REQ#
R3945 0Ohm CLK_WLAN_REQ#
ICH_CLKEN
R3948 10KOhm FSLC
R3950 33Ohm CLK_ICH14
C3919 10PF/50V
STP_PCI#
STP_CPU#
Latched Input Select
ITP_EN/PCICLK_F4
0 = SRC Pair
1 = CPU_ITP Pair
PCICLK0/REQ_SEL
0 = PCICLK0 (INT/PD)
1 = PEREQ#
SELPCIEX0_LCD#PCICLK3
0 = PCIe9/27M/LCD_SSCG
1 = PCIe0/DOT96 (INT/PU)
SELLCD_27#/PCICLK_F5
0 = 27FIX,SS
1 = LCD (INT/PU)
PEREQ3# control PCIE 2,4
PEREQ4# control PCIE 3,5,7
Latch Select Table
Pin5 | Pin9 | Pin14/15 | Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low) | SELLCD_27#=0 | PCIEX9 | 27FIX/SS
SELLCD_27#=1 | PCIEX9 | LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high) | x | DOT96 | PCIEX0
x | DOT96 | PCIEX0
Title : CLOCK GEN-ICS9LPR363
ASUSTeK COMPUTER INC. NB1
Engineer: Jerry Mou
Size Custom
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 39 of 95

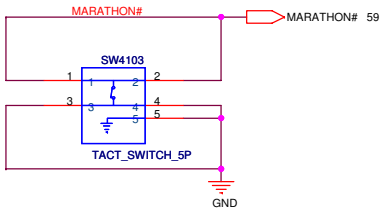
Title : Blank Page

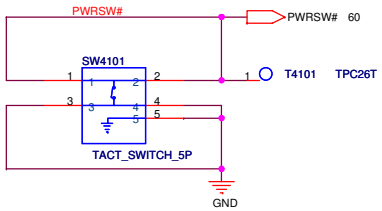
ASUSTeK COMPUTER INC

Engineer: Jerry Mou

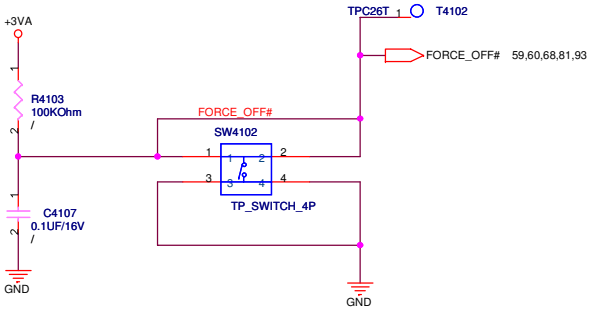
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 40 of 95

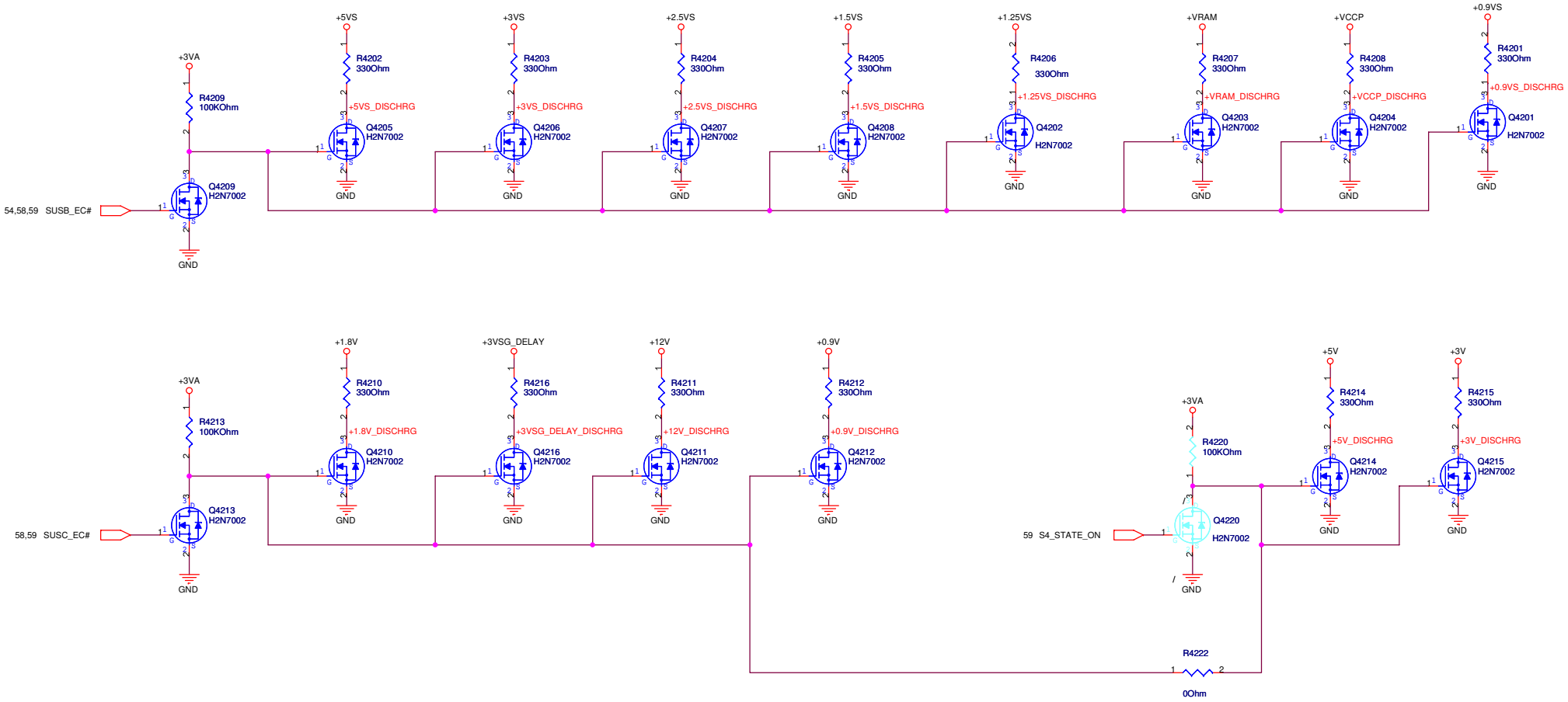




SHUT_DOWN#



ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 41 of 95	



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 42 of 95	

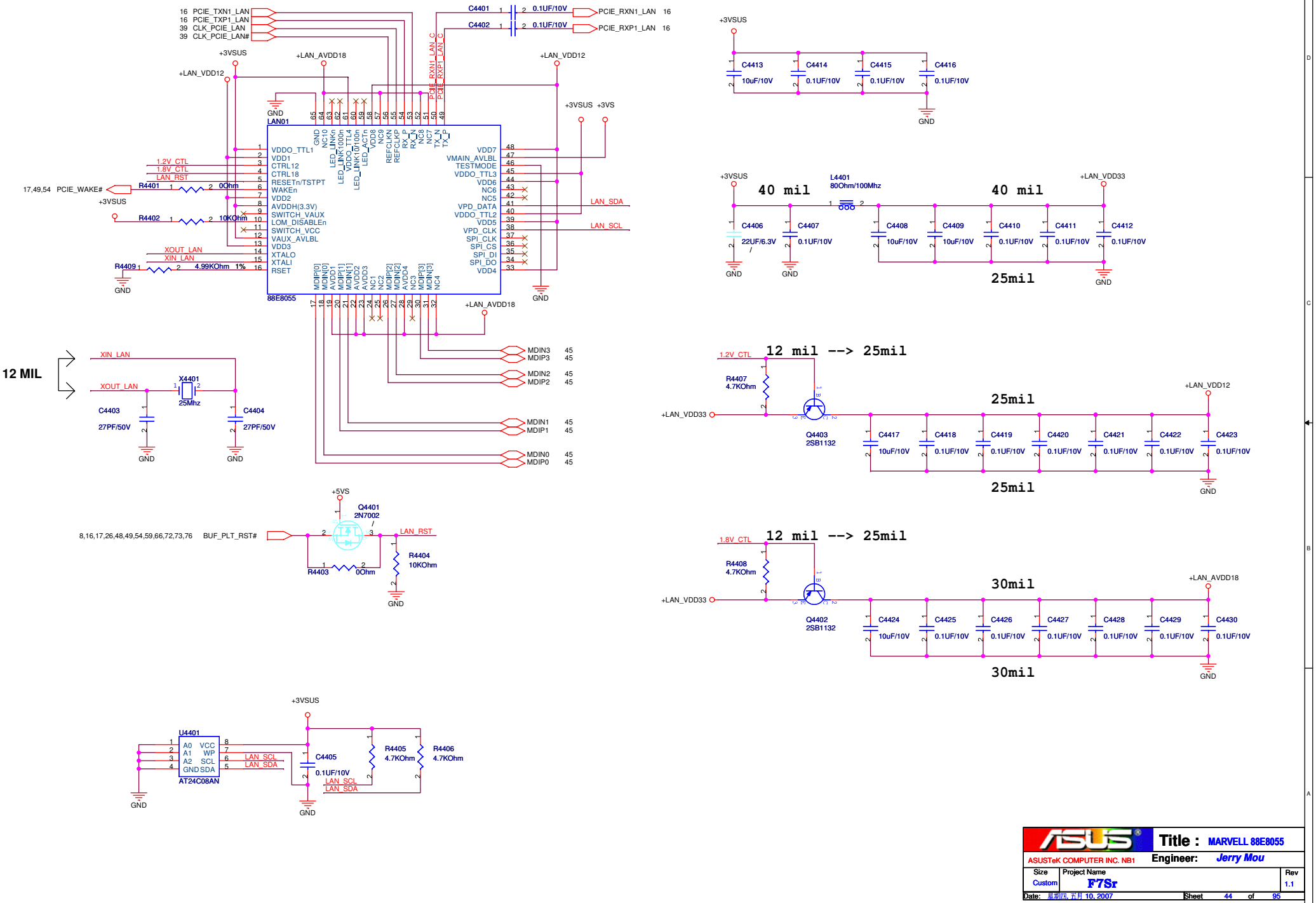
Title : Blank Page

ASUSTeK COMPUTER INC

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

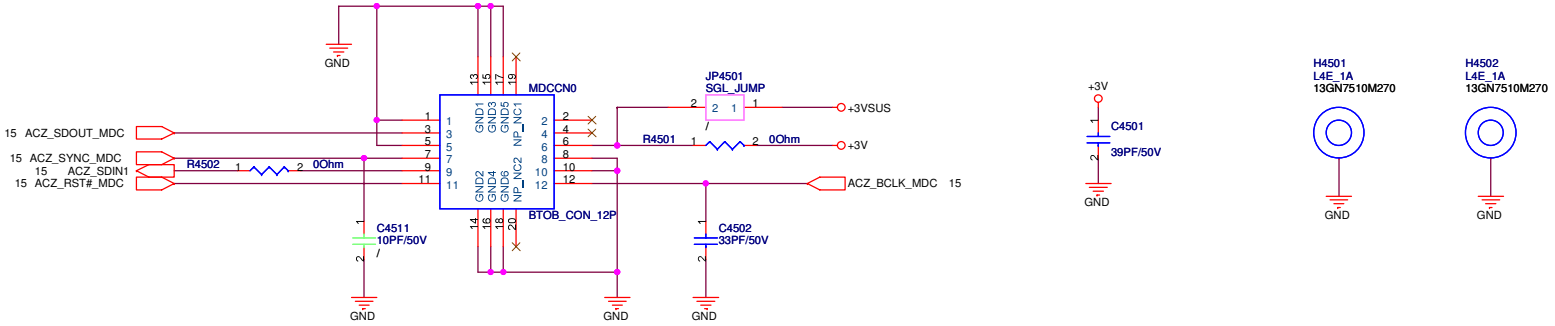
Date: 星期四, 五月 10, 2007 Sheet 43 of 95



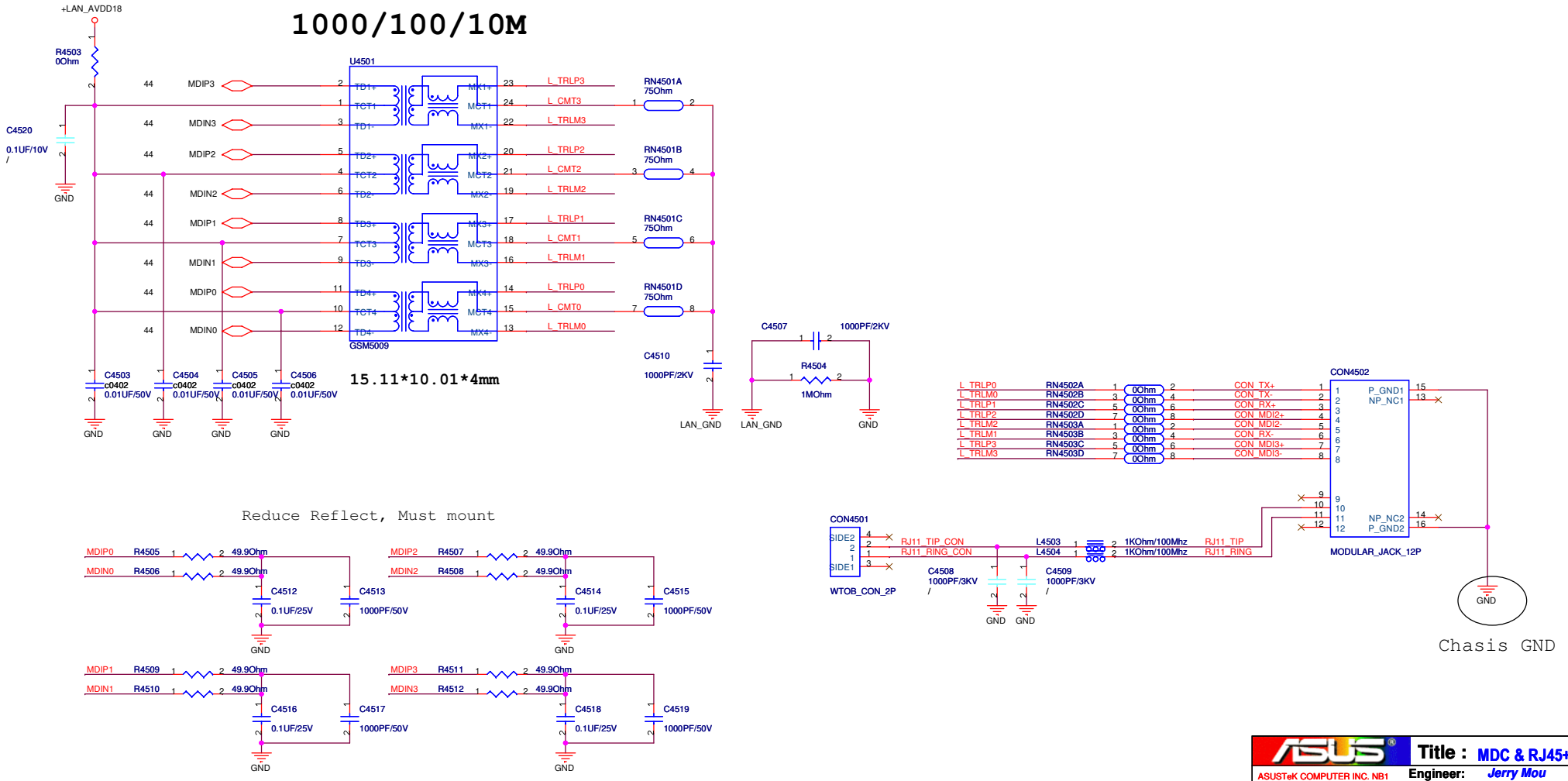
Title :	MARVELL 88E8055
ASUSTeK COMPUTER INC. NB1	Engineer: Jerry Mou
Size: Custom	Project Name: F7Sr
Rev: 1.1	
Date: 星期四, 五月 10, 2007	Sheet 44 of 95

Change to
13GN7510M270

MDC CONN.



LAN CONN.



ASUSTeK COMPUTER INC. NB1	Title : MDC & RJ45+11		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 45 of 95		

Title : Blank Page

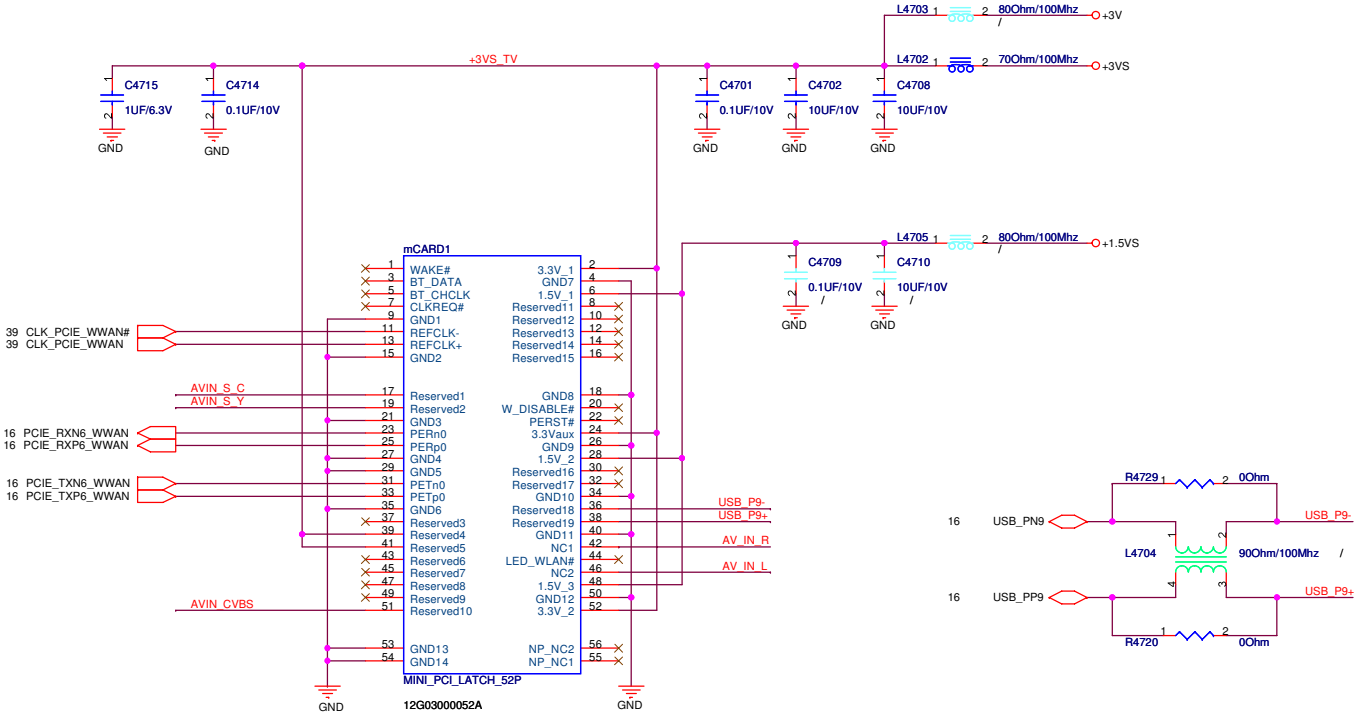
ASUSTeK COMPUTER INC

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007

Sheet 46 of 95

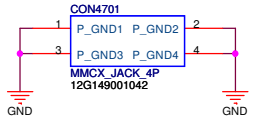


H = 5.2mm

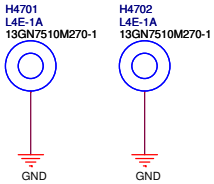
FOR TV TUNER

(UWB OPTION)

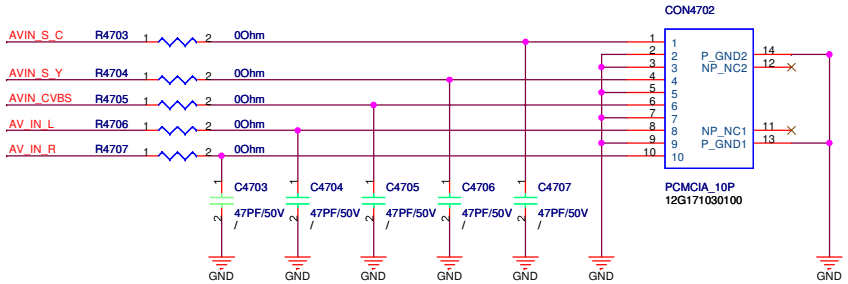
TV Conn.



ME P/N : 14G152075000

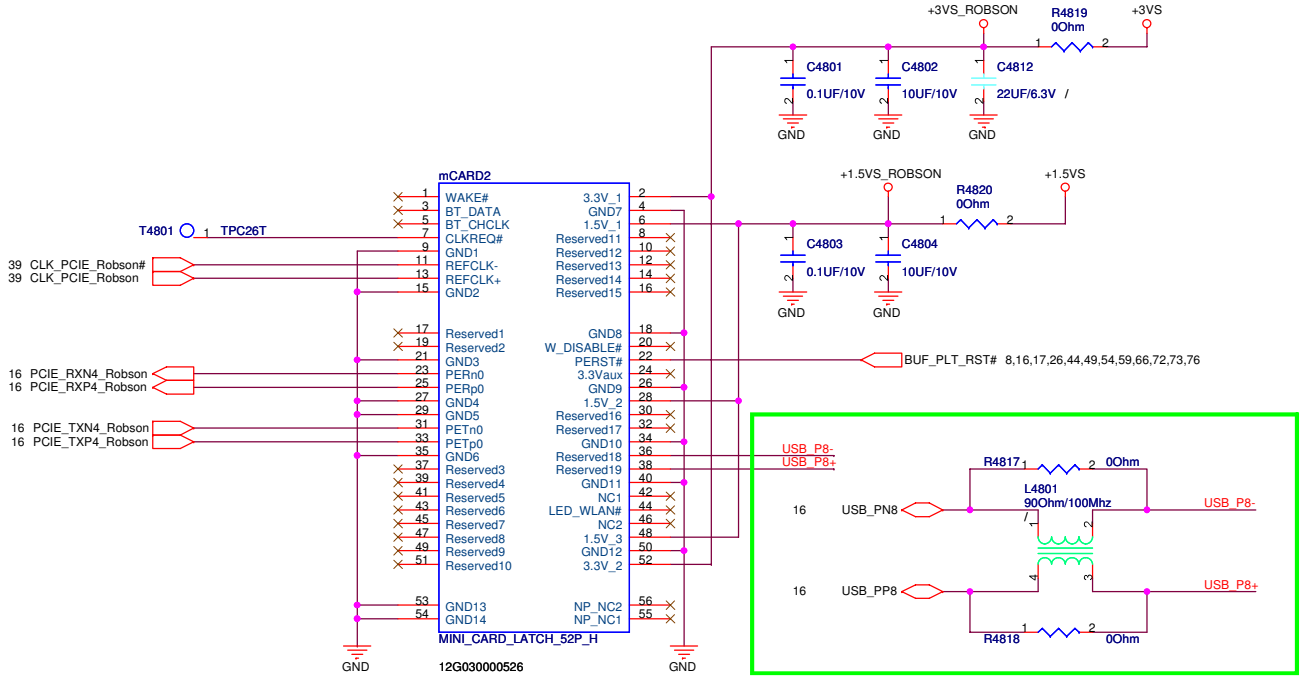


H = 3.0mm



<Variant Name>

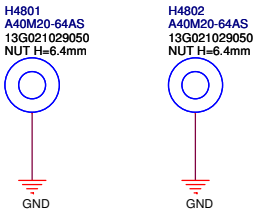
ASUSTeK COMPUTER INC. NB1	Title : MINI CARD (TV)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 47 of 95	



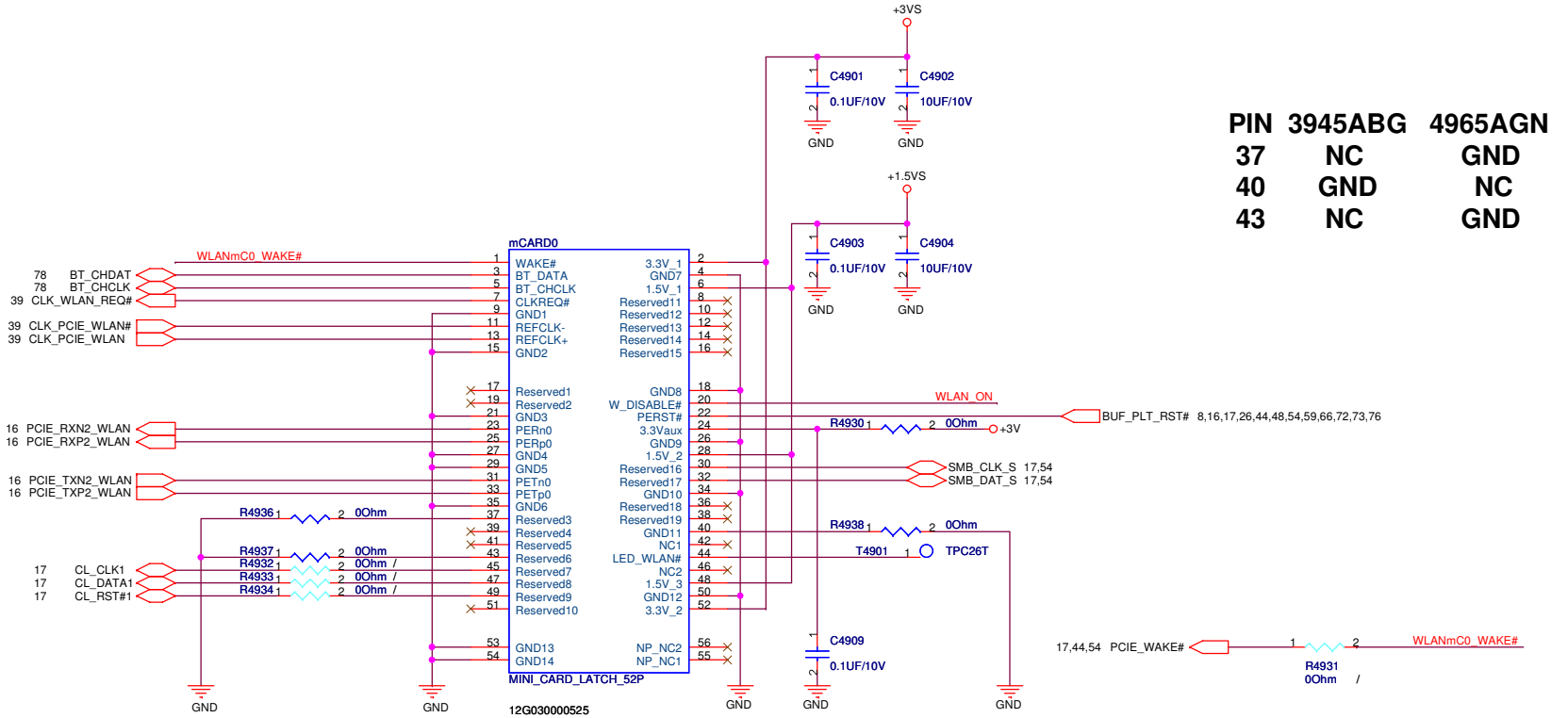
RESERVED

FOR ROBSON

H=9.0mm



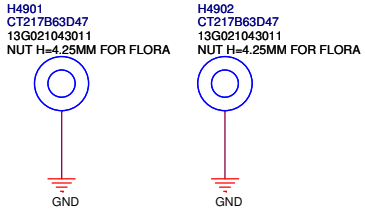
ASUSTeK COMPUTER INC. NB1	Title : MINI CARD-Robson	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 48 of 95	

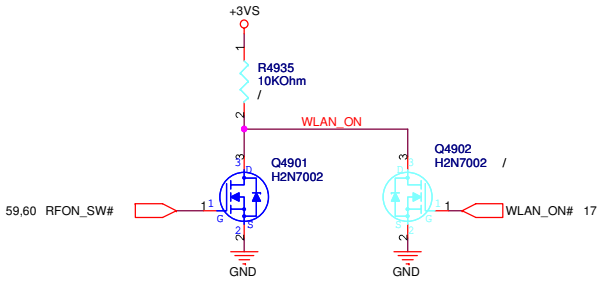


PIN	3945ABG	4965AGN
37	NC	GND
40	GND	NC
43	NC	GND

H = 6.75mm

FOR WLAN





ASUSTeK COMPUTER INC. NB1	Title : MINI CARD-Kedron		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 49 of 95		

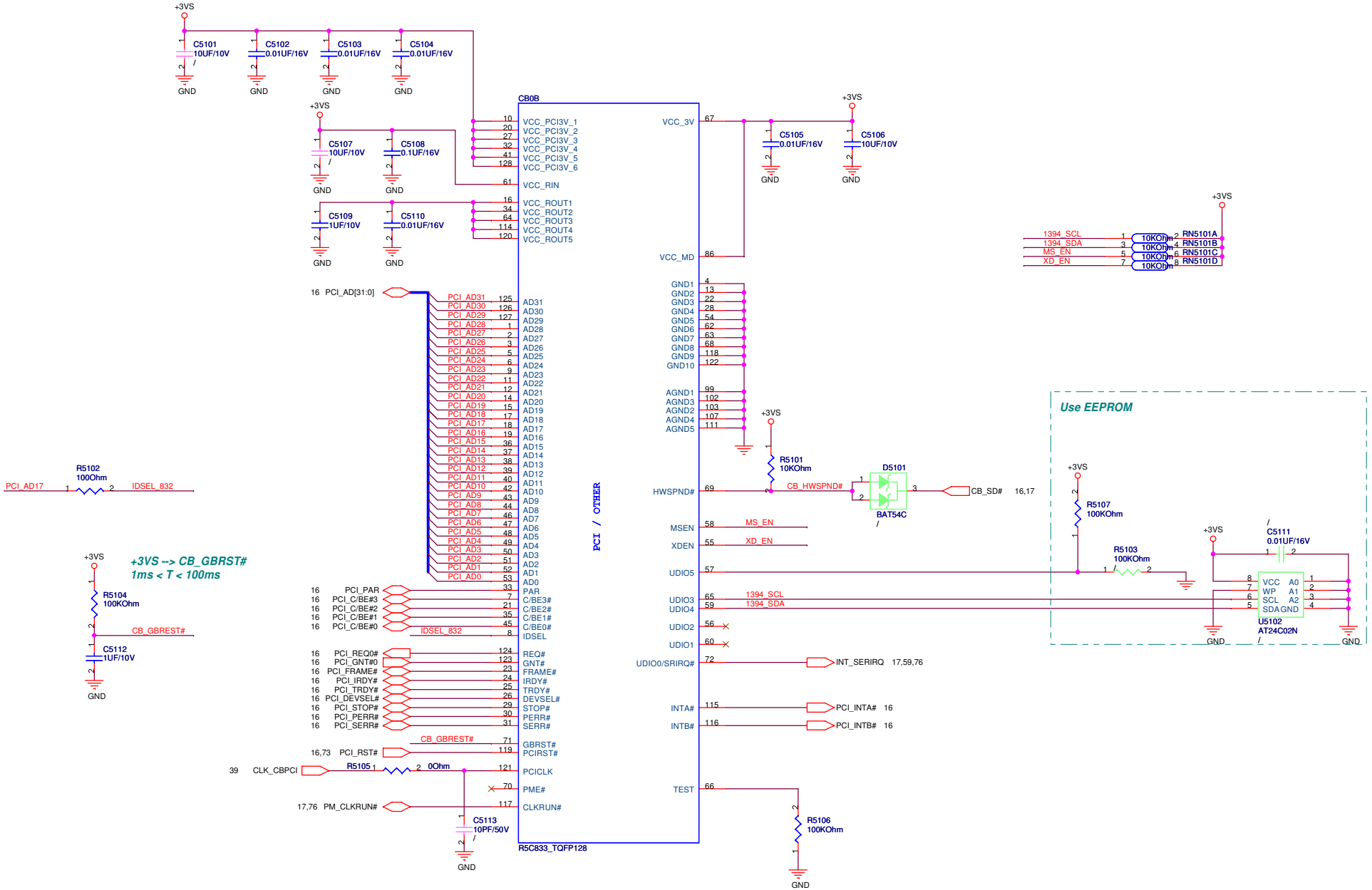
Title : Blank Page

ASUSTeK COMPUTER INC

Engineer: Jerry Mou

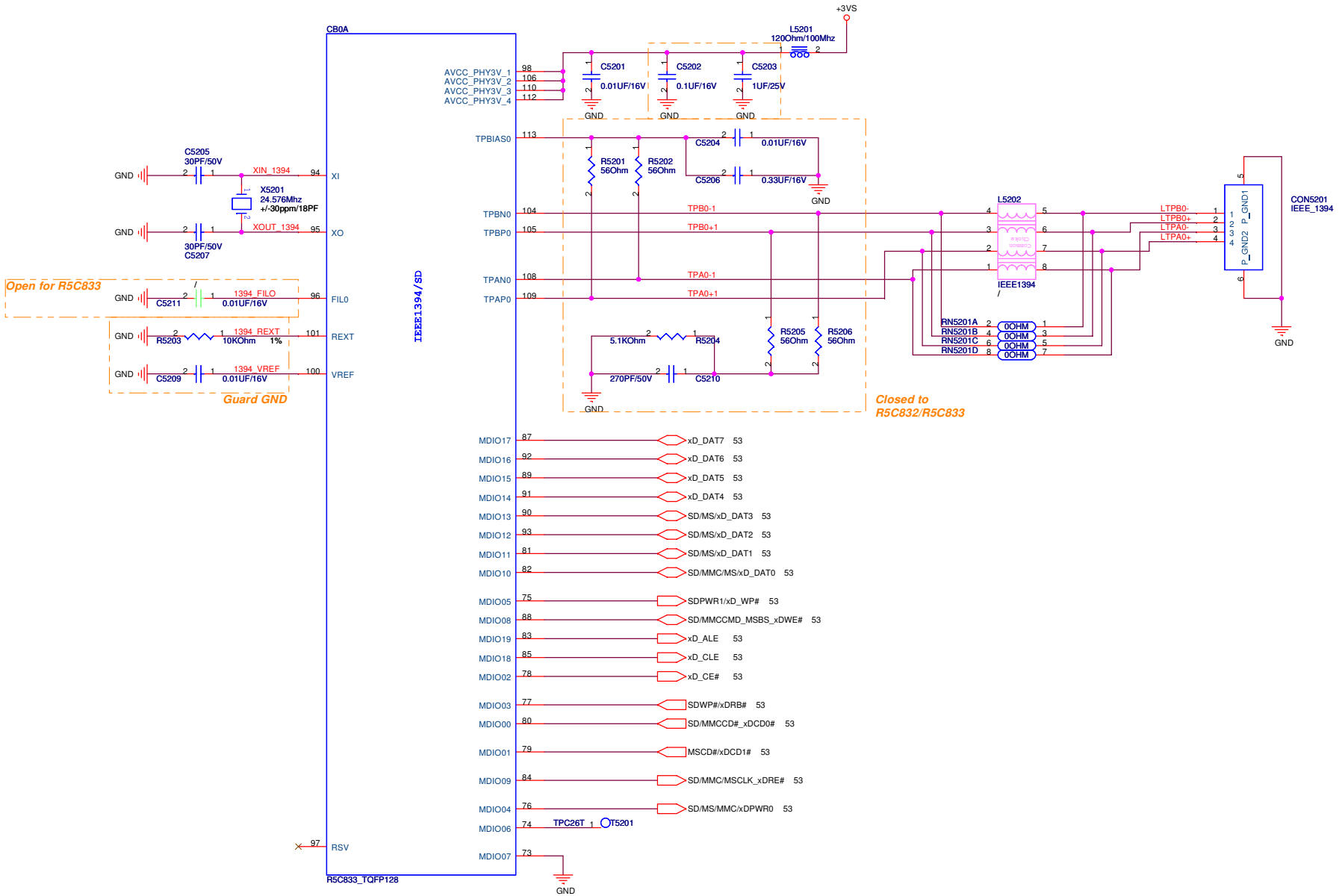
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 50 of 95



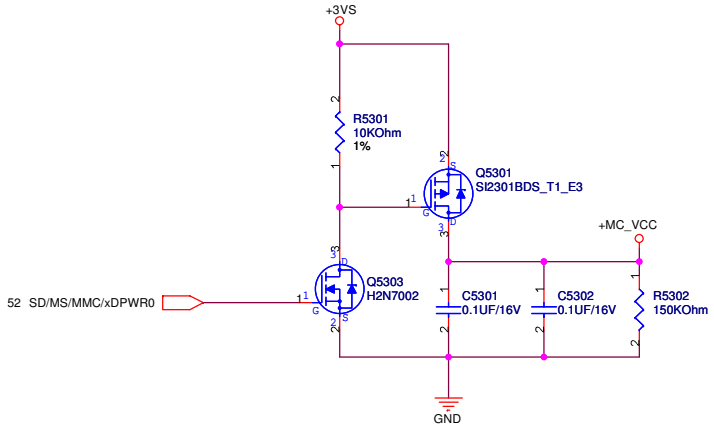
<Variant Name>

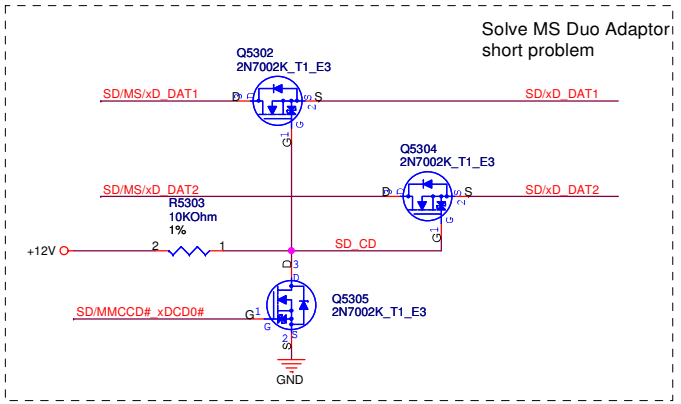
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C833(1)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 51 of 95	

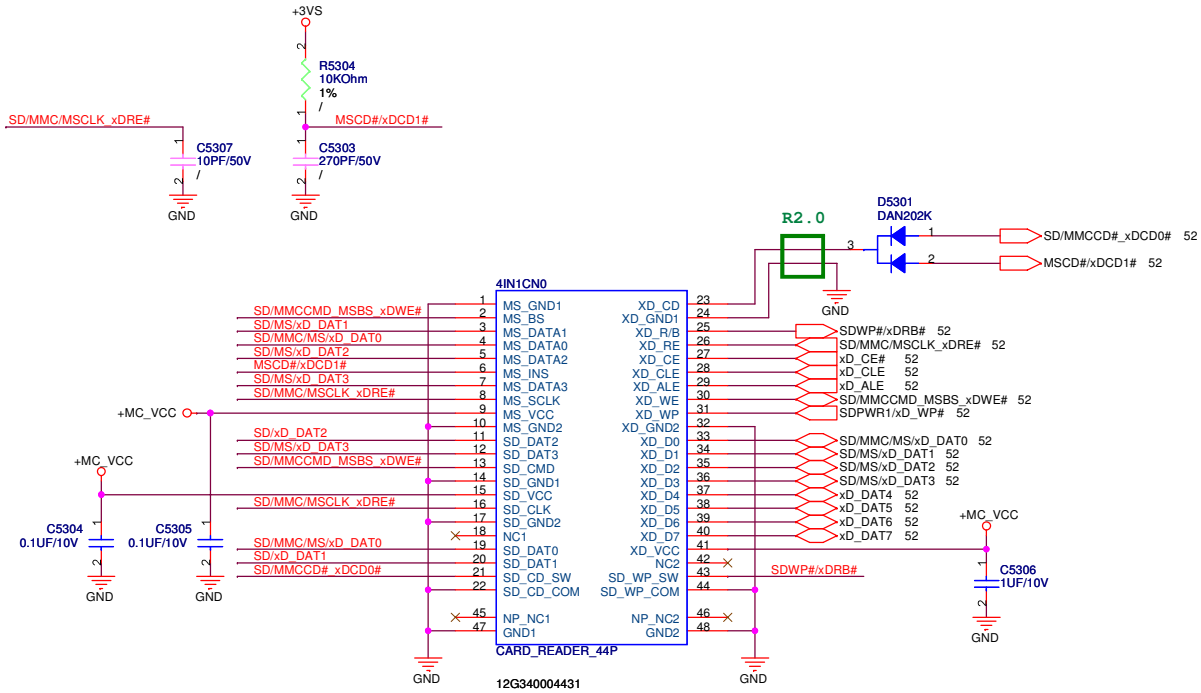


<Variant Name>

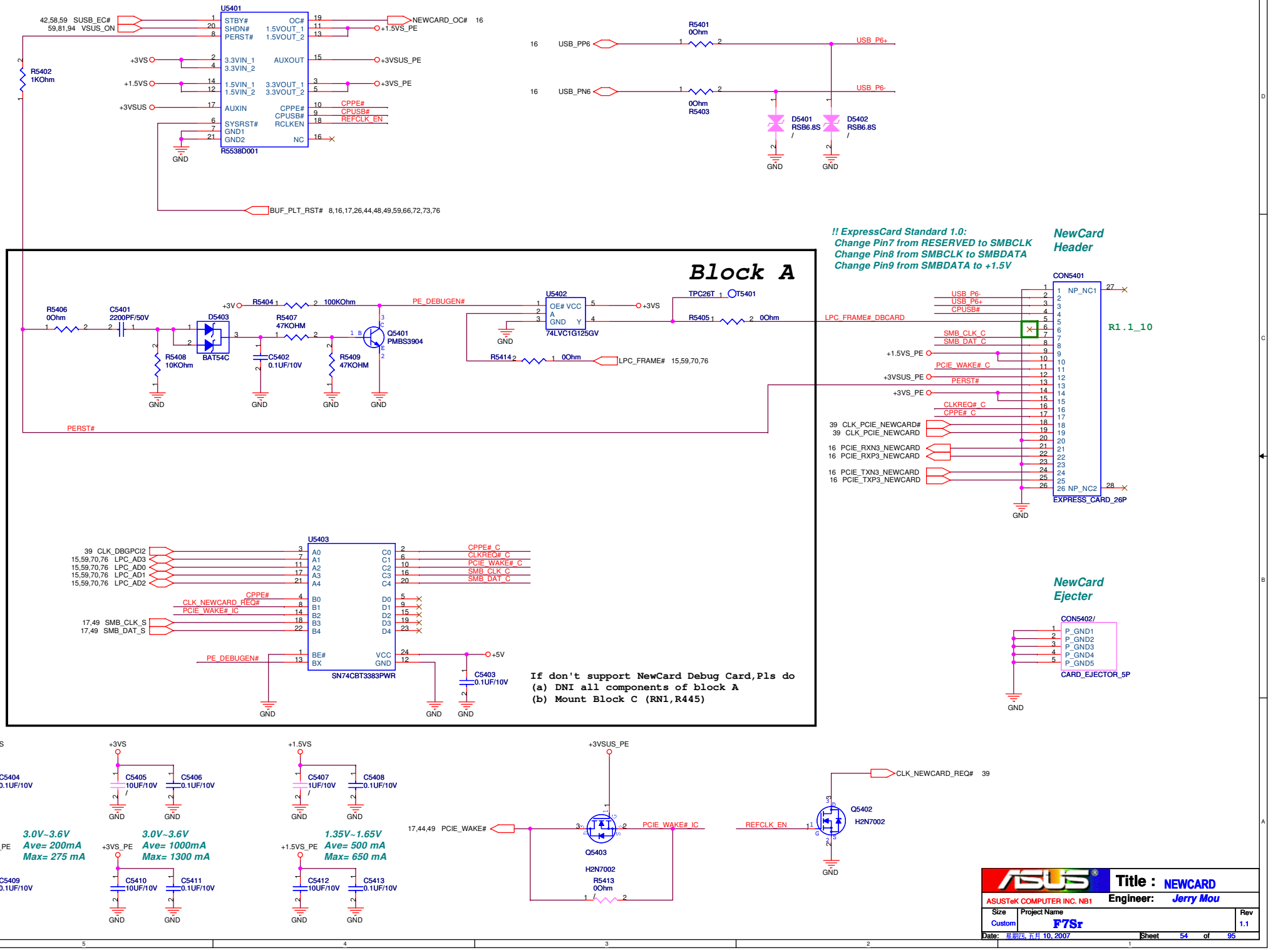
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C833(2)	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 52 of 95	







ASUSTeK COMPUTER INC	Title : 4 in 1 CARD READER	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 53 of 95	



ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 54 of 95	

<Variant Name>

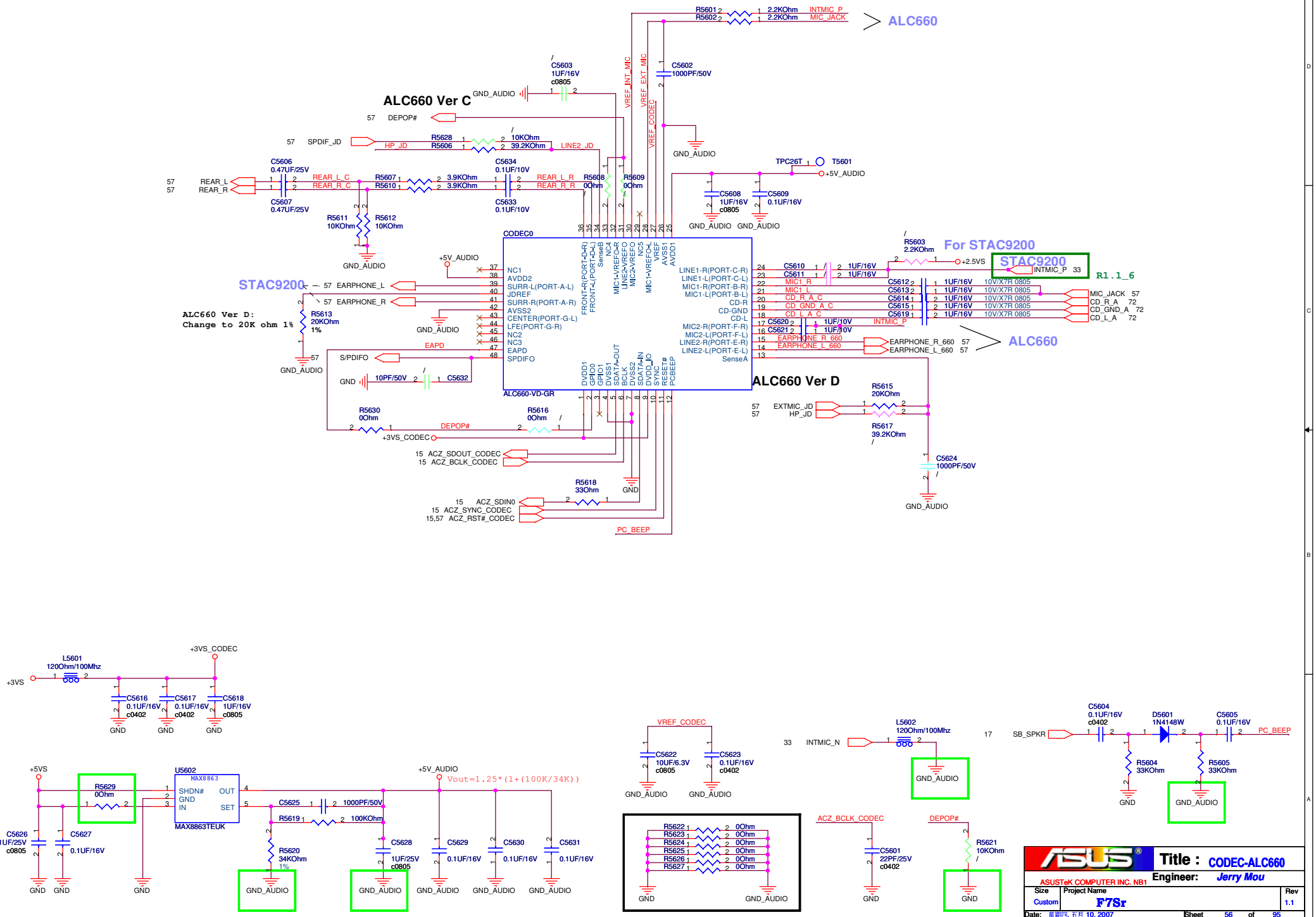
Title : Blank Page

ASUSTeK COMPUTER INC

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 55 of 95


ALC660 Ver C
ALC660 Ver D
STAC9200
For STAC9200
ALC660
CODEC0
ALC660-VD-GR
ALC660 Ver D:
Change to 20K ohm 1%
Title : CODEC-ALC660
ASUSTeK COMPUTER INC. NB1
Engineer: Jerry Mou
Size: Custom
Project Name: F7Sr
Rev: 1.1
Date: 星期四, 五月 10, 2007
Sheet 56 of 95

1->-6 V/V
0->NORMAL

To Internal Speaker Connector

TYPE	LINE_OUT	S/PDIF_OUT	NC
HP_JD	L	H	H
JACK_SW#	L	L	H

HP_JD
Earphones Jack In : Low
SPDIF Jack In or NC : High

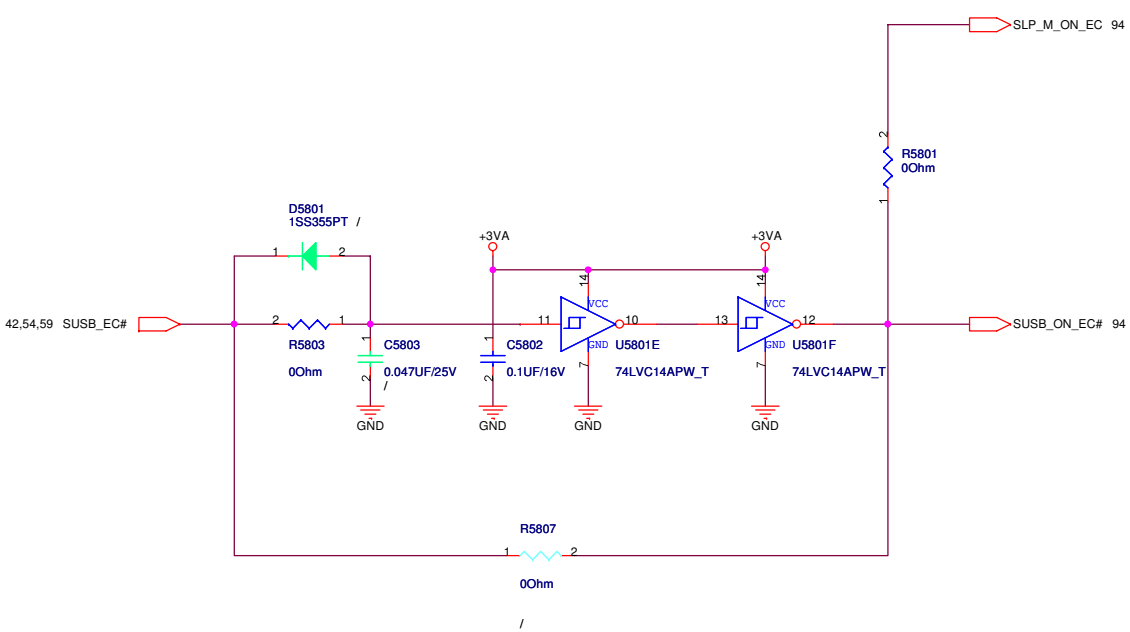
Earphone In Jack

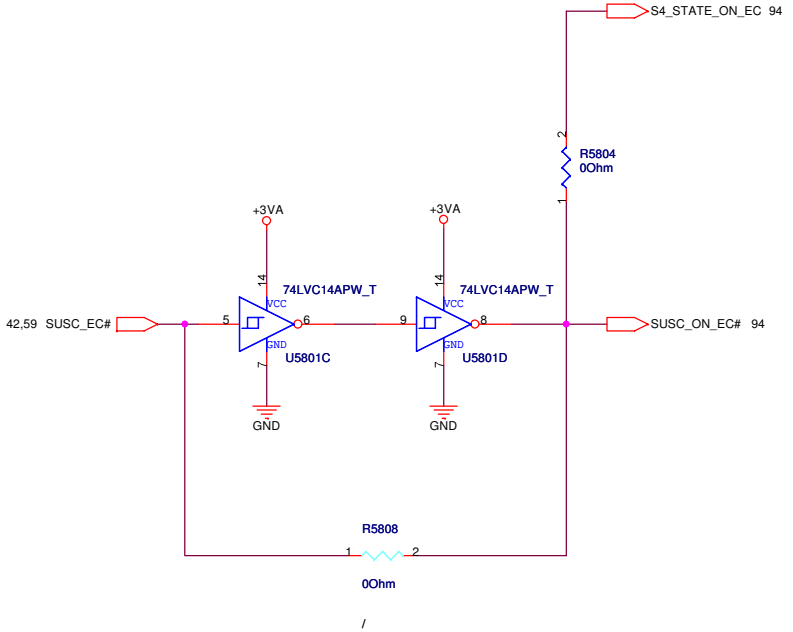
EXTERNAL MIC

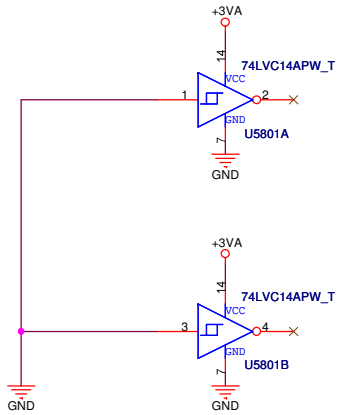
R1.2

R1.2

Title :	AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB1	Engineer: Jerry Mou
Size: Custom	Project Name: F7Sr
Rev: 1.1	
Date: 星期四, 五月 10, 2007	Sheet 57 of 95







ASUSTeK COMPUTER INC	Title : Sequence Control	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 58 of 94	

R1.1_14

For EC RESET

For PU/PD

For XTAL

For POWER

IT8511TE

EC0

LPC

FLASH ROM

KBMX

PS/2

SMBus

ADC

DAC

GPIO

Battery

Thermal Sensor

for Keyboard ID

R5930以後預留測試
ER後未用則移除

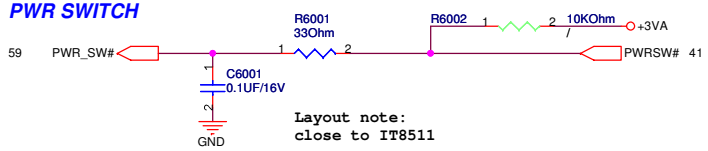
Reserved for iAMT

Title :	IT8511TE
ASUSTeK COMPUTER INC. NB1	Engineer: Jerry Mou
Size: Custom	Project Name: F7Sr
Rev: 1.1	
Date: 星期四, 五月 10, 2007	Sheet 59 of 95

R1.1_15

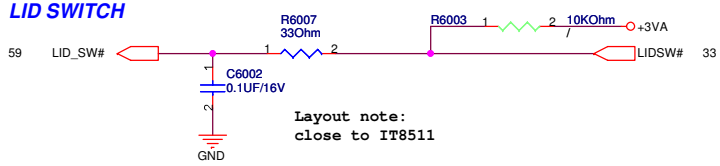
For Switch

PWR SWITCH



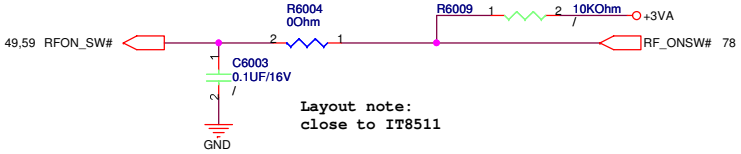
Layout note:
close to IT8511

LID SWITCH



Layout note:
close to IT8511

RF ON SWITCH

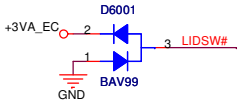


Layout note:
close to IT8511

If you don't use Audio DJ function, please use this schematics

Note:

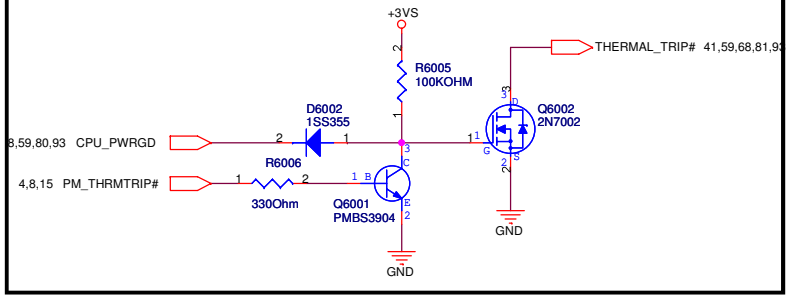
This LID_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.



Layout note:
close to connector

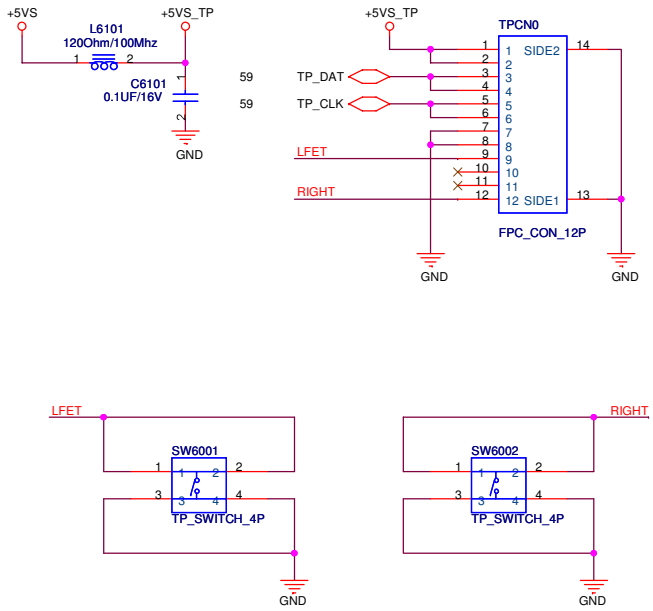
R1.1_15

For Thermal Control Method

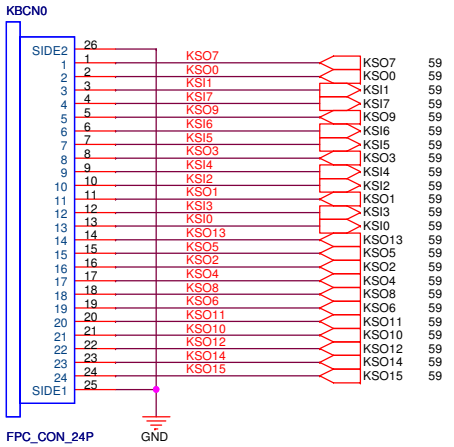


ASUSTeK COMPUTER INC	Title : Switches	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 60 of 95	

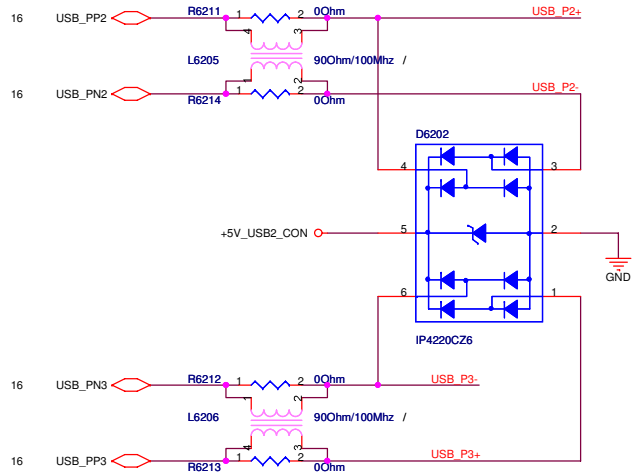
For Touch-Pad

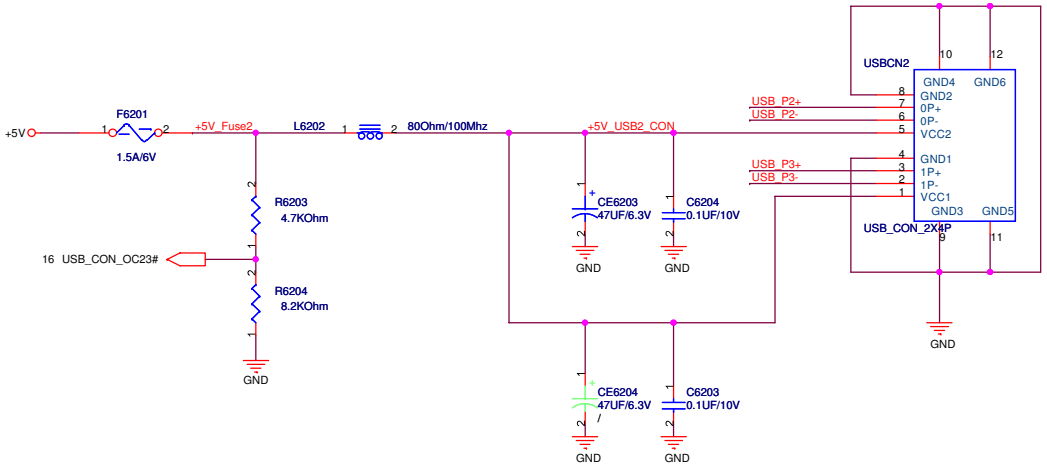


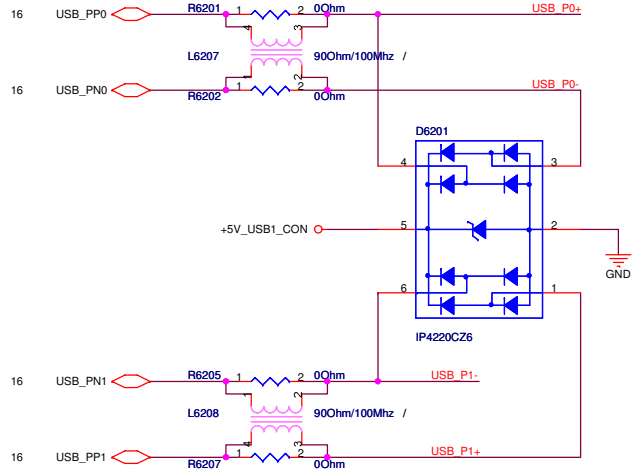
FOR A7 K/B , Matrix B

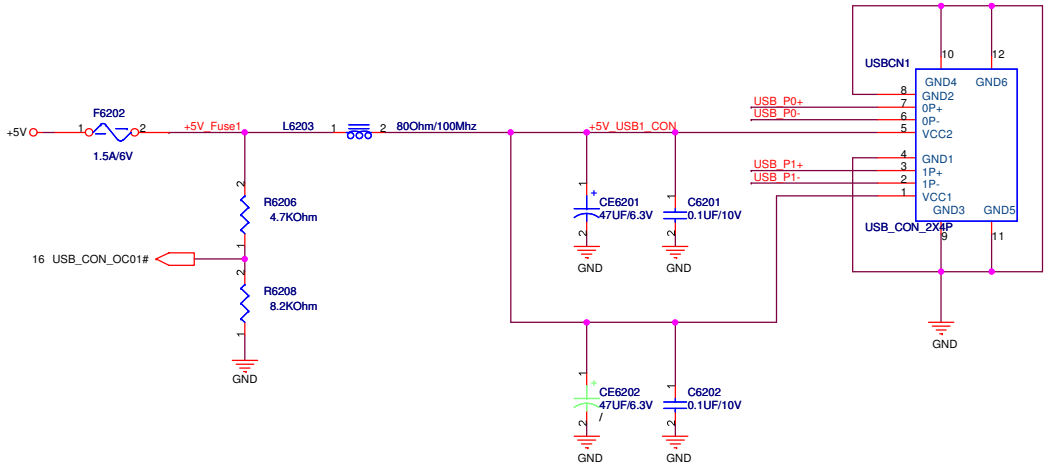


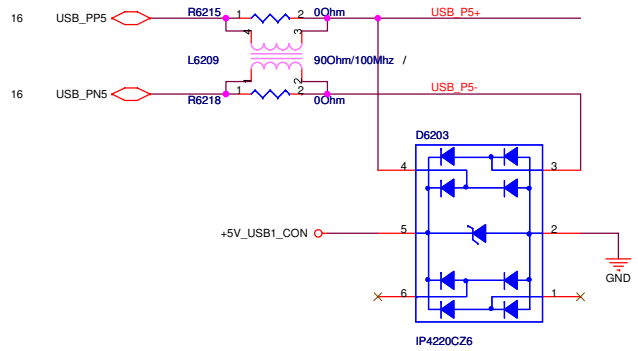
ASUSTeK COMPUTER INC. NB1	Title : Touch Pad & KB	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 61 of 95	

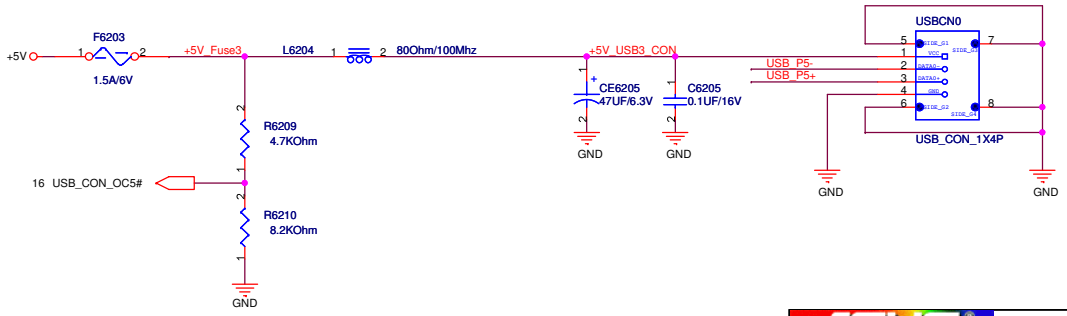












ASUSTeK COMPUTER INC	Title : USB CONN		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 62 of 95		

Title : Blank Page

ASUSTeK COMPUTER INC

Engineer: Jerry Mou

Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 63 of 95

ISA ROM

EC Hardware Strapping

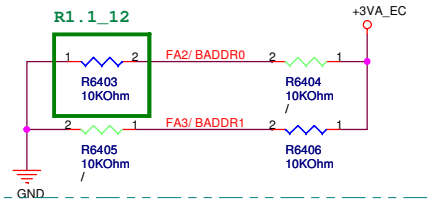
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

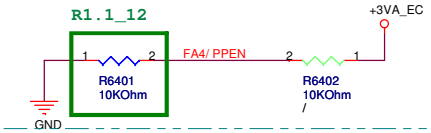


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

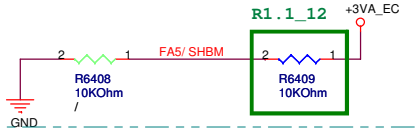
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



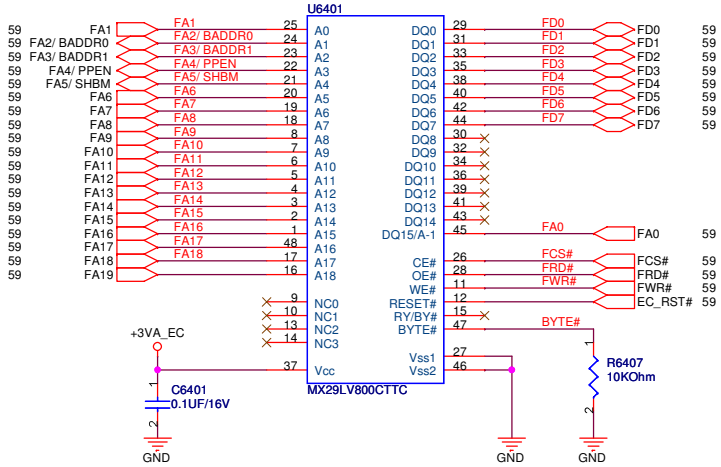
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

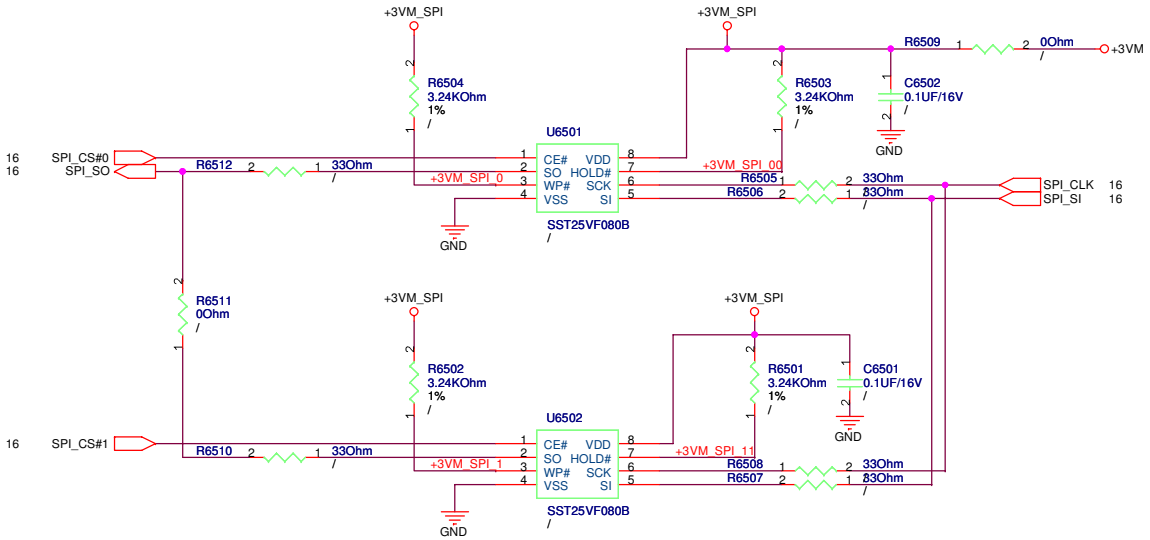
1: Enable Shared Memory with Host BIOS



8M TSOP

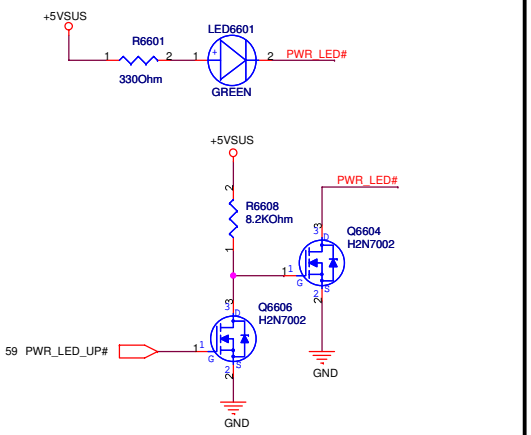


ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 64 of 95	

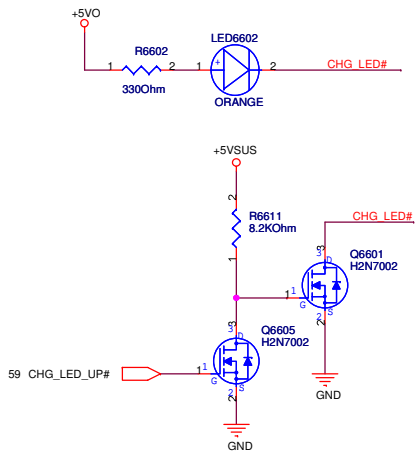


ASUSTeK COMPUTER INC. NB1	Title : SPI ROM	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 65 of 95	

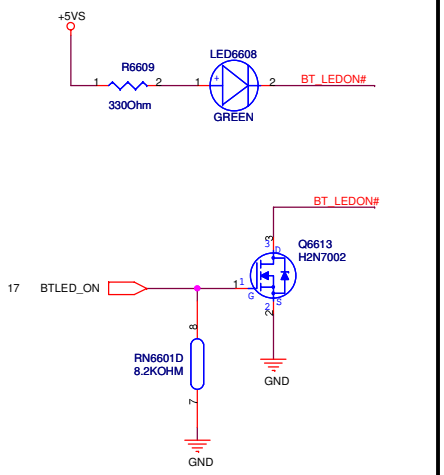
For Power LED



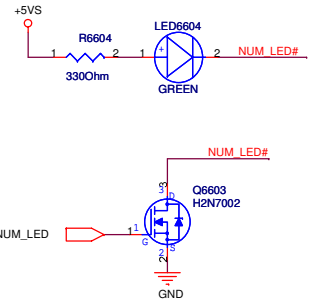
For Battery LED



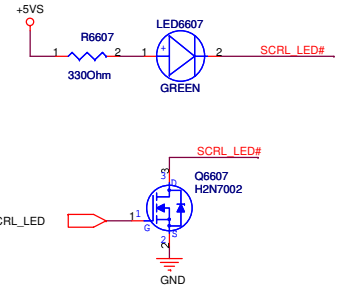
For BT LED



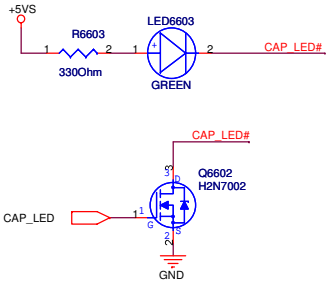
For Number Lock



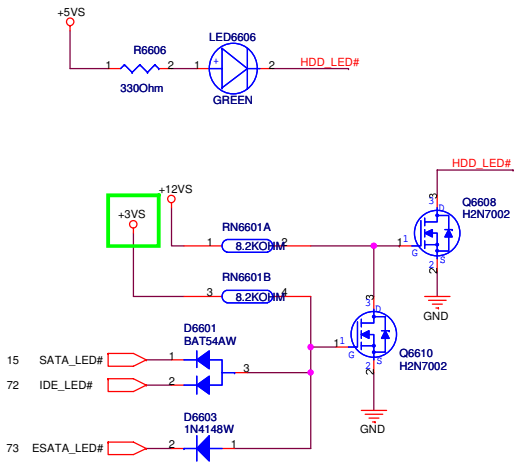
For Scroll Lock



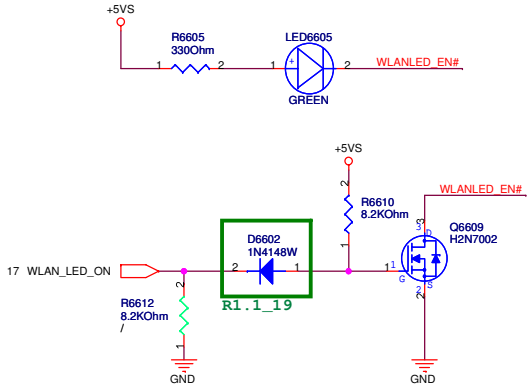
For Caps. Lock



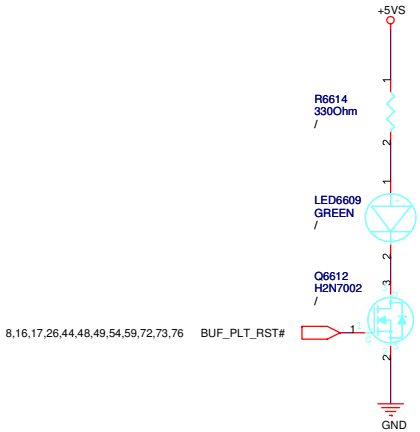
For SATA/IDE LED



For WireLess LED



Reserved LED



RN6601C
5 8.2KOHM 6

ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 66 of 95	

Title : Blank Page

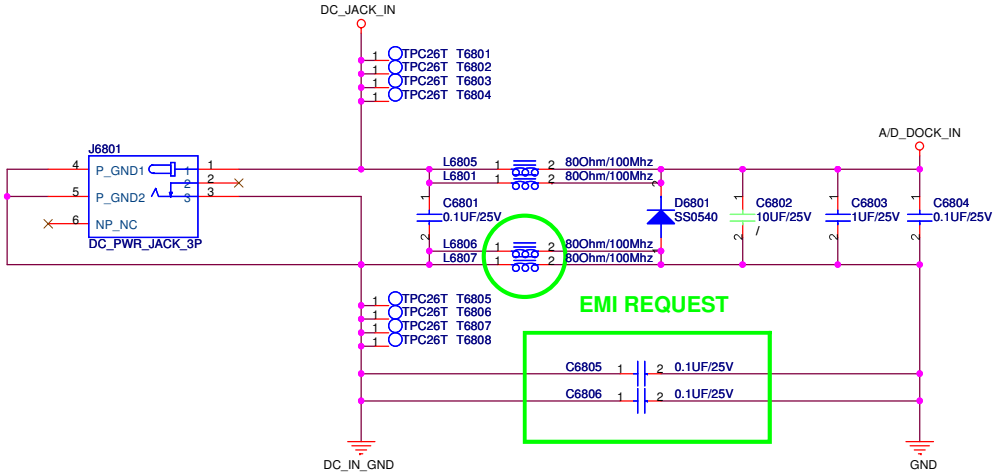
ASUSTeK COMPUTER INC

Engineer: Jerry Mou

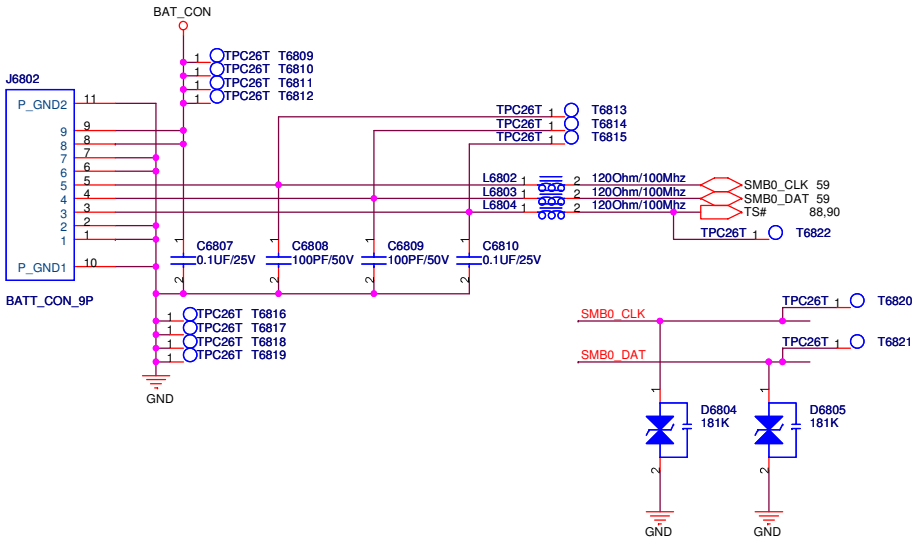
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 67 of 95

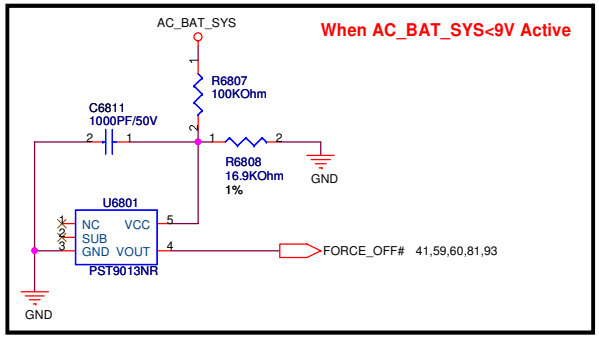
DC IN



BAT IN



Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 68 of 95	

Title : Blank Page

ASUSTeK COMPUTER INC

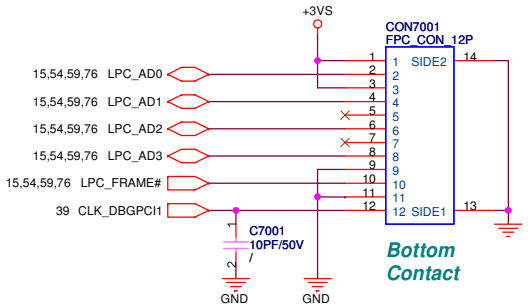
Engineer: Jerry Mou

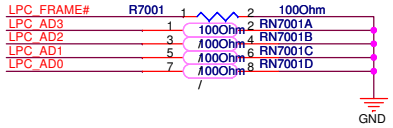
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 69 of 95

For Debug

If support NewCard Debug Card,
Pls don't mount all components.





ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 70 of 95	

Title : Blank Page

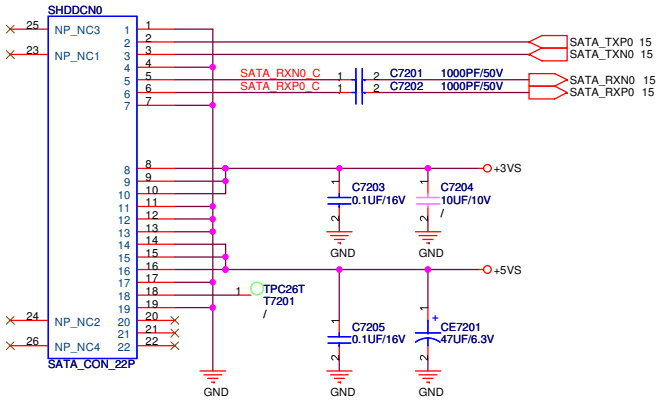
ASUSTeK COMPUTER INC

Engineer: Jerry Mou

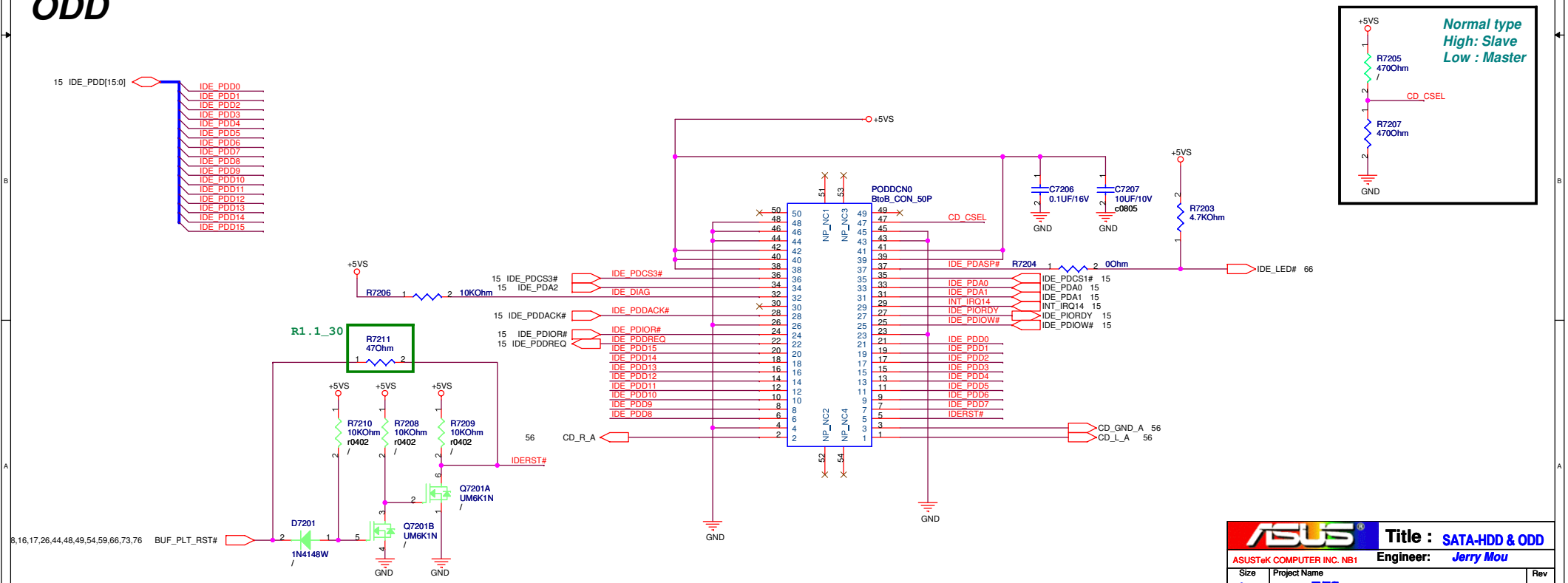
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 71 of 95

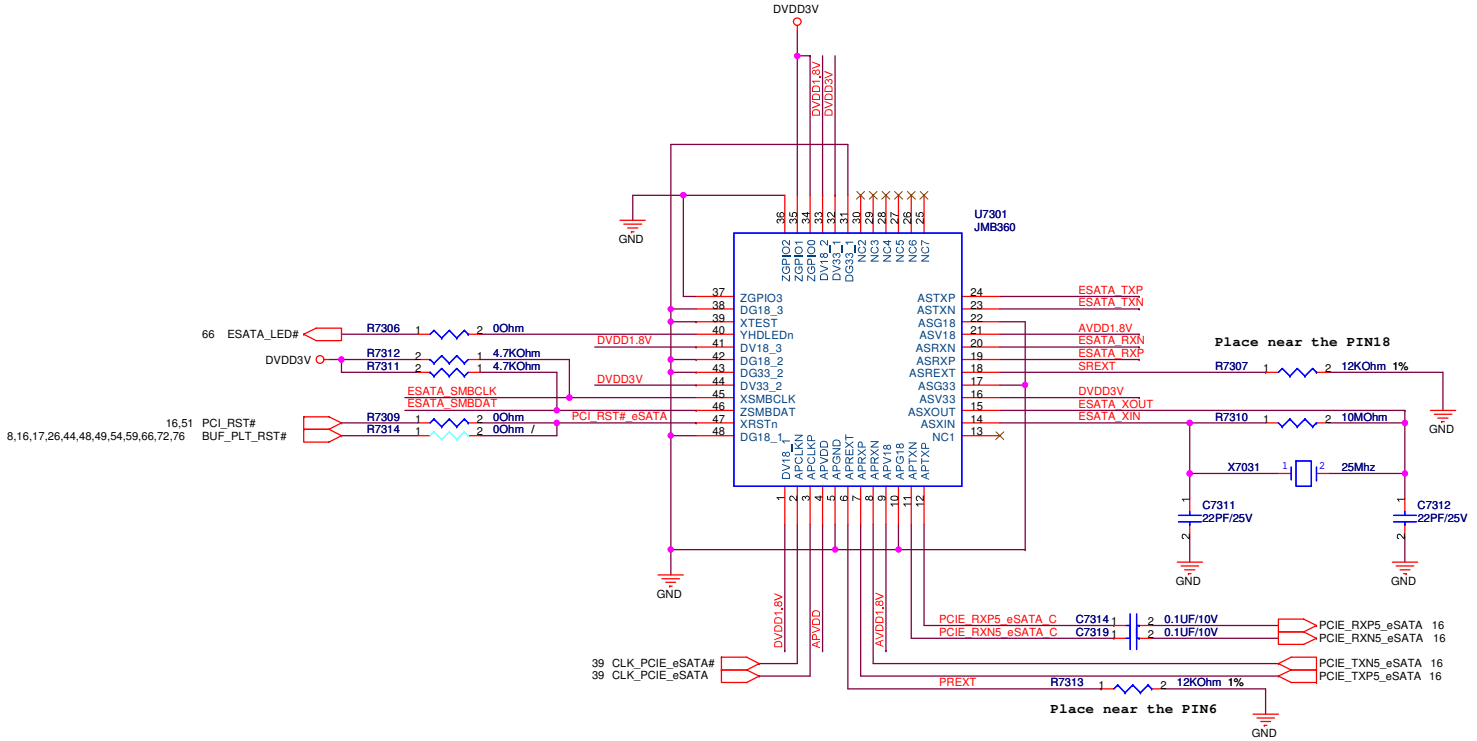
SATA HDD



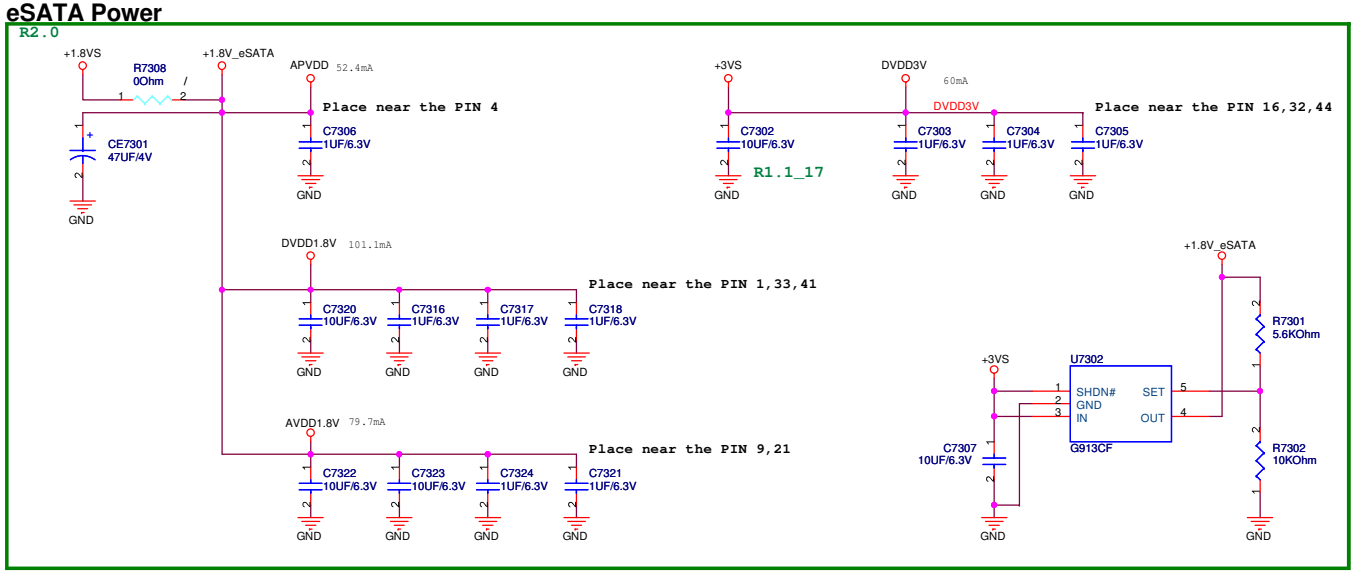
ODD



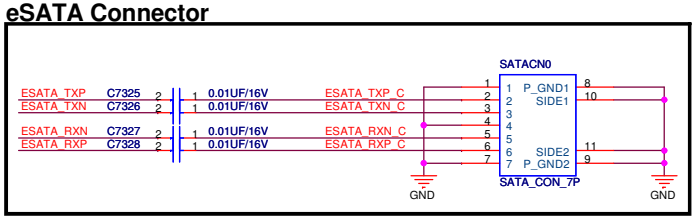
ASUSTeK COMPUTER INC. NB1	Title : SATA-HDD & ODD	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 72 of 95	



eSATA Power

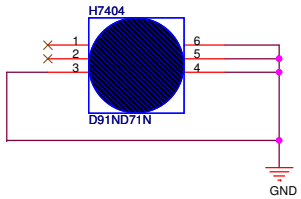


eSATA Connector

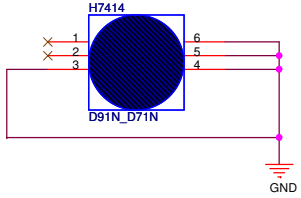


ASUSTeK COMPUTER INC. NB1	Title : eSATA		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 73 of 95		

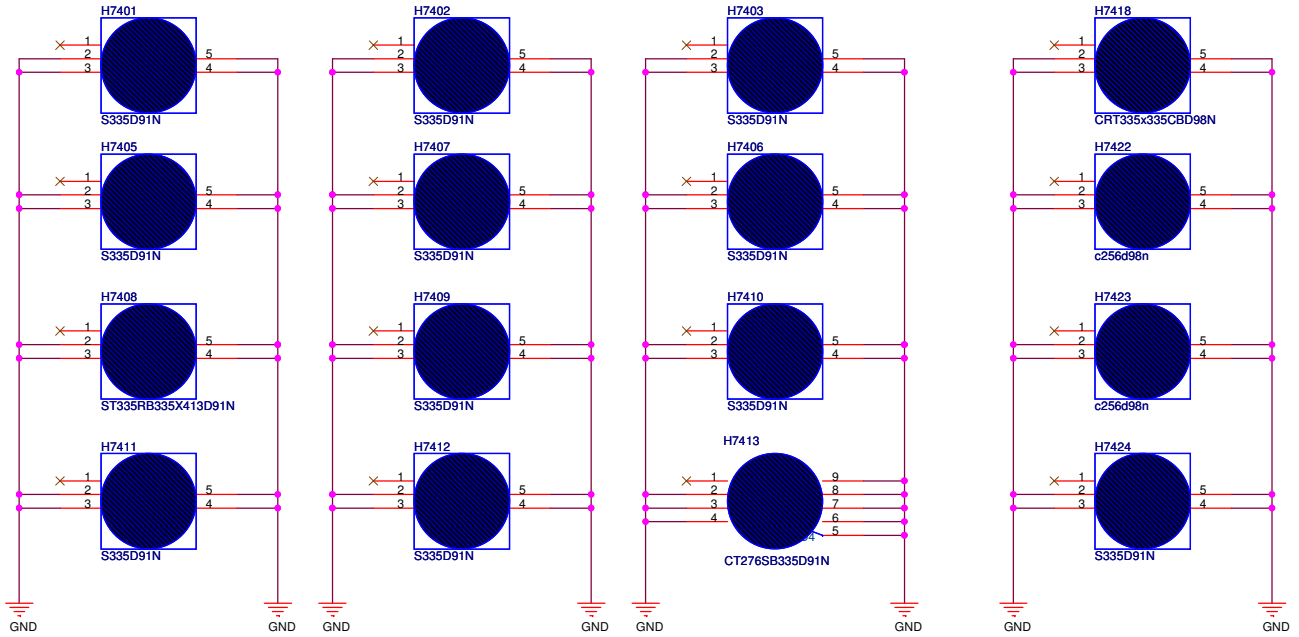
FOR LEFT UNDER



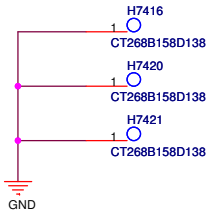
FOR RIGHT UP



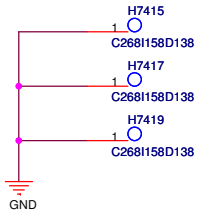
FOR SCREW HOLE

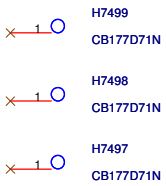


FOR CPU



FOR VGA





ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 74 of 95	

Title : Blank Page

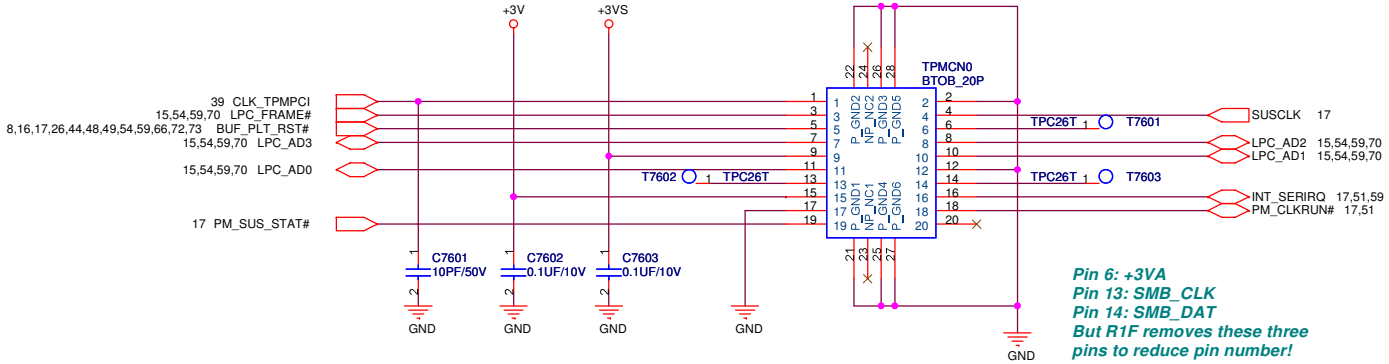
ASUSTeK COMPUTER INC

Engineer: Jerry Mou

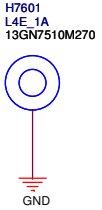
Size	Project Name	Rev
Custom	F7Sr	1.1

Date: 星期四, 五月 10, 2007 Sheet 75 of 95

For TPM module



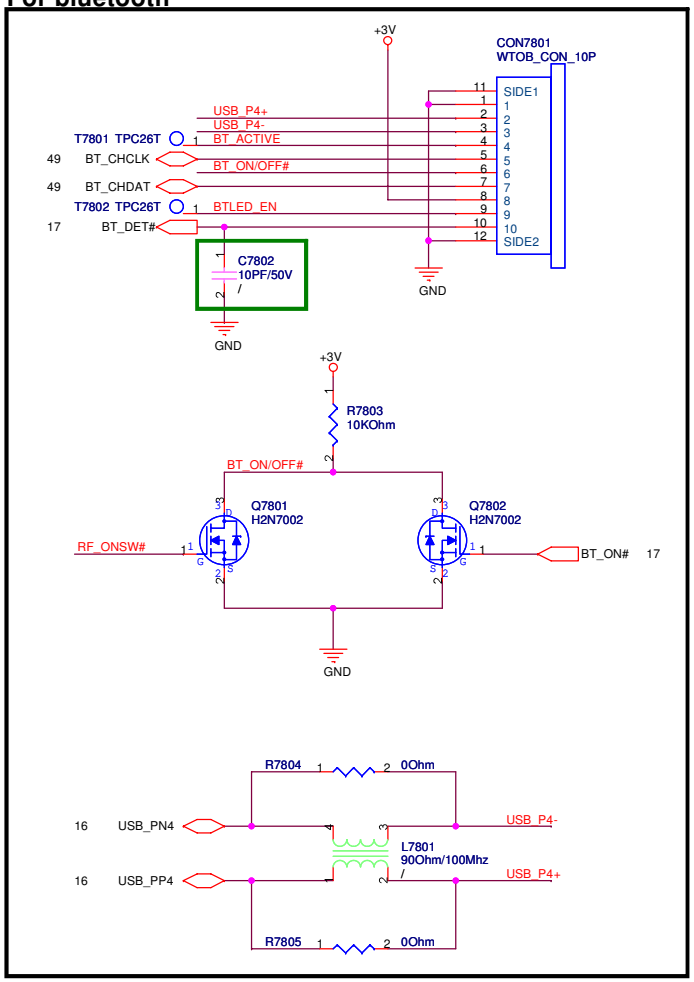
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!



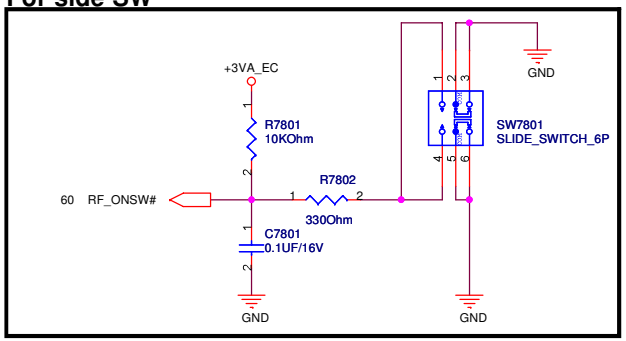
ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 76 of 95	

ASUSTeK COMPUTER INC	Title : SPRING		
	Engineer: Jerry Mou		
Size: Custom	Project Name: F7Sr		Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 77 of 95		

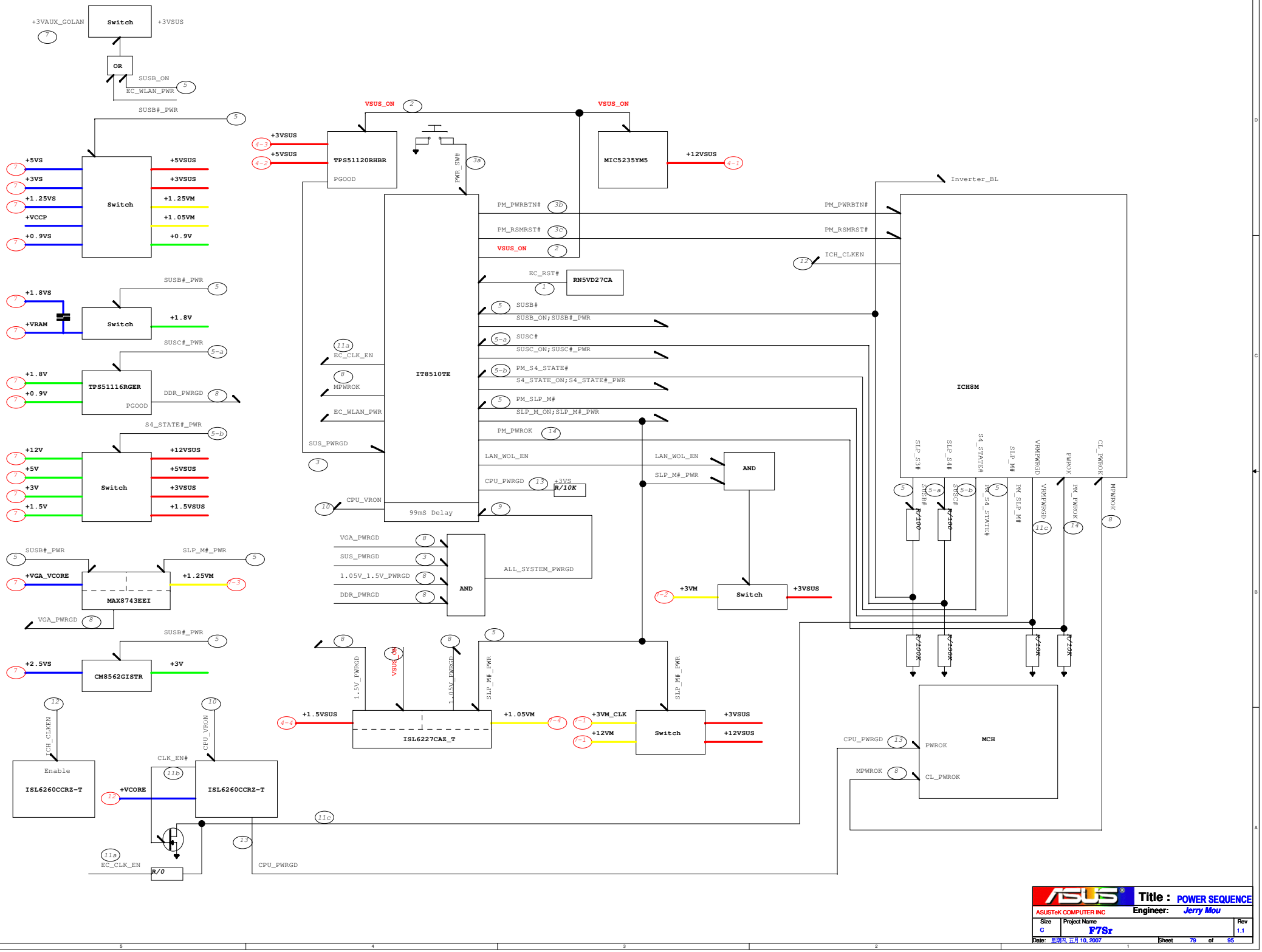
For bluetooth

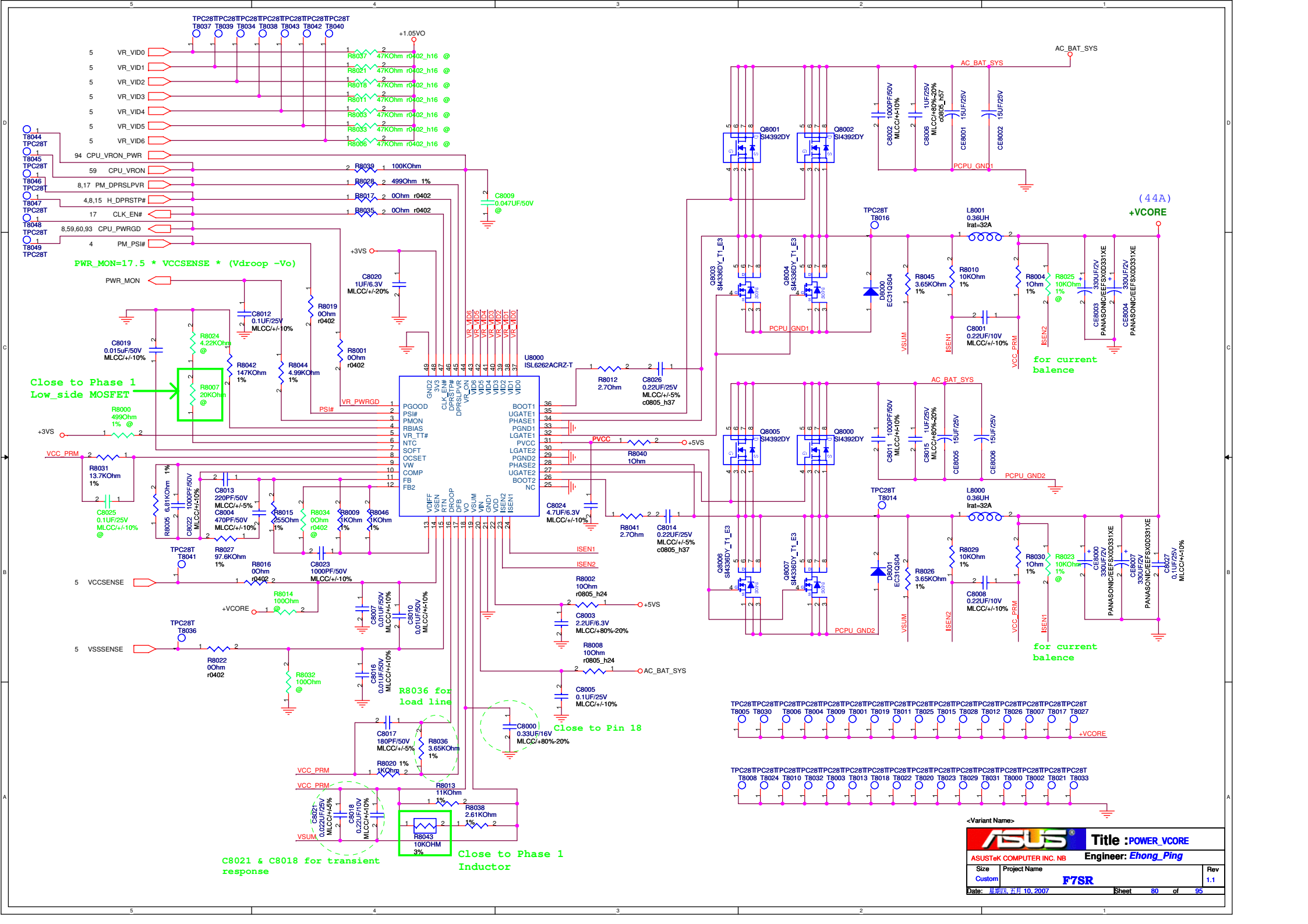


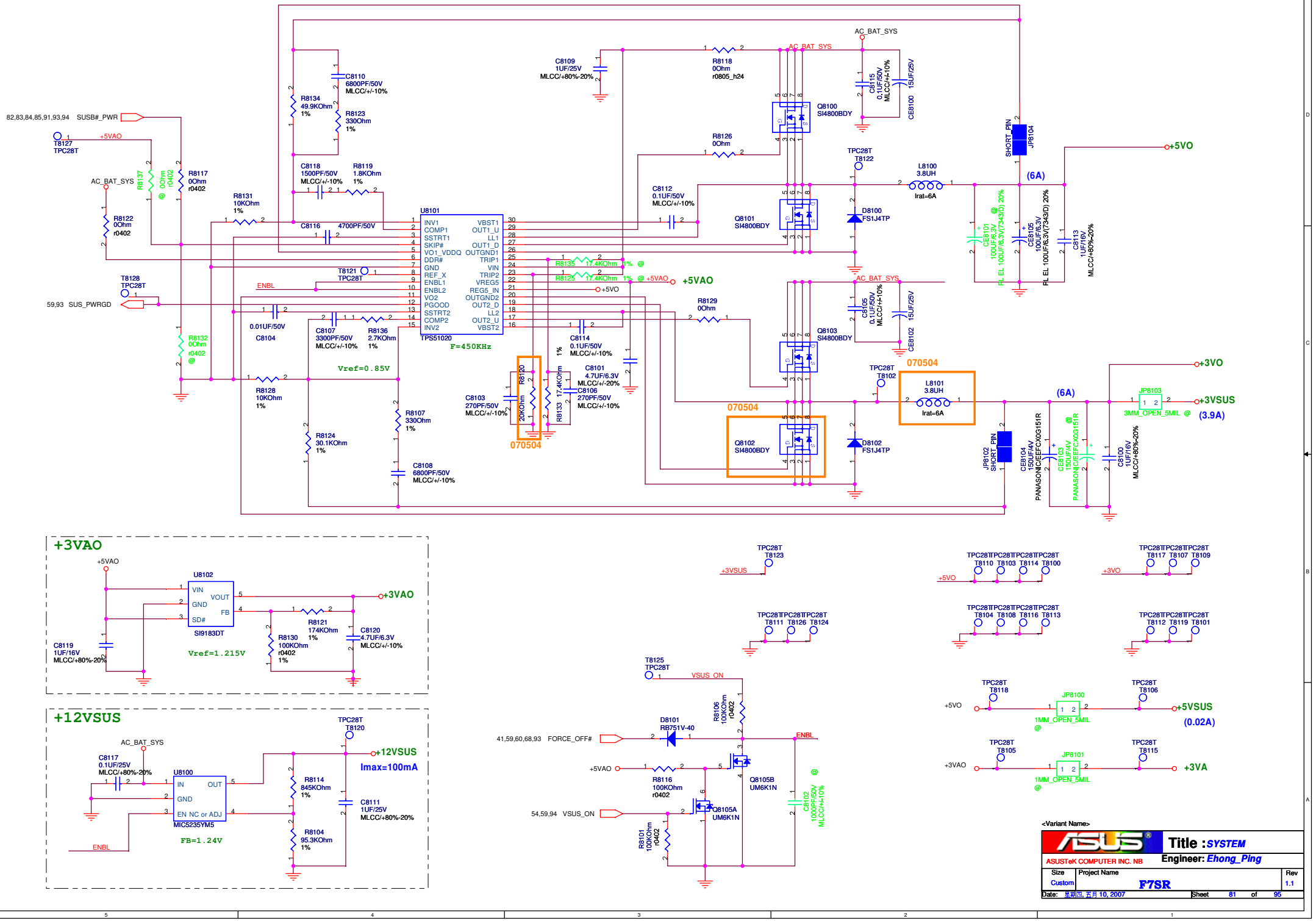
For side SW

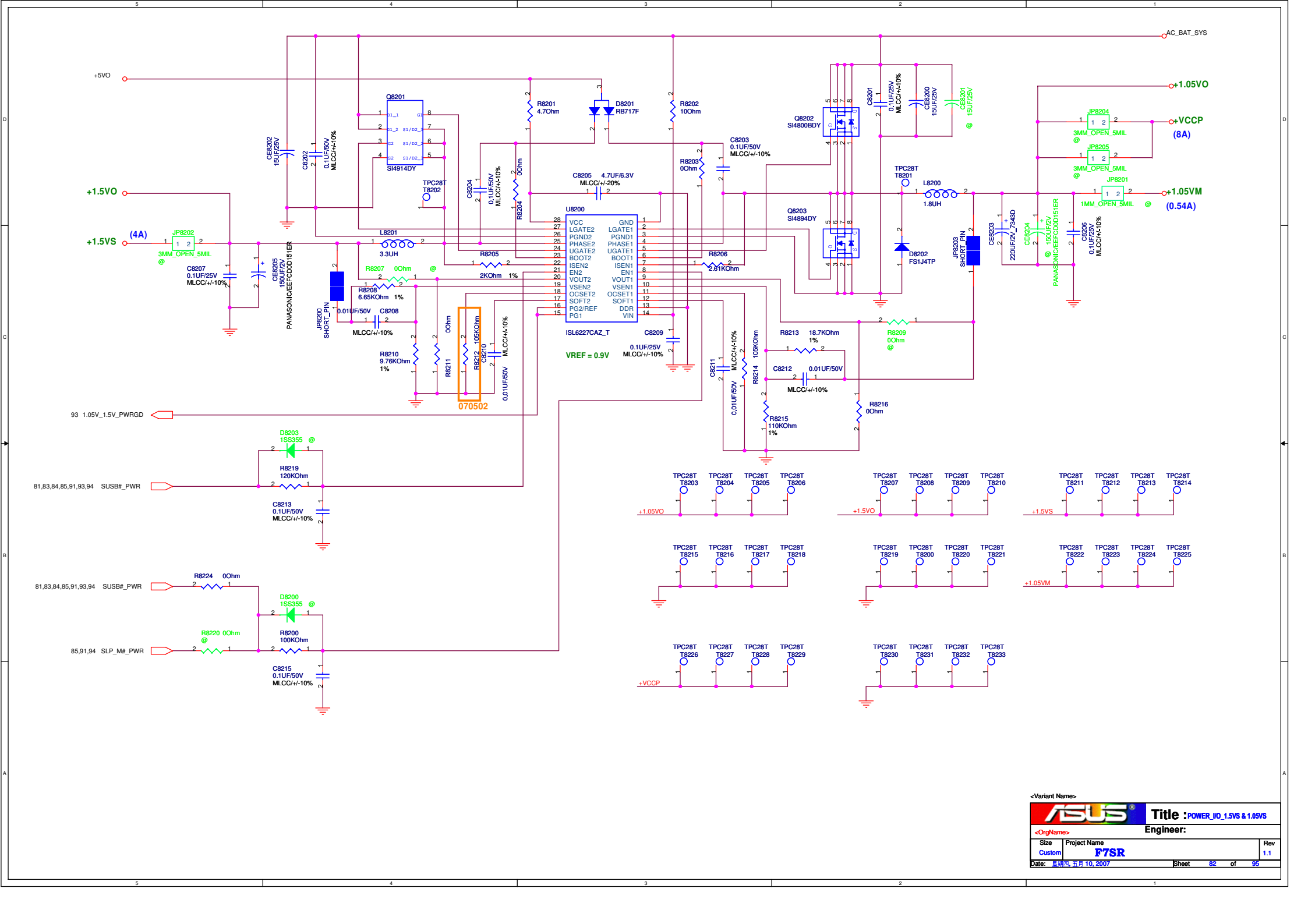


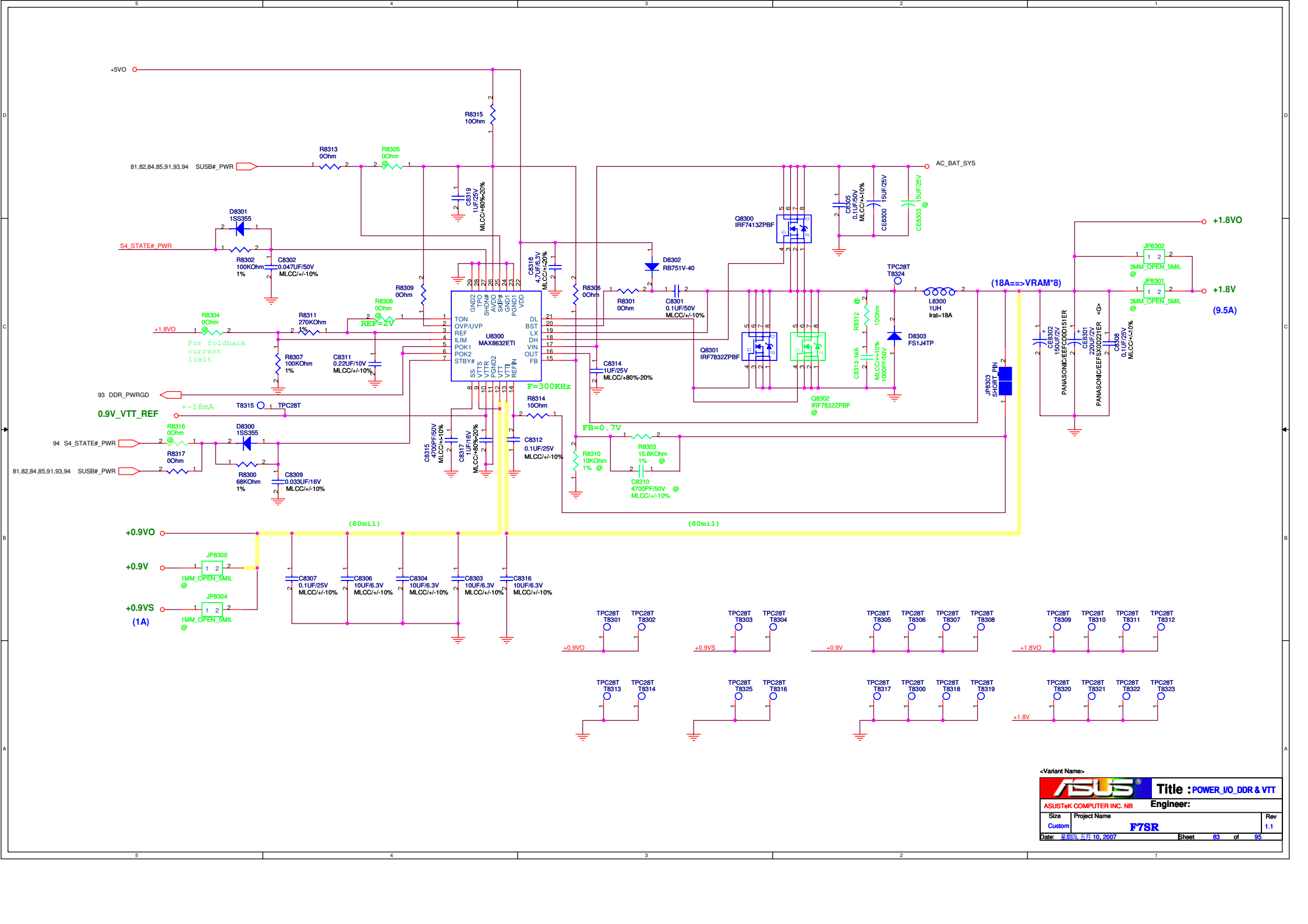
ASUSTeK COMPUTER INC	Title : Bluetooth	
	Engineer: Jerry Mou	
Size: Custom	Project Name: F7Sr	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 78 of 95	


+3VAUX_GOLAN
Switch
+3VSUS
OR
SUSB_ON
EC_WLAN_PWR
SUSB#_PWR
+5VS
+3VS
+1.25VS
+VCCP
+0.9VS
Switch
+5VSUS
+3VSUS
+1.25VM
+1.05VM
+0.9V
+1.8VS
+VRAM
Switch
+1.8V
SUSC#_PWR
TPS51116RGER
PGOOD
DDR_PWRGD
S4_STATE#_PWR
+12V
+5V
+3V
+1.5V
Switch
+12VSUS
+5VSUS
+3VSUS
+1.5VSUS
SLP_M#_PWR
+VGA_VCORE
MAX8743EEI
+1.25VM
VGA_PWRGD
+2.5VS
CM8562GISTR
+3V
CH_CLKEN
CPU_VRON
Enable
ISL6260CCRZ-T
CLK_EN#
+VCORE
ISL6260CCRZ-T
EC_CLK_EN
R/0
CPU_PWRGD
VSUS_ON
+3VSUS
+5VSUS
TPS51120RHBR
PGOOD
PWR_SW#
MIC5235YM5
+12VSUS
IT8510TE
EC_CLK_EN
MPWROK
EC_WLAN_PWR
SUS_PWRGD
CPU_VRON
99mS Delay
PM_PWRBTN#
PM_RSMRST#
VSUS_ON
EC_RST#
RN5VD27CA
SUSB#
SUSB_ON;SUSB#_PWR
SUSC#
SUSC_ON;SUSC#_PWR
PM_S4_STATE#
S4_STATE_ON;S4_STATE#_PWR
PM_SLP_M#
SLP_M_ON;SLP_M#_PWR
PM_PWROK
LAN_WOL_EN
CPU_PWRGD
+3VS
R/10K
VGA_PWRGD
SUS_PWRGD
1.05V_1.5V_PWRGD
DDR_PWRGD
AND
ALL_SYSTEM_PWRGD
LAN_WOL_EN
SLP_M#_PWR
AND
+3VM
Switch
+3VSUS
1.5V_PWRGD
VSUS_ON
1.05V_PWRGD
SLP_M#_PWR
SLP_M#_PWR
+1.5VSUS
ISL6227CAZ_T
+1.05VM
+3VM_CLK
+12VM
Switch
+3VSUS
+12VSUS
Inverter_BL
PM_PWRBTN#
PM_RSMRST#
ICH_CLKEN
ICH8M
SLP_S3#
SLP_S4#
S4_STATE#
SLP_M#
VRMPWRGD
PWROK
CL_PWROK
SUSB#
SUSC#
PM_S4_STATE#
PM_SLP_M#
VRMPWRGD
PM_PWROK
MPWROK
R/100
R/100
R/100K
R/100K
R/10K
R/10K
CPU_PWRGD
MPWROK
MCH
PWROK
CL_PWROK
Title : POWER SEQUENCE
ASUSTeK COMPUTER INC
Engineer: Jerry Mou
Size C
Project Name F7Sr
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 79 of 95

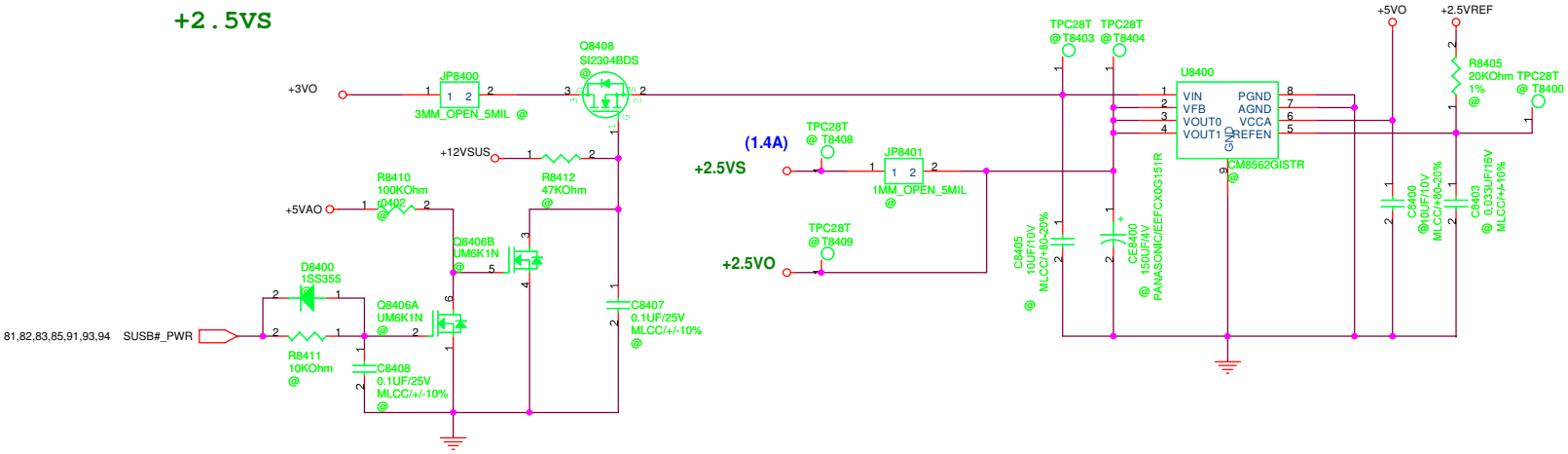

PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to Phase 1
Low_side MOSFET
R8036 for
load line
Close to Pin 18
C8021 & C8018 for transient
response
Close to Phase 1
Inductor
for current
balence
for current
balence
(44A)
+VCORE
U8000
ISL6262ACRZ-T
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Ehong_Ping
Size
Custom
Project Name
F7SR
Rev
1.1
Date: 星期四, 五月 10, 2007
Sheet 80 of 95


82,83,84,85,91,93,94 SUSB#_PWR
59,93 SUS_PWRGD
AC_BAT_SYS
+5VAO
+5VO
+3VO
+3VSUS
+3VAO
+12VSUS
U8101
TPS51020
F=450KHz
Vref=0.85V
U8102
SI9183DT
Vref=1.215V
U8100
MIC5235YM5
FB=1.24V
Q8100 SI4800BDY
Q8101 SI4800BDY
Q8103 SI4800BDY
Q8102 SI4800BDY
D8100 FS1J4TP
D8102 FS1J4TP
D8101 RB751V-40
Q8105B UM6K1N
Q8105A UM6K1N
L8100 3.8UH
L8101 3.8UH
Irat=6A
(6A)
(3.9A)
(0.02A)
Imax=100mA
070504
ENBL
VSUS_ON
FORCE_OFF#
VSUS_ON
SHORT_PIN
3MM_OPEN_5MIL
1MM_OPEN_5MIL
<Variant Name>
Title : SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Ehong_Ping
Size Custom
Project Name F7SR
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 81 of 95

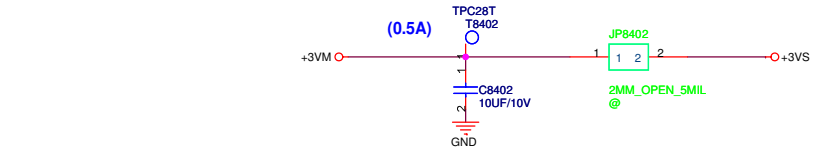

AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
(4A)
+1.05VO
+VCCP
(8A)
+1.05VM
(0.54A)
U8200
ISL6227CAZ_T
VREF = 0.9V
Q8201
SI4914DY
Q8202
SI4800BDY
Q8203
SI4894DY
D8201
RB717F
D8202
FS1J4TP
L8200
1.8UH
L8201
3.3UH
93 1.05V_1.5V_PWRGD
81,83,84,85,91,93,94 SUSB#_PWR
85,91,94 SLP_M#_PWR
070502
Title : POWER_I/O_1.5VS & 1.05VS
Engineer:
<OrgName>
Project Name
F7SR
Size
Custom
Rev
1.1
Date: 星期四, 五月 10, 2007
Sheet 82 of 95


+5VO
R8315 10Ohm
R8313 0Ohm
R8305 0Ohm
81,82,84,85,91,93,94 SUSB#_PWR
C8319 1UF/25V MLCC/+80%-20%
AC_BAT_SYS
D8301 1SS355
S4_STATE#_PWR
R8302 100KOhm 1%
C8302 0.047UF/50V MLCC/+/-10%
Q8300 IRF7413ZPBF
C8305 0.1UF/50V MLCC/+/-10%
CE8300 15UF/25V
CE8303 15UF/25V @
+1.8VO
JP8302 3MM_OPEN_5MIL @
JP8301 3MM_OPEN_5MIL @
+1.8V
(9.5A)
(18A==>VRAM*8)
TPC28T T8324
L8300 1UH Irat=18A
D8303 FS1J4TP
R8312 10Ohm
C8313 N/A
MLCC/+/-10% 1000PF/50V
R8309 0Ohm
R8308 0Ohm
REF=2V
R8304 0Ohm
For foldback current limit
R8311 270KOhm 1%
R8307 100KOhm 1%
C8311 0.22UF/10V MLCC/+/-10%
U8300 MAX8632ETI
GND2 TPO SHDN# AVDD SKIP# GND1 PGND1 VDD
TON OVP/UVP REF ILIM POK1 POK2 STBY#
DL BST LX DH VIN OUT FB
SS VTTS VTTR PGND2 VTT VTTI REFIN
C8318 4.7UF/6.3V MLCC/+/-20%
R8306 0Ohm
R8301 0Ohm
C8301 0.1UF/50V MLCC/+/-10%
D8302 RB751V-40
Q8301 IRF7832ZPBF
Q8302 IRF7832ZPBF @
C8314 1UF/25V MLCC/+80%-20%
JP8303 SHORT_PIN
C8302 150UF/2V PANASONIC/EEFCDD0151ER
C8307 220UF/2V PANASONIC/EEFSX0D221ER <G>
C8308 0.1UF/25V MLCC/+/-10%
93 DDR_PWRGD
+-18mA
T8315 TPC28T
0.9V_VTT_REF
R8314 10Ohm
F=300KHz
FB=0.7V
R8316 0Ohm
94 S4_STATE#_PWR
R8317 0Ohm
81,82,84,85,91,93,94 SUSB#_PWR
D8300 1SS355
R8300 68KOhm 1%
C8309 0.033UF/16V MLCC/+/-10%
C8315 470PF/50V MLCC/+/-10%
C8317 1UF/16V MLCC/+80%-20%
C8312 0.1UF/25V MLCC/+/-10%
R8310 10KOhm 1% @
R8303 15.8KOhm 1% @
C8310 4700PF/50V @ MLCC/+/-10%
(80mil)
(80mil)
+0.9VO
+0.9V
+0.9VS
(1A)
JP8300 1MM_OPEN_5MIL @
JP8304 1MM_OPEN_5MIL @
C8307 0.1UF/25V MLCC/+/-10%
C8306 10UF/6.3V MLCC/+/-10%
C8304 10UF/6.3V MLCC/+/-10%
C8303 10UF/6.3V MLCC/+/-10%
C8316 10UF/6.3V MLCC/+/-10%
TPC28T T8301 T8302 +0.9VO
TPC28T T8303 T8304 +0.9VS
TPC28T T8305 T8306 T8307 T8308 +0.9V
TPC28T T8309 T8310 T8311 T8312 +1.8VO
TPC28T T8313 T8314
TPC28T T8325 T8316
TPC28T T8317 T8300 T8318 T8319
TPC28T T8320 T8321 T8322 T8323 +1.8V
<Variant Name>
Title : POWER_I/O_DDR & VTT
ASUSTeK COMPUTER INC. NB
Engineer:
Size Custom
Project Name F7SR
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 83 of 95

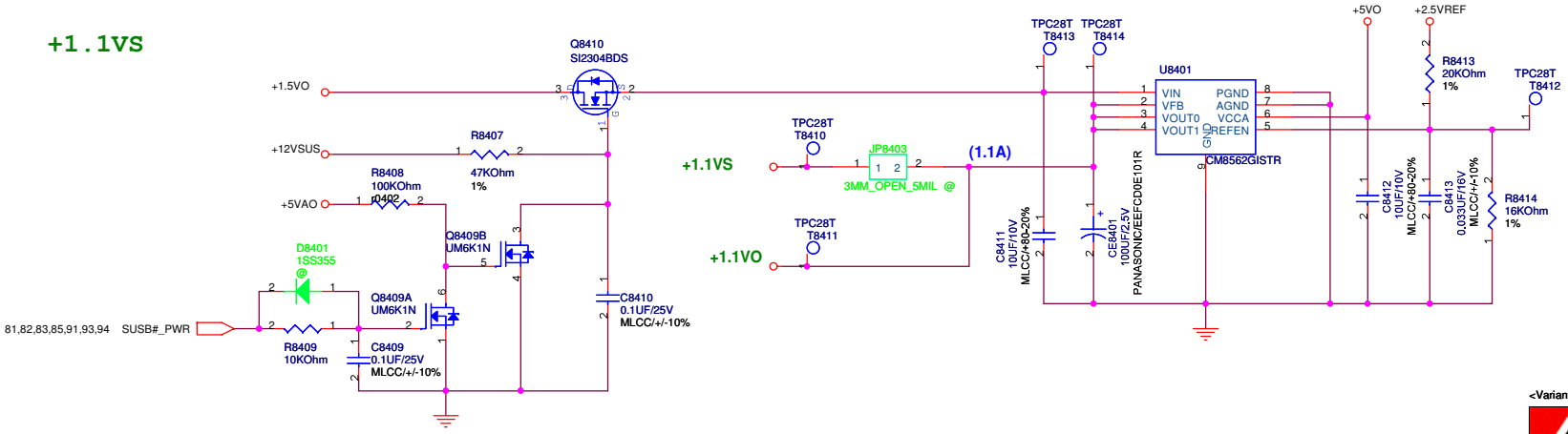
+2.5VS



+3VM

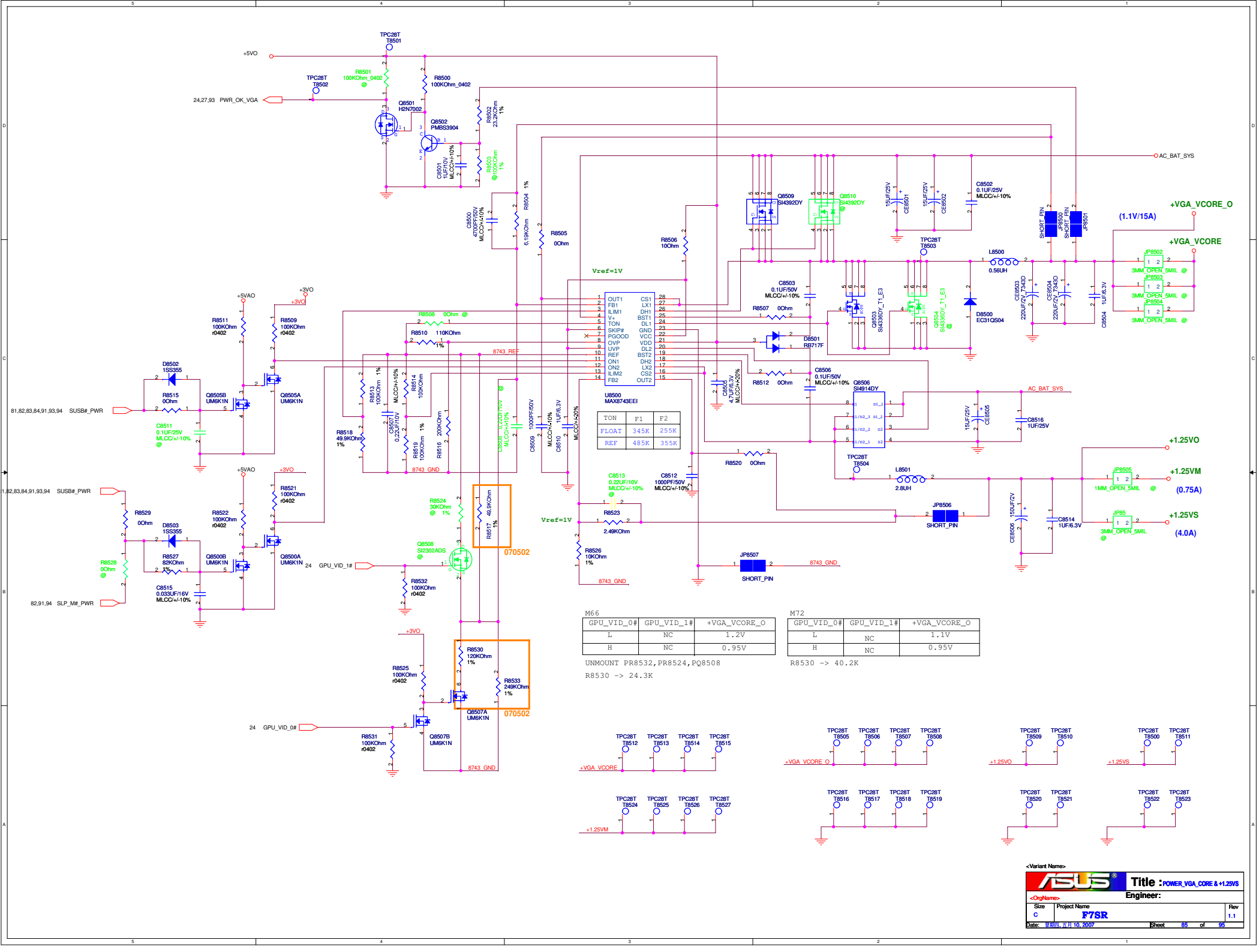


+1.1VS



<Variant Name>

ASUS	Title POWER_I/O_+3VM & +2.5VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7SR	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 84 of 95	


+5VO
TPC28T T8501
TPC28T T8502
R8501 100KOhm_0402 @
R8500 100KOhm_0402
24,27,93 PWR_OK_VGA
Q8501 H2N7002
Q8502 PMBS3904
R8502 23.2KOhm 1%
C8501 4.7UF/10V MLCC/+/-10%
R8503 @ 100KOhm 1%
C8500 4700PF/50V MLCC/+/-10%
R8504 6.19KOhm 1%
R8505 0Ohm
R8506 10Ohm
Vref=1V
U8500 MAX8743EEI
TON F1 F2
FLOAT 345K 255K
REF 485K 355K
Q8509 SI4392DY
Q8510 SI4392DY @
15UF/25V CE8501
15UF/25V CE8502
C8502 0.1UF/25V MLCC/+/-10%
AC_BAT_SYS
SHORT_PIN JP8500
SHORT_PIN JP8501
+VGA_VCORE_O
(1.1V/15A)
+VGA_VCORE
TPC28T T8503
L8500 0.56UH
C8503 0.1UF/50V MLCC/+/-10%
R8507 0Ohm
D8501 RB717F
Q8503 SI4336DY_T1_E3
Q8504 SI4336DY_T1_E3 @
D8500 EC31QS04
CE8503 220UF/2V_7343D
CE8504 220UF/2V_7343D
C8504 1UF/6.3V
JP8502 3MM_OPEN_5MIL @
JP8503 3MM_OPEN_5MIL @
JP8504 3MM_OPEN_5MIL @
R8508 0Ohm @
R8510 110KOhm 1%
8743_REF
+5VAO
+3VO
R8511 100KOhm r0402
R8509 100KOhm r0402
D8502 1SS355
R8515 0Ohm
Q8505B UM6K1N
Q8505A UM6K1N
81,82,83,84,91,93,94 SUSB#_PWR
C8511 0.1UF/25V MLCC/+/-10% @
R8513 100KOhm 1%
R8514 100KOhm
C8507 0.22UF/10V
R8518 49.9KOhm 1%
R8519 100KOhm 1%
R8516 200KOhm
C8508 0.22UF/10V MLCC/+/-10% @
C8509 100PF/50V MLCC/+/-10%
C8510 1UF/6.3V MLCC/+/-20%
8743_GND
C8505 4.7UF/6.3V MLCC/+/-20%
R8512 0Ohm
C8506 0.1UF/50V MLCC/+/-10%
Q8506 SI4914DY
AC_BAT_SYS
15UF/25V CE8505
C8516 1UF/25V
+1.25VO
TPC28T T8504
L8501 2.8UH
JP8505 1MM_OPEN_5MIL @
+1.25VM
(0.75A)
JP8506 SHORT_PIN
C8513 0.22UF/10V MLCC/+/-10% @
C8512 1000PF/50V MLCC/+/-10%
R8520 0Ohm
R8523 2.49KOhm
R8526 10KOhm 1%
JP8507 SHORT_PIN
8743_GND
150UF/2V CE8506
C8514 1UF/6.3V
JP85 3MM_OPEN_5MIL @
+1.25VS
(4.0A)
R8521 100KOhm r0402
R8522 100KOhm r0402
R8529 0Ohm
D8503 1SS355
R8527 82KOhm 1%
Q8500B UM6K1N
Q8500A UM6K1N
R8528 0Ohm @
C8515 0.033UF/16V MLCC/+/-10%
82,91,94 SLP_M#_PWR
R8524 30KOhm @ 1%
R8517 49.9KOhm 1%
070502
Q8508 SI2302ADS @
24 GPU_VID_1#
R8532 100KOhm r0402
R8530 120KOhm 1%
R8533 249KOhm 1%
R8525 100KOhm r0402
Q8507A UM6K1N
Q8507B UM6K1N
24 GPU_VID_0#
R8531 100KOhm r0402
M66
GPU_VID_0# GPU_VID_1# +VGA_VCORE_O
L NC 1.2V
H NC 0.95V
UNMOUNT PR8532,PR8524,PQ8508
R8530 -> 24.3K
M72
GPU_VID_0# GPU_VID_1# +VGA_VCORE_O
L NC 1.1V
H NC 0.95V
R8530 -> 40.2K
TPC28T T8512 T8513 T8514 T8515
+VGA_VCORE
TPC28T T8505 T8506 T8507 T8508
+VGA_VCORE_O
TPC28T T8509 T8510
+1.25VO
TPC28T T8500 T8511
+1.25VS
TPC28T T8524 T8525 T8526 T8527
+1.25VM
TPC28T T8516 T8517 T8518 T8519
TPC28T T8520 T8521
TPC28T T8522 T8523
<Variant Name>
Title : POWER_VGA_CORE & +1.25VS
<OrgName>
Engineer:
Size C
Project Name F7SR
Rev 1.1
Date: 星期四, 五月 10, 2007
Sheet 85 of 95

<Variant Name>

Title : N/A

<OrgName>

Engineer:

Size	Project Name	Rev
A	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 86 of 95

<Variant Name>

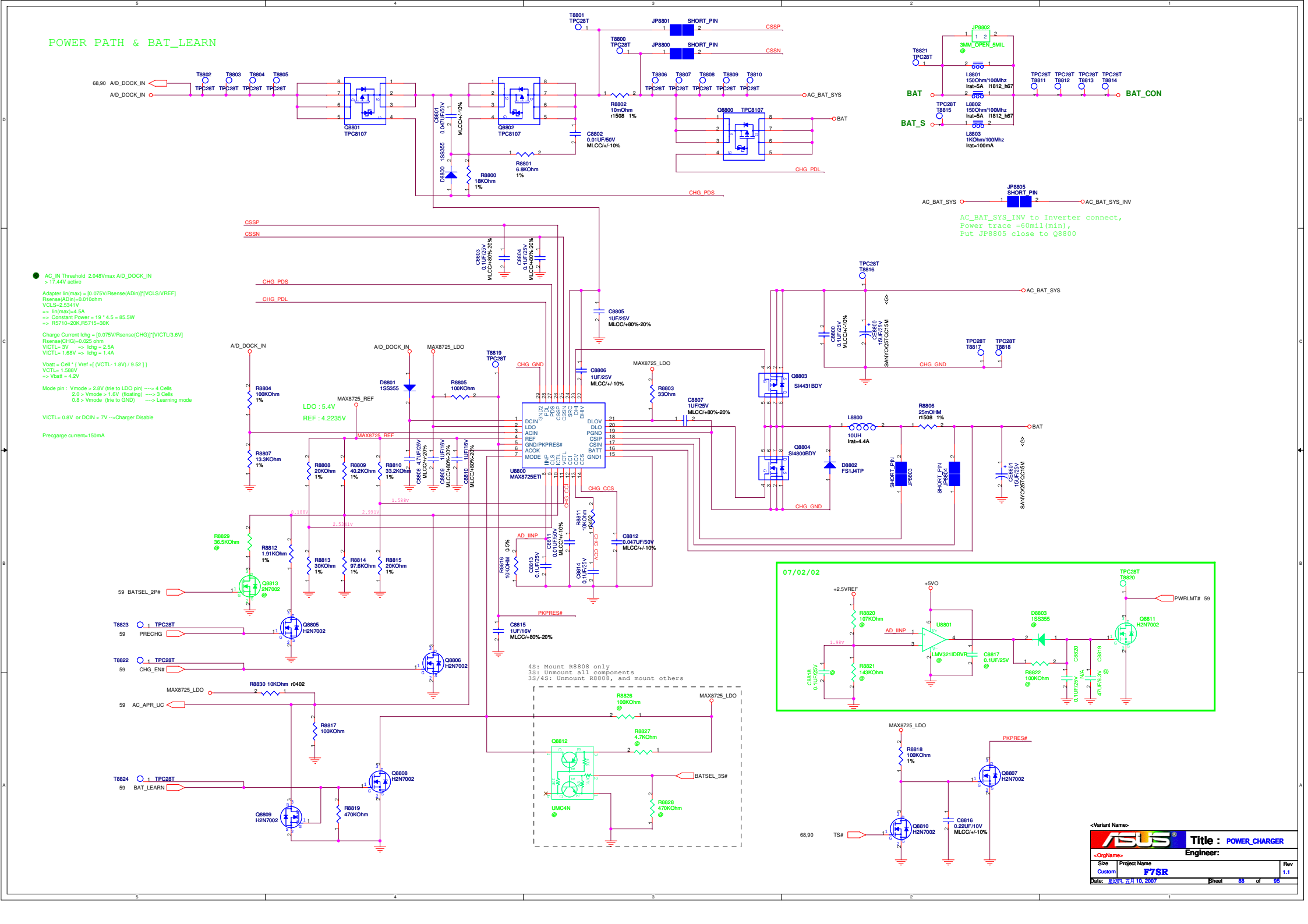
Title : N/A

<OrgName> Engineer:

Size	Project Name	Rev
C	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 87 of 95

POWER PATH & BAT_LEARN



<Variant Name>

Title : N/A

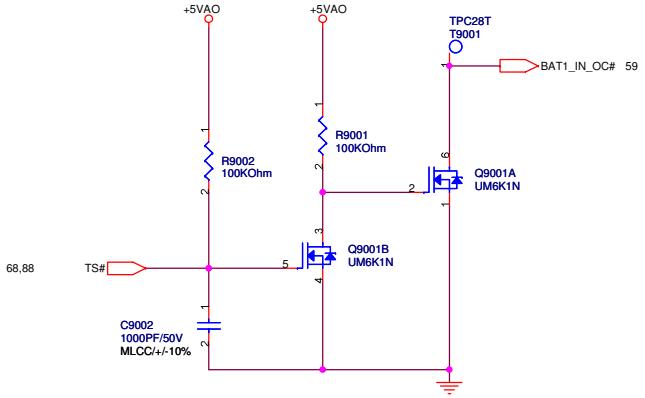
<OrgName>

Engineer:

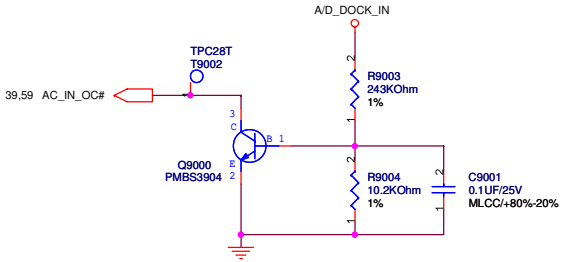
Size	Project Name	Rev
Custom	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 89 of 95

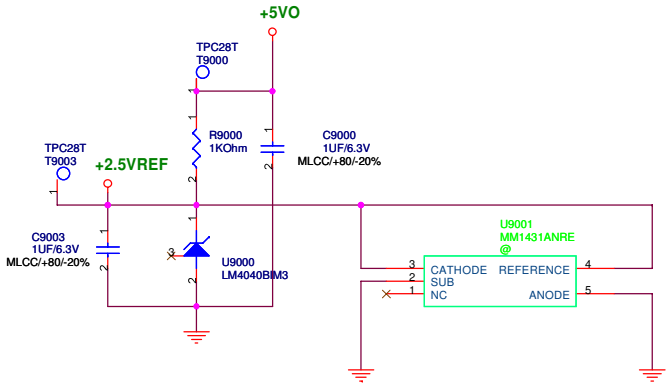
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



U9000 & U9001 colay

<Variant Name>

Title : POWER_DETECT

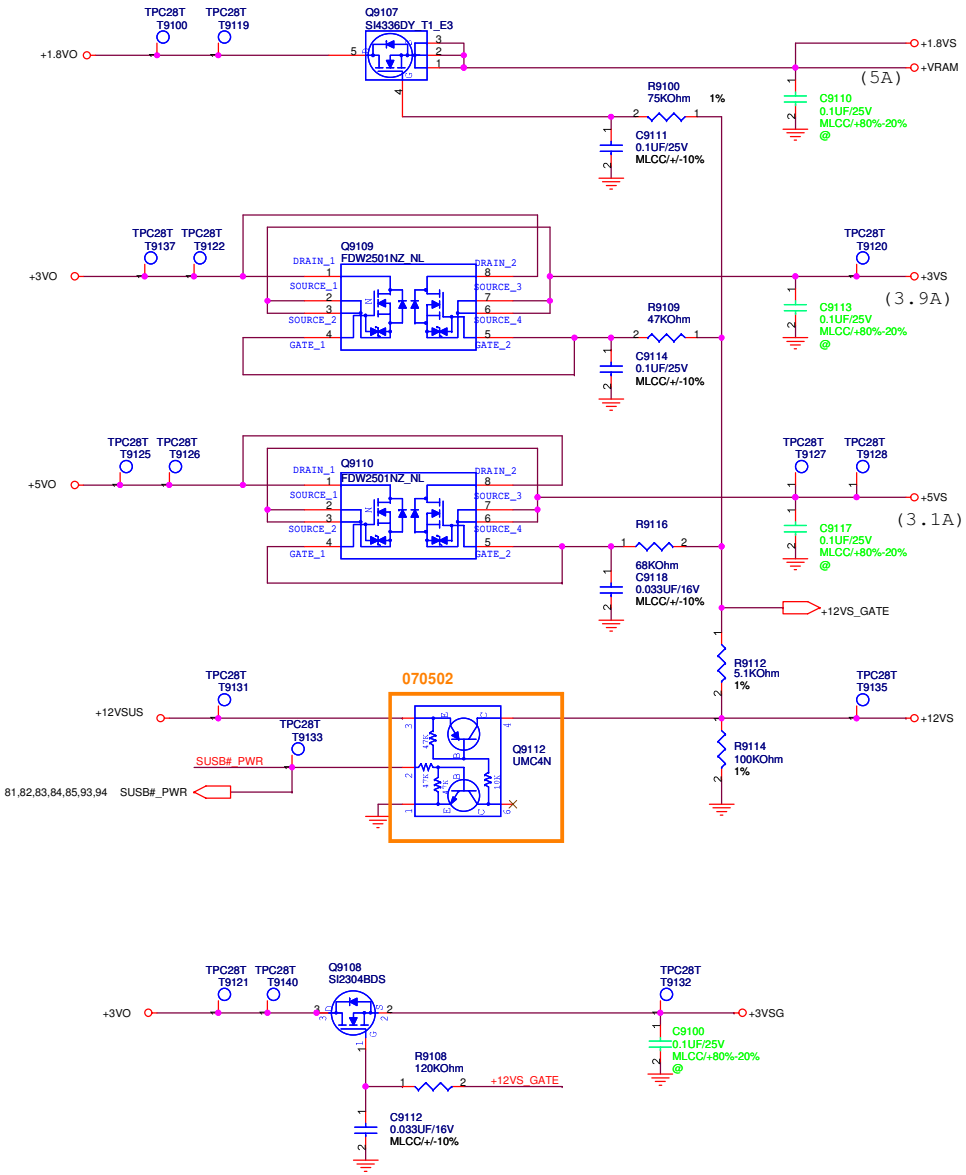
<OrgName>

Engineer:

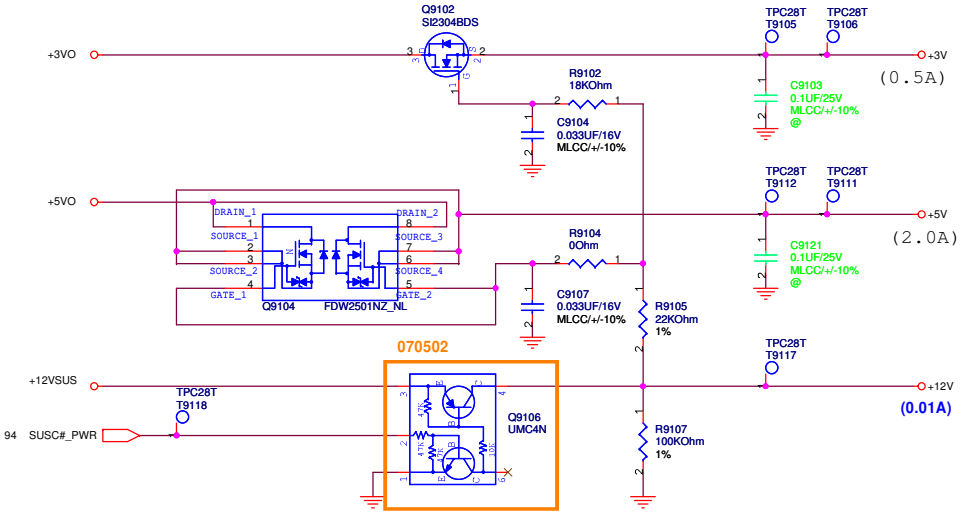
Size	Project Name	Rev
Custom	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 90 of 95

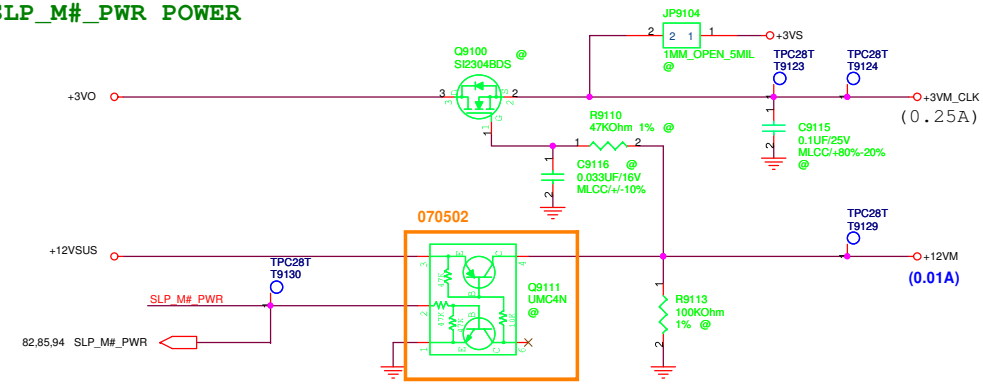
SUSB#_PWR POWER



SUSC#_PWR POWER



SLP_M#_PWR POWER



<Variant Name>

ASUS

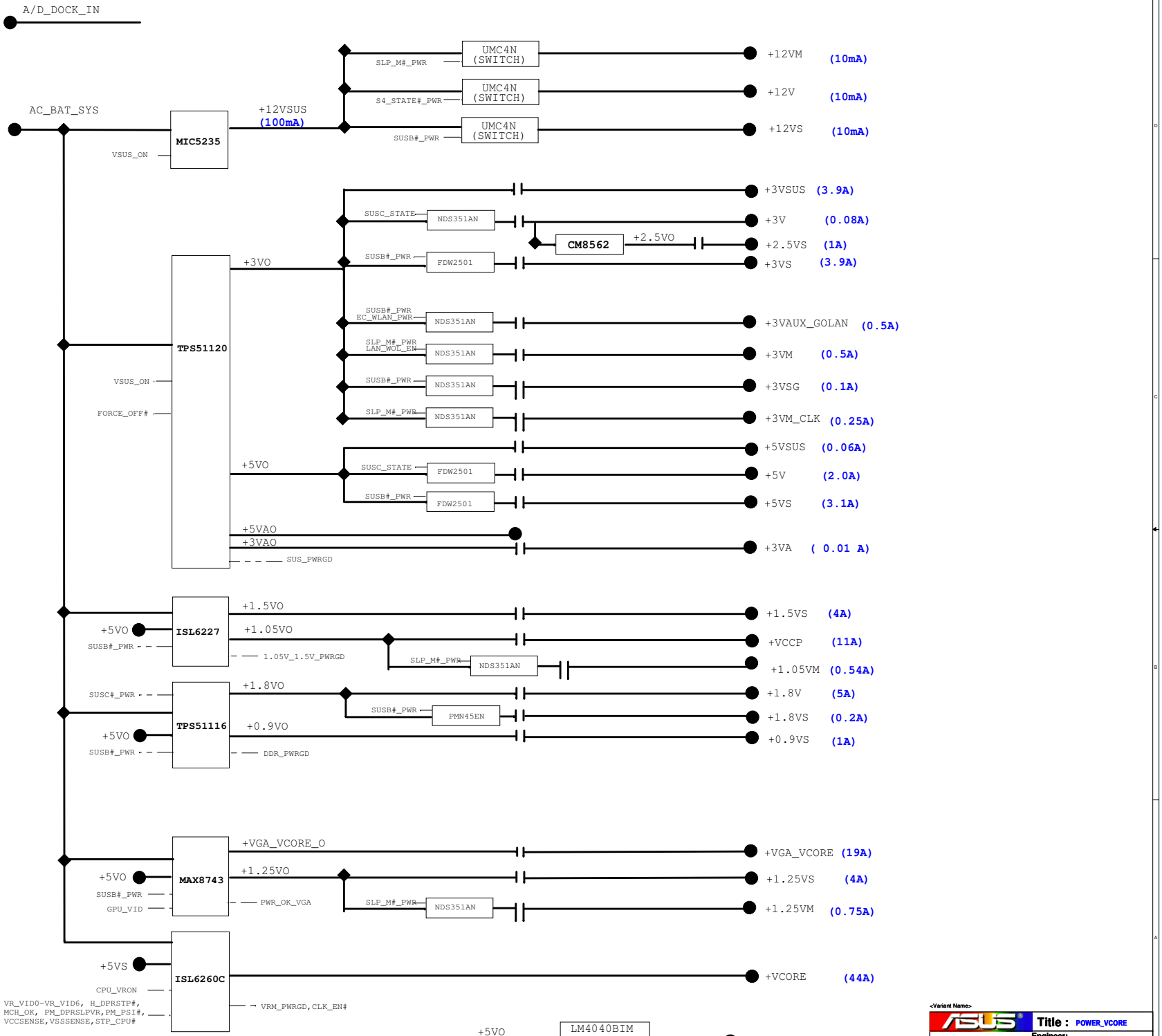
Title : POWER_LOAD SWITCH

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 91 of 95



<Variant Name>

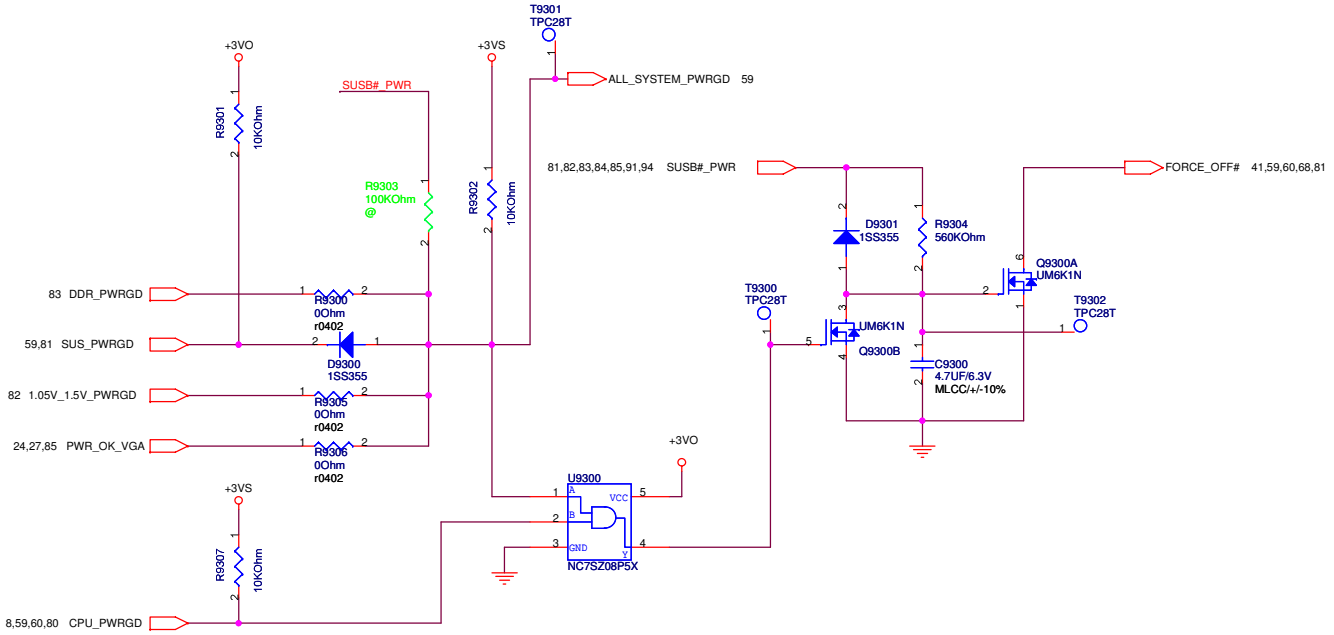
Title : POWER_VCORE

<OrgName> Engineer:

Size	Project Name	Rev
Custom	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 92 of 95

POWER GOOD DETECTER



<Variant Name>

Title : POWER_PROTECT

<OrgName>

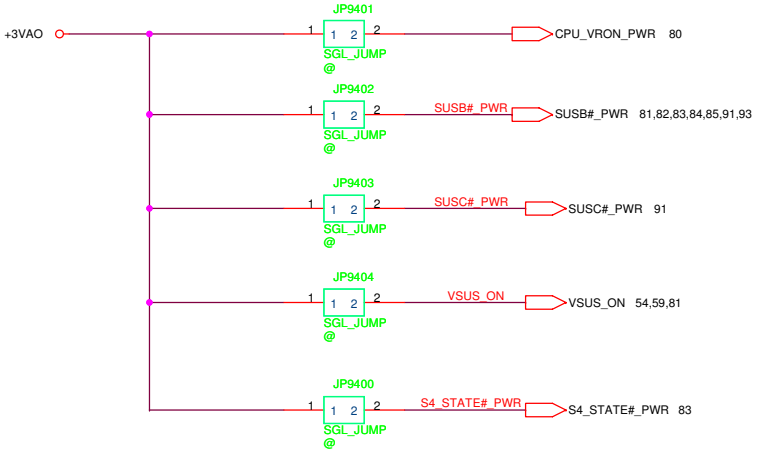
Engineer:

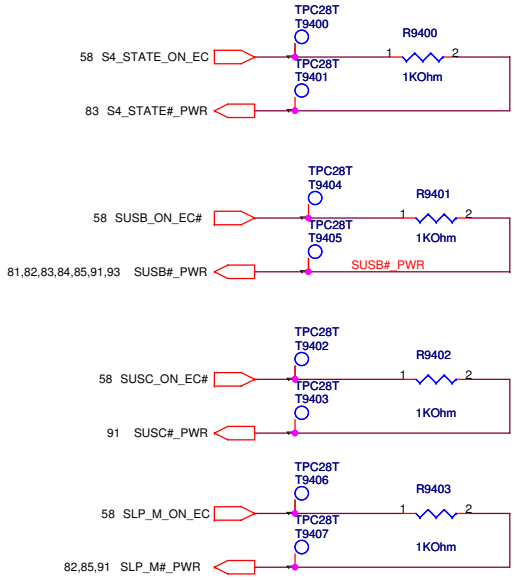
Size	Project Name	Rev
Custom	F7SR	1.1

Date: 星期四, 五月 10, 2007 Sheet 93 of 95

FOR POWER TEST

AC_BAT_SYS	AC_BAT_SYS	68,80,81,82,83,85,88
+3VA	+3VA	15,33,41,42,58,59,60,81
+1.5VSUS	+1.5VSUS	
+5VO	+5VO	66,81,82,83,84,85,88,90,91
+3VO	+3VO	81,84,85,91,93
+3VSUS	+3VSUS	16,17,18,44,45,54,59,81
+5VSUS	+5VSUS	18,66,81
+3V	+3V	33,42,45,47,49,54,57,76,78,91
+3VS	+3VS	4,8,12,15,16,17,18,32,33,35,37,42,44,47,48,49,51,52,53,54,56,57,59,60,66,70,72,73,76,80,84,91,93
+3VM	+3VM	17,18,20,21,39,65,84
+3VAUX_GOLAN	+3VAUX_GOLAN	
+3VM_CLK	+3VM_CLK	39,91
+12VSUS	+12VSUS	81,84,91
+12V	+12V	42,53,57,91
+12VS	+12VS	27,32,33,57,66,91
+5V	+5V	33,42,54,62,91
+5VS	+5VS	17,18,32,35,37,42,44,56,57,61,66,72,80,91
+2.5VO	+2.5VO	84
+2.5VS	+2.5VS	23,27,42,56,84
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	8,11,12,20,21,42,83
+VCCP	+VCCP	4,5,7,9,11,12,15,18,23,27,39,42,82
+1.05VM	+1.05VM	11,82
+0.9VO	+0.9VO	83
+0.9V	+0.9V	22,42,83
+0.9VS	+0.9VS	28,29,42,83
BAT	BAT	88
+2.5VREF	+2.5VREF	84,88,90
+VCORE	+VCORE	5,80
+VGA_VCORE	+VGA_VCORE	23,27,85
+VRAM	+VRAM	23,24,25,27,28,29,42,73,91
+1.25VS	+1.25VS	12,18,23,27,42,85
+1.25VM	+1.25VM	8,12,85
BAT_CON	BAT_CON	68,88
+1.1VS	+1.1VS	23,27,84





<Variant Name>

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7SR	Rev: 1.1
Date: 星期四, 五月 10, 2007	Sheet 94 of 95	

Rev	Date	Description
1.0	2006/07/	1. Initial release.
1.1	2006/09/29	1.Enable INTVRMEN and LAN100_SLP (Remove R1506, R1511).[15] 2.Change R0803 R0804 to 20ohm.[8] 3.Set PCIE graphic lane to normal mode.(Unmount R0809).[8] 4.Pull high 10Kohm at 3GSIM_DATA.[33] 5.Change INVCN0 to 20 pin.[33] 6.Change net name "INT_MIC_P" to "INTMIC_P".[56] 7.Change R5706 and R5707 to 75ohm.[56] 8.Change CE5701 and CE5702 to 100UF.[57] 9.Add +1.5V discharg circuit.[42] 10.Remove R5415.[54] 11.Change power "+12V" to "+12VS".[54] 12.Change R6401,R6403,R6409 to10KOhm.[64] 13.Change C2940 to0.1uF.[28] 14.Change EC_GPIO pin define for design IP.[59] 15.Add debounce and thermal circuit for EC design IP.[60] 16.Change C1612,C1613 to 0.1uF.[16] 17.Change C7302,C7308 to 10uF and remove C7315, C7307,C7321,C7301,C7309,C7313,C7310,C7320, C7321.[73] 18.Remove Q4401,Q5404 and change R1604 to 1Kohm.[16,44,54] 19.Revers D6602.[66] 20.Remove C4401,C4404.[44] 21.Colay M66/M76M.[23~30] 22.Connect ICH8M_LAN_RST# to GND.[17] 23.Add JACK detect circuit at DOS mode.[15] 24.Connect M_VREF_MCH to" 0.9V_VTT_REF".[8] 25.Change R0402 to 1Kohm.[4] 26.Change R3952 to 270Ohm.[39] 27.Swap "xD_GND1" and "xD_CD".[53] 28.Add R and C to avoid pop.[56] 29.Add 3G Led circuit.[66] 30.Connect "BUF_PLT_RST#" and "IDERST#" by 47Ohm.[72]

Rev	Date	Description

<Variant Name>

Title : History

ASUSTek COMPUTER INC

Engineer: Jack Chen

Size	Project Name	Rev
Custom	F3Se	1.1

Date: 星期四, 五月 10, 2007 Sheet 95 of 95