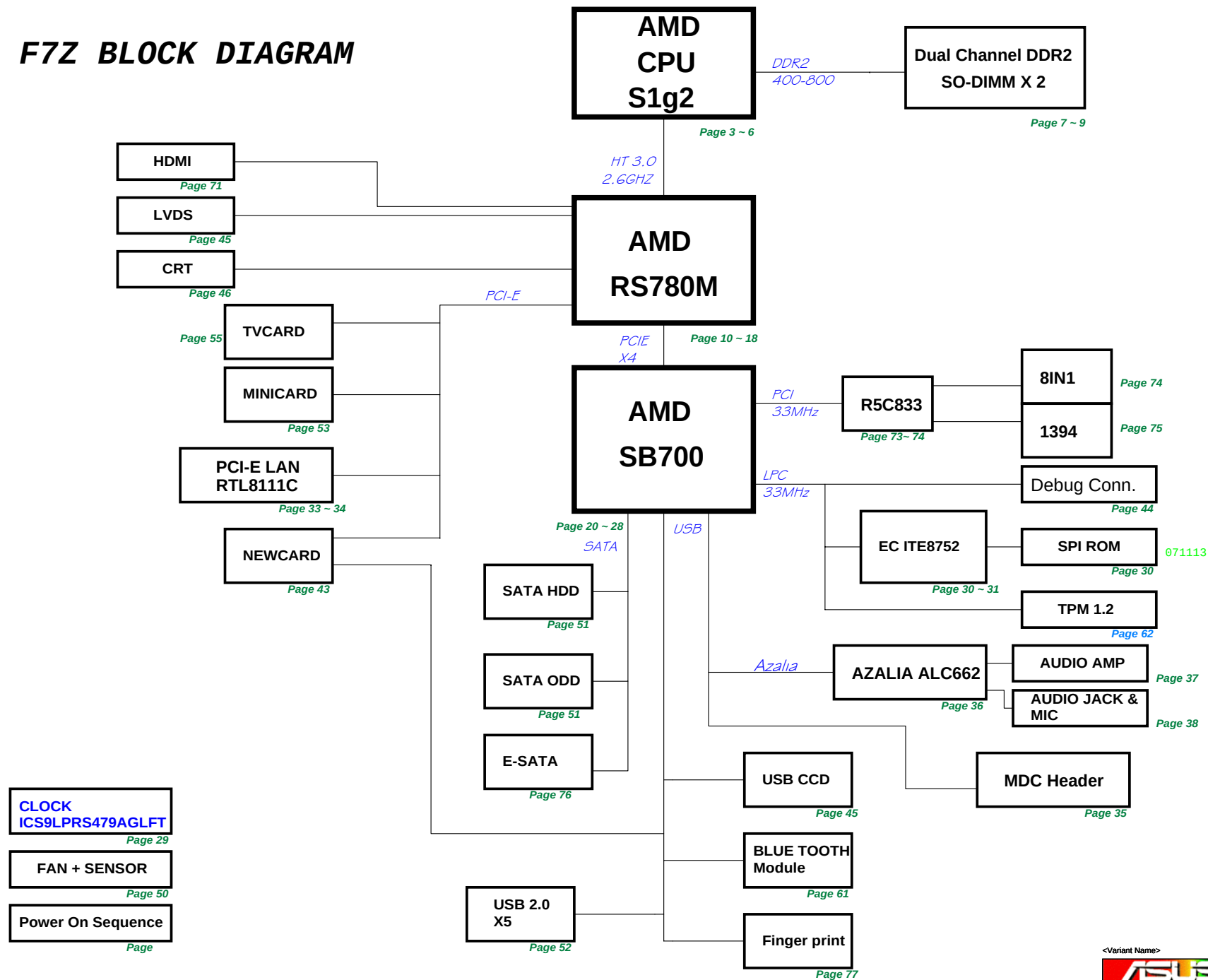
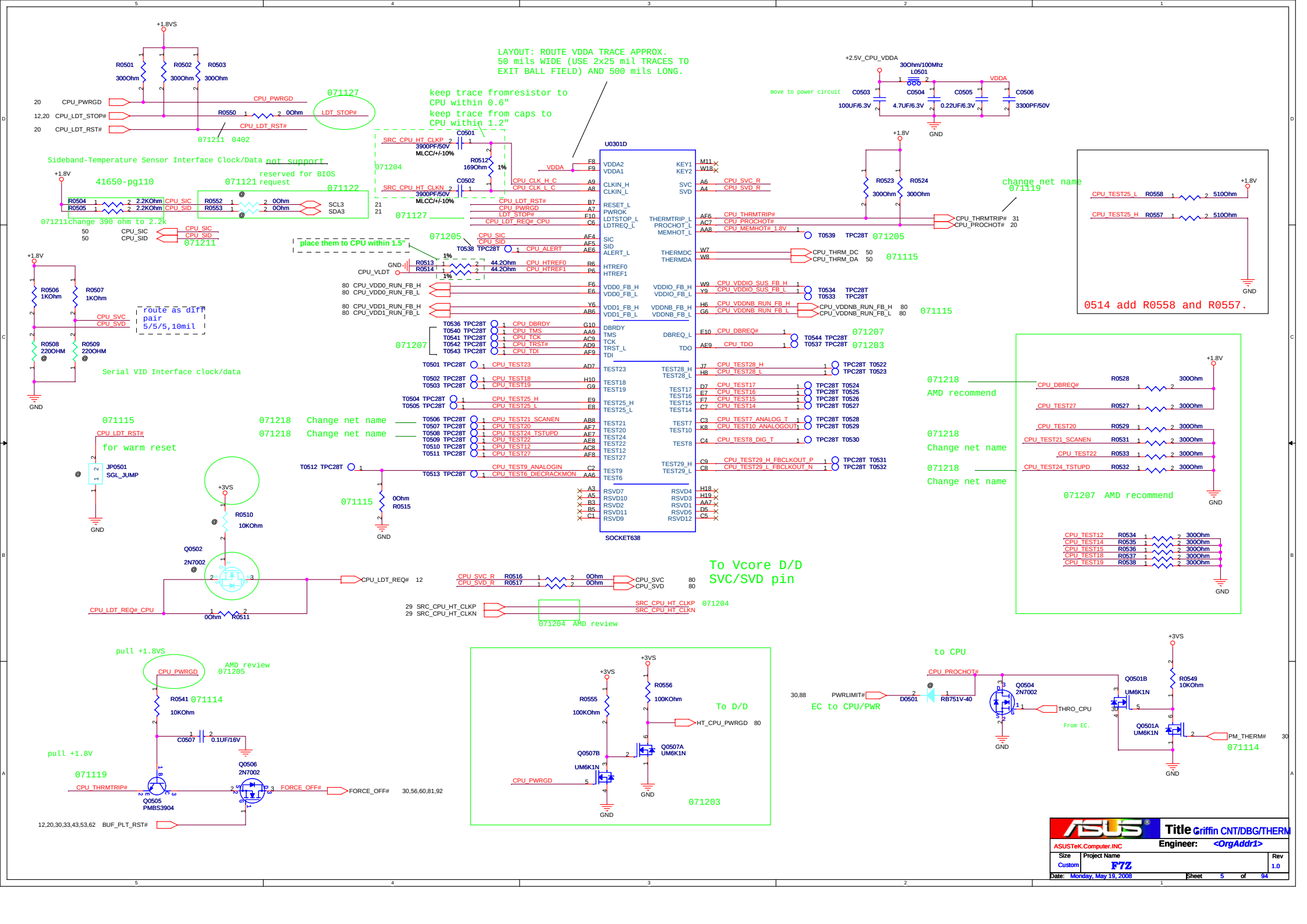
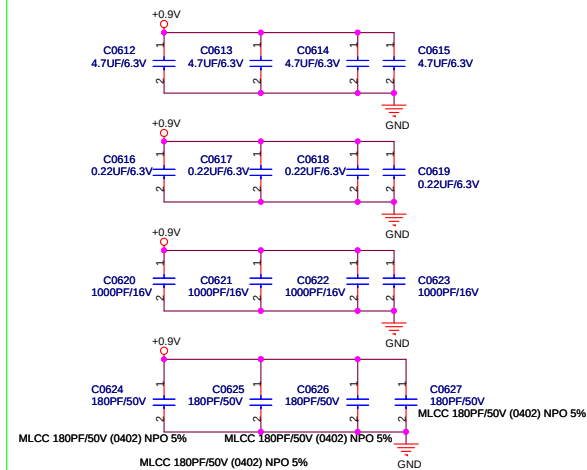
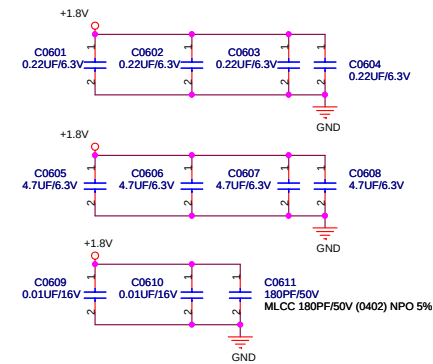
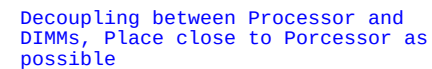
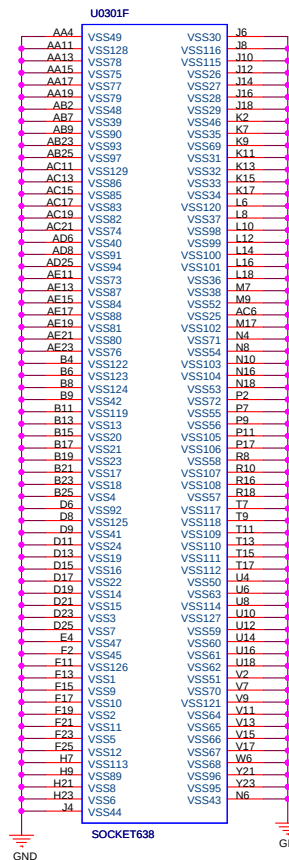
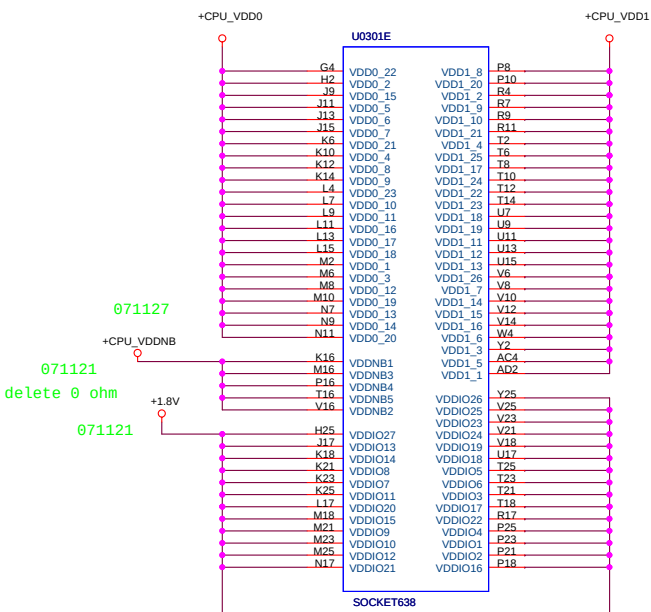


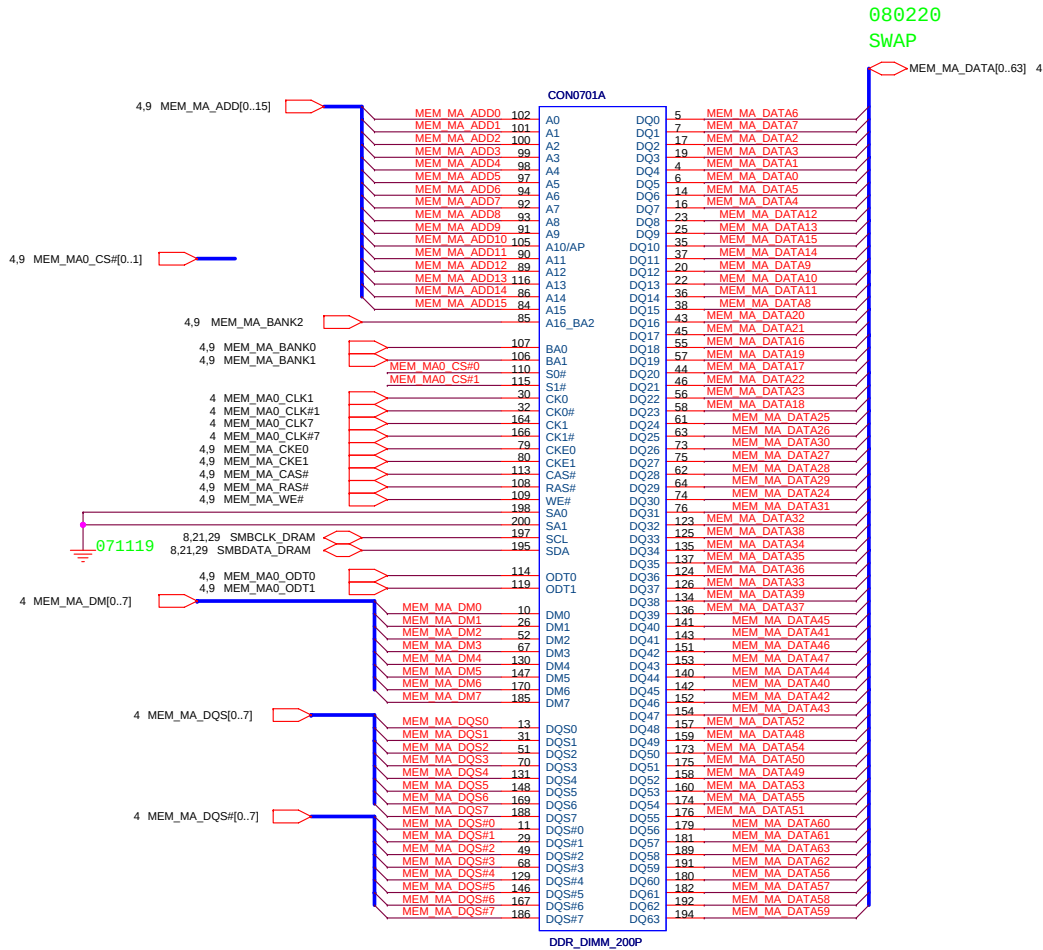
F7Z BLOCK DIAGRAM



	A	B	C	D	E
1					
2					
3					
4					
5					

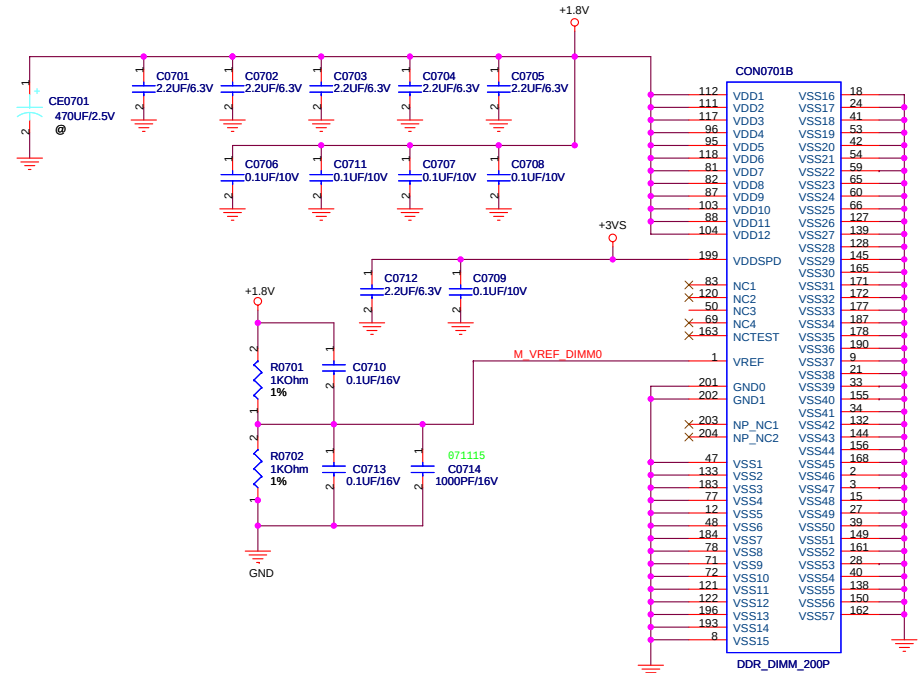




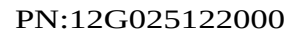
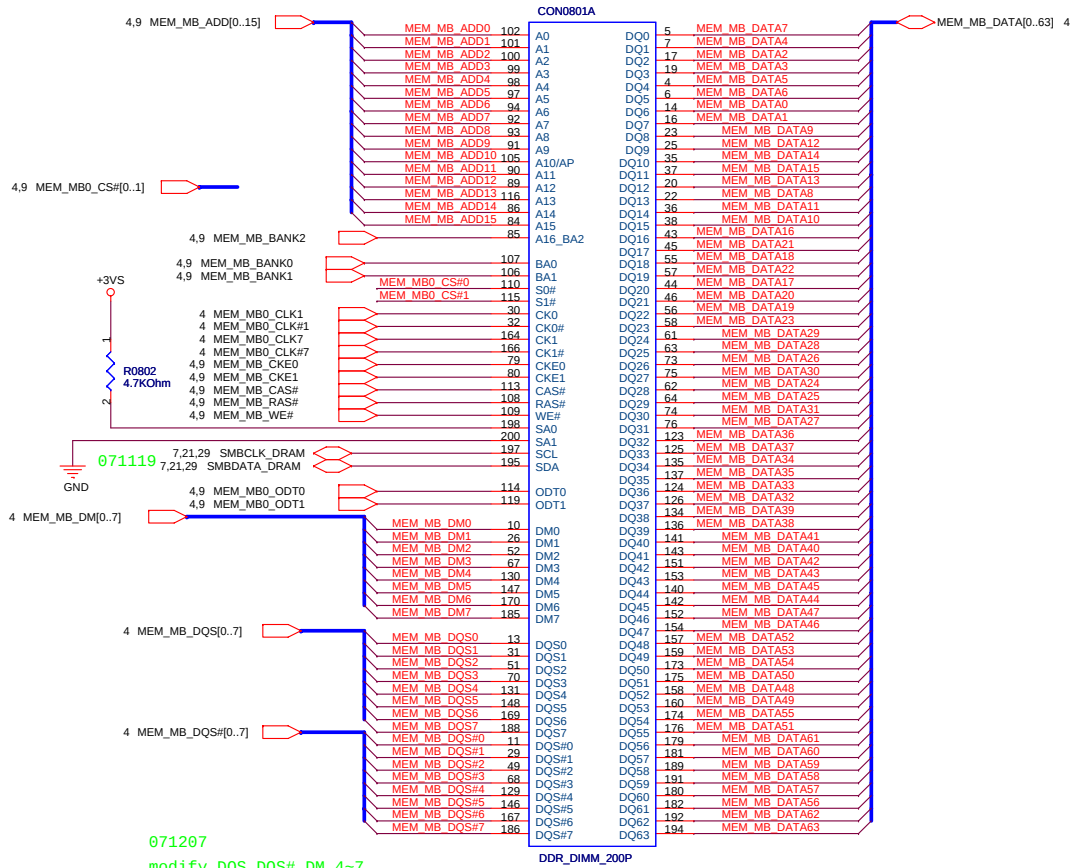


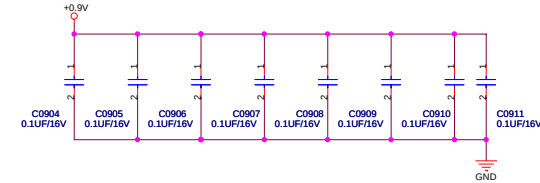
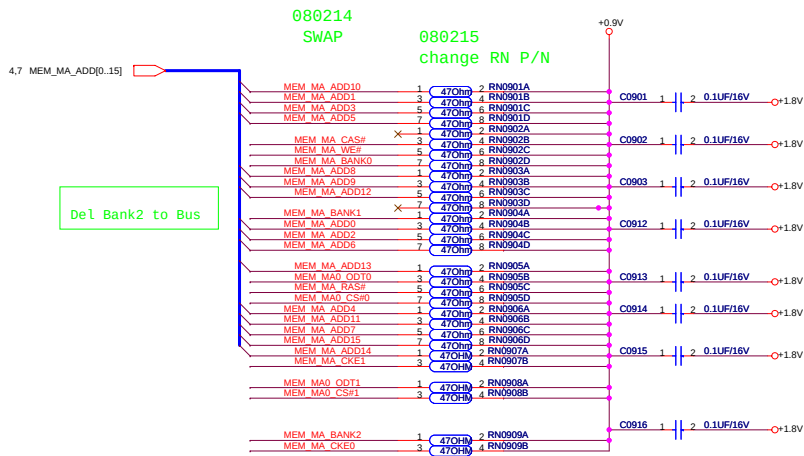
PN:12G025122006

modify 05/24



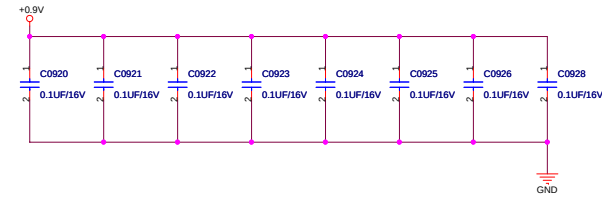
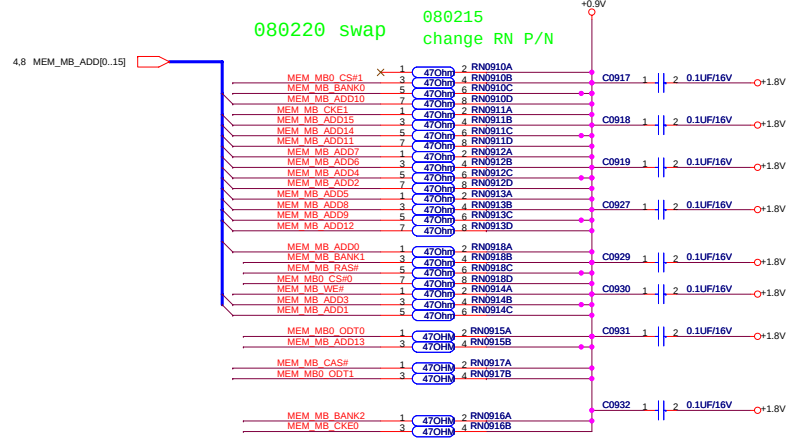
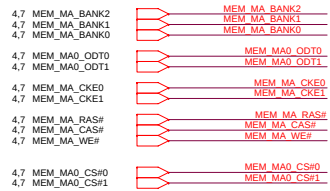
<Variant Name>



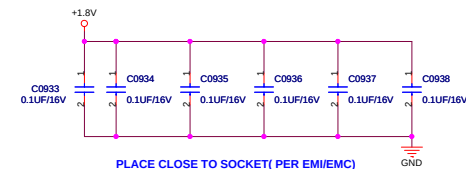
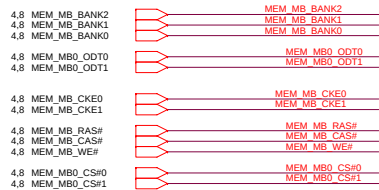


071207

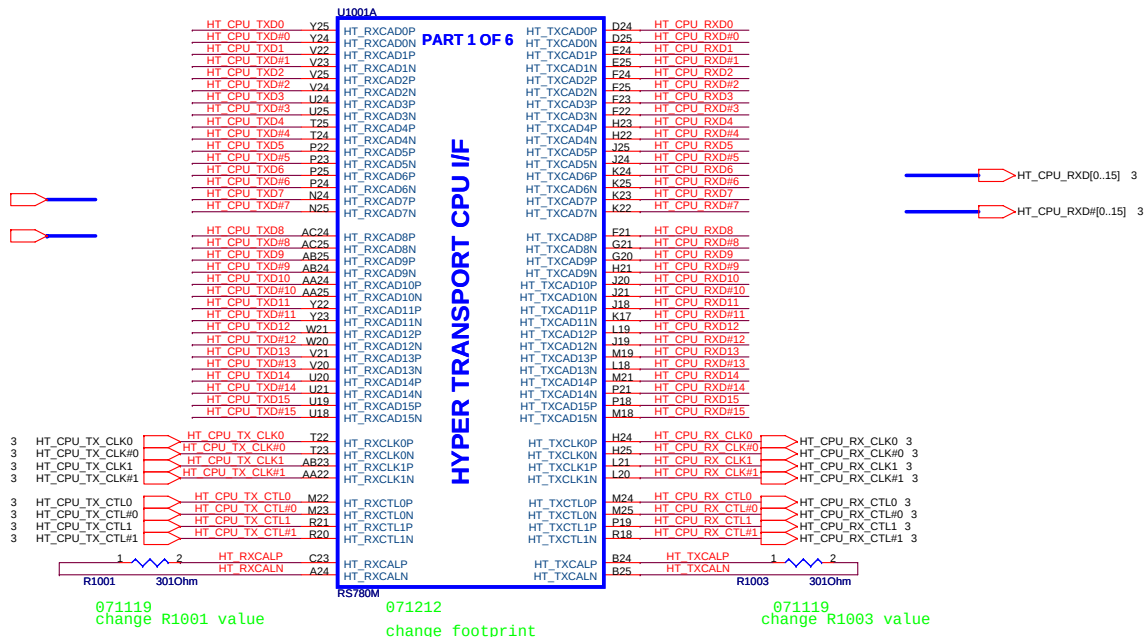
071121

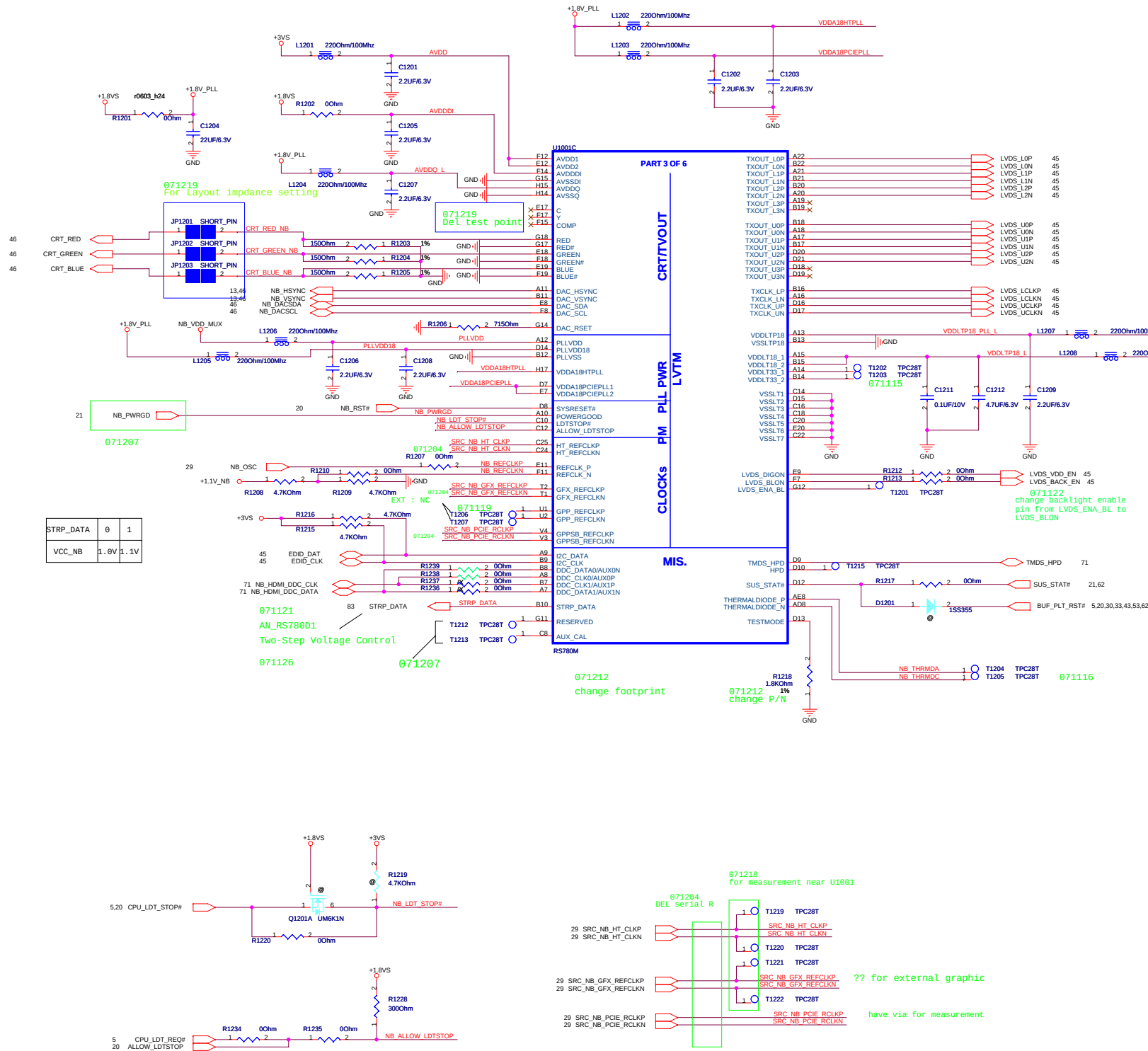


071211

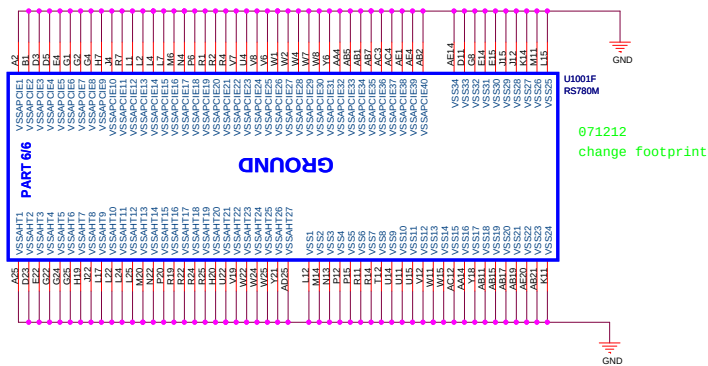
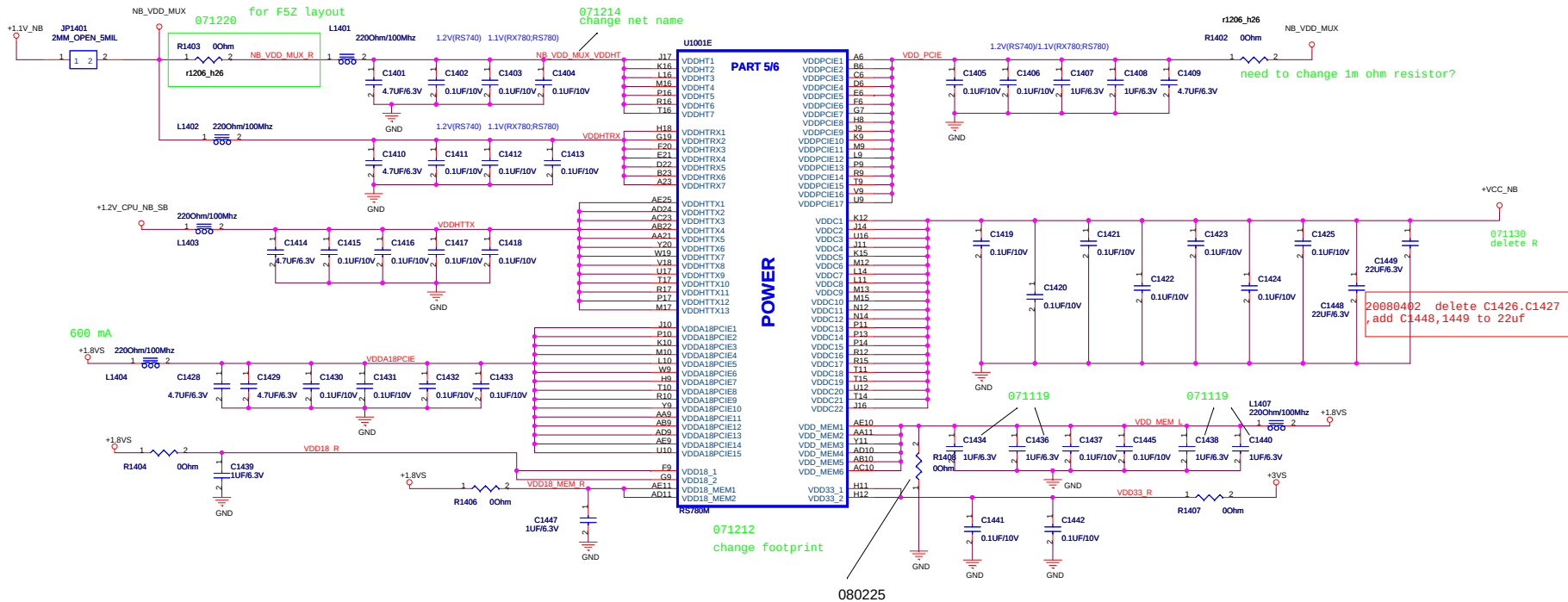


Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			











Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

Size

A

Project Name

F7Z

Rev

1.0

Date: Monday, May 19, 2008

Sheet 15 of 94

D

C

B

A



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

Size

A

Project Name

F7Z

Rev	
-----	--

1.0

Date: Monday, May 19, 2008

Sheet 16 of 94

D

C

B

A



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

Size

A

Project Name

F7Z

Rev

1.0

Date: Monday, May 19, 2008

Sheet 17 of 94

5

4

3

2

1

D

D

C

C

B

B

A

A



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

Size

A

Project Name

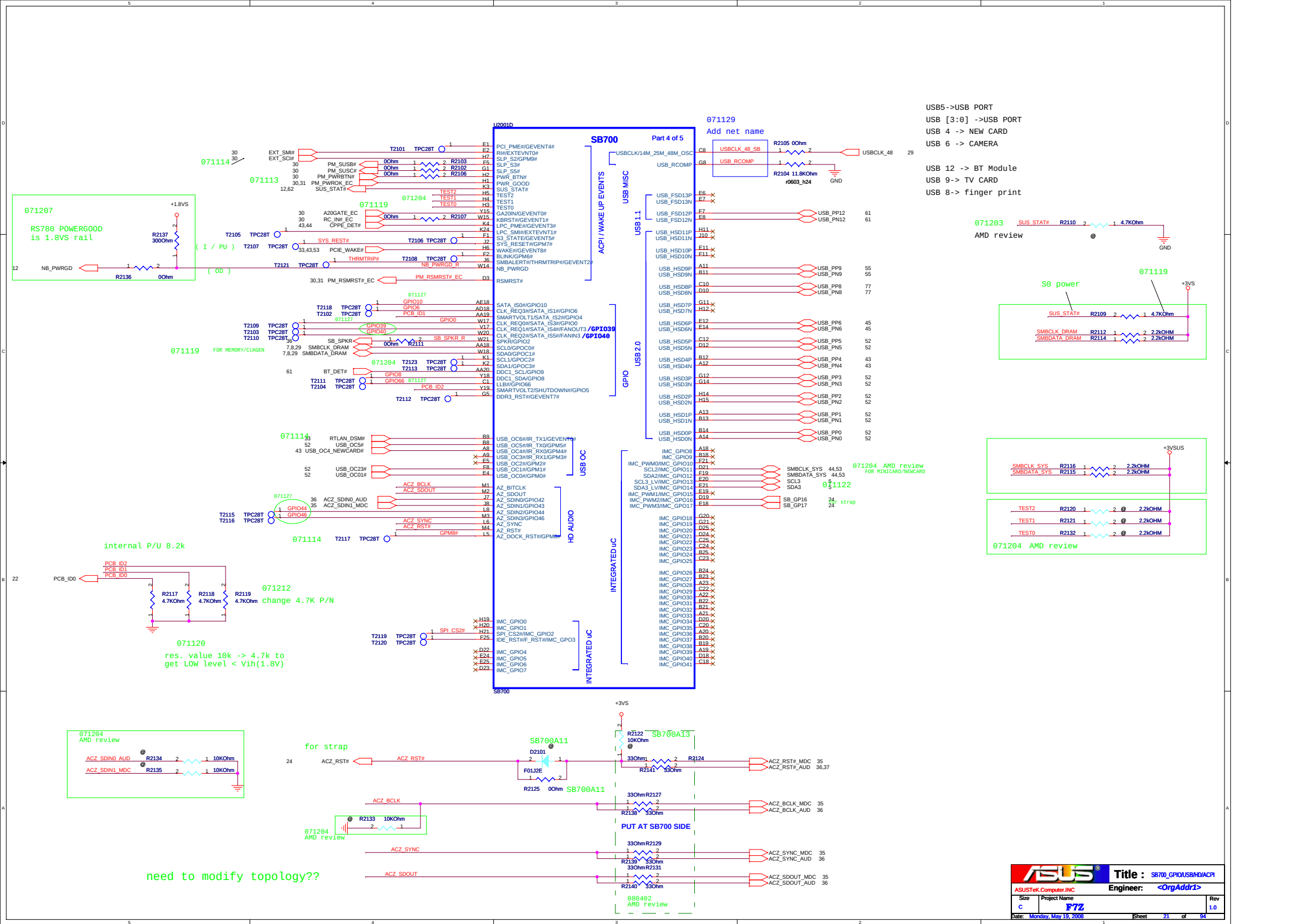
F7Z

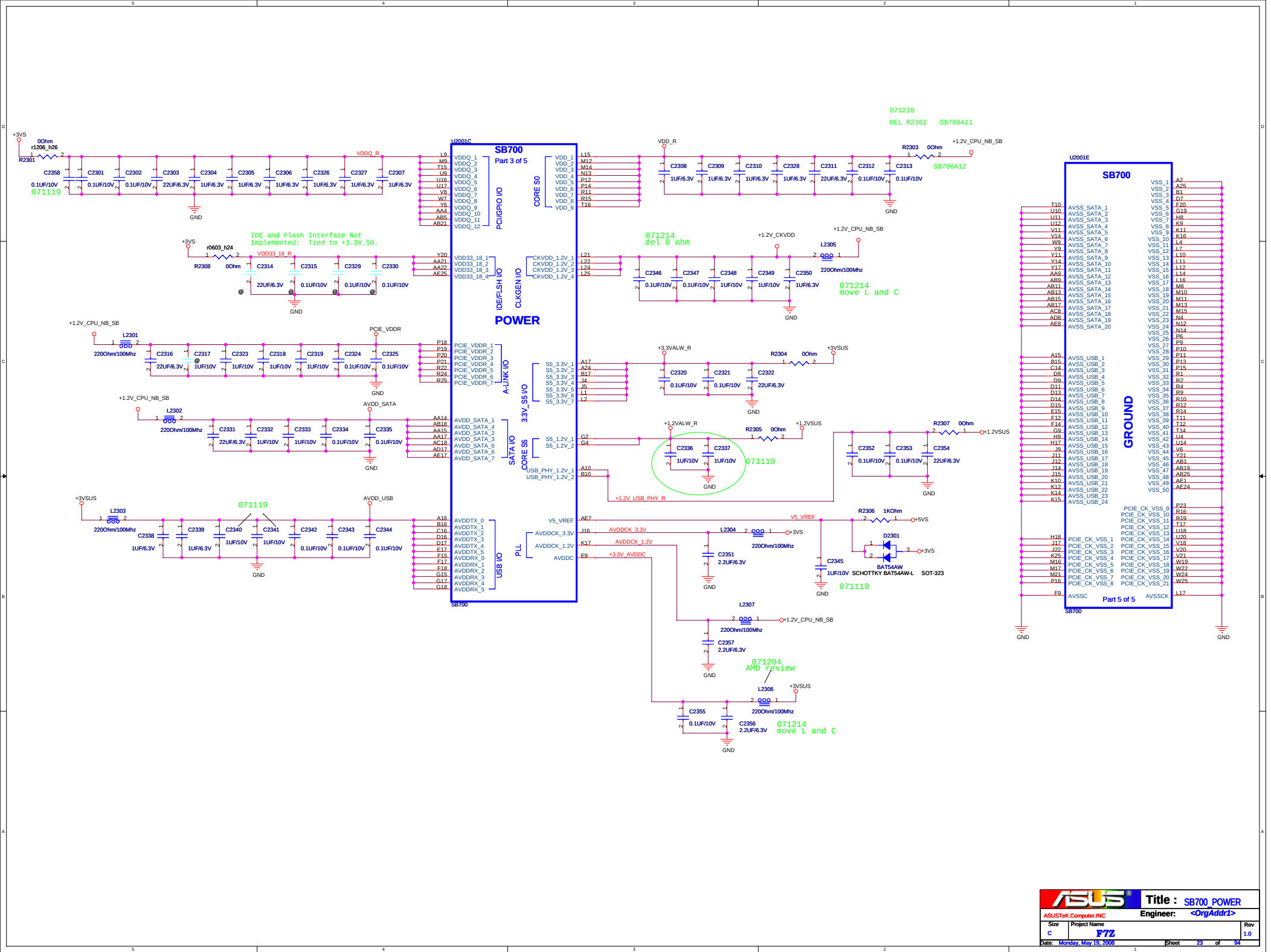
Rev

1.0

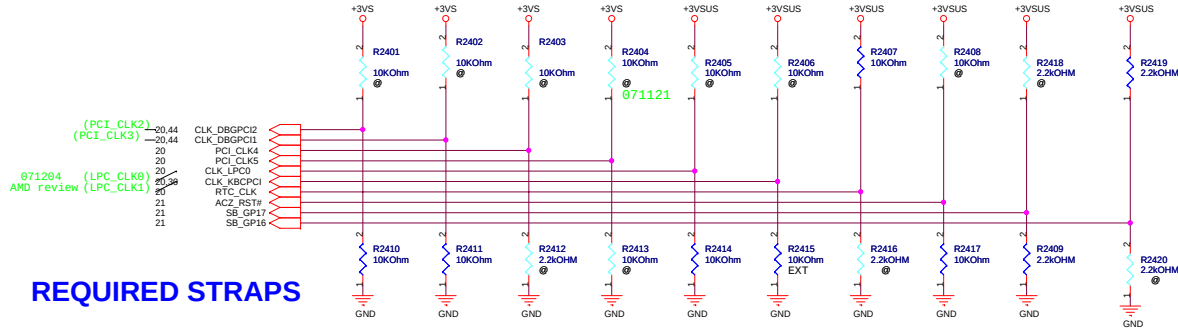
Date: Monday, May 19, 2008

Sheet 19 of 94



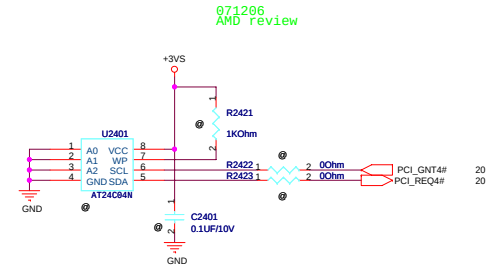


NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC	EC ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS			DISABLE PCI MEM BOOT	CLKGEN DISABLED	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.



D

C

B

A |



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

Size

A

Project Name

F7Z

Rev

1.0

Date: Monday, May 19, 2008

Sheet 26 of 94

D

C

B

A



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

Size

A

Project Name

F7Z

Rev

1.0

Date: Monday, May 19, 2008

Sheet 27 of 94

D

C

B

A



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *<OrgAddr1>*

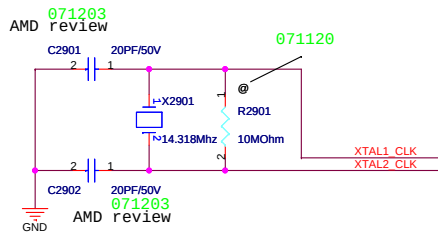
Size
A

Project Name	Rev
F7Z	1.0

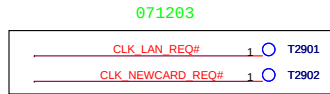
Rev
1.0

Date: Monday, May 19, 2008

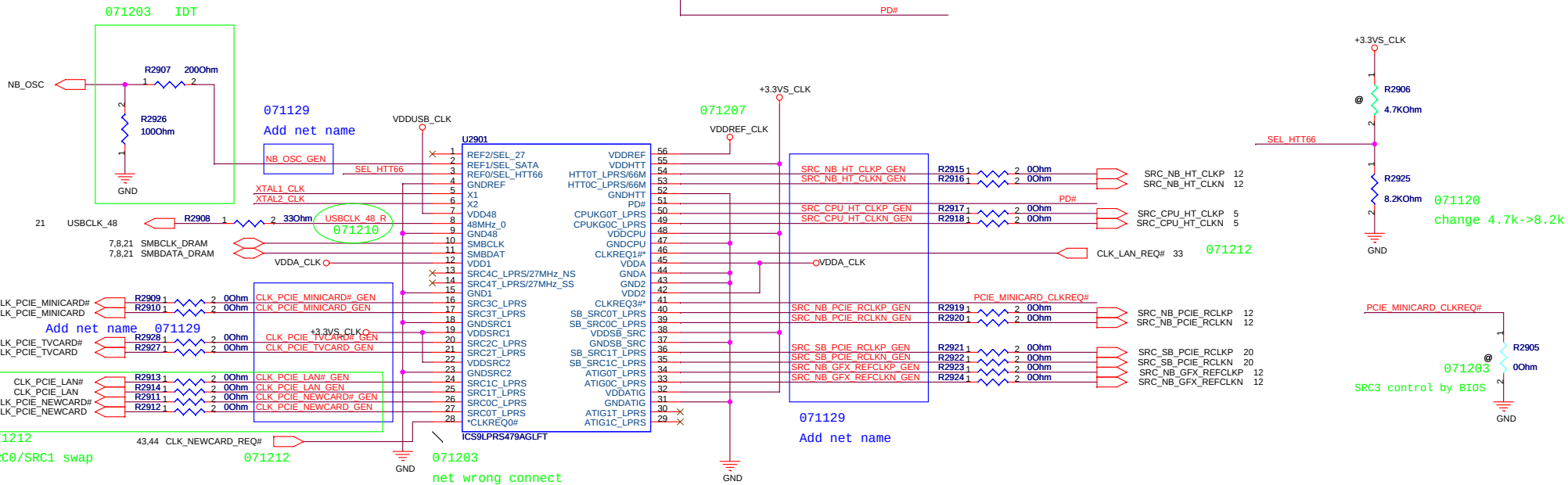
Sheet 28 of 94



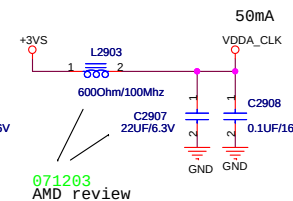
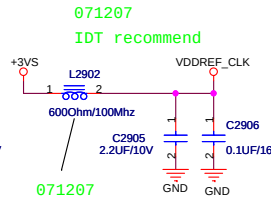
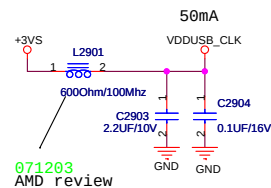
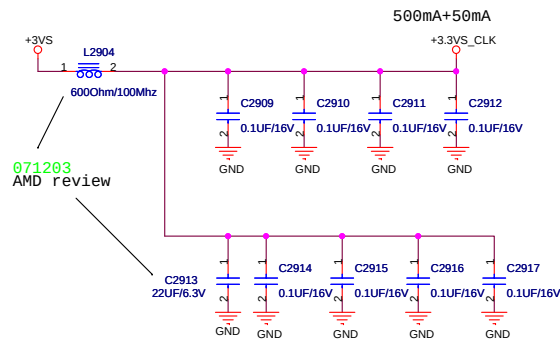
Modify to NC



SEL_HTTP66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock



Change from 489 to 479

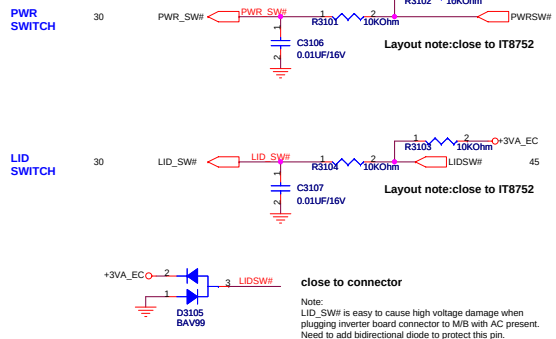


For Battery

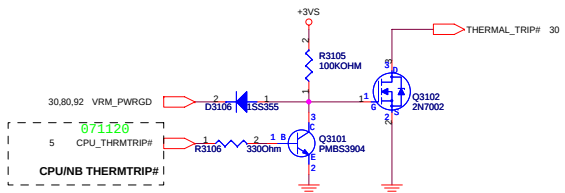
Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

In Page 60

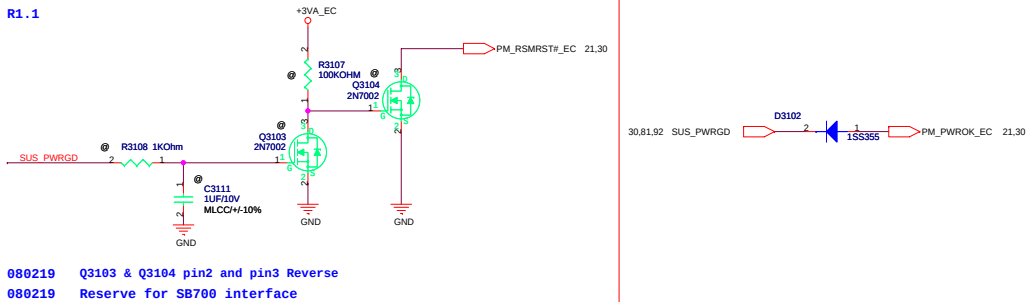
For Switch



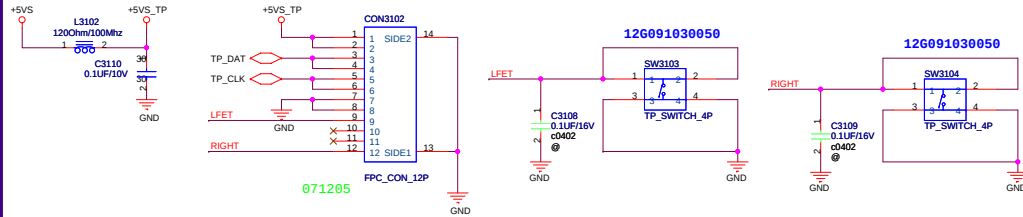
For Thermal Control Method



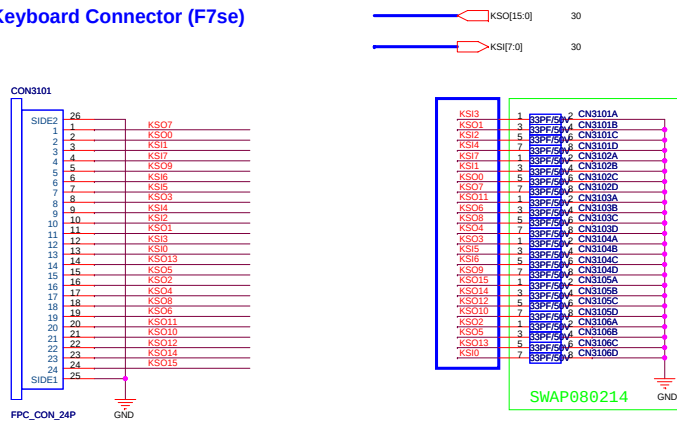
R1.1



Touch-Pad (F7se)

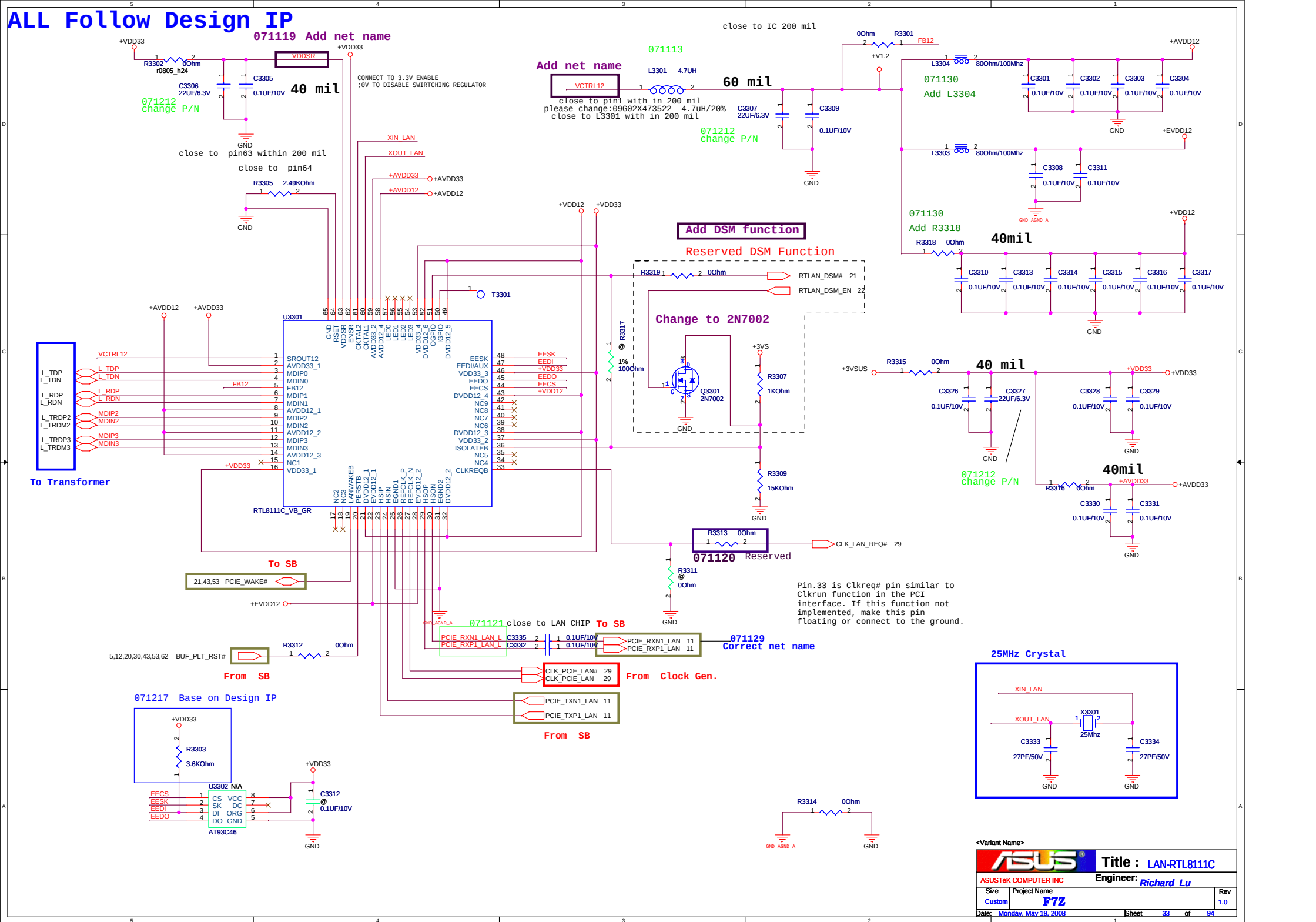


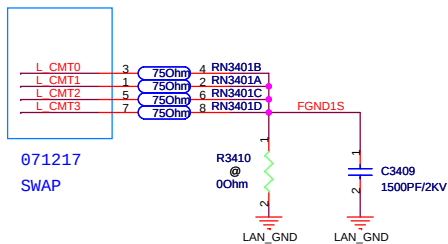
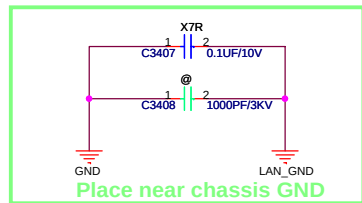
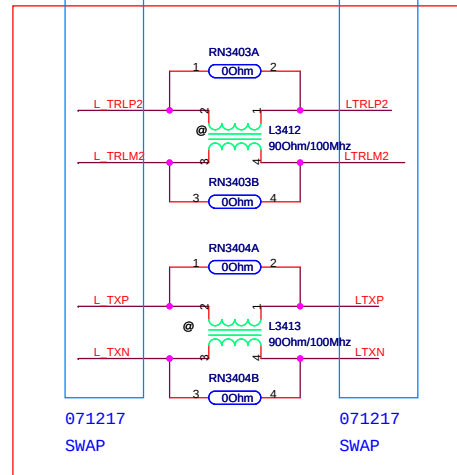
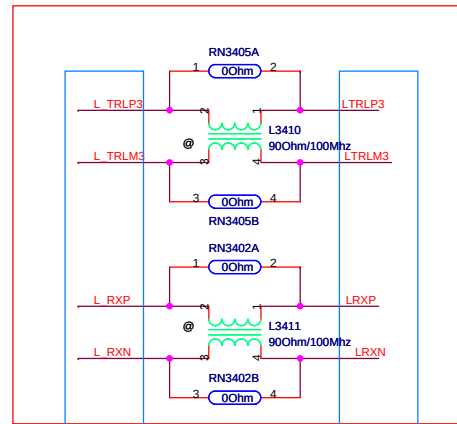
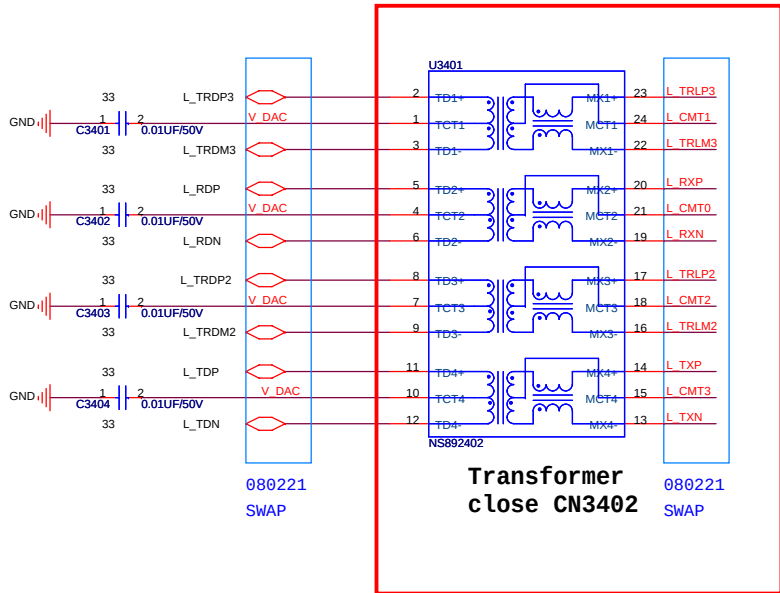
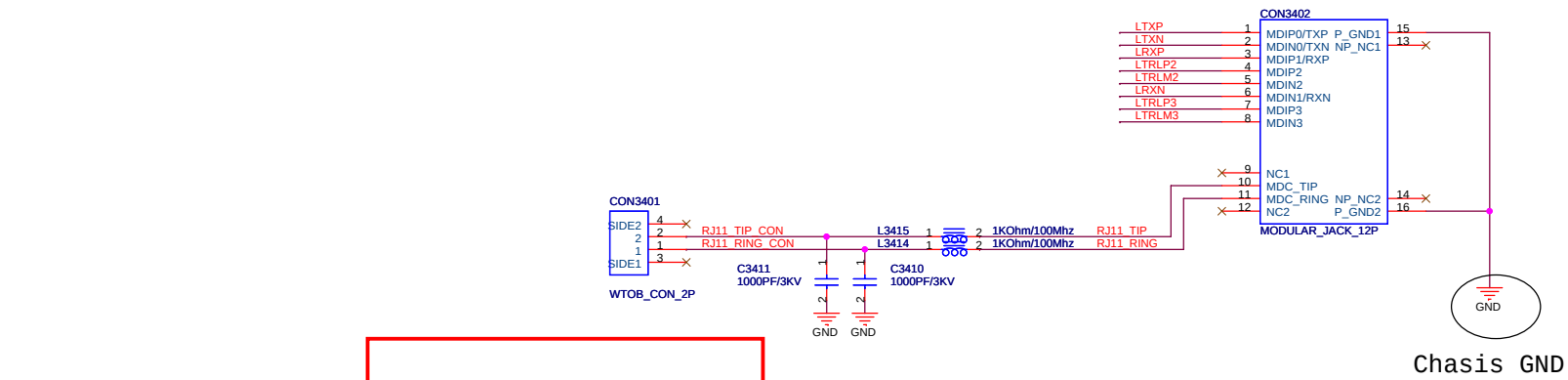
Keyboard Connector (F7se)



Remove all RST SCH and Change SW to other page

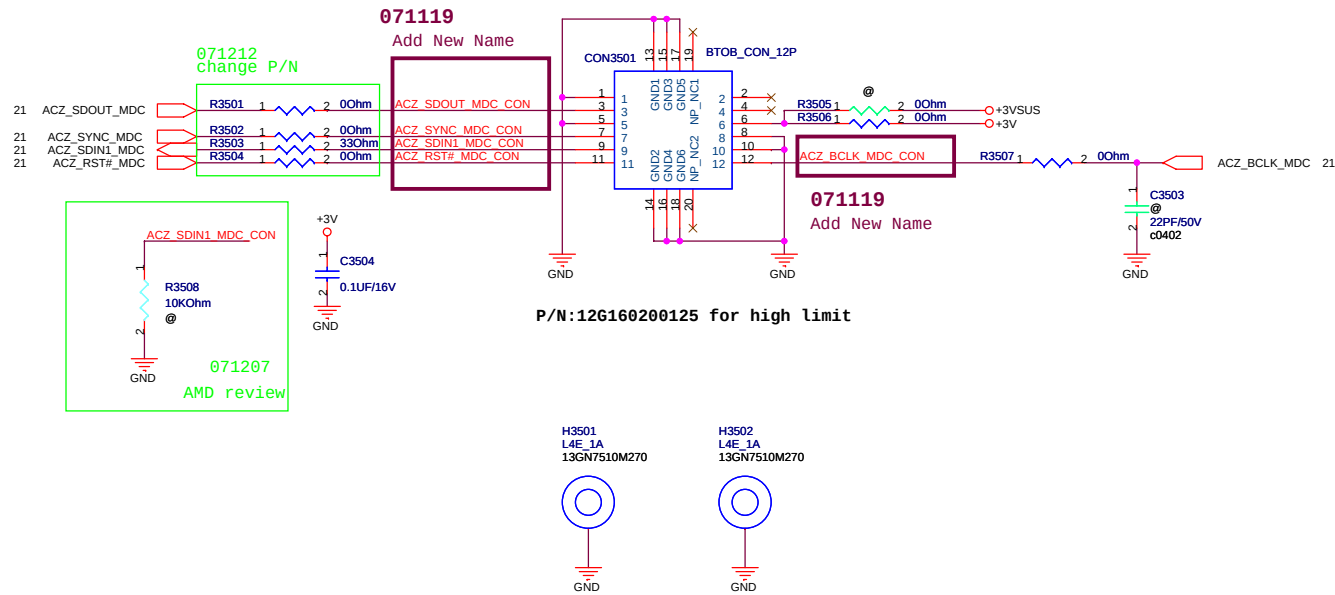
5	
ALL Follow Design IP	





<Variant Name>

MDC



<Variant Name>

ASUS		Title : LAN-MDC	
ASUSTek COMPUTER INC		Engineer: Richard Lu	
Size Custom	Project Name F7Z	Rev 1.0	
Date: Monday, May 19, 2008	Sheet 35 of 94		

AMP POWER

GAIN0	GAIN1	Av(1mv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

SPEAKER AMP

The diagram illustrates the electrical connections between the AMP POWER and SPEAKER AMP sections. Key components include:

- Input Stage:** +5VS_AMP and +5VS inputs are connected through capacitors C3701, C3702, and C3703 to the GND_AUDIO rail.
- Signal Source:** An 800nm/100Mhz signal source is connected to the input stage via a 100Ohm resistor.
- IC Connections:** The U3701 IC (G1431F2U) has its GND pins connected to GND_AUDIO, its VDD pin connected to +5VS_AMP, and its SHUTDOWN pin connected to GND.
- Output Stage:** The AC_OUTA_L and AC_OUTA_R outputs of the IC are connected to the H_SPK+ and H_SPK- speaker terminals. These outputs pass through capacitors C3706, C3707, and C3708 before reaching the speakers.
- Resistors:** Various resistors (R3702, R3703, R3704) are used for impedance matching and signal conditioning throughout the circuit.
- Capacitors:** Numerous capacitors (C3701-C3708) are used for decoupling, filtering, and timing purposes.

MUTE CONTROL

When Q3711A $V_{gs(th)} > 2V$, please mount R3374 by using VISTA in-box driver for ALC8XX

ALC663 has no 660_D_MUTE#

CON3701

4 SIDE2

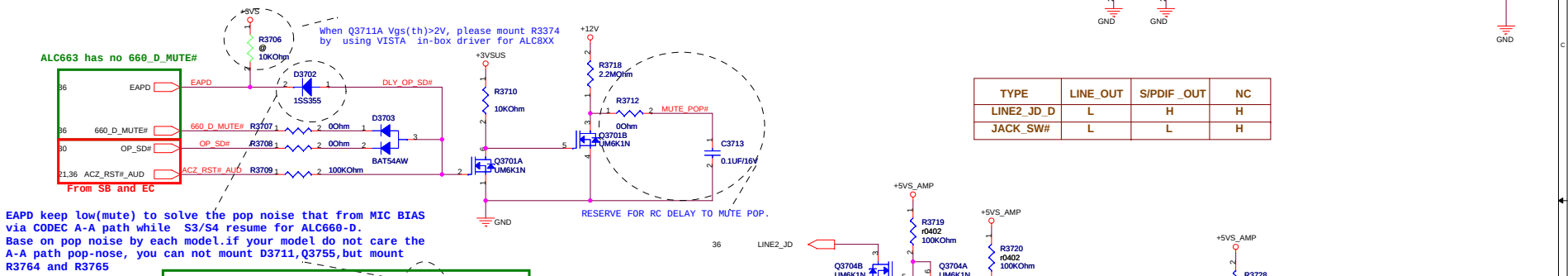
3

2

1 SIDE1

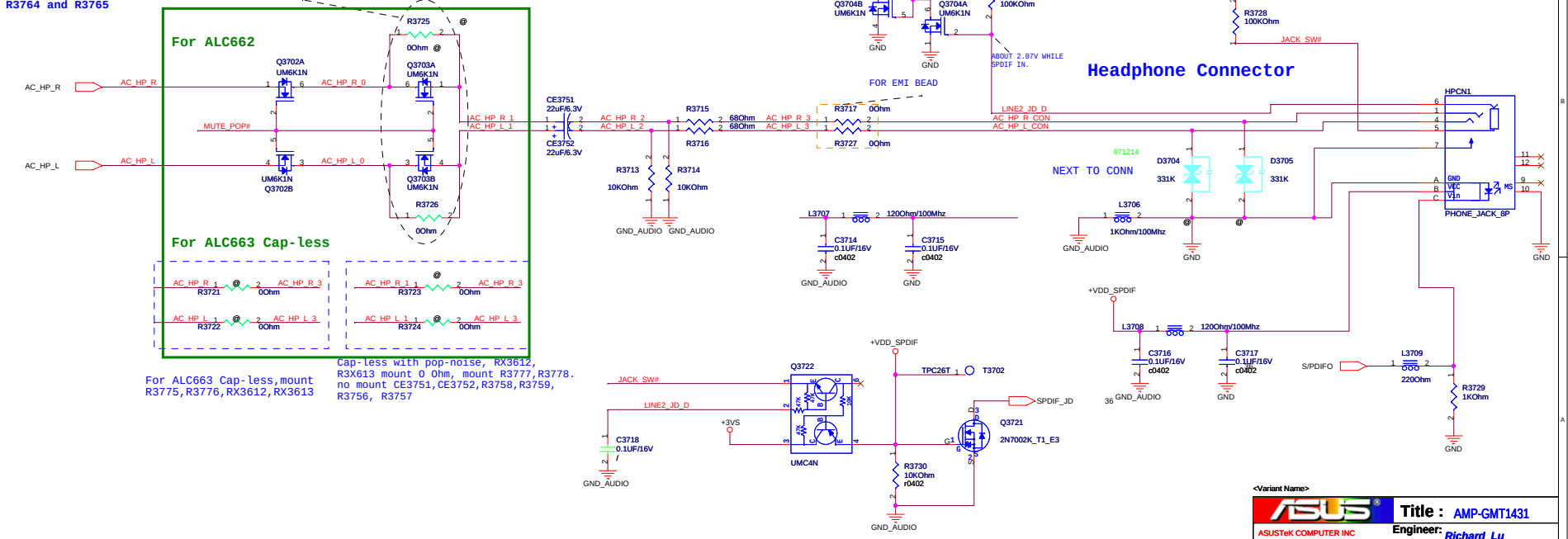
WTB0_CON_4P

GND

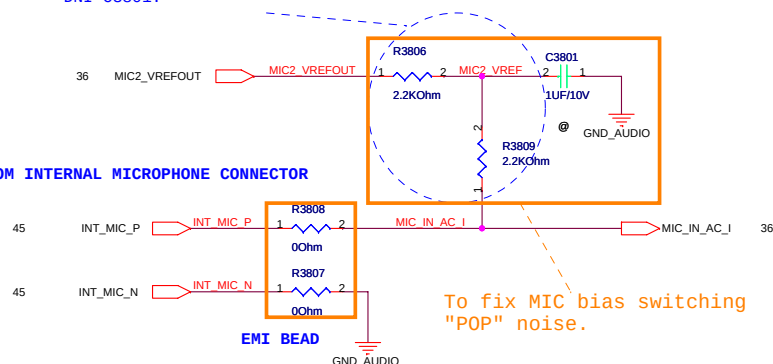


TYPE	LINE_OUT	S/PDIF_OUT	NC
LINE2_JD_D	L	H	H
JACK_SW#	L	L	H

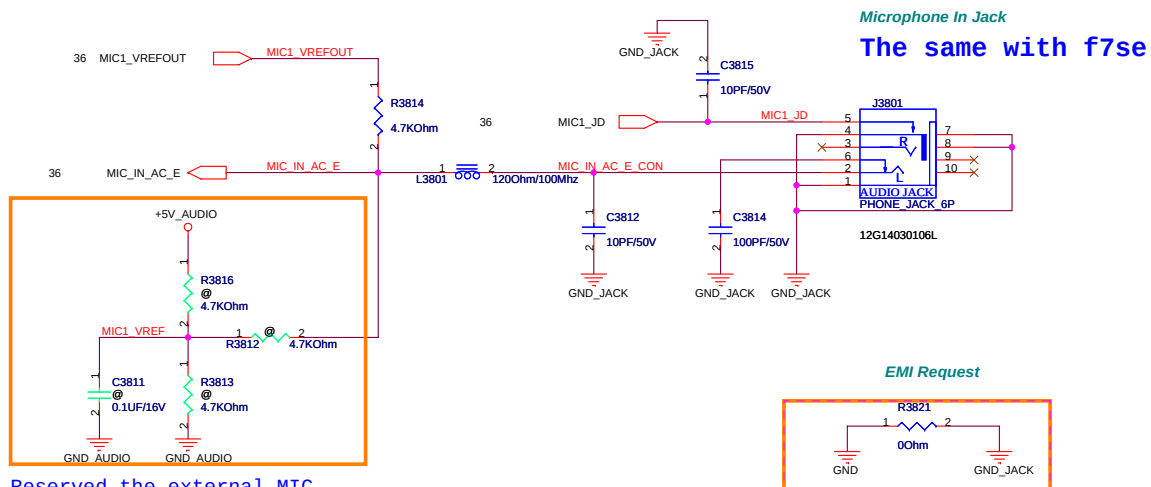
EAPD keep low(mute) to solve the pop noise that from MIC BIAS via CODEC A-A path while S3/S4 resume for ALC669-D. Base on pop noise by each model.if your model do not care the A-A path pop-noise, you can not mount D3711,Q3755,but mount R3764 and R3765



FROM INTERNAL MICROPHONE CONNECTOR



EXTERNAL MICROPHONE



F7Z

		Title : MIC-IN Jack	
ASUSTek COMPUTER INC		Engineer: <u>Richard Lu</u>	
Size Custom	Project Name F7Z		Rev 1.0
Date: <u>Monday, May 19, 2008</u>		Sheet <u>38</u>	of <u>94</u>

D

C

B

A

D

C

B

A

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Custom
------	--------

Project Name	F7Z
--------------	------------

Rev	
1.0	

Date: Monday, May 19, 2008

Sheet 41 of 94

D

C

B

A

D

C

B

A

5

4

3

2

1

<Variant Name>



Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

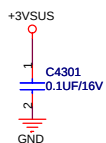
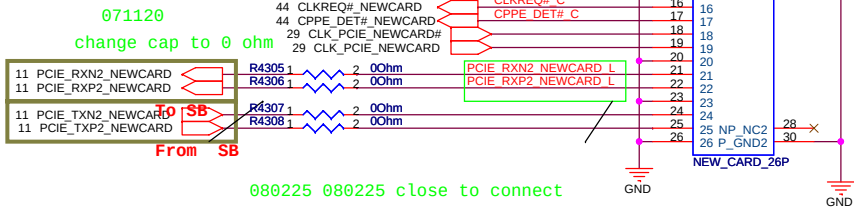
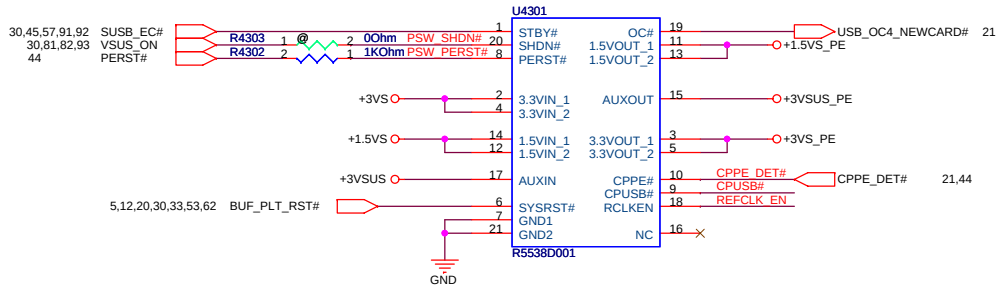
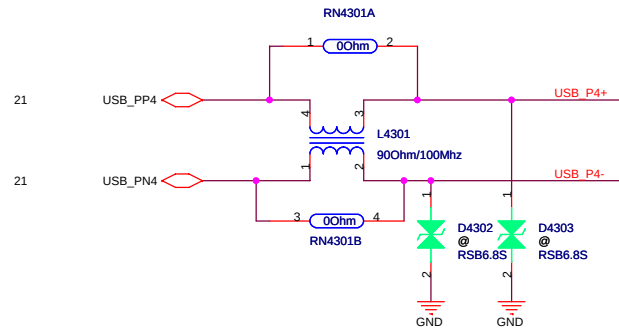
Size	Custom
------	--------

Project Name	F7Z
--------------	------------

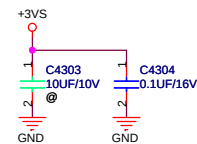
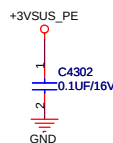
Rev	
1.0	

Date: Monday, May 19, 2008

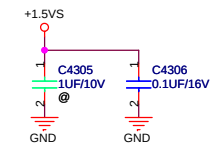
Sheet 42 of 94



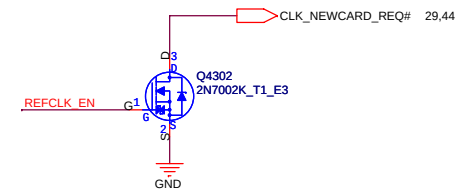
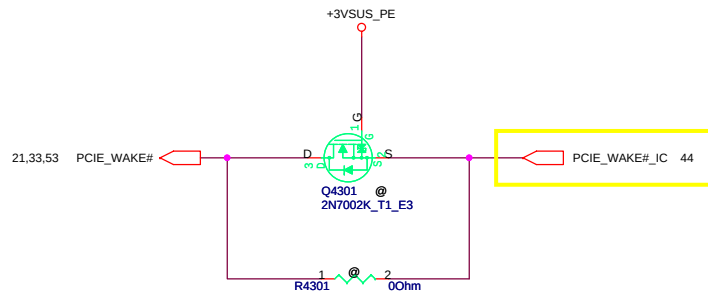
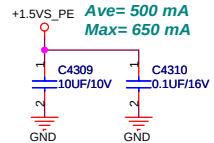
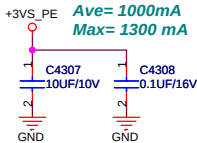
3.0V~3.6V
Ave= 200mA
Max= 275
mA



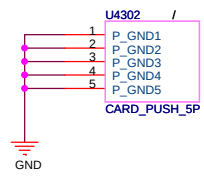
3.0V~3.6V
Ave= 1000mA
Max= 1300 mA



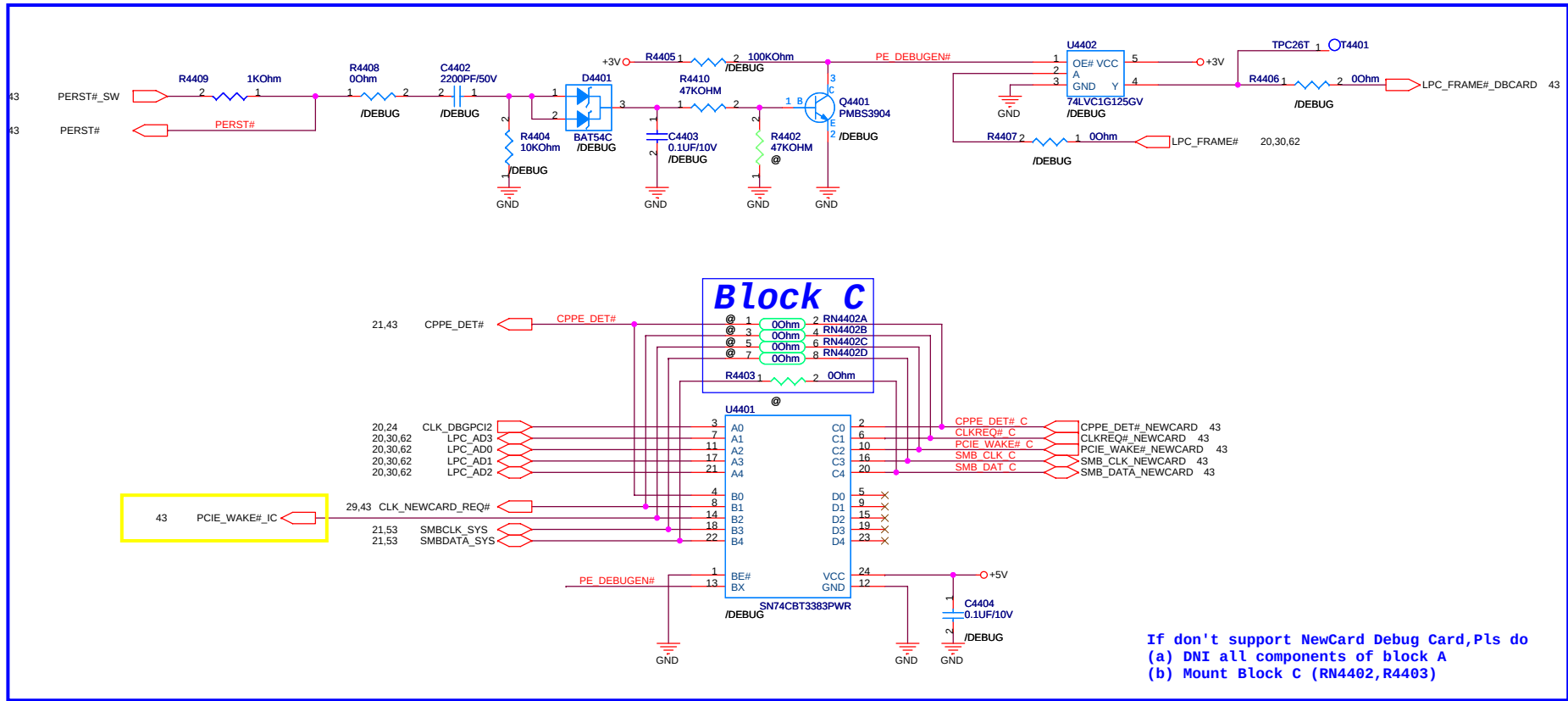
1.35V~1.65V
Ave= 500 mA
Max= 650 mA



NewCard
Ejecter

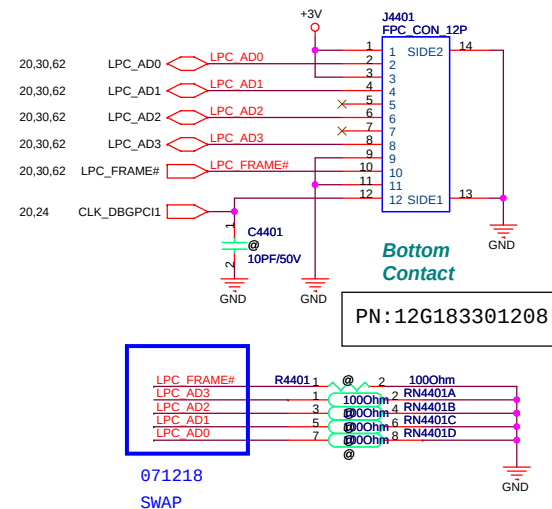


Block A



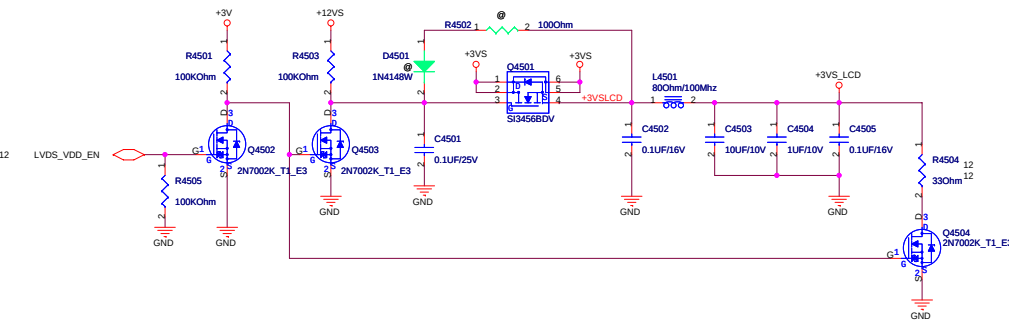
For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.



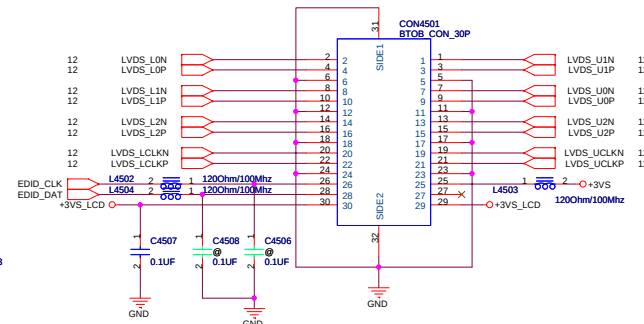
LCD Backlight Control

LCD Power



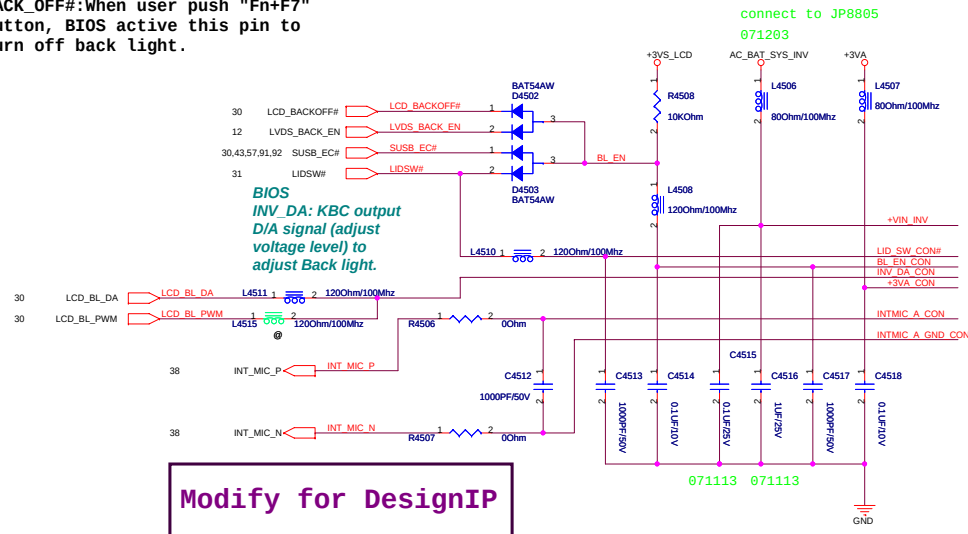
LCD LVDS Interface

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



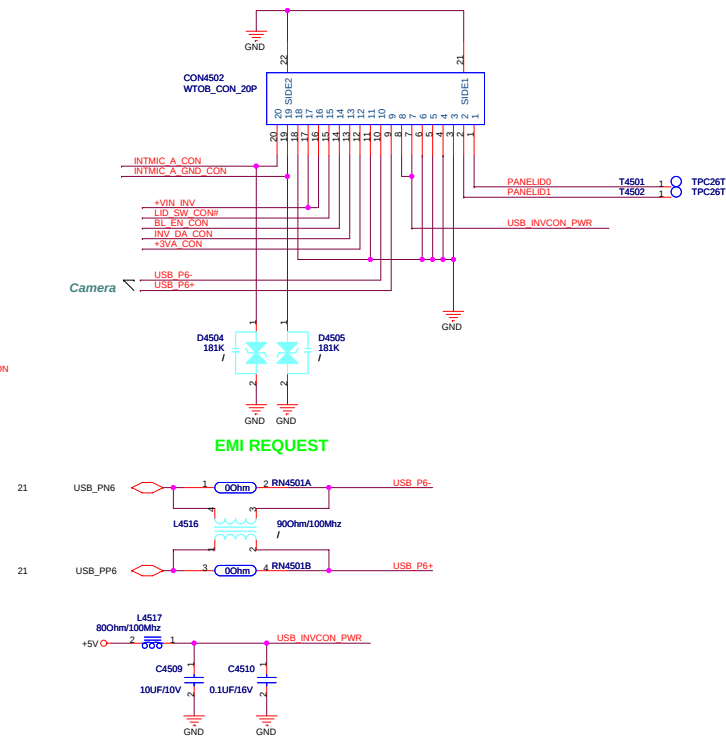
INVERTER Interface

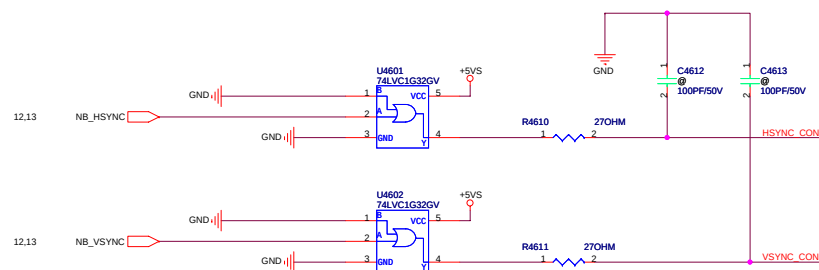
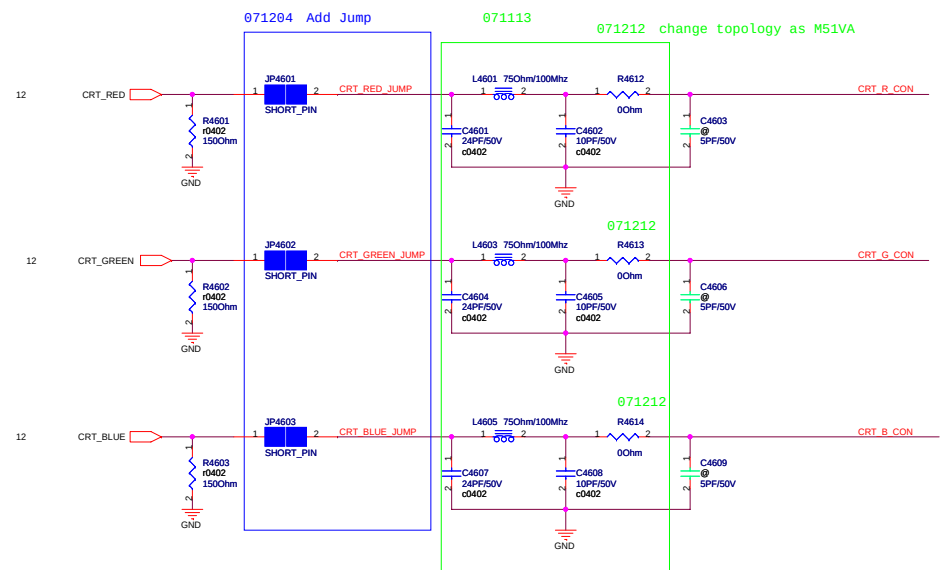
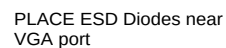
BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.



INVERTER
Interface/Speaker CONN.

Delete LID_SW SCH





	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

<Variant Name>

		Title : *	
ASUSTeK COMPUTER INC		Engineer: <i>Richard Lu</i>	
Size A	Project Name F7Z		Rev 1.0
Date: Monday, May 19, 2008		Sheet	47 of 94

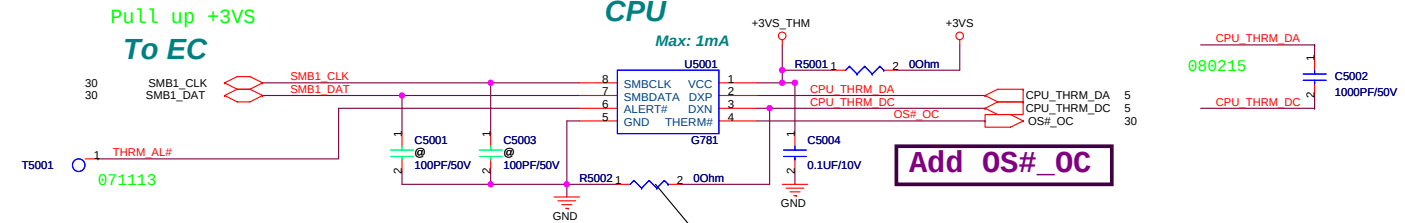


<Variant Name>

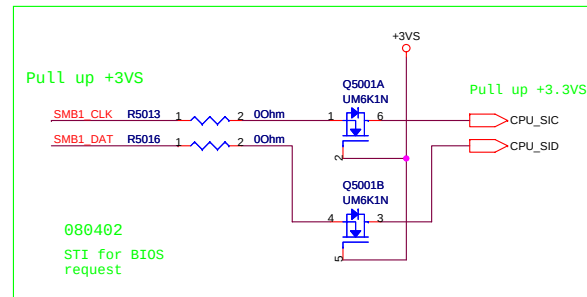
		Title : *	
ASUSTeK COMPUTER INC		Engineer: <i>Richard Lu</i>	
Size	Project Name	Rev	
Custom	F7Z	1.0	
Date: <i>Monday, May 19, 2008</i>		Sheet	48 of 94

5					4					3					2					1																																																																										
D																																																																																														
C																																																																																														
B																																																																																														
A																																																																																														
															<Variant Name> <table><tr><td colspan="5"></td><td colspan="5">Title : *</td></tr><tr><td colspan="5">ASUSTeK COMPUTER INC</td><td colspan="5">Engineer: <i>Richard Lu</i></td></tr><tr><td>Size</td><td colspan="12">Project Name</td><td>Rev</td><td></td></tr><tr><td><i>A</i></td><td colspan="12" rowspan="2"><i>F7Z</i></td><td><i>1.0</i></td><td></td></tr><tr><td colspan="15">Date: <i>Monday, May 19, 2008</i></td><td colspan="5">Sheet <i>49</i> of <i>94</i></td></tr></table>															Title : *					ASUSTeK COMPUTER INC					Engineer: <i>Richard Lu</i>					Size	Project Name												Rev		<i>A</i>	<i>F7Z</i>												<i>1.0</i>		Date: <i>Monday, May 19, 2008</i>															Sheet <i>49</i> of <i>94</i>				
					Title : *																																																																																									
ASUSTeK COMPUTER INC					Engineer: <i>Richard Lu</i>																																																																																									
Size	Project Name												Rev																																																																																	
<i>A</i>	<i>F7Z</i>												<i>1.0</i>																																																																																	
Date: <i>Monday, May 19, 2008</i>															Sheet <i>49</i> of <i>94</i>																																																																															
5					4					3					2					1																																																																										

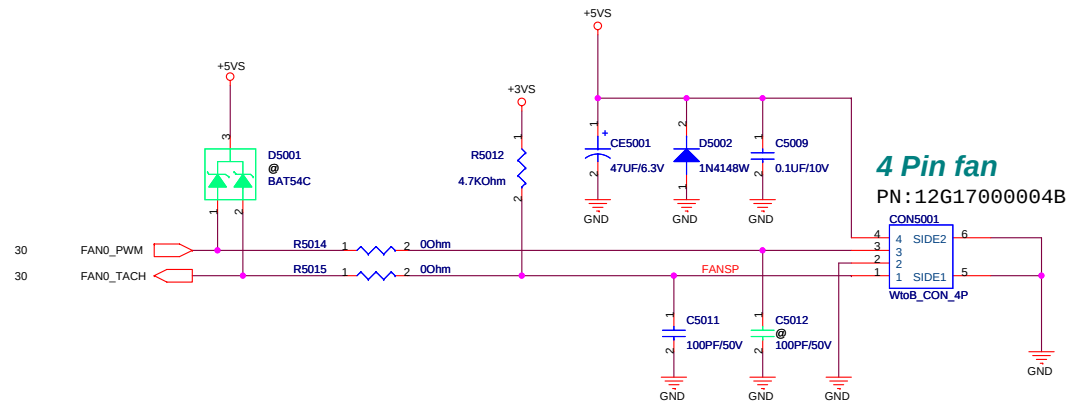
Thermal Sensor



080408 Close to DNX FOR G786



DC FAN Control



Route H_THERMDA and H_THERMDC on the same layer

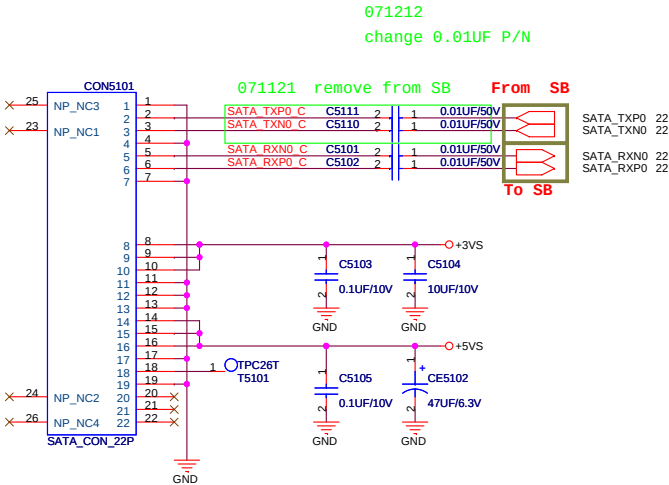
-----OTHER SIGNALS
15 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
15 mils
-----OTHER SIGNALS

Avoid FSB,Power

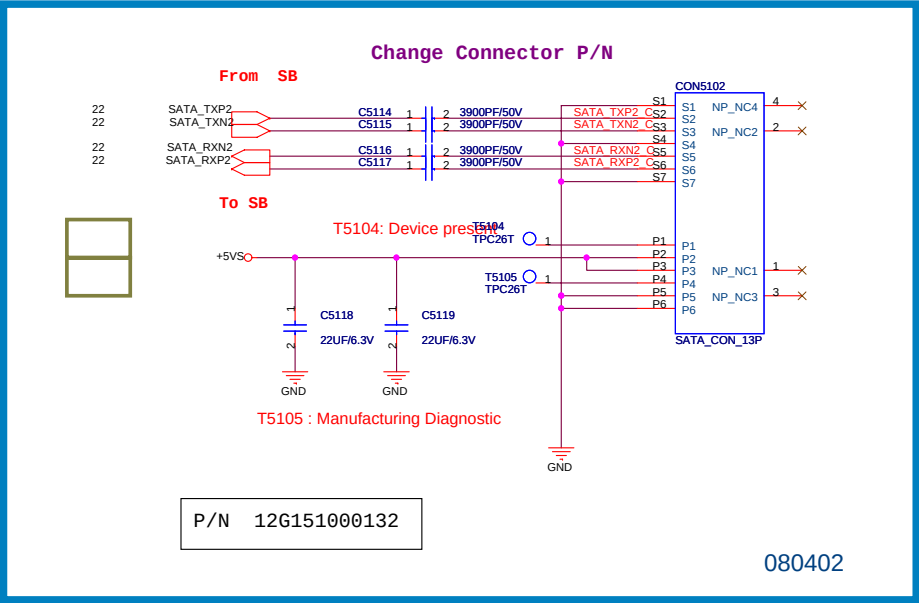
<Variant Name>

ASUS		Title : THER SENSOR & FAN	
ASUSTeK COMPUTER INC		Engineer: Richard Lu	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: Monday, May 19, 2008		Sheet	50 of 94

SATA HDD

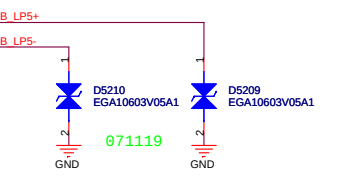
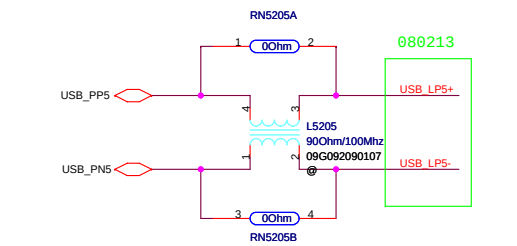
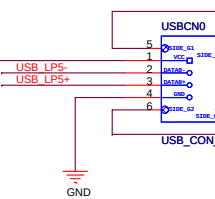
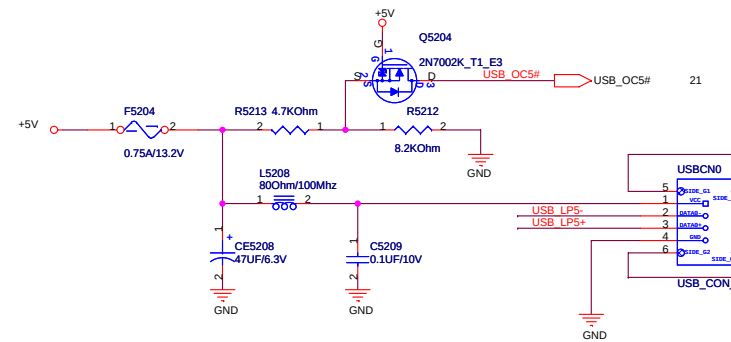
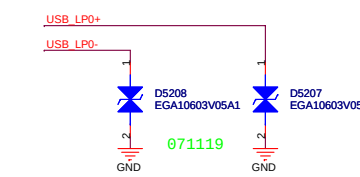
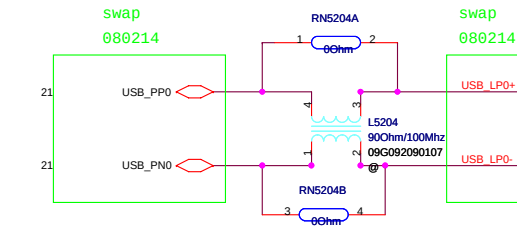
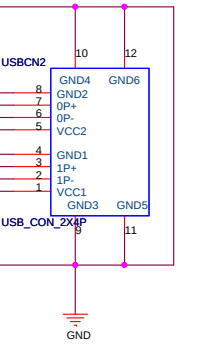
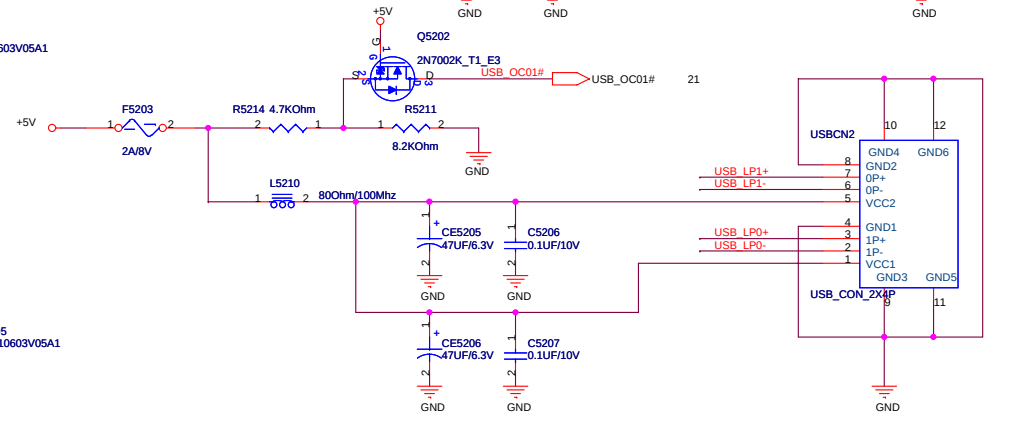
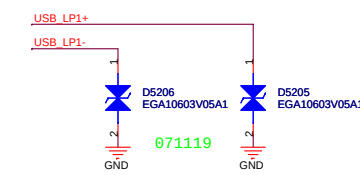
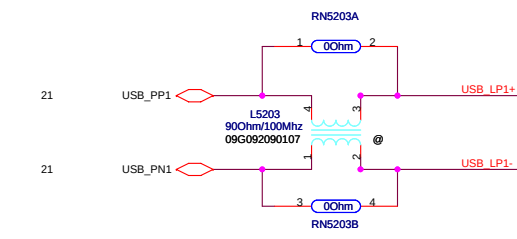
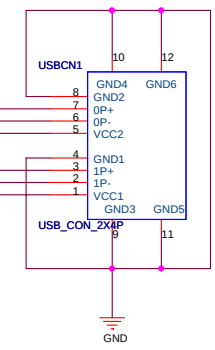
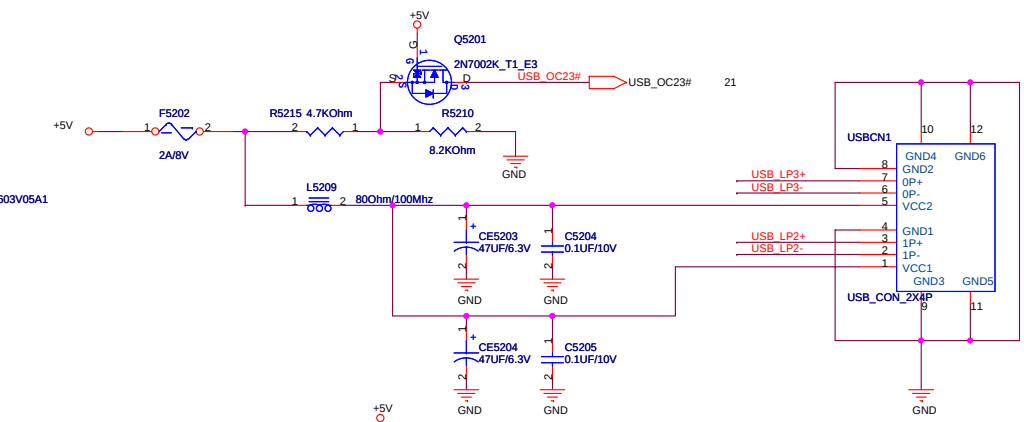
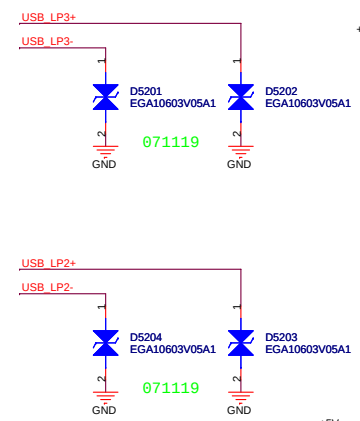
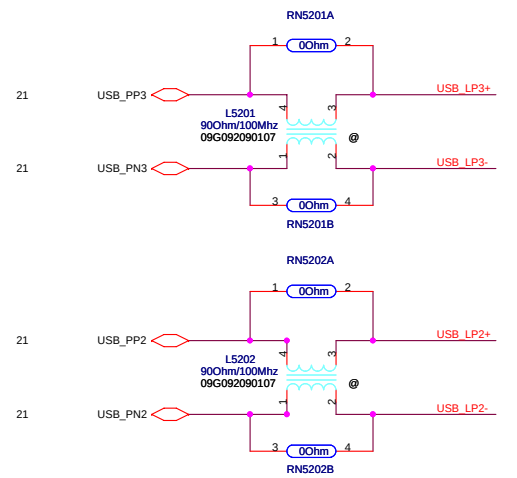


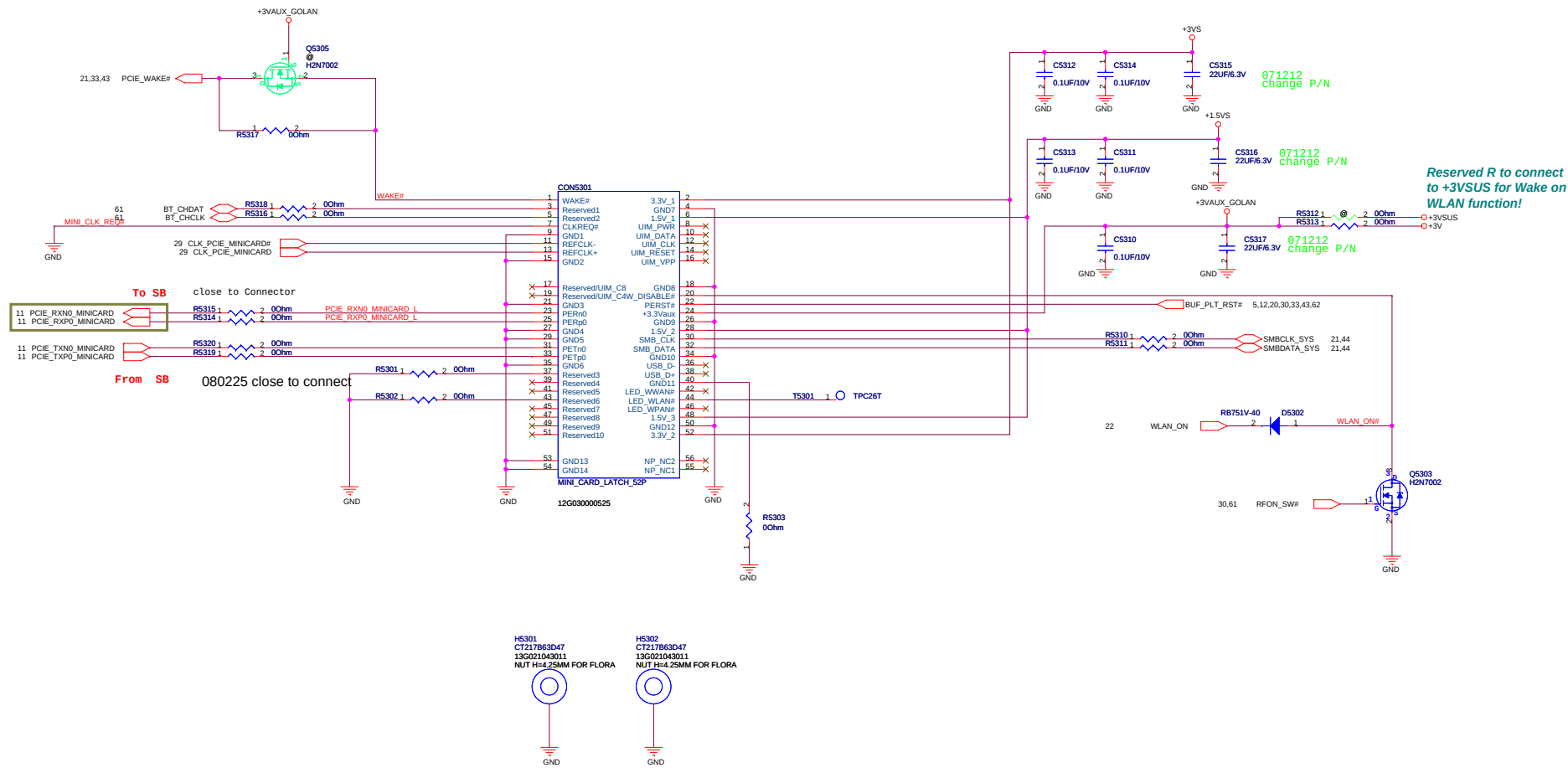
ODD



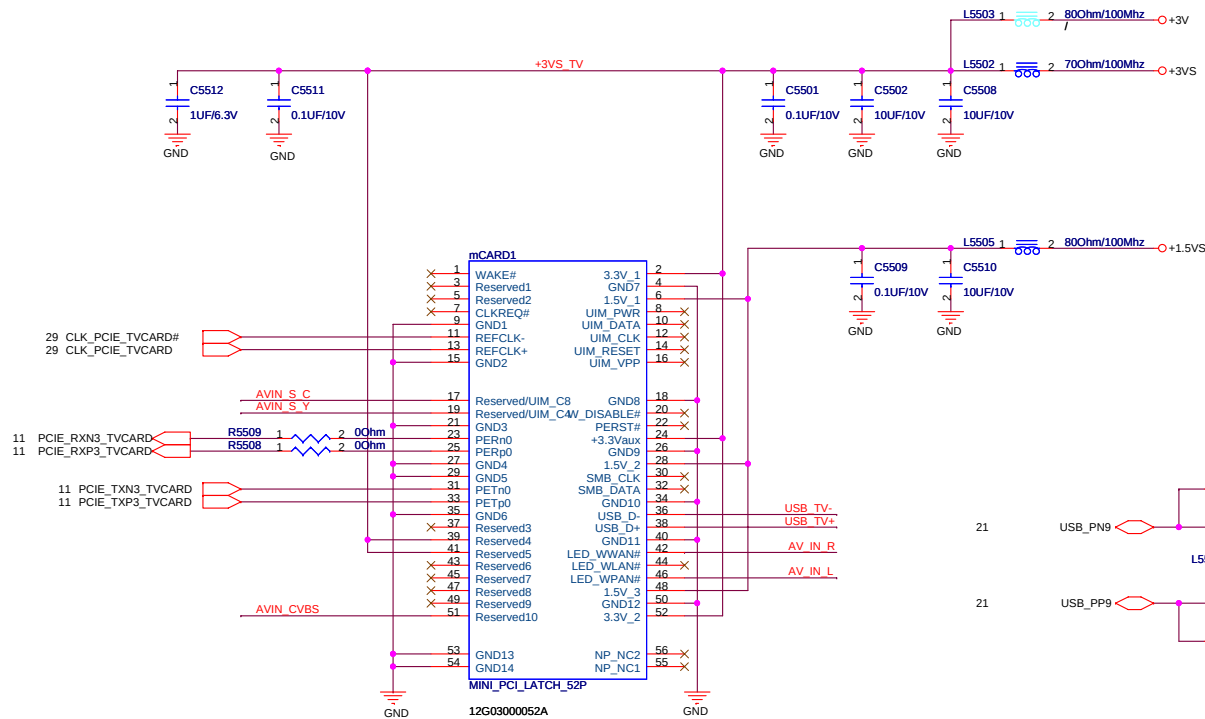
071119 change common
choke and R P/N

Change all MOS with ESD part

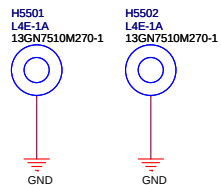




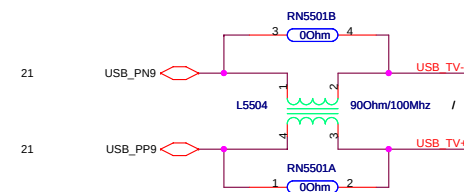
5					4					3					2					1				
D																								
C																								
B																								
A																								
<Variant Name>																								
															Title : *									
															Engineer: <i>Richard Lu</i>									
Size					Project Name															Rev				
<i>A</i>					<i>F7Z</i>															<i>1.0</i>				
Date: <i>Monday, May 19, 2008</i>															Sheet <i>54</i> of <i>94</i>									
5					4					3					2					1				



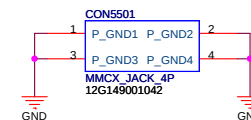
H = 5.2mm
FOR TV TUNER
(UWB OPTION)



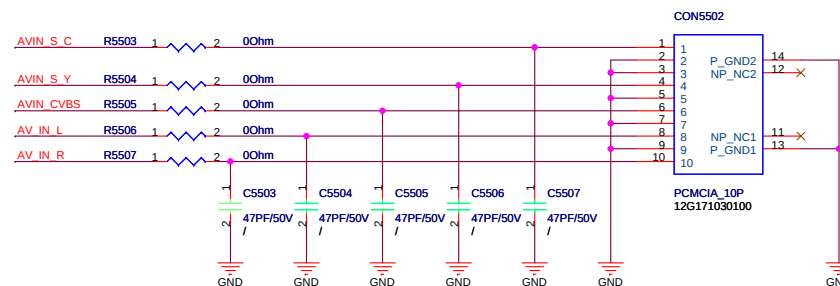
H = 3.0mm



TV Conn.



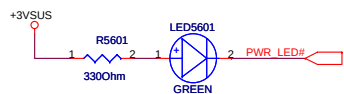
ME P/N : 14G152075000



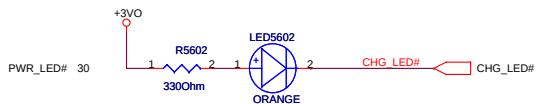
<Variant Name>

LED

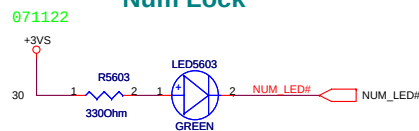
For POWER LED



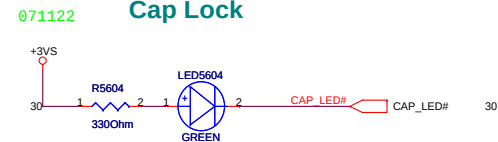
BATTERY LED



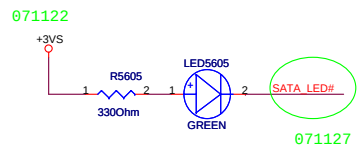
Num Lock



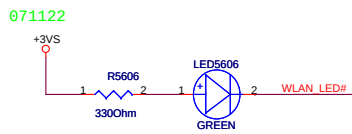
Cap Lock



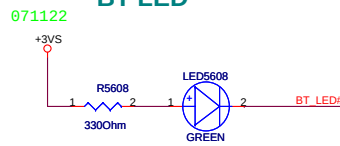
SATA/IDE LED



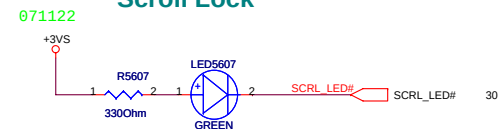
WireLess LED



BT LED

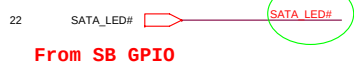


Scroll Lock

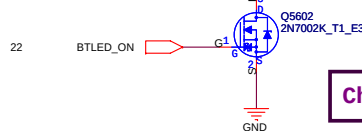
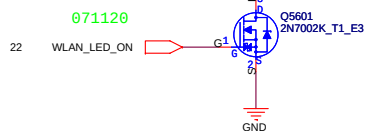


Change all LED for 5mA

delete D5601
071127



From SB GPIO

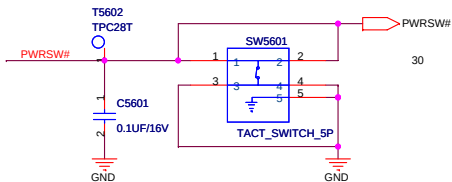


Change all MOS with ESD part

F5Z SWITCH CIRCUIT

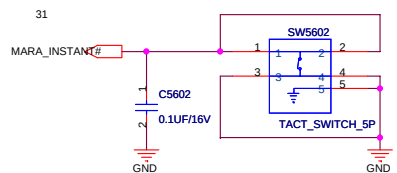
Move SW from P32 to P56

Power SW.



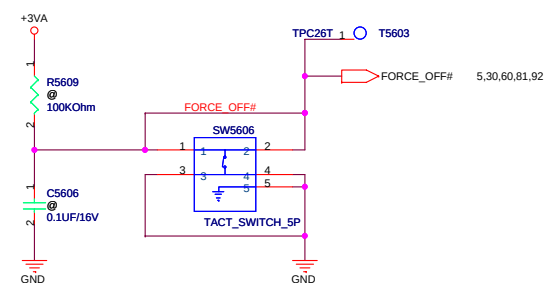
P/N: 12G091030050

Marathon SW.



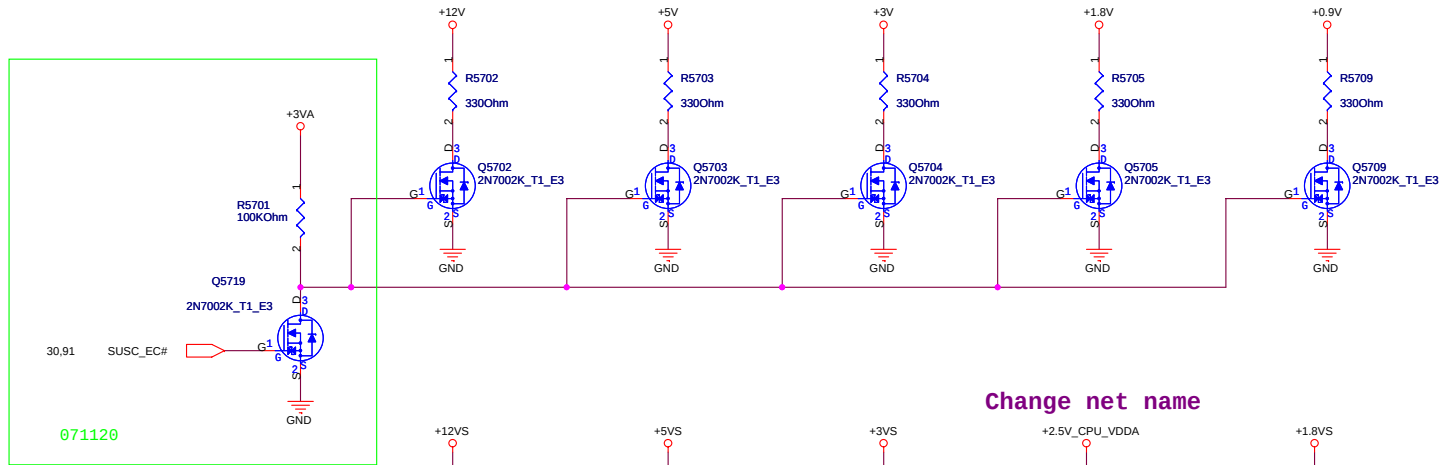
Add SHUT Down SCH

SHUT_DOWN#

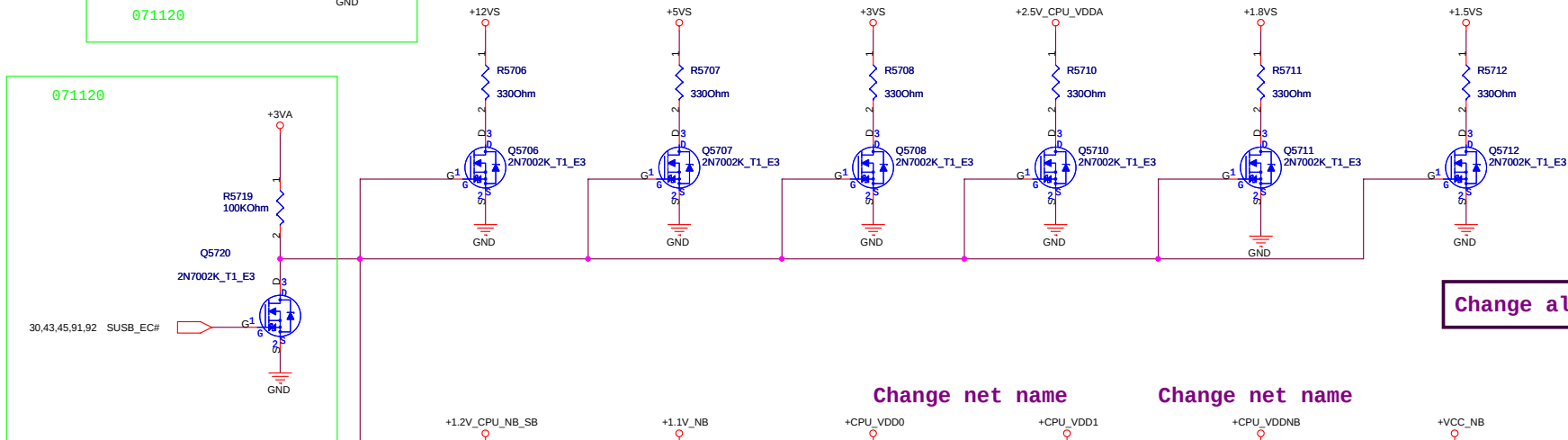


<Variant Name>

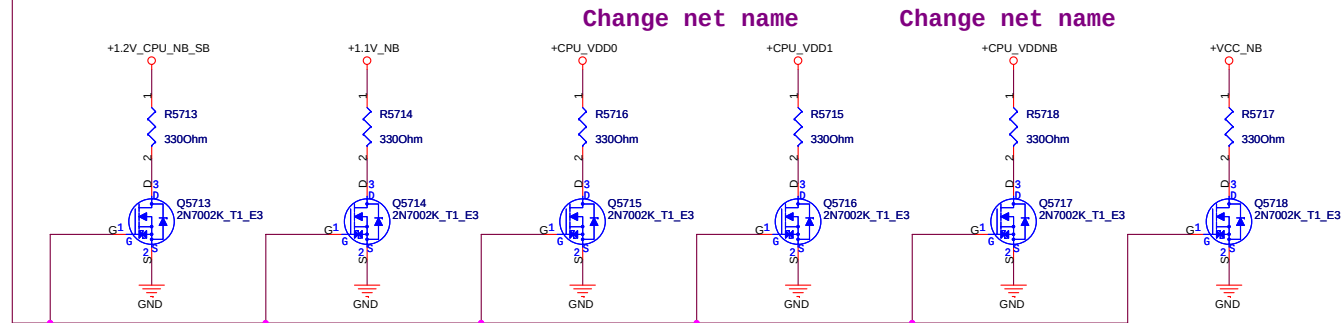
ASUS		Title : LED/PWR SWITCH	
ASUSTek COMPUTER INC		Engineer: Richard Lu	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: Monday, May 19, 2008		Sheet	56 of 94



Change net name



Change all MOS with ESD part



Change net name

Change net name



<Variant Name>

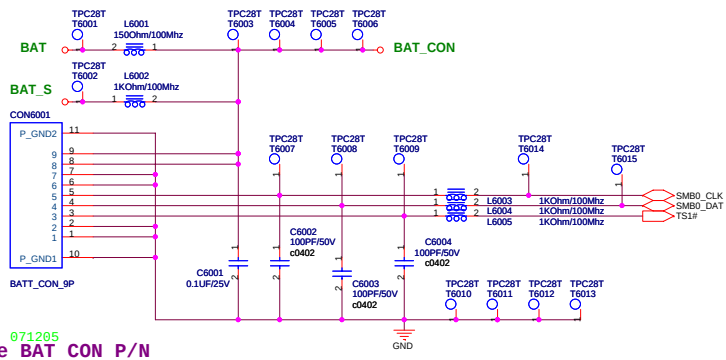
		Title : *	
ASUSTeK COMPUTER INC		Engineer: <i>Richard Lu</i>	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: <i>Monday, May 19, 2008</i>		Sheet	58 of 94

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

<Variant Name>

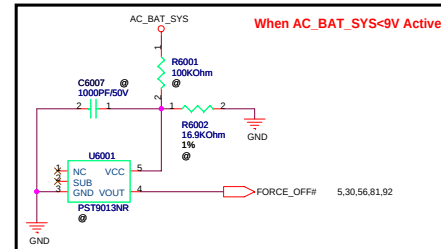
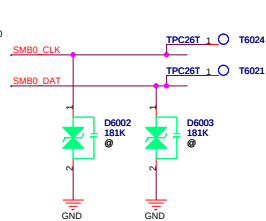
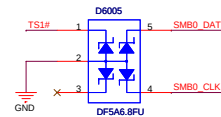
		Title : *	
ASUSTeK COMPUTER INC		Engineer: <i>Richard Lu</i>	
Size A	Project Name F7Z		Rev 1.0
Date: Monday, May 19, 2008		Sheet	59 of 94

071120 cahnge PL->L,PT->T,PC->C



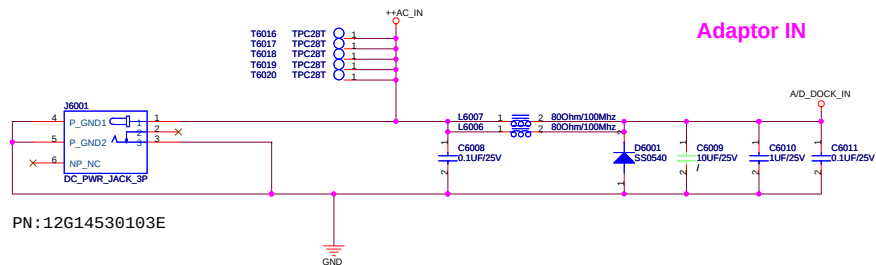
Change BAT CON P/N 071205

Without Battery & Pull out Adapter



Add for AC Adapter protect

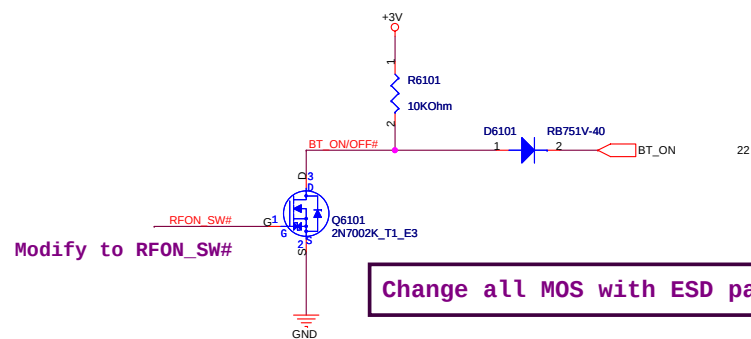
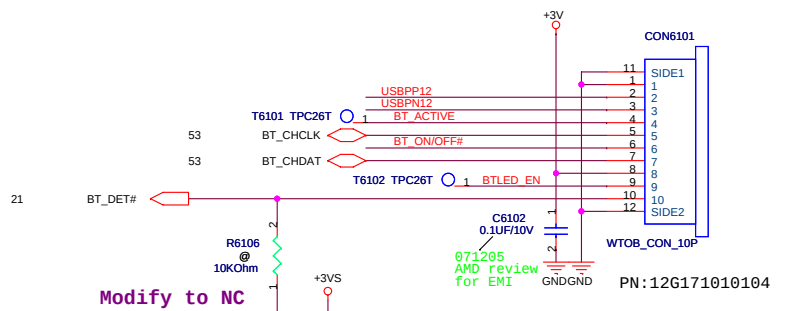
Adaptor IN



PN:12G14530103E

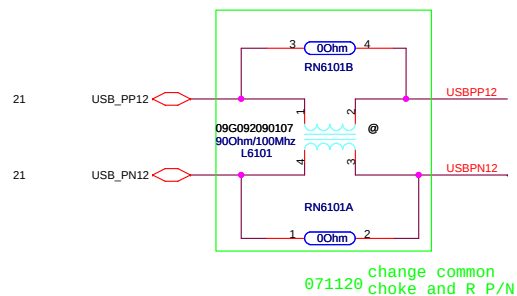
071218
Delete GND_DC , Bead
,and Test Point

For Bluetooth

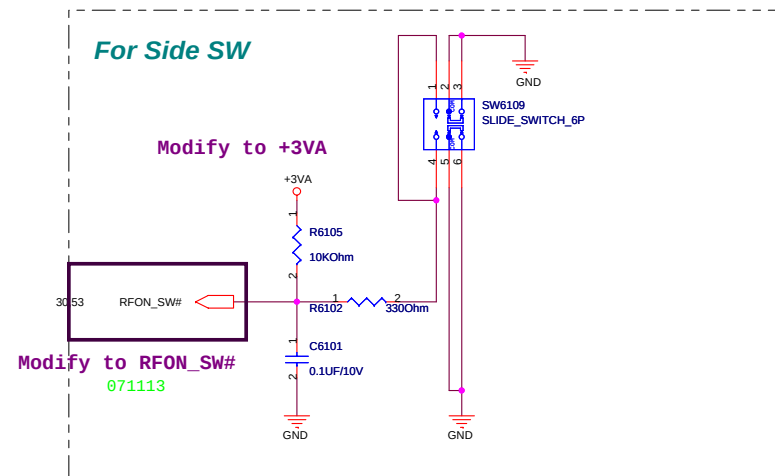


Change all MOS with ESD part

RN swap
071214



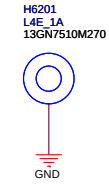
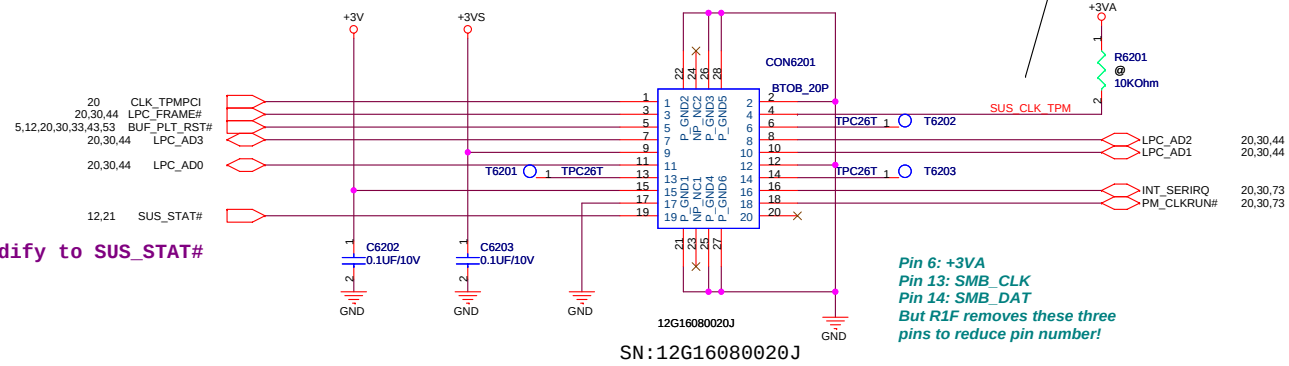
For Side SW



For TPM Module

Modify to SUS_STAT#

071120
TPM module has internal crystal



<Variant Name>

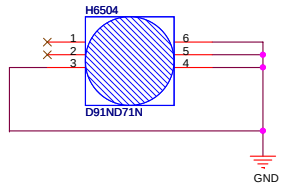
ASUS		Title : TPM	
ASUSTeK COMPUTER INC		Engineer: Richard Lu	
Size	Project Name	Rev	1.0
Custom	F7Z		
Date: Monday, May 19, 2008		Sheet	62 of 94



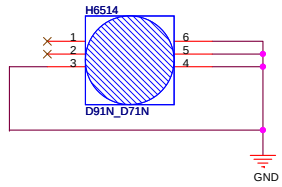
<Variant Name>

		Title : *	
ASUSTeK COMPUTER INC		Engineer: <i>Richard Lu</i>	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: <i>Monday, May 19, 2008</i>		Sheet	63 of 94

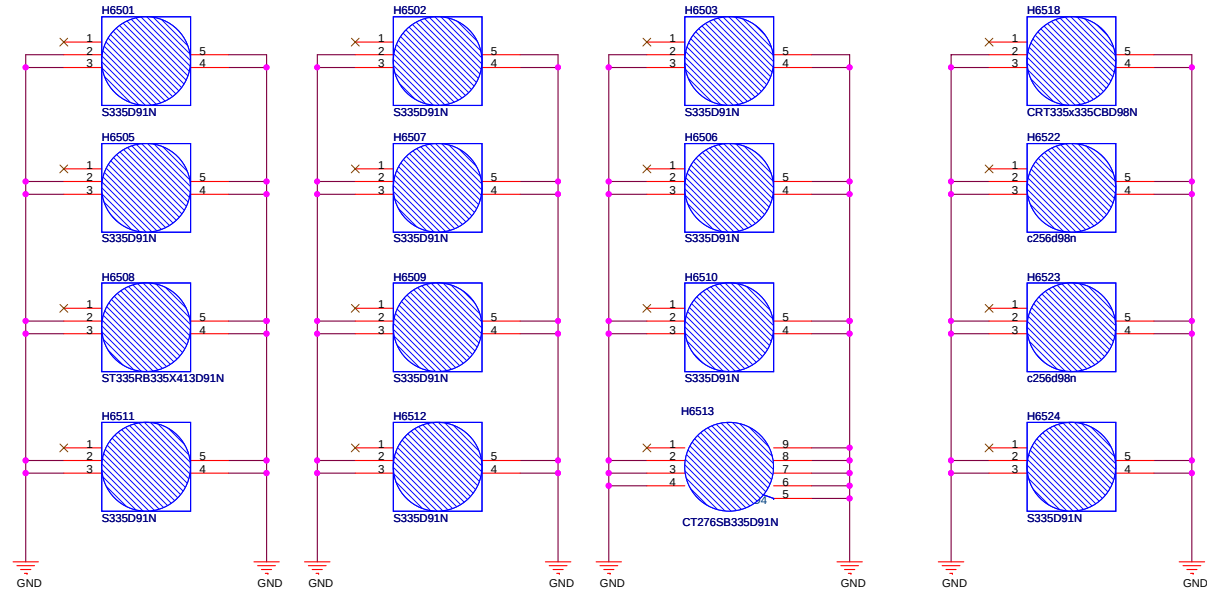
FOR LEFT UNDER



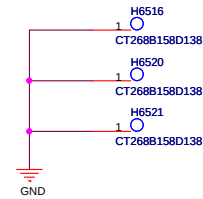
FOR RIGHT UP



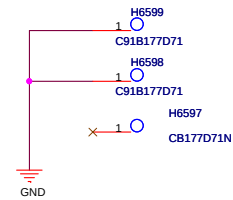
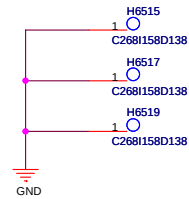
FOR SCREW HOLE



FOR CPU



FOR VGA



<Variant Name>

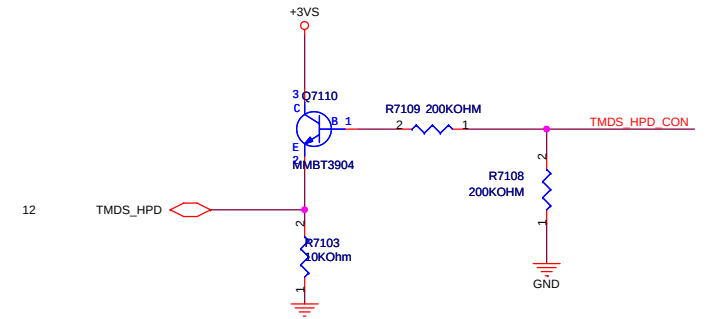
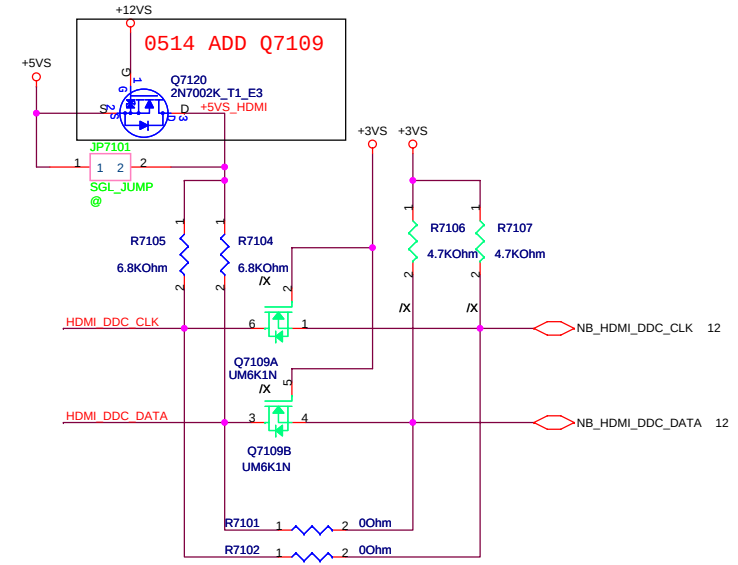
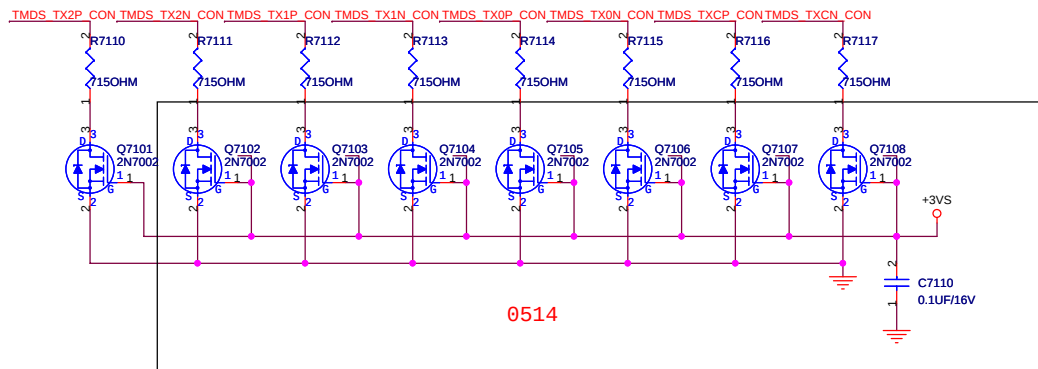
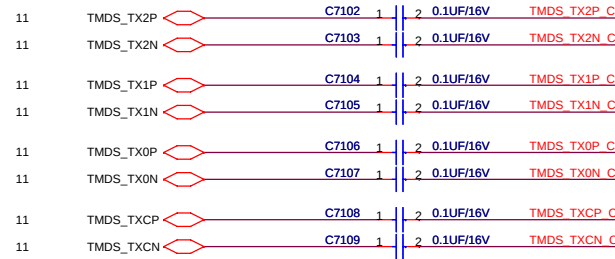
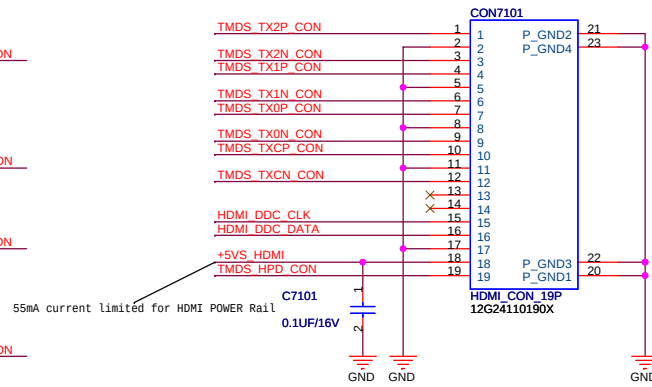
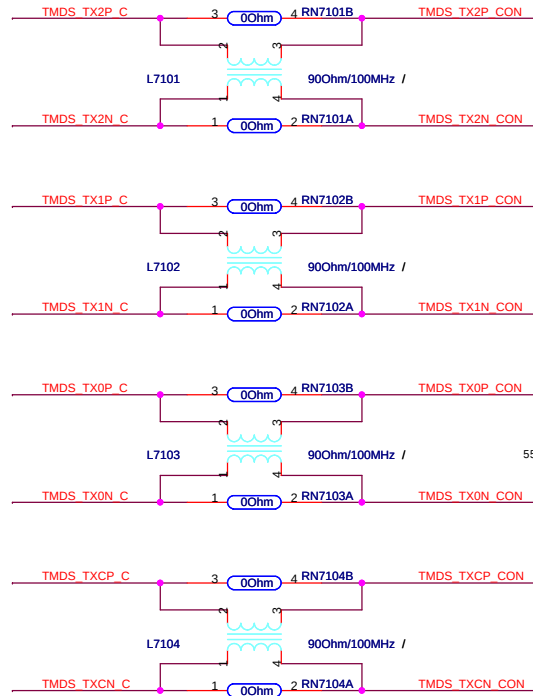
ASUS		Title : Screw Hole	
ASUSTeK COMPUTER INC.		Engineer: <OrgAddr1>	
Size	Project Name	Rev	
Custom	F7Z	1.0	
Date: Monday, May 19, 2008	Sheet	65	of 94



<Variant Name>

		Title : *	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: Monday, May 19, 2008		Sheet	70 of 94

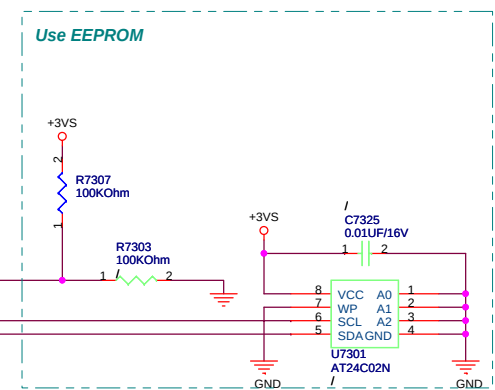
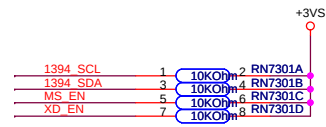
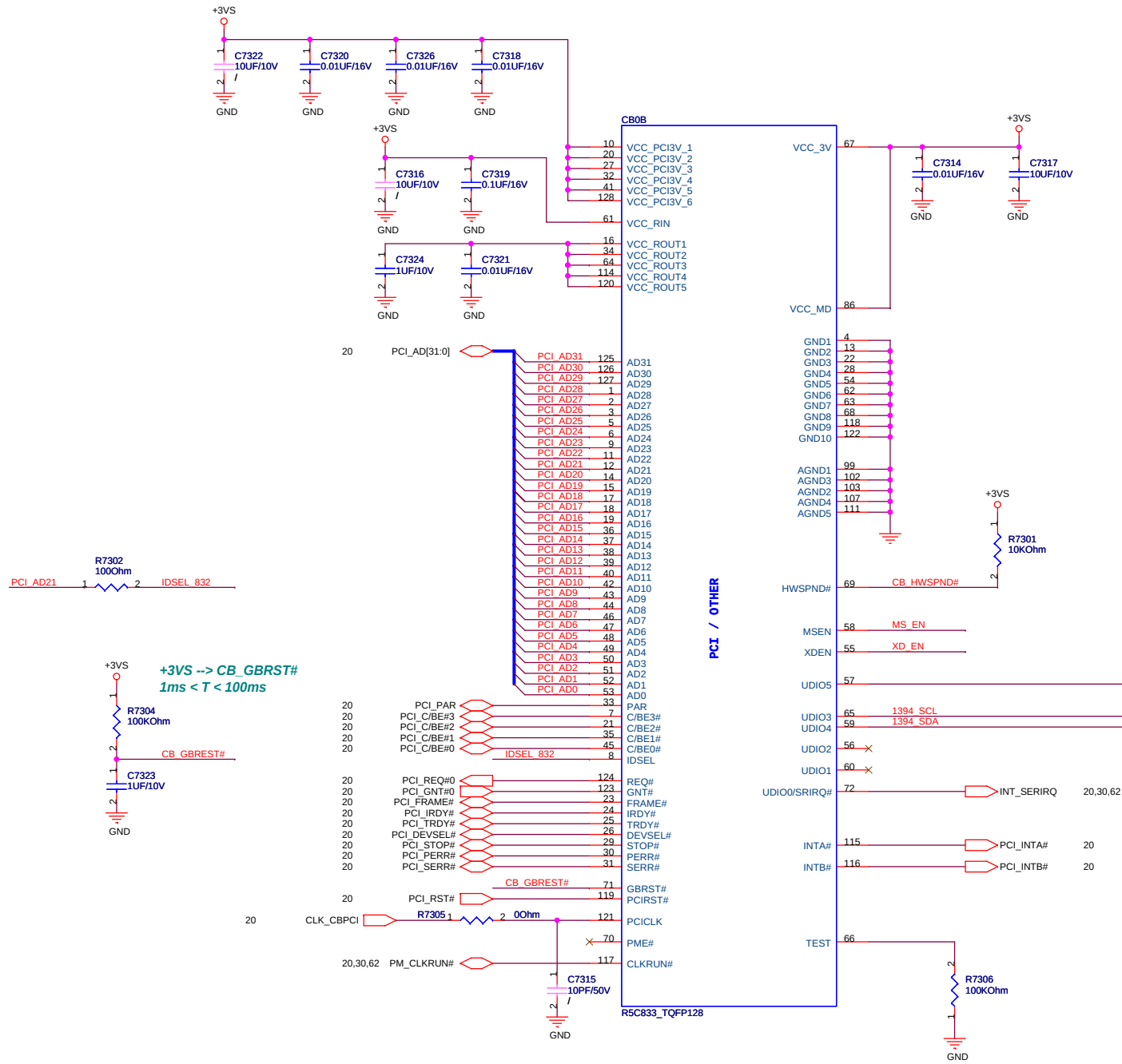
HDMI

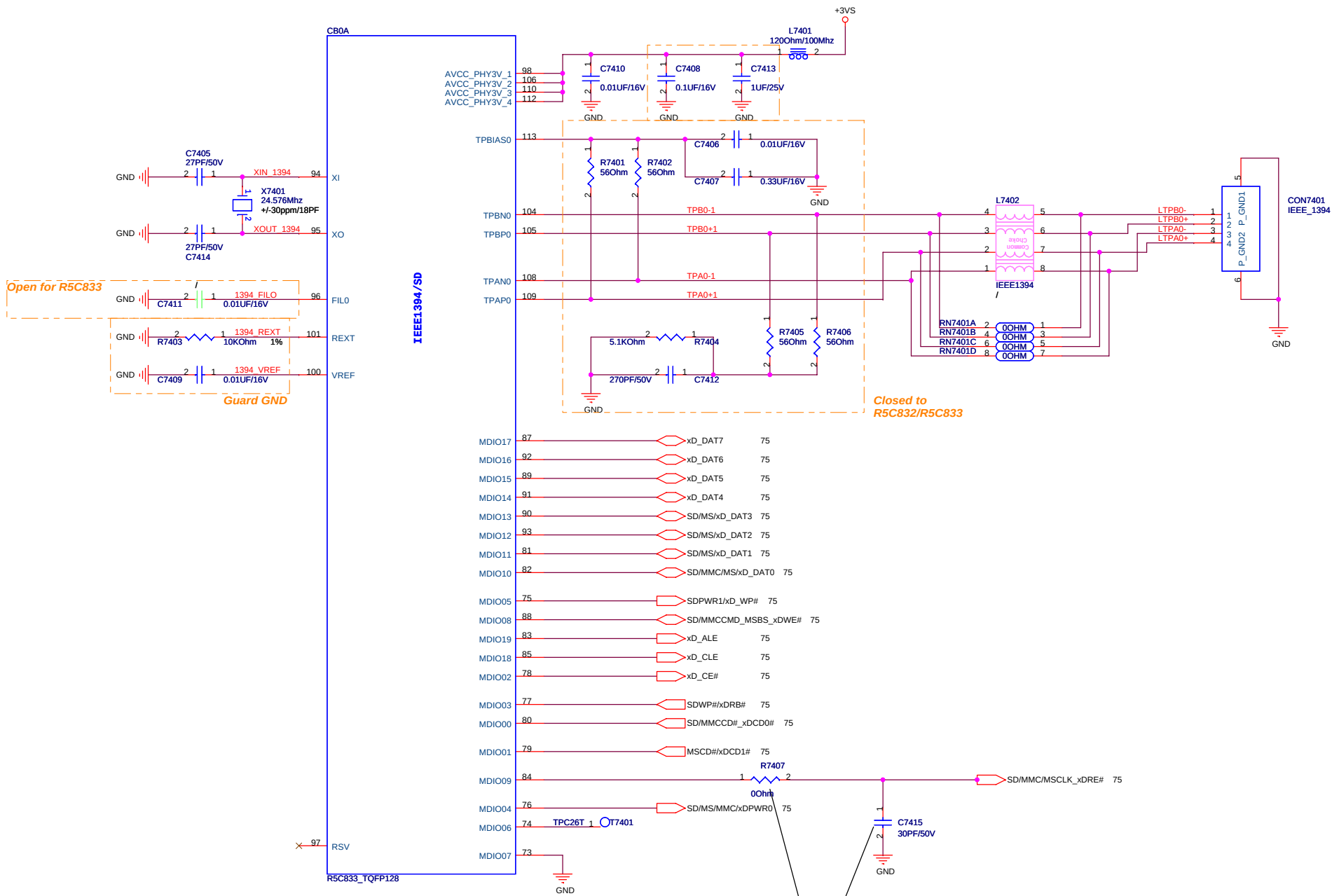


<Variant Name>



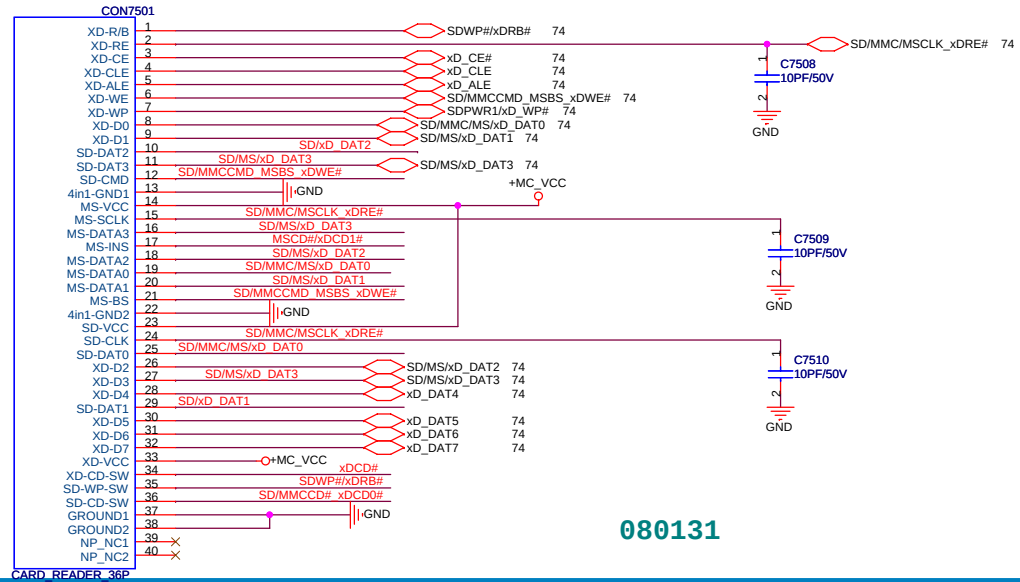
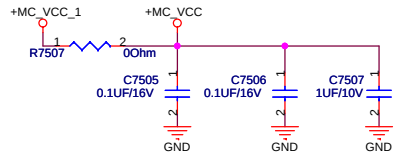
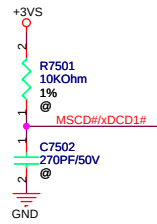
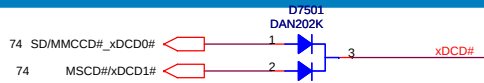
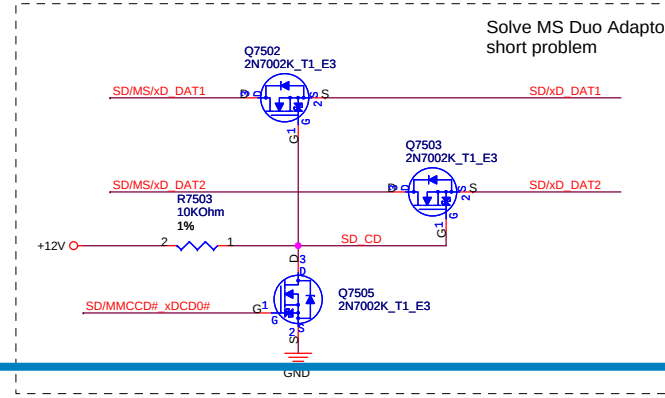
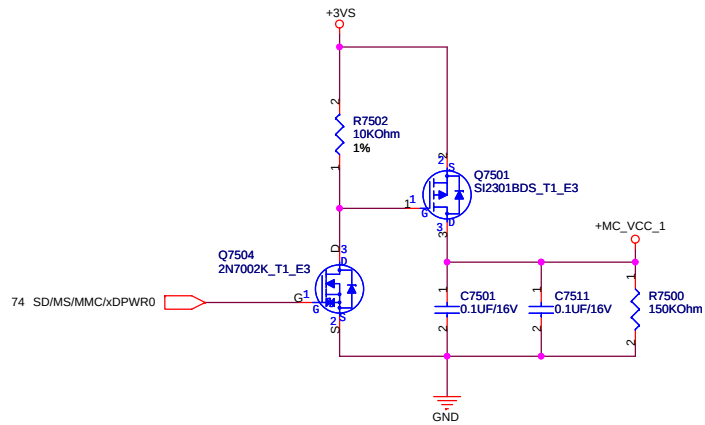
<Variant Name>			
		Title : *	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: Monday, May 19, 2008		Sheet	72 of 94





080408 Add r7407 and c7415 for EMI

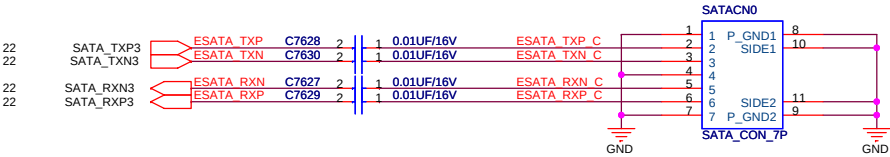
<Variant Name>

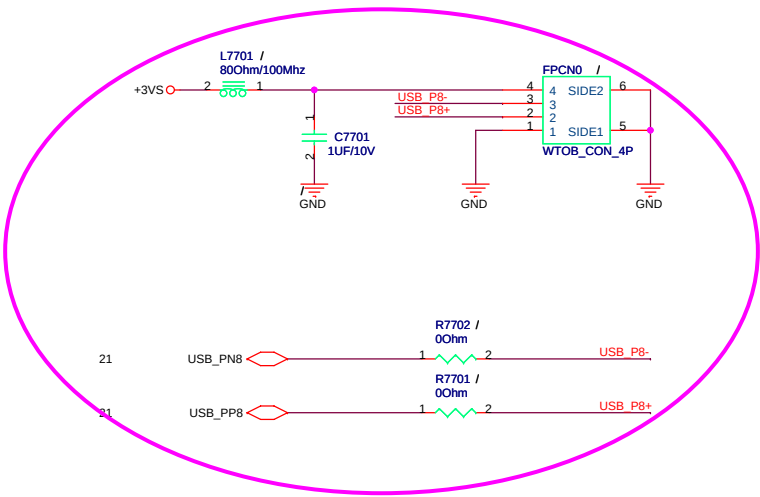


080131

<Variant Name>

eSATA Connector





080131 Change cardreader connect to 12G340003601.change CDROM connect to 12G151000132 .
080215 1.change thermal sensor to G781,change C5002 to 1000pf
 2.fix stuff TMP module can not boot

080217 change C3711/C3712/C3709/C3710 connect to GND
 change D7101 to 2 Pin
080219 Remove R3052 and R3108,move D3103 to R3052(N connect to EC side)
 change Q9101/Q9107 to 07G005161020(07G005357011)

080221 change ec to 8512 Page82 Page83
080222 add C0651/C0652/C0653/C0654

080225 add R1408/R4307/R4308/R5319/R5320

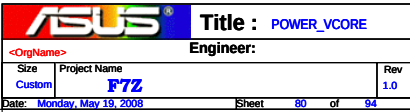
080408 Add r7407 and c7415 for EMI



<Variant Name>

		Title : *	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	F7Z		1.0
Date: Monday, May 19, 2008		Sheet 79 of 94	

SVC	SVD	Output	Pre_metal
0	0	1.4	1.1
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8



* Rocset = Ioc * DRC / 10uA

+1.2V0: ROCSET = R8213 ; R8215 = R8213=10KOhm; OCP>7.5A

+1.8V0: ROCSET = R8212 ; R8212 =R8211 =4.7KOhm ; OCP>14A

* VREF = 0.6V+-1%

+1.2V0 = VREF * (R8206 + R8214) / R8214 =1.2V+-2%

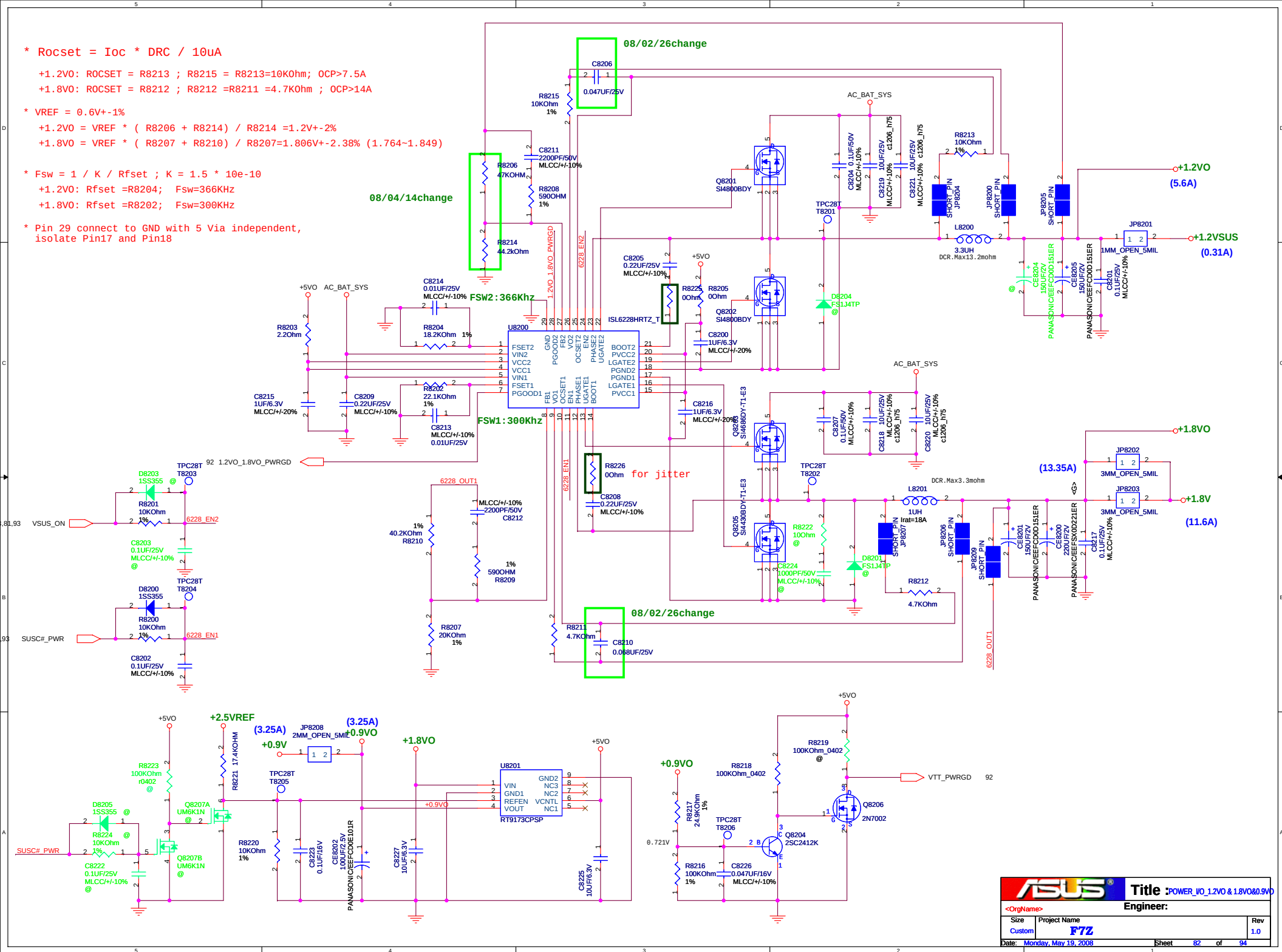
+1.8V0 = VREF * (R8207 + R8210) / R8207=1.806V+-2.38% (1.764~1.849)

* Fsw = 1 / K / Rfset ; K = 1.5 * 10e-10

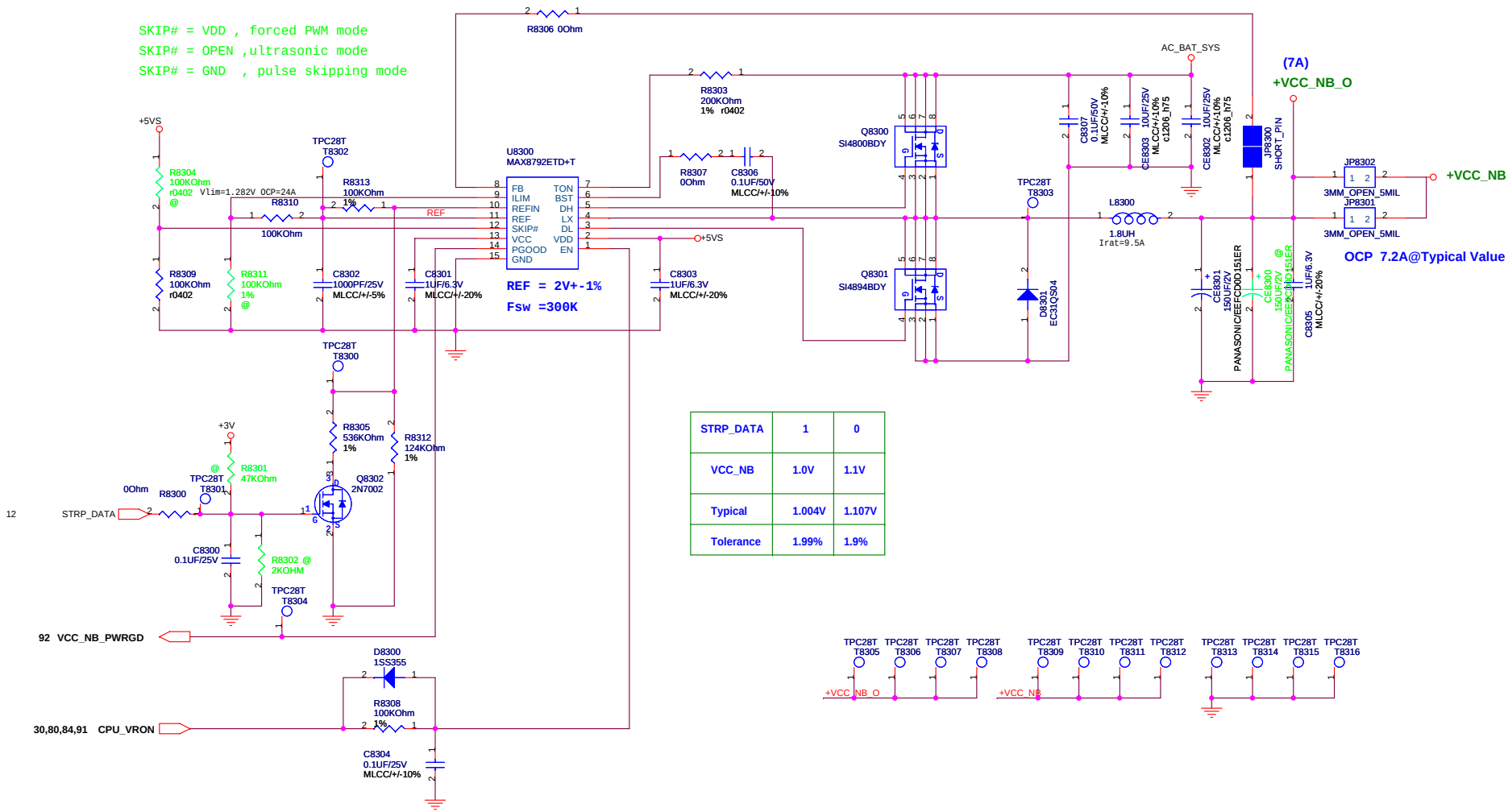
+1.2V0: Rfset =R8204; Fsw=366KHz

+1.8V0: Rfset =R8202; Fsw=300KHz

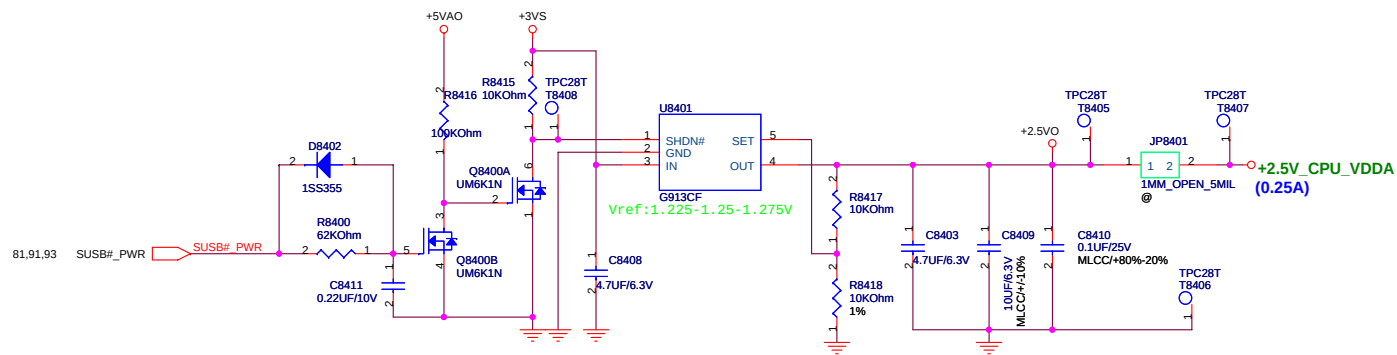
* Pin 29 connect to GND with 5 Via independent,
isolate Pin17 and Pin18



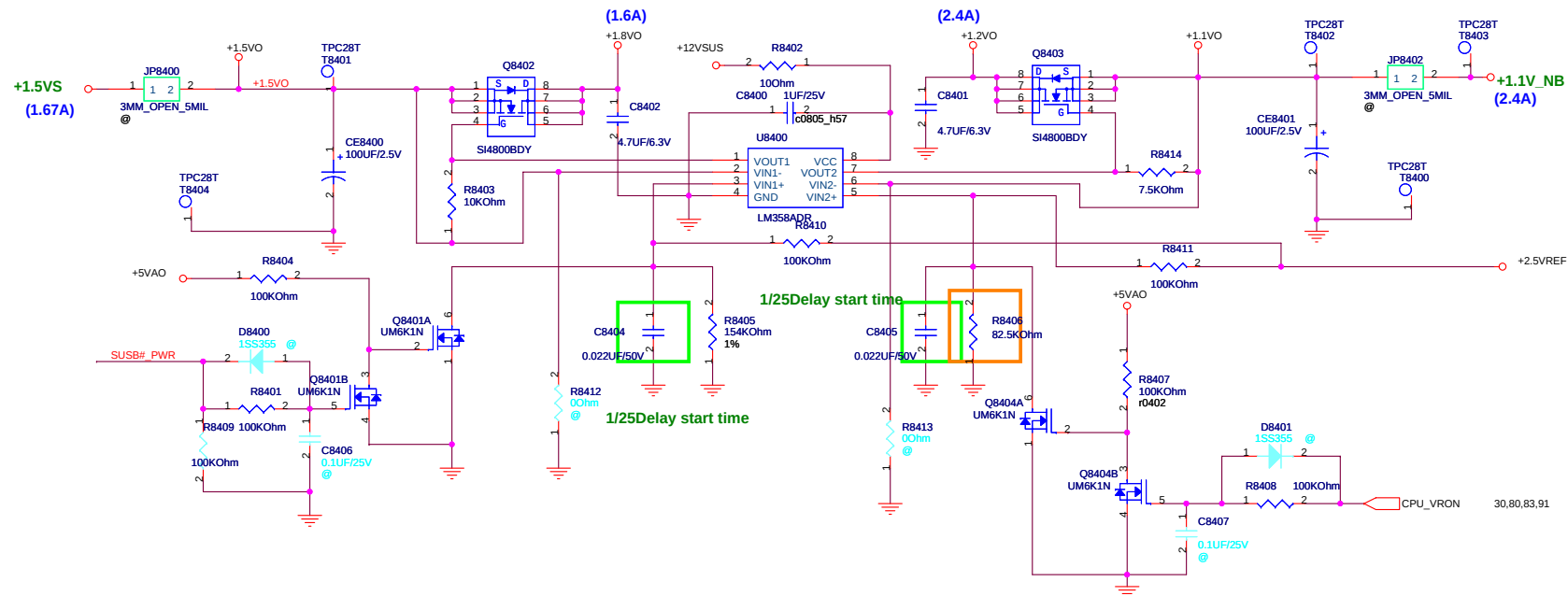
SKIP# = VDD , forced PWM mode
 SKIP# = OPEN ,ultrasonic mode
 SKIP# = GND , pulse skipping mode

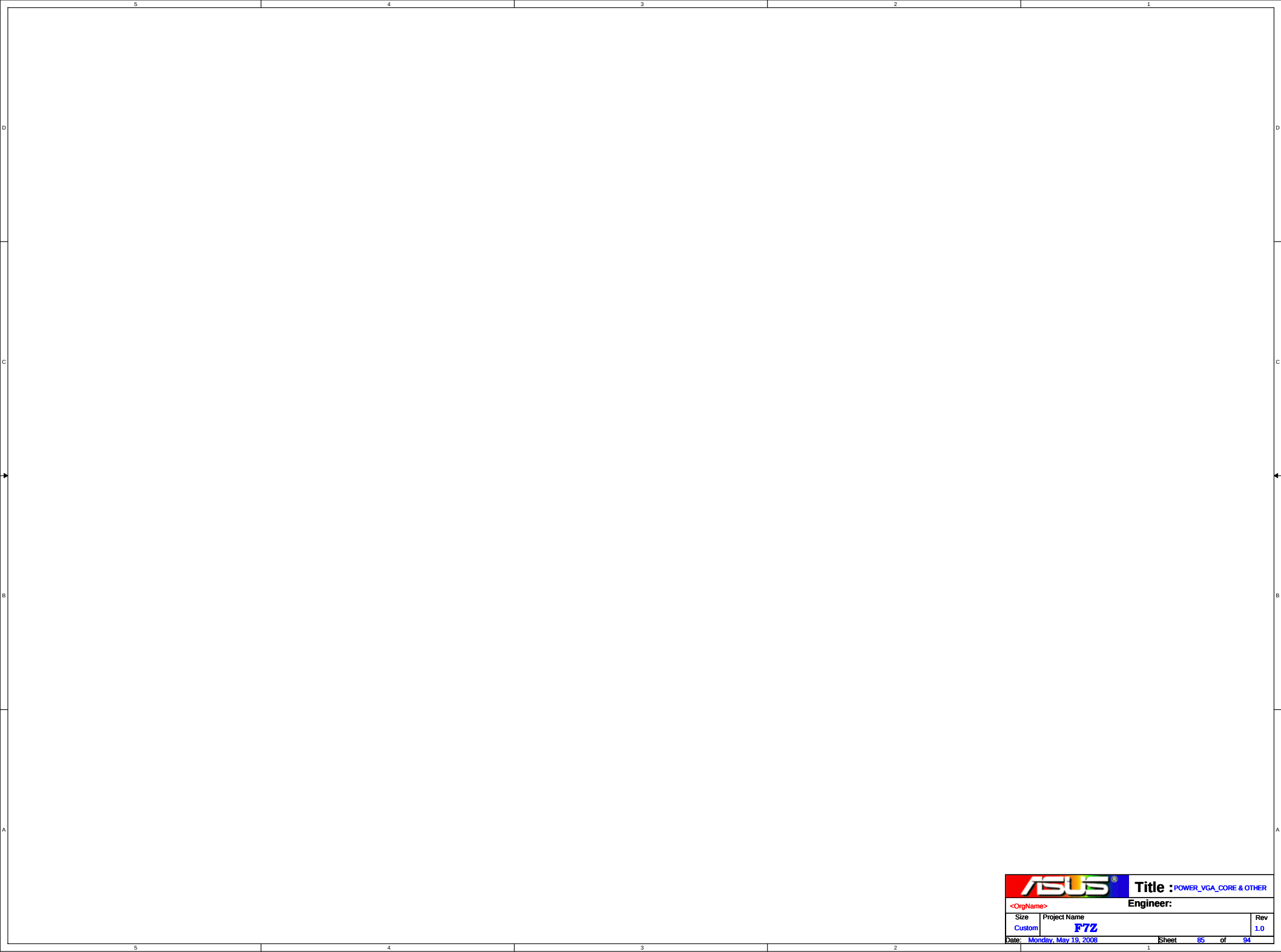


+2.5V_CPU_VDDA



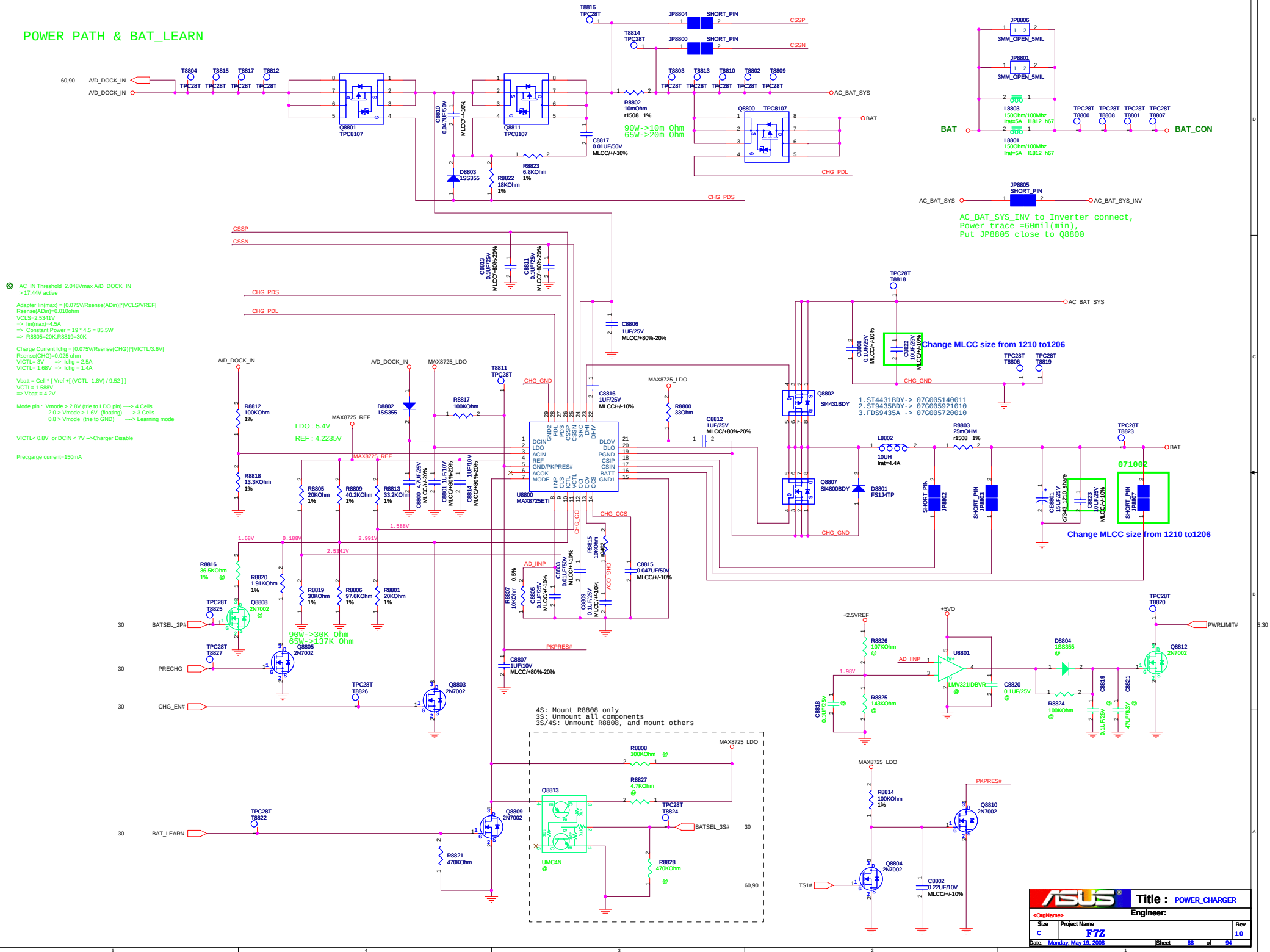
+1.5VS & +1.1V_NB





		Title : POWER_VGA_CORE & OTHER	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	F7Z	1.0	
Date: Monday, May 19, 2008		Sheet	85 of 94

POWER PATH & BAT_LEARN





Title : POWER_PIC

<OrgName>

Engineer:

Size
A

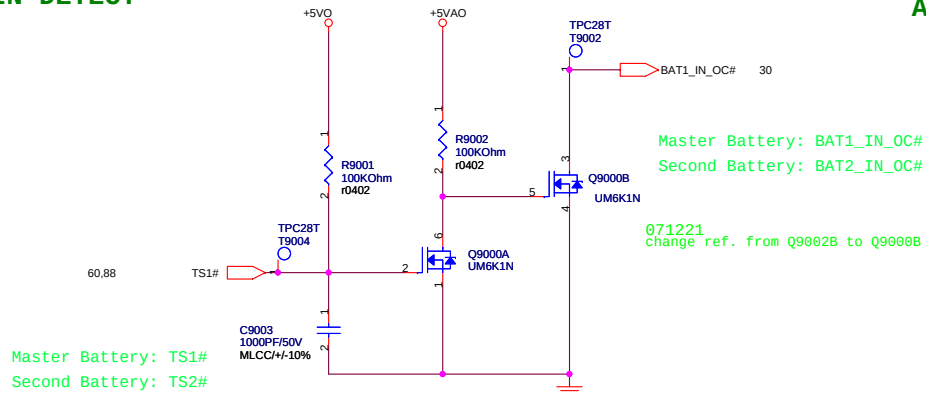
Project Name	F7Z
--------------	------------

Rev
1.0

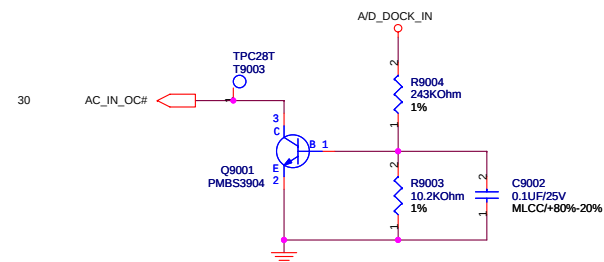
Date: Monday, May 19, 2008

Sheet 89 of 94

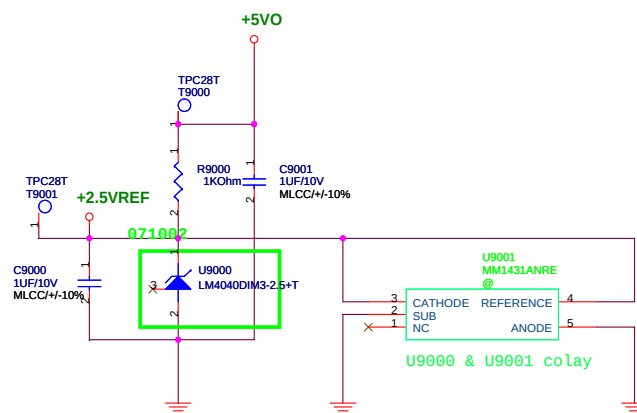
BATTERY IN DETECT



ADAPTER IN DETECT

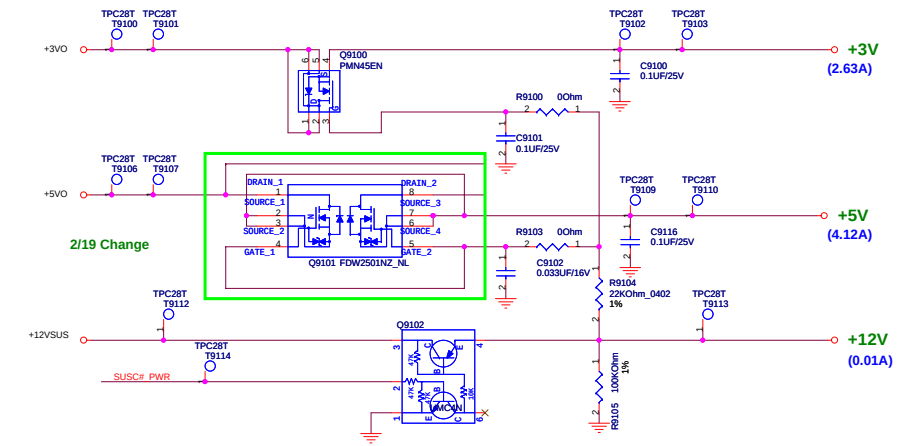


+2.5VREF

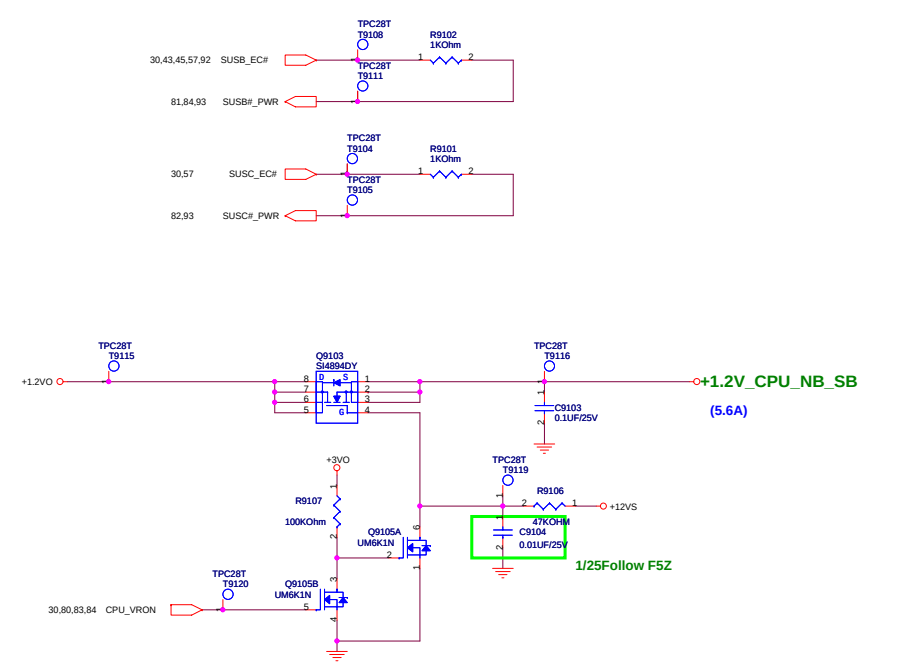
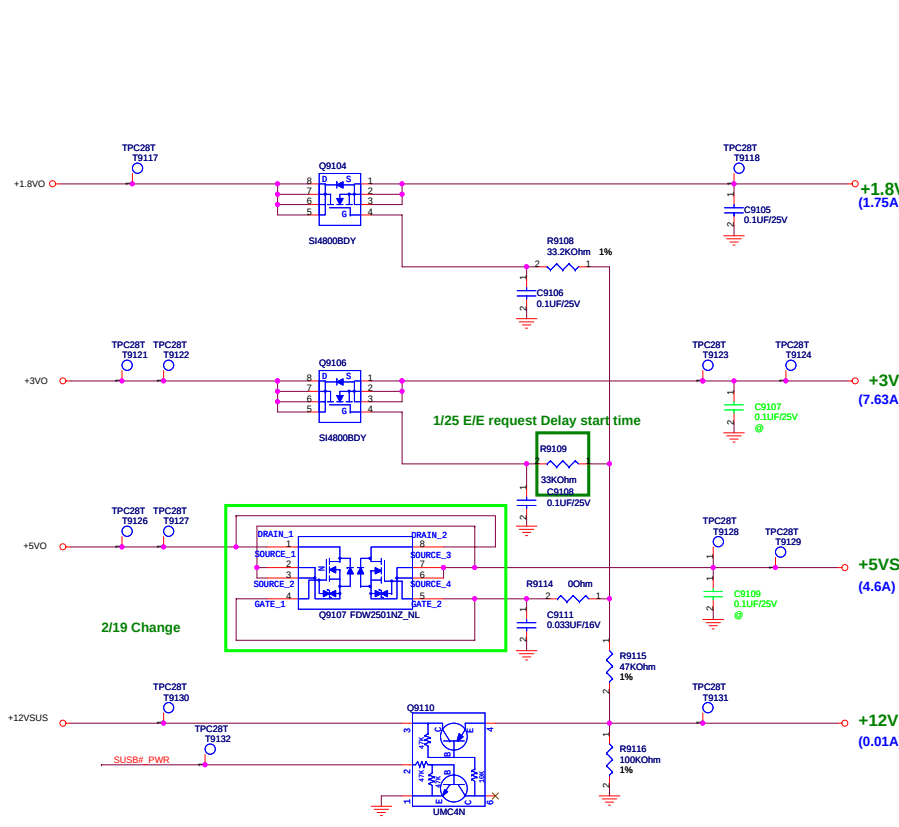


U9000 Main source change to 06G006002414(tolerance:1%).
Add second source 06G006002610 (tolerance:1%),
06G006002412 (tolerance:0.2%) and
06G006002020(tolerance:0.2%)

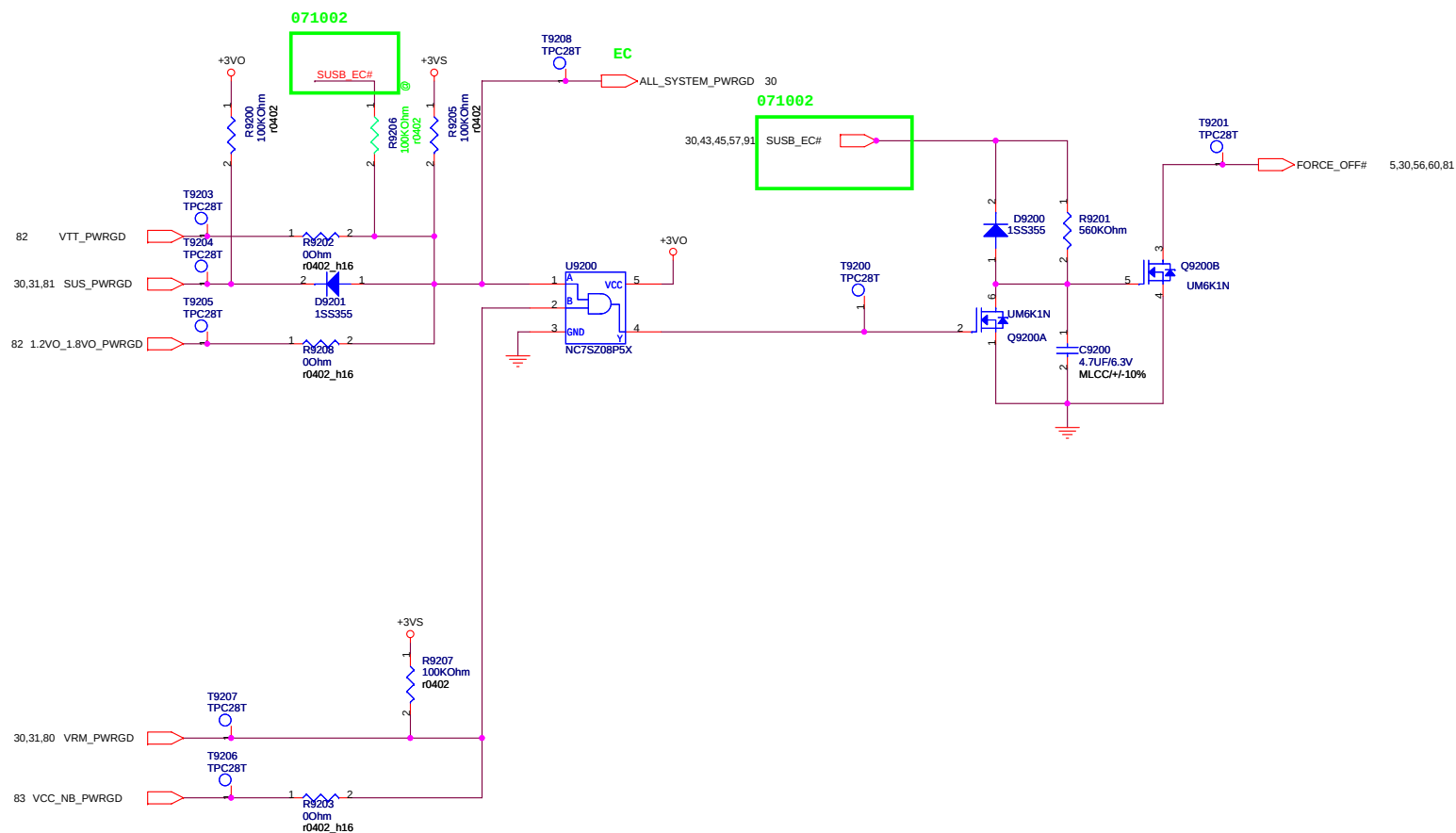
SUSC#_PWR POWER



SUSB#_PWR POWER



POWER GOOD DETECTOR



AC_BAT_SYS		AC_BAT_SYS	60,80,81,82,83,88
BAT		BAT	60,88
BAT_CON		BAT_CON	60,88
+2.5VREF		+2.5VREF	82,84,88,90
+3VA		+3VA	20,30,45,56,57,61,62,81
+5VAO		+5VAO	81,84,90
+5VO		+5VO	81,82,88,90,91
+5VSUS		+5VSUS	81
+5V		+5V	44,45,52,57,91
+5VS		+5VS	23,30,31,36,37,46,50,51,57,71,80,83,91
+3VO		+3VO	56,81,91,92
+3VSUS		+3VSUS	4,20,21,22,23,24,30,33,35,37,43,53,56,80,81
+3V		+3V	30,35,44,45,53,55,57,61,62,83,91
+3VS		+3VS	5,7,8,12,13,14,21,22,23,24,29,30,31,33,36,37,43,45,46,50,51,53,55,56,57,61,62,71,73,74,75,77,80,84,91,92
+12VSUS		+12VSUS	81,84,91
+12V		+12V	37,57,75,91
+12VS		+12VS	30,45,57,71,91
+1.8VO		+1.8VO	82,84,91
+1.8V		+1.8V	4,5,6,7,8,9,57,82
+1.8VS		+1.8VS	5,12,13,14,21,57,91
+0.9V		+0.9V	4,6,9,57,82
+0.9VO		+0.9VO	82
+2.5V_CPU_VDDA		+2.5V_CPU_VDDA	5,57,84
+1.5VS		+1.5VS	43,53,55,57,84
+1.5VO		+1.5VO	84
+1.1VO		+1.1VO	84
+1.1V_NB		+1.1V_NB	12,14,57,84
+1.2VO		+1.2VO	82,84,91
+1.2VSUS		+1.2VSUS	23,82
+1.2V_CPU_NB_SB		+1.2V_CPU_NB_SB	3,14,20,22,23,57,91
+VCC_NB_O		+VCC_NB_O	83
+VCC_NB		+VCC_NB	14,57,83
+CPU_VDD0		+CPU_VDD0	6,57,80
+CPU_VDD1		+CPU_VDD1	6,57,80
+CPU_VDDNB_O		+CPU_VDDNB_O	80
+CPU_VDDNB		+CPU_VDDNB	6,57,80

FOR POWER TEST

