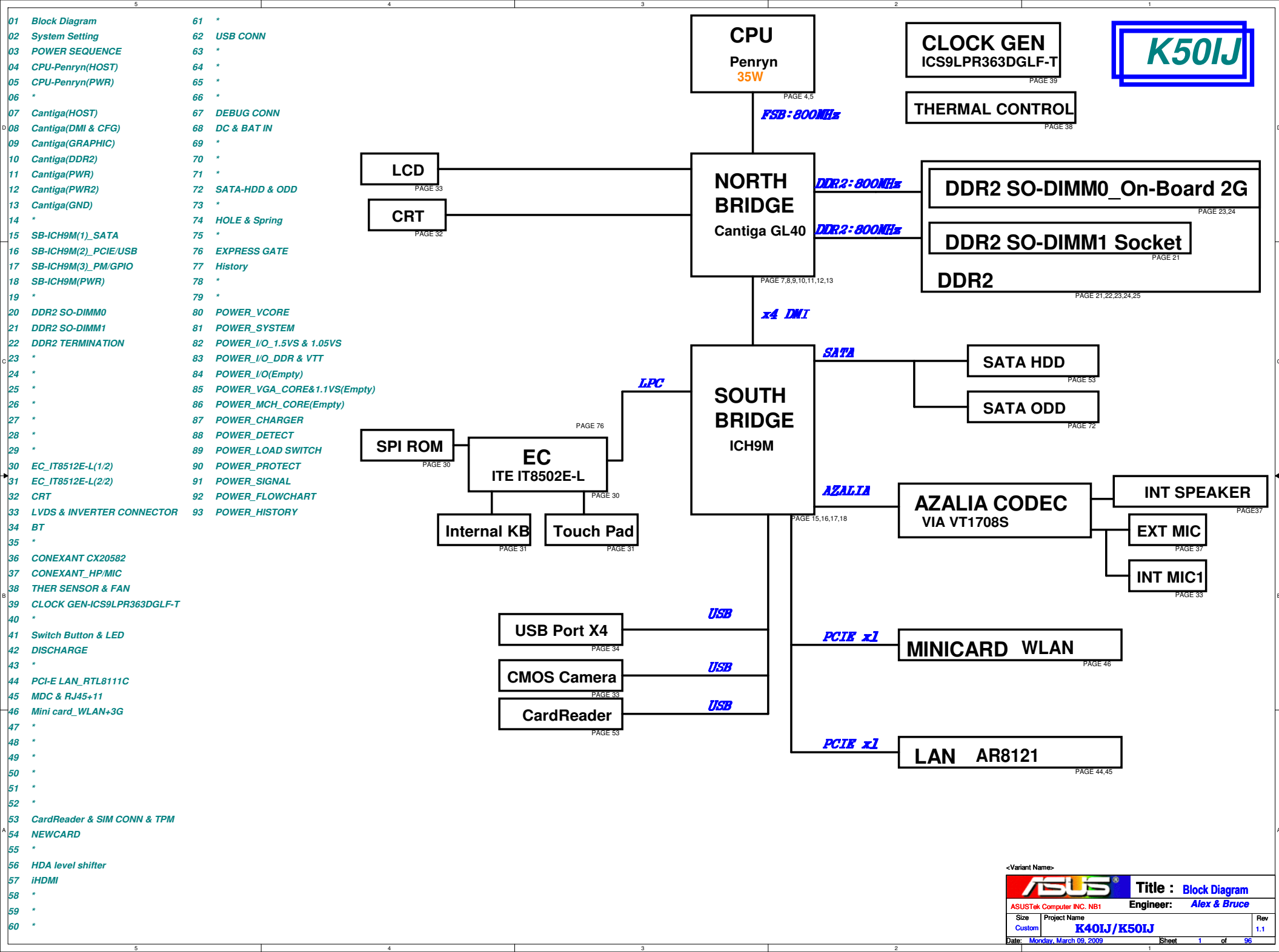
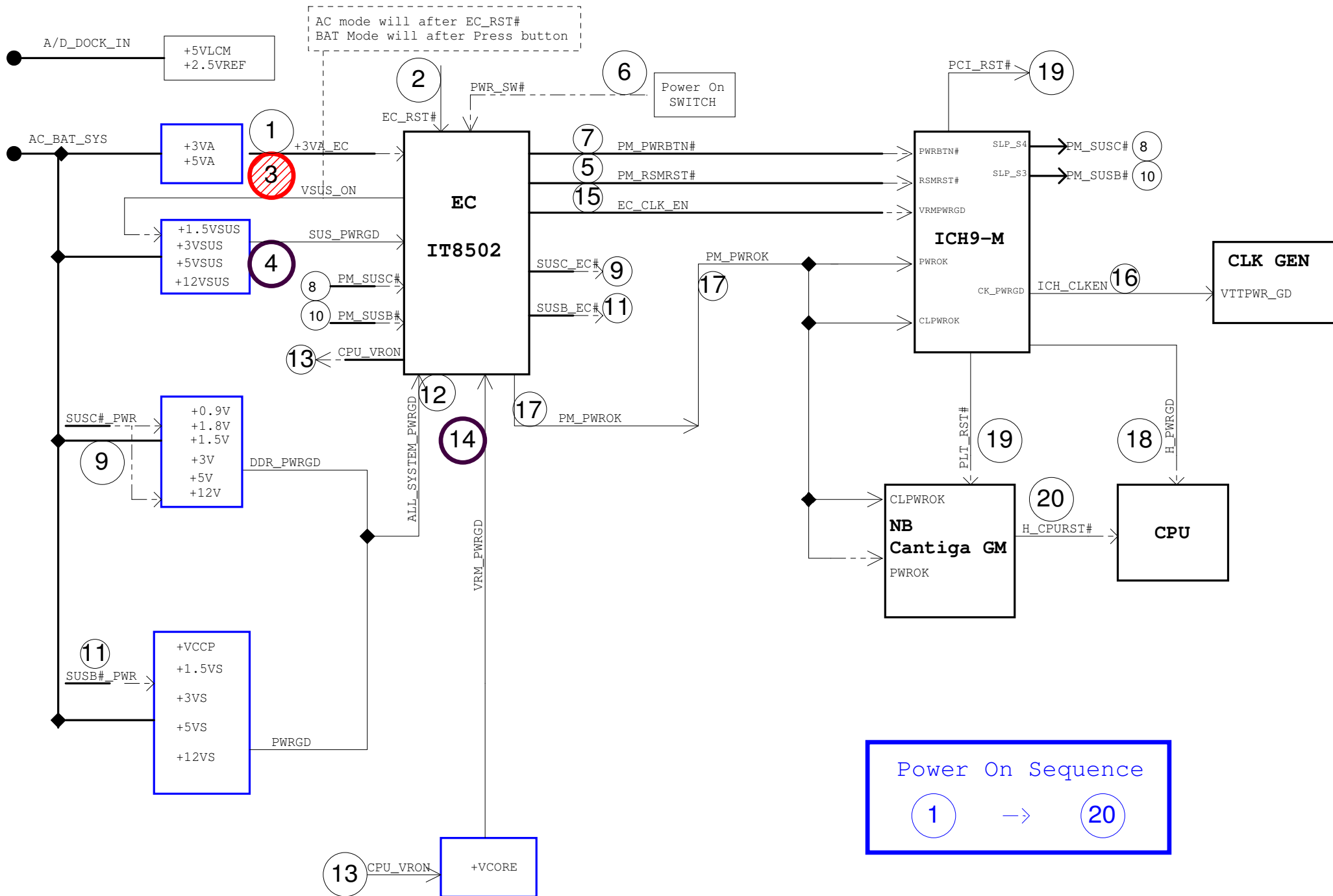
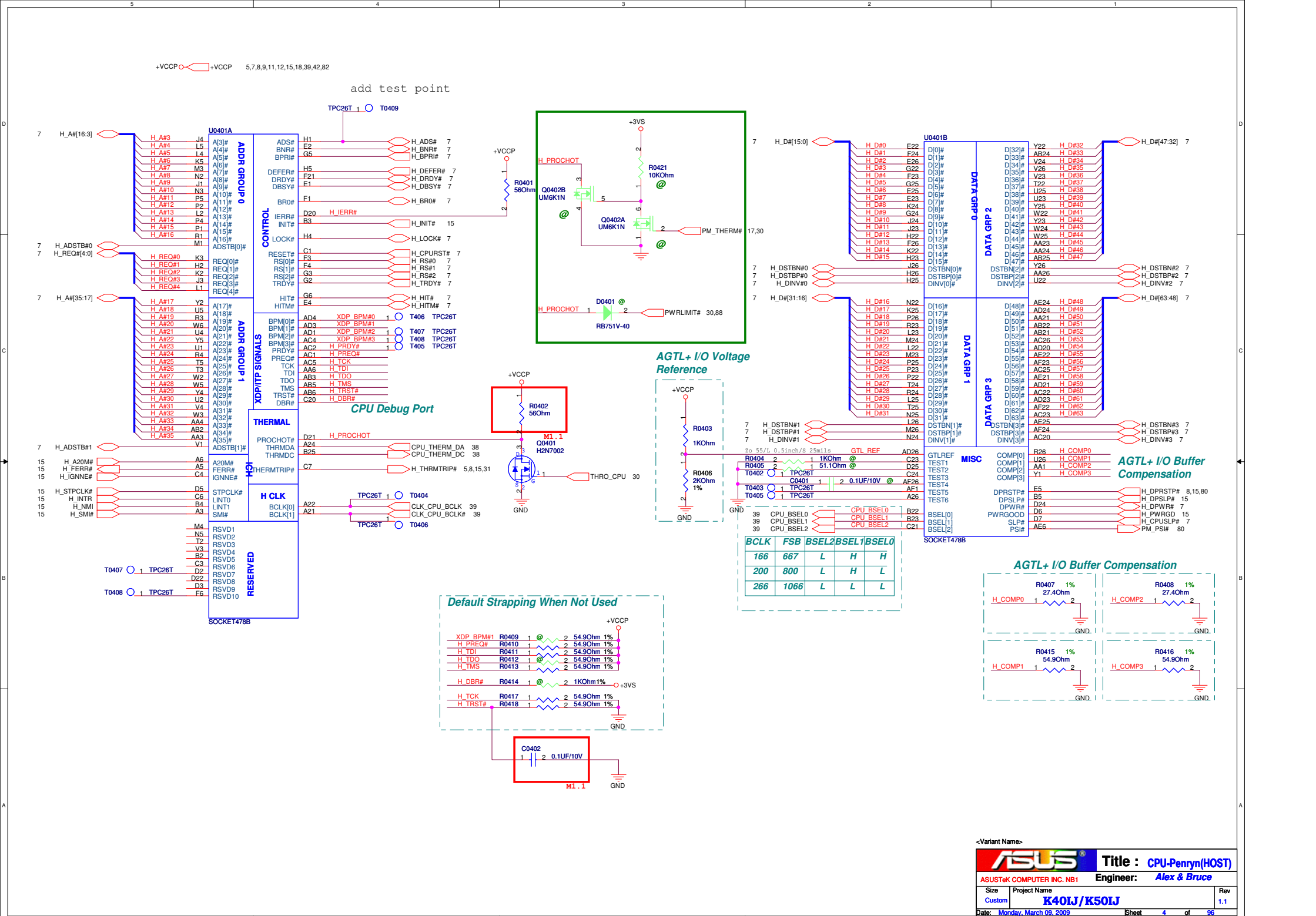
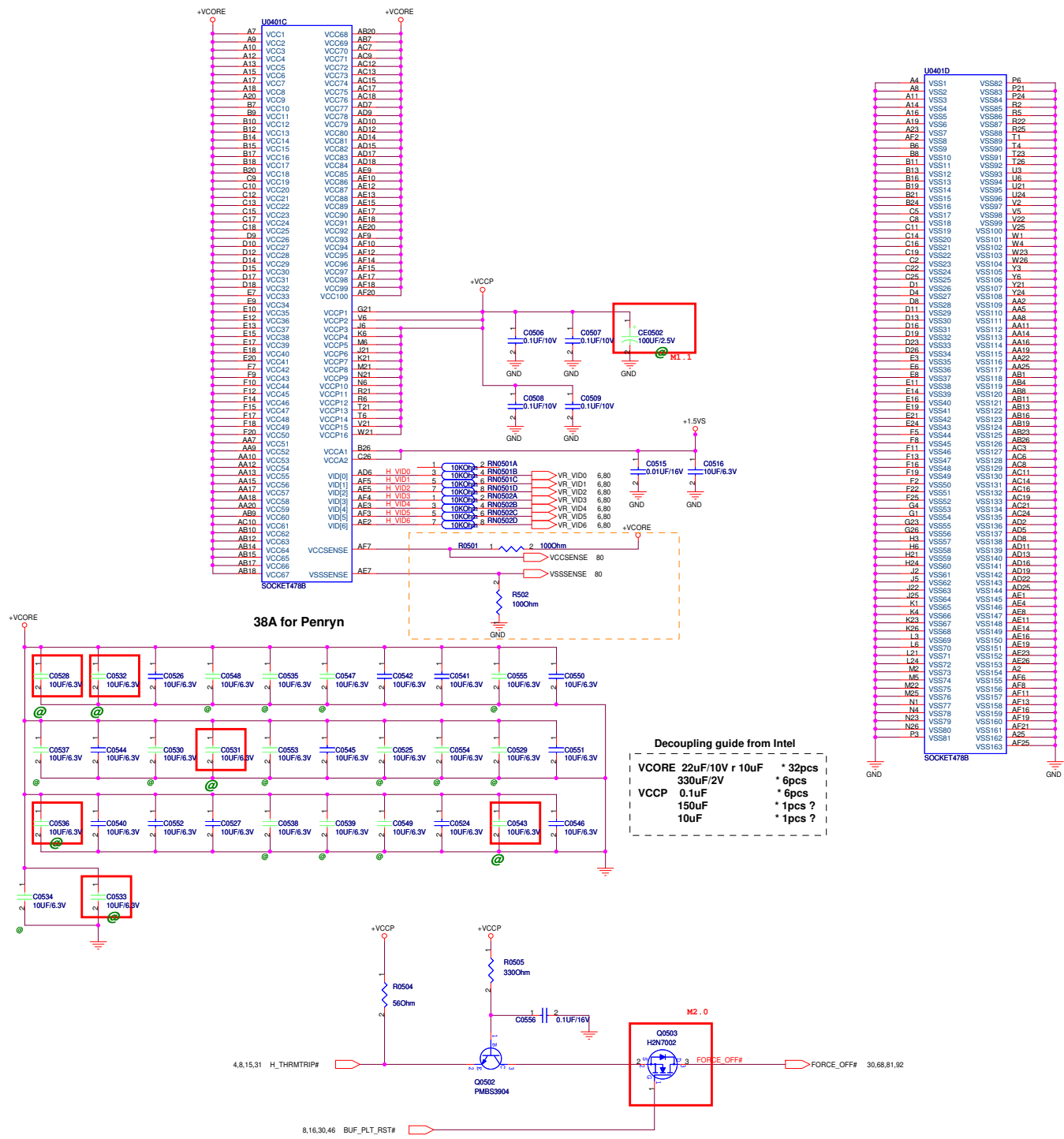


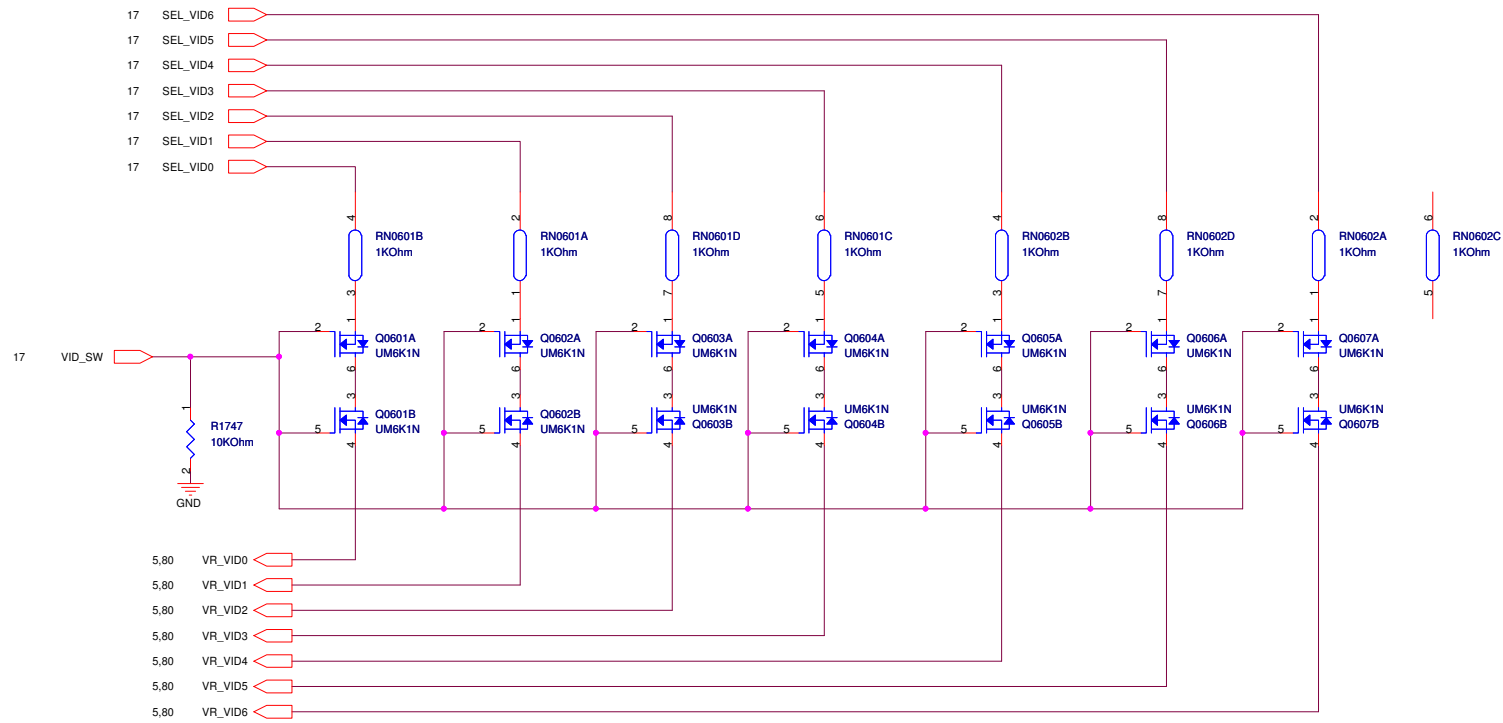


5				4				3				2				1			
GPIO3 Internal Pull High, Go Low= Flash Descriptor Security will be Overriden																			
INT PU*: PU or PD in special time																			
																</			





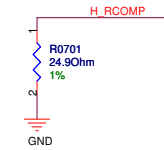




<Variant Name>

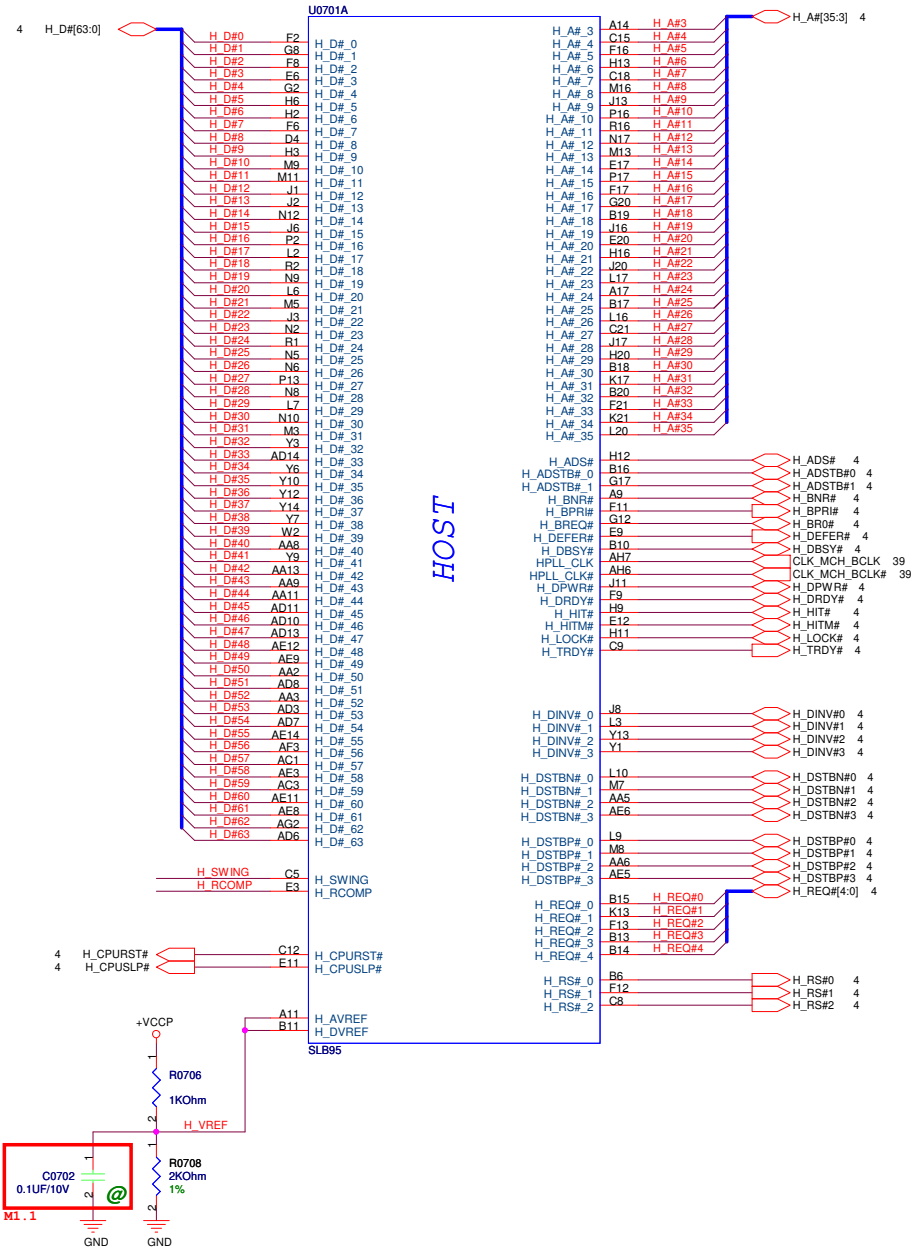
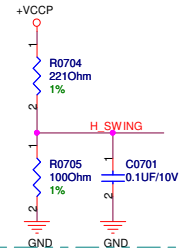
RCOMP

For Calibrating the FSB I/O Buffer



Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



<Variant Name>

GMCH Strapping

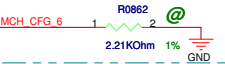
CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)



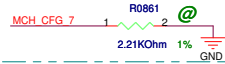
CFG6: iTMP

0 = Enabled
1 = Disabled (D)



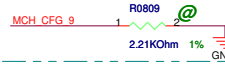
CFG7: ME TLS

0 = ME TLS with no confidentiality
1 = ME TLS with confidentiality (D)



CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)



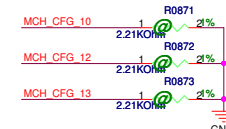
CFG10 : PCIE Loopback enable

CFG13:12 : GMCH Test Mode

0 = Enabled
1 = Disabled (D)

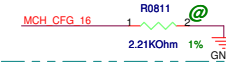
CFG13:12 : GMCH Test Mode

00 = Reserved
10 = XOR Mode Enable
01 = All Z Mode Enable
11 = Normal Operation (D)



CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)



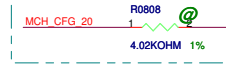
CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed



CFG20 : Concurrent SDVO / PCie

0 = Only one is operational (D)
1 = operate simultaneous



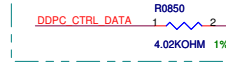
SDVO_CTRL_DATA : SDVO/iHDMI/DP Interface Present

0 = SDVO/iHDMI/DP Disabled (D)
1 = SDVO/iHDMI/DP Enabled

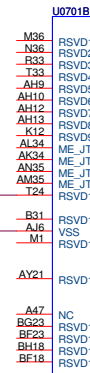
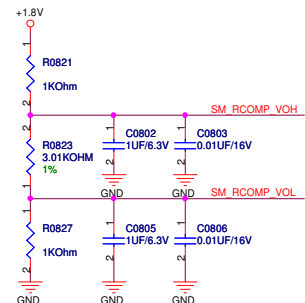
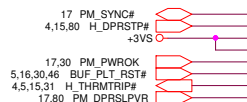
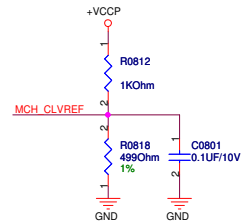
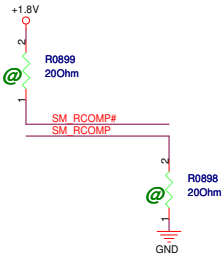


DDPC_CTRL_DATA : SDVO/iHDMI/DP Device Present

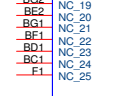
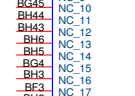
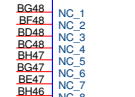
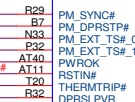
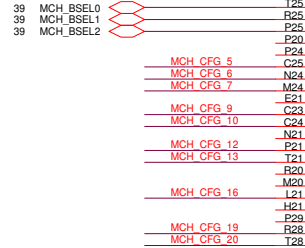
0 = No SDVO/iHDMI/DP (D)
1 = SDVO/iHDMI/DP Present



Only one of the CFG10/CFG12/CFG13 DDPC_CTRL_DATA & SDVO_CTRL_DATA straps can be enabled at any time. should both be high to enable Display Port.



BCLK	FSB	BSEL2	BSEL1	BSEL0
266	1066	L	L	L
166	667	L	H	H
200	800	L	H	L



RSVD

DDR

CLK

DM

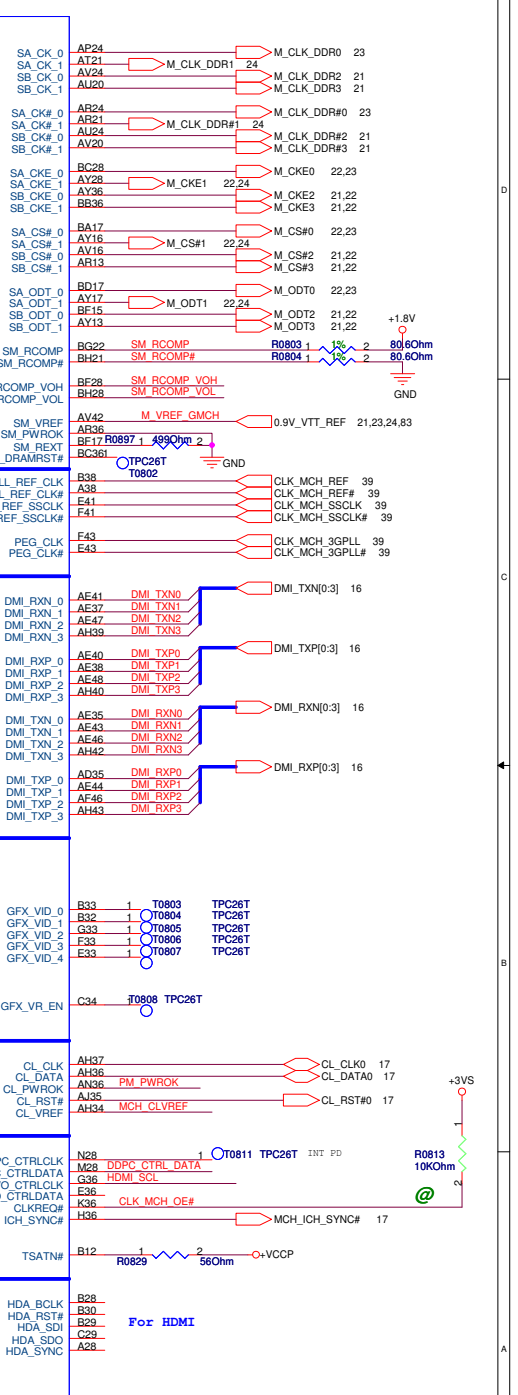
GRAPHICS VID

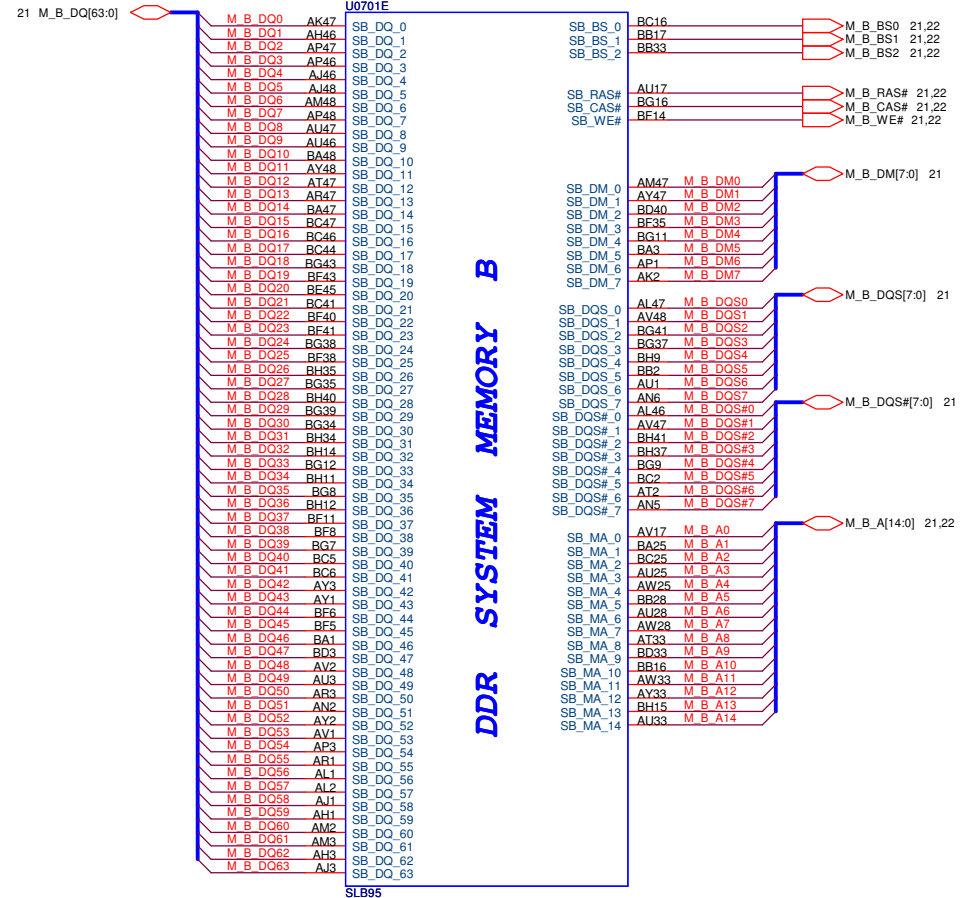
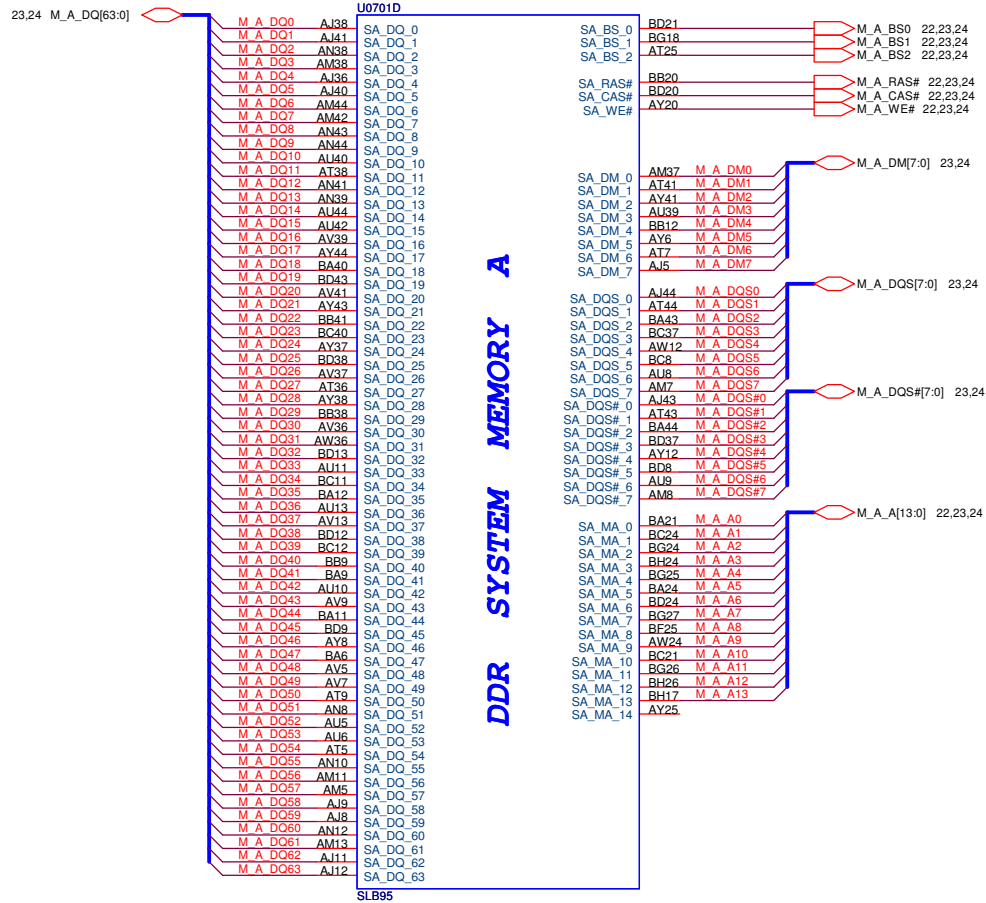
PM

ME

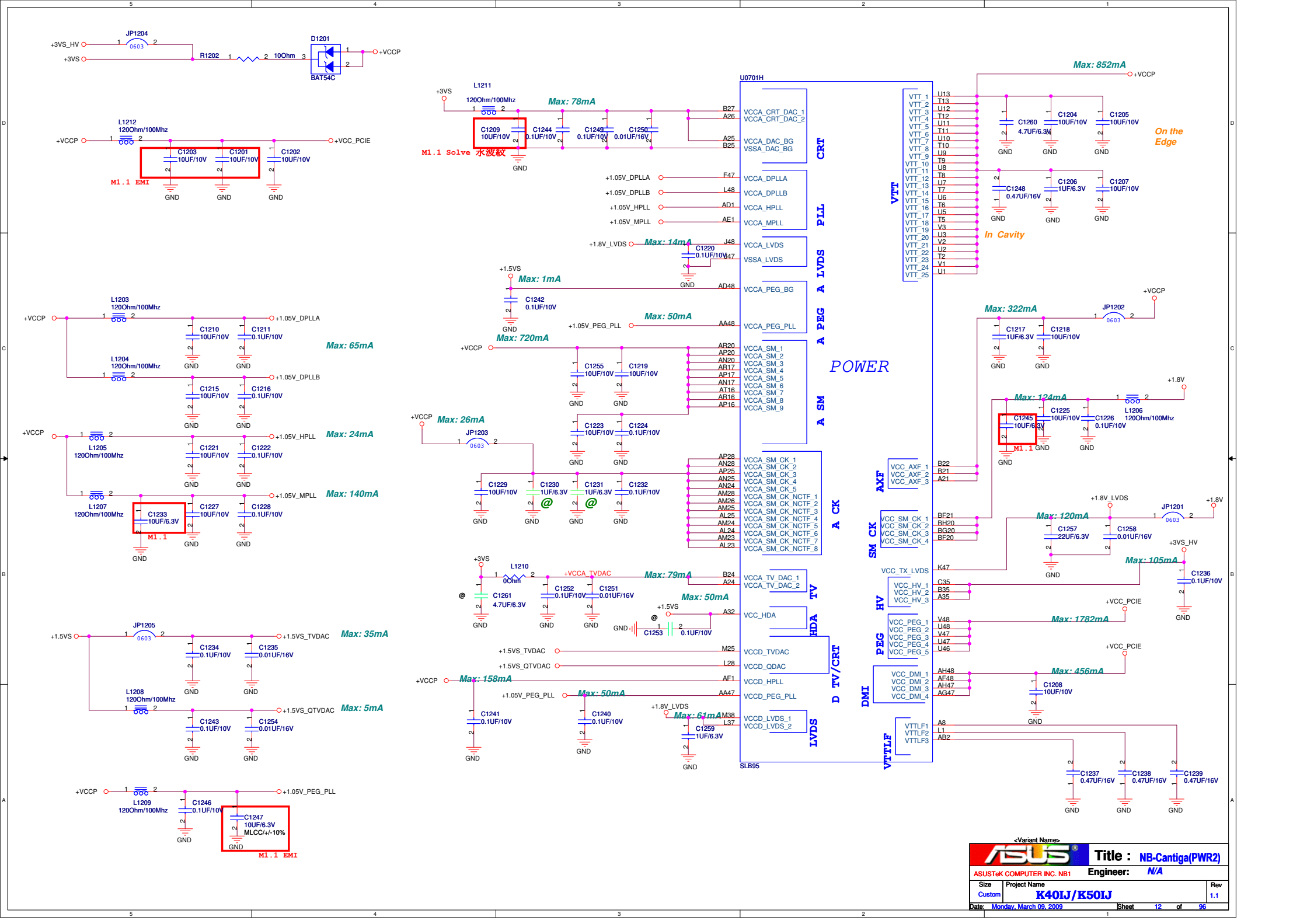
MISC

HDA

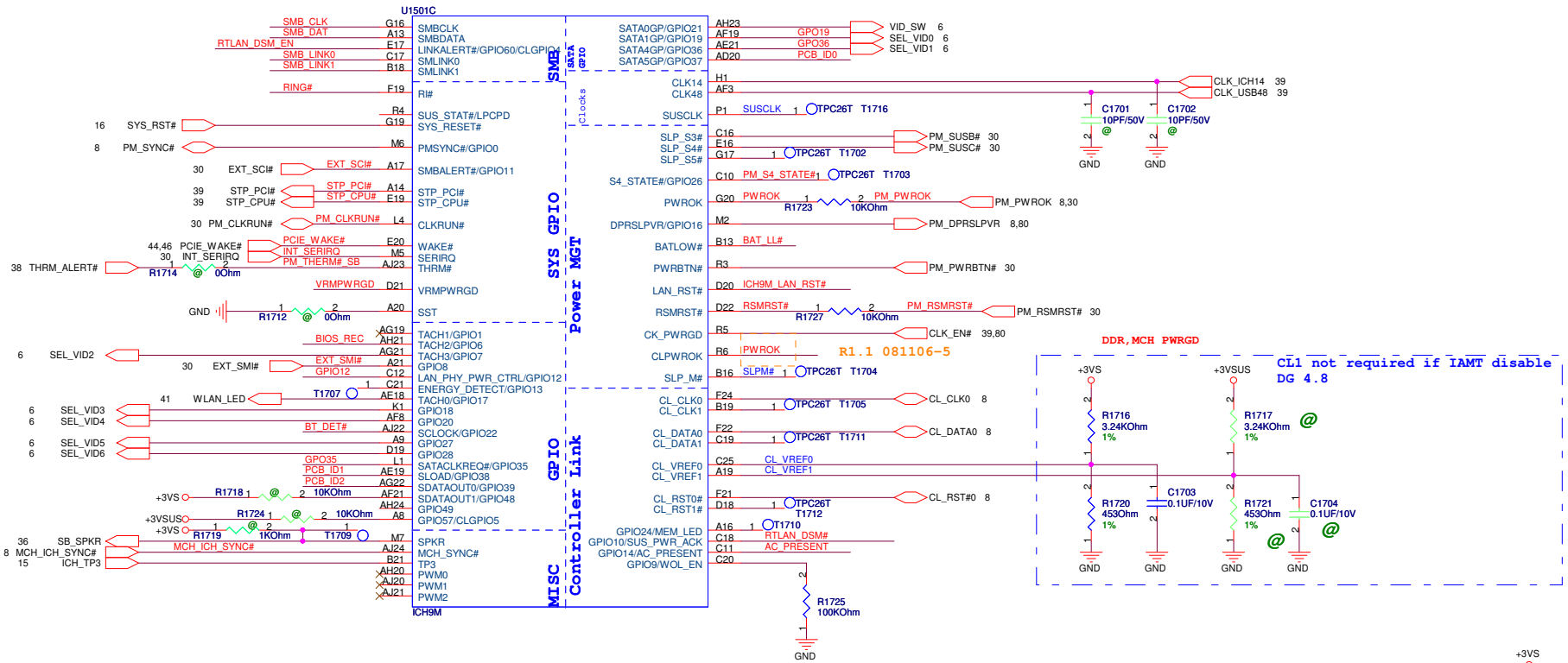




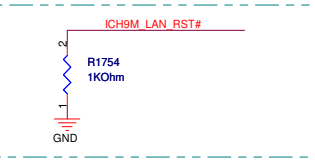
<Variant Name>





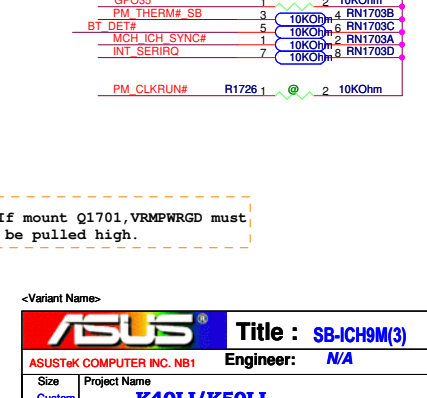
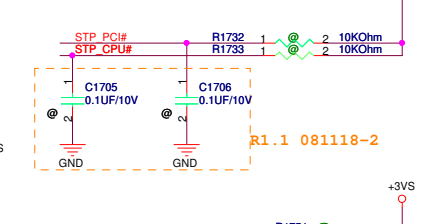
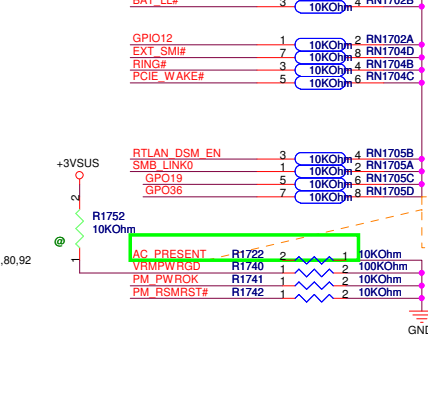
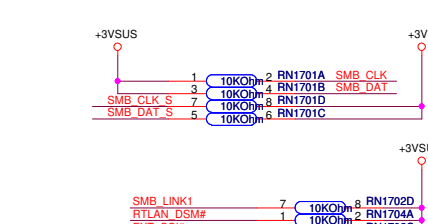
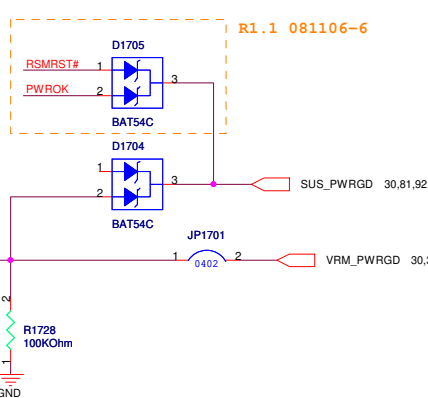
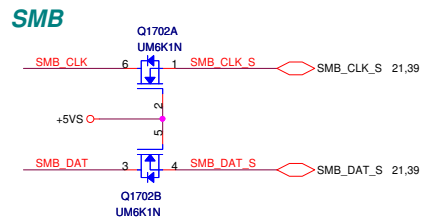
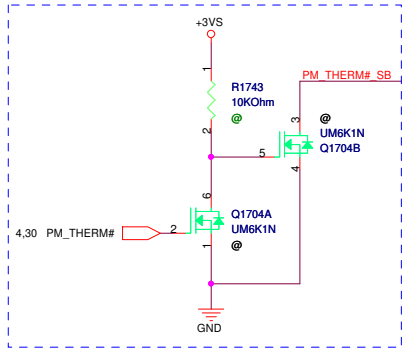
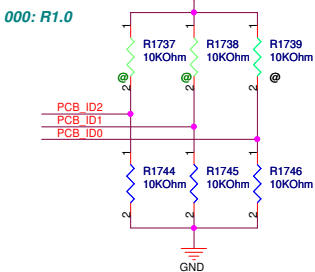


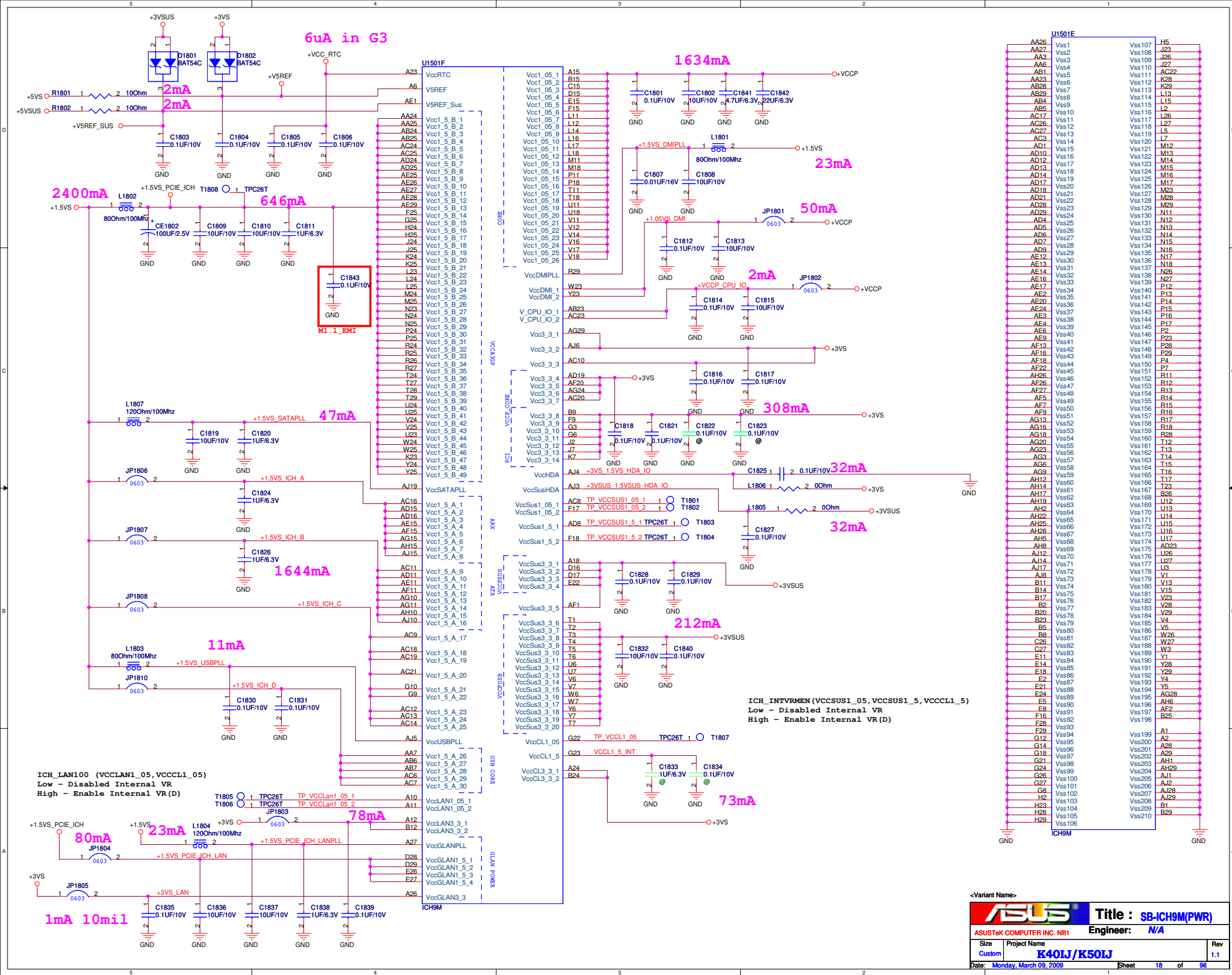
No Reboot Strap
Low = Default
High = No Reboot

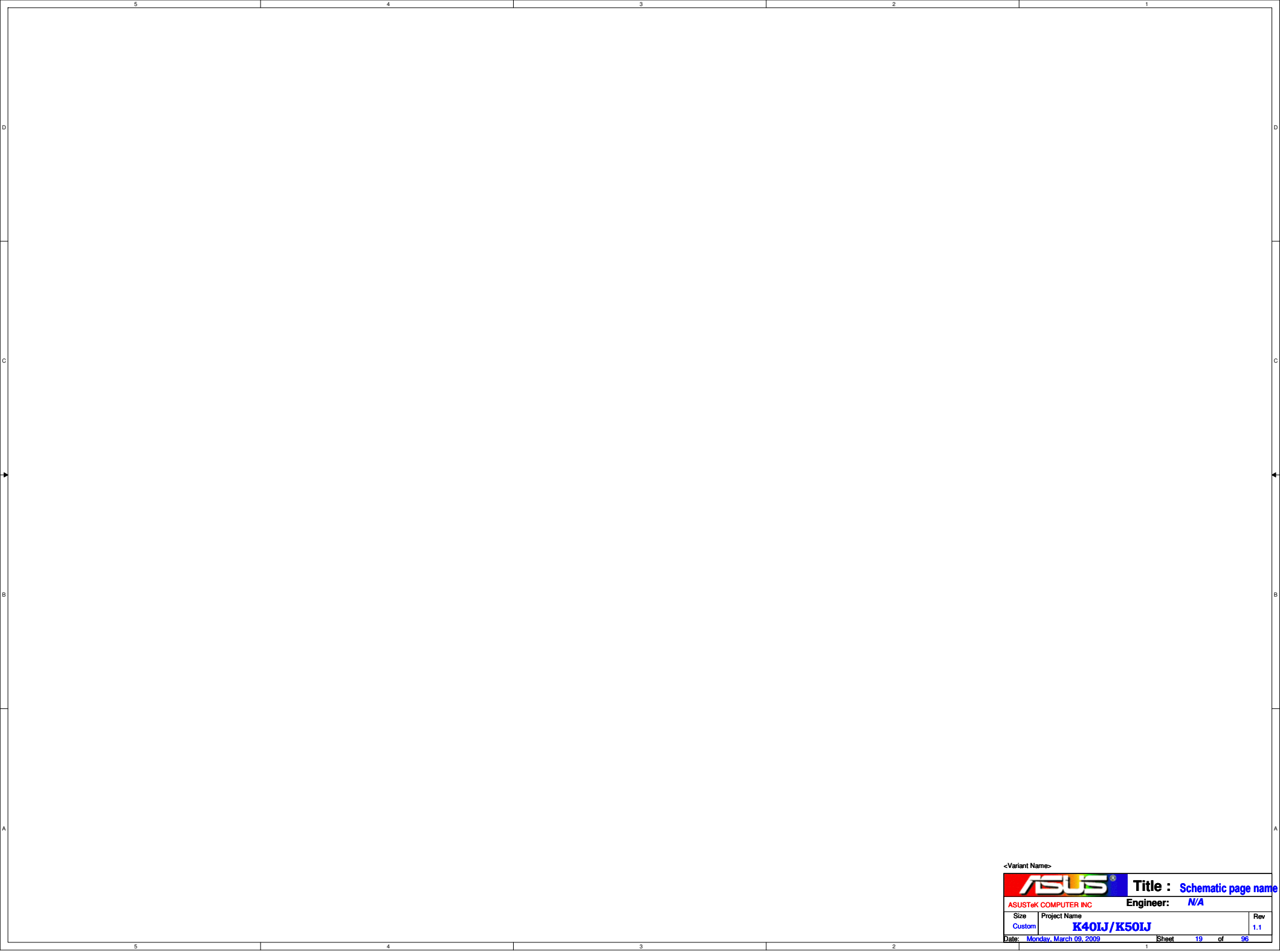


For BIOS Recovery
Place Near the Open Door

PCB_ID[0:2]
000: R1.0









<Variant Name>



Title : **DDR2 SO-DIMM0**

ASUSTeK COMPUTER INC. NB1

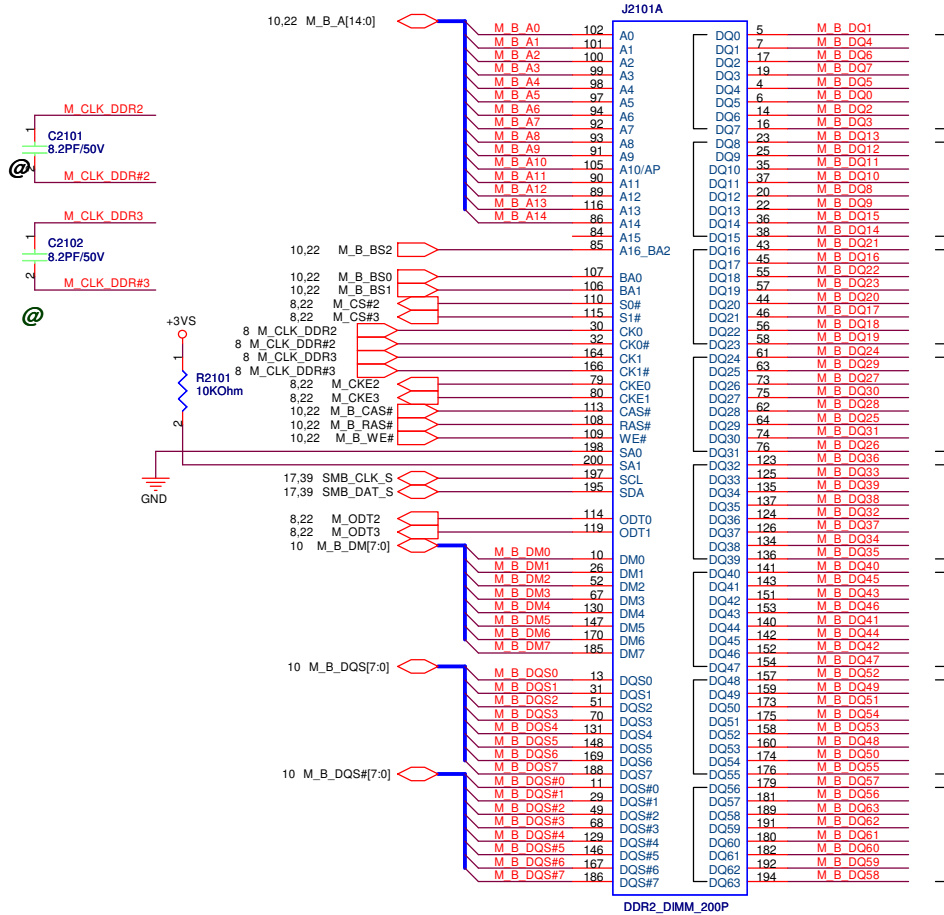
Engineer: **N/A**

Size	Project Name	Rev
A3	K40IJ/K50IJ	1.1

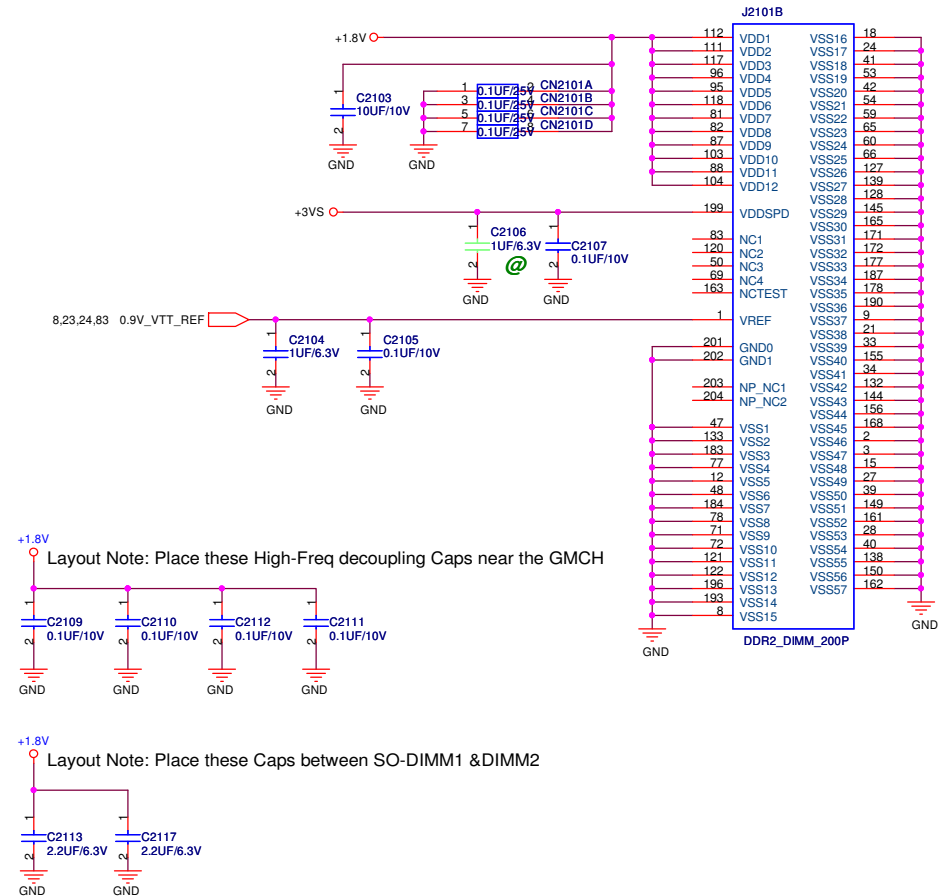
Date: **Monday, March 09, 2009** Sheet **20** of **96**

DDR2 200P H=9.2mm (Reverse Type)

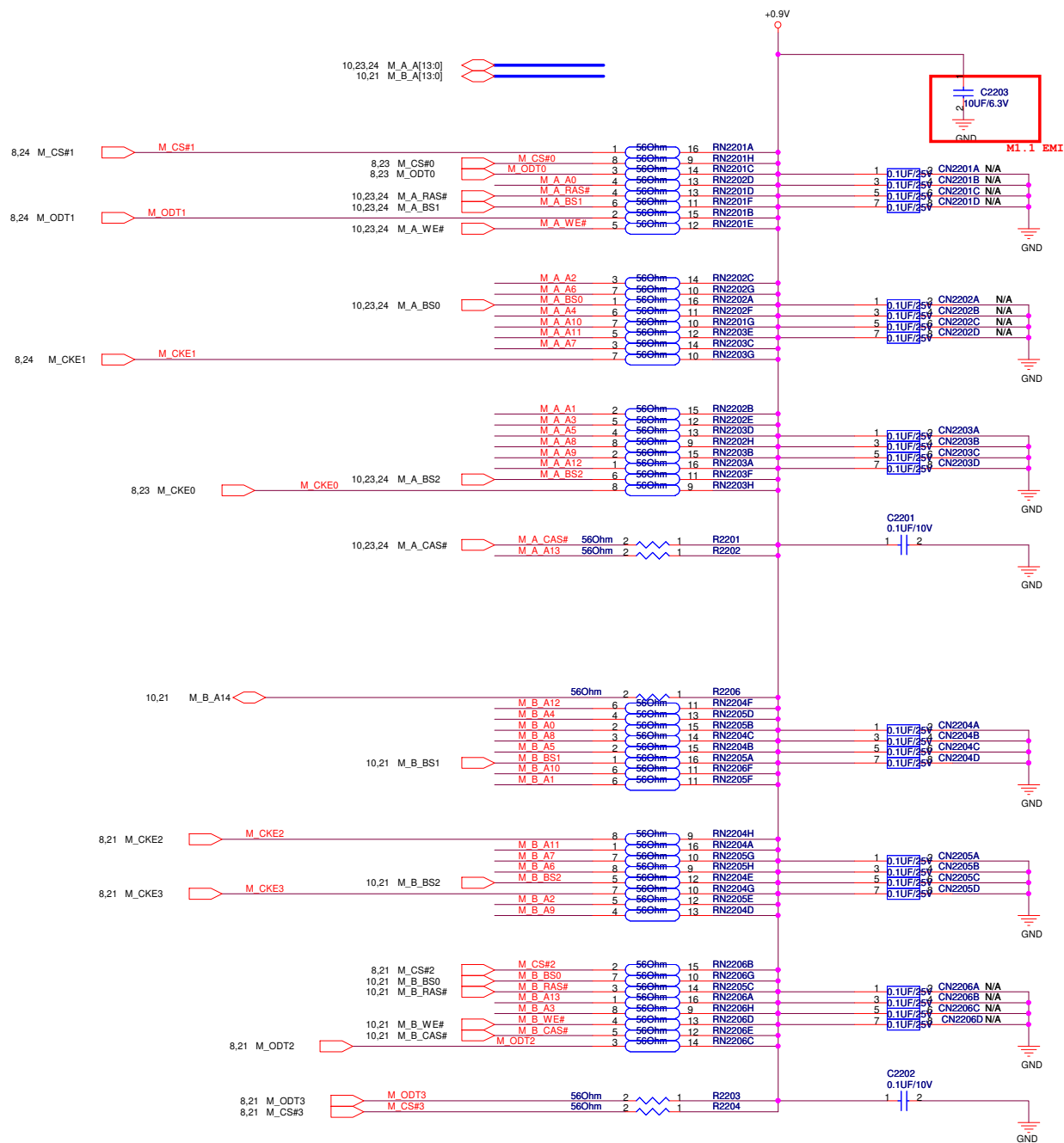
M_B_DQ[63:0] 10

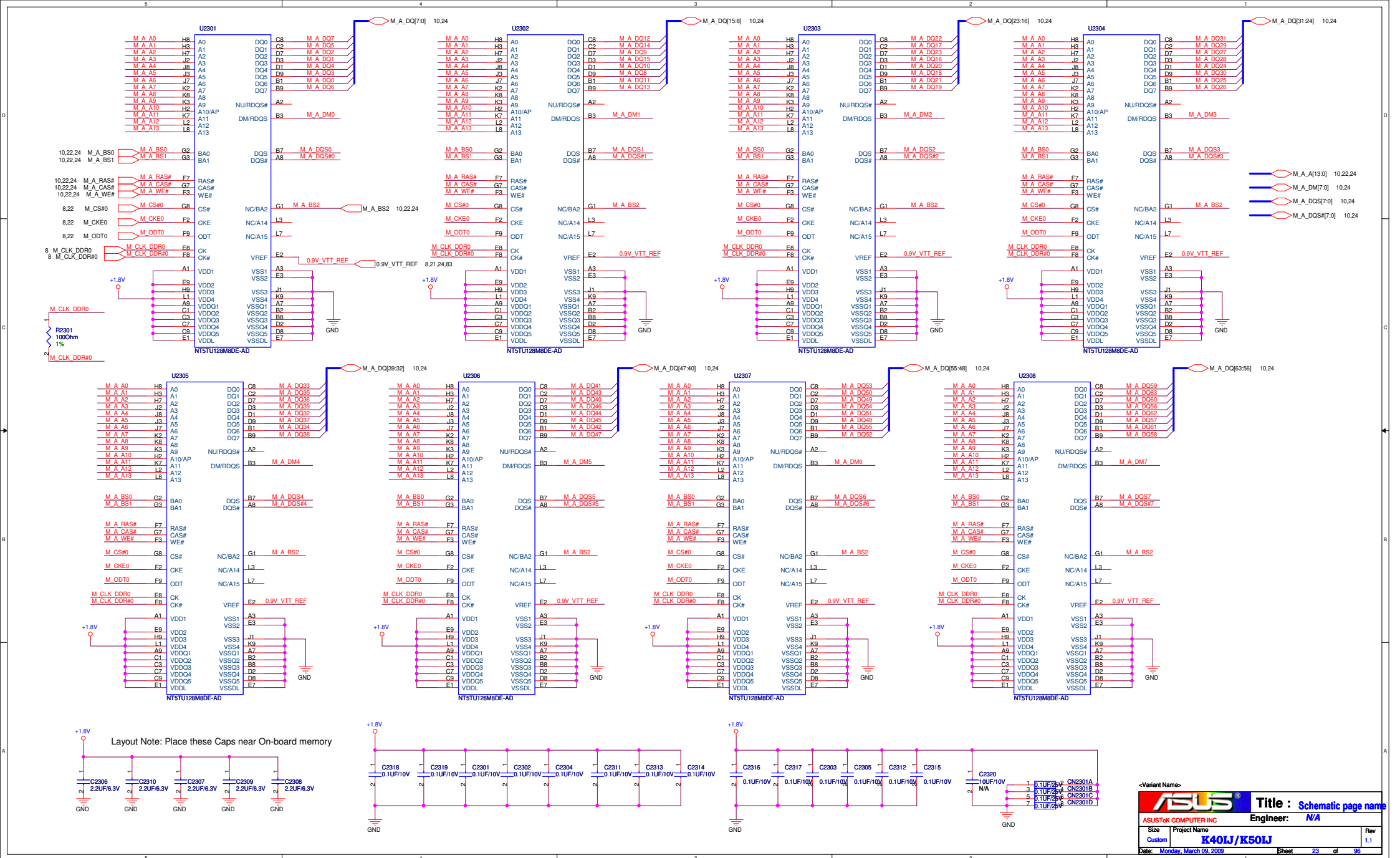


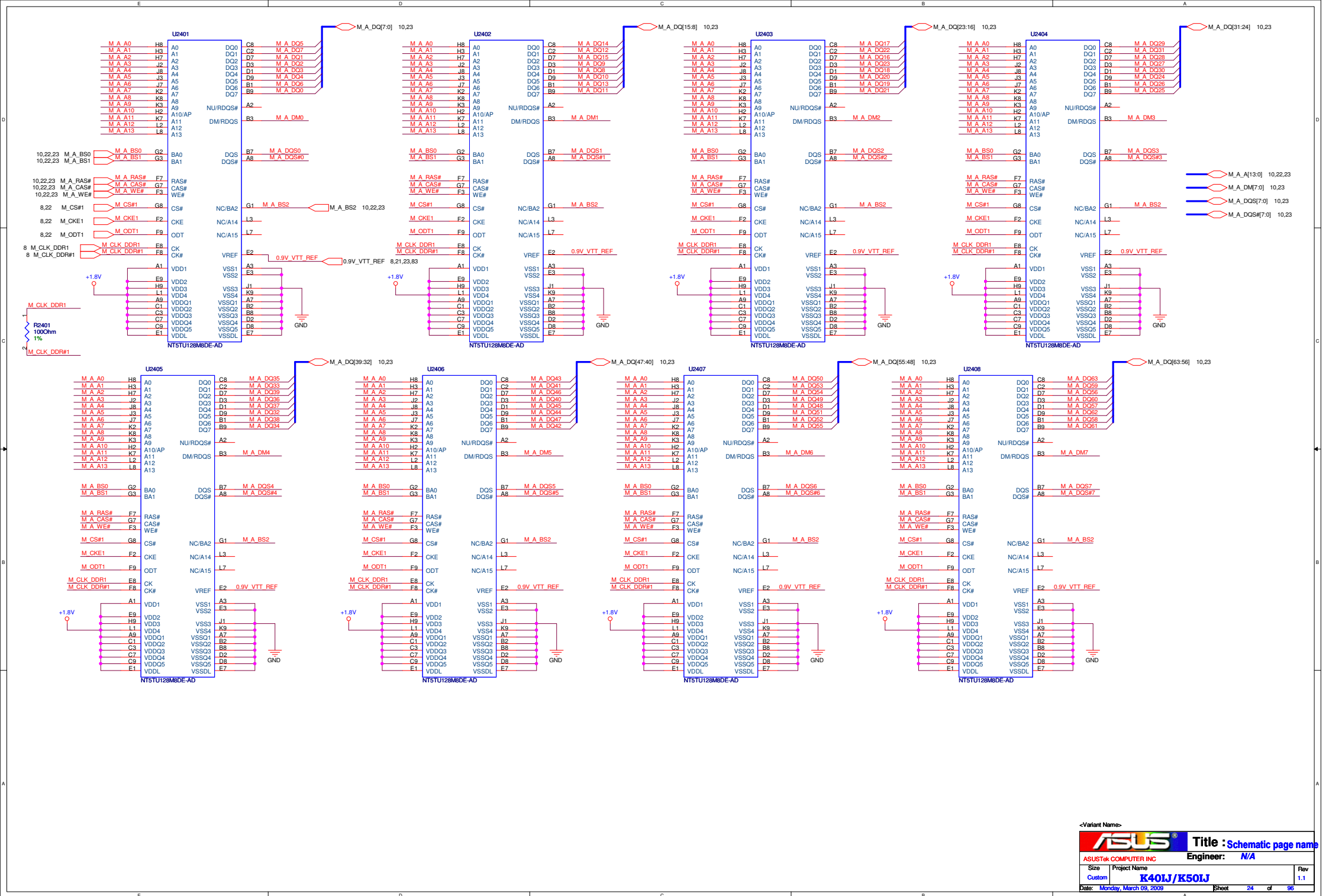
DDR2_DIMM_200P



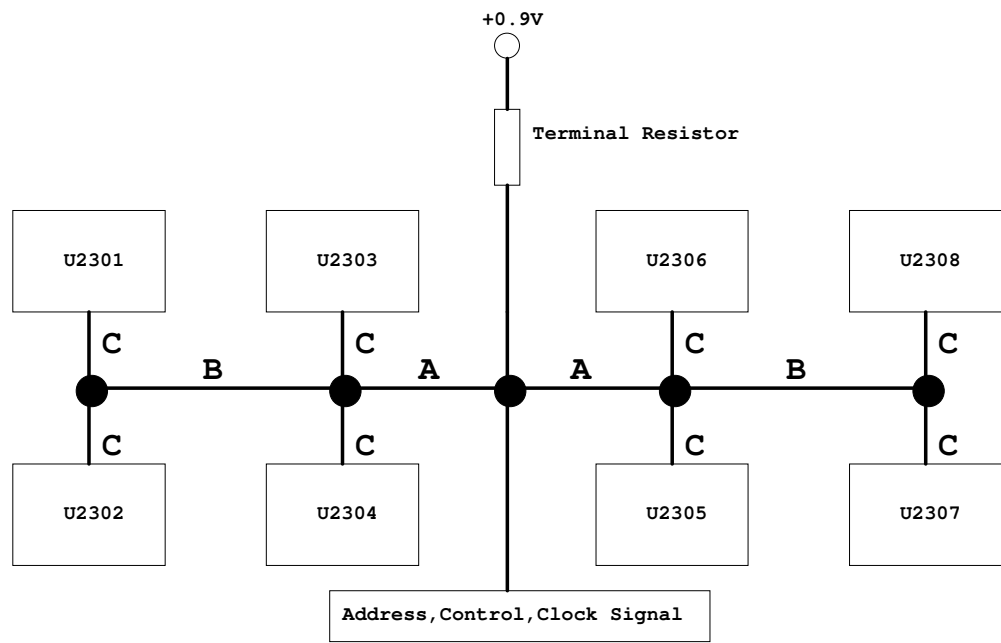
<Variant Name>

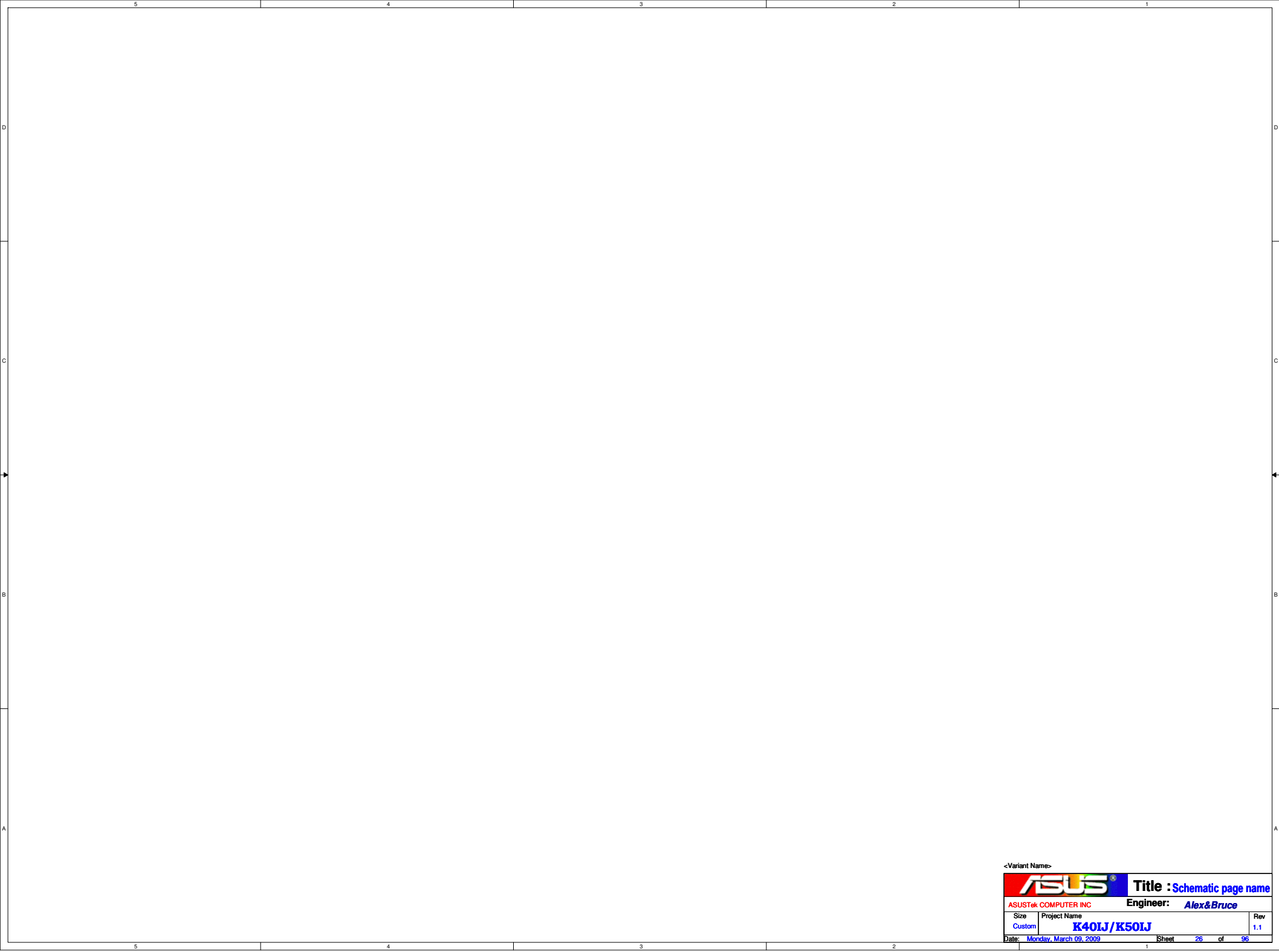


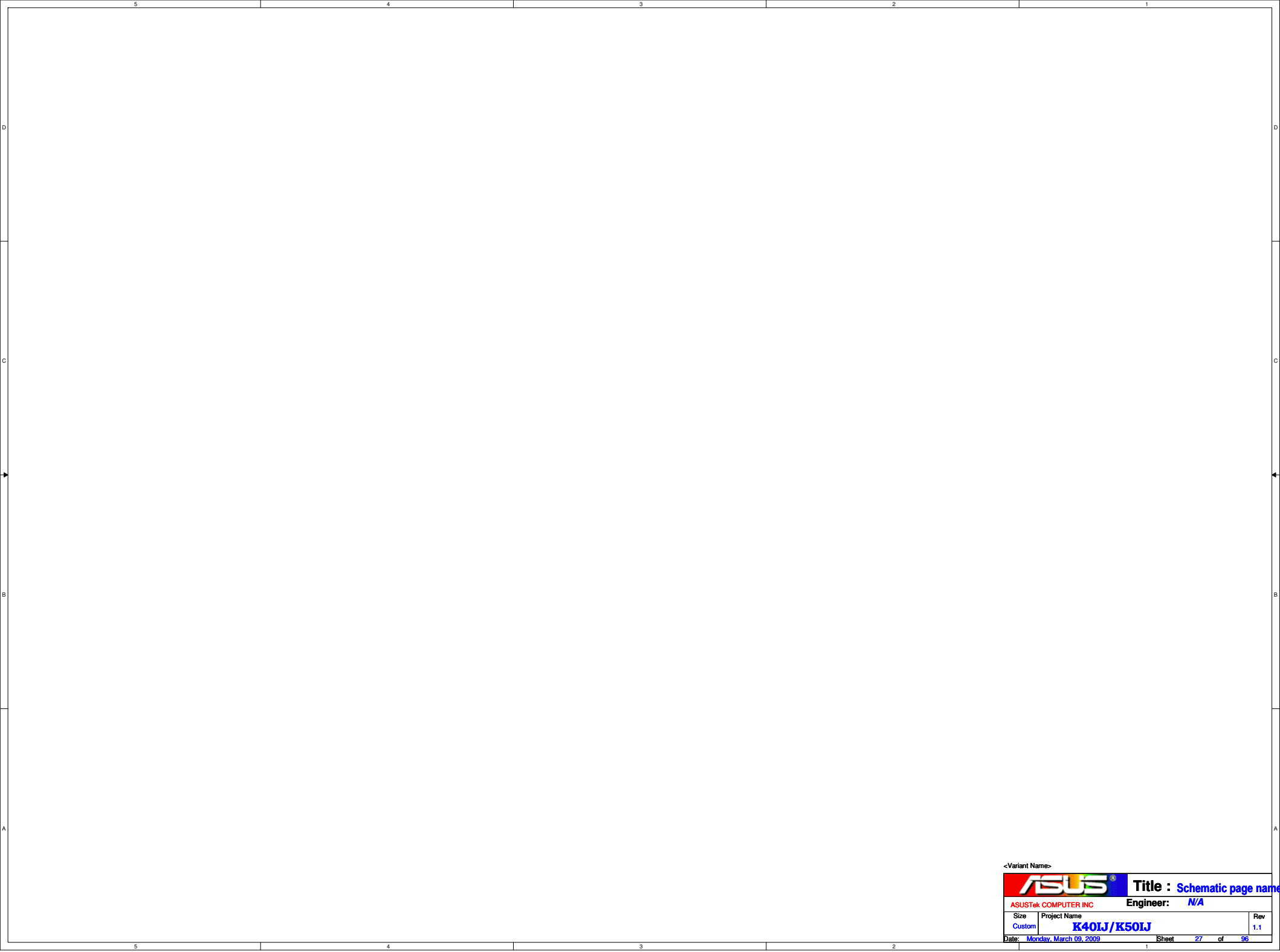




<Variant Name>







<Variant Name>



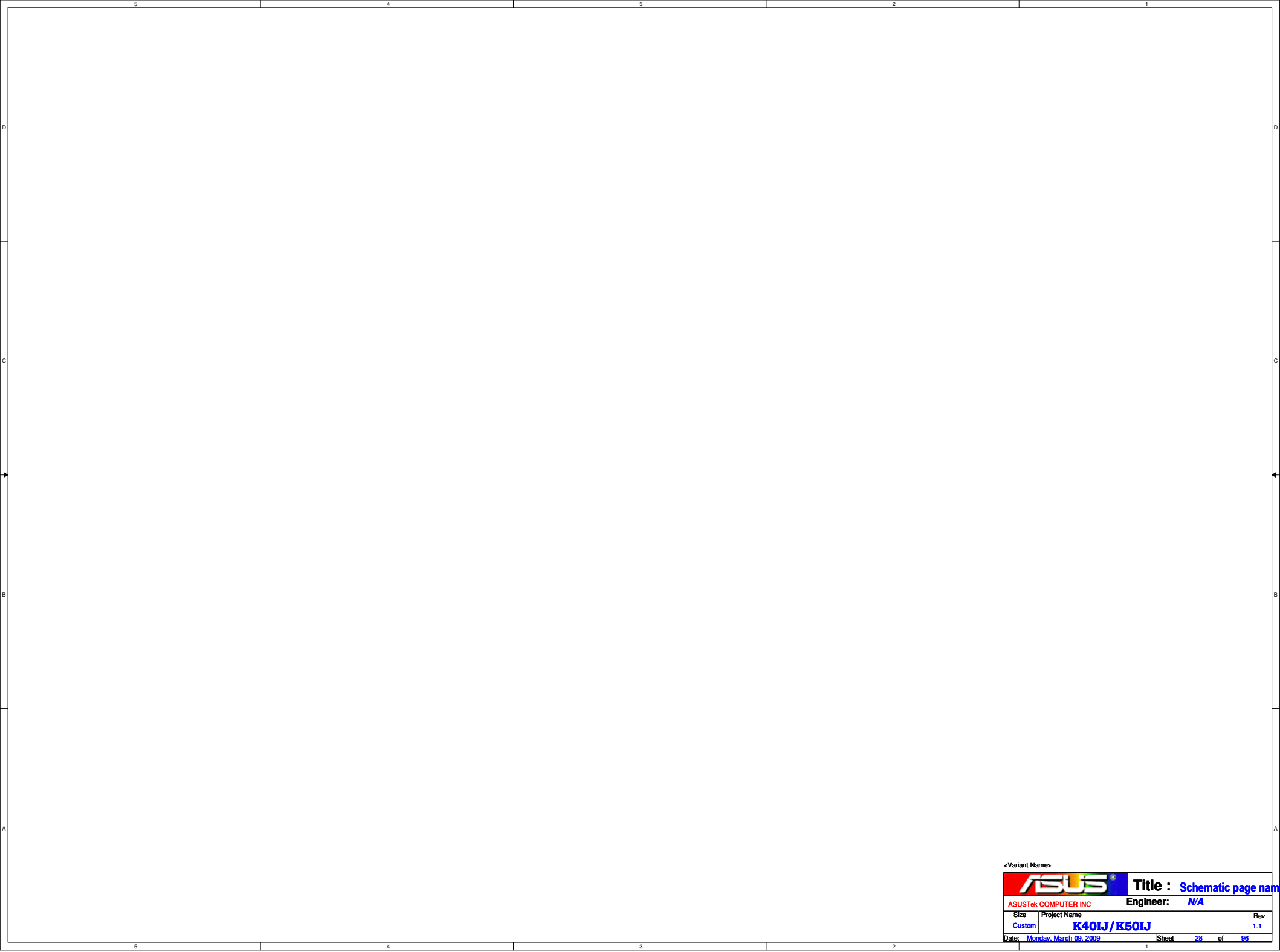
Title : Schematic page name

ASUSTek COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009Sheet 27 of 96



<Variant Name>



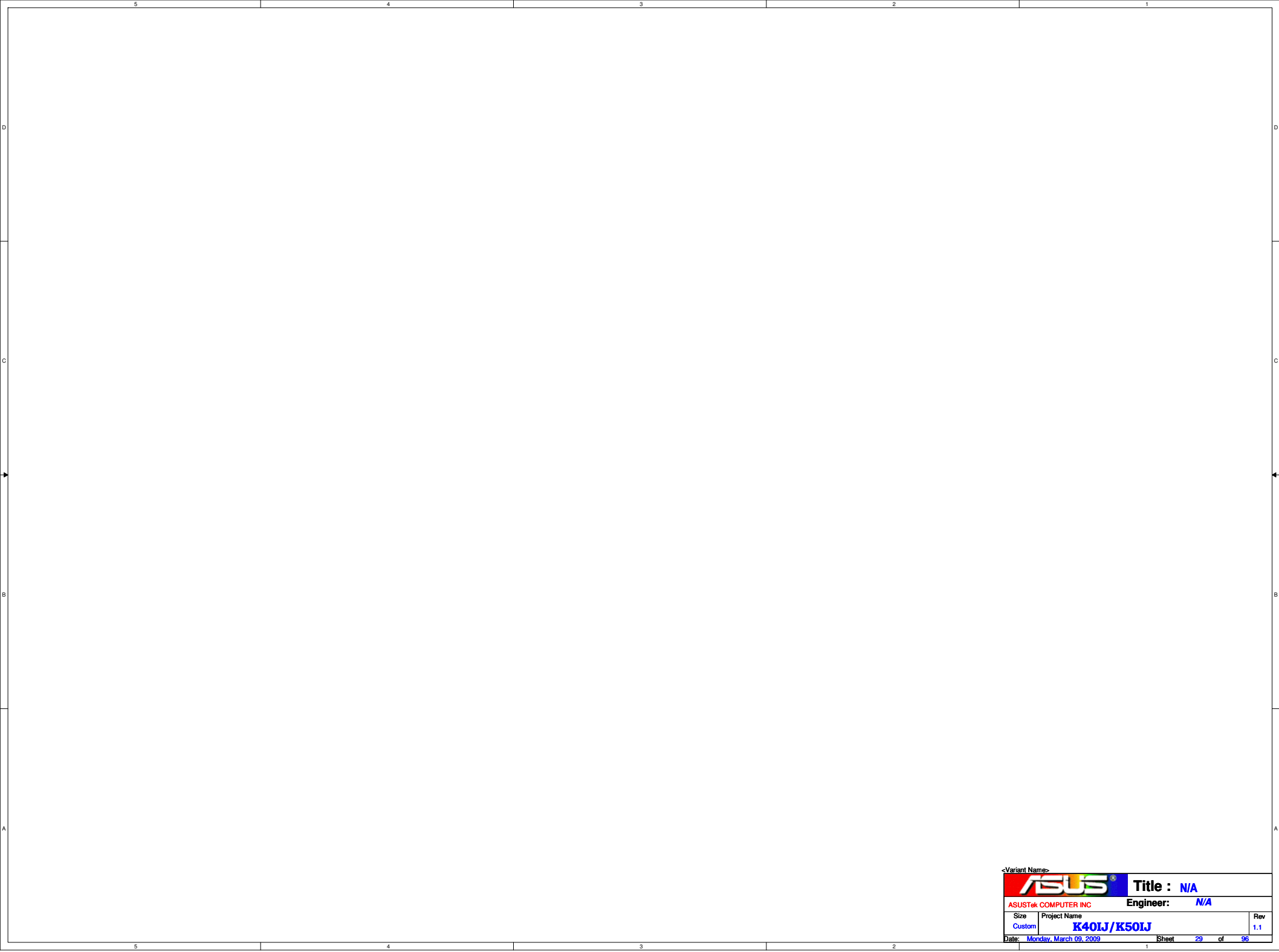
Title : Schematic page name

ASUSTek COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009Sheet 28 of 96



<Variant Name>



Title : **N/A**

ASUSTek COMPUTER INC

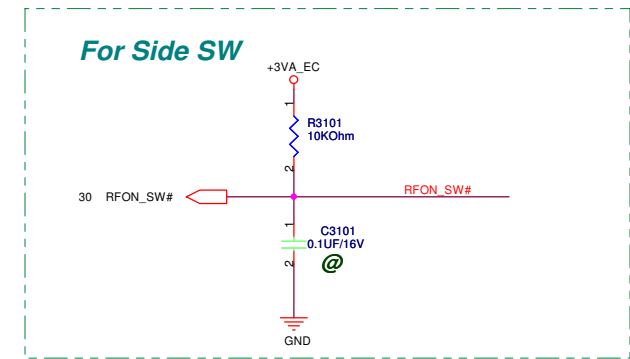
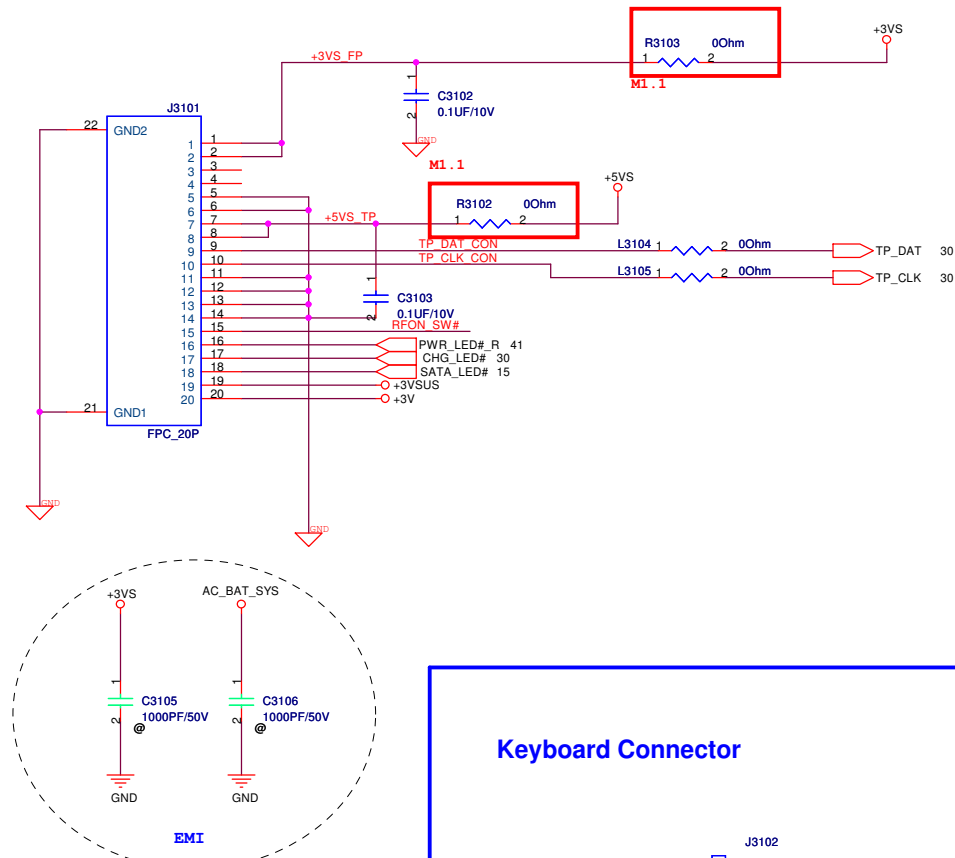
Engineer: **N/A**

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

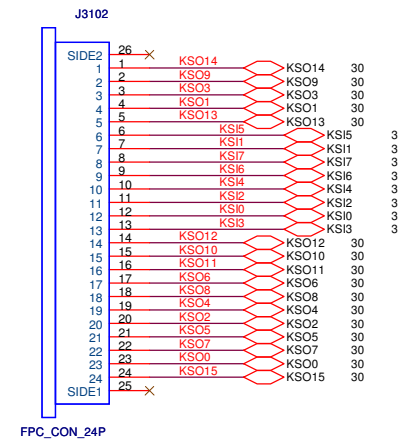
Date: **Monday, March 09, 2009**

Sheet **29** of **96**

TouchPad & FingerPrint

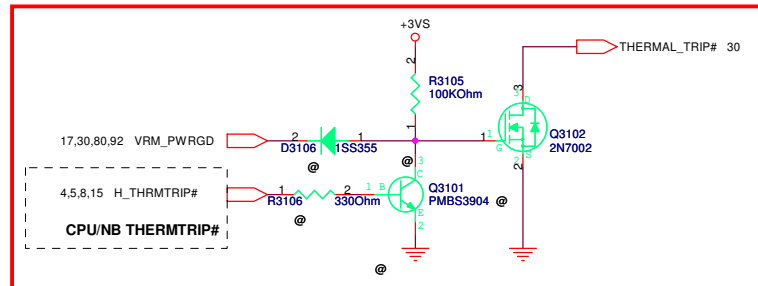


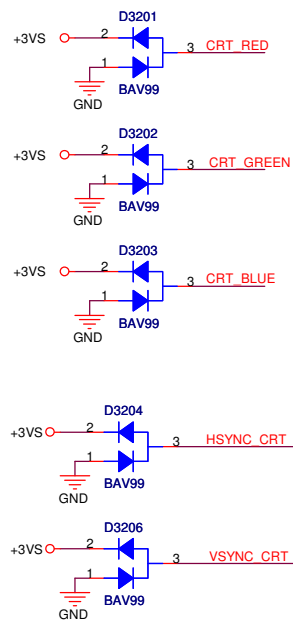
Keyboard Connector



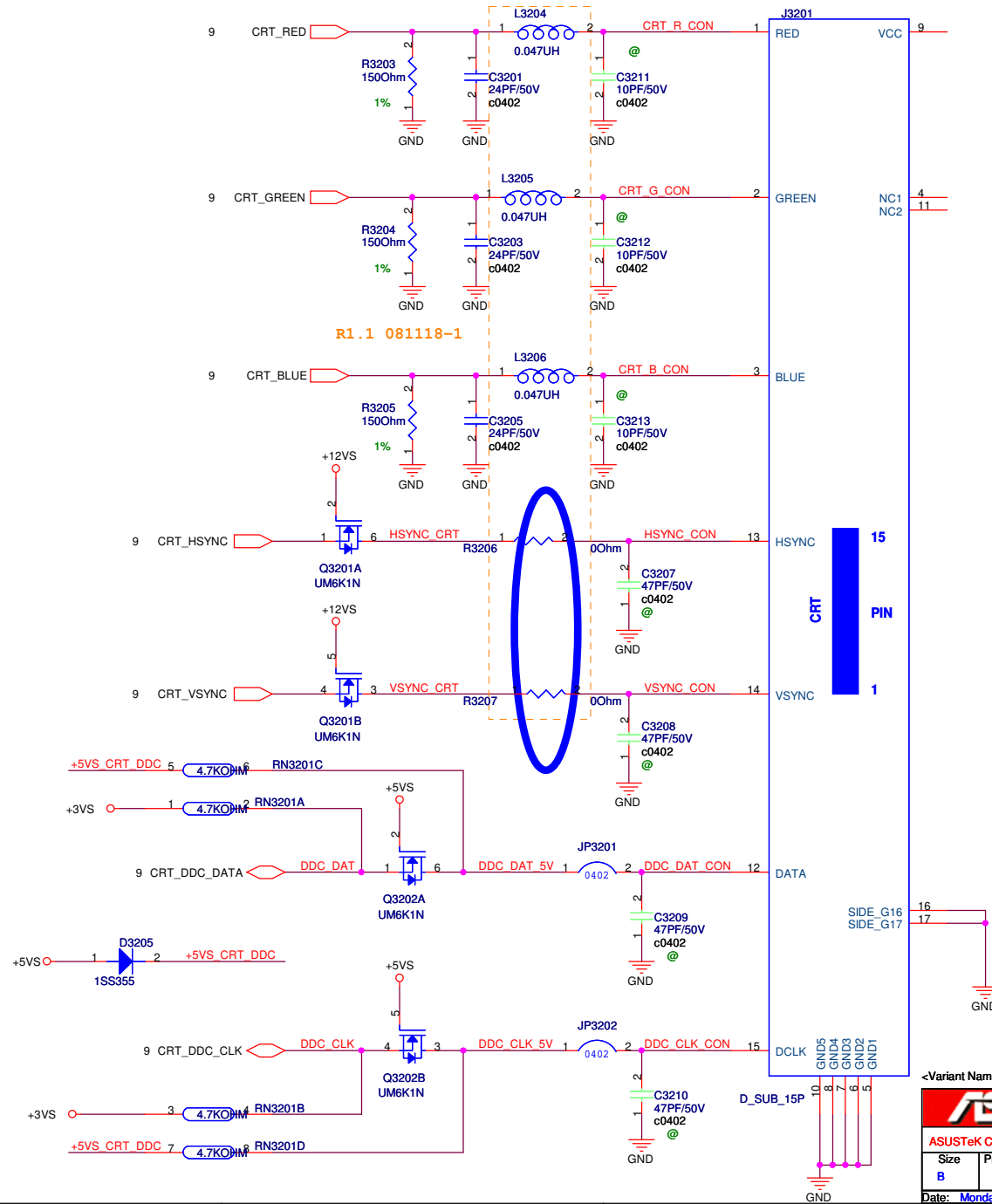
For Thermal Control Method

Remove redundant components



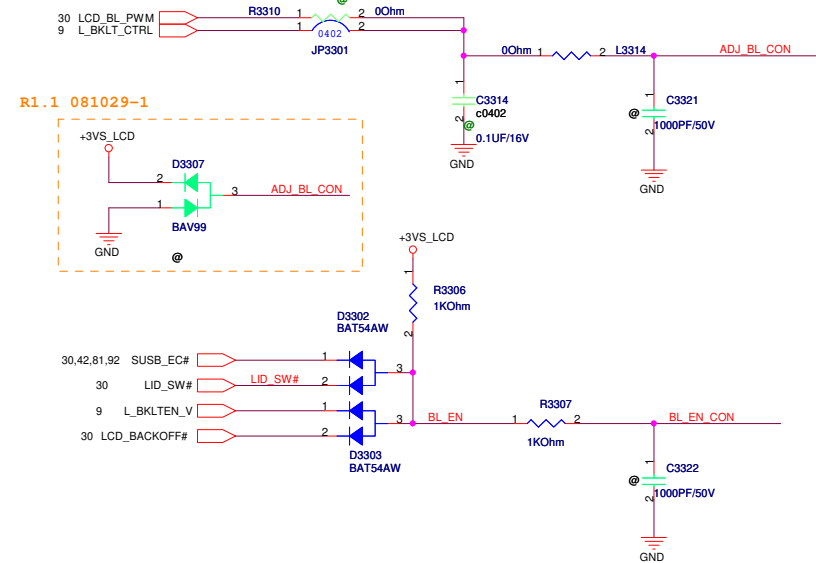
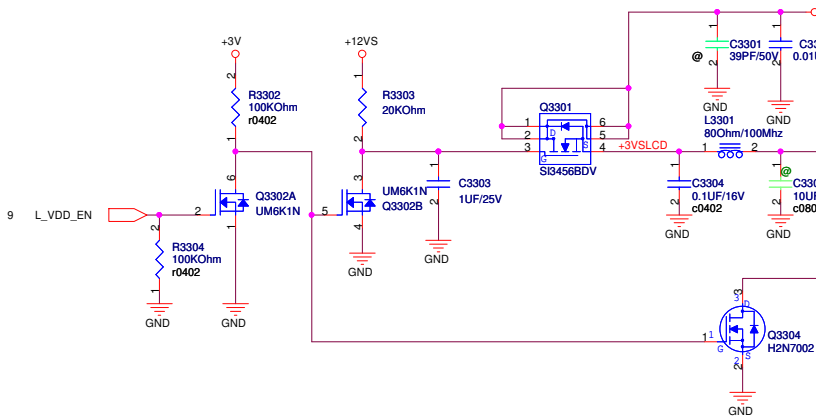


PLACE ESD Diodes near VGA port

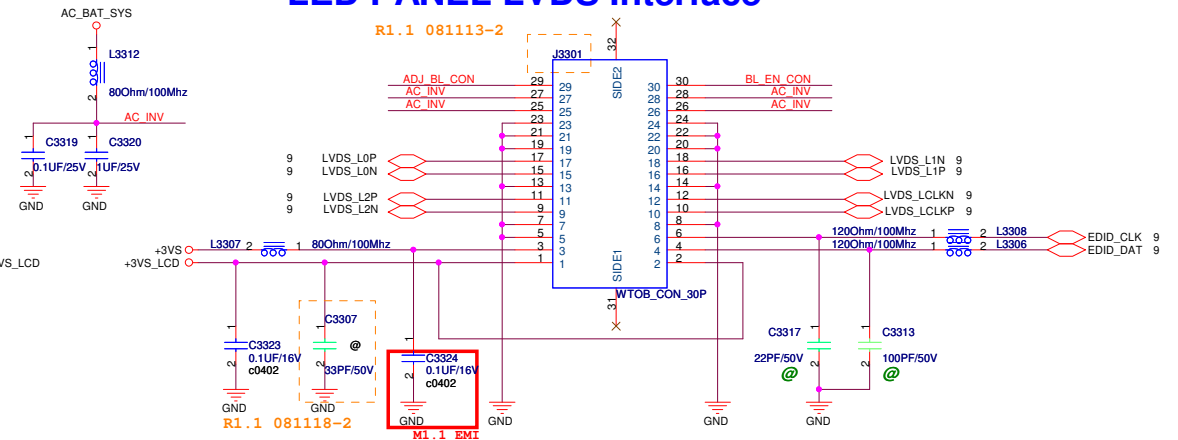


ASUS		Title : CRT	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size B	Project Name K40IJ/K50IJ	Rev 1.1	
Date: Monday, March 09, 2009		Sheet 32 of 96	

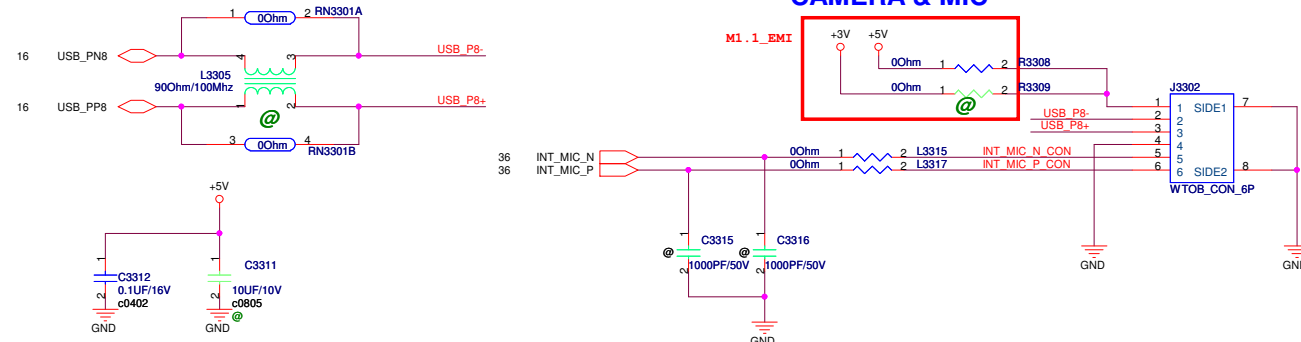
LCD Power



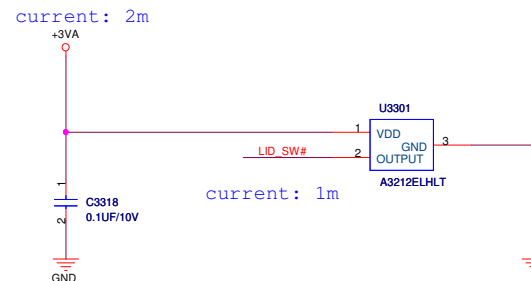
LED PANEL LVDS Interface



CAMERA & MIC



Hall effect switch



<Variant Name>

ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	K40LJ/K50LJ		1.1
Date: Monday, March 09, 2009	Sheet	33	of 96

For Bluetooth

<Variant Name>

		Title : BT	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	34 of 96

5	4	3	2	1
D				D
C				C
B				B
A				A

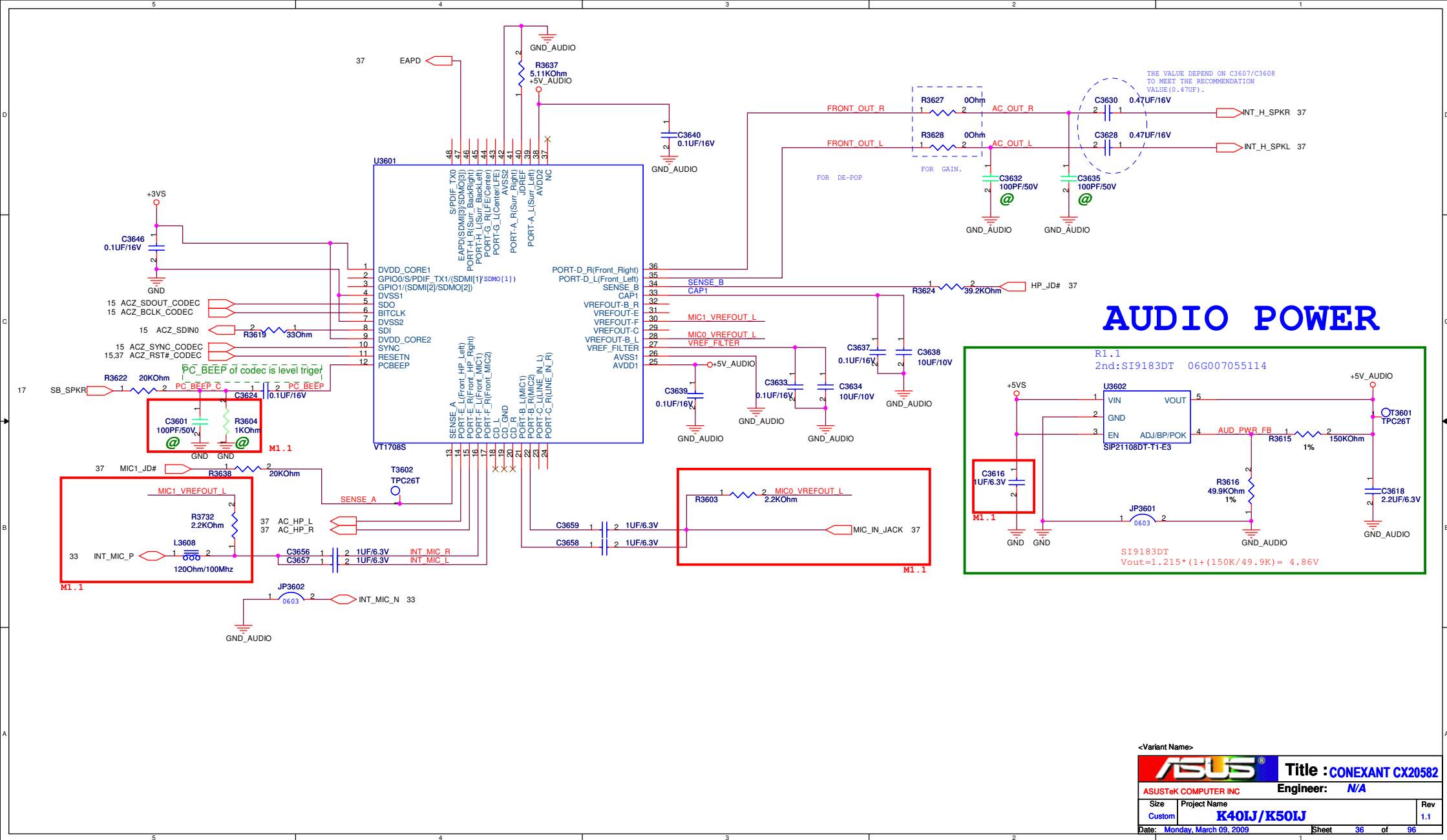
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Title : N/A

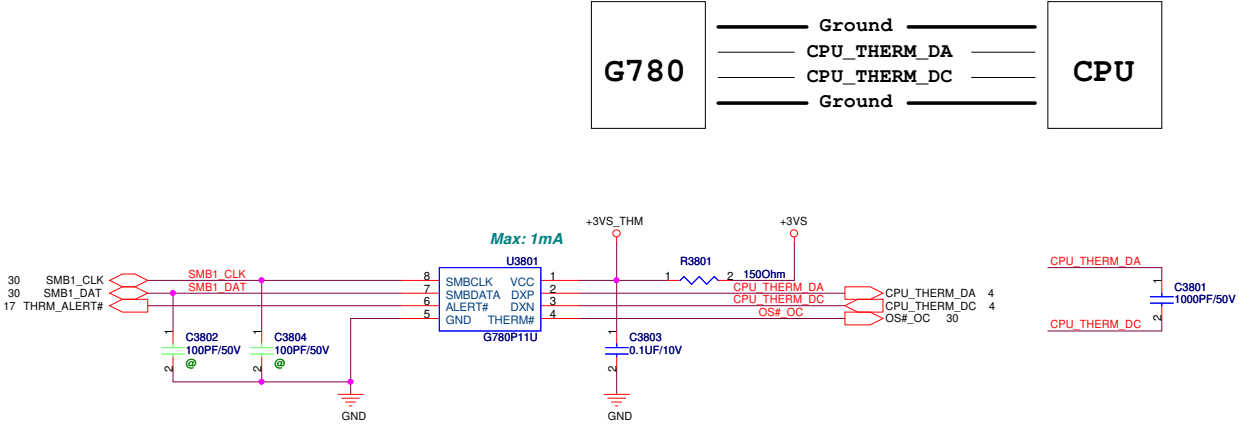
ASUSTek COMPUTER INCEngineer: N/A

Size A	Project Name K40IJ/K50IJ	Rev 1.1
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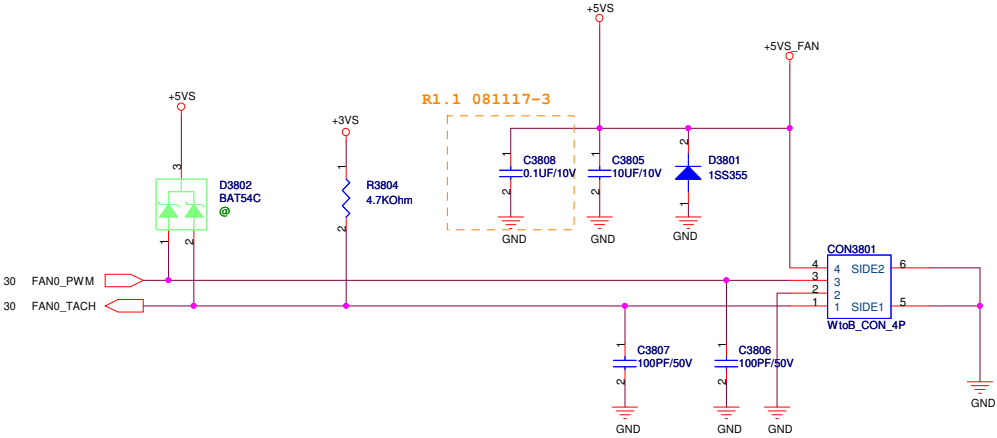
Date: Monday, March 09, 2009Sheet 35 of 96

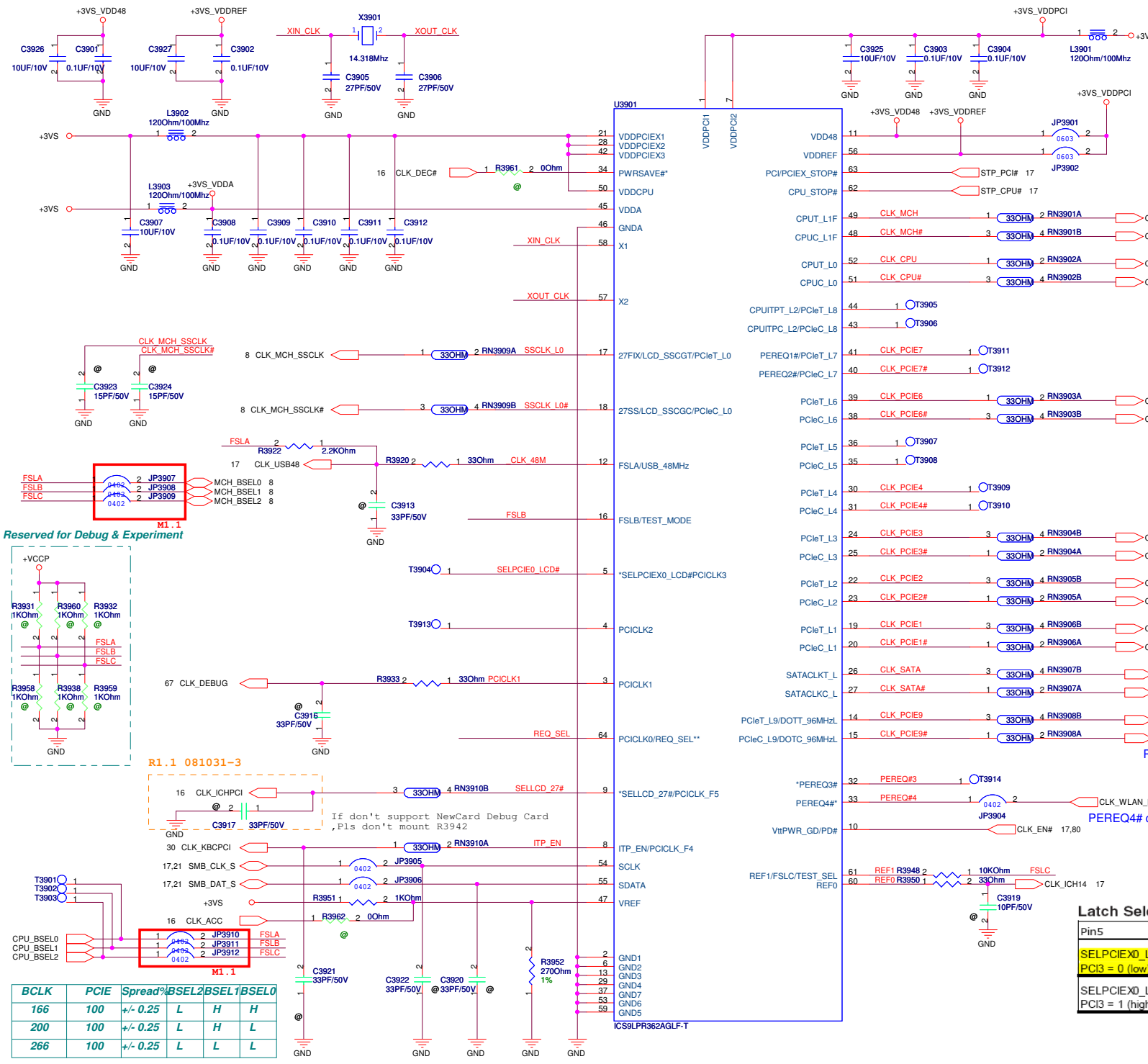


Thermal Sensor

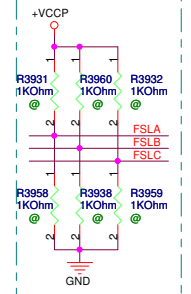


add 2nd source :06G023096010





Reserved for Debug & Experiment



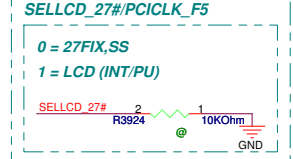
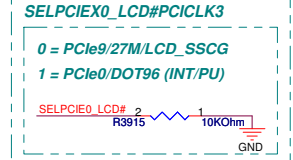
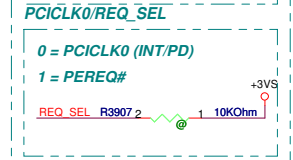
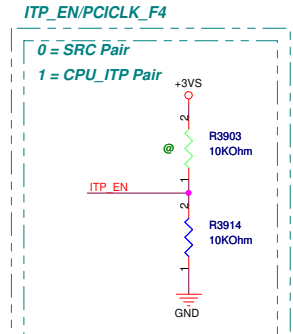
R1.1 081031-3

If don't support NewCard Debug Card, Pls don't mount R3942

M1.1

BCLK	PCIE	Spread%	BSEL2	BSEL1	BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L
266	100	+/- 0.25	L	L	L

Latched Input Select



PEREQ3# control PCIE 2,4

PEREQ4# control PCIE 3,5,7

Latch Select Table

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD#/ PCIE3 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	27FIX/SS LCD
SELPCIE0_LCD#/ PCIE3 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE9 DOT96	PCIE9 PCIE0

<Variant Name>

Title :CLOCK GEN-ICS9LPR363

ASUSTeK COMPUTER INC. NB1

Engineer: Alex & Bruce

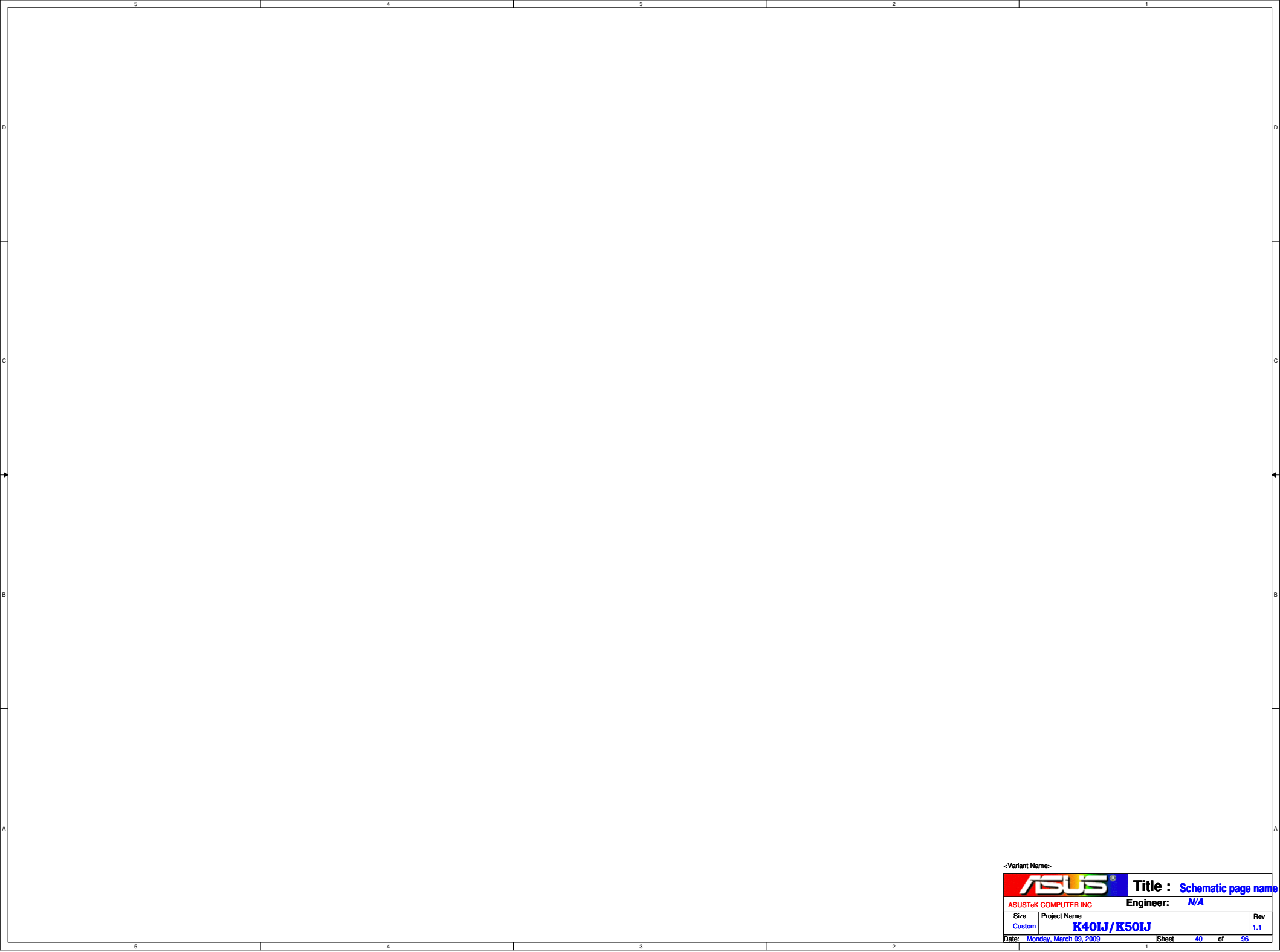
Size Custom

Project Name K40LJ/K50LJ

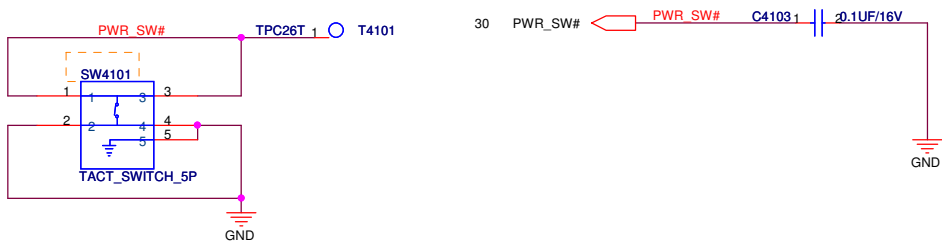
Date: Monday, March 09, 2009

Rev 1.1

Sheet 39 of 96

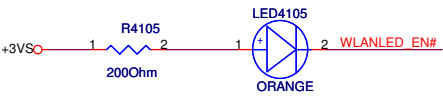


SWITCH BUTTON

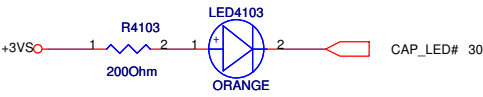


LED

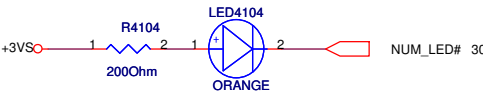
For WireLess LED



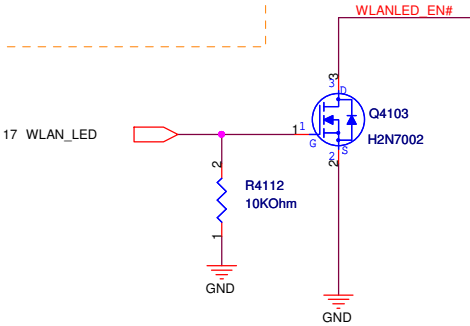
for Cap. Lock



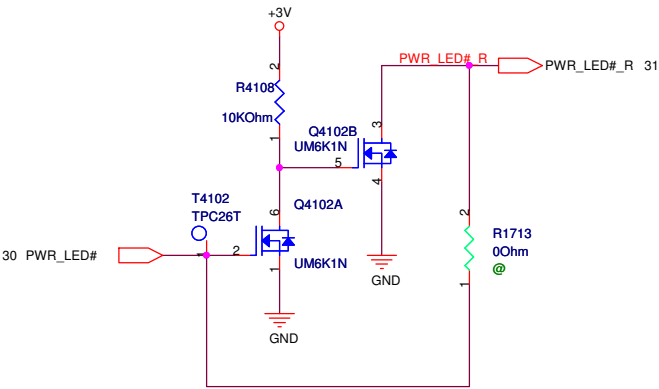
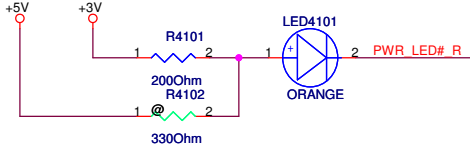
for Num Lock



R1.1 081031-4

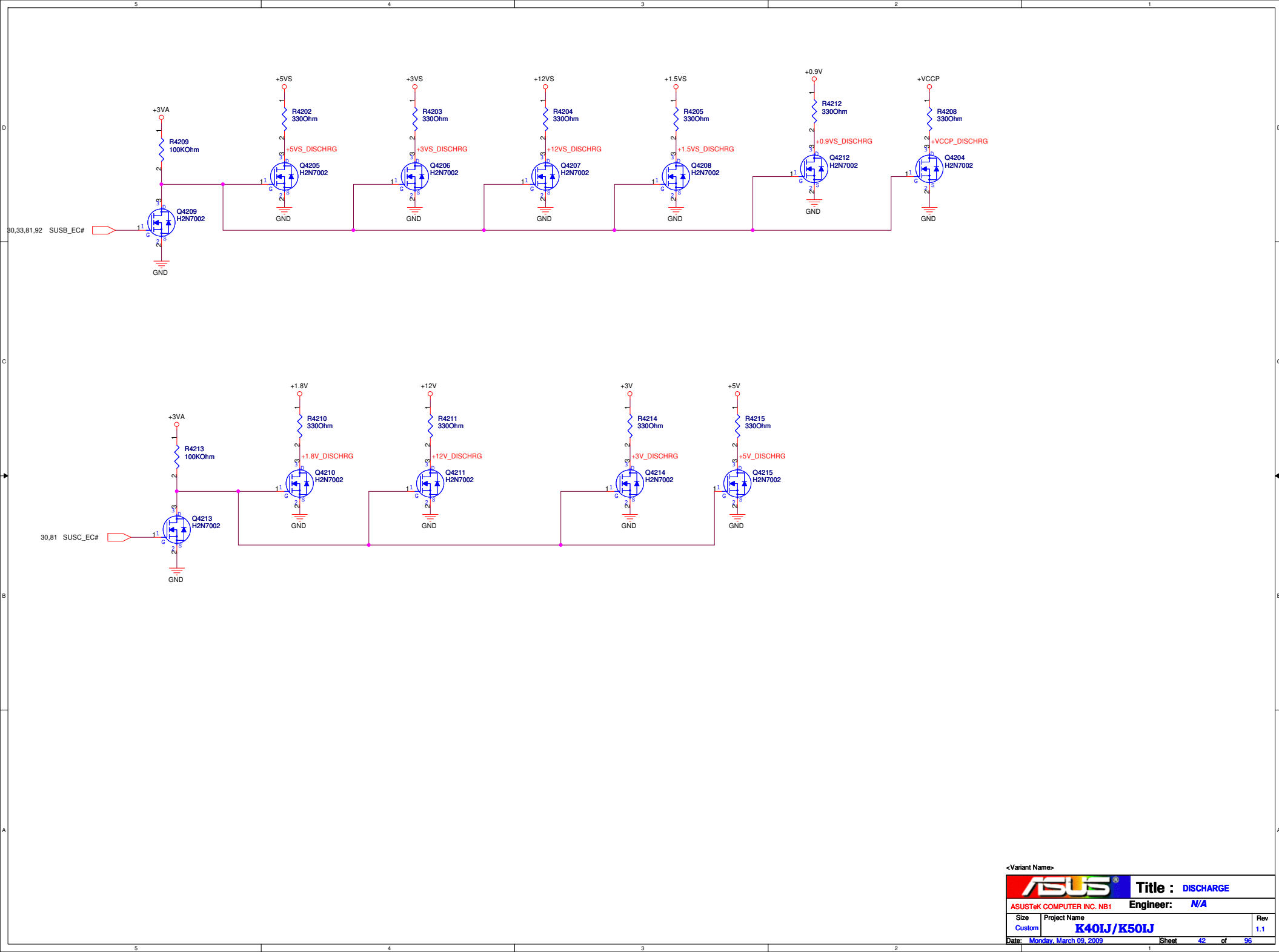


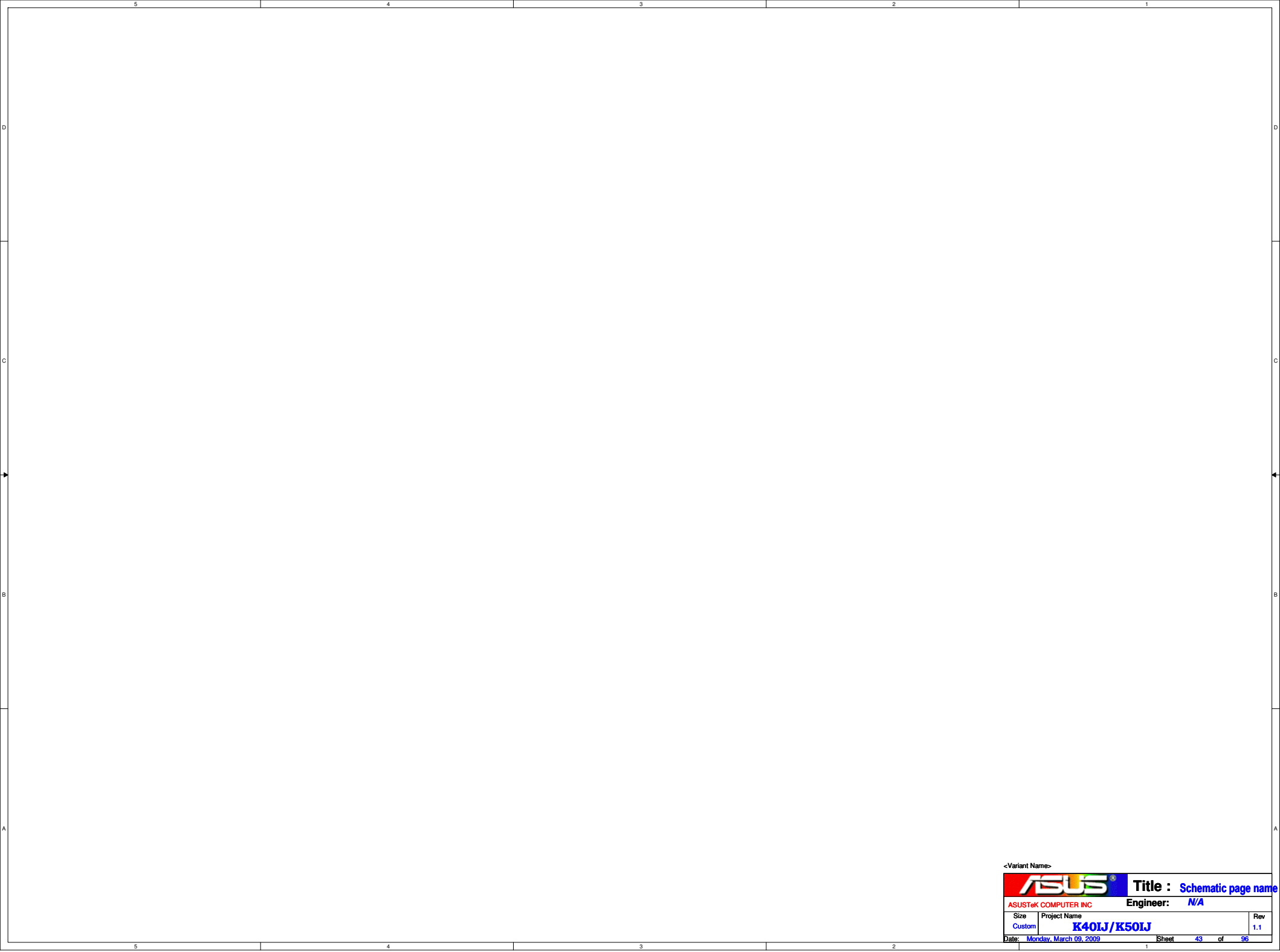
For POWER LED

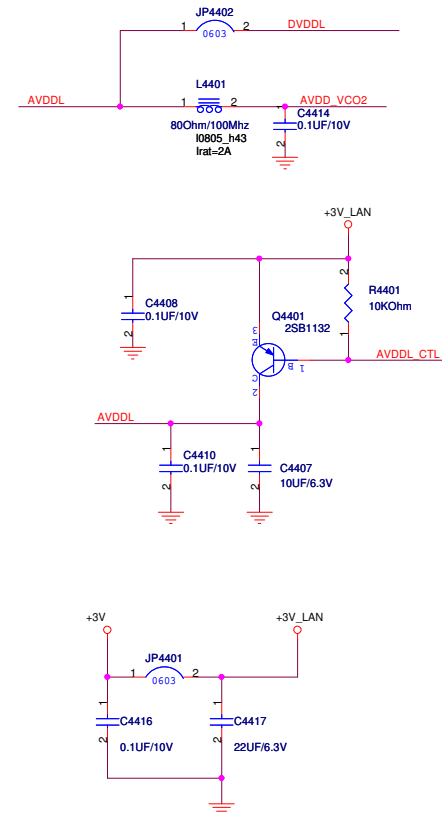
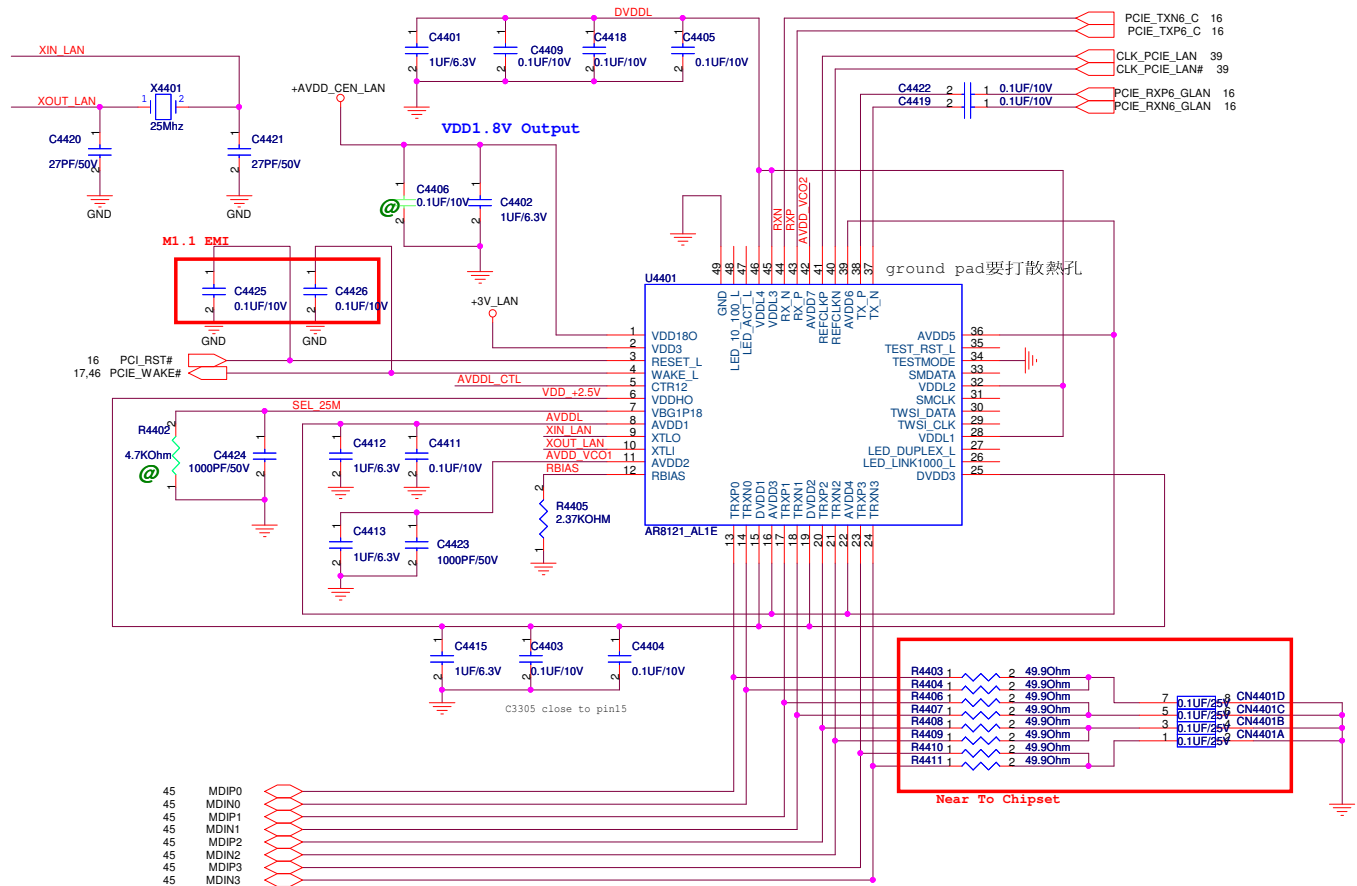


<Variant Name>

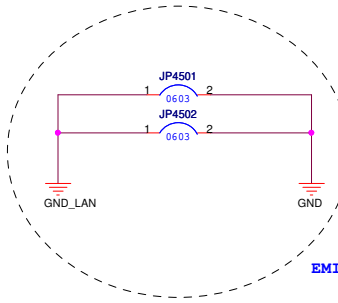
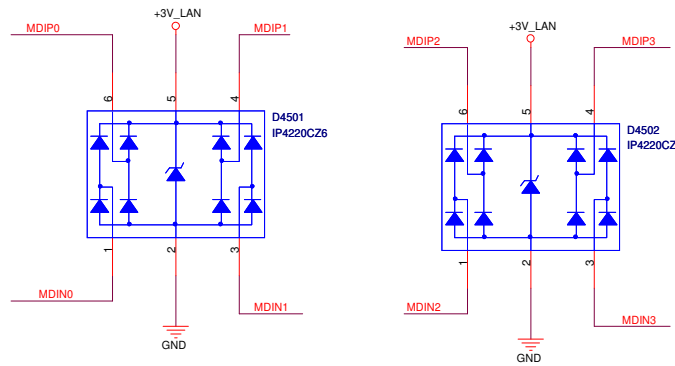
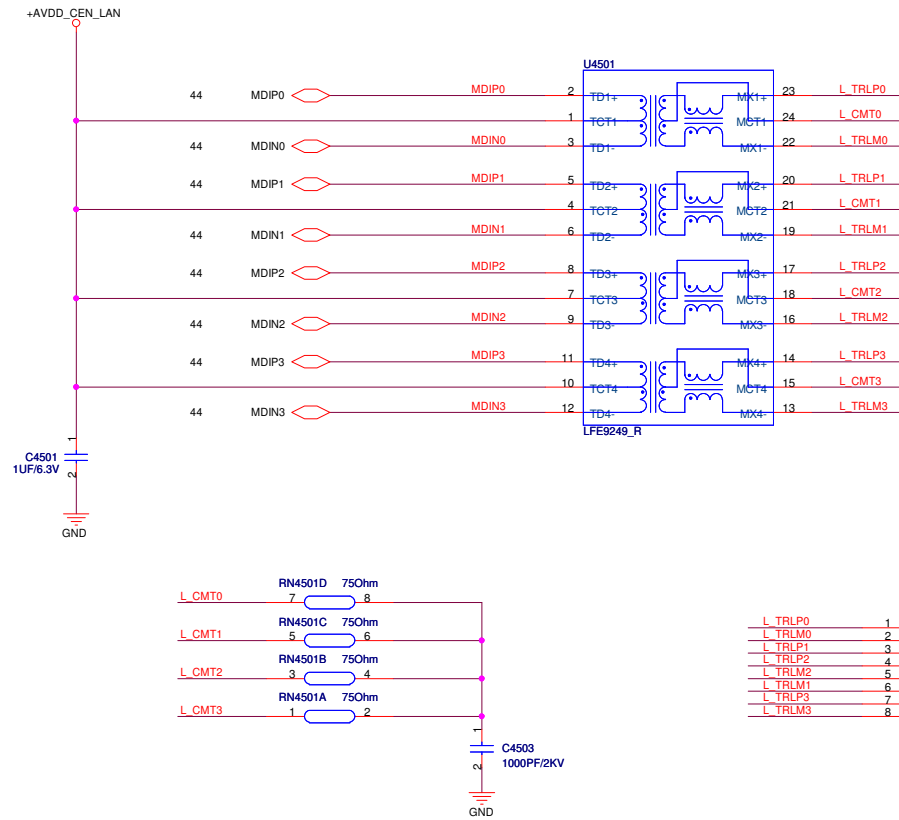
		Title : Switch Button & LED	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size B	Project Name K40IJ/K50IJ		Rev 1.1
Date: Monday, March 09, 2009		Sheet 41	of 96

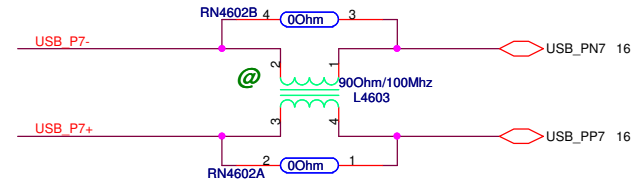
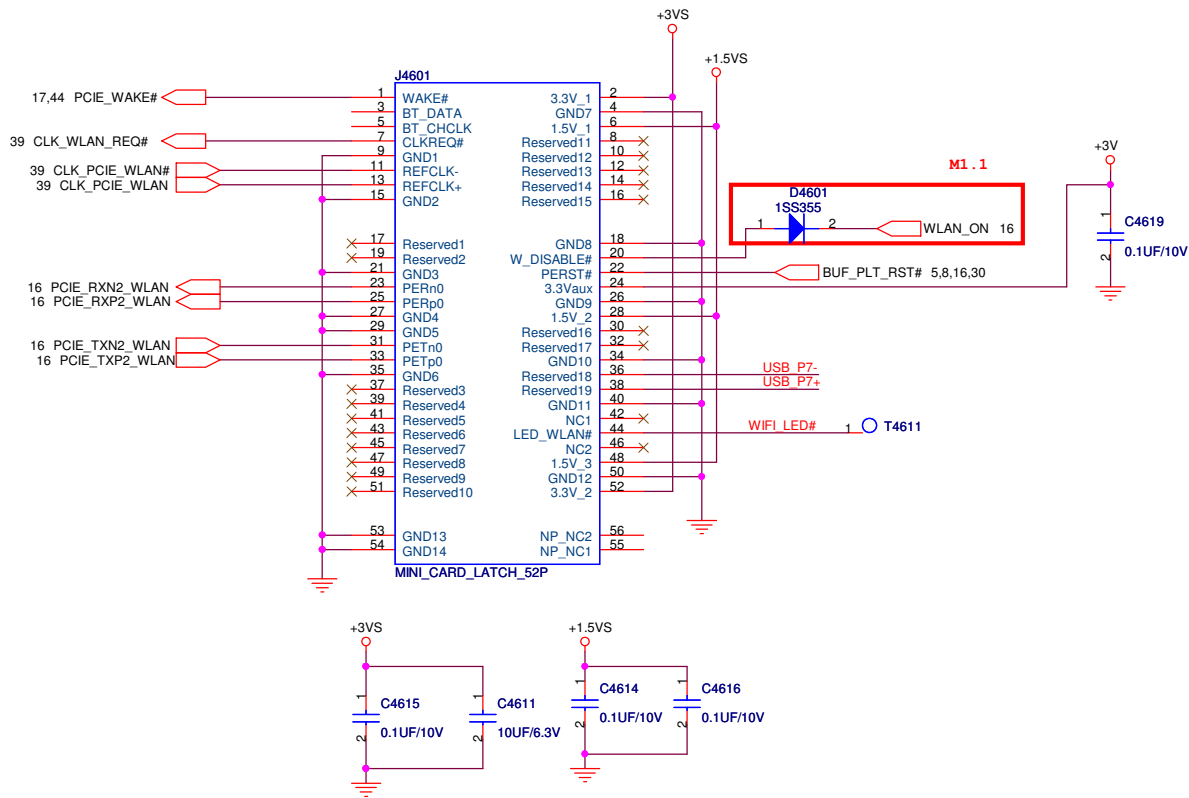






LAN CONN.

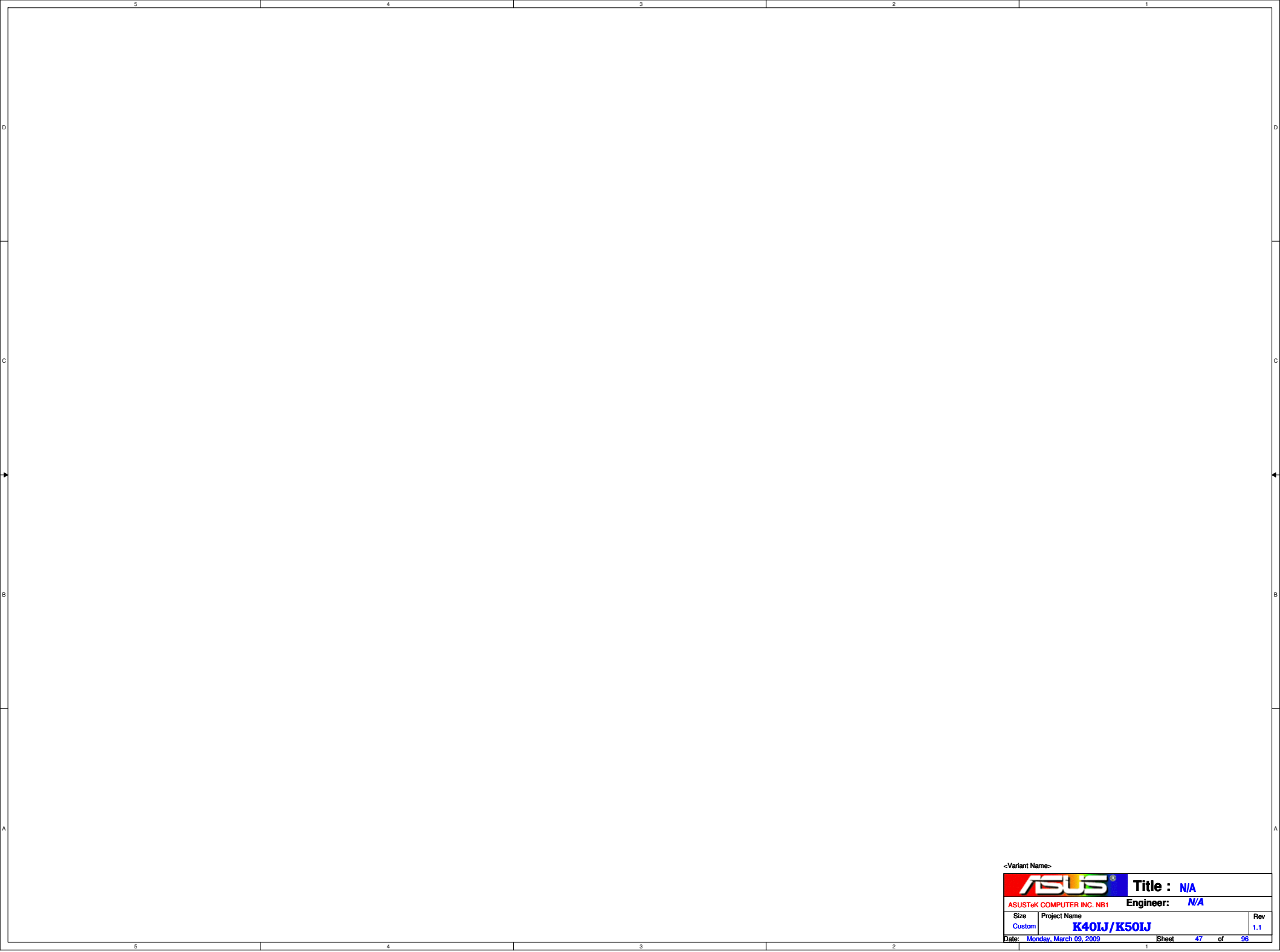


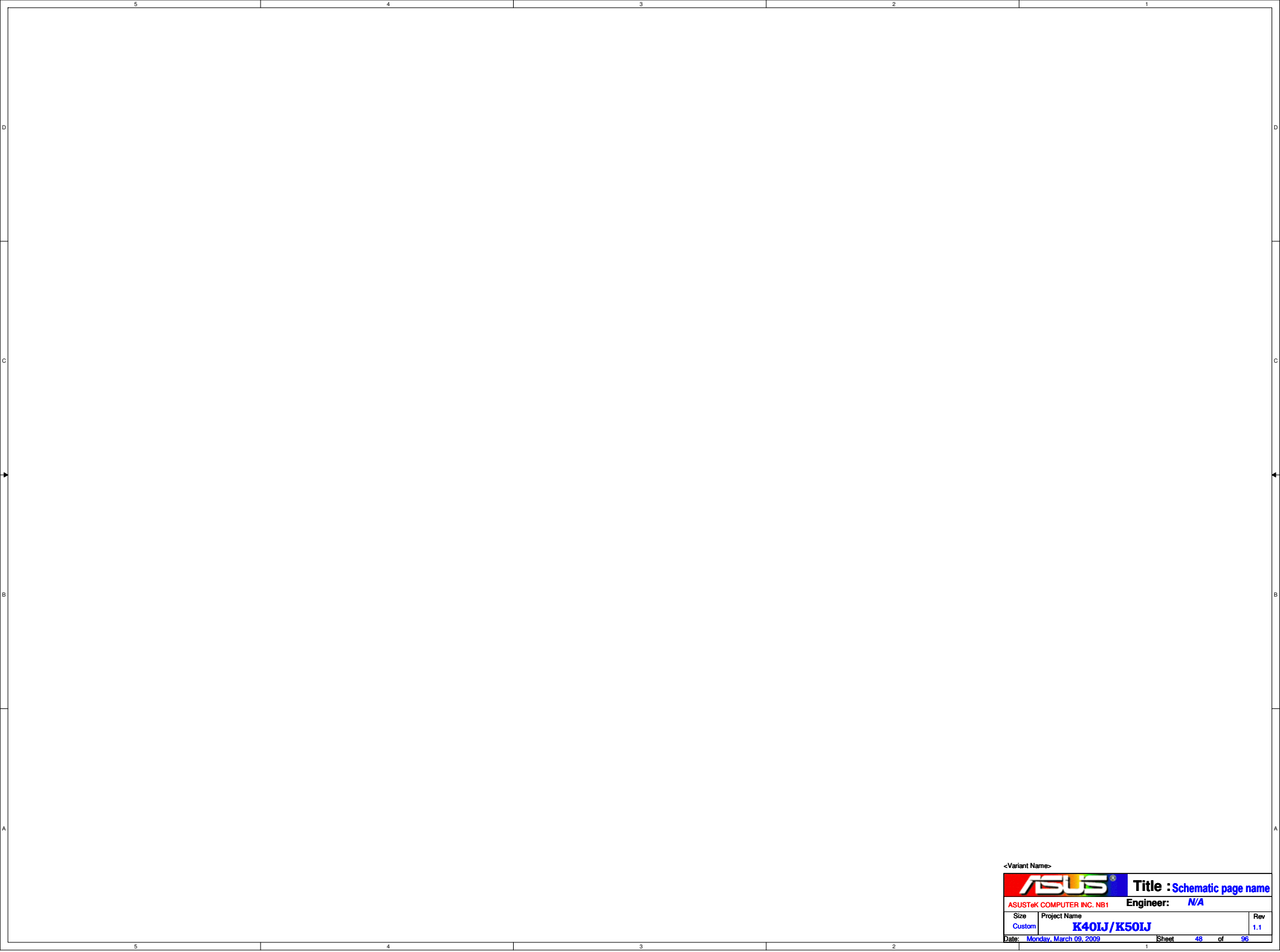


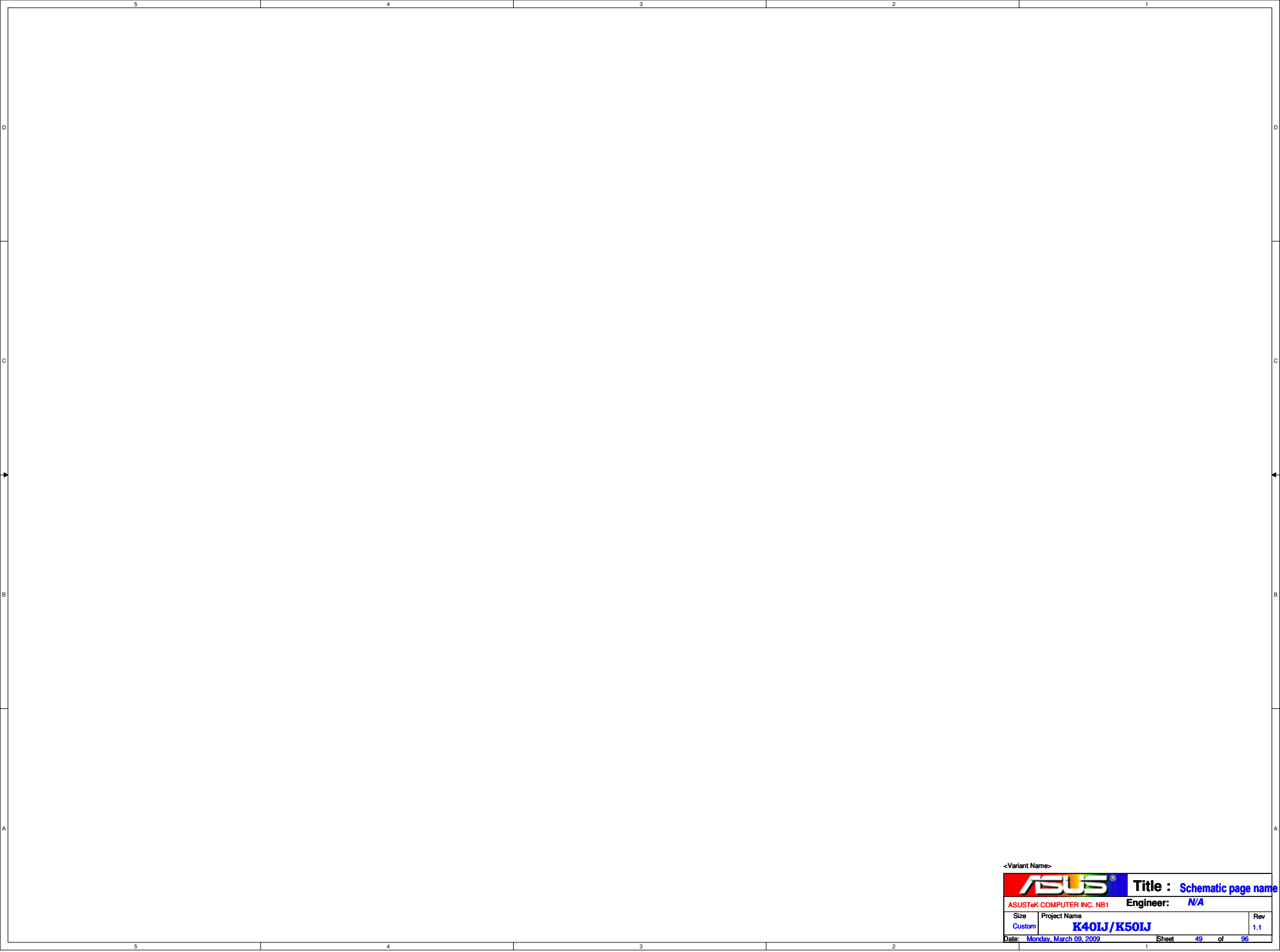
WLAN H=7.5mm

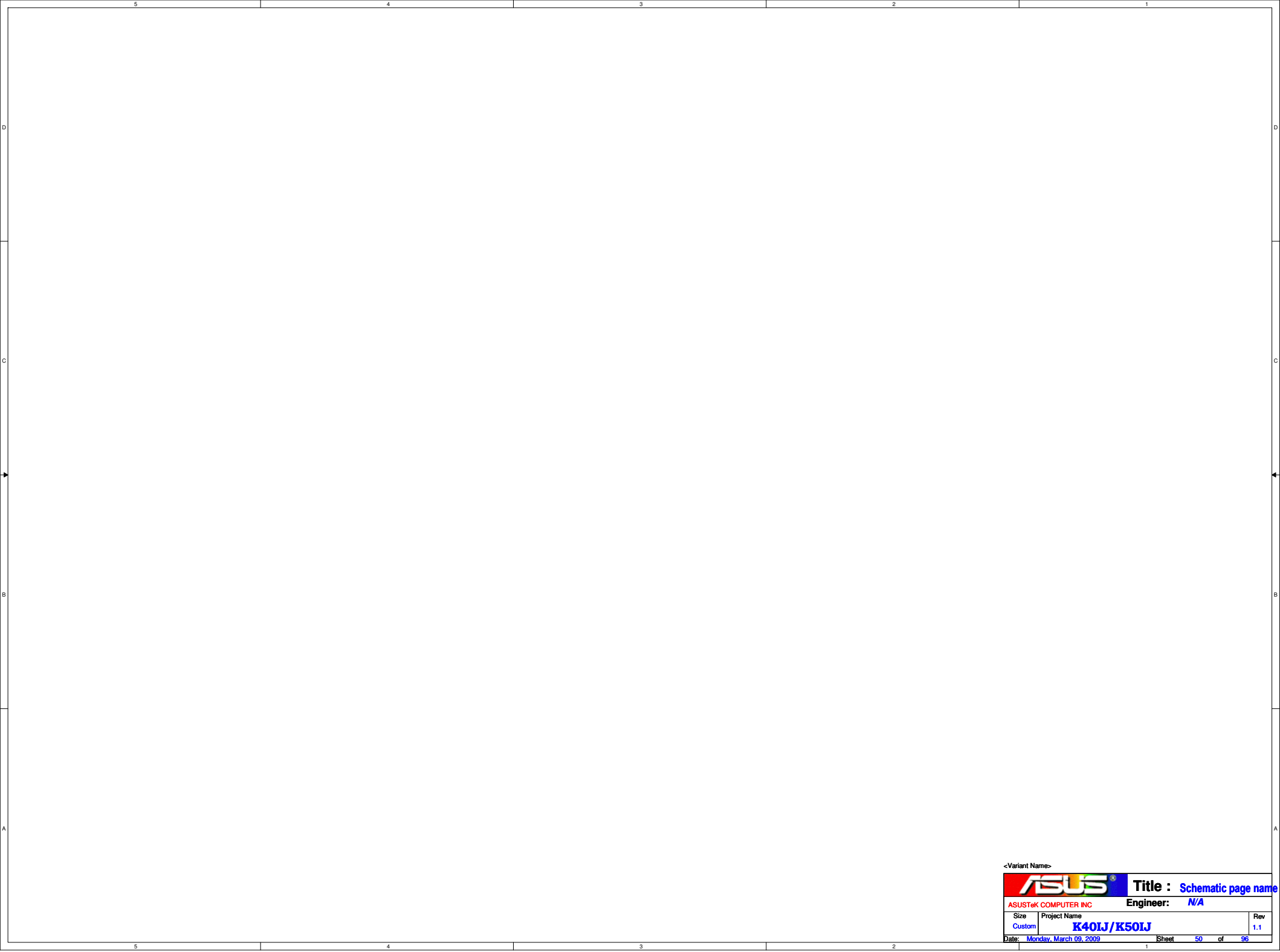
<Variant Name>

ASUS		Title :Mini card_WLAN+3G	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size Custom	Project Name K40IJ/K50IJ		Rev 1.1
Date: Monday, March 09, 2009		Sheet 46 of 96	









<Variant Name>



Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

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D

D

C

C

B

B

A

A

<Variant Name>



Title : N/A

ASUSTeK COMPUTER INC. NB1

Engineer: **N/A**

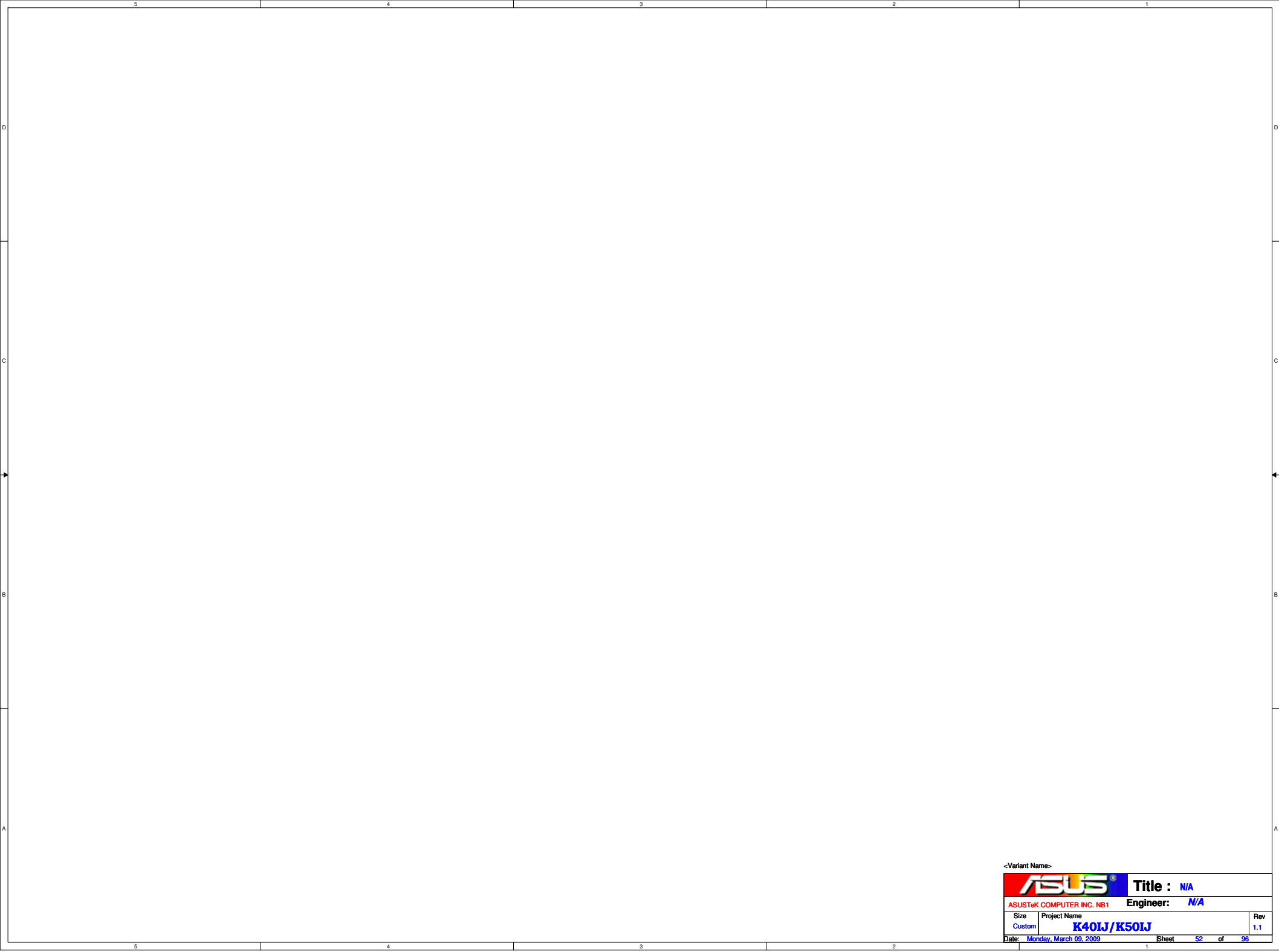
Size
Custom

Project Name	K40IJ/K50IJ
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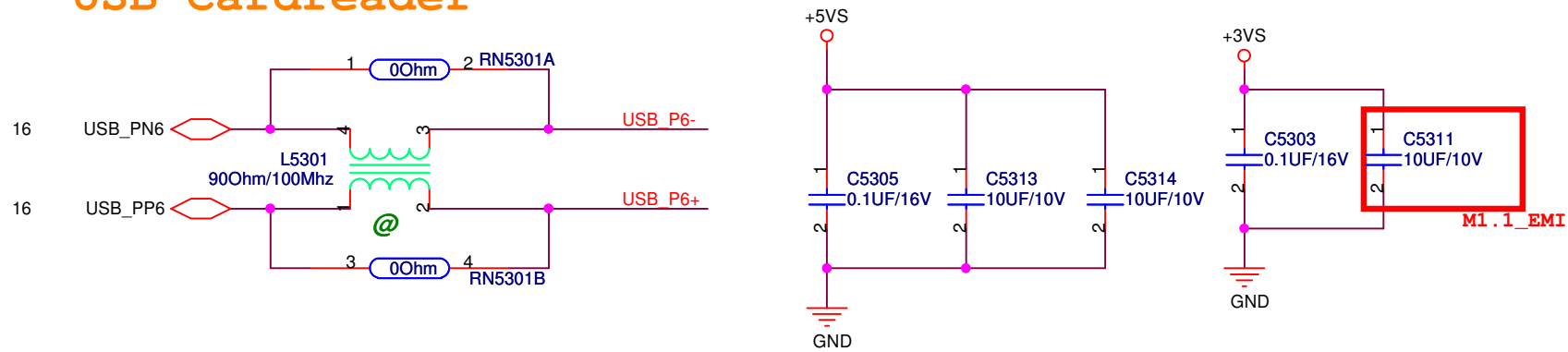
Rev	
1.1	

Date: Monday, March 09, 2009

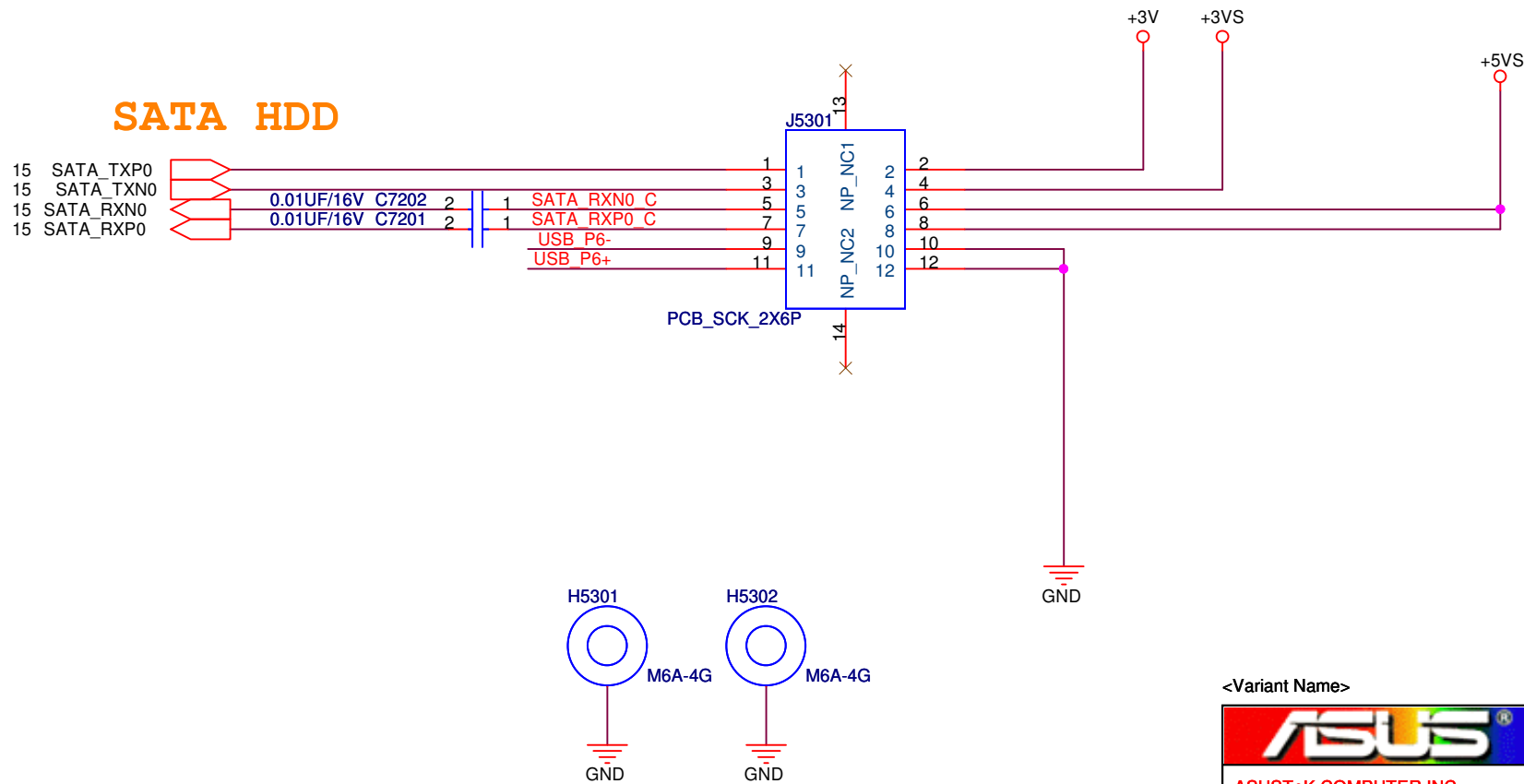
Sheet 51 of 96



USB Cardreader

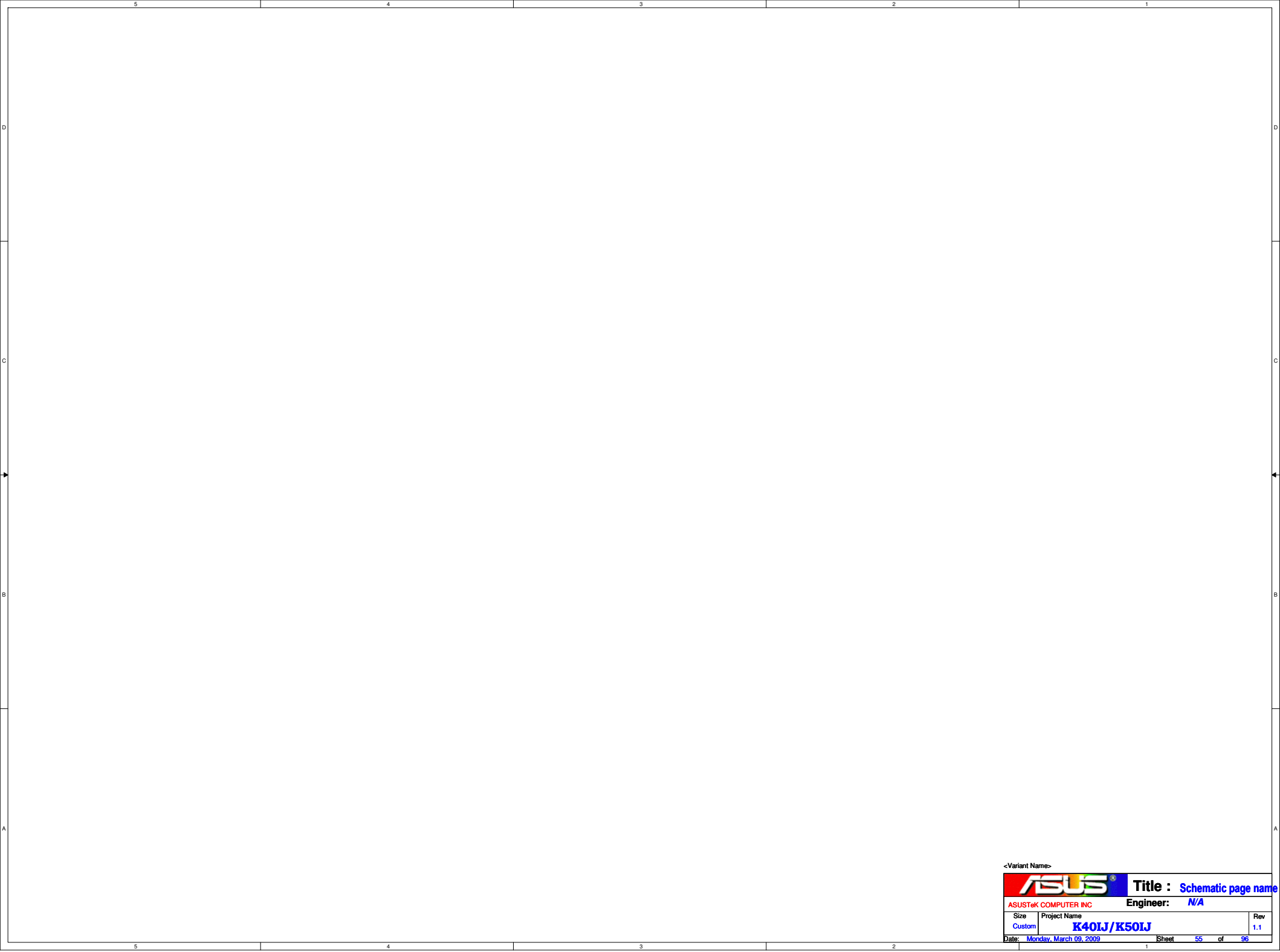


SATA HDD



<Variant Name>

ASUS		Title :SATA_HDD & Cardreader	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size Custom	Project Name K40IJ/K50IJ		Rev 1.1
Date: Monday, March 09, 2009		Sheet 53 of 96	



<Variant Name>



Title : Schematic page name

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009Sheet 55 of 96

HDMI WtoB Connector

HDCP ROM

<Variant Name>



Title : iHDMI

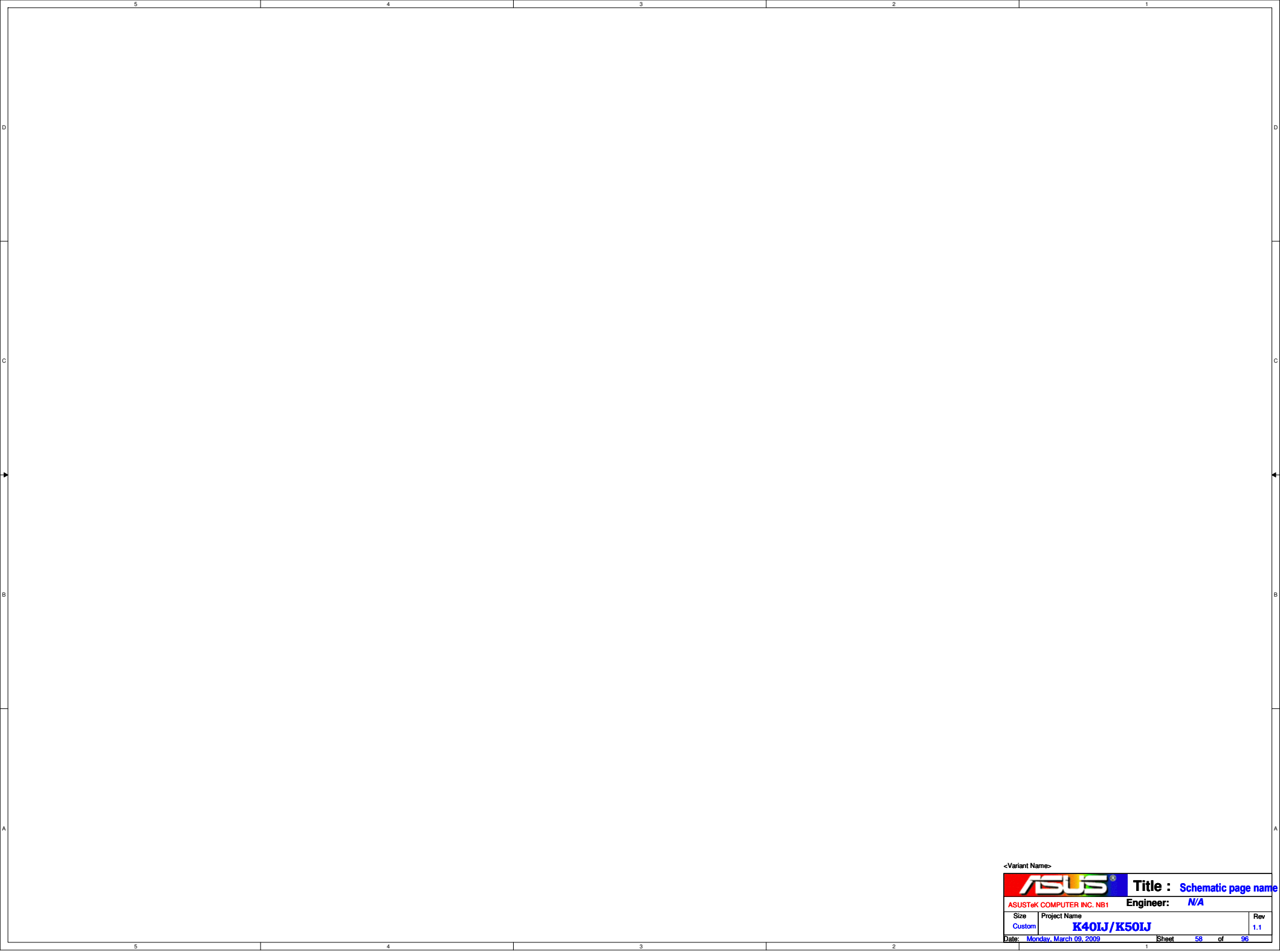
ASUSTeK COMPUTER INC. NB1Engineer: N/A

Size
B

Project Name

Rev
1.1

Date: Monday, March 09, 2009Sheet 57 of 96



<Variant Name>



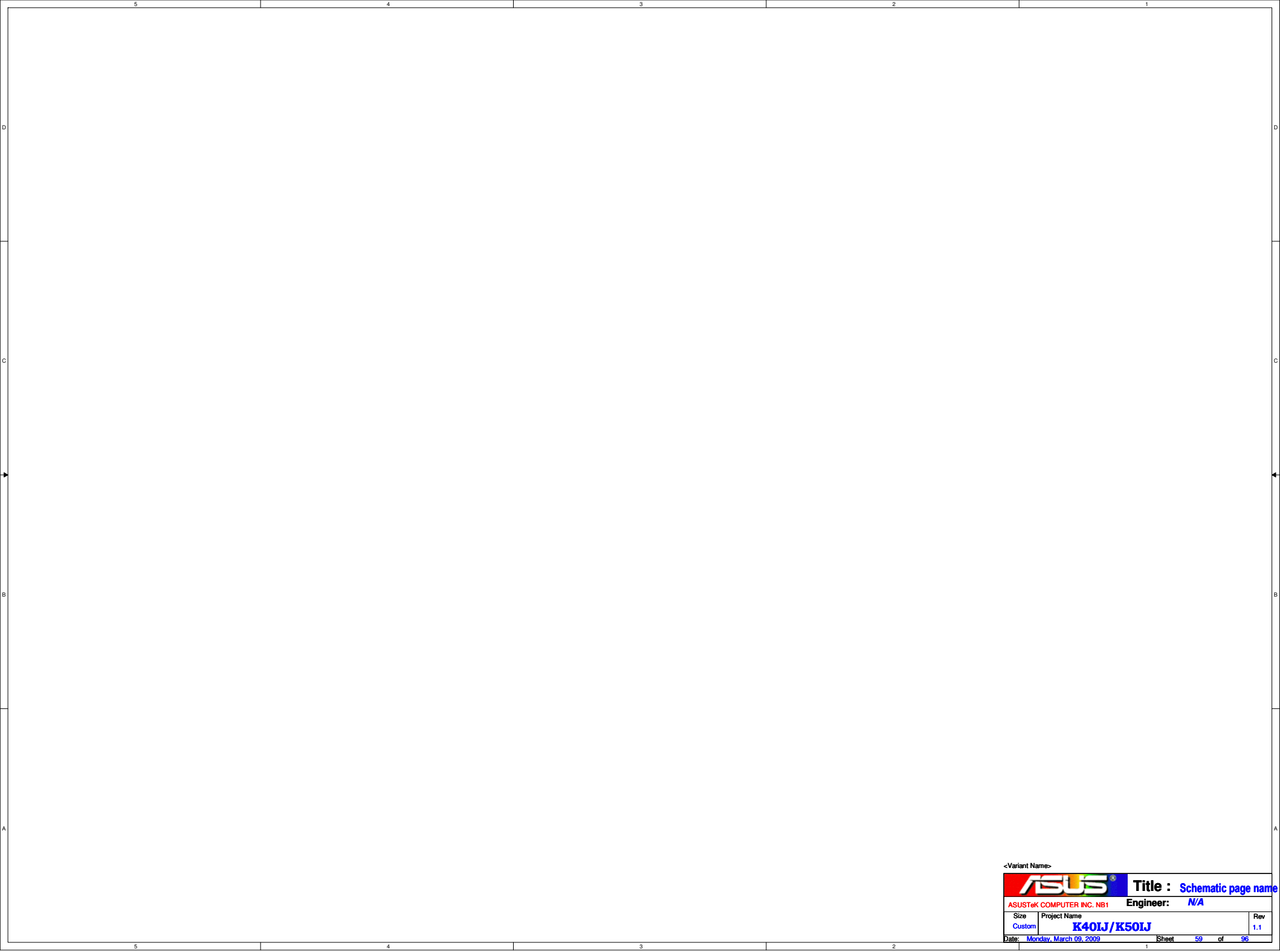
Title : Schematic page name

ASUSTeK COMPUTER INC. NB1

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009Sheet 58 of 96



<Variant Name>



Title : Schematic page name

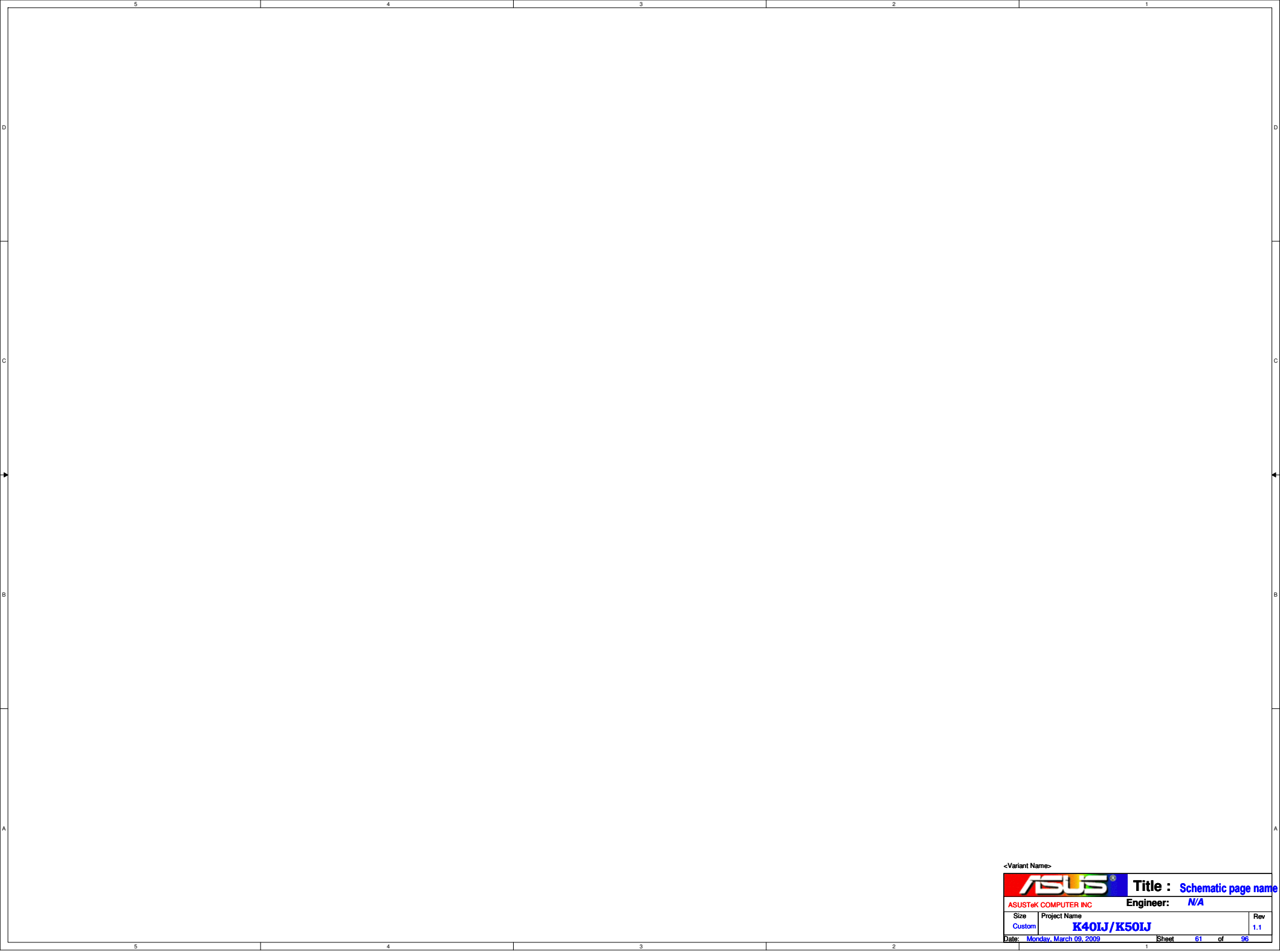
ASUSTeK COMPUTER INC. NB1

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

Date: Monday, March 09, 2009Sheet 59 of 96





<Variant Name>



Title : Schematic page name

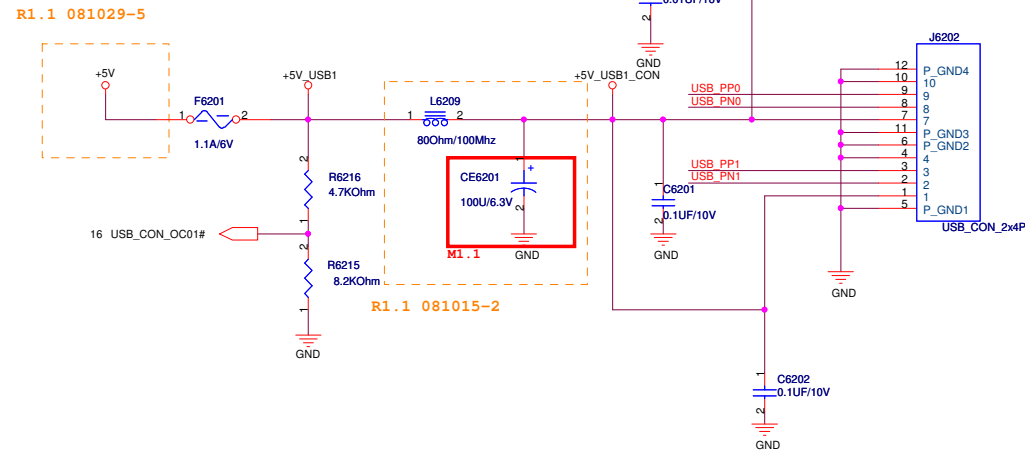
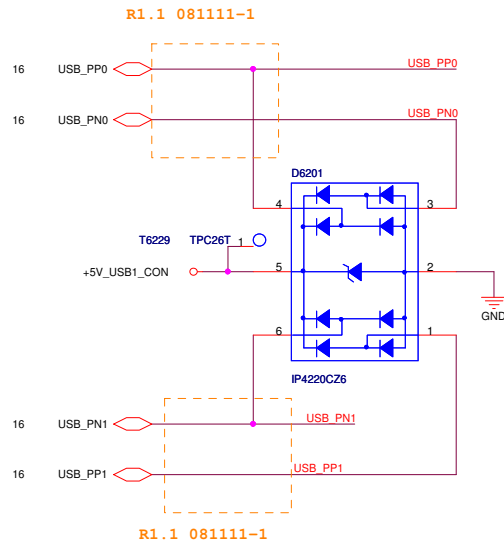
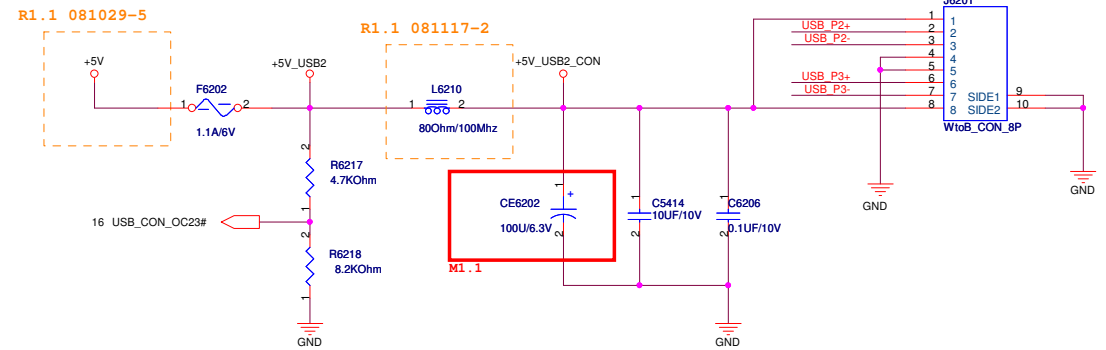
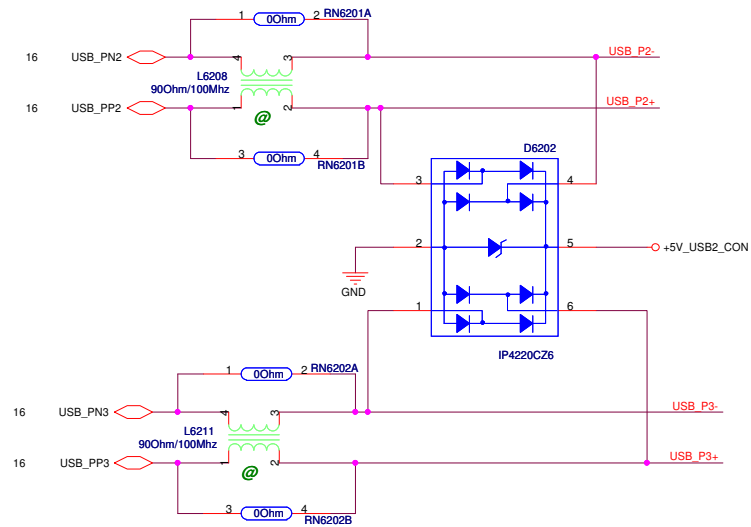
ASUSTeK COMPUTER INC

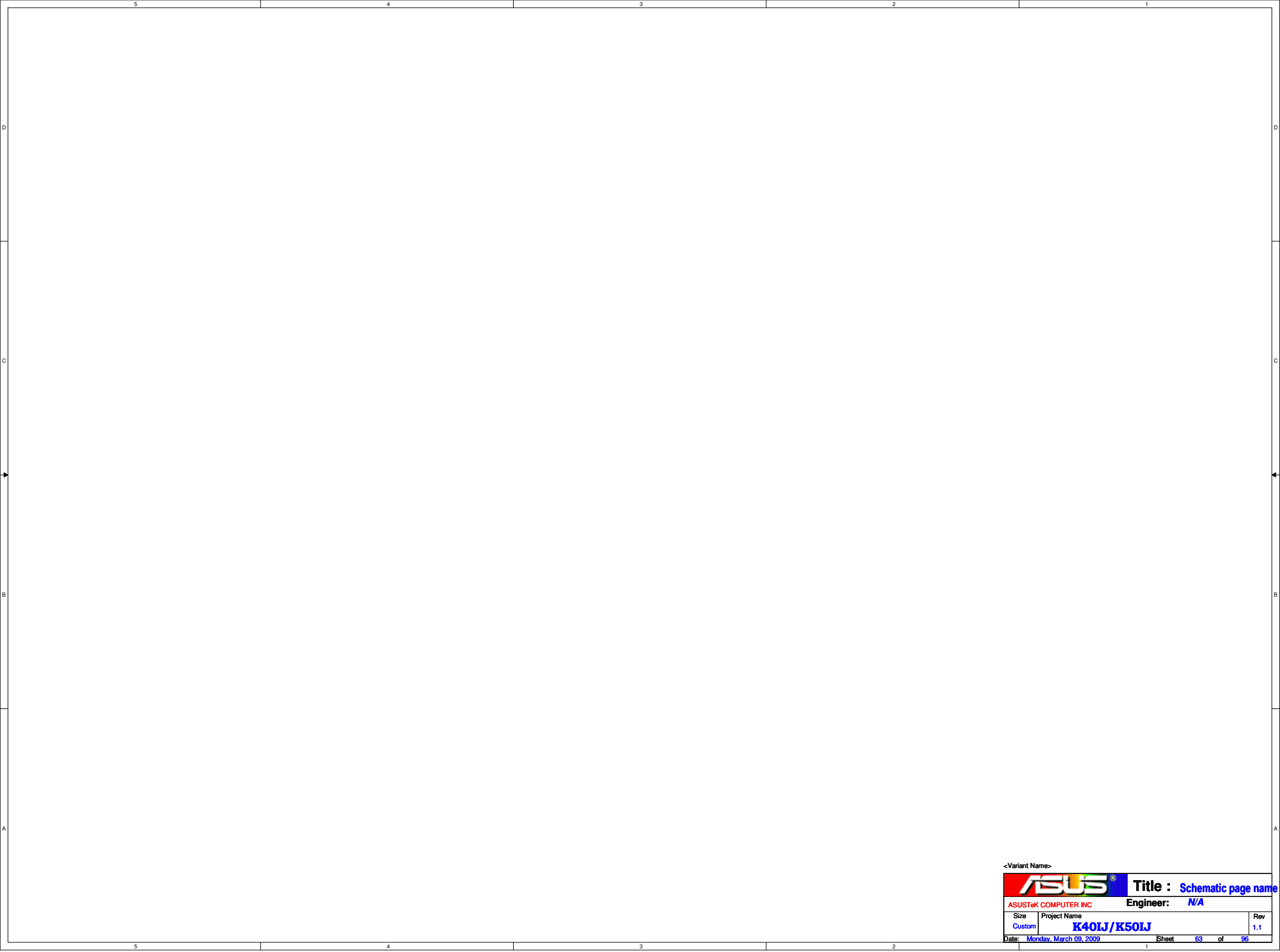
Engineer: N/A

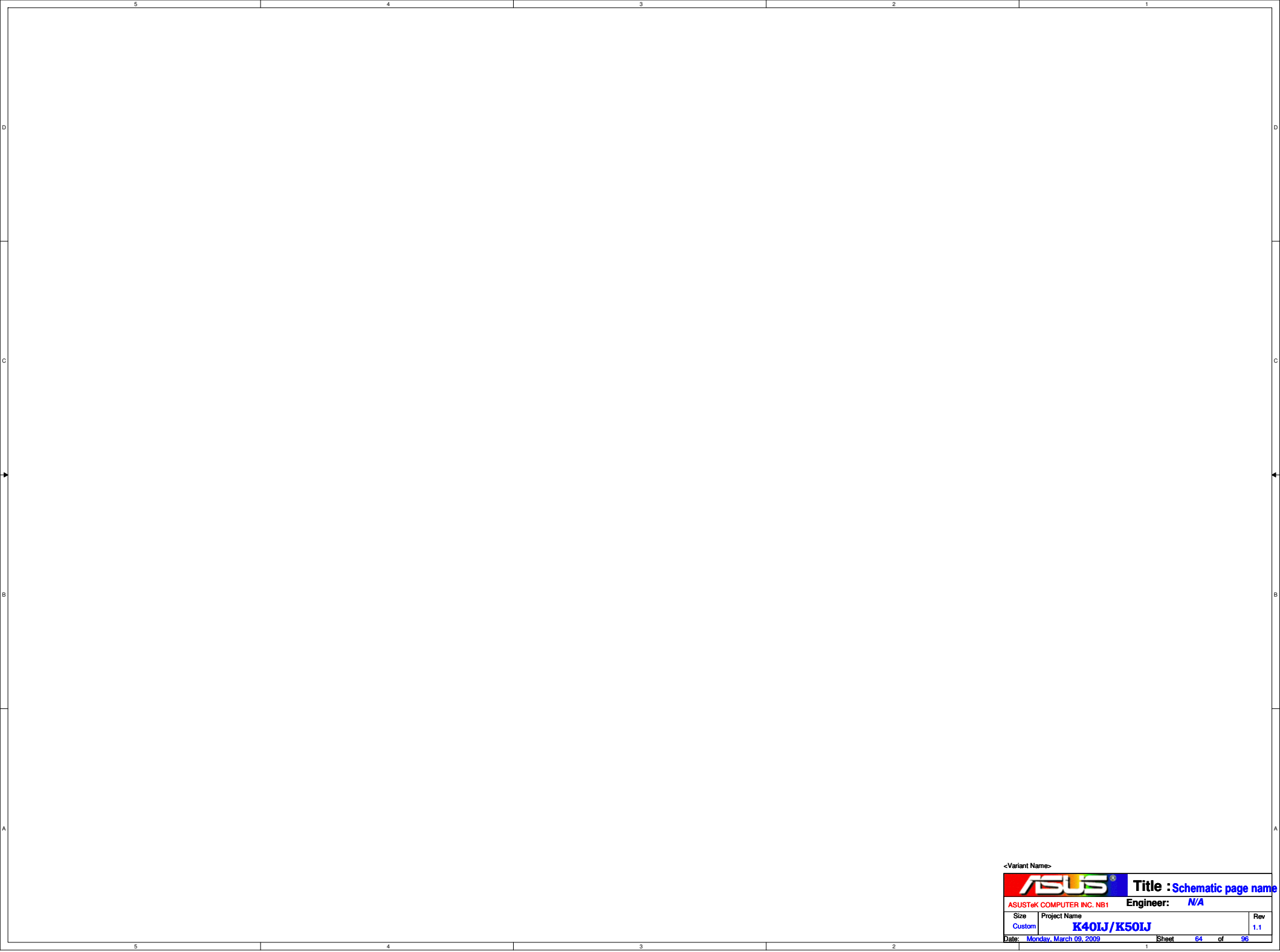
Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

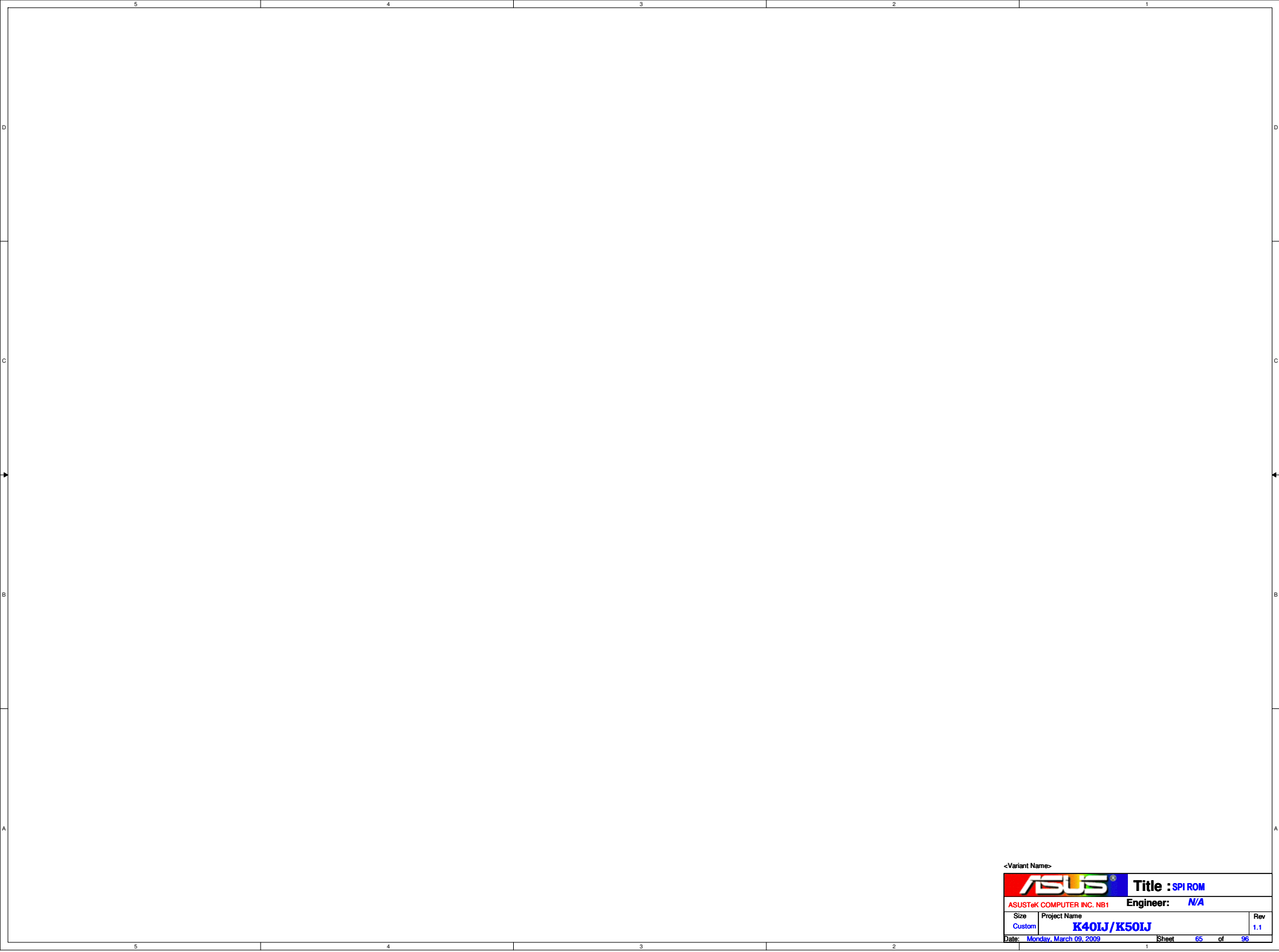
Date: Monday, March 09, 2009Sheet 61 of 96

USB IO Board









<Variant Name>

		Title : SPI ROM	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	65 of 96

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>



Title : LED

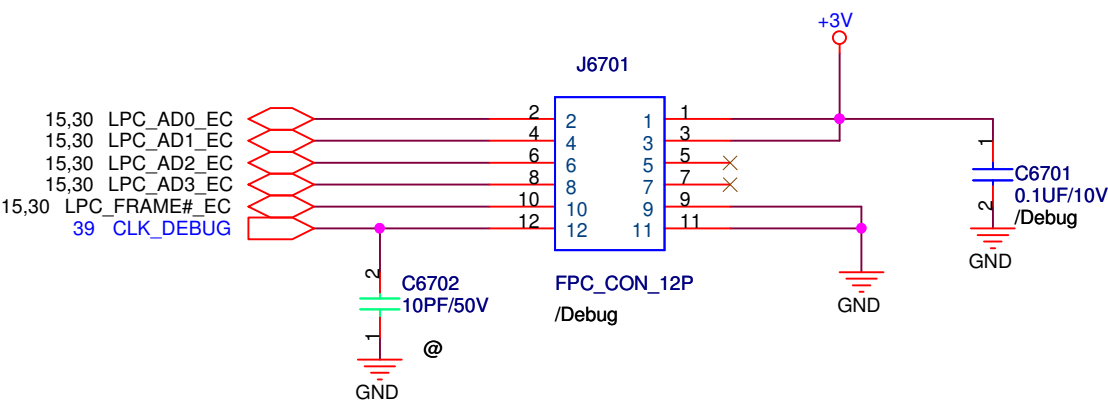
ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

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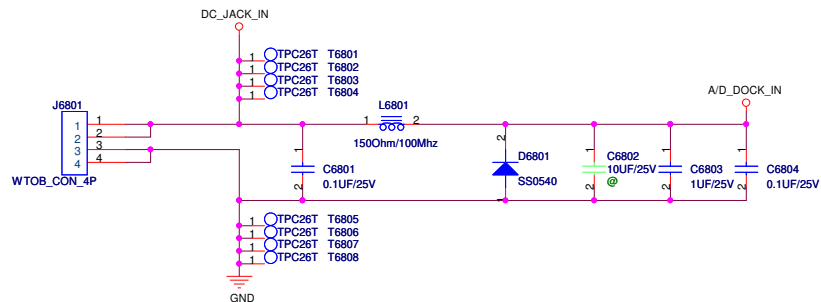
LPC DEBUG PORT



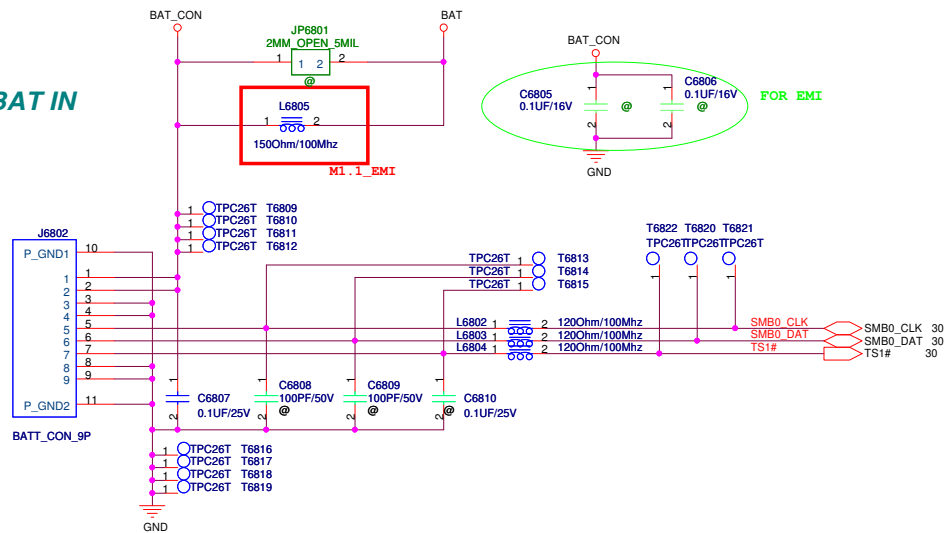
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		Title : DEBUG CONN	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size A	Project Name K40IJ/K50IJ		Rev 1.1
Date: Monday, March 09, 2009		Sheet 67 of 96	

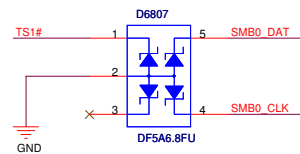
DC IN



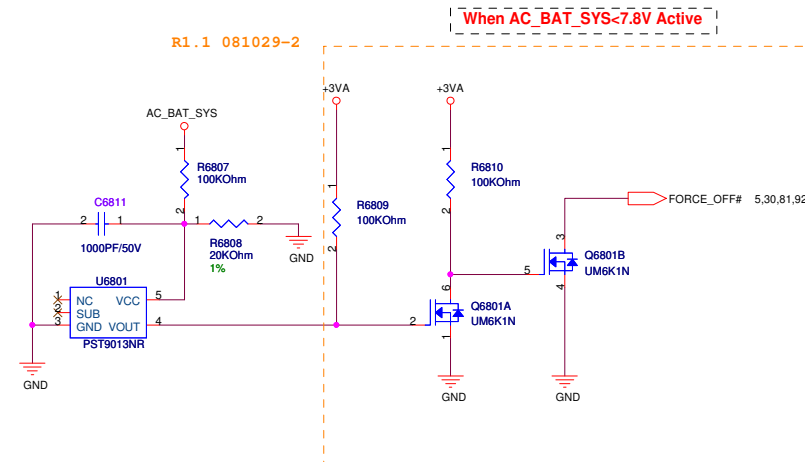
BAT IN



Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

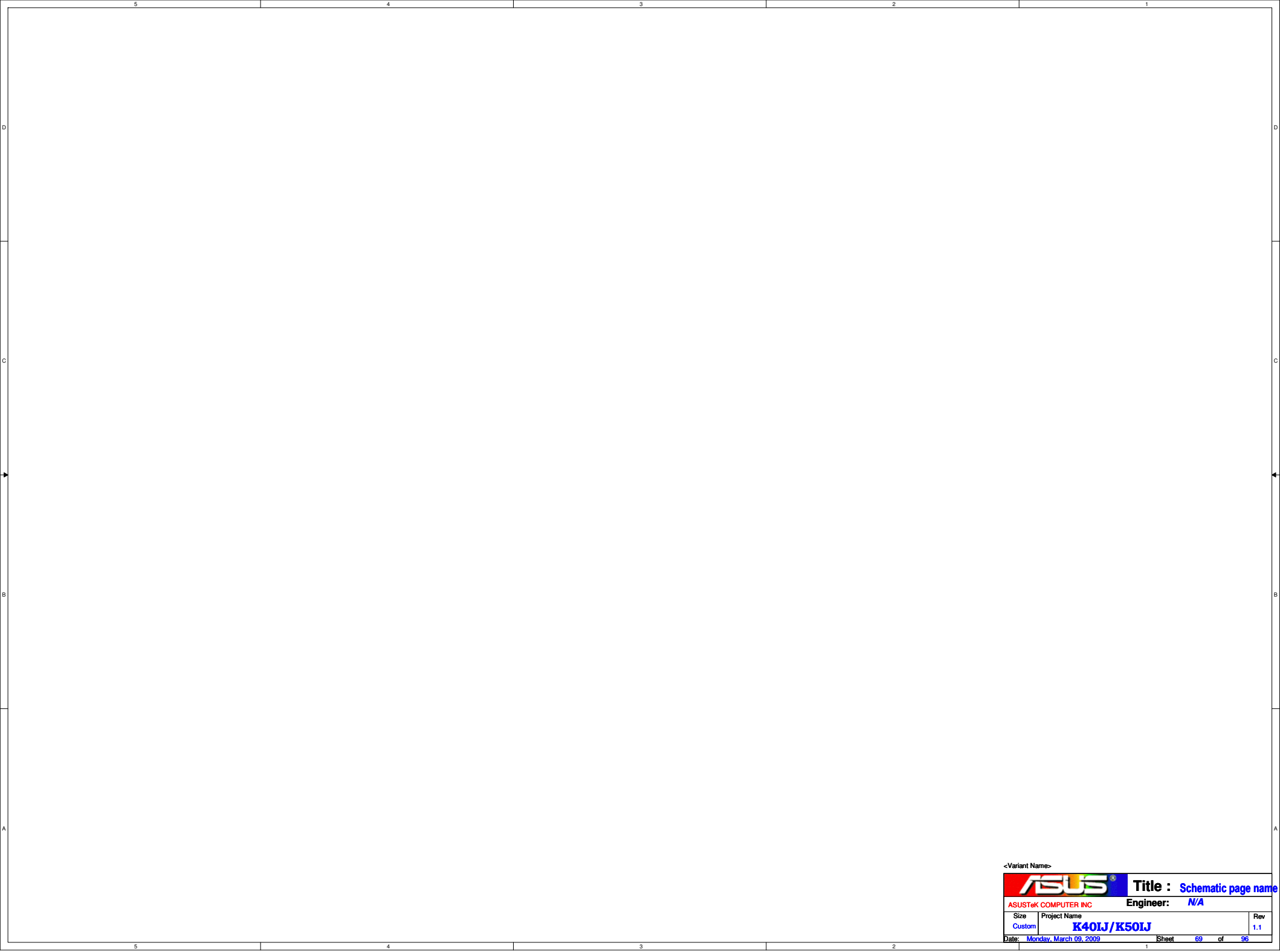


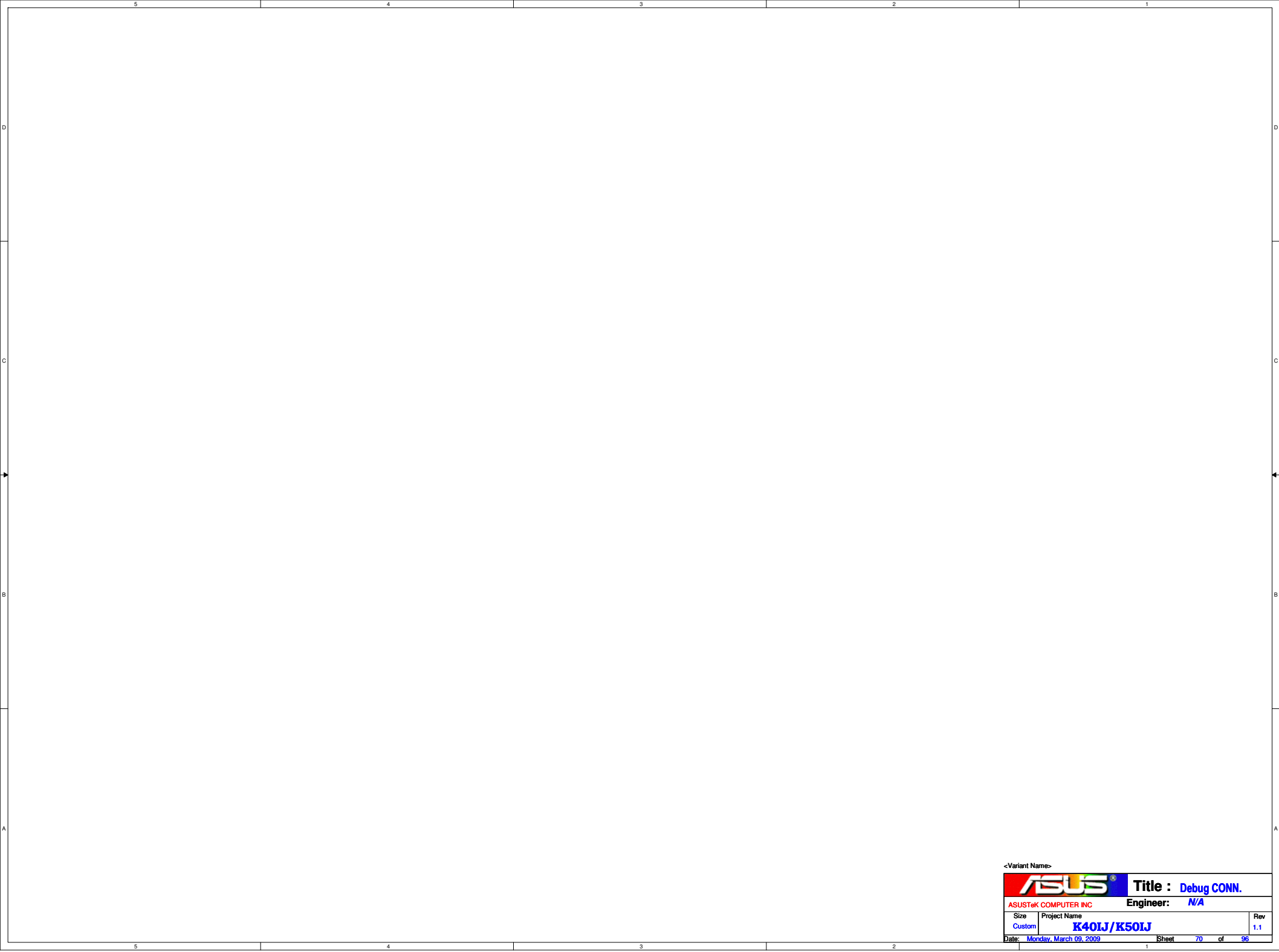
Without Battery & Pull out Adapter



<Variant Name>

ASUS		Title : DC & BAT IN	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name	Rev	
Custom	K40IJ/K50IJ	1.1	
Date: Monday, March 09, 2009		Sheet	68 of 96





<Variant Name>



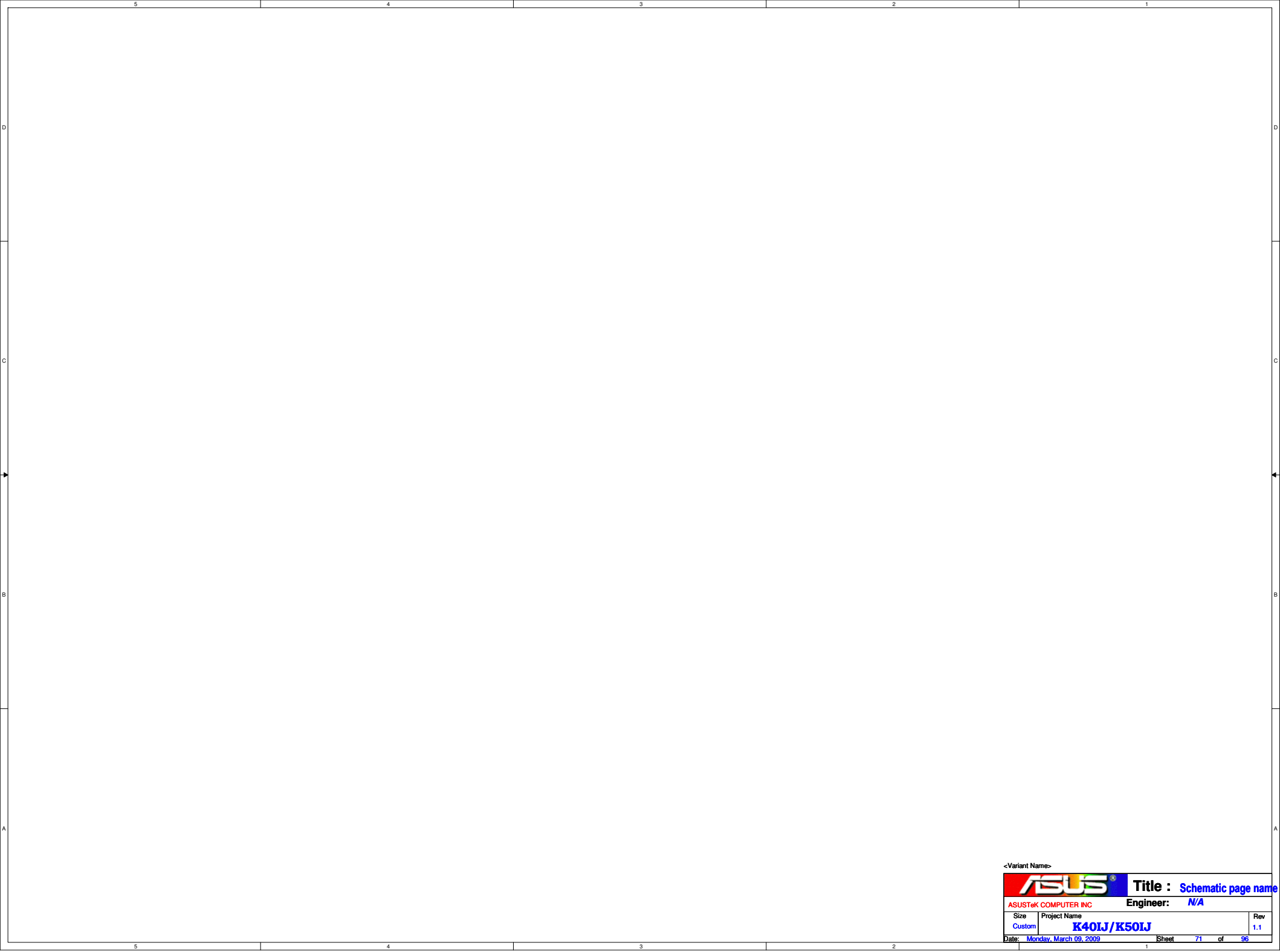
Title : Debug CONN.

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

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<Variant Name>



Title : Schematic page name

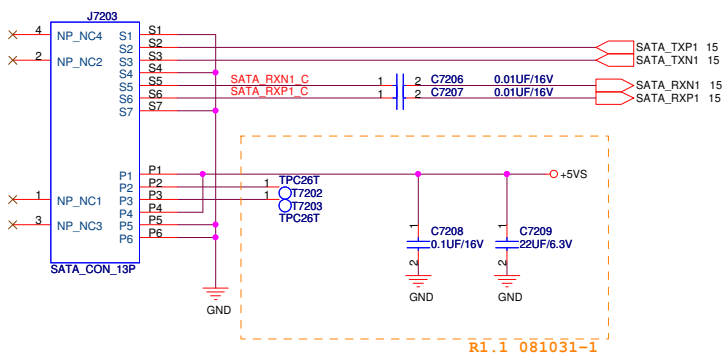
ASUSTeK COMPUTER INC

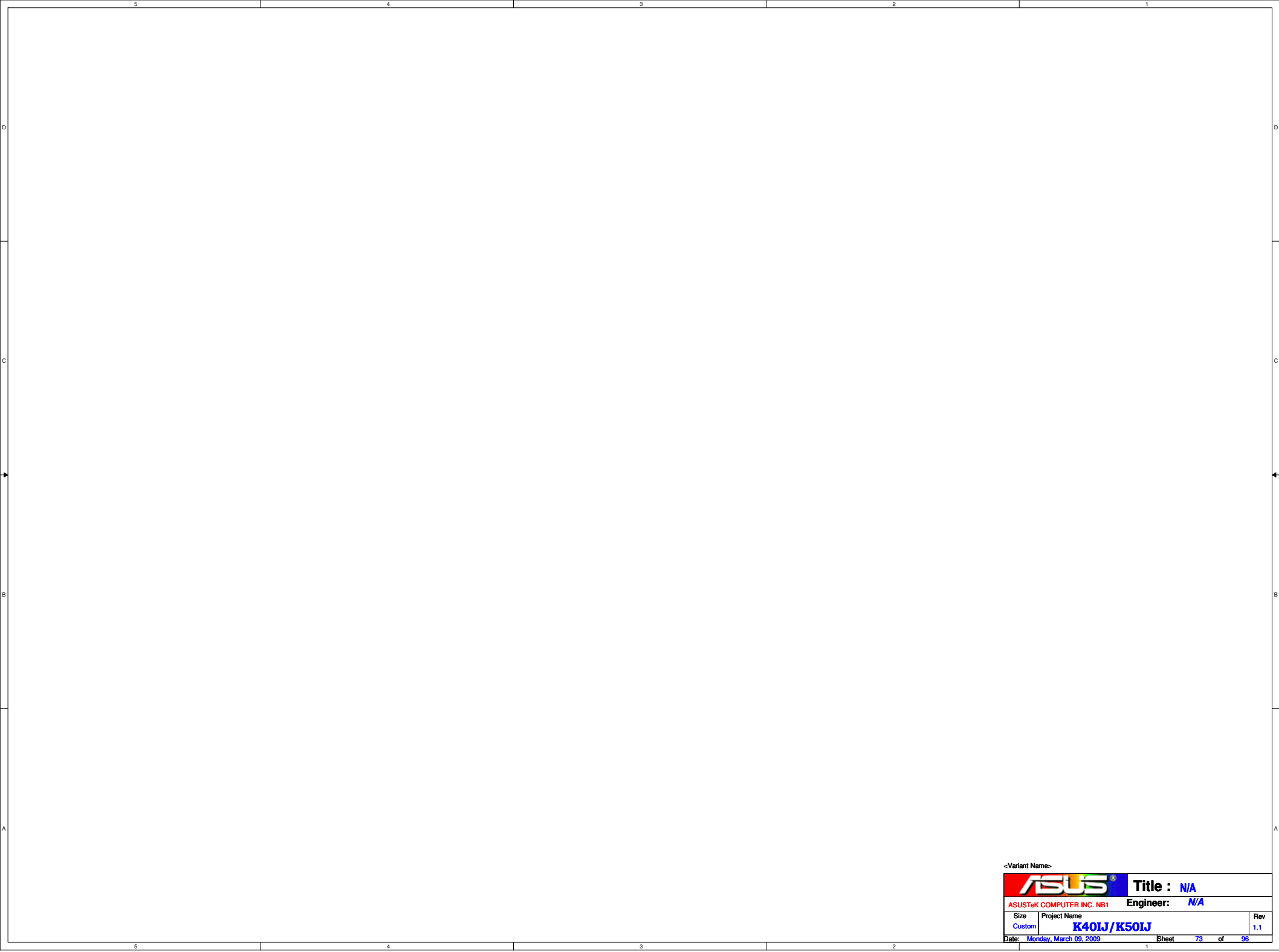
Engineer: N/A

Size	Project Name	Rev
Custom	K40IJ/K50IJ	1.1

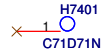
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ODD

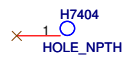
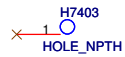
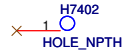




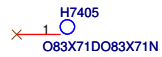
Hole-A



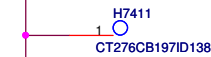
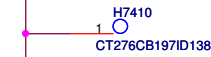
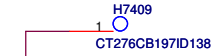
Hole-B



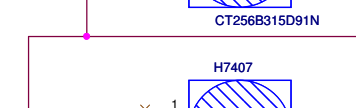
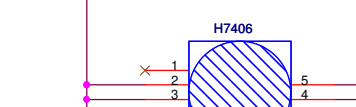
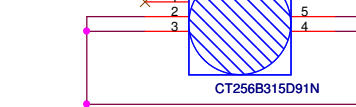
Hole-C



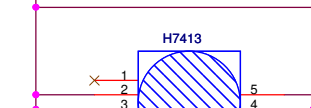
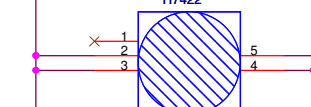
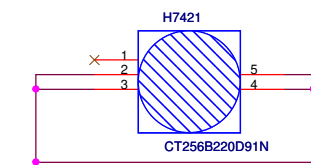
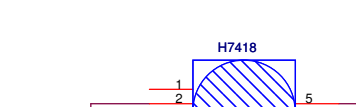
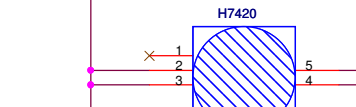
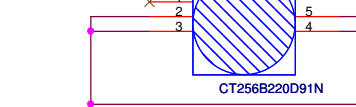
Hole-D



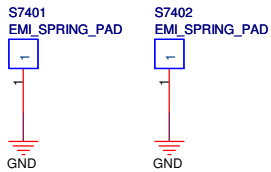
Hole-E



Hole-F



Spring



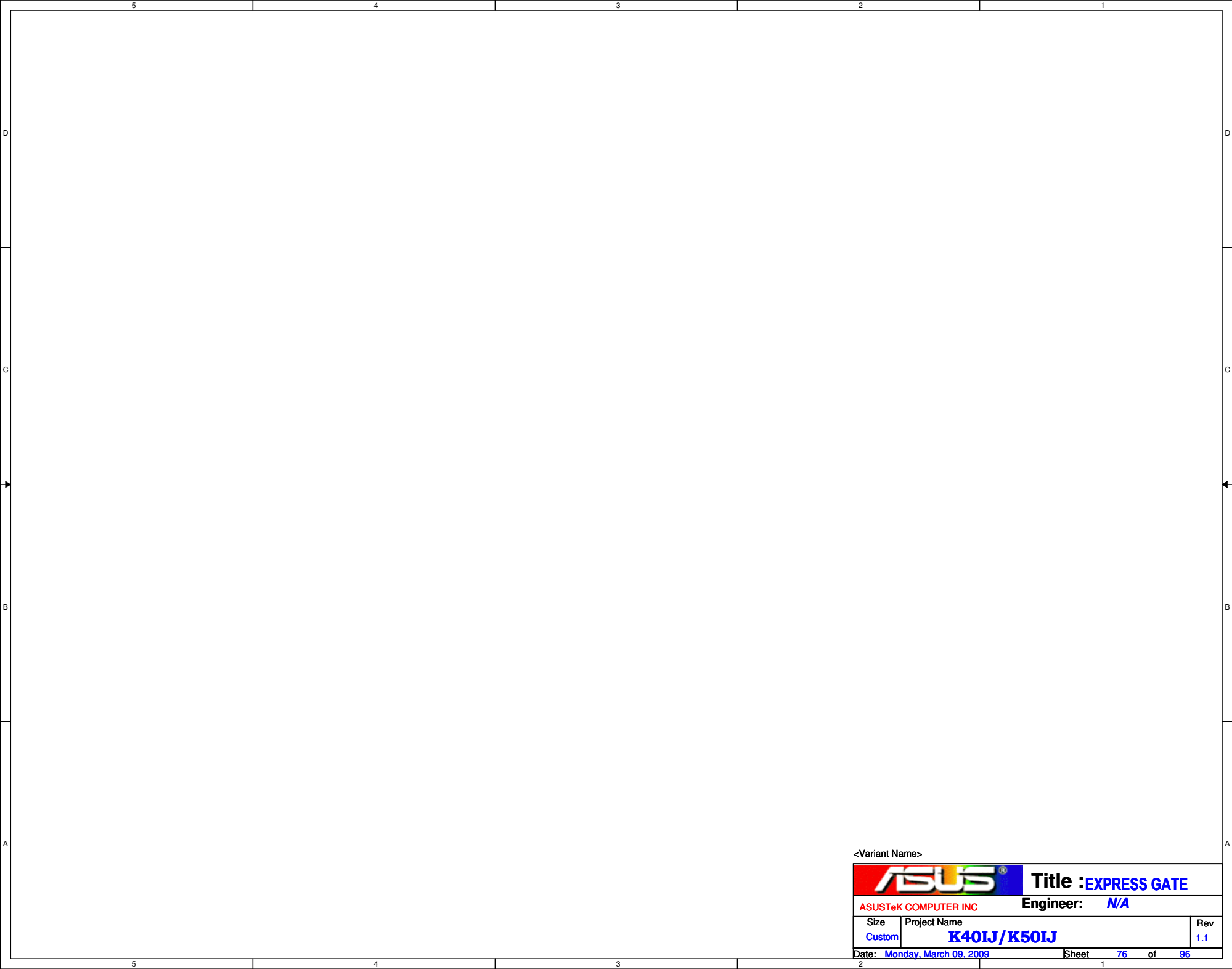
<Variant Name>

		Title : Hole	
ASUSTeK COMPUTER INC		Engineer: Leon Guo	
Size B	Project Name K40IJ/K50IJ		Rev 1.1
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	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
A	K40IJ/K50IJ		1.1
Date: Monday, March 09, 2009		Sheet	75 of 96



<Variant Name>



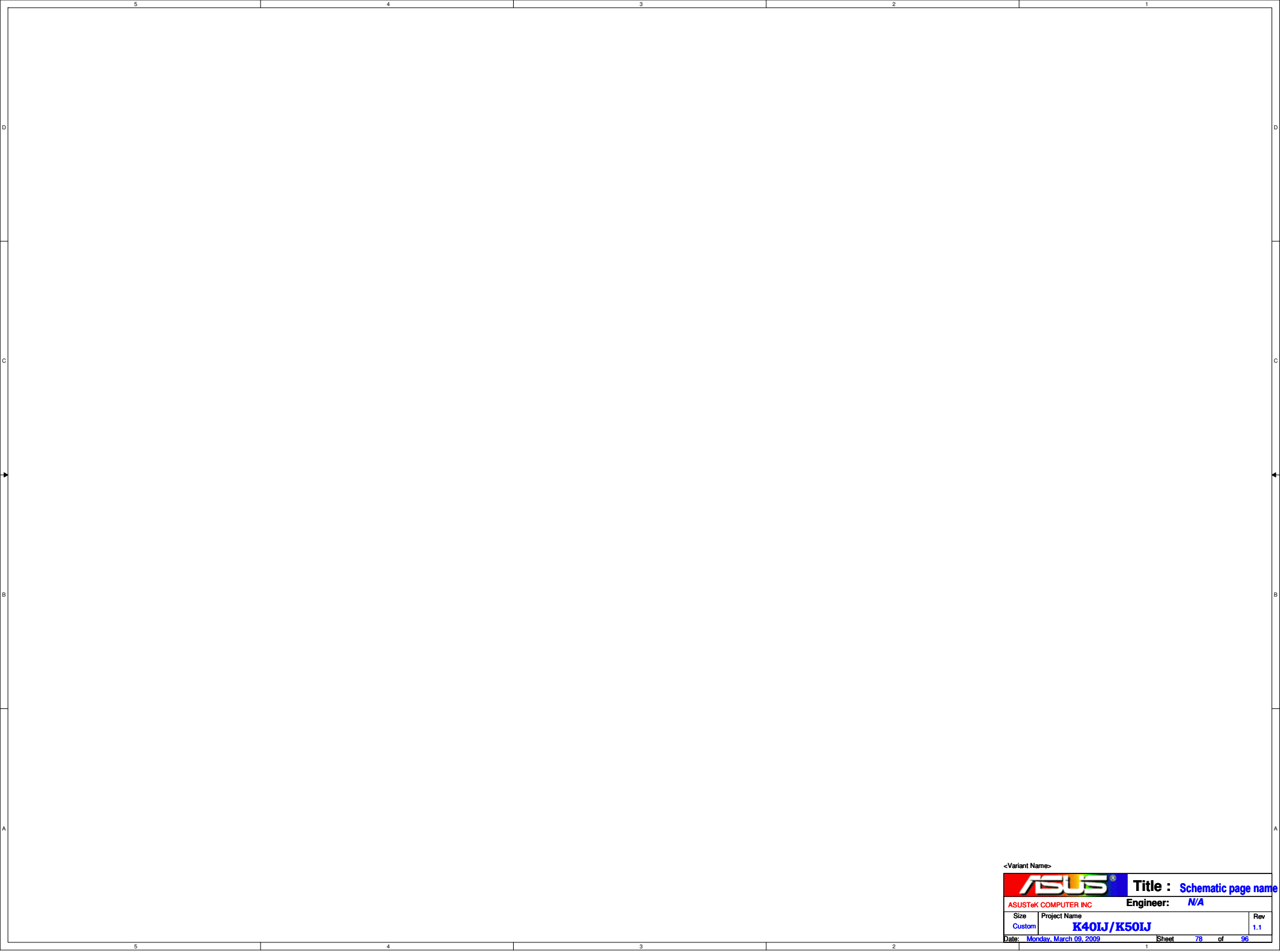
Title :EXPRESS GATE

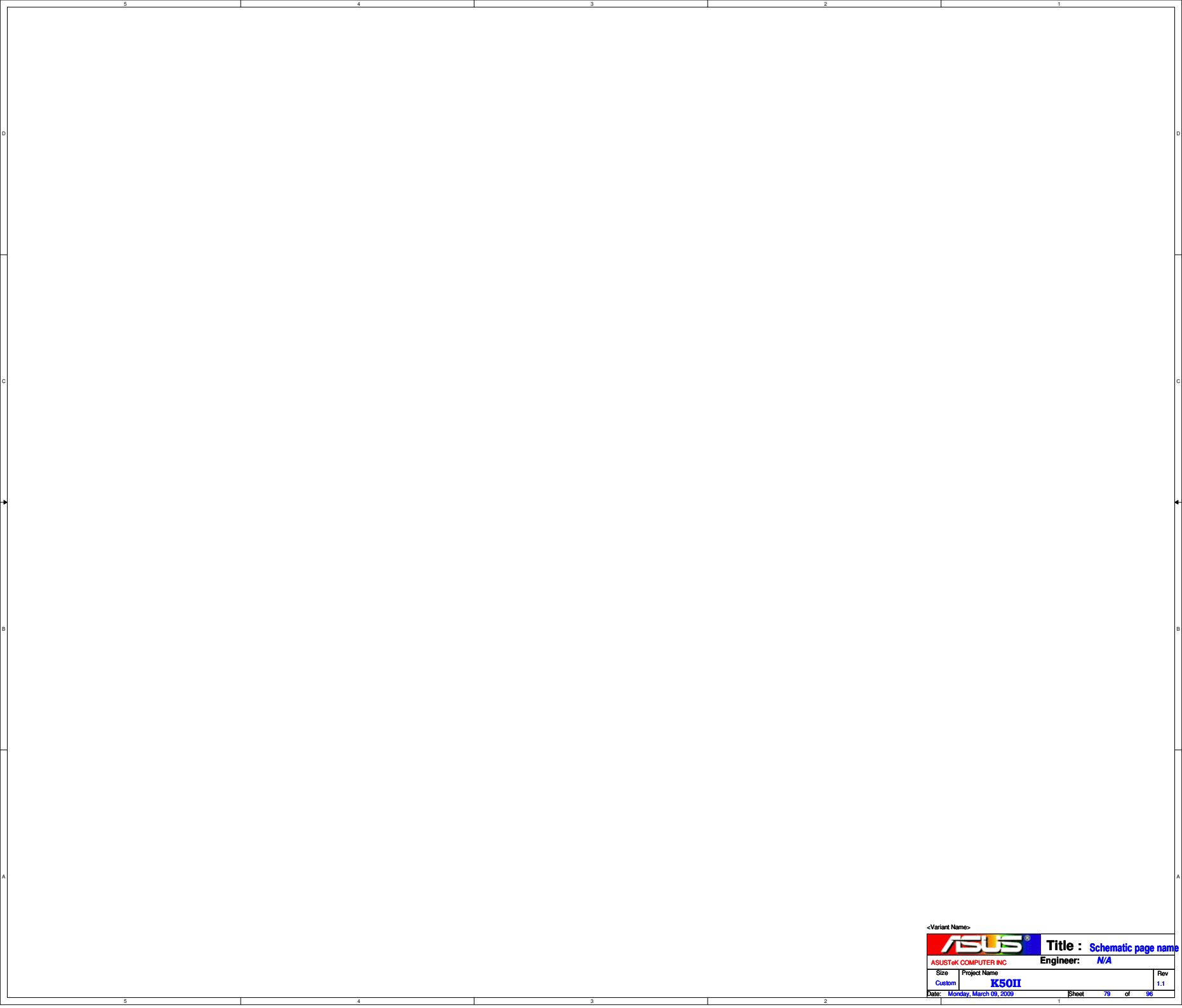
ASUSTeK COMPUTER INC

Engineer: N/A

Size Custom	Project Name K40IJ/K50IJ	Rev 1.1
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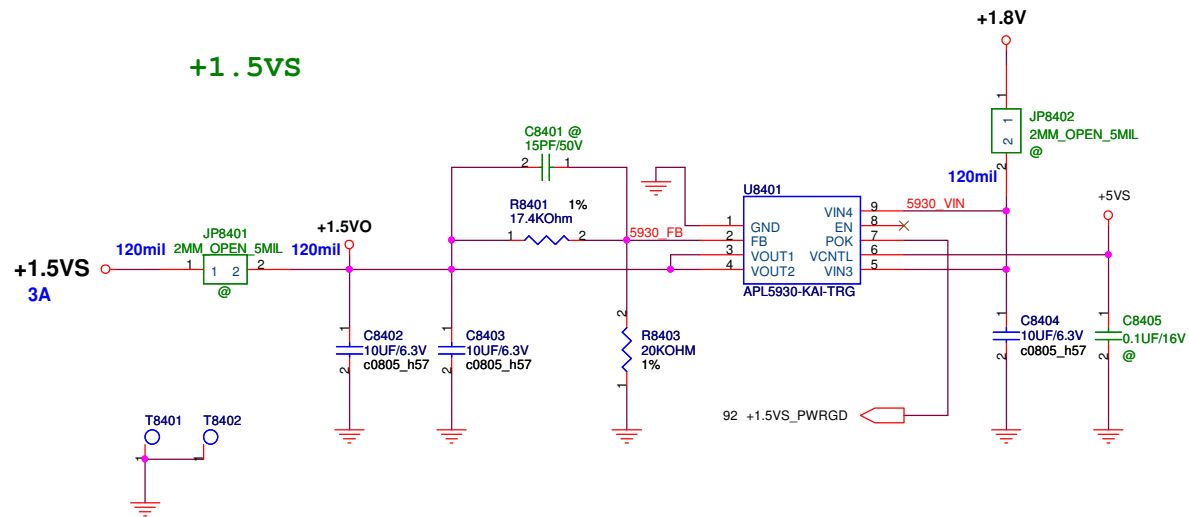
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Total count: 7 pcs

<Variant Name>

ASUS		Title :POWER I/O_+1.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Morris	
Size B	Project Name K50		Rev 1.0
Date: Monday, March 09, 2009		Sheet 84	of 96

D

C

B

A

<Variant Name>



Title :

ASUSTeK COMPUTER INC. NB1

Engineer:

Size
A

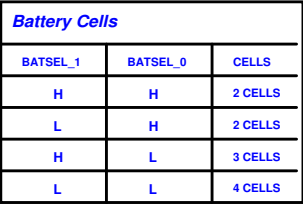
Project Name

Rev	
1.0	

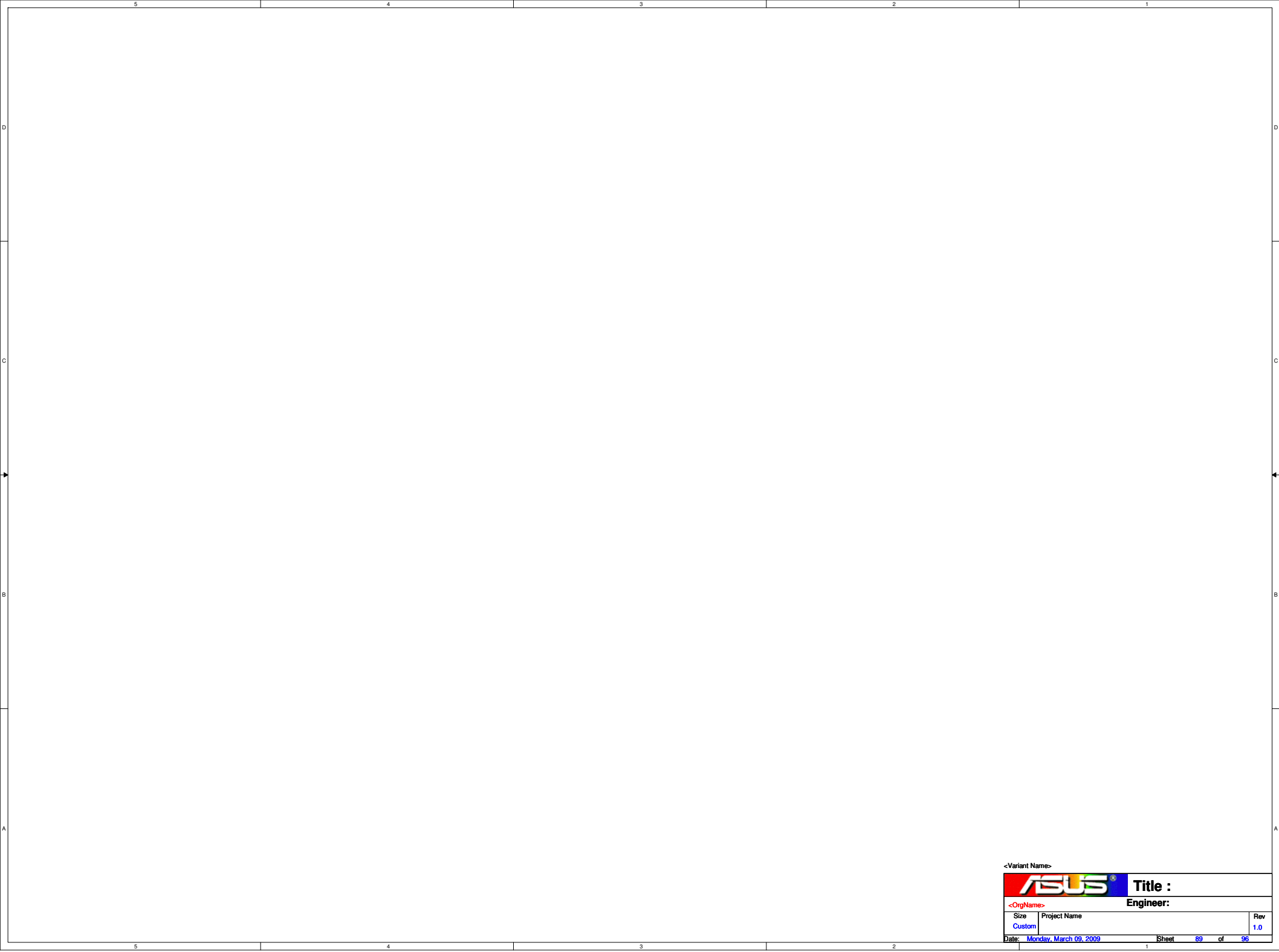
Date: Monday, March 09, 2009

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5	4	3	2	1						
D				D						
C				C						
B				B						
A				A						
<Variant Name> ASUS® Title : <OrgName> Engineer: <table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>Custom</td><td></td><td>1.0</td></tr></table> Date: Monday, March 09, 2009Sheet 87 of 96					Size	Project Name	Rev	Custom		1.0
Size	Project Name	Rev								
Custom		1.0								
5	4	3	2	1						



		Title : CHARGER_202	
ASUSTeK COMPUTER INC. NB3		Engineer: Morris	
Size Custom	Project Name K50		F 1
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<Variant Name>



Title :

<OrgName>

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: [Monday, March 09, 2009](#) Sheet [89](#) of [96](#)

BATTERY IN DETECT

<Variant Name>



Title :POWER_DETECT

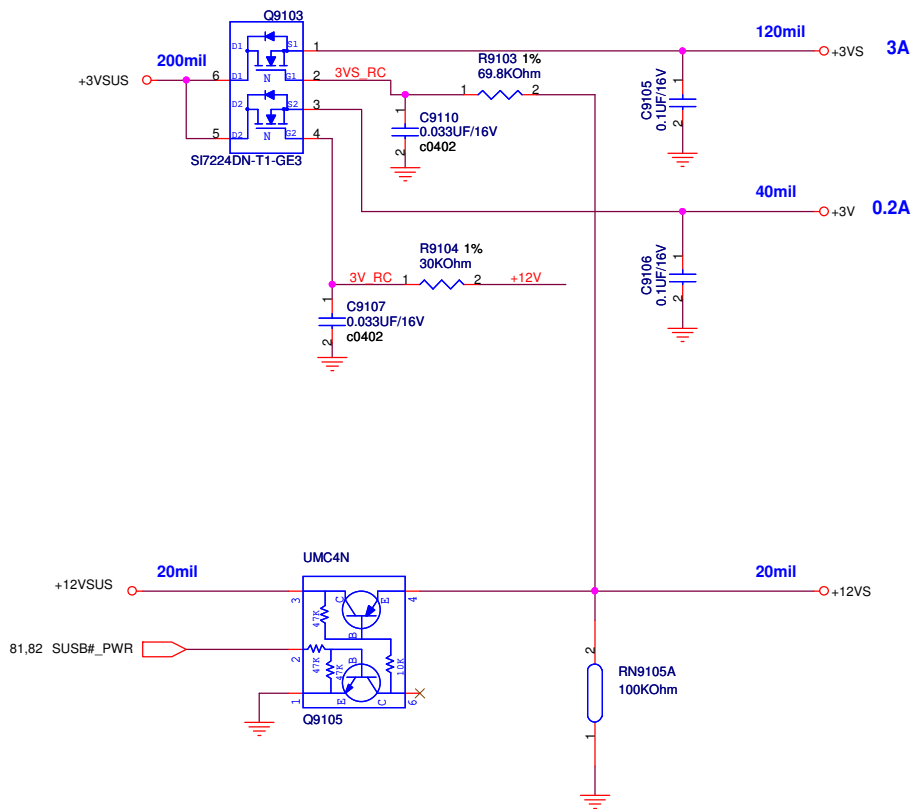
ASUSTeK COMPUTER INC. NB

Engineer: Morris

Size	Project Name	Rev
Custom	K50II	1.0

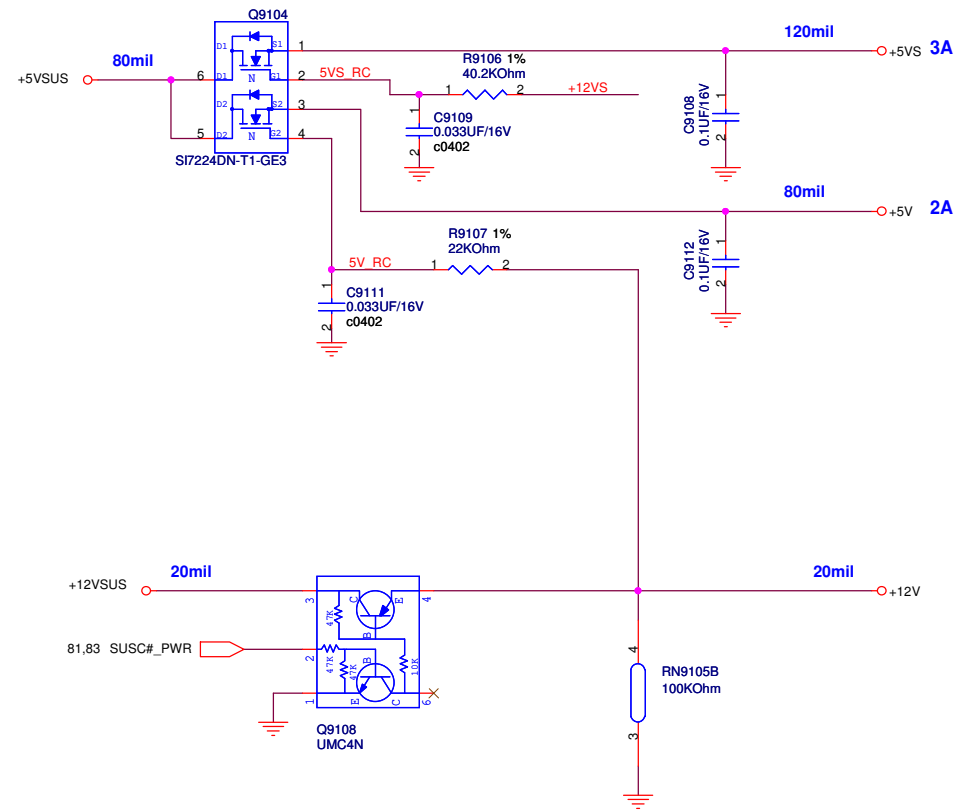
Date: Monday, March 09, 2009Sheet 90 of 96

SUSB#_PWR POWER



Total count: 19 pcs

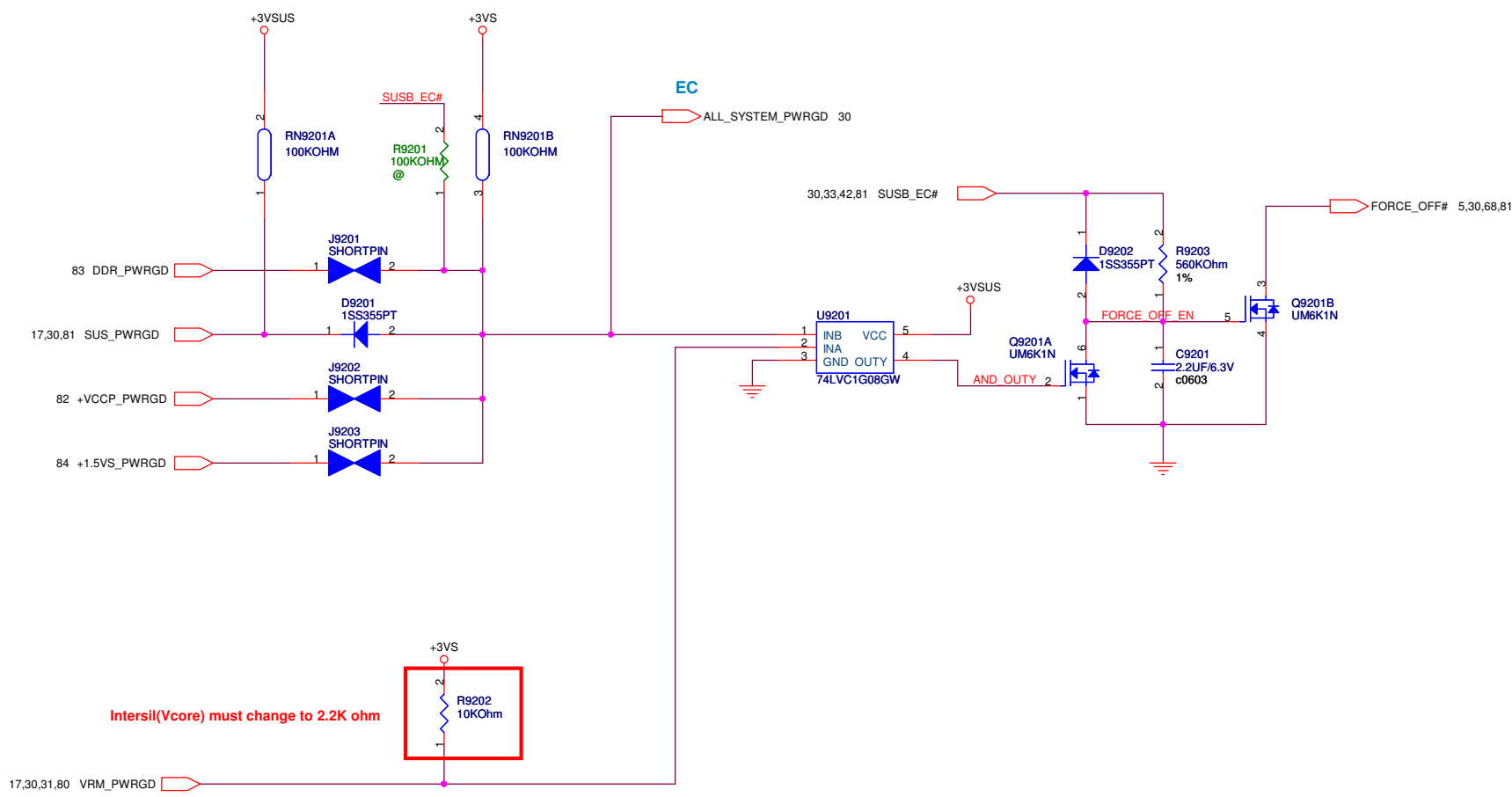
SUSC#_PWR POWER



<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris</i>	
Size B	Project Name K50		Rev 1.0
Date: Monday, March 09, 2009		Sheet 91 of 96	

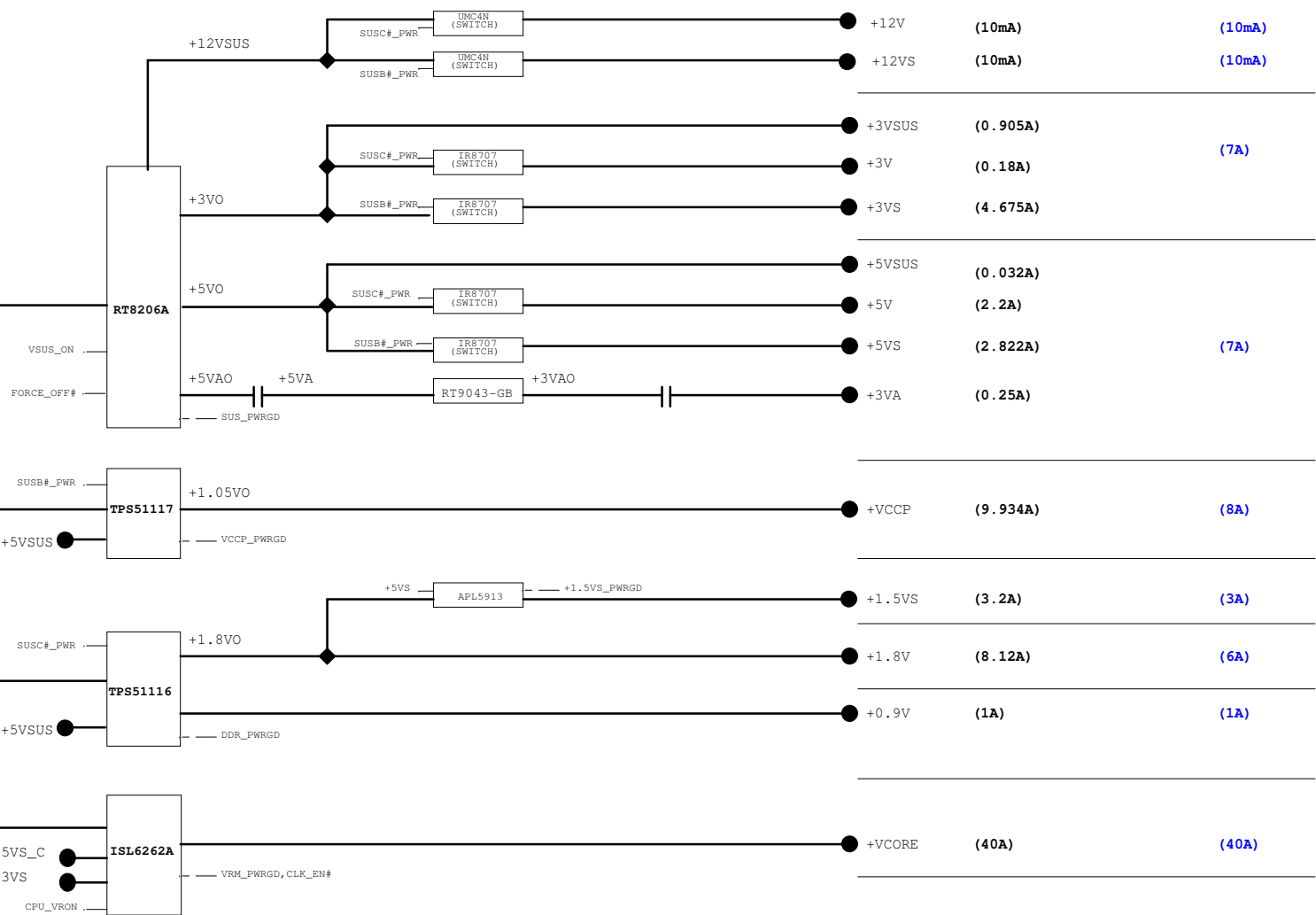
POWER GOOD DETECTOR



Total count: 8 pcs



AC_BAT_SYS



K50
Non-IAMT
Design rating

+12V	(10mA)	(10mA)
+12VS	(10mA)	(10mA)
+3VSUS	(0.905A)	
+3V	(0.18A)	(7A)
+3VS	(4.675A)	
+5VSUS	(0.032A)	
+5V	(2.2A)	
+5VS	(2.822A)	(7A)
+3VA	(0.25A)	
+VCCP	(9.934A)	(8A)
+1.5VS	(3.2A)	(3A)
+1.8V	(8.12A)	(6A)
+0.9V	(1A)	(1A)
+VCORE	(40A)	(40A)