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QBL50 Schematics Document

AMD Sabine

APU Llano / Hudson M2_M3 / Vancouver Whistler

UMA only / PX Muxless with BACO

2011-04-25

Rev:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/03/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title: Cover Page			
Size: B	Document Number: QBL50 LA-7551P		Rev: 1.0
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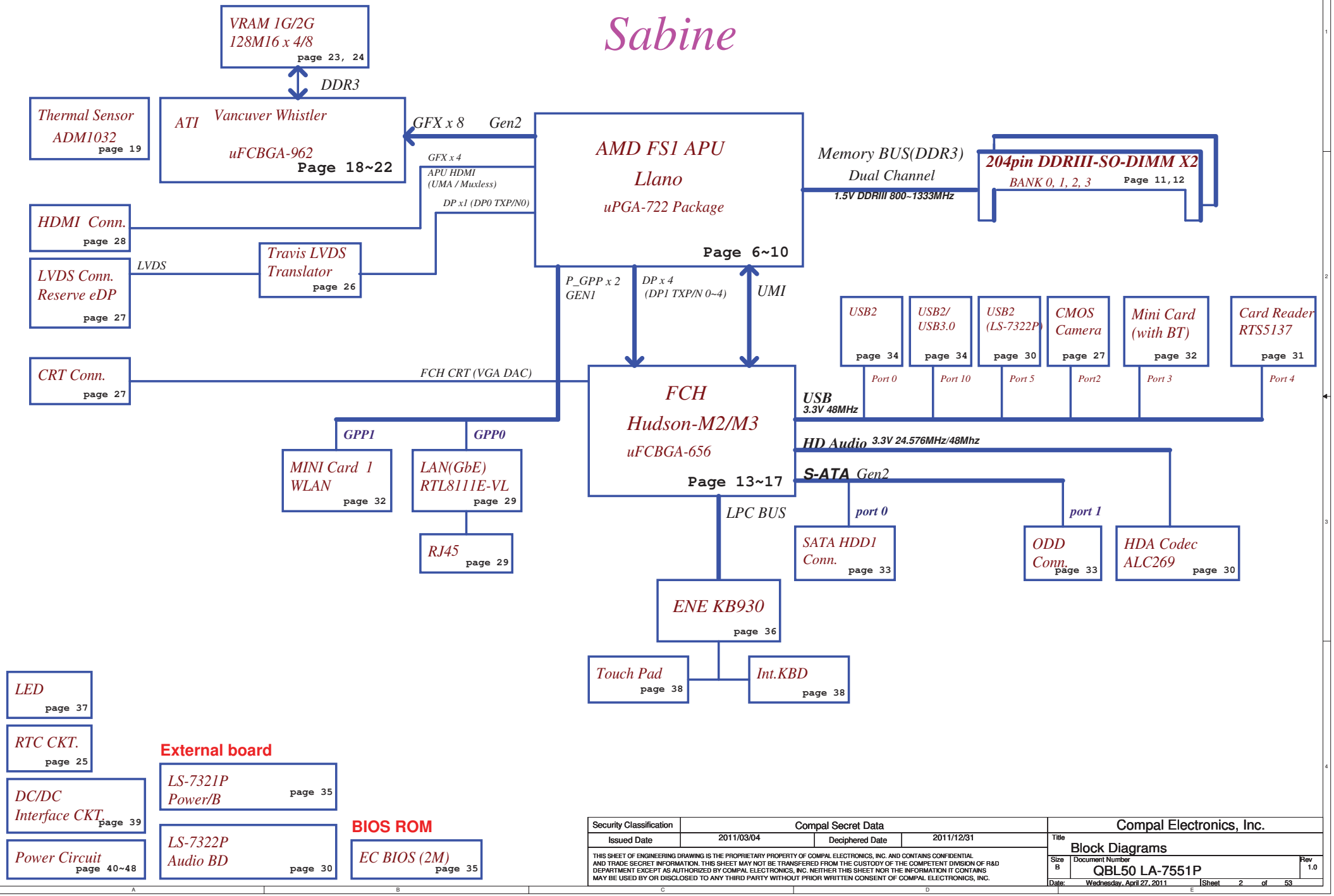
Model Name : QBL50



Security Classification	Compal Secret Data		
Issued Date	2011/03/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: B	Document Number: QBL50 LA-7551P		Rev: 1.0
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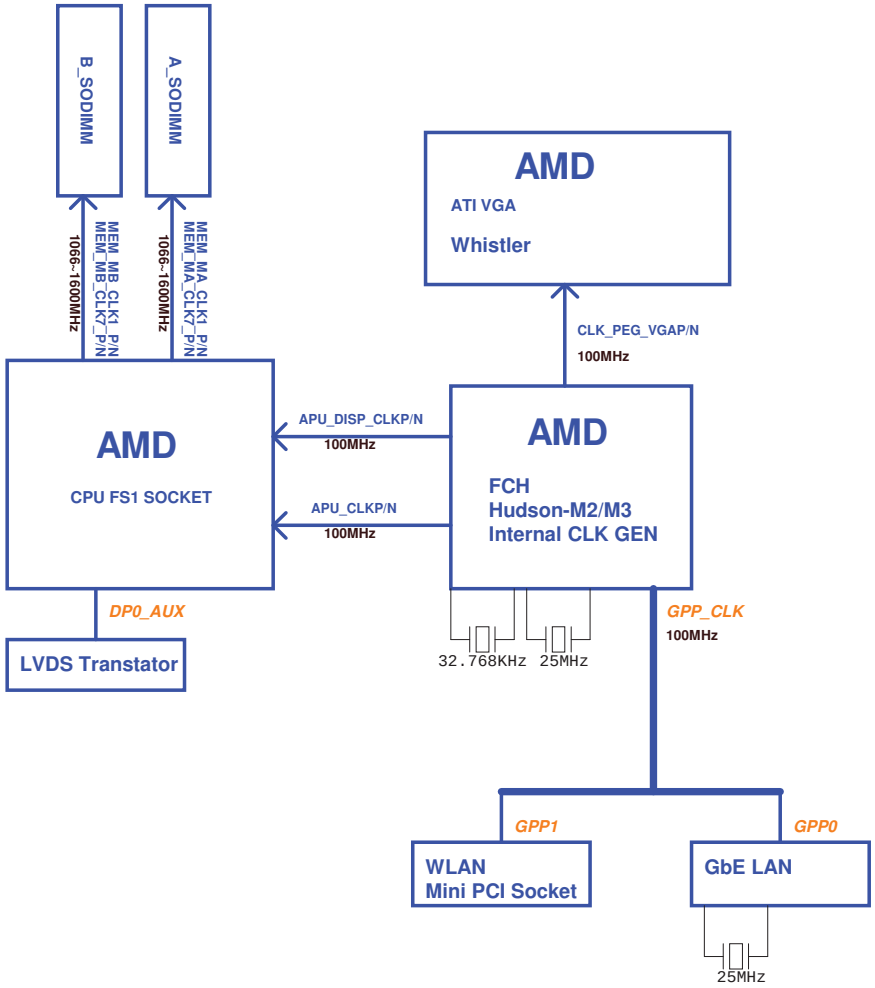
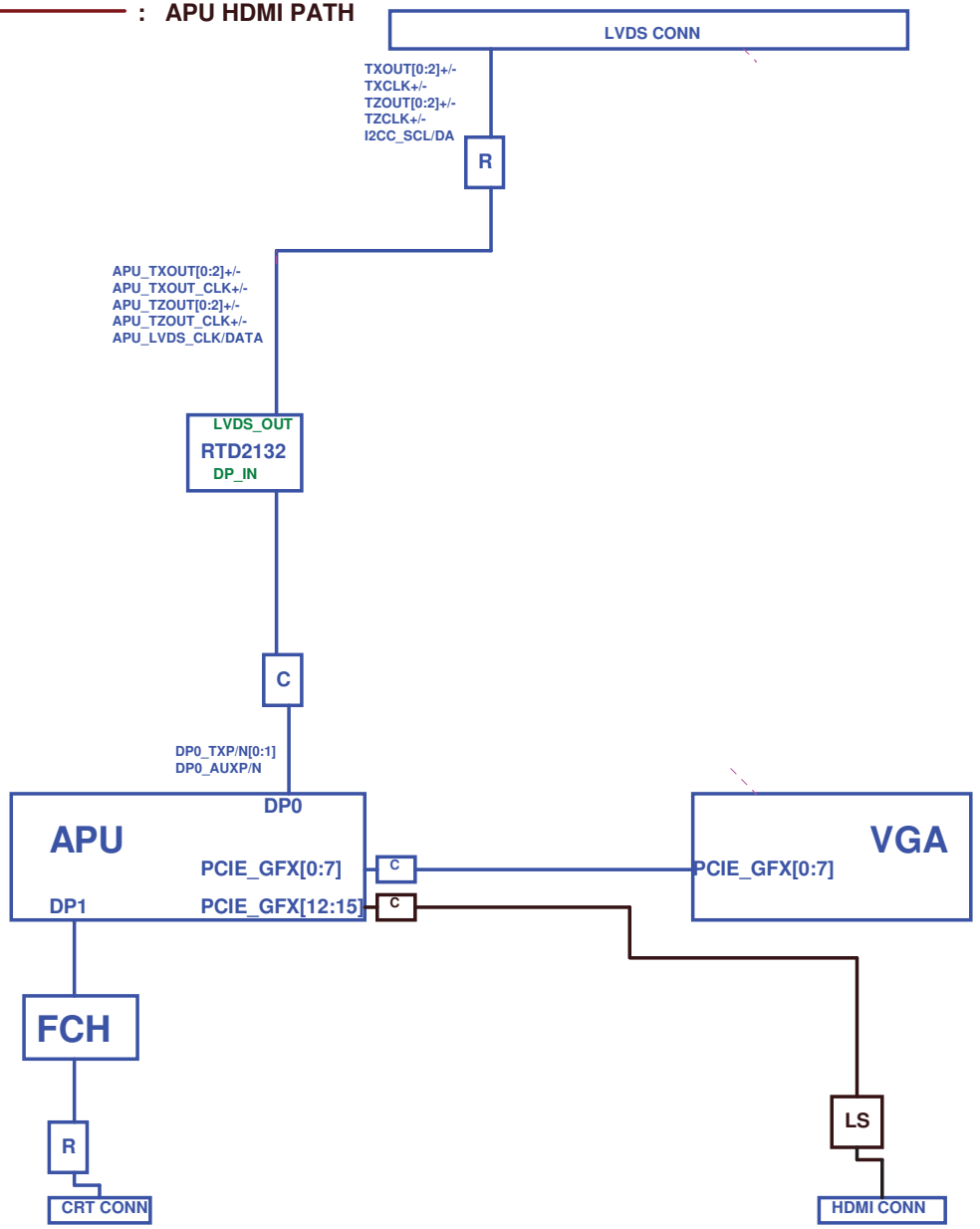
CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION

: LVDS PATH

: APU HDMI PATH



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Title	CLOCK / DISPLAY DISTRIBUTION		
Size: Custom	Document Number: QBL50 LA-7551P		Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_IO	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

BOM Structure	BTO Item
VGA@	Use VGA (Mux)
X76@	VRAM ID Table
M2@	Use Hudson-M2
M3@	Use Hudson-M3
USB30@	USB30 on M/B
USB20@	USB20 on M/B

M3@ U25

FCH M3
Part Number = SA000043ID0

BOM Config

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (VGA)	1001 101X b	9AH
(APU)		
RTD2132S (TL)		

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	D0
DDR DIMM2	1101 001X b	D2

FCH SM Bus 1 address

Device	Address	HEX

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Title: Notes List

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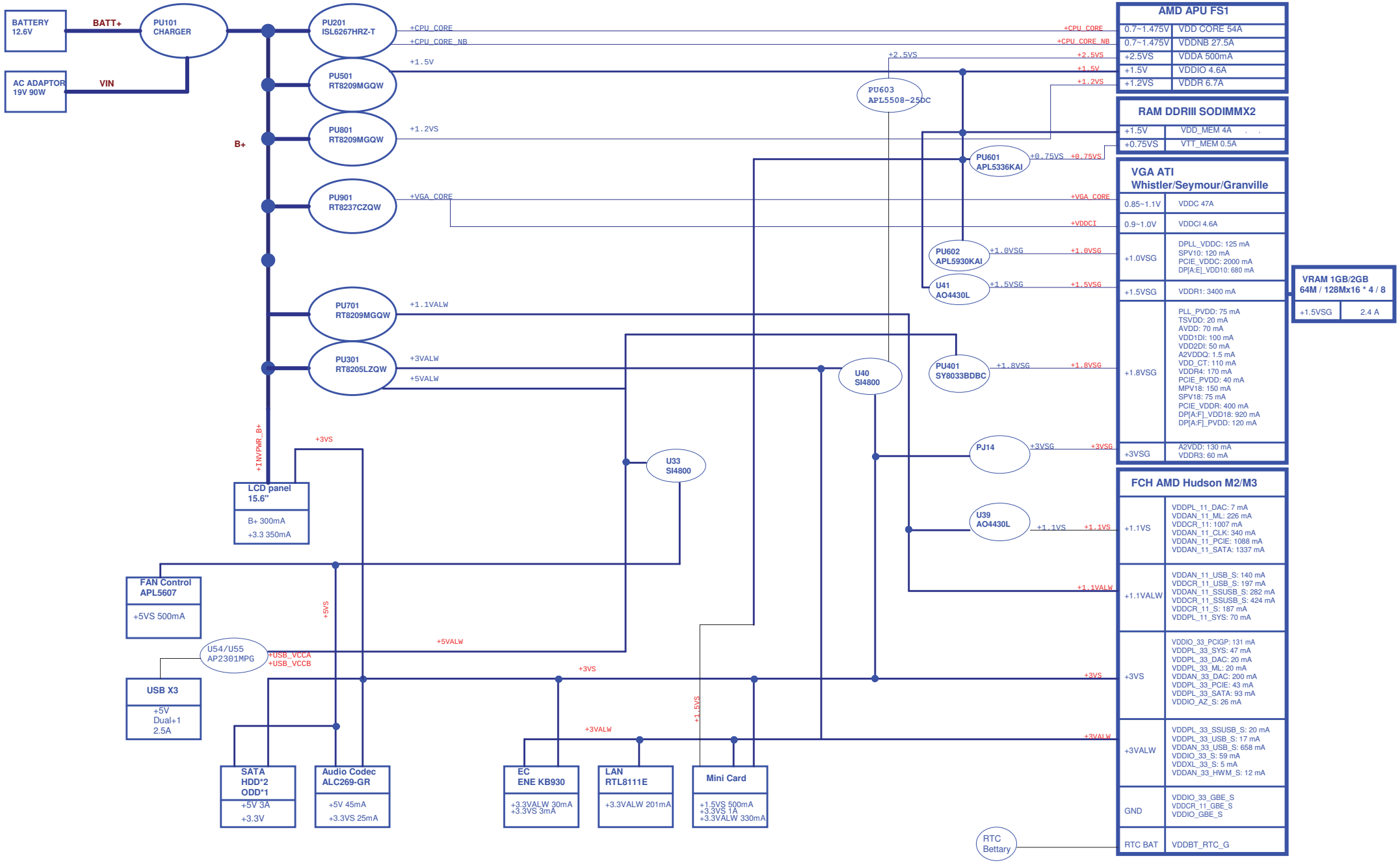
Date: Friday, April 29, 2011 | Sheet 4 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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18 PCIE_GTX_C_FRX_P[0..7]
18 PCIE_GTX_C_FRX_N[0..7]

PCIE_FTX_C_GRX_P[0..7] 18
PCIE_FTX_C_GRX_N[0..7] 18

APU To HDMI

PCIE_FTX_GRX_P[12..15] 28
PCIE_FTX_GRX_N[12..15] 28

JCPU1A — CONN@ — PCI EXPRESS — GRAPHICS

PCIE_GTX_C_FRX_P0	AA8	P_GFX_RXP0	P_GFX_TXP0	AA2	PCIE_FTX_GRX_P0	C917	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P0
PCIE_GTX_C_FRX_N0	AA9	P_GFX_RXN0	P_GFX_TXN0	AA3	PCIE_FTX_GRX_N0	C918	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N0
PCIE_GTX_C_FRX_P1	Y7	P_GFX_RXP1	P_GFX_TXP1	Y2	PCIE_FTX_GRX_P1	C919	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P1
PCIE_GTX_C_FRX_N1	Y8	P_GFX_RXN1	P_GFX_TXN1	Y1	PCIE_FTX_GRX_N1	C920	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N1
PCIE_GTX_C_FRX_P2	W5	P_GFX_RXP2	P_GFX_TXP2	Y4	PCIE_FTX_GRX_P2	C921	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P2
PCIE_GTX_C_FRX_N2	W6	P_GFX_RXN2	P_GFX_TXN2	Y5	PCIE_FTX_GRX_N2	C922	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N2
PCIE_GTX_C_FRX_P3	W8	P_GFX_RXP3	P_GFX_TXP3	W2	PCIE_FTX_GRX_P3	C923	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P3
PCIE_GTX_C_FRX_N3	W9	P_GFX_RXN3	P_GFX_TXN3	W3	PCIE_FTX_GRX_N3	C924	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N3
PCIE_GTX_C_FRX_P4	V7	P_GFX_RXP4	P_GFX_TXP4	V2	PCIE_FTX_GRX_P4	C925	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P4
PCIE_GTX_C_FRX_N4	V8	P_GFX_RXN4	P_GFX_TXN4	V1	PCIE_FTX_GRX_N4	C926	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N4
PCIE_GTX_C_FRX_P5	U5	P_GFX_RXP5	P_GFX_TXP5	V4	PCIE_FTX_GRX_P5	C927	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_P5
PCIE_GTX_C_FRX_N5	U6	P_GFX_RXN5	P_GFX_TXN5	V5	PCIE_FTX_GRX_N5	C928	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N5
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PCIE_GTX_C_FRX_N7	T8	P_GFX_RXN7	P_GFX_TXN7	T1	PCIE_FTX_GRX_N7	C932	VGA@	0.1U_0402_16V7K	PCIE_FTX_C_GRX_N7
	R5	P_GFX_RXP8	P_GFX_TXP8	T4					
	R6	P_GFX_RXN8	P_GFX_TXN8	T5					
	R8	P_GFX_RXP9	P_GFX_TXP9	R2					
	R9	P_GFX_RXN9	P_GFX_TXN9	R3					
	P7	P_GFX_RXP10	P_GFX_TXP10	P2					
	P8	P_GFX_RXN10	P_GFX_TXN10	P1					
	N5	P_GFX_RXP11	P_GFX_TXP11	P4					
	N6	P_GFX_RXN11	P_GFX_TXN11	P5					
	N8	P_GFX_RXP12	P_GFX_TXP12	N2	PCIE_FTX_GRX_P12				
	N9	P_GFX_RXN12	P_GFX_TXN12	N3	PCIE_FTX_GRX_N12				
	M7	P_GFX_RXP13	P_GFX_TXP13	M2	PCIE_FTX_GRX_P13				
	M8	P_GFX_RXN13	P_GFX_TXN13	M1	PCIE_FTX_GRX_N13				
	L5	P_GFX_RXP14	P_GFX_TXP14	M4	PCIE_FTX_GRX_P14				
	L6	P_GFX_RXN14	P_GFX_TXN14	M5	PCIE_FTX_GRX_N14				
	L8	P_GFX_RXP15	P_GFX_TXP15	L2	PCIE_FTX_GRX_P15				
	L9	P_GFX_RXN15	P_GFX_TXN15	L3	PCIE_FTX_GRX_N15				

For UMA Mux.

2 / 1 / 0 / CK — *To HDMI*

GPP

29 PCIE_DTX_C_FRX_P0	AC5	P_GPP_RXP0	P_GPP_TXP0	AD4	PCIE_FTX_DRX_P0	C950	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P0 29	*GLAN*
29 PCIE_DTX_C_FRX_N0	AC6	P_GPP_RXN0	P_GPP_TXN0	AD5	PCIE_FTX_DRX_N0	C951	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N0 29	
32 PCIE_DTX_C_FRX_P1	AC8	P_GPP_RXP1	P_GPP_TXP1	AC2	PCIE_FTX_DRX_P1	C952	0.1U_0402_16V7K	PCIE_FTX_C_DRX_P1 32	*WLAN*
32 PCIE_DTX_C_FRX_N1	AC9	P_GPP_RXN1	P_GPP_TXN1	AC3	PCIE_FTX_DRX_N1	C953	0.1U_0402_16V7K	PCIE_FTX_C_DRX_N1 32	
	AB7	P_GPP_RXP2	P_GPP_TXP2	AB2					
	AB8	P_GPP_RXN2	P_GPP_TXN2	AB1					
	AA5	P_GPP_RXP3	P_GPP_TXP3	AB4					
	AA6	P_GPP_RXN3	P_GPP_TXN3	AB5					

UMI_LINK

13 UMI_MTX_C_FRX_P0	AF8	P_UMI_RXP0	P_UMI_TXP0	AF1	UMI_FTX_MRX_P0	C956	0.1U_0402_16V7K	UMI_FTX_C_MRX_P0 13	
13 UMI_MTX_C_FRX_N0	AF7	P_UMI_RXN0	P_UMI_TXN0	AF2	UMI_FTX_MRX_N0	C957	0.1U_0402_16V7K	UMI_FTX_C_MRX_N0 13	
13 UMI_MTX_C_FRX_P1	AE6	P_UMI_RXP1	P_UMI_TXP1	AF5	UMI_FTX_MRX_P1	C958	0.1U_0402_16V7K	UMI_FTX_C_MRX_P1 13	
13 UMI_MTX_C_FRX_N1	AE5	P_UMI_RXN1	P_UMI_TXN1	AF4	UMI_FTX_MRX_N1	C959	0.1U_0402_16V7K	UMI_FTX_C_MRX_N1 13	
13 UMI_MTX_C_FRX_P2	AE9	P_UMI_RXP2	P_UMI_TXP2	AE3	UMI_FTX_MRX_P2	C960	0.1U_0402_16V7K	UMI_FTX_C_MRX_P2 13	
13 UMI_MTX_C_FRX_N2	AE8	P_UMI_RXN2	P_UMI_TXN2	AE2	UMI_FTX_MRX_N2	C961	0.1U_0402_16V7K	UMI_FTX_C_MRX_N2 13	
13 UMI_MTX_C_FRX_P3	AD8	P_UMI_RXP3	P_UMI_TXP3	AD1	UMI_FTX_MRX_P3	C962	0.1U_0402_16V7K	UMI_FTX_C_MRX_P3 13	
13 UMI_MTX_C_FRX_N3	AD7	P_UMI_RXN3	P_UMI_TXN3	AD2	UMI_FTX_MRX_N3	C963	0.1U_0402_16V7K	UMI_FTX_C_MRX_N3 13	

+1.2VS — R539 1 2 P_ZVDDP 196_0402_1% — K5 P_ZVDDP

K4 P_ZVSS — R540 1 2 196_0402_1%

AMD_TOPEDO_FS-1

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

C935 1 2 0.1U_0402_16V4Z

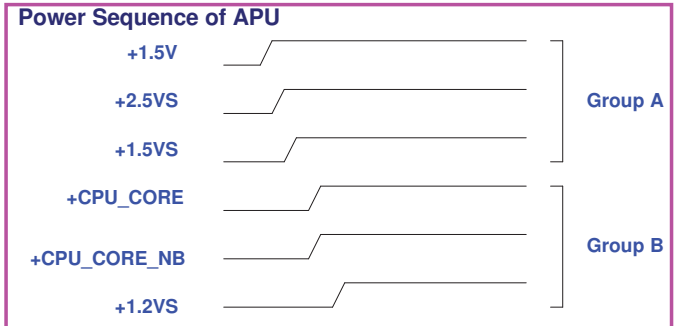
+3VS — R535 1 2 31.6K_0402_1% — R536 1 2 30K_0402_1%

8,14 APU_SID — APU_SID — Q9 BSH111 1N_SOT23-3 — EC_SMB_DA — R537 0_0402_5% — EC_SMB_DA2 19,36

8,14 APU_SIC — APU_SIC — Q10 BSH111 1N_SOT23-3 — EC_SMB_CK — R538 0_0402_5% — EC_SMB_CK2 19,36

To EC

Power Sequence of APU



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Compal Electronics, Inc.

Title: AMD FS1 PCIE / UMI / TSI

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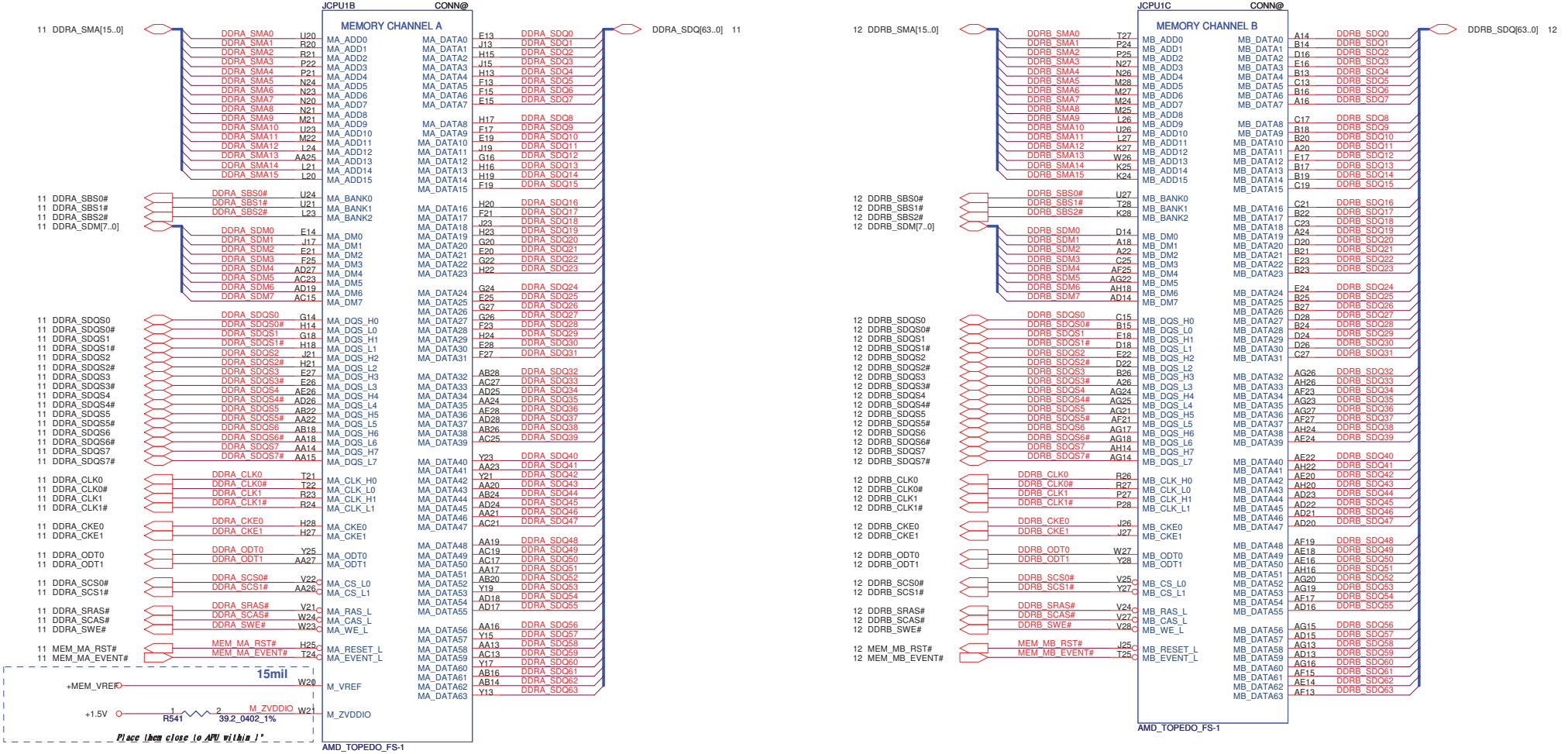
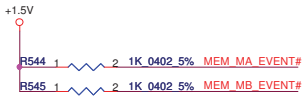
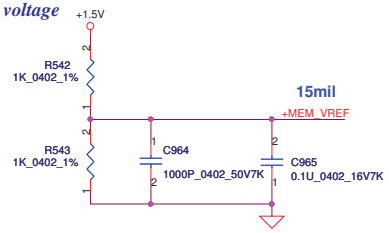


EVENT# pull high



0.75V reference voltage



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: AMD FS1 DDRIII I/F

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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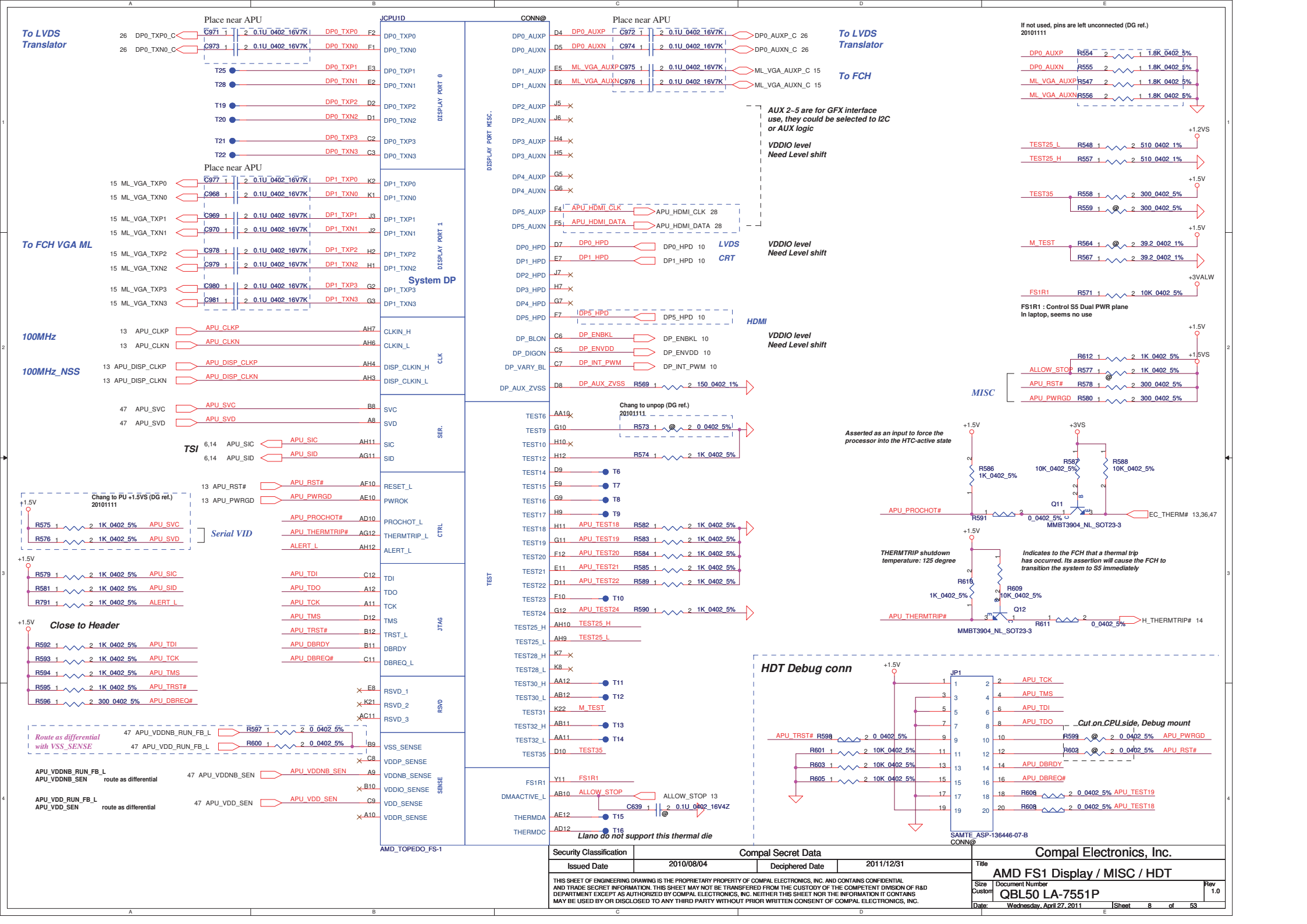

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Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: AMD FS1 Display / MISC / HDT

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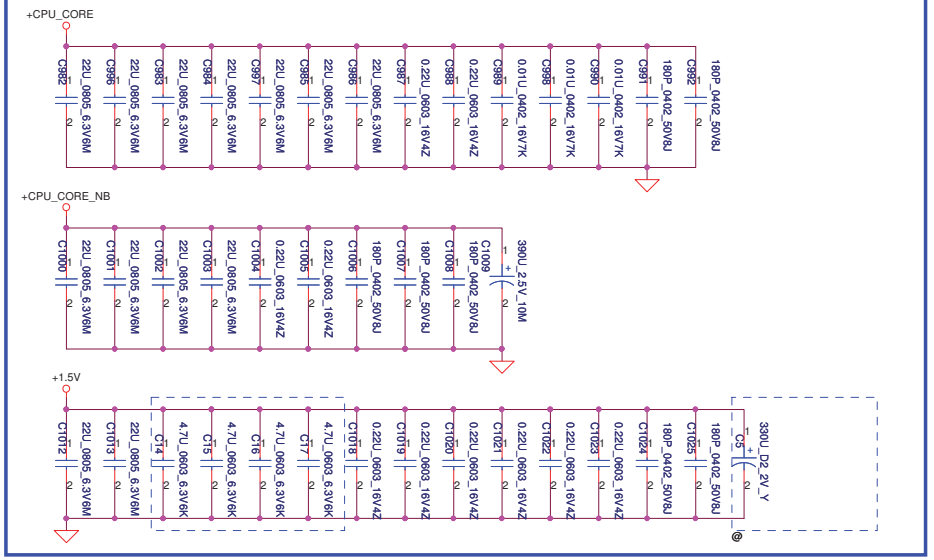
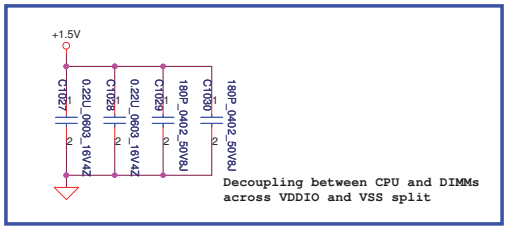
Power Name	Consumption
VDD +CPU_CORE	50A
VDDNB +CPU_CORE_NB	22.5A
VDDIO +1.5V	4A
VDDP / VDDR +1.2VS	3A / 3.5A
VDDA +2.5VS	0.75A

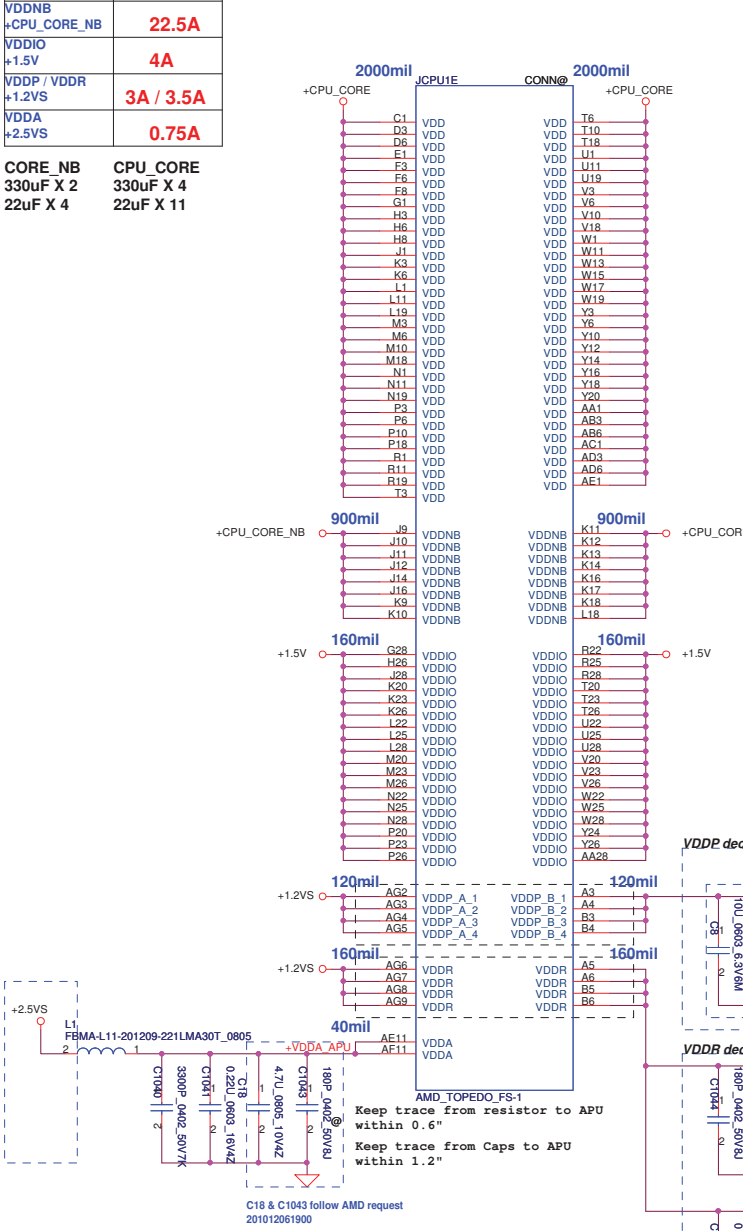
CORE_NB	CPU_CORE
330uF X 2	330uF X 4
22uF X 4	22uF X 11

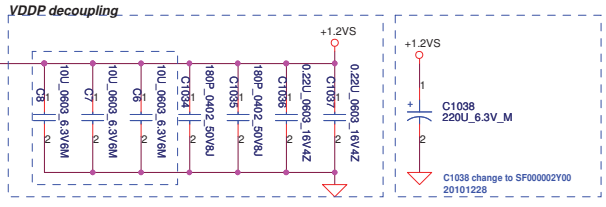
CPU BOTTOM SIDE DECOUPLING

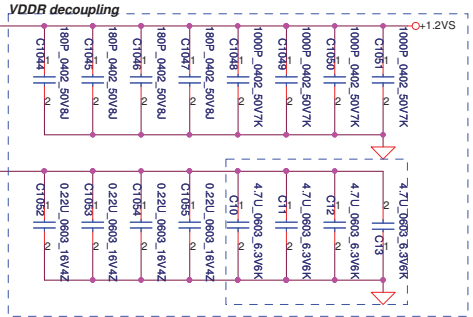


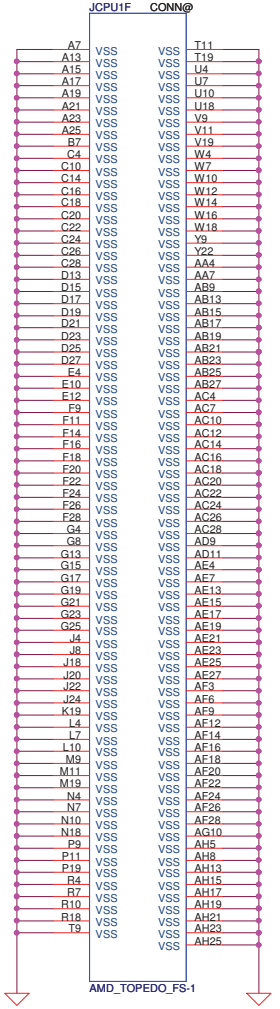


Decoupling between CPU and DIMMs across VDDIO and VSS split









Demo Board Capacitor (include PWM side)

CPU_CORE	CORE_NB	VDDIO_SUS (CPU side)	VDDIO_SUS (DIMM x2)	VDDP/R_PWM	VDDP	VDDR
470uF x 6	470uF x 4	680uF x 1	100uF x 4	470uF x 2	10uF x 3	4.7uF x 4
22uF x 9	22uF x 6	330uF x 1	0.1uF	10uF x 1	0.22uF x 2	0.22uF x 4
0.22uF x 2	0.22uF x 2	22uF x 3			180pF x 2	1nF x 4
180pF x 2	180uF x 3	4.7uF x 4				180pF x 4
10nF x 3		0.22uF x 6				
		180pF x 4				

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: AMD FS1 PWR / GND

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

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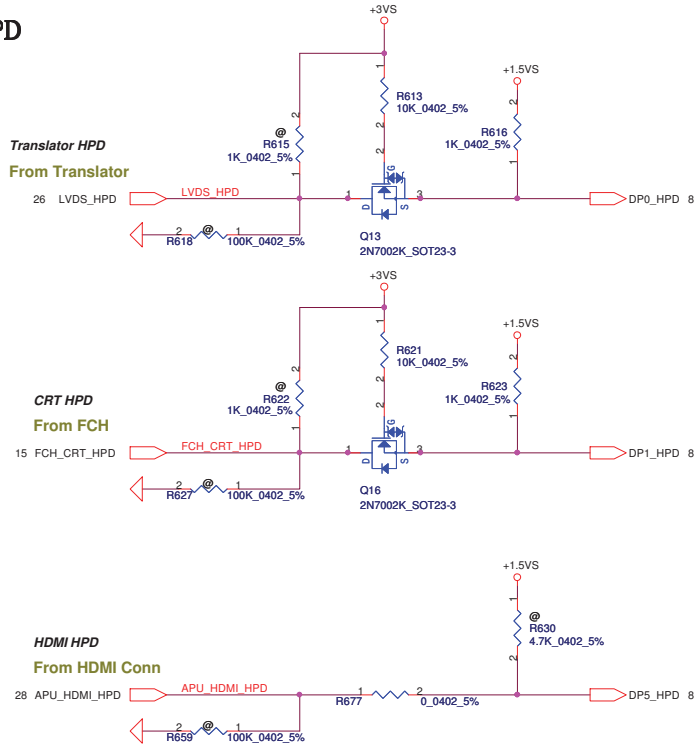
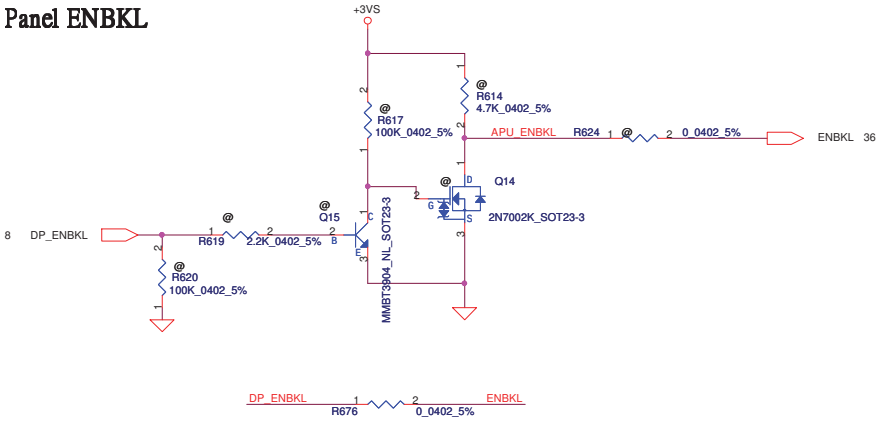
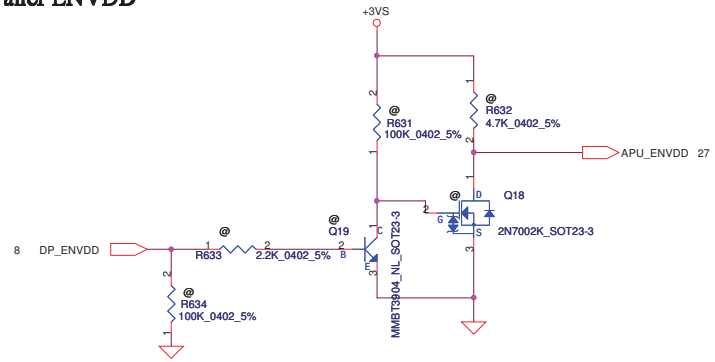
HPD



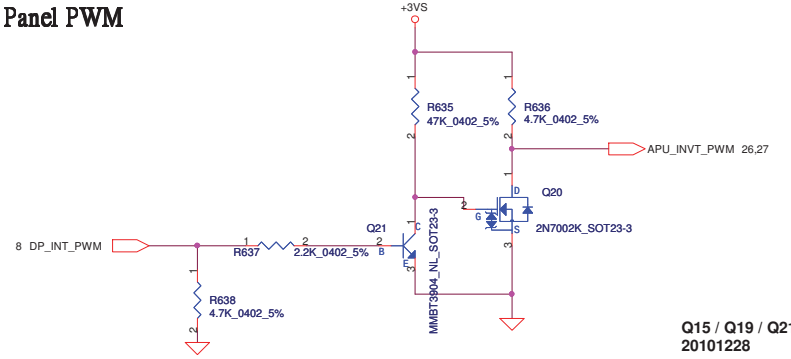
Panel ENBKL



Panel ENVDD



Panel PWM



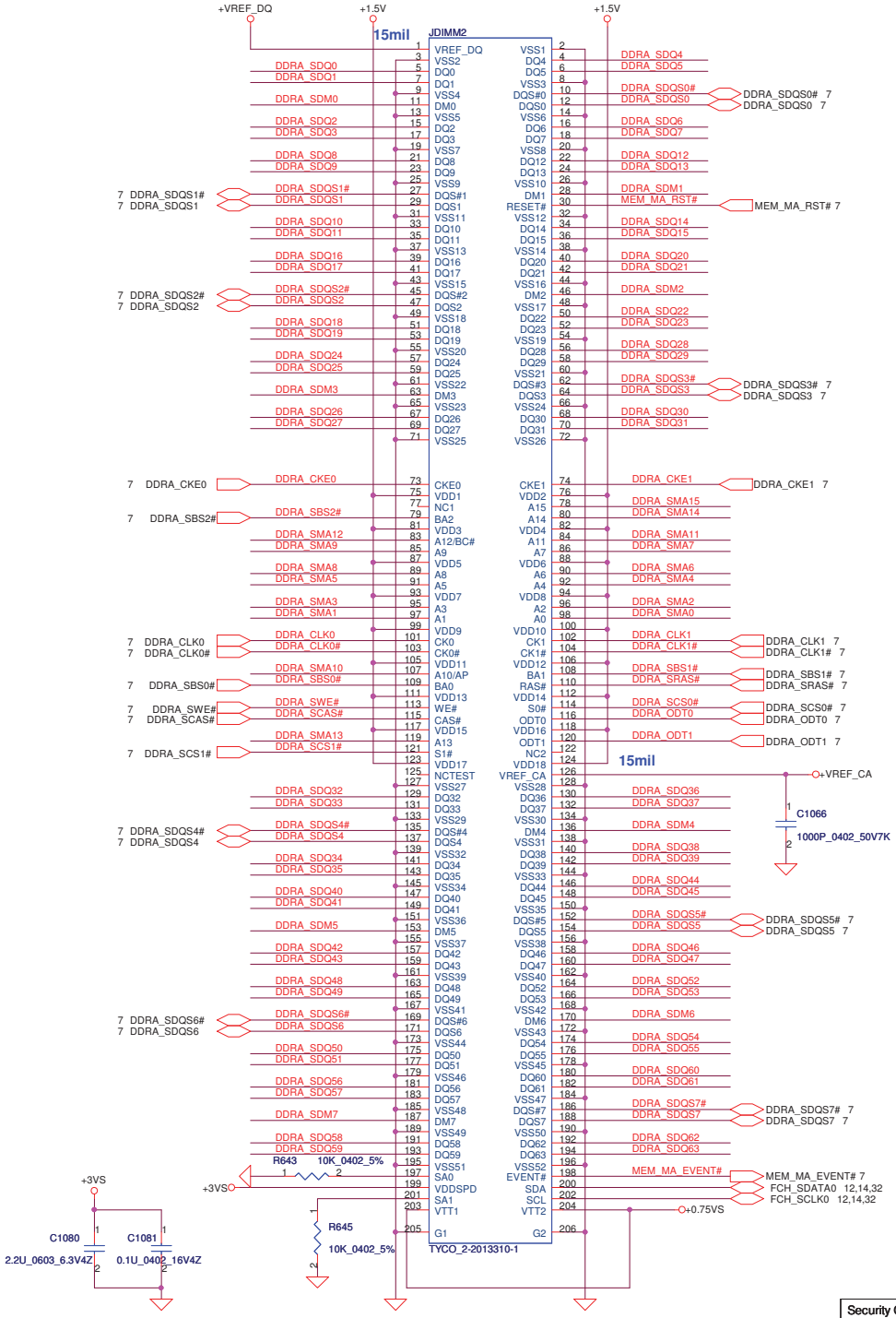
Q15 / Q19 / Q21 change to SB000006A00
20101228

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Title: AMD FS1 Singal Level Shifter

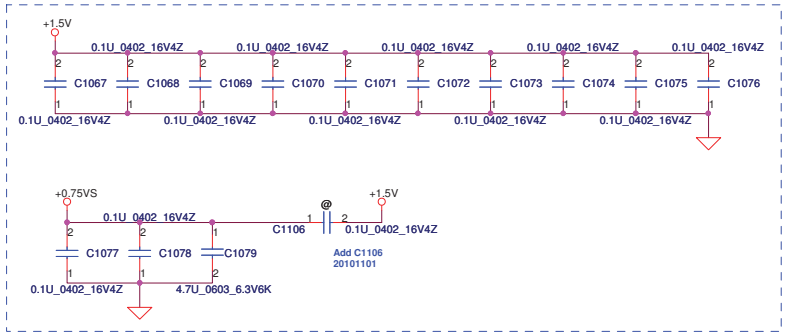
Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

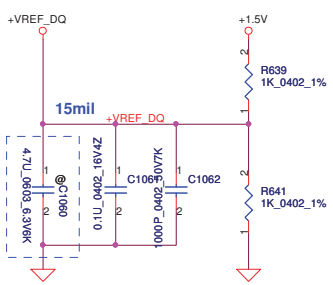
Date: Wednesday, April 27, 2011 Sheet 10 of 53

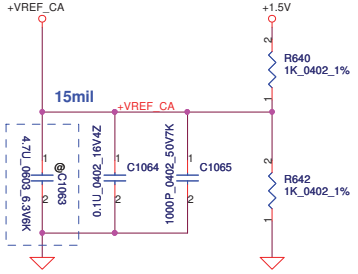


DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 7
DDRA_SDM[0..7] → DDRA_SDM[0..7] 7
DDRA_SMA[0..15] → DDRA_SMA[0..15] 7

Place near DIMM1







DIMM_A STD H:9.2mm

<Address: 00>

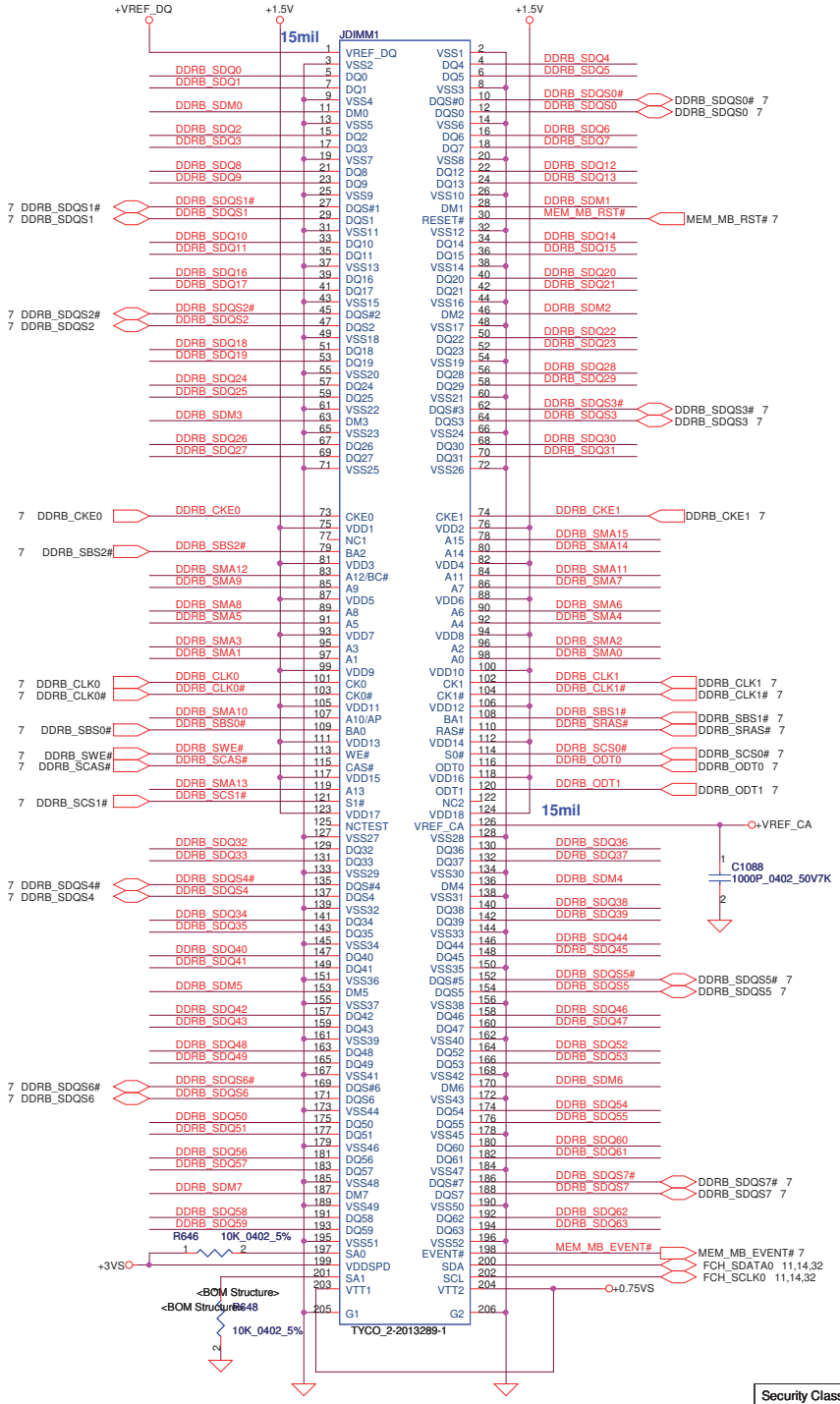
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

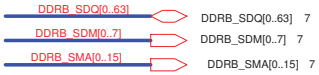
Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 11 of 53

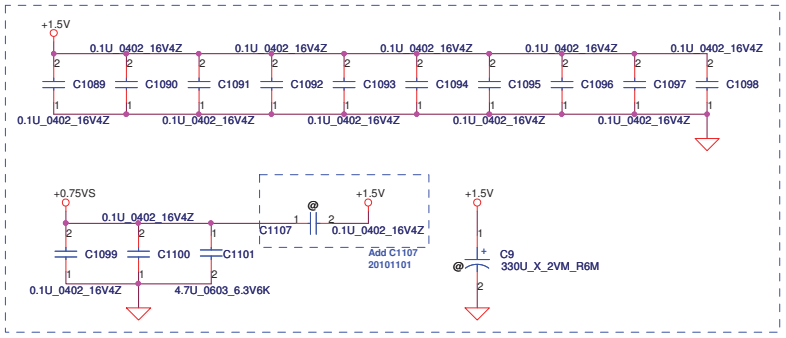


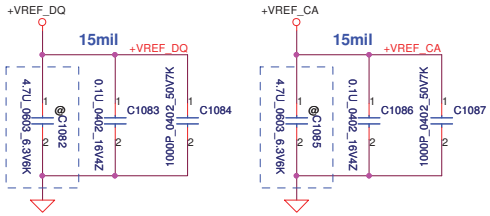
DIMM_B STD H:5.2mm

<Address: 01>



Place near DIMM2





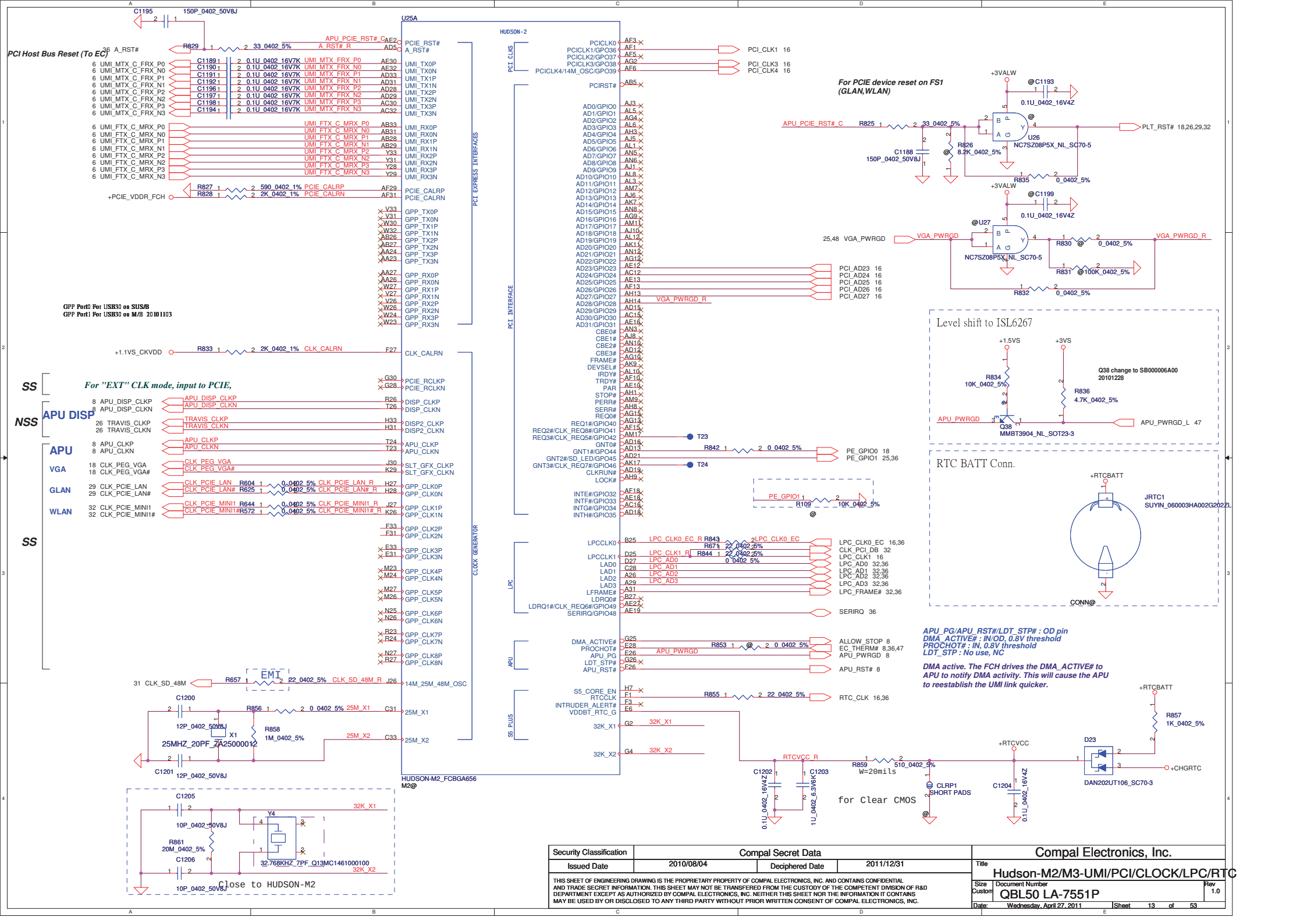
Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 Sheet 12 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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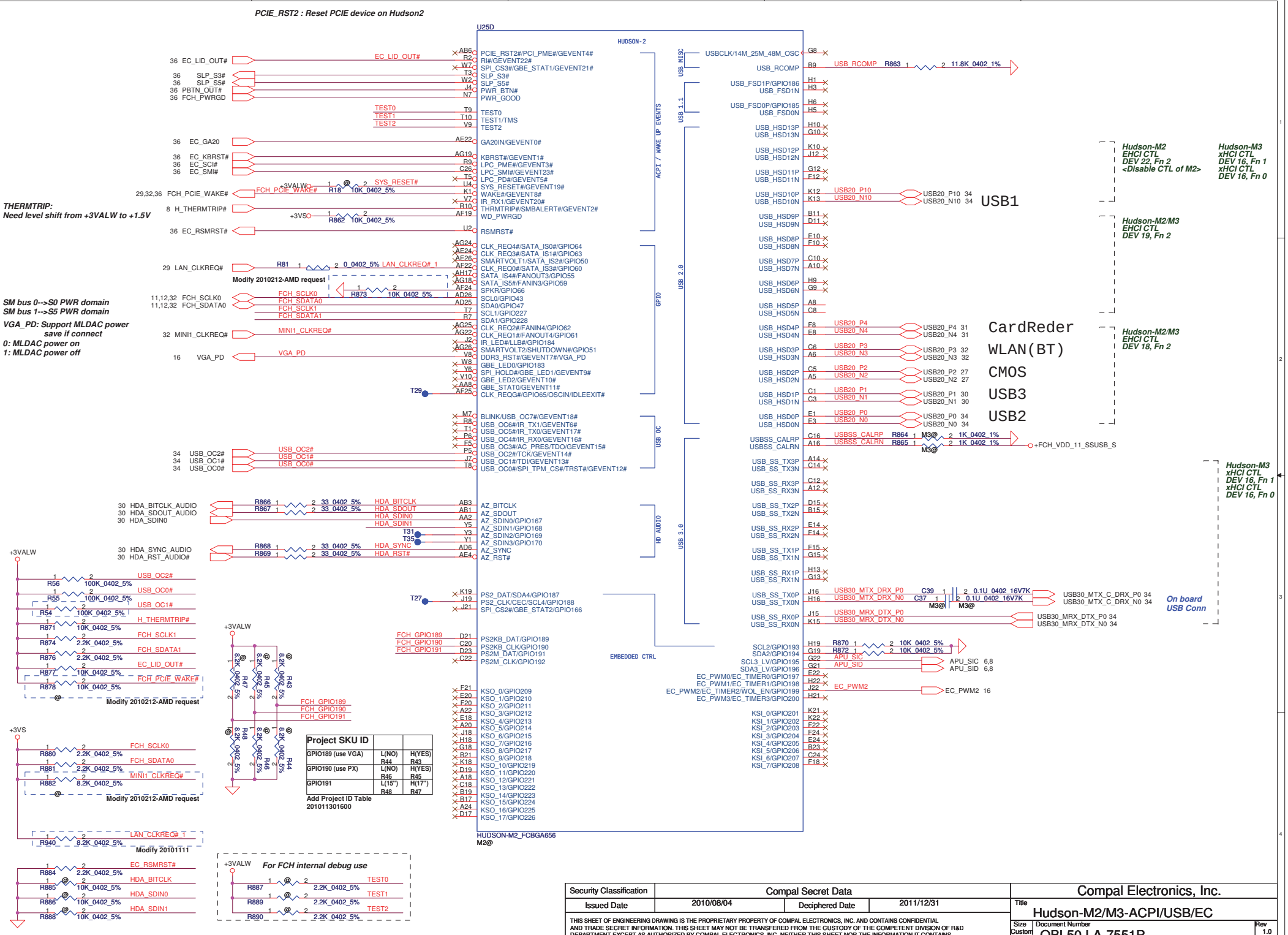

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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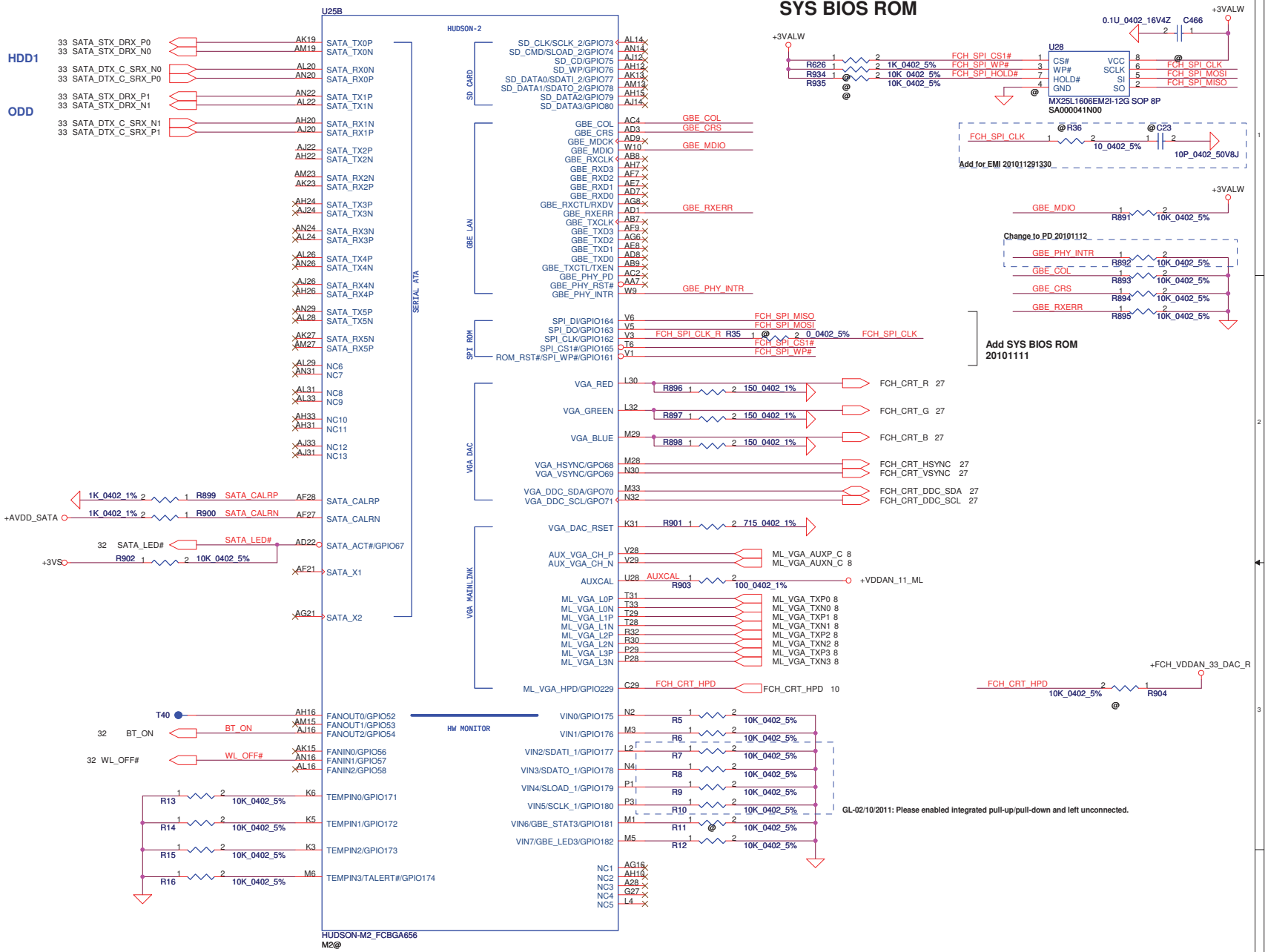
SYS BIOS ROM



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Hudson-M2/M3-SATA/GBE/HWM

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

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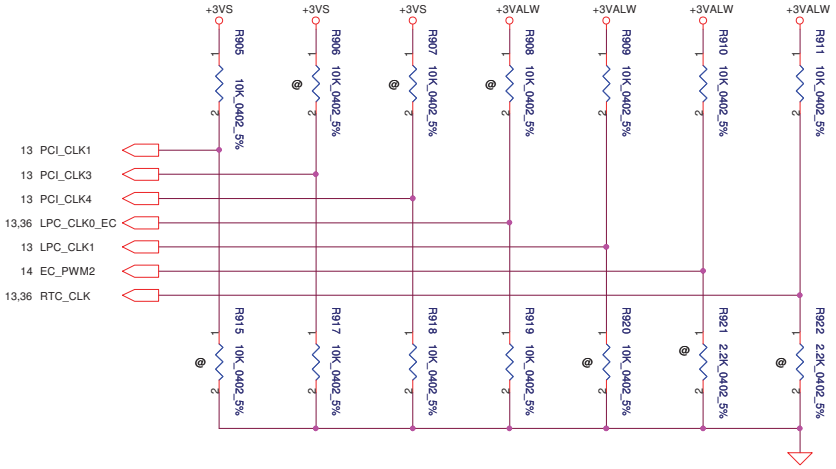
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

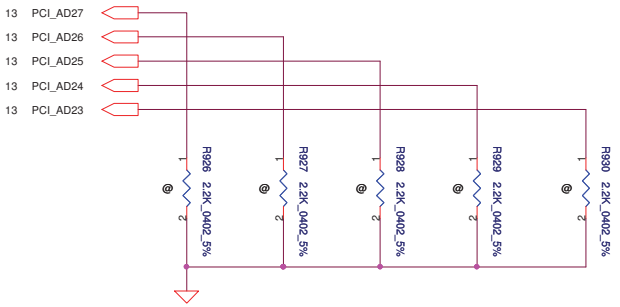


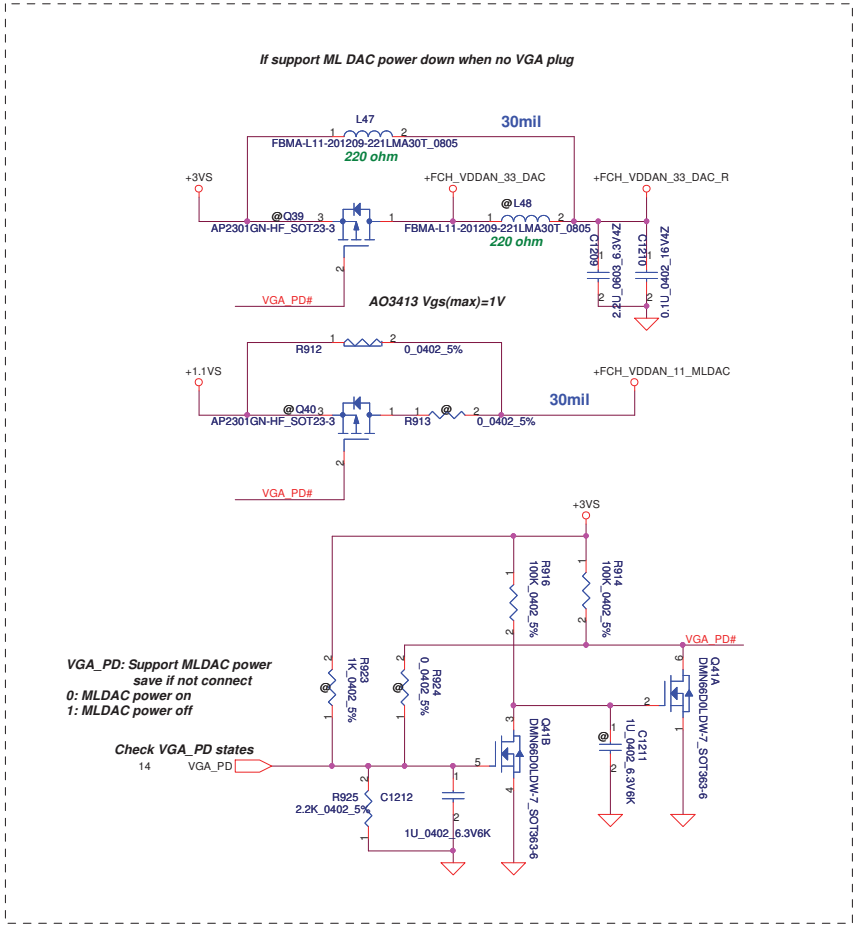
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

PCI_AD26

	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 16 of 53

C1218 / C1219 / C1247 Change to SE00000I10
20101228

VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

LDO_CAP: Internally generated 1.8V supply for the RGB outputs

For A11: Cap = 1nF
For A12, Cap = DNI

R1242 change to 2.2uf-AMD request
20110212

change to 0ohm-AMD request
20110212

change to four 1uf-AMD request
20110212

For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S
Connected to VSS.

AMD reply:
VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3/1.5V_S5 rail if Wake on Ring is supported

Connected to VSS through a dedicated via.

Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

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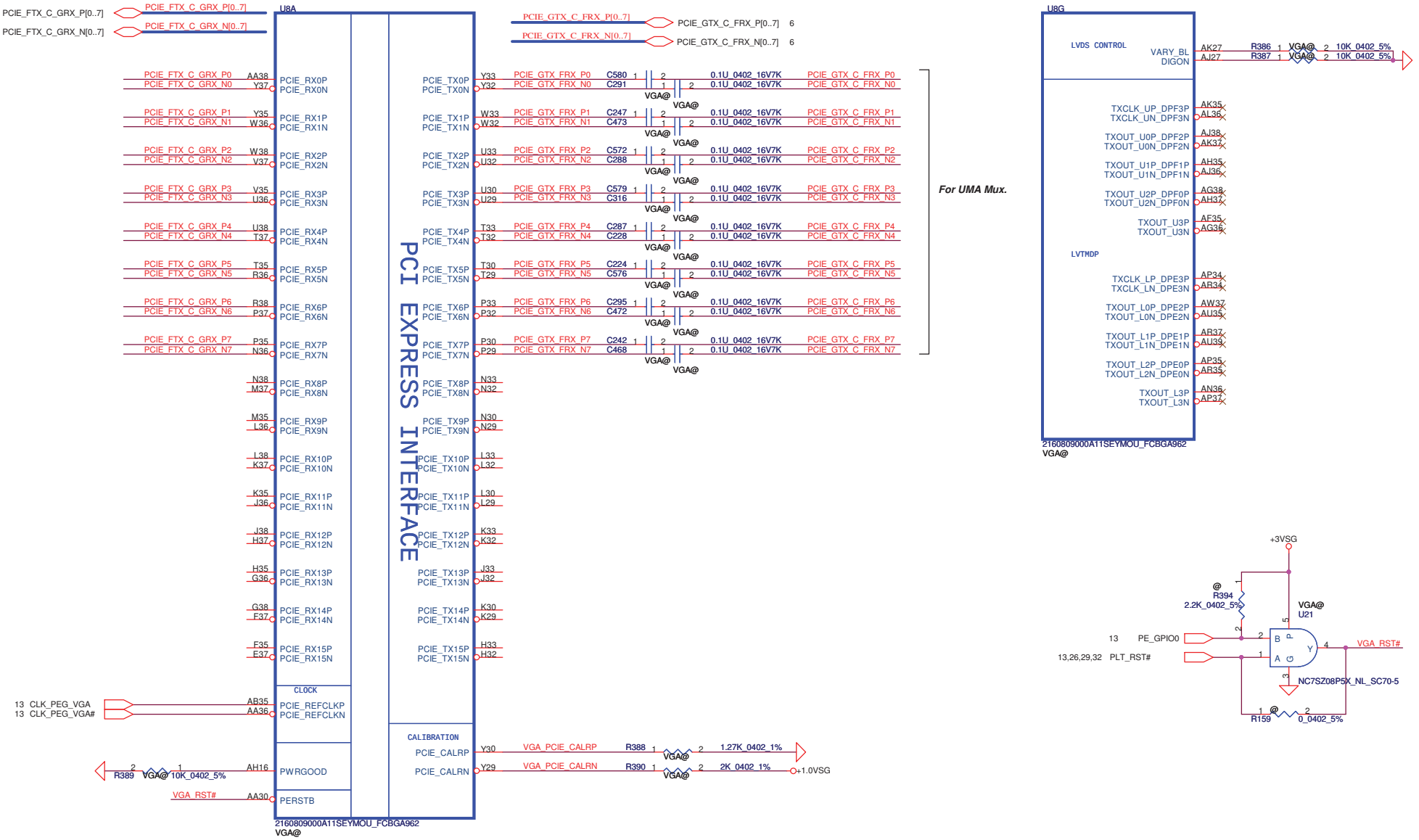
GFX PCIE LANE REVERSAL

<DIGON>
Controls panel digital power on/off.
Active High ,external PD need

<VARY_BL>
LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines CONFIG[3:0] the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines 256 MB 001 * the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	00
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour

Not share via for other GND

VRAM ID

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004GS30 64M16x8 K4W1G1646G-BC11	0	0	0	0
Samsung SA00004TA0 128M16x8 K4W2G1646C-HC11	0	0	0	1
Hynix SA00004IS60 64M16x8 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16x8 H5TQ2G63BFR-11C	0	1	0	1

GPIO5 fast-power reduction:
HW control will casue display disturb should use SW method control
GPIO6 voltage control signal ,No use can NC

Move to DDCCLK_AUX3P,DDCDATA_AUX3N,

GPIO7 Controls backlight on/off.
Active High ,need external PD
If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt
Critical temperature fault
Reserved

External BIOS device
ON(1)/OFF(0) inter PD
Internal Debug
no use can floating
ON(1)/OFF(0)
Stereo Sync
no use can NC
For ATI Cross fire
no use can NC

Future ASIC call MLPS.
OLD ASIC is Fan PWM

External VGA Thermal Sensor

ADM1032ARMZ-2REEL_MSOP8

Q8A DMN66D0LDW-7_SOT363-6

Q8B DMN66D0LDW-7_SOT363-6

HSYNC:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

GPIO8 Serial-ROM output from ROM. GPIO9 Serial-ROM input to ROM. GPIO10 Serial-ROM clock to ROM. GPIO22 erternal BIOS-ROM enable	if GPIO22 High ,GPIO 11-13->CFG[0:2] Config ROM type ,GPU has internal PD if GPIO22 Low ,GPIO 11-13->CFG[0:2] Config Primary memory-aperture size CFG[3:0] 128MB 000 256MB 001 * 64MB 010
GPIO8,GPIO9,GPIO10 no use can NC GPIO22 Enable need 3K PH ,no use must NC	

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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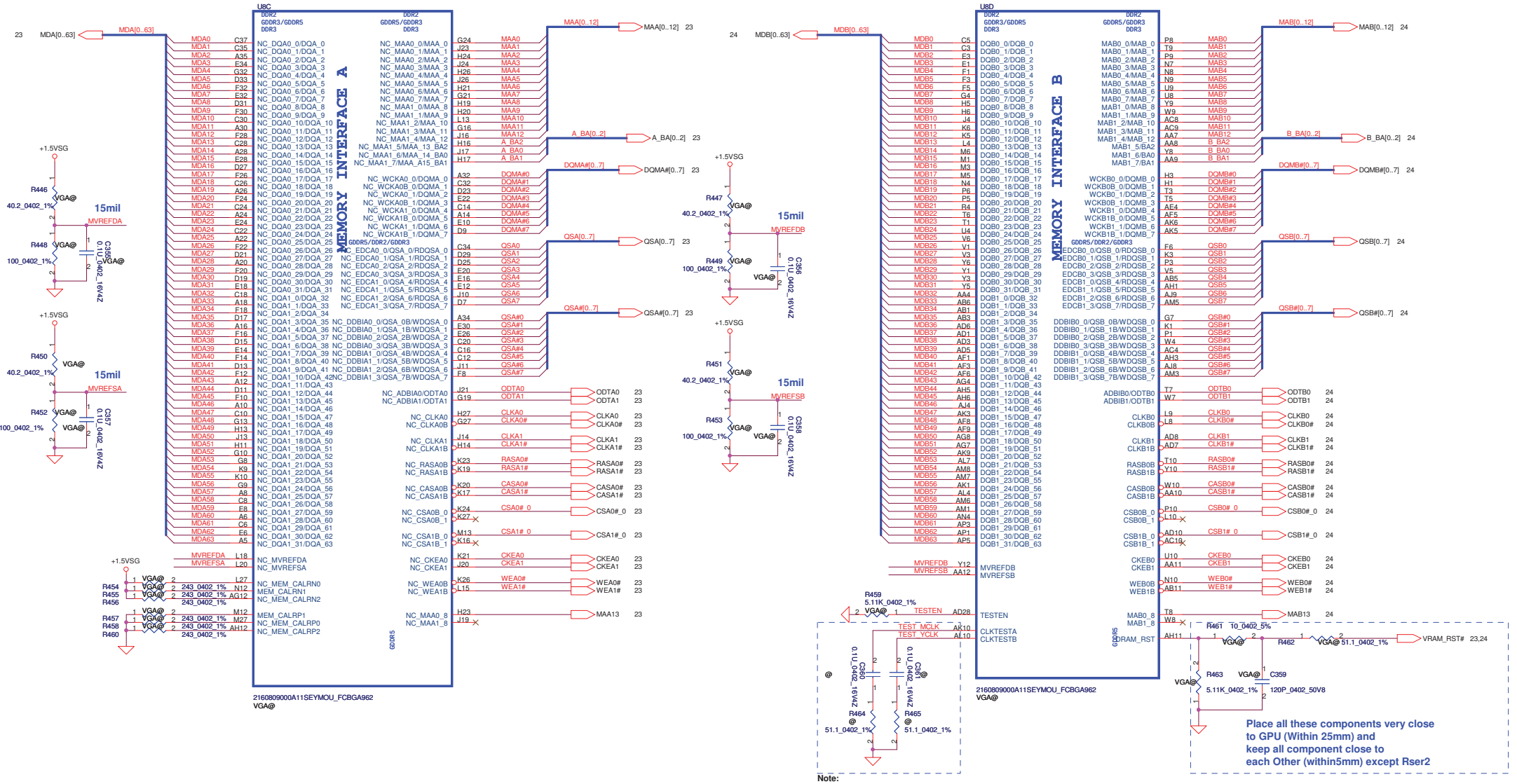


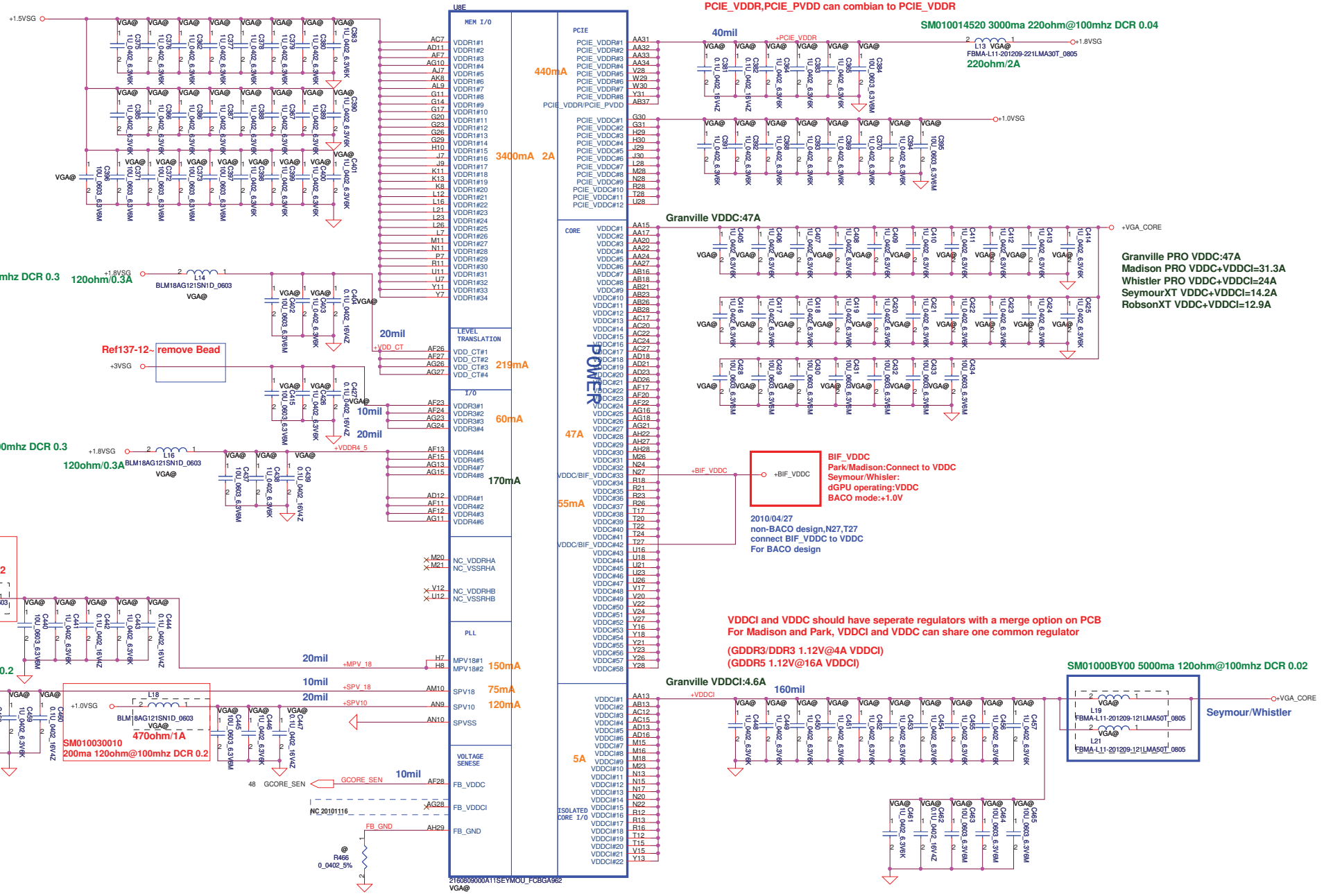
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Vancouver_Memory

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 Sheet 20 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title	Vancouver_Power/GND	
Size: Custom	Document Number: QBL50 LA-7551P	Rev: 1.0
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DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

GND

216080900 0A11SEYMOU_FCBGA962
VGA@

REF137-13 update

U8H

Manhatann:300mA
Seymour:150mA

Manhatann:220mA
Seymour:110mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
FootPrint

DP mode:300mA
LVDS mode:440mA

DP mode:220mA
LVDS mode:240mA

PX_EN 25,36
PX_EN: PU at P.20
SBIOS will control VGA power on/off.
High :BACO mode enable
LOW:BACO disable

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

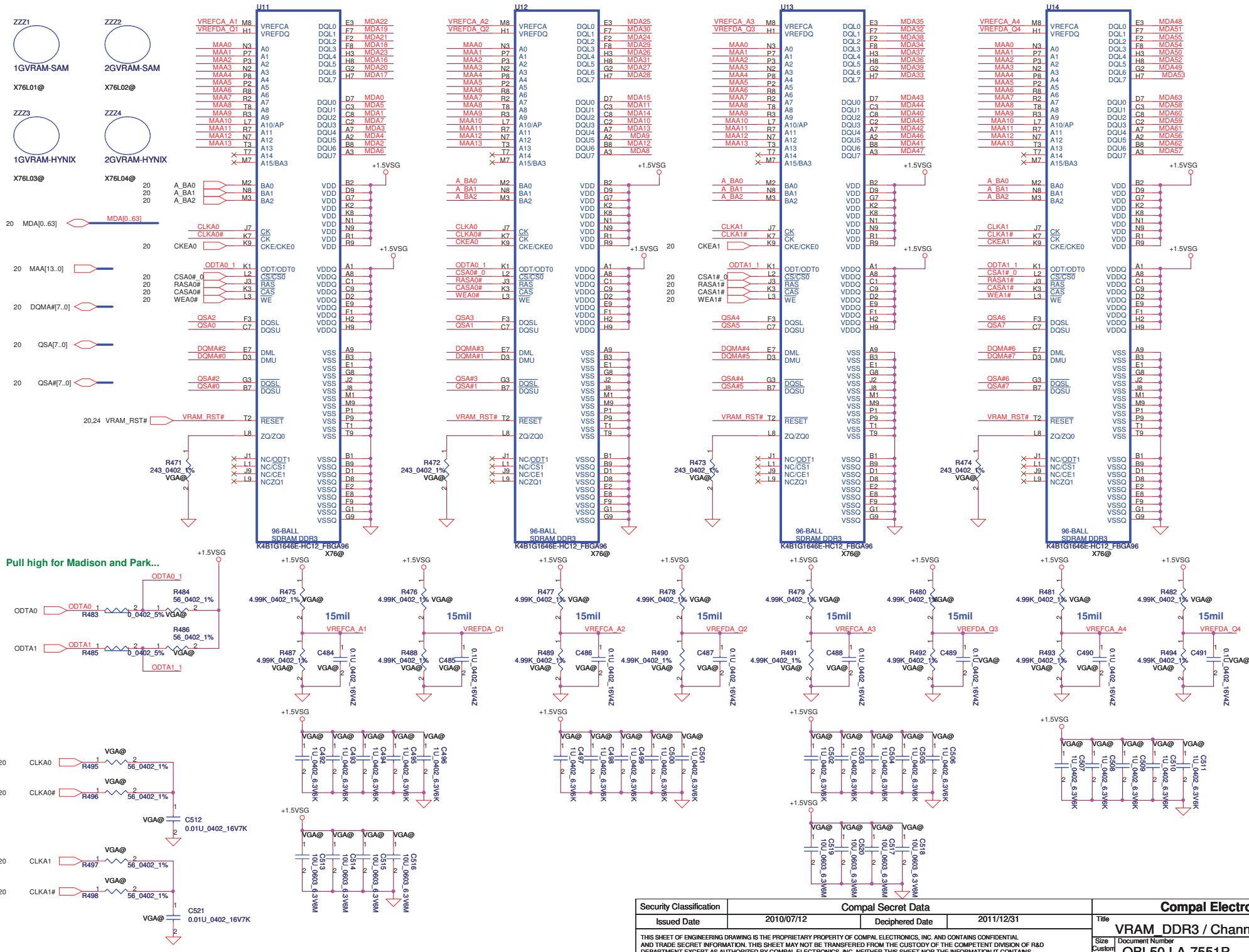
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 22 of 53



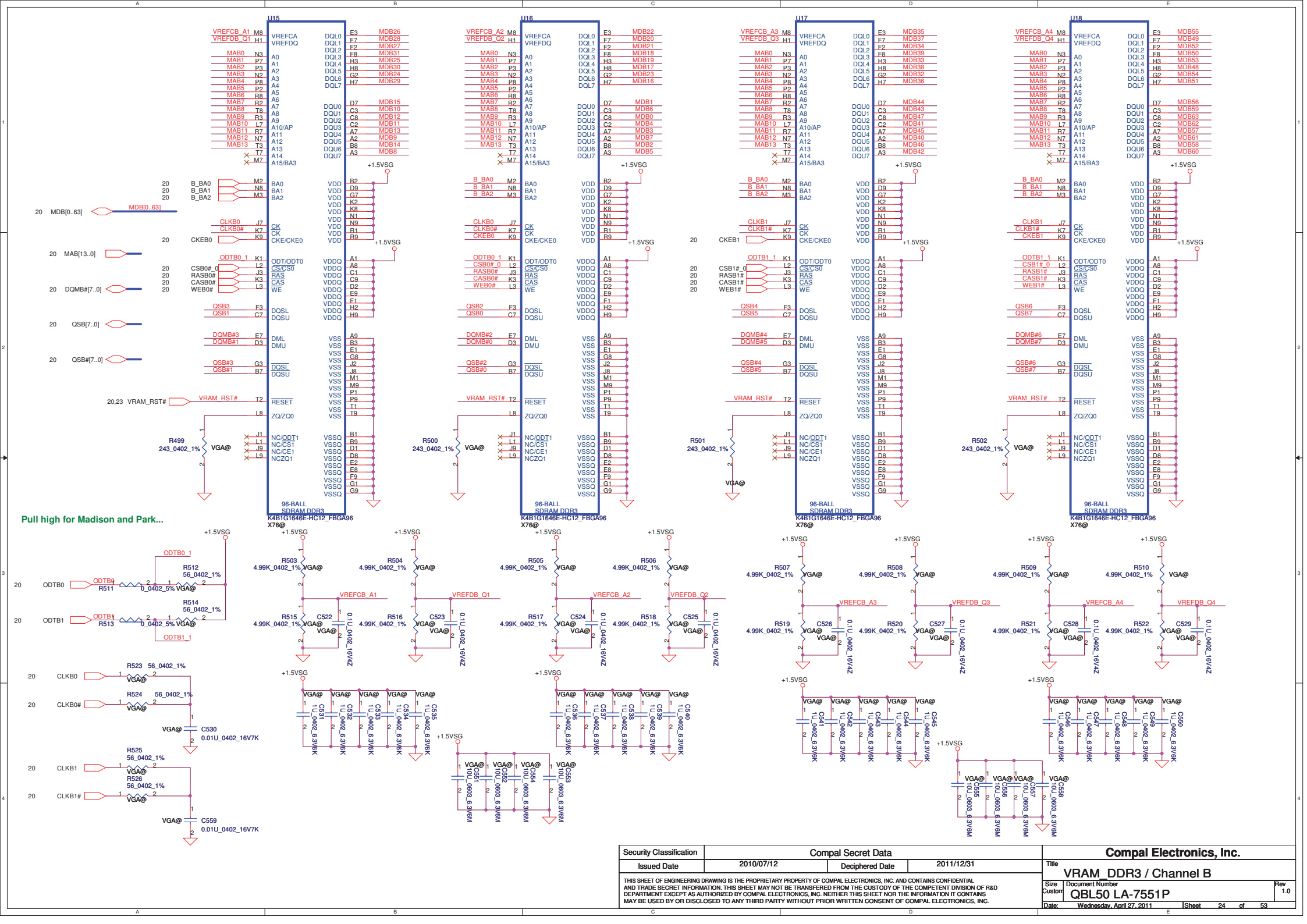
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 | Sheet 23 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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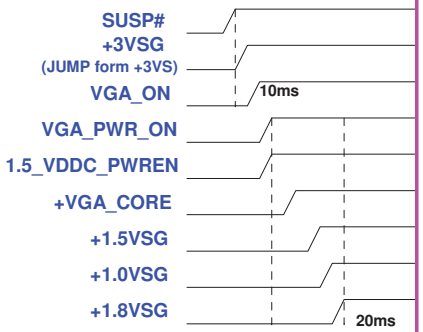
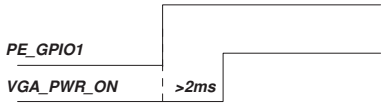
Power Sequence of Whistler and Seymour

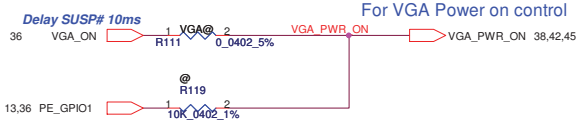


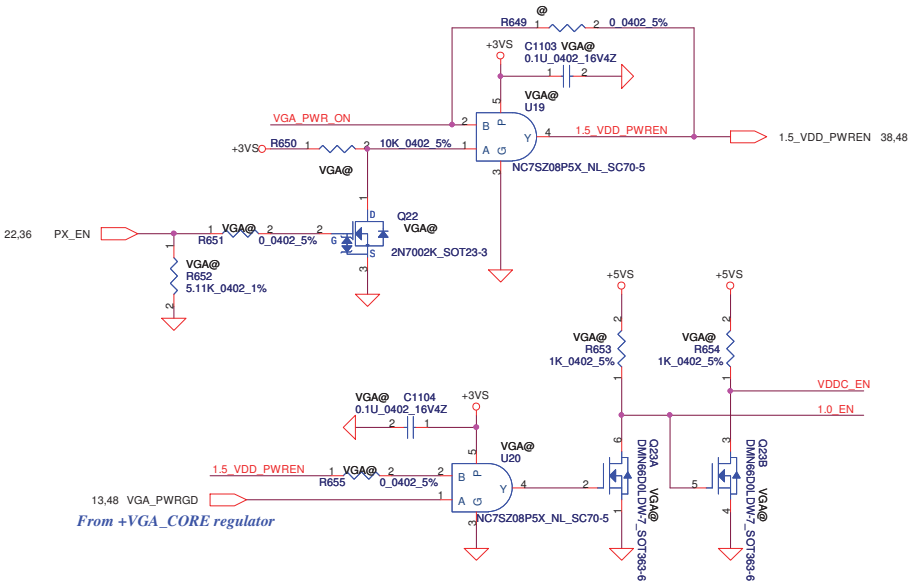
For PX sequence, >2mS delay is required between PE_GPIO1 and VGA_PWR_ON

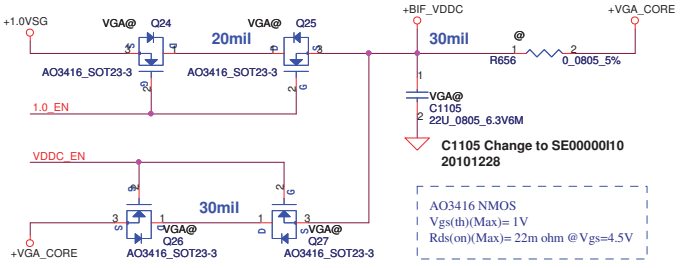


VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table	
	Whislter
VGA_PWR_ON source signal	VGA_ON
+3.3VSG	SUSP#
+1.8VSG	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON
+VDDCI	Combine with +VGA_CORE
+VGA_CORE	1.5_VDDC_PWREN
+1.5VSG	1.5_VDDC_PWREN







Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: VGA power sequence and BACO

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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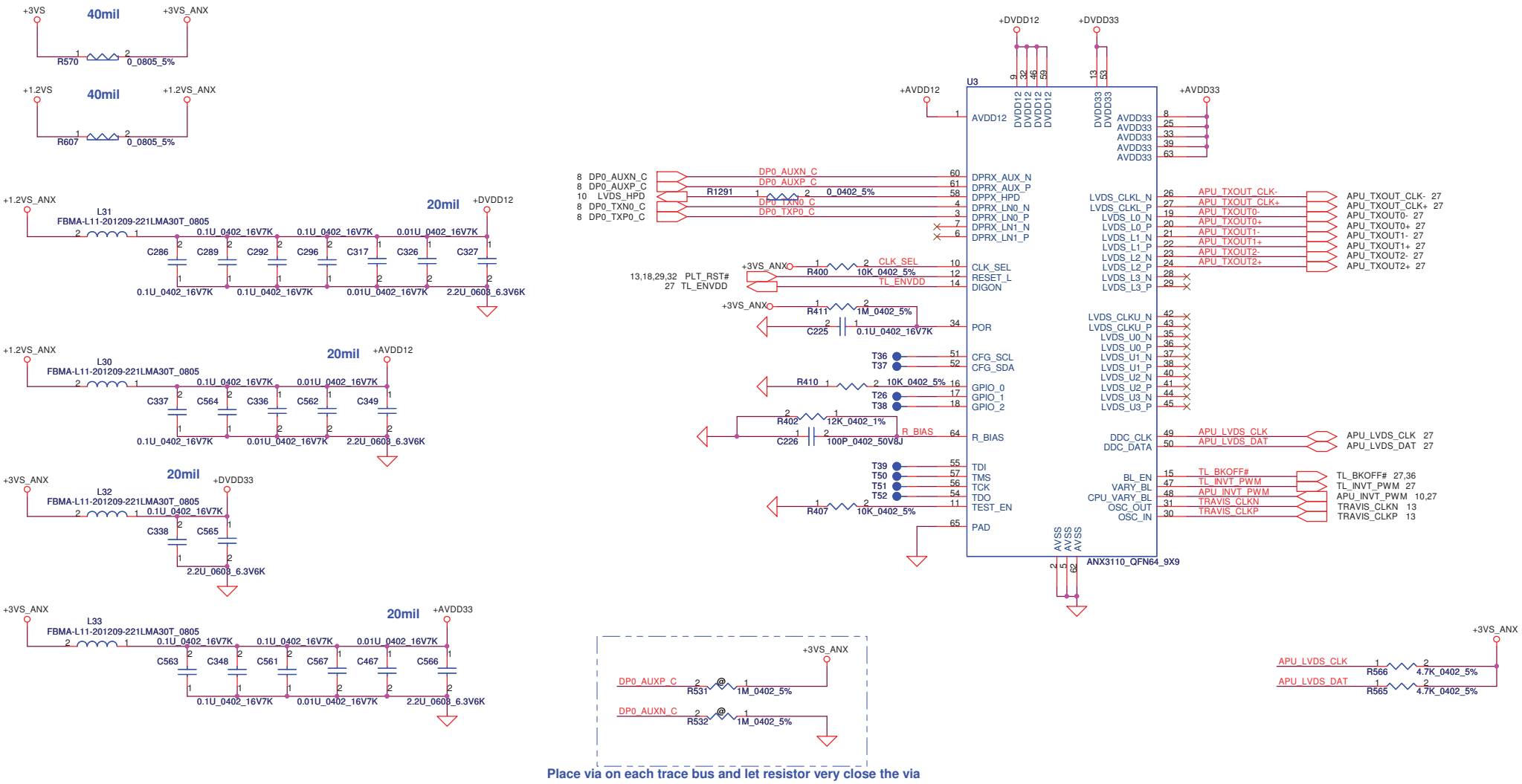

Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: ***LVDS Translator-ANX3110***

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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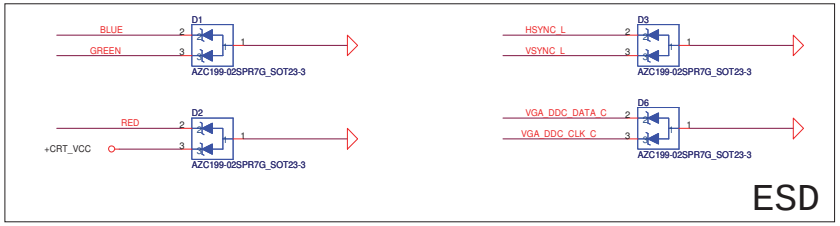
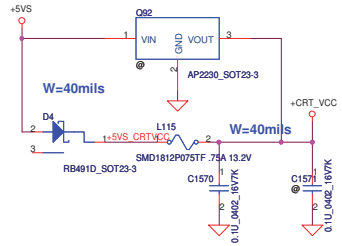
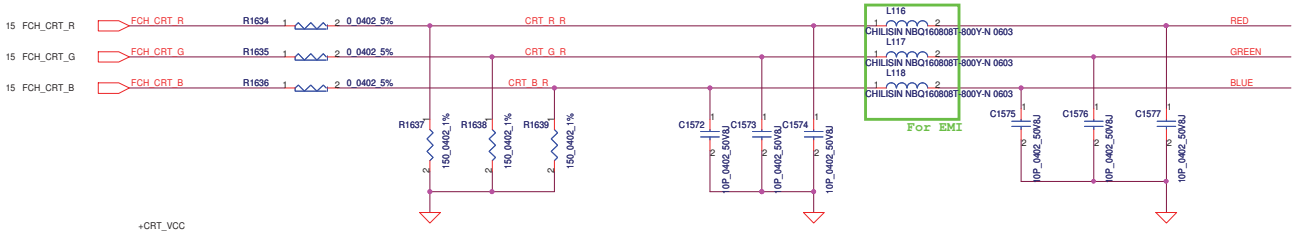
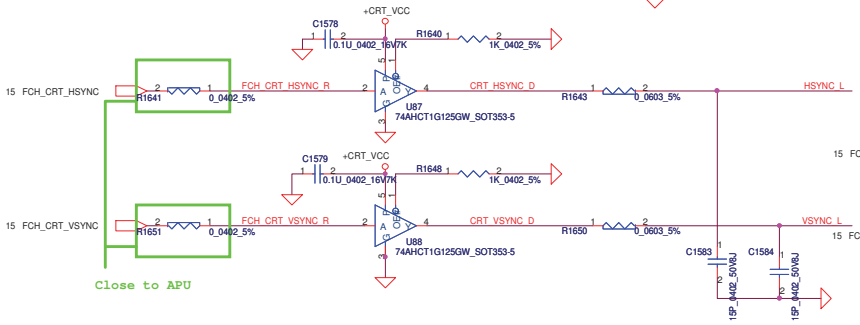
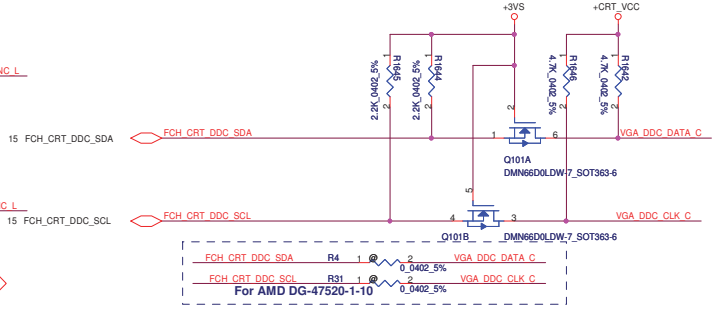
CRT

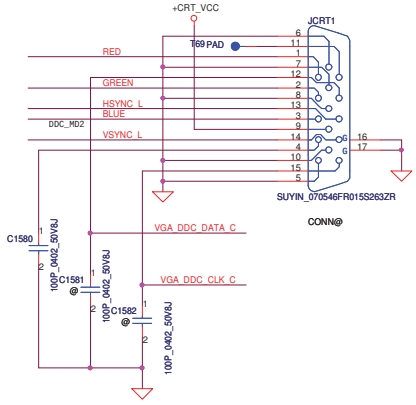




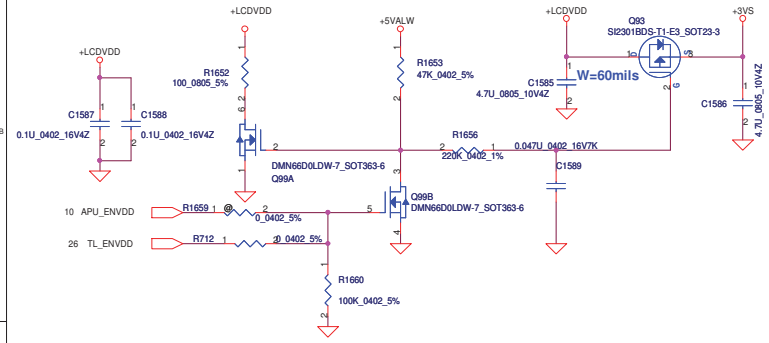




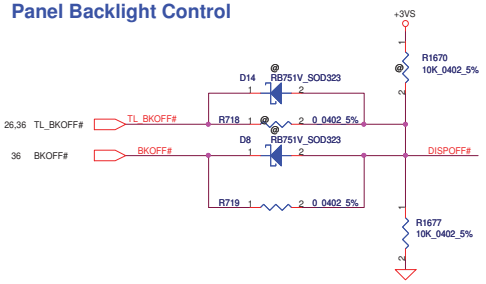




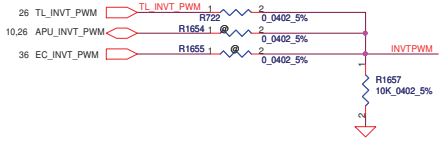
Panel LCDVDD Control

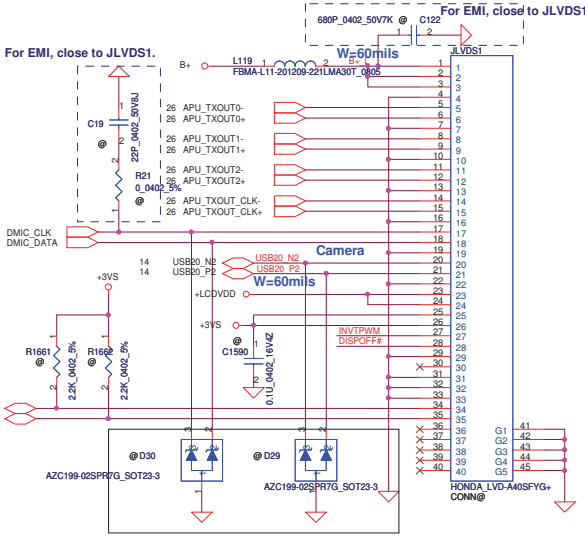


Panel Backlight Control



Panel PWM Control





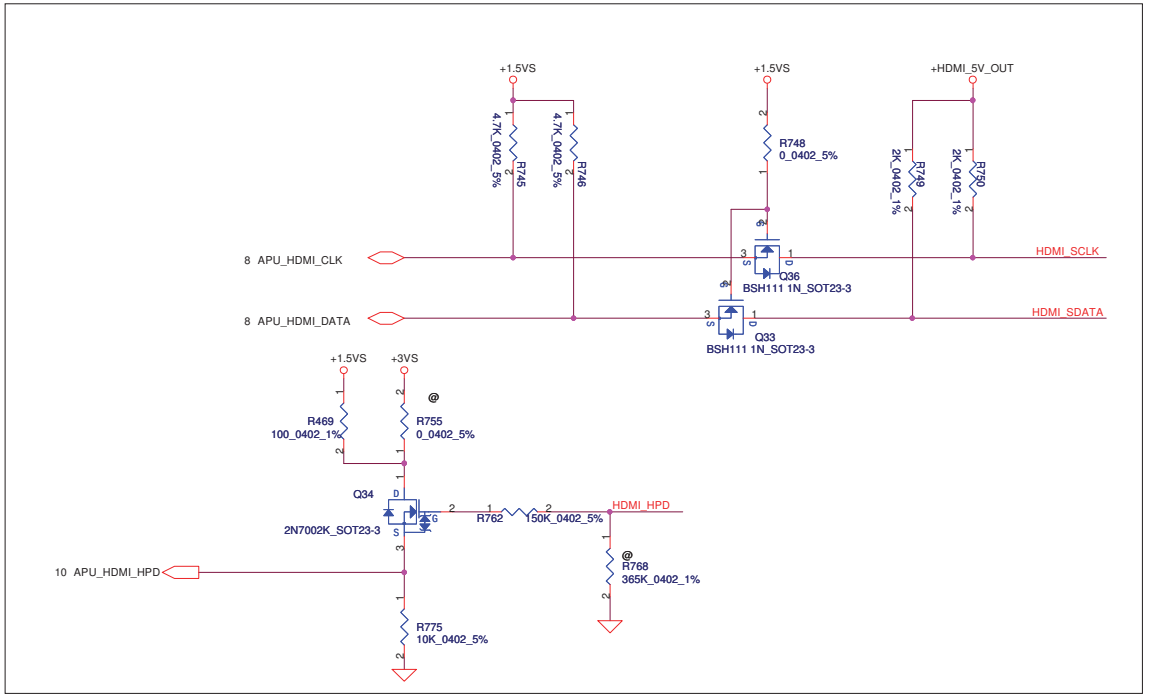
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

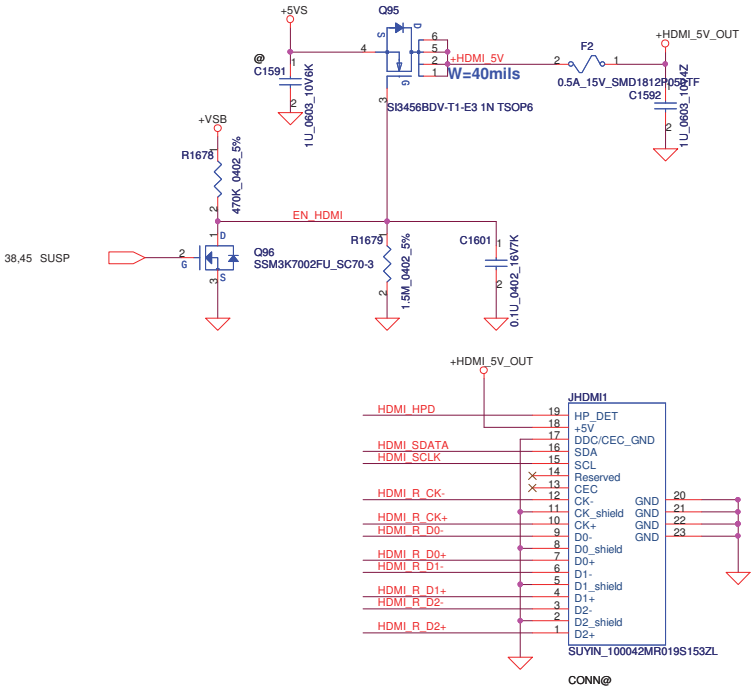
Compal Electronics, Inc.

Title: P10-LVDS/CRT CONN

Size	Document Number	Rev
C	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 Sheet 27 of 53

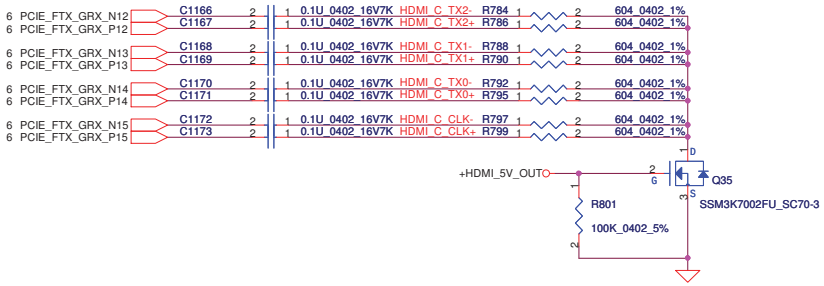


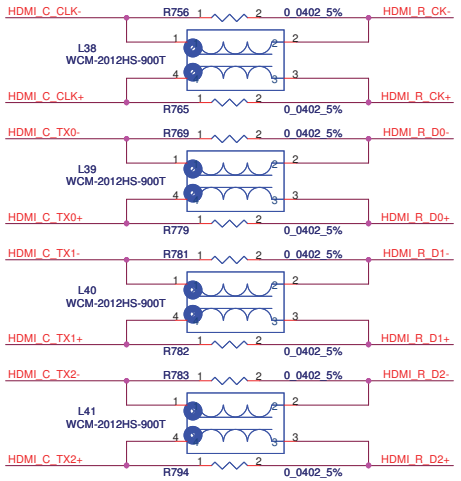


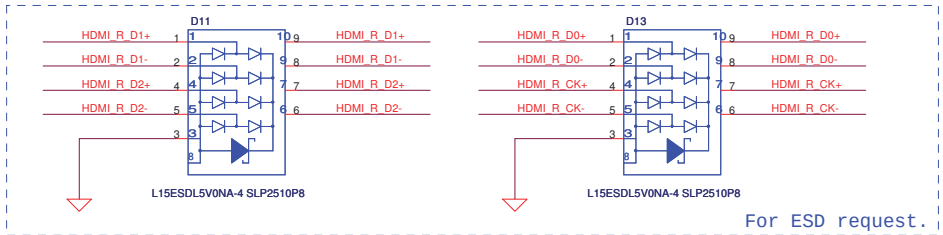
From APU

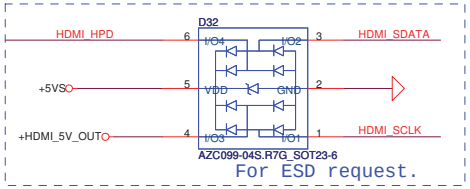
Near the connector

UMA use 604 ohm
VGA use 499 ohm









Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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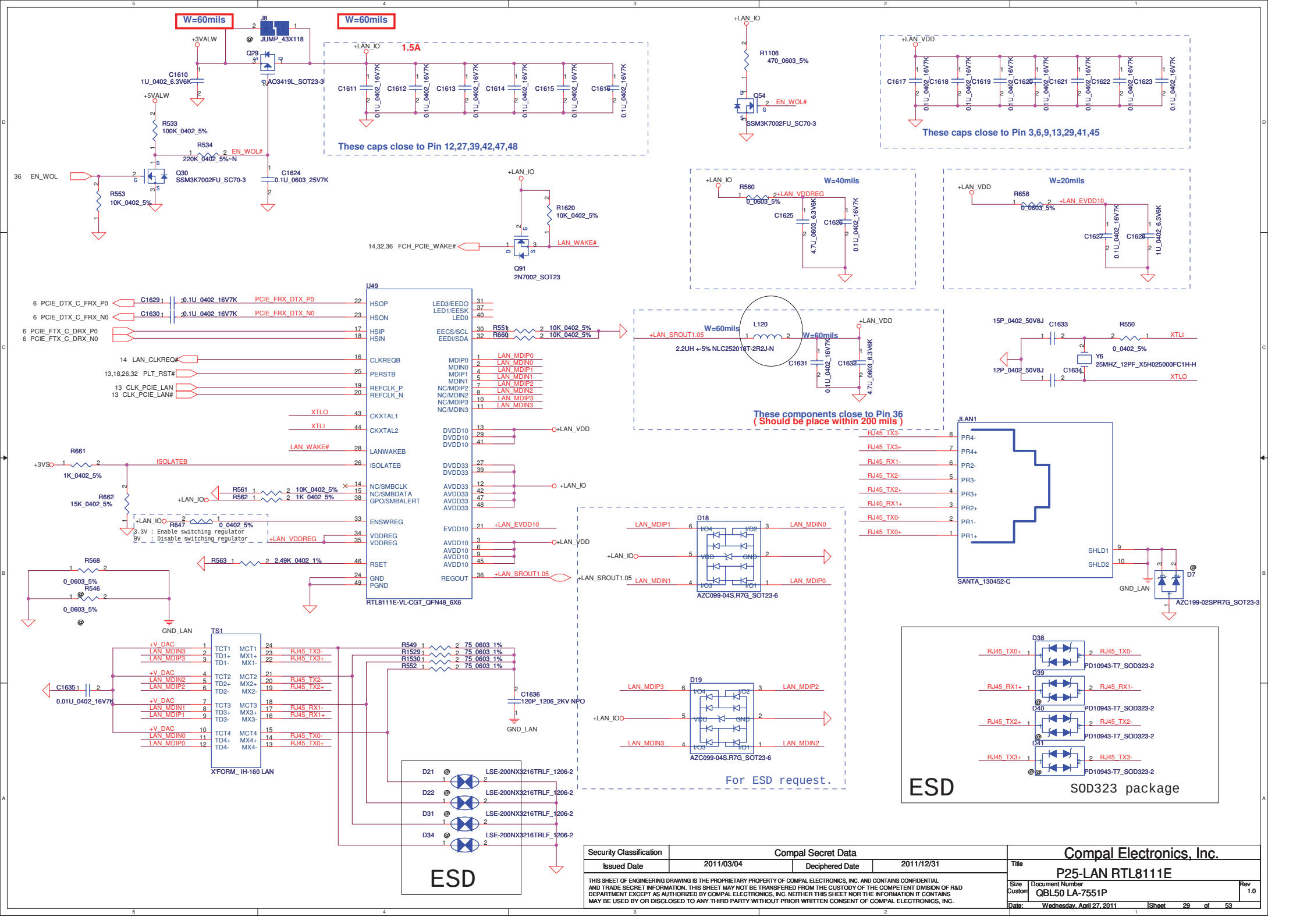
W=60mils
W=60mils
1.5A
+3VALW
+5VALW
+LAN_IO
+LAN_VDD
JUMP_43X118
AO3419L_SOT23-3
SSM3K7002FU_SC70-3
These caps close to Pin 12,27,39,42,47,48
These caps close to Pin 3,6,9,13,29,41,45
EN_WOL
EN_WOL#
LAN_WAKE#
FCH_PCIE_WAKE#
2N7002_SOT23
W=40mils
W=20mils
+LAN_EVDD10
+LAN_VDDREG
W=60mils
2.2UH +-5% NLC252018T-2R2J-N
These components close to Pin 36
(Should be place within 200 mils)
RTL8111E-VL-CGT_QFN48_6X6
3.3V : Enable switching regulator
0V : Disable switching regulator
SANTA_130452-C
AZC199-02SPR7G_SOT23-3
AZC099-04S.R7G_SOT23-6
X'FORM_IH-160 LAN
LSE-200NX3216TRLF_1206-2
For ESD request.
ESD
SOD323 package
PD10943-T7_SOD323-2
Compal Secret Data
2011/03/04
2011/12/31
Compal Electronics, Inc.
P25-LAN RTL8111E
QBL50 LA-7551P
Wednesday, April 27, 2011
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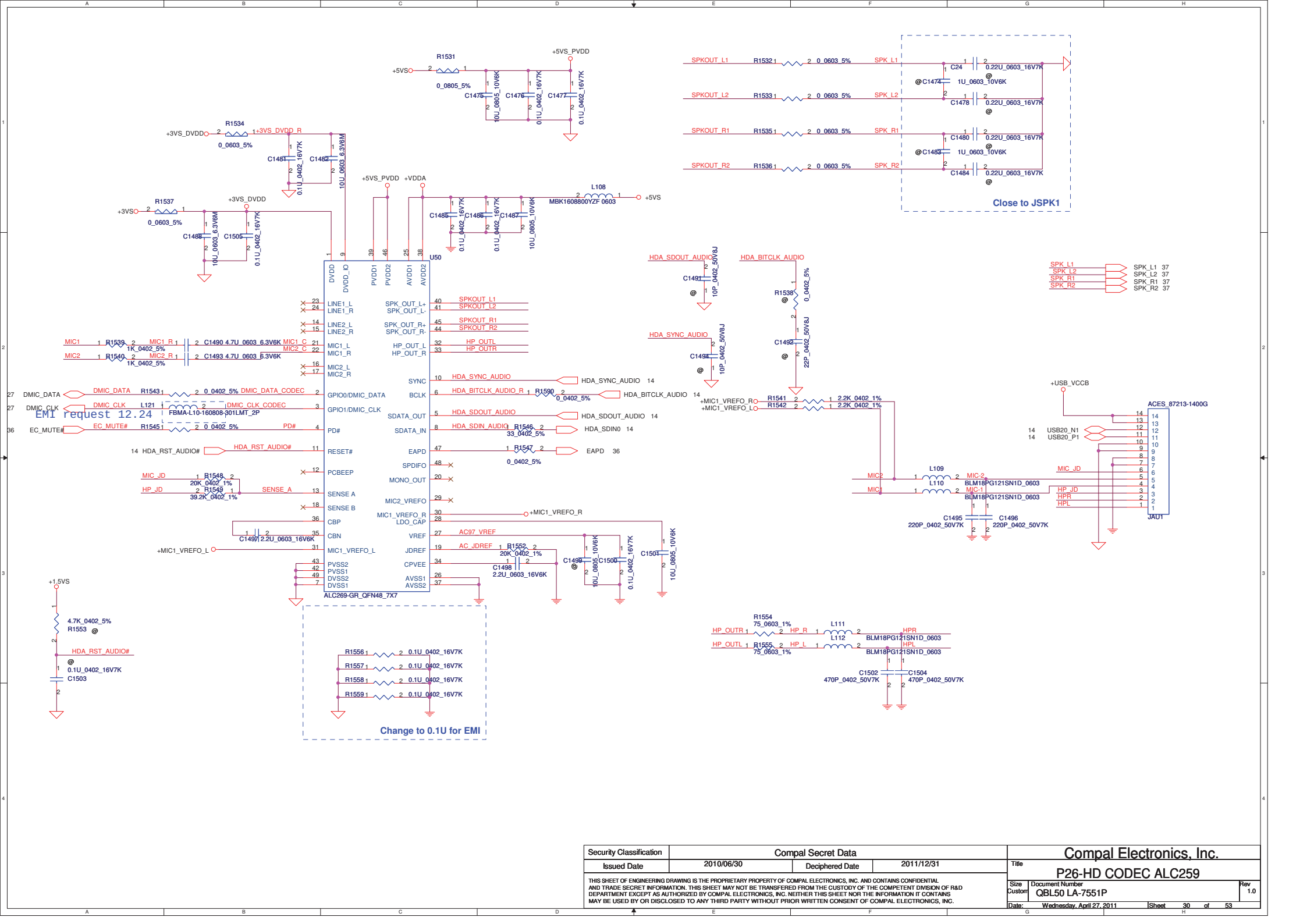

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P26-HD CODEC ALC259

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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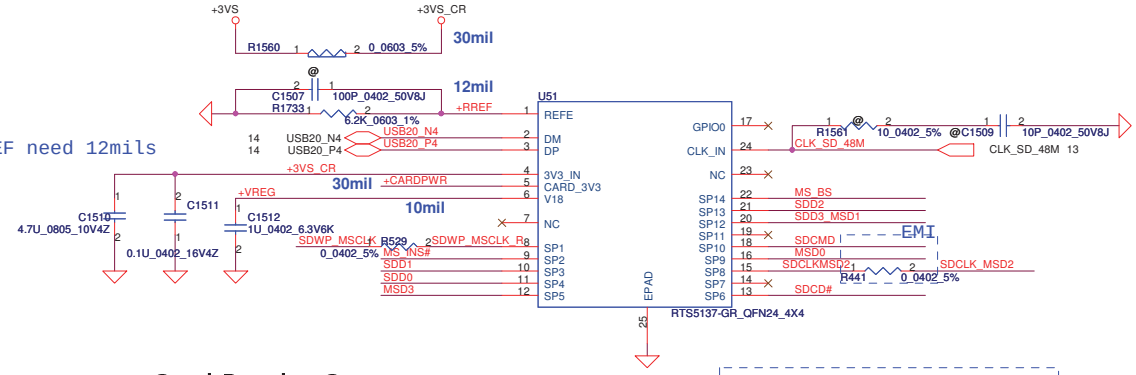
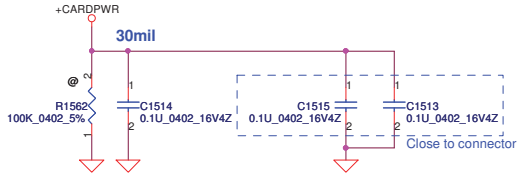
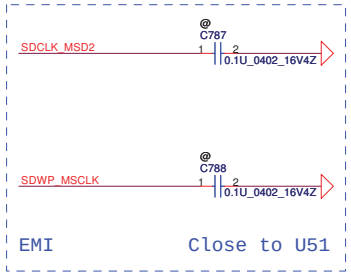
Card Reader RTS5137
(only SD/MMC/MS function)

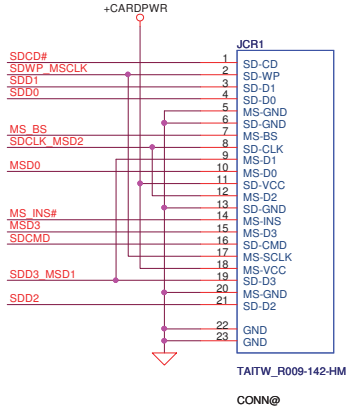
+RREF & +VREF need 12mils



Card Reader Connector







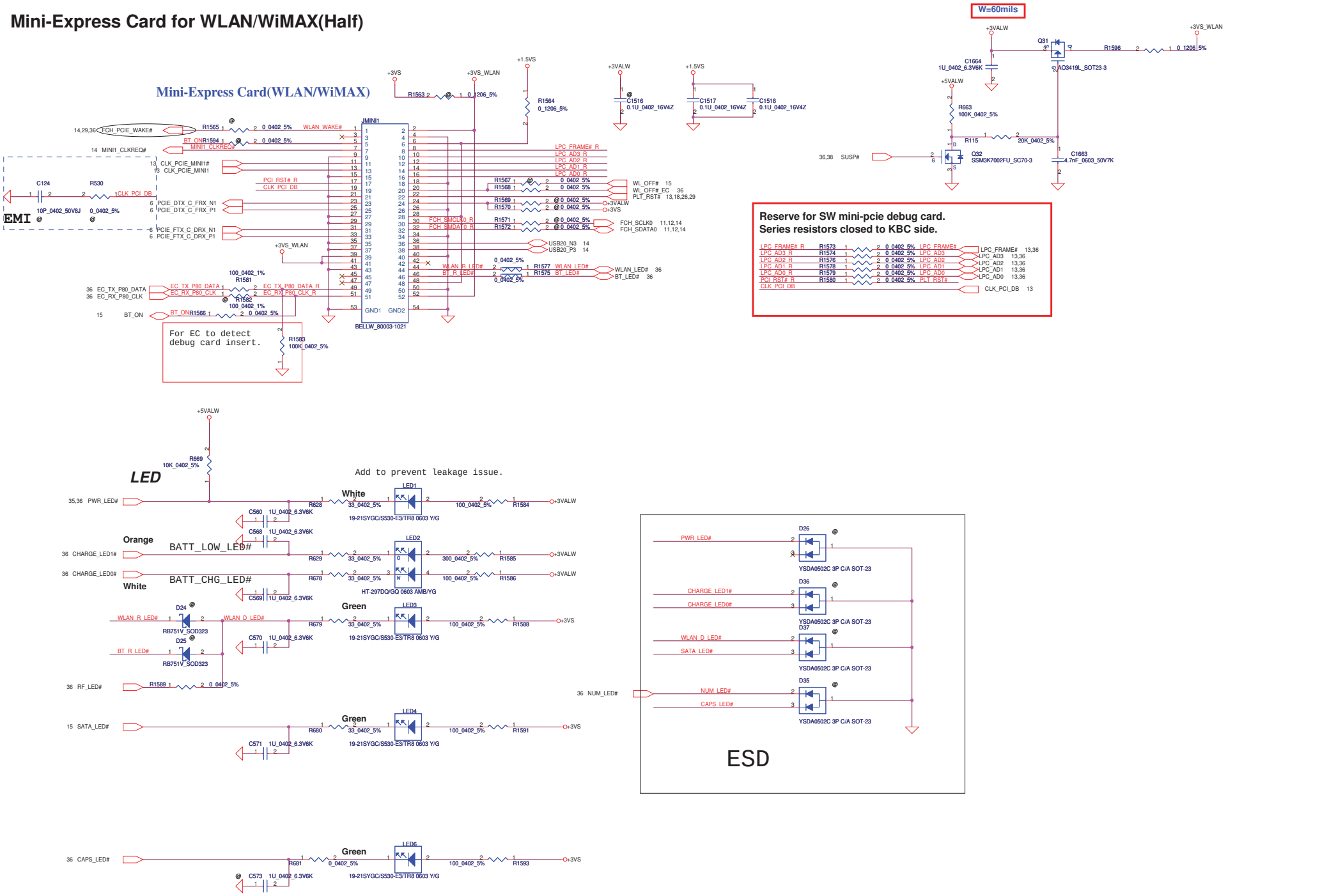
Compal Electronics, Inc.

Title: P27-RTS5137 Media Card Controller

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 Sheet 31 of 53

Mini-Express Card for WLAN/WiMAX(Half)

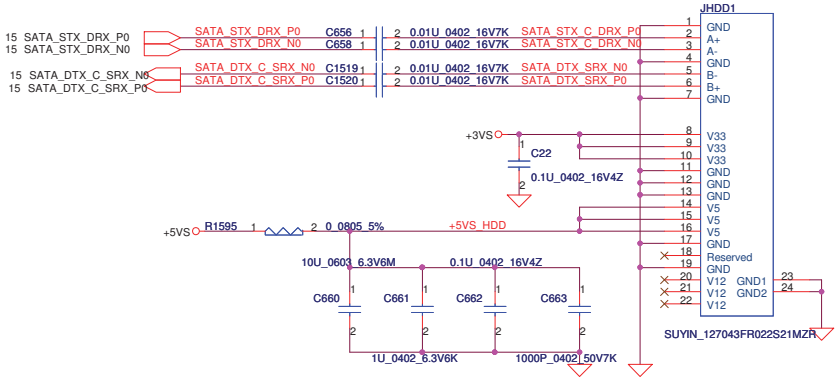


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

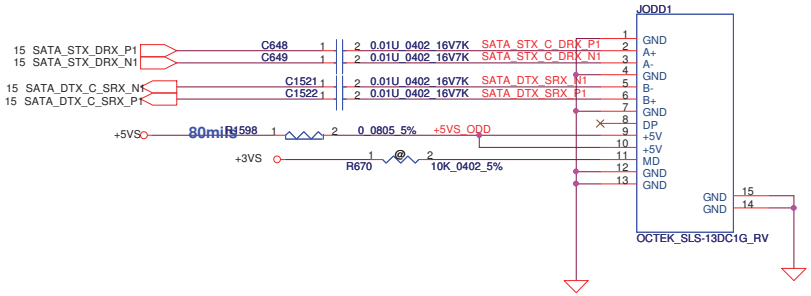
Compal Electronics, Inc.

Title	P28-Mini PCIE/LED	
Size	Document Number	Rev
	QBL50 LA-7551P	1.0
Date: Wednesday, April 27, 2011	Sheet 32 of 53	

SATA HDD Conn.



SATA ODD FFC Conn.



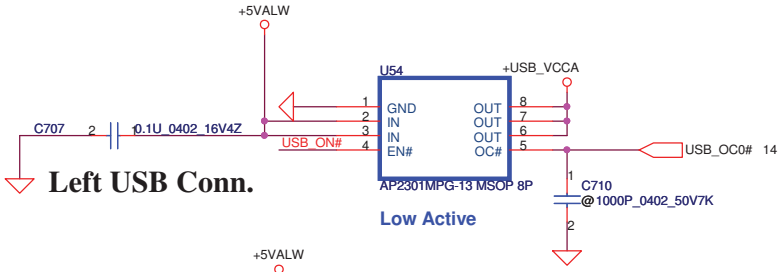
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

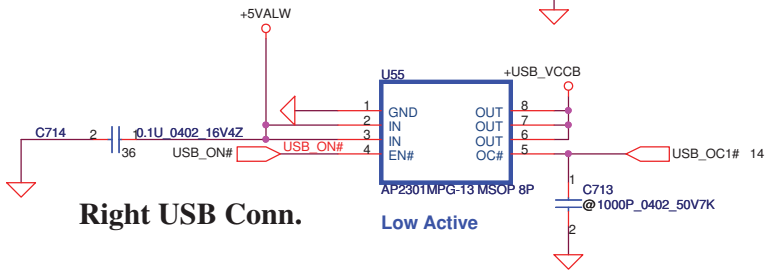
Compal Electronics, Inc.

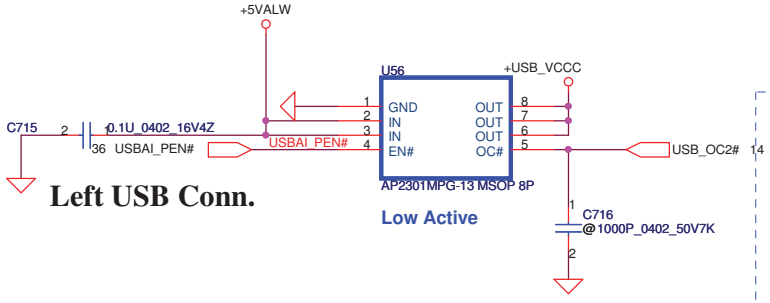
Title: P29-HDD & ODD CONN

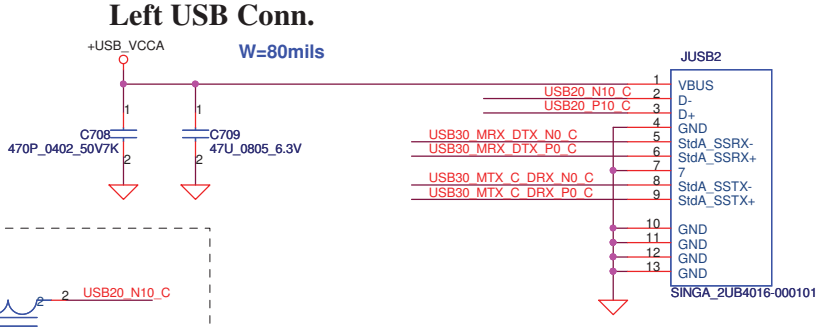
Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 33 of 53

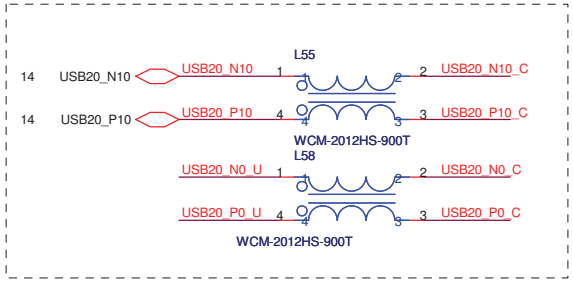


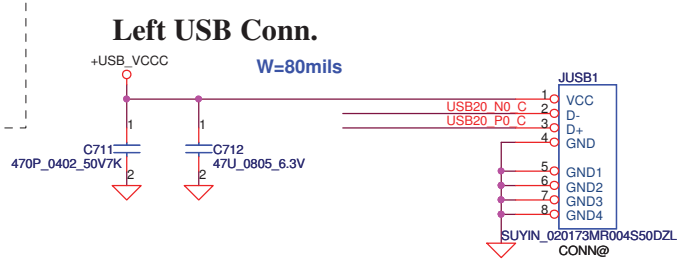


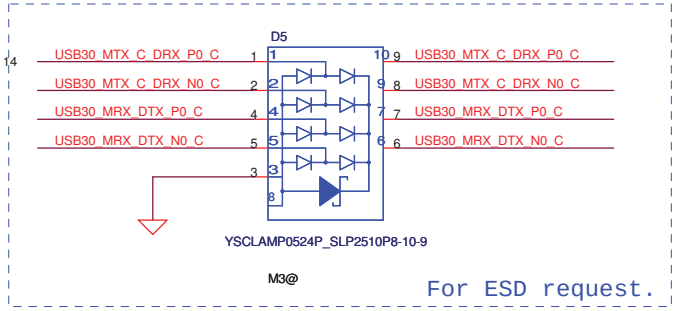


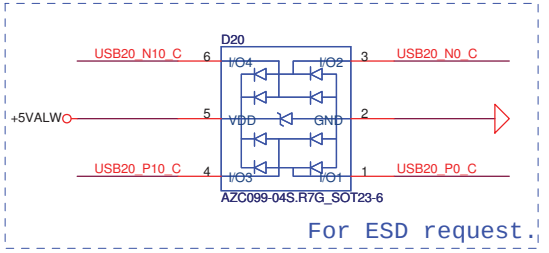


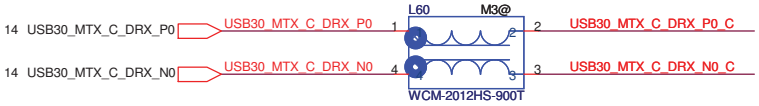
EMI request

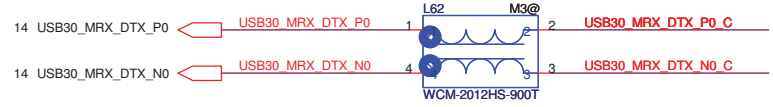




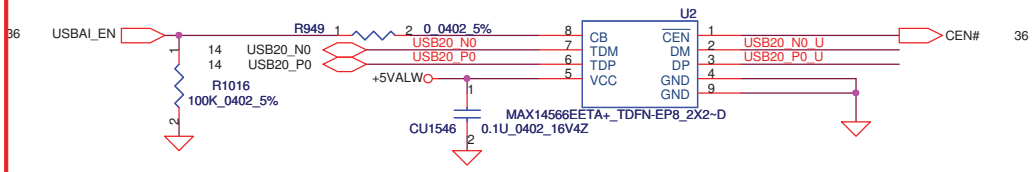








AI CHARGER

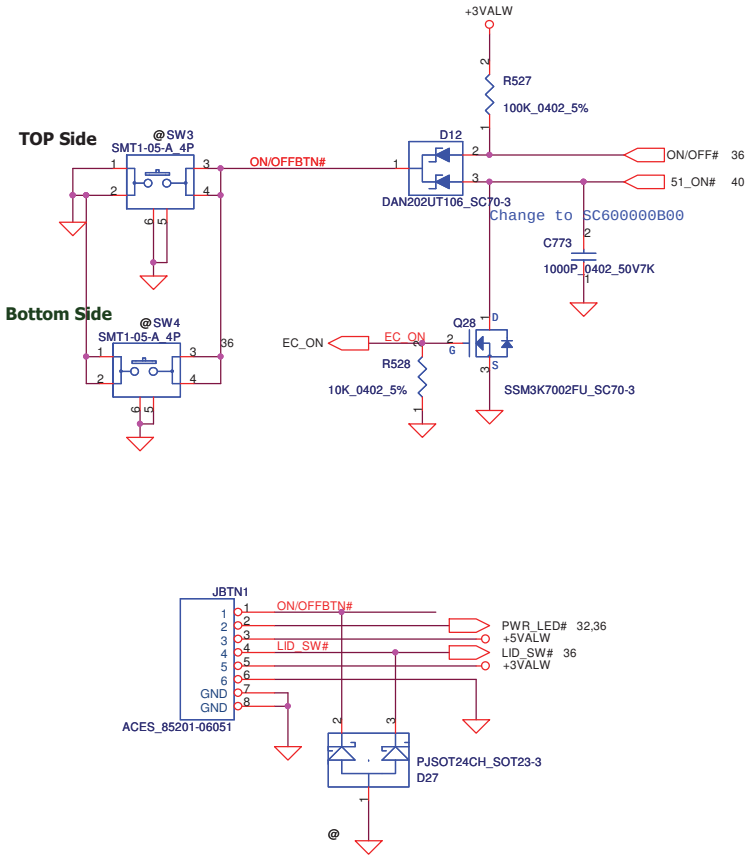


CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

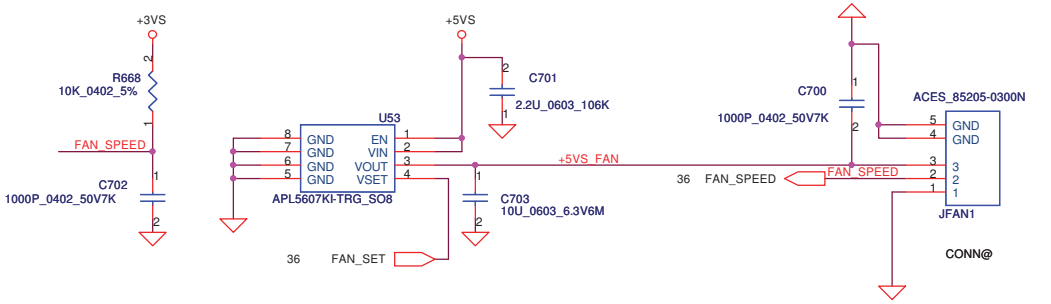
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

Compal Electronics, Inc.	
Title	P32-USB/BT/USBsub
Size: Custom	Document Number: QBL50 LA-7551P
Rev	1.0
Date: Friday, April 29, 2011	Sheet 34 of 53

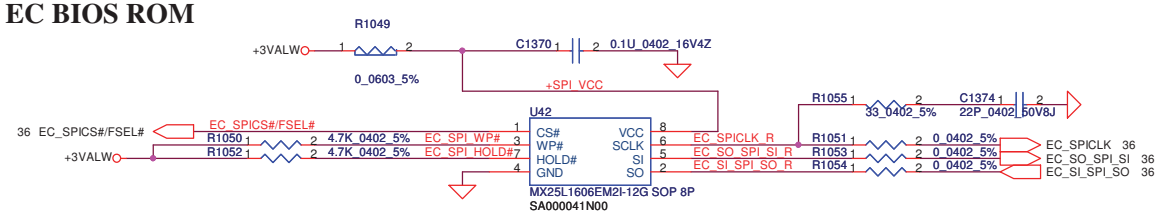
ON/OFF switch **Power Button**



Fan Control Circuit



EC BIOS ROM



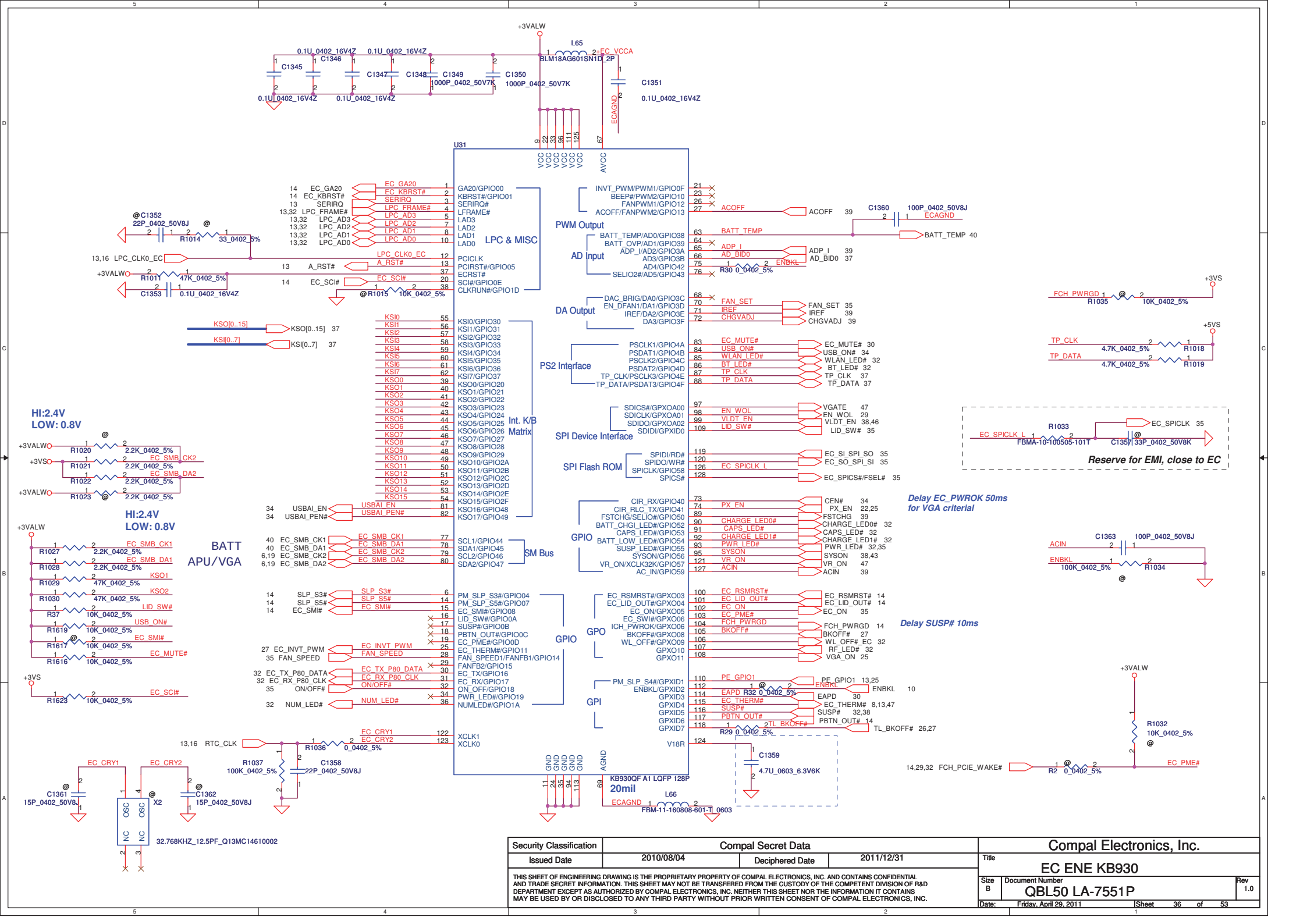
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P31-KB /SW/TP/Lid

Size: B | Document Number: QBL50 LA-7551P | Rev: 1.0

Date: Wednesday, April 27, 2011 | Sheet 35 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

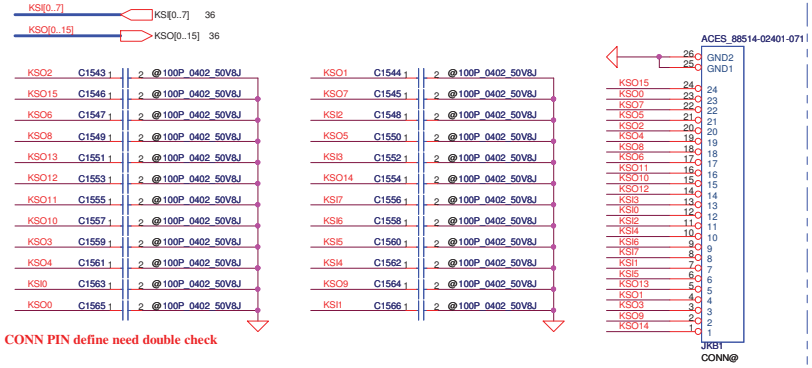
Compal Electronics, Inc.

Title: EC ENE KB930

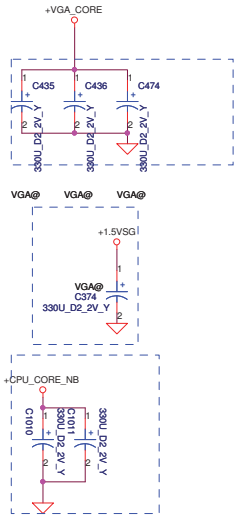
Size	Document Number	Rev
B	QBL50 LA-7551P	1.0

Date: Friday, April 29, 2011 Sheet 36 of 53

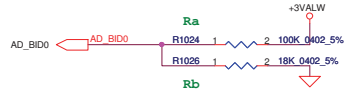
INT_KBD Conn.



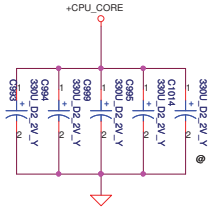
CONN PIN define need double check



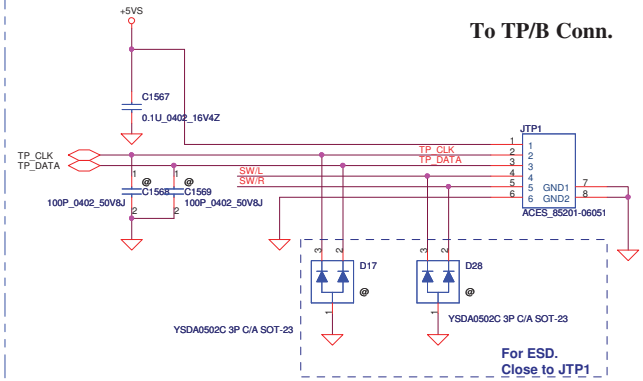
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R10 MP	100K	18K	0.5V
3	Reserve	100K	33K	0.82V

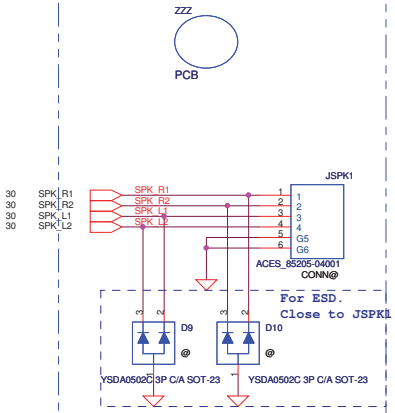


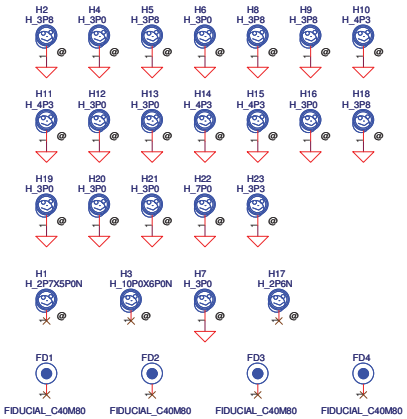
P9 FS1 PWR/GND



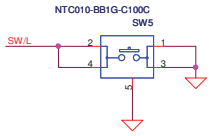
To TP/B Conn.



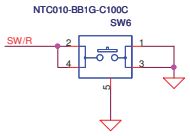


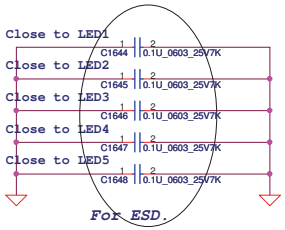


Left side Button



Right side Button





Note: Differential page:
P1,P2,P9,P29,P37
And Power schematic.

Security Classification	Compal Secret Data		
Issued Date	2011/03/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: P33-Other IO/USB (right)

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

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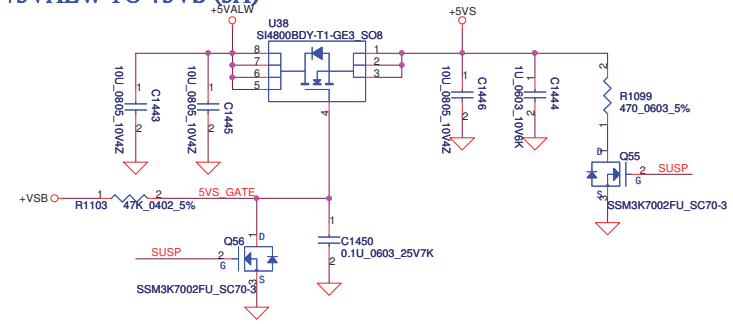
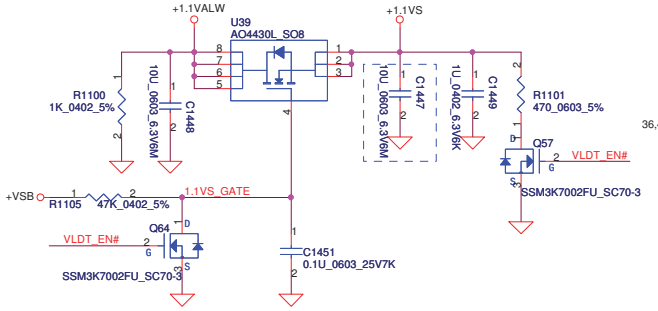
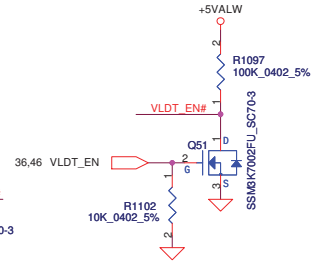
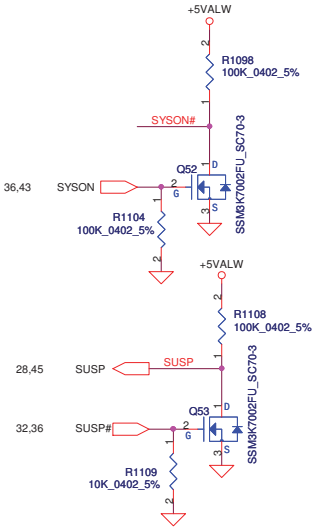
+5VALW TO +5VS (5A)



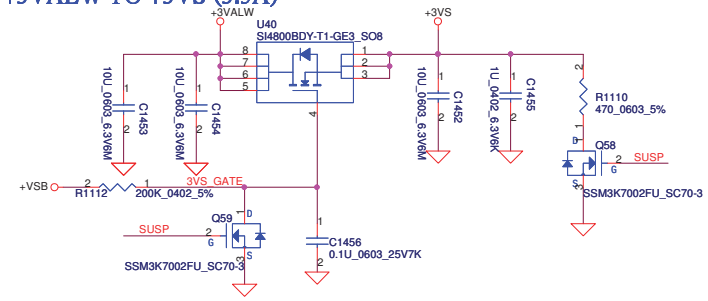
+1.1VALW TO +1.1VS (1.1A)



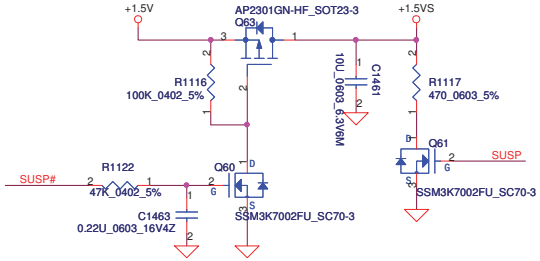




+3VALW TO +3VS (3.3A)

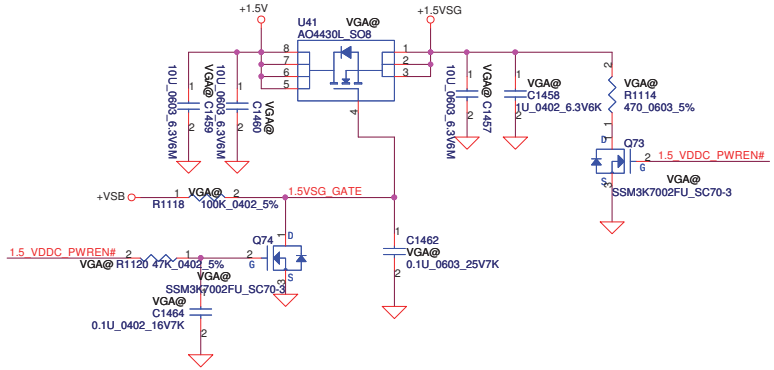


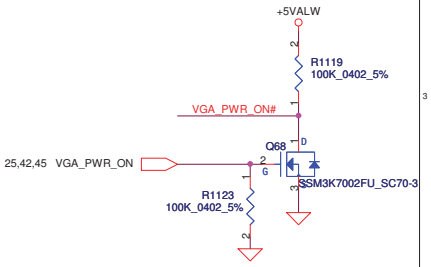
+1.5V TO +1.5VS (1.5A)



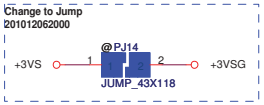
VGA Power

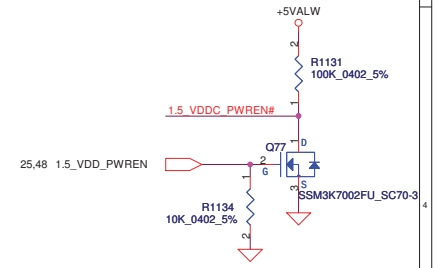
+1.5V to +1.5VSG (1.5A)

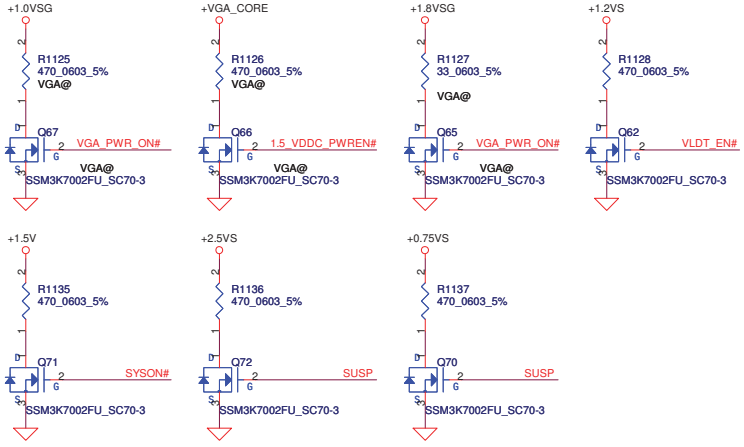




+3VS to +3VSG (3.3A)







Security Classification	Compal Secret Data		
Issued Date	2010/08/04	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	QBL50 LA-7551P	1.0

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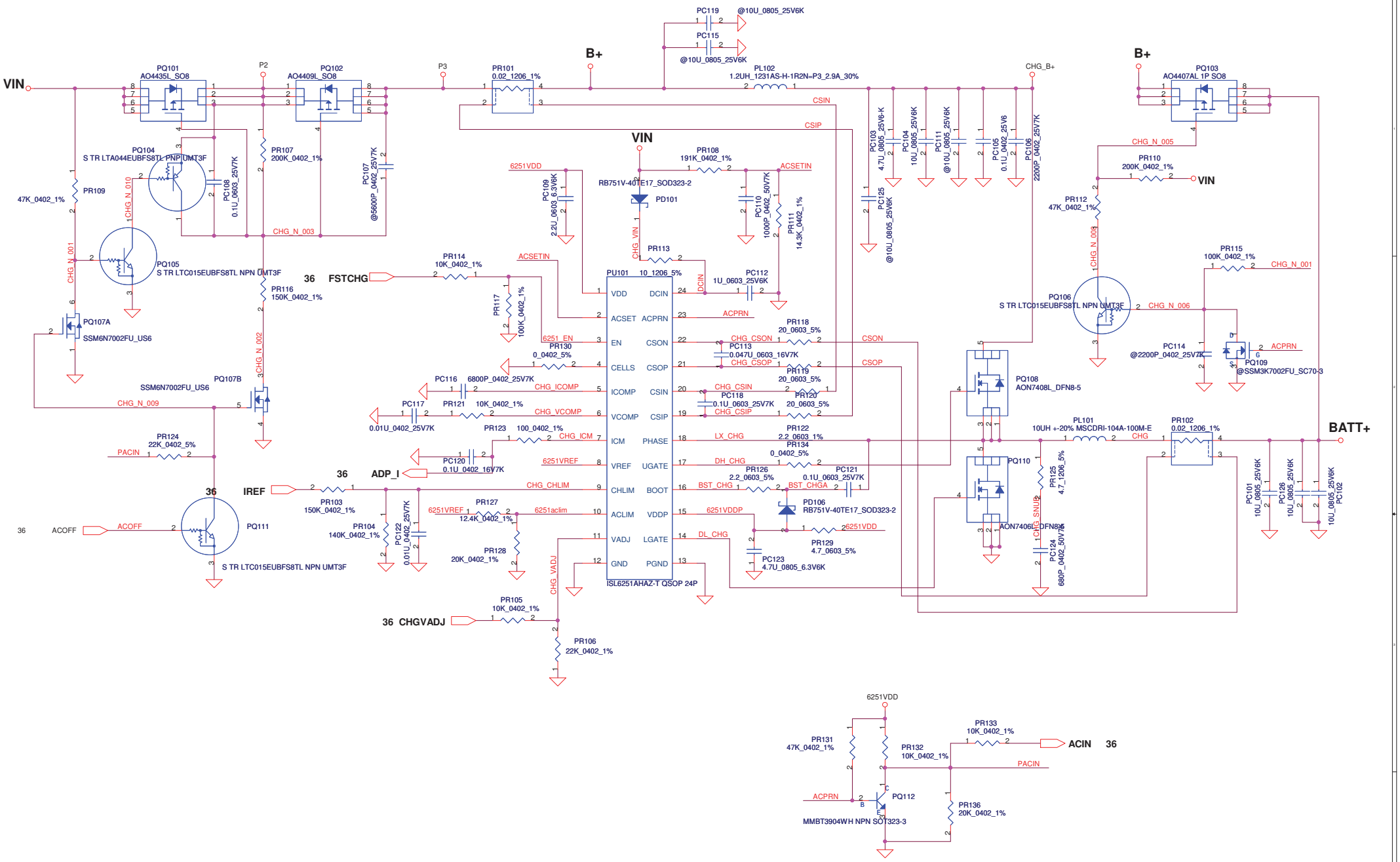


Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

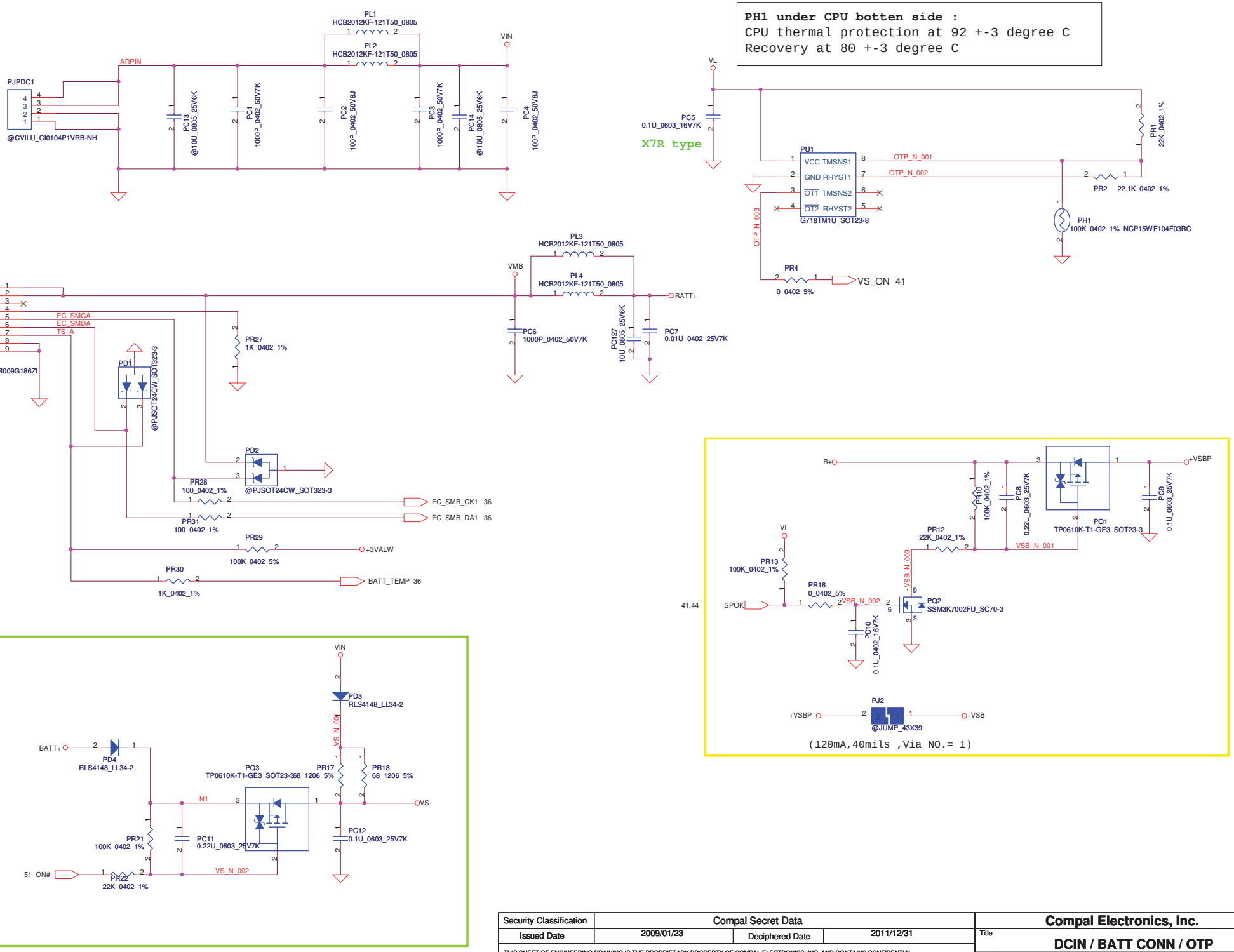
Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
		1.0

Date: Wednesday, April 27, 2011 | Sheet 39 of 53

PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C



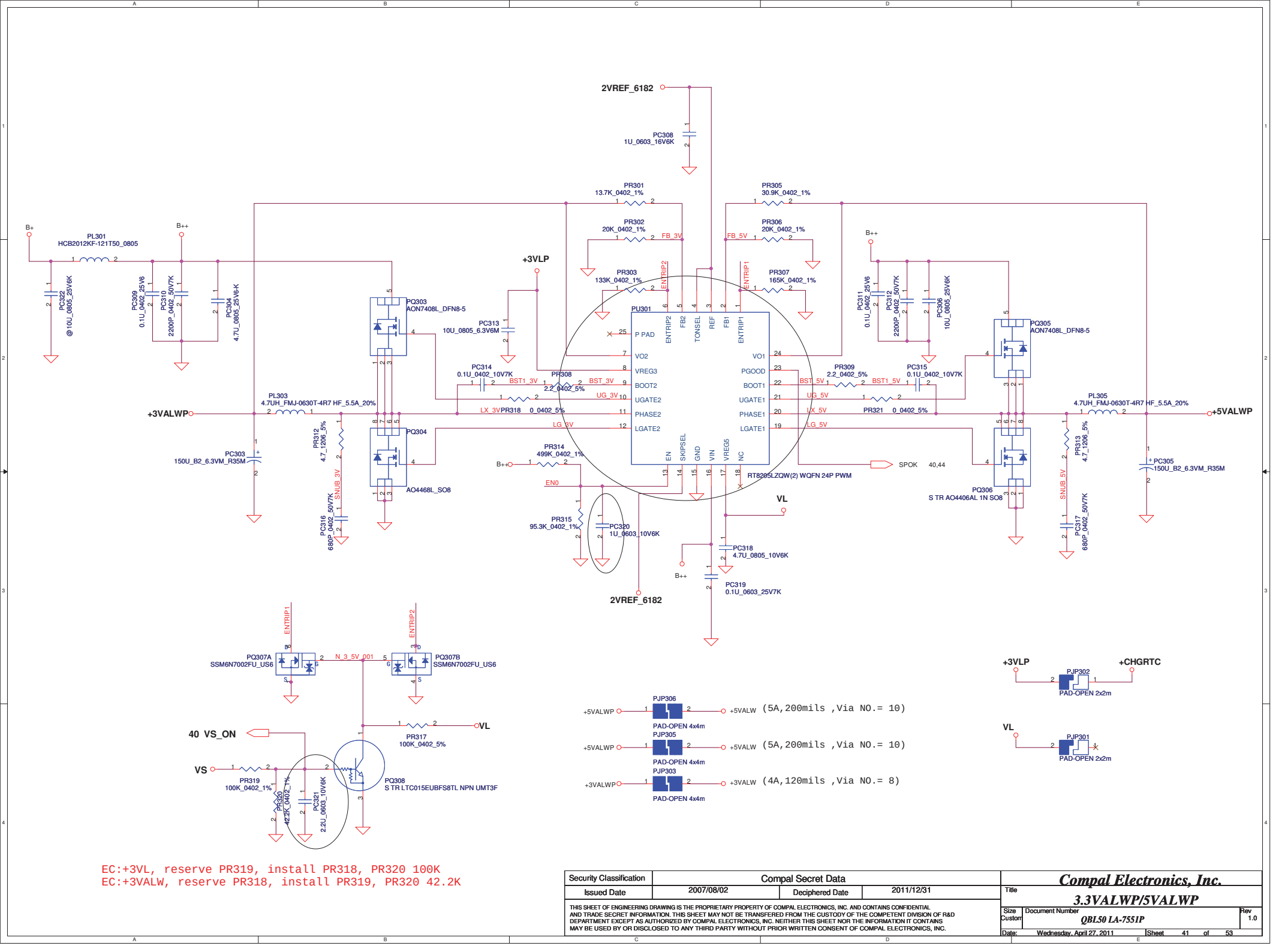
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	1.0

Date: Wednesday, April 27, 2011 | Sheet 40 of 53



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

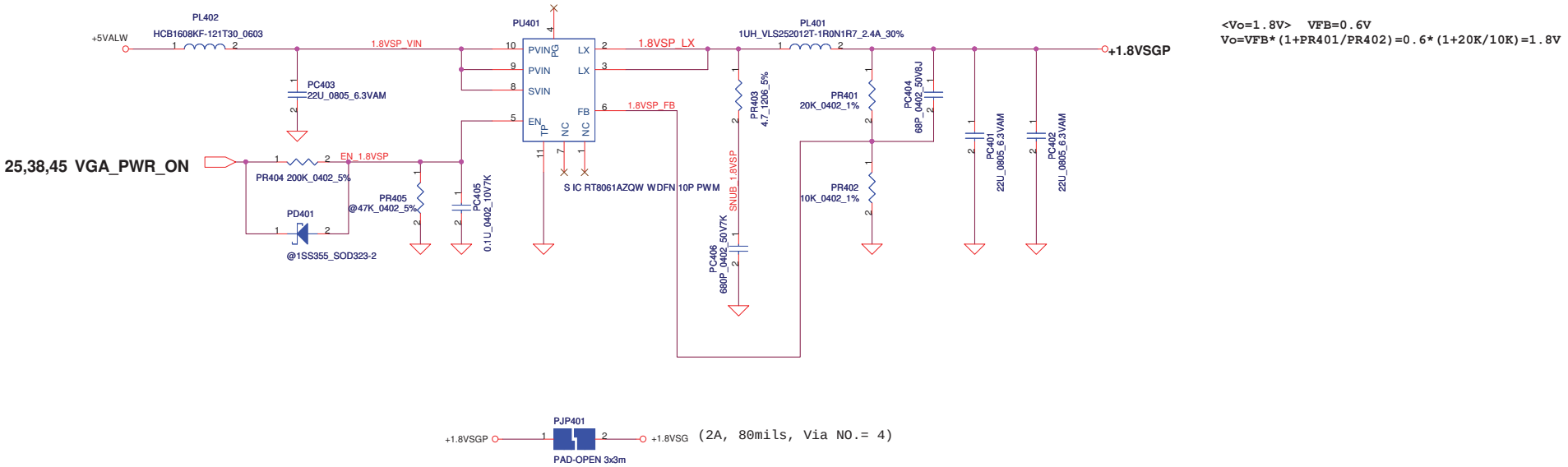
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: 3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 Sheet 41 of 53



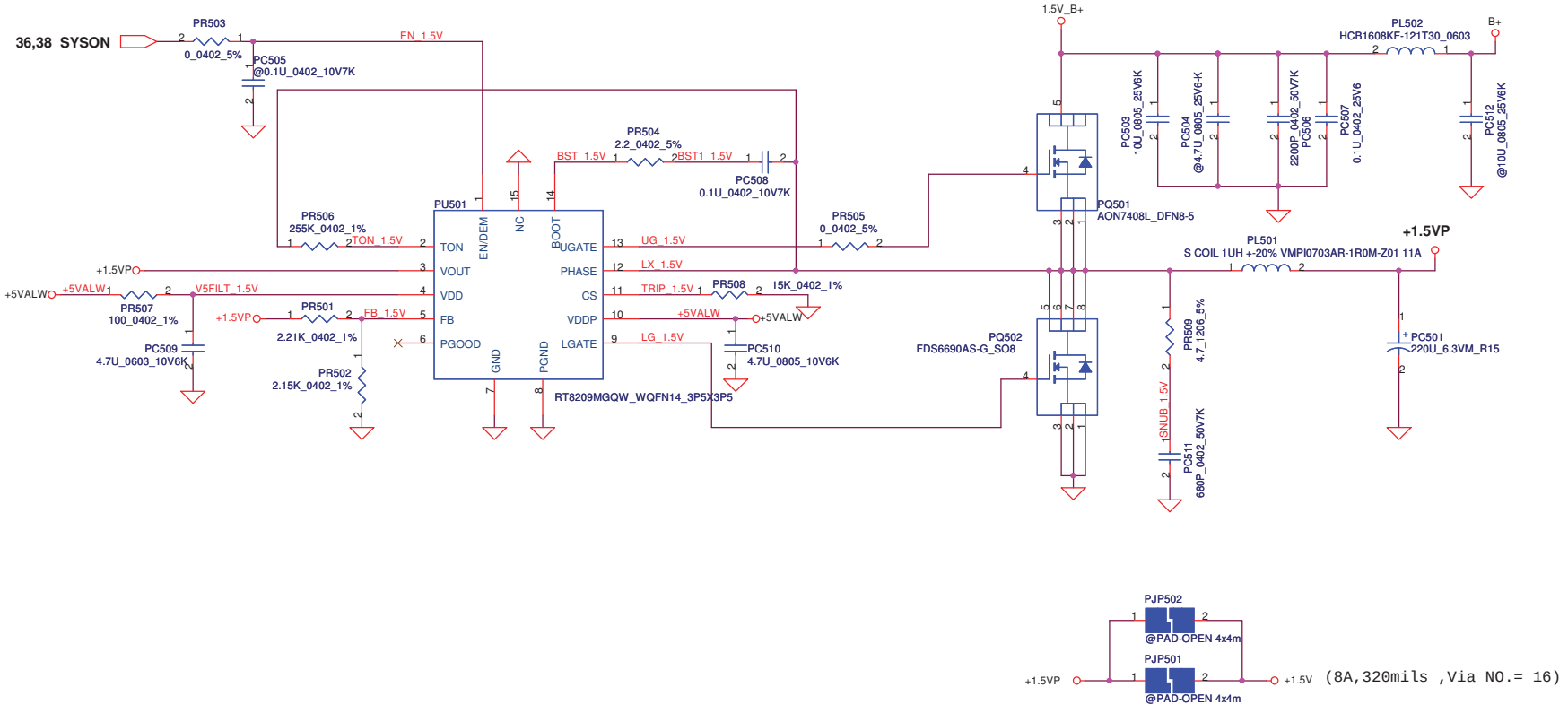
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **+1.8VSGP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	1.0

Date: Wednesday, April 27, 2011 | Sheet 42 of 53



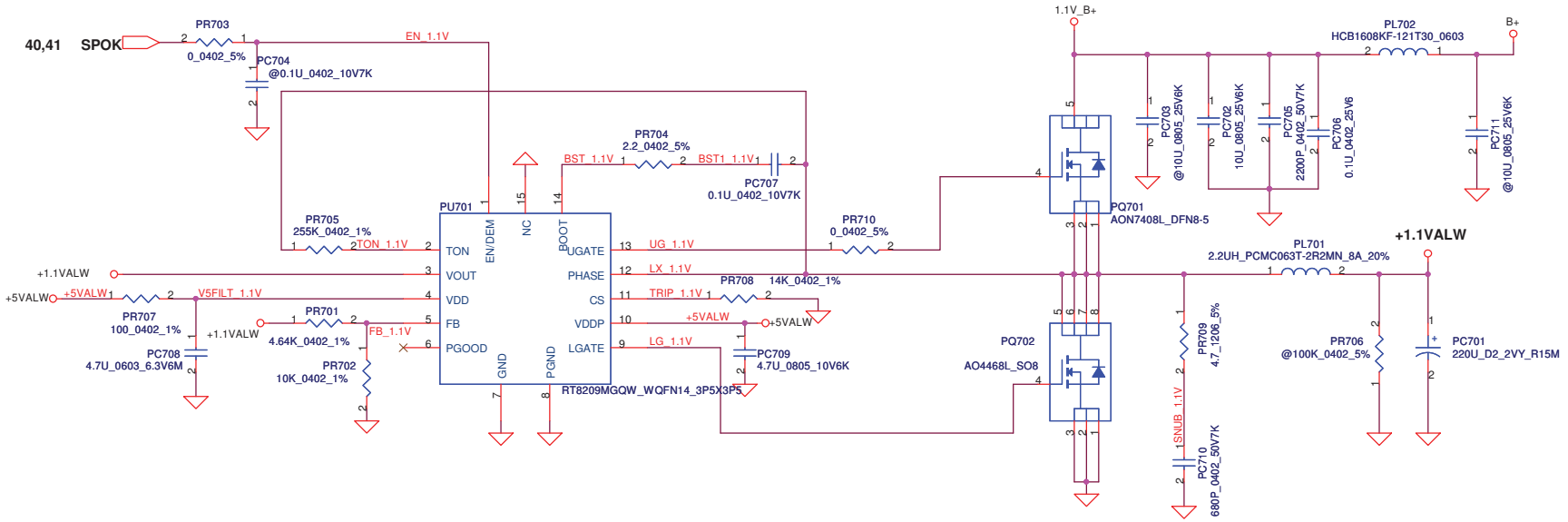
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 | Sheet 43 of 53



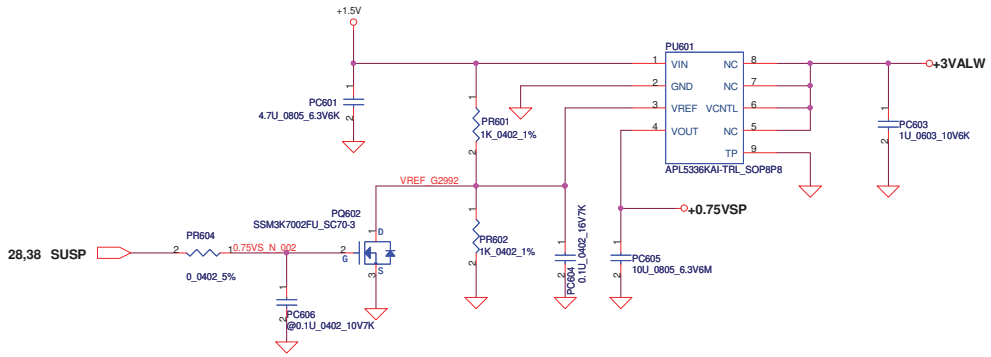
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2011/12/31

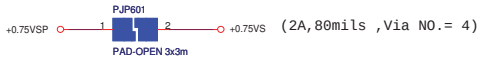
Compal Electronics, Inc.

Title: PWR+1.1VALWP

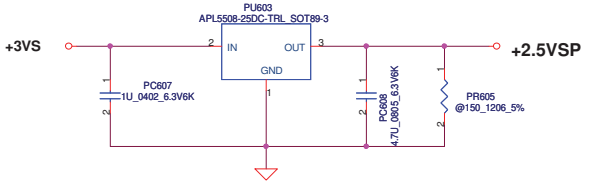
Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

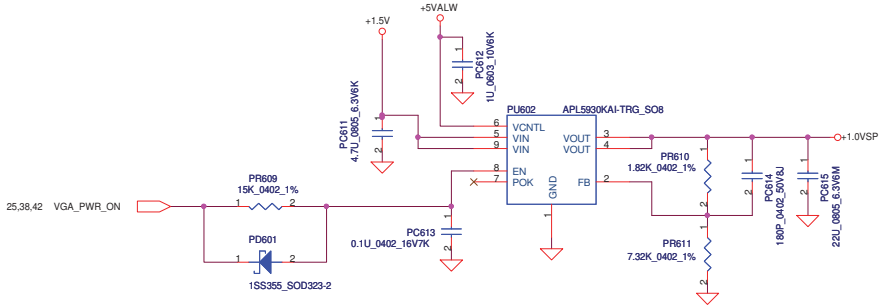
Date: Wednesday, April 27, 2011 | Sheet 44 of 53





(2A,80mils ,Via NO.= 4)





(2.5A,100mils ,Via NO.= 5)

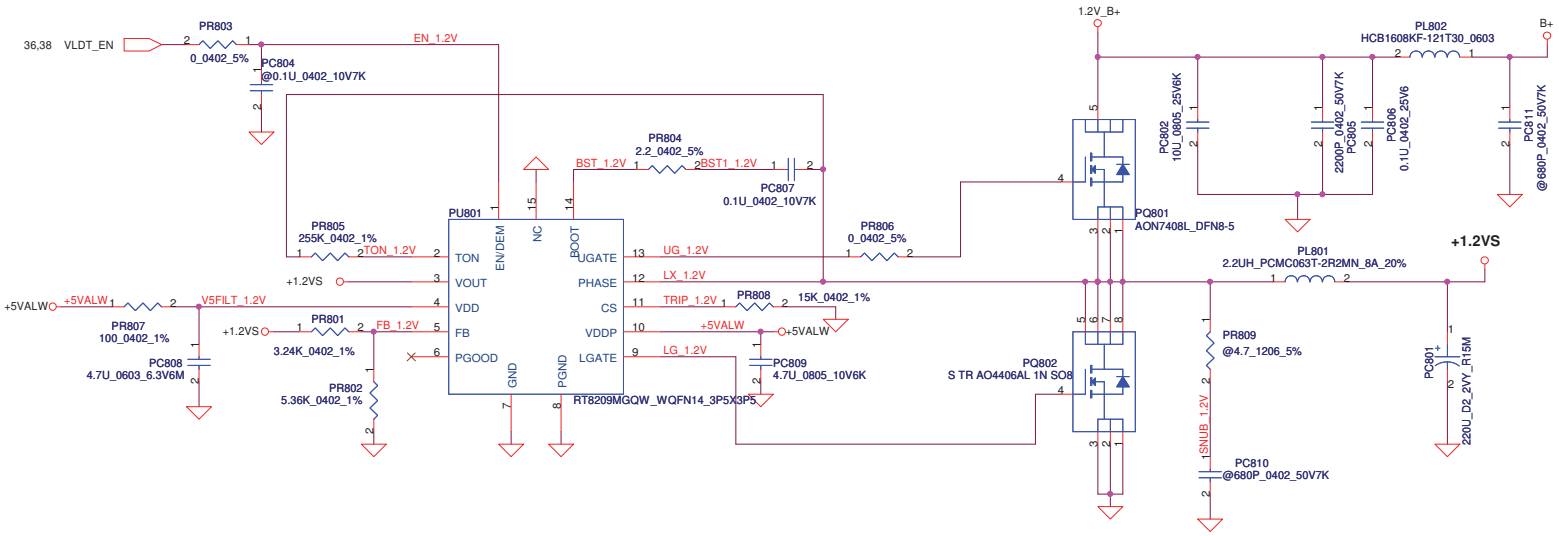
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **PWR 0.75VSP/1.0VSP/2.5VSP**

Size	Document Number	Rev
	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 | Sheet 45 of 53



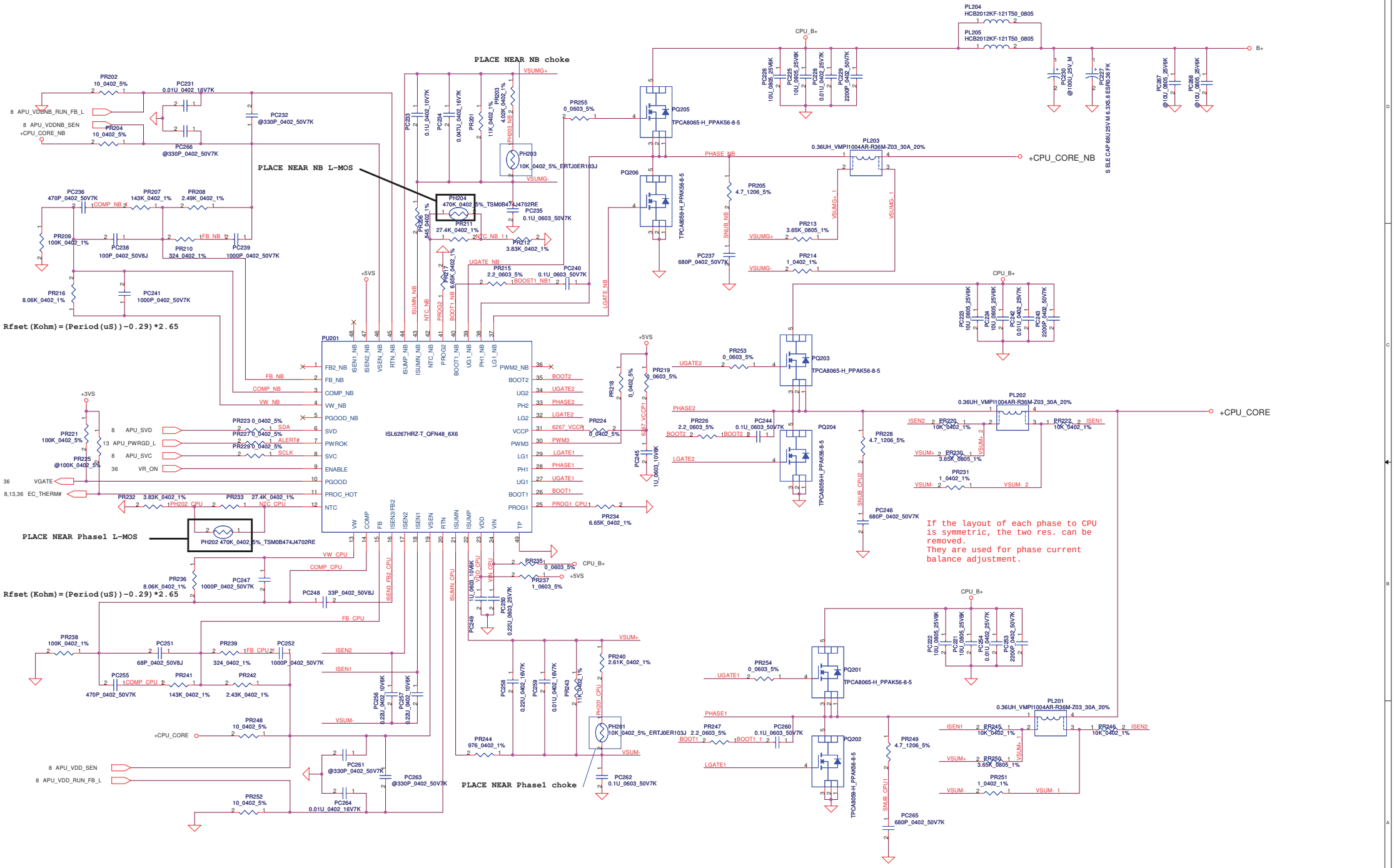
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: **+1.2VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	1.0

Date: Wednesday, April 27, 2011 | Sheet 46 of 53



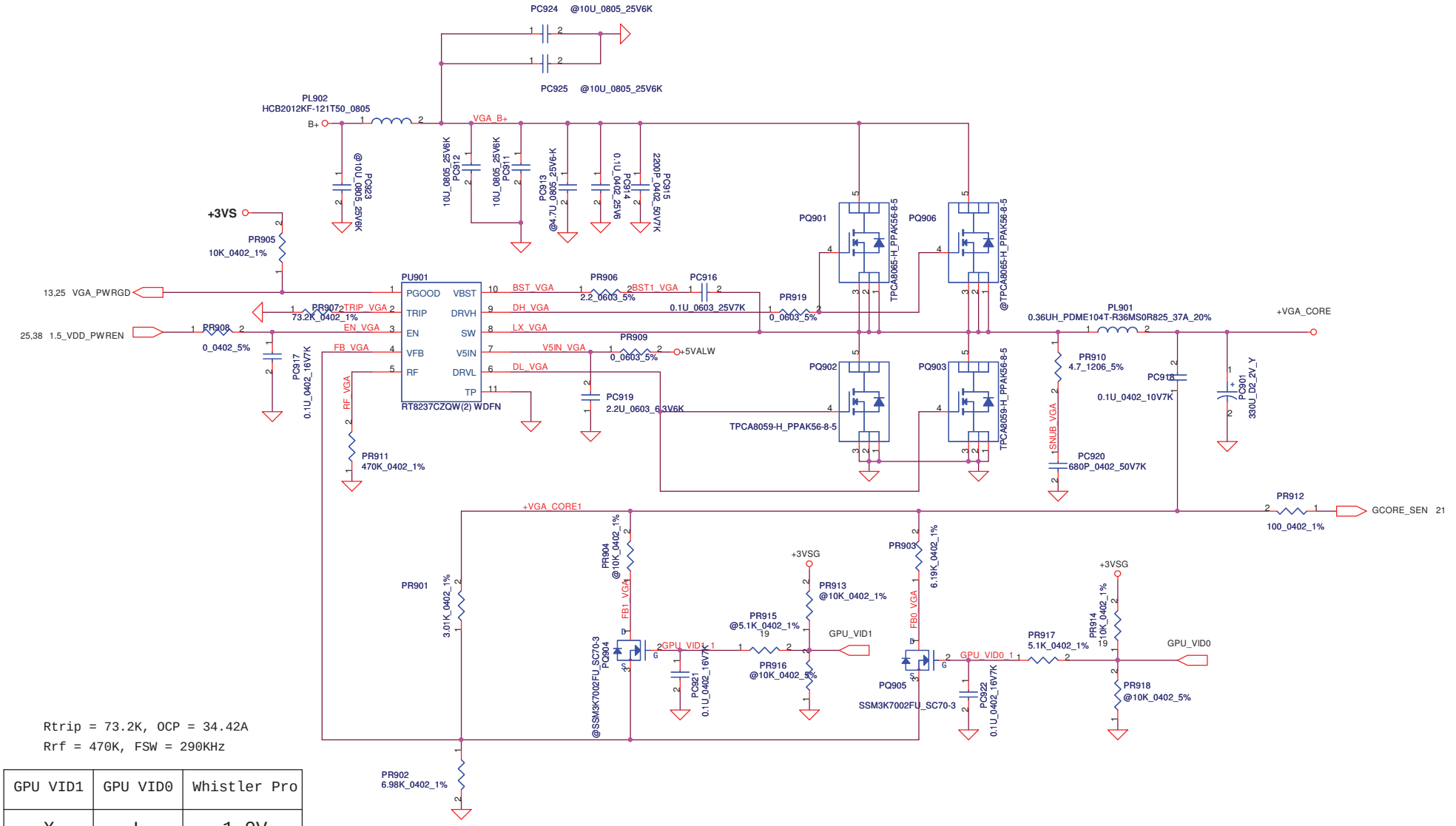
Security Classification	Compal Secret Data		
Issued Date	2010/11/11	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title: PWR_+CPU_CORE/+CPU_CORE_NB

Size	Document Number	Rev
	QBL50 LA-7551P	1.0

Date: Wednesday, April 27, 2011 | Sheet 47 of 53



Rtrip = 73.2K, OCP = 34.42A
Rrf = 470K, FSW = 290KHz

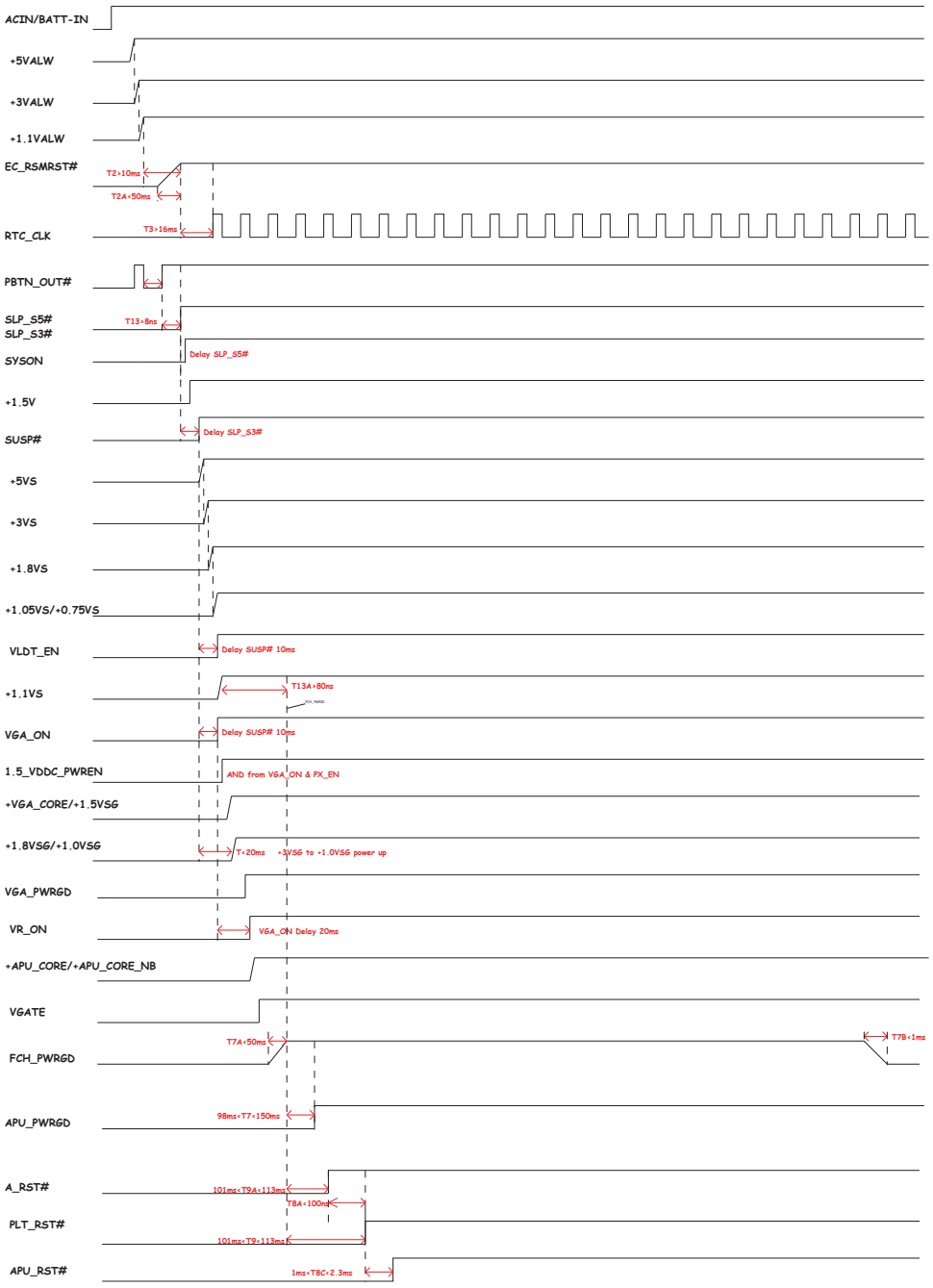
GPU VID1	GPU VID0	Whistler Pro
X	L	1.0V
X	H	0.9V
H	L	
H	H	

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title: VGA_CORE			
Size	Document Number: QBL50 LA-7551P		Rev: 1.0
Date: Wednesday, April 27, 2011	Sheet 48 of 53		

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

POWER SEQUENCE



Security Classification	Compal Secret Data		
Issued Date	2010/08/30	Deciphered Date	2011/10/31

Title	Power Sequence	
Size	Document Number	Rev
	QBL50 LA-7551P	1.0
Date:	Wednesday, April 27, 2011	Sheet of

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For AMD reuqest	0.11	PG#26	Translator change to ANX3110	03/15	ER
2		For AI charge function	0.11	PG#34	Add U2 & U56	03/15	ER
3		For PBL60 MEMO	0.11	PG#32	Change LED1 to Green color.	03/15	ER
4		For switch quality of ME.	0.11	PG#37	Change SW5,SW6 to 100g switch for ME.	03/15	ER
5		For LED brightness.	0.11	PG#32	Change R1584 to 200 ohm. Change R1586,R1588,R1591,R1592,R1593 to 100 ohm	03/15	ER
6		For DFB.	0.12	PG#11	JDIMM1 footprint change to FOX_AS0A626-J8SG-7H_204P-T	03/17	ER
7		For USB3.0 & AI charge.	0.12	PG#34	USBP0 connect to JUSB1 and USBP10 connect to JUSB2.	03/17	ER
8		For Back light function.	0.12	PG#36	U31.15 connect to ENBKL from APU.	03/17	ER
9		For HDMI HPD issue.	0.12	PG#10	Q34 change to 2N7002(ESD) Add R469 to +1.5VS.	03/19	ER
10		For DP0_HPD & DP1_HPD from AMD recommend.	0.12	PG#10	Swap Q13.1 & Q13.3, R618 unmount. Swap Q16.1 & Q16.3, R627 unmount.	03/19	ER
11		For Travis Vendor request	0.12	PG#26	Del DP0_TXN0_C & DP0_TXP0_C	03/22	ER
12		For LED1	0.12	PG#32	LED1 connect to +3VALW	03/22	ER
13		For EC SMBUS	0.2	PG#36	R1021,R1022 change to install.	03/24	ER
14		For Sourcer recommend	0.2		SE100105Z80 change to SE000000K80	03/24	ER
15		For Sourcer recommend	0.2		SE103225Z80 change to SE000008880	03/24	ER
16		For Sourcer recommend	0.2		SB000006A00 change to SB000006A10	03/24	ER
17		For Thermal	0.2	PG#37	Del H4	03/24	ER
18		For +5VS rising time	0.2	PG#38	R1103 change to 47K	03/24	ER
19		For Crystal EA	0.2	PG#29	C1634 change to 12P & C1633 change to 15P	03/24	ER
20		For Crystal EA	0.2	PG#13	C1200 & C1201 change to 12P	03/24	ER
21		For Crystal EA	0.2	PG#19	C353 change to 15P & C354 change to 12P	03/24	ER
22		For EMI request	0.2	PG#36	R1033 change to SM01000DI00 R1055 change to 33 ohm	03/24	ER
23		For EMI request	0.2	PG#28	L38,L39,L40,L41 change to SM070001S00	03/24	ER
24		For EMI request	0.2	PG#27	D1,D2,D3,D6 change to install	03/24	ER
25		For Crystal EA	0.2	PG#13	C1205,C1206 change to 10P	03/24	ER
26		For AI charge	0.2	PG#36 PG#34	U2 reserve CEN# to EC	03/25	ER
27		For AMD spec	0.2	PG#27	R1642 & R1646 change to 4.6K ohm	03/29	ER

Compal Electronics, Inc.

Title: HW-PIR

Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For EMI reuqest	0.2	PG#30	R1555,R1556,R1557,R1558 change to 0.1uf	03/29	ER
2		For share ROM reuqest	0.2	PG#15 PG#16	U28,R626,R934,R935,R35 change to Un-install R921 change un-install & U910 change to install	03/29	ER
3		For EMI reuqest	0.2	PG#34	D5 change to SC300001Y00 (YSCLAMP0524P)	03/29	ER
4		For Crystal vendor recommend	0.21	PG#13	Y4 change to SJ100007N00 (32.768K 7PF)	04/07	PR
5		For EMI recommend	0.21	PG#29	TS1 change to SP050006F00 (IH-160)	04/07	PR
6		For discharge EA	0.21	PG#38	R1127 change from 470 ohm to 33 ohm	04/07	PR
7		For leakage current	0.21	PG#27	R1644,R1645,Q101 change to install R4,R31 change to un-install	04/07	PR
8		For EMI recommend	0.21	PG#29	C1636 change from 1000P to 120P	04/08	PR
9		For thermal recommend	0.21	PG#19	Add R78, R79, R80, R82	04/18	PR
10		Reserve PX_EN signal	0.21	PG#36	Reserve signal PX_EN to EC pin 74	04/18	PR
11		Swap JDIMM1 & JDIMM2 location	0.21	PG#11 PG#12	Follow ME BOM	04/18	PR
12		Do not use for MP	0.21	PG#35	Del SW3 SW4	04/18	PR
13		Change Boarrd ID to PR10	0.21	PG#37	Change R1036 to 18k	04/18	PR
14		For DFB request del co-lay schematiic	0.21	PG#34	Del R672~R675, R664~R667	04/18	PR
15		For EMI request	0.22	PG#29	ADD D7	04/19	PR
16		For EMI request	1.0	PG#13	unstuff C1193	04/25	PR
17		For Customer change FCH P/N	1.0	PG#13 ~17	location U25, for M2 change to SA000042C80, M3 change to SA000043ID0	04/25	PR
18		For ESD request	1.0	PG#32	R628,R629,R678,R679,R680,R681 change from 0ohm to 33ohm & Add 1uF for C560,C568,C569,C570,C573,C571	04/27	PR
19							
20							
21							
22							
23							
24							
25							
26							
27							

Compal Electronics, Inc.
Title: HW-PIR
Size: Custom | Document Number: QBL50 LA-7551P | Rev: 1.0
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For MP cost down	1.0		As picture	03/15	PR
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							

Reference	Value	Source Part	Source Library	Page	Schematic
R22	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R23	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R24	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R26	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R27	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R28	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R81	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P14-HUD...	SCHEMA...
R483	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P23-VRA...	SCHEMA...
R485	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P23-VRA...	SCHEMA...
R511	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P24-VRA...	SCHEMA...
R513	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P24-VRA...	SCHEMA...
R537	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P06-FS1 ...	SCHEMA...
R538	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P06-FS1 ...	SCHEMA...
R591	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R598	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R606	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R608	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R611	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P08-FS1 ...	SCHEMA...
R647	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN ...	SCHEMA...
R912	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P16-HUD...	SCHEMA...
R945	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1291	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P26-LVD...	SCHEMA...
R1575	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini...	SCHEMA...
R1577	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P32-Mini...	SCHEMA...
R1634	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1635	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1636	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1641	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1651	0_0402_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R19	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R20	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R25	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R560	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN ...	SCHEMA...
R658	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P29-LAN ...	SCHEMA...
R1049	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P35-FAN ...	SCHEMA...
R1145	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1148	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1534	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P30-HD ...	SCHEMA...
R1537	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P30-HD ...	SCHEMA...
R1560	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P31-RTS...	SCHEMA...
R1643	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R1650	0_0603_5%	R-SHORT	X:\CIS_SYMB...	P27-LVD...	SCHEMA...
R570	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P26-LVD...	SCHEMA...
R607	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P26-LVD...	SCHEMA...
R937	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R938	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R941	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P17-HUD...	SCHEMA...
R1531	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P30-HD ...	SCHEMA...
R1595	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P33-HDD...	SCHEMA...
R1598	0_0805_5%	R-SHORT	X:\CIS_SYMB...	P33-HDD...	SCHEMA...

Compal Electronics, Inc.

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