

Compal Confidential

QCL40 MB Schematic Document

LA-8221P

Rev: 0.2

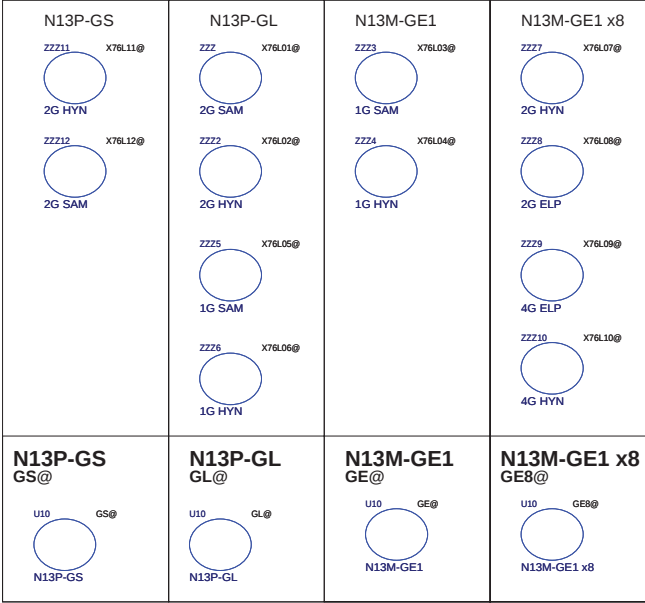
2011.09.28

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Security Classification	Compal Secret Data			Compal Electronics, Inc. Block Diagram		
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X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8

ER37



DIS@: VGA componet
GEL@: N13P-GL or N13M-GE1
GSL@: N13P-GL or N13P-GS
GS@: N13P-GS

930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

9012@: EC(ENE 9012 chip)

SMBUS Control Table							
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DAI	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DAI2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

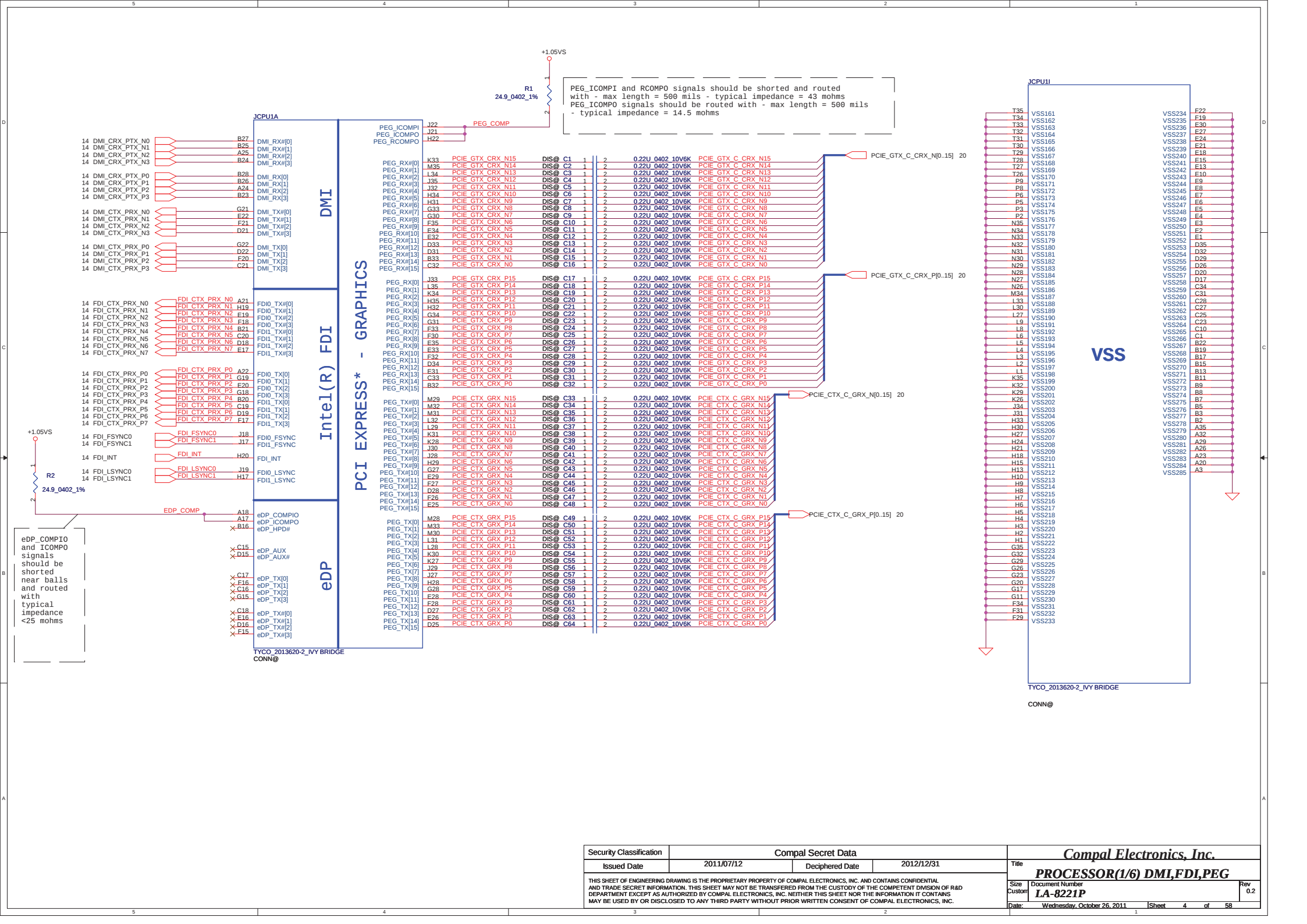
Voltage Rails

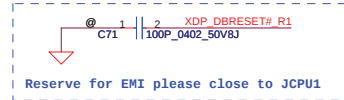
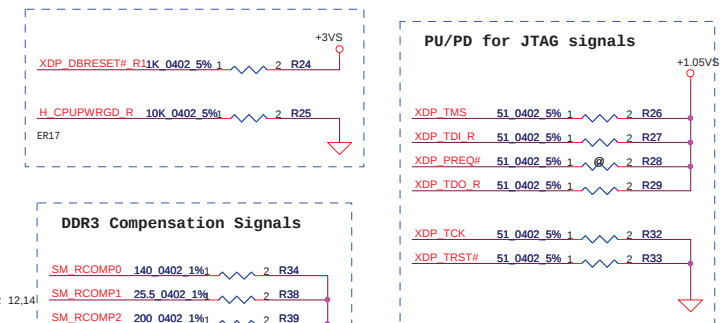
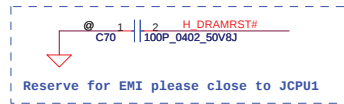
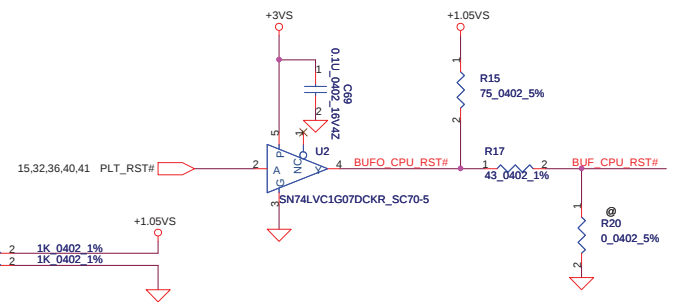
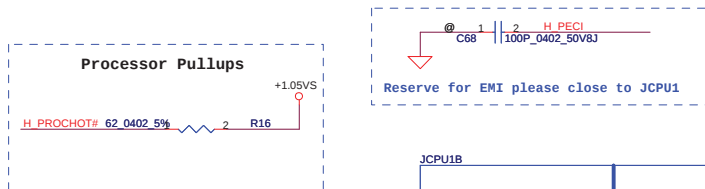
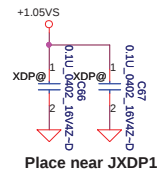
Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

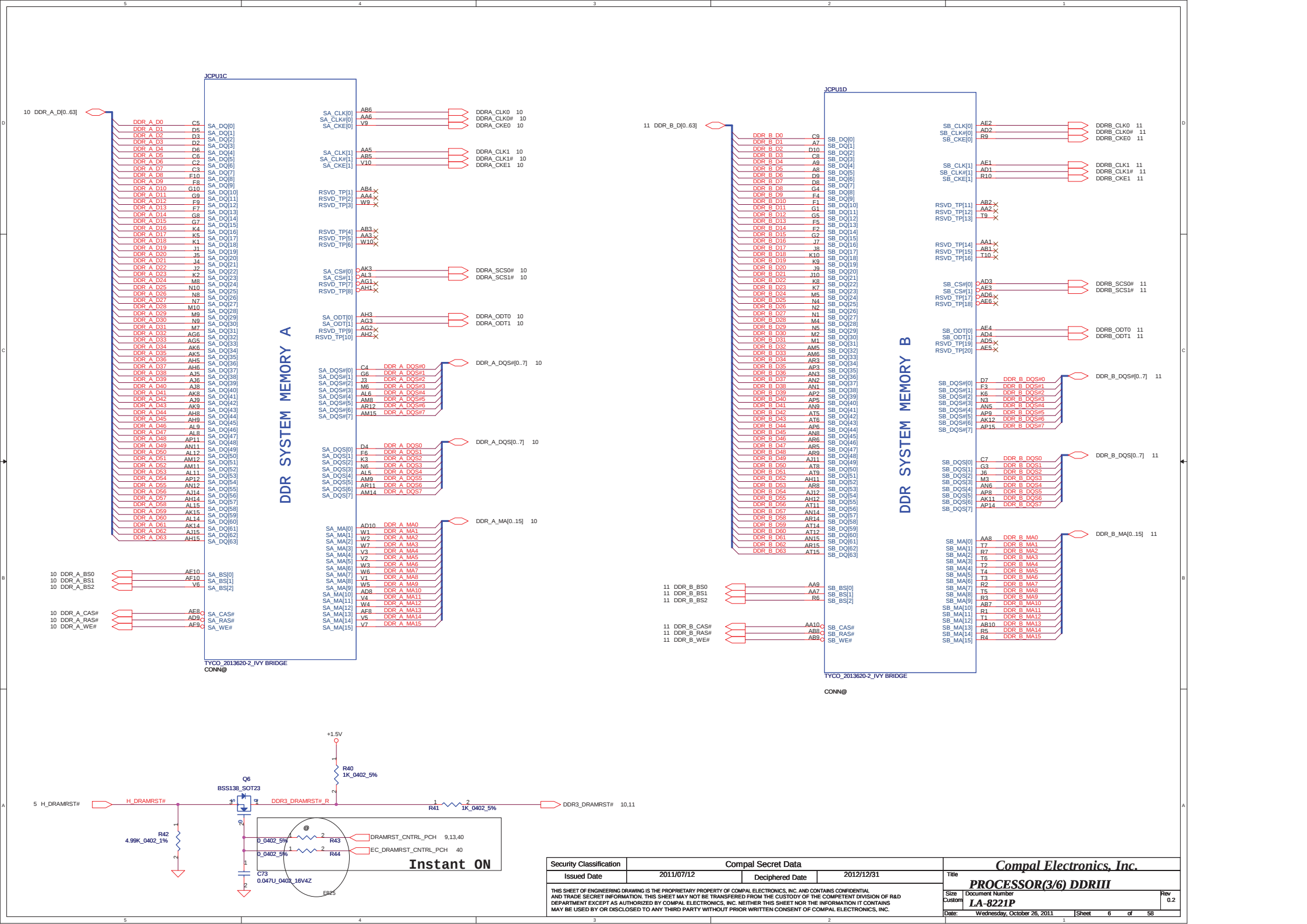
PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None
	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
	13	None

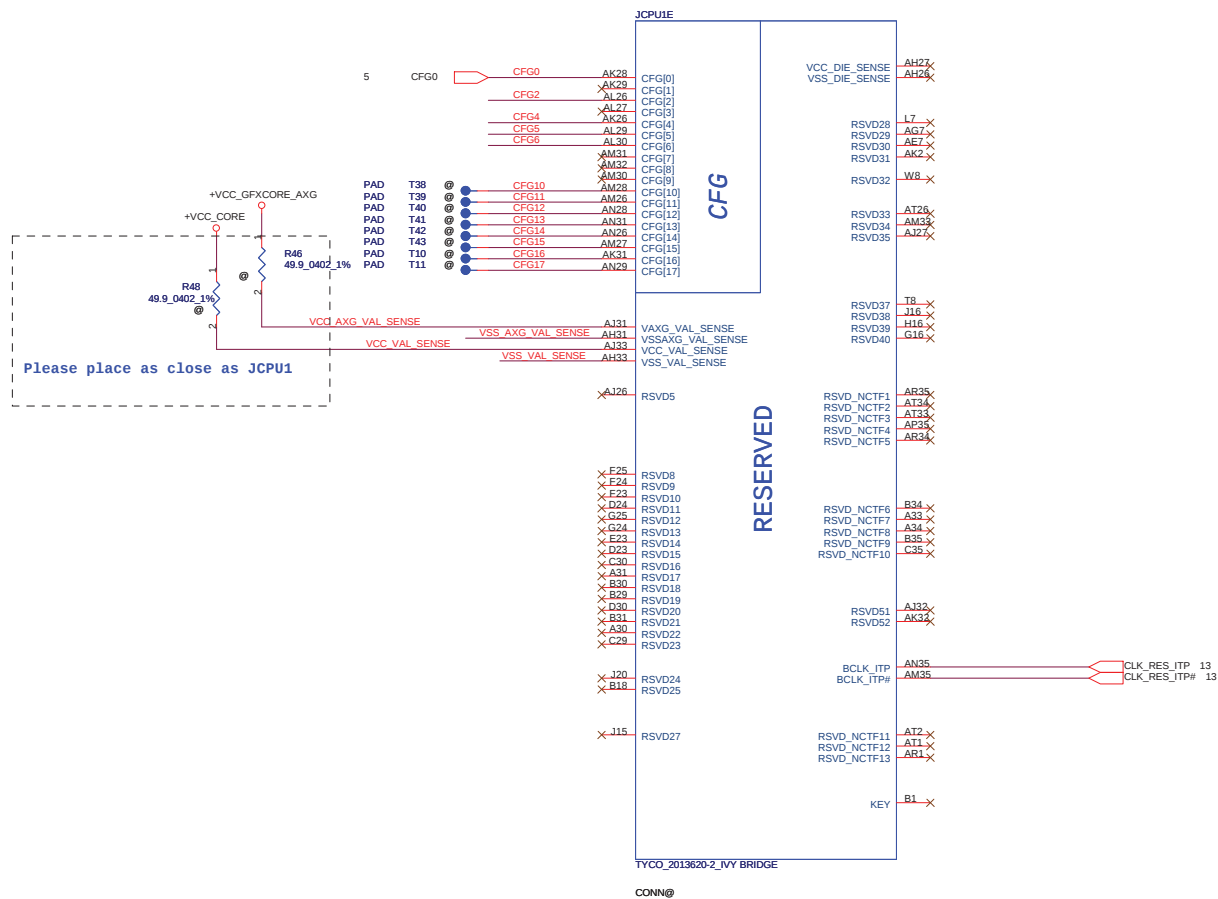
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



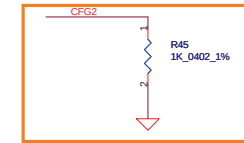


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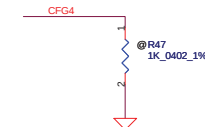


CFG Straps for Processor



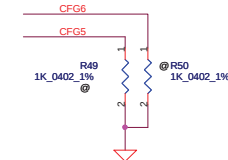
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed
------	--



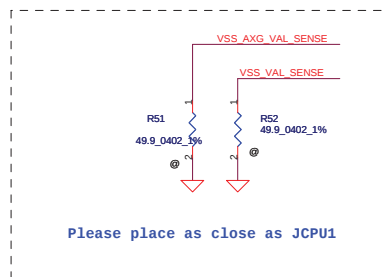
Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

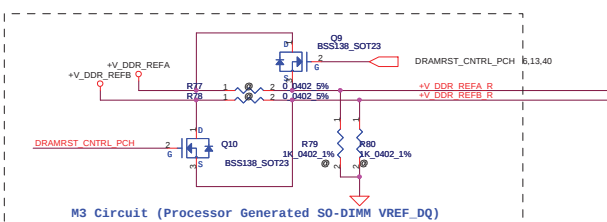


PCIe Port Bifurcation Straps

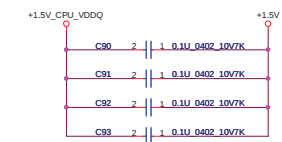
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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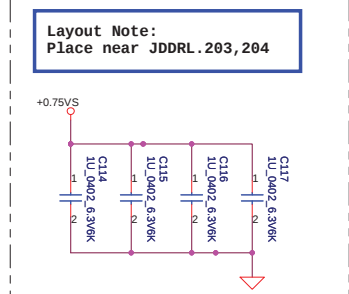
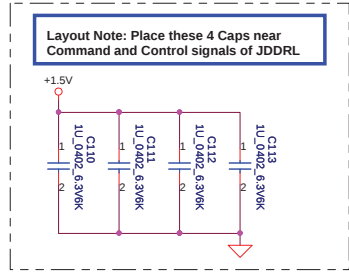
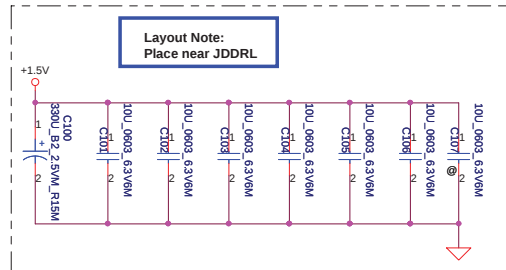
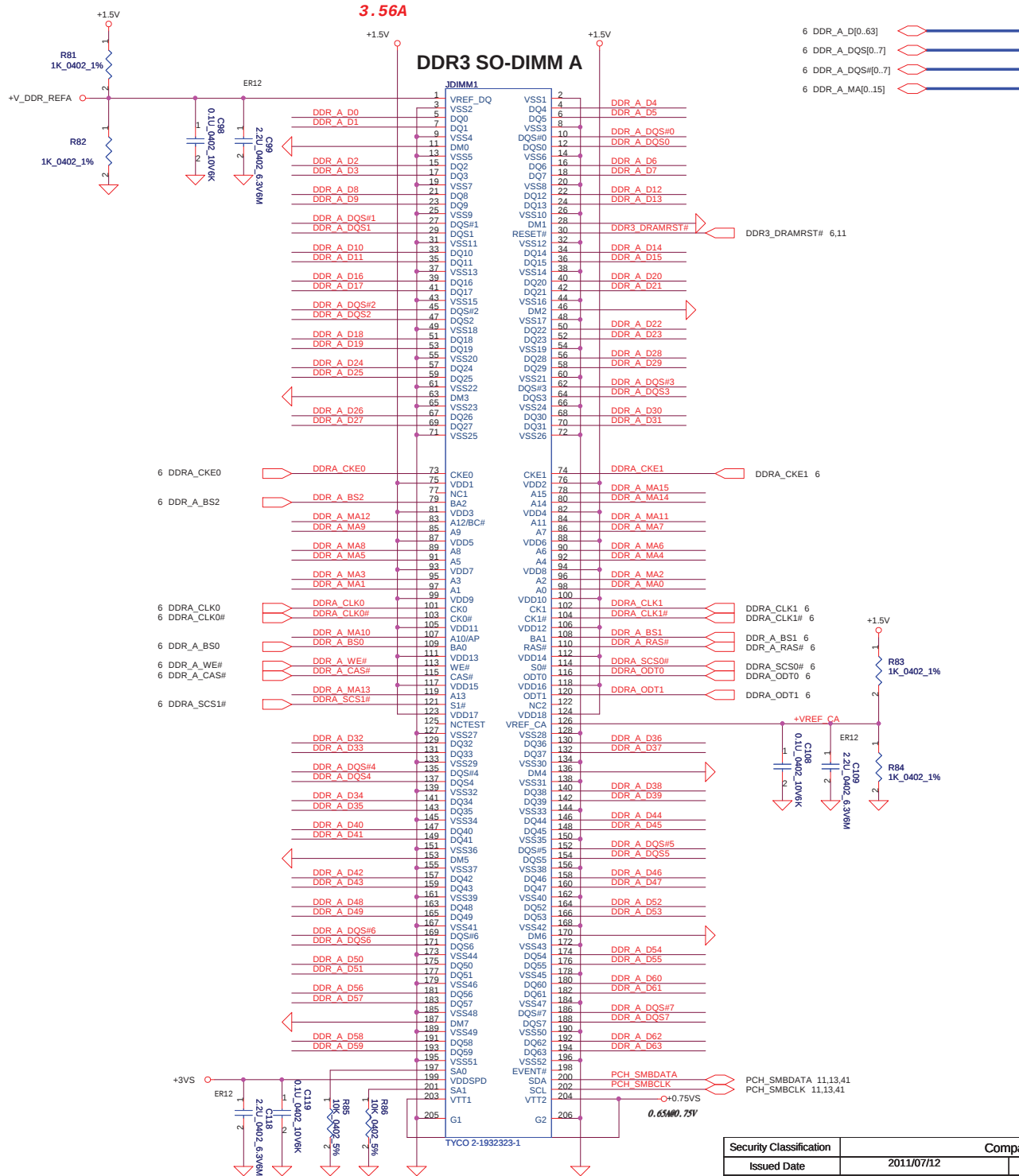


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A7B5	V5S1	V5S81	A202
A7B6	V5S2	V5S82	A203
A7B7	V5S3	V5S83	A204
A7B8	V5S4	V5S84	A205
A7B9	V5S5	V5S85	A206
A7C1	V5S6	V5S86	A207
A7C2	V5S7	V5S87	A208
A7C3	V5S8	V5S88	A209
A7C4	V5S9	V5S89	A210
A7C5	V5S10	V5S90	A211
A7C6	V5S11	V5S91	A212
A7C7	V5S12	V5S92	A213
A7C8	V5S13	V5S93	A214
A7C9	V5S14	V5S94	A215
A7C10	V5S15	V5S95	A216
A7C11	V5S16	V5S96	A217
A7C12	V5S17	V5S97	A218
A7C13	V5S18	V5S98	A219
A7C14	V5S19	V5S99	A220
A7C15	V5S20	V5S100	A221
A7C16	V5S21	V5S101	A222
A7C17	V5S22	V5S102	A223
A7C18	V5S23	V5S103	A224
A7C19	V5S24	V5S104	A225
A7C20	V5S25	V5S105	A226
A7C21	V5S26	V5S106	A227
A7C22	V5S27	V5S107	A228
A7C23	V5S28	V5S108	A229
A7C24	V5S29	V5S109	A230
A7C25	V5S30	V5S110	A231
A7C26	V5S31	V5S111	A232
A7C27	V5S32	V5S112	A233
A7C28	V5S33	V5S113	A234
A7C29	V5S34	V5S114	A235
A7C30	V5S35	V5S115	A236
A7C31	V5S36	V5S116	A237
A7C32	V5S37	V5S117	A238
A7C33	V5S38	V5S118	A239
A7C34	V5S39	V5S119	A240
A7C35	V5S40	V5S120	A241
A7C36	V5S41	V5S121	A242
A7C37	V5S42	V5S122	A243
A7C38	V5S43	V5S123	A244
A7C39	V5S44	V5S124	A245
A7C40	V5S45	V5S125	A246
A7C41	V5S46	V5S126	A247
A7C42	V5S47	V5S127	A248
A7C43	V5S48	V5S128	A249
A7C44	V5S49	V5S129	A250
A7C45	V5S50	V5S130	A251
A7C46	V5S51	V5S131	A252
A7C47	V5S52	V5S132	A253
A7C48	V5S53	V5S133	A254
A7C49	V5S54	V5S134	A255
A7C50	V5S55	V5S135	A256
A7C51	V5S56	V5S136	A257
A7C52	V5S57	V5S137	A258
A7C53	V5S58	V5S138	A259
A7C54	V5S59	V5S139	A260
A7C55	V5S60	V5S140	A261
A7C56	V5S61	V5S141	A262
A7C57	V5S62	V5S142	A263
A7C58	V5S63	V5S143	A264
A7C59	V5S64	V5S144	A265
A7C60	V5S65	V5S145	A266
A7C61	V5S66	V5S146	A267
A7C62	V5S67	V5S147	A268
A7C63	V5S68	V5S148	A269
A7C64	V5S69	V5S149	A270
A7C65	V5S70	V5S150	A271
A7C66	V5S71	V5S151	A272
A7C67	V5S72	V5S152	A273
A7C68	V5S73	V5S153	A274
A7C69	V5S74	V5S154	A275
A7C70	V5S75	V5S155	A276
A7C71	V5S76	V5S156	A277
A7C72	V5S77	V5S157	A278
A7C73	V5S78	V5S158	A279
A7C74	V5S79	V5S159	A280
A7C75	V5S80	V5S160	A281

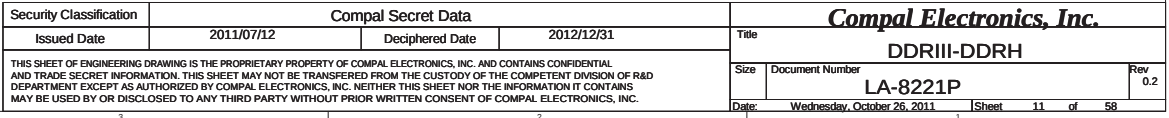


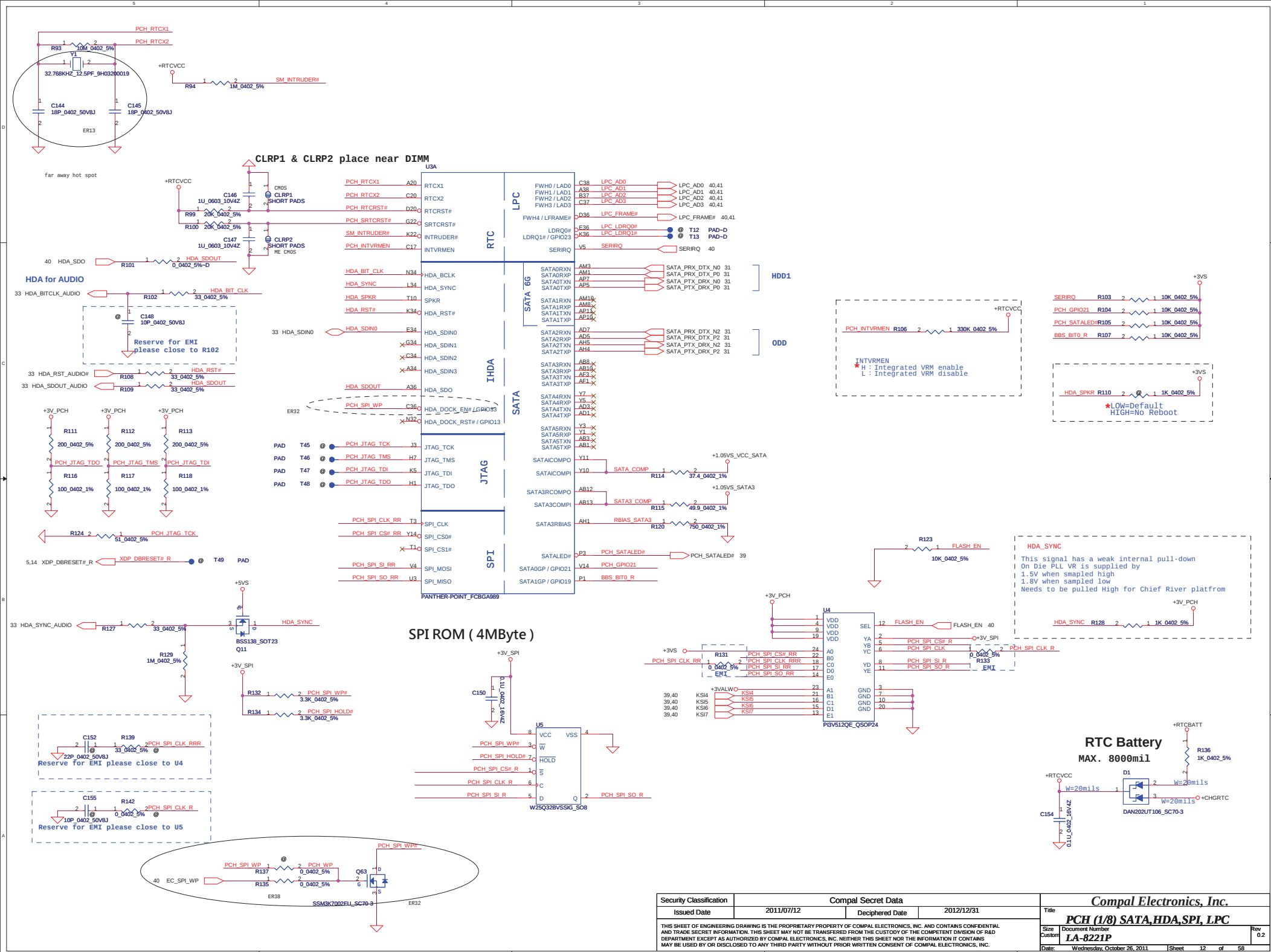


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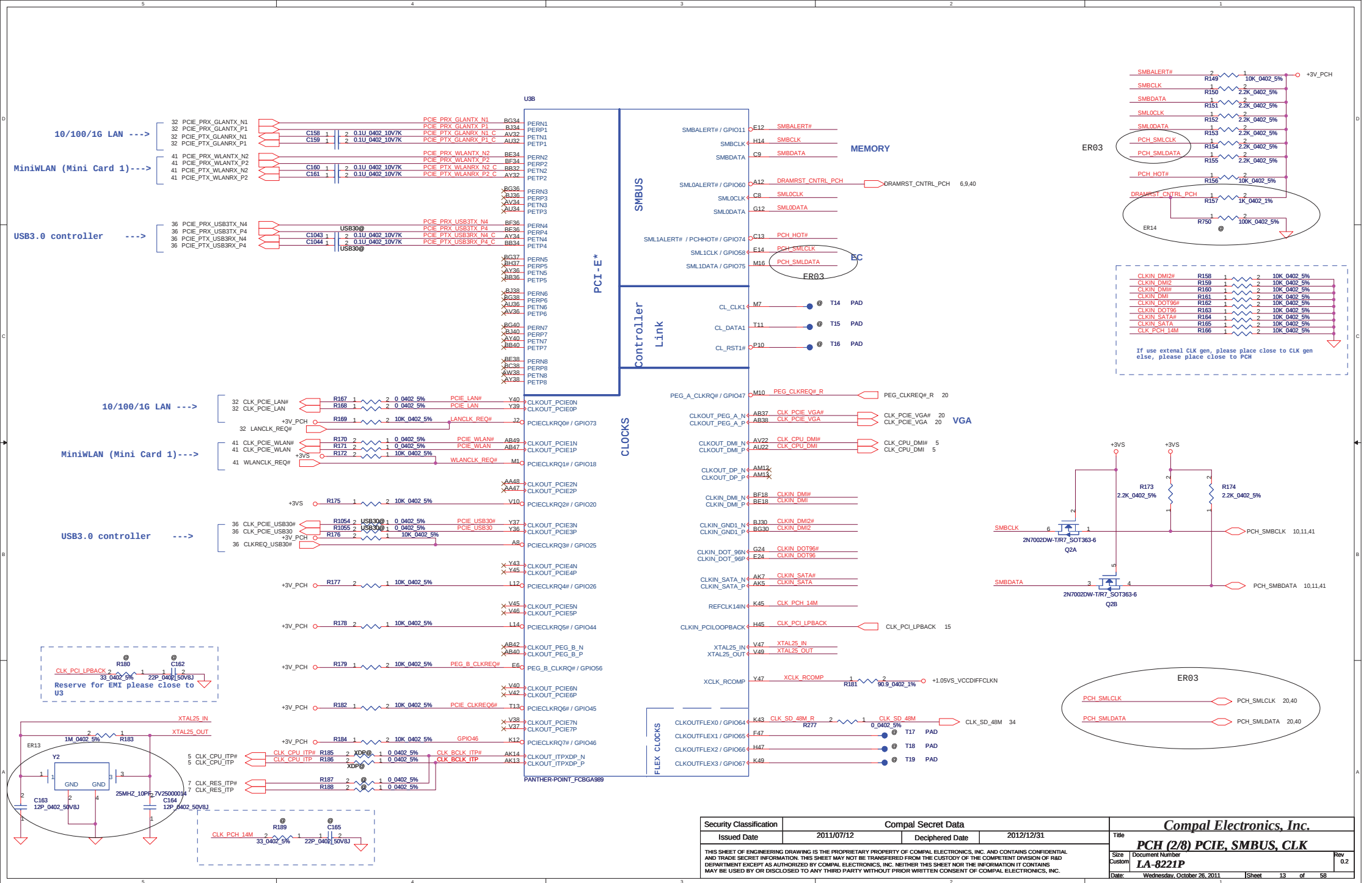
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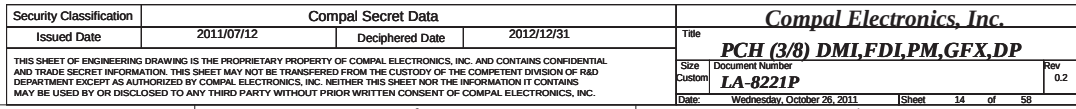


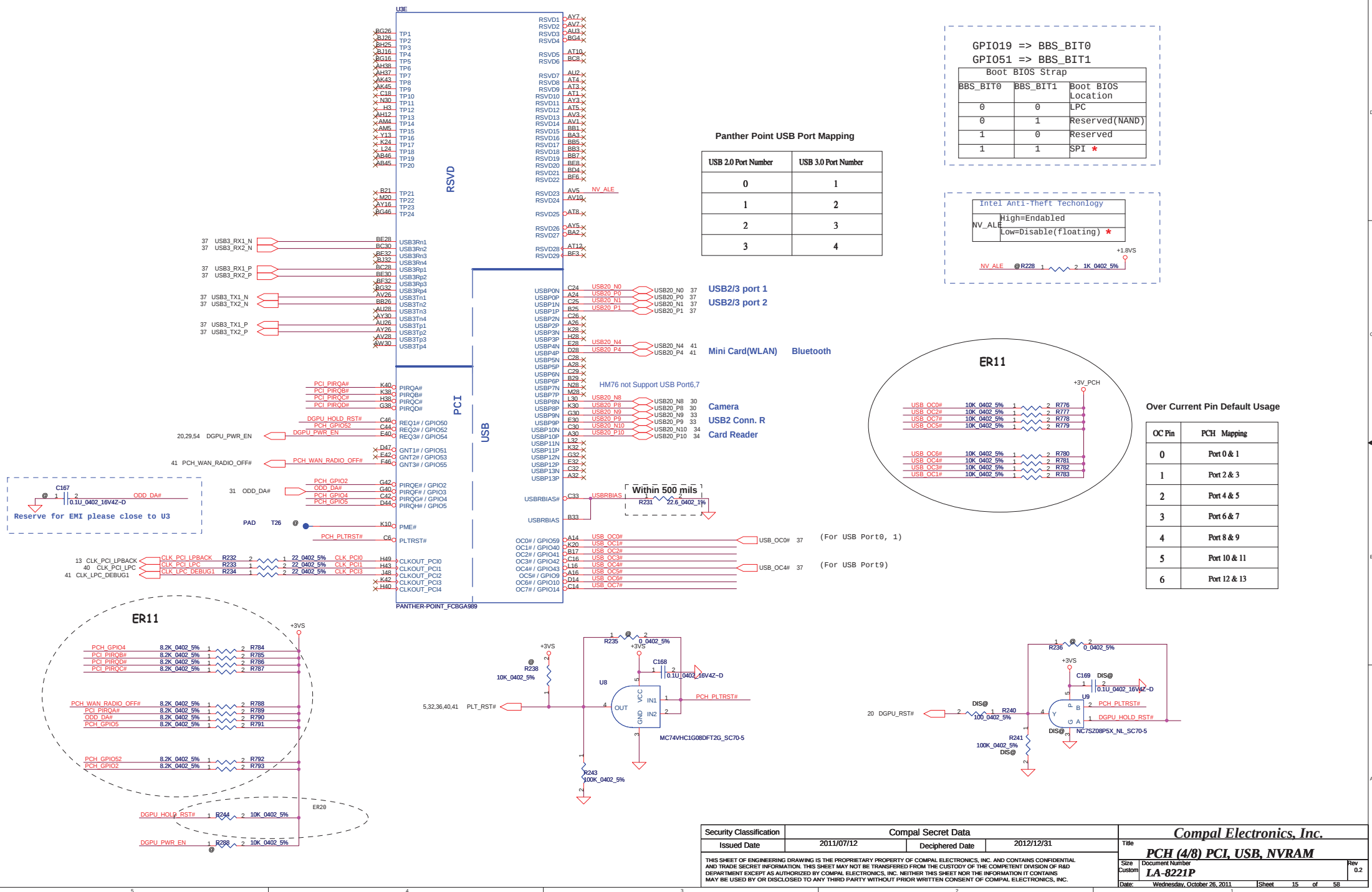


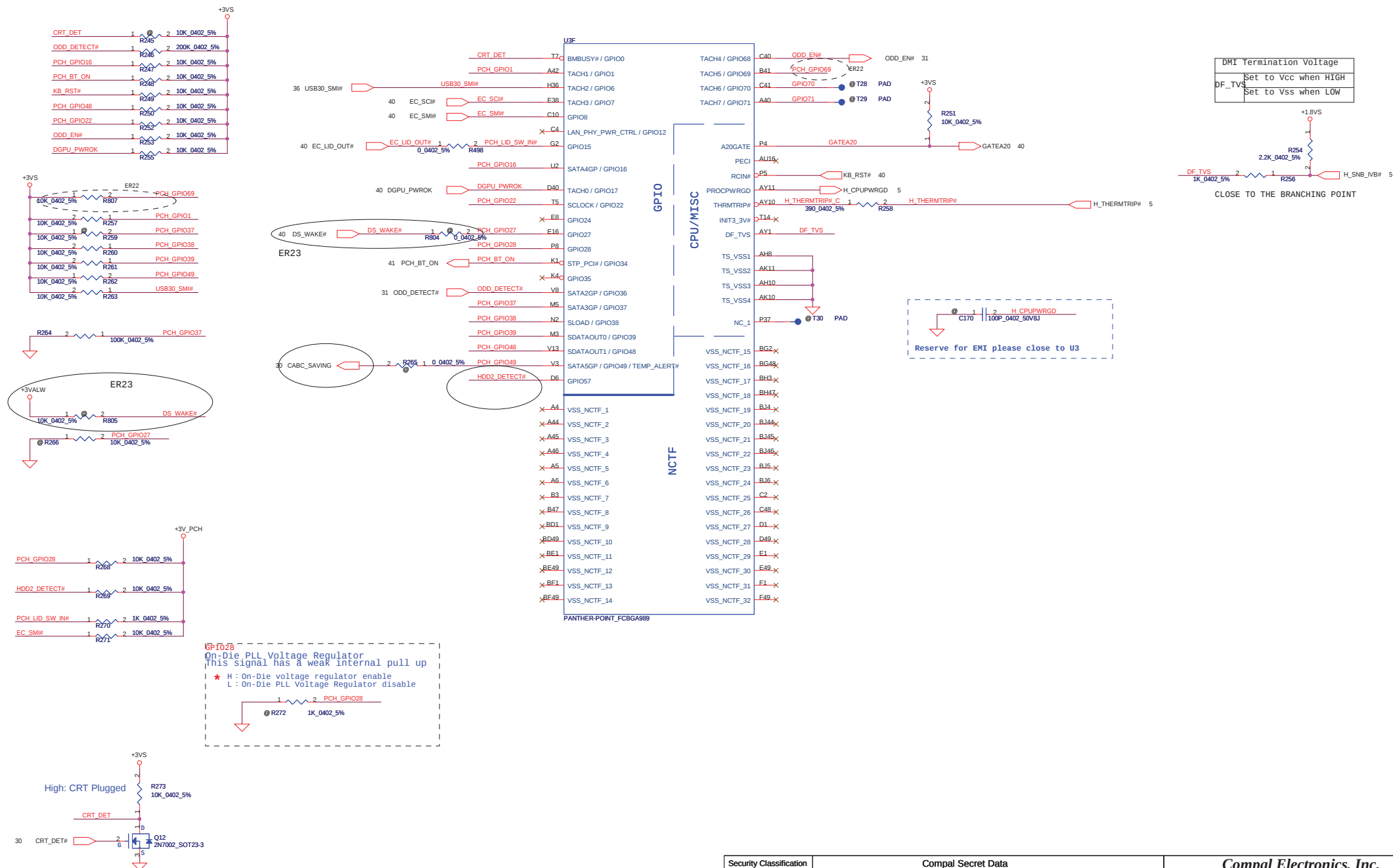
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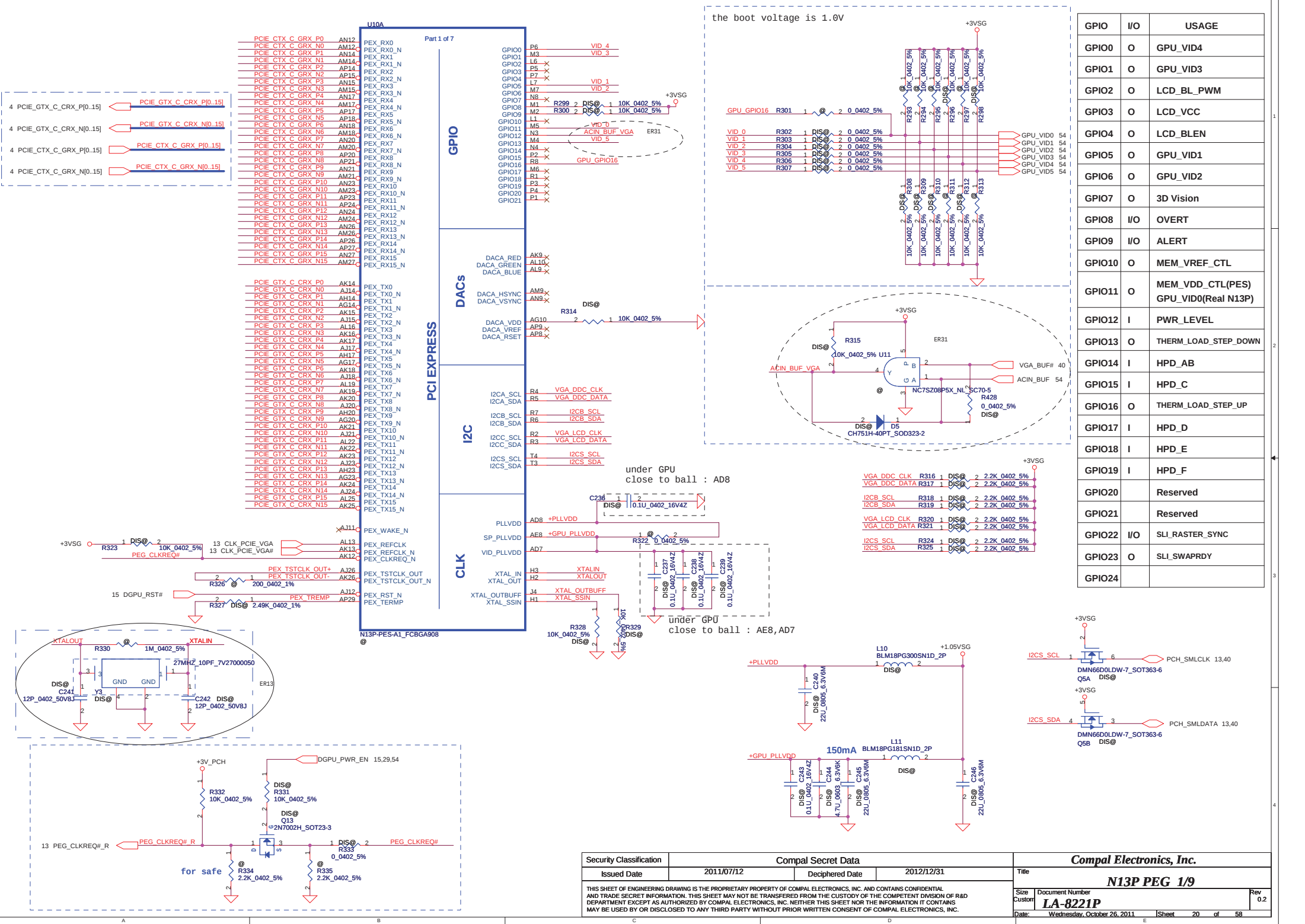
U3H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN3
AD33	VSS[28]	VSS[107] AN31
AD34	VSS[29]	VSS[108] AP12
AD36	VSS[30]	VSS[109] AP19
AD37	VSS[31]	VSS[110] AP28
AD38	VSS[32]	VSS[111] AP30
AD39	VSS[33]	VSS[112] AP32
AD4	VSS[34]	VSS[113] AP38
AD40	VSS[35]	VSS[114] AP4
AD42	VSS[36]	VSS[115] AP42
AD43	VSS[37]	VSS[116] AP46
AD45	VSS[38]	VSS[117] AP8
AD46	VSS[39]	VSS[118] AR2
AD8	VSS[40]	VSS[119] AR48
AE2	VSS[41]	VSS[120] AT11
AE3	VSS[42]	VSS[121] AT13
AE10	VSS[43]	VSS[122] AT18
AE12	VSS[44]	VSS[123] AT22
AD14	VSS[45]	VSS[124] AT26
AD16	VSS[46]	VSS[125] AT28
AE16	VSS[47]	VSS[126] AT30
AE19	VSS[48]	VSS[127] AT32
AE24	VSS[49]	VSS[128] AT34
AE26	VSS[50]	VSS[129] AT39
AE27	VSS[51]	VSS[130] AT42
AE29	VSS[52]	VSS[131] AT46
AE31	VSS[53]	VSS[132] AT7
AE38	VSS[54]	VSS[133] AU24
AF4	VSS[55]	VSS[134] AU30
AF42	VSS[56]	VSS[135] AV16
AF46	VSS[57]	VSS[136] AV20
AF5	VSS[58]	VSS[137] AV24
AF7	VSS[59]	VSS[138] AV30
AF3	VSS[60]	VSS[139] AV38
AG19	VSS[61]	VSS[140] AV4
AG2	VSS[62]	VSS[141] AV43
AG31	VSS[63]	VSS[142] AV8
AG48	VSS[64]	VSS[143] AW14
AH11	VSS[65]	VSS[144] AW18
AH3	VSS[66]	VSS[145] AW2
AH36	VSS[67]	VSS[146] AW22
AH39	VSS[68]	VSS[147] AW26
AH40	VSS[69]	VSS[148] AW28
AH42	VSS[70]	VSS[149] AW32
AH46	VSS[71]	VSS[150] AW34
AH7	VSS[72]	VSS[151] AW38
AJ19	VSS[73]	VSS[152] AW40
AJ21	VSS[74]	VSS[153] AW48
AJ24	VSS[75]	VSS[154] AV11
AJ33	VSS[76]	VSS[155] AY12
AJ34	VSS[77]	VSS[156] AY22
AK12	VSS[78]	VSS[157] AY28
AK3	VSS[79]	VSS[158]

PANTHER-POINT_FCBGA989

U3I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L13
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] P16
BB16	VSS[174]	VSS[274] M18
BB20	VSS[175]	VSS[275] M22
BB22	VSS[176]	VSS[276] M24
BB24	VSS[177]	VSS[277] M30
BB28	VSS[178]	VSS[278] M32
BB30	VSS[179]	VSS[279] M34
BB38	VSS[180]	VSS[280] M38
BB4	VSS[181]	VSS[281] M4
BB46	VSS[182]	VSS[282] M42
BC14	VSS[183]	VSS[283] M46
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] P20
BC26	VSS[187]	VSS[287] N47
BC32	VSS[188]	VSS[288] P11
BC34	VSS[189]	VSS[289] P18
BC36	VSS[190]	VSS[290] T33
BC40	VSS[191]	VSS[291] P40
BC42	VSS[192]	VSS[292] P43
BC48	VSS[193]	VSS[293] P47
BD46	VSS[194]	VSS[294] P7
BD5	VSS[195]	VSS[295] R2
BE22	VSS[196]	VSS[296] R48
BE26	VSS[197]	VSS[297] T12
BE40	VSS[198]	VSS[298] T31
BE10	VSS[199]	VSS[299] T37
BE12	VSS[200]	VSS[300] T4
BE16	VSS[201]	VSS[301] W34
BE20	VSS[202]	VSS[302] T46
AP8	VSS[203]	VSS[303] T47
BE24	VSS[204]	VSS[304] T8
BE26	VSS[205]	VSS[305] V11
BE28	VSS[206]	VSS[306] V17
BD3	VSS[207]	VSS[307] V26
BE30	VSS[208]	VSS[308] V27
BE38	VSS[209]	VSS[309] V29
BE40	VSS[210]	VSS[310] V31
BE4	VSS[211]	VSS[311] V36
BG17	VSS[212]	VSS[312] V39
BG21	VSS[213]	VSS[313] V43
BG33	VSS[214]	VSS[314] V7
BG44	VSS[215]	VSS[315] W17
BG8	VSS[216]	VSS[316] W19
BH11	VSS[217]	VSS[317] W2
BH15	VSS[218]	VSS[318] W27
BH17	VSS[219]	VSS[319] W48
BH19	VSS[220]	VSS[320] Y12
H10	VSS[221]	VSS[321] Y38
BH27	VSS[222]	VSS[322] Y4
BH31	VSS[223]	VSS[323] Y42
AV30	VSS[224]	VSS[324] Y46
BH35	VSS[225]	VSS[325] Y8
BH39	VSS[226]	VSS[326] BG29
BH43	VSS[227]	VSS[327] N24
BH7	VSS[228]	VSS[328] A33
D3	VSS[229]	VSS[329] AD47
D12	VSS[230]	VSS[330] B43
D16	VSS[231]	VSS[331] BE10
D18	VSS[232]	VSS[332] BG41
D22	VSS[233]	VSS[333] G14
D24	VSS[234]	VSS[334] H16
D26	VSS[235]	VSS[335] I36
D30	VSS[236]	VSS[336] BG22
D32	VSS[237]	VSS[337] BG24
D34	VSS[238]	VSS[338] C22
D38	VSS[239]	VSS[339] AP13
D42	VSS[240]	VSS[340] M14
D8	VSS[241]	VSS[341] AP3
E18	VSS[242]	VSS[342] AP3
E26	VSS[243]	VSS[343] BE16
G18	VSS[244]	VSS[344] BC16
G20	VSS[245]	VSS[345] BG28
G26	VSS[246]	VSS[346] BJ28
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

PANTHER-POINT_FCBGA989

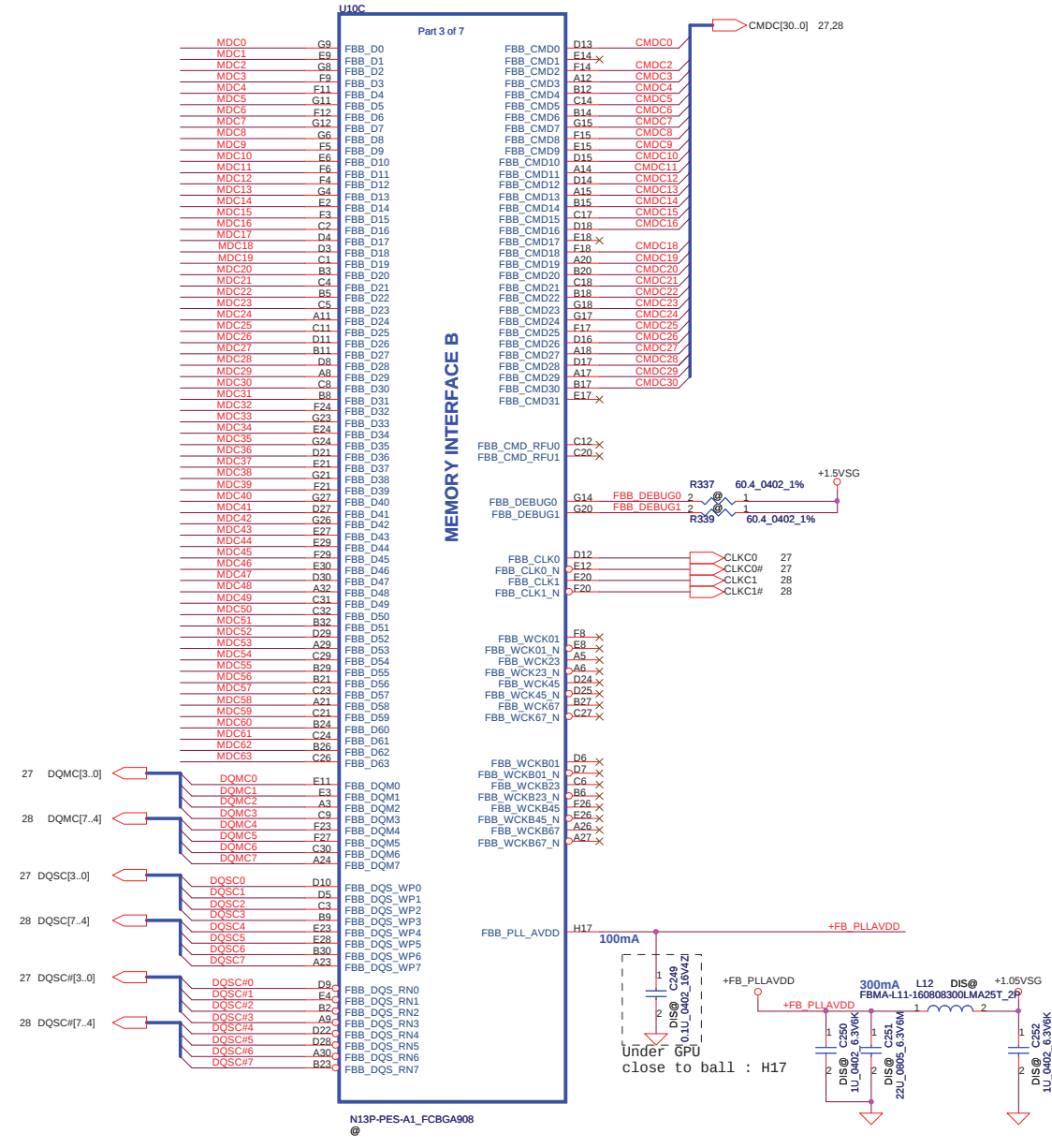
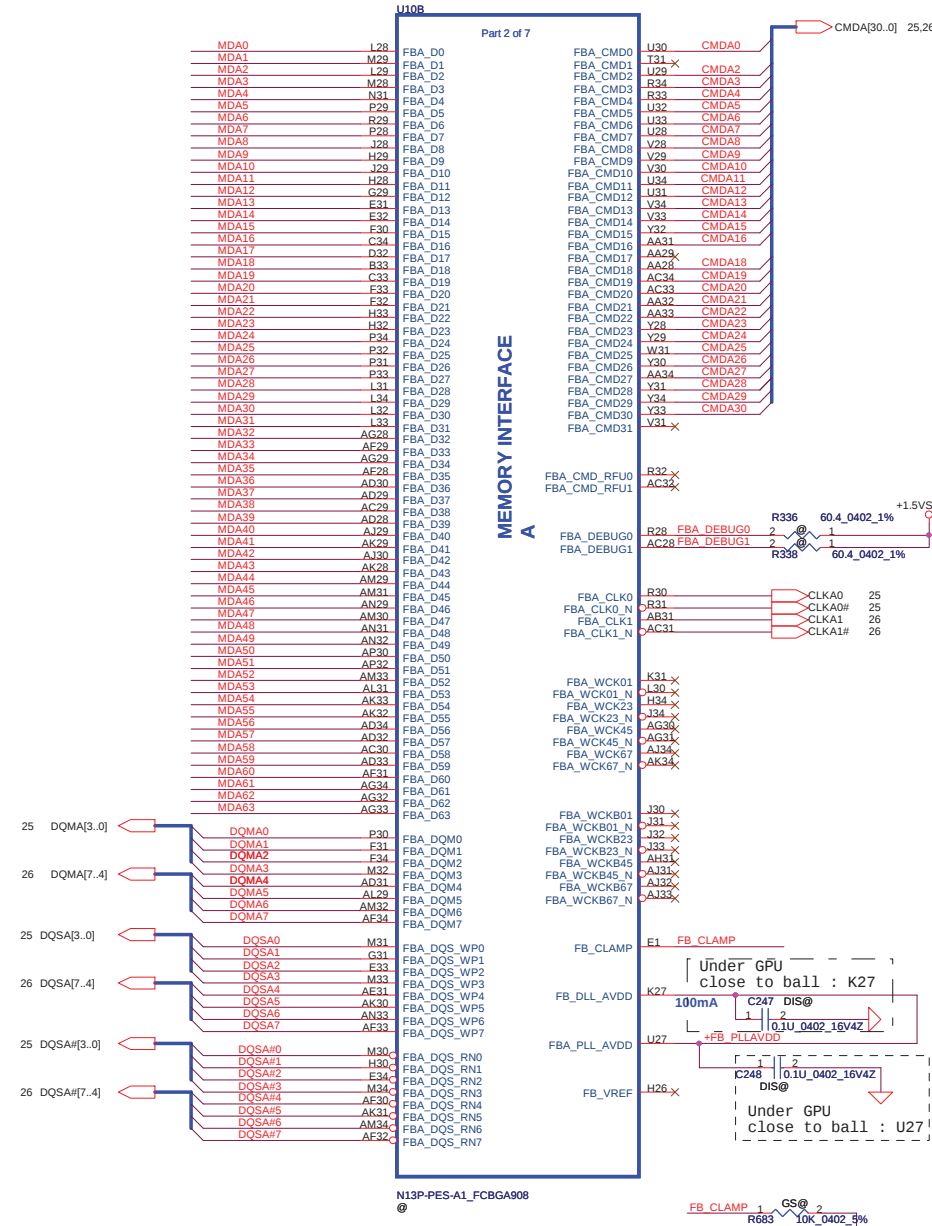
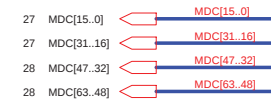
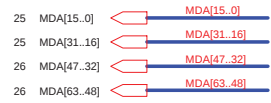
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

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Size	Document Number	Rev				
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VRAM Interface

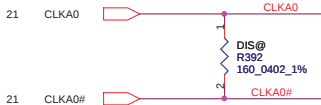
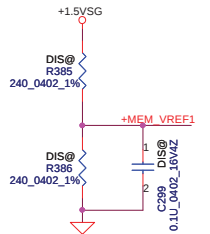
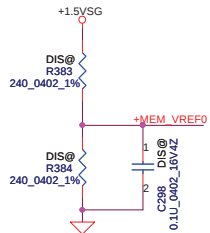


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Issued Date			2011/07/12	Deciphered Date	2012/12/31	
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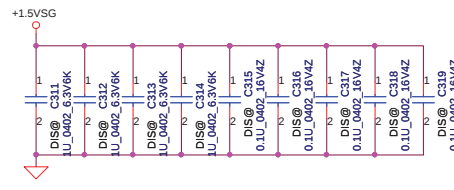
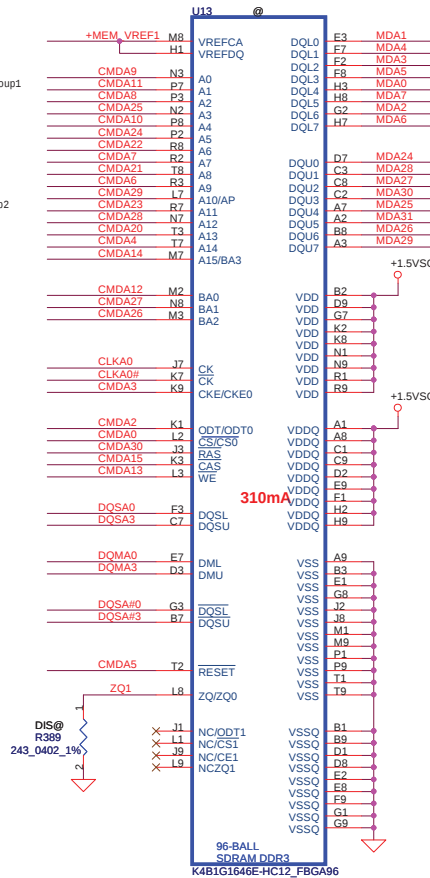
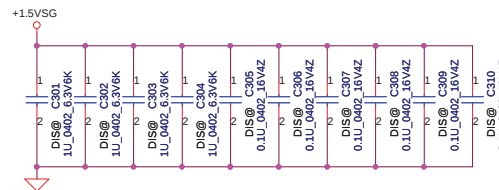
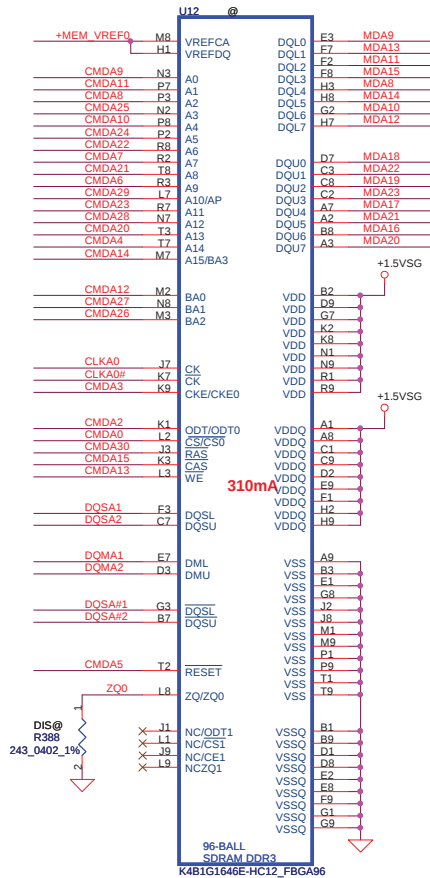
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

21.26 DQSA[7..0] DQSA[7..0]
21.26 DQSA[17..0] DQSA[17..0]
21.26 DQMA[7..0] DQMA[7..0]
21.26 MDA[63..0] MDA[63..0]
21.26 CMDA[30..0] CMDA[30..0]



NV recommend 6720



CMDA2 R390 1 DIS@ 2 10K 0402 5%
CMDA3 R391 1 DIS@ 2 10K 0402 5%
CMDA5 R393 1 DIS@ 2 10K 0402 5%
CMDA18 R394 1 DIS@ 2 10K 0402 5%
CMDA19 R395 1 DIS@ 2 10K 0402 5%

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

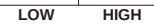
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD : SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

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128Mx16 DDR3 *8==>2GB

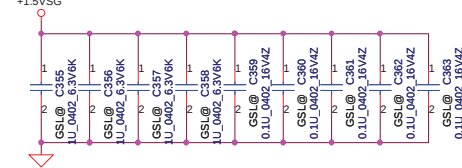
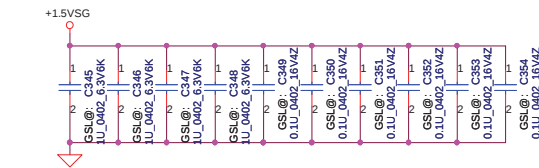
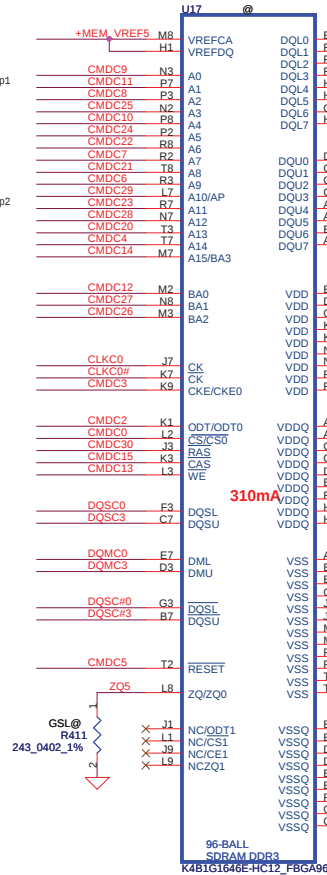
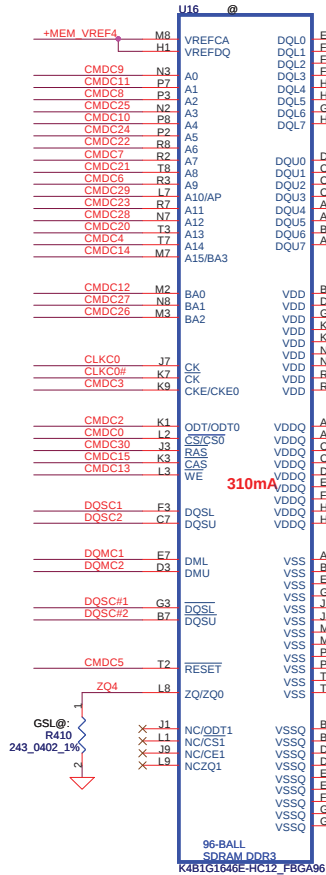
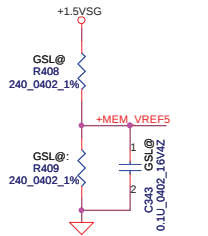
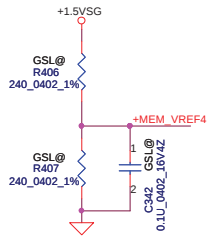


VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

21.28 DQSC[7..0] DQSC[7..0]
21.28 DQSC# [7..0] DQSC# [7..0]
21.28 DQMC[7..0] DQMC[7..0]
21.28 MDC[63..0] MDC[63..0]
21.28 CMDC[30..0] CMDC[30..0]



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

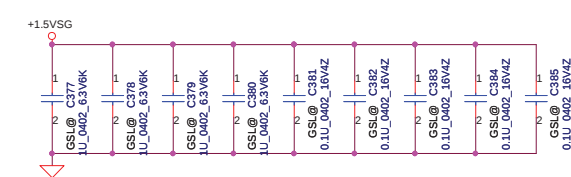
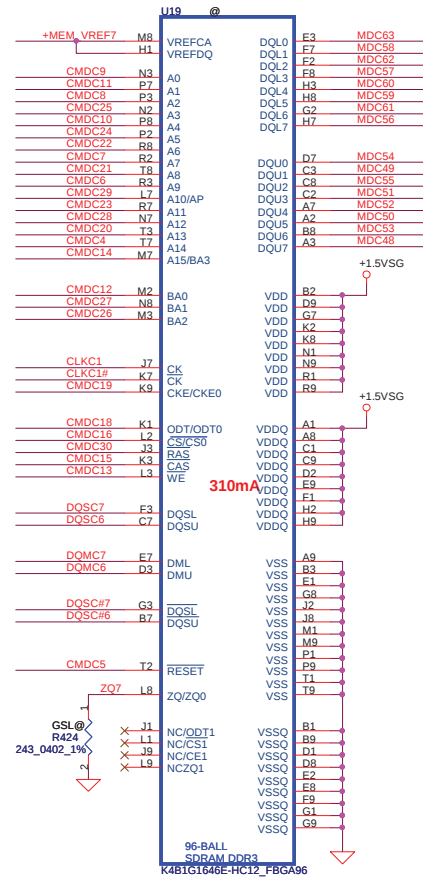
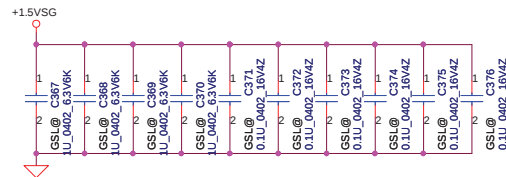
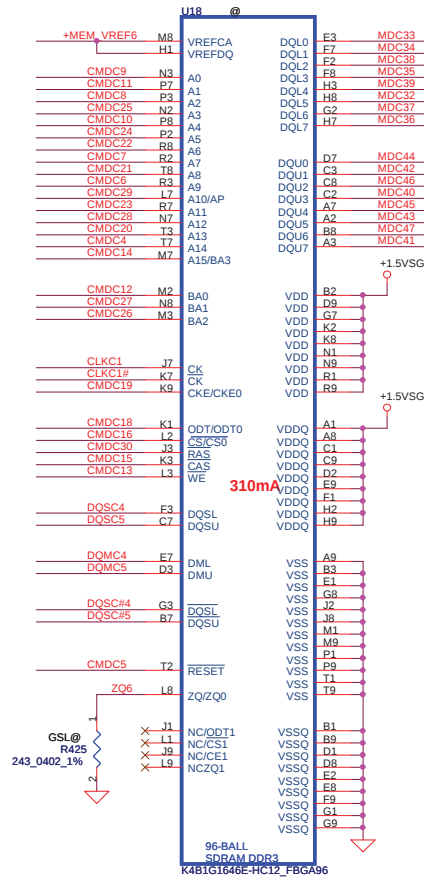
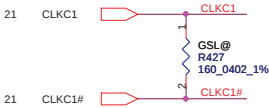
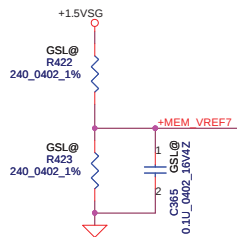
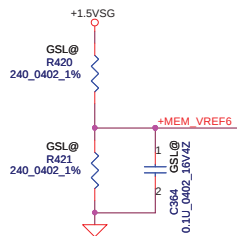
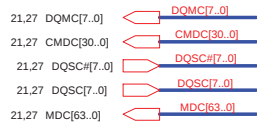
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEX	10k
	RST	10k
	CS*	No Termination

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				Rev	0.2

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

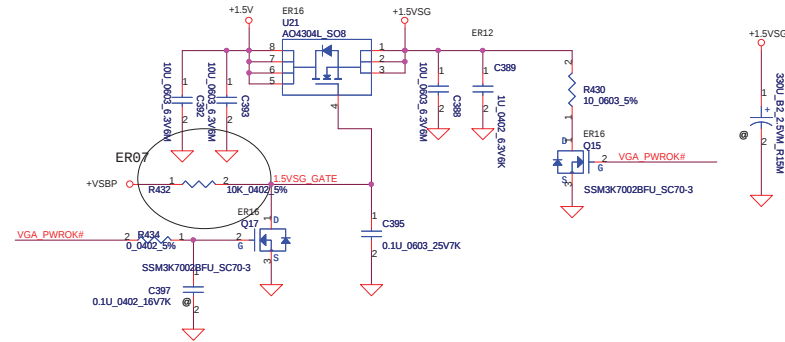


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

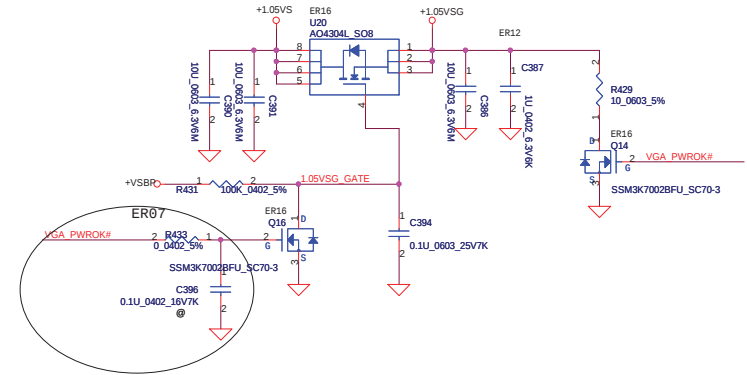
LOW HIGH

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				Date	Wednesday, October 26, 2011	Sheet 28 of 58

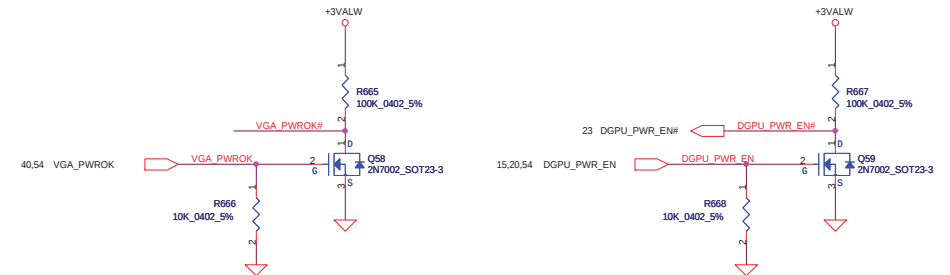
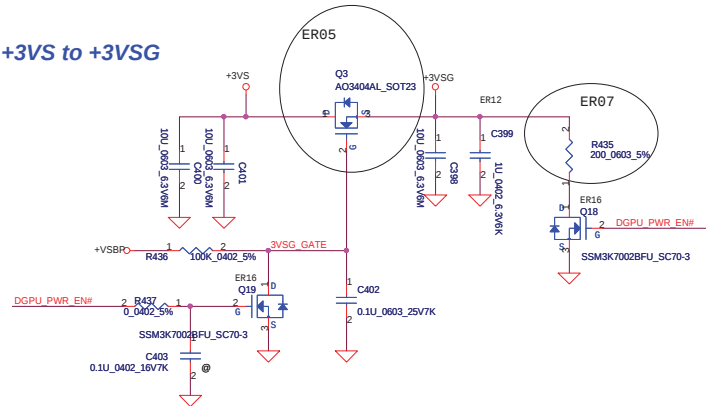
+1.5V to +1.5VSG



+VCCP to +1.05VSG

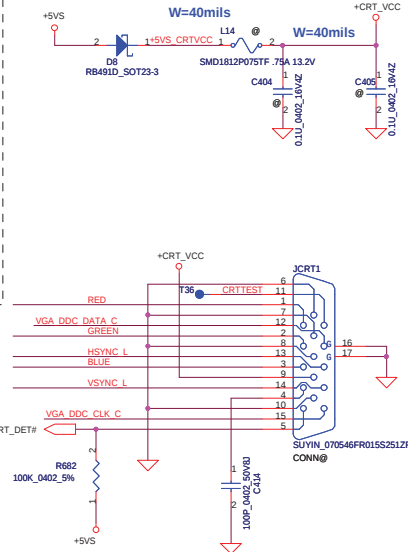
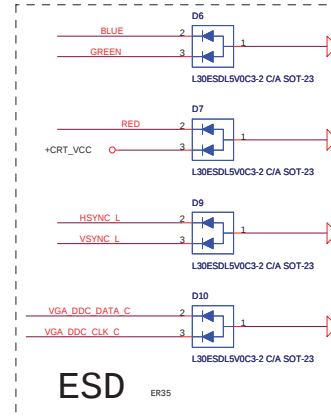
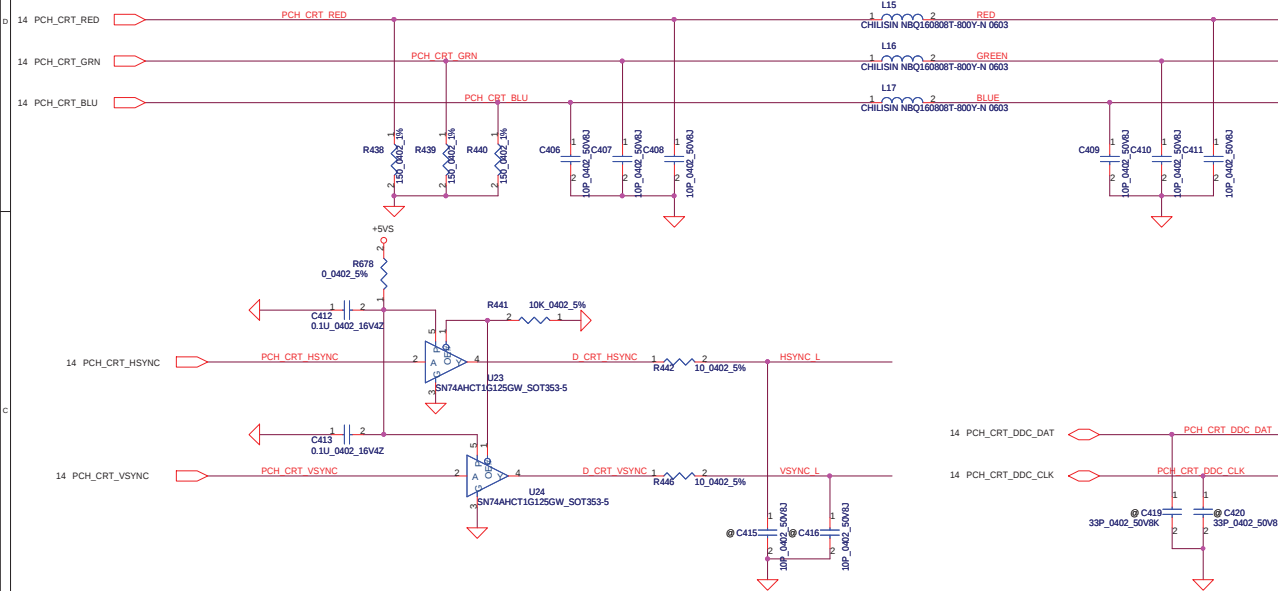


+3VS to +3VSG

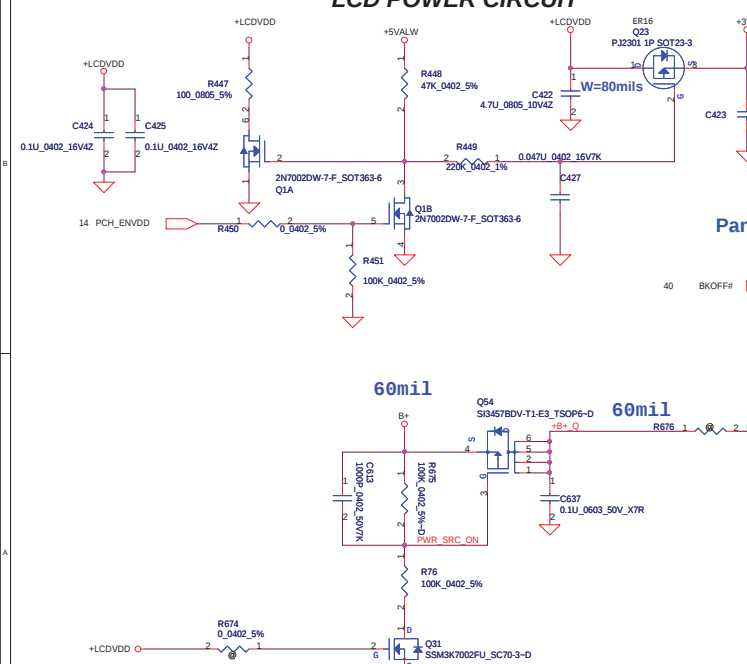


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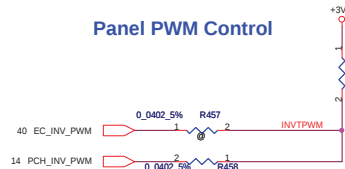
CRT



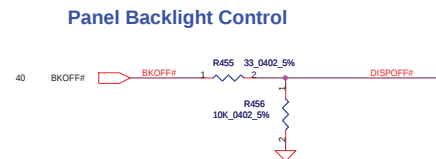
LCD POWER CIRCUIT



Panel PWM Control

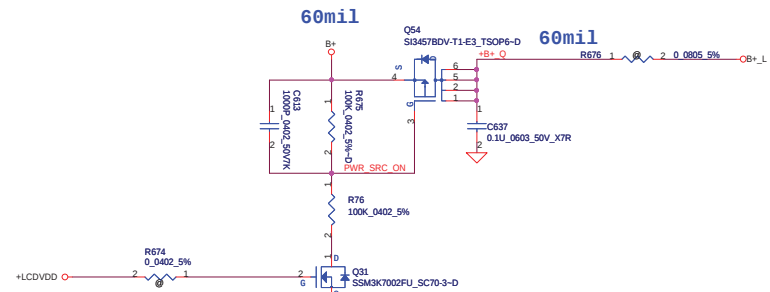


Panel Backlight Control

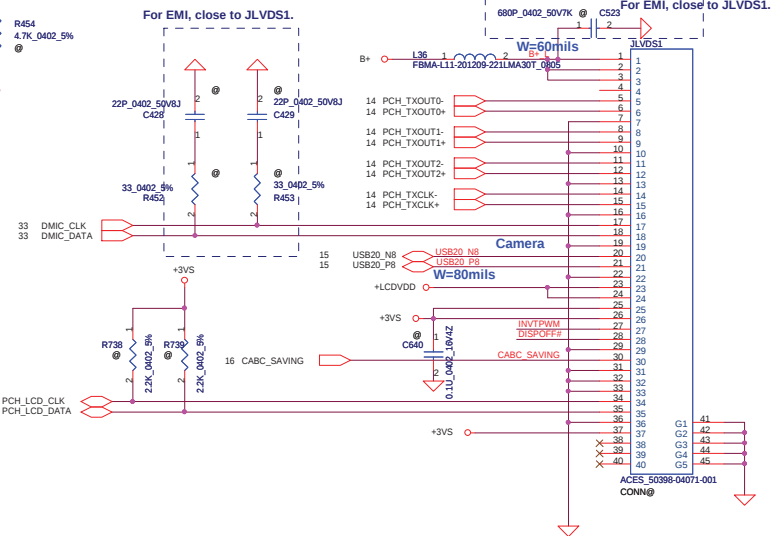


60mil

60mil

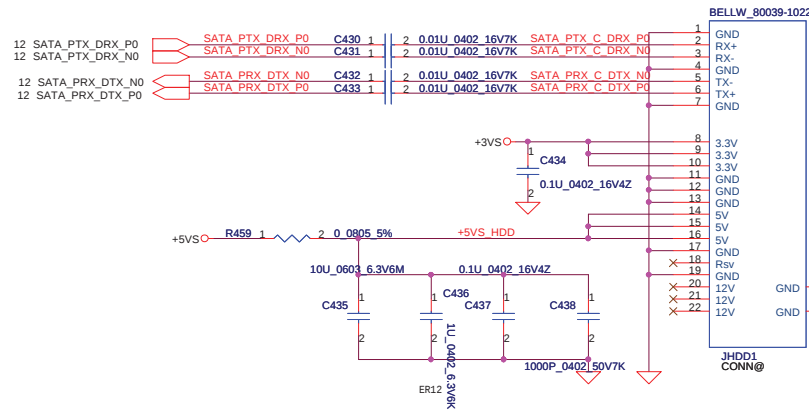


For EMI, close to JLVDS1.

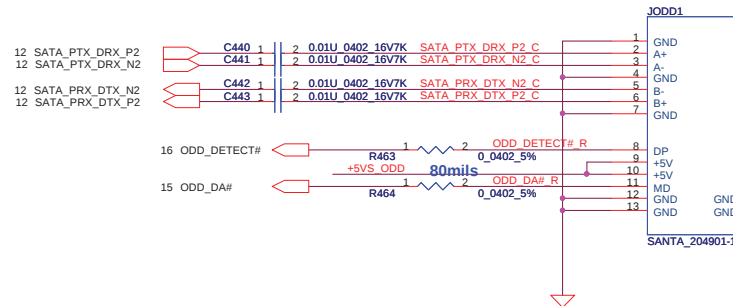


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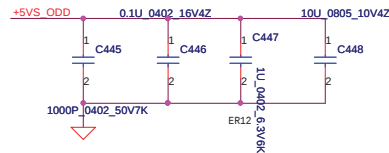
SATA HDD Conn.



SATA ODD Conn.



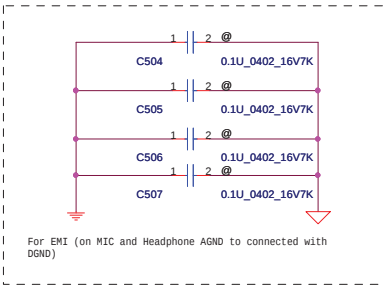
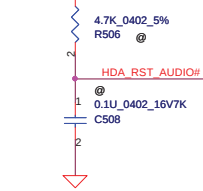
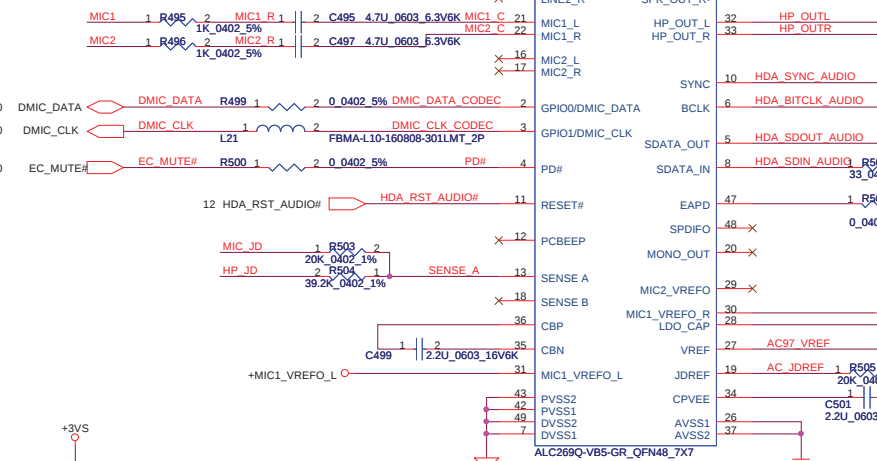
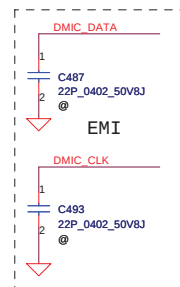
Place caps. near ODD CONN.



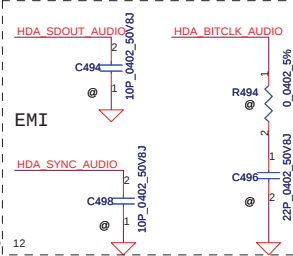
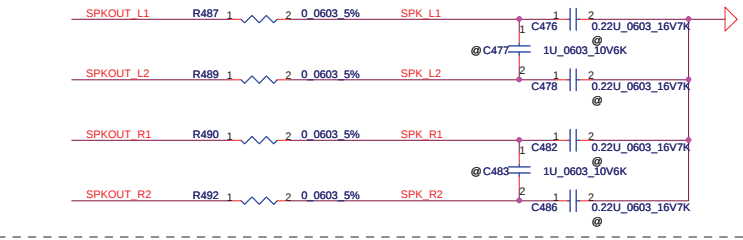
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	HDD & ODD CONN	
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Compal Electronics, Inc.

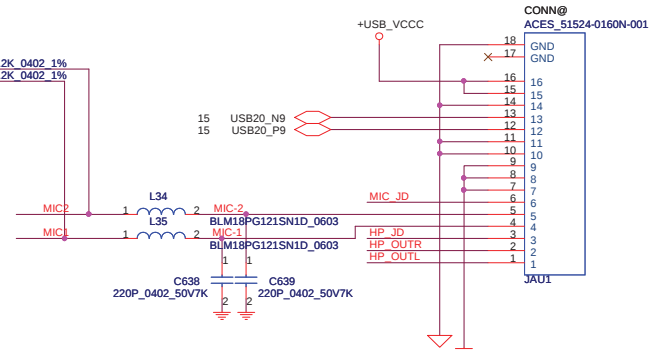
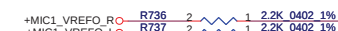
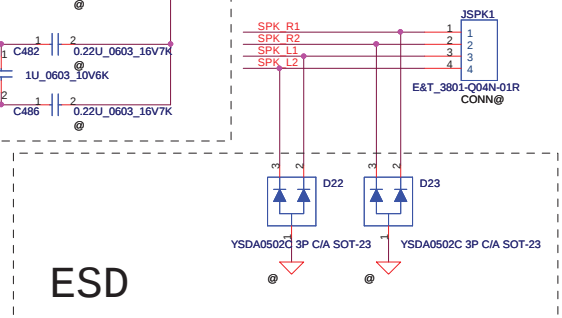
Rev 0.2



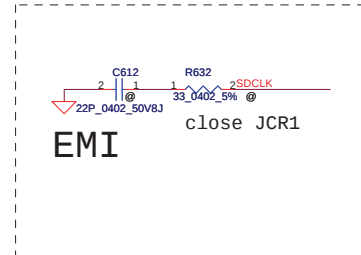
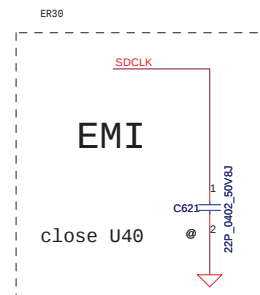
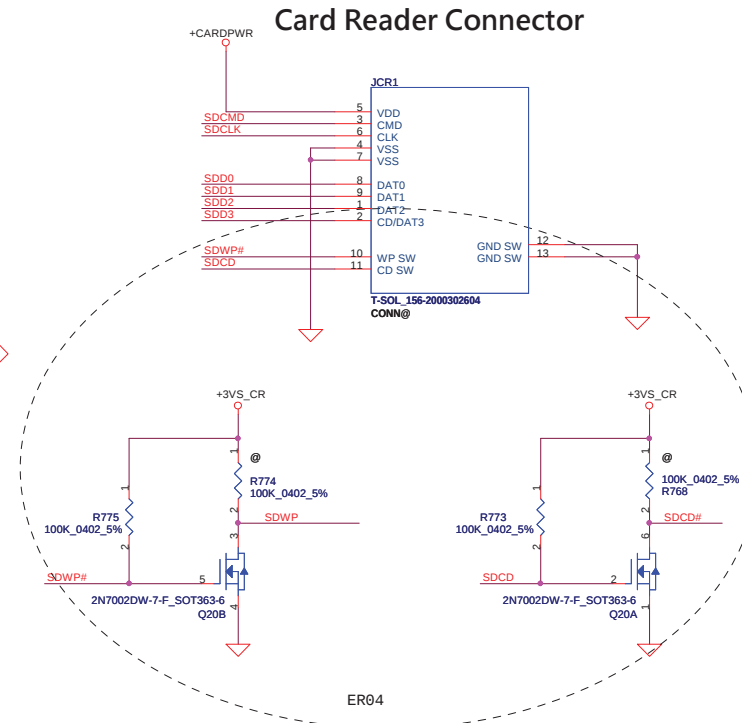
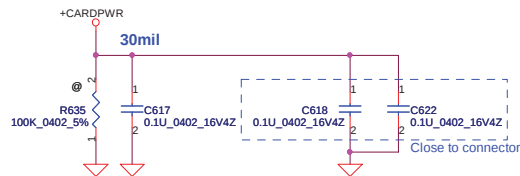
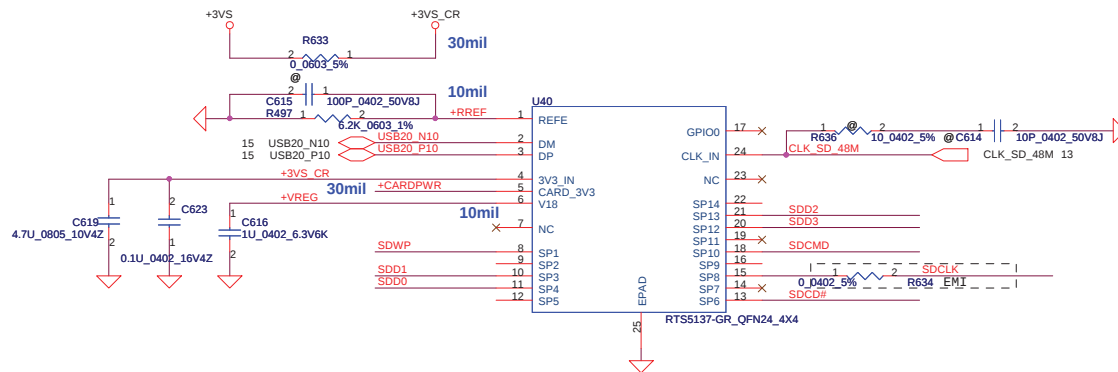
EMI



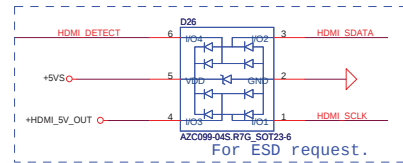
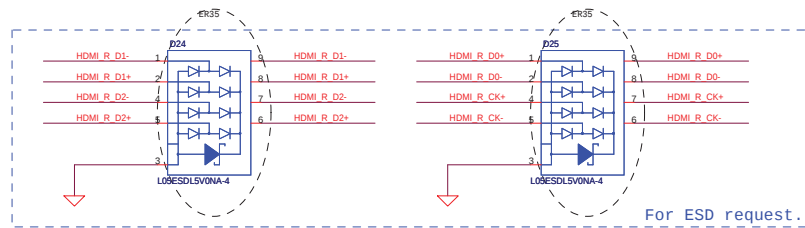
ESD



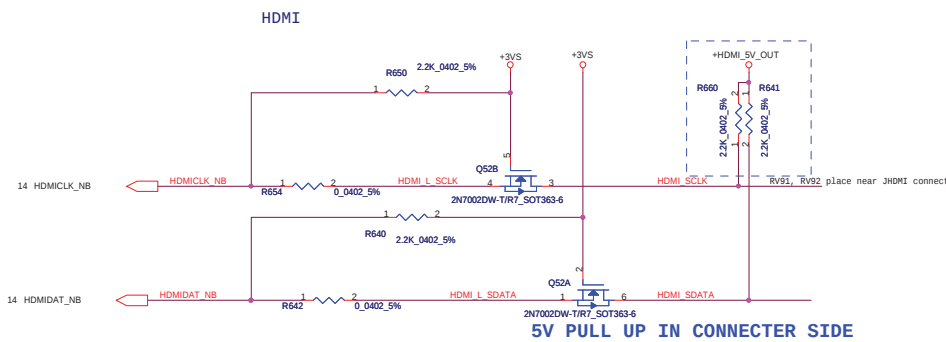
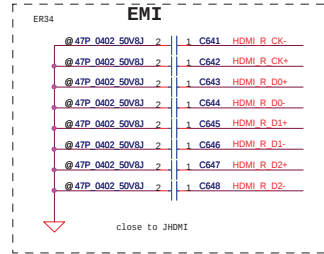
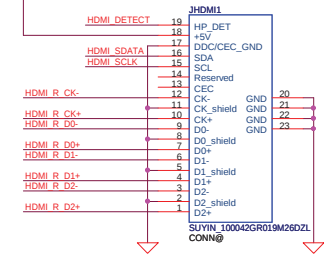
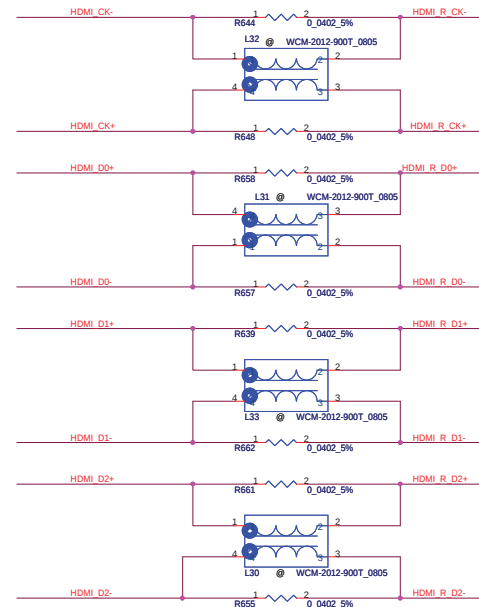
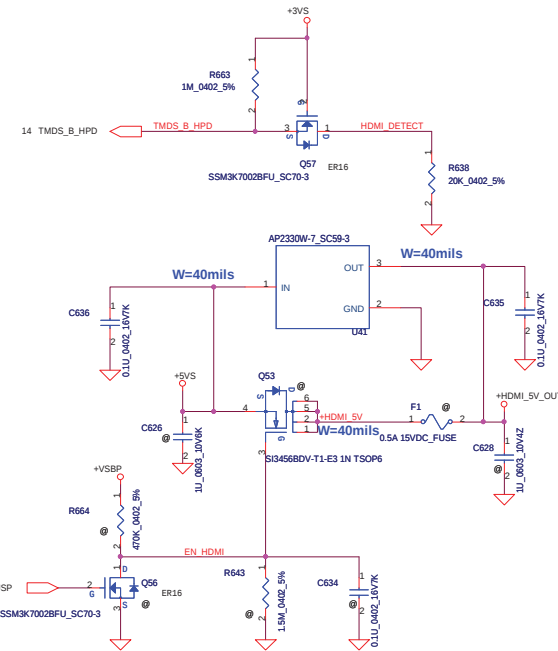
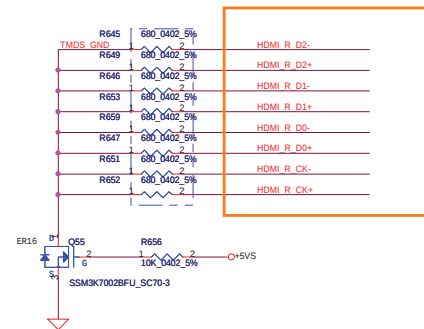
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/07/12		Deciphered Date		2012/12/31		Title			
								HD CODEC ALC269			
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		Size		Document Number						Rev	
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14	TMDS_B_CLK	0.1U 0402 16V7K	2	1	C625	HDMI CK+
14	TMDS_B_CLK#	0.1U 0402 16V7K	2	1	C624	HDMI CK-
14	TMDS_B_DATA0	0.1U 0402 16V7K	2	1	C630	HDMI D0+
14	TMDS_B_DATA0#	0.1U 0402 16V7K	2	1	C631	HDMI D0-
14	TMDS_B_DATA1	0.1U 0402 16V7K	2	1	C633	HDMI D1+
14	TMDS_B_DATA1#	0.1U 0402 16V7K	2	1	C627	HDMI D1-
14	TMDS_B_DATA2	0.1U 0402 16V7K	2	1	C629	HDMI D2+
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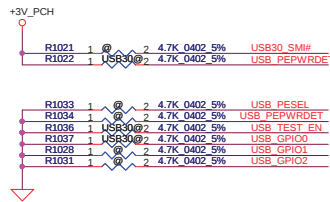
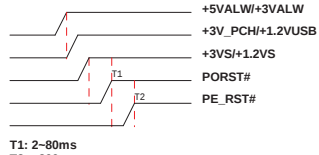


5V PULL UP IN CONNECTOR SIDE

Security Classification	Compal Secret Data	Title	HDMI Connector
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	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

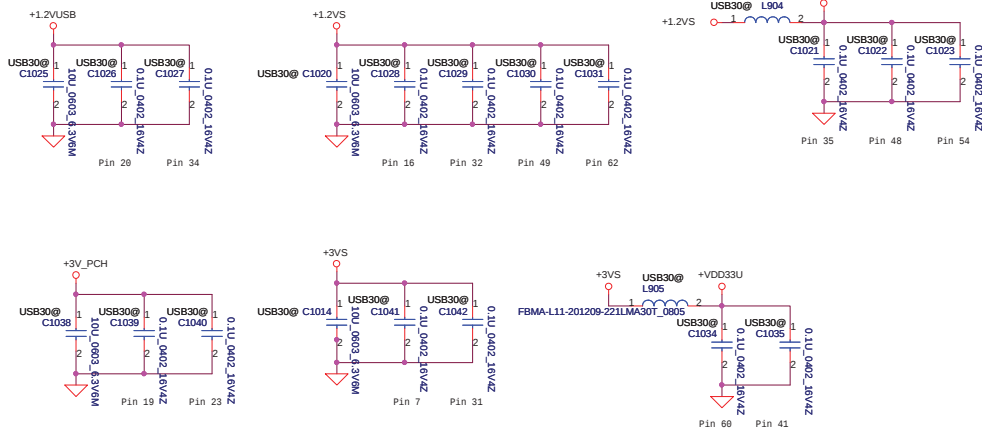
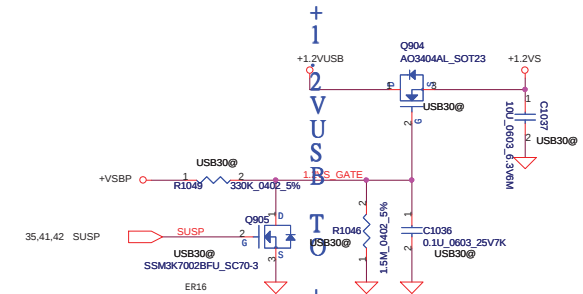
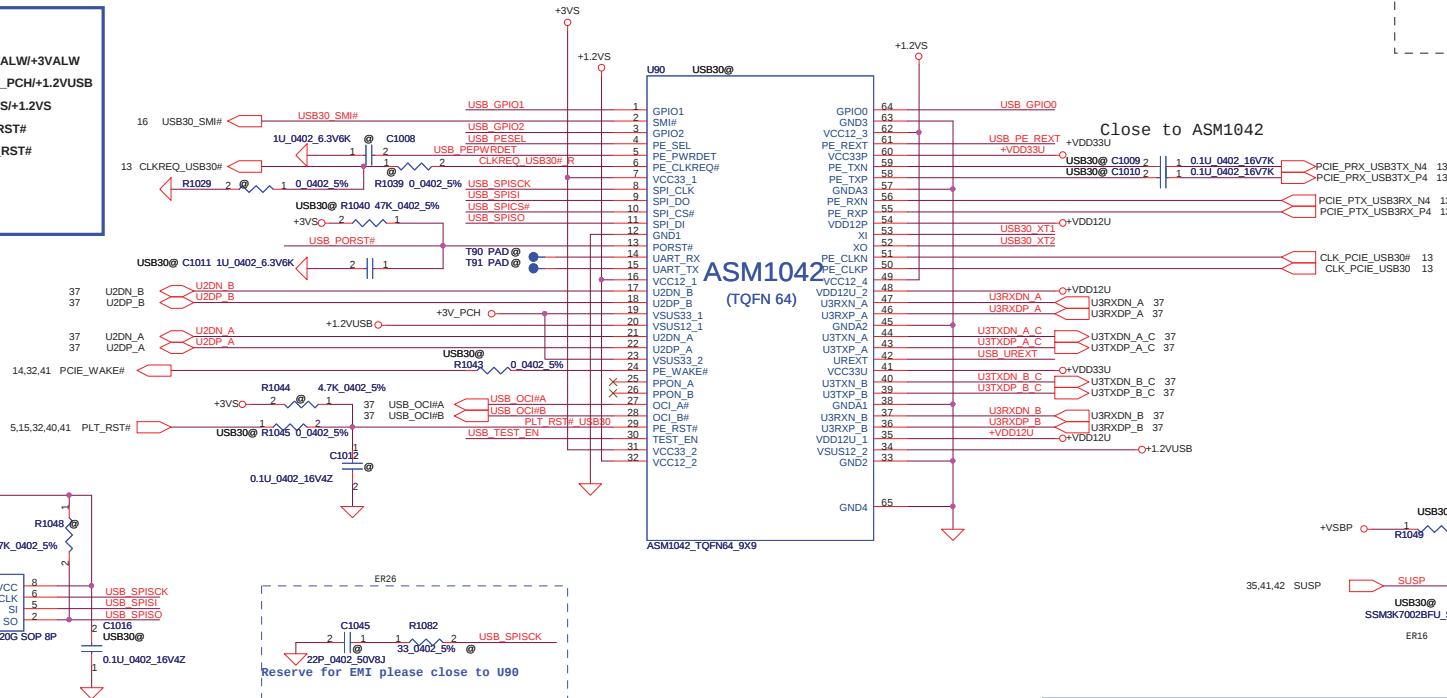
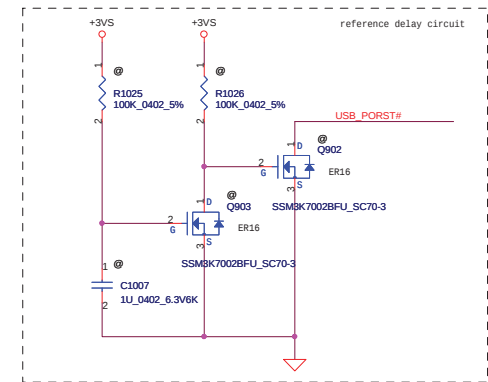
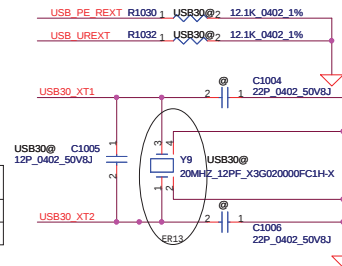
ASM1042



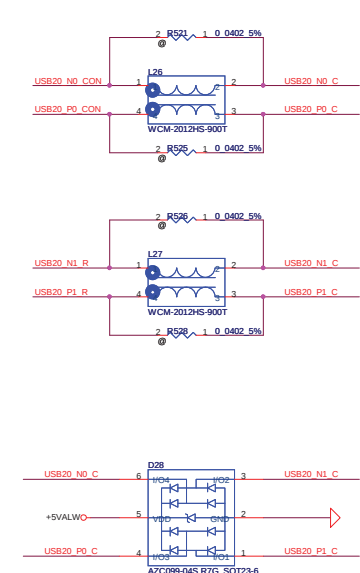
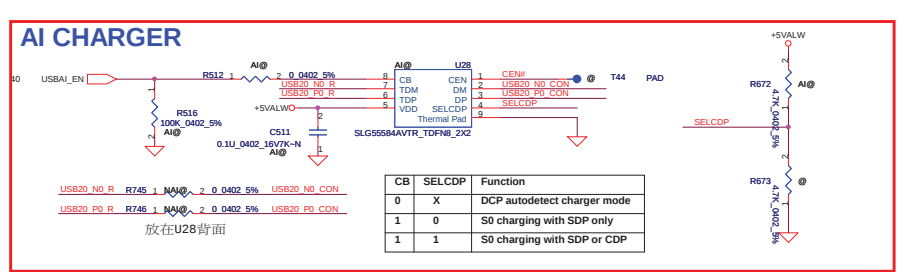
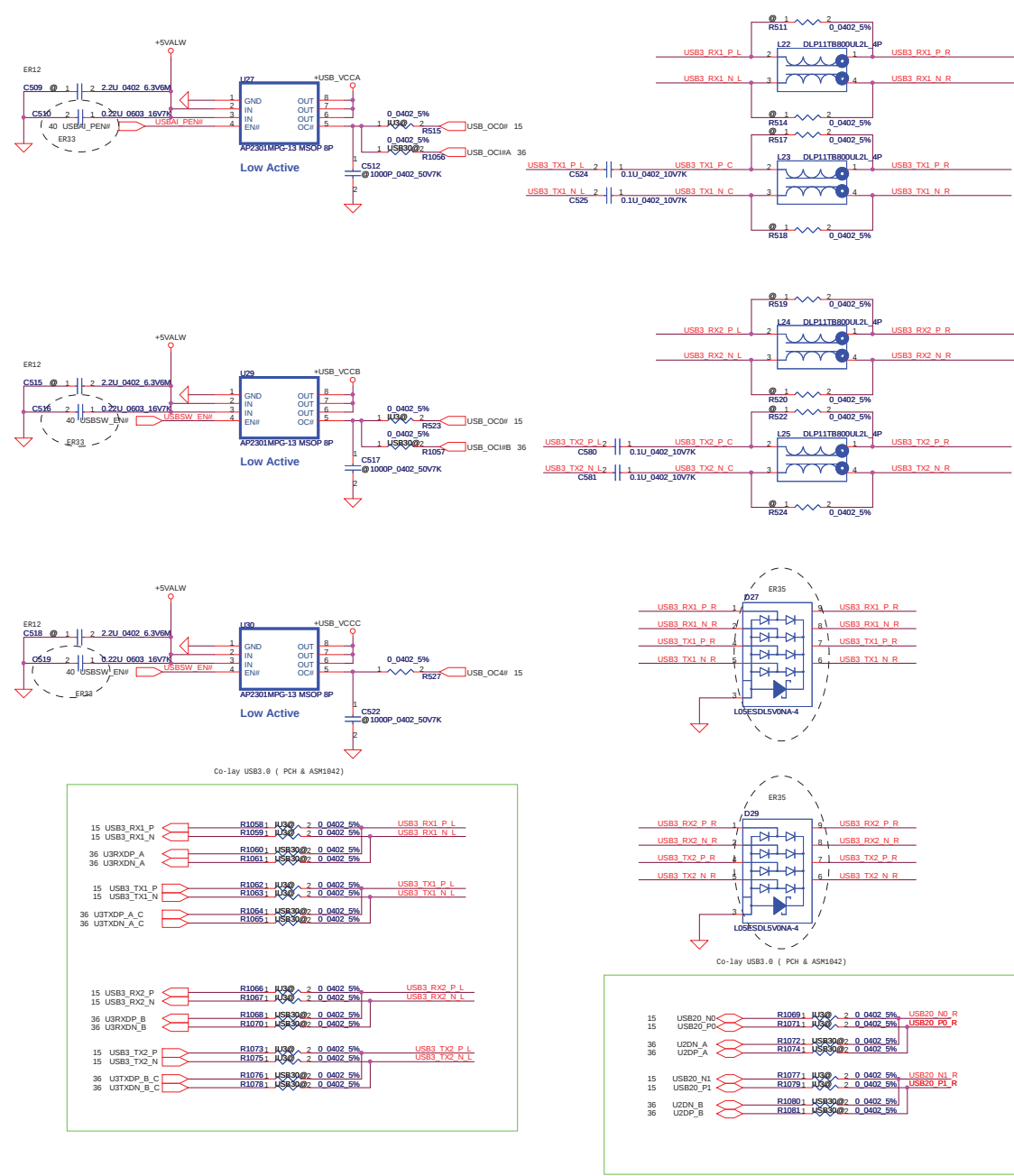
USB_PEPWRDET

	R1034	R1022
S1	Mount	@
* S3	@	Mount

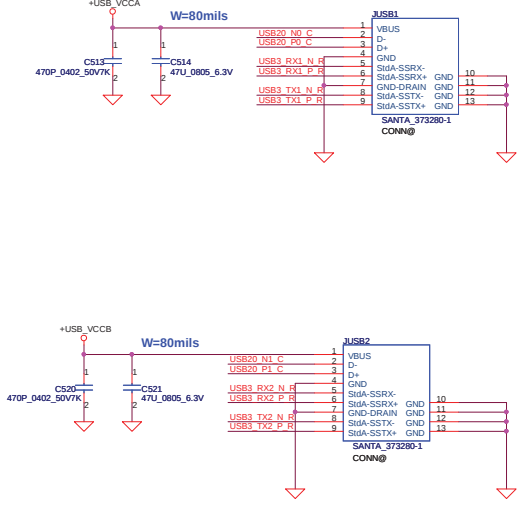
	R1033
* Other applaction	@
Express Card/Mini Card	Mount



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Issued Date	2010/01/	Deciphered Date	2012/06/30	Title USB3.0 controller		
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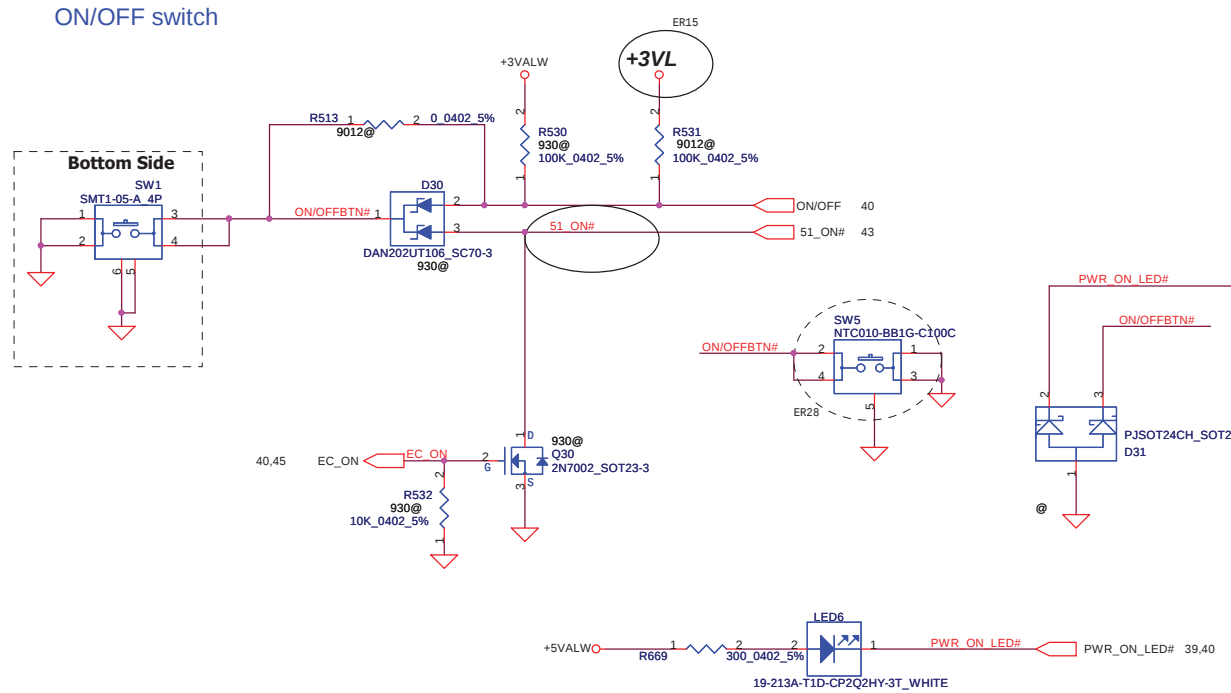
charger port: left side & near user



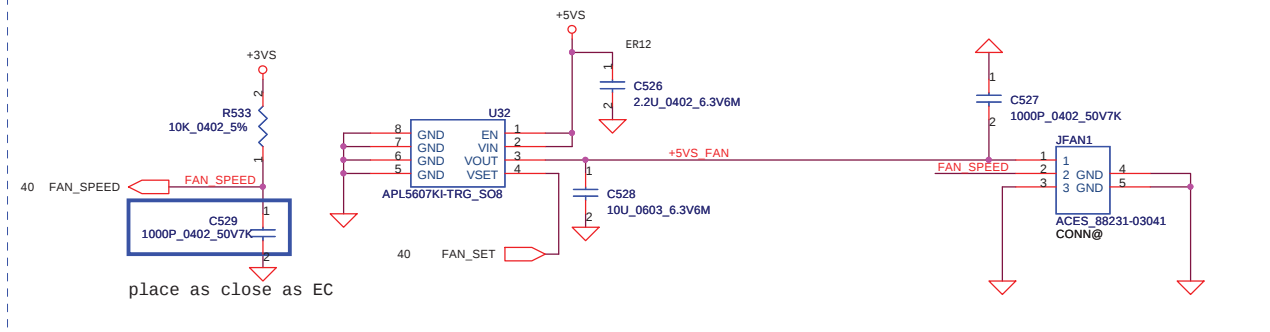
ER02 Add USB3.0 (ASM1042)

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				1A-8221P
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				0.2
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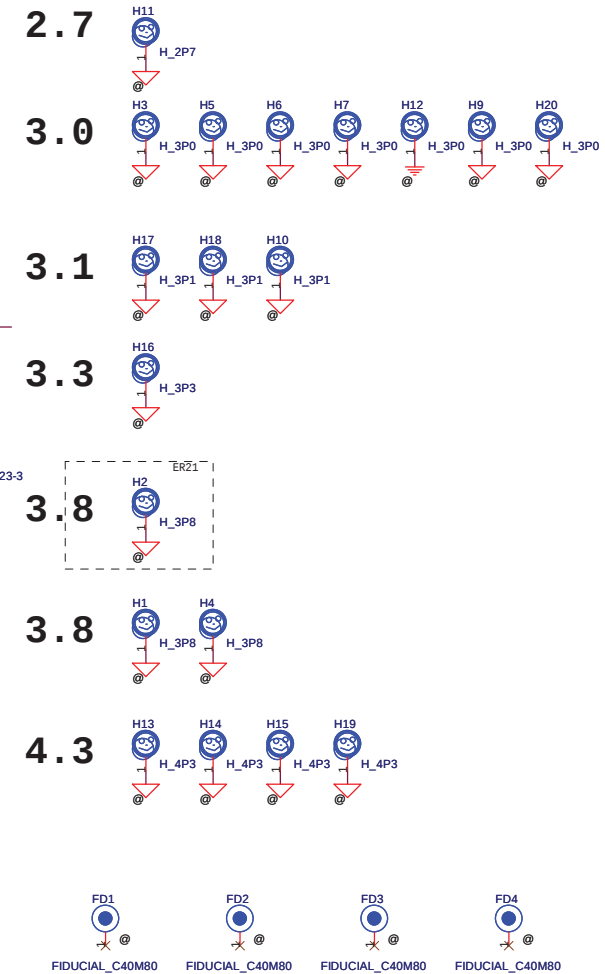
Power Button



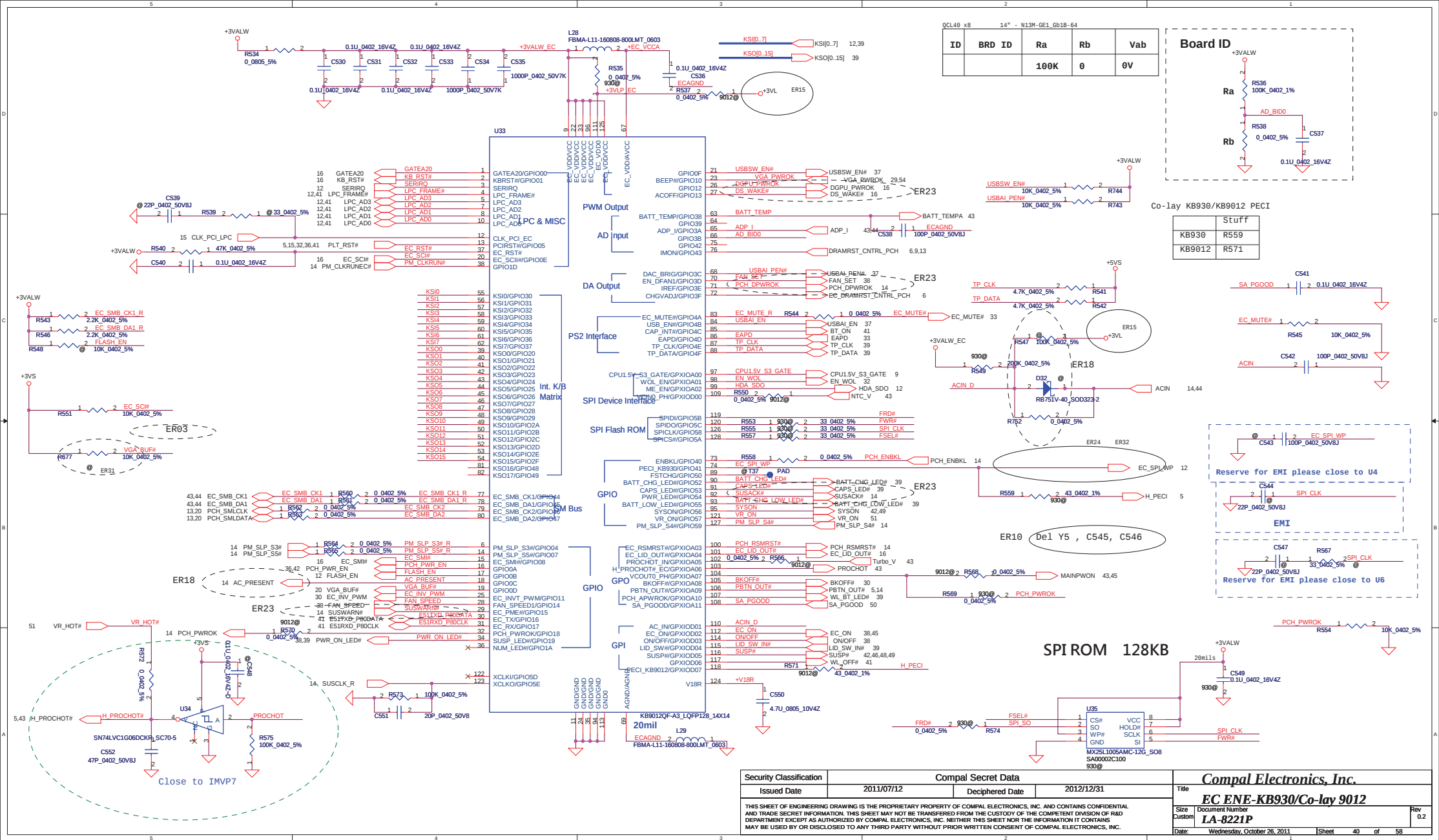
Fan Control Circuit

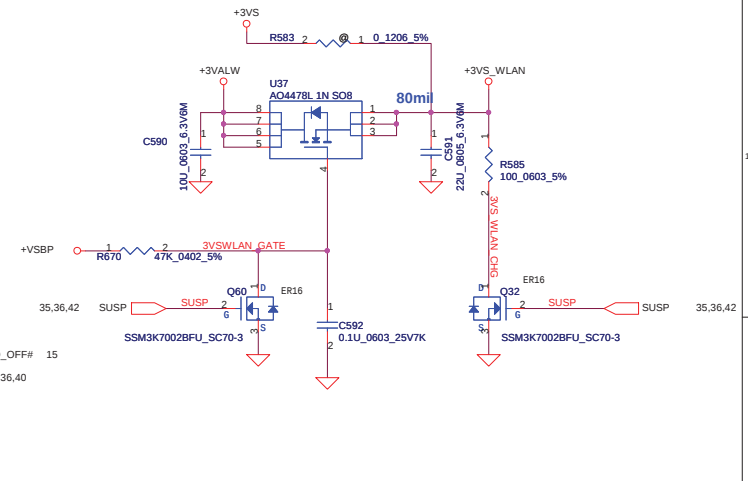


Screw Hole

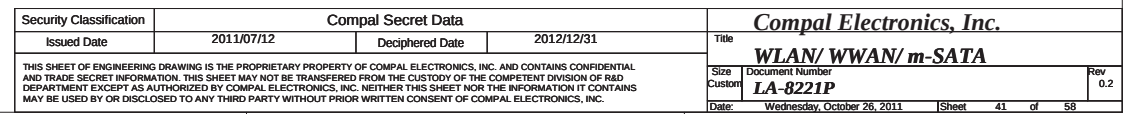


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title		
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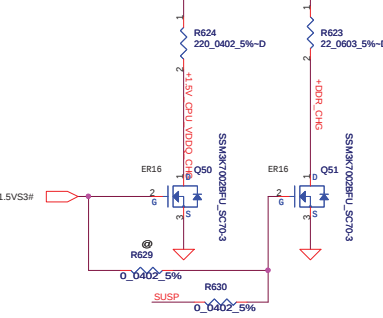
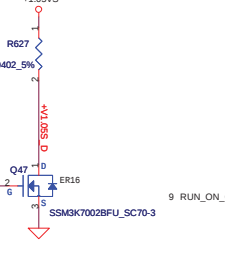
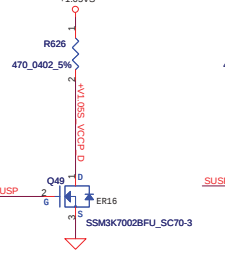
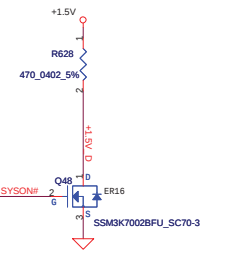
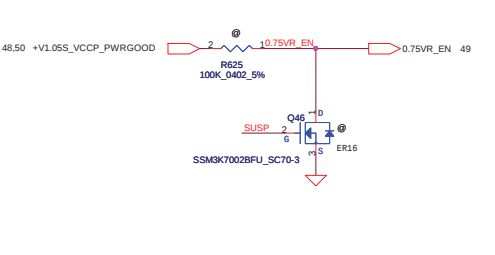
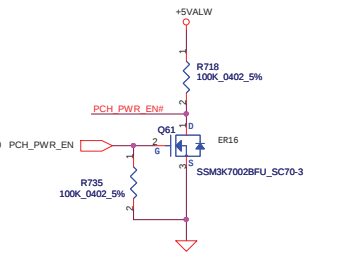
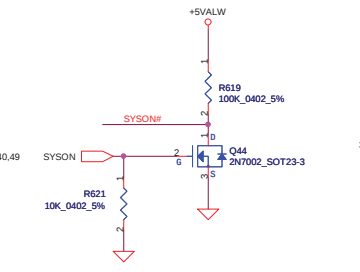
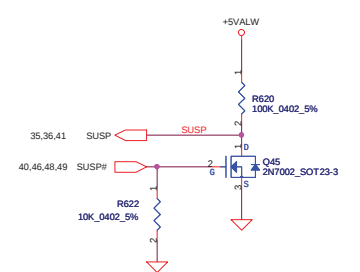
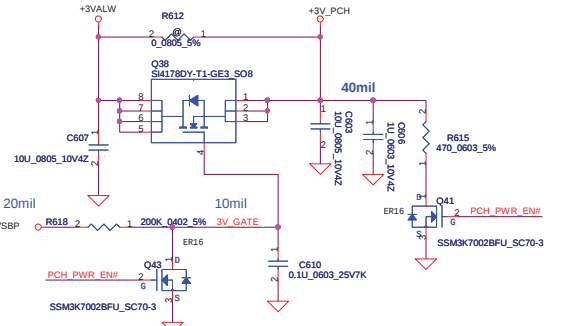
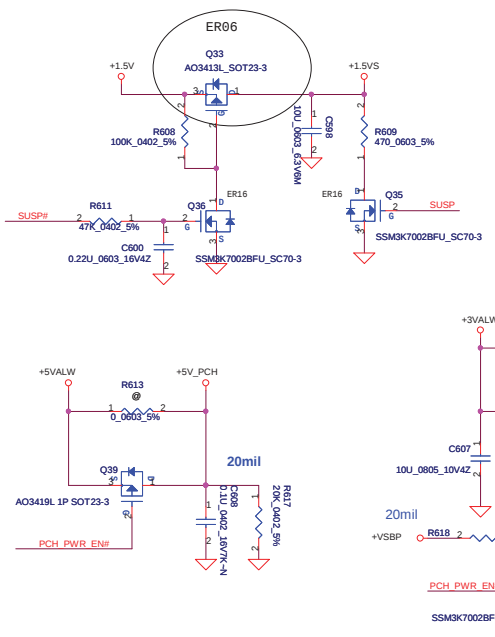
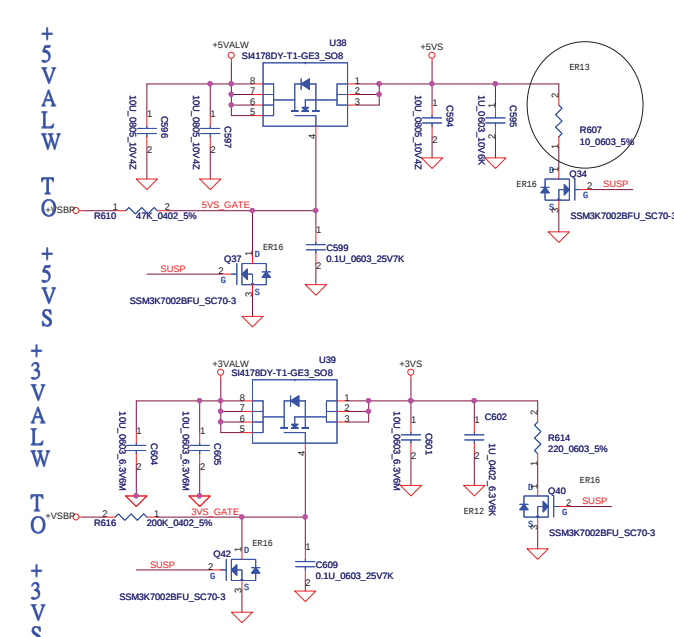


LPC FRAME#	R599	1	2	0 0402 5%	LPC FRAME#	
LPC_A03 R	R600	1	2	0 0402 5%	LPC_A03	LPC_FRAME# 12.40
LPC_A02 R	R601	1	2	0 0402 5%	LPC_A02	LPC_A03 12.40
LPC_A01 R	R602	1	2	0 0402 5%	LPC_A01	LPC_A02 12.40
LPC_A00 R	R603	1	2	0 0402 5%	LPC_A00	LPC_A01 12.40
PCI_RST# R	R604	1	2	0 0402 5%	PLT_RST#	LPC_A00 12.40
CLK LPC_DEBUG1	R	1	2	0 0402 5%	CLK LPC_DEBUG1	15



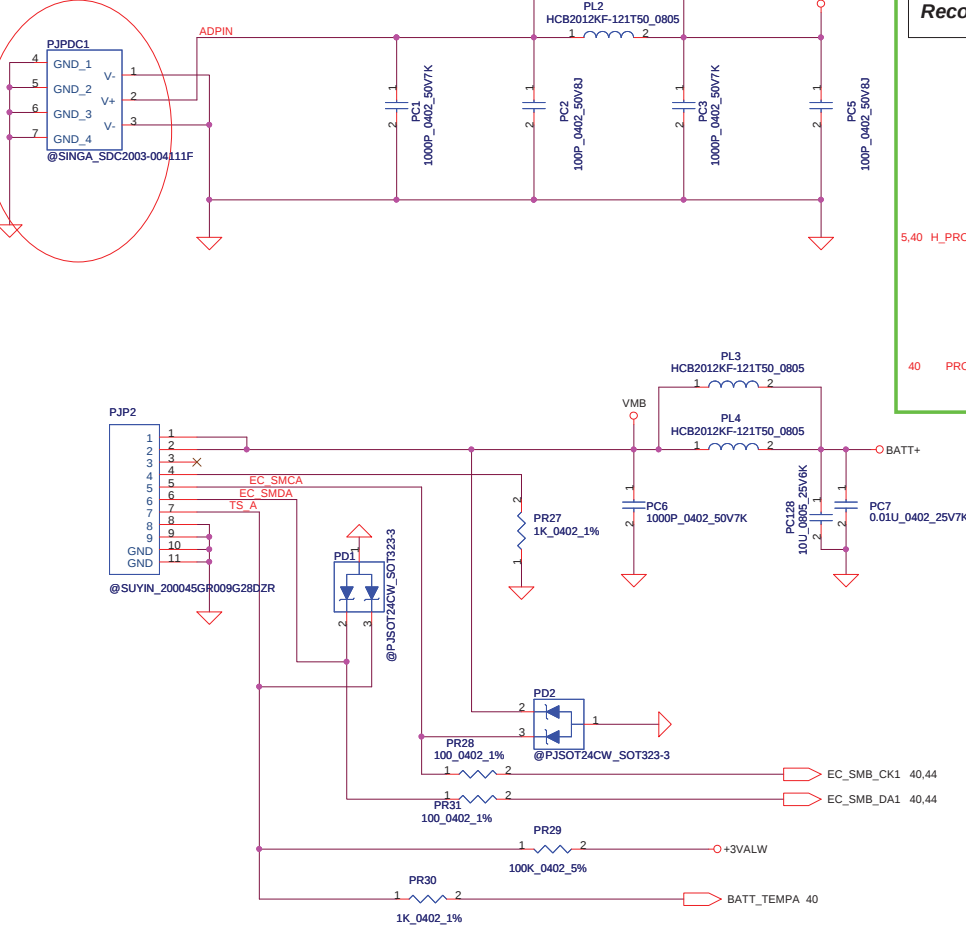
+5VALW
TO
+5VS
+3VALW
TO
+3VS

+1.5V
TO
+1.5VS

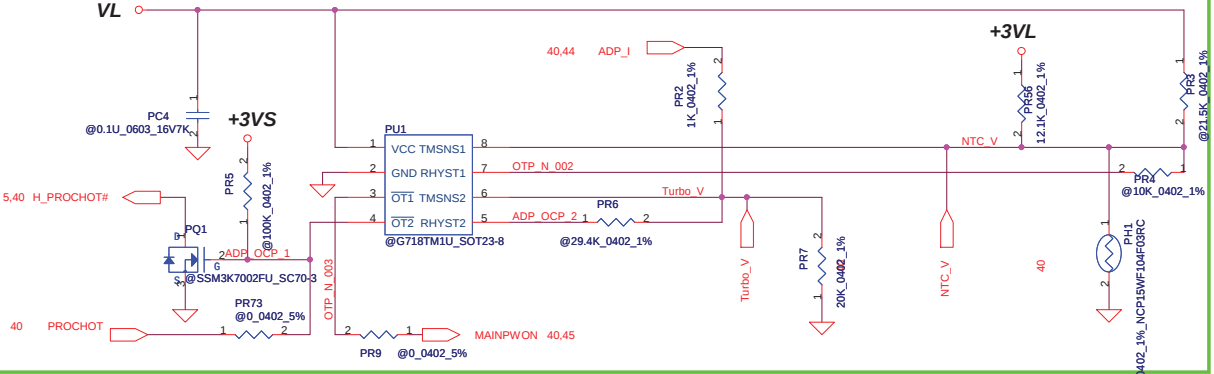


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Size Custom				Document Number
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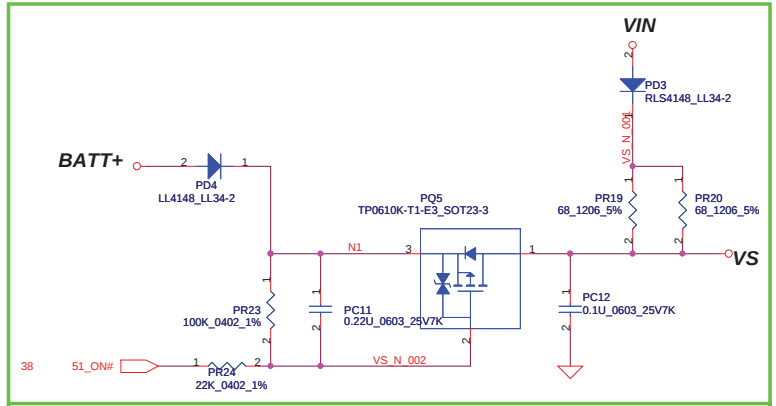
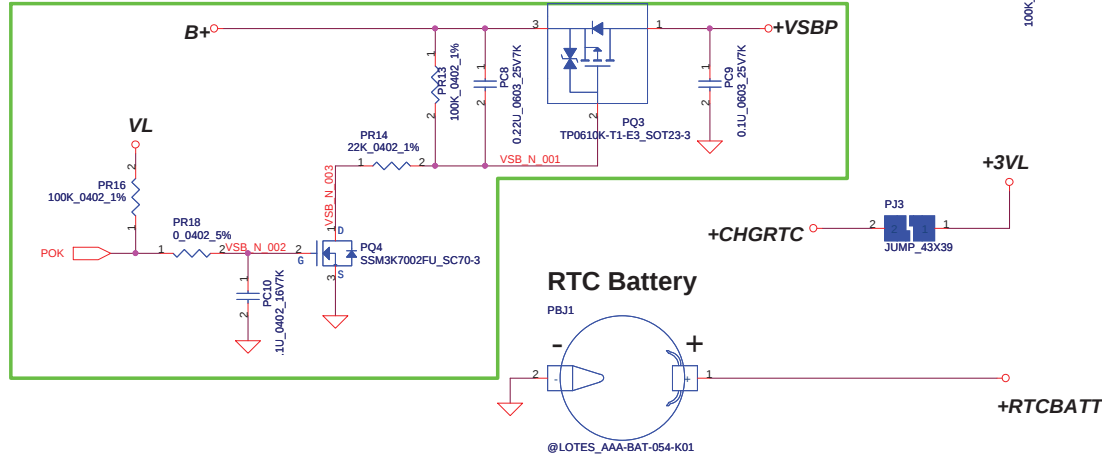
DCIN jack P/N:DC301008L00,
need dogle confirm P/N with ME



PH1 under CPU botten side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

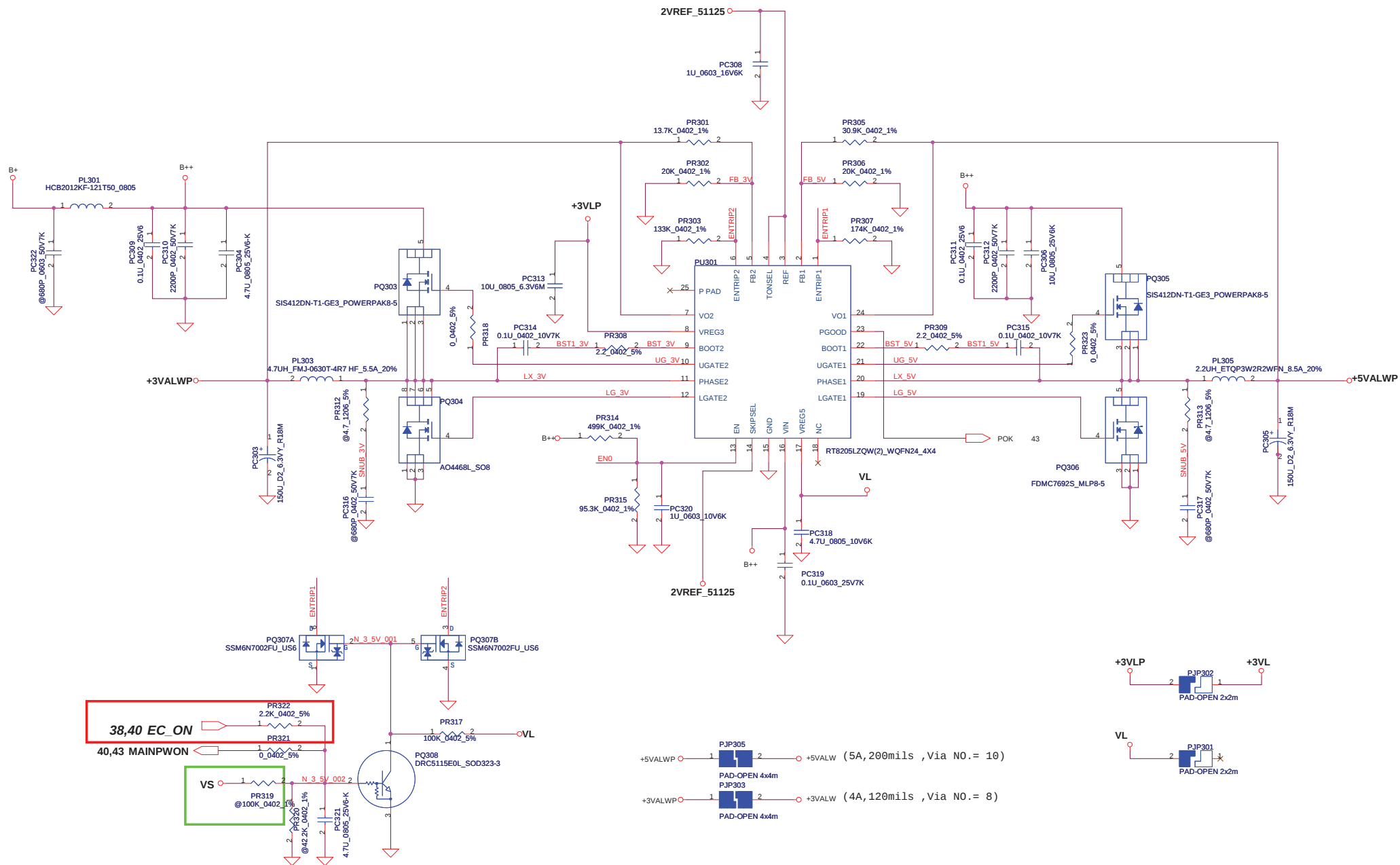


For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56



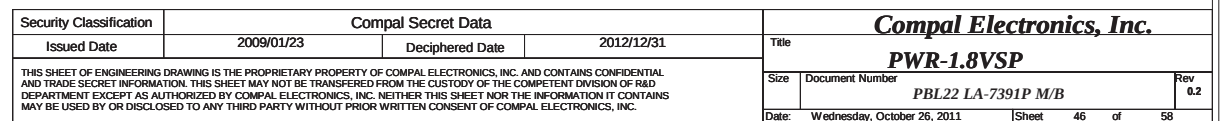
For KB9012 --> Remove all 51_ON# circuit

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										PWR-DCIN / BATT CONN / OTP	
										Size	
										Document Number	
										PBL22 LA-7391P M/B	
										Rev	
										0.2	
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										Wednesday, October 26, 2011	
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										43	
										of	
										58	



For KB930 --> Keep PR319, Remove PR322
 For KB9012 (Red square) --> Remove PR319
 Keep PR322

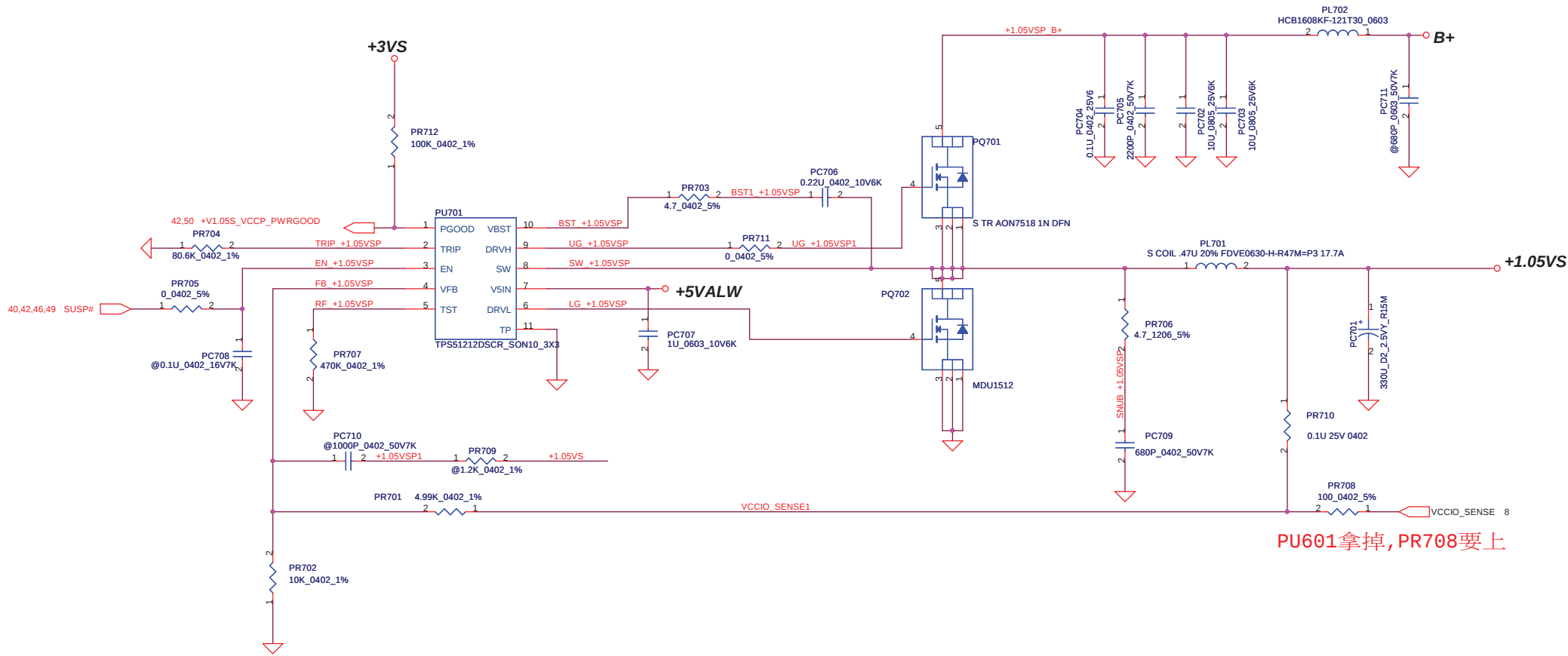
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(8.5A,360mils ,Via N0.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

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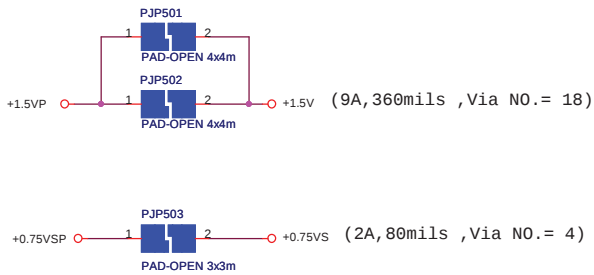


(12A, 480mils ,Via N0.= 24)

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Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



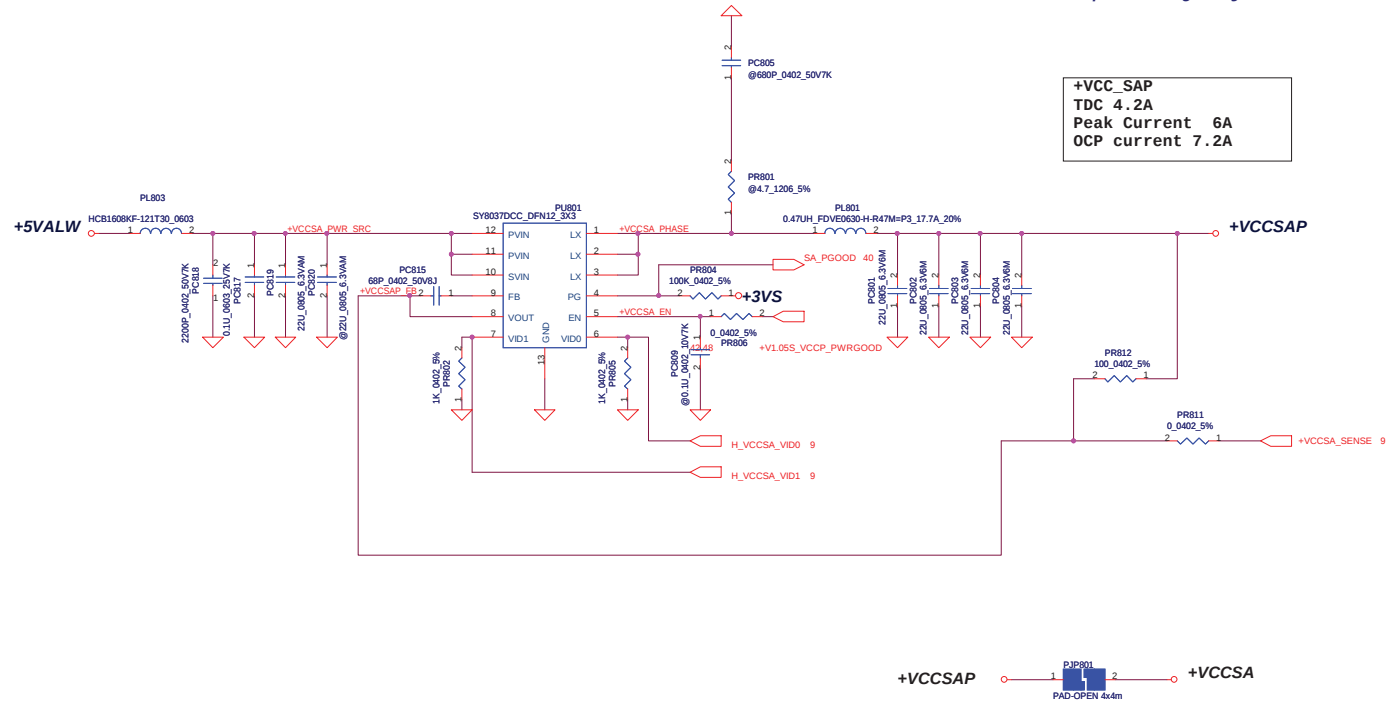
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Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	PWR-1.5VP / +0.75VSP
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				Document Number	PBL22 LA-7391P M/B
				Date	Wednesday, October 26, 2011
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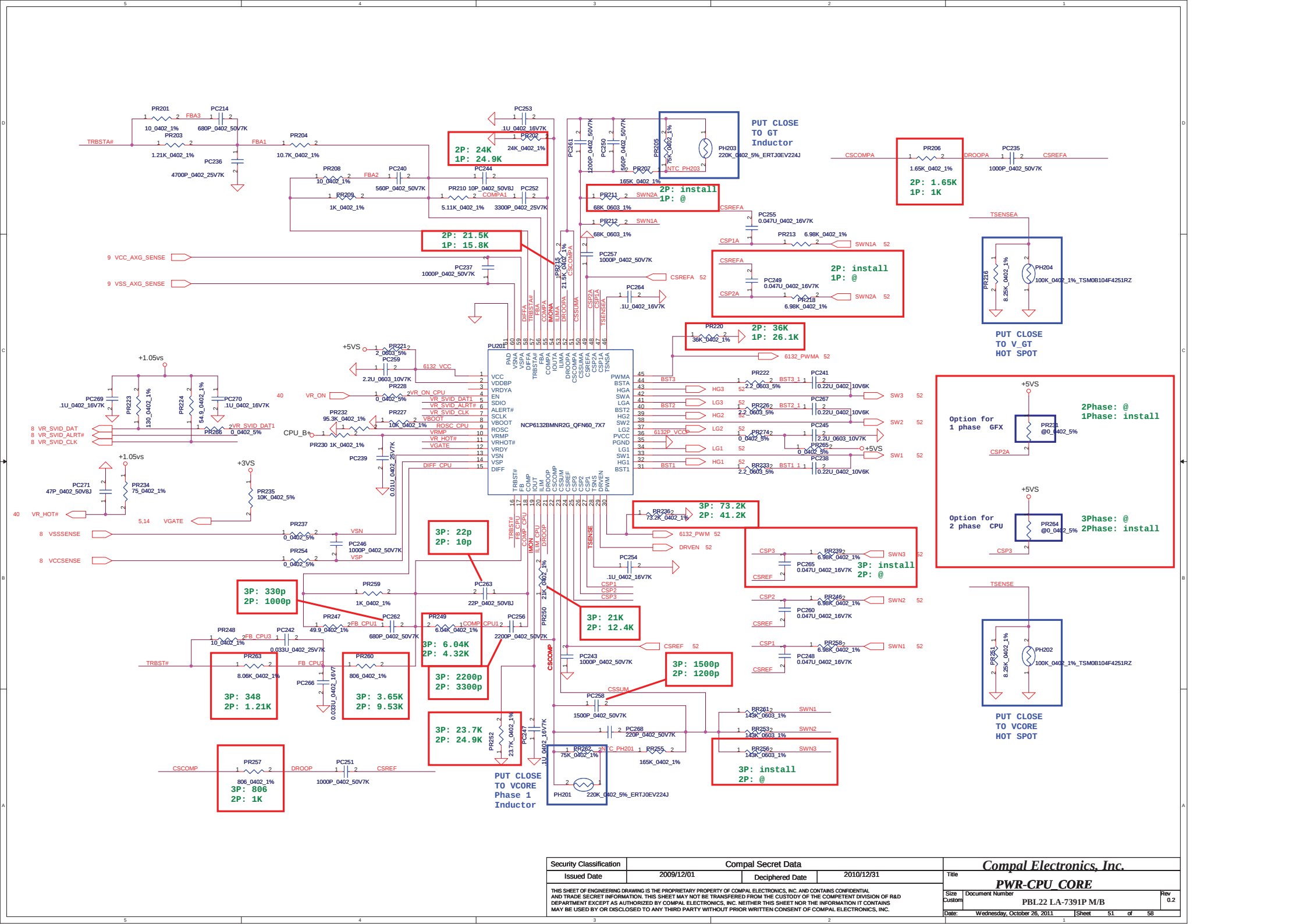
The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

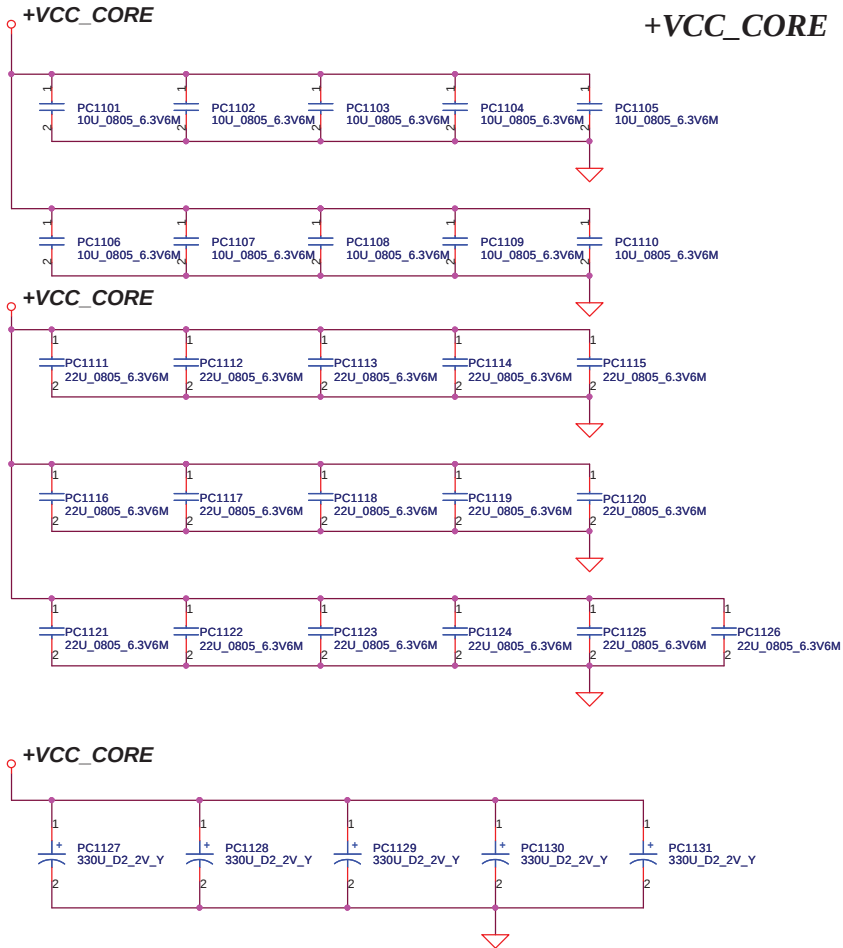
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

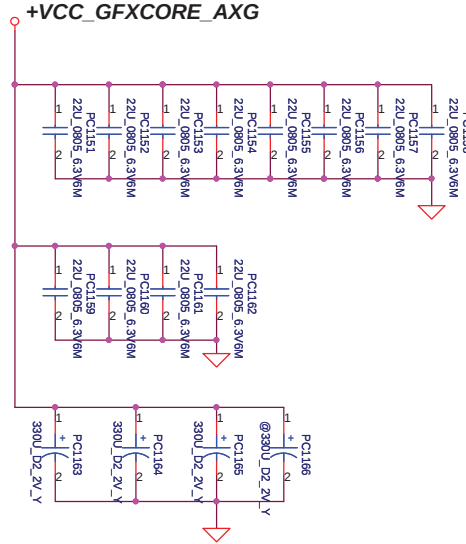
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A





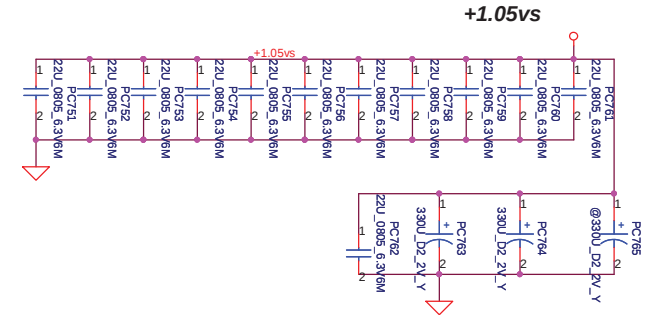


+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

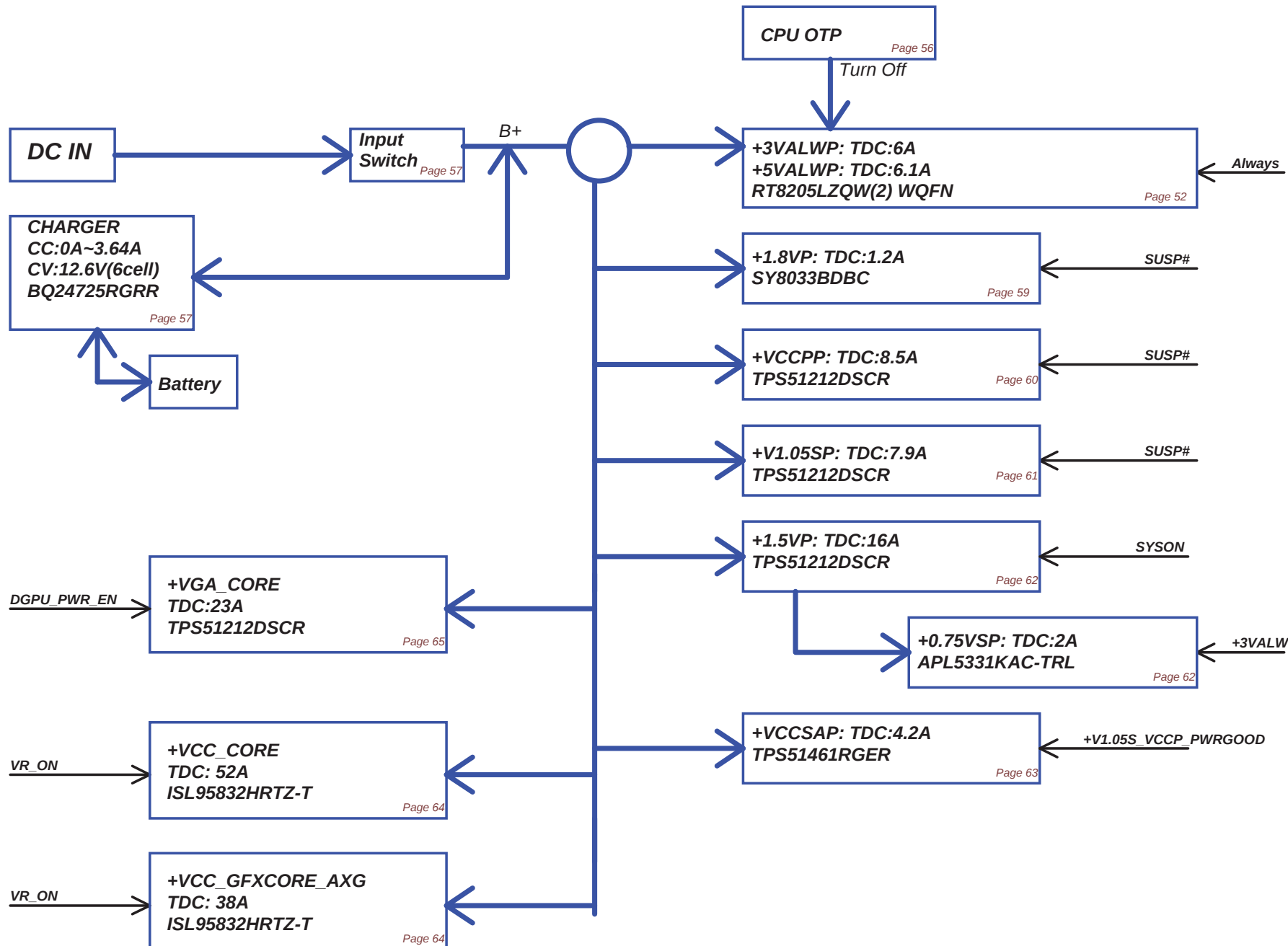
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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Power block

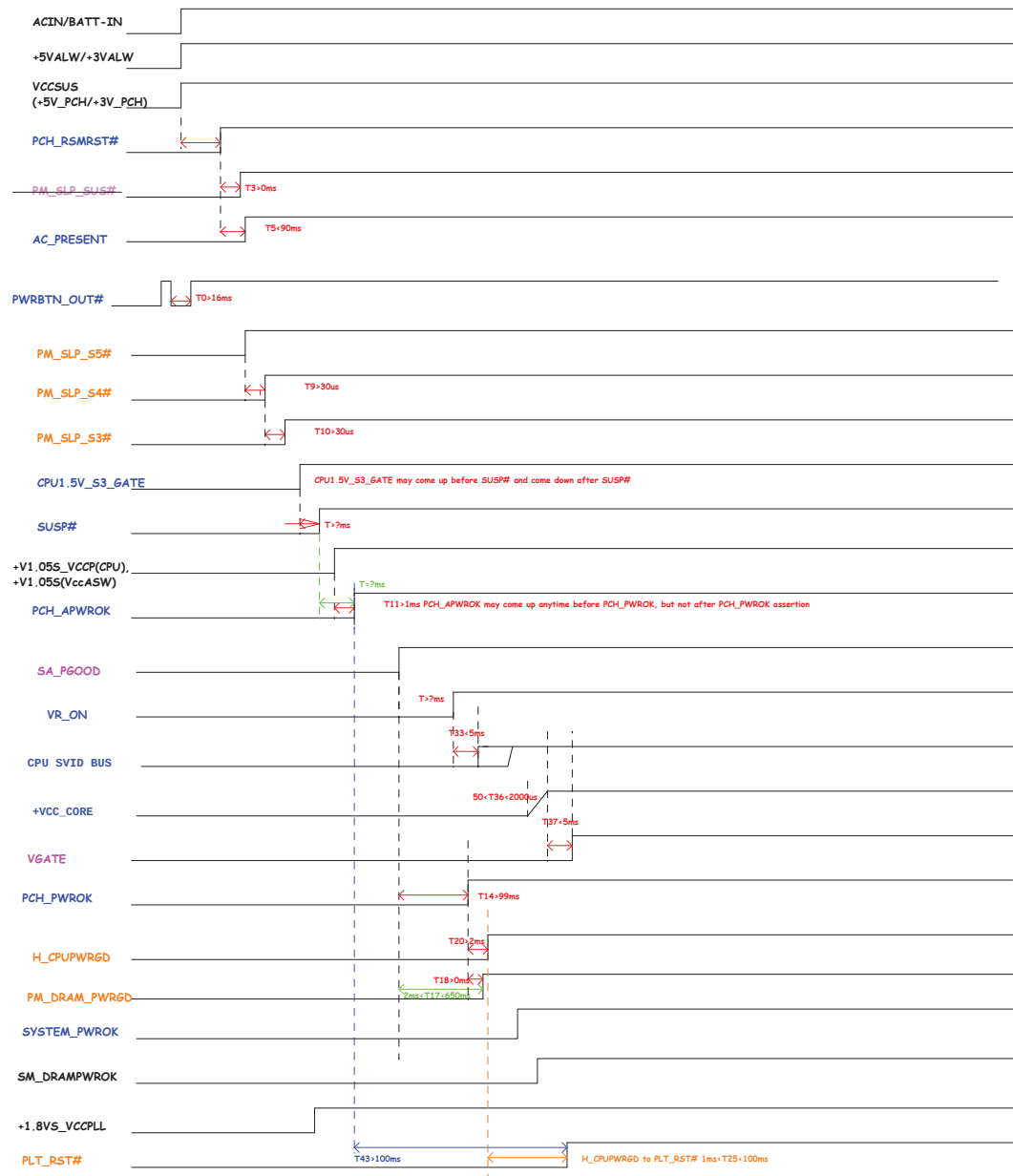


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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		Add USB3.0(ASM1042) & non AI co-lay	0.2	36	Add ASM1042 co-lay	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13	Delete Q3. (connect pin S & D) Remove R135, R137	09/21	
ER04		Design change for card reader	0.2	40	Del R552, R556	09/21	
ER05		HW Design (PURC demand)	0.2	34	Add Q20, R773, R775 Reserve R768, R774. Change Net name at Card reader Conn	09/21	
ER06		HW Design (PURC demand)	0.2	29	Change to Q3(A03404L) from U22(A04430L)	09/21	
ER07		HW Design (PURC demand)	0.2	42	Change Q33 to A03413L from AP23016N	09/21	
ER08		Fine-tune GPU timing	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER09		HW Design (reserve)	0.2	18	Reserve R290	09/21	
ER10	KB connector reverse	HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER11		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER12		HW Design (PURC demand)	0.2	15	Del R229, R230 (10K) Add R776-R783 (10K) Del R237, R239, R242 (8.2K) Add R784-R793 (8.2K)	09/30	
ER13		HW Design (PURC demand)	0.2	29, 31 37, 38 10, 11	Change P/N C387, C389, C399, C436, C447, C602 Change C315, C518, C526 (0402) Change P/N C99, C109, C118, C126, C140, C141. (0402)	10/03	
ER14		HW Design(XTAL fine-tune)	0.2	42, 43 13, 12 20, 36	Change R607 to 10 ohm Change Y3, C241, C242. Change Y1, C144, C145 Change Y4, C469, C473. Change Y2, C163, C164 Change Y9	10/07	
ER15		HW Design for instant on function	0.2	13 5	Reserve R750 R276 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER16		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38, P40)	10/07	
ER17		HW Design (PURC demand)	0.2		Change P/N Q7, U26, U21. Change P/N Q14-Q19, Q25, Q27-Q29, Q32, Q34-Q37, Q40-Q43, Q46-Q51, Q55-Q57, Q60, Q61, Q902, Q903, Q905. Change P/N Q23	10/14	
ER18		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER19		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER20		change for GPU H/W strapping STRAPI to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	
ER21		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R242 Add C149 0.1uF Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER22		Modify H2 size	0.2	38	Modify H2 size	10/17	

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				LA-8221P		0.2
				Date:	Wednesday, October 26, 2011	Sheet