

Compal Confidential

QCL40 MB Schematic Document

LA-8224P

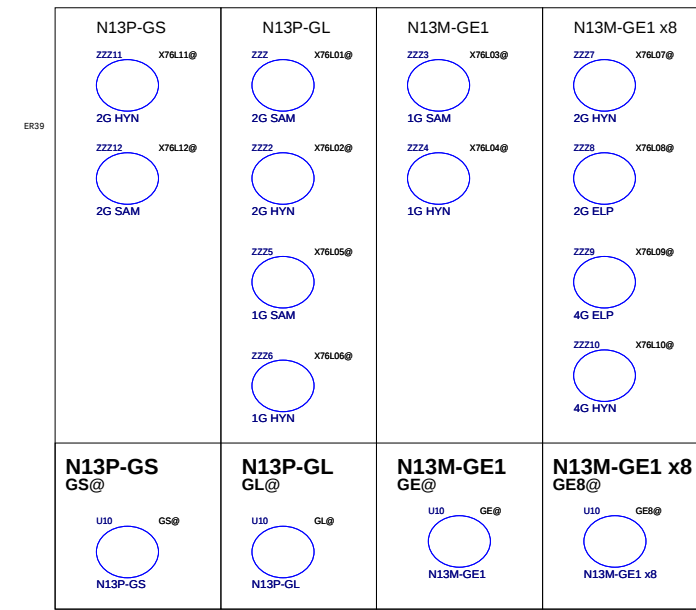
Rev: 0.2

2011.09.28

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				Size	Rev
				Custart	0.2
				Date:	Thursday, October 27, 2011
				Sheet	1 of 59

Security Classification		Compal Secret Data		Compal Electronics, Inc. Block Diagram		
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				Date: Thursday, October 27, 2011	Sheet 2 of 59	

X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GE8@: N13M-GE1_GB1b

9012@: EC(ENE 9012 chip)
930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :



: means Digital Ground



: means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

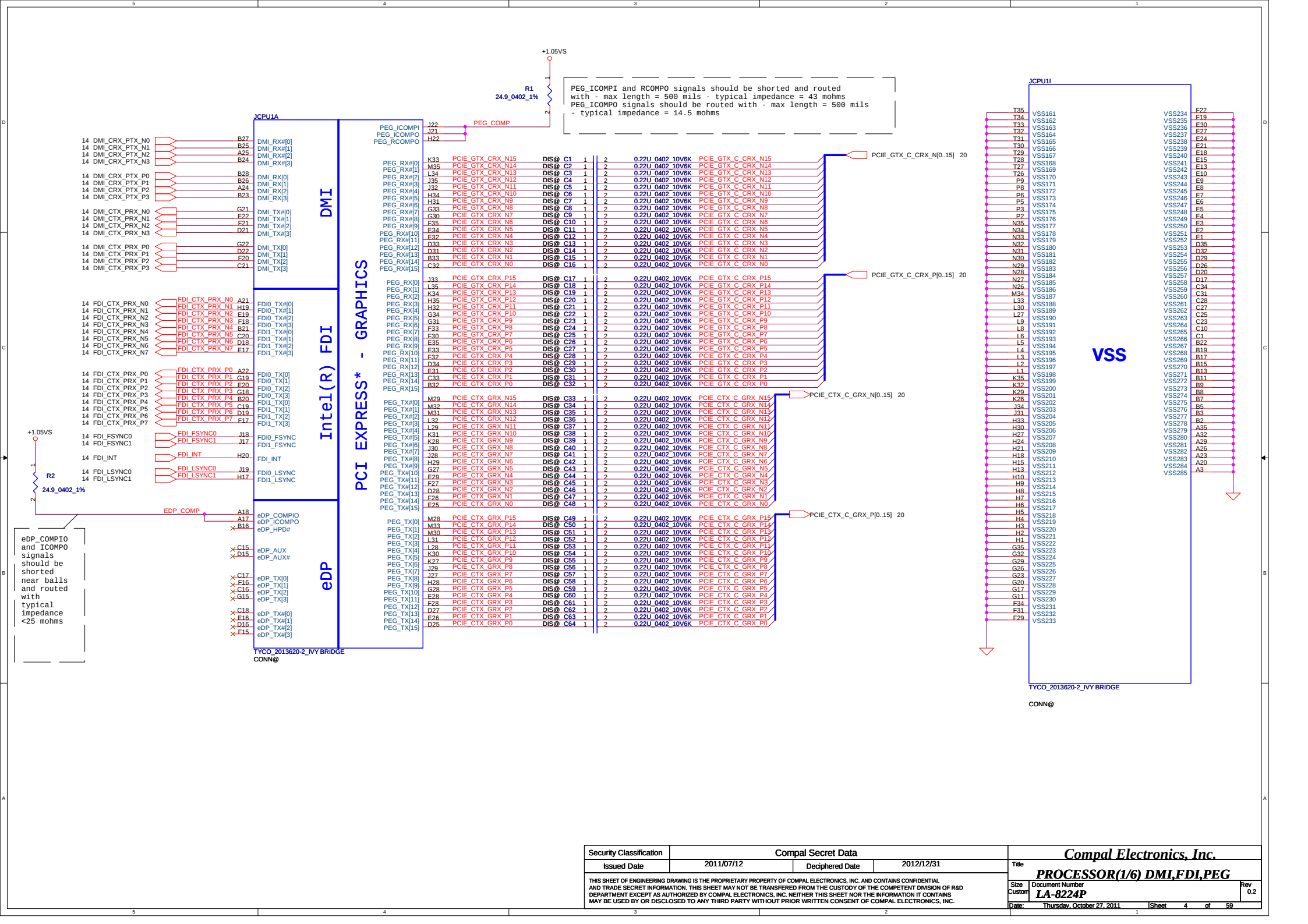
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

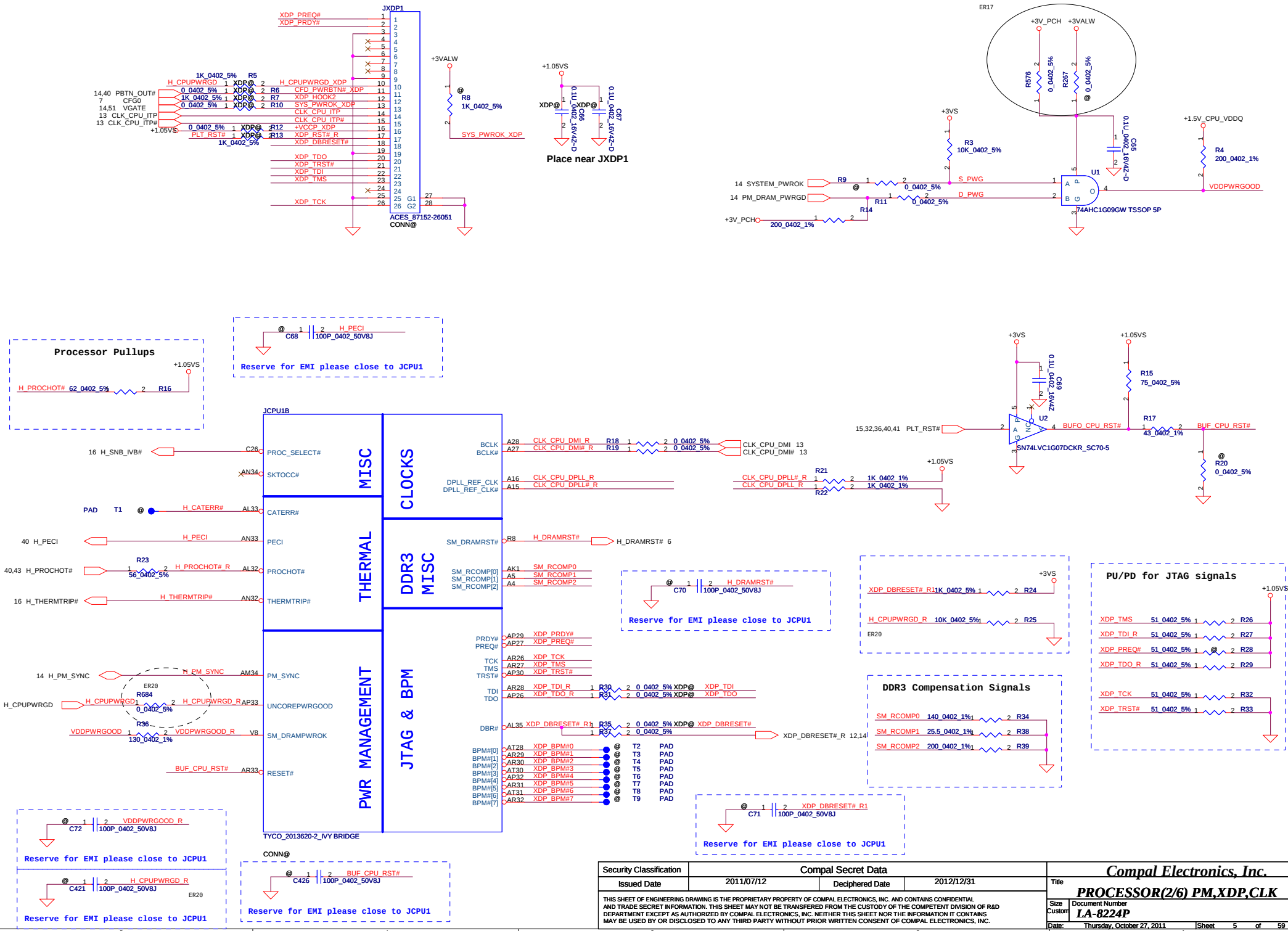
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				Date:	Thursday, October 27, 2011	Sheet 3 of 59

PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

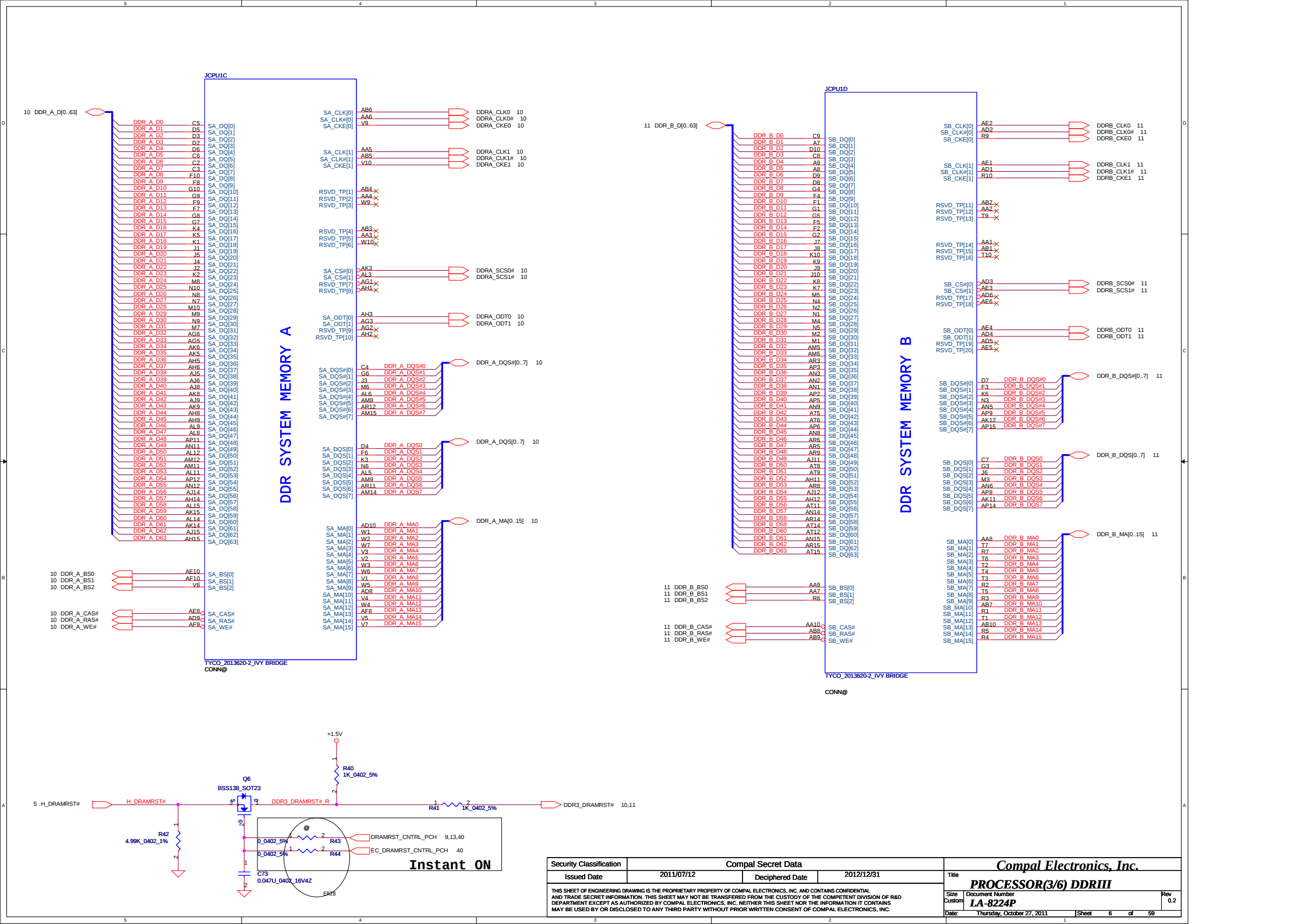
PCH	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
	13	None

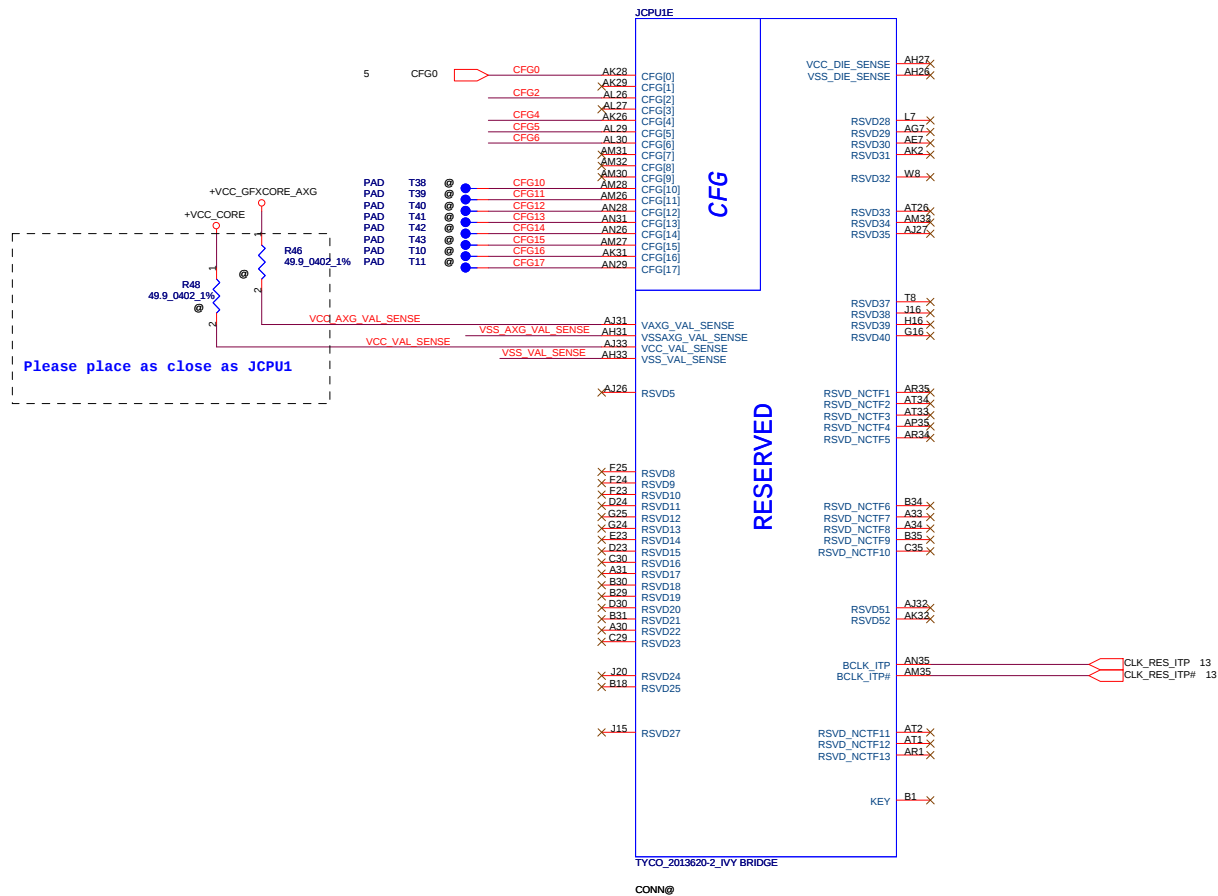
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



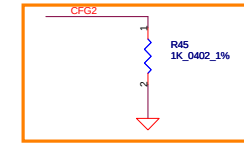


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	PROCESSOR(2/6) PM,XDP,CLK	
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				Date: Thursday, October 27, 2011	Rev 0.2
				Sheet 5	of 59



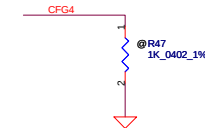


CFG Straps for Processor



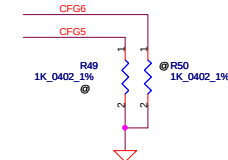
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed
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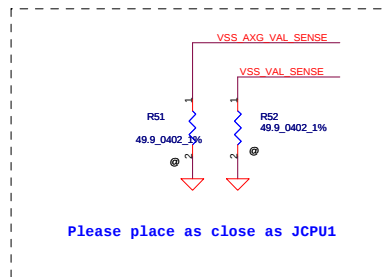
Display Port Presence Strap

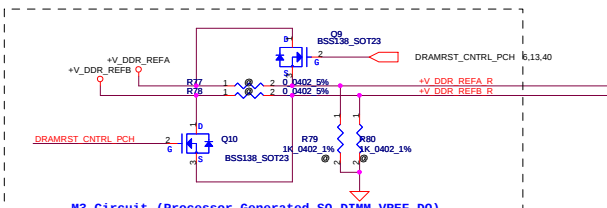
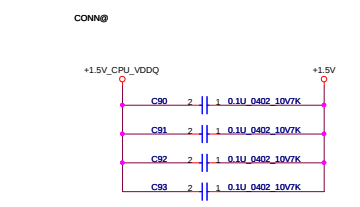
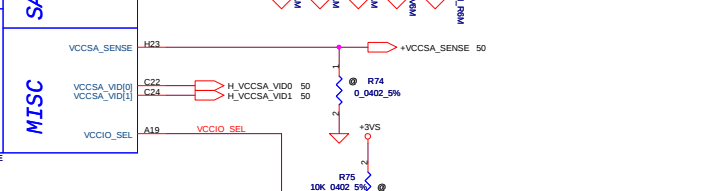
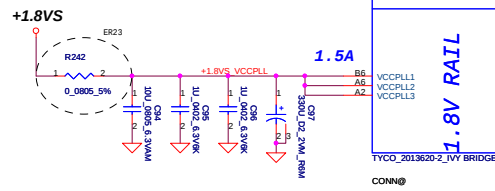
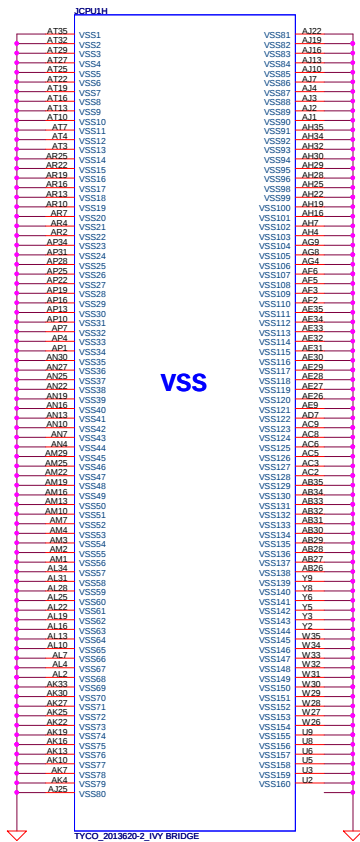
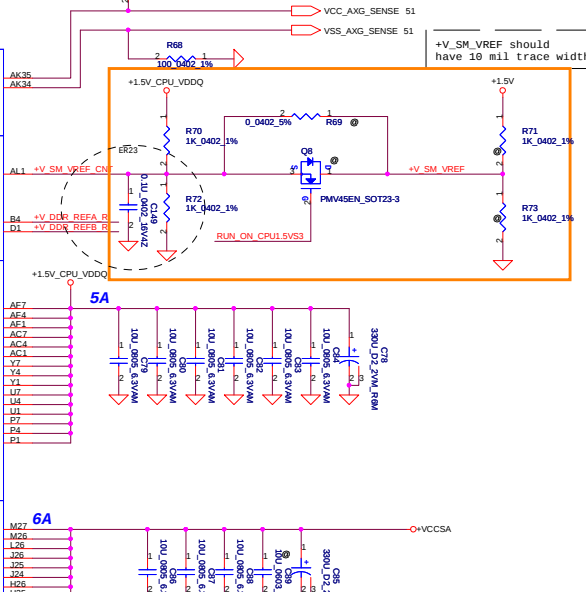
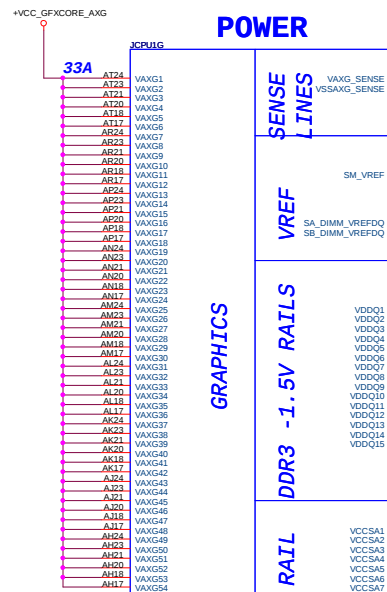
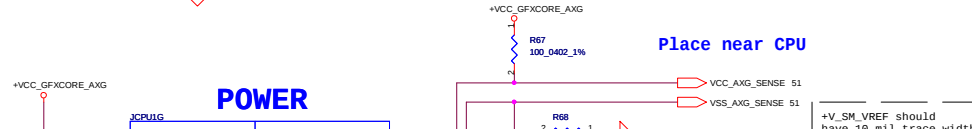
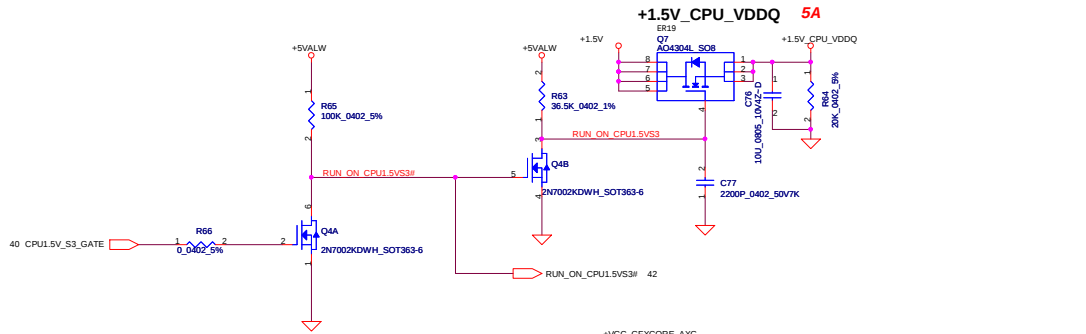
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
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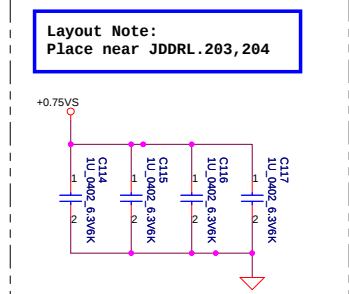
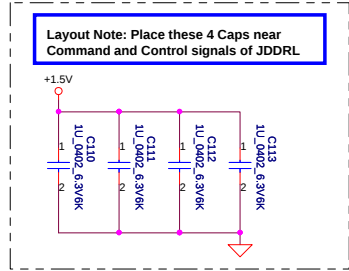
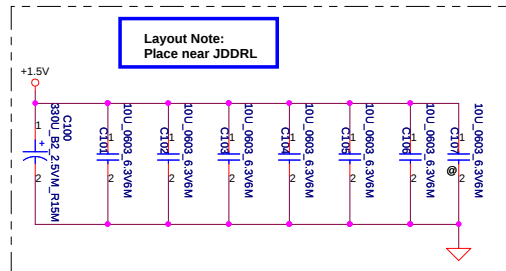
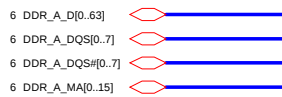
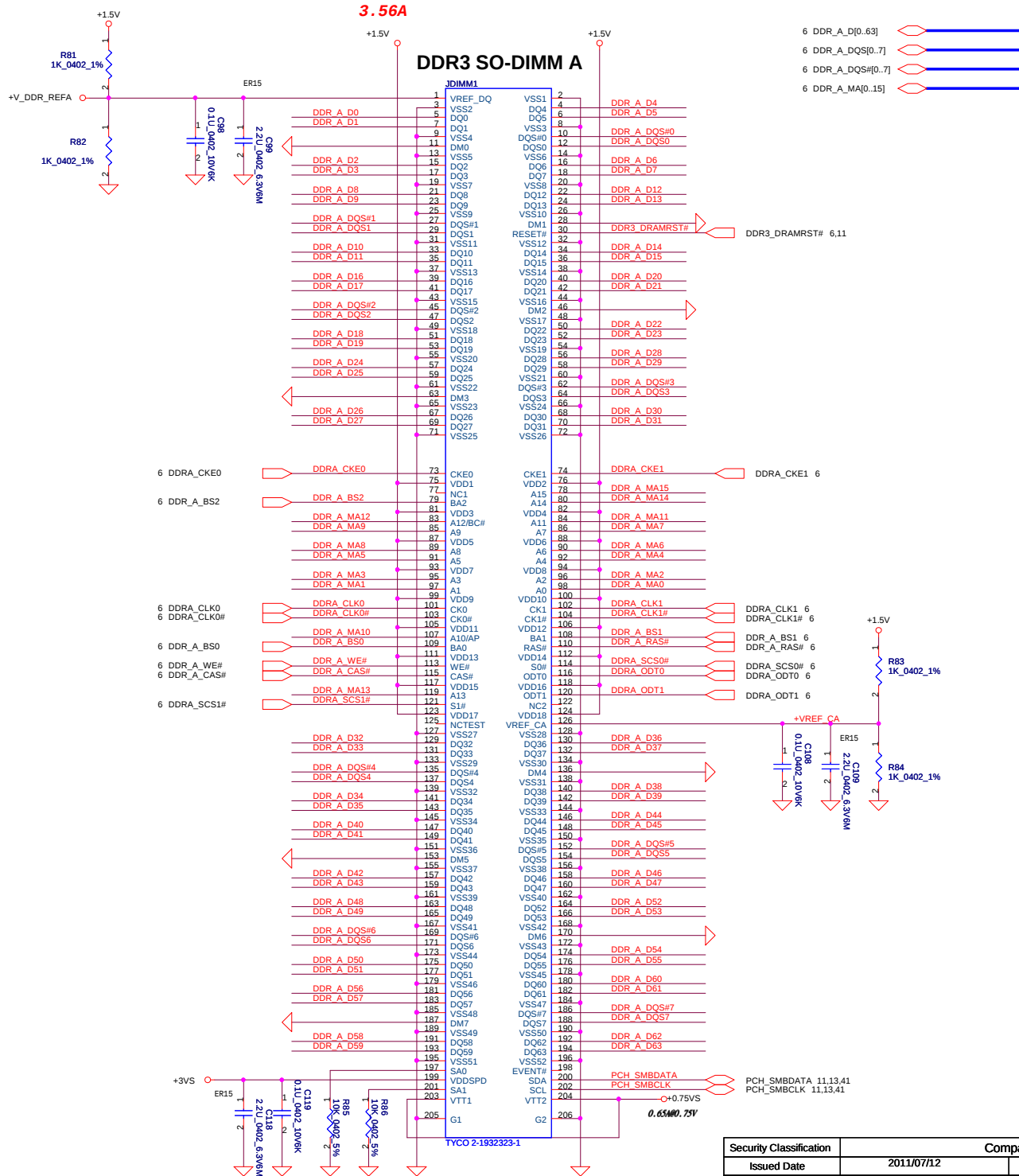
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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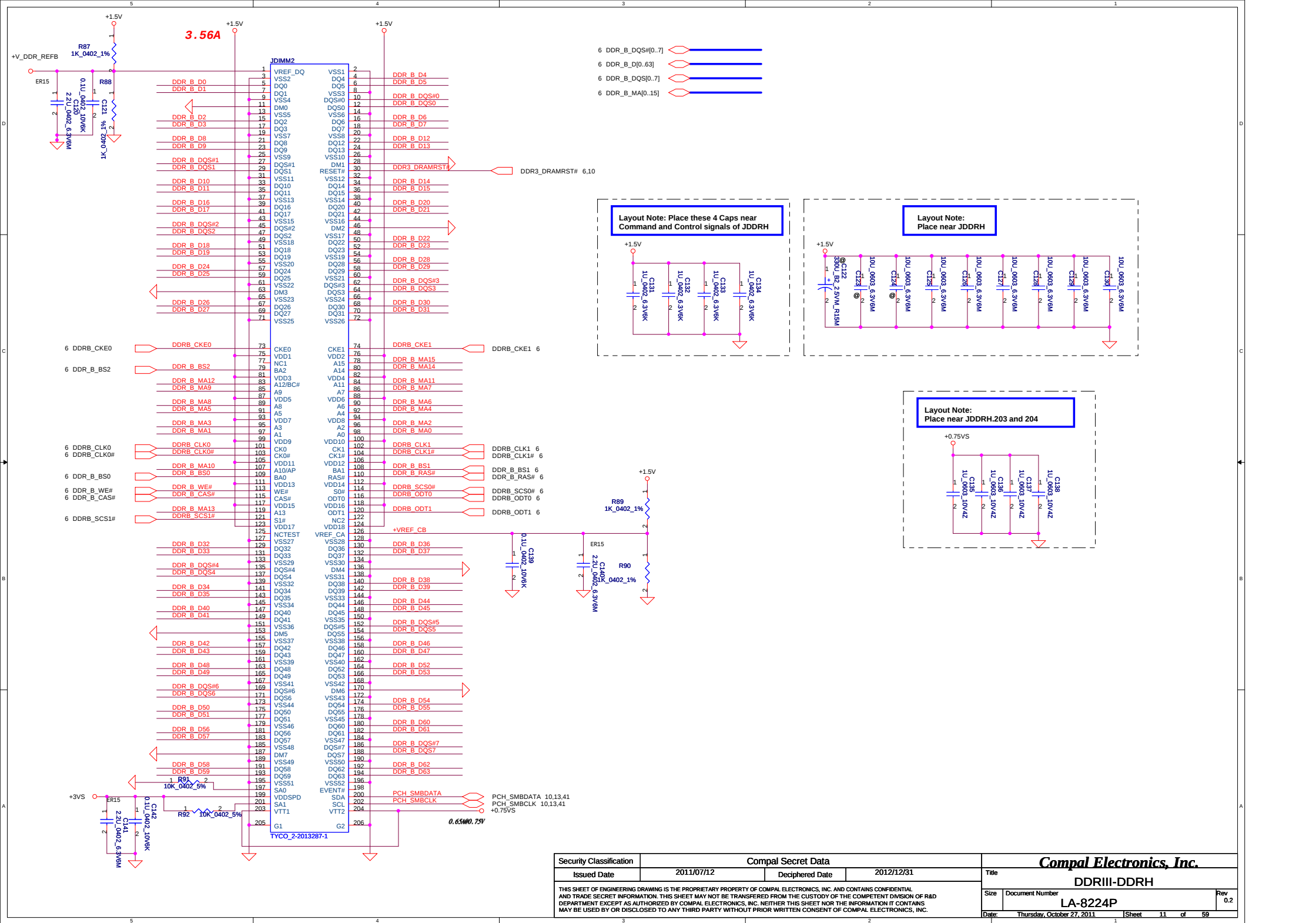


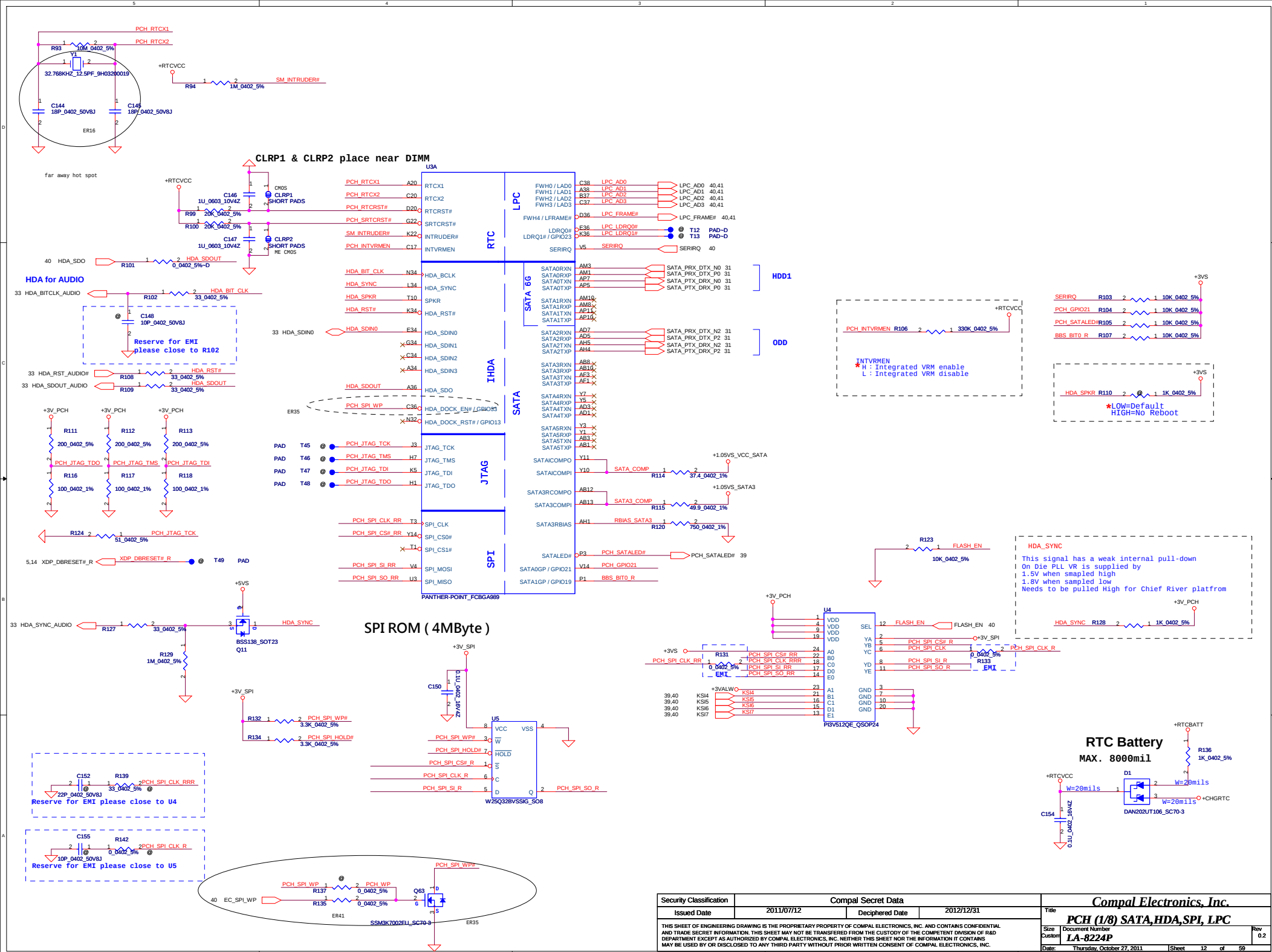


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Processor(6/6) PWR,VSS
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Date:	Thursday, October 27, 2011	Sheet:	9 of 59	Rev: 0.2

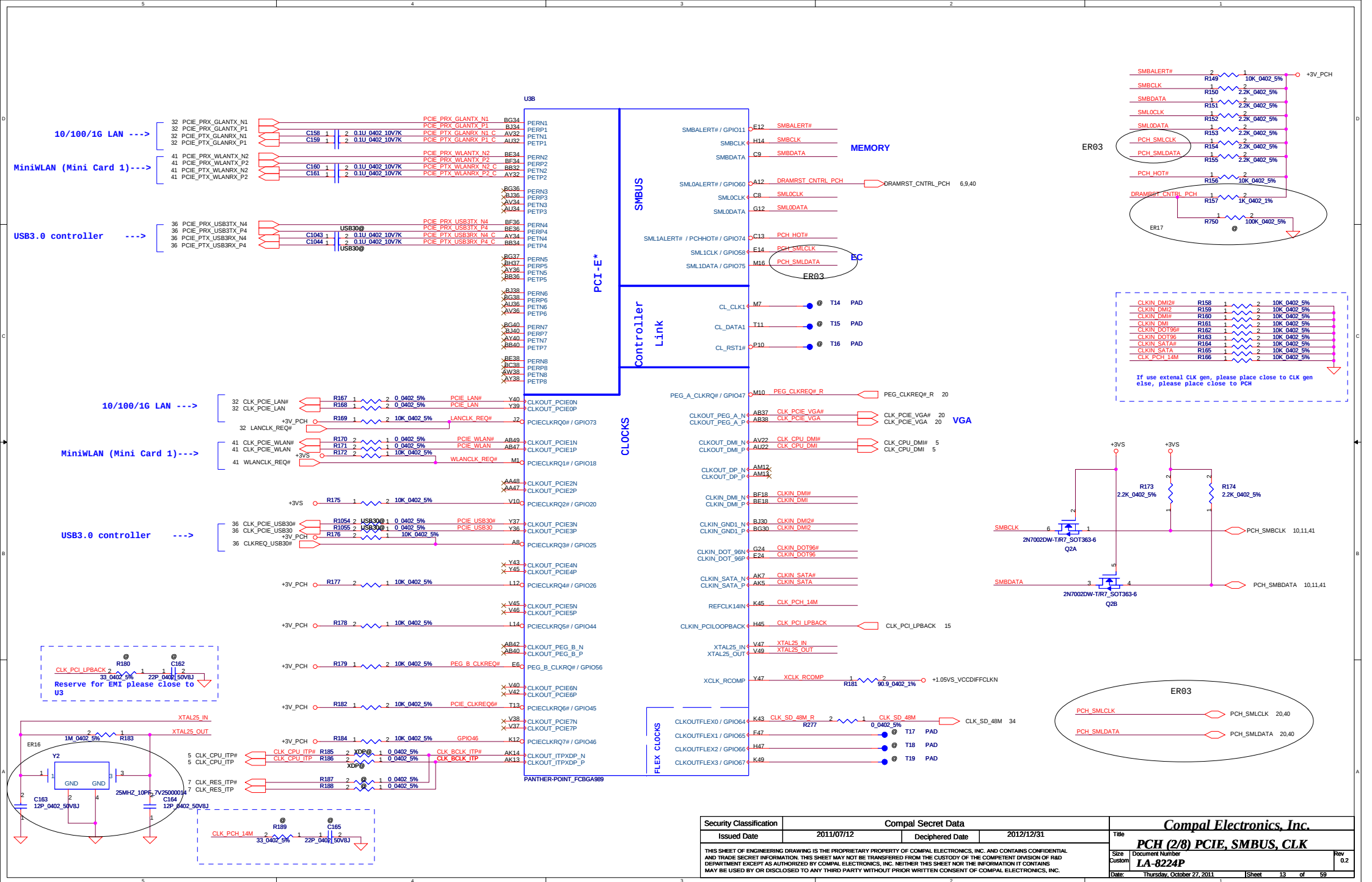


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Date				Thursday, October 27, 2011				10 of 59		

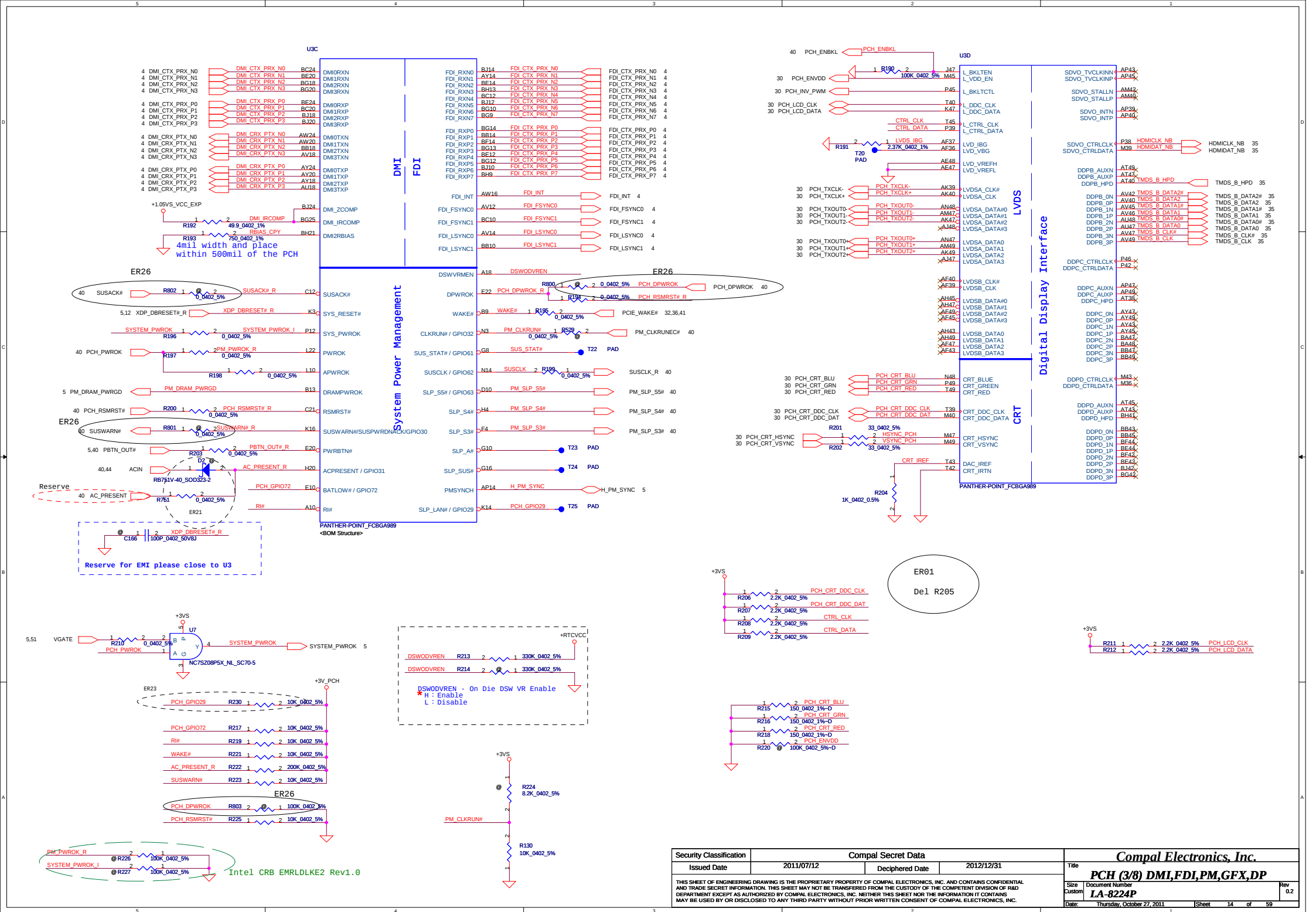


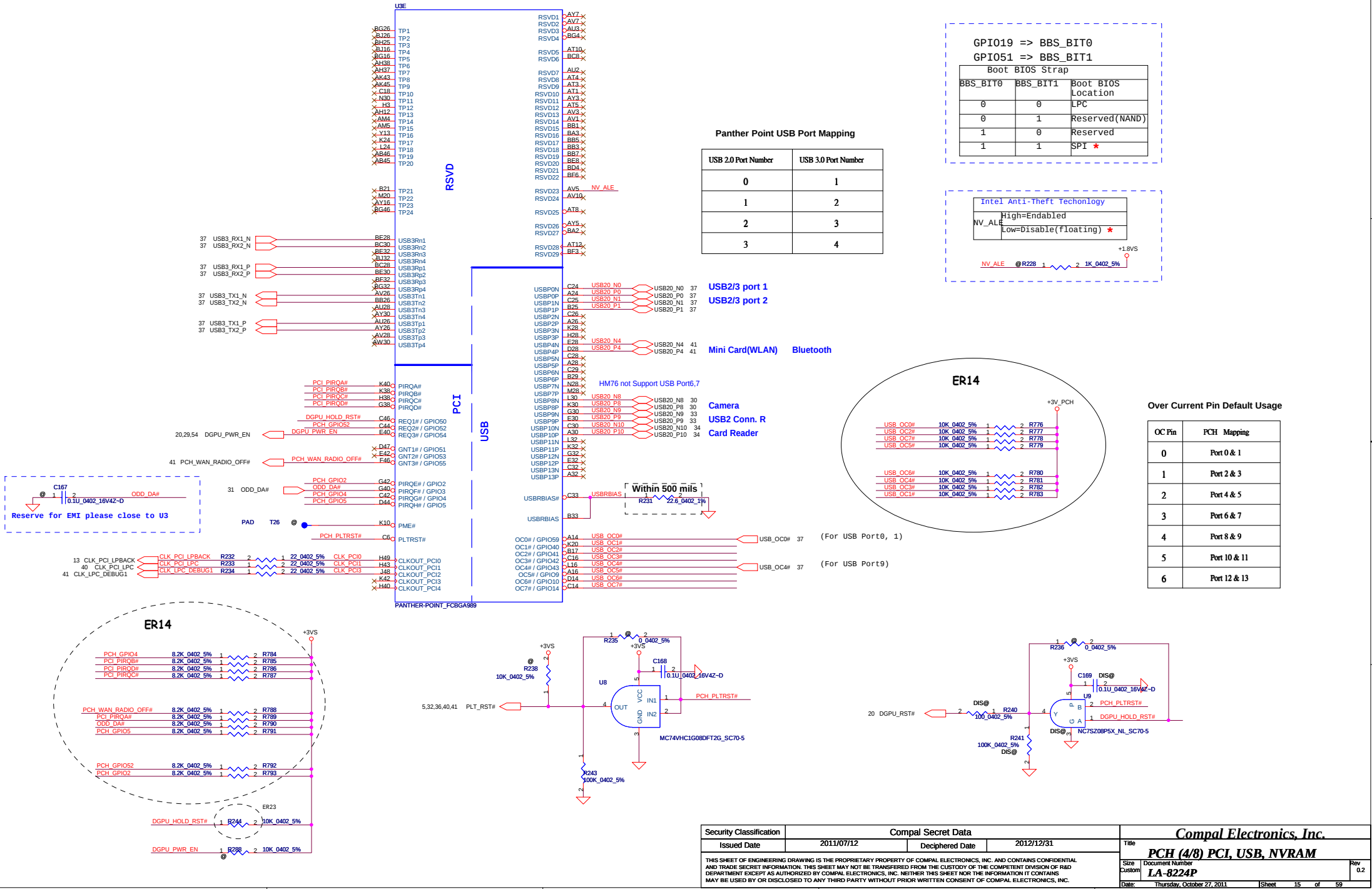


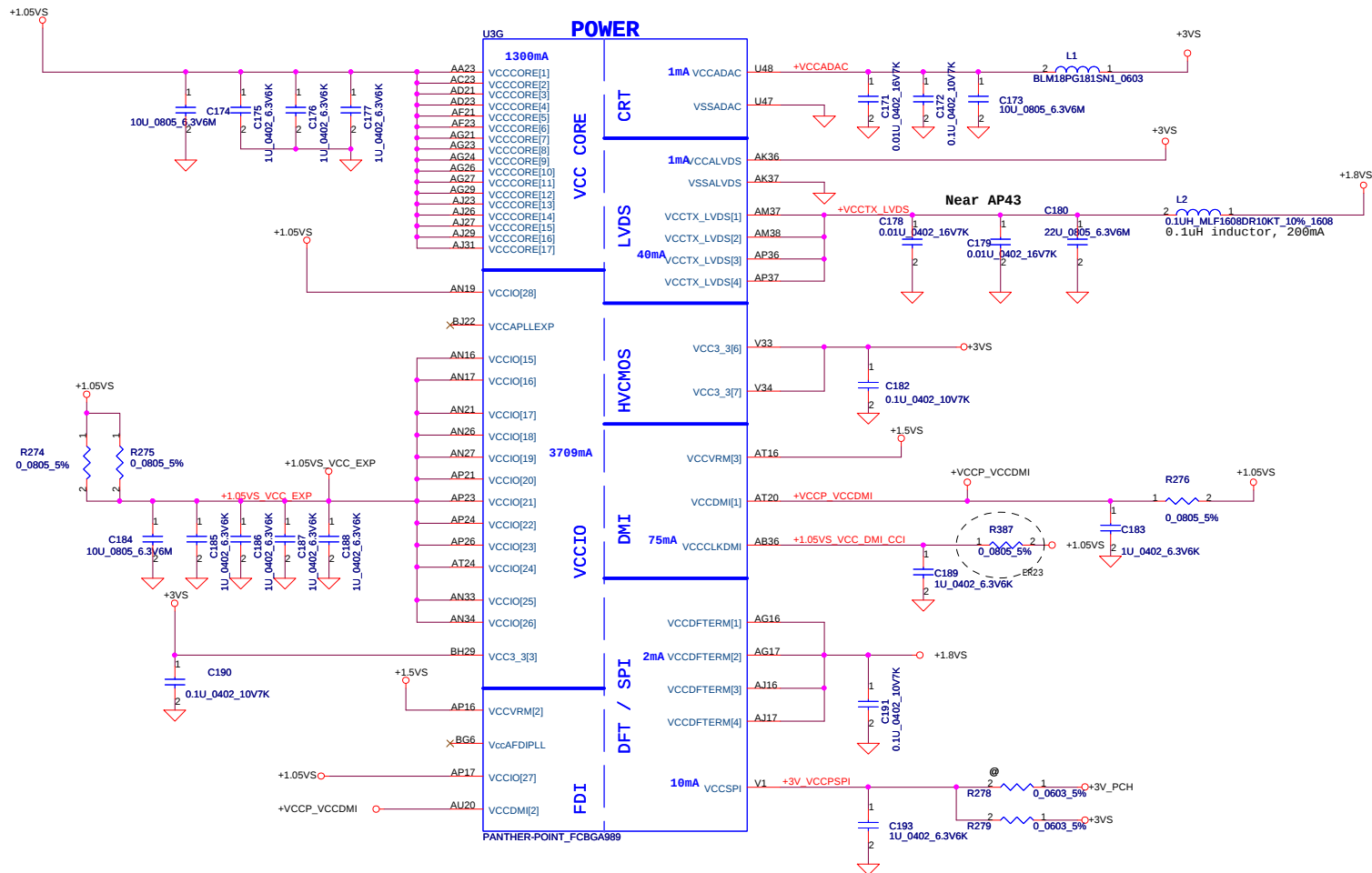
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				Cust	LA-8224P	0.2
				Date:	Thursday, October 27, 2011	Sheet 12 of 59



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PCH (2/8) PCIE, SMBUS, CLK		Rev 0.2	
Size	Document Number	LA-8224P	
Custom	Document Number	LA-8224P	
Date	Thursday, October 27, 2011	Sheet	13 of 59







PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLb	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

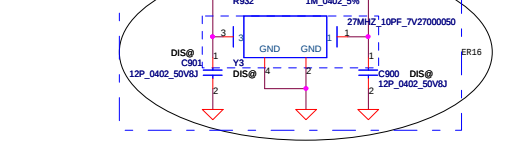
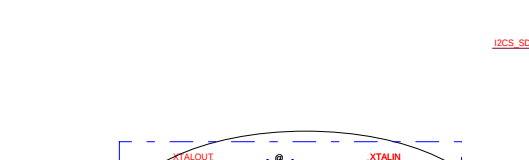
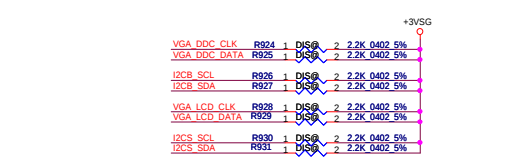
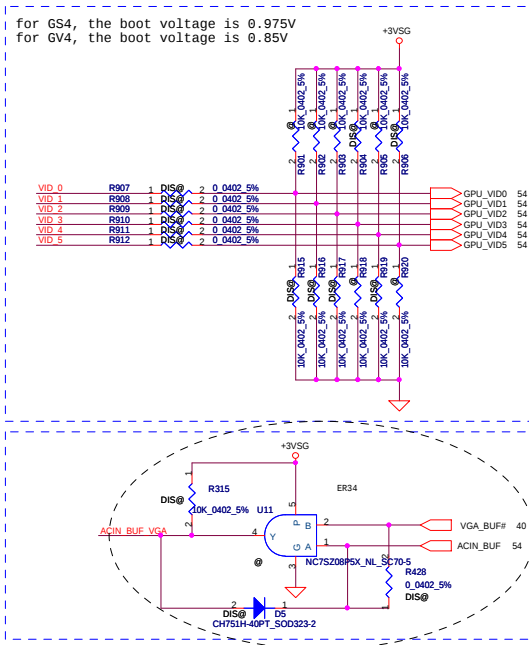
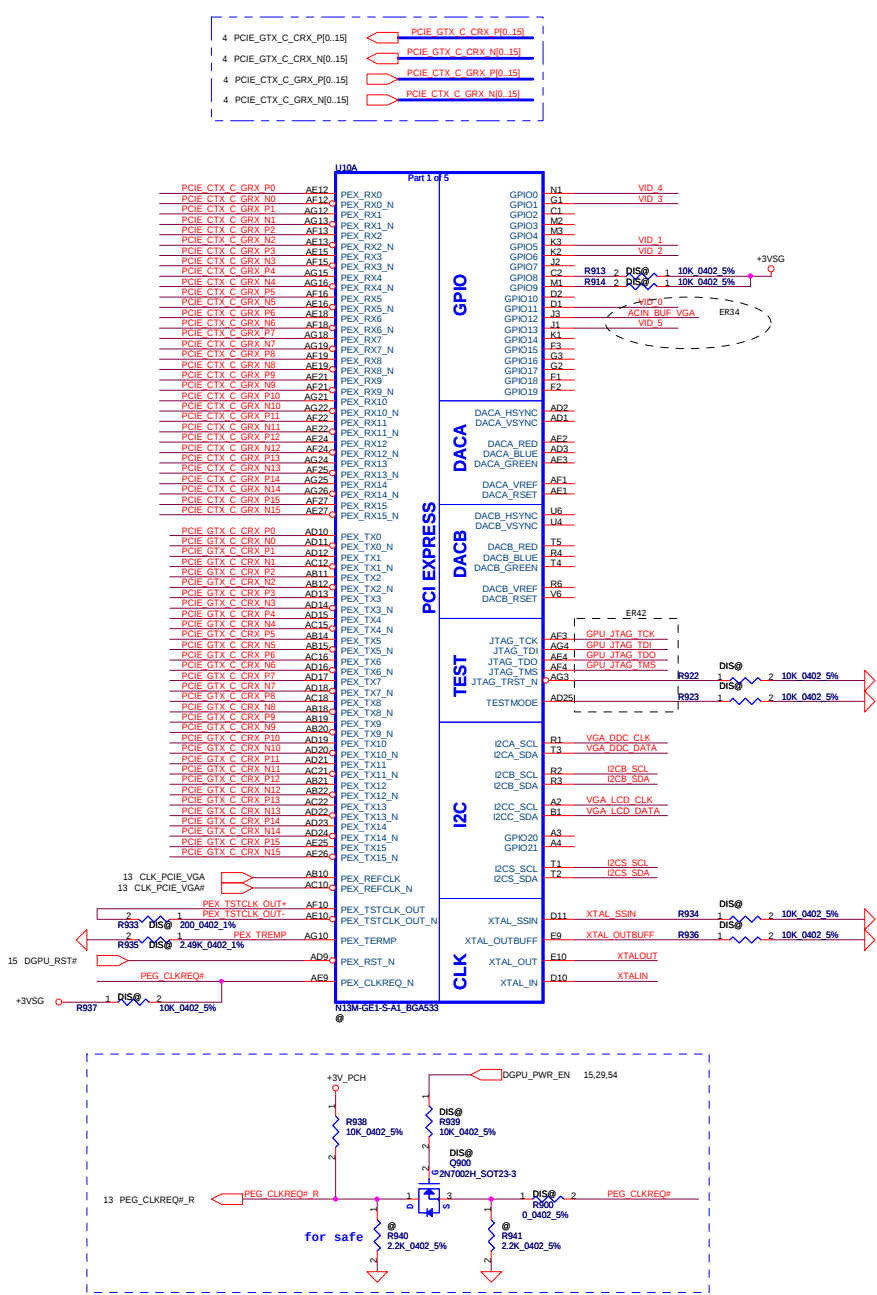
U3H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	VSS[81]
AA3	VSS[3]	VSS[82]
AA33	VSS[4]	VSS[83]
AA34	VSS[5]	VSS[84]
AB11	VSS[6]	VSS[85]
AB14	VSS[7]	VSS[86]
AB39	VSS[8]	VSS[87]
AB4	VSS[9]	VSS[88]
AB43	VSS[10]	VSS[89]
AB5	VSS[11]	VSS[90]
AB7	VSS[12]	VSS[91]
AC19	VSS[13]	VSS[92]
AC2	VSS[14]	VSS[93]
AC21	VSS[15]	VSS[94]
AC24	VSS[16]	VSS[95]
AC33	VSS[17]	VSS[96]
AC34	VSS[18]	VSS[97]
AD12	VSS[19]	VSS[98]
AD10	VSS[20]	VSS[99]
AD11	VSS[21]	VSS[100]
AD12	VSS[22]	VSS[101]
AD13	VSS[23]	VSS[102]
AD19	VSS[24]	VSS[103]
AD24	VSS[25]	VSS[104]
AD26	VSS[26]	VSS[105]
AD27	VSS[27]	VSS[106]
AD33	VSS[28]	VSS[107]
AD34	VSS[29]	VSS[108]
AD36	VSS[30]	VSS[109]
AD37	VSS[31]	VSS[110]
AD38	VSS[32]	VSS[111]
AD39	VSS[33]	VSS[112]
AD4	VSS[34]	VSS[113]
AD40	VSS[35]	VSS[114]
AD42	VSS[36]	VSS[115]
AD43	VSS[37]	VSS[116]
AD45	VSS[38]	VSS[117]
AD46	VSS[39]	VSS[118]
AD8	VSS[40]	VSS[119]
AE2	VSS[41]	VSS[120]
AE3	VSS[42]	VSS[121]
AE10	VSS[43]	VSS[122]
AE12	VSS[44]	VSS[123]
AD14	VSS[45]	VSS[124]
AD16	VSS[46]	VSS[125]
AE16	VSS[47]	VSS[126]
AE19	VSS[48]	VSS[127]
AE24	VSS[49]	VSS[128]
AE26	VSS[50]	VSS[129]
AE27	VSS[51]	VSS[130]
AE29	VSS[52]	VSS[131]
AF31	VSS[53]	VSS[132]
AF38	VSS[54]	VSS[133]
AF4	VSS[55]	VSS[134]
AF42	VSS[56]	VSS[135]
AF46	VSS[57]	VSS[136]
AF5	VSS[58]	VSS[137]
AF7	VSS[59]	VSS[138]
AF8	VSS[60]	VSS[139]
AG19	VSS[61]	VSS[140]
AG2	VSS[62]	VSS[141]
AG31	VSS[63]	VSS[142]
AG48	VSS[64]	VSS[143]
AH11	VSS[65]	VSS[144]
AH3	VSS[66]	VSS[145]
AH36	VSS[67]	VSS[146]
AH39	VSS[68]	VSS[147]
AH40	VSS[69]	VSS[148]
AH42	VSS[70]	VSS[149]
AH46	VSS[71]	VSS[150]
AH7	VSS[72]	VSS[151]
AJ19	VSS[73]	VSS[152]
AJ21	VSS[74]	VSS[153]
AJ24	VSS[75]	VSS[154]
AJ33	VSS[76]	VSS[155]
AJ34	VSS[77]	VSS[156]
AK12	VSS[78]	VSS[157]
AK3	VSS[79]	VSS[158]

PANTHER-POINT_FCBGA989

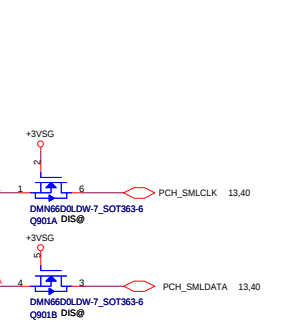
U3I		
AY4	VSS[159]	VSS[259]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B15	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
BC14	VSS[183]	VSS[283]
BC18	VSS[184]	VSS[284]
BC2	VSS[185]	VSS[285]
BC22	VSS[186]	VSS[286]
BC26	VSS[187]	VSS[287]
BC32	VSS[188]	VSS[288]
BC34	VSS[189]	VSS[289]
BC36	VSS[190]	VSS[290]
BC40	VSS[191]	VSS[291]
BC42	VSS[192]	VSS[292]
BC48	VSS[193]	VSS[293]
BD46	VSS[194]	VSS[294]
BD5	VSS[195]	VSS[295]
BE22	VSS[196]	VSS[296]
BE26	VSS[197]	VSS[297]
BE40	VSS[198]	VSS[298]
BF10	VSS[199]	VSS[299]
BF12	VSS[200]	VSS[300]
BF16	VSS[201]	VSS[301]
BF20	VSS[202]	VSS[302]
BF22	VSS[203]	VSS[303]
BF24	VSS[204]	VSS[304]
BF26	VSS[205]	VSS[305]
BF28	VSS[206]	VSS[306]
BF30	VSS[207]	VSS[307]
BF38	VSS[208]	VSS[308]
BF40	VSS[209]	VSS[309]
BF9	VSS[210]	VSS[310]
BG17	VSS[211]	VSS[311]
BG21	VSS[212]	VSS[312]
BG33	VSS[213]	VSS[313]
BG44	VSS[214]	VSS[314]
BG68	VSS[215]	VSS[315]
BH11	VSS[216]	VSS[316]
BH15	VSS[217]	VSS[317]
BH17	VSS[218]	VSS[318]
BH19	VSS[219]	VSS[319]
H10	VSS[220]	VSS[320]
BH27	VSS[221]	VSS[321]
BH31	VSS[222]	VSS[322]
BH33	VSS[223]	VSS[323]
BH35	VSS[224]	VSS[324]
BH39	VSS[225]	VSS[325]
BH43	VSS[226]	VSS[326]
BH7	VSS[227]	VSS[327]
D3	VSS[228]	VSS[328]
D12	VSS[229]	VSS[329]
D16	VSS[230]	VSS[330]
D18	VSS[231]	VSS[331]
D22	VSS[232]	VSS[332]
D24	VSS[233]	VSS[333]
D26	VSS[234]	VSS[334]
D30	VSS[235]	VSS[335]
D32	VSS[236]	VSS[336]
D34	VSS[237]	VSS[337]
D38	VSS[238]	VSS[338]
D42	VSS[239]	VSS[339]
D8	VSS[240]	VSS[340]
E18	VSS[241]	VSS[341]
E26	VSS[242]	VSS[342]
G18	VSS[243]	VSS[343]
G20	VSS[244]	VSS[344]
G26	VSS[245]	VSS[345]
G28	VSS[246]	VSS[346]
G36	VSS[247]	VSS[347]
G48	VSS[248]	VSS[348]
H12	VSS[249]	VSS[349]
H18	VSS[250]	VSS[350]
H22	VSS[251]	VSS[351]
H26	VSS[252]	VSS[352]
H30	VSS[253]	
H32	VSS[254]	
H34	VSS[255]	
F3	VSS[256]	
F3	VSS[257]	
F3	VSS[258]	

PANTHER-POINT_FCBGA989

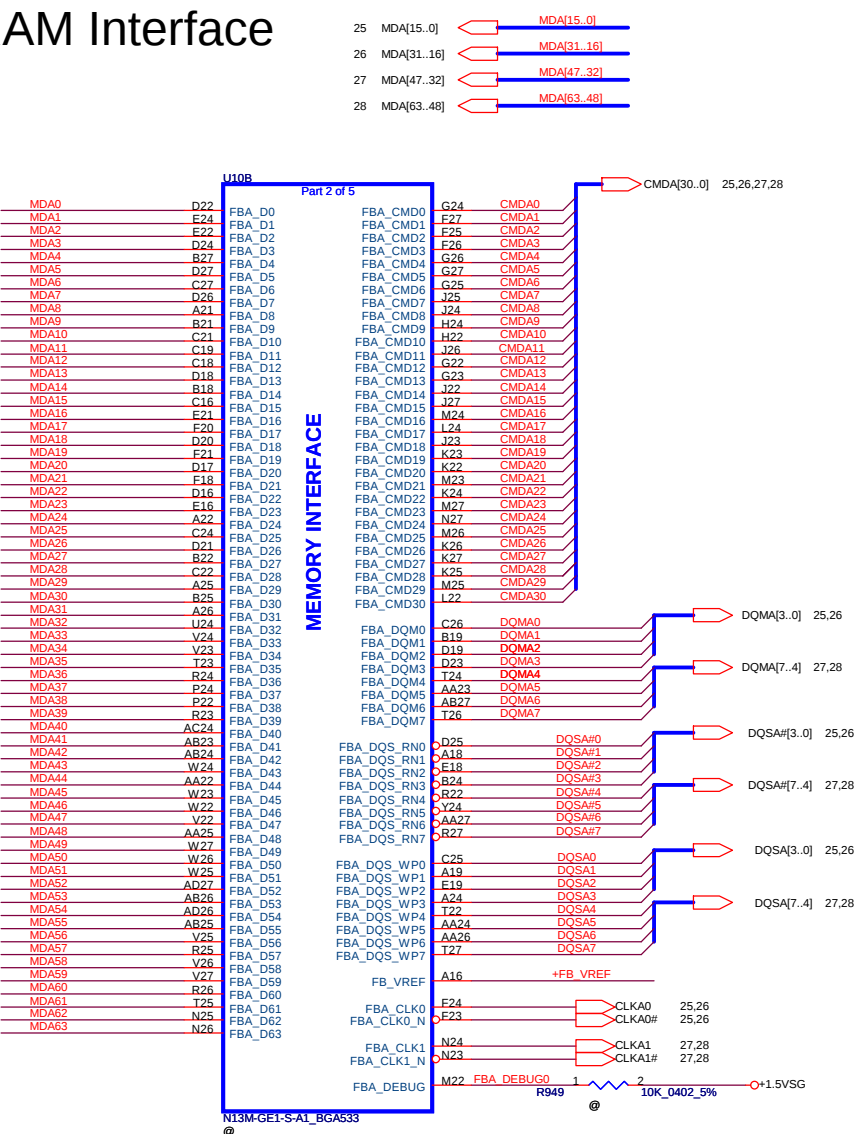
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				Date: Thursday, October 27, 2011	Rev 0.2
				Sheet 19 of 59	



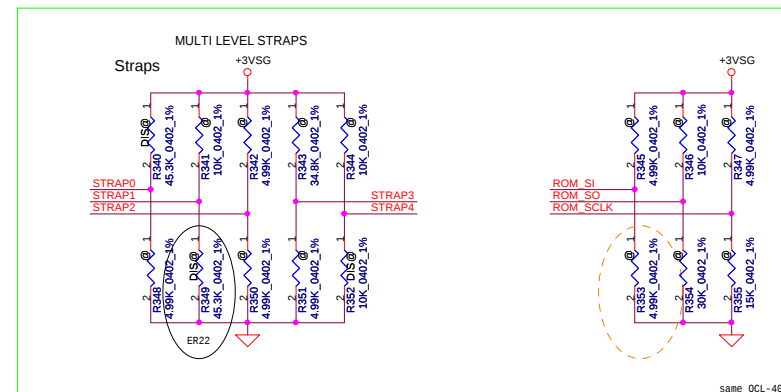
GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VDD
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT#
GPIO9	I/O	ALERT#
GPIO10	O	MEM_VREF_CTL
GPIO11	O	GPU_VID0
GPIO12	I	PWR_LEVEL
GPIO13	O	GPU_VID5
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	MEM_VDD_CTL
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved



VRAM Interface



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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		Deciphered Date		N13M VRAM 2/9	
		2012/12/31		Size	
				Document Number	
				LA-8224P	
				Rev	
				0.2	
				Date	
				Thursday, October 27, 2011	
				Sheet	
				21 of 59	

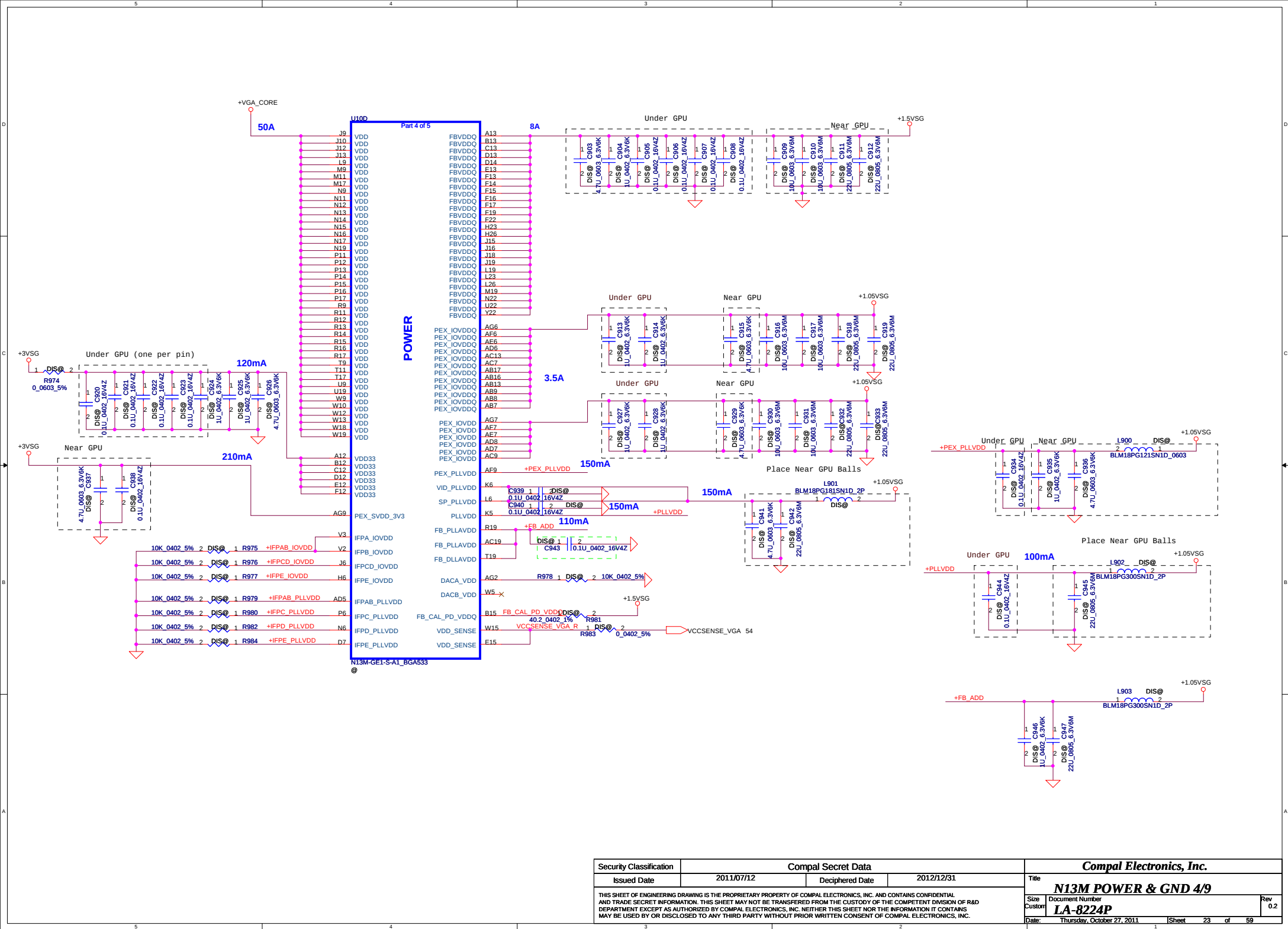


GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	667+ MHz	256M* 8" 8 2GB	HYNIX SA000056O00 HS7Q2G83CFR-H9C	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 10K	R PL 30K	R PH 5K
N13M-GE1	667+ MHz	256M* 8" 8 2GB	ELPIDA SA000056P90 EDJ2108BCSE-DJ-F	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 5K	R PL 30K	R PH 5K
N13M-GE1	667+ MHz	512M* 8" 8 4GB	HYNIX SA00005BL00 HS7Q4G83MFR-PBC	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 15K	R PL 30K	R PH 5K
N13M-GE1	667+ MHz	512M* 8" 8 4GB	ELPIDA SA000005A00 EDJ4208BBBG-GN-F	R PH 45K	R PL 45K	R PH 5K	R PL 5K	R PL 10K	R PL 20K	R PL 30K	R PH 5K

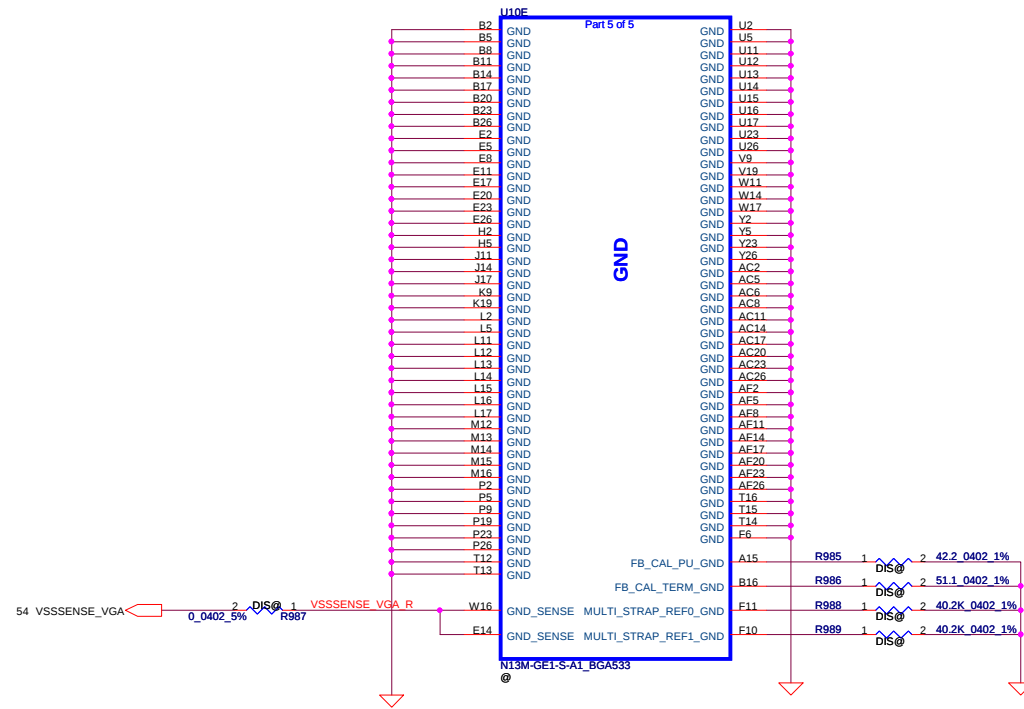
256M*8*8
1. SA000056000
DDR3 1600 256*8 1.5V FBGA78
HYNIX/H5TQ2G83CFR-PBC
2. SA000056P00
DDR3 1600 256*8 1.5V FBGA78
ELPIDA/EDJ2108BDBG-GN-F

512M*8*8
1. SA00005BL00
DDR3 1600 512M*8 1.5V FBGA78
HYNIX/H5TQ4G83MFR-PBC
2. SA00005AA00
DDR3 1600 512M*8 1.5V FBGA78
ELPIDA/EDJ4208BBBG-GN-F

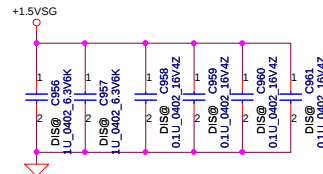
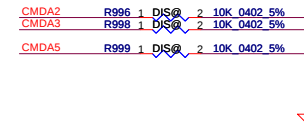
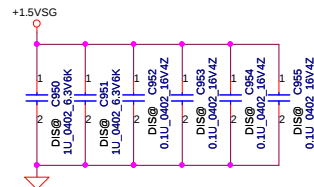
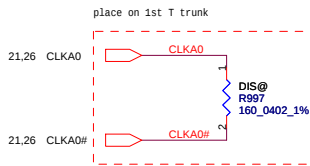
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				Date:	Thursday, October 27, 2011		Sheet 22 of 59



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				Date:	Thursday, October 27, 2011	Sheet



256Mx8 DDR3 *8==>2GB

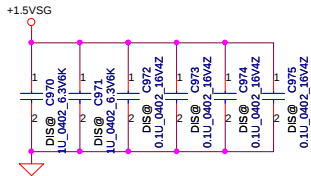
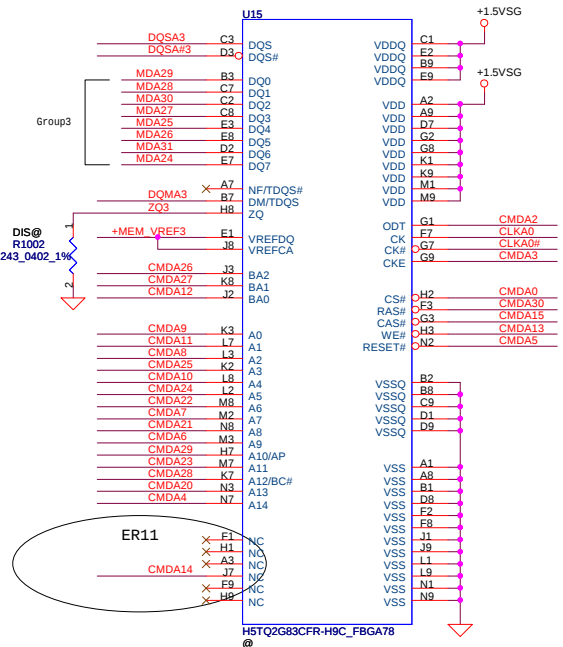
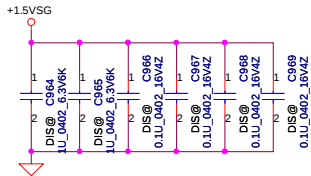
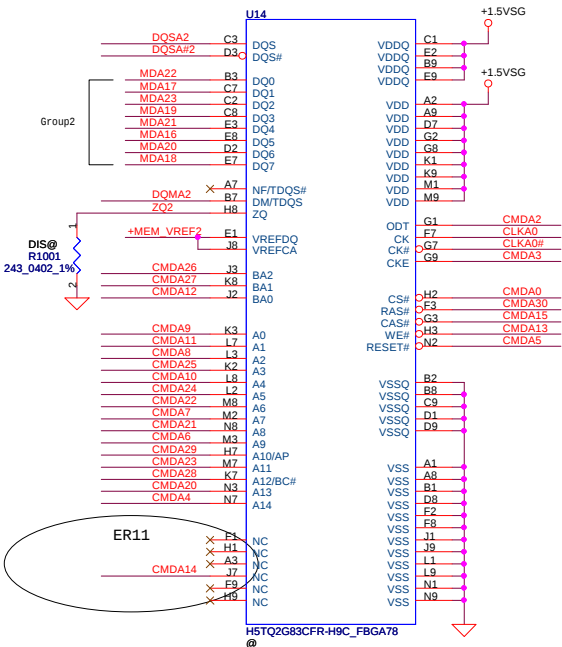
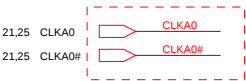
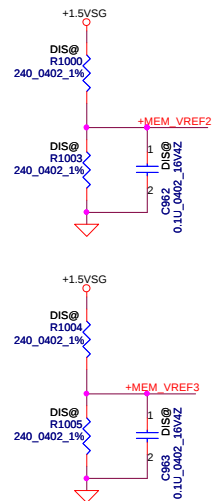
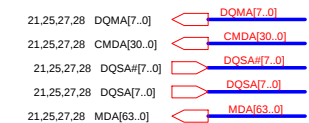


	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)
Elpida : SAxxxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx)

VRAM DDR3 chips

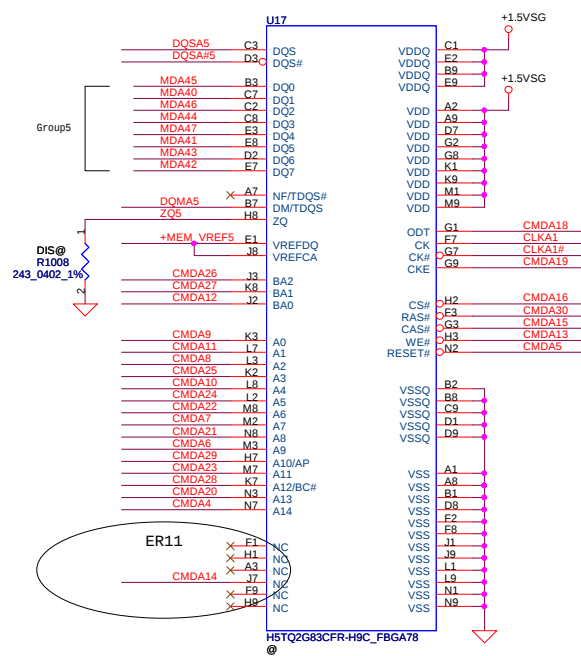
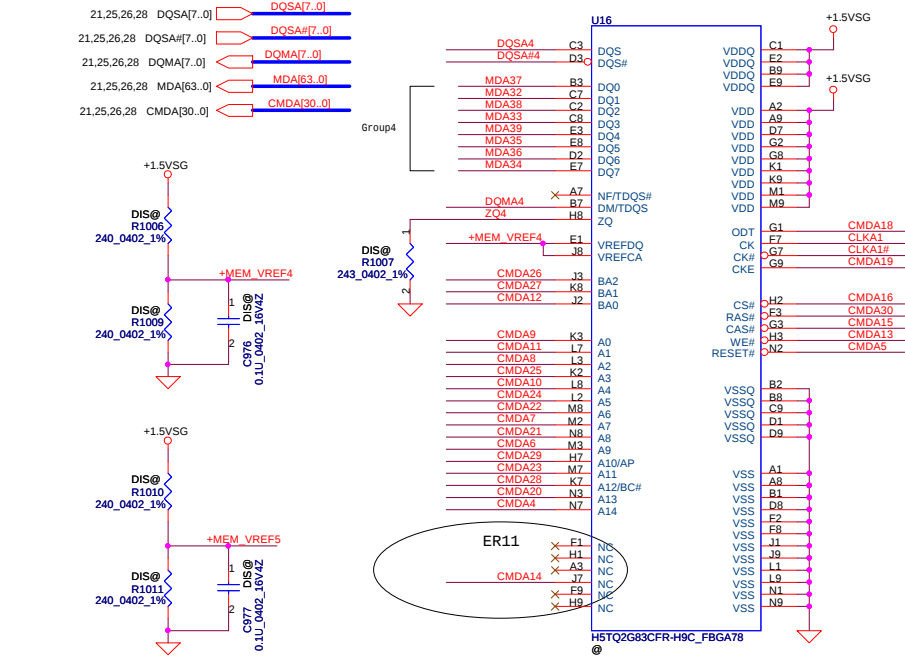
256Mx8 DDR3 *8==>2GB



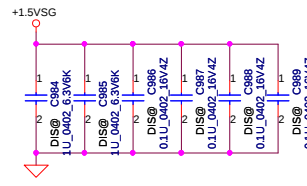
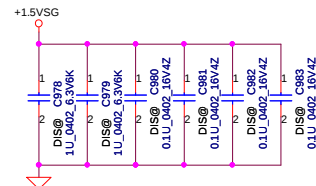
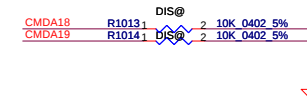
Mode D Address	0...31	32...63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

VRAM DDR3 chips

256Mx8 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

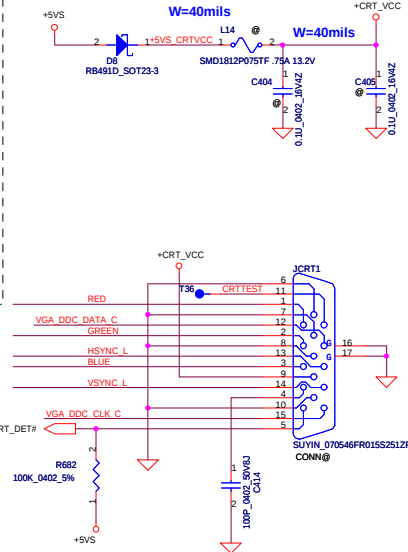
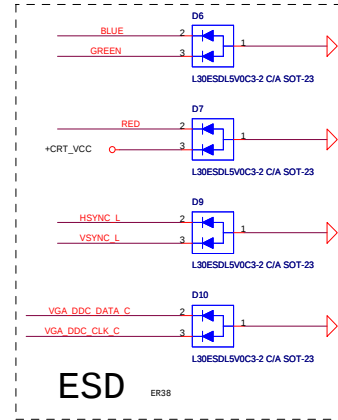
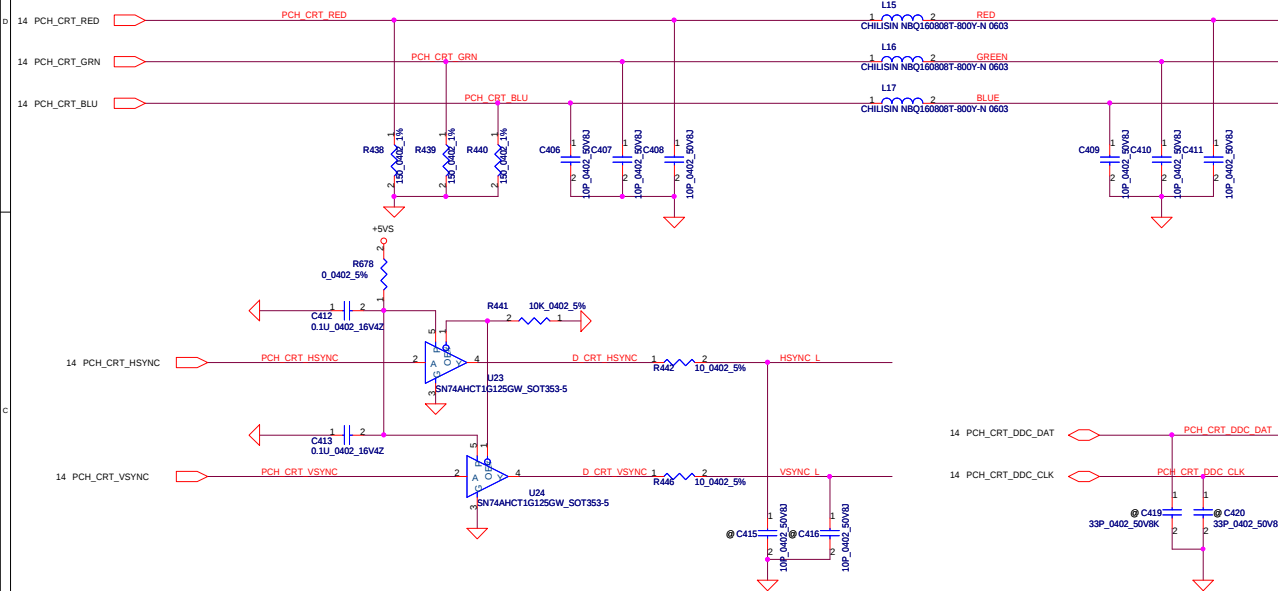


Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA)

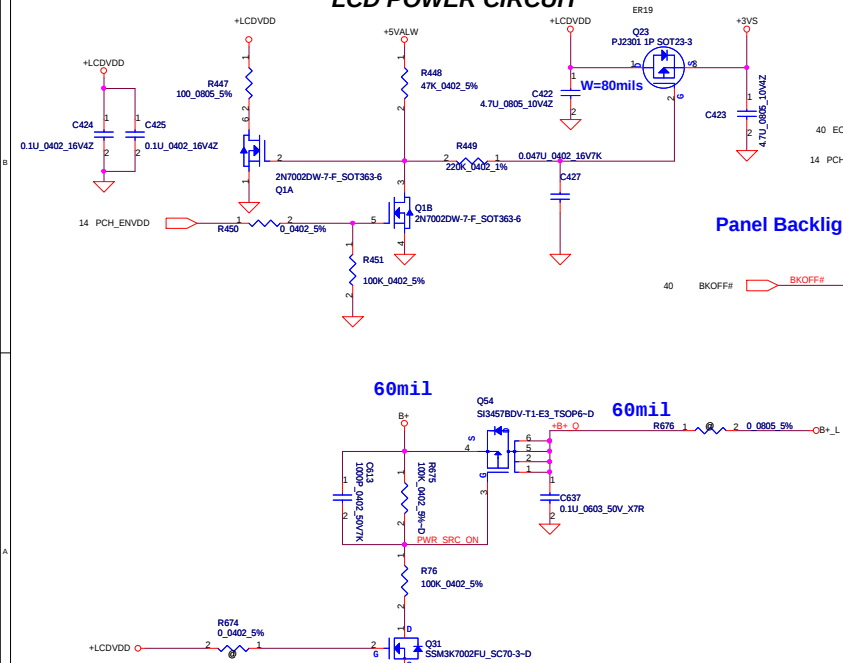
Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxx)

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				Sheet 27 of 59	

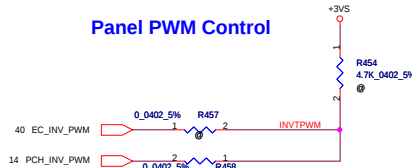
CRT



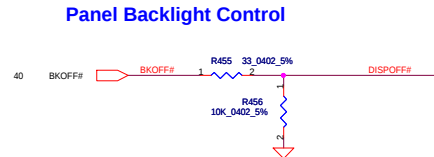
LCD POWER CIRCUIT



Panel PWM Control



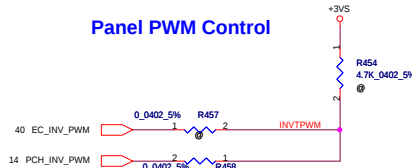
Panel Backlight Control



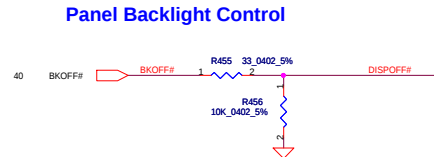
60mil

60mil

Panel PWM Control



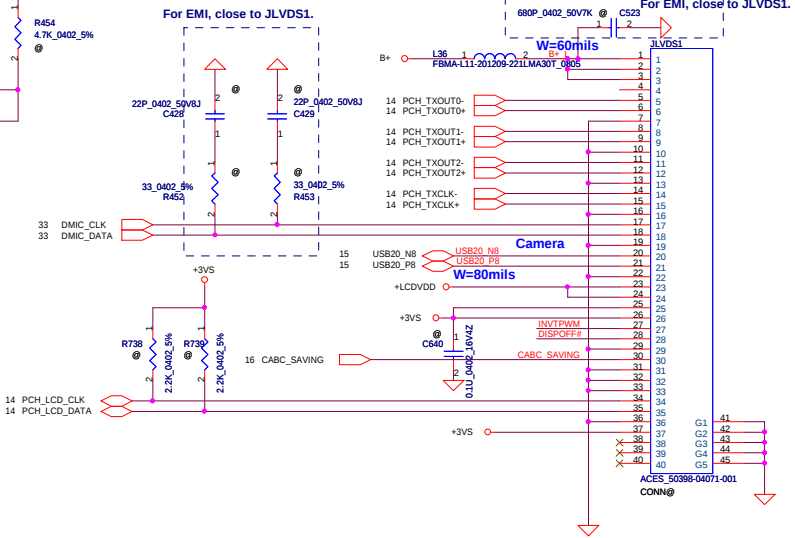
Panel Backlight Control



60mil

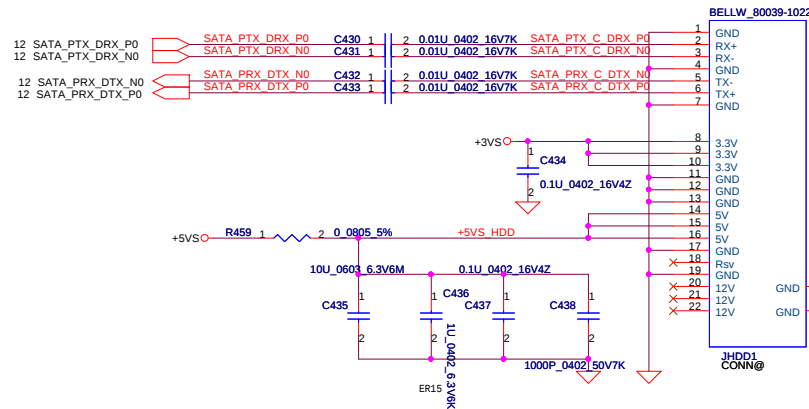
60mil

For EMI, close to JLVDS1.

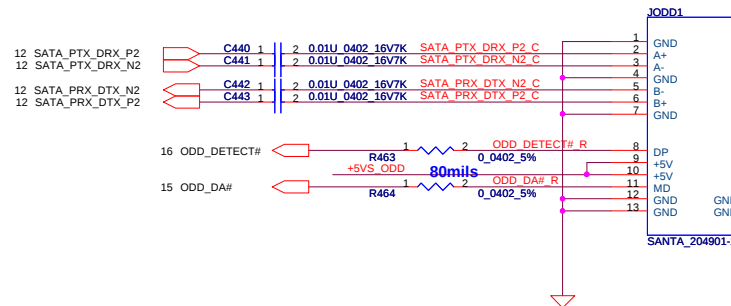


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Compal Electronics, Inc.				LA-8224P
LVDS/CRT CONN				Rev
Date: Thursday, October 27, 2011				Sheet 30 of 59

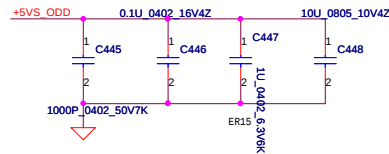
SATA HDD Conn.



SATA ODD Conn.

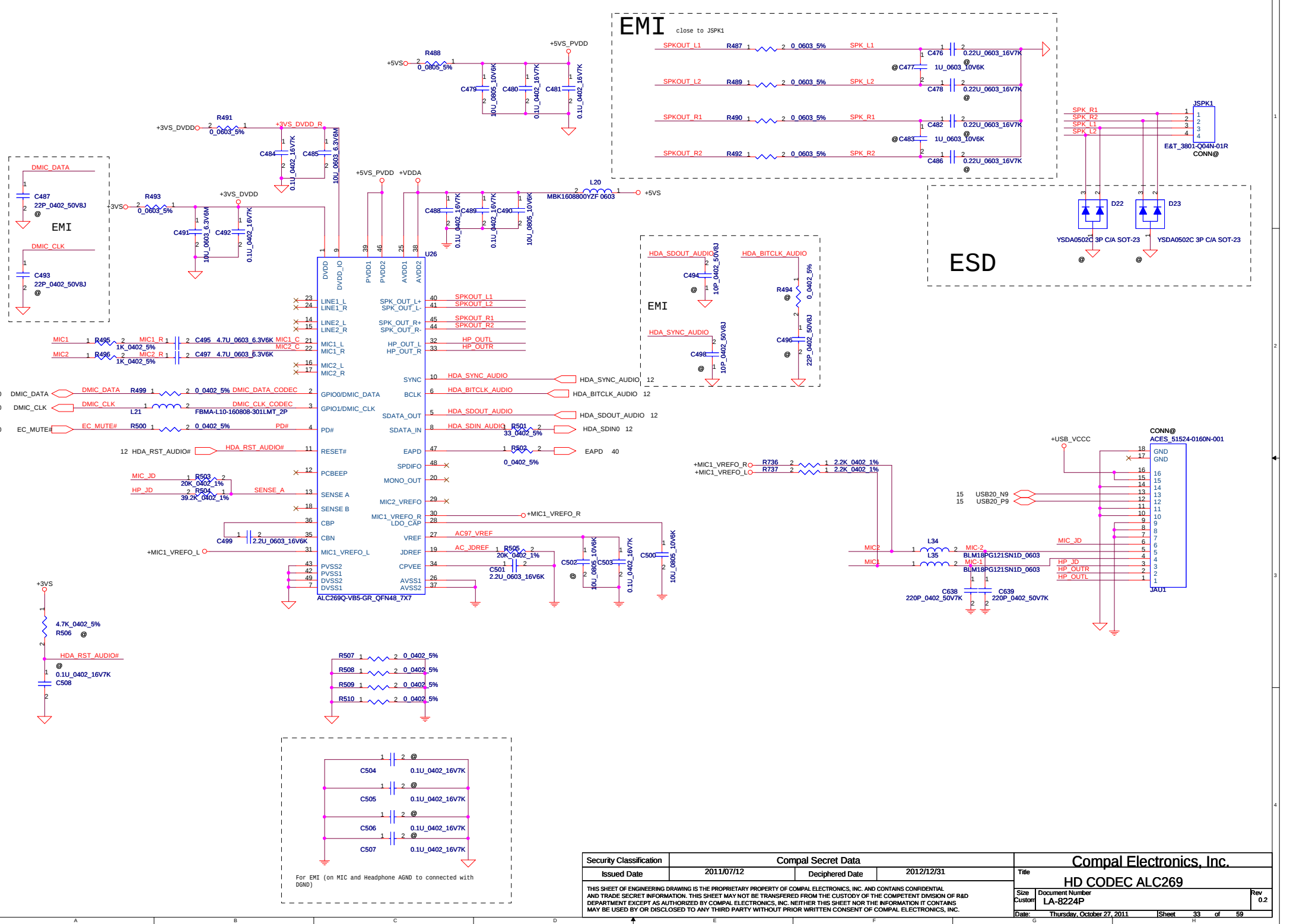


Place caps. near ODD CONN.

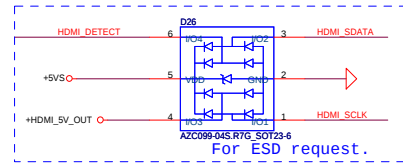
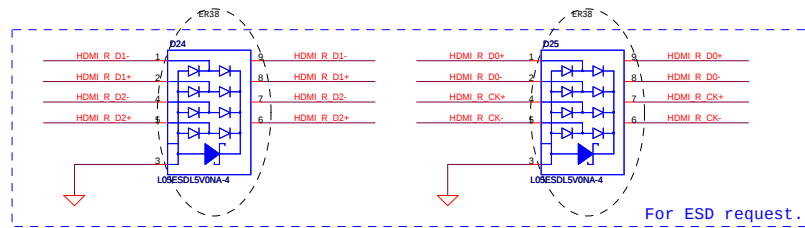


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Issued Date				2011/07/12				Title			
				Deciphered Date				HDD & ODD CONN			
				2012/12/31				Size B			
								Document Number			
								LA-8224P			
								Date: Thursday, October 27, 2011			
								Sheet 31 of 59			
								Rev 0.2			

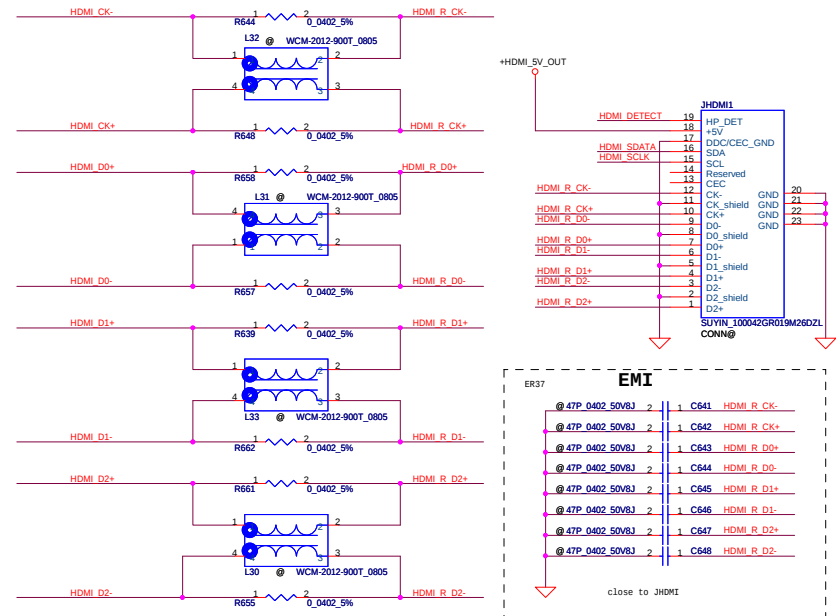
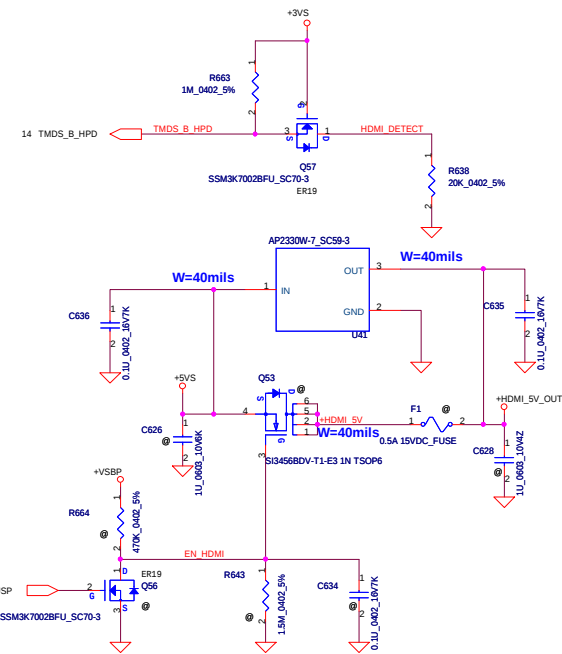
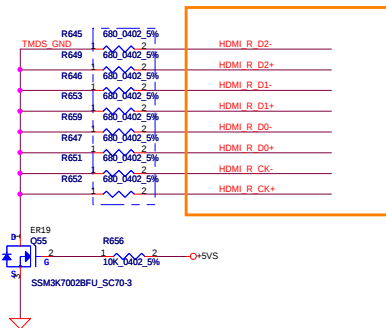
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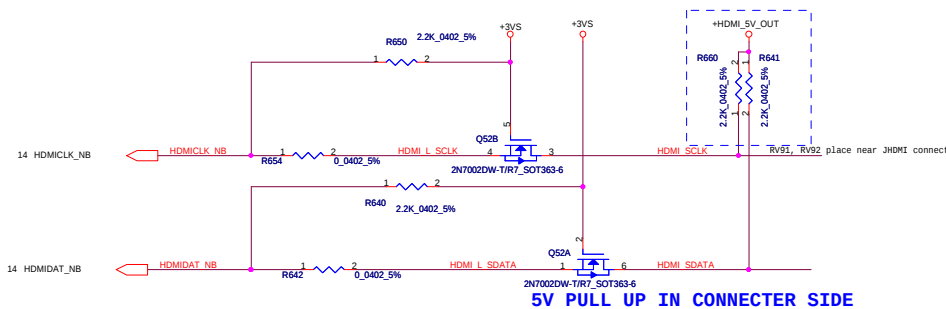
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
Custom	LA-8224P	0.2		Thursday, October 27, 2011	
Sheet		33		of	
59					



14	TMDS_B_CLK	0.1U 0402 16V7K	2	1	C625	HDMI CK+
14	TMDS_B_CLK#	0.1U 0402 16V7K	2	1	C624	HDMI CK-
14	TMDS_B_DATA0	0.1U 0402 16V7K	2	1	C630	HDMI D0+
14	TMDS_B_DATA0#	0.1U 0402 16V7K	2	1	C631	HDMI D0-
14	TMDS_B_DATA1	0.1U 0402 16V7K	2	1	C633	HDMI D1+
14	TMDS_B_DATA1#	0.1U 0402 16V7K	2	1	C627	HDMI D1-
14	TMDS_B_DATA2	0.1U 0402 16V7K	2	1	C629	HDMI D2+
14	TMDS_B_DATA2#	0.1U 0402 16V7K	2	1	C632	HDMI D2-



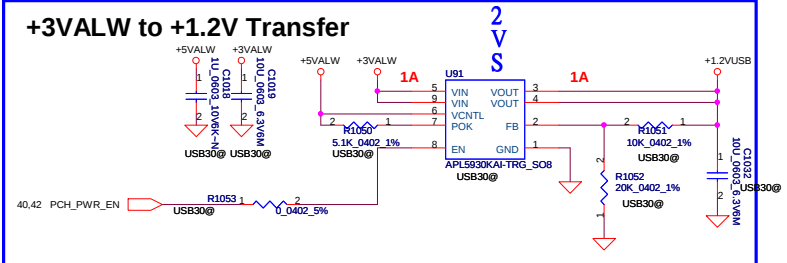
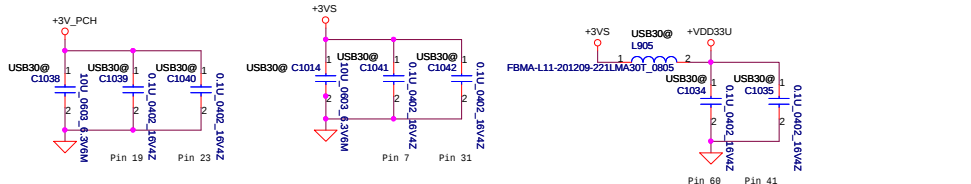
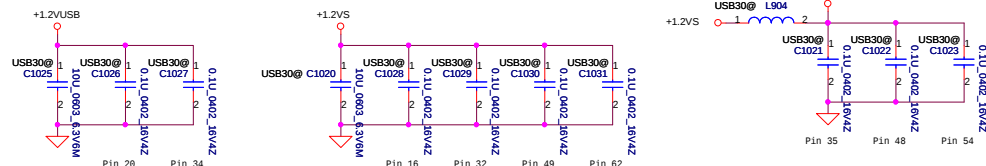
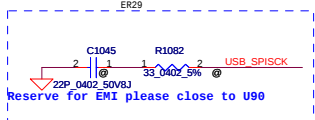
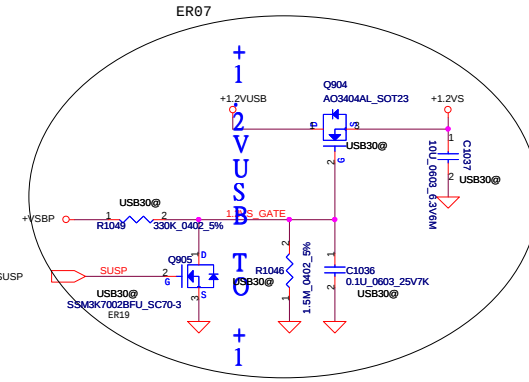
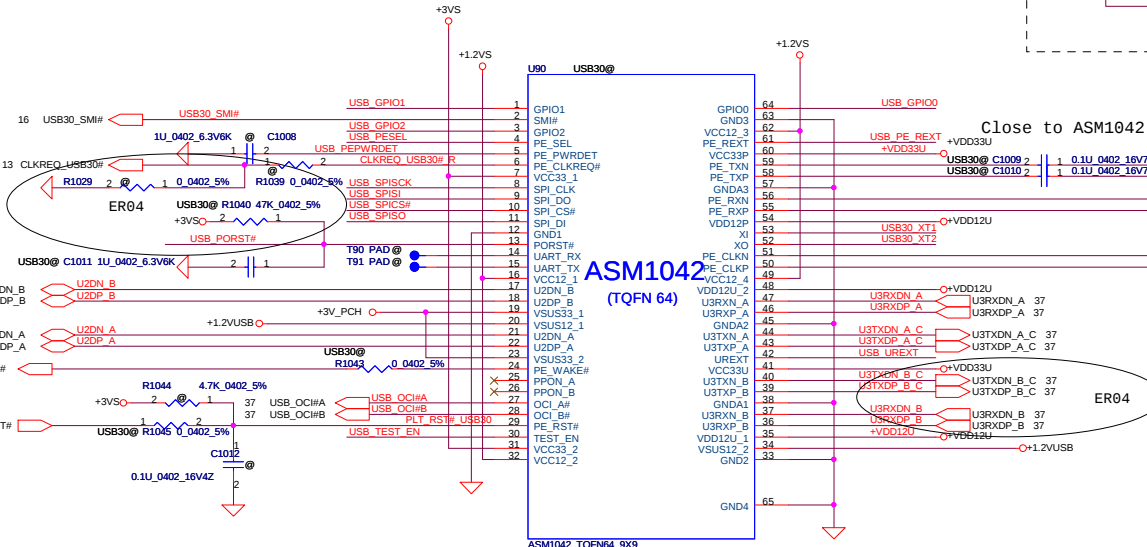
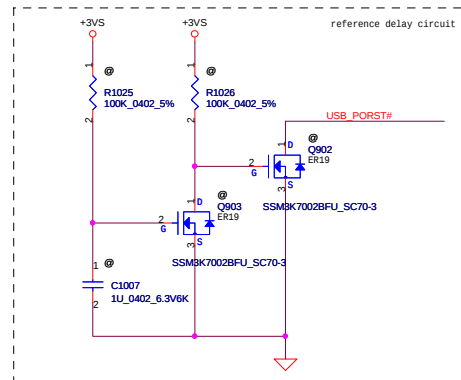
HDMI



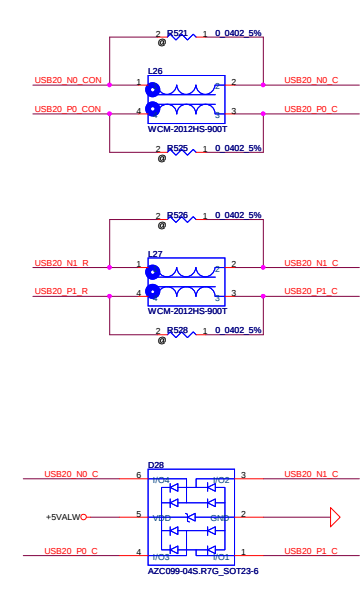
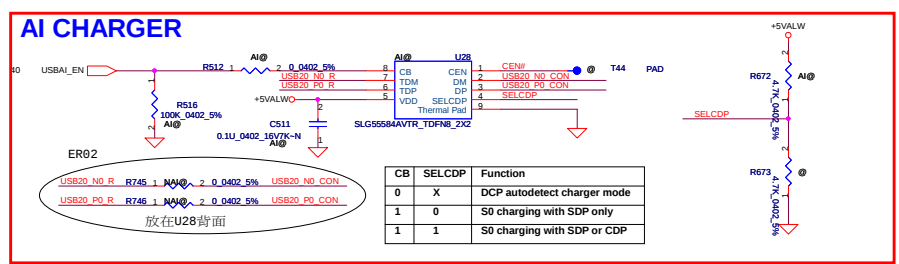
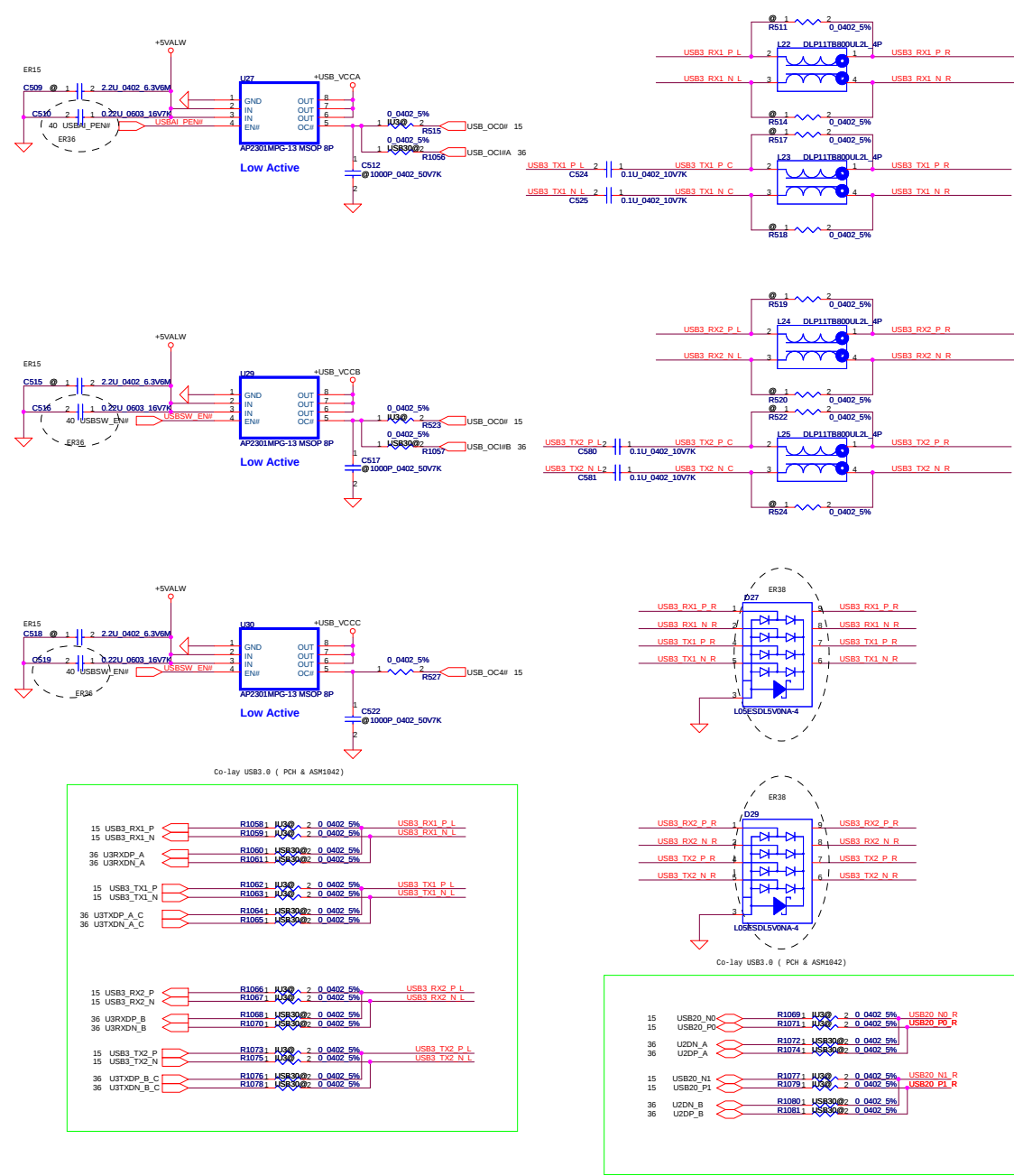
5V PULL UP IN CONNECTER SIDE

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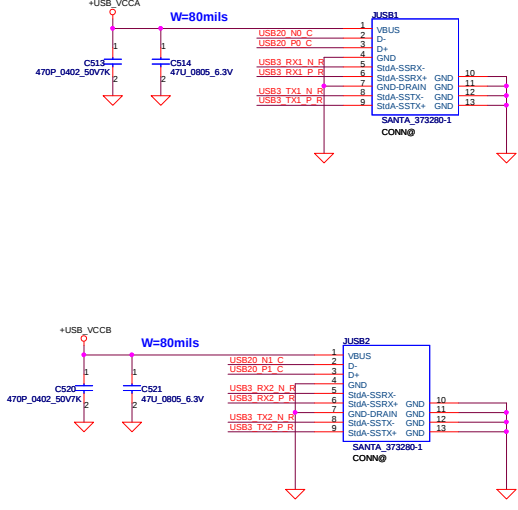
Power Sequence

USB_PESSELBusiness Card/Mini

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Issued Date	2010/01/	Deciphered Date	2012/06/30	Title USB3.0 controller		
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				Custom	LA-8224P	0.2
				Date:	Thursday, October 27, 2011	Sheet 36 of 59

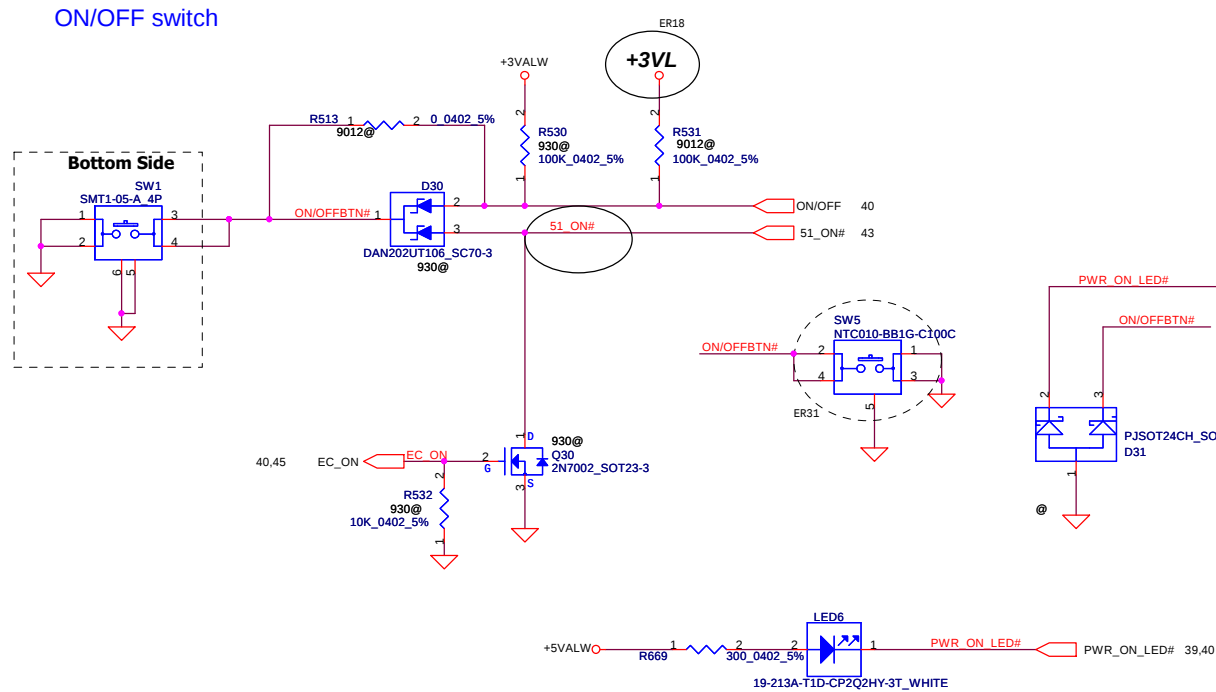


charger port: left side & near user

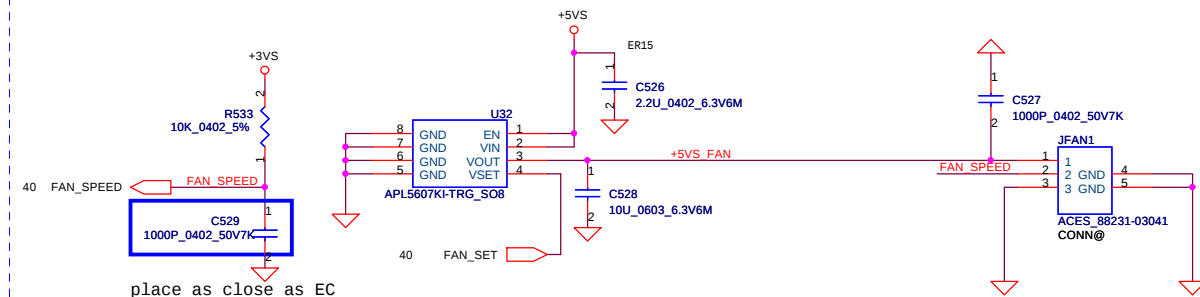


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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Size	210mm	Document Number	LA-8224P	Rev 0.2	
Date	Thursday, October 27, 2011	Sheet	37	of 59	

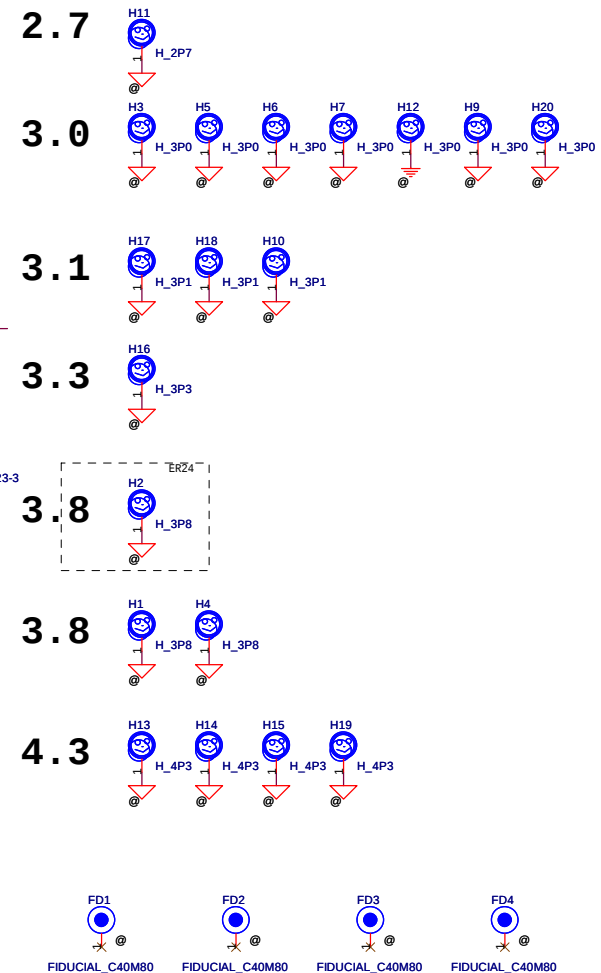
Power Button



Fan Control Circuit

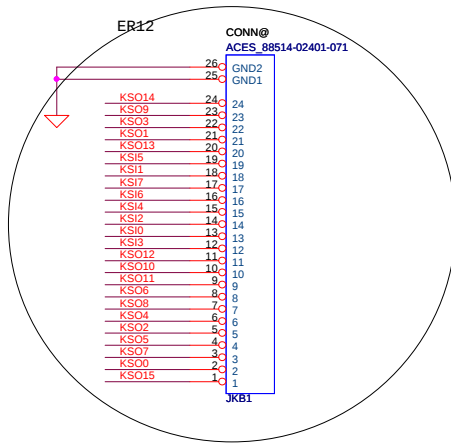
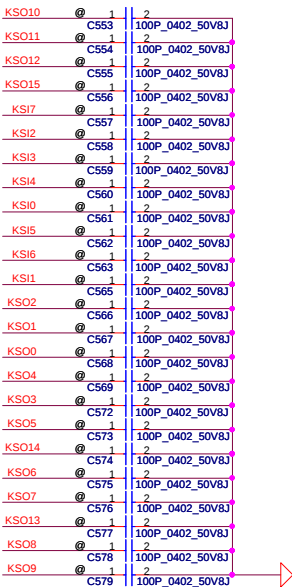


Screw Hole

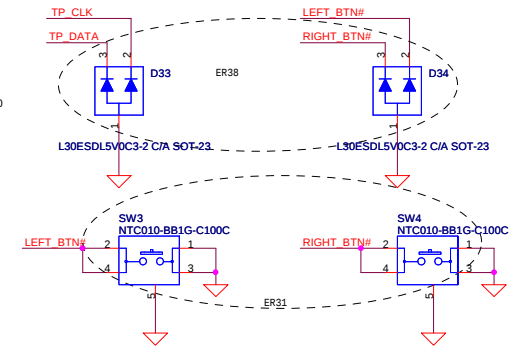
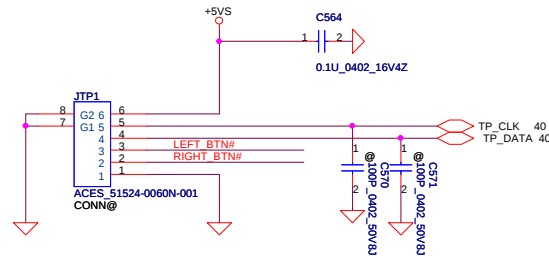


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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title		
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				Custom	LA-8224P	0.2
				Date:	Thursday, October 27, 2011	Sheet 38 of 59

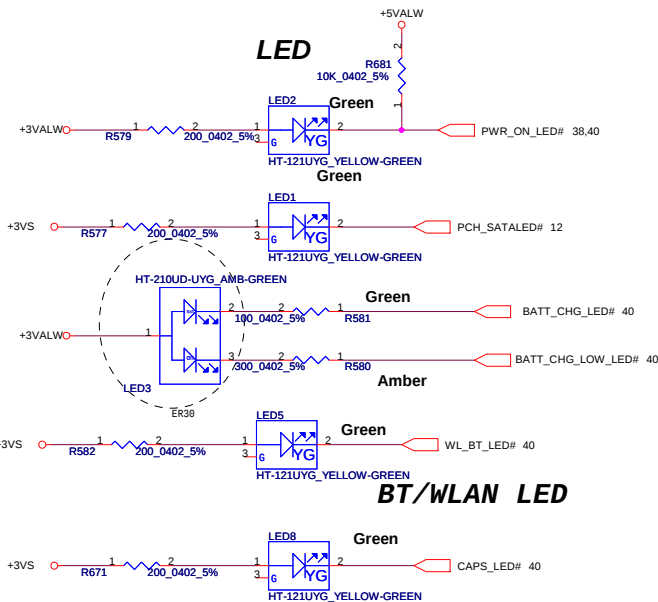
INT_KBD Conn.



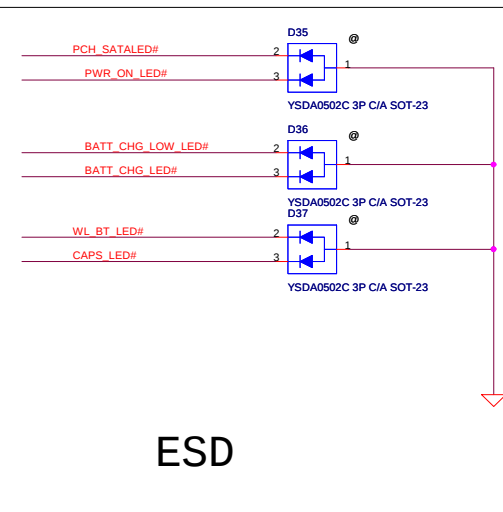
Touch/B Connector



LED

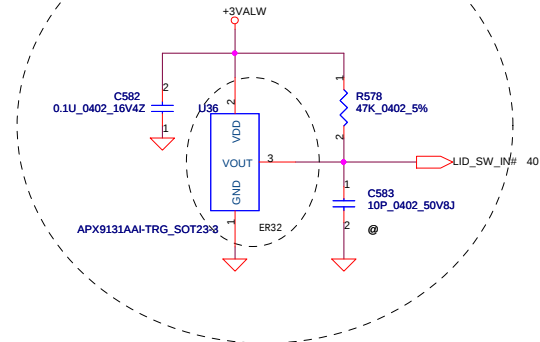


BT/WLAN LED

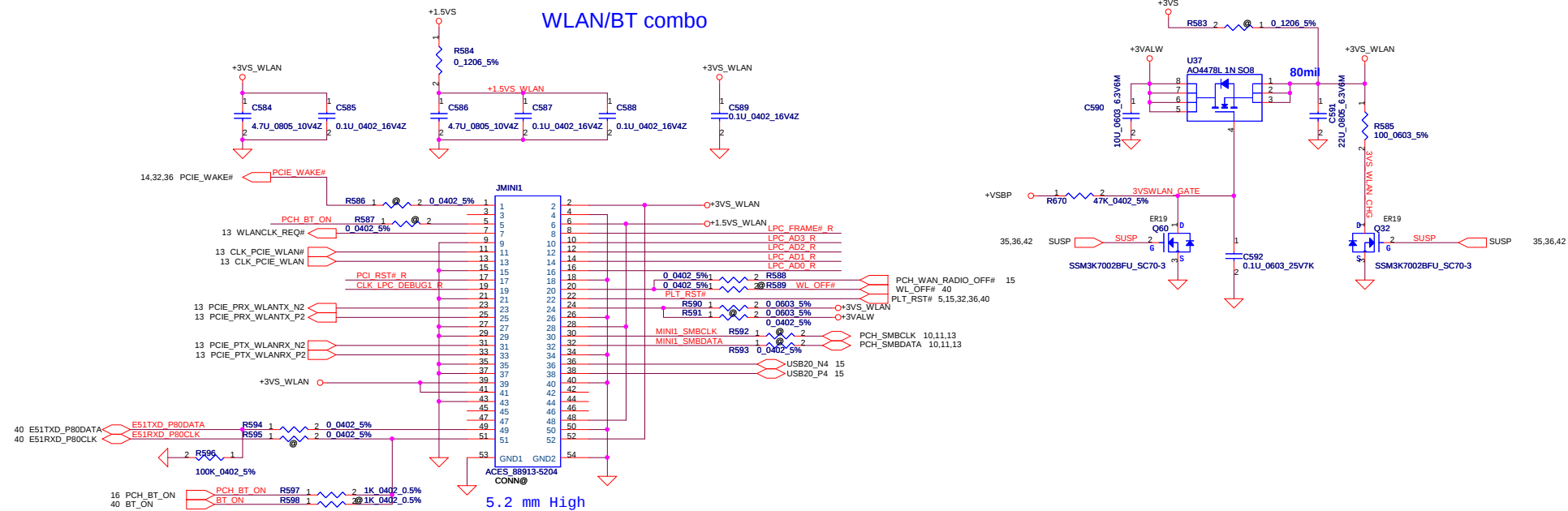


ESD

Lid Switch (Hall Effect Switch)



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				B	LA-8224P
				Date	Thursday, October 27, 2011
				Sheet	39 of 59
				Rev	0.2



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				Size	Document Number	Rev
				LA-8224P		
				Date:	Thursday, October 27, 2011	Sheet 41 of 59

Compal Electronics, Inc.

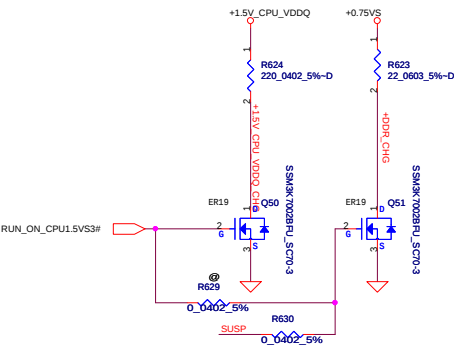
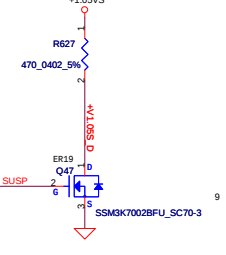
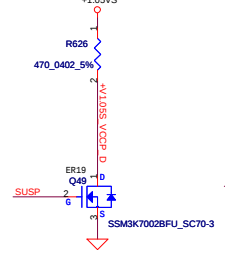
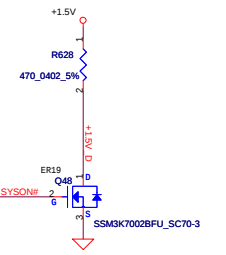
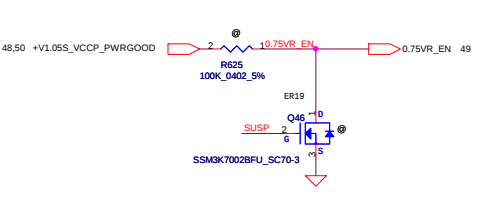
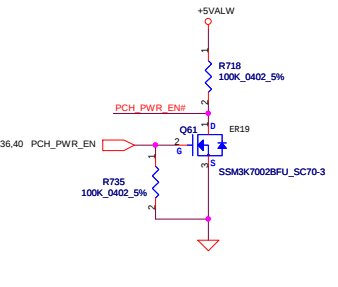
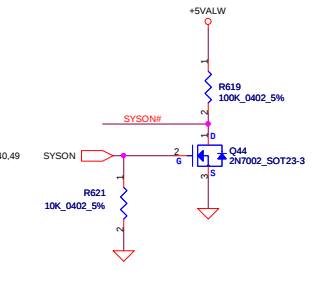
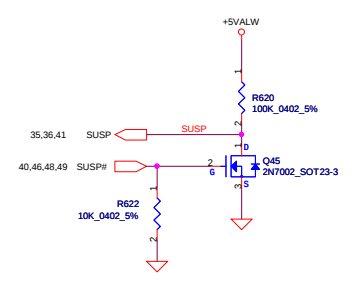
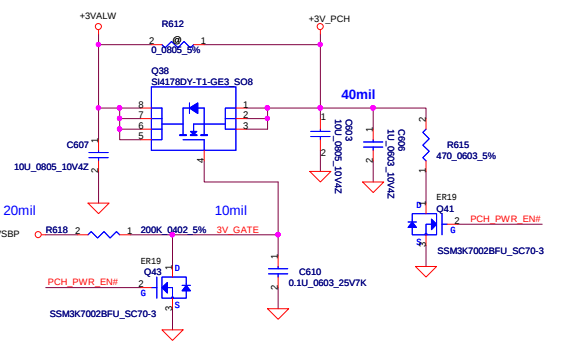
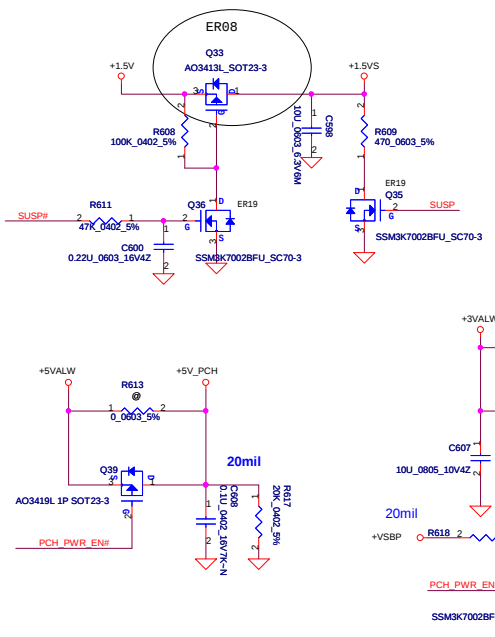
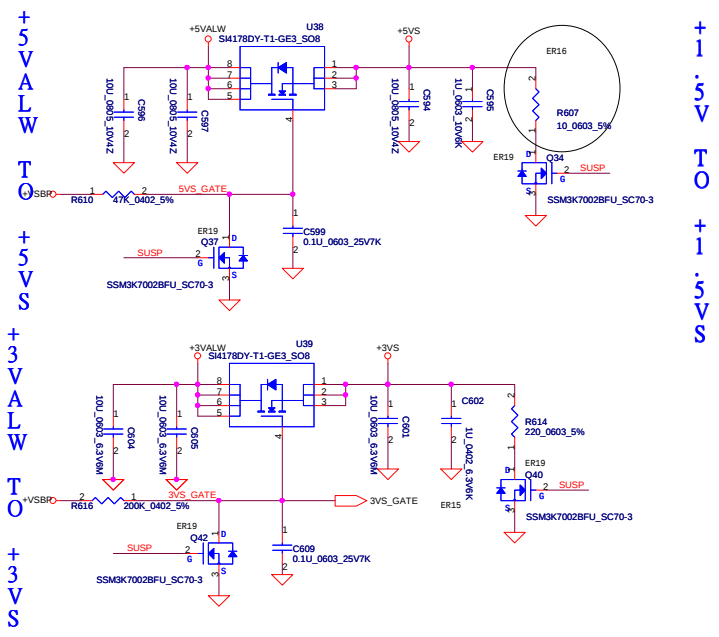
WLAN/ WWAN/ m-SATA

LA-8224P

Thursday, October 27, 2011

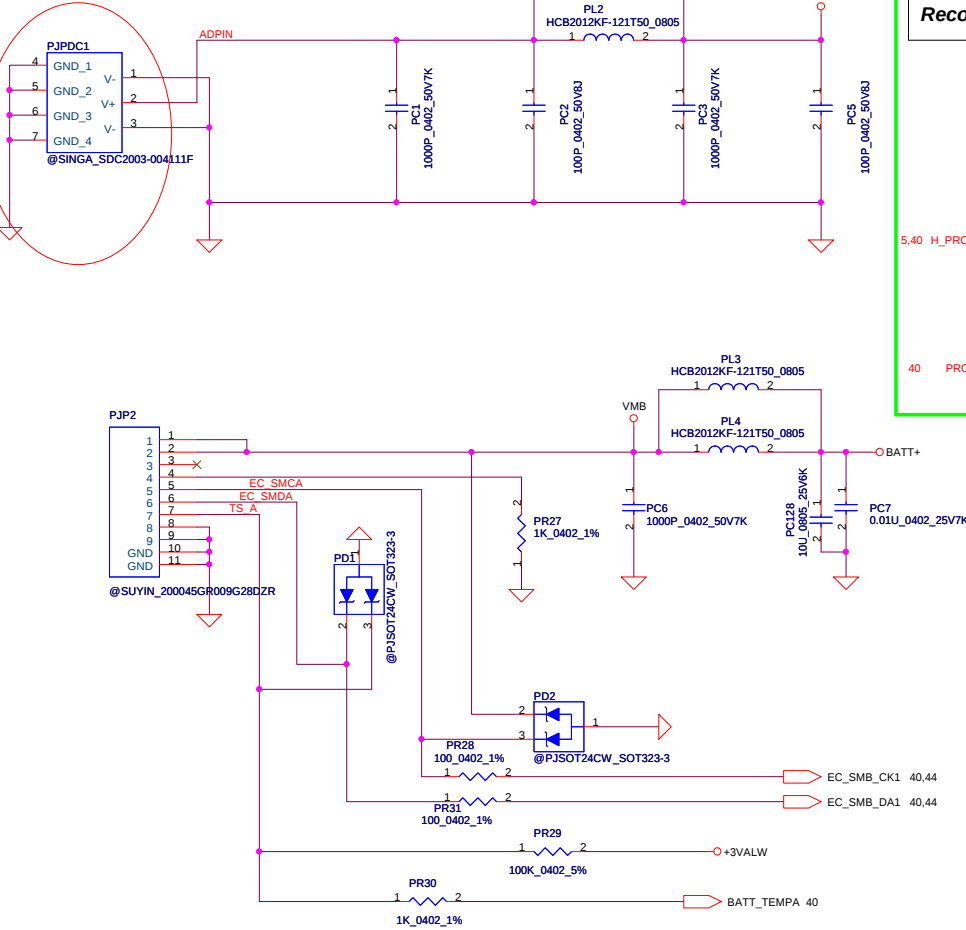
Sheet 41 of 59

Rev 0.2

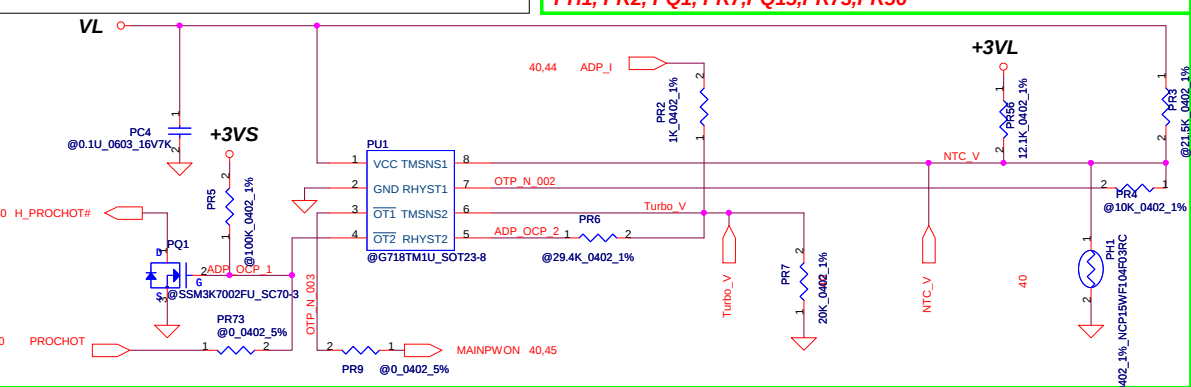


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				DC/DC Interface			
				Size			
				Custom			
				LA-8224P			
Date:				Thursday, October 27, 2011			
Sheet				42 of 59			

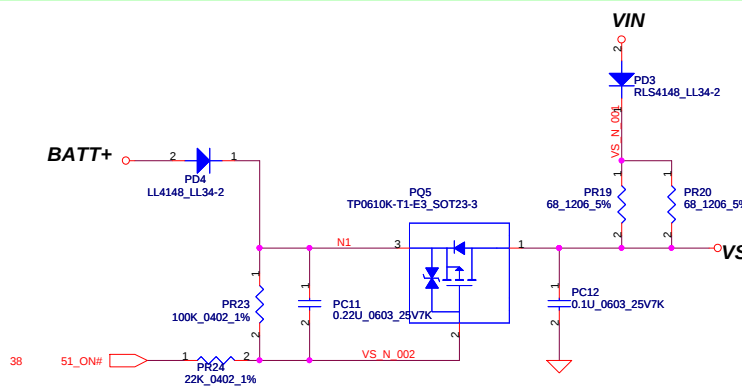
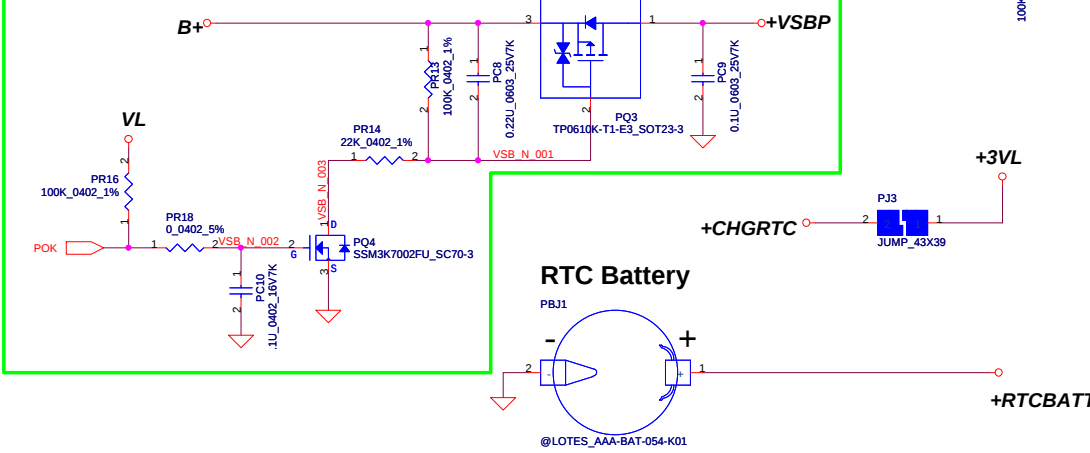
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



PH1 under CPU botten side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

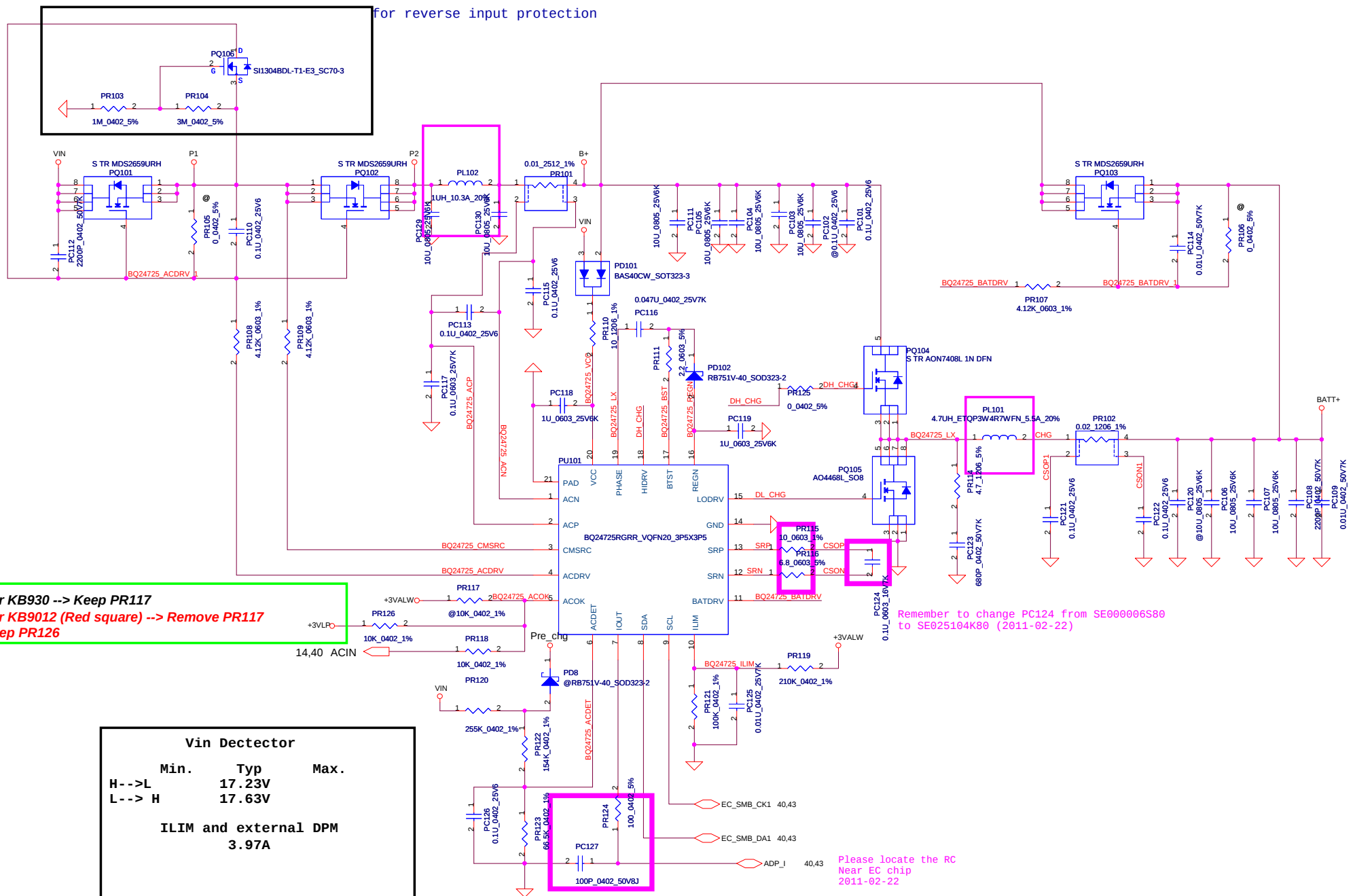


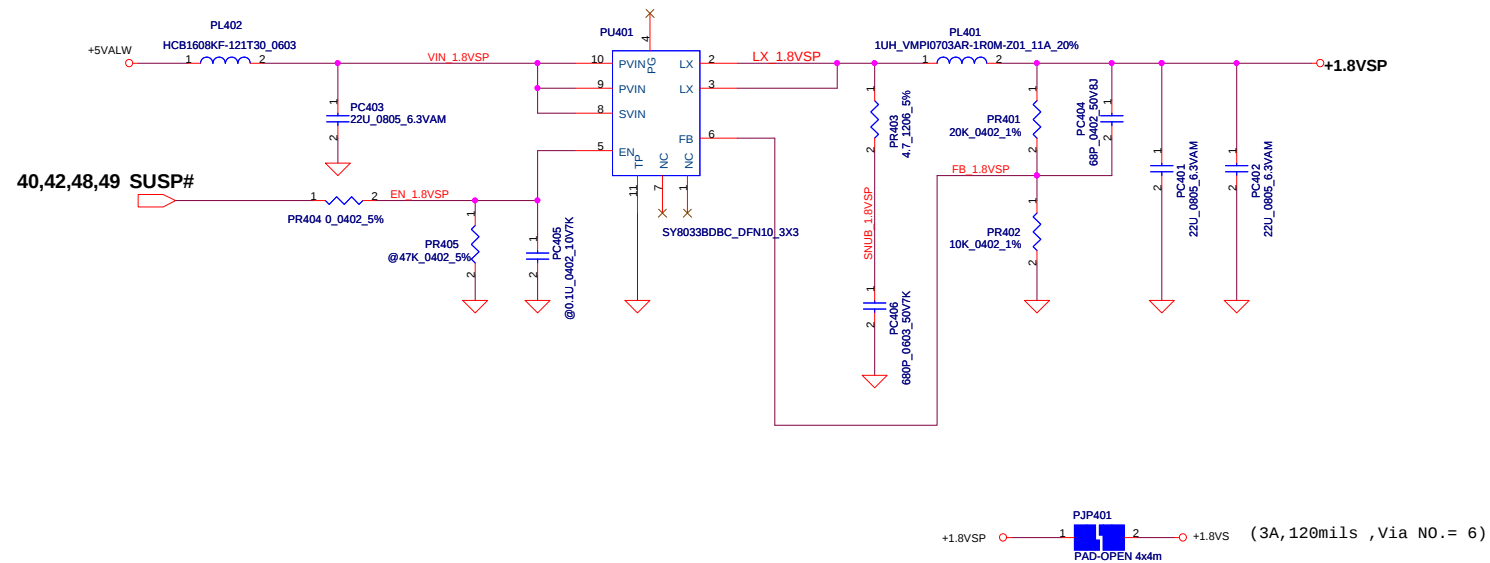
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56



For KB9012 --> Remove all 51_ON# circuit

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Size	Document Number	PBL22 LA-7391P M/B			Date: Thursday, October 27, 2011
Sheet	43	of 59			





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Size		Document Number		Rev	
Date: Thursday, October 27, 2011		Sheet 46 of 59		0.2	

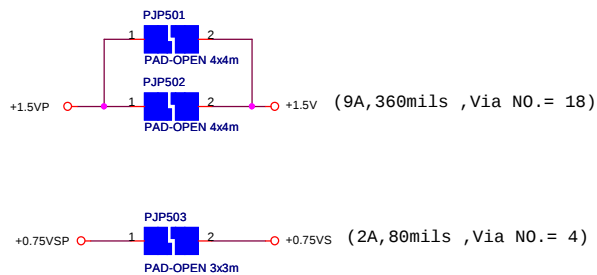
(8.5A,360mils ,Via N0.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date: Thursday, October 27, 2011	Rev 0.2
				Sheet 47 of 59	

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

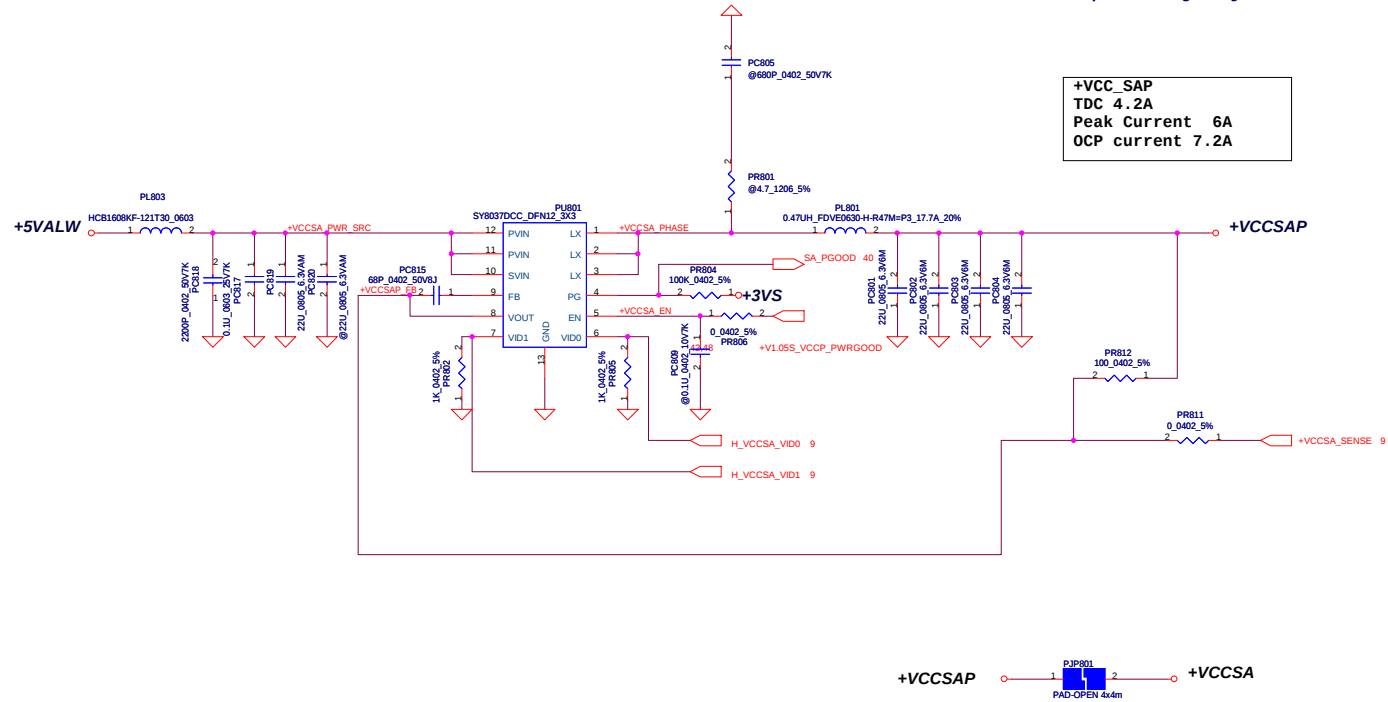


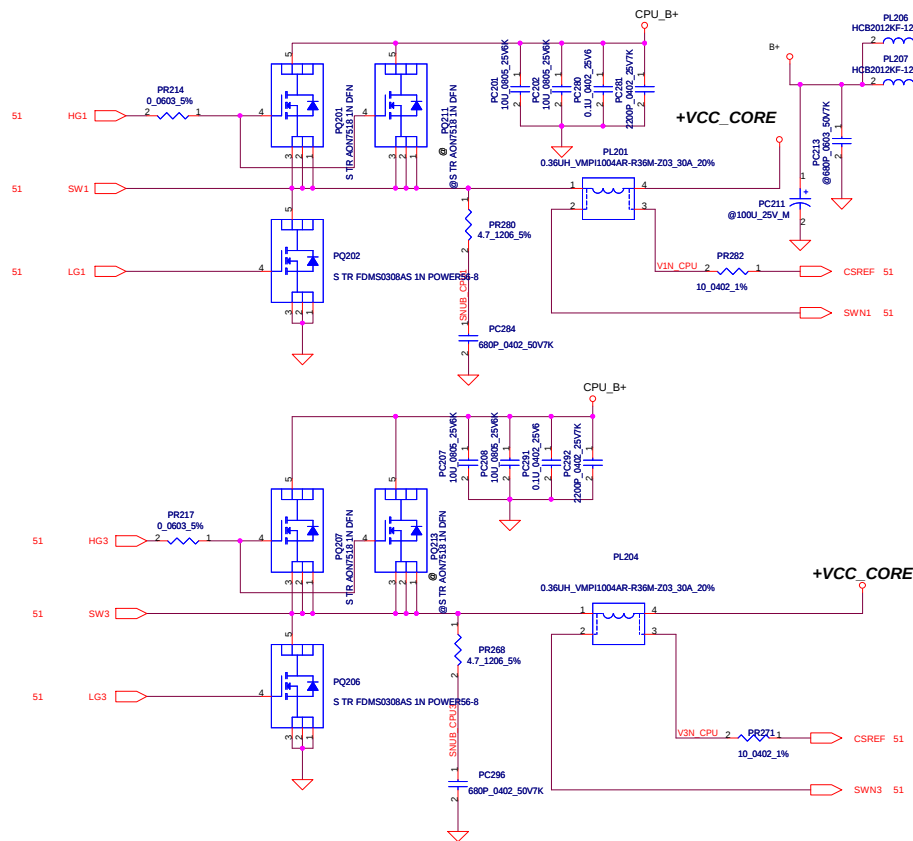
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Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	
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Size	Custom	Document Number	PBL22 LA-7391P M/B	Rev	0.2
Date:	Thursday, October 27, 2011	Sheet	49	of	59

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



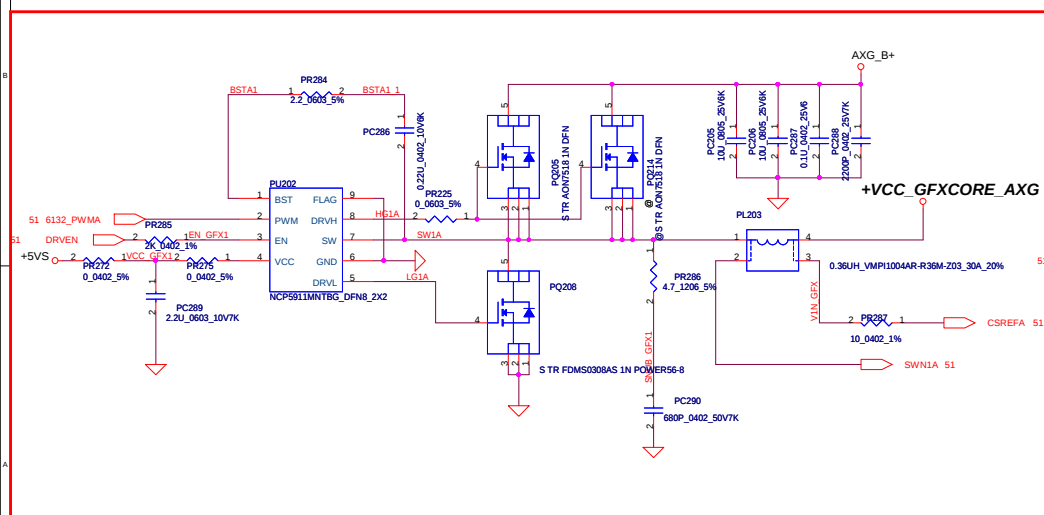


QC 45W CPU
VID1=0.9V
Icc_Max=94A
Icc_Dyn=66A
R_TDC=56A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
Icc_Max=53A
Icc_Dyn=43A
R_TDC=33A
R_LL=1.9m ohm
OCP~65A

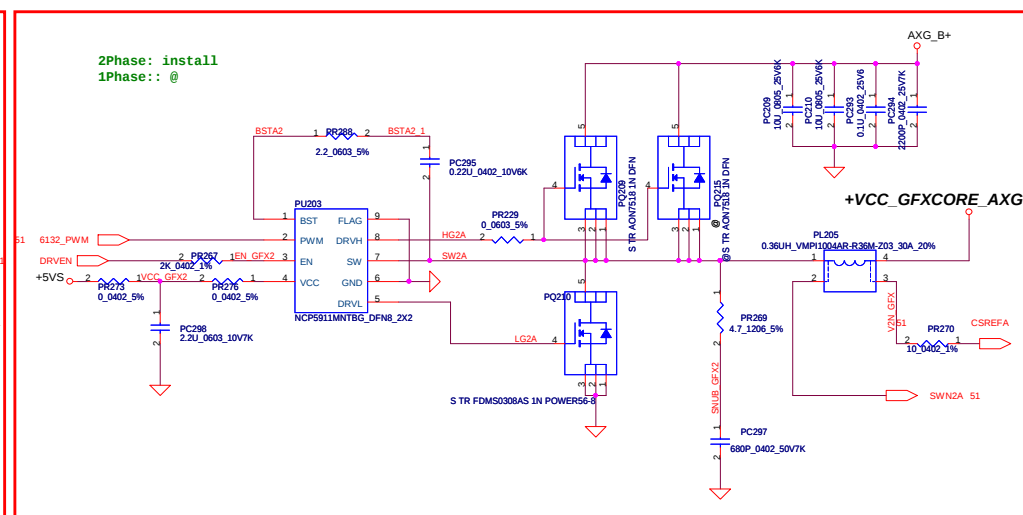
QC 45W CPU
solution: 3+2
MOS: cpu_core --> 上1(CSD17308)下1(TPCA8059)
Gfx_core --> 上1(CSD17308)下1(TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core --> 上1(CSD17308)下1(TPCA8059)
Gfx_core --> 上1(CSD17308)下1(TPCA8057)

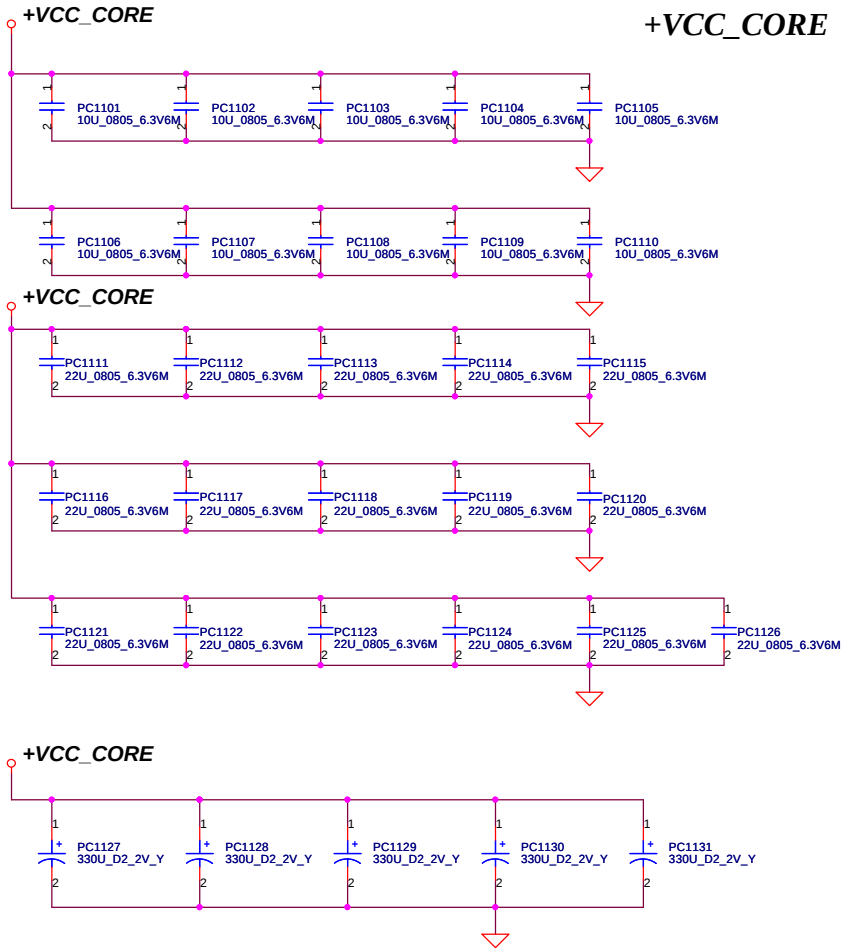


QC 45W GT2
VID1=1.23V
Icc_Max=46A
Icc_Dyn=37A
R_TDC=38A
R_LL=3.9m ohm
OCP~55A

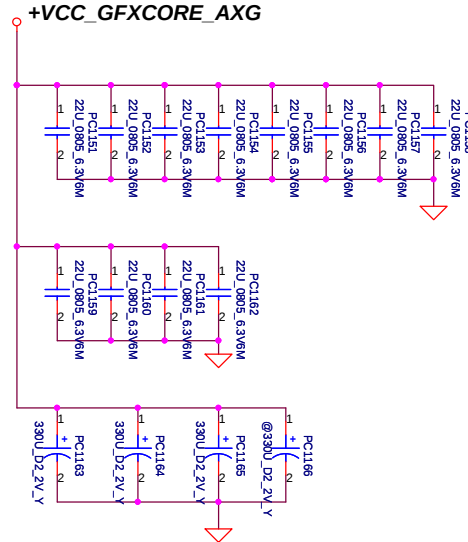
DC 35W GT2
VID1=1.23V
Icc_Max=33A
Icc_Dyn=20.2A
R_TDC=21.5A
R_LL=3.9m ohm
OCP~40A



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				Date:	Thursday, October 27, 2011
				Sheet	52 of 59

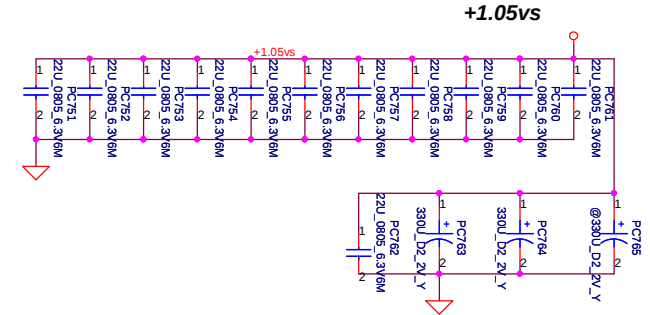


+VCC_GFXCORE_AXG



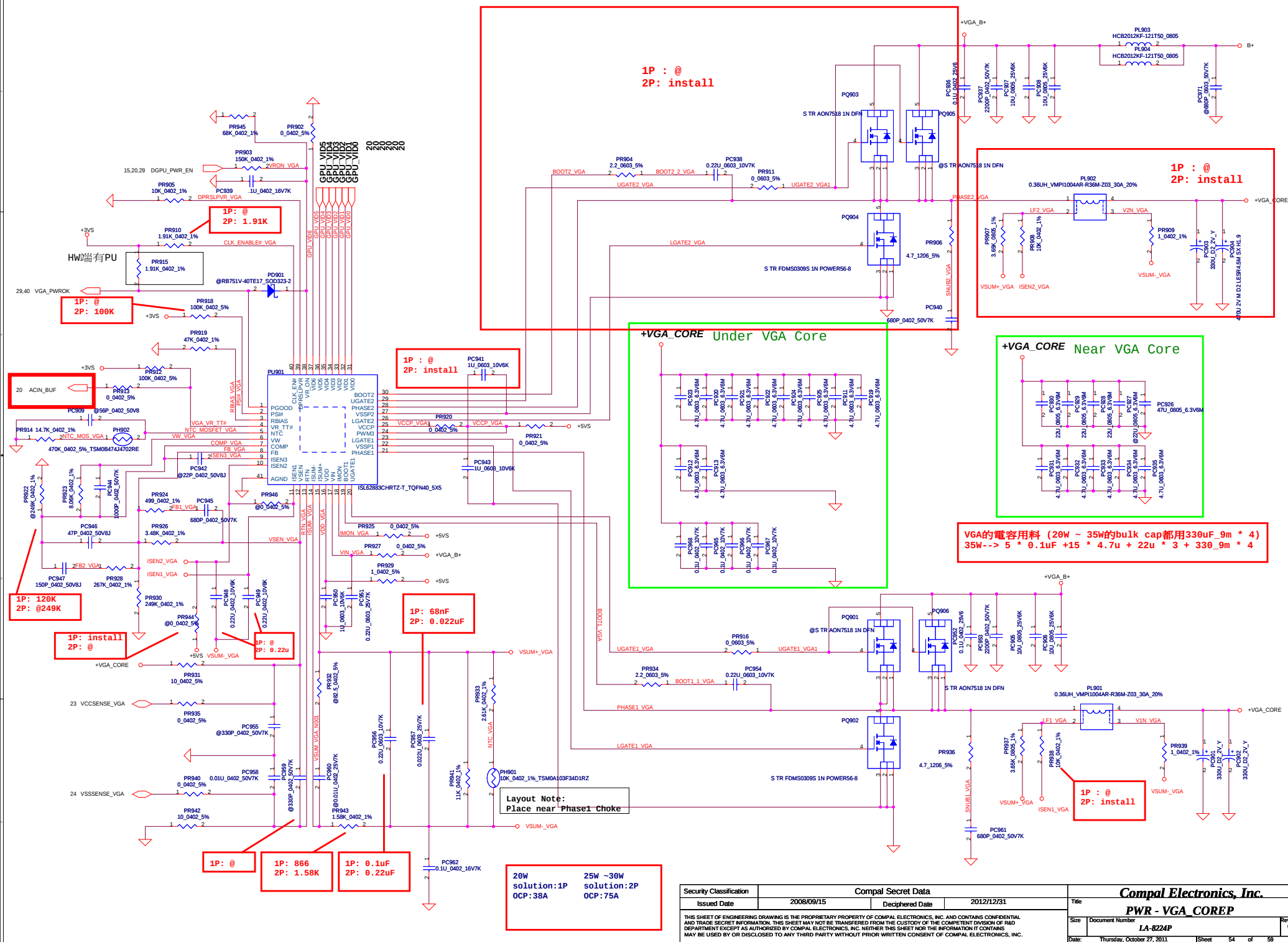
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

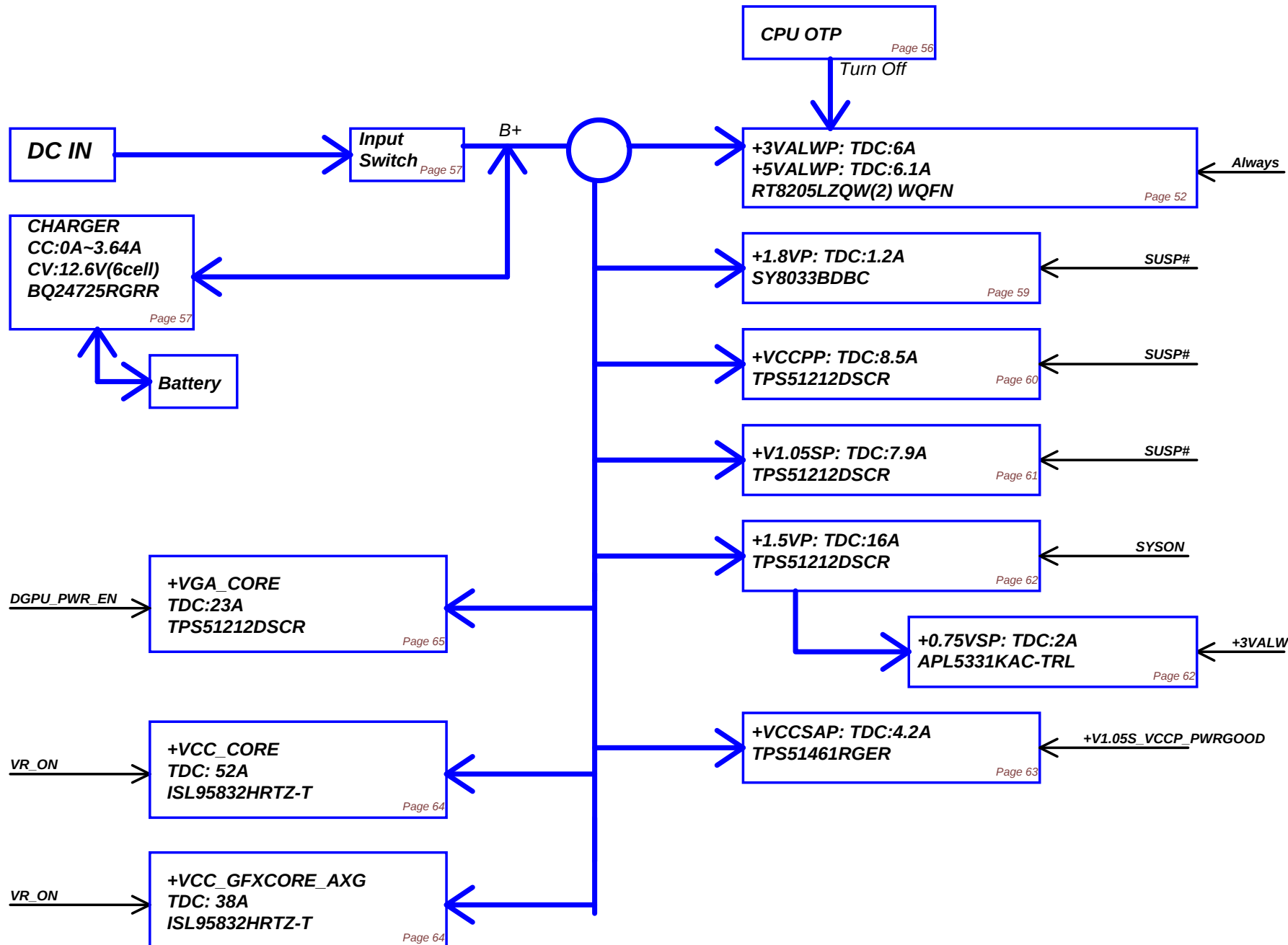


Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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				Date	Thursday, October 27, 2011
				Sheet	53 of 59
				Rev	0.2



Power block

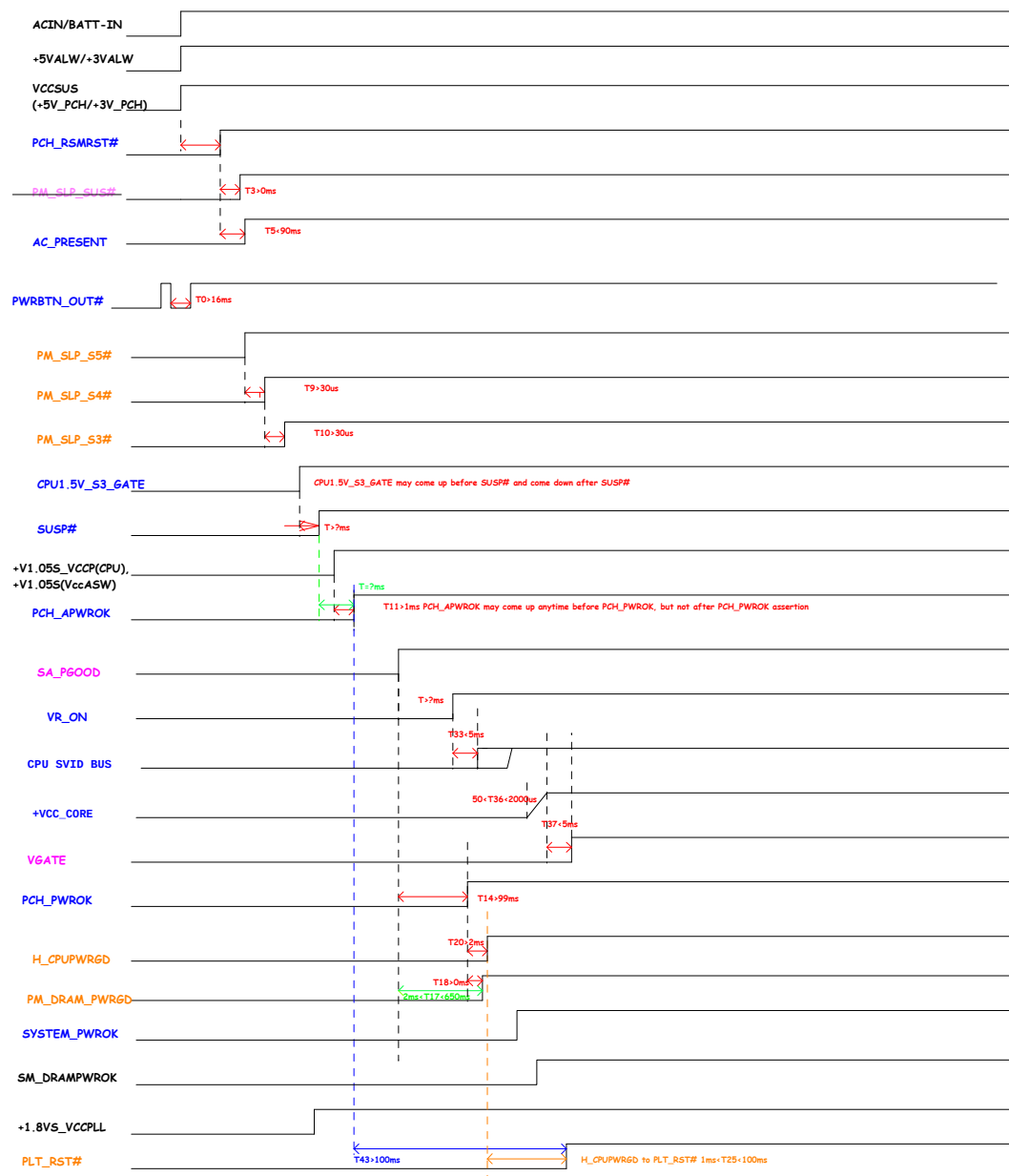


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				Customer	0.2
				Date	Thursday, October 27, 2011
				Sheet	55 of 59

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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							LA-8224P			0.2
				Date:			Thursday, October 27, 2011			Sheet 56 of 59

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by Intel® MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		For non AI co-lay	0.2	37	Add R745,R746 for non AI AI parts change to AI@	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13 40	Delete Q3. (connect pin S & D) Remove R135, R137 Del R552, R556	09/21	
ER04	Can't detect USB30 (JUSB2)	HW Design (PCB2)	0.2	36	Swap U90,39/40 to U90,36/37 net Change R1040 to 47K from 4.7K ohm Reserve R1029	09/21	
ER05		Design change for card reader	0.2	34	Add Q20, R773, R775 Reserve R768, R774 Change Net name at Card reader Conn	09/22	
ER06		HW Design (PURC demand)	0.2	29	Change to Q3(A03404L) from U22(A04430L)	09/21	
ER07		HW Design(PCB2)	0.2	36	Change R1049 to 330k Change Q904 to A03404L from AP2301GN Change R1046 to 1.5M	09/21	
ER08		HW Design (PURC demand)	0.2	42	Change Q33 to A03413L from AP2301GN	09/21	
ER09		Fine-tune GPU timing	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER10		HW Design (reserve)	0.2	18	Reserve R290	09/21	
ER11		HW Design(PCB2) for add VRAM DDR3 512MX8	0.2	25,26, 27,28	Add CMDA14 signal (U12-U19 pin J7)	09/28	
ER12		HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER13		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER14		HW Design (PURC demand)	0.2	15	Del R229,R230 (10K) Add R776-R783 (10K) Del R237,R239,R242 (8.2K) Add R784-R793 (8.2K)	09/30	
ER15		HW Design (PURC demand)	0.2	29,31 37,38 10,11	Change P/N C387, C389, C399, C436, C447, C602 Change P/N C389, C515, C518, C526, (0402) Change P/N C99, C100, C110, C120, C140, C141. (0402)	10/03	
ER16		HW Design(XTAL fine-tune)	0.2	42,12 13,32 20,36	Change R607 to 10 ohm Change Y3, C900, C901. Change Y1, C144, C145 Change Y4, C469, C473. Change Y2, C163, C164 Change Y9	10/07	
ER17		HW Design for instant on function	0.2	13 5	Reserve R750 R576 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER18		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38,P40)	10/07	
ER19		HW Design (PURC demand)	0.2		Change P/N Q7, U20, U21. Change P/N Q14-Q19, Q25, Q27-Q29, Q32, Q34-Q37, Q40-Q43, Q46-Q51, Q55-Q57, Q60, Q61, Q902, Q903, Q905. Change P/N Q23	10/14	
ER20		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER21		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER22		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	

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					EE-PIR-1		
					Size	Document Number	Rev
					Custom	LA-8224P	0.2
					Date: Thursday, October 27, 2011		
					Sheet 58 of 59		

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER23		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R289 , Add C149 0.1uf Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER24		Modify H2 size	0.2	38	Modify H2 size	10/17	
ER25		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER26		Reserve for Deep Sx	0.2	14,16 40	Add unstuff R800, R801, R802, R803, R804, R805 Add PCH_DPWR0K, DS_WAKE#, SUSACK#, SUSWARN#	10/19	
ER27		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER28		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER29		RF request	0.2	36	Reserve R1082 , C1045	10/19	
ER30		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER31		PRUC request	0.2	38 39	Change SW3, SW4, SW5 P/N	10/20	
ER32		PRUC request	0.2	39	Change U36 P/N	10/20	
ER33		For EMI request (without MS_CLK)	0.2	34	Remove R637, C611, R631, C620.	10/20	
ER34		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER35		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER36		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER37		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641-C648	10/20	
ER38		For ESD request	0.2	37,35 30,39	Change D27, D29, D24, D25. Change D6, D7, D9, D10, D33, D34.	10/20	
ER39		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 -ZZZ12 for N13P-GS & N13M-GE1 x8) & P/N	10/25	
ER40		update Power circuit	0.2	43-56	update Power circuit. (PC211)	10/26	
ER41		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	
ER42		Add test point for DFT	0.2	20	Add GPU_JTAG_TCK, GPU_JTAG_TDI, GPU_JTAG_TDO, GPU_JTAG_TMS	10/27	
ER43		For ASM1042 OC# pull-up	0.2	37	Reserve R1023, R1024 un-stuff	10/27 b	

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