1.5A

CPU_VLDT

U0301A

HT LINK

VLDT_A2 D1
VLDT_A3 D2
VLDT_A1 D3
VLDT_A4 D4

VLDT_B1 AE2
VLDT_B2 AE3
VLDT_B3 AE4
VLDT_B4 AE5

HT_CPU_RXD0	E3	L0_CADIN_H[0]	L0_CADOUT_H[0]
HT_CPU_RXD#0	E2	L0_CADIN_L[0]	L0_CADOUT_L[0]
HT_CPU_RXD1	E1	L0_CADIN_H[1]	L0_CADOUT_H[1]
HT_CPU_RXD#1	F1	L0_CADIN_L[1]	L0_CADOUT_L[1]
HT_CPU_RXD2	G3	L0_CADIN_H[2]	L0_CADOUT_H[2]
HT_CPU_RXD#2	G2	L0_CADIN_L[2]	L0_CADOUT_L[2]
HT_CPU_RXD3	G1	L0_CADIN_H[3]	L0_CADOUT_H[3]
HT_CPU_RXD#3	H1	L0_CADIN_L[3]	L0_CADOUT_L[3]
HT_CPU_RXD4	J1	L0_CADIN_H[4]	L0_CADOUT_H[4]
HT_CPU_RXD#4	K1	L0_CADIN_L[4]	L0_CADOUT_L[4]
HT_CPU_RXD5	L3	L0_CADIN_H[5]	L0_CADOUT_H[5]
HT_CPU_RXD#5	L2	L0_CADIN_L[5]	L0_CADOUT_L[5]
HT_CPU_RXD6	L1	L0_CADIN_H[6]	L0_CADOUT_H[6]
HT_CPU_RXD#6	M1	L0_CADIN_L[6]	L0_CADOUT_L[6]
HT_CPU_RXD7	N3	L0_CADIN_H[7]	L0_CADOUT_H[7]
HT_CPU_RXD#7	N2	L0_CADIN_L[7]	L0_CADOUT_L[7]
HT_CPU_RXD8	E5	L0_CADIN_H[8]	L0_CADOUT_H[8]
HT_CPU_RXD#8	F5	L0_CADIN_L[8]	L0_CADOUT_L[8]
HT_CPU_RXD9	F3	L0_CADIN_H[9]	L0_CADOUT_H[9]
HT_CPU_RXD#9	F4	L0_CADIN_L[9]	L0_CADOUT_L[9]
HT_CPU_RXD10	G5	L0_CADIN_H[10]	L0_CADOUT_H[10]
HT_CPU_RXD#10	H5	L0_CADIN_L[10]	L0_CADOUT_L[10]
HT_CPU_RXD11	H3	L0_CADIN_H[11]	L0_CADOUT_H[11]
HT_CPU_RXD#11	H4	L0_CADIN_L[11]	L0_CADOUT_L[11]
HT_CPU_RXD12	K3	L0_CADIN_H[12]	L0_CADOUT_H[12]
HT_CPU_RXD#12	K4	L0_CADIN_L[12]	L0_CADOUT_L[12]
HT_CPU_RXD13	L5	L0_CADIN_H[13]	L0_CADOUT_H[13]
HT_CPU_RXD#13	M5	L0_CADIN_L[13]	L0_CADOUT_L[13]
HT_CPU_RXD14	M3	L0_CADIN_H[14]	L0_CADOUT_H[14]
HT_CPU_RXD#14	M4	L0_CADIN_L[14]	L0_CADOUT_L[14]
HT_CPU_RXD15	N5	L0_CADIN_H[15]	L0_CADOUT_H[15]
HT_CPU_RXD#15	P5	L0_CADIN_L[15]	L0_CADOUT_L[15]

CPU_VLDT

AD1	HT_CPU_TXD0	
AC1	HT_CPU_TXD#0	
AC2	HT_CPU_TXD1	
AC3	HT_CPU_TXD#1	
AB1	HT_CPU_TXD2	
AA1	HT_CPU_TXD#2	
AA2	HT_CPU_TXD3	
AA3	HT_CPU_TXD#3	
W2	HT_CPU_TXD4	
W3	HT_CPU_TXD#4	
V1	HT_CPU_TXD5	
U1	HT_CPU_TXD#5	
U2	HT_CPU_TXD6	
U3	HT_CPU_TXD#6	
T1	HT_CPU_TXD7	
R1	HT_CPU_TXD#7	
AD4	HT_CPU_TXD8	
AD3	HT_CPU_TXD#8	
AD5	HT_CPU_TXD9	
AC5	HT_CPU_TXD#9	
AB4	HT_CPU_TXD10	
AB3	HT_CPU_TXD#10	
AB5	HT_CPU_TXD11	
AA5	HT_CPU_TXD#11	
Y5	HT_CPU_TXD12	
W5	HT_CPU_TXD#12	
V4	HT_CPU_TXD13	
V3	HT_CPU_TXD#13	
V5	HT_CPU_TXD14	
U5	HT_CPU_TXD#14	
T4	HT_CPU_TXD15	
T3	HT_CPU_TXD#15	

10 HT_CPU_RXD[0..15]
10 HT_CPU_RXD#[0..15]

HT_CPU_TXD[0..15] 10
HT_CPU_TXD#[0..15] 10

10 HT_CPU_RX_CLK0	HT_CPU_RX_CLK0	J3	L0_CLKIN_H[0]
10 HT_CPU_RX_CLK#0	HT_CPU_RX_CLK#0	J2	L0_CLKIN_L[0]
10 HT_CPU_RX_CLK1	HT_CPU_RX_CLK1	J5	L0_CLKIN_H[1]
10 HT_CPU_RX_CLK#1	HT_CPU_RX_CLK#1	K5	L0_CLKIN_L[1]
10 HT_CPU_RX_CTL0	HT_CPU_RX_CTL0	N1	L0_CTLIN_H[0]
10 HT_CPU_RX_CTL#0	HT_CPU_RX_CTL#0	P1	L0_CTLIN_L[0]
10 HT_CPU_RX_CTL1	HT_CPU_RX_CTL1	P3	L0_CTLIN_H[1]
10 HT_CPU_RX_CTL#1	HT_CPU_RX_CTL#1	P4	L0_CTLIN_L[1]

L0_CLKOUT_H[0]	Y1	HT_CPU_TX_CLK0	HT_CPU_TX_CLK0 10
L0_CLKOUT_L[0]	W1	HT_CPU_TX_CLK#0	HT_CPU_TX_CLK#0 10
L0_CLKOUT_H[1]	Y4	HT_CPU_TX_CLK1	HT_CPU_TX_CLK1 10
L0_CLKOUT_L[1]	Y3	HT_CPU_TX_CLK#1	HT_CPU_TX_CLK#1 10
L0_CTLOUT_H[0]	R2	HT_CPU_TX_CTL0	HT_CPU_TX_CTL0 10
L0_CTLOUT_L[0]	R3	HT_CPU_TX_CTL#0	HT_CPU_TX_CTL#0 10
L0_CTLOUT_H[1]	T5	HT_CPU_TX_CTL1	HT_CPU_TX_CTL1 10
L0_CTLOUT_L[1]	R5	HT_CPU_TX_CTL#1	HT_CPU_TX_CTL#1 10

SOCKET638

Change P/N to 12G011306380

071113

Do not cross plane.

+1.1VS

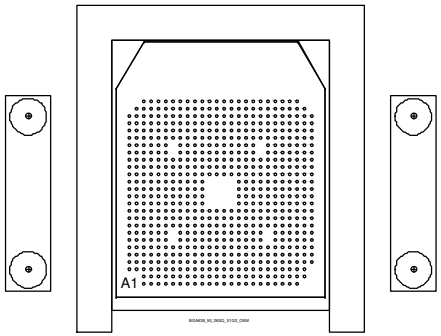
1MM_OPEN_5MIL
JP301

CPU_VLDT

C0302 c0805_h37 10UF/6.3V
C0303 c0805_h37 10UF/6.3V
C0304 10UF/6.3V
C0305 0.1UF/16V
C0306 0.1UF/16V
C0308 180PF/50V
C0307 180PF/50V

GND GND

Place close to socket



* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

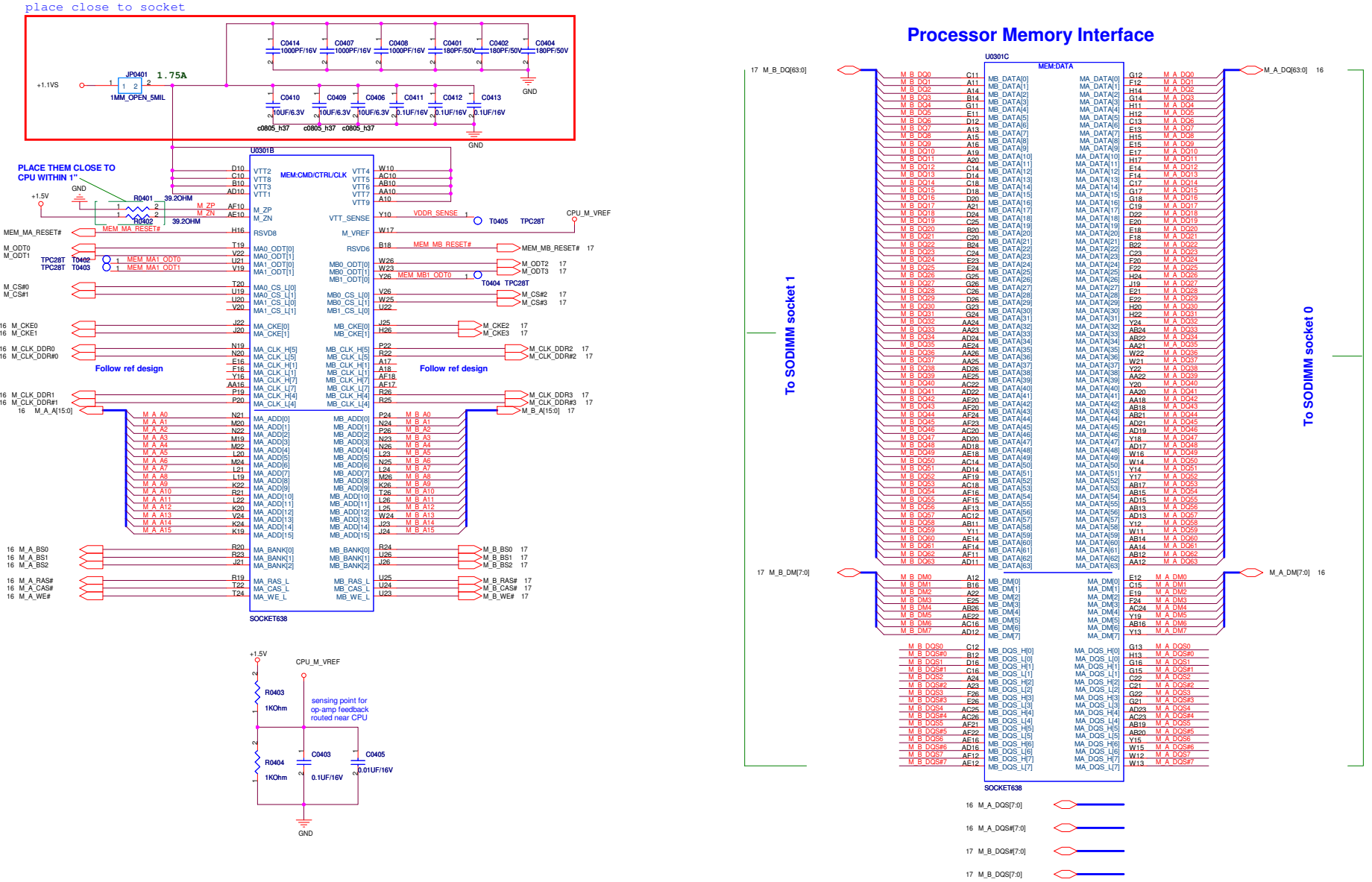
ASUSTeK COMPUTER INC. NB1

Title : Griffin HT I/F

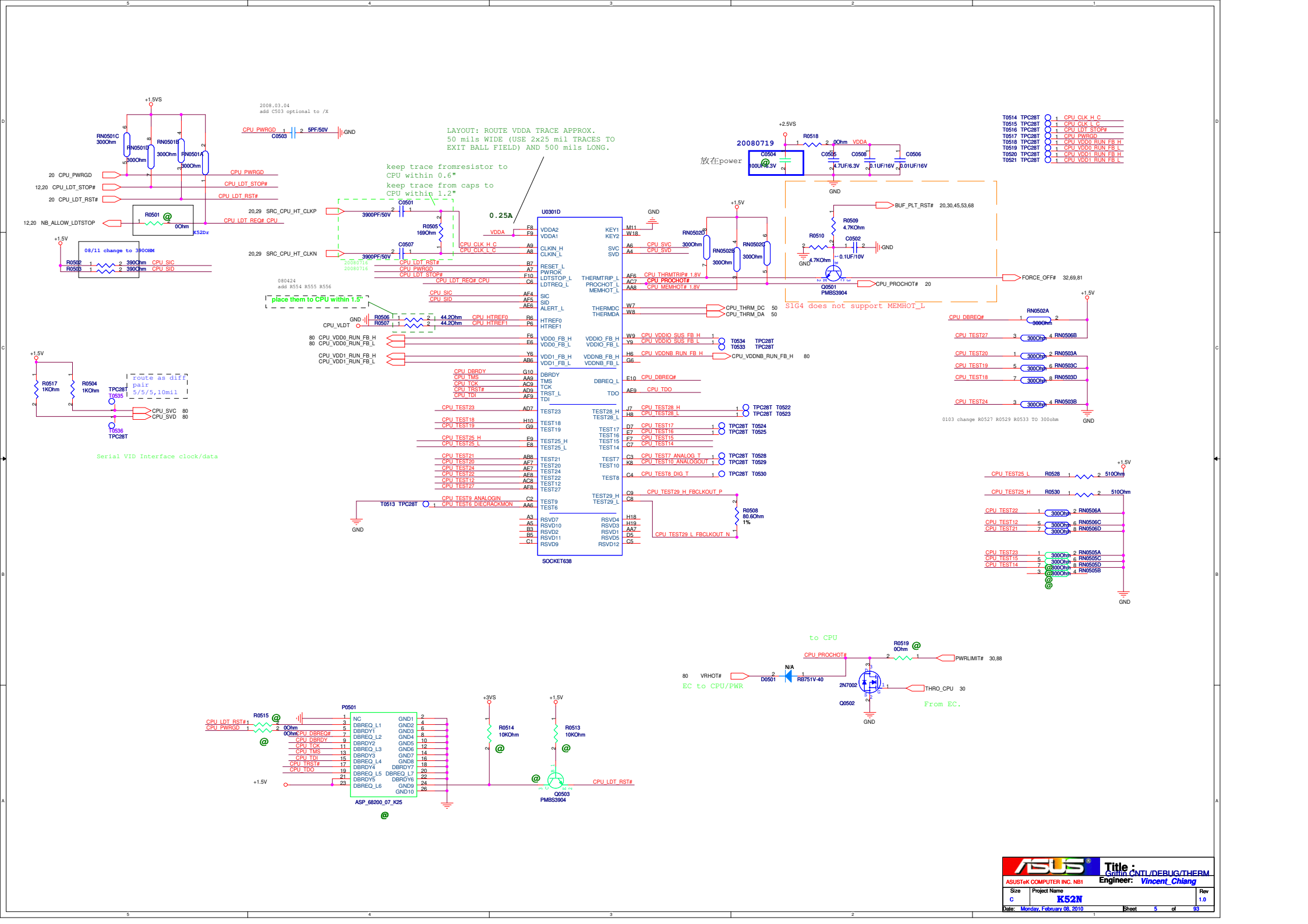
Engineer: Vincent_Chiang

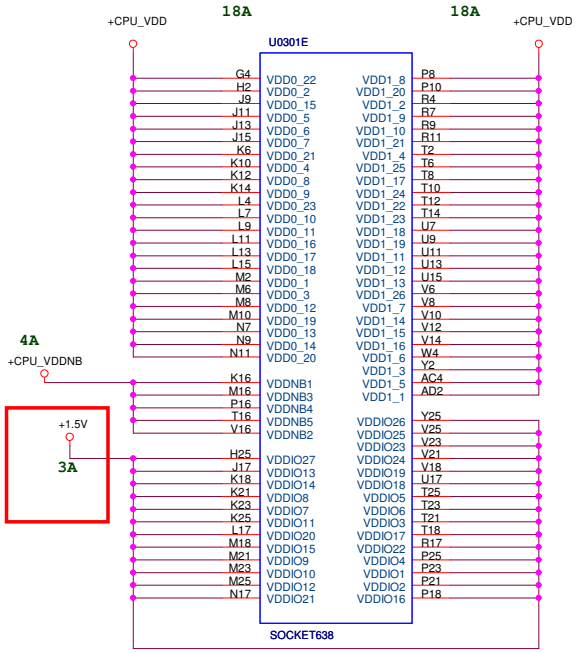
Size	Project Name	Rev
B	K52N	1.0

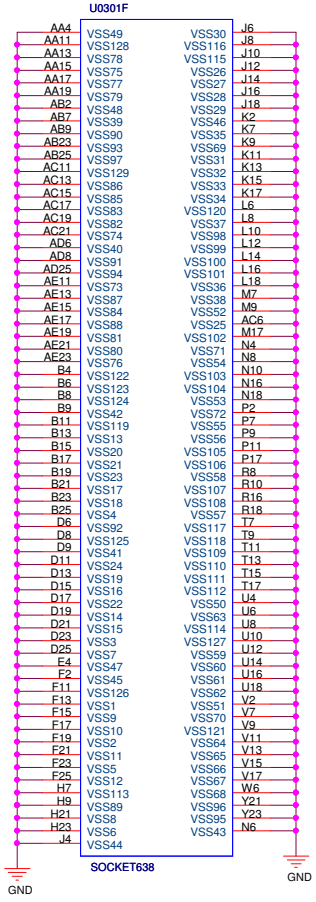
Date: Monday, February 08, 2010 Sheet 3 of 93



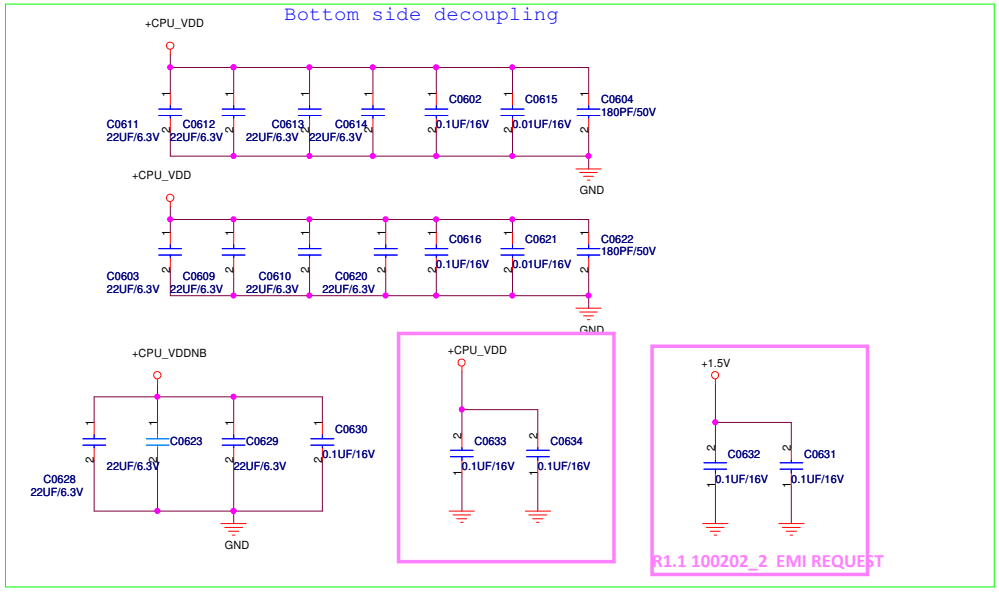
ASUSTeK COMPUTER INC. NB1	Title: Merlin DDR2 MEMORY I/F		
	Engineer: Vincent_Chiang		
Size: C	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 4 of 93		

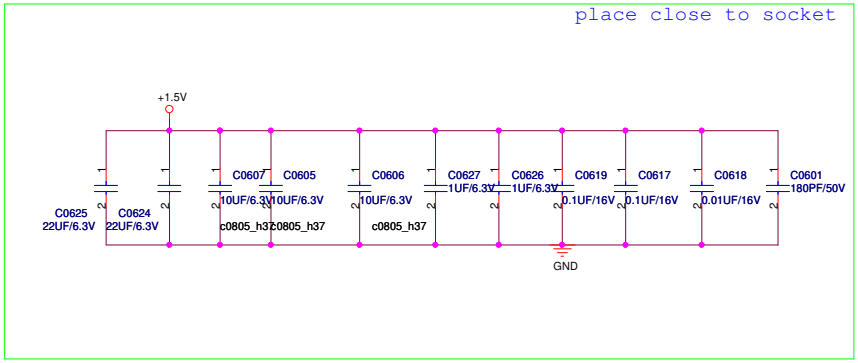

LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
0.25A
place them to CPU within 1.5"
route as diff
pair
5/5/5,10mil
Serial VID Interface clock/data
08/11 change to 390OHM
2008.03.04
add C503 optional to /X
080424
add R554 R555 R556
20080719
放在power
U0301D
SOCKET638
S1G4 does not support MEMHOT_L
0103 change R0527 R0529 R0533 TO 300ohm
to CPU
EC to CPU/PWR
From EC.
P0501
ASP_68200_07_K25
Title : Griffin CNTL/DEBUG/THERM
Engineer: Vincent_Chiang
ASUSTeK COMPUTER INC. NB1
Size C
Project Name K52N
Rev 1.0
Date: Monday, February 08, 2010
Sheet 5 of 93



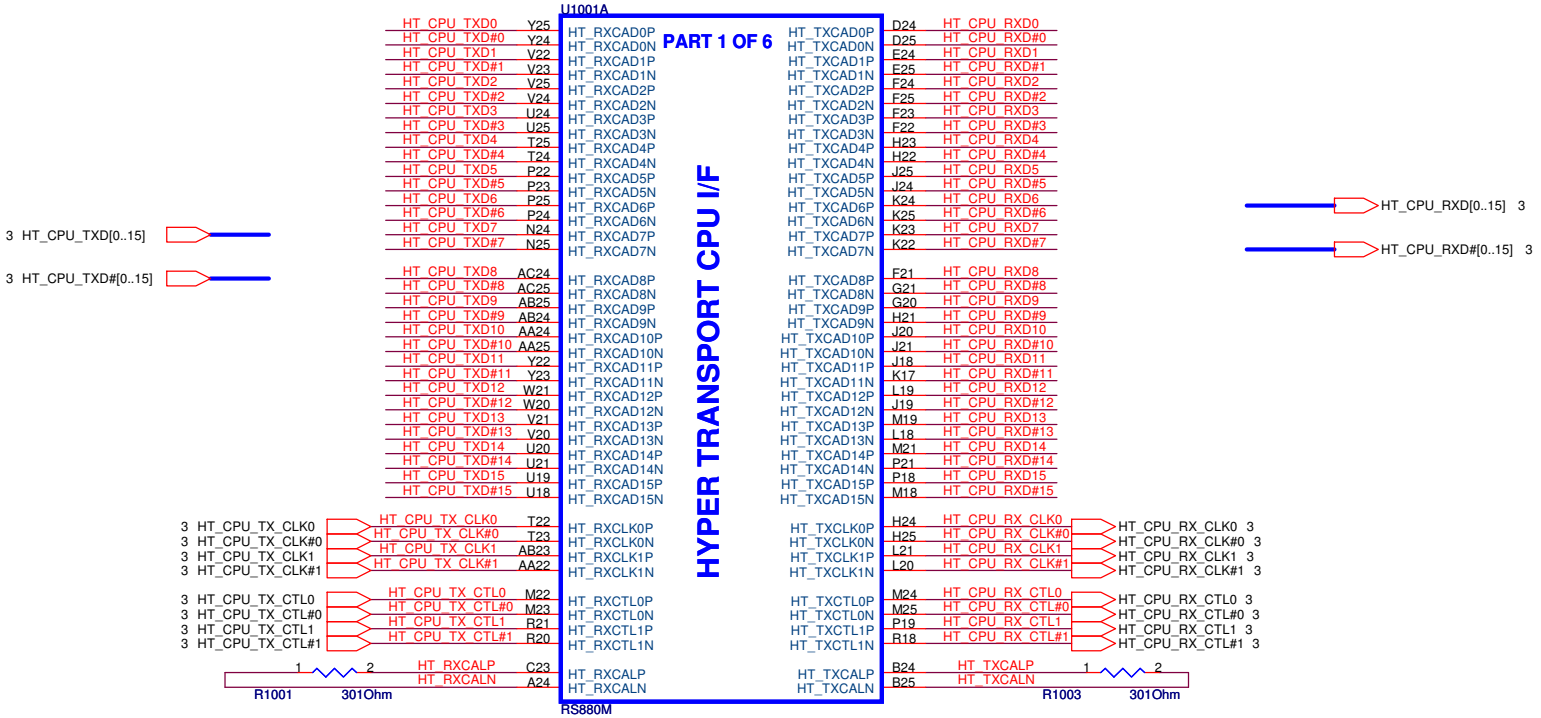


Decoupling between Processor and DIMMs, Place close to Porcessor as possible

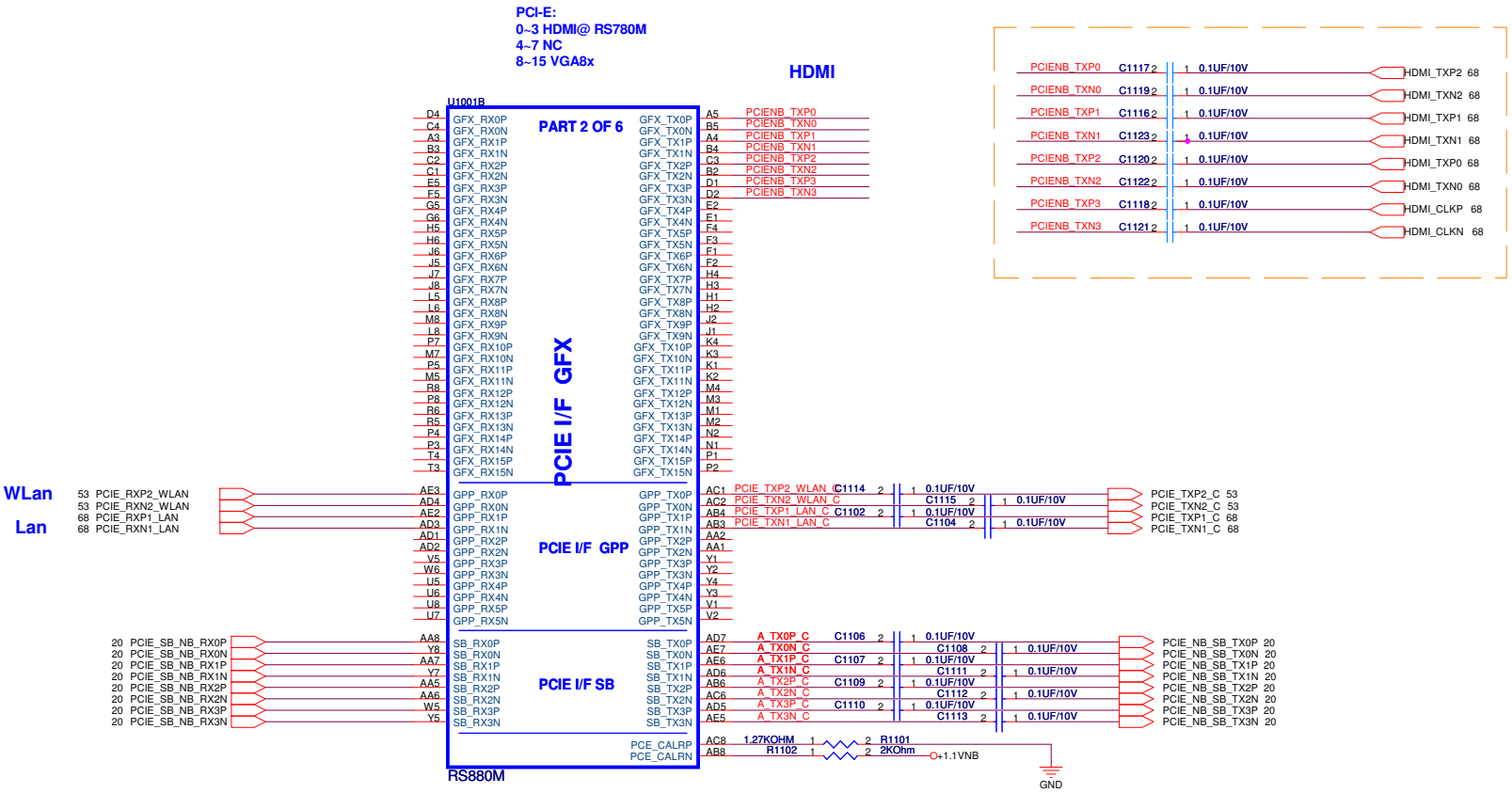




ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 6 of 93	



ASUSTeK COMPUTER INC. NB1	Title : RS880M-HT LINK I/F	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 10 of 93	



Title :	RS880M-PCIE LINK I/F
ASUSTeK COMPUTER INC. NB1	Engineer: Vincent_Chiang
Size: Custom	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 11 of 93

NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

RS780 POWERGOOD is 1.8VS rail

Single channel

U1001C — RS880M — PART 3 OF 6

CRT/TVOUT: AVDD1, AVDD2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, RESERVED1–4, RED, RED#, GREEN, GREEN#, BLUE, BLUE#, DAC_HSYNC, DAC_VSYNC, DAC_SDA, DAC_SCL, DAC_RSET

PLL PWR: PLLVDD, PLLVDD18, PLLVSS, VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

PM: SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP

CLOCKs: HT_REFCLKP, HT_REFCLKN, REFCLK_P, REFCLK_N, GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP, GPPSB_REFCLKN

MIS.: I2C_DATA, I2C_CLK, DDC_DATA0/AUX0N, DDC_CLK0/AUX0P, DDC_CLK1/AUX1P, DDC_DATA1/AUX1N, STRP_DATA, AUX_CAL

LVTM: TXOUT_L0P/N, TXOUT_L1P/N, TXOUT_L2P/N, TXCLK_LP/LN, TXCLK_UP/UN, TXOUT_U0P/N, TXOUT_U1P/N, TXOUT_U2P/N, TXOUT_U3P/N, VDDLTP18, VSSLTP18, VDDLT18_1, VDDLT18_2, VDDLT33_1, VDDLT33_2, VSSLT1–7, LVDS_DIGON, LVDS_BLON, LVDS_ENA_BL, TMDS_HPD, HPD, SUS_STAT#, THERMALDIODE_P/N, TESTMODE

L1201 120Ohm/100Mhz 0603 Irat=600mA — AVDD1 — 110mA,RX881 GND
C1201 2.2UF/10V

+1.8VS r0603_h24 — R1202 0Ohm — AVDDDI — 20mA,RX881 GND
C1205 0.1UF/10V, C1206 0.1UF/10V

L1202 120Ohm/100Mhz 0603 Irat=600mA — AVDDQ_L — 4mA,RX881 GND
C1207 2.2UF/10V

L1206 220Ohm/100Mhz — +1.1VNB — 65mA,RX881 GND
C1208 2.2UF/10V

L1203 120Ohm/100Mhz 0603 Irat=600mA — PLLVDD18
C1204 2.2UF/10V

L1204 120Ohm/100Mhz 0603 Irat=600mA — VDDA18HTPLL — 20mA,RX881 GND
C1203 2.2UF/10V

L1205 120Ohm/100Mhz 0603 Irat=600mA — VDDA18PCIEPLL — 120mA
C1210 2.2UF/10V

R1207 330Ohm — NB_PWRGD — NB_RST# — CPU_LDT_STOP#1V8 — NB_ALLOW_LDTSTOP

SHORT_PIN JP1201 — 68 RED_GPU — R1203 150Ohm 1% — RED
SHORT_PIN JP1202 — 68 GREEN_GPU — R1204 150Ohm 1% — GREEN
SHORT_PIN JP1203 — 68 BLUE_GPU — R1205 150Ohm 1% — BLUE

13,68 CRT_HSYNC
13,68 CRT_VSYNC
68 NB_DACSDA
68 NB_DACSCL

R1206 715Ohm

20,29 SRC_NB_HT_CLKP — NB_HT_REFCLKP
20,29 SRC_NB_HT_CLKN — NB_HT_REFCLKN
20,29 NB_REFCLK_P
20 NB_REFCLK_N — NB_REFCLK_N_C

RN1202A 4.7KOhm — SRC_NB_GFX_REFCLKP_C
RN1202B 4.7KOhm — SRC_NB_GFX_REFCLKN_C

+1.1VNB — RN1203A 4.7KOhm, RN1203B 4.7KOhm

20,29 NBLINK_RCLKP
20,29 NBLINK_RCLKN

45 EDID_R_DAT_GPU — EDID_DAT
45 EDID_R_CLK_GPU — EDID_CLK
68 HDMI_DDC_CLK

R1213 0Ohm, R1212 0Ohm

RN1201A 4.7KOhm, RN1201B 4.7KOhm — +3VS

R1.1 100127_1 Change EDID CLK/DAT Circuit

STRP_DATA	0	1
VCC_NB	.95V	1.1V

R1211 2KOhm @

net AUC_CAL Refence F50z

R1210 1.8KOHM

U1201 NC7SZ08P5X — +1.8VS — R1209 1KOhm @
5,20 CPU_LDT_STOP# — CPU_LDT_STOP#1V8

K52Dr

R1208 1KOhm — 5,20 NB_ALLOW_LDTSTOP

LVDS_L0P/N_GPU 45
LVDS_L1P/N_GPU 45
LVDS_L2P/N_GPU 45
LVDS_LCLKP/N_GPU 45

VDDLTP18_PLL_L — L1207 120Ohm/100Mhz 0603 Irat=600mA
VDDLTP18_L — L1208 120Ohm/100Mhz 0603 Irat=600mA

T1202 TPC28T, T1203 TPC28T
VDDLT33 for 740 only
C1211 0.1UF/10V, C1212 4.7UF/6.3V, C1209 2.2UF/10V

Check the VDDLT33 power connection

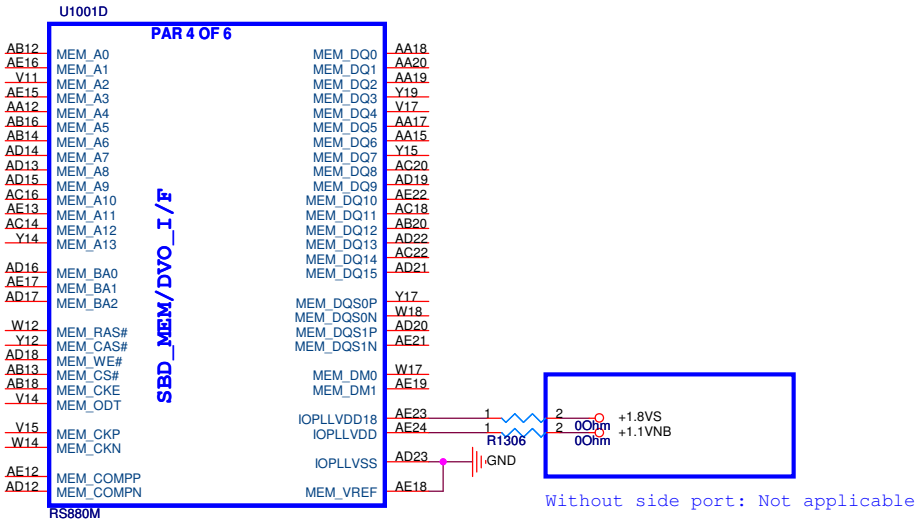
L_VDD_EN_GPU 45
NB_LCD_BL_PWM 45
L_BACKEN_GPU 45

PR — R1214 4.7KOhm

HDMI_HP — HDMI_HP 68
SUS_STAT# — SUS_STAT# 21

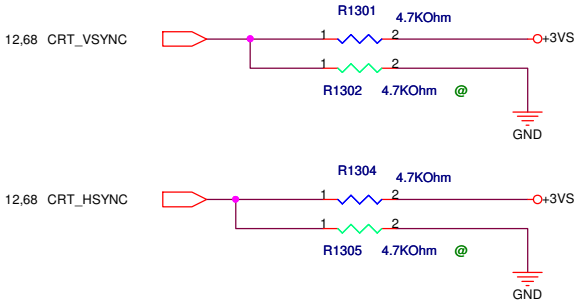
T1205 TPC28T, T1204 TPC28T

Title :	RS880M-SYSTEM I/F
ASUSTeK COMPUTER INC. NB1	Engineer: Vincent_Chiang
Size: Custom	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 12 of 93



Without side port: Not applicable

080118
Disable Side Port Memory
R1.1



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

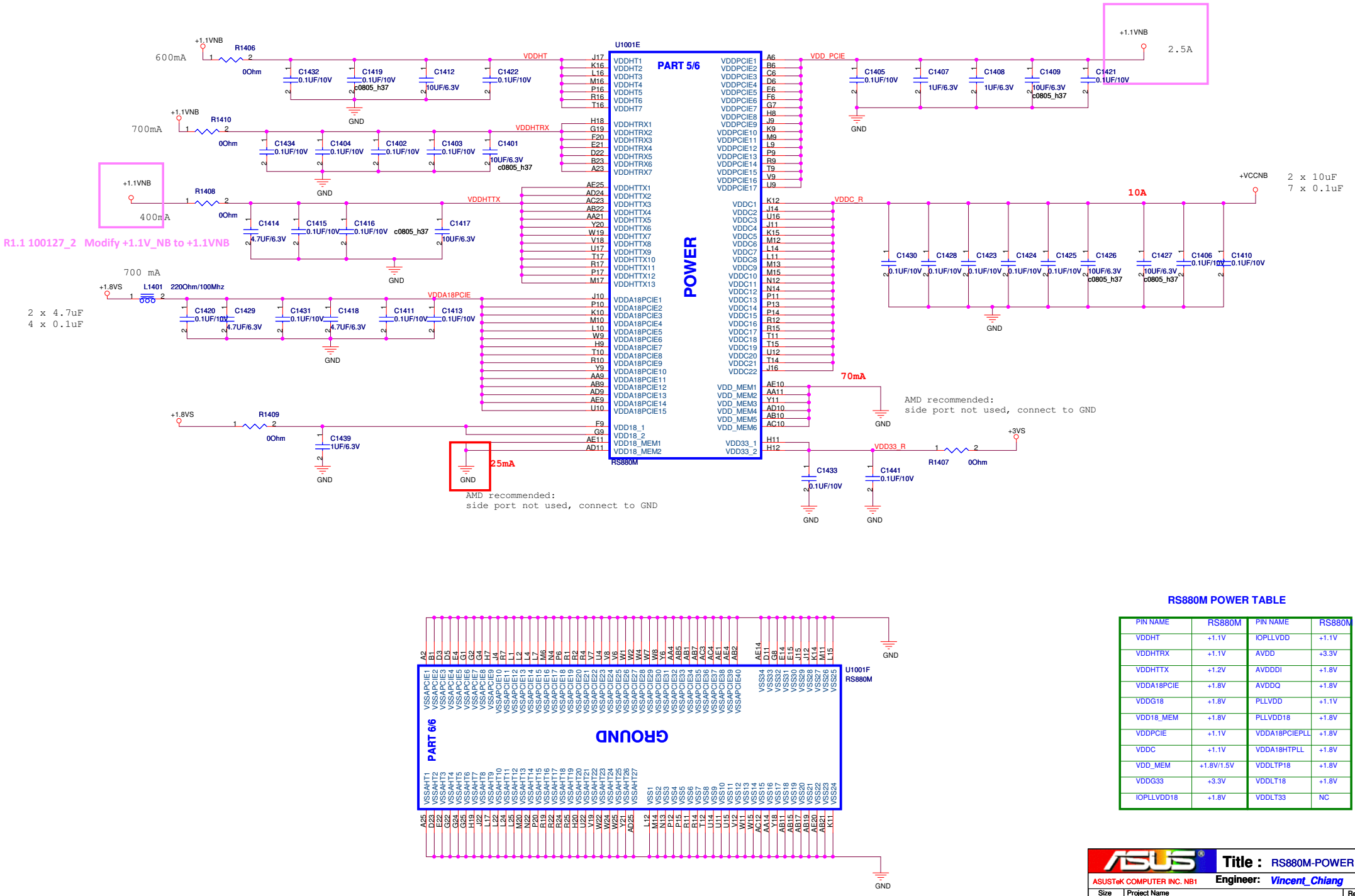
STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

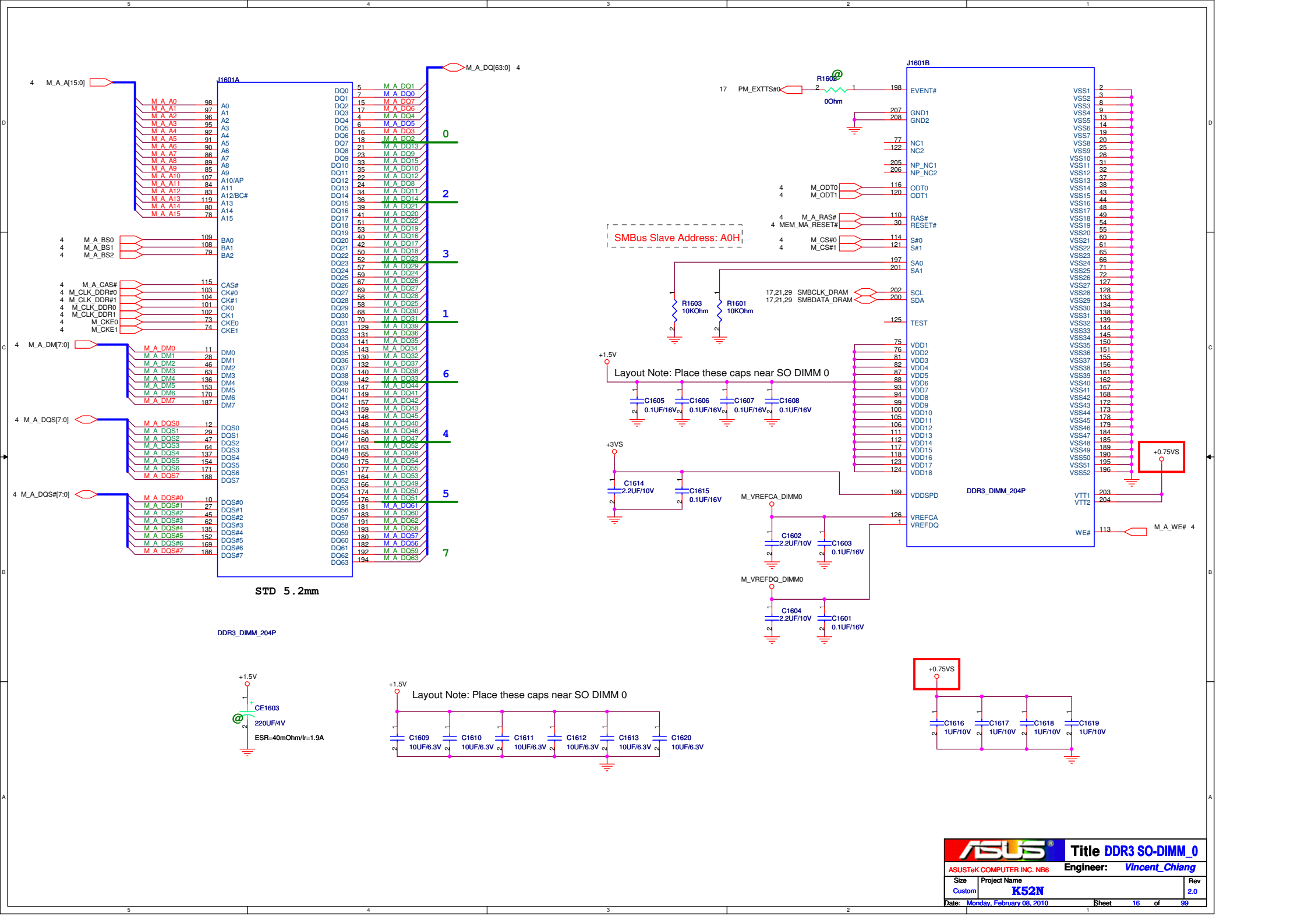
ASUSTeK COMPUTER INC. NB1	Title : RS880M-SPMEM/STRAPS	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 13 of 93	



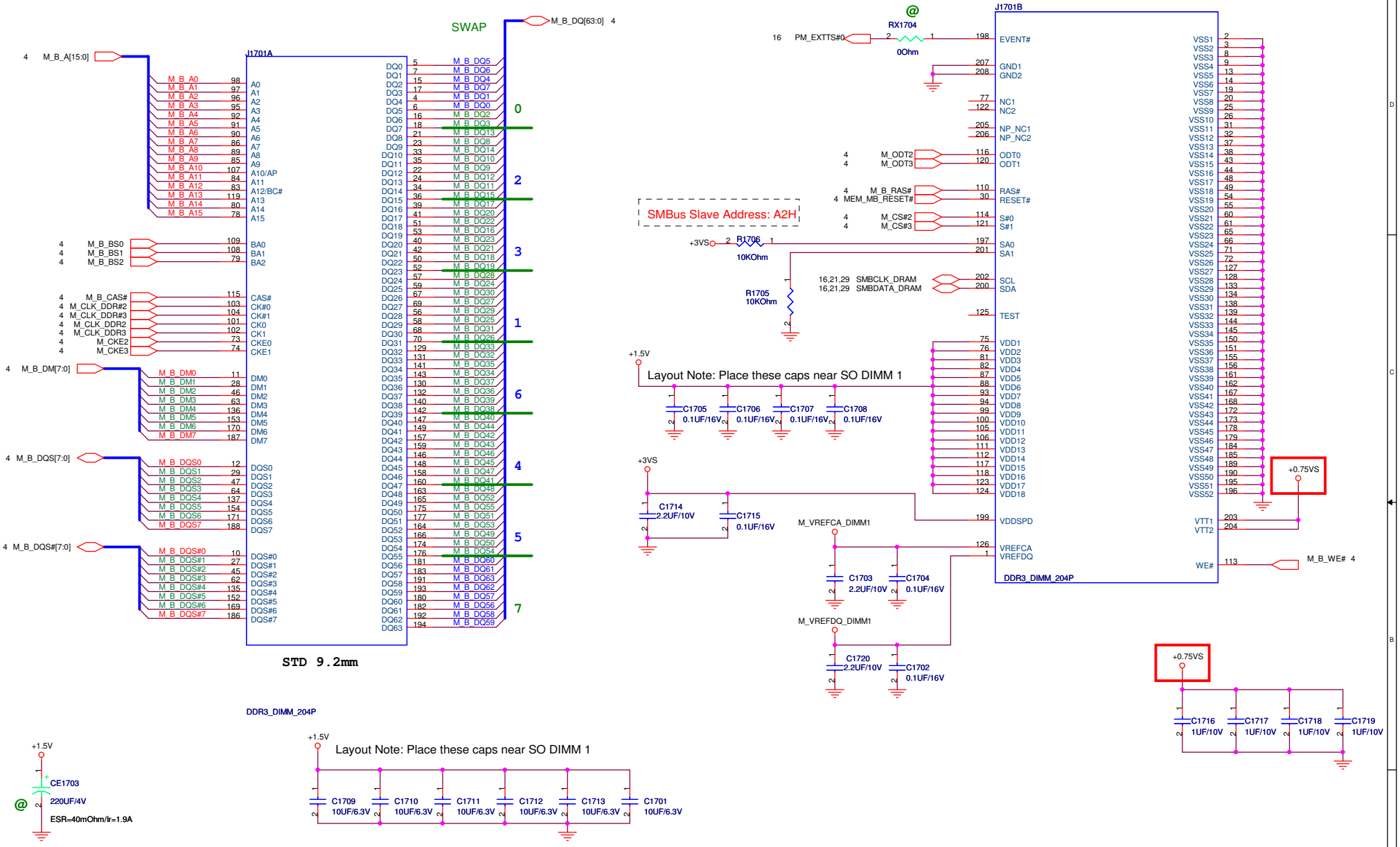
RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

ASUSTeK COMPUTER INC. NB1	Title : RS880M-POWER		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 14 of 93		



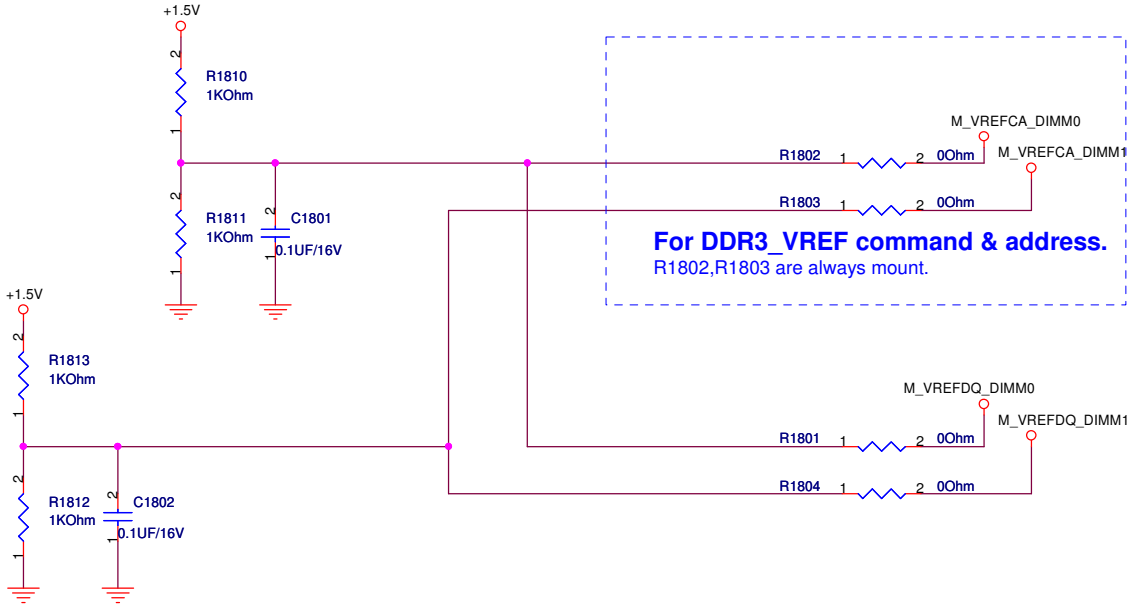
Title	DDR3 SO-DIMM_0	
ASUSTeK COMPUTER INC. NB6	Engineer:	Vincent_Chiang
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 16 of 99	



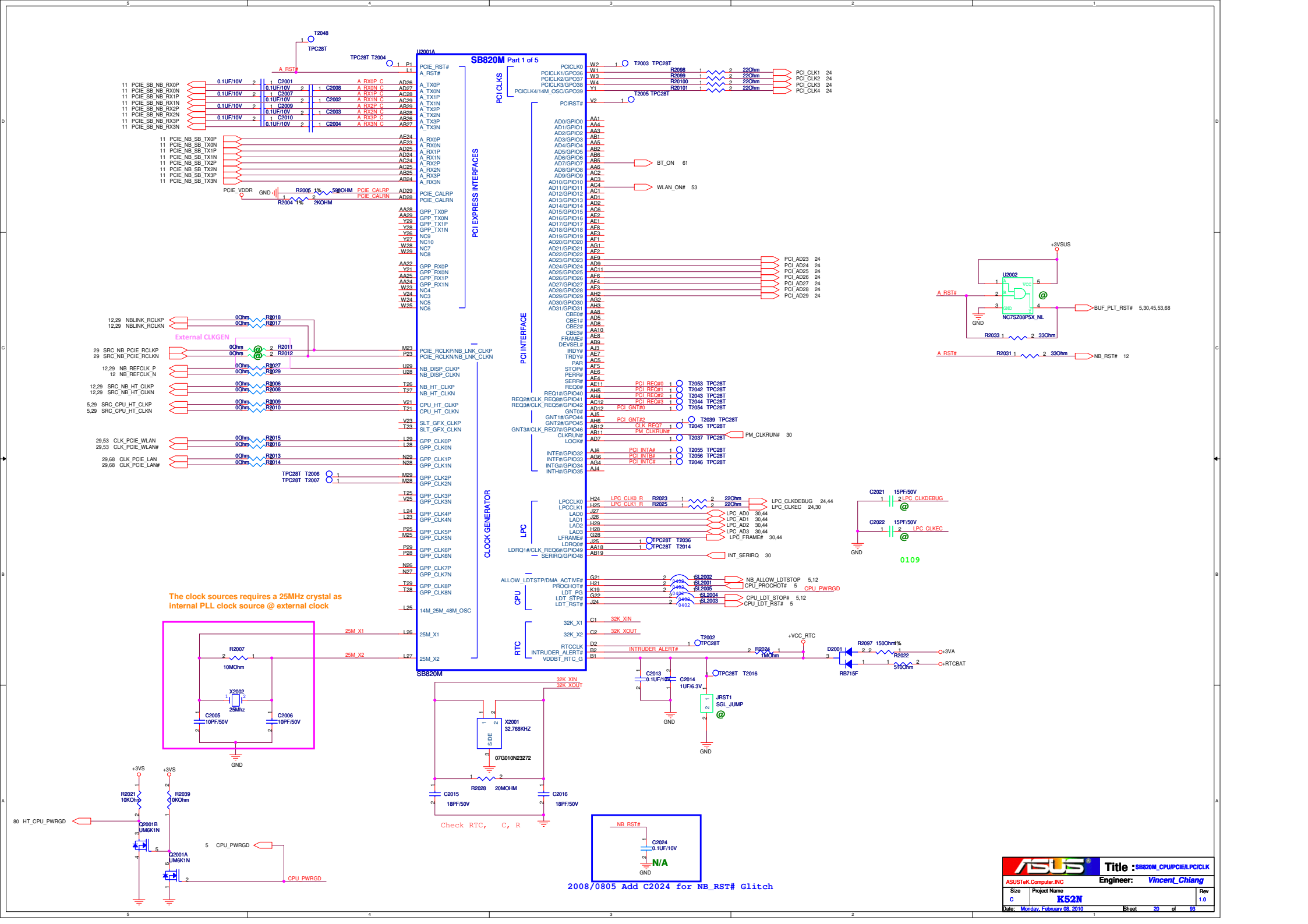
ASUSTeK COMPUTER INC. NB6	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 17 of 99	

Title DDR3 SO-DIMM_1

DDR3 Vref



ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 18 of 99	


SB820M Part 1 of 5
U2001A
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
PCI CLKS
LPC
CPU
RTC
SB820M
External CLKGEN
The clock sources requires a 25MHz crystal as internal PLL clock source @ external CLK
Check RTC, C, R
2008/0805 Add C2024 for NB_RST# Glitch
0109
Title : SB820M_CPU/PCIE/LPC/CLK
ASUSTeK.Computer.INC
Engineer: Vincent_Chiang
Project Name K52N
Size C
Rev 1.0
Date: Monday, February 08, 2010
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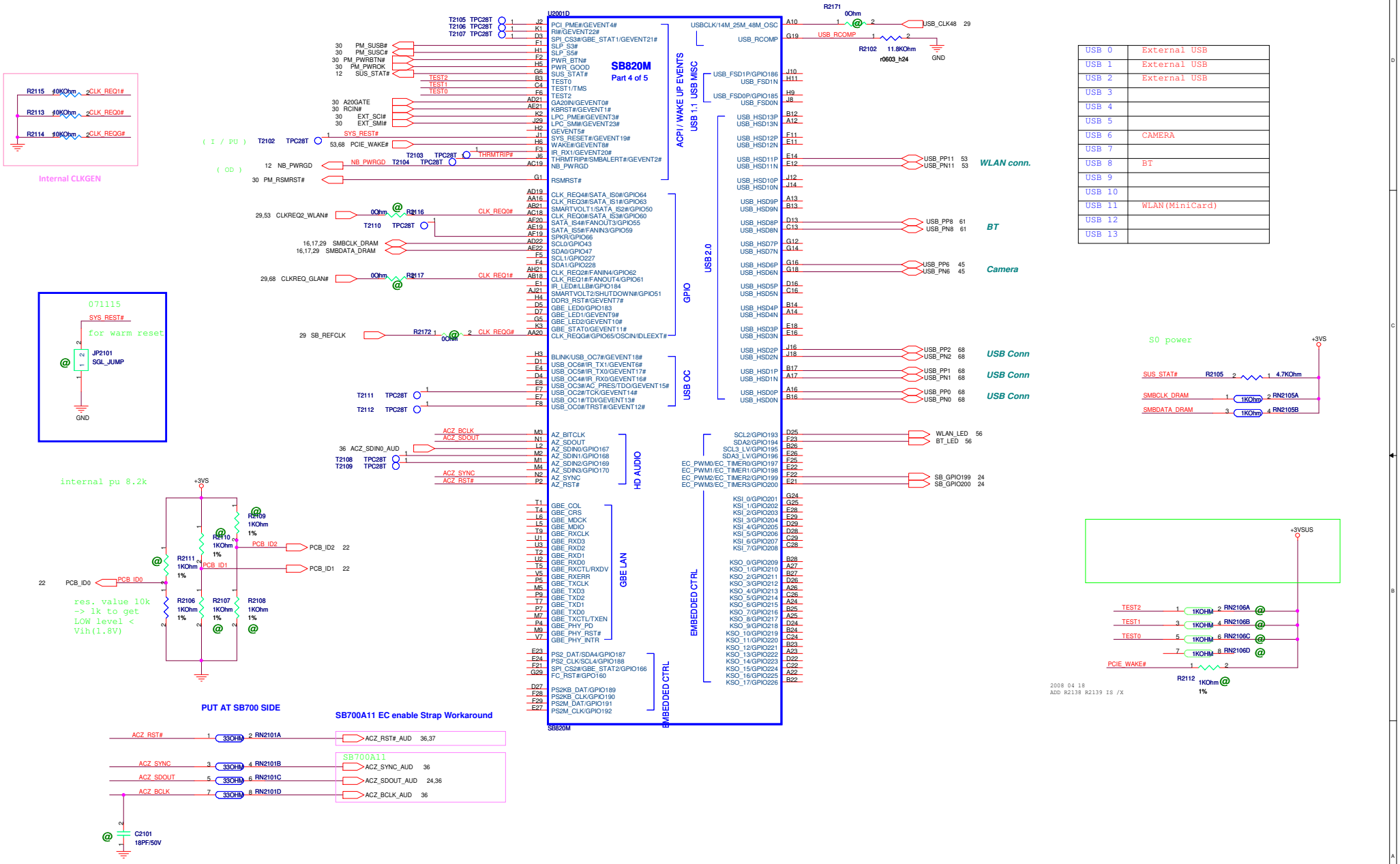


USB 0	External USB
USB 1	External USB
USB 2	External USB
USB 3	
USB 4	
USB 5	
USB 6	CAMERA
USB 7	
USB 8	BT
USB 9	
USB 10	
USB 11	WLAN(MiniCard)
USB 12	
USB 13	

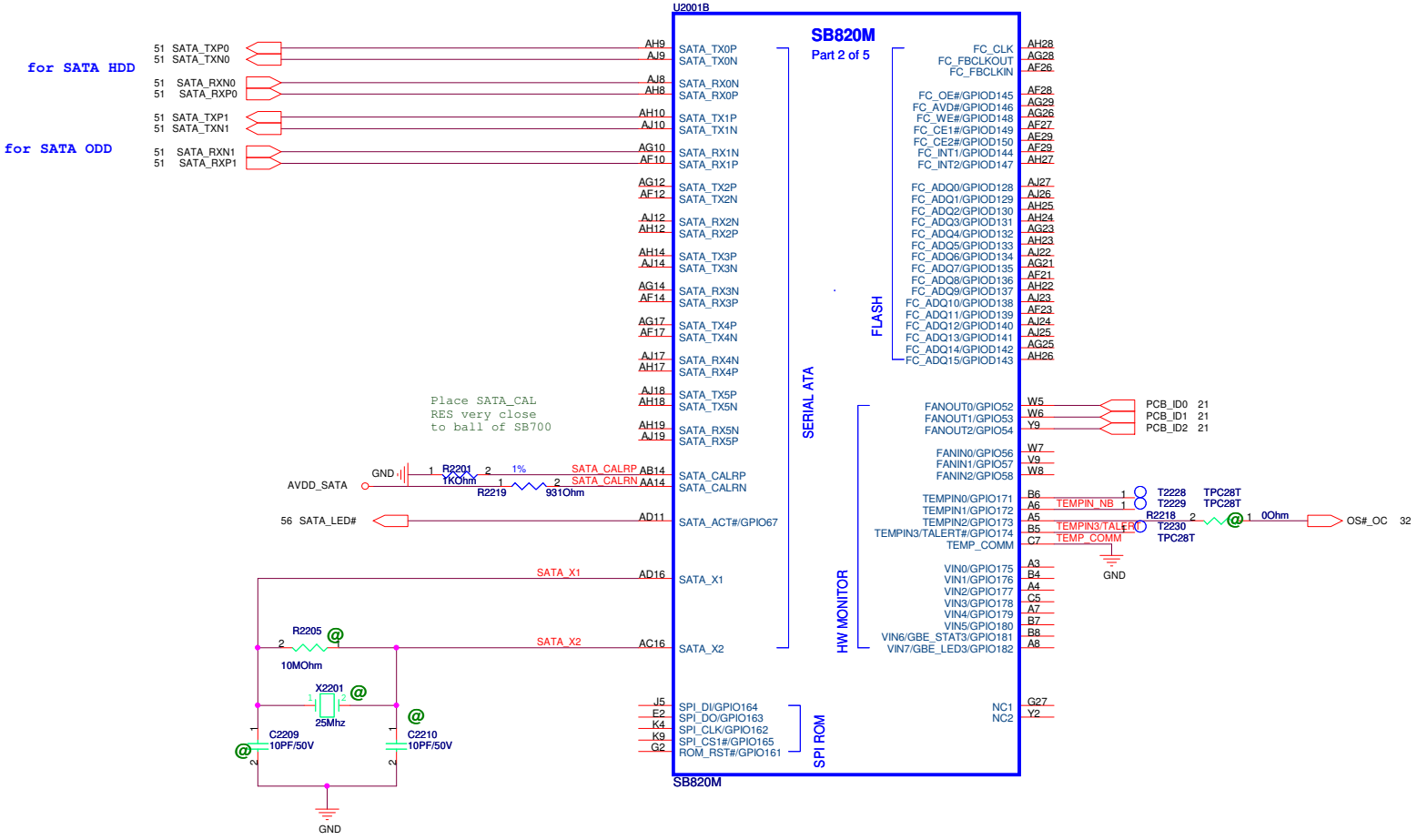
ASUSTeK.Computer.INC

Title : SB700_GPIO/USB/HD/ACPI

Engineer: Vincent_Chiang

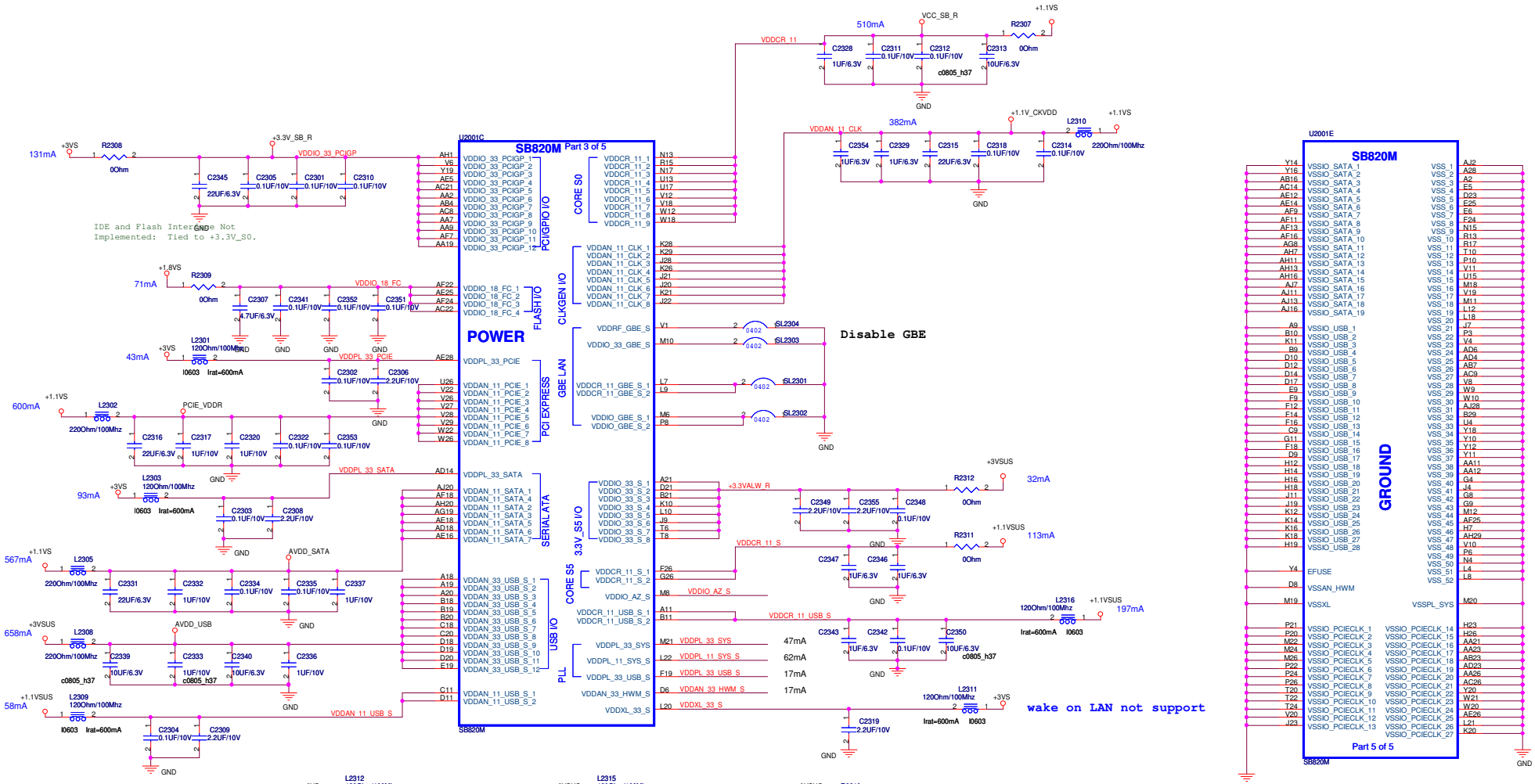
Size	Project Name	Rev
C	K52N	1.0

Date: Monday, February 08, 2010 Sheet 21 of 93

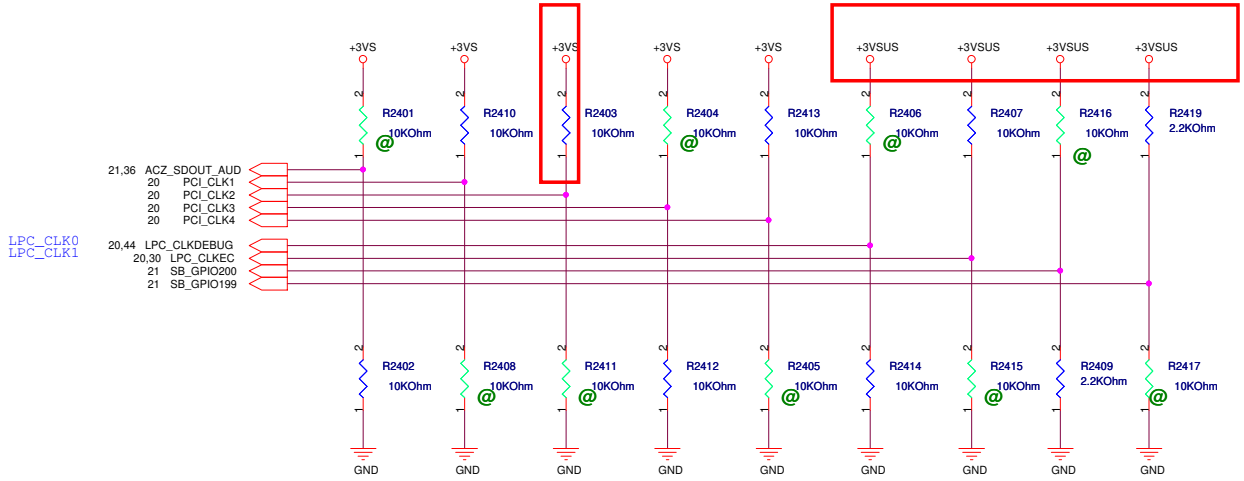


ASUSTeK.Computer.INC	Title : SB820M_PATA/SATA	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 22 of 93	

Check power Level and state

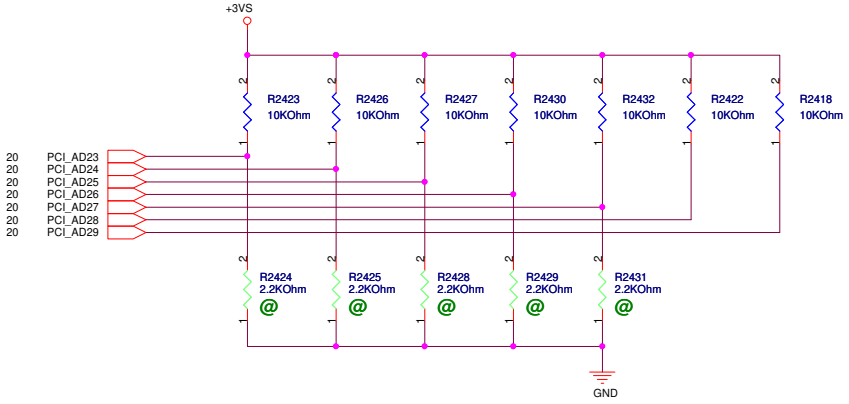


ASUSTeK.COMPUTER.INC	Title : SB820M_POWER		
	Engineer: Vincent_Chiang		
Size: C	Project Name: K52N	Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 23 of 93		



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled Modify	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

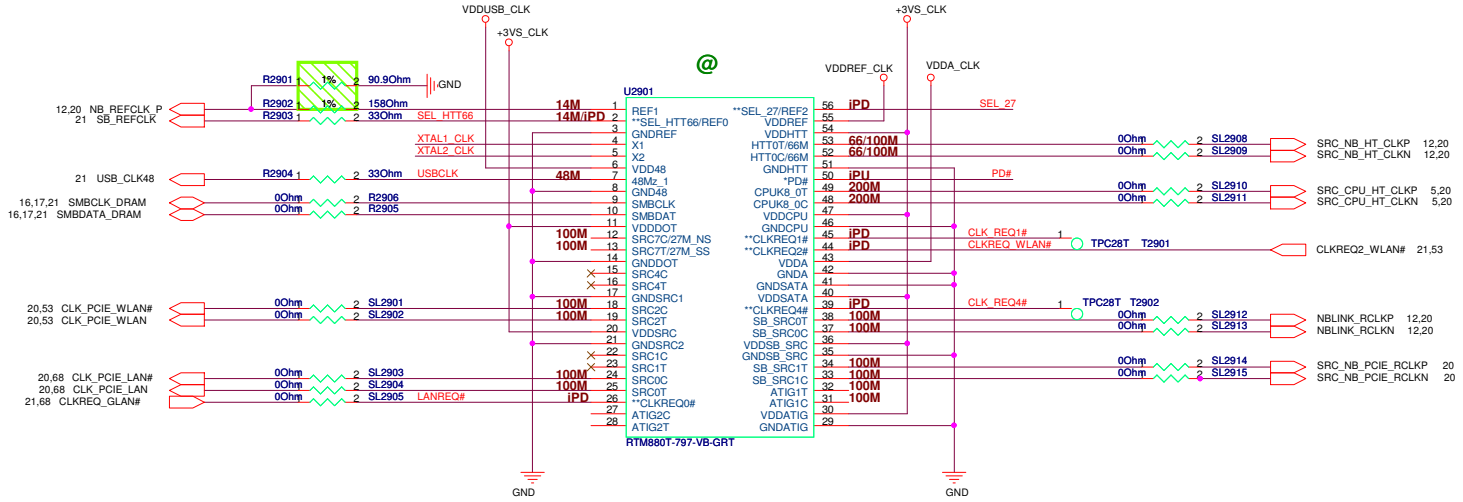
ASUSTeK.Computer.INC

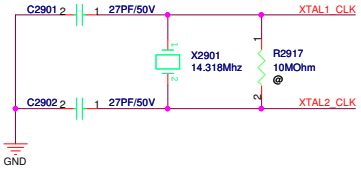
Title : SB820M_STRAP

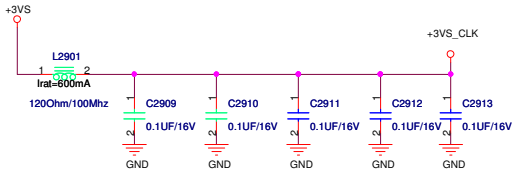
Engineer: Vincent_Chiang

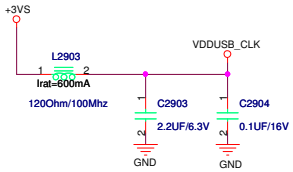
Size	Project Name	Rev
Custom	K52N	1.0

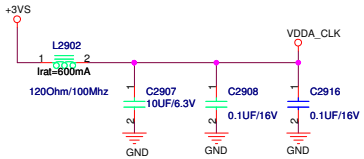
Date: Monday, February 08, 2010 Sheet 24 of 93

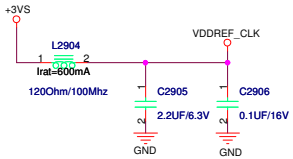


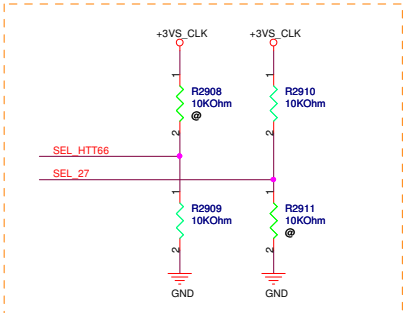






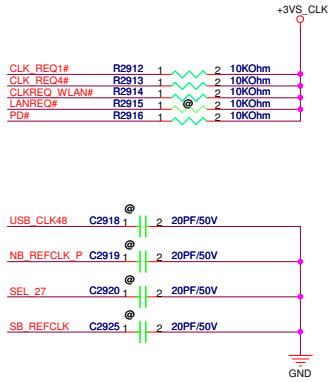






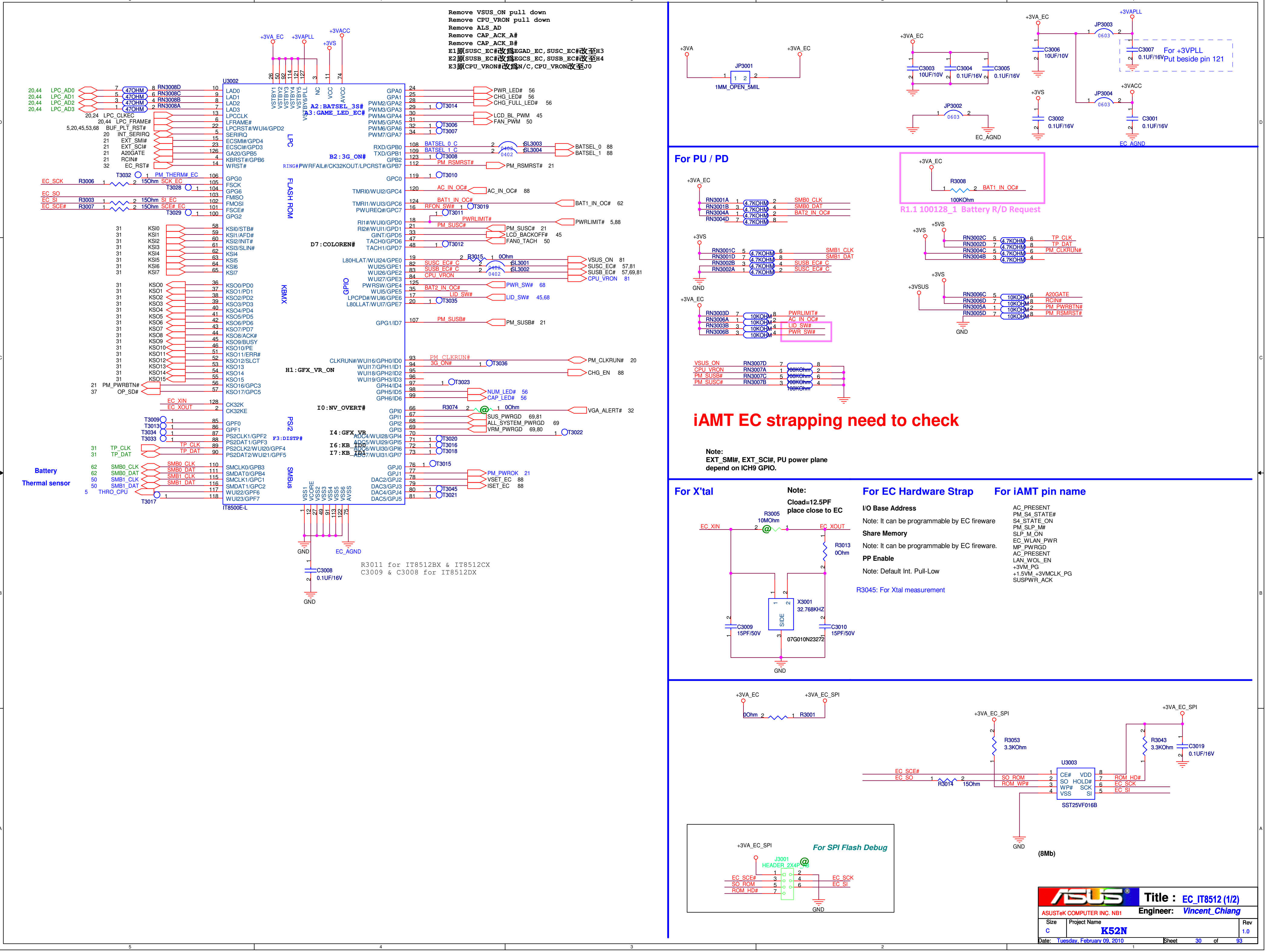
SEL_HTT66
0 : 100 MHz differential HTT clock (Default)
1 : 66MHz single ended HTT clock

SEL_27
0 : 100 MHz differential Spread SRC clock
1 : 27MHz spread/non-spreading single clock (Default)



<Variant Name>

ASUSTeK COMPUTER INC	Title : ICS9LPRS489AGLFT	
	Engineer:	
Size: Custom	Project Name: K51AB	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 29 of 93	



Remove VSUS_ON pull down
Remove CPU_VRON pull down
Remove ALS_AD
Remove CAP_ACK_A#
Remove CAP_ACK_B#
E1原SUSC_EC#改為EGAD_EC,SUSC_EC#改至H3
E2原SUSB_EC#改為EGCS_EC,SUSB_EC#改至H4
E3原CPU_VRON#改為N/C,CPU_VRON改至J0
U3002
IT8500E-L
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
A2:BATSEL_3S#
A3:GAME_LED_EC#
B2:3G_ON#
D7:COLOREN#
H1:GFX_VR_ON
I0:NV_OVERT#
I4:GFX_VR
I6:KB_ID0
I7:KB_ID1
F3:DISTP#
Battery
Thermal sensor
R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX
1MM_OPEN_5MIL
For +3VPLL
Put beside pin 121
For PU / PD
R1.1 100128_1 Battery R/D Request
iAMT EC strapping need to check
Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.
For X'tal
Note:
Cload=12.5PF
place close to EC
X3001
32.768KHZ
07G010N23272
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
R3045: For Xtal measurement
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
U3003
SST25VF016B
(8Mb)
For SPI Flash Debug
J3001
HEADER_2X4P
ASUSTeK COMPUTER INC. NB1
Title : EC_IT8512 (1/2)
Engineer: Vincent_Chiang
Size C
Project Name K52N
Rev 1.0
Date: Tuesday, February 09, 2010
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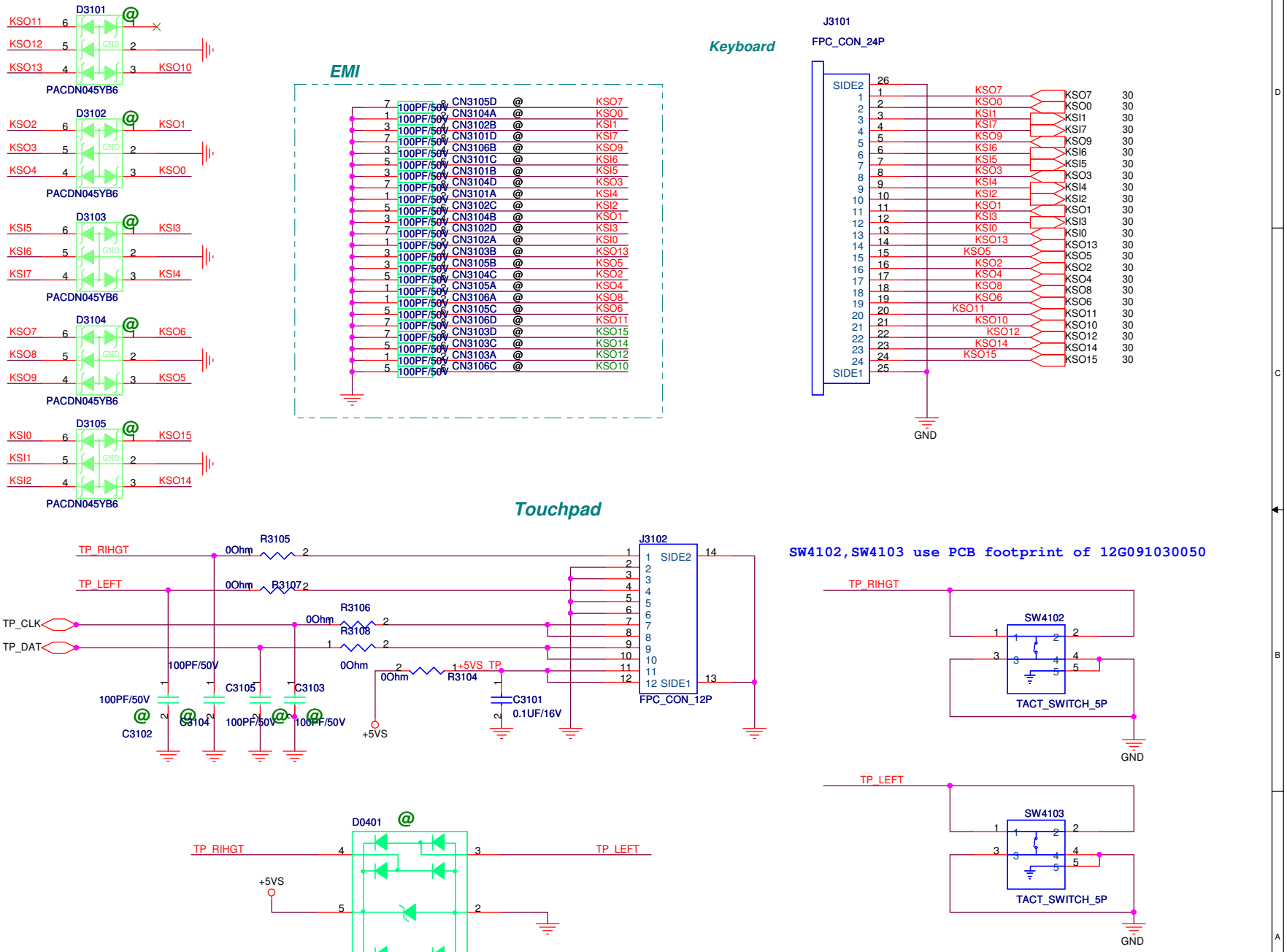
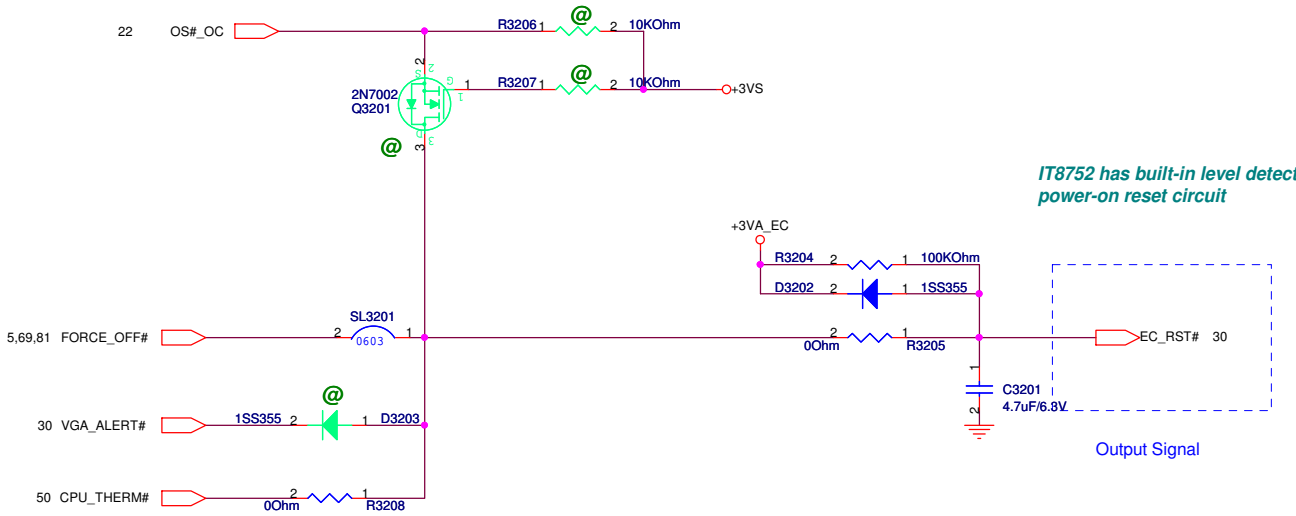


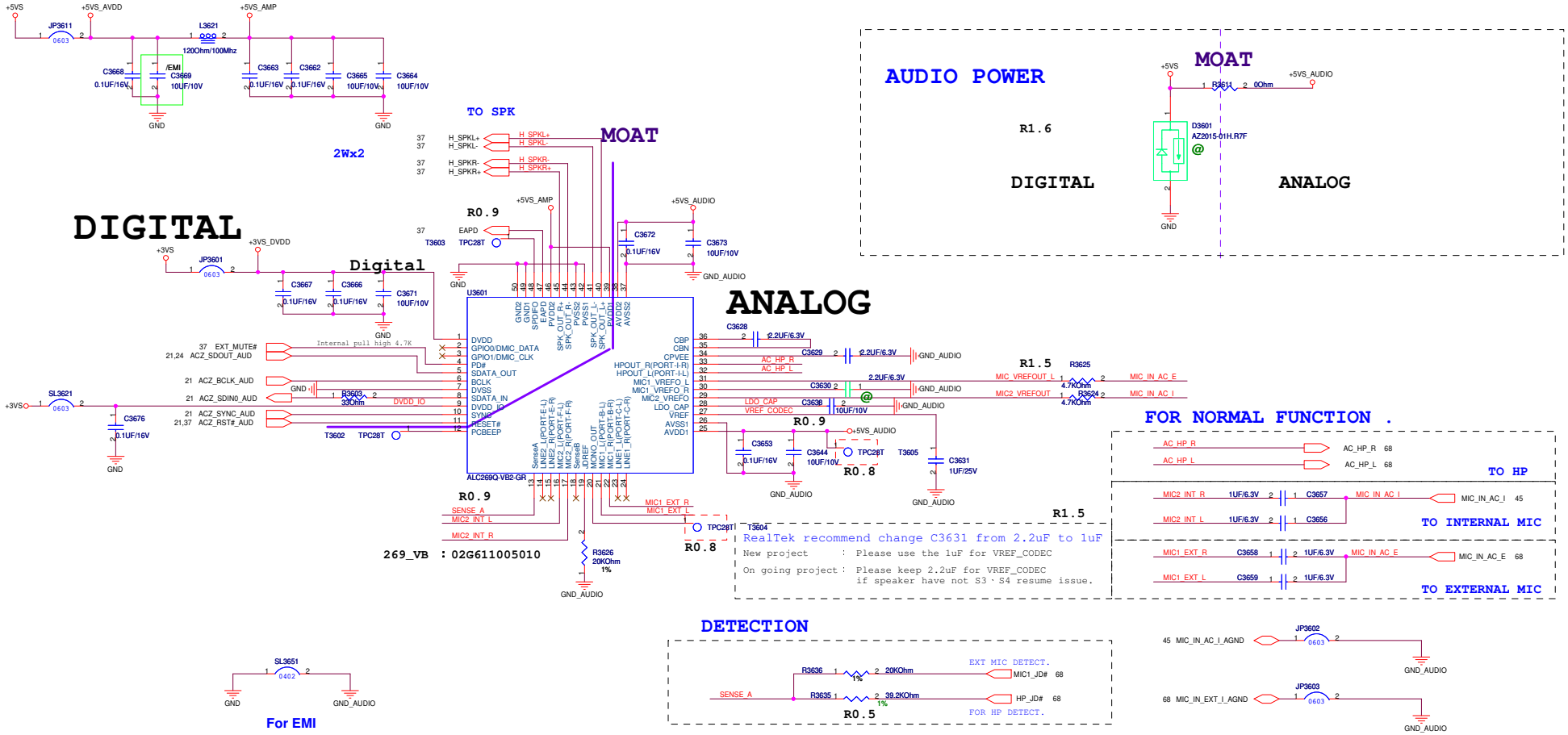
Title :	EC_IT8541(2/2)KB, TP	
ASUSTeK COMPUTER INC. NB4	Engineer:	Vincent_Chiang
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 31 of 99	

Thermal Policy

Main Board



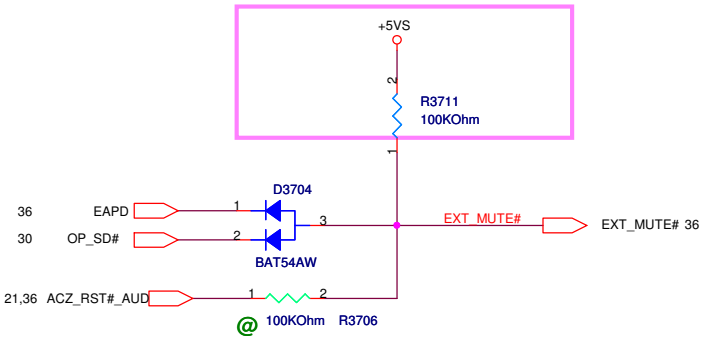
ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 32 of 99	



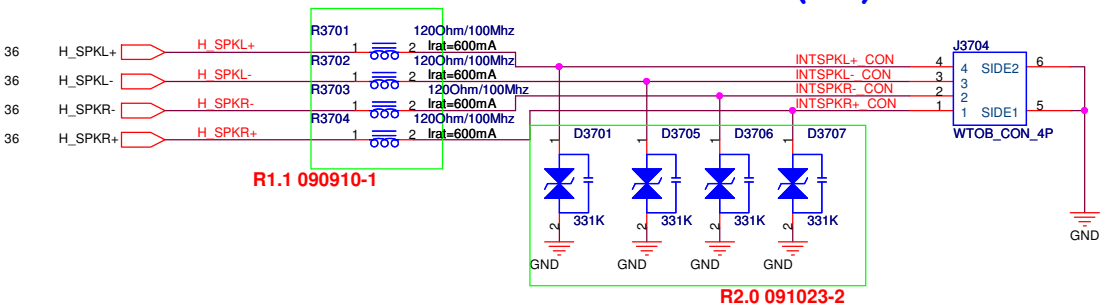
<variant_name>

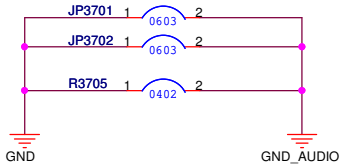
ASUSTeK COMPUTER INC. NB2	Title : CODEC ALC 269	
	Engineer: Leon	
Size: C	Project Name: K52Jr	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 36 of 99	

R1.1 100129_1 Change +3VS to +5VS



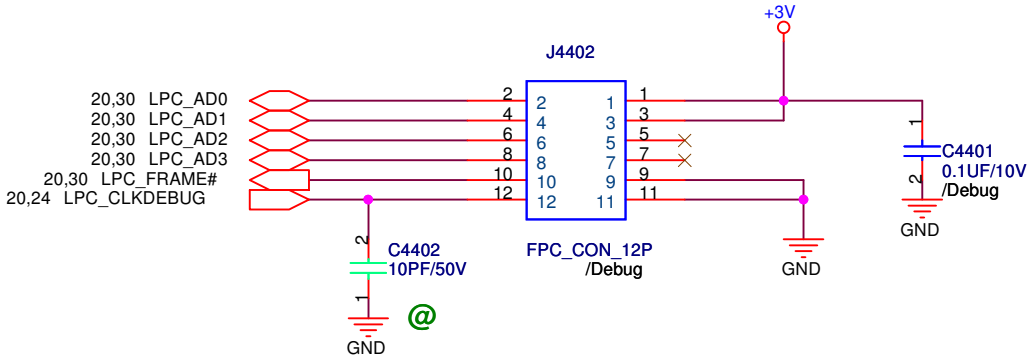
SPEAKER CONNECTOR (2W)



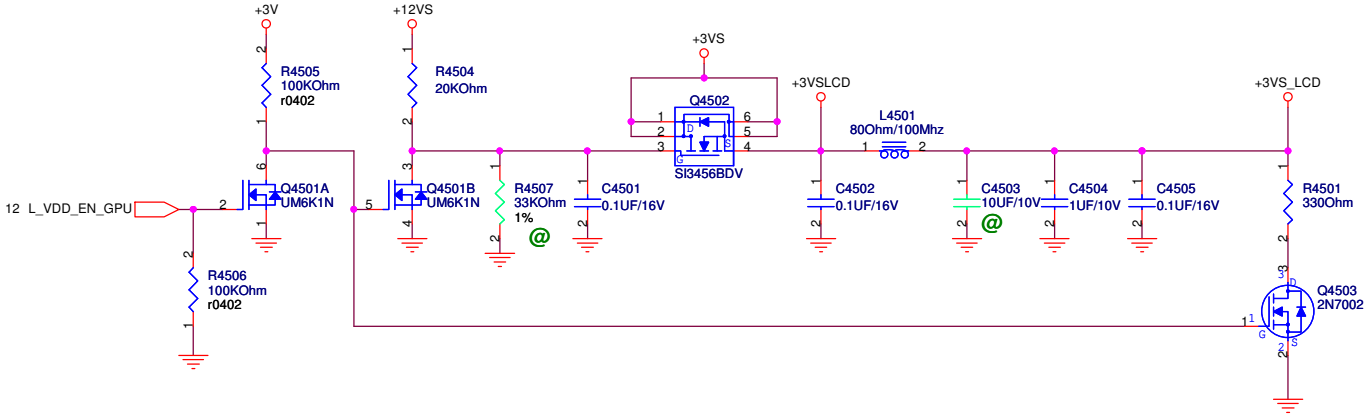


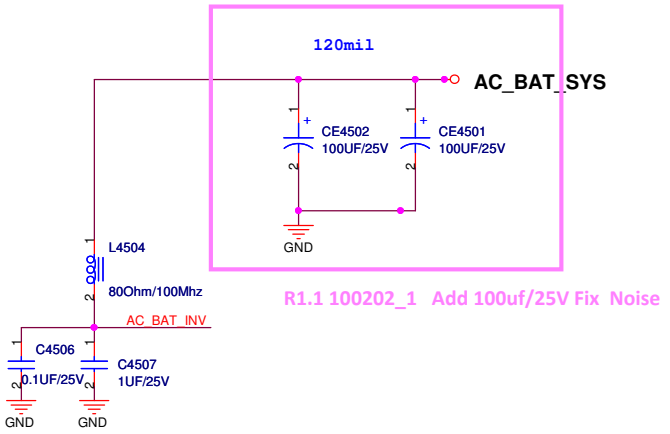
ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP	
	Engineer: Leon	
Size: B	Project Name: K52Jr	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 37 of 99	

LPC Debug Port



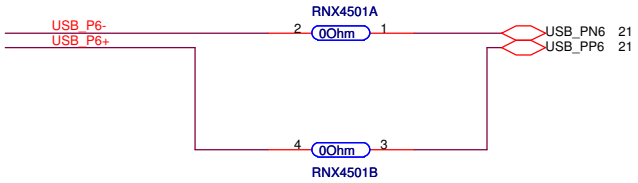
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 44 of 99	

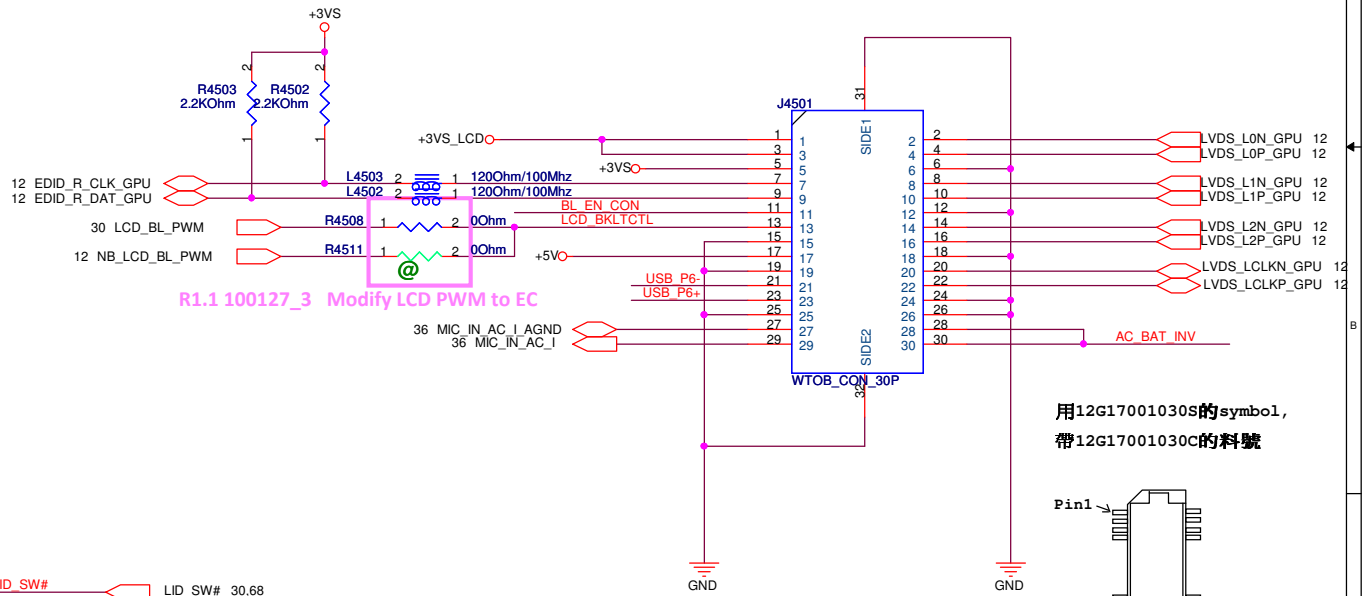




R1.1 100202_1 Add 100uf/25V Fix Noise

CAMERA & MIC

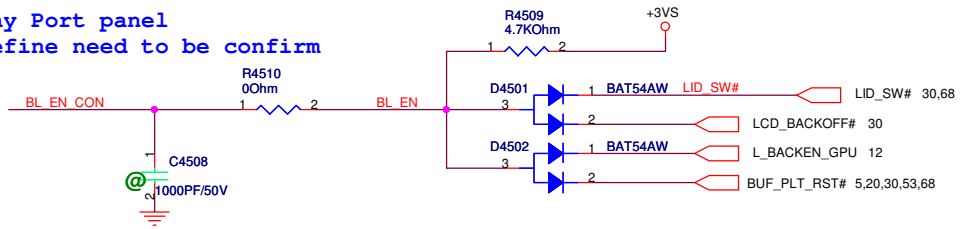




R1.1 100127_3 Modify LCD PWM to EC

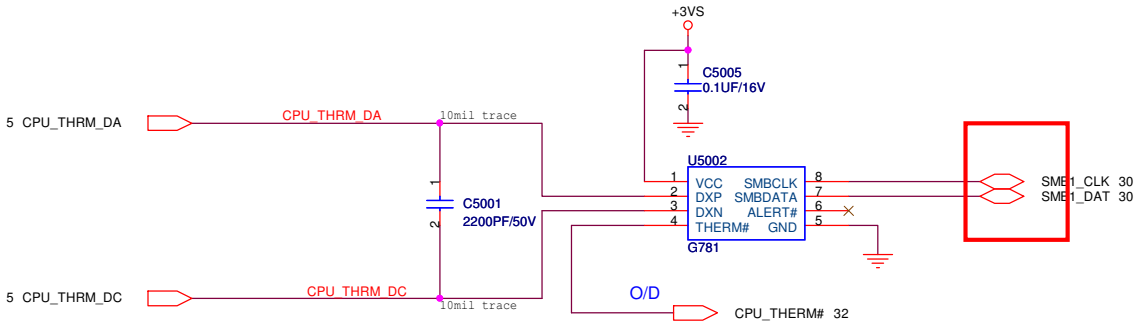
用12G17001030S的symbol,
帶12G17001030C的料號

Display Port panel pin define need to be confirm



ASUSTeK COMPUTER INC. NB4	Title : CRT_LCD Panel	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 45 of 99	

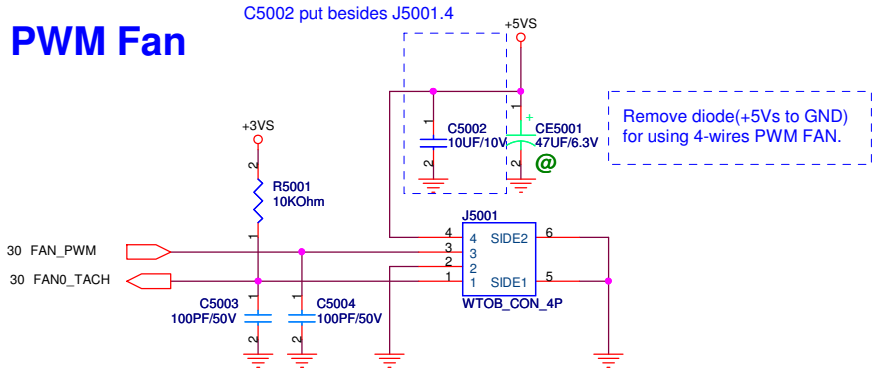
CPU Thermal Sensor



SMBUS addr=1001100x (98)

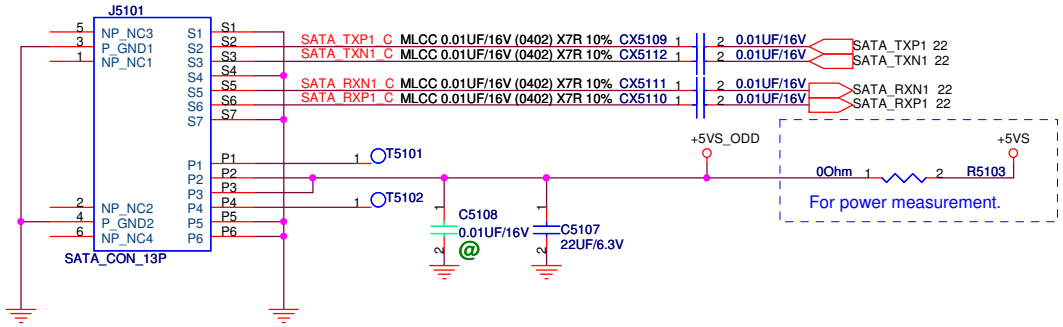
U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

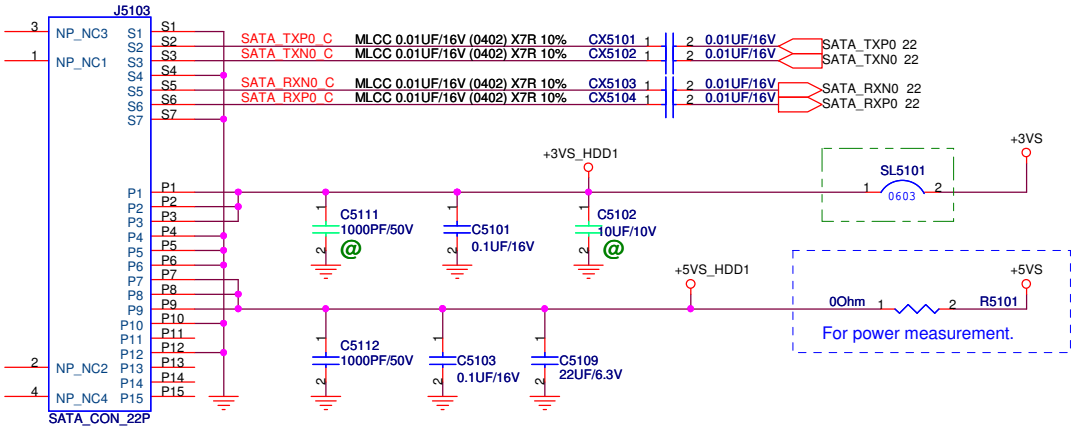


Title : FAN_Fan & Sensor		
ASUSTeK COMPUTER INC. NB4	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 50 of 99	

ODD



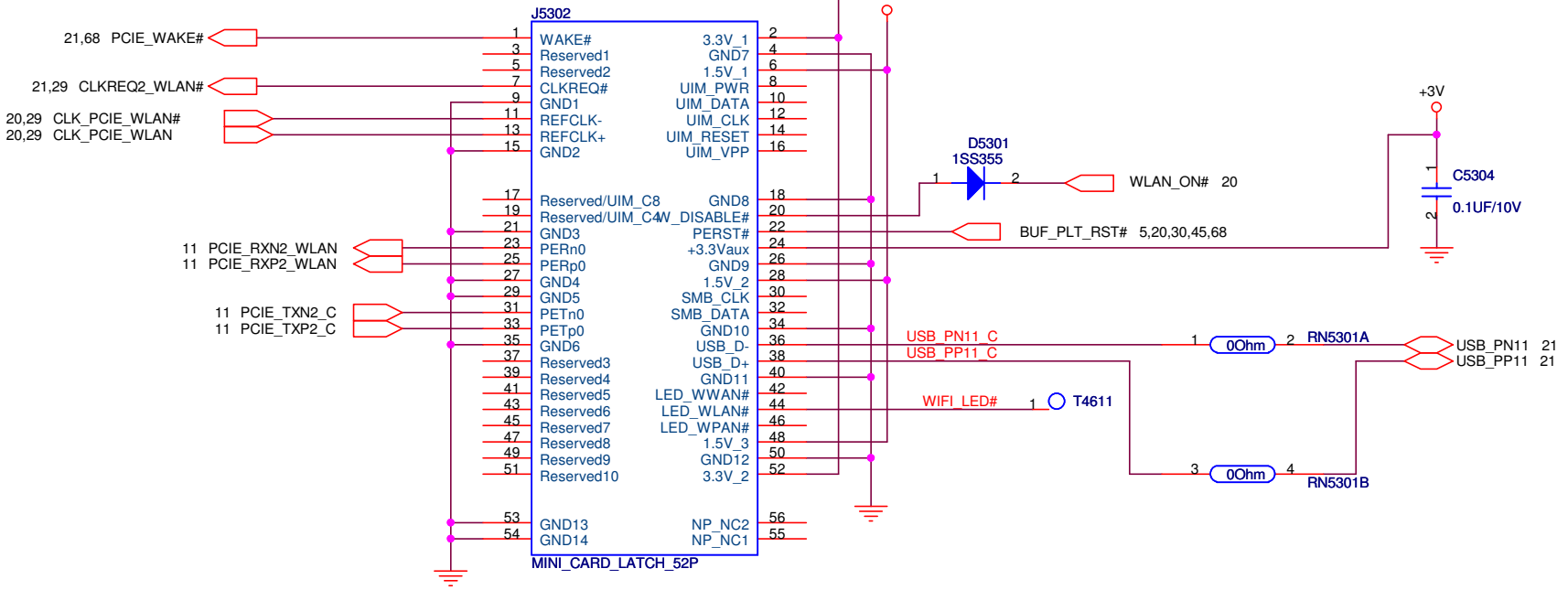
HDD (1st)



ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 51 of 99	

Suppport wake from S3 only

使用12G03010052F symbol

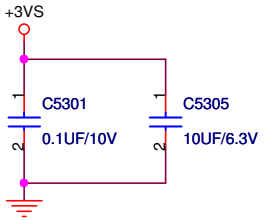


WLAN

WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

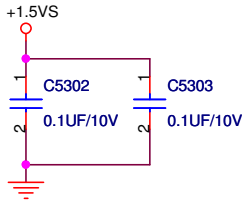
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

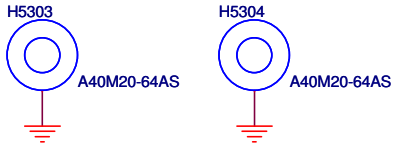


WLAN nuts:

Minicard spec R1.2:

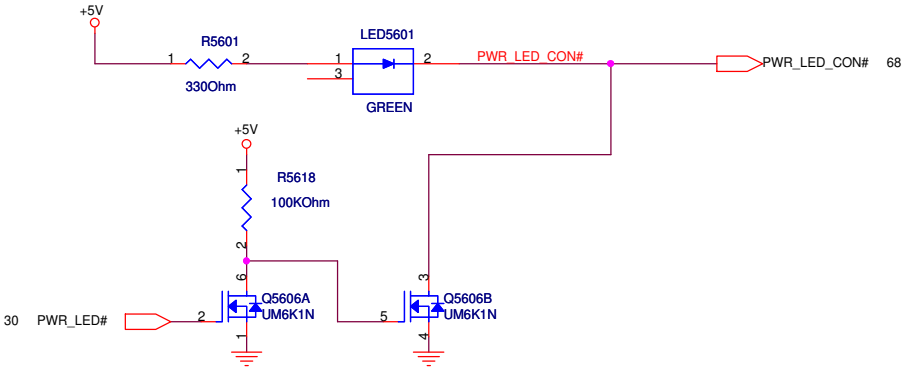
Full size card= 2pcs.

Half size card= 2pcs.

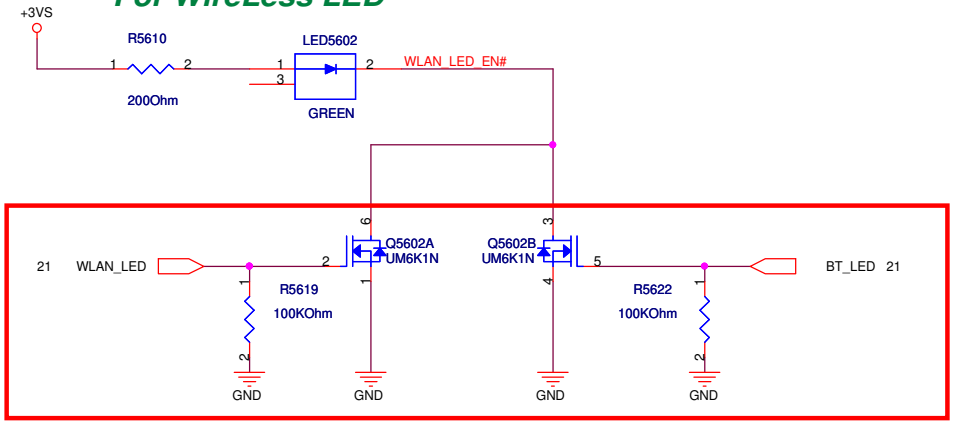


ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 53 of 99	

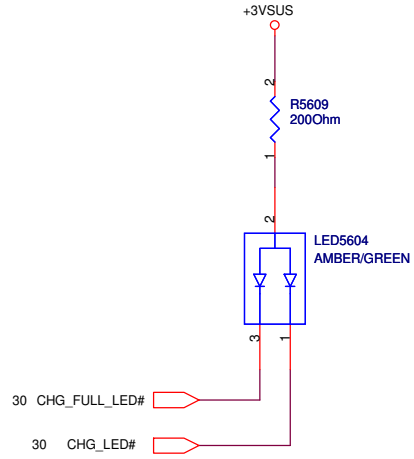
For POWER LED



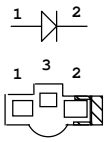
For WireLess LED



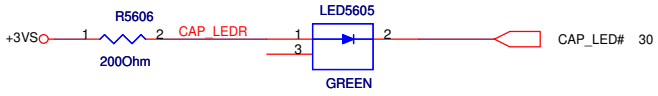
Charge LED



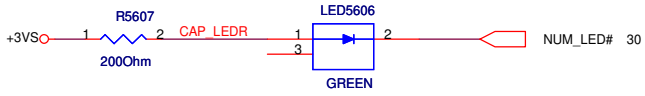
Side Light LED symbol



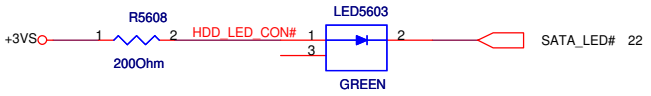
Cap. Lock LED



for Num Lock



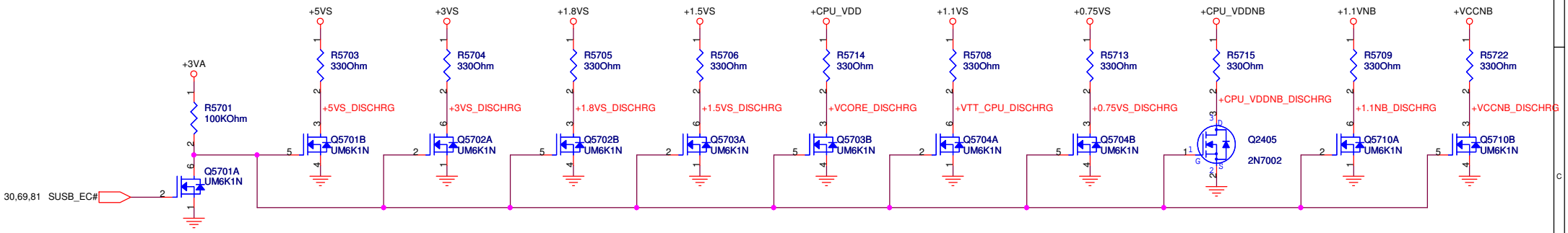
HDD LED

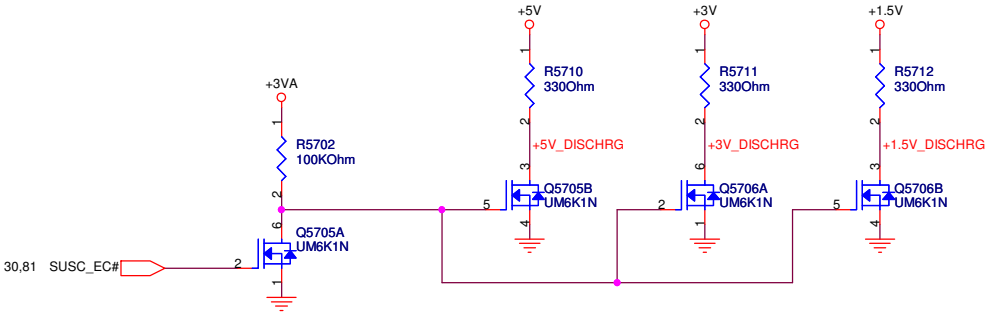


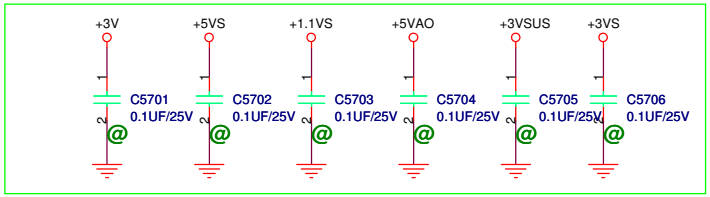
ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 56 of 99	

Main Board

Remove +2.5Vs is for ATI GFX

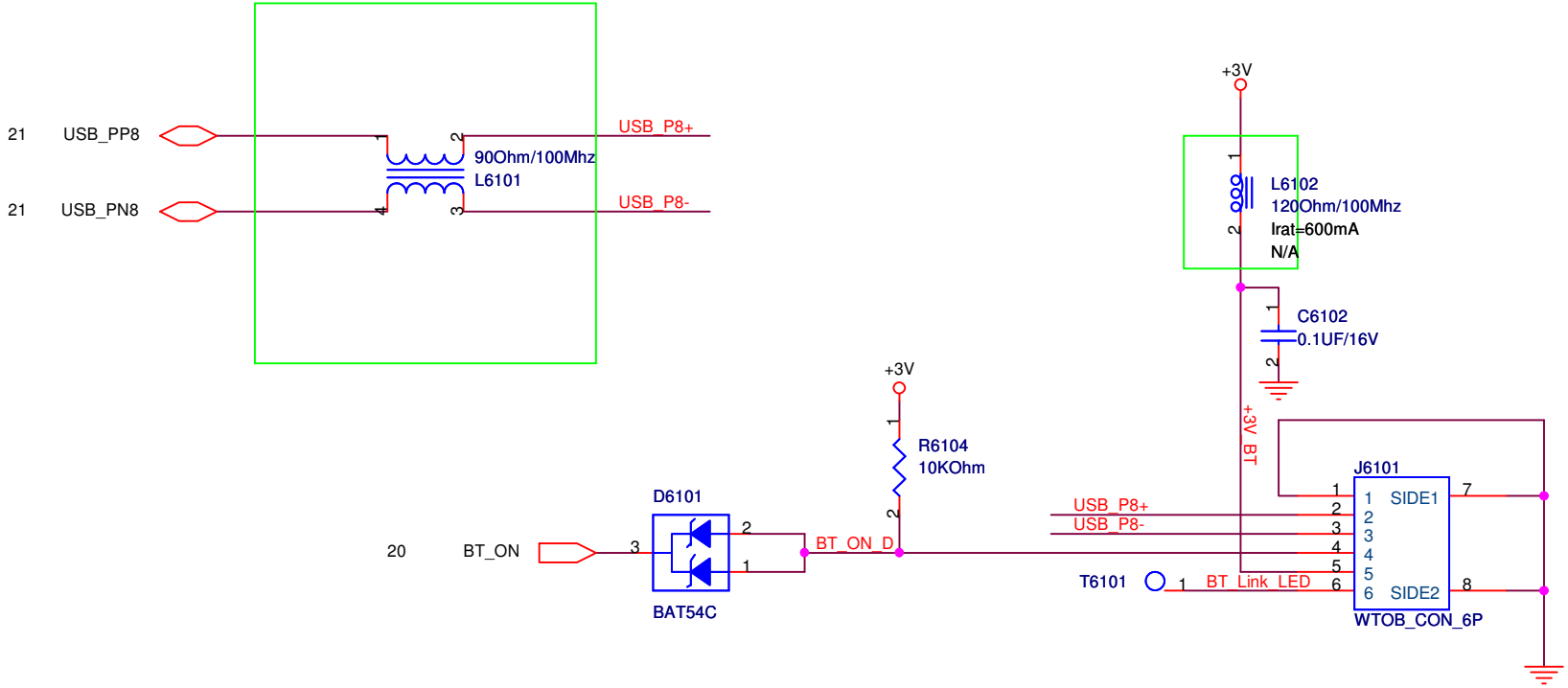






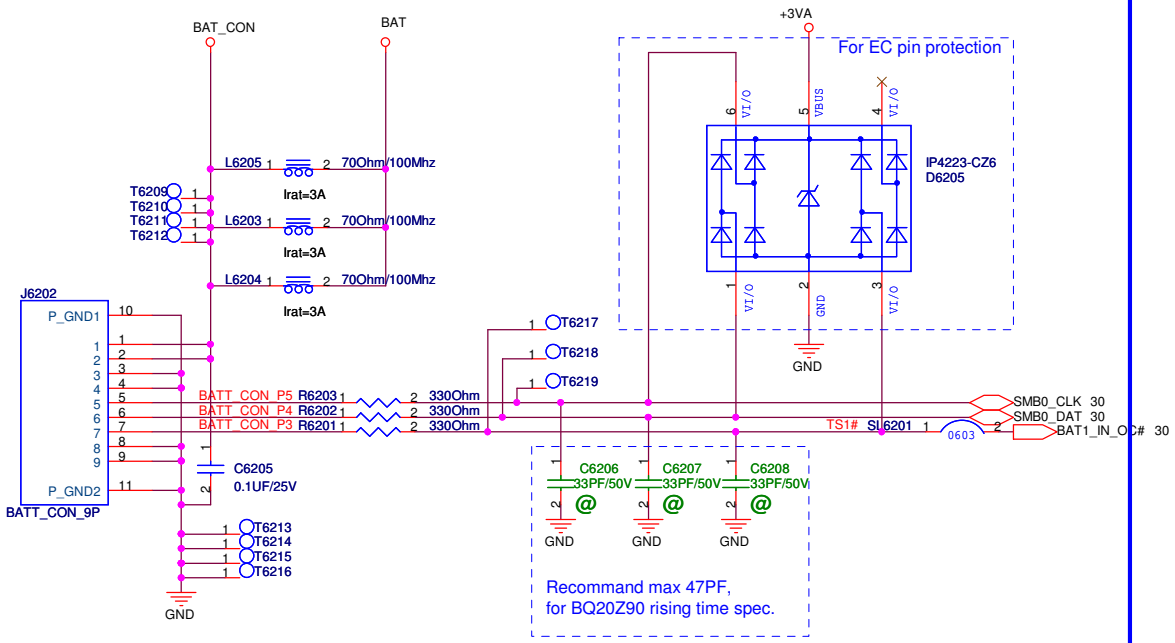
ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 57 of 99	

BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 61 of 99	

Battery Connector

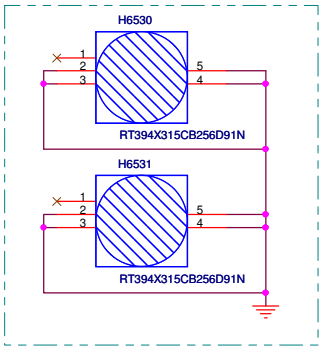


Total count: 11 pcs

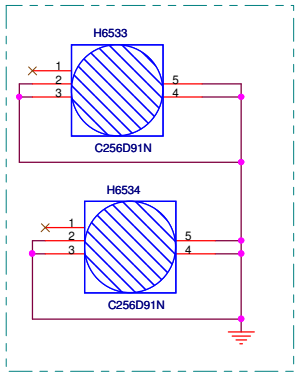
ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 62 of 99	

Main Board

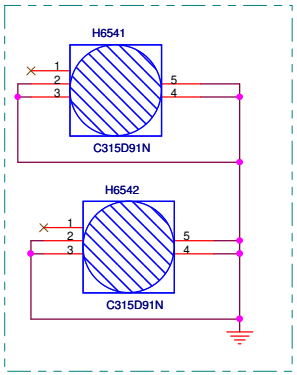
Screw Hole A



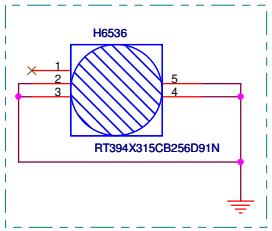
Screw Hole B



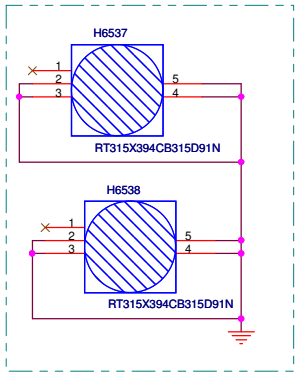
Screw Hole I



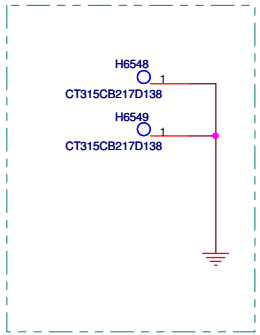
Screw Hole C



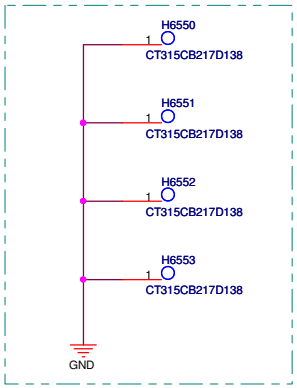
Screw Hole F



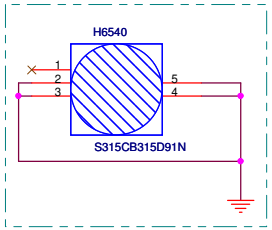
Screw Hole E



Screw from k52JR

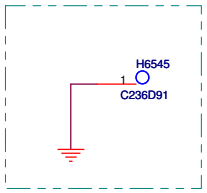


Screw Hole H



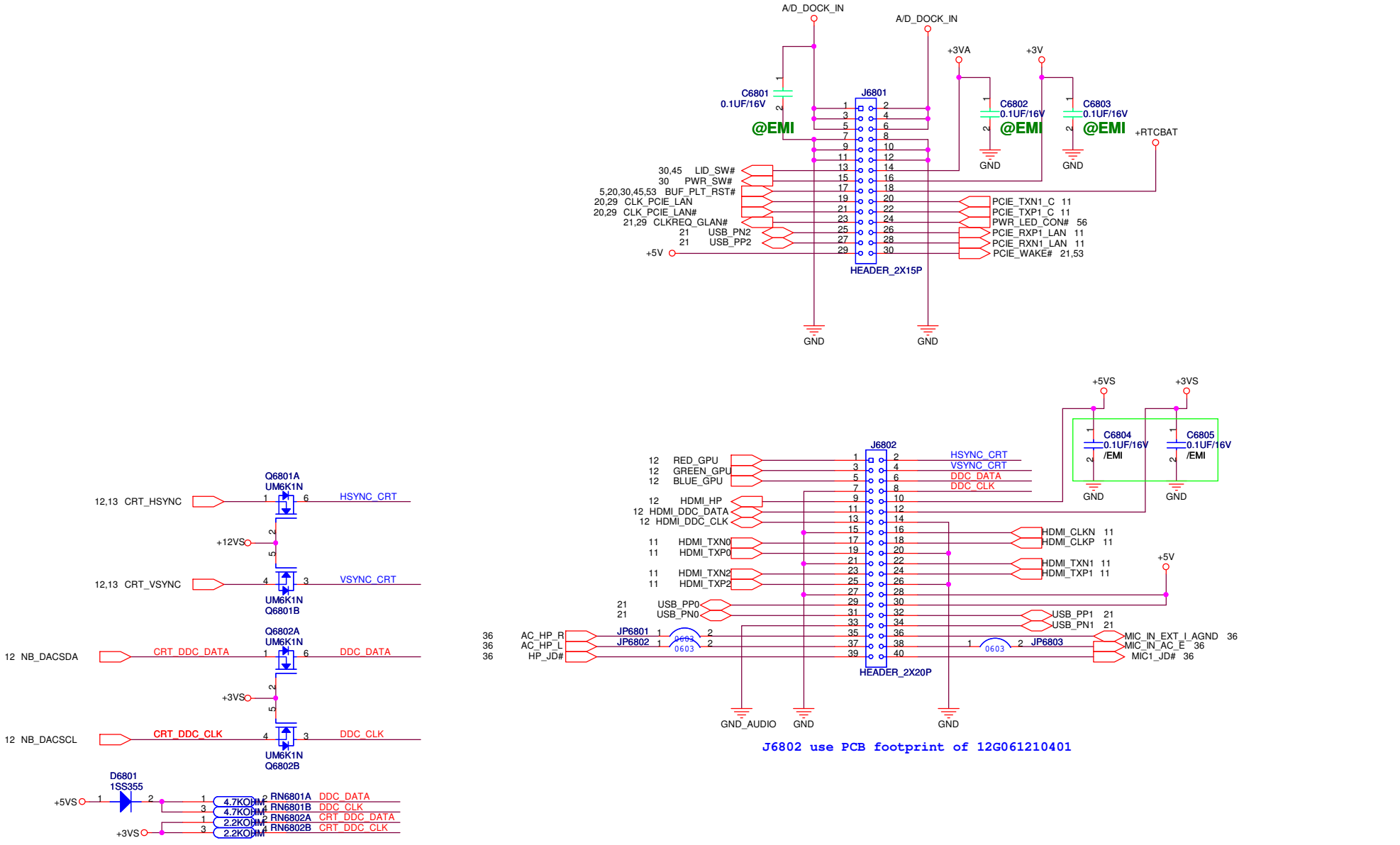
Tooling Hole K

Screw Hole O



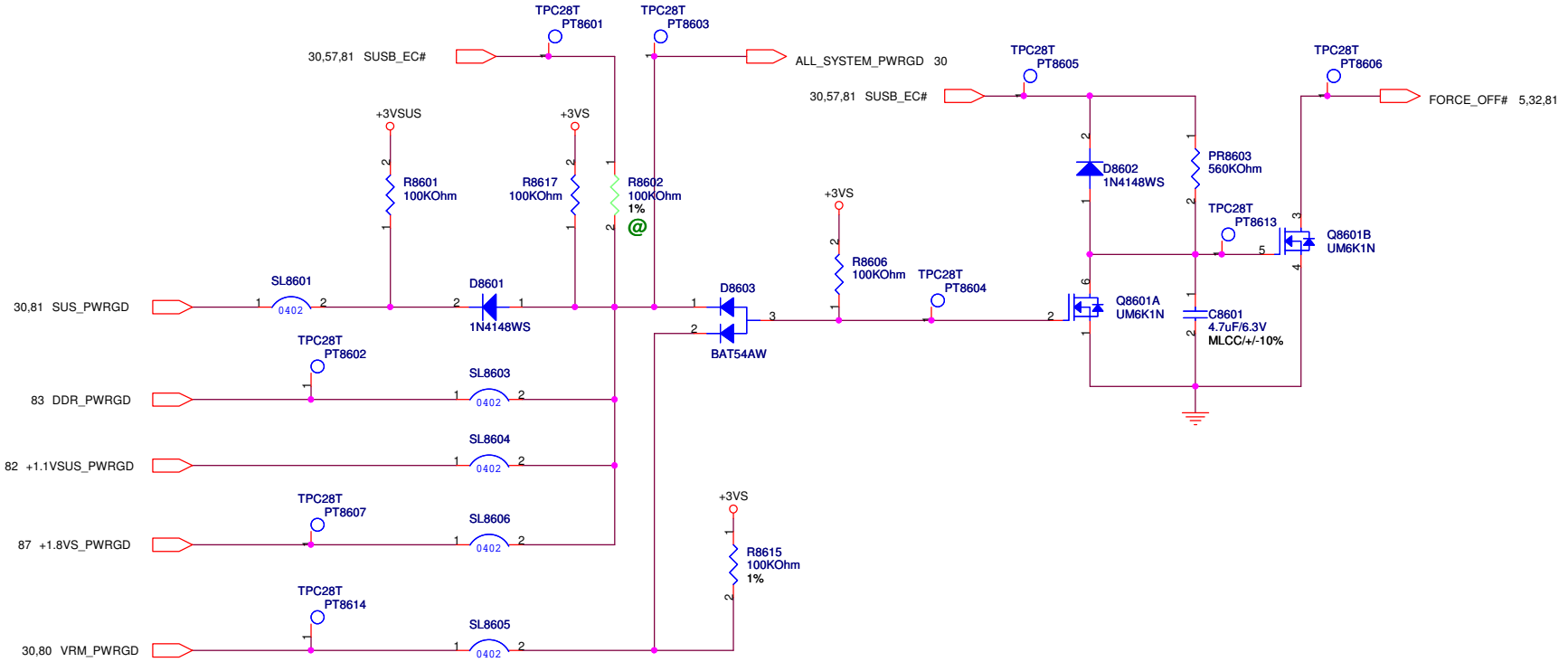
Tooling Hole L

ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 65 of 99	



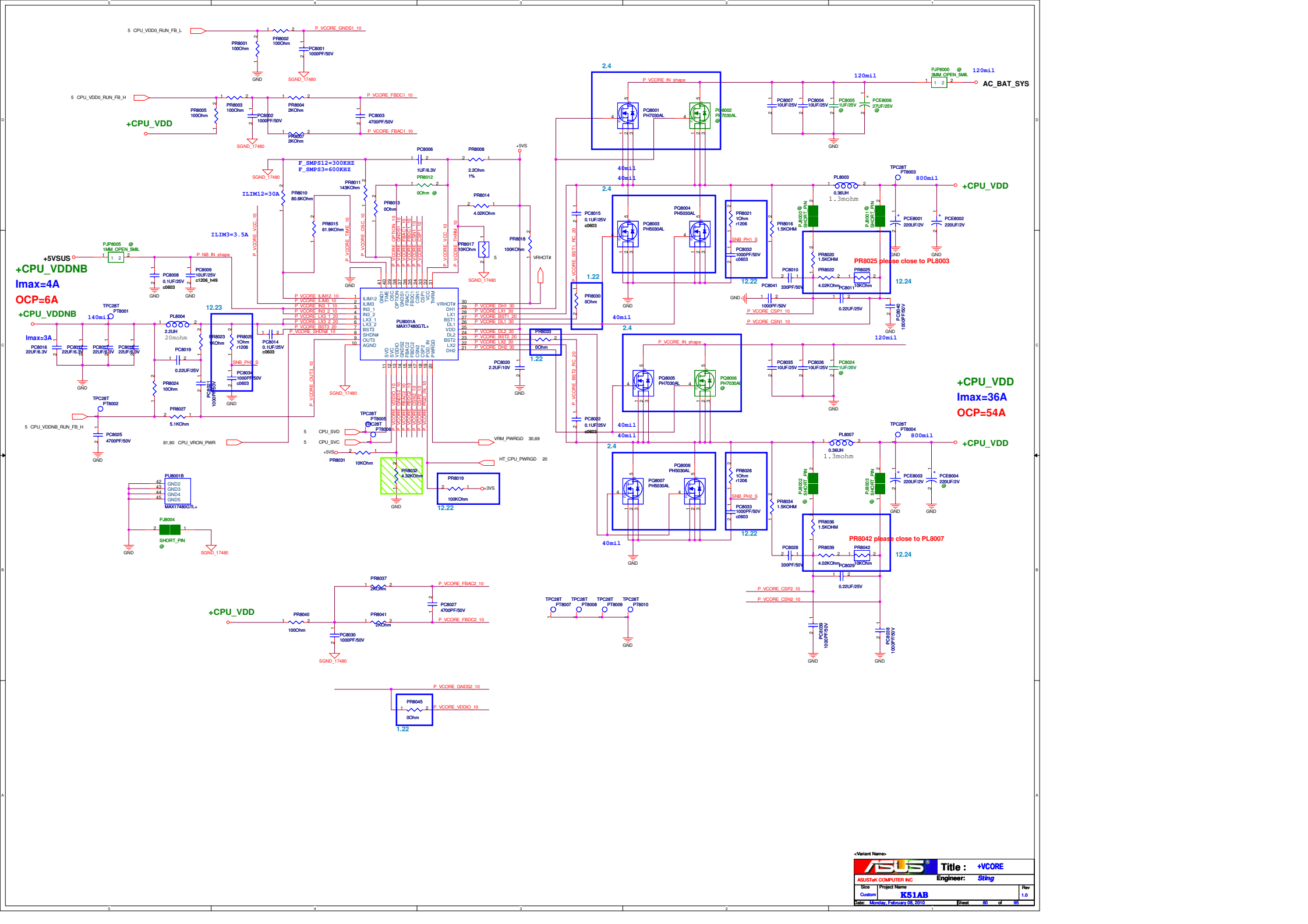
ASUSTeK COMPUTER INC. NB4	Title : IO Connector	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 68 of 99	

POWER GOOD DETECTER

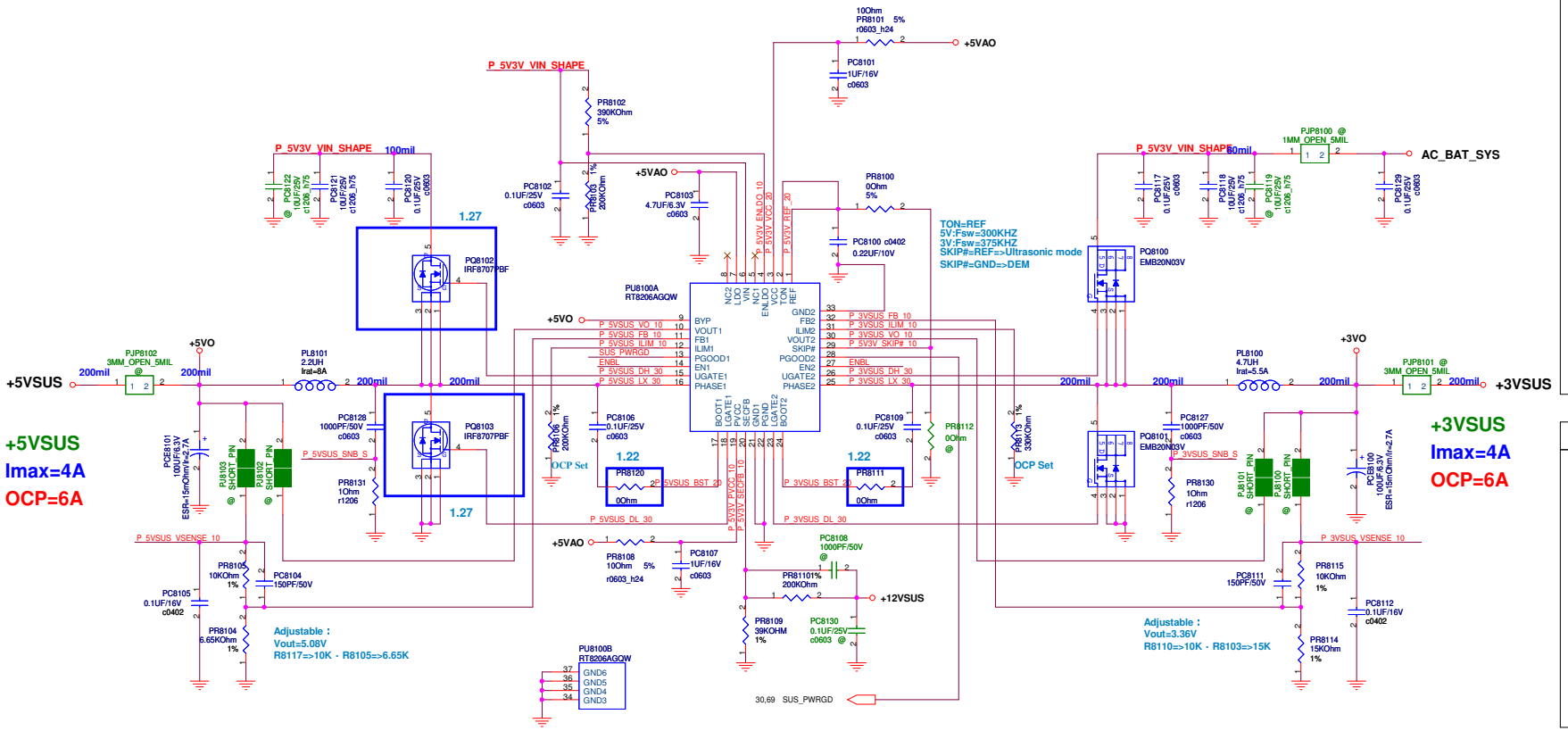


<Variant Name>

ASUSTeK COMPUTER INC	Title : GOOD_DETECTER	
	Engineer: Vincent_Chiang	
Size: B	Project Name	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 69 of 95	


+CPU_VDDNB
Imax=4A
OCP=6A
+CPU_VDD
Imax=36A
OCP=54A
AC_BAT_SYS
+5VSUS
+CPU_VDD
F_SMPS12=300KHZ
F_SMPS3=600KHZ
ILIM12=30A
ILIM3=3.5A
PR8025 please close to PL8003
PR8042 please close to PL8007
PU8001A MAX17480GTL+
PU8001B MAX17480GTL+
PJ8004 SHORT_PIN
PJP8000 3MM_OPEN_5MIL
PJP8005 1MM_OPEN_5MIL
PL8003 0.36UH 1.3mohm
PL8004 2.2UH 20mohm
PL8007 0.36UH 1.3mohm
PQ8001 PH7030AL
PQ8002 PH7030AL
PQ8003 PH5030AL
PQ8004 PH5030AL
PQ8005 PH7030AL
PQ8006 PH7030AL
PQ8007 PH5030AL
PQ8008 PH5030AL
PR8030 0Ohm
PR8033 0Ohm
PR8031 10KOhm
PR8032 4.32KOhm
PR8019 100KOhm
PR8045 0Ohm
PR8040 100Ohm
PR8041 2KOhm
PR8037 2KOhm
PC8030 1000PF/50V
PC8027 4700PF/50V
PC8020 2.2UF/10V
PC8022 0.1UF/25V c0603
PC8014 0.1UF/25V c0603
PC8015 0.1UF/25V c0603
PC8029 10UF/25V c1206_h49
PC8031 1000PF/50V
PC8034 1000PF/50V c0603
PC8032 1000PF/50V c0603
PC8033 1000PF/50V c0603
PC8039 1000PF/50V
PC8035 1000PF/50V
PC8041 330PF/50V
PC8028 330PF/50V
PC8040 100PF/50V
PC8016 22UF/6.3V
PC8017 22UF/6.3V
PC8018 22UF/6.3V
PC8007 10UF/25V
PC8004 10UF/25V
PC8005 1UF/25V
PC8026 10UF/25V
PC8024 1UF/25V
PCE8006 270UF/25V
PCE8001 220UF/2V
PCE8002 220UF/2V
PCE8003 220UF/2V
PCE8004 220UF/2V
PC8001 1000PF/50V
PC8002 1000PF/50V
PC8003 4700PF/50V
PR8001 100Ohm
PR8002 100Ohm
PR8003 100Ohm
PR8004 2KOhm
PR8005 100Ohm
PR8006 1UF/6.3V
PR8007 2KOhm
PR8008 2.2Ohm 1%
PR8010 80.6KOhm
PR8011 143KOhm
PR8012 0Ohm @
PR8013 0Ohm
PR8014 4.02KOhm
PR8015 61.9KOhm
PR8017 10KOhm
PR8018 100KOhm
PR8016 1.5KOHM
PR8020 1.5KOHM
PR8021 1Ohm r1206
PR8022 4.02KOhm
PR8025 10KOhm
PR8026 1Ohm r1206
PR8034 1.5KOHM
PR8036 1.5KOHM
PR8039 4.02KOhm
PR8042 10KOhm
PR8023 9KOhm
PR8029 1Ohm r1206
PR8024 10Ohm
PR8027 5.1KOhm
PC8019 0.22UF/25V
PC8011 0.22UF/25V
PC8029 0.22UF/25V
PC8025 4700PF/50V
PC8008 0.1UF/25V c0603
TPC28T PT8001
TPC28T PT8002
TPC28T PT8003
TPC28T PT8004
TPC28T PT8005
TPC28T PT8006
TPC28T PT8007
TPC28T PT8008
TPC28T PT8009
TPC28T PT8010
SNB_PH1_S
SNB_PH2_S
P_VCORE_IN_shape
P_NB_IN_shape
P_VCORE_GNDS1_10
P_VCORE_FBDC1_10
P_VCORE_FBAC1_10
P_VCORE_GNDS2_10
P_VCORE_VDDIO_10
P_VCORE_FBAC2_10
P_VCORE_FBDC2_10
P_VCORE_CSP2_10
P_VCORE_CSN2_10
P_VCORE_CSP1_10
P_VCORE_CSN1_10
P_VCORE_DH1_30
P_VCORE_LX1_30
P_VCORE_BST1_20
P_VCORE_DL1_30
P_VCORE_DL2_30
P_VCORE_BST2_20
P_VCORE_LX2_30
P_VCORE_DH2_30
P_VCORE_BST1_RC_20
P_VCORE_BST2_RC_20
P_VCORE_ILIM12_10
P_VCORE_ILIM3_10
P_VCORE_IN3_2_10
P_VCORE_IN3_1_10
P_VCORE_LX3_1_20
P_VCORE_LX3_2_20
P_VCORE_BST3_20
P_VCORE_SHDN#_10
P_VCORE_OUT3_10
P_VCORE_OPTION_10
P_VCORE_TIME_10
P_VCORE_OSC_10
P_VCORE_VCC_10
P_VCORE_THRM_10
VRHOT#
VRM_PWRGD 30,69
HT_CPU_PWRGD 20
81,90 CPU_VRON_PWR
5 CPU_SVD
5 CPU_SVC
5 CPU_VDD0_RUN_FB_L
5 CPU_VDD0_RUN_FB_H
5 CPU_VDDNB_RUN_FB_H
GND
SGND_17480
+5VS
+3VS
120mil
800mil
40mil
140mil
2.4
1.22
12.22
12.23
12.24
<Variant Name>
Title : +VCORE
ASUSTeK COMPUTER INC
Engineer: Sting
Size Custom
Project Name K51AB
Rev 1.0
Date: Monday, February 08, 2010
Sheet 80 of 85

+5VSUS / +3VSUS POWER SUPPLY



Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.96A
2. Ripple Current:
   Irip=2.61A
3. Ripple Voltage:
   ESR/1=15mohm
   V=39.15mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm
5. MOSFET Spec:
   H-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)
   L-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.96A
2. Ripple Current:
   Irip=1.55A
3. Ripple Voltage:
   ESR/1=15mohm
   V=23.25mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm

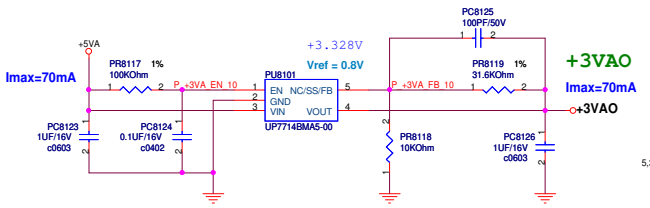
Controller

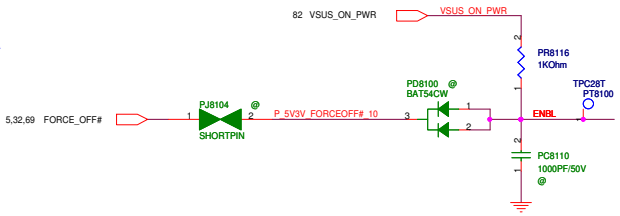
+5VSUS:

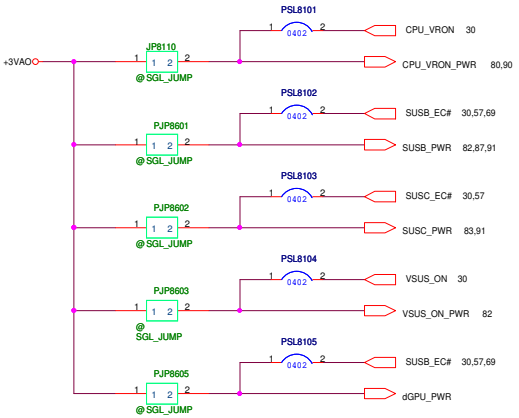
1. Voltage & Current:
   +5VSUS: 5V / 4A
2. Frequency:
   F=300KHZ
3. OCP:
   Set PR8106=357 Kohm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Soft start time:
   The Soft Start duration is 2ms
5. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.25 A

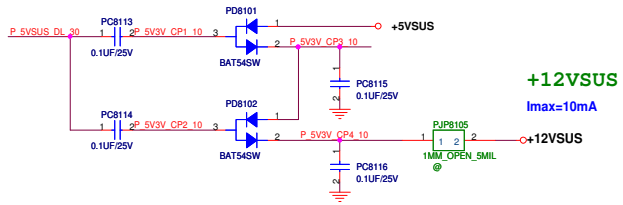
+3.VSUS

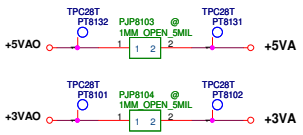
1. Voltage&Current:
   +3VSUS: 3.3V / 4A
2. Frequency:
   F=375KHZ
3. OCP:
   Set PR8113=357KOhm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.165 A

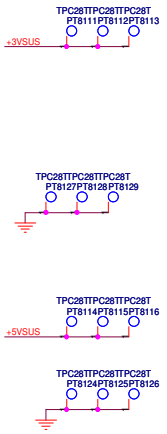








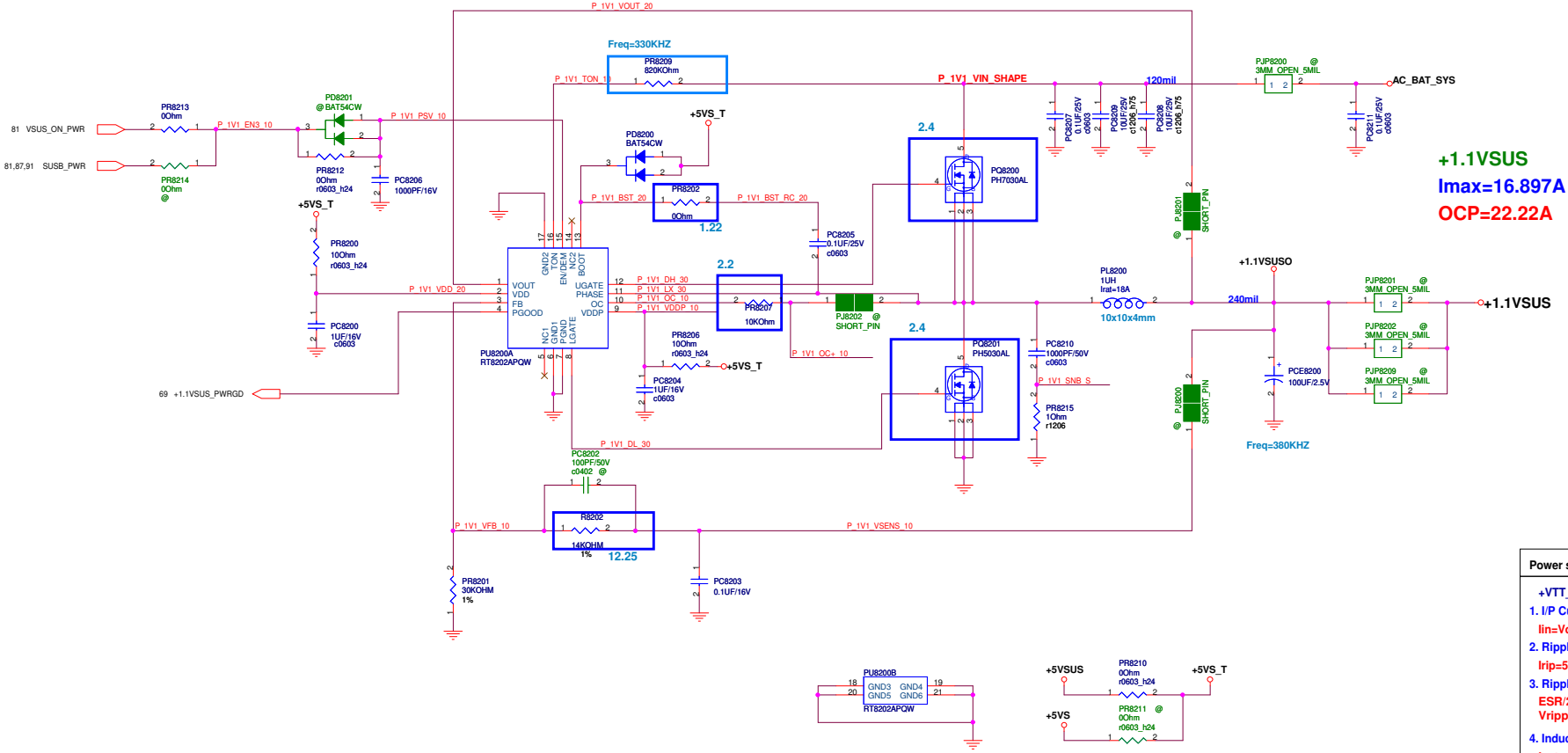




<variant_name>

ASUSTeK COMPUTER INC. NB	Title : POWER_SYSTEM	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 81 of 95	

+1.1VSUS POWER SUPPLY



PT8200 TPC28T +1.1VSUSO
PT8201 TPC28T +1.1VSUSO
PT8202 TPC28T +1.1VSUS
PT8203 TPC28T +1.1VSUS
PT8204 TPC28T GND
PT8205 TPC28T GND

Controller

+VTT_CPU:

1. Voltage & Current:
   +VTT_CPU: 1.05V / 15A
2. Frequency:
   F=330KHZ
3. OCP:
   Set PR8207=4.99 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26A
4. Soft start time:
   The SS duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.342 A

Power stage

+VTT_CPU:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.33A
2. Ripple Current:
   Irip=5.36A
3. Ripple Voltage:
   ESR/2=7.5mohm
   Vripple=40.26mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.6mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

<Variant Name>

Title : POWER_I/O_+VCCP

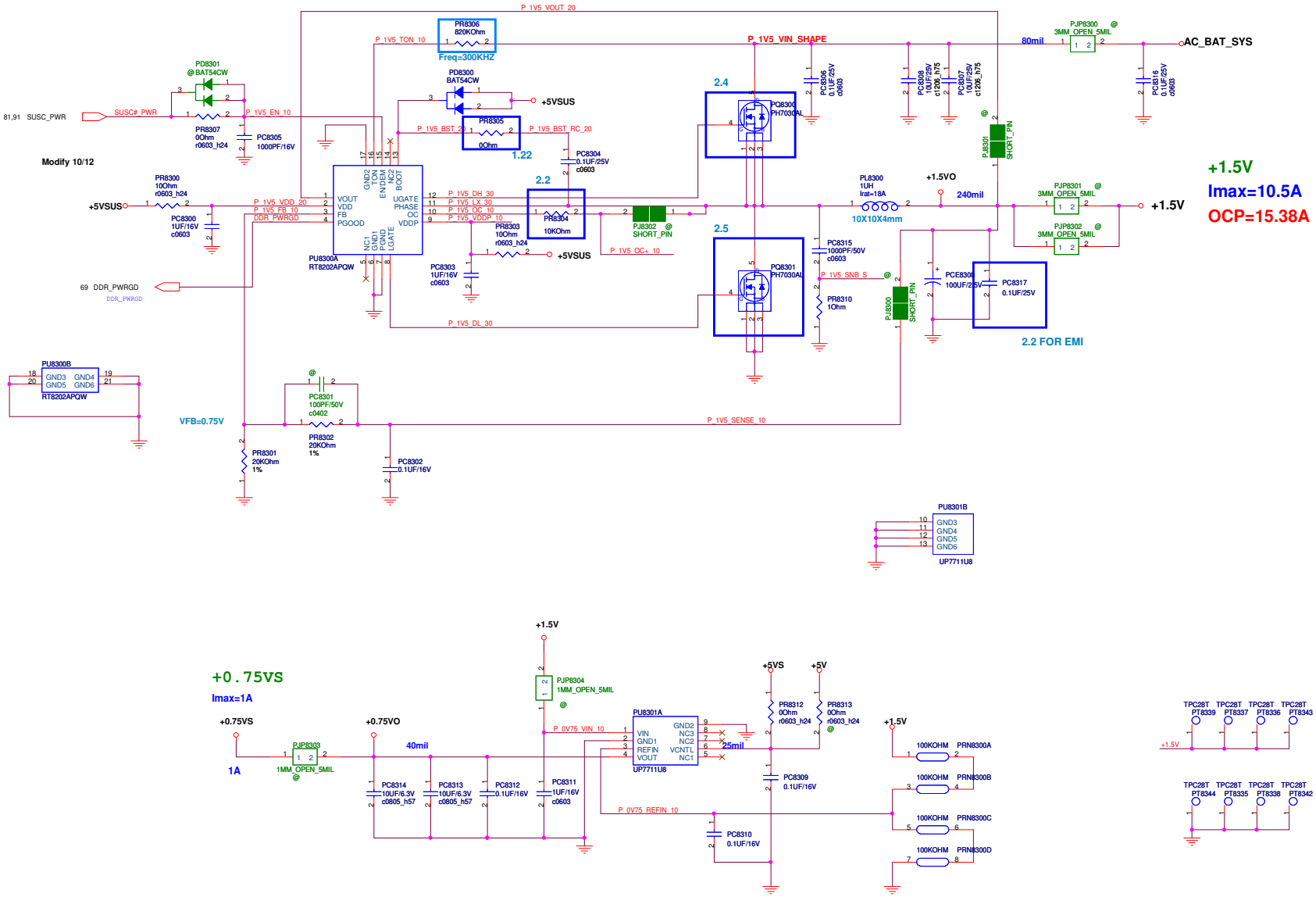
ASUSTeK COMPUTER INC. NB

Engineer: Matt_Wang

Size	Project Name	Rev
Custom	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 82 of 95

+1.5V & +0.75VS POWER SUPPLY



Power stage

DDR III:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.22A
2. Ripple Current:
   Irip=4.62A
3. Ripple Voltage:
   ESR/1=15mohm
   V=69.3mV
4. Inductor Spec:
   Isat=12.7A
   Idc=9.5A
   DCR=8.5mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

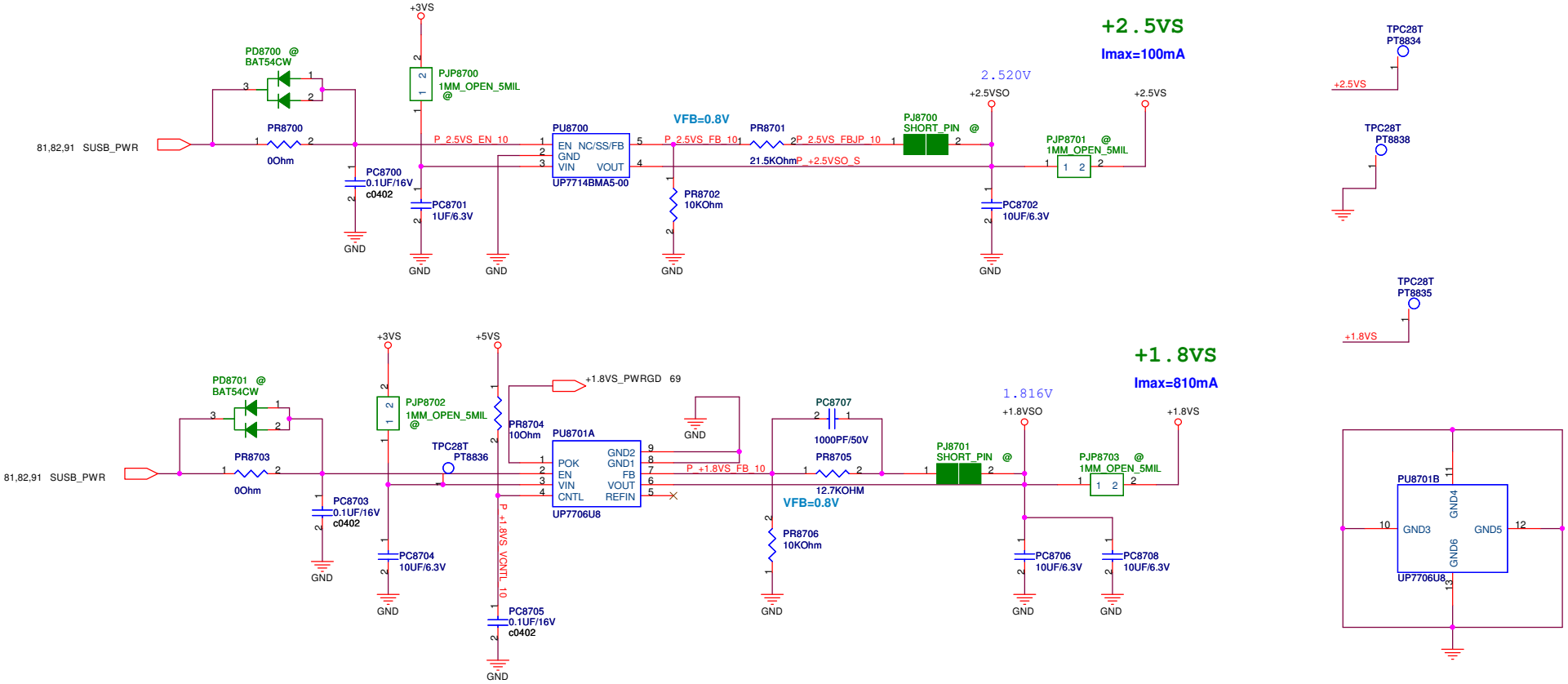
Controller

DDR III:

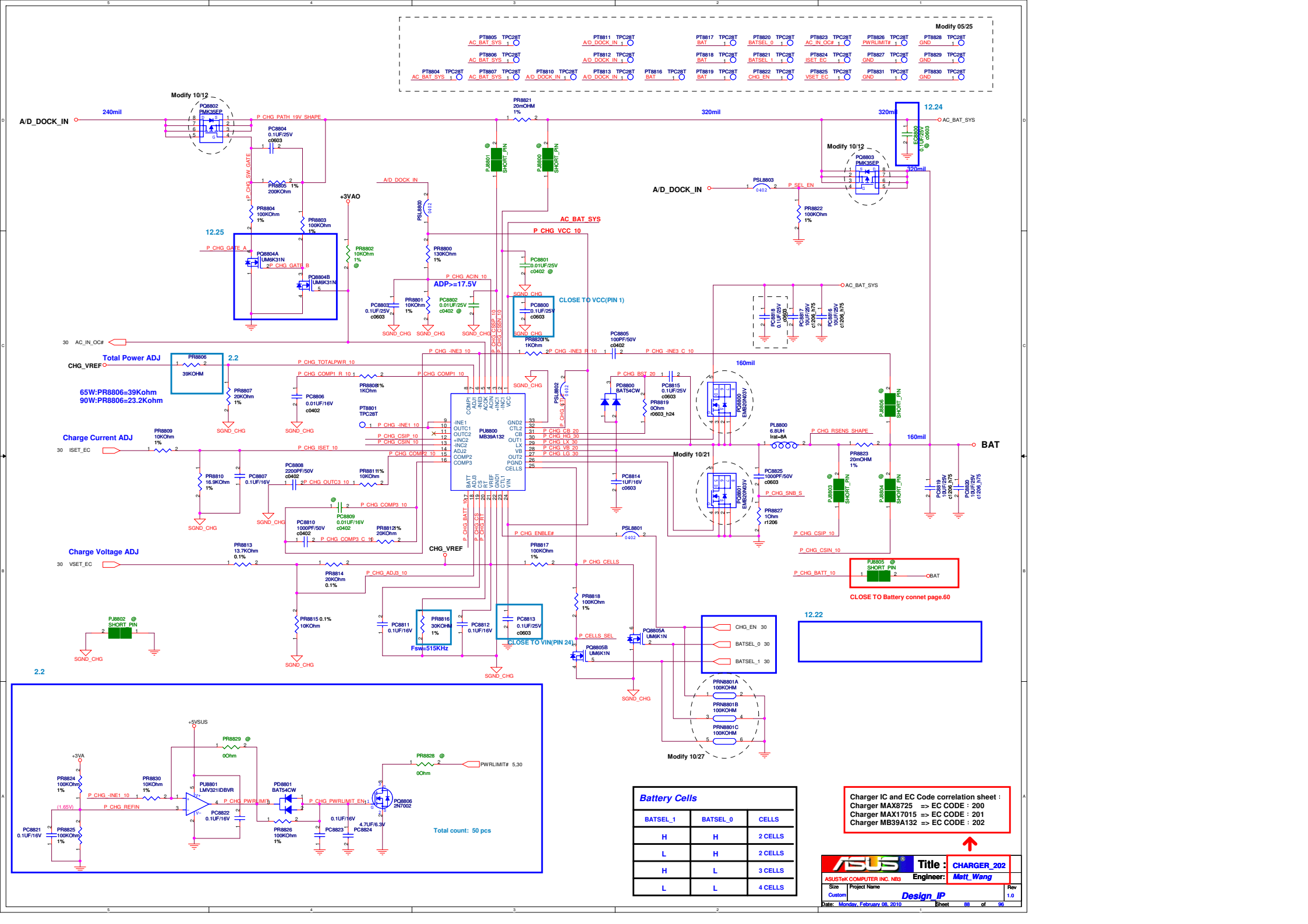
1. Voltage & Current:
   +1.5V: 1.5V / 10A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8302=12 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=14.3A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.244 A
1. Voltage & Current:
   +0.75V: 0.75V / 1A

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_DDR	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 83 of 95	



ASUSTek Computer INC.	Title :	
	Engineer:	
Size: A3	Project Name: Oemga	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 87 of 95	


Modify 05/25
PT8805 TPC28T AC_BAT_SYS
PT8806 TPC28T AC_BAT_SYS
PT8804 TPC28T AC_BAT_SYS
PT8807 TPC28T AC_BAT_SYS
PT8811 TPC28T A/D_DOCK_IN
PT8812 TPC28T A/D_DOCK_IN
PT8810 TPC28T A/D_DOCK_IN
PT8813 TPC28T A/D_DOCK_IN
PT8816 TPC28T BAT
PT8817 TPC28T BAT
PT8818 TPC28T BAT
PT8819 TPC28T BAT
PT8820 TPC28T BATSEL_0
PT8821 TPC28T BATSEL_1
PT8822 TPC28T CHG_EN
PT8823 TPC28T AC_IN_OC#
PT8824 TPC28T ISET_EC
PT8825 TPC28T VSET_EC
PT8826 TPC28T PWRLIMIT#
PT8827 TPC28T GND
PT8831 TPC28T GND
PT8828 TPC28T GND
PT8829 TPC28T GND
PT8830 TPC28T GND
A/D_DOCK_IN
240mil
Modify 10/12
PQ8802 PMK35EP
P_CHG_PATH_19V_SHAPE
PC8804 0.1UF/25V c0603
P_CHG_SW_GATE
PR8805 1% 200KOhm
PR8804 100KOhm 1%
PR8803 100KOhm 1%
+3VAO
12.25
P_CHG_GATE_A
PQ8804A UM6K31N
P_CHG_GATE_B
PQ8804B UM6K31N
PR8802 10KOhm 1%
PSL8800 0402
PR8821 20mOHM 1%
PJ8801 @ SHORT_PIN
PJ8800 @ SHORT_PIN
AC_BAT_SYS
P_CHG_VCC_10
PR8800 130KOhm 1%
P_CHG_ACIN_10
ADP>=17.5V
PC8801 0.01UF/25V c0402 @
SGND_CHG
CLOSE TO VCC(PIN 1)
PC8800 0.1UF/25V c0603
PC8803 0.1UF/25V c0603
PR8801 10KOhm 1%
PC8802 0.01UF/25V c0402 @
P_CHG_CSSP_10
P_CHG_CSSN_10
PR8820 1% 1KOhm
P_CHG_INE3_R_10
P_CHG_INE3_10
P_CHG_INE3_C_10
PC8805 100PF/50V c0402
320mil
12.24
AC_BAT_SYS
EC8800 0.1UF/25V c0603 @
Modify 10/12
PQ8803 PMK35EP
PSL8803 0402
P_SEL_EN
PR8822 100KOhm 1%
PC8818 0.1UF/25V c0603
PC8817 10UF/25V c1206_h75
PC8816 10UF/25V c1206_h75
30 AC_IN_OC#
Total Power ADJ
CHG_VREF
PR8806 39KOHM
2.2
P_CHG_TOTALPWR_10
65W:PR8806=39Kohm
90W:PR8806=23.2Kohm
PR8807 20KOhm 1%
P_CHG_COMP1_R_10
PR8808 1% 1KOhm
P_CHG_COMP1_10
PC8806 0.01UF/16V c0402
PT8801 TPC28T
P_CHG_INE1_10
PU8800 MB39A132
P_CHG_CSIP_10
P_CHG_CSIN_10
P_CHG_COMP2_10
P_CHG_ISET_10
P_CHG_CB_20
P_CHG_HG_30
P_CHG_LX_30
P_CHG_VB_20
P_CHG_LG_30
PSL8802 0402
P_CHG_BST_20
PD8800 BAT54CW
PC8815 0.1UF/25V c0603
PR8819 0Ohm c0603_h24
160mil
PQ8800 EMB20N03V
PJ8806 @ SHORT_PIN
PL8800 6.8UH Irat=8A
P_CHG_RSENS_SHAPE
160mil
BAT
Charge Current ADJ
30 ISET_EC
PR8809 10KOhm 1%
PR8810 16.9KOhm 1%
PC8807 0.1UF/16V
PC8808 2200PF/50V c0402
P_CHG_OUTC3_10
PR8811 1% 10KOhm
PC8809 0.01UF/16V c0402 @
P_CHG_COMP3_10
PC8810 1000PF/50V c0402
P_CHG_COMP3_C_10
PR8812 1% 20KOhm
Modify 10/21
PC8814 1UF/16V c0603
PQ8801 EMB20N03V
PC8825 1000PF/50V c0603
P_CHG_SNB_S
PR8827 1Ohm r1206
PR8823 20mOHM 1%
PJ8803 @ SHORT_PIN
PJ8804 @ SHORT_PIN
PC8819 10UF/25V c1206_h75
PC8820 10UF/25V c1206_h75
P_CHG_CSIP_10
P_CHG_CSIN_10
P_CHG_BATT_10
PJ8805 @ SHORT_PIN
CLOSE TO Battery connet page.60
Charge Voltage ADJ
30 VSET_EC
PR8813 13.7KOhm 0.1%
PR8814 20KOhm 0.1%
P_CHG_ADJ3_10
CHG_VREF
PR8817 100KOhm 1%
P_CHG_CELLS
PR8818 100KOhm 1%
P_CELLS_SEL
PQ8805A UM6K1N
PQ8805B UM6K1N
CHG_EN 30
BATSEL_0 30
BATSEL_1 30
PRN8801A 100KOHM
PRN8801B 100KOHM
PRN8801C 100KOHM
Modify 10/27
PJ8802 @ SHORT_PIN
PR8815 0.1% 10KOhm
PC8811 0.1UF/16V
PR8816 30KOHM 1%
Fsw=515KHz
PC8812 0.1UF/16V
PC8813 0.1UF/25V c0603
CLOSE TO VIN(PIN 24)
12.22
2.2
+5VSUS
PR8829 @ 0Ohm
+3VA
PR8824 100KOhm 1%
PR8830 10KOhm 1%
PU8801 LMV321IDBVR
P_CHG_INE1_10
(1.65V)
P_CHG_REFIN
P_CHG_PWRLIMIT
PD8801 BAT54CW
P_CHG_PWRLIMIT_EN
PQ8806 2N7002
PR8828 @ 0Ohm
PWRLIMIT# 5,30
PC8821 0.1UF/16V
PR8825 100KOhm 1%
PC8822 0.1UF/16V
PR8826 100KOhm 1%
PC8823 0.1UF/16V
PC8824 4.7UF/6.3V
Total count: 50 pcs
Battery Cells
BATSEL_1 | BATSEL_0 | CELLS
H | H | 2 CELLS
L | H | 2 CELLS
H | L | 3 CELLS
L | L | 4 CELLS
Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202
ASUSTeK COMPUTER INC. NB3
Title : CHARGER_202
Engineer: Matt_Wang
Size Custom
Project Name Design_IP
Rev 1.0
Date: Monday, February 08, 2010
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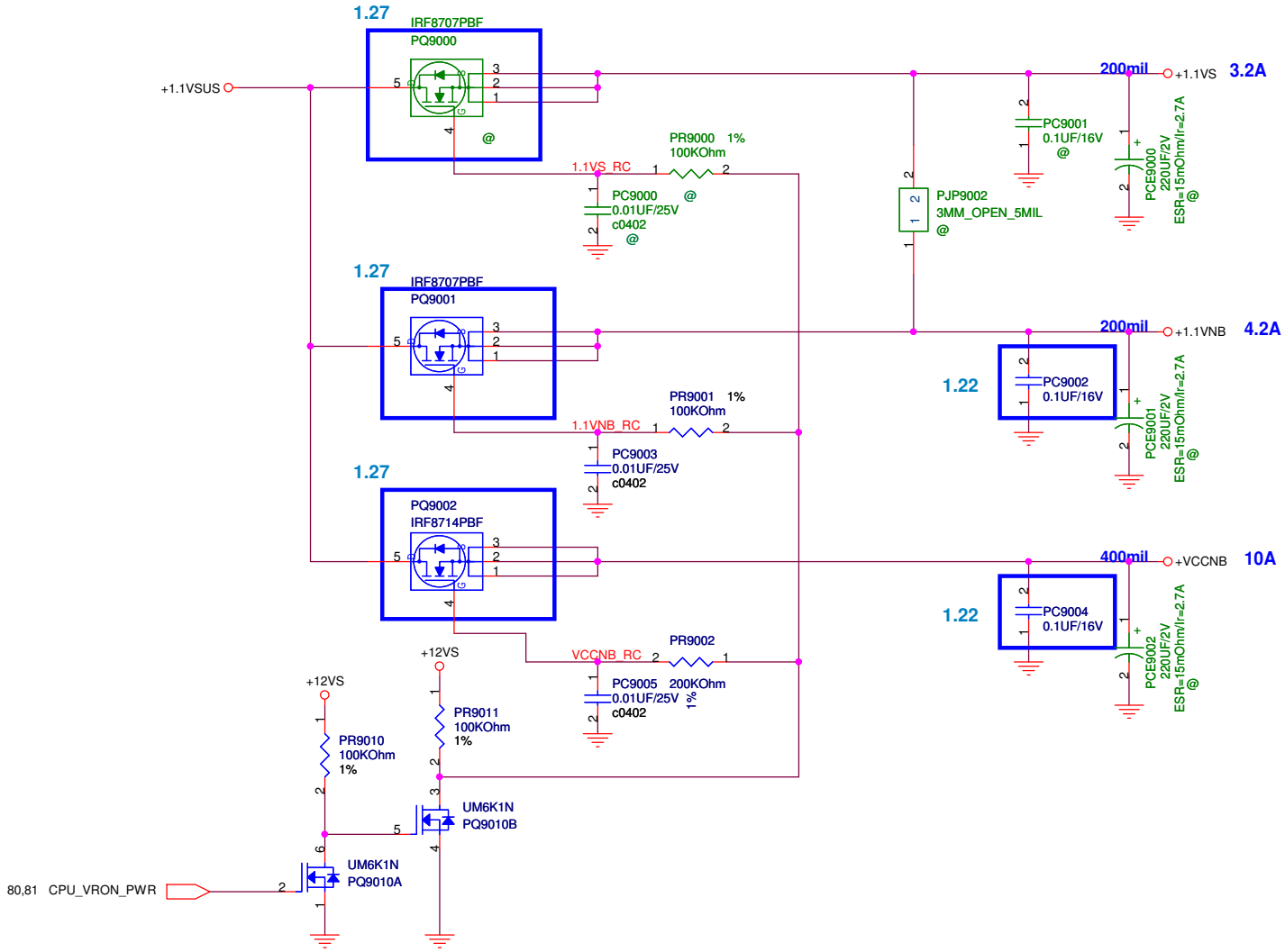

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
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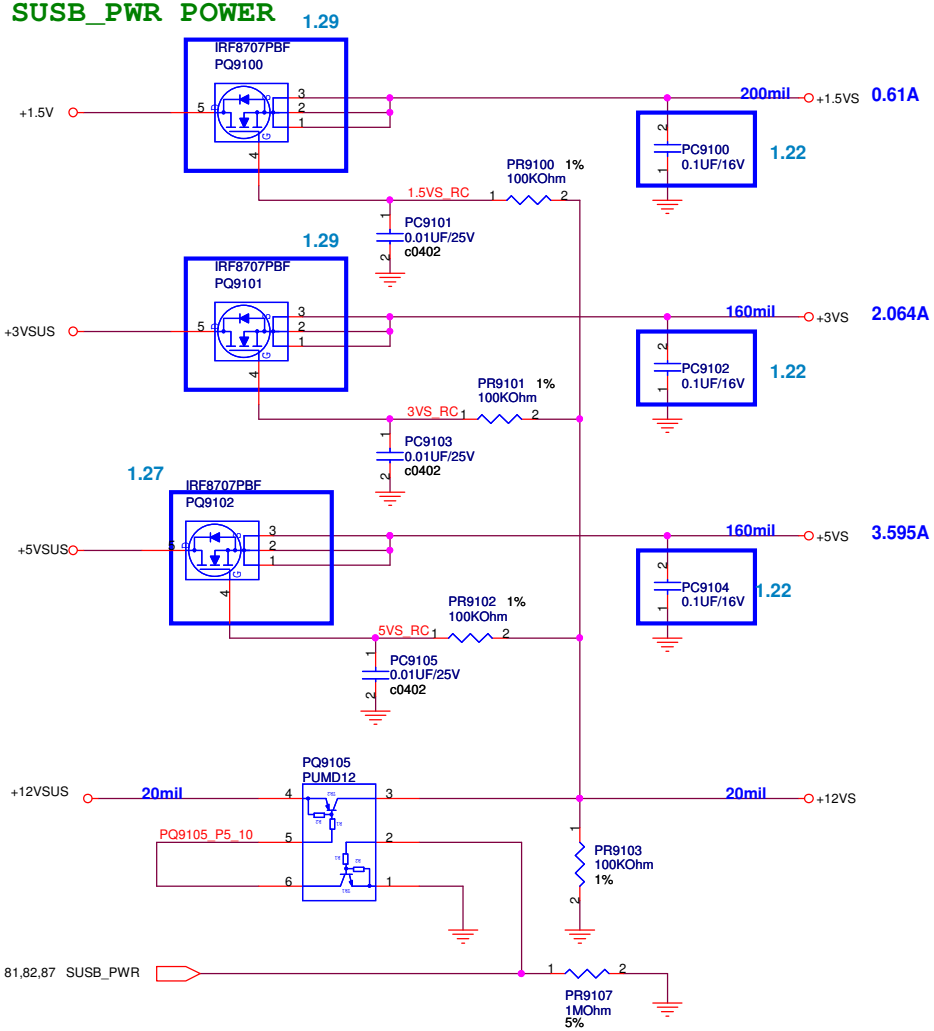

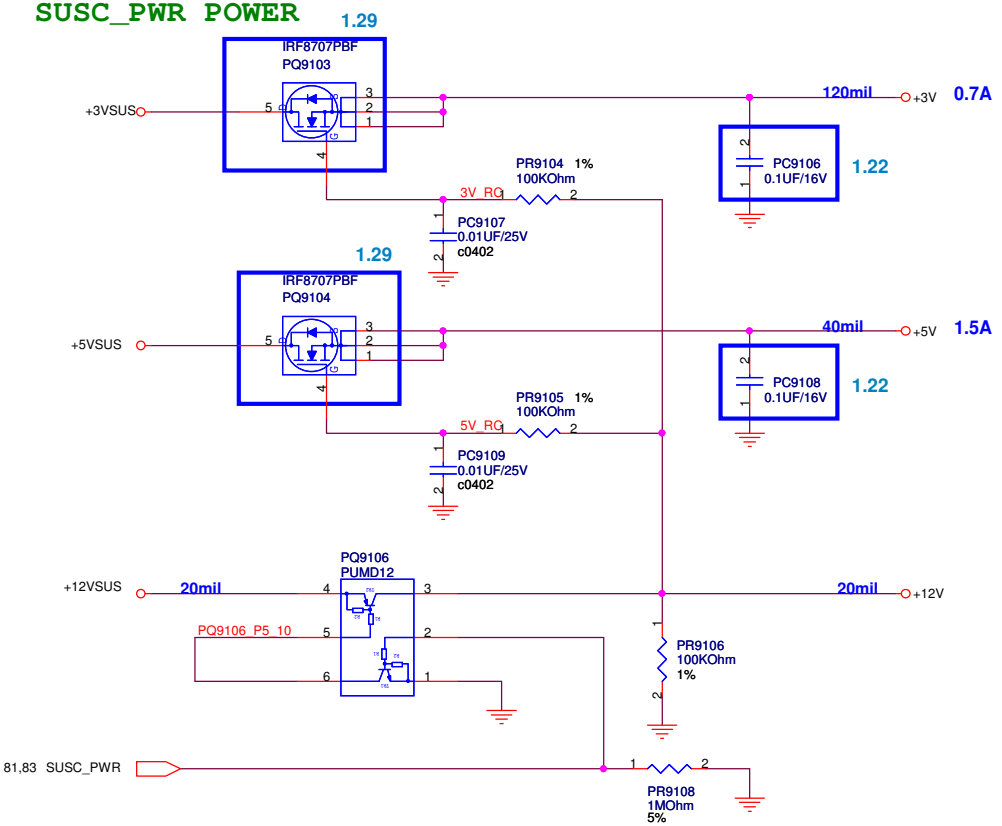

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_LOAD SWITCH

Engineer: Matt_Wang

Size	Project Name	Rev
B	Design_IP	1.0

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