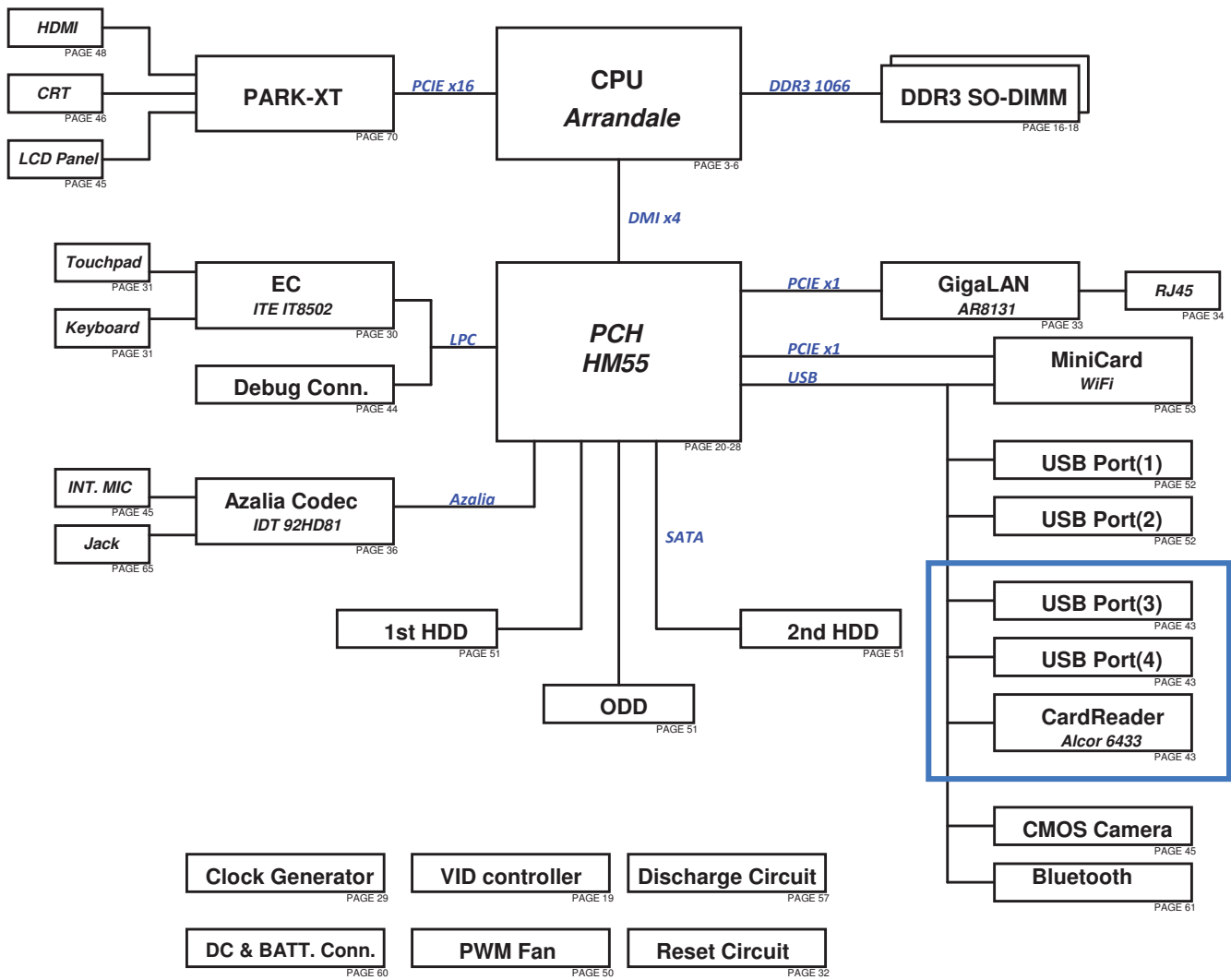


PAGE	Content
1	Block Diagram
2	System Setting
3	CPU(1)_DMI, PEG, FDI, CLK, MISC
4	CPU(2)_DDR3
5	CPU(3)_CFG, RSVD, GND
6	CPU(4)_PWR
7	CPU(5)_XDP
16	DDR3 SO-DIMM_0
17	DDR3 SO-DIMM_1
18	DDR3 CA_DQ VOLTAGE
19	VID controller
20	PCH_IBEX(1)SATA, IHDA, RTC, LPC
21	PCH_IBEX(2)_PCIE, CLK, SMB, PEG
22	PCH_IBEX(3)_FDI, DMI, SYS PWR
23	PCH_IBEX(4)_DP, LVDS, CRT
24	PCH_IBEX(5)_PCI, NVRAM, USB
25	PCH_IBEX(6)CPU, GPIO, MISC
26	PCH_IBEX(7)_POWER, GND
27	PCH_IBEX(8)_POWER, GND
28	PCH_SPI ROM, OTH
29	CLK_ICS9LPR362
30	EC_IT8541(1/2)
31	EC_IT8541(2/2)KB, TP
32	RST_Reset Circuit
33	HANKSVILLE
34	LAN_RJ45
36	CODEC-ALC269
37	AUD_Amp & Jack
40	CB_R5C833
41	CB_R5C833
42	CB_4in1 CardReader
43	CB_NewCard
44	BUG_Debug
45	CRT_LCD Panel
46	CRT_D-Sub
48	TV_HDMI
50	FAN_Fan & Sensor
51	XDD_HDD & ODD
52	USB_USB Port *2
53	MINICARD(WLAN)
56	LED_Indicator
57	DSG_Discharge
60	DC_DC & BAT Conn.
61	BT_Bluetooth
65	ME_Conn & Skew Hole
67	PCH_XDP, ONFI
70	VGA_M96 Main (1)
71	VGA_M96 Main (2)
72	VGA_M96 MEM CHANNEL A
73	VGA_M96 MEM CHANNEL B
74	VGA_M96 Power (1)
75	VGA_M96 Power (2)
76	VGA_M96 THERMAL/Memory SS
77	VGA_M96 Straps
78	VGA_POWER_VGA_CORE & RAM
79	VGA_POWER_VGA_+1.2VS_+1.1VS
80	PW_VCORE(MAX17034)
81	PW_SYSTEM(MAX17020)
82	PW_I/O_VTT_CPU&+1.1VM
83	PW_I/O_DDR & VTT& +1.8VS
84	PW_I/O_3VM & ME_+VM_PWEGD
86	PW_+VGFX_CORE(MAX17028)
88	PW_CHARGER(MAX17015)
90	PW_DETECT
91	PW_LOAD SWITCH
92	PW_PROTECT
93	PW_SIGNAL
94	PW_FLOWCHART

K72JK Schematic R2.0



- Power**
- VCORE** Page 80
- System** Page 81
- 1.5VS & 1.05VS** Page 82
- DDR & VTT** Page 83
- +2.5VS** Page 84
- Charger** Page 86
- Detect** Page 90
- Load Switch** Page 91
- Power Protect** Page 92

Daughter Board

PCH GPIO	Usage	Signal Name	Pull Up / Pull Down	Power
GPIO 00	GPO			+3VS
GPIO 01	GPO		INT PU 20K	+3VS
GPIO [02:05]	Native	PCI_INT[E:H]#	EXT PU 10K	+5VS
GPIO 06	GPO		INT PU 20K	+3VS
GPIO 07	GPO		INT PU 20K	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC#5	EXT PU 10K	+3VSUS
GPIO 10	Native	USB_OC#6	EXT PU 10K	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU 10K	+3VSUS
GPIO 12	GPO			+3VSUS
GPIO 13	GPO		INT PD 20K	+3VSUS
GPIO 14	GPO	USB_OC#7	EXT PU 10K	+3VSUS
GPIO 15	GPO	BT_LED	INT PD 20K	+3VSUS
GPIO 16	GPO		EXT PU 10K	+3VS
GPIO 17	GPO		INT PU 20K	+3VS
GPIO 18	Native	CLKREQ1#	EXT PU 10K	+3VS
GPIO 19	Native	SATA1GP	EXT PU 10K	+3VS
GPIO 20	Native	CLKREQ2#	EXT PD 10K	+3VS
GPIO 21	Native	SATA0GP	EXT PU 10K	+3VS
GPIO 22	GPO	WLAN_LED		+3VS
GPIO 23	GPO		INT PU 20K	+3VS
GPIO 24	GPO			+3VSUS
GPIO 25	Native	CLKREQ3#	EXT PU 10K	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU 10K	+3VSUS
GPIO 27	GPO		INT PU 20K	+3VSUS
GPIO 28	GPO	WLAN_ON#	INT PU 20K	+3VSUS
GPIO 29	GPO			+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU 10K	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU 10K	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU 10K	+3VS
GPIO 33	GPI	PCH_SPI_OV	INT PU 20K	+3VS
GPIO 34	Native	STP_PCI#		+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PD 10K	+3VS
GPIO 36	GPO		EXT PU 10K	+3VS
GPIO 37	GPO		EXT PU 10K	+3VS
GPIO 38	GPI	PCB_ID0	EXT PU/PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PU/PD	+3VS
GPIO 40	Native	USB_OC#1	EXT PU 10K	+3VSUS
GPIO 41	Native	USB_OC#2	EXT PU 10K	+3VSUS
GPIO 42	Native	USB_OC#3	EXT PU 10K	+3VSUS
GPIO 43	Native	USB_OC#4	EXT PU 10K	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU 10K	+3VSUS
GPIO 45	Native	CLK_REQ6#	INT & EXT PU	+3VSUS
GPIO 46	GPO			+3VSUS
GPIO 47	Native	CLKREQ_PEG#A	EXT PD 10K	+3VSUS
GPIO 48	GPO			+3VS
GPIO 49	Native	TEMP_ALERT#	EXT PU 10K	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU 10K	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU 20K	+3VS
GPIO 52	Native	PCI_REQ2#	EXT PU 10K	+5VS
GPIO 53	Native	PCI_GNT2#	INT PU 20K	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PU 10K	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU 20K	+3VS
GPIO 56	Native	CLKREQ_PEG#B	EXT PU 10K	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU 10K	+3VSUS
GPIO 59	Native	USB_OC#0	EXT PU 10K	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU 10K	+3VSUS
GPIO 61	Native	SUS_STAT#		+3VSUS
GPIO 62	Native	SUSCLK		+3VSUS
GPIO 63	Native	SLP_S5#		+3VSUS
GPIO 64	Native	CLK_OUT0	INT PD 20K	+3VS
GPIO 65	Native	CLK_OUT1	INT PD 20K	+3VS
GPIO 66	Native	CLK_OUT2	INT PD 20K	+3VS
GPIO 67	Native	CLK_CARD_READER_48	INT PD 20K	+3VS
GPIO 72	Native	PM_BATLOW#	INT PU 20K	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU 10K	+3VSUS
GPIO 74	Native	SML1ALERT#	EXT PU 10K	+3VSUS
GPIO 75	Native	SML1_DATA	EXT PU 10K	+3VSUS

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	CHG_LED#
GPA2		CHG_FULL_LED#
GPA3		-
GPA4	0	LCD_BL_PWM
GPA5	0	FAN0_PWM
GPA6		-
GPA7		-
GPB0	0	BATSEL_0
GPB1	0	BATSEL_1
GPB2		ME_AC_PRESENT_EC
GPB3	I0	SMB0_CLK
GPB4	I0	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RCIN#
GPB7	0	PM_RSMRST#
GPC0		-
GPC1	I0	SMB1_CLK
GPC2	I0	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	0	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	-
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		SD_CD#_EC
GPE0	0	VSUS_ON
GPE1	0	-
GPE2	0	-
GPE3	0	-
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0	0	-
GPF1		-
GPF2	I	-
GPF3		-
GPF4	I	TP_CLK
GPF5	I0	TP_DAT
GPF6	0	THRO_CPU
GPF7		PCH_SPI_OV
GPG0		ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2	0	OCMV_CTL0
GPG6	0	OCMV_CTL1
GPH0	I0	PM_CLKRUN#
GPH1	0	-
GPH2	0	CHG_EN
GPH3	0	SUSC_EC#
GPH4	0	SUSB_EC#
GPH5	0	NUM_LED#
GPH6	0	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	-
GPI6	I	-
GPI7	I	-
GPJ0	0	CPU_VRON
GPJ1	0	PM_PWROK
GPJ2	0	VSET_EC
GPJ3	0	ISET_EC
GPJ4	0	-
GPJ5		-

EC GPIO	Use As	Signal Name
GPI00	I	
GPI01	I	
GPI02		-
GPI03		-
GPI04	I	
GPI05	I	
GPI06	0	
GPI07		-
GPI08		-
GPI09		
GPI010		-
GPI011		-
GPI012	0	
GPI013		-
GPI014	0	
GPI015		-
GPI016		-
GPI017		-
GPI018		-
GPI019		-
GPI020		-
GPI021		-
GPI022		-
GPI023		-
GPI024		-
GPI025		-
GPI026		-
GPI027		-
GPI028		-
GPI029		-
GPI030		-
GPI031		-
GPI032		-
GPI033		-
GPI034		-
GPI035		-
GPI036		-
GPI037		-

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
Clock Generator(ICS9LRS3162)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
EC Master (SMB1)		
SM-Bus Device	SM-Bus Address	
CPU Thermal Sensor(G781)	1001100x (98)	
VGA Thermal IC(G781-1)	1001101x (9A)	

Device Identification

CPU Thermal Sensor P/N:			component name
1st	06G023048011		G781F
S			
S			
S			
Clock Gen P/N:			component name
1st	06G011610010		ICS9LRS3162
S			
S			
VGA Thermal Sensor			component name
1st	06G023048020		G781-1
S			
S			

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	

	K72J
0	USB port
1	USB port
2	USB port (D/B)
3	USB port (D/B)
4	
5	MiniCard (Full)
6	
7	
8	MiniCard (Half)
9	Camera
10	
11	Card Reader
12	Bluetooth
13	

FDI disable: (For discrete graphic)

1. NC:

FDI_TX#[0:7], FDI_RX#[0:7], FDI_RX#[0:7], FDI_RX#[0:7]
VCC_AXGSENSE, VSS_AXGSENSE

2. Pull-down to GND via 1KΩ ± 5% resistor:

FDI_FSYNC[0:1], FDI_LSYNC[0:1], FDI_INT, GFX_IMON
~15mW power saving. (DG R0.8 P.70)

3. Connected to GND:

VCCAXG,

4. Can be connected to GND directly:

DPLL_REF_CLK, DPLL_REF_CLK#

5. Connect to +V1.05S rail:

VCCFDIPLL



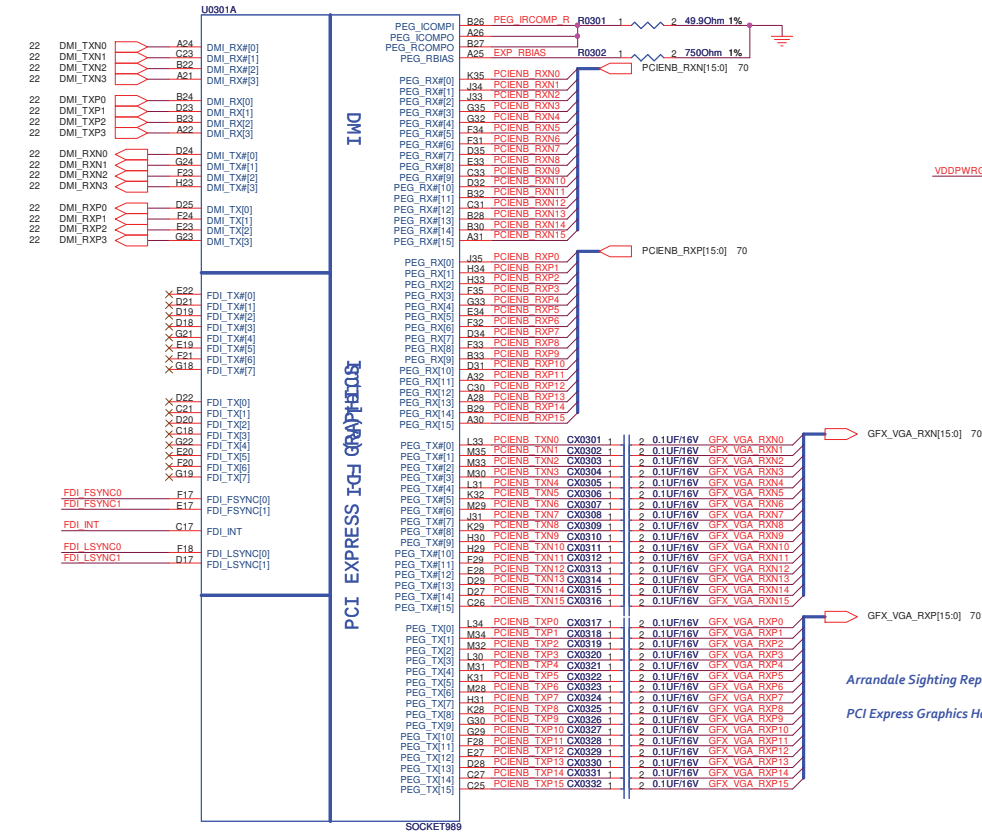
DG R1.1 P.83:

*FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1]
can be ganged together with one resistor.

*On the other hand, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],
FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as
no connect without any power or functional impact.

Arrandale Sighting Report :

System May Hang With DMI L1 Enabled.



Arrandale Sighting Report :

PCI Express Graphics Hang With L1 Enabled in Rare Cases.

CPU Socket : 12G011909890

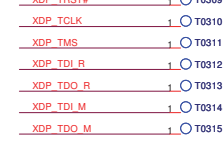
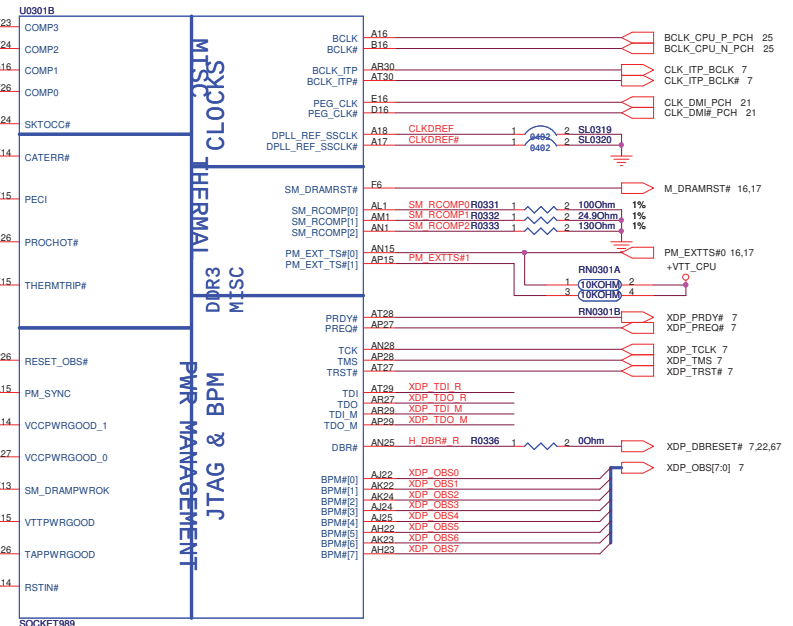
Molex : 12G011909891

Tape & Reel : 12G011909893

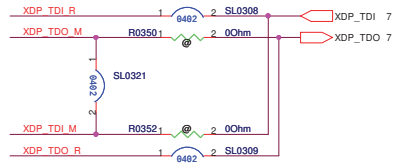
For CPU Boundary Scan

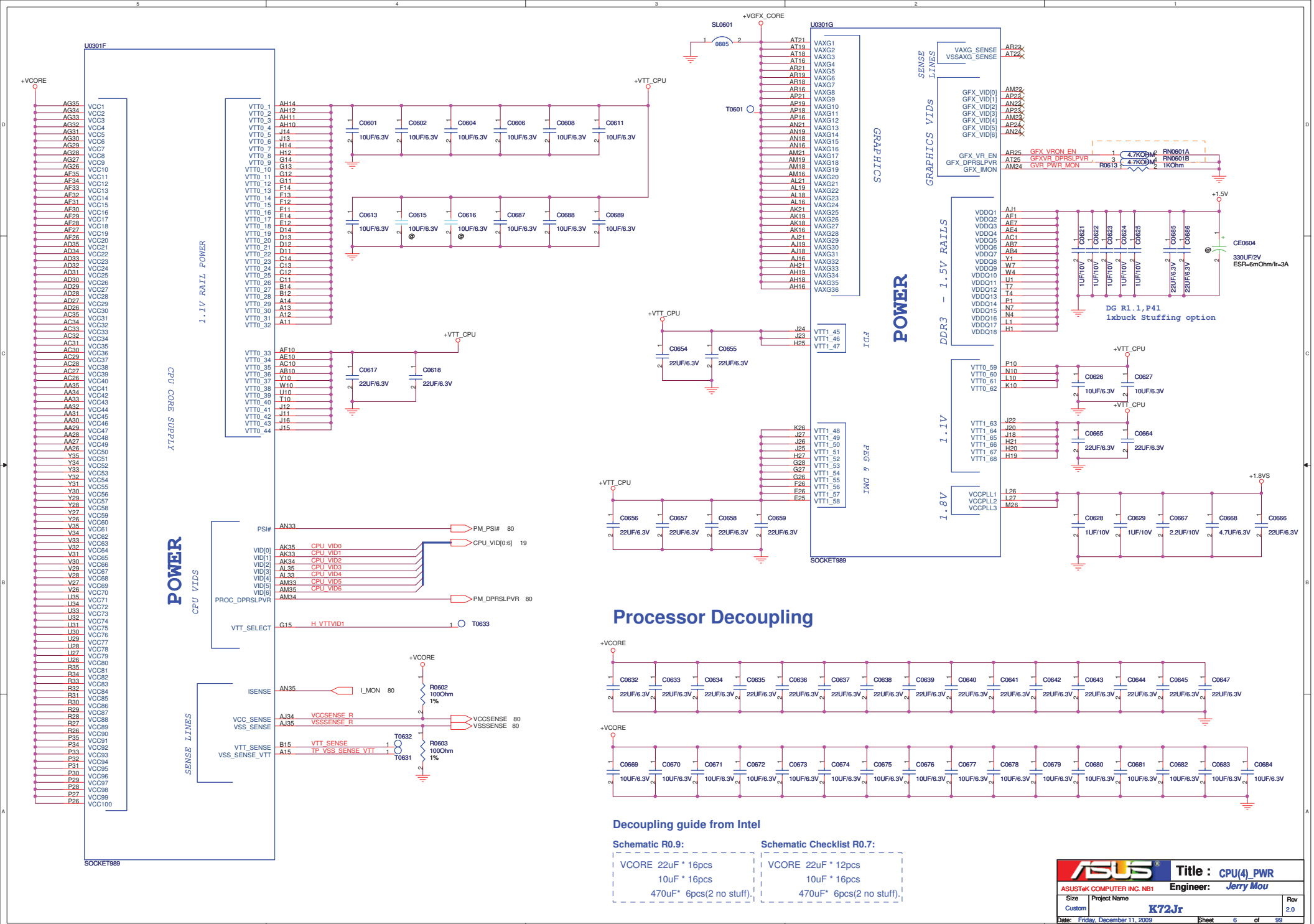
DG R1.1 P.109:

*On Clarkfield rPGA only designs, VCCPWGOOD_1 on the
Clarkfield processor can be left as No Connect.

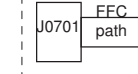
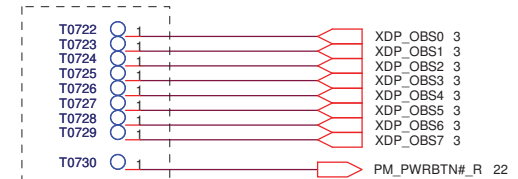
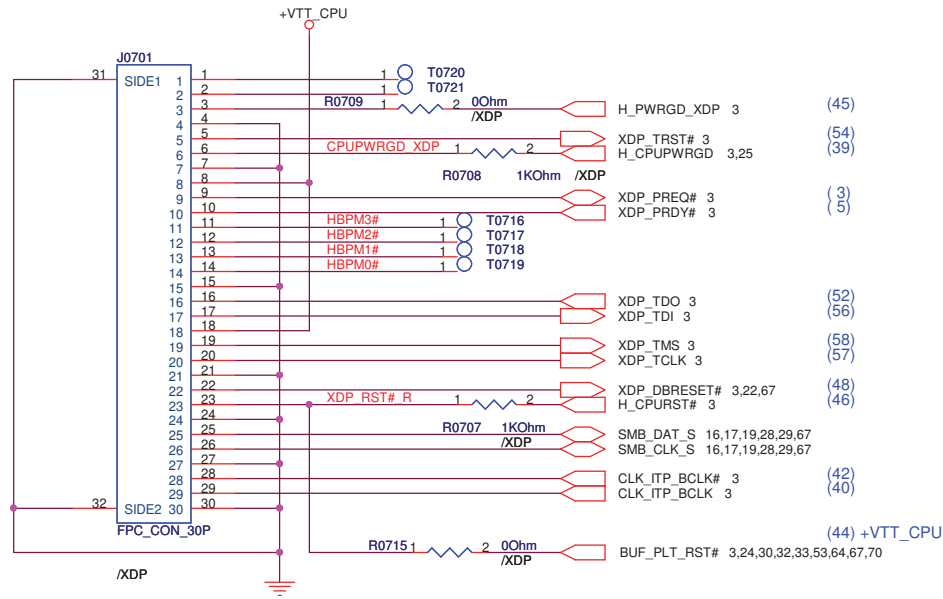


JTAG MAPPING



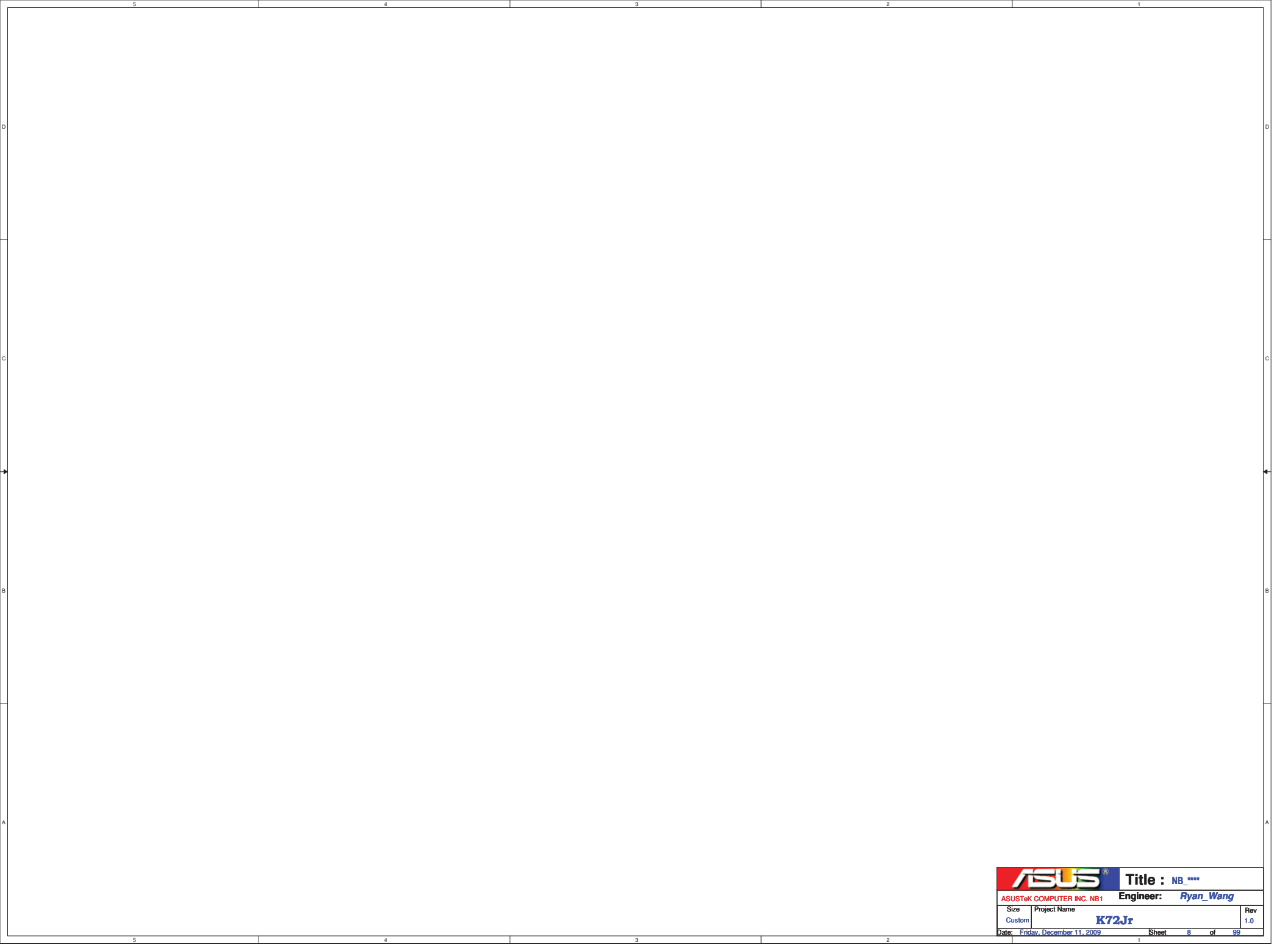


CPU XDP connector

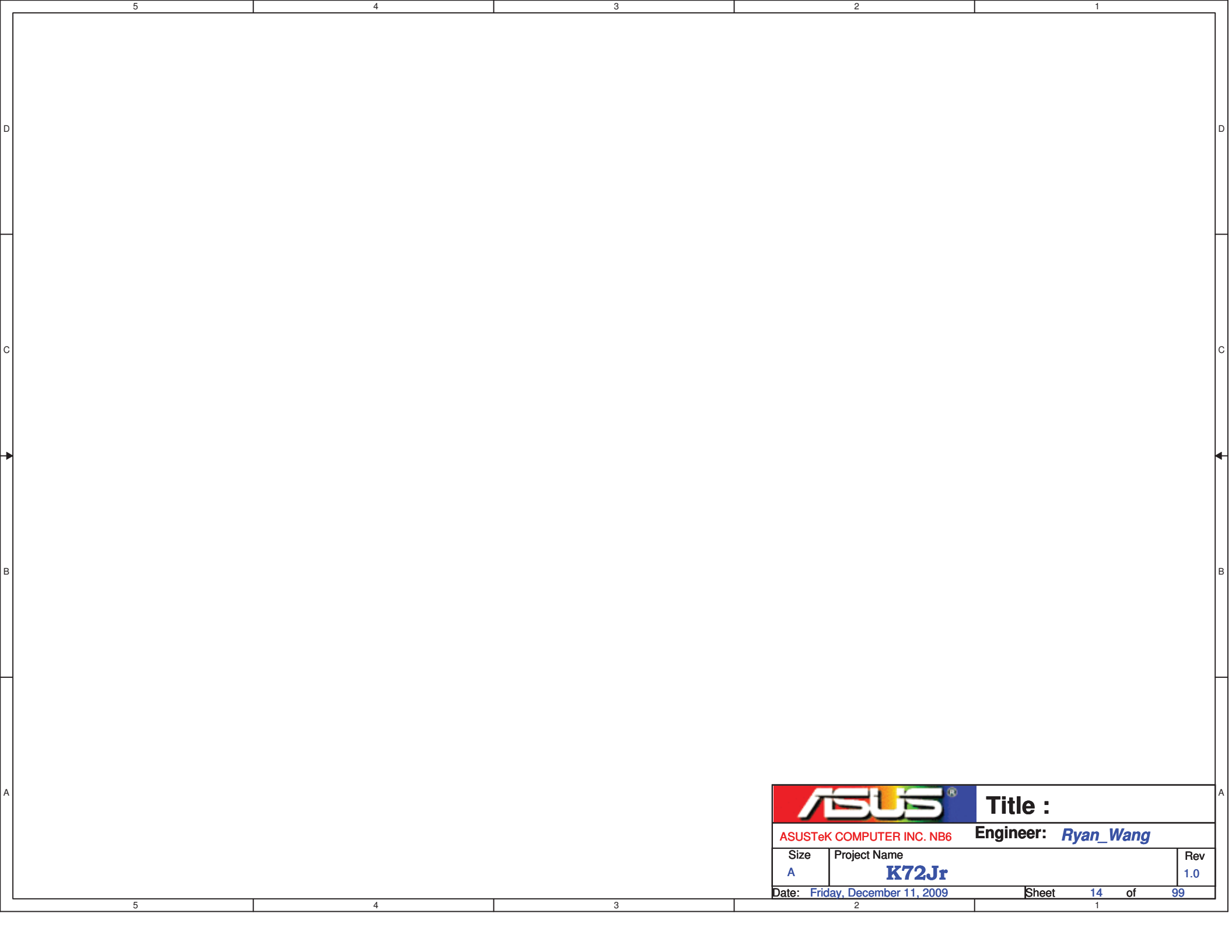


Put these test point near J0701.

Put it away from the FFC path.



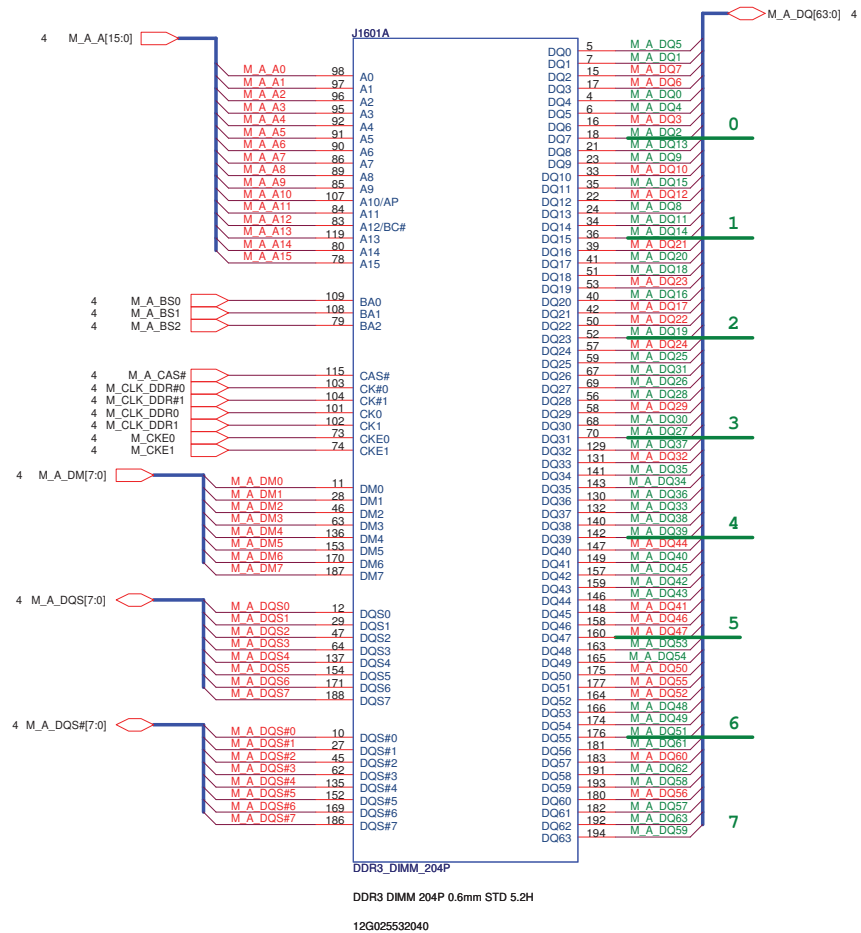
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ASUSTeK COMPUTER INC. NB1		Engineer: <i>Ryan_Wang</i>	
Size	Project Name		Rev
Custom	K72Jr		1.0
Date: Friday, December 11, 2009		Sheet	8 of 99



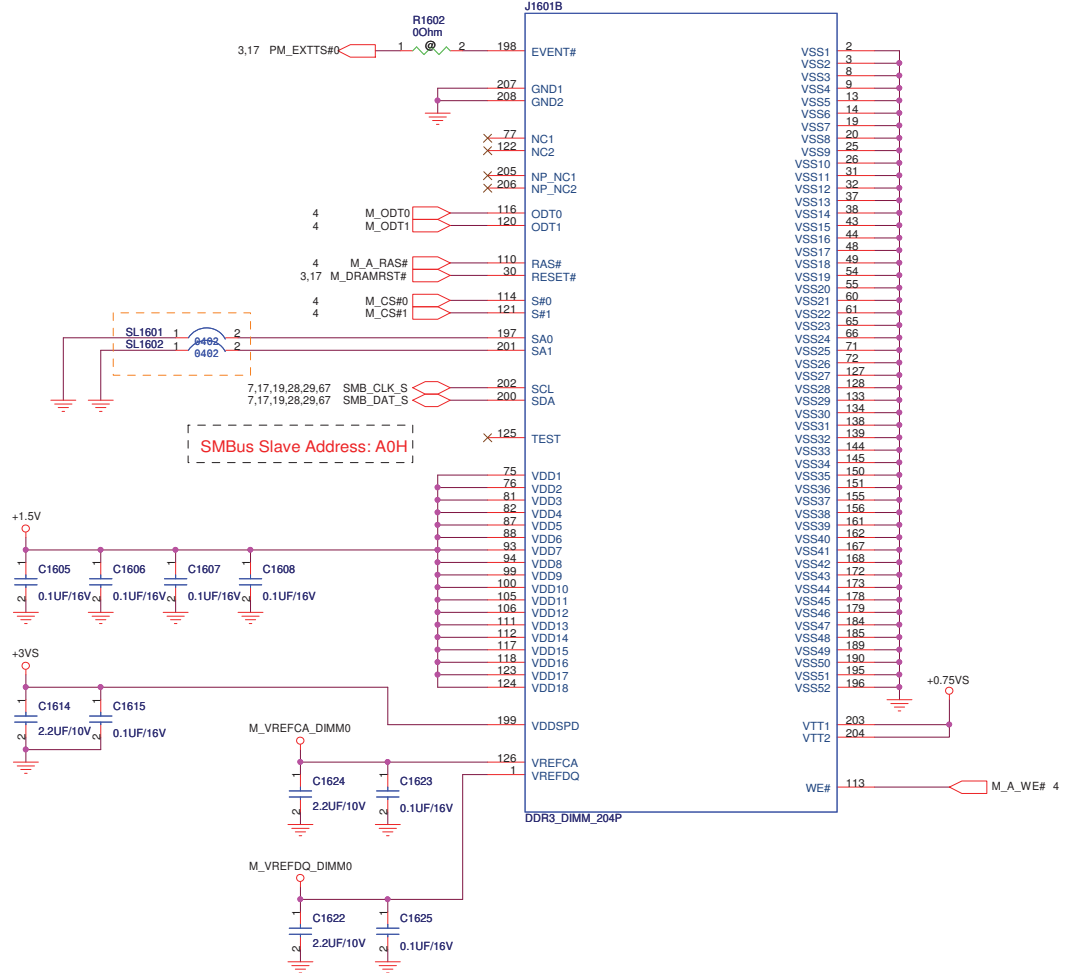
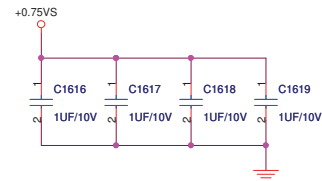
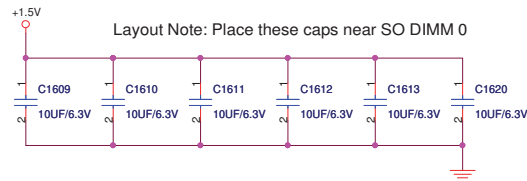
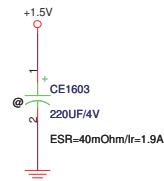
		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>Ryan_Wang</i>	
Size A	Project Name K72Jr		Rev 1.0
Date: <i>Friday, December 11, 2009</i>		Sheet	14 of 99

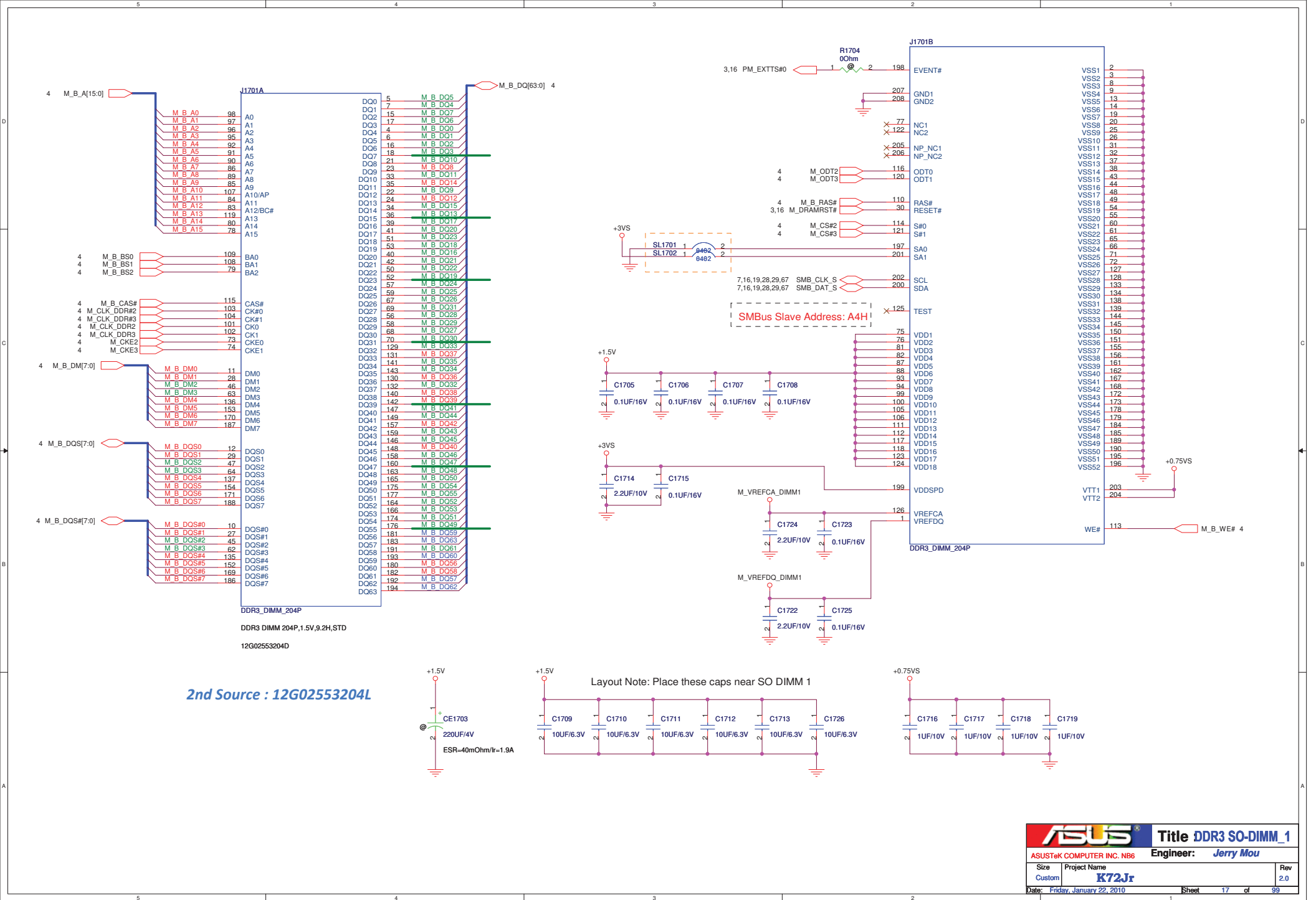
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>Ryan_Wang</i>	
Size A	Project Name K72Jr		Rev 1.0
Date: <i>Friday, December 11, 2009</i>		Sheet	15 of 99



Tyco new P/N : 12G02553204G
2nd Source : 12G02553204K

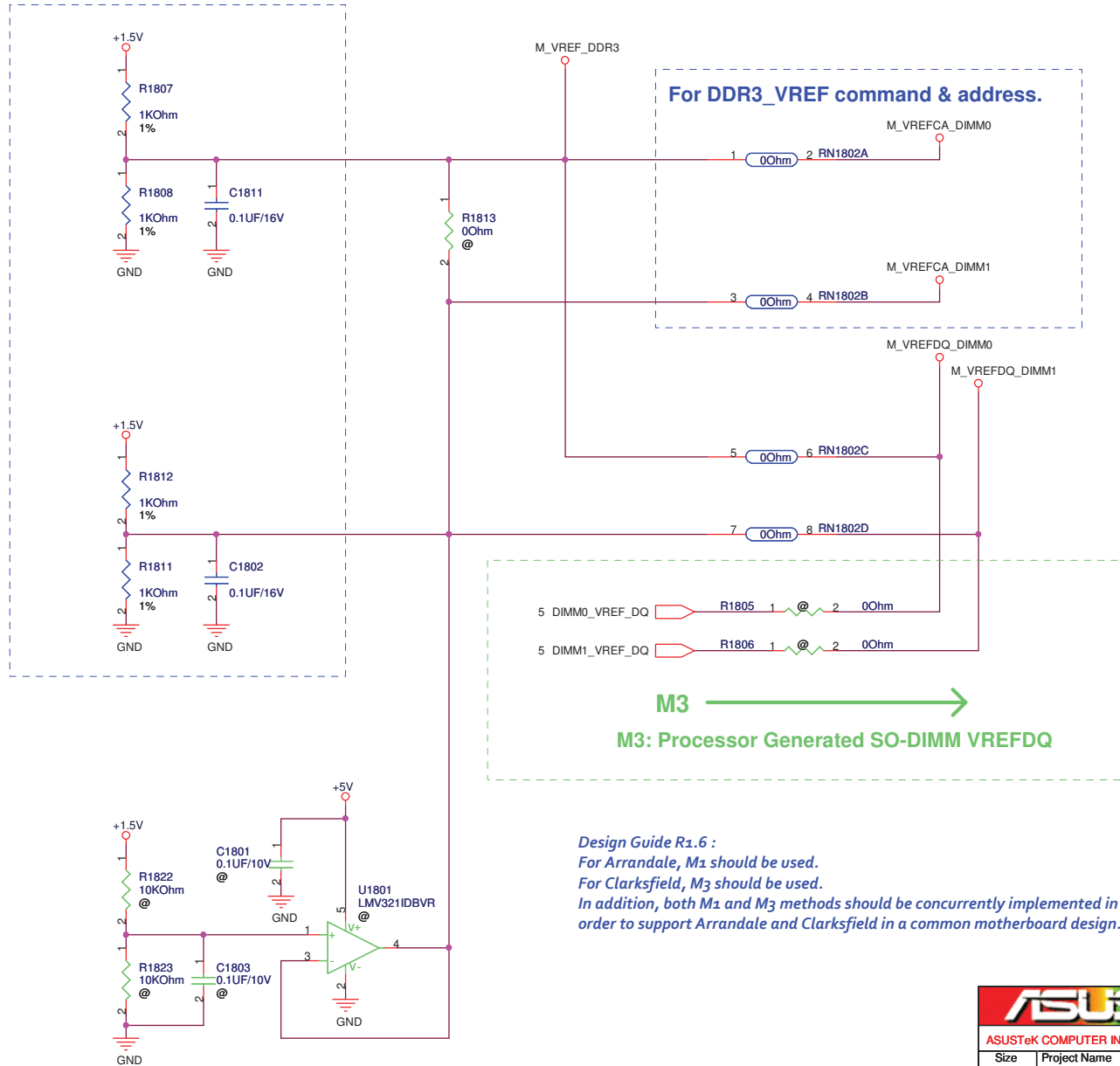


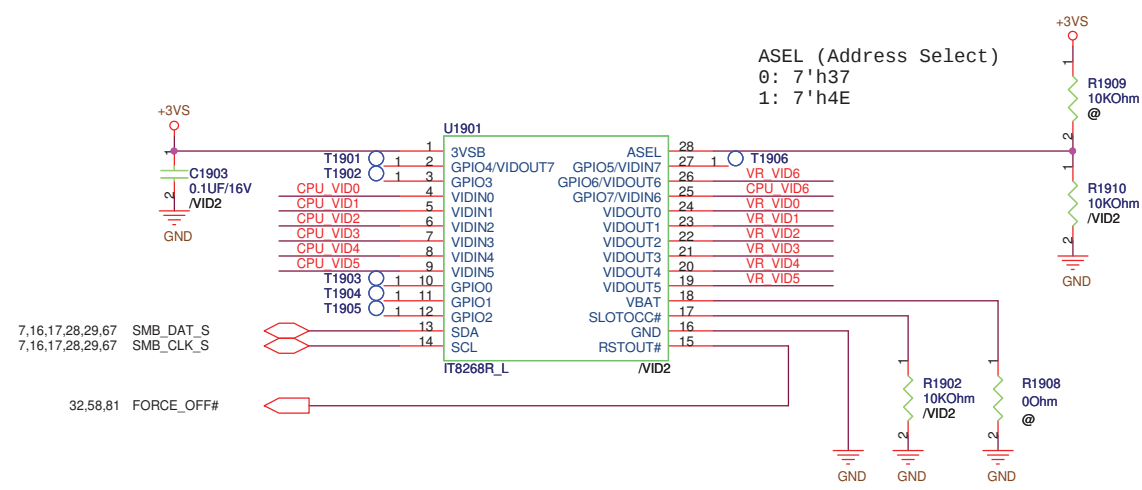
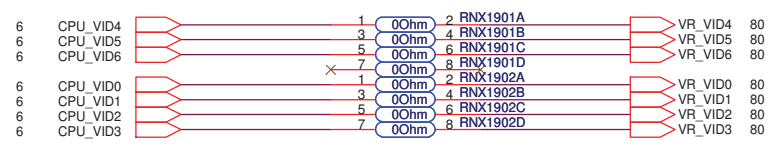


Default M1 

DDR3 Vref

Intel Document Number: 400755

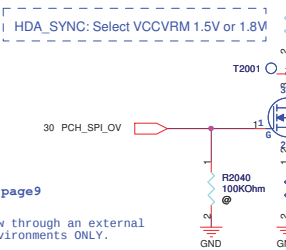
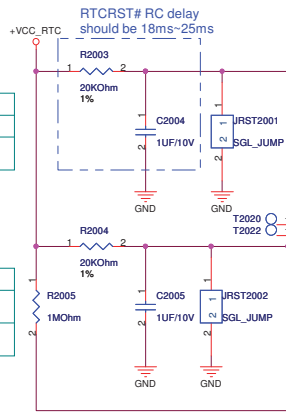




ASEL (Address Select)
 0: 7'h37
 1: 7'h4E

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

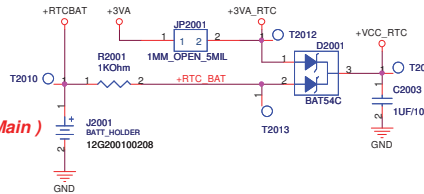
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



414044 Design Guide R1.11 Update: page9

GPIO33:
This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

Without connecting GPIO33, customers may not be able to override SPI flash contents.



12G20010020J (Main)

Strap information:

HDA_SPKR: No reboot strap
Low: Disable.
High: Enable

HDA_DOCK_EN#:
1. Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2. GPIO33 low on the rising edge of PWROK,
Will also disable Intel ME.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)

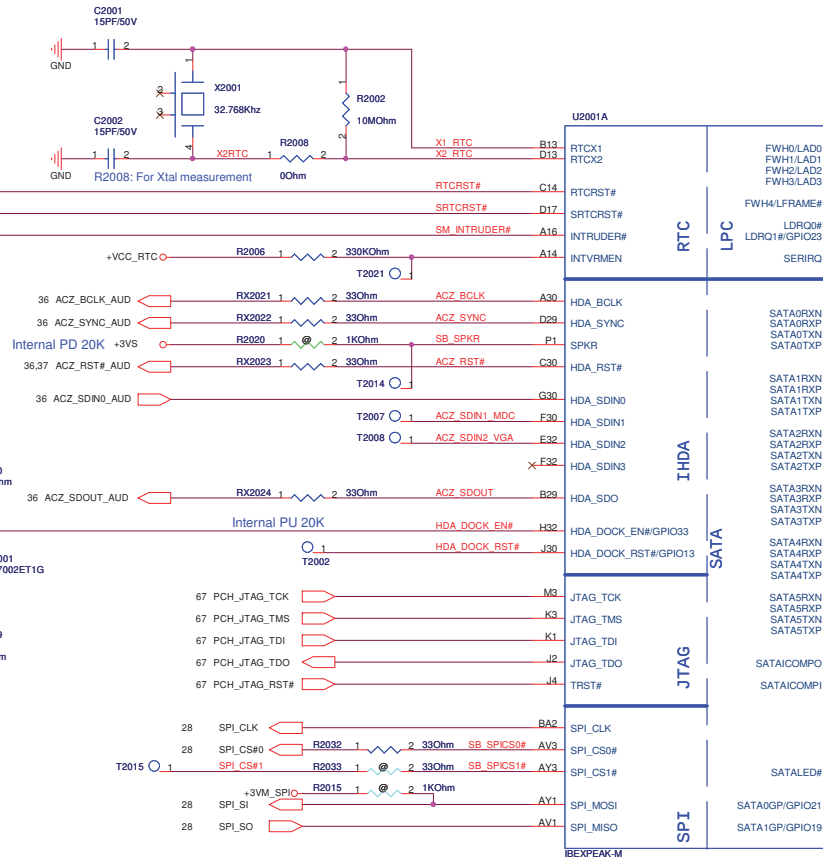
MoW 11, 2009 :

Ibex peak JTAG and Ibex Peak Test Interface requirements

For pre-production systems, please refer to the latest Calpella Platform Debug Port Design Guide (Doc #385422)

		Pre-Production Systems	Production Systems
PCH Pin	RefDes	ES1	ES2
TDO	R1	No Stff	200 Ohms
	R2	No Stff	100 Ohms
	R3	200 Ohms	200 Ohms
TMS	R4	100 Ohms	100 Ohms
	R5	200 Ohms	200 Ohms
TDI	R6	100 Ohms	100 Ohms
TCK	R7	51 Ohms	51 Ohms
	R8	20K Ohms	Not Applicable ¹
		10K Ohms	Not Applicable ¹
TRST#	R9		Not Applicable ¹

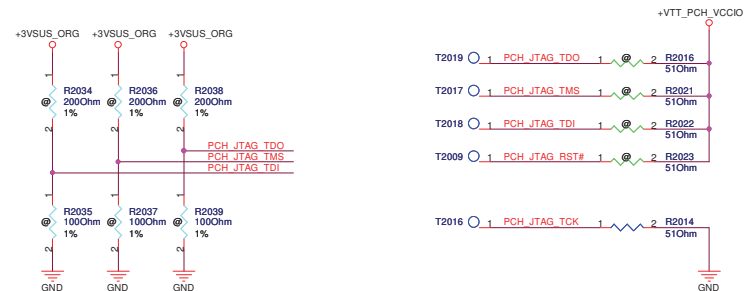
Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes



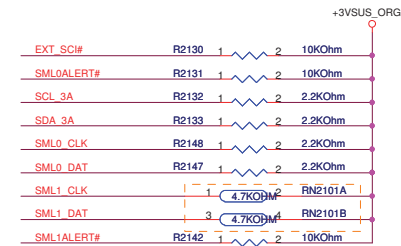
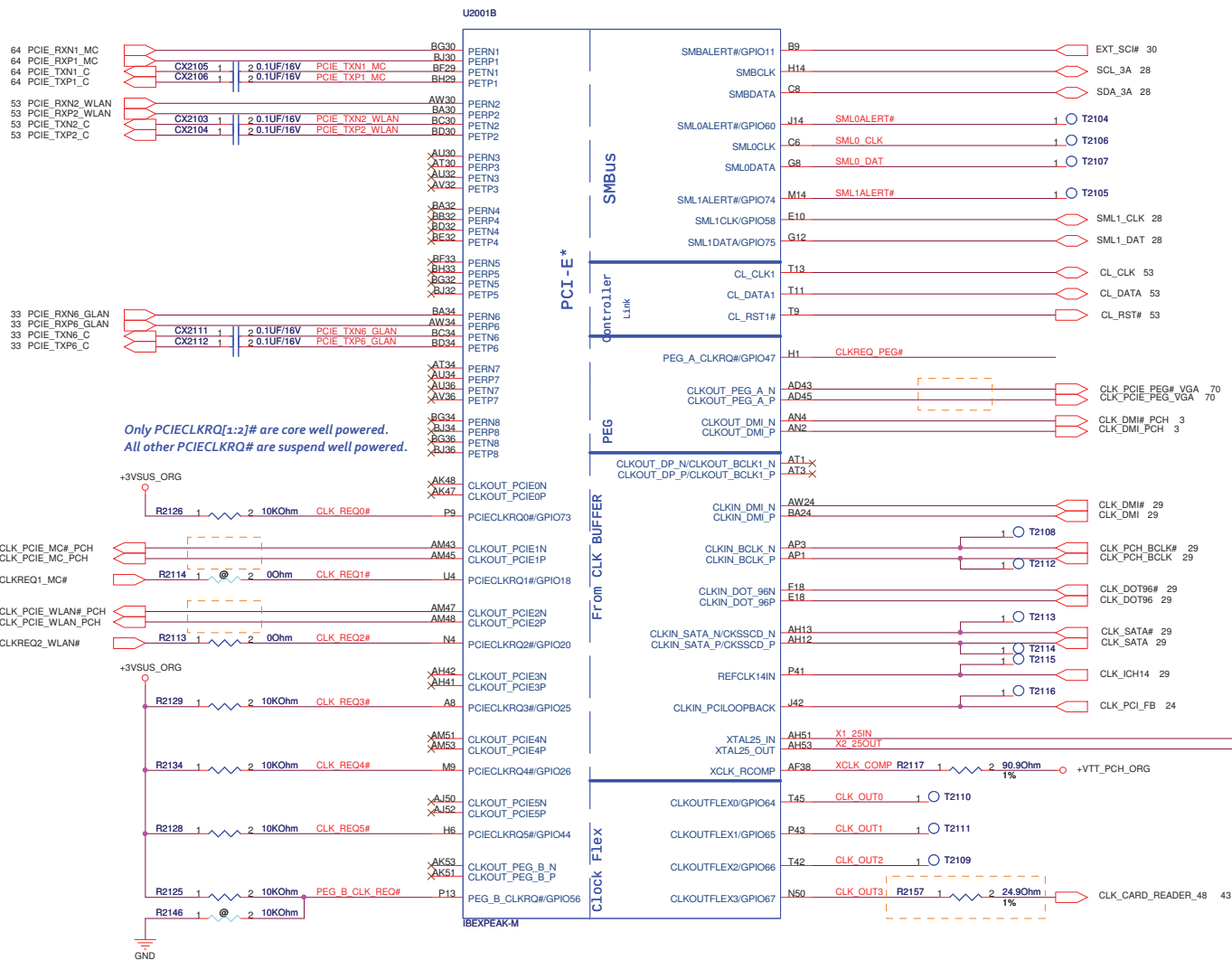
02G010026101

C.S BD82HM55 904127

GA INT IBEXPEAK HM55

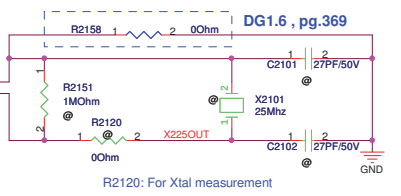
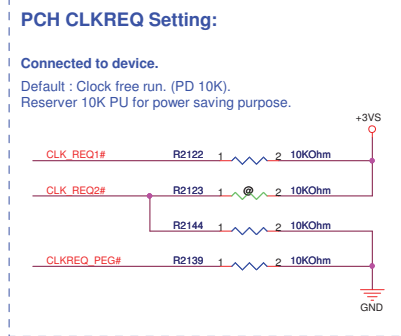


ASUS		Title : PCH - SATA, HDA	
ASUSTek COMPUTER INC. N96		Engineer: Jerry Mou	
Size	Project Name		Rev
Custom	K72Jr		2.0
Date:	Fri, Dec 11, 2009	Sheet	20 of 99

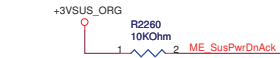


DG R1.1,page 43:

The pull-up resistor value for SML0DATA and SML0CLK has been updated from 4.7 K $\pm 5\%$ to 2.2 K $\pm 5\%$ to support 400-kHz bus speed



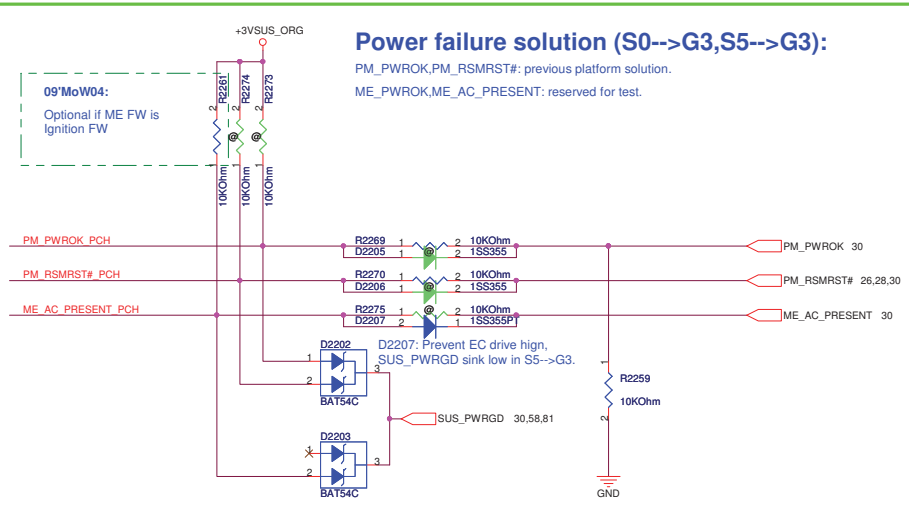
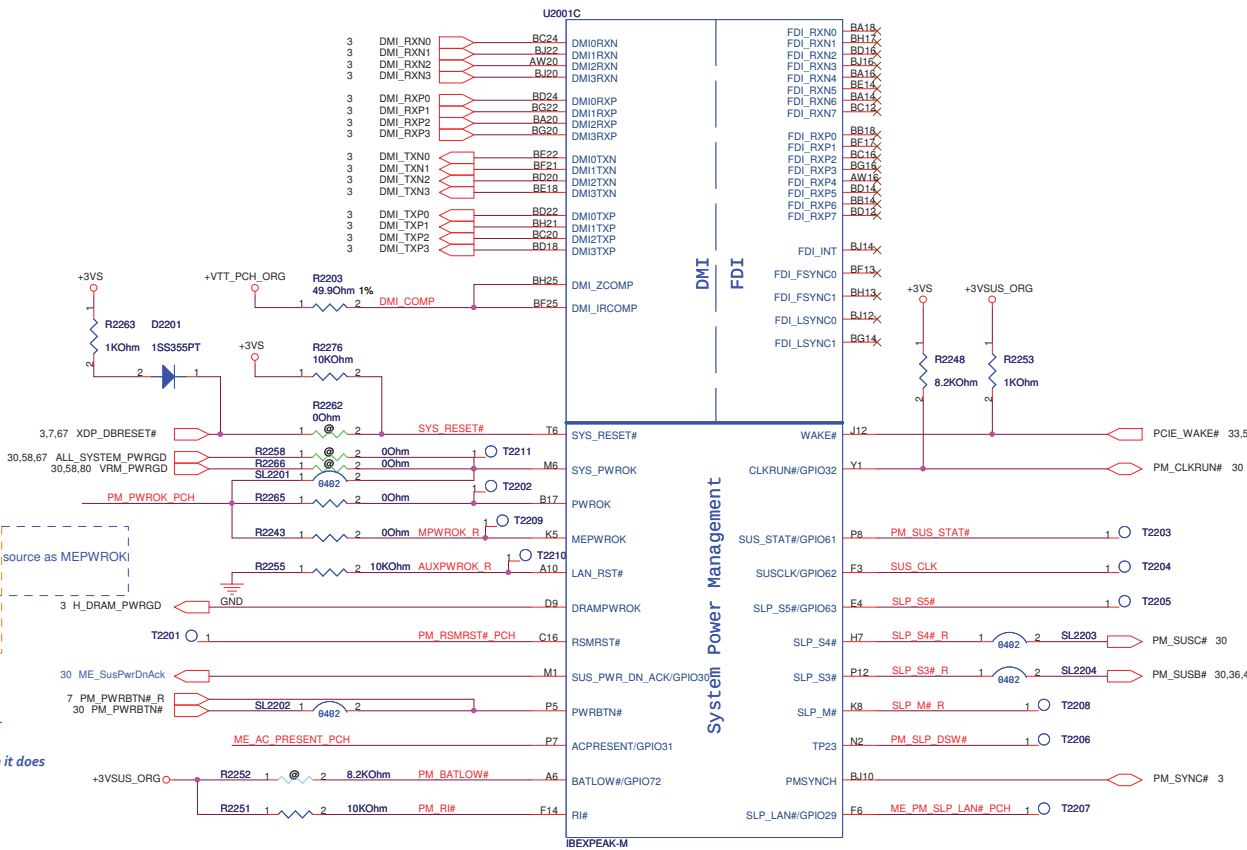
EDS 1.0: Intel LAN
 Enabled : LAN_RST# connected to the same source as MEPWROK
 Disabled : LAN_RST# must be grounded
 Disabled : SLP_LAN#->NC.
 P27. Disabled : VCCLAN connected to GND.

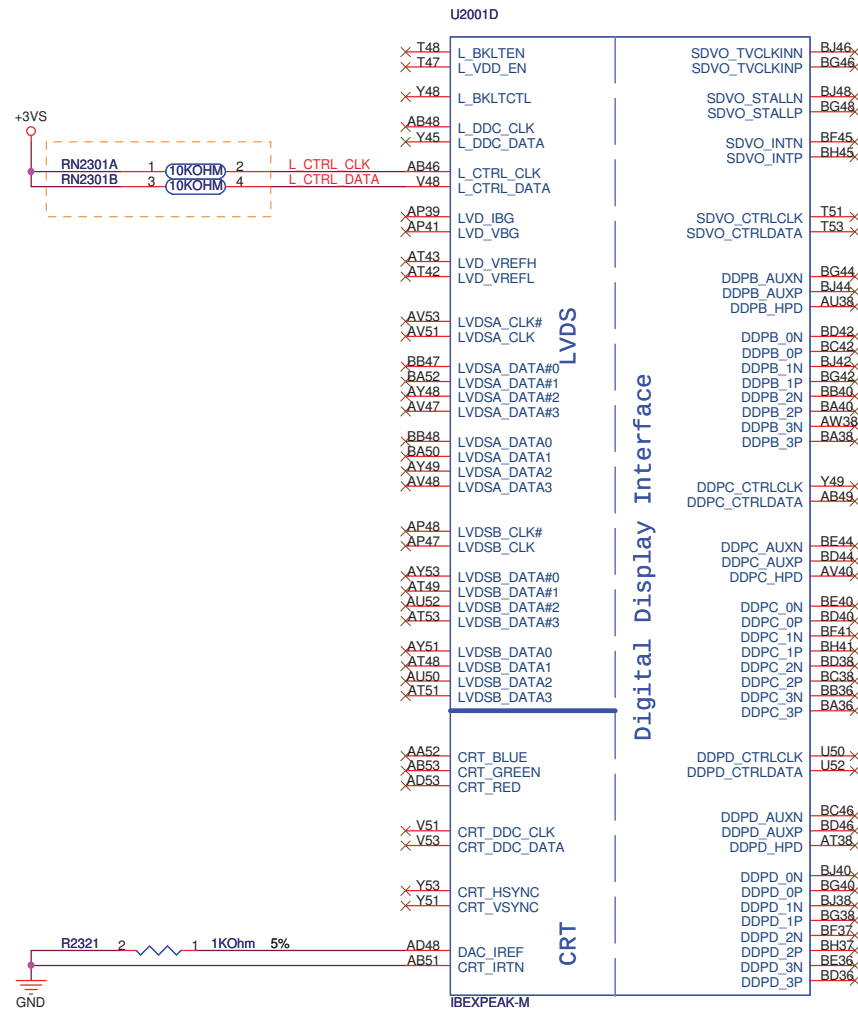


SUS_PWR_DN_ACK :
 Active high. Asserted by Intel ME when it does not require the PCH Suspend well to be powered.

ACPRESENT :
 Active high. Asserted by EC when the platform is connected to an AC source.

MoW z6 , 2009 :
 The minimum time from WLAN device power valid until MEPWROK assertion is 20 mSecs.





Port	Strap	How to enable the port	How to Disable the Port
LVDS	L_DDC_DATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
Port B	SDVO_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
Port C	DDPC_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
Port D	DDPD_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm resistor	NC
eDP on CPU	CFG[4]	Pulled the signal down to the GND through a 3.3K ohm resistor	NC

Title : PCH - LVDS,CRT

ASUSTeK COMPUTER INC. NB6
 Engineer: Jerry Mou

Size	Project Name	Rev
Custom	K72Jr	2.0

Date: Friday, December 11, 2009
 Sheet 23 of 99

GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap

PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

Sampled on rising edge of PWROK.



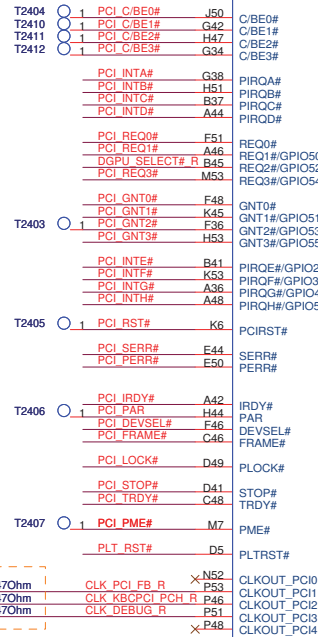
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/
Top-Block swap override

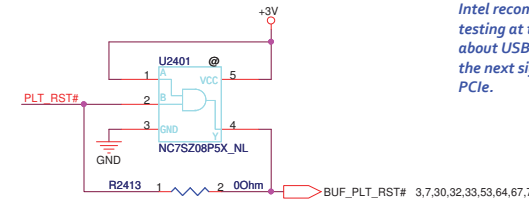
High=Default



K72J	
0	USB port
1	USB port
2	USB port (D/B)
3	USB port (D/B)
4	
5	MiniCard (Full)
6	
7	
8	MiniCard (Half)
9	Camera
10	
11	Card Reader
12	Bluetooth
13	



IBEXPEAK-M



PCI

USB

WVRAM

MoW 02 , 2009

Intel recommends that customers do not perform USB or SATA Signal Quality testing at this time. Ibox Peak Sightings Report Rev. 004 contains a new sighting about USB Eye Diagram Failure. A similar sighting about SATA will be available in the next sightings report release. Customers may begin Signal Quality testing on PCIe.

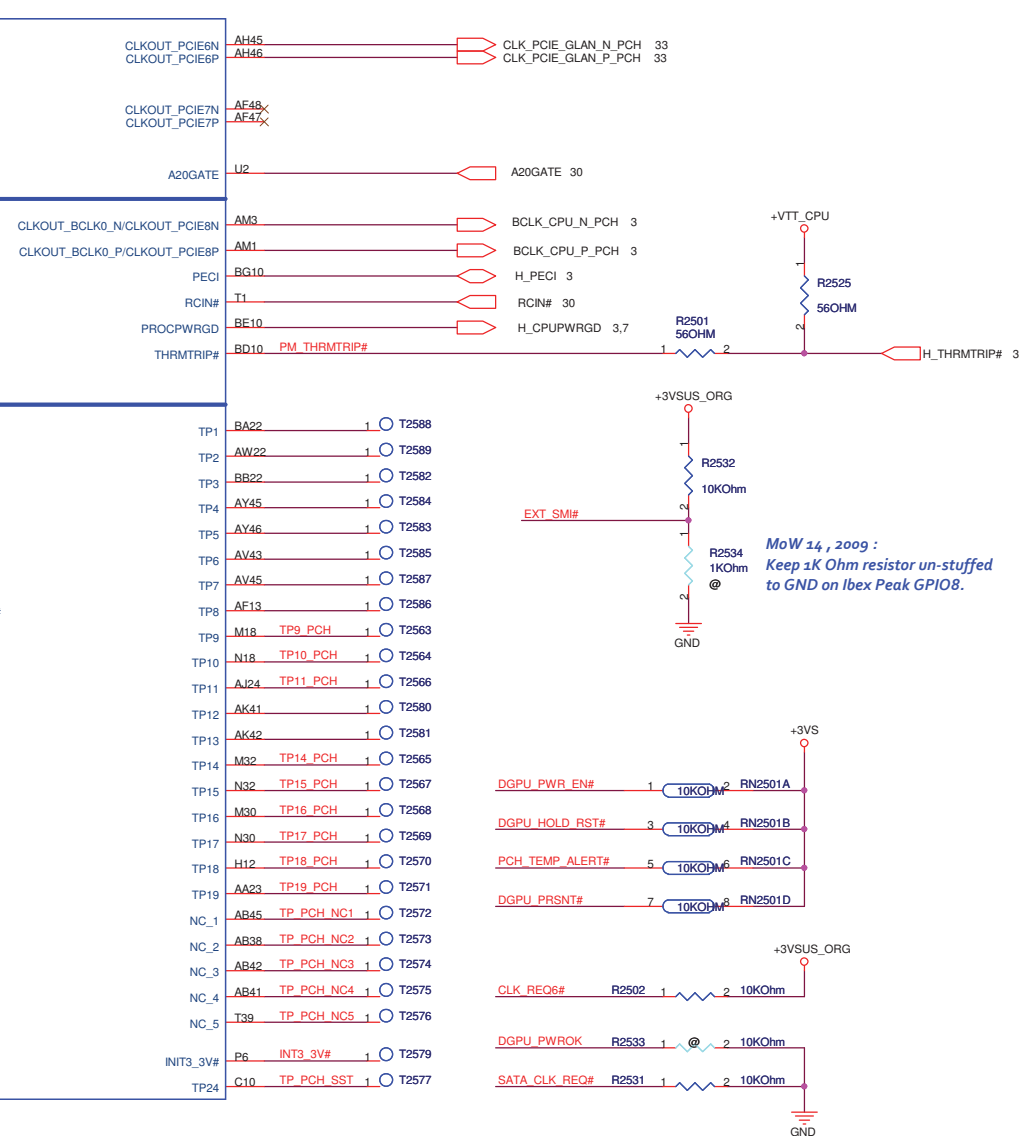
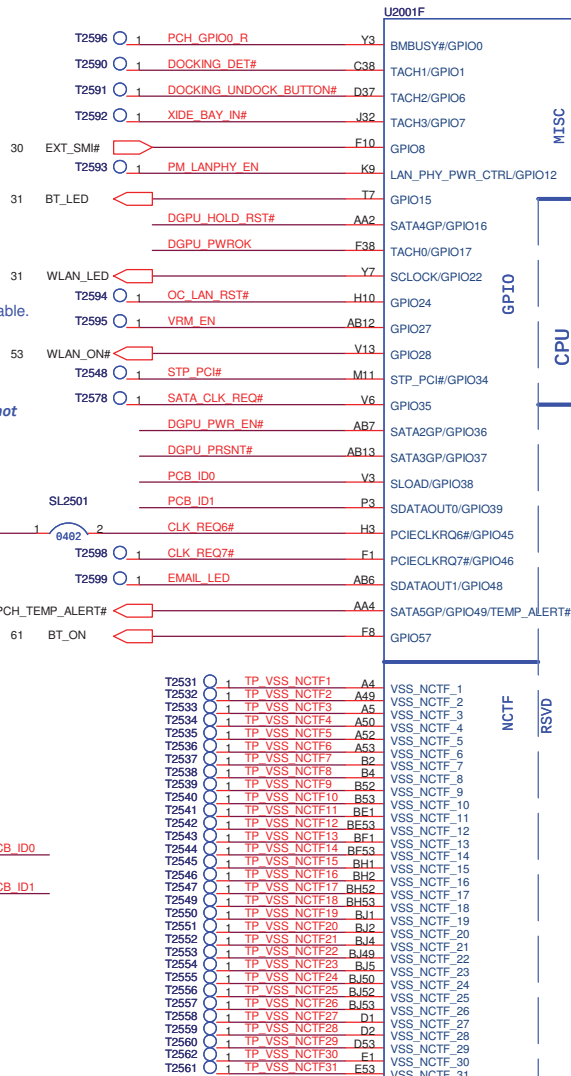
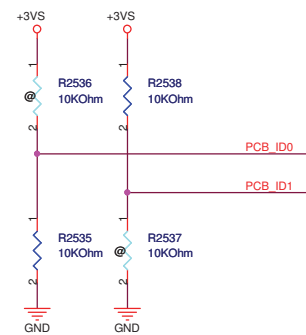
		Title : PCH - PCI,USB	
ASUSTek COMPUTER INC. N86		Engineer: Jerry Mou	
Size Custom	Project Name K72Jr	Rev 2.0	
Date: Friday, December 11, 2009		Sheet 24	of 99

GPIO 15: Default internal PD 20K.

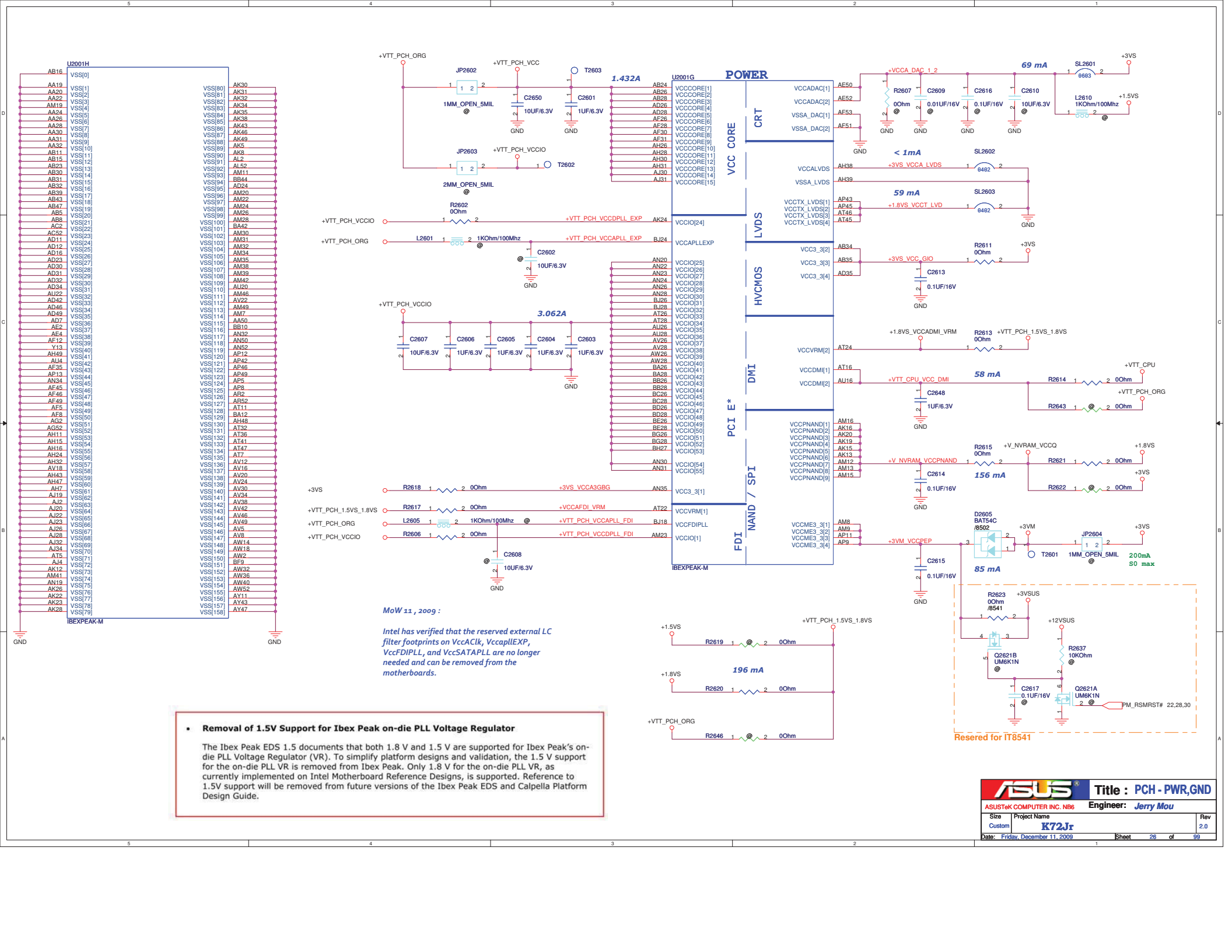
GPIO 27: Enable VCCVRM, Low=disable.
Default internal pull up.

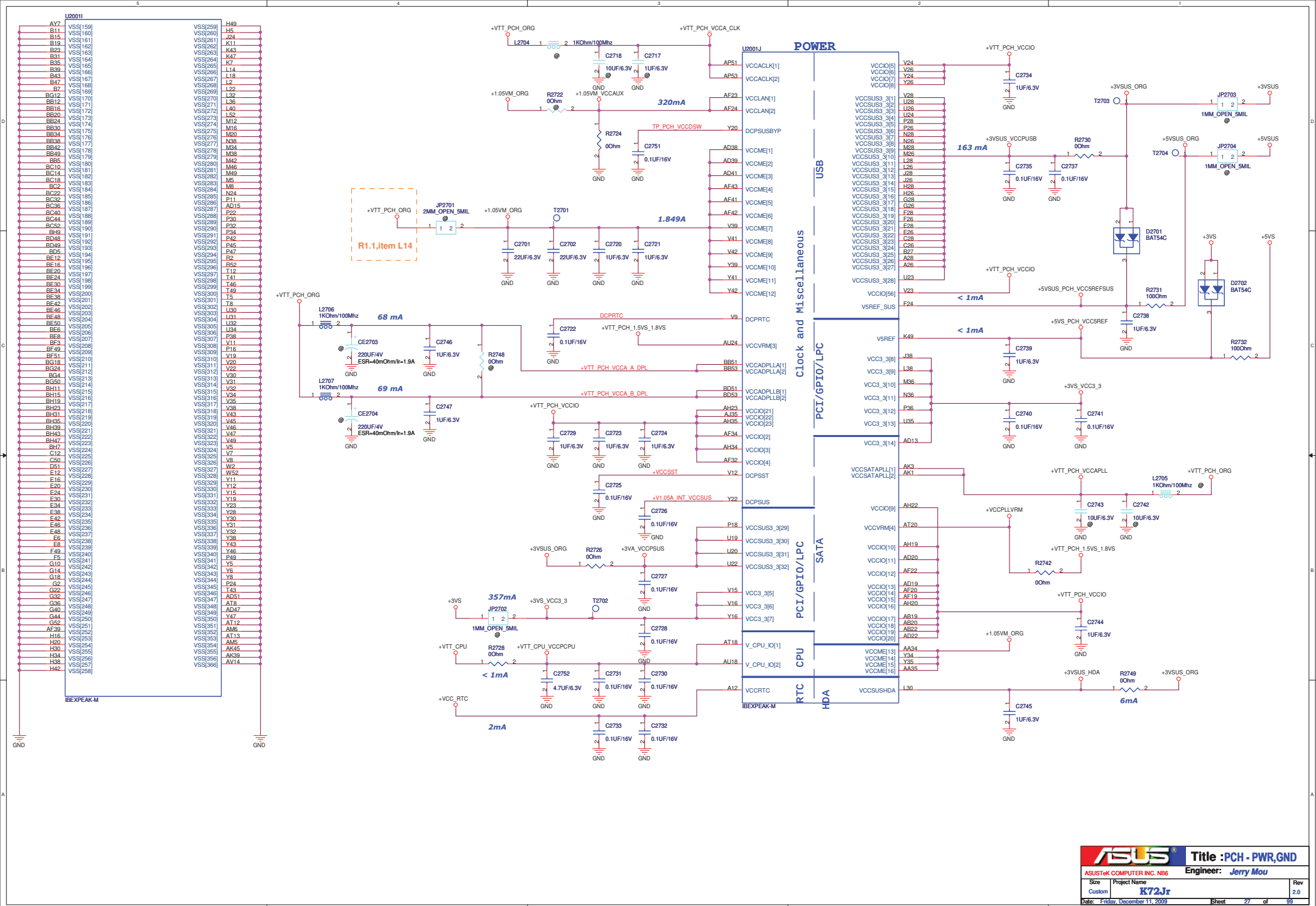
GPIO 28: Default internal PU 20K.

MoW 50, 2008 :
SATACLKREQ# protocol not
supported on Ibox Peak.



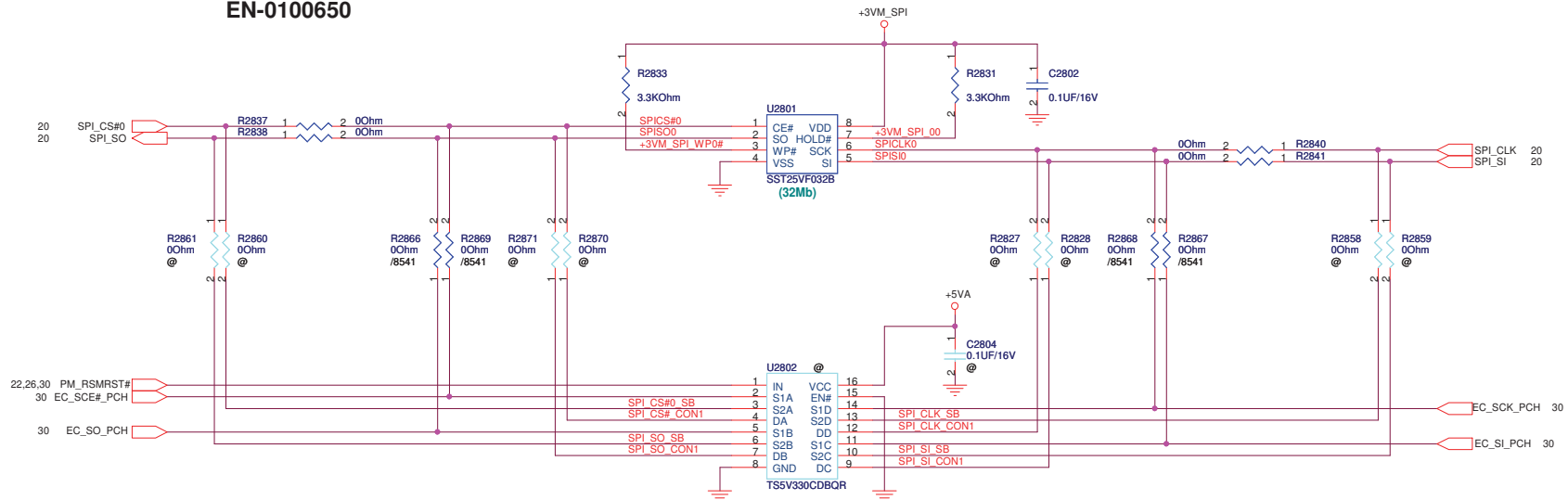
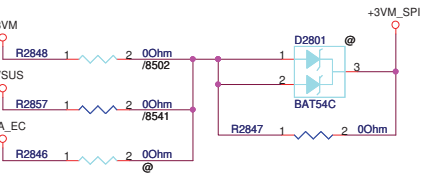
MoW 14, 2009 :
Keep 1K Ohm resistor un-stuffed
to GND on Ibox Peak GPIO8.





PCH SPI ROM

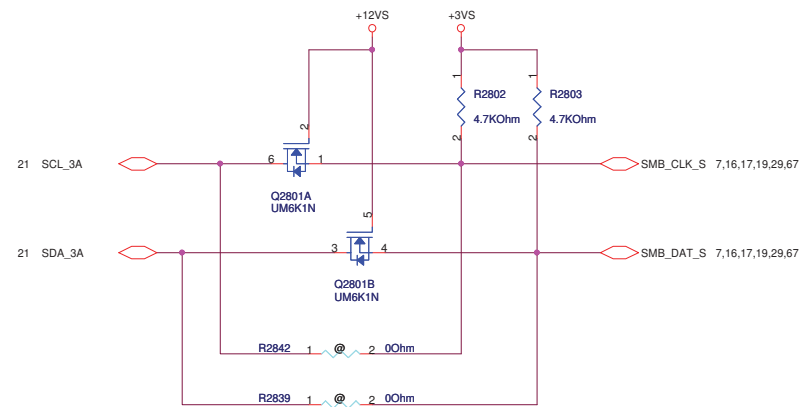
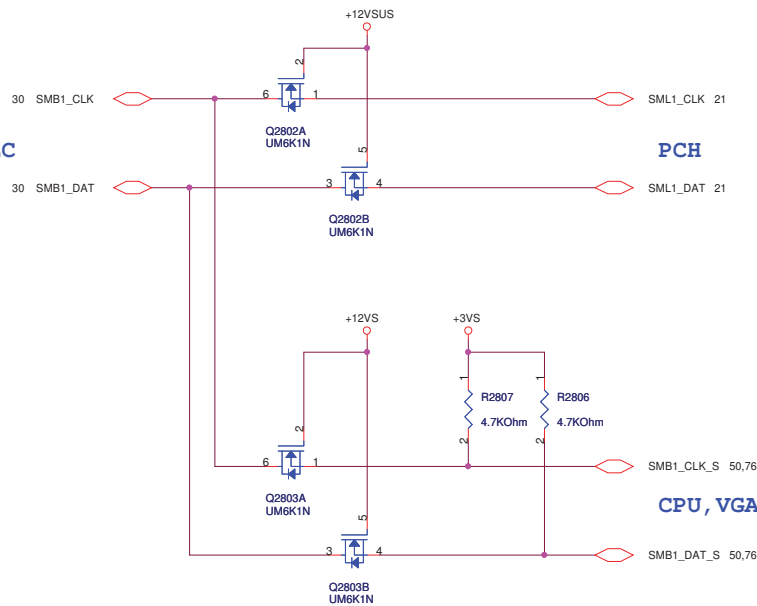
EN-0100650



EC

PCH

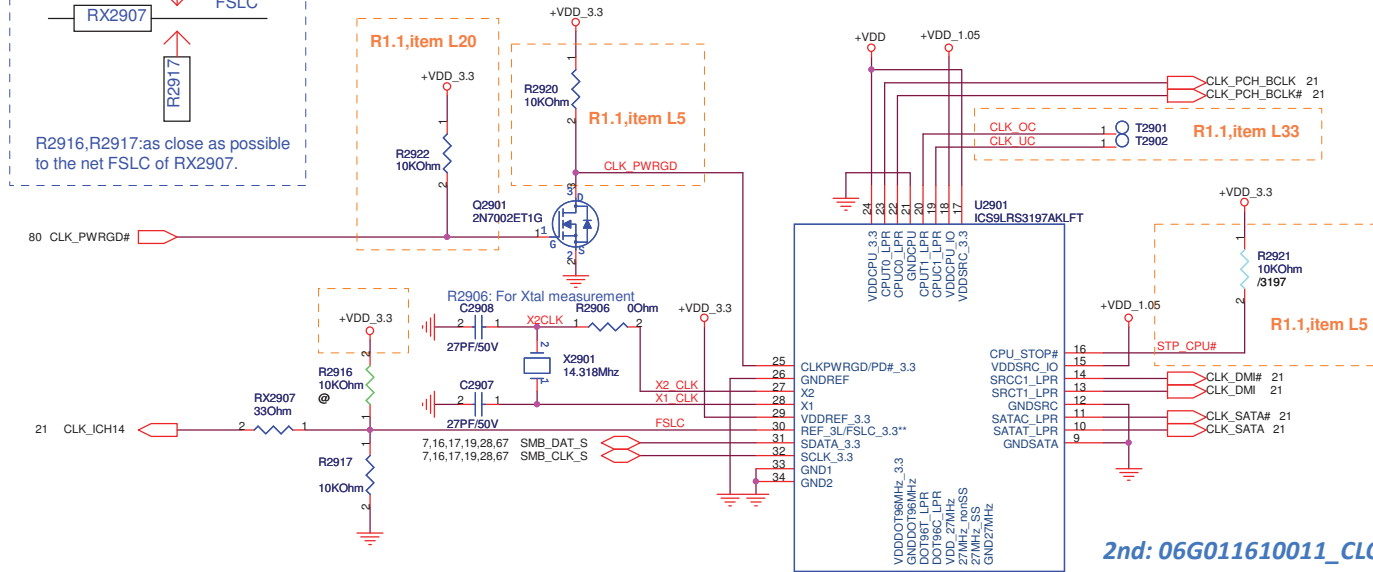
CPU, VGA Thermal



Layout note:

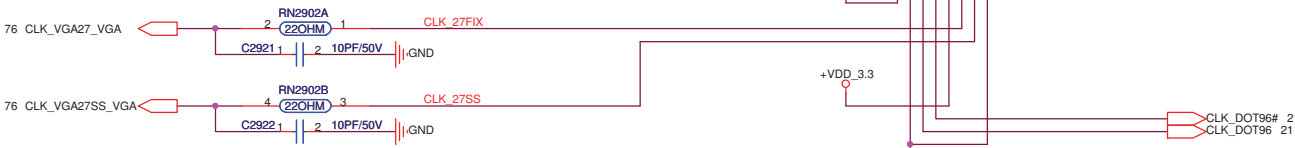
R2916, R2917: as close as possible to the net FSLC of RX2907.

BCLK	FSLC
133	0
100	1



3162 Pin16 : T-track

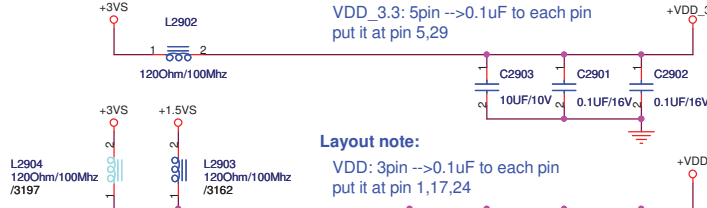
2nd: 06G011610011_CLOCK GEN 3162B(A改成B)



Layout note:
VDD_3.3: 5pin --> 0.1uF to each pin
put it at pin 5,29

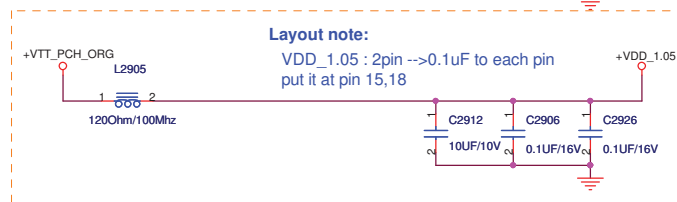
9LRS3197----mount L2904,unmount L2903

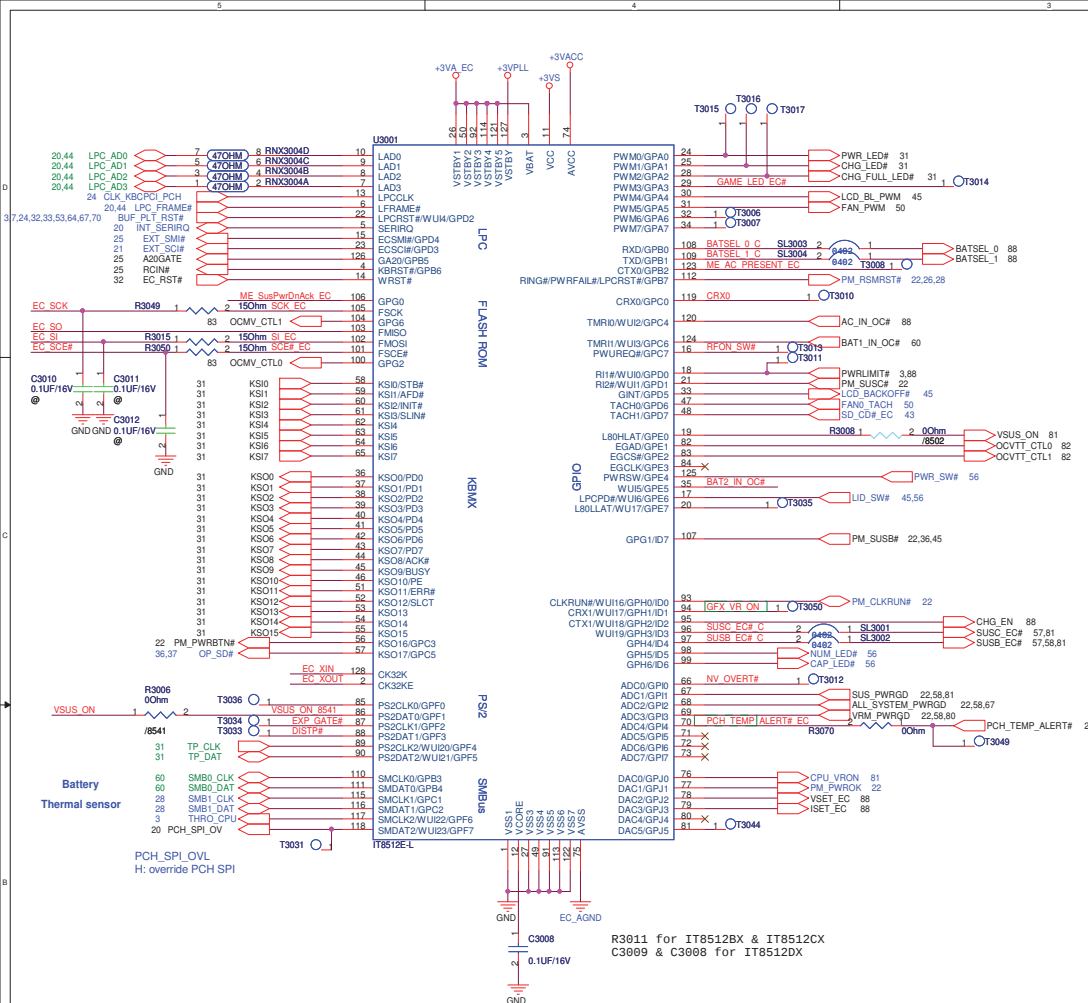
9LVS3162----mount L2903,unmount L2904,R2921



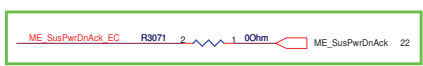
Layout note:
VDD: 3pin --> 0.1uF to each pin
put it at pin 1,17,24

Layout note:
VDD_1.05 : 2pin --> 0.1uF to each pin
put it at pin 15,18



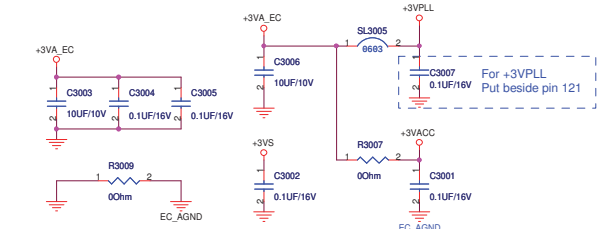
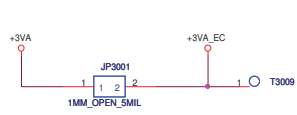


06G042030010 EMBEDDED CONTROLLER IT8570E

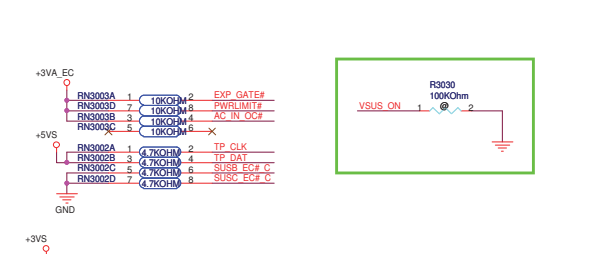
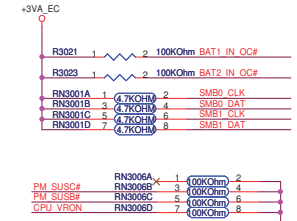


Calpella DG R1.6 page 237:
ME_SusPwrOnAck: Required for all platforms
ME_AC_PRESENT: Required for all platforms except platforms with Ignition Firmware.(10K PU optional)

For IT8752 Power

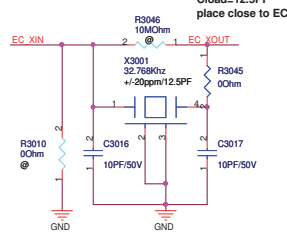


For PU / PD



Note:
EXT_SMI#, EXT_SC#, PU power plane
depend on ICH9 GPIO.

For X'tal

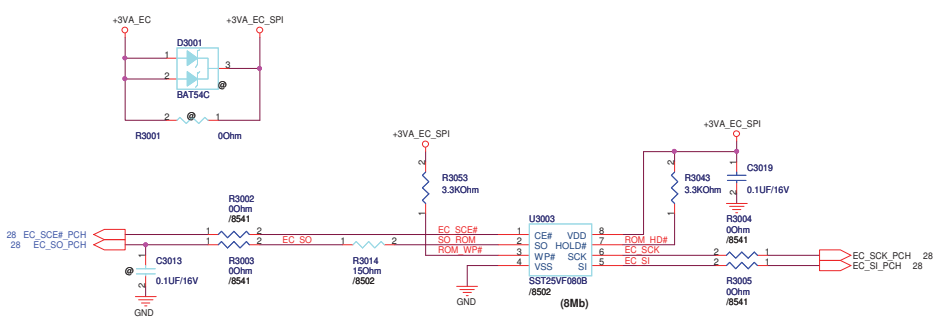


For EC Hardware Strap

I/O Base Address
Note: It can be programmable by EC firmware
Share Memory
Note: It can be programmable by EC firmware.
PP Enable
Note: Default Int. Pull-Low

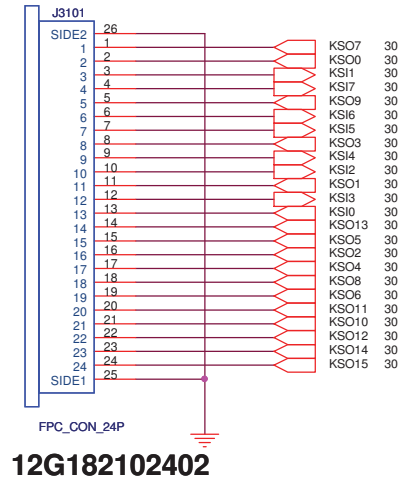
For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

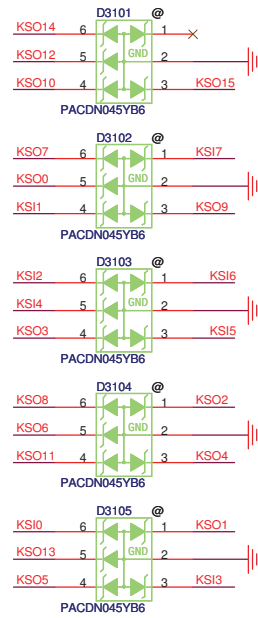
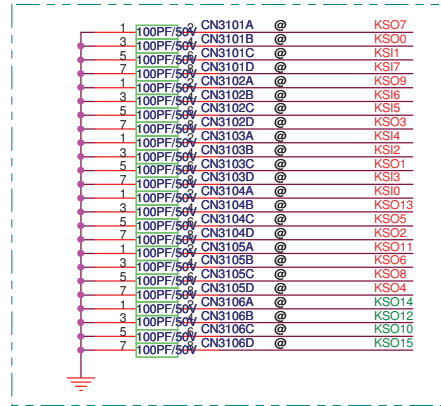


Keyboard

TOP connector 下接觸
PIN1上面 KSO7 ; 下面 KSO24

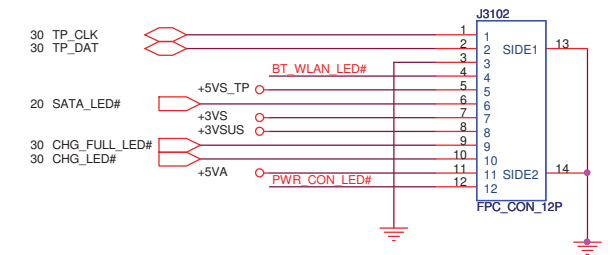


EMI

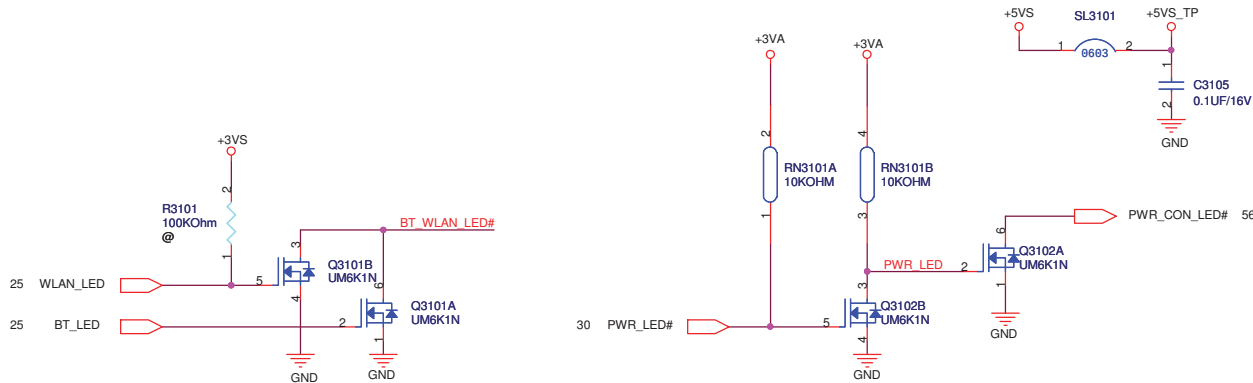


12 Pin Touch-Pad Conn.

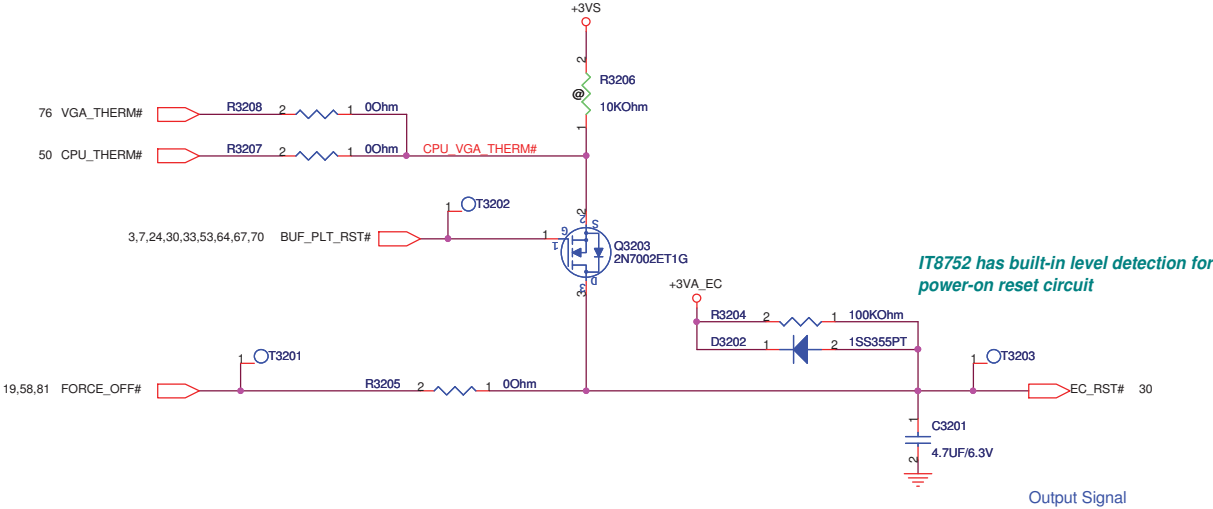
TP M/B TOP 上接觸 PIN1 左邊 CLK ; TP
SMALL BOTTOM 下接觸. Cable 折兩次



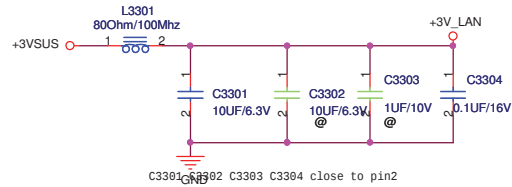
12G18340120C



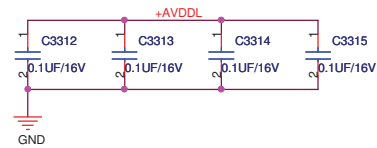
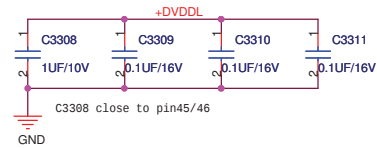
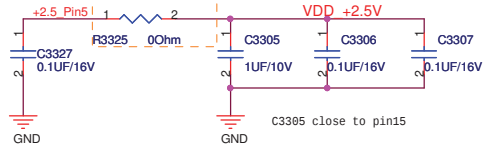
Thermal Policy



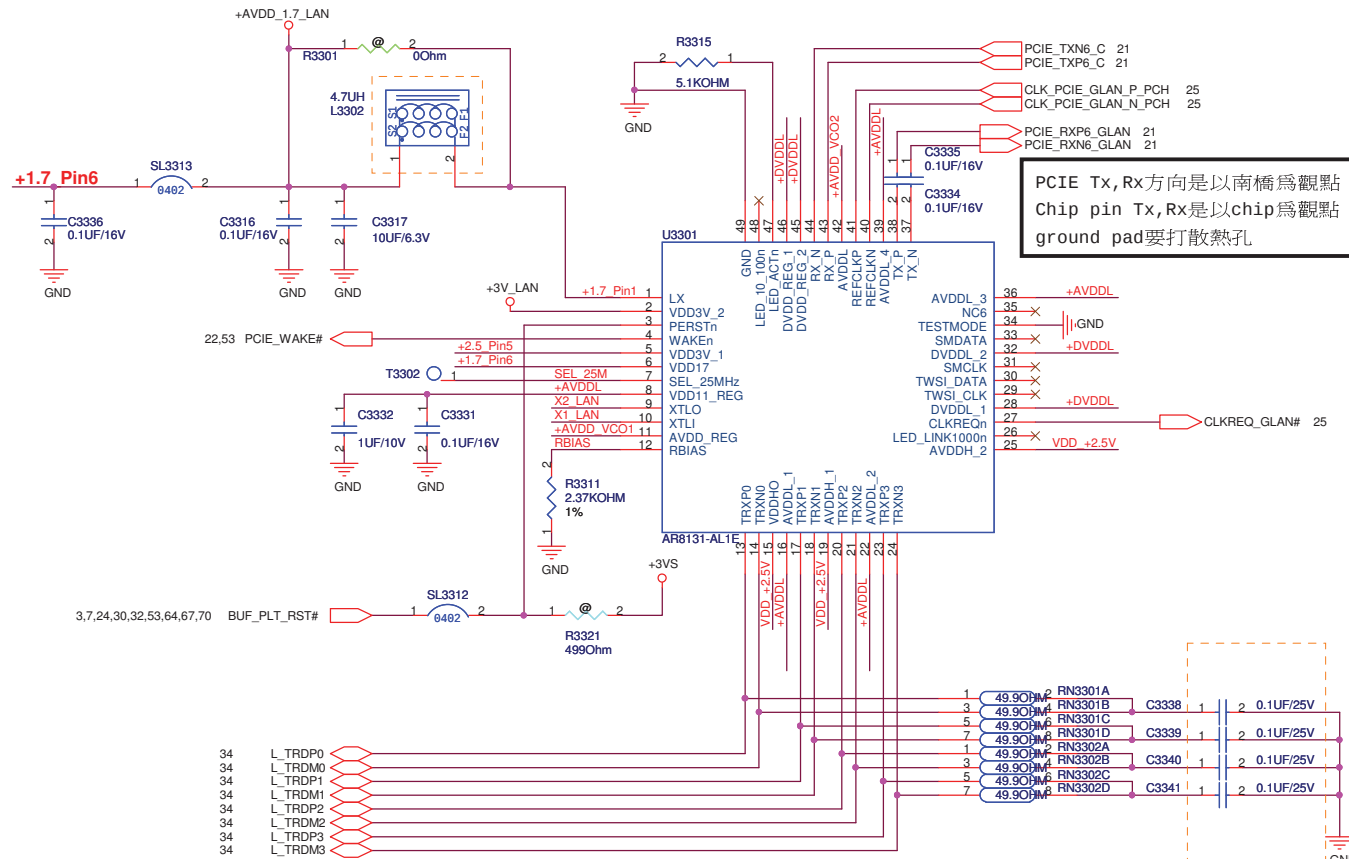
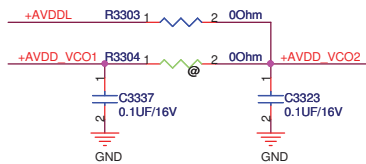
R1.1,item L34



For Design IP: R3325: 0 Ohm

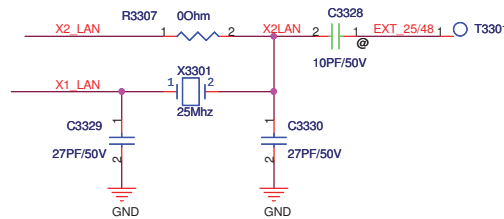


AR8131 with overclock: Remove R3315, R3303
Not overclock: Remove R3304

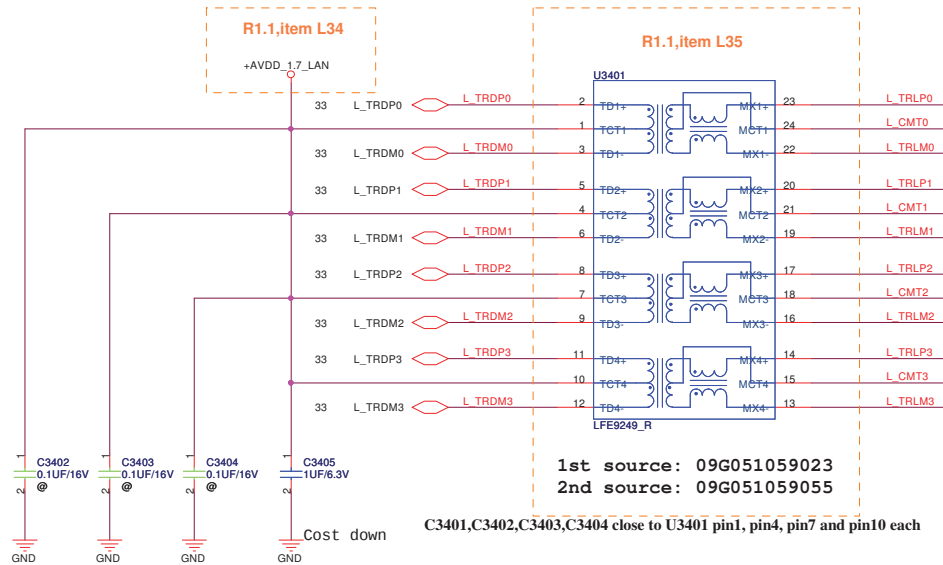


PCIE Tx, Rx方向是以南橋為觀點
Chip pin Tx, Rx是以chip為觀點
ground pad要打散熱孔

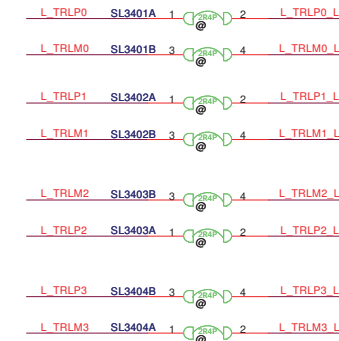
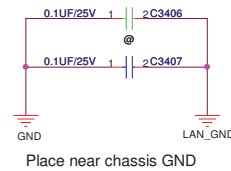
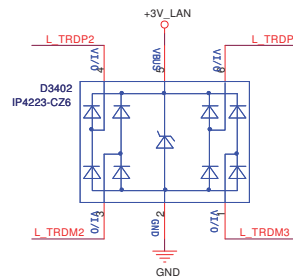
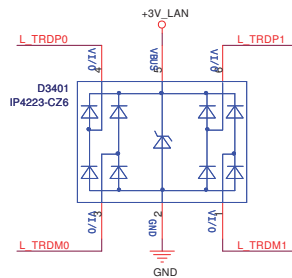
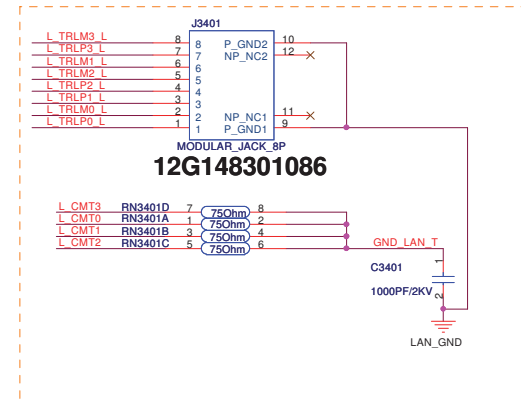
AR8131/25MHz: Remove C3328

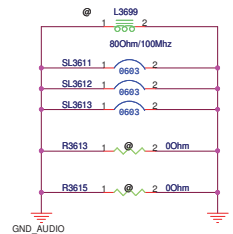


ASUS		Title : LAN-AR8131	
ASUSTek COMPUTER INC. NB4		Engineer: Jerry Mou	
Size B	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009		Sheet 33	of 100



connector without modem





Audio Power

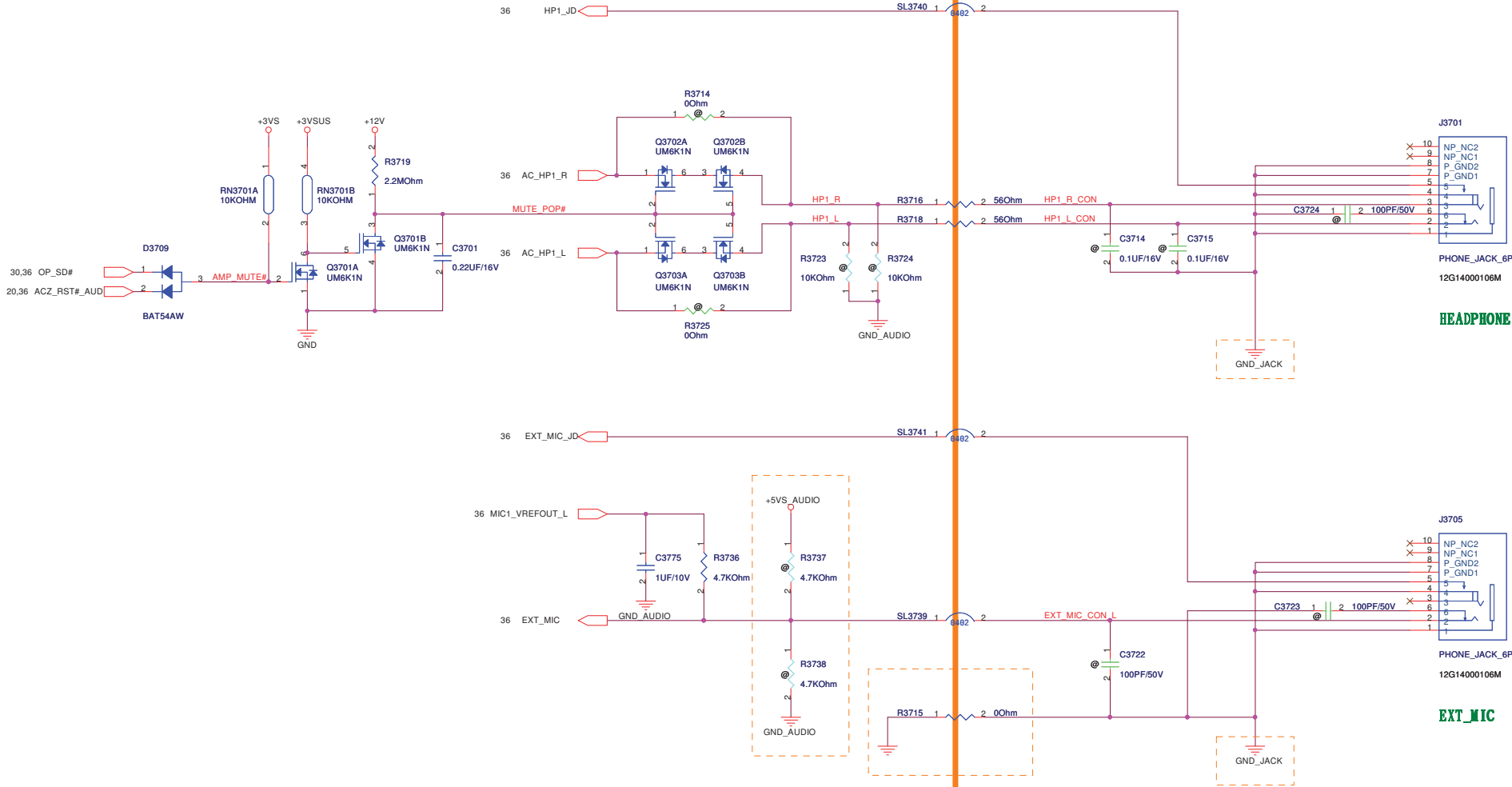
FOR RESET MODE:

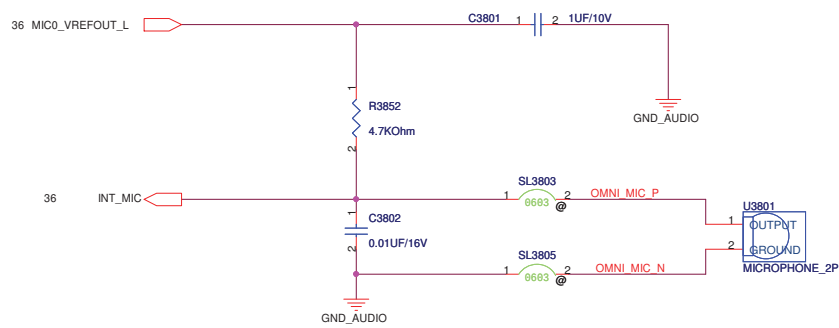
$$V_o = 1.25 * (1 + R_{2505} / R_{2505})$$

$$= 1.25 * (1 + 100K / 34.8K) = 4.84$$

The circuit diagram shows a power supply section with a 22.30, 45 PM_USB# and a 1.5V regulator (L3602) connected to a 100KHz/100mHz signal source. The signal source is connected to a 100KHz/100mHz signal source. The circuit includes a U3602 op-amp, a U6G007342012 op-amp, and various passive components like resistors (R3602, R3617, R3619, R3625, R3632), capacitors (C3626, C3627, C3628, C3632), and a 1000PF/50V capacitor. The circuit is powered by +5V and GND. The output is labeled T3610 and T3611. The circuit is labeled 'Try 0 ohm'.

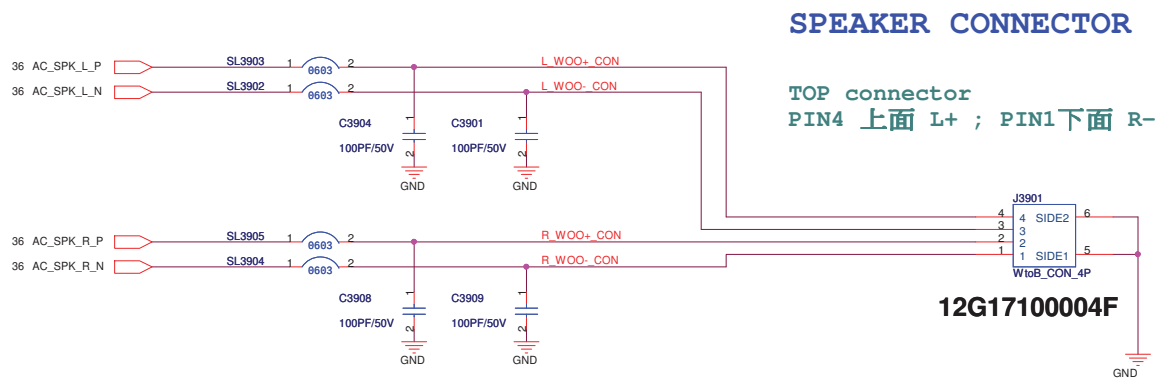
ASUS		Title : CODEC IDT92HD81	
ASUSTeK COMPUTER INC. NB2		Engineer: Jerry Mou	
Size Custom	Project Name K72Jr	Rev 2.0	
Date: Friday, December 11, 2009	Sheet	36	of 100

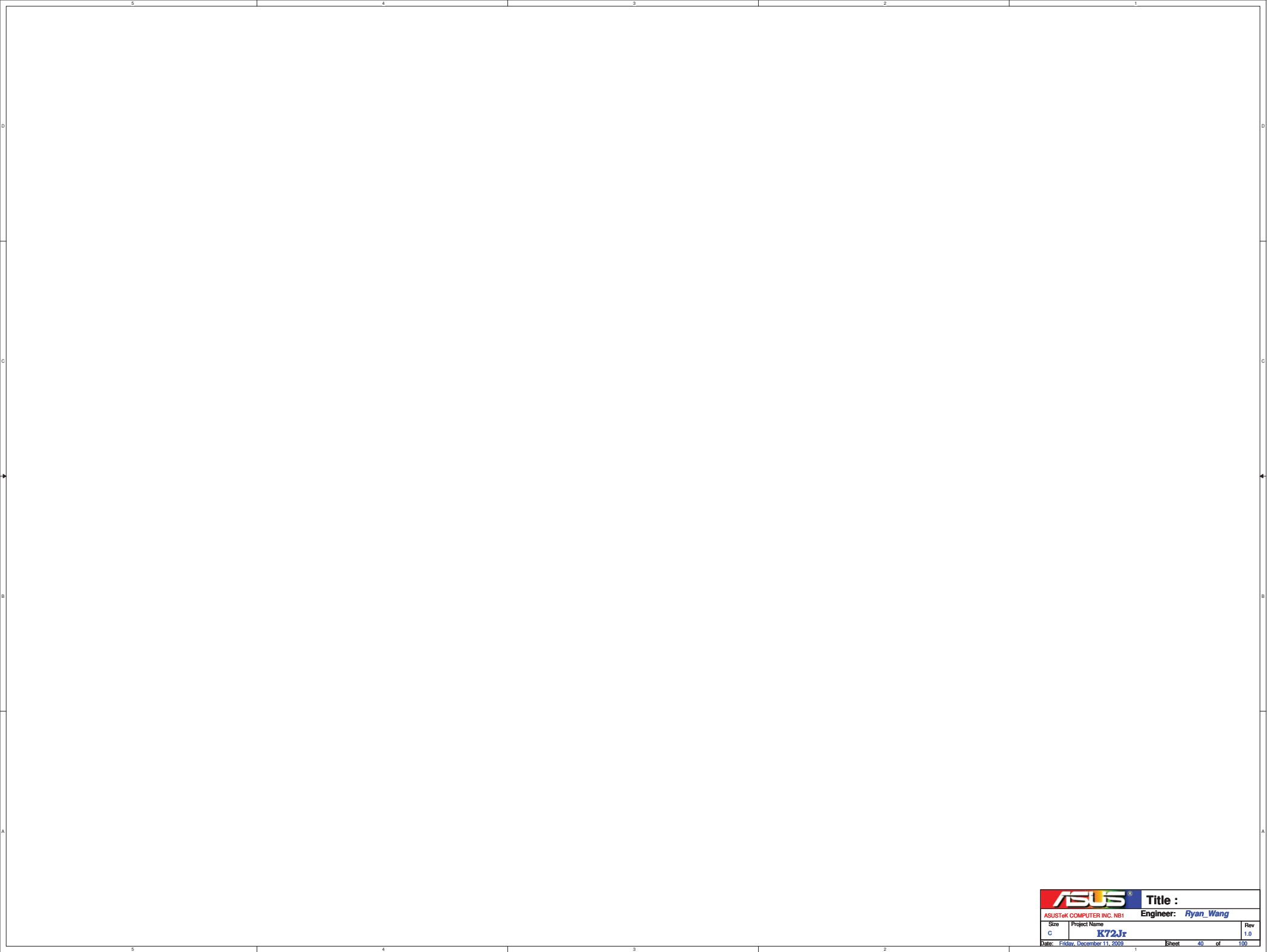




<Variant Name>

ASUS		Title : AUD_I_MIC	
ASUSTeK COMPUTER INC. NB2		Engineer: Jerry Mou	
Size Custom	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009		Sheet	38 of 100

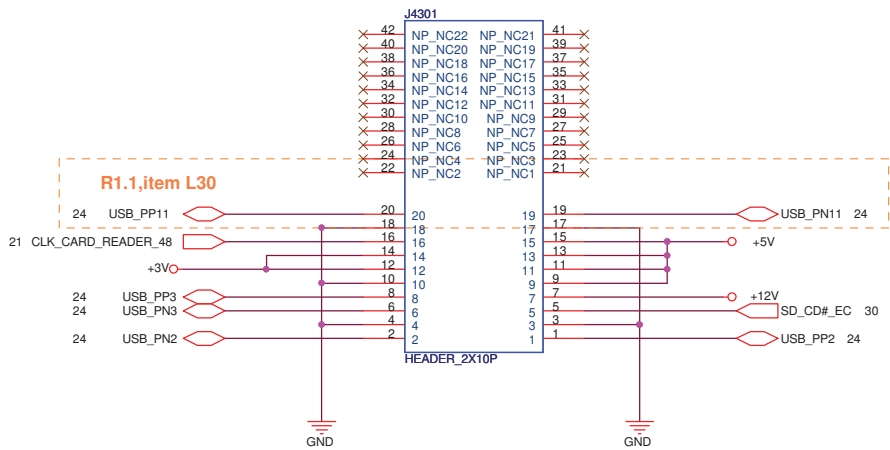




		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Ryan_Wang</i>	
Size	Project Name	Rev	
C	K72Jr	1.0	
Date: Friday, December 11, 2009		Sheet 40	of 100

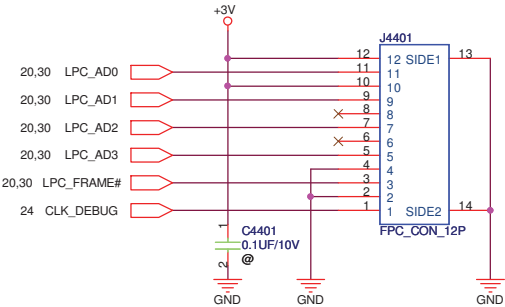
K72J USB Board_20 Pin CON

TOP connector
左上 PIN20 USB_PP4 ; 右上 PIN19 USB_PN4
左下 PIN2 USB_PN2 ; 右下 PIN1 USB_PP2

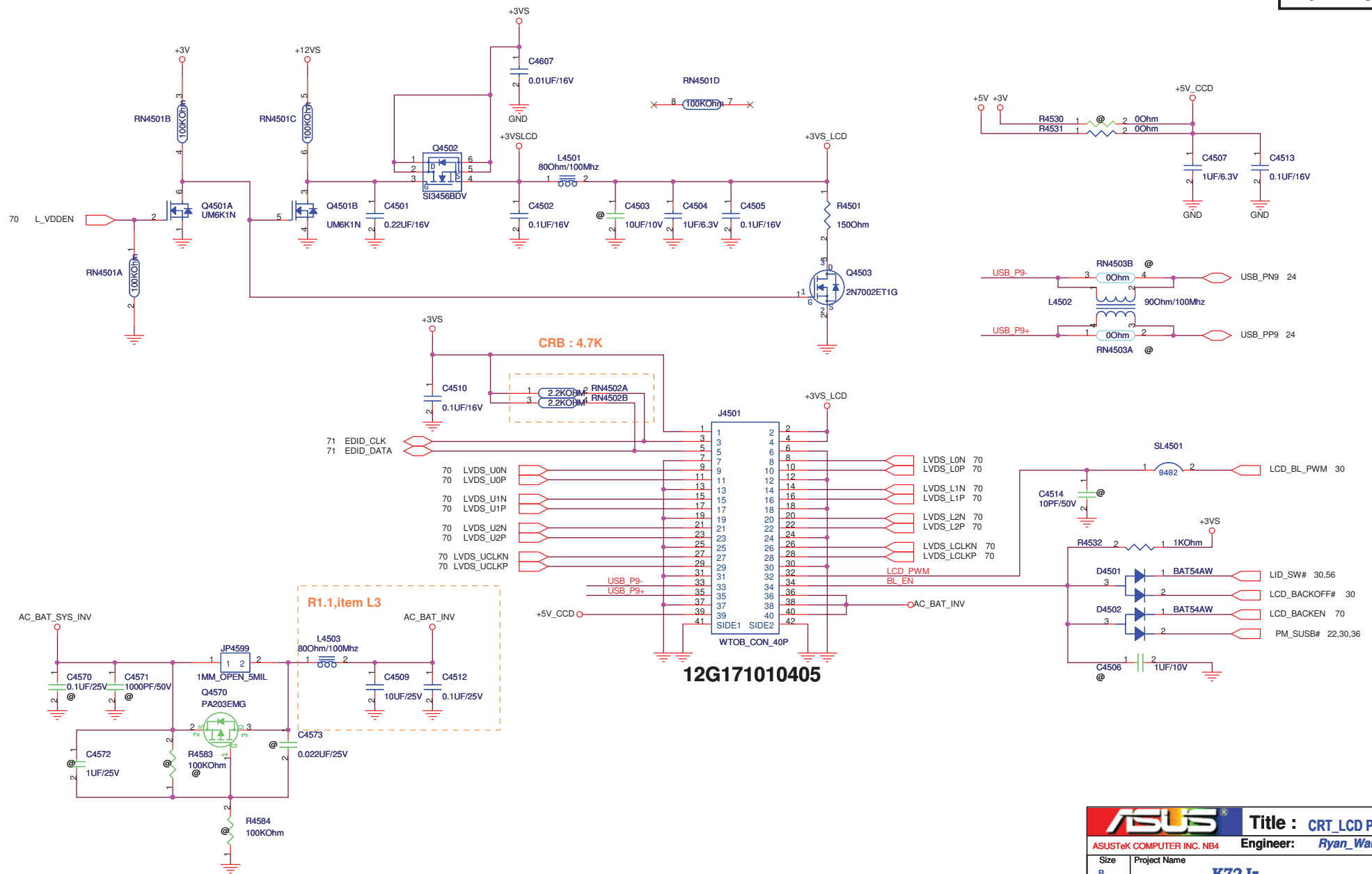


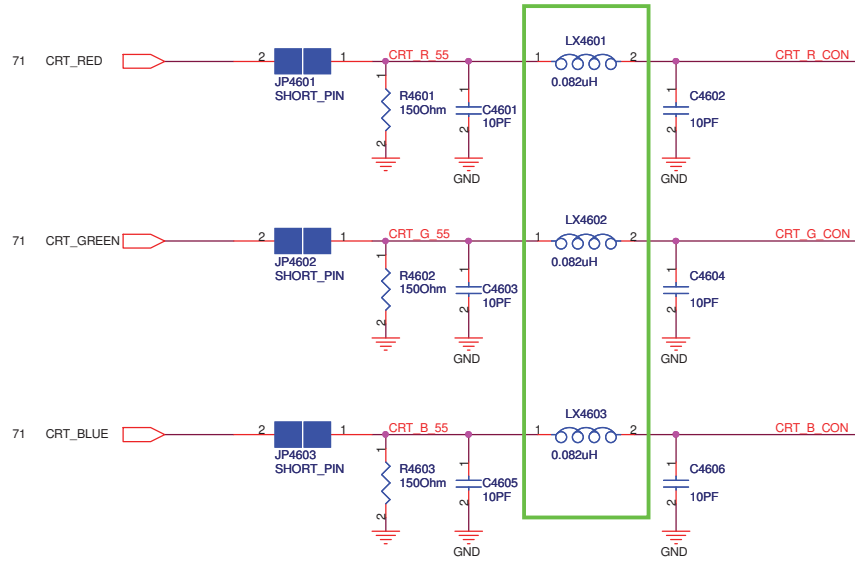
2nd : 12G06120020A

LPC Debug Port

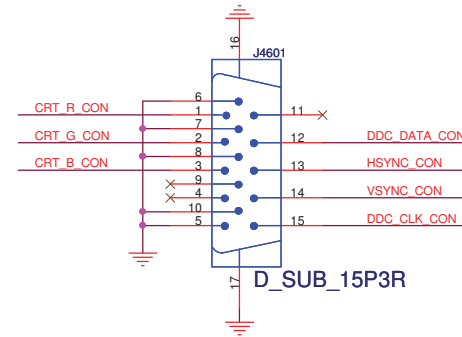
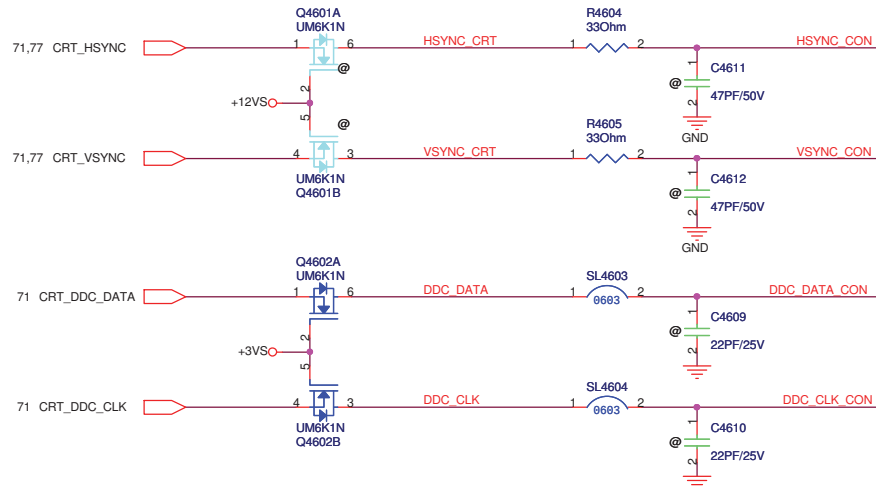


TP M/B TOP 下接觸 PIN1 上面 CLK ; Pin 12 下面 +3V

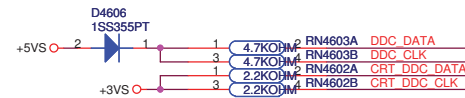
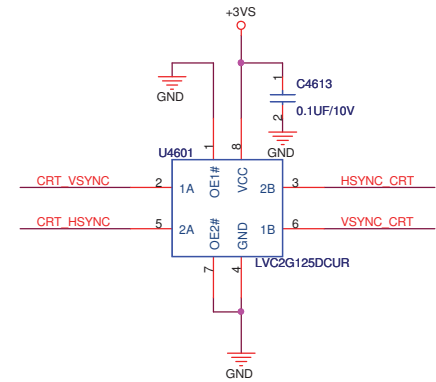




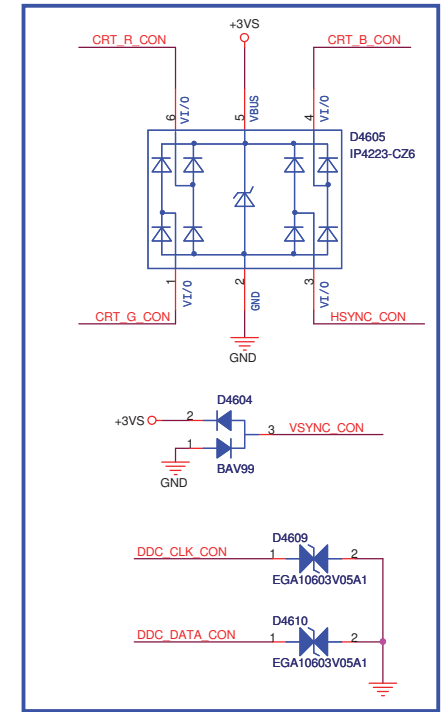
09G013047105



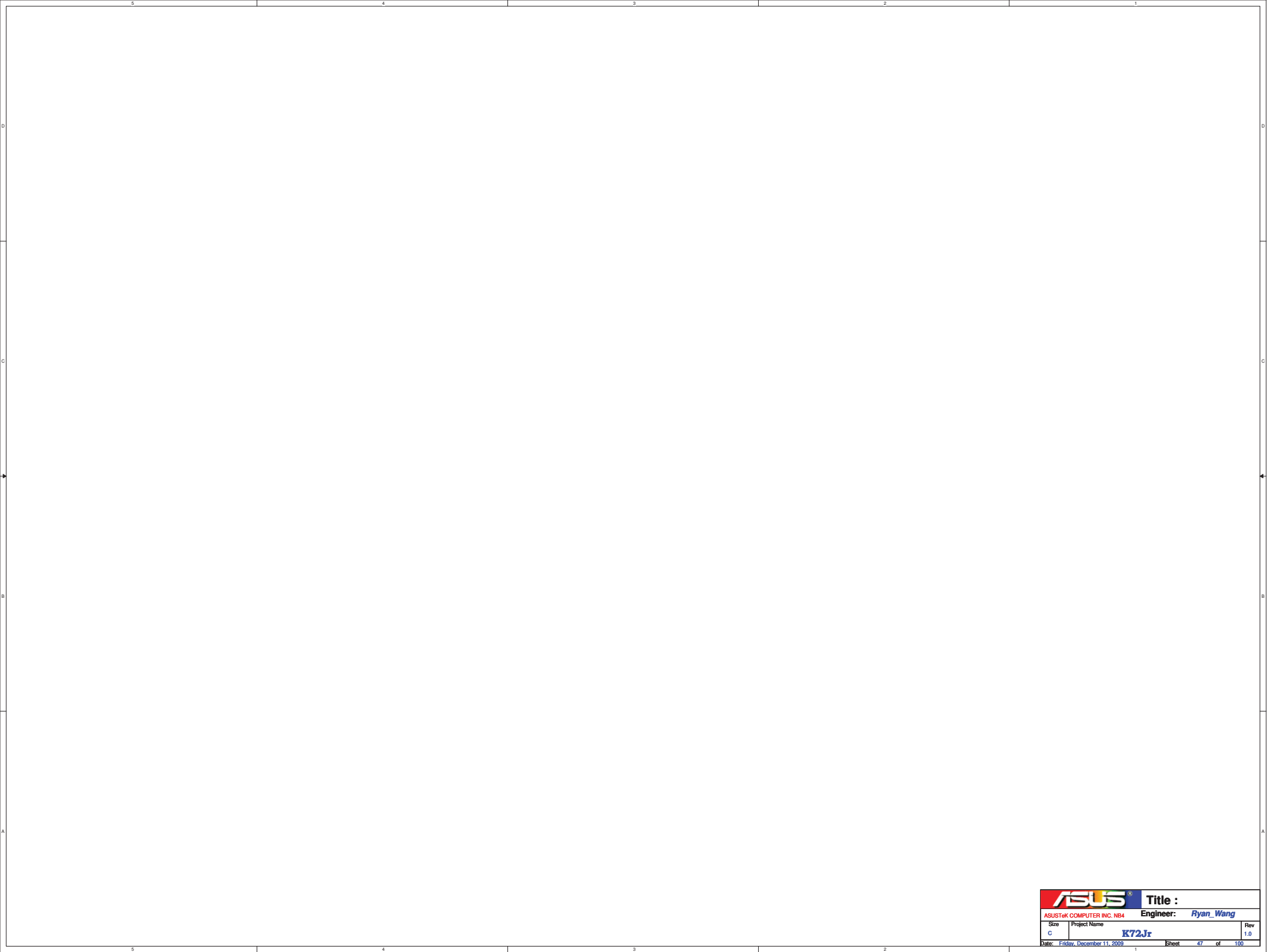
12G101102155



PLACE ESD Diodes near connector



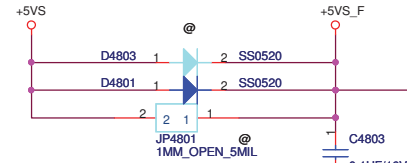
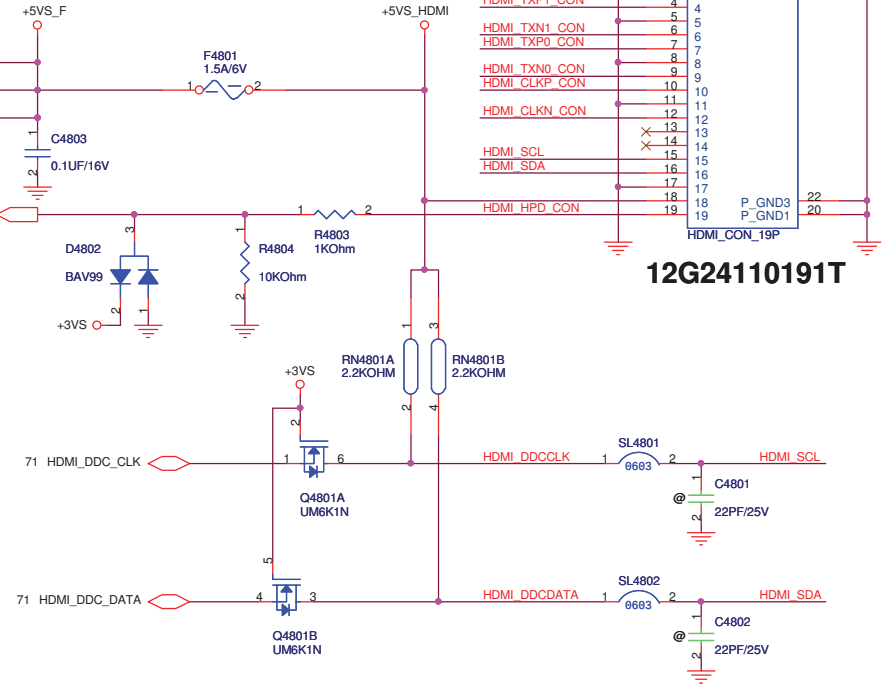
ASUS		Title : CRT_D-Sub	
ASUSTek COMPUTER INC. NB4		Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0	
Date: Friday, December 11, 2009		Sheet 46 of 100	



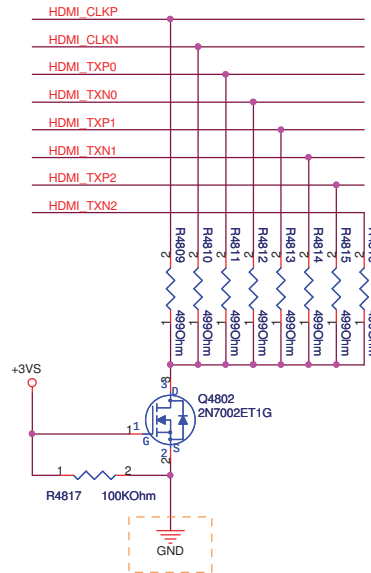
		Title :	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>Ryan_Wang</i>	
Size	Project Name		Rev
C	K72Jr		1.0
Date: Friday, December 11, 2009		Sheet 47	of 100

PLACE HDMI 0.1uF near connector J4801

71	HDMI_CLKP_VGA	C4804	1	2	0.1UF/16V	HDMI_CLKP
71	HDMI_CLKN_VGA	C4805	1	2	0.1UF/16V	HDMI_CLKN
71	HDMI_TXP0_VGA	C4806	1	2	0.1UF/16V	HDMI_TXP0
71	HDMI_TXN0_VGA	C4807	1	2	0.1UF/16V	HDMI_TXN0
71	HDMI_TXP1_VGA	C4808	1	2	0.1UF/16V	HDMI_TXP1
71	HDMI_TXN1_VGA	C4809	1	2	0.1UF/16V	HDMI_TXN1
71	HDMI_TXP2_VGA	C4810	1	2	0.1UF/16V	HDMI_TXP2
71	HDMI_TXN2_VGA	C4811	1	2	0.1UF/16V	HDMI_TXN2

F4801 changed to 07G014020210
POLYSWITCH SMD 0.2A/24V(1206)

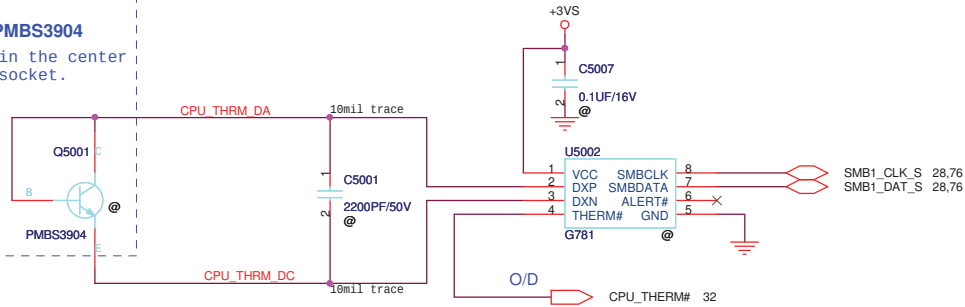
12G24110191T



CPU Thermal Sensor

PHILIP PMBS3904

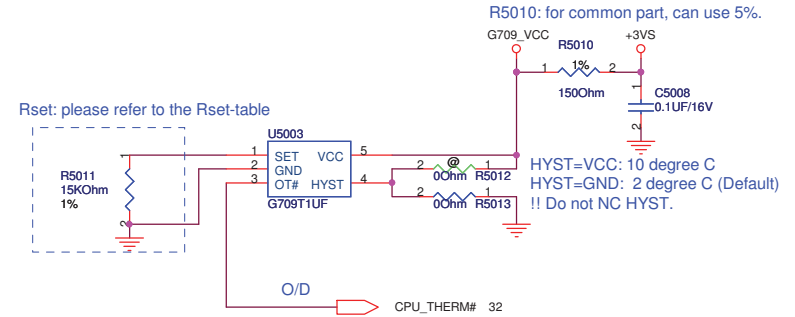
Place in the center of CPU socket.



SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

CPU Thermal Sensor



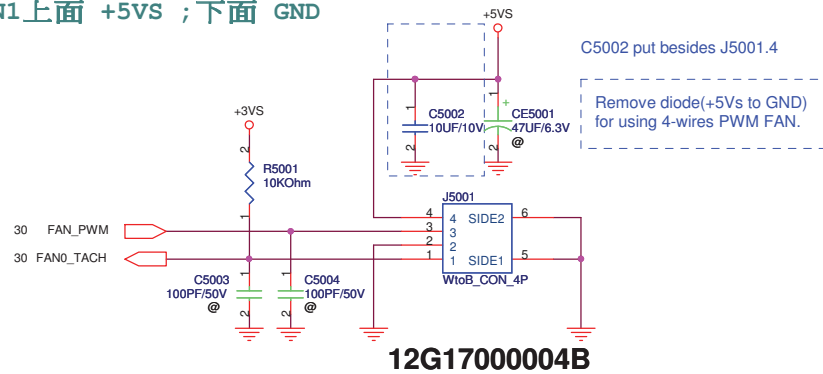
Layout note:

Place U5003 at the center of the CPU socket.

PWM Fan

BOTTOM connector

PIN1上面 +5VS ;下面 GND



$$R_{set}(Kohm)=0.0012T^{\circ}T-0.9308^{\circ}T+96.147$$

Resistor Accuracy: +/- 1%

G709 Temperature Threshold Accuracy: -4.7 degree C ~ +4.7 degree C

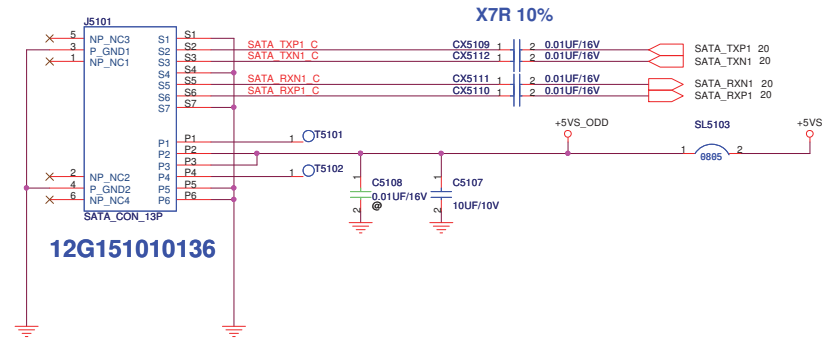
Set center temperature=96.06 degree C

Rset value is depend on thermal request.

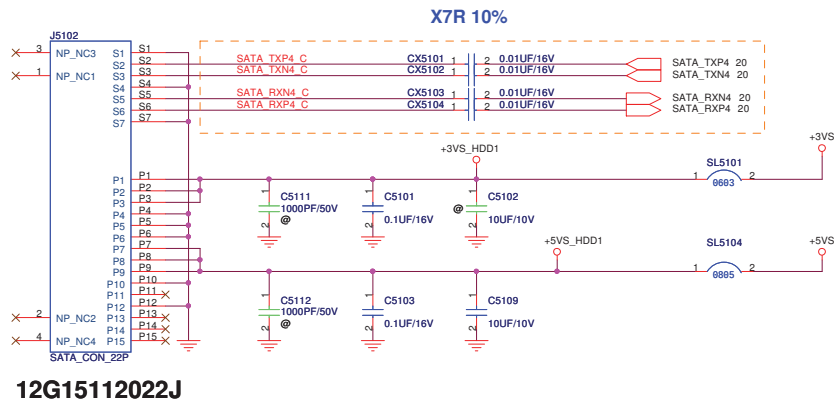
For M60J,possible board shutdown temperature: 91 ~ 101 degree C.

ASUS		Title : FAN_Fan & Sensor	
ASUSTeK COMPUTER INC. NB4		Engineer: Ryan_Wang	
Size B	Project Name K72Jr	Rev 2.0	
Date: Friday, December 11, 2009		Sheet 50 of 100	

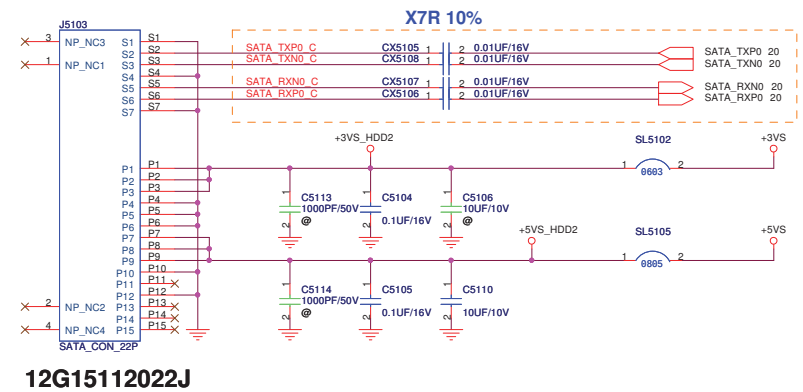
ODD

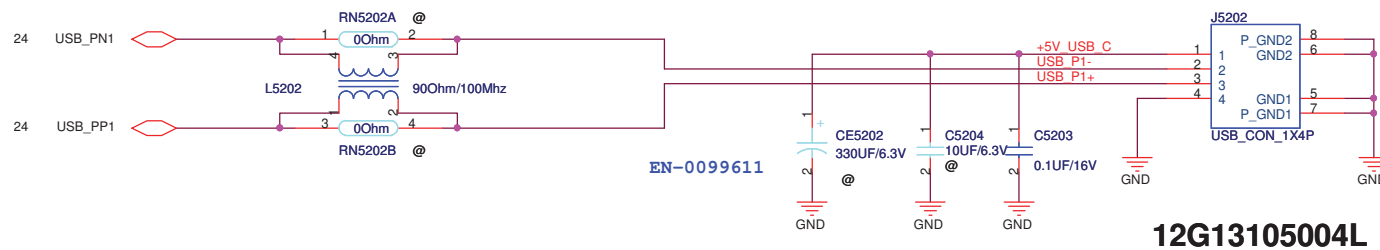
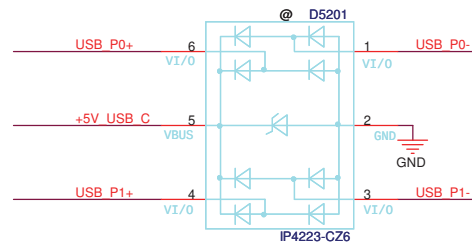
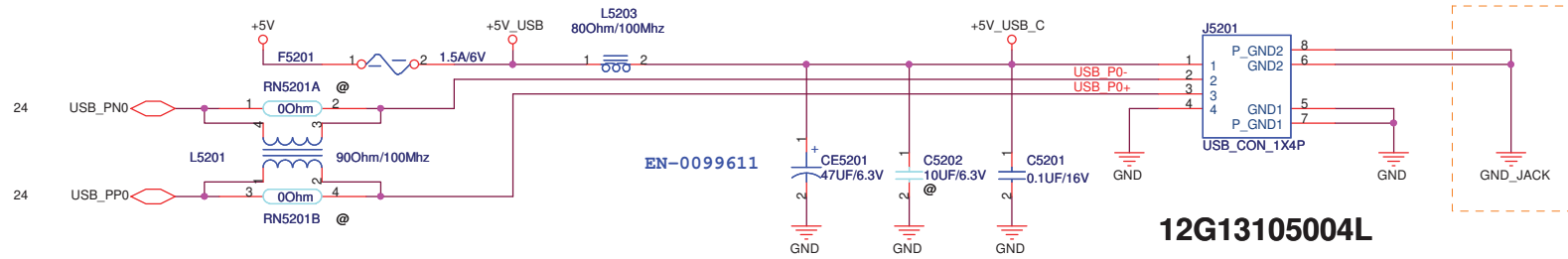


HDD (2nd) Right side

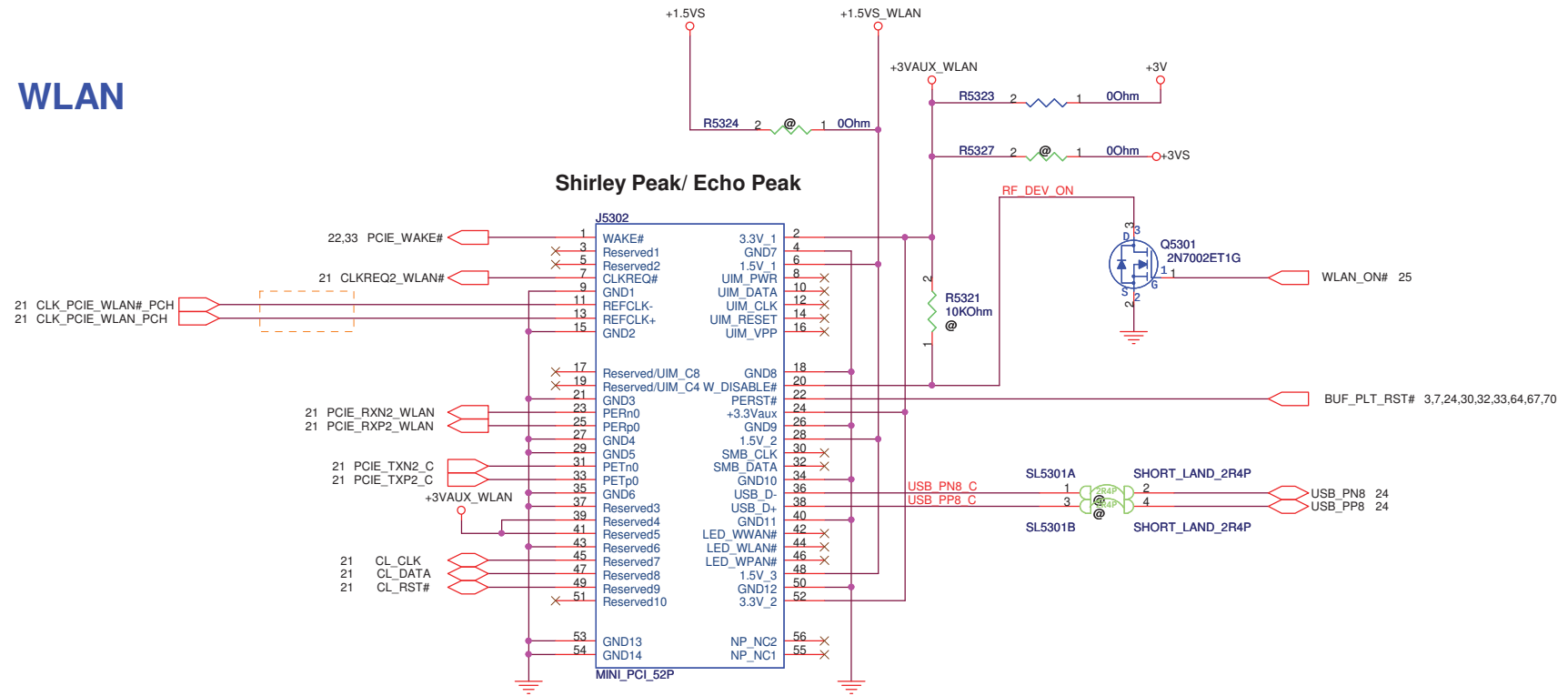


HDD (1st) Left side





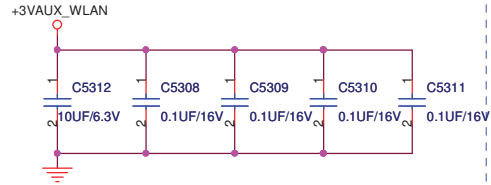
WLAN



WLAN +3VAUX bypass capacitor:

Place 0.1uF near pin 2, 24, 52, 39 41.

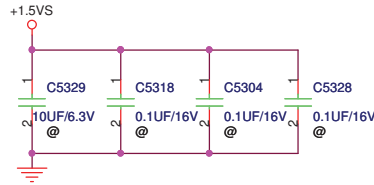
Place 10uF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capacitor:

Place 0.1uF near pin 6, 28, 48.

Place 10uF near +1.5VS source side.

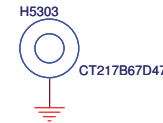


WLAN nuts:

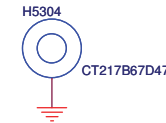
Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.



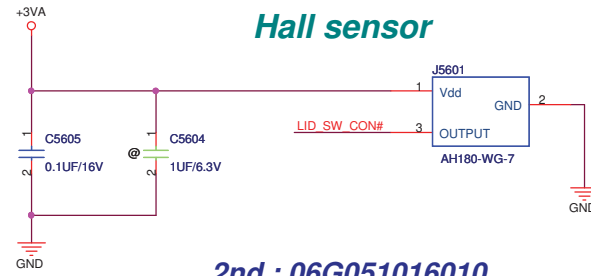
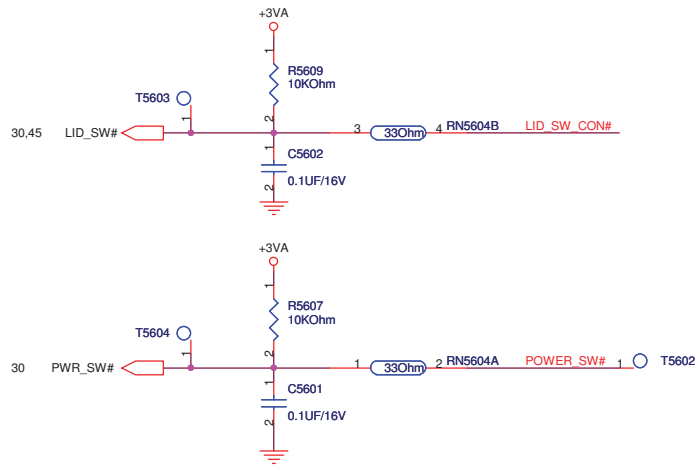
13G021043011



13G021043011

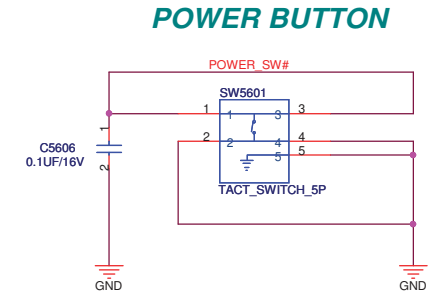
2ND : 13G021085000

ASUS		Title :MINICARD(WLAN)	
ASUSTeK COMPUTER INC. NB6		Engineer: Jerry Mou	
Size	Project Name	Rev	
Custom	K72Jr	2.0	
Date: Friday, December 11, 2009		Sheet	53 of 100



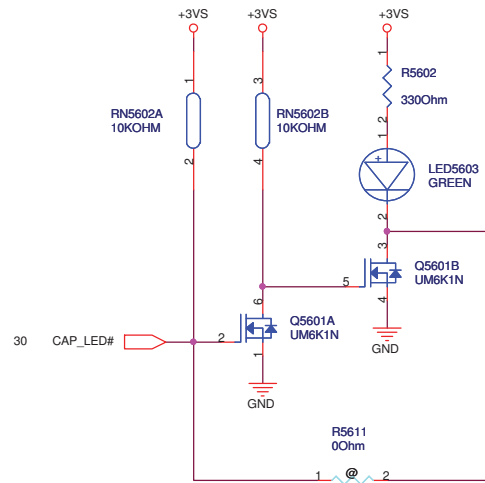
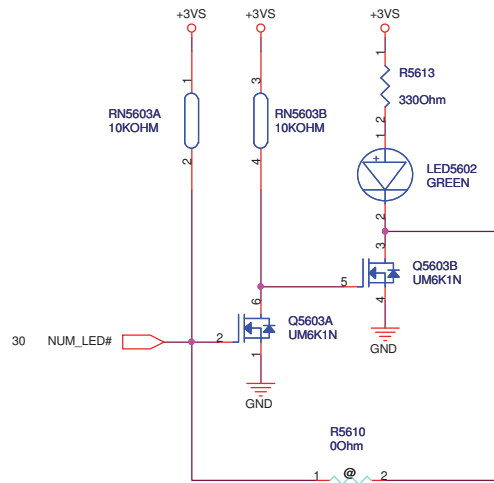
2nd : 06G051016010

(3rd : 06G036022010)



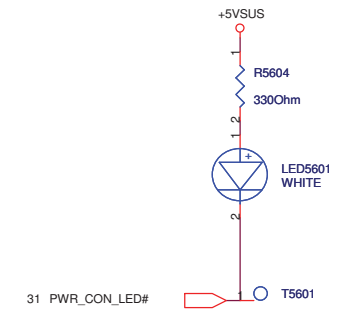
2nd : 07G015200351

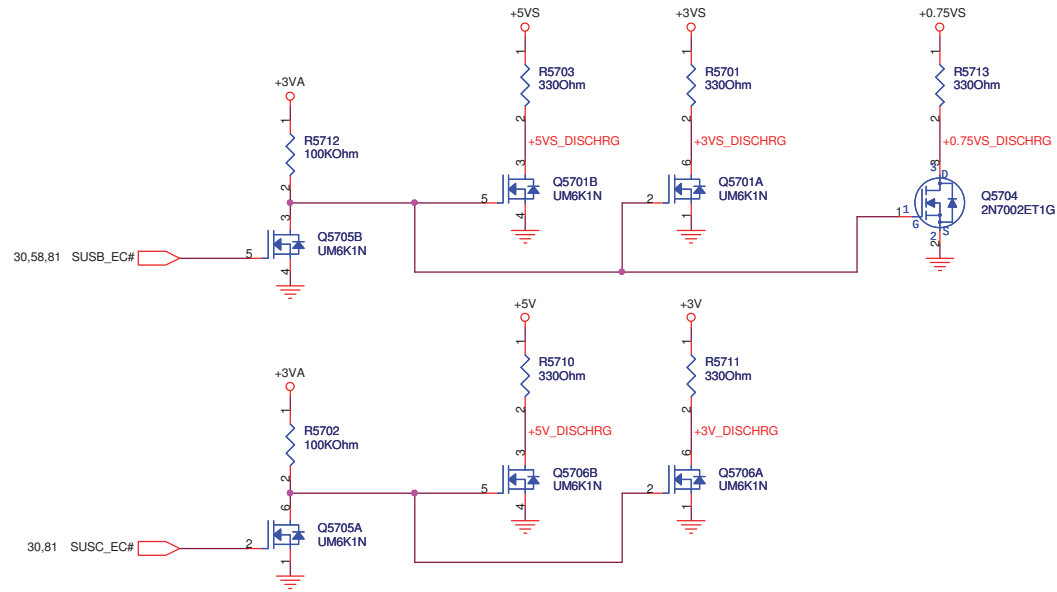
(3rd : 07G015500051)

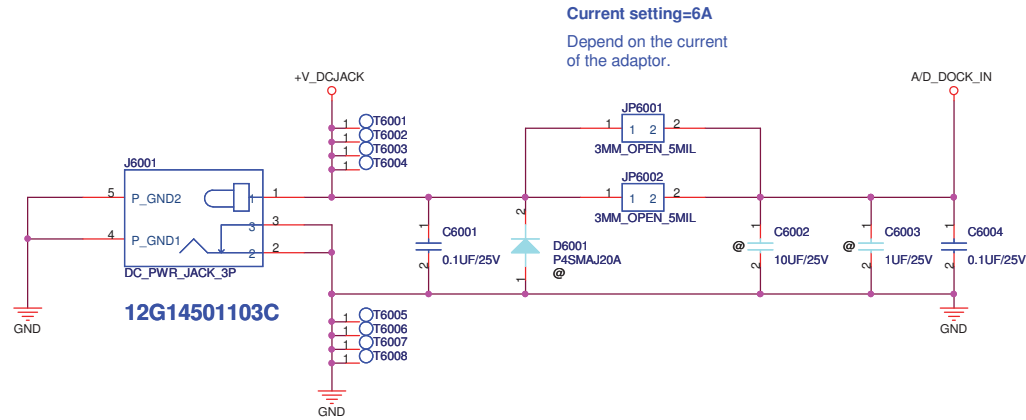


2nd : 07G01570130A

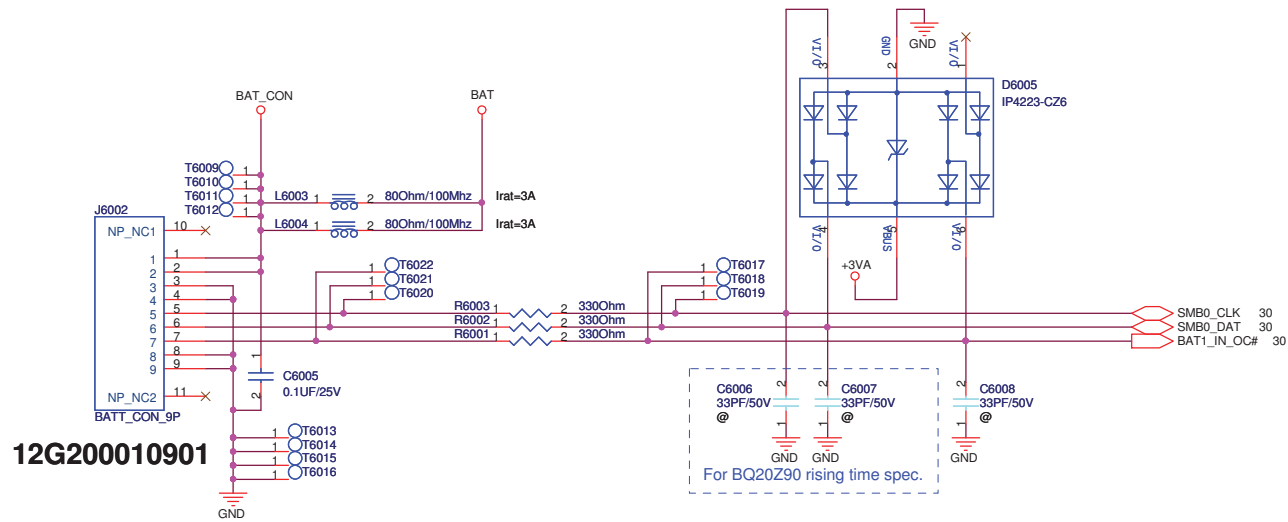
(3rd : 07G015L0042A)







DC Jack

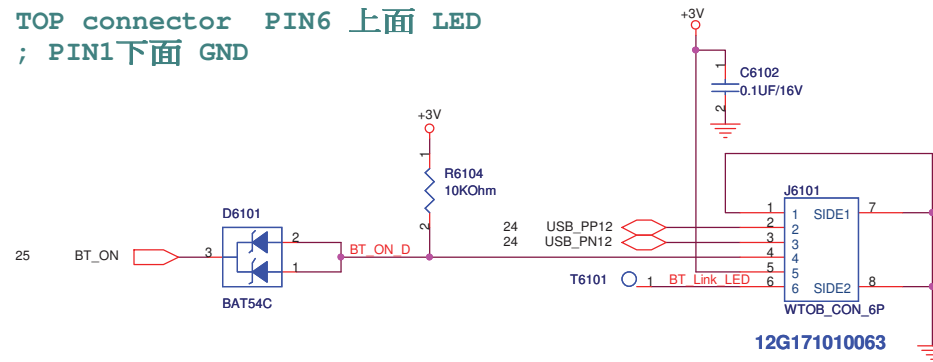


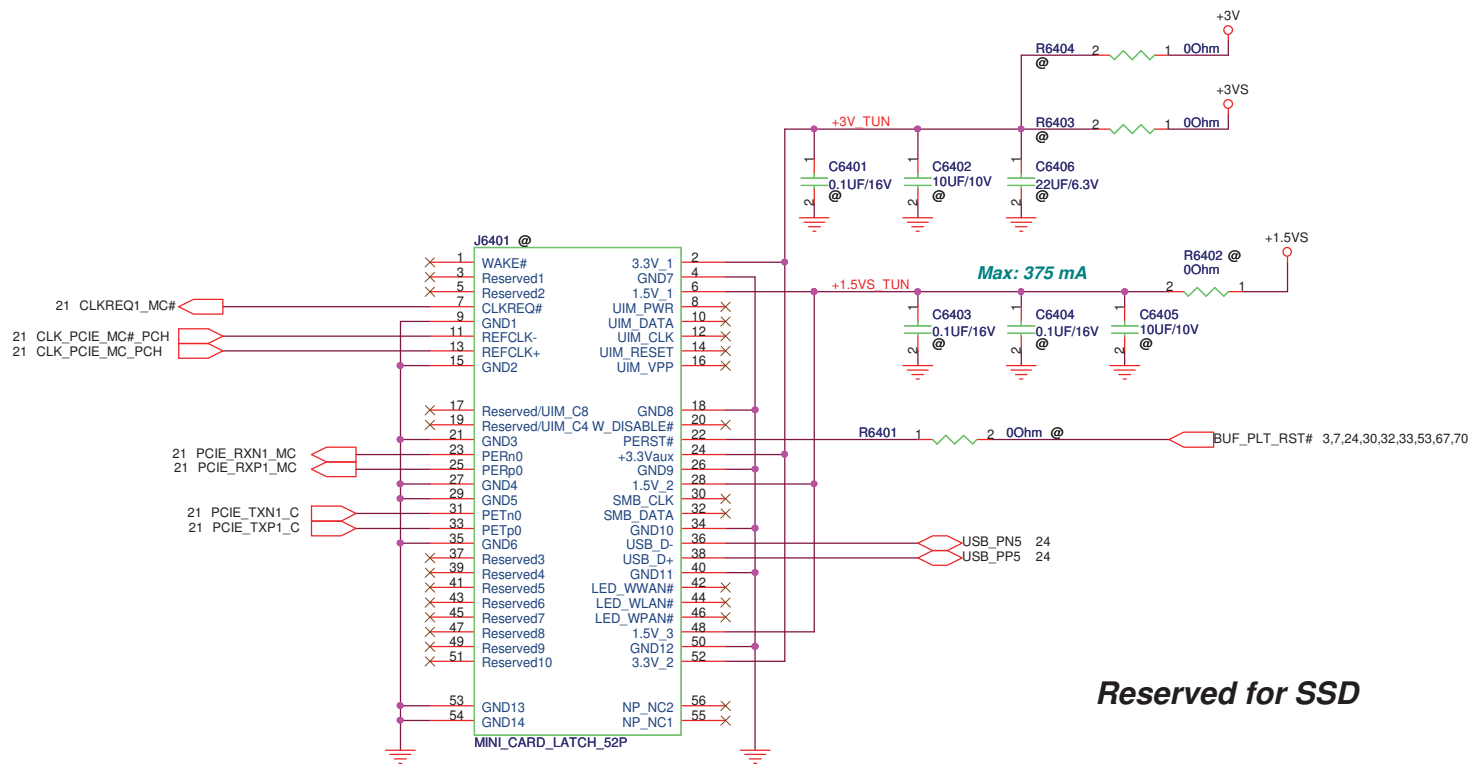
Battery Connector

ASUS		Title : DC_DC & BAT Conn.	
ASUSTeK COMPUTER INC. NB4		Engineer: Ryan_Wang	
Size B	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009		Sheet	60 of 100

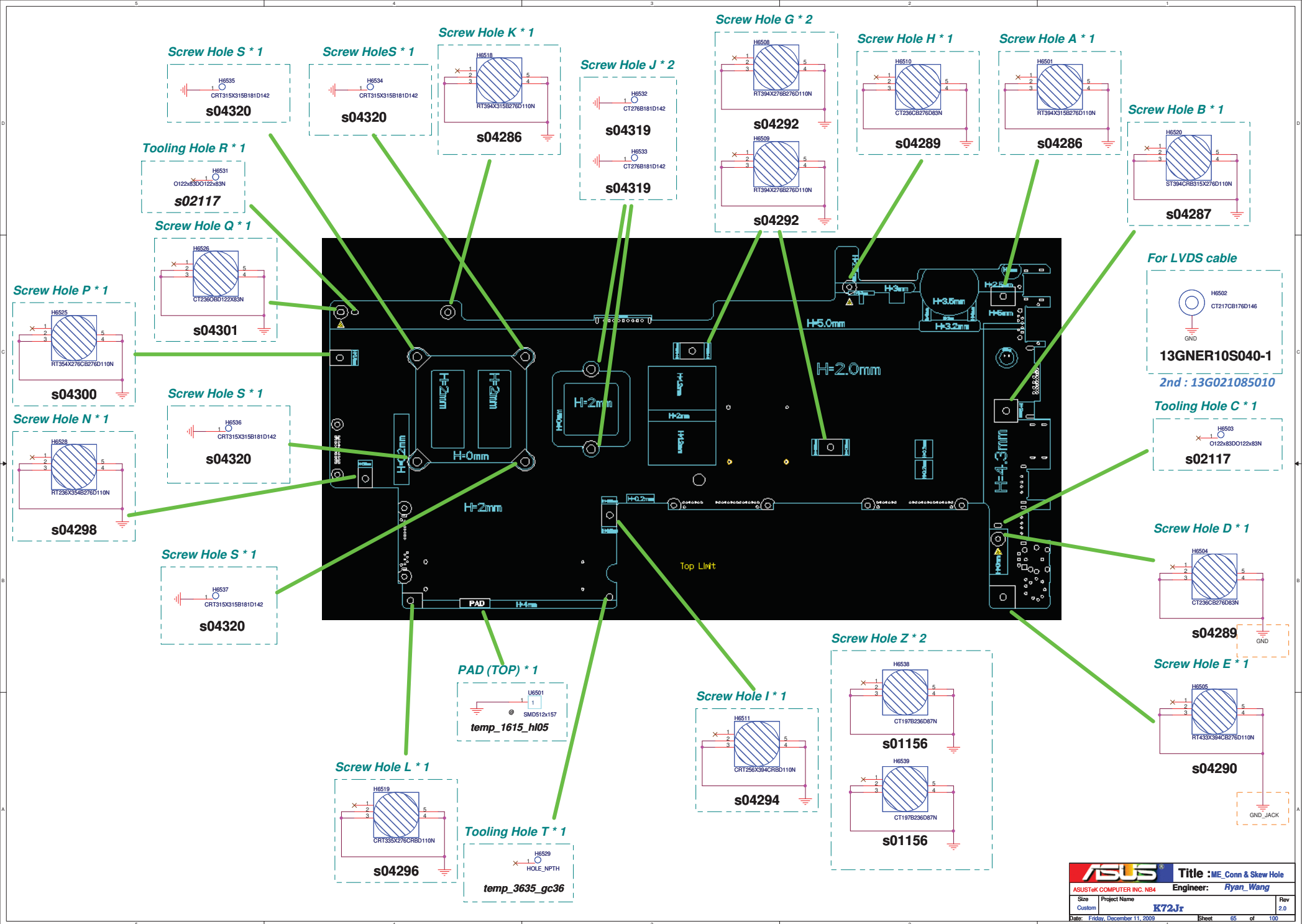
BLUETOOTH

TOP connector PIN6 上面 LED
; PIN1下面 GND

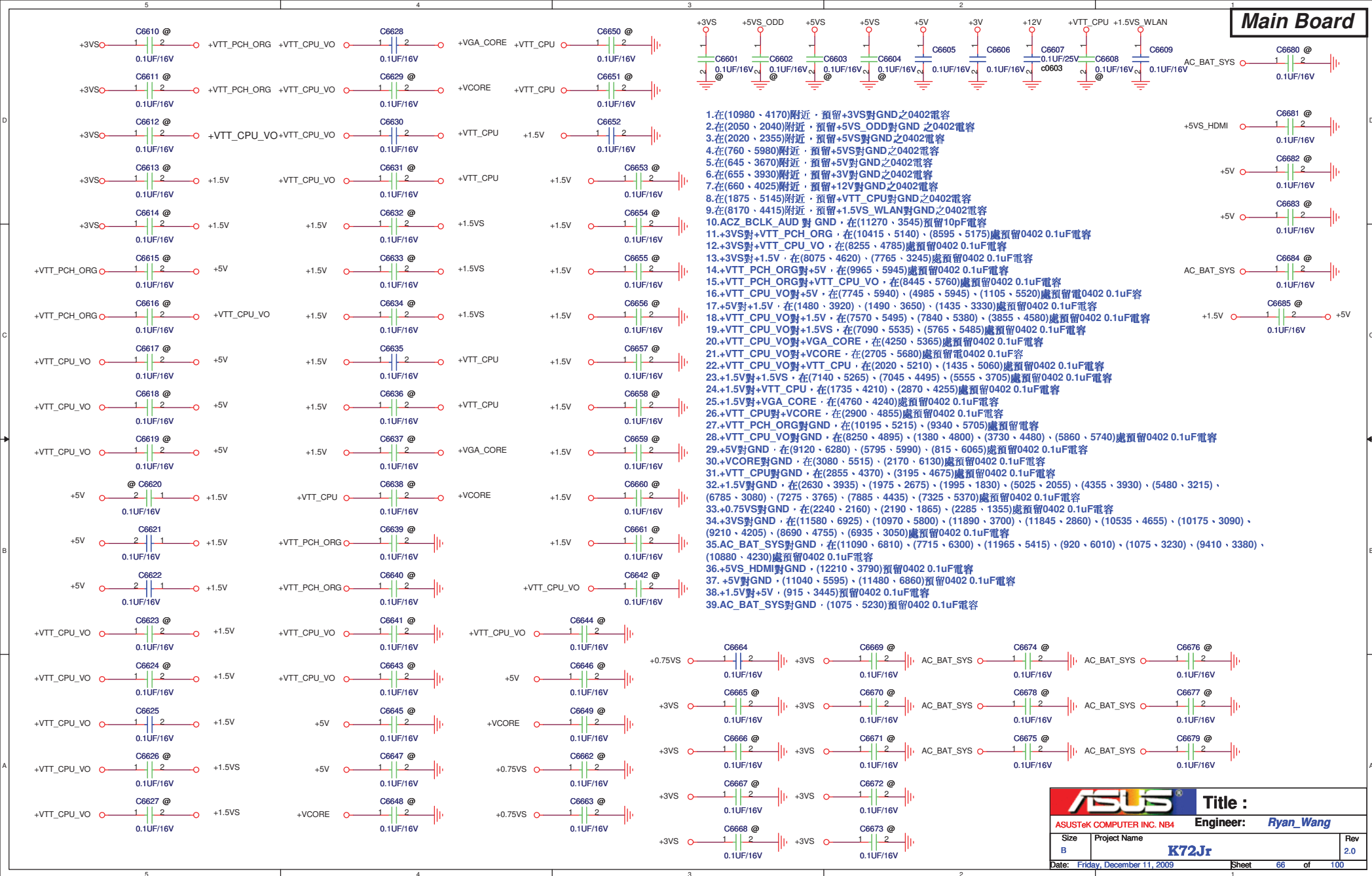




		Title :	
ASUSTeK COMPUTER INC. NB4		Engineer: <i>Ryan_Wang</i>	
Size Custom	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009		Sheet	64 of 100



Main Board



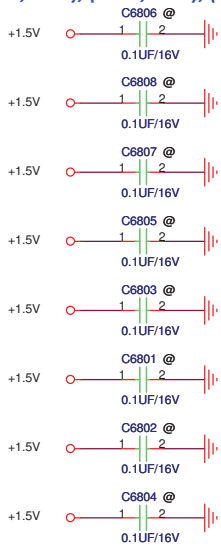
The diagram shows the J6701 connector with the following connections:

- Pin 1:** T6741
- Pin 2:** T6742
- Pin 3:** T6743
- Pin 4:** PCH_JTAG_RST#_R (39)
- Pin 5:** ALL_SYSTEM_PWRGD 22,30,58 (54)
- Pin 6:** PCH_JTAG_TDO_R (52)
- Pin 7:** PCH_JTAG_TDI_R (56)
- Pin 8:** PCH_JTAG_TMS_R (58)
- Pin 9:** PCH_JTAG_TCK_R (57)
- Pin 10:** T6744
- Pin 11:** T6745
- Pin 12:** T6746
- Pin 13:** T6747
- Pin 14:** T6748
- Pin 15:** T6749
- Pin 16:** XDP_DBRESET# 3,7,22 (48)
- Pin 17:** BUF_PLT_RST# 3,7,24,30,32,33,53,64,76 (49)
- Pin 18:** SMB_DAT_S 7,16,17,19,28,29
- Pin 19:** SMB_CLK_S 7,16,17,19,28,29
- Pin 20:** T6750
- Pin 21:** T6751
- Pin 22:** T6750
- Pin 23:** T6751
- Pin 24:** T6750
- Pin 25:** T6751
- Pin 26:** T6750
- Pin 27:** T6751
- Pin 28:** T6750
- Pin 29:** T6751
- Pin 30:** T6750

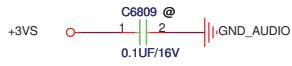
The +3VS power rail is connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30.

20	PCH_JTAG_TCK		R6723	1	2	00hm	/XDP	PCH_JTAG_TCK_R
20	PCH_JTAG_TMS		R6721	1	2	00hm	/XDP	PCH_JTAG_TMS_R
20	PCH_JTAG_TDI		R6722	1	2	00hm	/XDP	PCH_JTAG_TDI_R
20	PCH_JTAG_TDO		R6724	1	2	00hm	/XDP	PCH_JTAG_TDO_R
20	PCH_JTAG_RST#		R6725	1	2	00hm	/XDP	PCH_JTAG_RST#_R

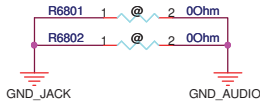
2009/8/25
1.5V對GND, (1975,4025), (3250,4075), (3325,2310), (3870,2300), (3445,1720), (3735,1805), (3225,1420), (3635,1500)預留0402 電容



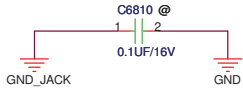
INT_MIC 跨 +3VS & GND_Audio 在in2切割，預留+3VS對GND_AUDIO 電容



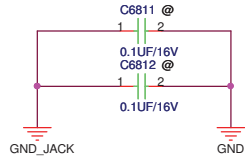
GND_Jack對GND_AUDIO 留0 歐姆電阻: (11990, 2240), (11895, 1695)



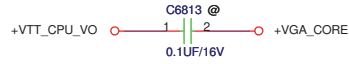
GND_Jack對GND: (12015, 2405)預留電容



GND_audio對GND: (11655, 2495), (11655, 2200)預留電容



+VTT_CPU_VO對+VGA_Core: (5310, 5430)預留電容

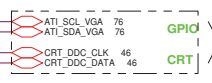
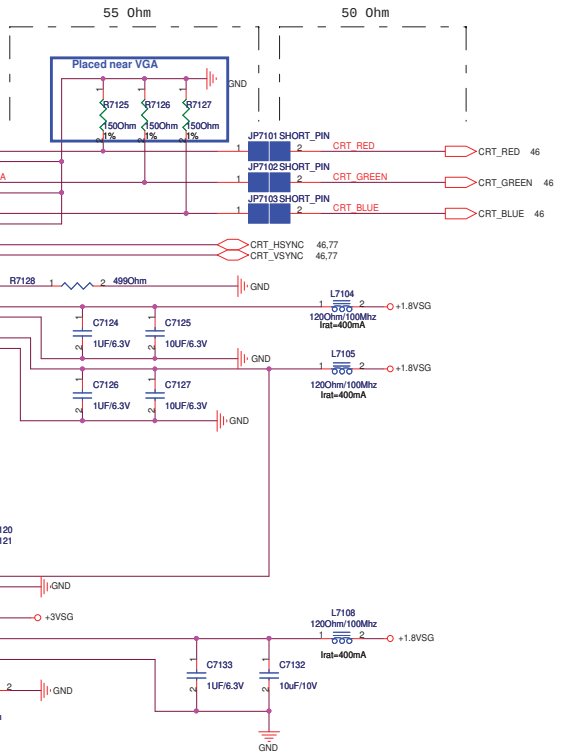
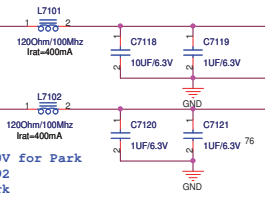
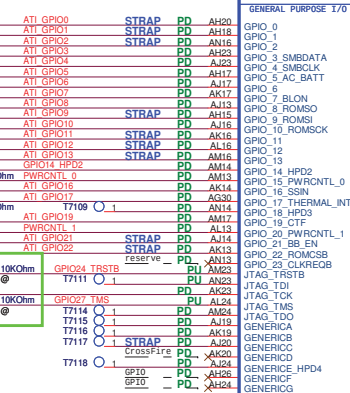
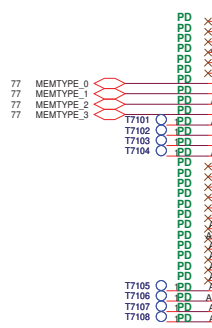


+5V對+VTT_CPU_VO:(2565, 5990)預留電容



ASUS®		Title : OTH_LCM	
ASUSTeK COMPUTER INC. NB4		Engineer: Ryan_Wang	
Size B	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009		Sheet 68	of 100

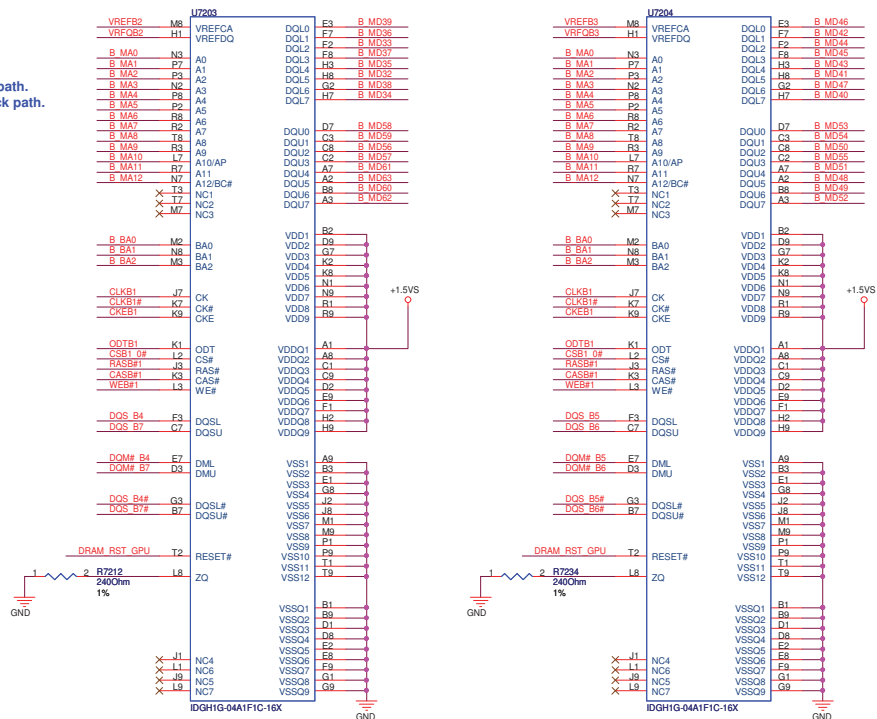




Need pulled high(3.3V or 5V) before VDDC is powered up

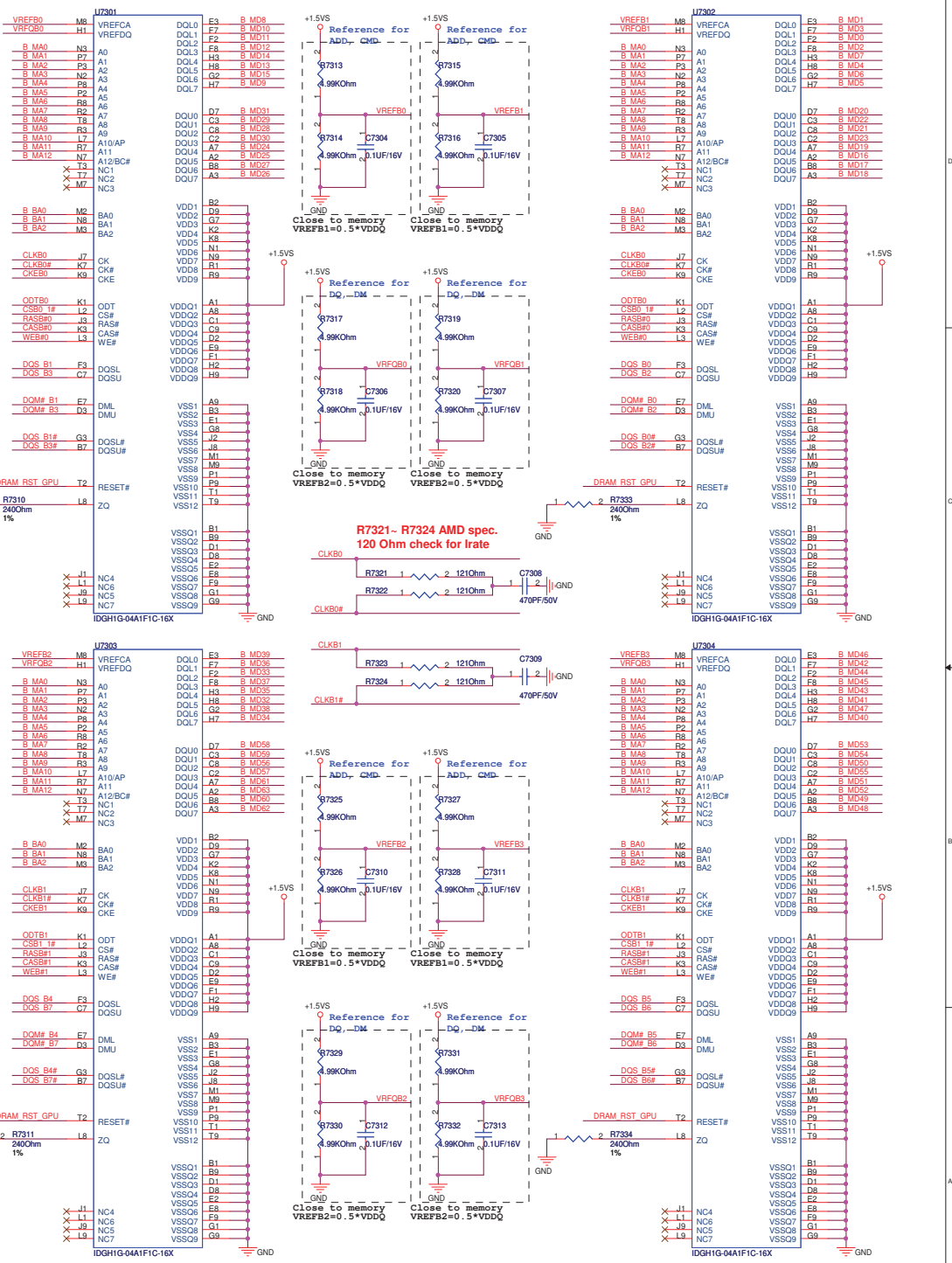
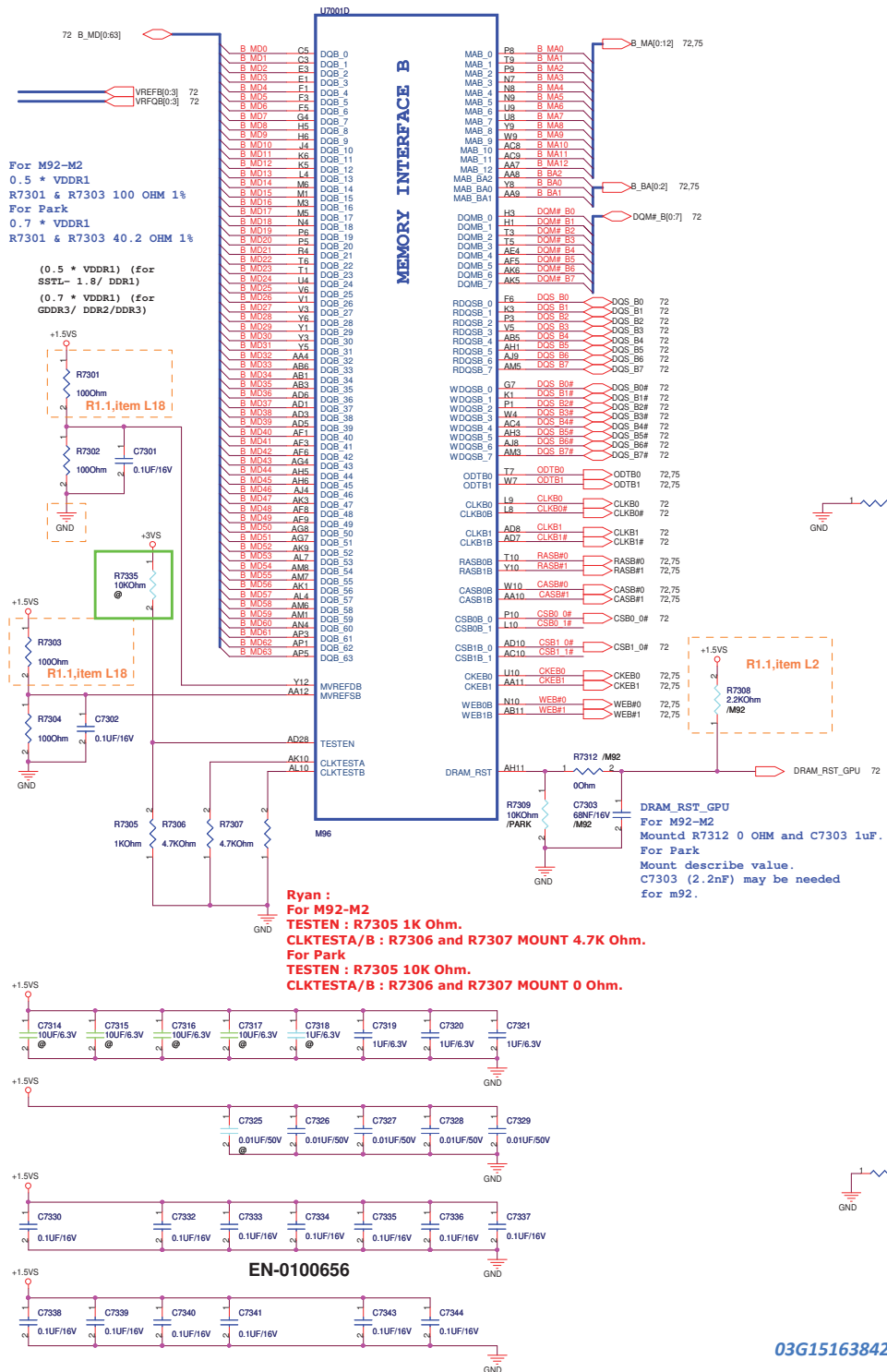
	B_MDIO[6:3]	73
	B_MIO[14:1]	73,75
	B_BA0[2]	73,75
	DOMM_B[0:7]	73
	VREFB[0:3]	73
	VREFCB[0:3]	73
	ODS_B0	73
	ODS_B1	73
	ODS_B2	73
	ODS_B3	73
	ODS_B4	73
	ODS_B5	73
	ODS_B6	73
	ODS_B7	73
	ODS_B0#	73
	ODS_B1#	73
	ODS_B2#	73
	ODS_B3#	73
	ODS_B4#	73
	ODS_B5#	73
	ODS_B6#	73
	ODS_B7#	73
	ODTB0	73,75
	ODTB1	73,75
	CLKB0	73
	CLKB0#	73
	CLKB1	73
	CLKB1#	73
	RASB0	73,75
	RASB1	73,75
	CASB0	73,75
	CASB1	73,75
	KEB0	73,75
	KEB1	73,75
	WEB0	73,75
	WEB1	73,75
	CSB0_0#	73
	CSB1_0#	73
	CSB0_RST_GPU	73
	CSB1_RST_GPU	73

C37		D24	
C35	D0A 0	MAA 0	H24
C34	D0A 1	MAA 1	H23
C33	D0A 2	MAA 2	H22
C32	D0A 3	MAA 3	H21
C31	D0A 4	MAA 4	H20
C30	D0A 5	MAA 5	H19
C29	D0A 6	MAA 6	H18
C28	D0A 7	MAA 7	H17
C27	D0A 8	MAA 8	H16
C26	D0A 9	MAA 9	H15
C25	D0A 10	MAA 10	H14
C24	D0A 11	MAA 11	H13
C23	D0A 12	MAA 12	H12
C22	D0A 13	MAA 13	H11
C21	D0A 14	MAA 14	H10
C20	D0A 15	MAA 15	H09
C19	D0A 16	MAA, BA1	H08
C18	D0A 17		
C17	D0A 18	DOMA 0	C32
C16	D0A 19	DOMA 1	D23
C15	D0A 20	DOMA 2	E22
C14	D0A 21	DOMA 3	F21
C13	D0A 22	DOMA 4	G20
C12	D0A 23	DOMA 5	H19
C11	D0A 24	DOMA 6	I18
C10	D0A 25	DOMA 7	J17
C09	D0A 26		
C08	D0A 27	ROSA 0	C31
C07	D0A 28	ROSA 1	D22
C06	D0A 29	ROSA 2	E21
C05	D0A 30	ROSA 3	F20
C04	D0A 31	ROSA 4	G19
C03	D0A 32	ROSA 5	H18
C02	D0A 33	ROSA 6	I17
C01	D0A 34	ROSA 7	J16
C00	D0A 35	WOGSA 0	A34
		WOGSA 1	E33
		WOGSA 2	F32
		WOGSA 3	G31
		WOGSA 4	H30
		WOGSA 5	I29
		WOGSA 6	J28
		WOGSA 7	
		ODTA0	J21
		ODTA1	K20
		CLKA0	H27
		CLKA0B	G27
		CLKA1	J14
		CLKA1B	K13
		RASAB0	K20
		RASAB1	K19
		CASAB0	K24
		CASAB1	K23
		CASOB 0	K24
		CASOB 1	K23
		CASIB 0	M13
		CASIB 1	K16
		CKEAD	K26
		CKEAI	L15
		RSVD 1	AF28
		RSVD 2	AG28
		RSVD 3	AL34

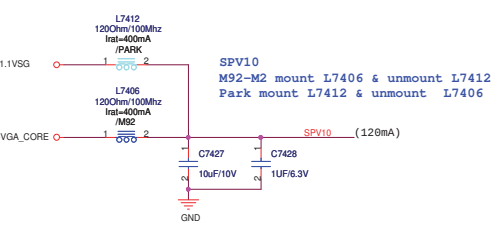
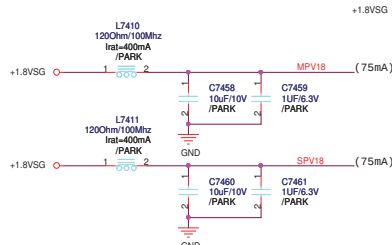
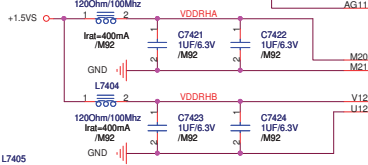
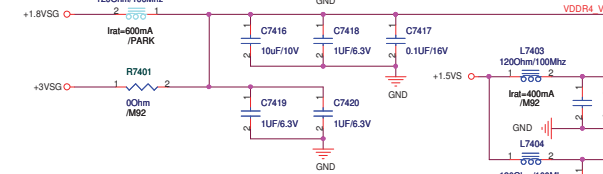
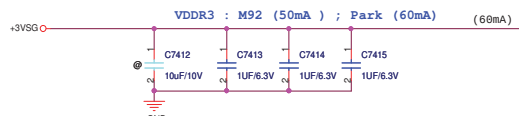
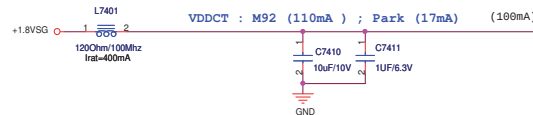
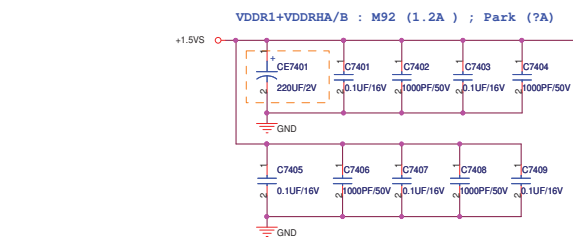


		Title : VRAM RANK0	
ASUSTek COMPUTER INC. NBD4		Engineer: Jerry Mou	
Size C	Project Name K72Jr		Rev 2.0
Date: Friday, January 22, 2010		Sheet 72 of 100	

Channel B: Dual 1GB Rank DDR3 (Rank1)



03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C



HEM I/O

AG7	VDDR1_1
AG8	VDDR1_2
AG9	VDDR1_3
AG10	VDDR1_4
AG11	VDDR1_5
AG12	VDDR1_6
AG13	VDDR1_7
AG14	VDDR1_8
AG15	VDDR1_9
AG16	VDDR1_10
AG17	VDDR1_11
AG18	VDDR1_12
AG19	VDDR1_13
AG20	VDDR1_14
AG21	VDDR1_15
AG22	VDDR1_16
AG23	VDDR1_17
AG24	VDDR1_18
AG25	VDDR1_19
AG26	VDDR1_20
AG27	VDDR1_21
AG28	VDDR1_22
AG29	VDDR1_23
AG30	VDDR1_24
AG31	VDDR1_25
AG32	VDDR1_26
AG33	VDDR1_27
AG34	VDDR1_28
AG35	VDDR1_29
AG36	VDDR1_30
AG37	VDDR1_31
AG38	VDDR1_32
AG39	VDDR1_33
AG40	VDDR1_34

LEVEL TRANSLATION

AF26	VDD_CT_1
AF27	VDD_CT_2
AF28	VDD_CT_3

I/O

AF23	VDDR3_1
AF24	VDDR3_2
AF25	VDDR3_3
AF26	VDDR3_4
AF27	VDDR3_5
AF28	VDDR3_6
AF29	VDDR3_7
AF30	VDDR3_8
AF31	VDDR3_9
AF32	VDDR3_10
AF33	VDDR3_11
AF34	VDDR3_12
AF35	VDDR3_13
AF36	VDDR3_14
AF37	VDDR3_15
AF38	VDDR3_16
AF39	VDDR3_17
AF40	VDDR3_18
AF41	VDDR3_19
AF42	VDDR3_20
AF43	VDDR3_21
AF44	VDDR3_22
AF45	VDDR3_23
AF46	VDDR3_24
AF47	VDDR3_25
AF48	VDDR3_26
AF49	VDDR3_27
AF50	VDDR3_28
AF51	VDDR3_29
AF52	VDDR3_30
AF53	VDDR3_31
AF54	VDDR3_32
AF55	VDDR3_33
AF56	VDDR3_34

HEM CLK

M20	VDDR4_1
M21	VDDR4_2
M22	VDDR4_3
M23	VDDR4_4

PLL

AB37	PCIE_PVDD
H7	NC_MPV18_1
H8	NC_MPV18_2
H9	NC_MPV18_3

BACK BIOS

AM10	SPV10
AM11	SPV10
AM12	SPV10

For M92-M2
VDDR4 or VDDR5 can be +3.3V or +1.8V
For Park
VDDR4 and VDDR5 must be +1.8V

VDDR4_VDDR5 : 3.3V for M92 ; 1.8V for Park
M92-M2 mount R7401& unmount L7402
Park mount L7402 & unmount R7401

POWER

PCIE

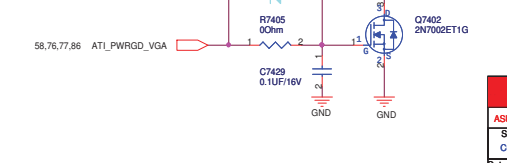
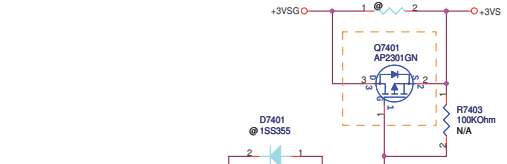
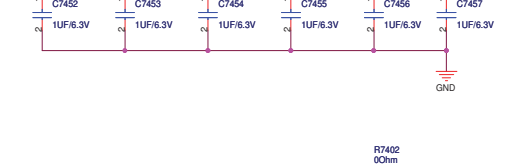
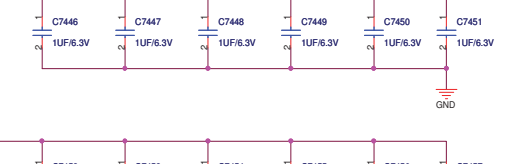
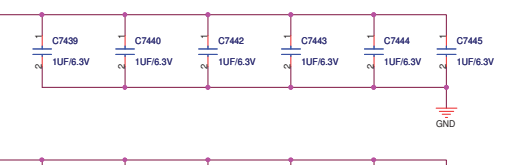
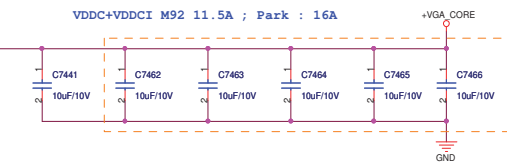
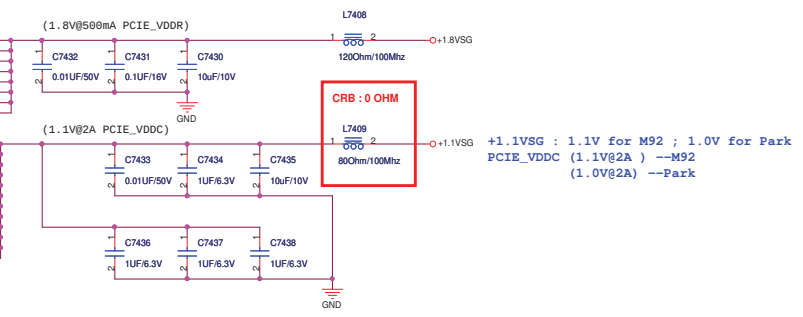
PCIE_VDDR_1	AA31
PCIE_VDDR_2	AA32
PCIE_VDDR_3	AA33
PCIE_VDDR_4	AA34
PCIE_VDDR_5	AA35
PCIE_VDDR_6	AA36
PCIE_VDDR_7	AA37
PCIE_VDDR_8	AA38
PCIE_VDDR_9	AA39
PCIE_VDDR_10	AA40
PCIE_VDDR_11	AA41
PCIE_VDDR_12	AA42
PCIE_VDDR_13	AA43
PCIE_VDDR_14	AA44
PCIE_VDDR_15	AA45
PCIE_VDDR_16	AA46
PCIE_VDDR_17	AA47
PCIE_VDDR_18	AA48
PCIE_VDDR_19	AA49
PCIE_VDDR_20	AA50
PCIE_VDDR_21	AA51
PCIE_VDDR_22	AA52
PCIE_VDDR_23	AA53
PCIE_VDDR_24	AA54
PCIE_VDDR_25	AA55
PCIE_VDDR_26	AA56
PCIE_VDDR_27	AA57
PCIE_VDDR_28	AA58
PCIE_VDDR_29	AA59
PCIE_VDDR_30	AA60
PCIE_VDDR_31	AA61
PCIE_VDDR_32	AA62
PCIE_VDDR_33	AA63
PCIE_VDDR_34	AA64

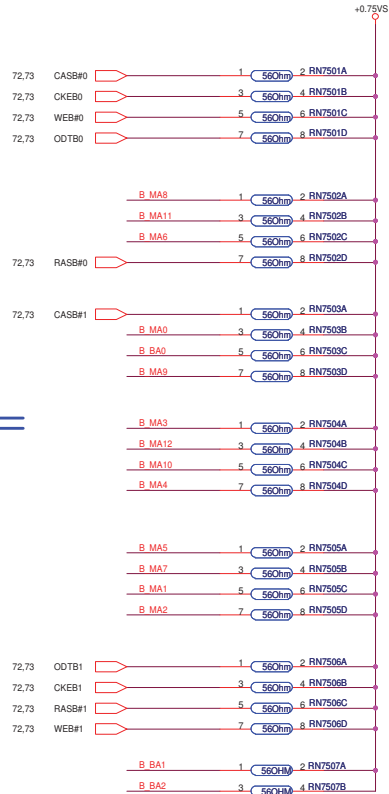
CORE

VDDC_1	AA15
VDDC_2	AA16
VDDC_3	AA17
VDDC_4	AA18
VDDC_5	AA19
VDDC_6	AA20
VDDC_7	AA21
VDDC_8	AA22
VDDC_9	AA23
VDDC_10	AA24
VDDC_11	AA25
VDDC_12	AA26
VDDC_13	AA27
VDDC_14	AA28
VDDC_15	AA29
VDDC_16	AA30
VDDC_17	AA31
VDDC_18	AA32
VDDC_19	AA33
VDDC_20	AA34
VDDC_21	AA35
VDDC_22	AA36
VDDC_23	AA37
VDDC_24	AA38
VDDC_25	AA39
VDDC_26	AA40
VDDC_27	AA41
VDDC_28	AA42
VDDC_29	AA43
VDDC_30	AA44
VDDC_31	AA45
VDDC_32	AA46
VDDC_33	AA47
VDDC_34	AA48
VDDC_35	AA49
VDDC_36	AA50
VDDC_37	AA51
VDDC_38	AA52
VDDC_39	AA53
VDDC_40	AA54
VDDC_41	AA55
VDDC_42	AA56
VDDC_43	AA57
VDDC_44	AA58
VDDC_45	AA59
VDDC_46	AA60
VDDC_47	AA61
VDDC_48	AA62
VDDC_49	AA63
VDDC_50	AA64
VDDC_51	AA65
VDDC_52	AA66
VDDC_53	AA67
VDDC_54	AA68
VDDC_55	AA69
VDDC_56	AA70
VDDC_57	AA71
VDDC_58	AA72
VDDC_59	AA73
VDDC_60	AA74
VDDC_61	AA75
VDDC_62	AA76
VDDC_63	AA77
VDDC_64	AA78
VDDC_65	AA79
VDDC_66	AA80
VDDC_67	AA81
VDDC_68	AA82
VDDC_69	AA83
VDDC_70	AA84
VDDC_71	AA85
VDDC_72	AA86
VDDC_73	AA87
VDDC_74	AA88
VDDC_75	AA89
VDDC_76	AA90
VDDC_77	AA91
VDDC_78	AA92
VDDC_79	AA93
VDDC_80	AA94
VDDC_81	AA95
VDDC_82	AA96
VDDC_83	AA97
VDDC_84	AA98
VDDC_85	AA99
VDDC_86	AA100

ISOLATED CORE I/O

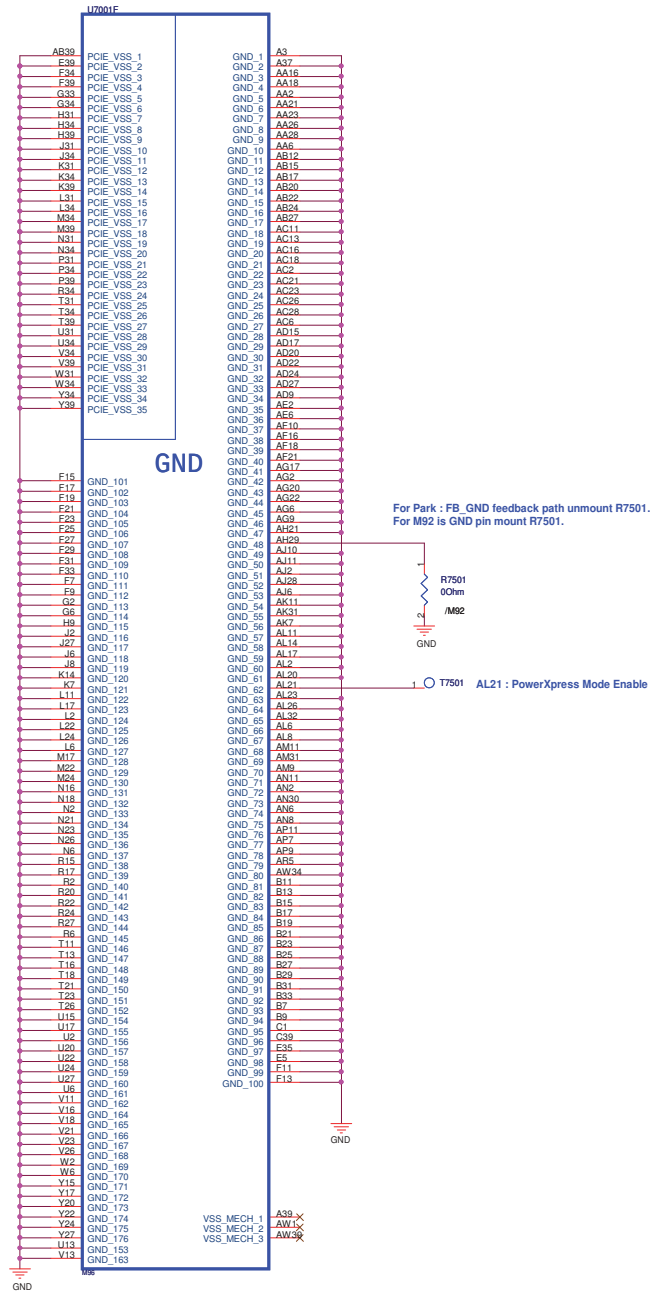
VDDCI_1	M15
VDDCI_2	M16
VDDCI_3	M17
VDDCI_4	M18





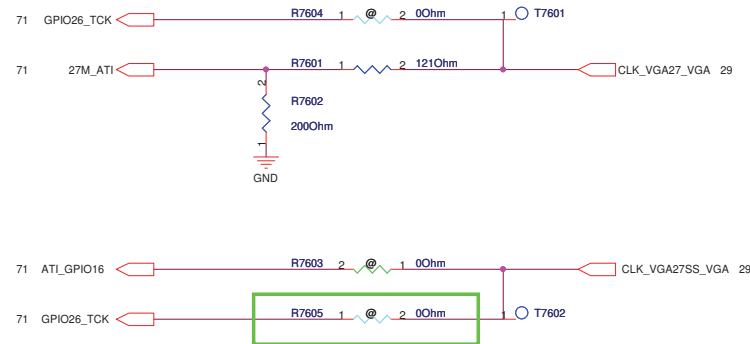
72.73 B_MA[0:12]

72.73 B_BA[0:2]

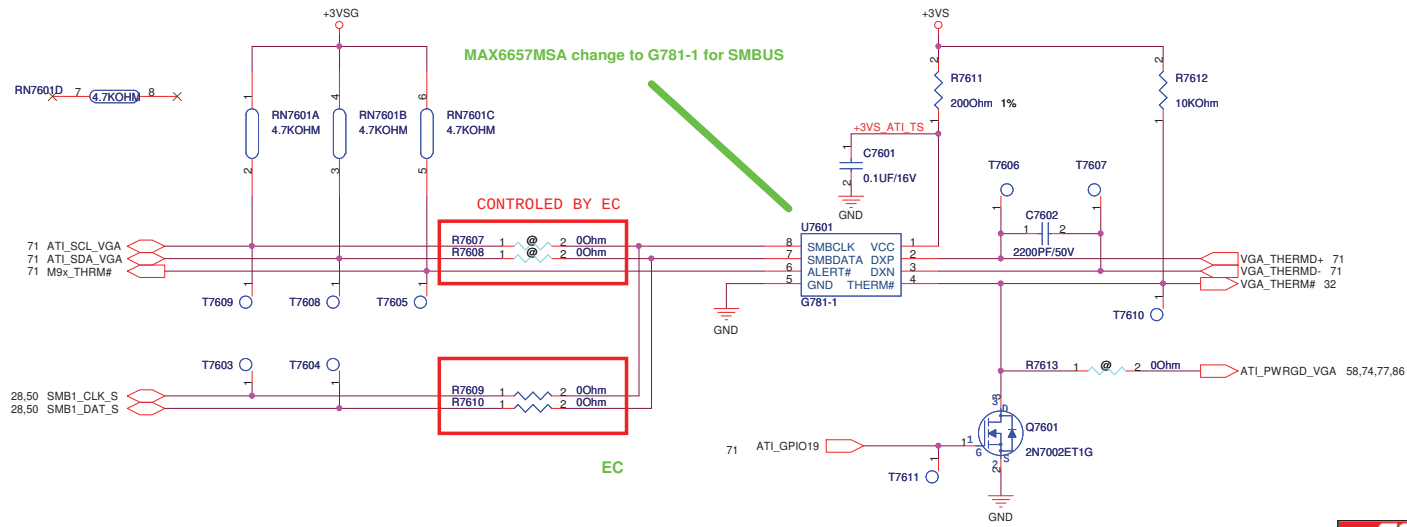


Memory Clock SS (Reserved)

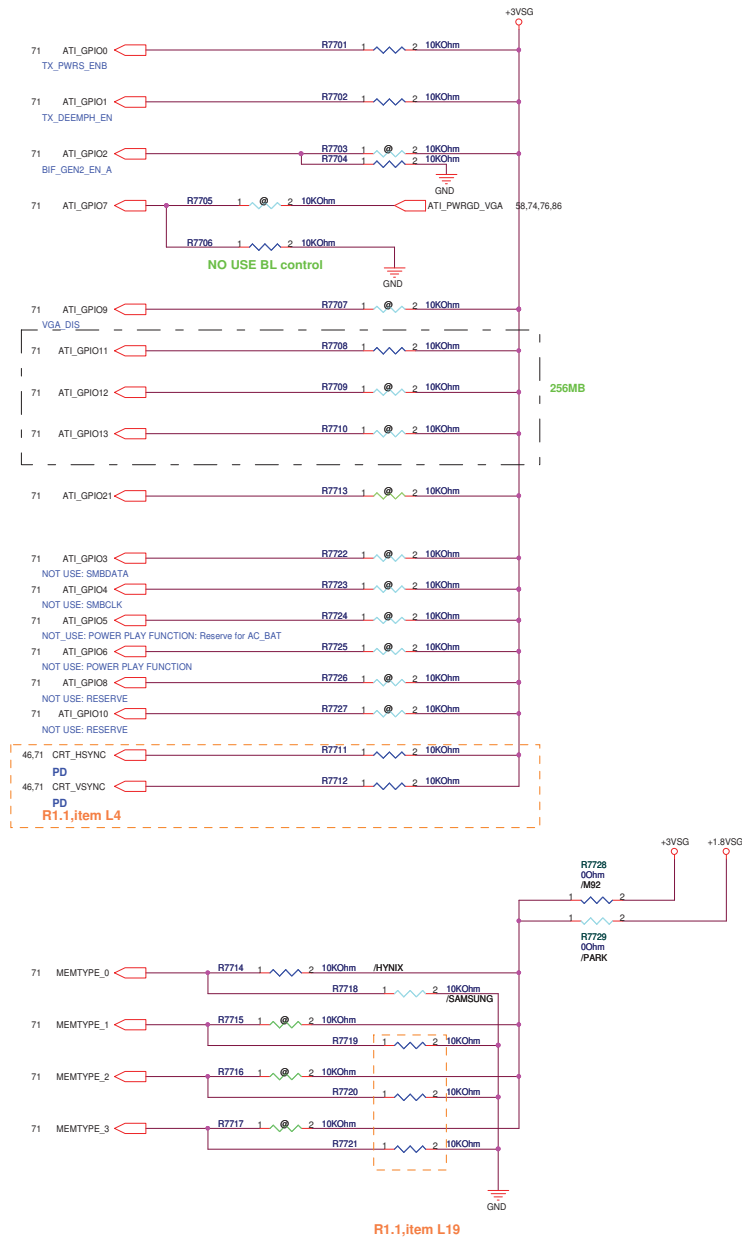
S0 (Spread Percentage Select):
GND: TBD%
VDD: TBD% (default PU)
NC : TBD%



	SMBUS SLAVE ADDRESS
G781	98 (1 0 0 1 1 0 0)
G781-1	9A (1 0 0 1 1 0 1)



OPTION STRAPS



VDD4_VDDR5 : 3.3V for M92 ; 1.8V for Park
M92-M2 mount R7401& unmount L7402
Park mount L7402 & unmount R7401

M92 Straps

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
VIP_DEVICE_STRAP_EN	V2SYNC	0 - Ignore VIP device straps (DVPDATA_20) 1 - Use VIP device straps (DVPDATA_20)	0 (internal pull-down)
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: Full Tx output swing This setting can only be used if the PCIe bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled	0 (internal pull-down)
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1, then Config(2:0) defines the ROM type. If BIOS_ROM_EN=0, then Config(2:0) defines the primary memory aperture size. 128MB---x000 32MB---Not Support 2GB---Not Support 256MB---x001 512MB---Not Support 4GB---Not Support 64MB---x010 1GB---Not Support	0000 (internal pull-down)
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
AUD[1] AUD[0]	PEG_CRT_HSYNC_VGA PEG_CRT_VSYNC_VGA	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI	0 (internal pull-down)
Reserved	H2SYNC GPIO 21_BB_EN GENERICC	ATI internal use only . THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

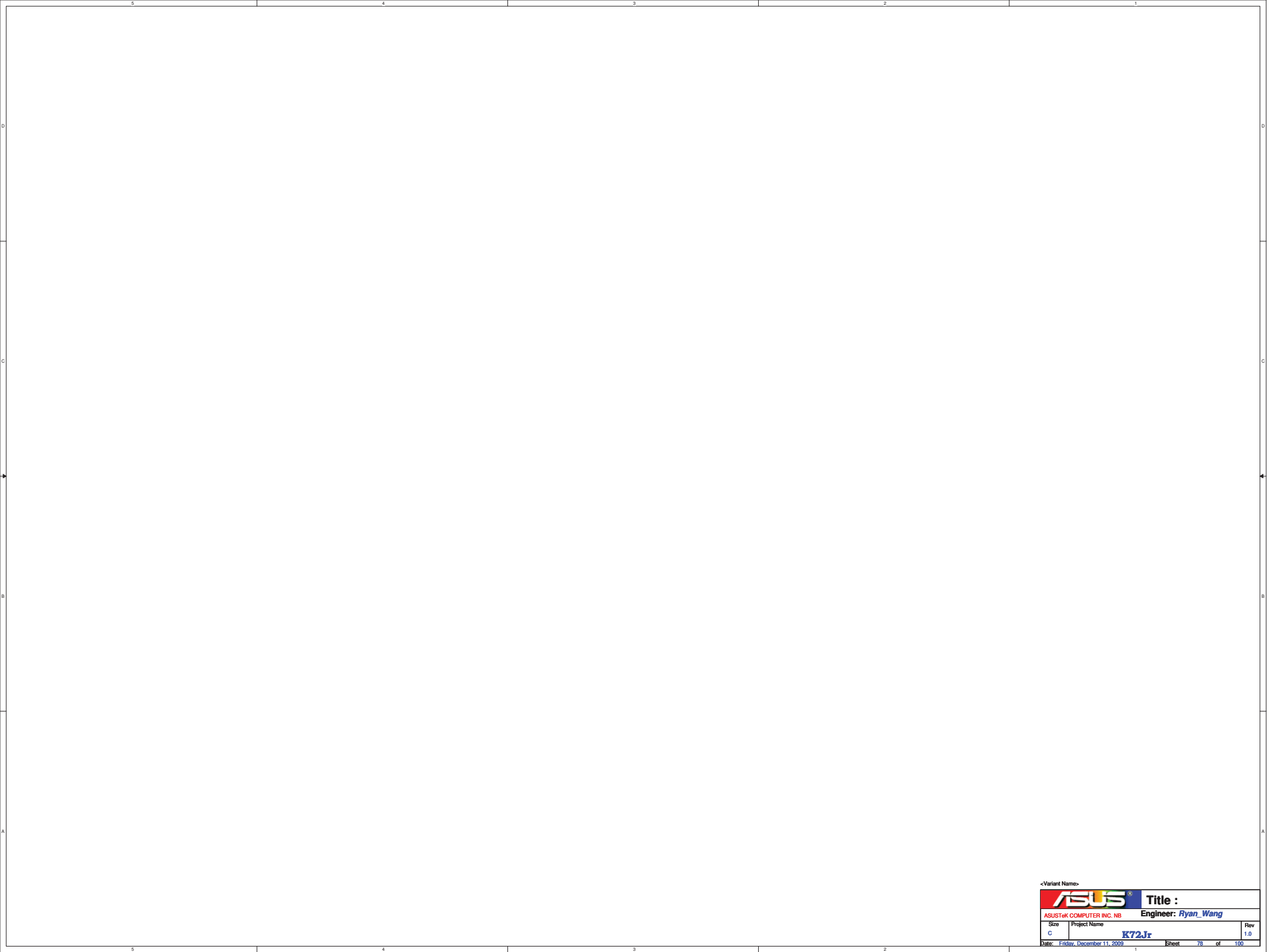
AUDIO_EN	VIP_3	Enable HD Audio function in the PCI configuration space 0 - Disable HD Audio 1 - Enable HD Audio	0 (internal pull-down)
64BAR_EN_A	VIP_5	Enable 64-bit BARs Most commonly this strap is left at the default (32-bit BARs)	0 (internal pull-down)
MSI_DIS	VIP_1	Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present	0 (internal pull-down)
VIP_DEVICE	VHAD_0	VIP_DEVICE_STRAP_EN is set 0 =>not used VIP Host interface VIP_DEVICE_STRAP_EN is set 1 =>used VIP Host interface	0 (internal pull-down)
DEBUG ACCESS	GPIO4	Debug_access strap 3.3V ---ON 0V ---OFF	0 (internal pull-down)
DEBUG_L2C_ENABLE	GPIO6	ATI internal use only . Other logic must not affect this signal during RESET Recommended to 0	0 (internal pull-down)

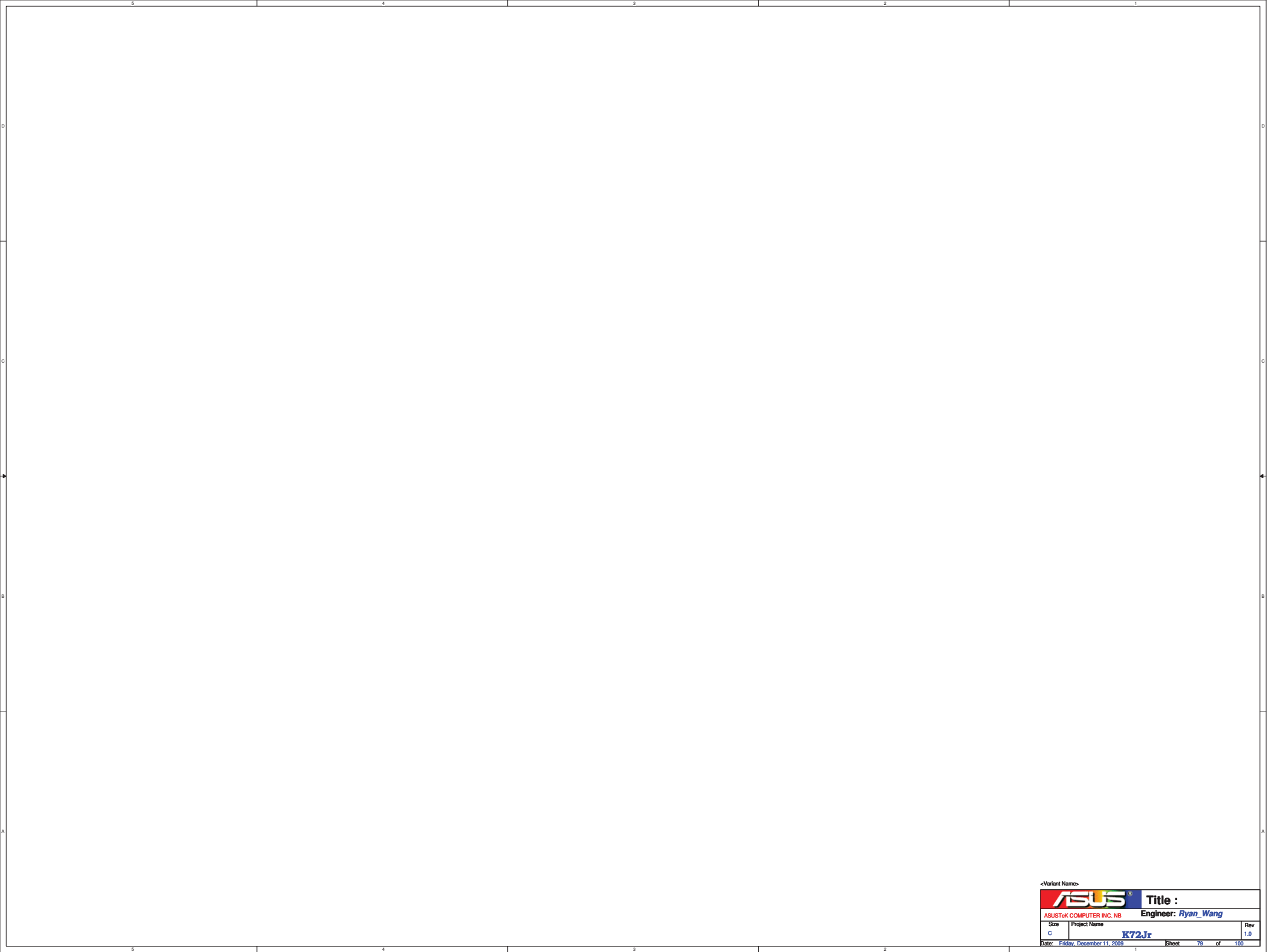
Dual Rank DDR3 1GB need AMD check pull low or high for following DDR3 VRAM
03G151638020 DDR3 64M*16-1.2 FBGA-96 SAMSUNG/K4W1G1646E-HC12
03G151638421 DDR3 64M*16-1.2 FBGA-96 HYNIX/H5TQ1G63BFR-12C

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR3 Memory Type	Channel Size
Samsung	0000	0	64M*16 (512MB) Dual Rank 512*2 = 1G	B channel dual-link
Hynix	0001	1	64M*16 (512MB) Dual Rank 512*2 = 1G	B channel dual-link

+VGA_CORE	RTop	RBot	PWRCNTL_0	PWRCNTL_1
0.9V	8K	40K	Low	Low
1V	8K	40K 60.4K	High	Low
1.1V	8K	40K 30.1K	Low	High
1.2V	8K	40K 60.4K 30.1K	High	High





<Variant Name>

**ASUS**[®]

Title :

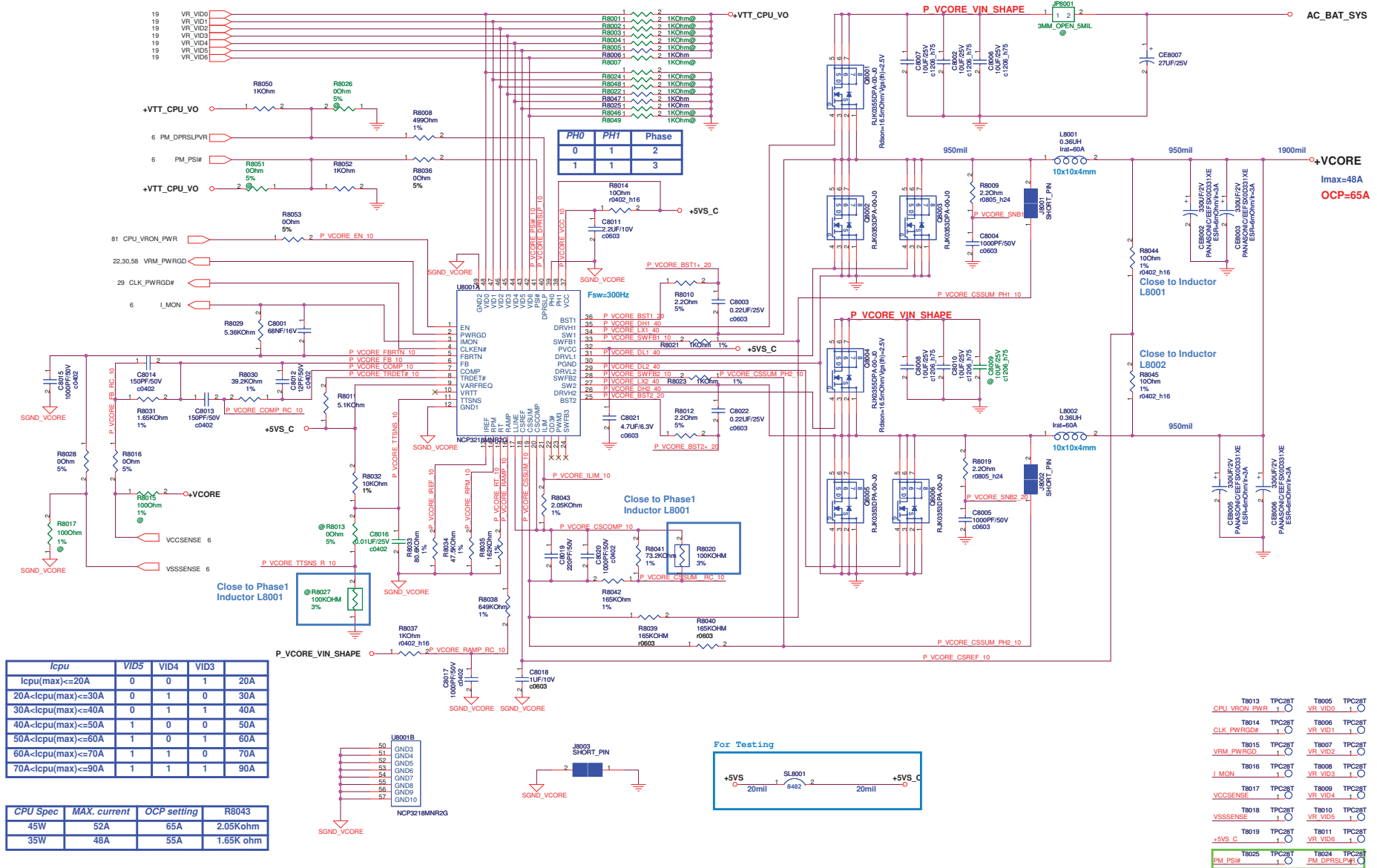
ASUSTeK COMPUTER INC. NB

Engineer: *Ryan_Wang*

Size	Project Name	Rev
C	K72Jr	1.0

Date: Friday, December 11, 2009Sheet 79 of 100

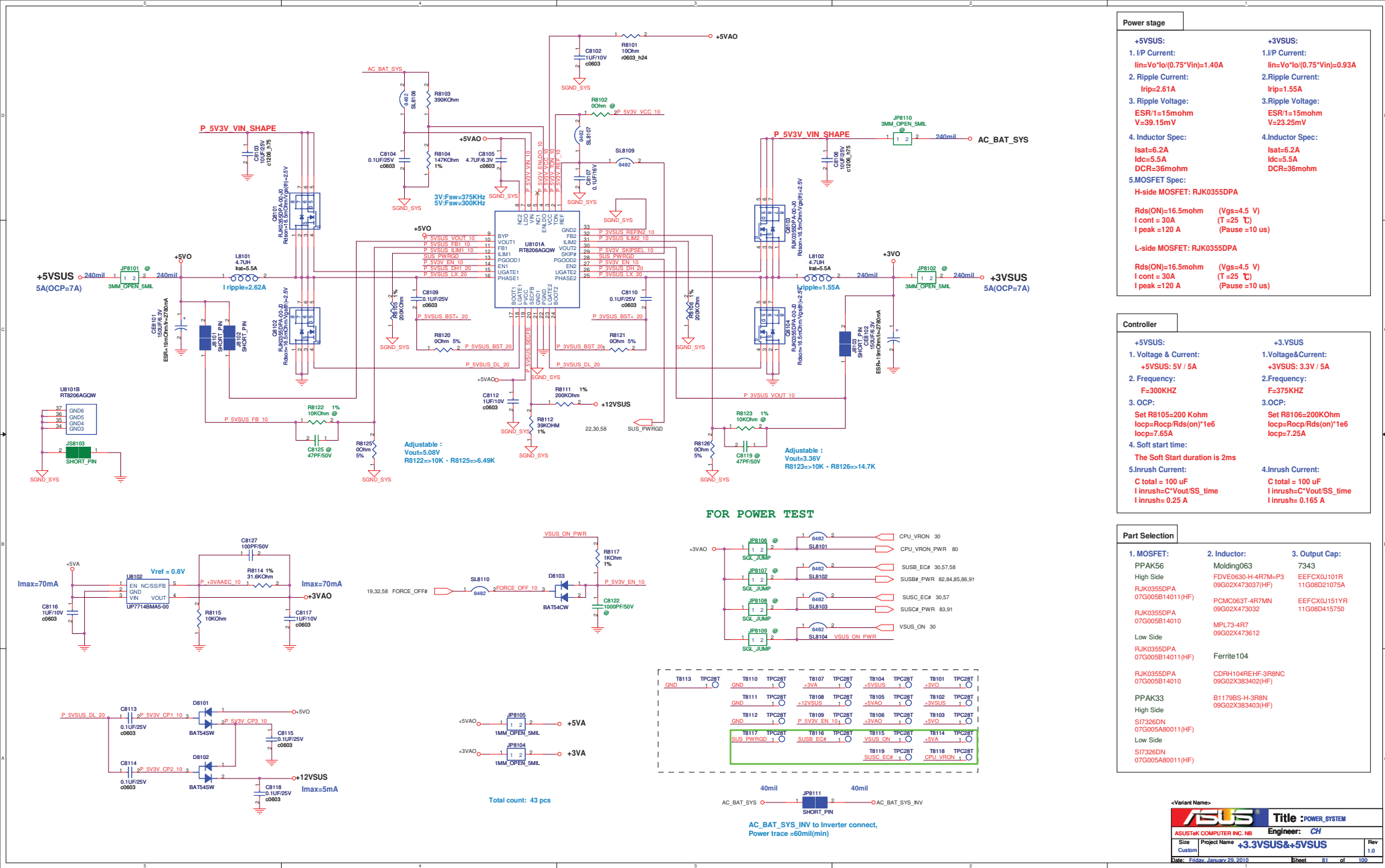
IMVP6.5 CPU VCORE REGULATOR



Total count: 73 pcs

<Variant Name>

ASUS		Title : +VCORE	
ASUSTEK COMPUTER INC. NBI		Engineer: CH	
Size	Project Name		Rev
Custom	K72J		1.0
Date: Friday, January 28, 2010		Sheet	80 of 100

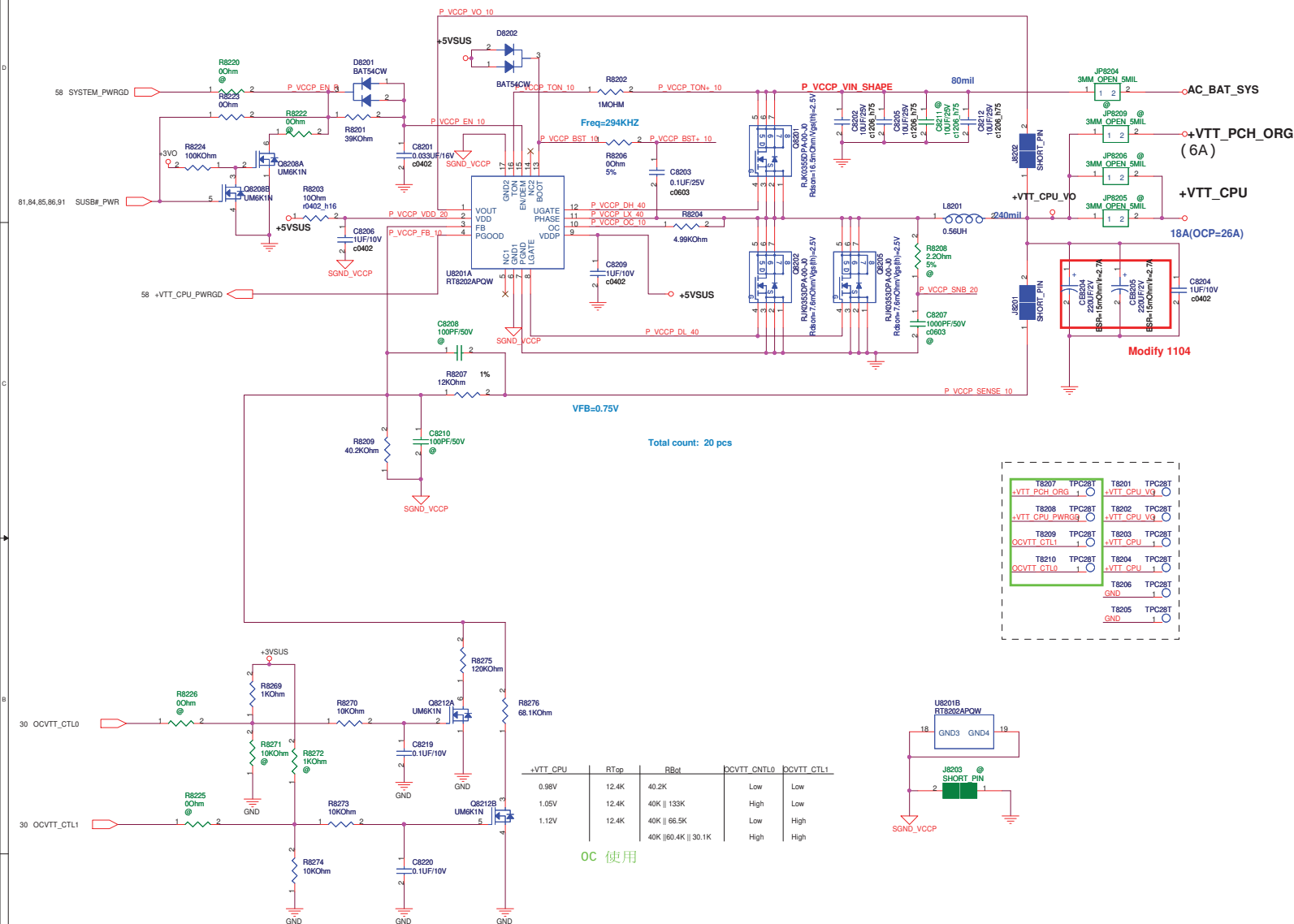


Power stage	
+5VSUS: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.40A$ 2. Ripple Current: $I_{rip} = 2.61A$ 3. Ripple Voltage: $ESR/1 = 15m\Omega$ $V = 23.15mV$ 4. Inductor Spec: $I_{sat} = 6.2A$ $I_{dc} = 5.5A$ $DCR = 36m\Omega$ 5. MOSFET Spec: H-side MOSFET: RJK0355DPA $R_{ds(on)} = 16.5m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause $\geq 10\mu s$) L-side MOSFET: RJK0355DPA $R_{ds(on)} = 16.5m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause $\geq 10\mu s$)	+3VSUS: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 0.93A$ 2. Ripple Current: $I_{rip} = 1.55A$ 3. Ripple Voltage: $ESR/1 = 15m\Omega$ $V = 23.15mV$ 4. Inductor Spec: $I_{sat} = 6.2A$ $I_{dc} = 5.5A$ $DCR = 36m\Omega$

Controller	
+5VSUS: 1. Voltage & Current: +5VSUS: 5V / 5A 2. Frequency: F = 300KHZ 3. OCP: Set R8105 = 200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1e6$ $I_{ocp} = 7.65A$ 4. Soft start time: The Soft Start duration is 2ms 5. Inrush Current: $C_{total} = 100\mu F$ $I_{inrush} = C \cdot V_{out} / SS_time$ $I_{inrush} = 0.25A$	+3VSUS: 1. Voltage & Current: +3VSUS: 3.3V / 5A 2. Frequency: F = 375KHZ 3. OCP: Set R8106 = 200Kohm $I_{ocp} = R_{ocp} / R_{ds(on)} \cdot 1e6$ $I_{ocp} = 7.25A$ 4. Inrush Current: $C_{total} = 100\mu F$ $I_{inrush} = C \cdot V_{out} / SS_time$ $I_{inrush} = 0.165A$

Part Selection		
1. MOSFET: PPAK56 High Side RJK0355DPA 07G005B14011(HF) Low Side RJK0355DPA 07G005B14010(HF) PPAK33 High Side Si7326DN 07G005A80011(HF) Low Side Si7326DN 07G005A80011(HF)	2. Inductor: Molding063 7343 FDVE0530-H-4R7M-P3 09G02X473037(HF) PCMC063T-4R7MN 09G02X473032 MPL73-4R7 09G02X473612 Ferrite104 CDRH104REHF-3R8NC 09G02X383402(HF) B1179BS-H-3R8N 09G02X383403(HF)	3. Output Cap: 7343 EEFCXJ101R 11G08D21075A EEFCXJ151YR 11G08D415750

+VCCP POWER SUPPLY



Power stage

+VTT_CPU:

- 1. I/P Current:**
 $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 1.32A$
- 2. Ripple Current:**
 $I_{rip} = 5.9A$
- 3. Ripple Voltage:**
 $ESR / 1 = 10mohm$
 $V = 59mV$
- 4. Inductor Spec:**
 $I_{sat} = 30.5A$
 $I_{dc} = 22.9A$
 $DCR = 1.4mohm$
- 5. MOSFET Spec:**
H-side MOSFET: RJK0355DPA
- $R_{ds(ON)} = 16.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

L-side MOSFET: RJK0353DPA

Rds(ON)=7.6mohm (Vgs=4.5 V)
I cont = 35A (T=25 °C)
I peak =140 A (Pause =10 us)

Controller

+VTT_CPU

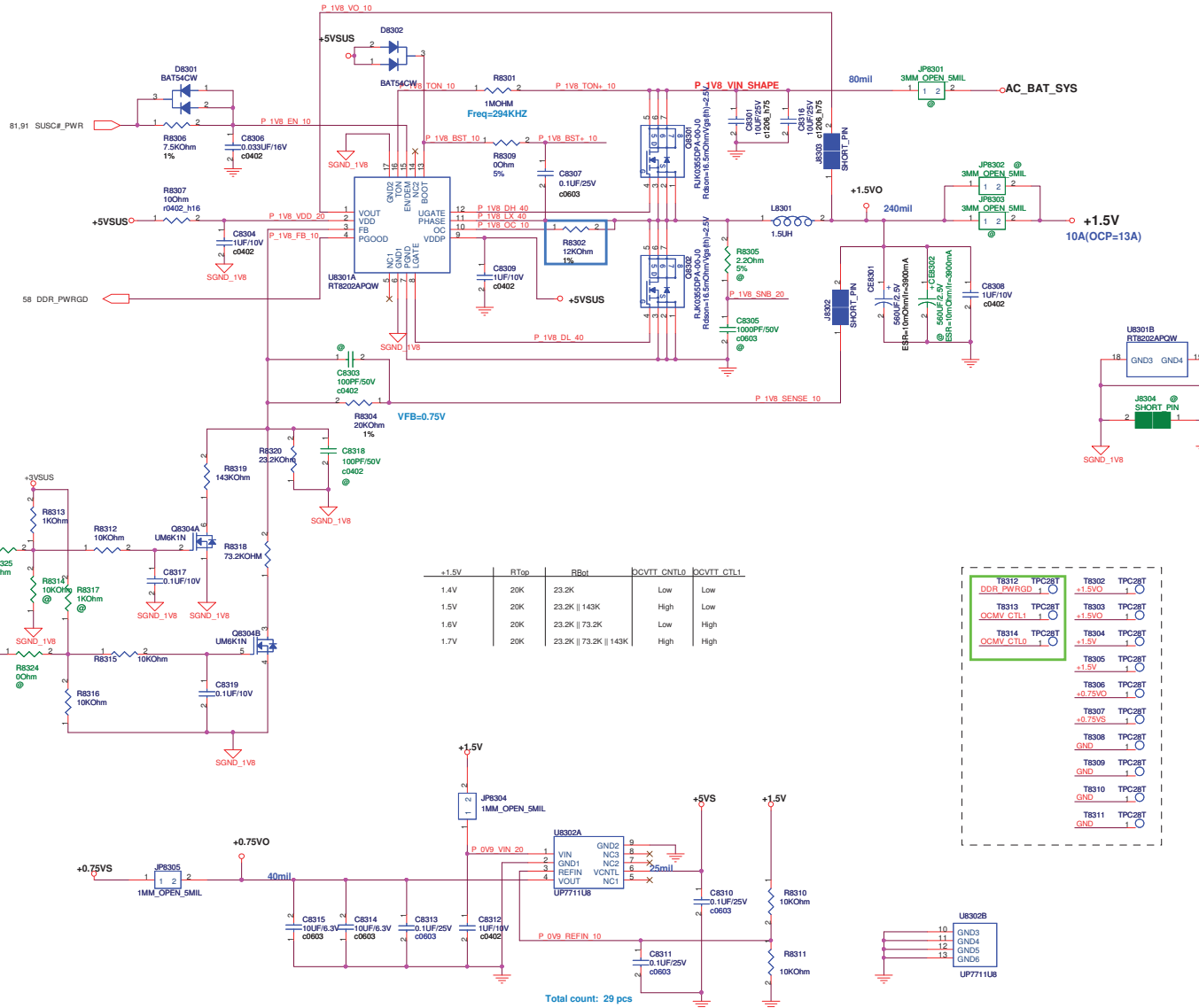
1. Voltage & Current:
+VCCP: 1.05V / 26A
2. Frequency:
F=294KHZ
3. OCP:
Set R8204=4.99 Kohm
Iocp=Rocp*20uA/Rds(on)
Iocp=26.26A
4. Soft start time:
The Soft Start duration is 1.35ms
5. Inrush Current:
C total = 220 uF
I inrush=C*Vout/SS_time
I inrush= 0.17 A

Part Selection

- | 1. MOSFET: | 2. Inductor: | 3. Output Cap: |
|--------------------------------|---|--------------------------------|
| PPAK56 | Molding063 | 7343 |
| High Side | FDVE0630-H-1R0M=P3
09G02X103506(HF) | EEFCX0D221YR
11G08D1227D0 |
| RJK035SDPA
07G005B14011(HF) | PCMC063T-1R0MN
09G02X103022 | EEFCX0D221R
11G08D2227D1 |
| RJK035SDPA
07G005B14010 | MPC7301R0M1
09G02X103H11 | ACAS2R0S221E15
11G09D2227D0 |
| Low Side | | |
| RJK035SDPA
07G005A92010 | Ferrite104 | |
| | FDUE1040D-H-1R0M=P3
09G02X103T25(HF) | |
| PPAK33 | | |
| High Side | PCMC104T-1R0MN
09G02X103J00 | |
| S17356DN
07G005A80011(HF) | MPO104-1R0
09G02X103R01 | |

<Variant Name>

+1.5V & 0.75VS POWER SUPPLY



Power stage

- DDR II:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.052A$
 - Ripple Current:**
 $I_{rip} = 3.07A$
 - Ripple Voltage:**
 $ESR/1 = 10mohm$
 $V = 30.7mV$
 - Inductor Spec:**
 $I_{sat} = 10.9A$
 $I_{dc} = 10A$
 $DCR = 12.1mohm$
 - MOSFET Spec:**
H-side MOSFET: RJK0355DPA
 $R_{ds(ON)} = 16.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

- L-side MOSFET: RJK0355DPA**
 $R_{ds(ON)} = 16.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

Controller

- DDR II:**
- Voltage & Current:**
 $+1.5V: 1.5V / 10A$
 $+0.75V: 0.75V / 1A$
 - Frequency:**
 $F = 294KHZ$
 - OCF:**
Set $R8302 = 12Kohm$
 $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$
 $I_{ocp} = 14A$
 - Soft start time:**
The Soft Start duration is 1.35ms
 - Inrush Current:**
 $C_{total} = 560uF$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.17A$

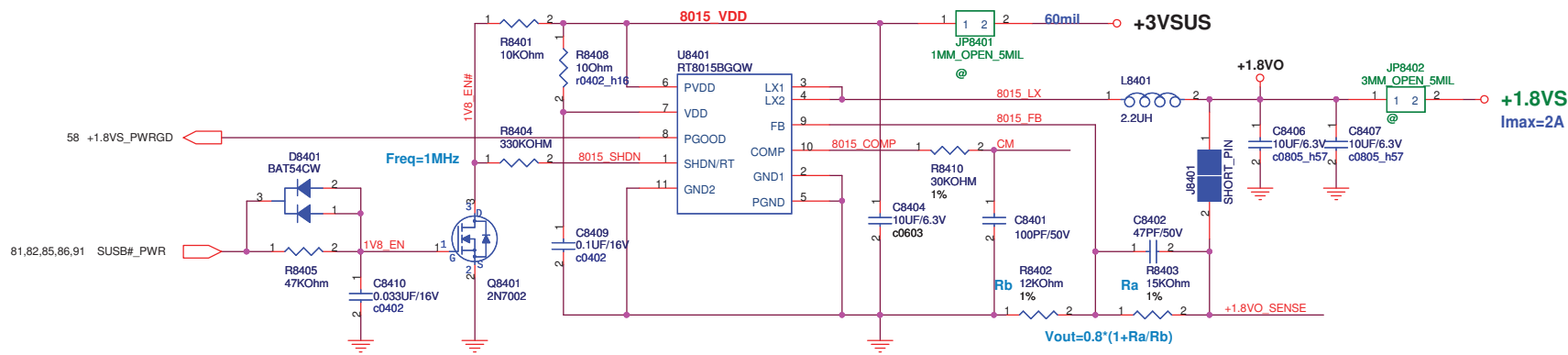
Part Selection

- MOSFET:**
PPAK56
High Side
RJK0355DPA
07G005B14011(HF)
- Inductor:**
Molding063
FDVE0630-H-2R2M-P3
09G02X223809(HF)
- Output Cap:**
7343
EEFCX0D221YR
11G08D1227D0

<Variant Name>

ASUS		Title : POWER_IO_DDR	
ASUSTek COMPUTER INC. NB		Engineer: CH_LU	
Size	Project Name	Rev	
Custom	K72J	1.0	
Date: Friday, January 29, 2010		Sheet	83 of 100

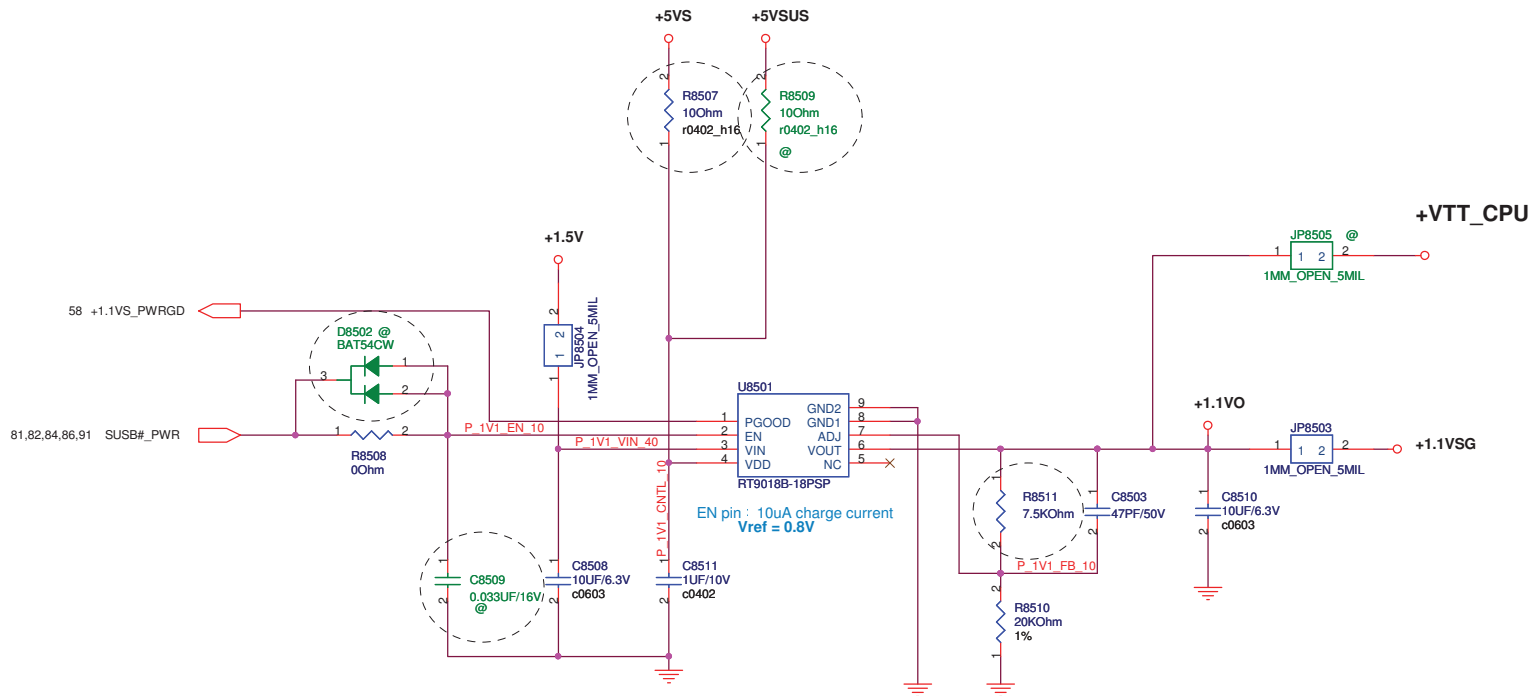
+1.8V POWER SUPPLY



+1.8VS @ 2A

1. Supply Voltage:
 $V_{IN} = 3.3V$ (2.6V ~ 5.5V)
2. Supply Voltage:
 $V_{OUT} = 1.8V / 2A$
3. Current Limit:
 $I_{limit} = 3.2A$
4. Continue Current:
 $I_{cont} = 2A$
5. Feedback Voltage:
 $V_{FB} = 0.8V$
6. Switching Frequency:
 $R_{rt} = 330\text{ Kohm}$
 $F_{sw} = 1\text{ MHz}$

T8403	TPC28T
+1.8VO	1
T8404	TPC28T
+1.8VS	1
T8405	TPC28T
GND	1
T8406	TPC28T
GND	1
T8407	TPC28T
+1.8VS PWRGD	1



Total count: 9 pcs

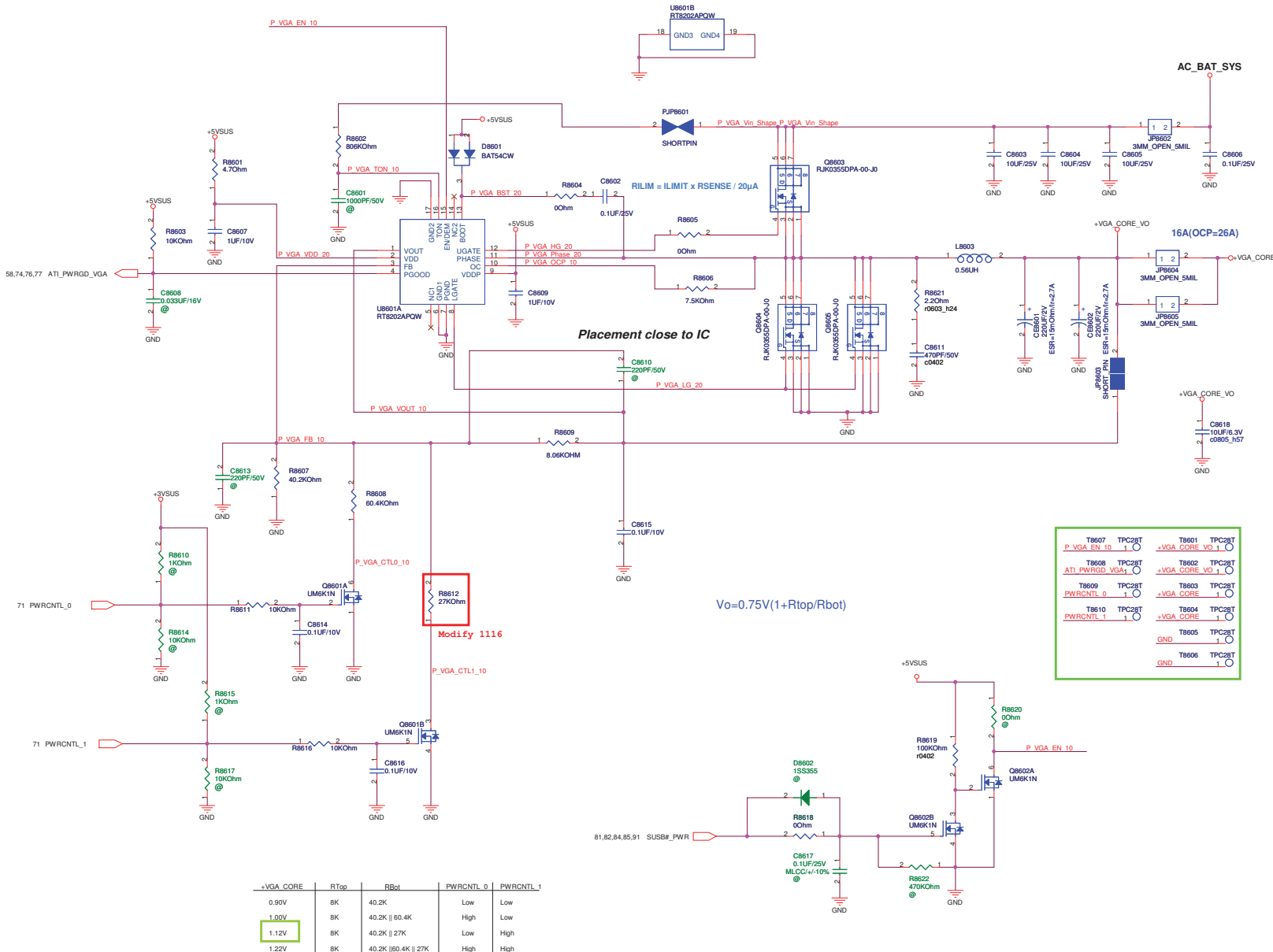
T8511	TPC28T	T8507	TPC28T
+VTT_CPU	1	+1.1VO	1
T8512	TPC28T	T8508	TPC28T
+1.1VS_PWRQ.D	1	+1.1VSG	1
		T8509	TPC28T
		GND	1
		T8510	TPC28T
		GND	1

+1.1VSG @ 2A

- Dropout Voltage:**
 $\Delta V = 0.4V$ ($I_o = 2A$)
- Current Limit:**
 $I_{limit} = 4A$
- Continue Current:**
 $I_{cont} = 2A$
- Power Dissipation:**
 $R_{thjc} = 52^\circ C/W$
 $P_d = 1.9W$
- EN Voltage:**
 $V_{rising} = 1.4V$
 $V_{falling} = 0.8V$
- Supply Voltage:**
 $V_{IN} = 1.5V$
- Inrush current:**
 $T_{ss} = 5ms$
 $C_{total} = 10\mu F$
 $I_{inrush} = 0.003A$

<Variant Name>

ASUS		Title :	
ASUSTeK COMPUTER INC. NB1		Engineer:	
Size B	Project Name		Rev 1.0
Date: Friday, January 29, 2010		Sheet 85 of 100	



Power stage

+VGA_CORE:

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.12A$
2. Ripple Current:
 $I_{rip} = 5.63A$
3. Ripple Voltage:
 $ESR/2 = 7.5m\Omega$
 $V = 42.22mV$
4. Inductor Spec:
 $I_{sat} = 30.5A$
 $I_{dc} = 22.9A$
 $DCR = 1.7m\Omega$
5. MOSFET Spec:
H-side MOSFET: RJK0355DPA
 $R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)
L-side MOSFET: RJK0355DPA
 $R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause = 10 us)

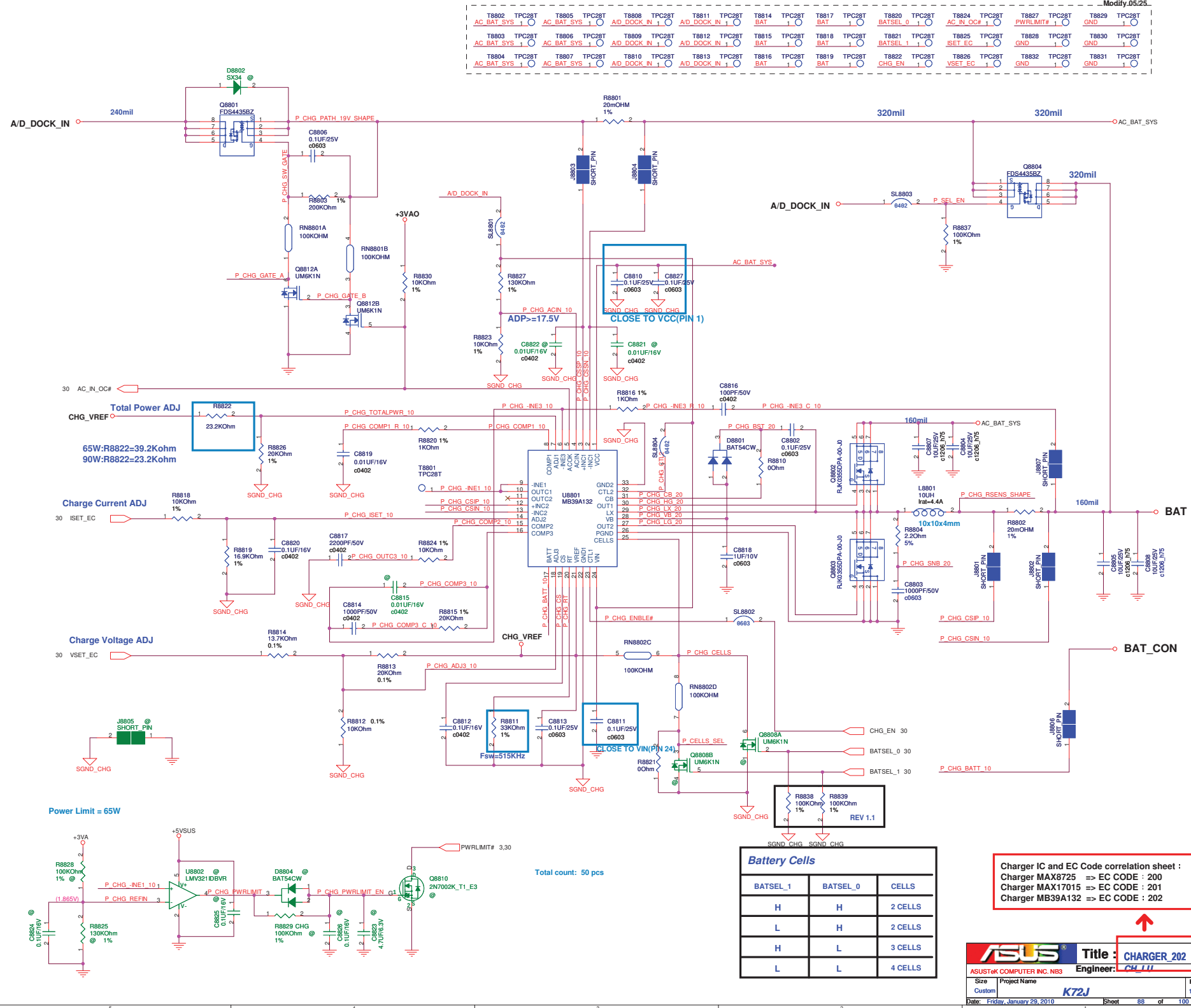
Controller

+VGA_CORE:

1. Voltage & Current:
+VGA_CORE: 1.1V / 16A
2. Frequency:
 $F = 253KHz$
3. OCP:
Set $R8606 = 7.5K\Omega$
 $I_{ocp} = R_{ocp} \cdot 20\mu A / R_{ds(on)}$
 $I_{ocp} = 26A$
4. Soft start time:
The Soft Start duration is 1.35ms
5. Inrush Current:
 $C_{total} = 440\mu F$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.296A$

T8607	TPC28T	T8601	TPC28T
P_VGA_EN_10	1	+VGA_CORE_VO_1	1
T8608	TPC28T	T8602	TPC28T
ATI_PWRGD_VGA_1	1	+VGA_CORE_VO_1	1
T8609	TPC28T	T8603	TPC28T
PWRCNTL_0	1	+VGA_CORE_1	1
T8610	TPC28T	T8604	TPC28T
PWRCNTL_1	1	+VGA_CORE_1	1
		T8605	TPC28T
		T8606	TPC28T
			1

+VGA_CORE	RTop	RBot	PWRCNTL_0	PWRCNTL_1
0.90V	8K	40.2K	Low	Low
1.00V	8K	40.2K 60.4K	High	Low
1.12V	8K	40.2K 27K	Low	High
1.22V	8K	40.2K 60.4K 27K	High	High



Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

BATTERY IN DETECT

<Variant Name>



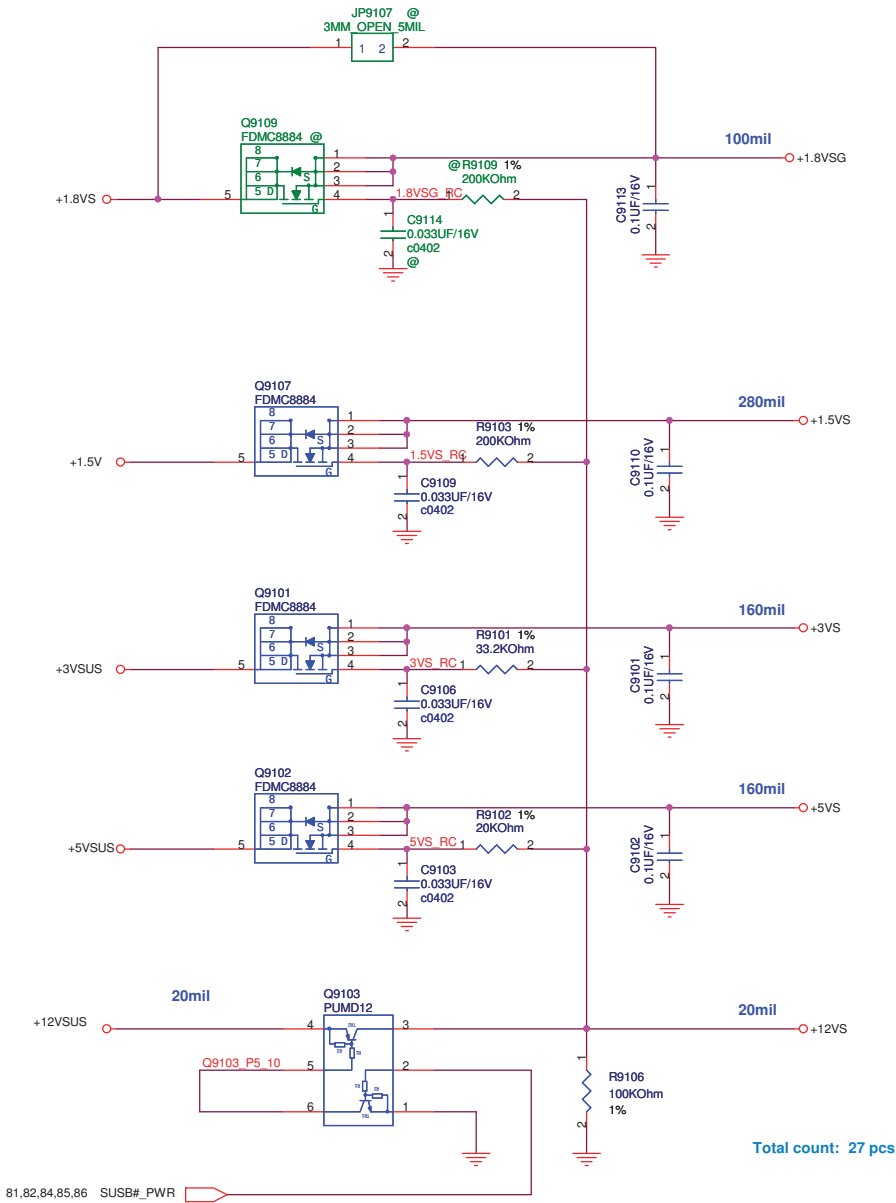
Title :POWER_DETECT

ASUSTeK COMPUTER INC. NBEngineer: Morris

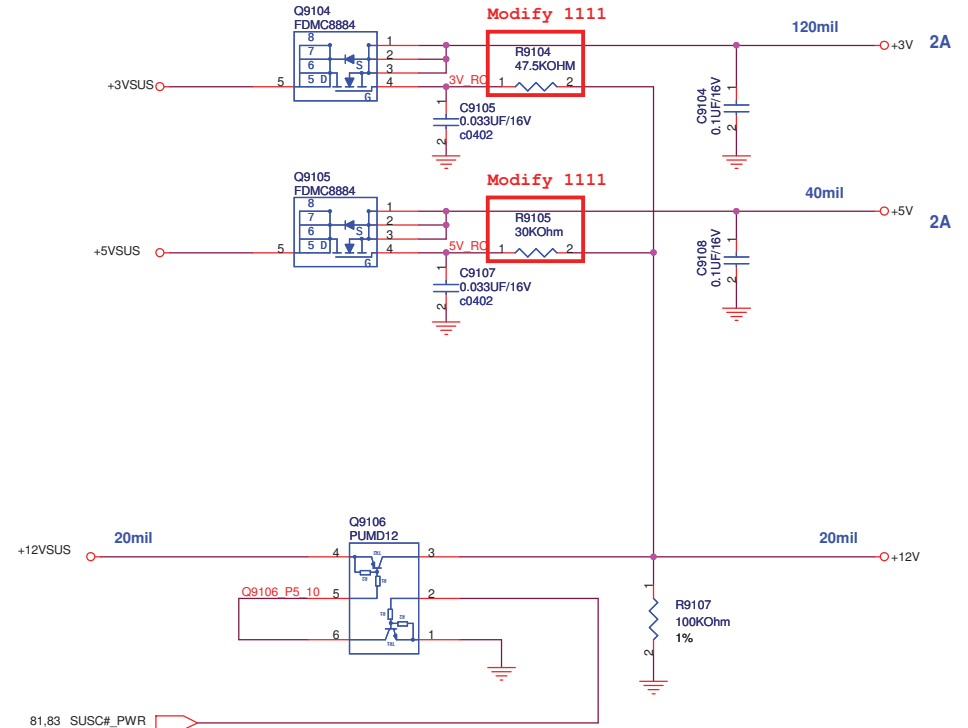
Size	Project Name	Rev
Custom	Design IP	1.0

Date: Friday, January 29, 2010Sheet 90 of 100

SUSB#_PWR POWER



SUSC#_PWR POWER



+12VS	T9107	TPC28T	1	+1.8VSG	T9101	TPC28T	1
+3V	T9108	TPC28T	1	+1.5VS	T9102	TPC28T	1
+5V	T9109	TPC28T	1	+3VS	T9103	TPC28T	1
+12V	T9110	TPC28T	1	+5VS	T9104	TPC28T	1
GND	T9111	TPC28T	1	GND	T9105	TPC28T	1
GND	T9112	TPC28T	1	GND	T9106	TPC28T	1

<Variant Name>

ASUS Title : POWER_LOAD SWITCH

ASUSTek COMPUTER INC. NB Engineer: CH_LU

Size	Project Name	Rev
B	K72J	1.0

Date: Friday, January 29, 2010 Sheet 91 of 100

History

R1.0 to R1.1 :

Page 3 : Change R0363,R0364 to RN0302.
Remove SL0311,SL0312.
Change R0366,R0367 to SL0319,SL0320.
Change R0351 to SL0321.

Page 5 : DNI R0501,R0502,R0505,R0506.

Page 6 : Remove R0616,R0601.
Change R0607 to SL0601.
Change R0605,R0606 to RN0601.

Page 14 : Change CE1407 from 220uF to 100uF for cost down.
Change CE1401~CE1403,CE1406 from POSCAP to TAN for cost down.
Change JP1402 to R1414,R1415 for EMI request.
Correct CE1404 part reference to C1450.

Page 16 : Change R1605,R1606 to SL1601,SL1602.

Page 17 : Change R1705,R1706 to SL1701,SL1702.

Page 18 : Change C1811,C1802 from 0.1uF/10V to 0.1uF/16V.
Remove R1809,R1810.
Change R1801,R1802,R1803,R1804 to RN1802.

Page 19 : Add OC/UC circuit (IT8268).

Page 21 : Remove RX2105,RX2106,RX2107,RX2108,RX2140,RX2141.
Change R2136,R2137 to RN2101.

Page 22 : Chaneg R2257 to SL2201.
Remove R2245.
Change R2246 to SL2202.
Change R2239,R2240 to SL2203,SL2204.

Page 23 : Change R2322,R2323 to RN2301.

Page 24 : Change RX2401,RX2404,RX2406 from 22ohm to 47ohm.
Remove T2413.
Change RP2401~RP2403 to RN2401~RN2405.
Change Card Reader to USB port 11.

Page 25 : Remove R2504,R2523.

Page 26 : Remove JP2601.
Add D2605,R2623,Q2621,R2637,C2617 for ITE8541.

Page 27 : Change +VTT_PCH to +VTT_PCH_ORG.

Page 28 : Change SPI ROM circuit for ITE8541.

Page 29 : Add R2922 for CLK_PWRGD# (open drain).
Add +VDD_1.05 for ICS9LVS3162.

Page 30 : Add U3004 co-lay with U3003.
Add R3010 for X'tal free option.
Add R3008,R3006 for ITE8541 VSUS_ON.
Add OCVTT_CTL0/1,OCMV_CTL0/1 for OC/UC option.

Page 31 : Change C3105 from 0.1uF/10V to 0.1uF/16V.

Page 33 : Remove R3314.
Remove AR8121 option circuit.

Page 34 : Change Transformer to 09G051059023 / 09G051059055.
Change +AVDD_CEN_LAN to +AVDD_1.7_LAN.

Page 37 : Change Jack Ground from GND_AUDIO to GND_JACK.
Add SL3740 for HP1_JD , SL3741 for EXT_MIC_JD.

Page 45 : Change R4501 from 330ohm to 150ohm.
C4507 from 1uF/10V to 1uF/6.3V.
Change C4511(0.1uF/10V) to C4513(0.1uF/16V).
Change RNX4501,LX4501 to SL4501.
Change C4514 connect to R4529 pin1.
Change L4503,C4509,C4512 connection.

Page 48 : Change VGND to GND.
Change F4801 from 0.2A/30V to 1.5A/6V.
Add D4803.

Page 53 : Remove RX5305,RX5306.

Page 56 : Change C5605 from 0.1uF/10V to 0.1uF/16V.
Change LED5601~LED5603 from BLUE to GREEN.
Change LED voltage from +5VS/+5VA to +3VS/+3VSUS.
Add CAP_LED#,NUM_LED# pull-up for open drain signal.

Page 57 : Change Q5703B to NC , R5708 pin1 to +VTT_CPU_VO.

Page 58 : Add R5836 (DNI).

Page 60 : Remove L6001,L6002.

Page 65 : Add H6502 for LVDS cable.

Page 68 : Add caps for EMI request.

Page 70 : Change VGND to GND.

Page 71 : Remove R7124.

Page 73 : Change VGND to GND.

Page 74 : Change CE7401 from 3528 to 7343 type.
Change all +VGA_CORE 0.01uF to 1uF for PARK.

Page 75 : Add RN7501~RN7507 for dual rank memory.

Page 76 : Change VGND to GND.

Page 80 : Mount R8050,R8052.
Change R8050,R8051,VID pull-up to +VTT_CPU_VO.

Page 82 : Change +VTT_PCH to +VTT_PCH_ORG.
Add OV/UV circuit , remove 1.1V support.

Page 83 : Add OV/UV circuit.

Page 84 : Change R8405 from 330K to 200K ohm for +1.8VS timing.

Page 86 : Change 5V_RUN to +5VSUS , VGND to GND.

Page 91 : Change JP8207 to JP9107.

*** Change all M92 parts to PARK parts ***

		Title : HISTORY	
<OrgName>		Engineer: Jerry Mou	
Size Custom	Project Name K72Jr		Rev 2.0
Date: Friday, December 11, 2009		Sheet	96 of 98

R1.1 to R1.2 :

Page 20 : Change C2001,C2002 from 18pF to 15pF.

Page 24 : DNI U2401 , mount R2413.

Page 26 : DNI D2605 , mount R2623 for ITE8541.

Page 28 : DNI R2848 , mount R2857 for ITE8541.
Mount R2866~R2869 for ITE8541.

Page 29 : DNI L2904 & R2921 , mount L2903 for ICS9LVS3162.

Page 30 : DNI R3008 , mount R3006 for ITE8541.
Change C3016,C3017 from 15pF to 10pF.
DNI U3003,R3014 , mount R3002~R3005 for ITE8541.

Page 33 : Add R3321 for signal integrity.

Page 36 : Add D3601 for pop noise.

Page 37 : Change D3709 from RB717F to BAT54AW.
Change C3701 to X7R.

Page 45 : Change C4504 from 1uF/10V to 1uF/6.3V.

Page 47 : Change C4804~C4811 to X5R type.
Change R4801,R4802 to RN4801.

Page 57 : DNI R5705,R5706,Q5703,R5708,R5714,R5715,Q5707,R5712.

Page 58 : Change D5801 from BAT54CW to BAT54C.

Page 65 : Remove H6521,H6522,H6506,H6507,H6523,H6524.

Page 74 : Change L7405 to 09G013120400.
DNI Q7401,L7407 , mount R7402.
Change R7402 to 0805 type.

Page 75 : DNI R7501 for PARK.
Change pin AL21 to test point.

Page 82 : DNI R8220 & R8222 , mount R8223.
Add R8225 & R8226.
DNI R8271 & R8272.

Page 83 : Add R8324 & R8325.
DNI R8314 & R8317.

Page 84 : Change R8405 from 200K to 47K ohm for +1.8VS timing.

Page 85 : Add JP8505 , R8509.
Change R8511 from 7.5K to 5.1K ohm.
DNI U8501 related circuit for cost down.

R1.2 to R1.3 :

Page 21 : Change R2157 from 39 ohm to 15 ohm for single load.

Page 25 : Change PCB ID resistors.

Page 30 : Change R3021,R3023 from 47K ohm to 100K ohm for battery team request.
Add R3030 for VSUS_ON connection.
Delete J3001 & U3004 from schematic.
Add R3011 & Q3002 for ITE8570 X'tal free option.

Page 38 : Change R3852 to 0 ohm , C3801 to DNI.

Page 40 : Change SL4501 to L4502 for EMI request.

Page 52 : Change SL5201,SL5202 to L5201,L5202 for EMI request.

Page 65 : Modify H6518 shape for ME request.

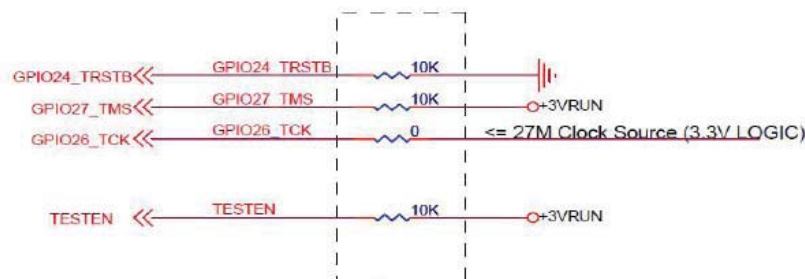
Page 71 : Change R7128 to 0402 type.

Page 77 : Change R7714 to /HYNIX , R7718 to /SAMSUNG.

Page 80 : Change 8029 to 5.36K , C8001 to 68nF , R8032 to 10K , C8019 to 220pF.
Change R8039,R8040 to 165K ohm.

Page 82 : Change CE8202 to C8221 & C8222 (DNI).

Page 70~77 : Add PARK errarta items as below.



In current reference design, TESTEN is pulled down through a resistor and GPIO24_TRSTB may be pulled-high or floating. To implement option 2, both of these resistors should be depopulated (keep the resistor pad for debugging purposes).

Option 2 requires that:

- 1) TESTEN and GPIO27_TMS be pulled high (3.3V)
- 2) GPIO24_TRSTB be pulled to ground (0V), and
- 3) A clock source (1KHz ~27MHz, 3.3V level) be provided on GPIO26_TCK (through a 0 Ohm resistor). The 27MHz oscillator output can be used (if present).

R1.3 to R2.0 :

Page 19 : Add R1903.

Page 20 : DNI R2034~R2039 for Production PCH.

Page 21 : Change R2157 from 15 ohm to 24.9 ohm.

Page 32 : Mount R3207 for G709.

Page 36 : Change INT_MIC to Codec Port A for feedback issue.

Page 37 : Change Phone Jack P/N from 12G14030106L to 12G14000106M.

Page 38 : Change Internal Mic reference voltage to codec output.

Page 46 : DNI Q4601 , mount U4601 , change SL4601 & SL4602 to 33 ohm for HDMI audio disappear issue.

Page 48 : DNI D4803 for cost down.

Page 50 : Add G709 circuit , DNI G781 circuit.

Page 51 : Change R5101~R5103 to short land.

Page 56 : Change LED5601 from Green to White , R5604 pin1 from +3VSUS to +5VSUS.

Page 57 : Delete Q5702 & Q5703 & Q5707 discharge circuit , change Q5704 to 2N7002.

Page 60 : Delete JP6003 & JP6004.

Page 65 : Delete H6527.

Page 66 : Change C6607 from 0.1uF/16V to 0.1uF/25V.

Page 71 : Add U7101 & R7131 for PARK errata E2 , DNI R7121 & R7124 for production PARK.

Page 73 : DNI R7335 , mount R7305 for production PARK.

Page 76 : DNI R7605 for production PARK.

Page 82 : Modify CE8204 & CE8205 package.

Page 91 : Change R9104 to 47.5K , R9105 to 30K for power on fail issue.