



Part Number = DAZ0J200100

Compal Confidential

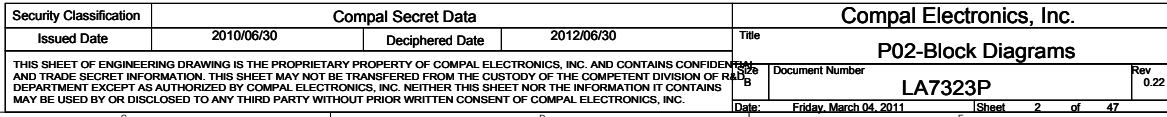
K73 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

2010-02-22

REV: 0.22

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	PCH	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	PCH	X	X	V	X	X	X

BOM Structure

15@ : E240 1.5GHz
16@ :E350 1.6GHz
X76@ : VRAM second source
LS@ : Level Shift
NLS@ :non Level Shift
USB30@ :USB3.0

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI (WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

Symbol Note :



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Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

VDDR3(3.3VSG)

PCIE_VDDC(1.0V)

VDDR1(1.5VSG)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

Note: Do not drive any IOs before VDDR3 is ramped up.

T4+16clock

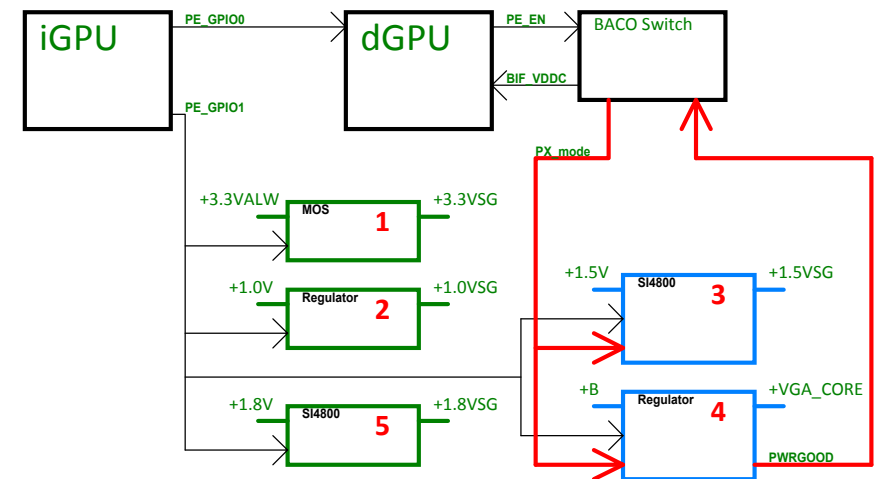
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

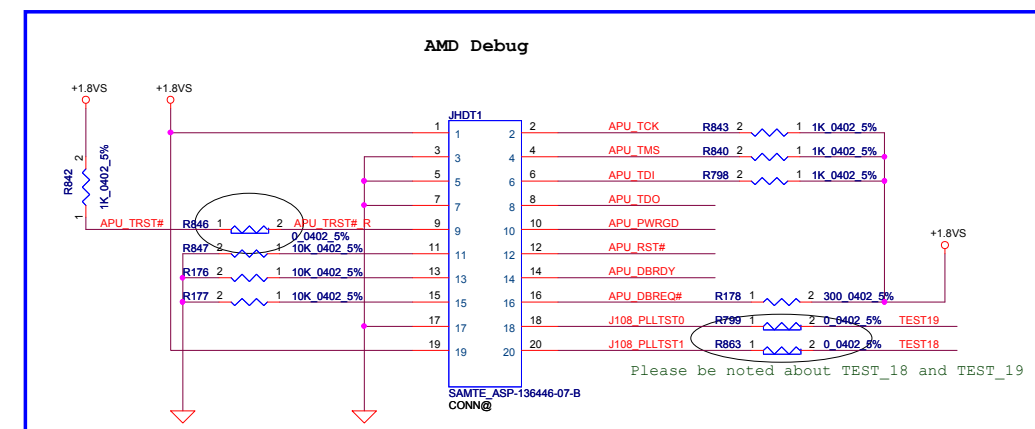
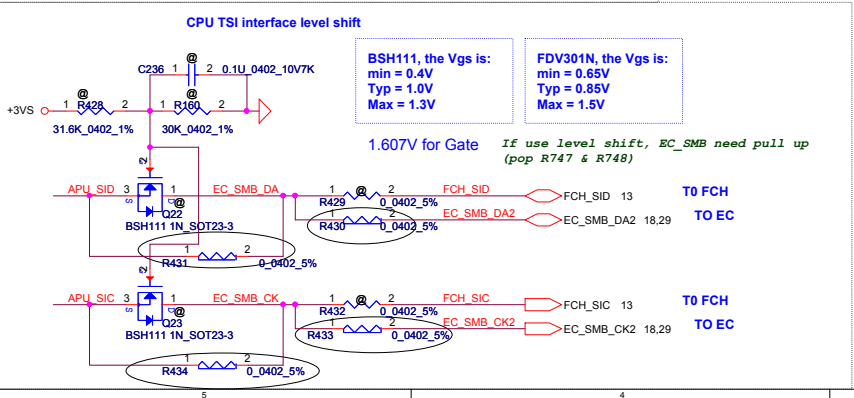
BACO option :

PE_GPIO0 : High -> Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



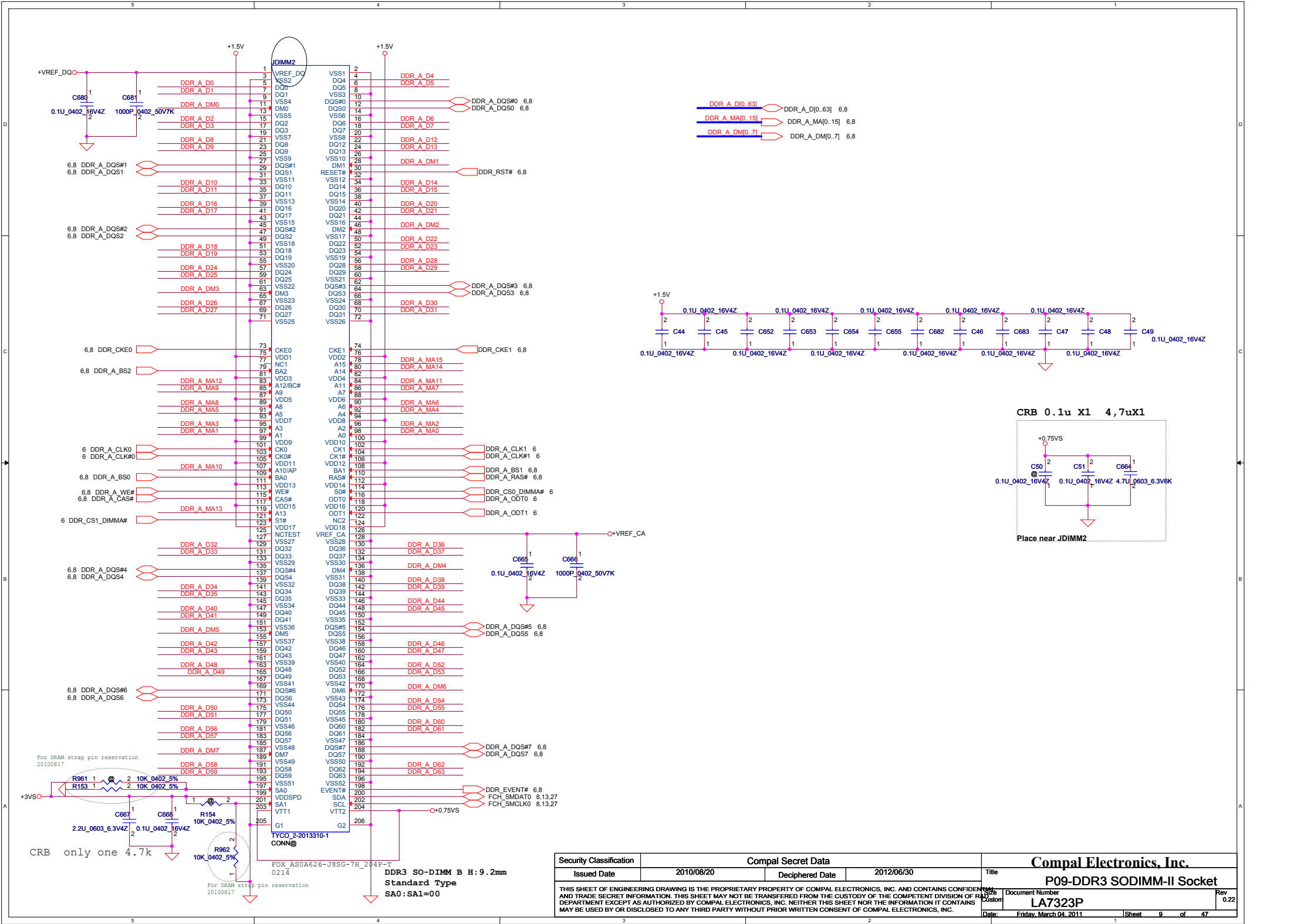
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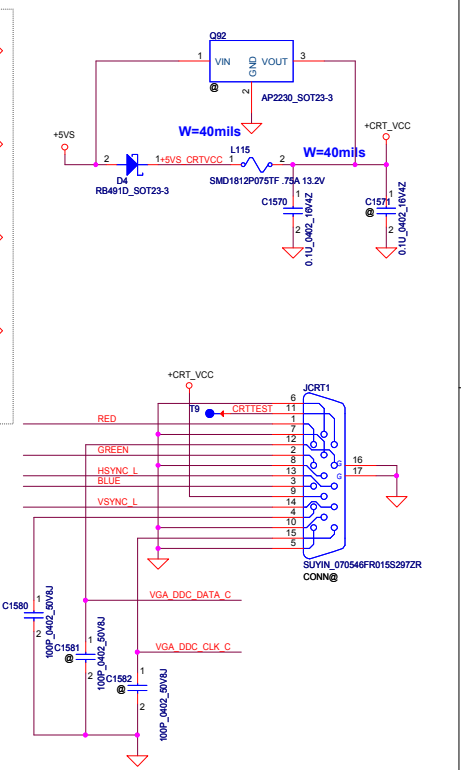
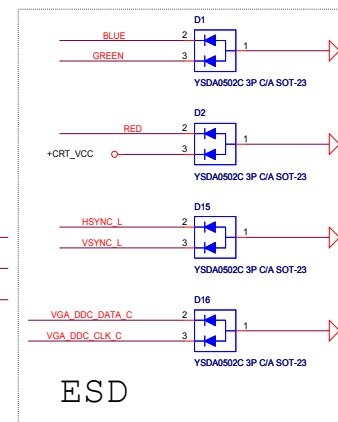
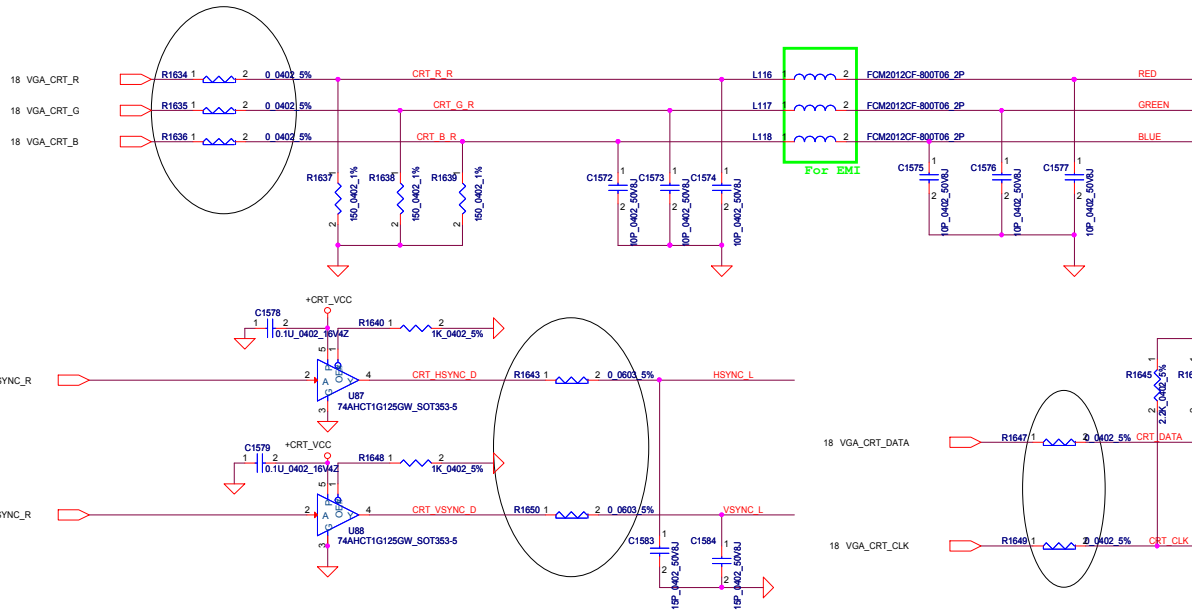
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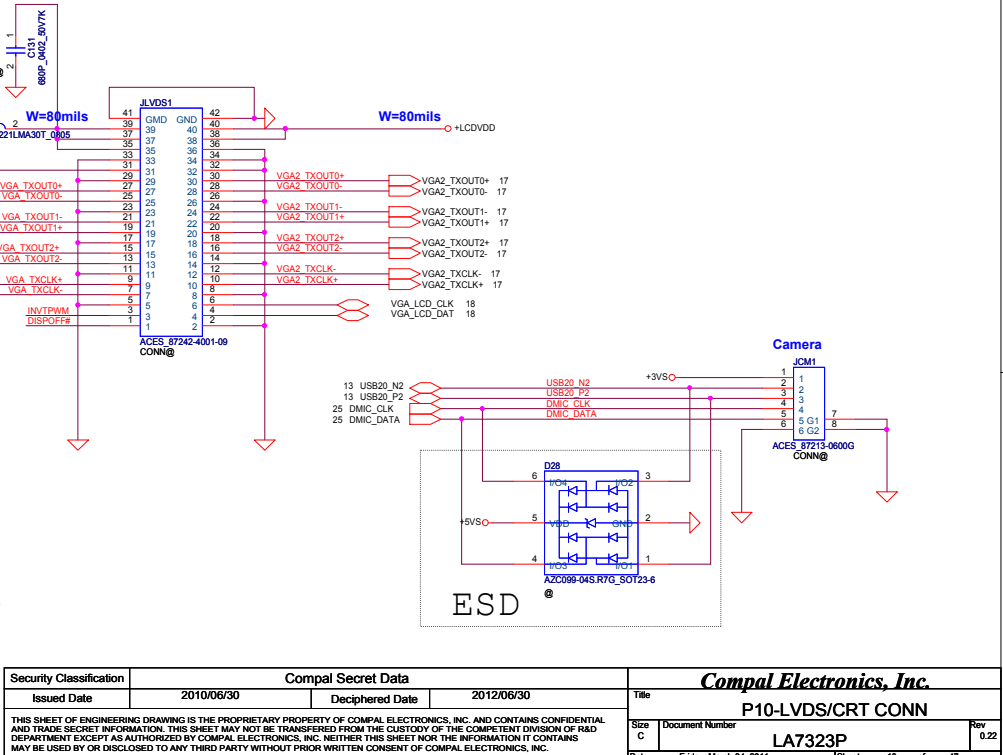
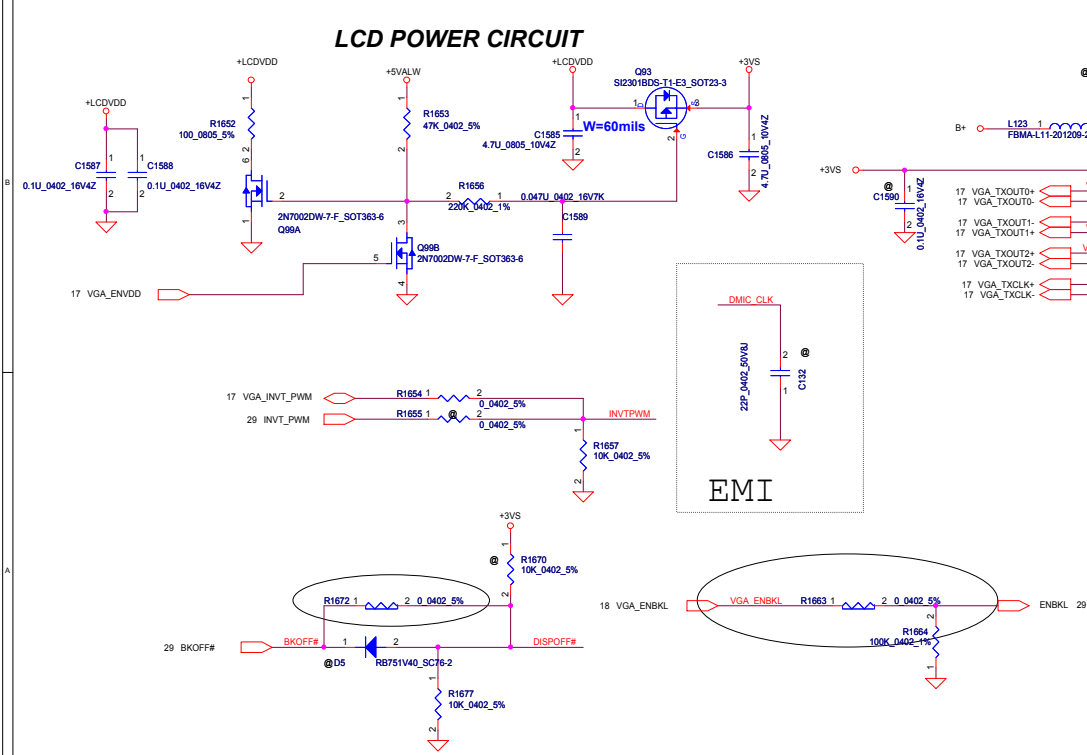
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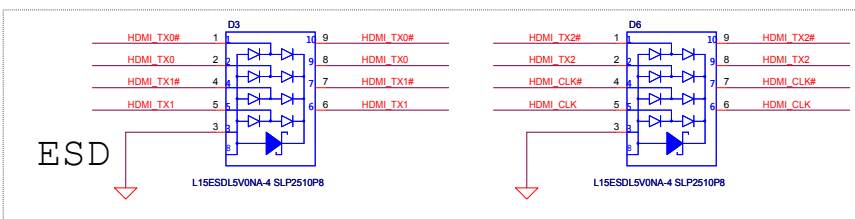
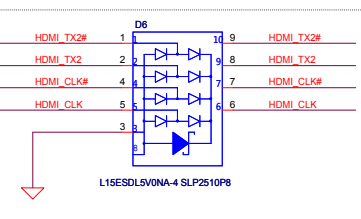
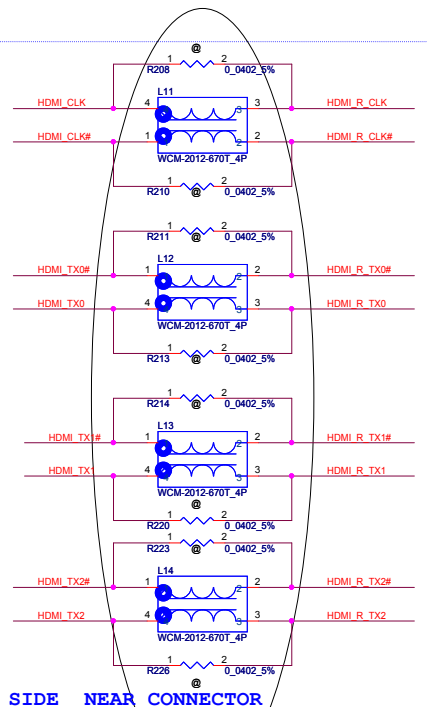
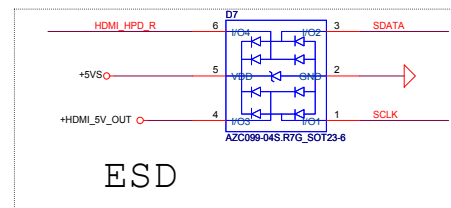
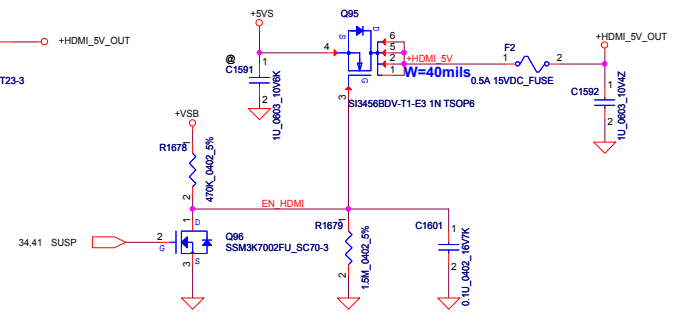
CRT



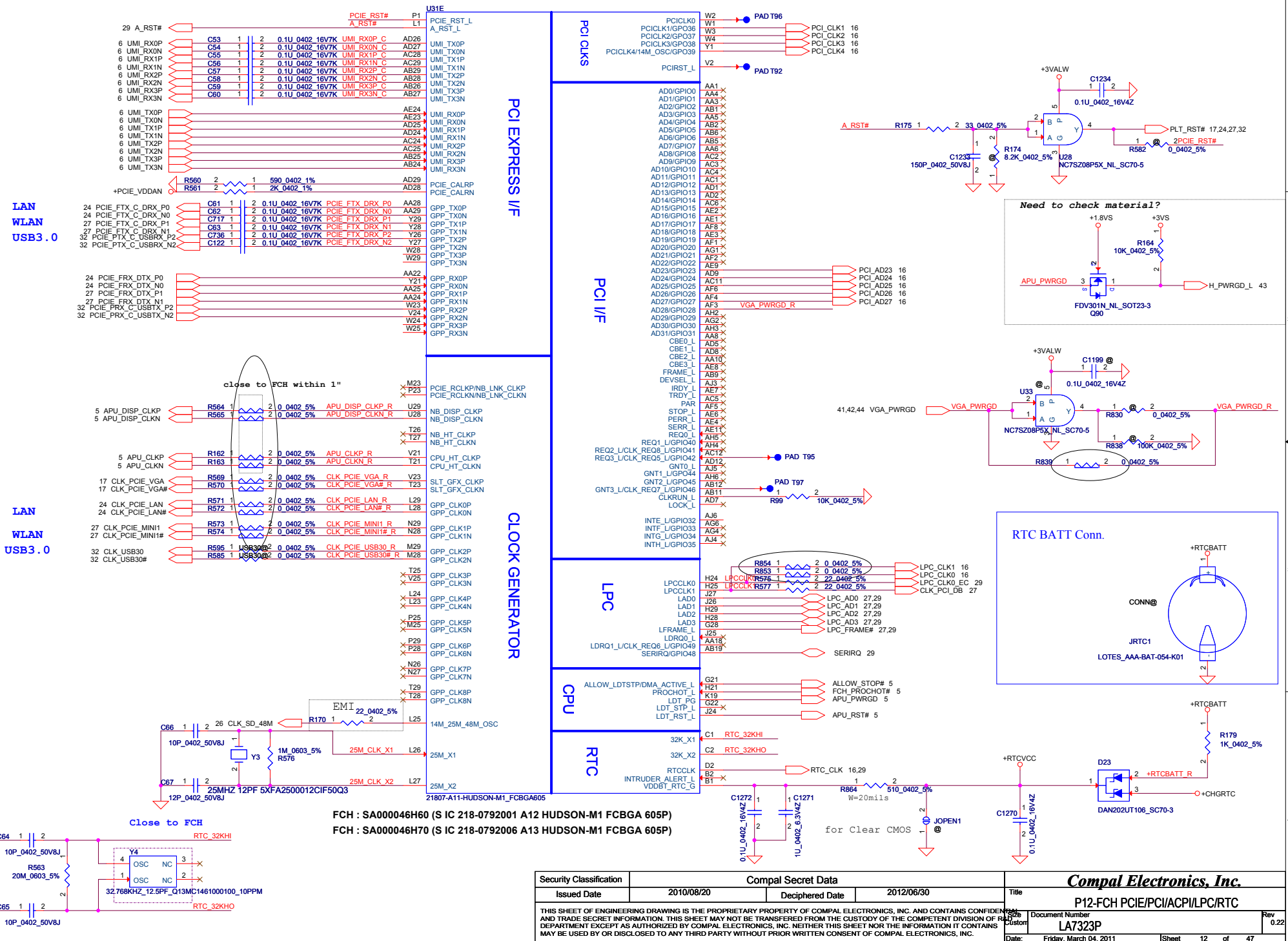
LCD POWER CIRCUIT

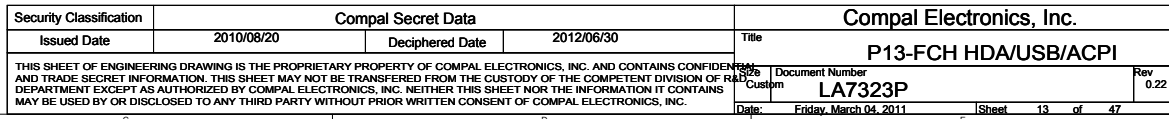


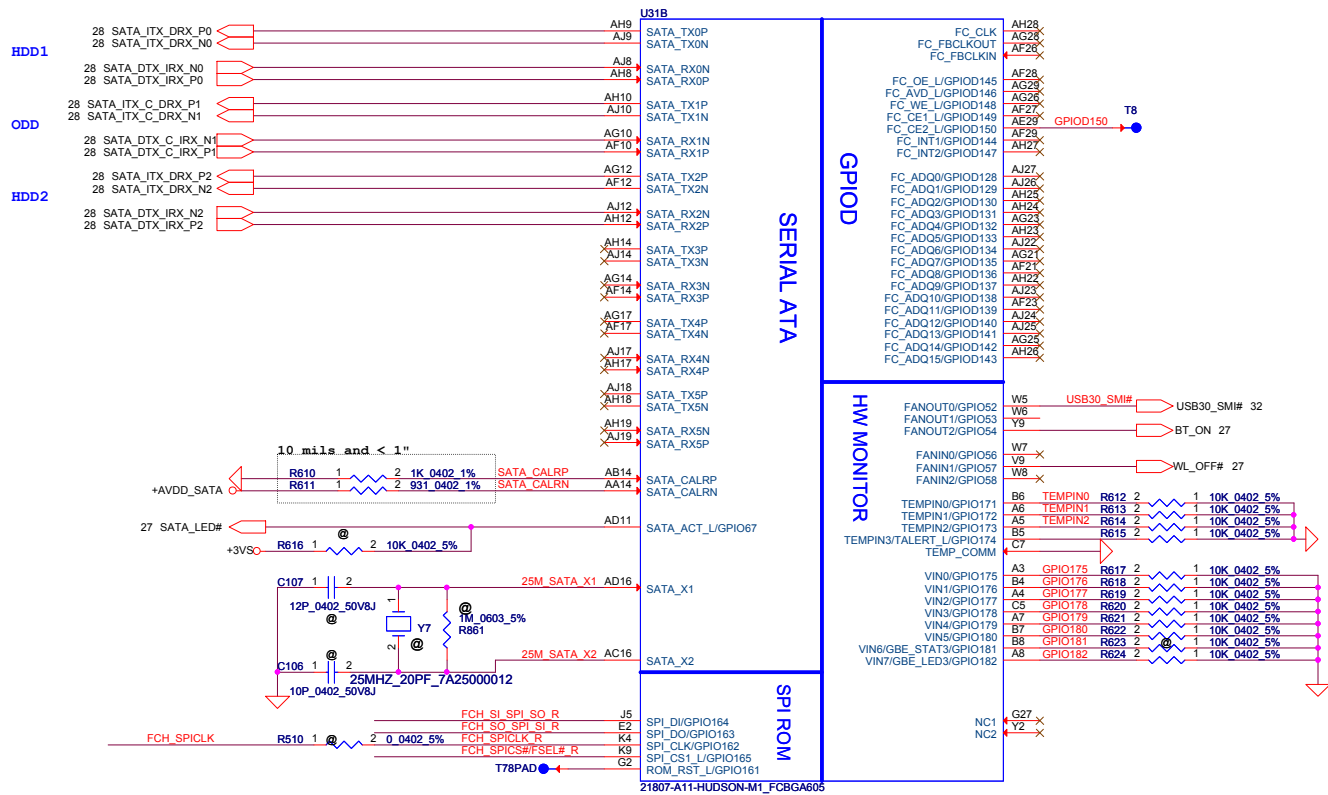
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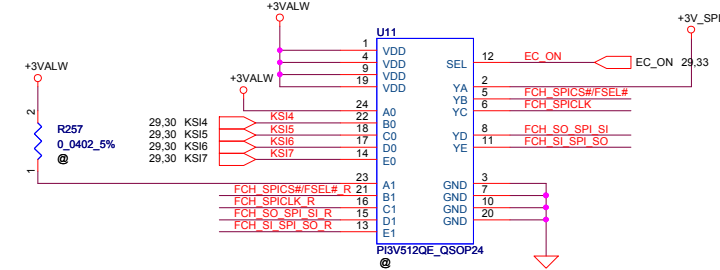
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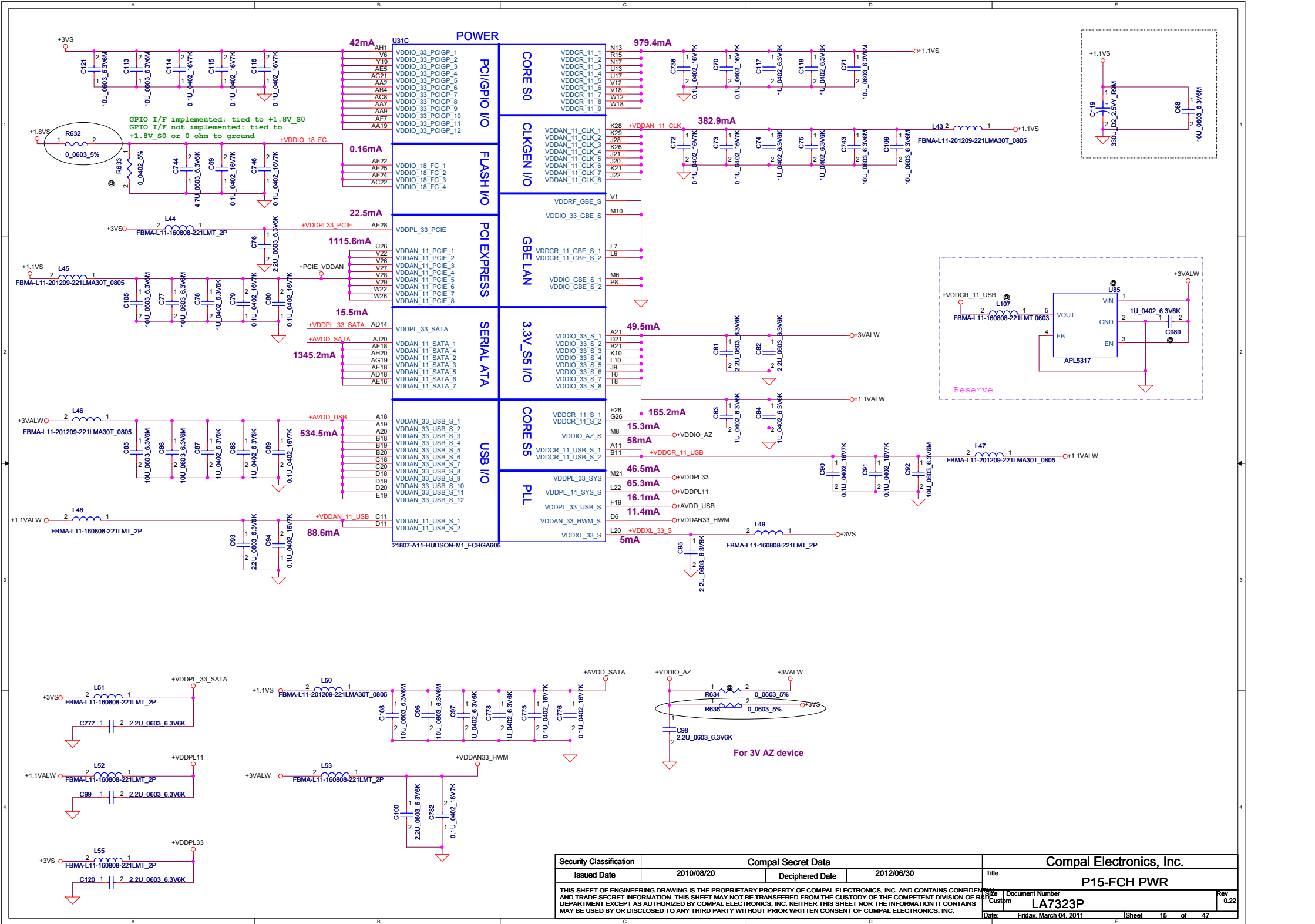


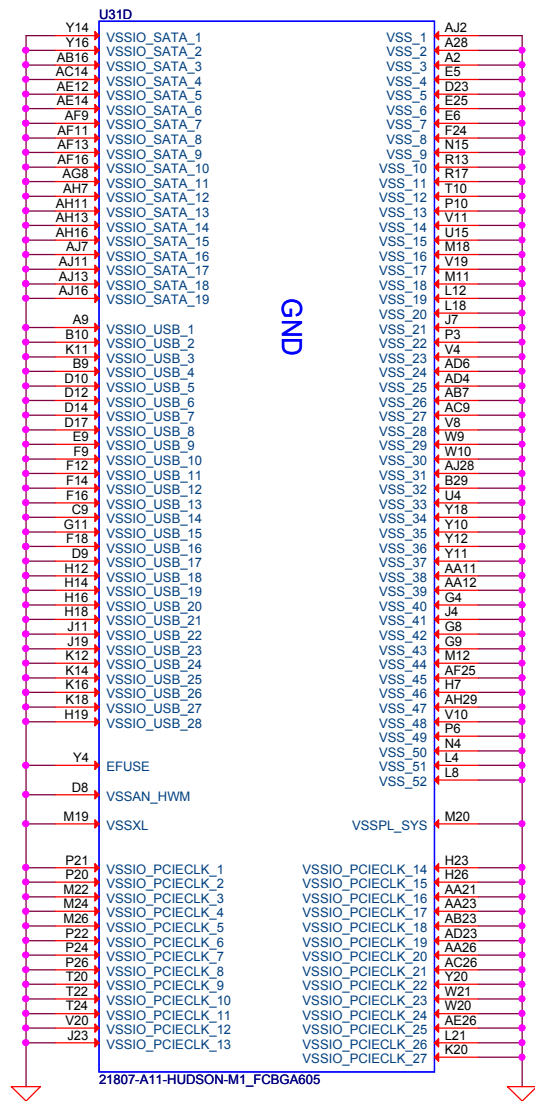


VIN6/GBE_STAT3/GPIO181
Enable integrated pull-down/up and leave unconnected



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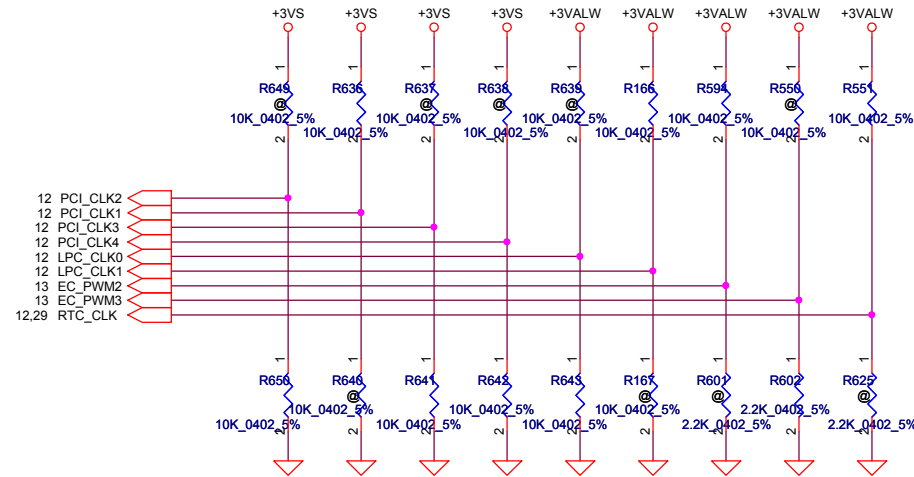




REQUIRED STRAPS

Check Internal PU/PD

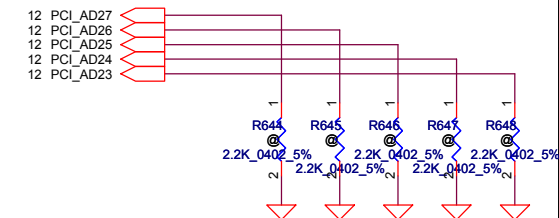
	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2	EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L) *	
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)	



DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved



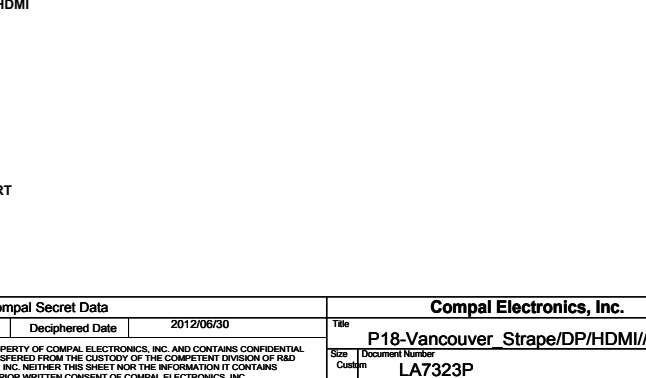
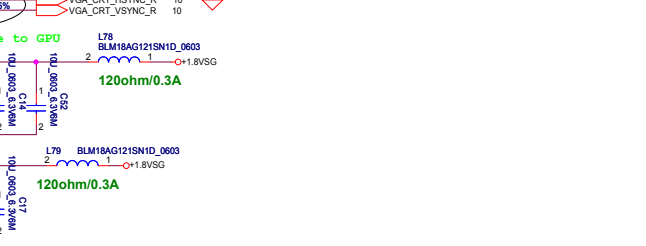
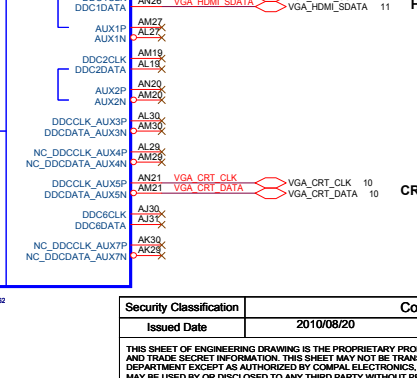
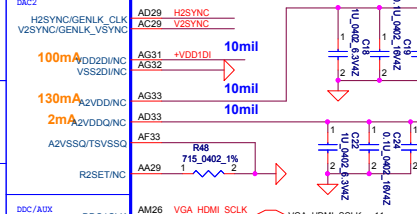
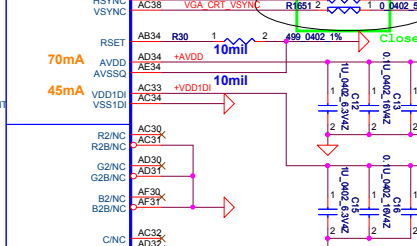
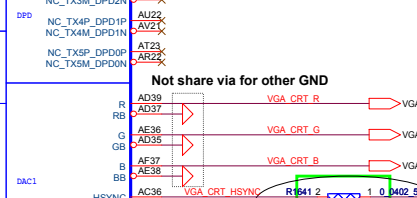
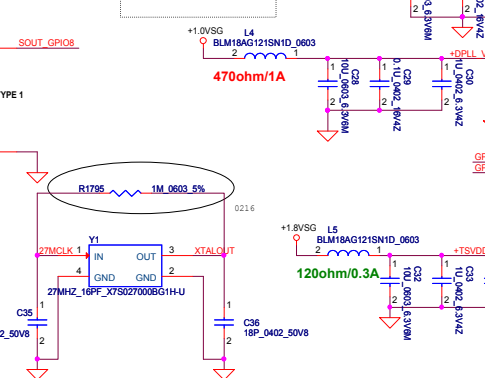
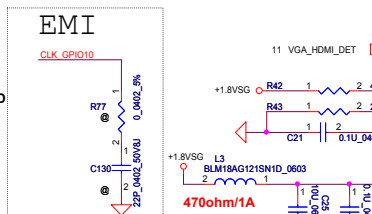
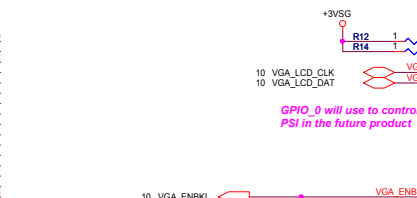
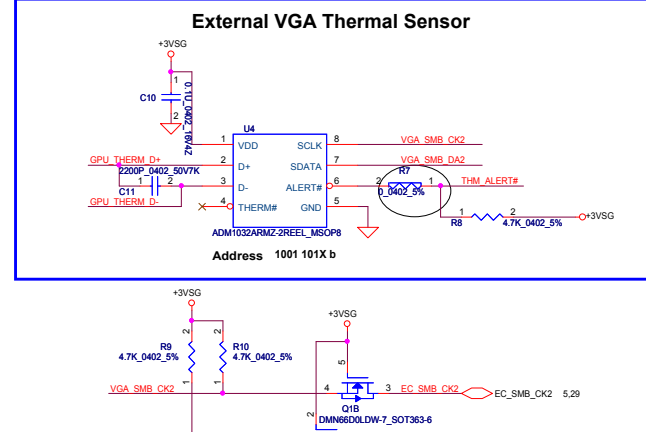
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GFX PCIE LANE REVERSAL



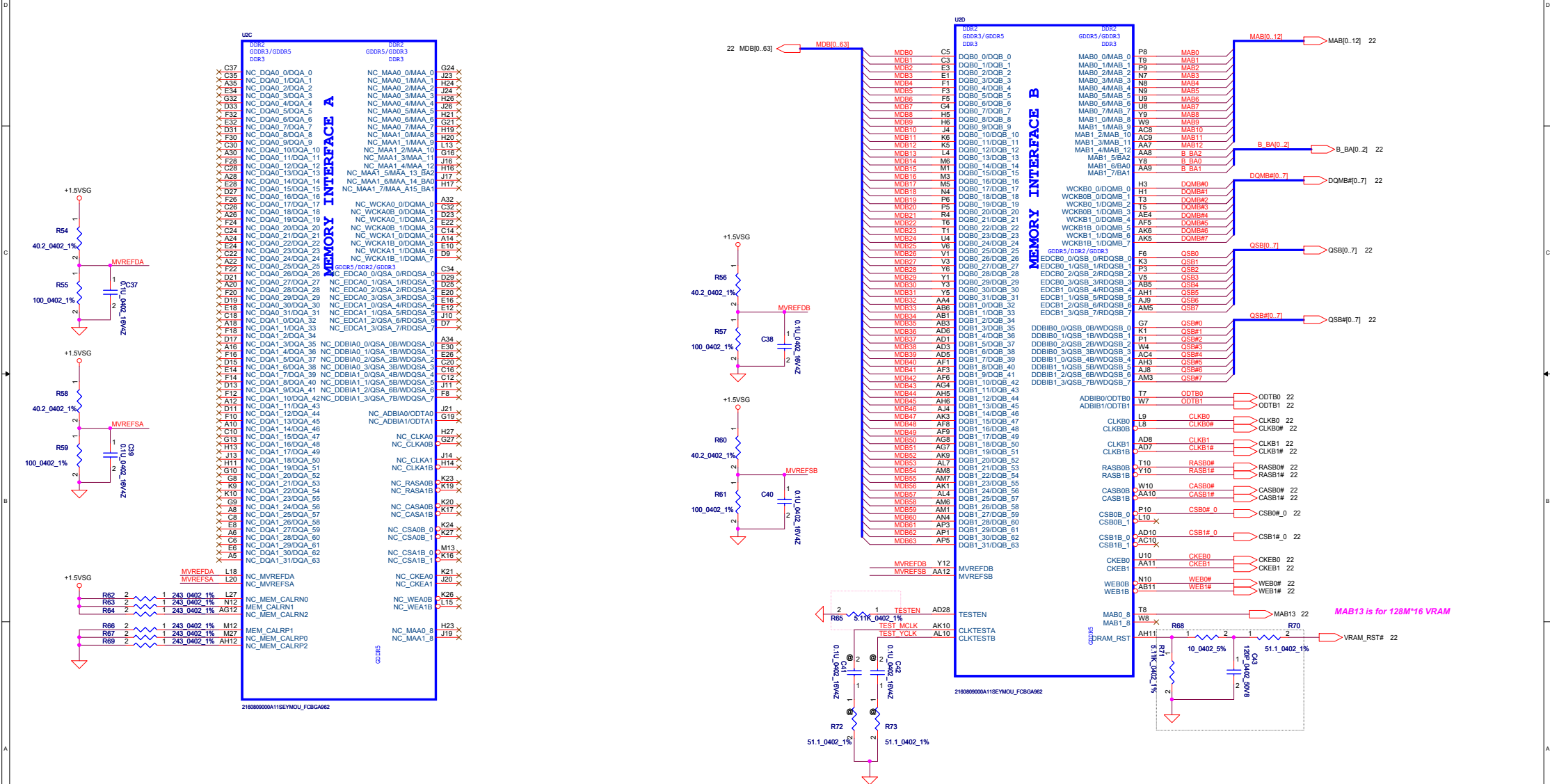
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MUT1 GFX	
✓AR8	NC_DVPCNTL_MVP_0
✓AUS3	NC_DVPCNTL_MVP_1
✓AP8	NC_DVPCNT_0
✓AW8	NC_DVPCNTL_1
✓AP3	NC_DVPCNT_2
✓ART1	NC_DVPCNTL_2
✓AUT1	NC_DVPCLK
VRAM_I00	DVDPDATA_0
VRAM_I01	DVDPDATA_1
VRAM_I02	DVDPDATA_2
VRAM_I03	DVDPDATA_3
	DVDPDATA_4
	DVDPDATA_5
	DVDPDATA_6
	DVDPDATA_7
	DVDPDATA_8
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	DVDPDATA_13
	DVDPDATA_14
	DVDPDATA_15
	DVDPDATA_16
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	NC_DVDPDATA_19
	NC_DVDPDATA_20
	NC_DVDPDATA_21

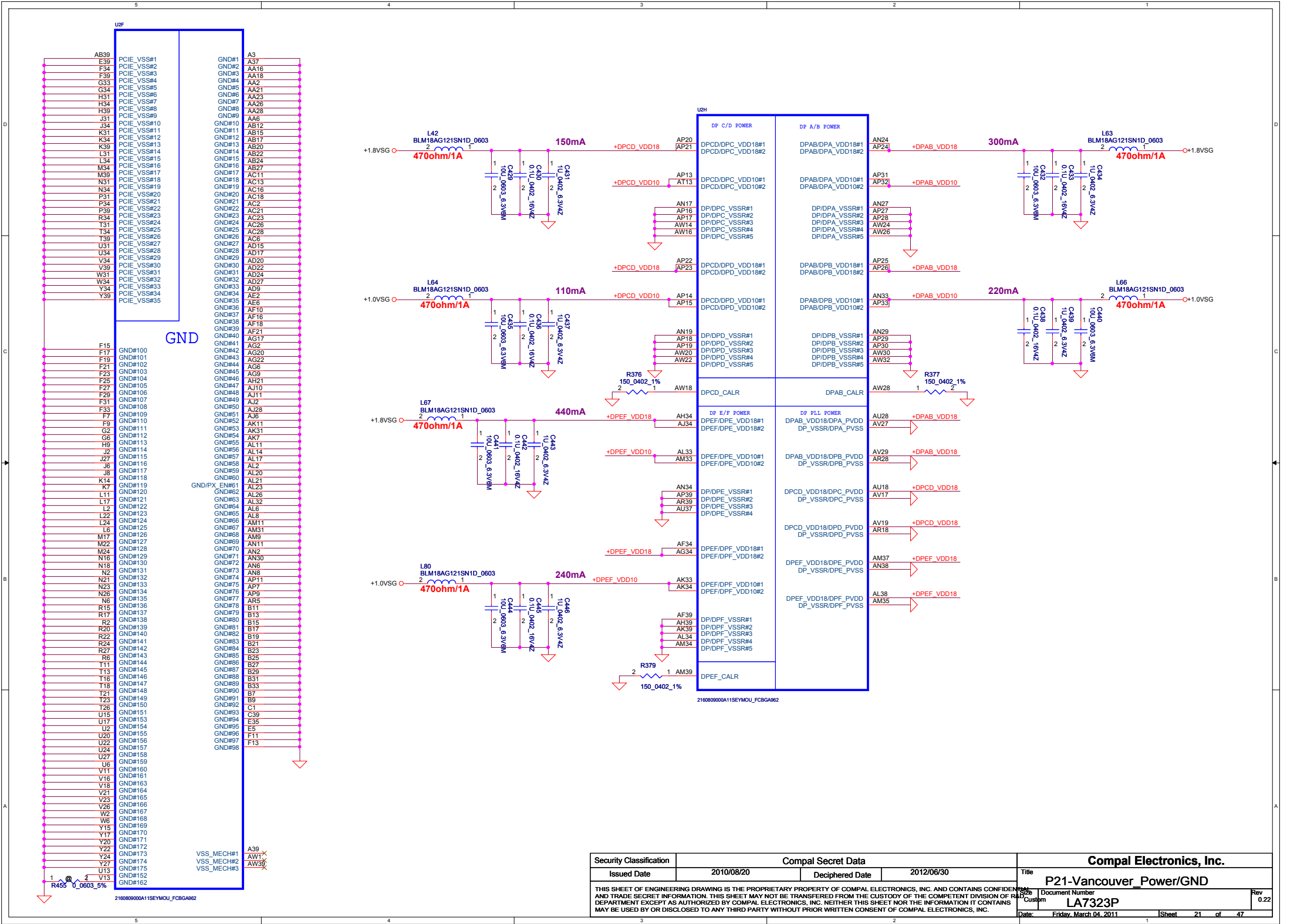


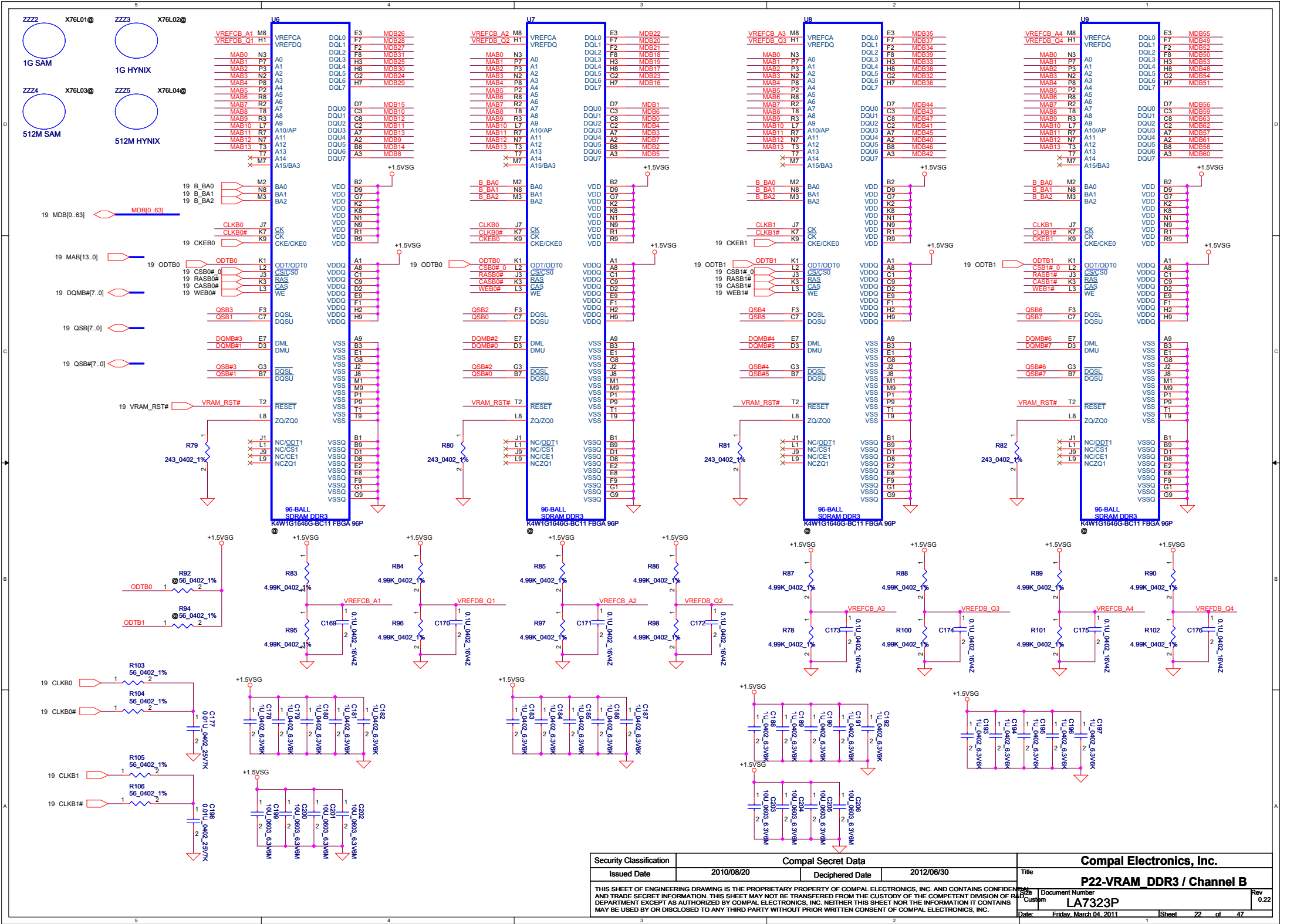
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Robson, Seymour only support single channel memory (channel B only)



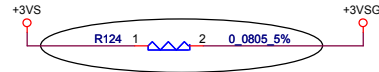
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2010/08/20		2012/06/30		P19-Vancouver_Memory	
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		Customer		LA7323P	
Date:		Friday, March 04, 2011		Sheet 19 of 47	
				Rev 0.22	



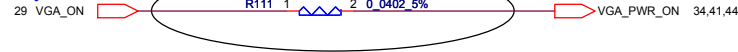


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Issued Date	2010/08/20	Deciphered Date	2012/06/30	Title	P22-VRAM_DDR3 / Channel B
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				Document Number	0.22
				Date:	Friday, March 04, 2011
				Sheet	22 of 47

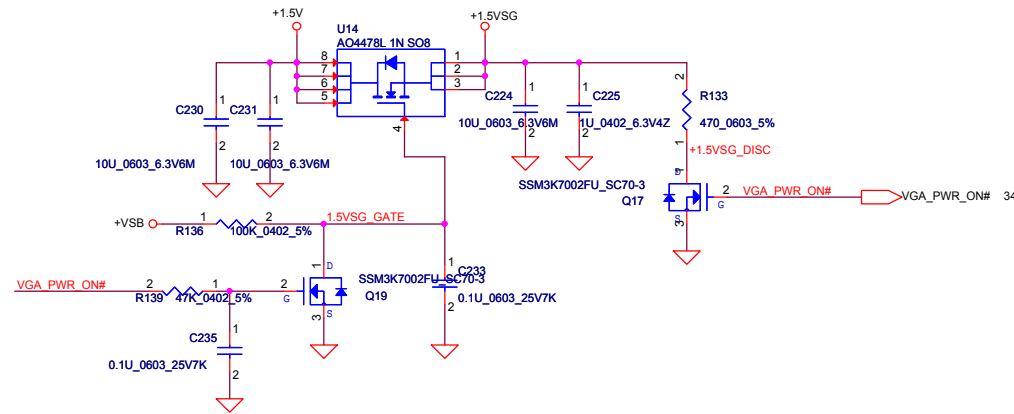
+3.3VS TO +3.3VSG



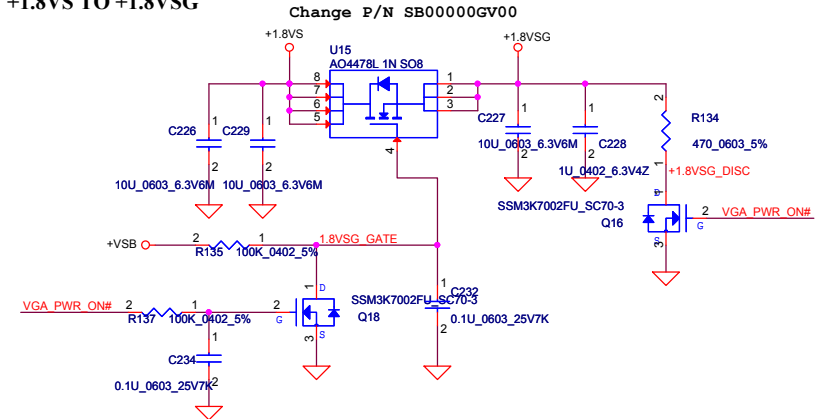
Delay SUSP# 10ms



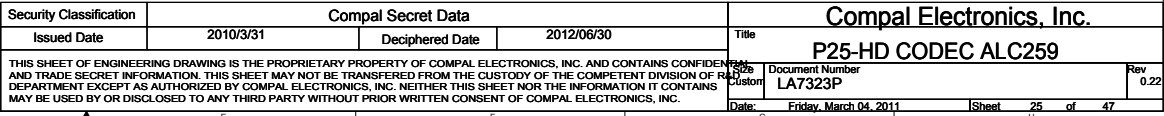
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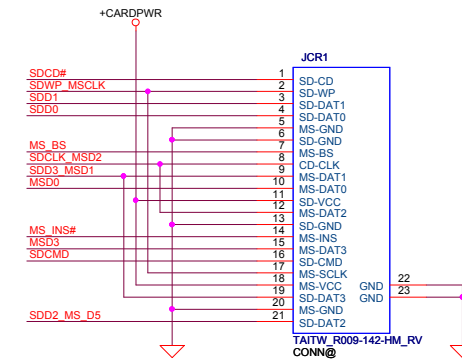
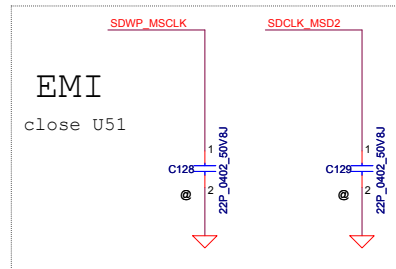
+1.8VS TO +1.8VSG



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				Custom	LA7323P
				Date	Friday, March 04, 2011
				Sheet	23 of 47
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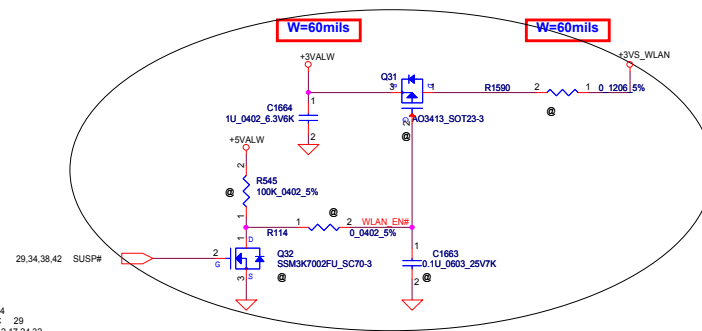
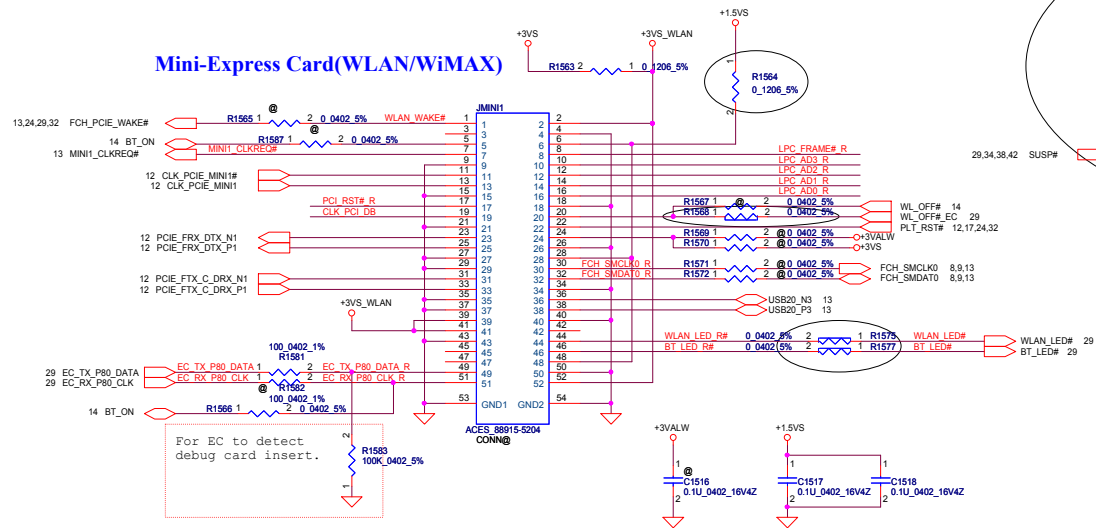


The schematic shows the input circuit for the ADXL345. The +CARDPWV input is connected to a 30mil trace. This trace passes through a 156 ohm resistor (R1562, 100K_0402_5%) and a 0.1uF capacitor (C1514, 0.1U_0402_16V4Z) to ground. The trace then splits to connect to two more capacitors, C1515 and C1513, both 0.1uF 0402 16V4Z, which are also connected to ground. A note 'Close to connector' points to the capacitors.

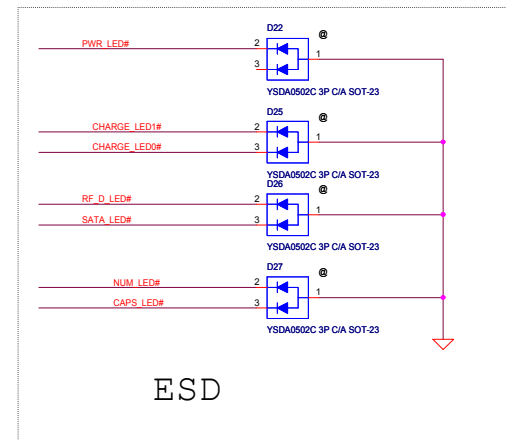
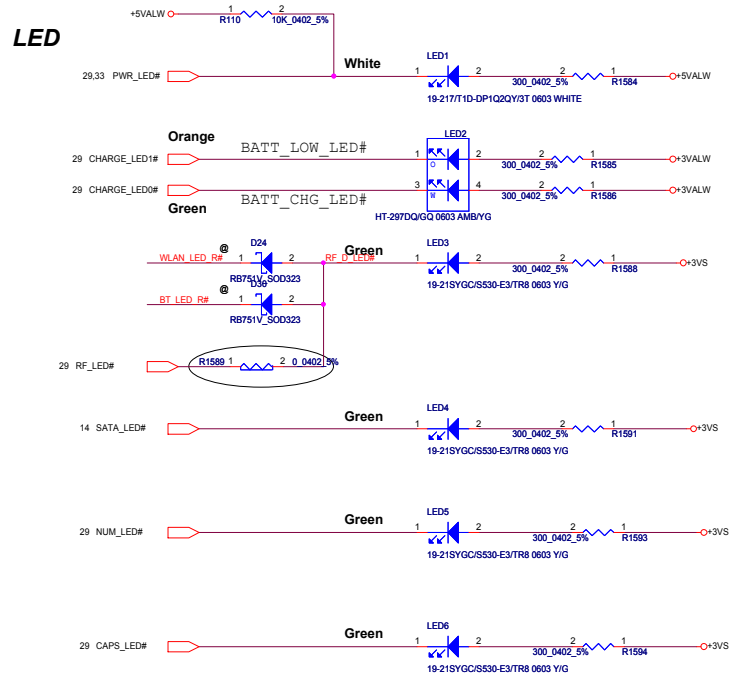
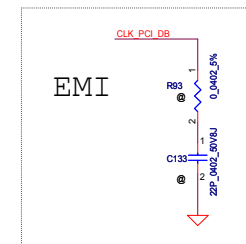
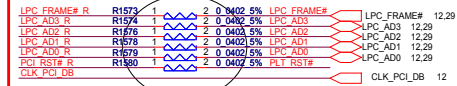


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								Document Number	
Date: Friday, March 04, 2011								Sheet 26 of 47	

Mini-Express Card for WLAN/WiMAX(Half)

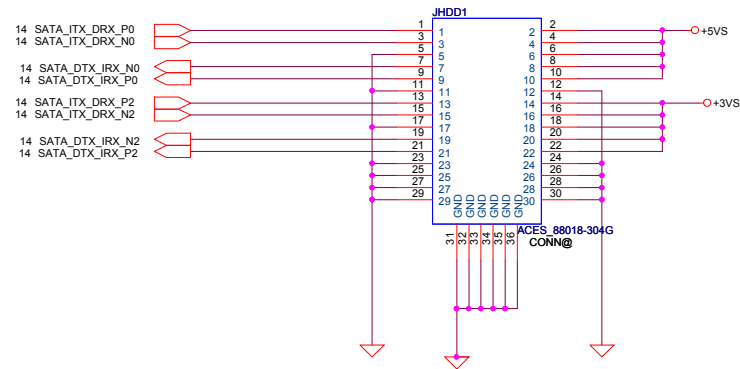


**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

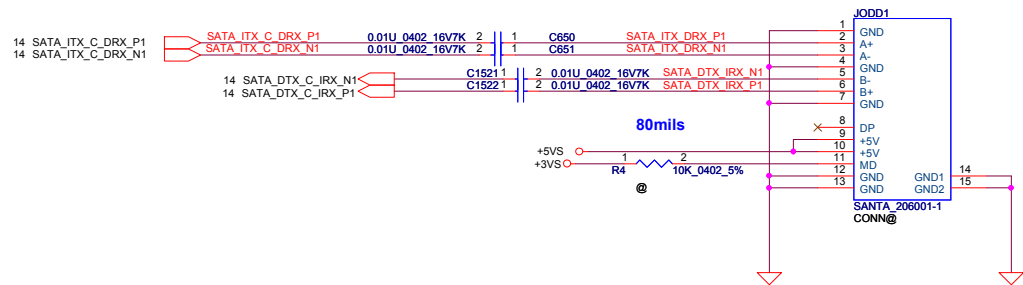


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Issued Date	2010/06/30	Deciphered Date	2012/06/30		
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SATA HDD BTB Conn.

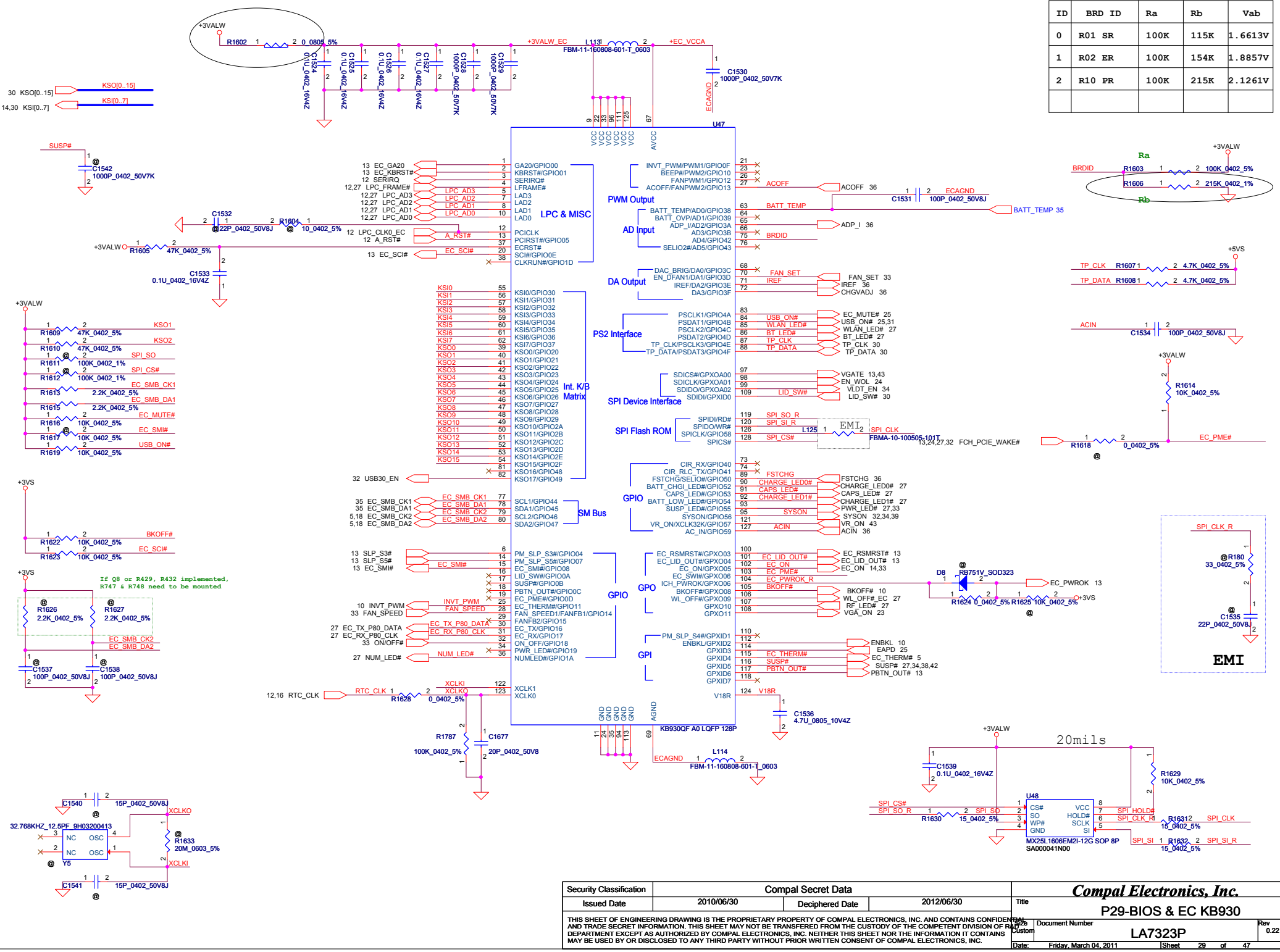


SATA ODD FFC Conn.

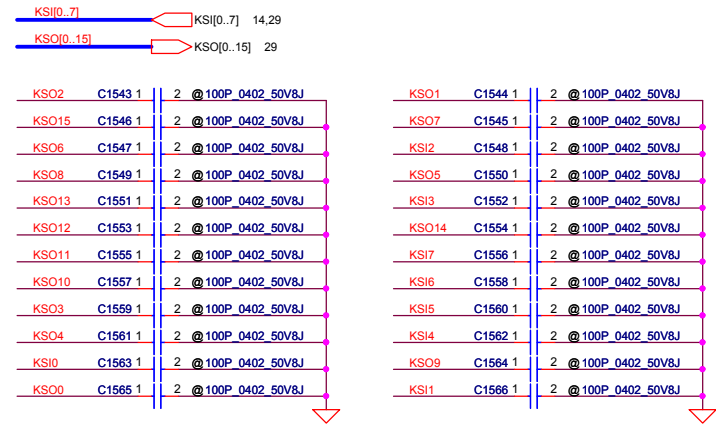


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Issued Date	2010/08/20	Deciphered Date	2012/06/30	Title		
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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	115K	1.6613V
1	R02 ER	100K	154K	1.8857V
2	R10 PR	100K	215K	2.1261V

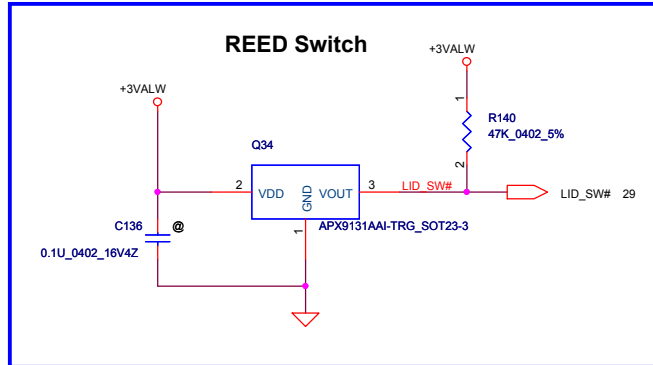
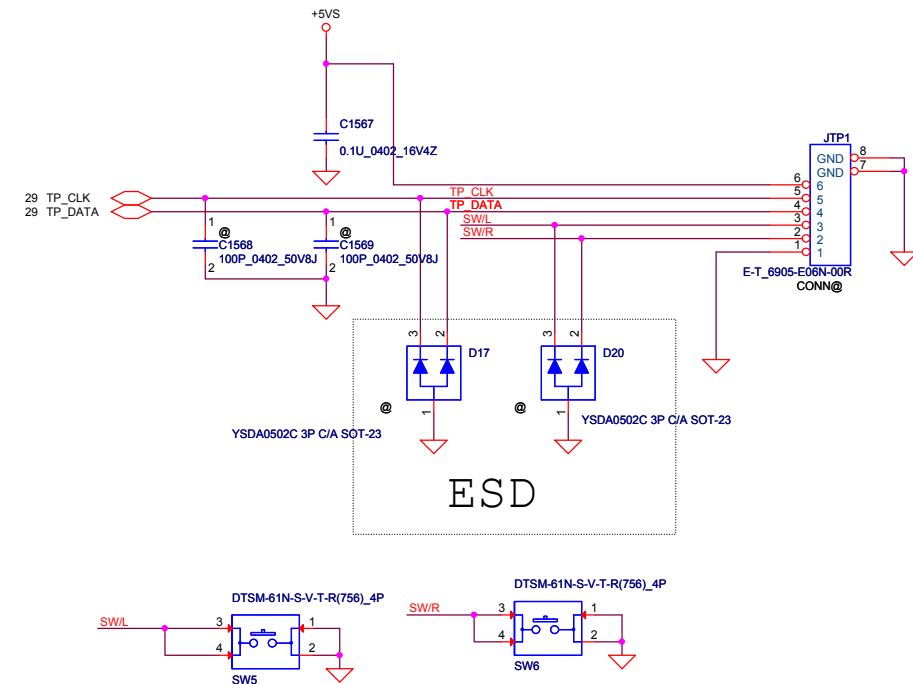


INT_KBD Conn.

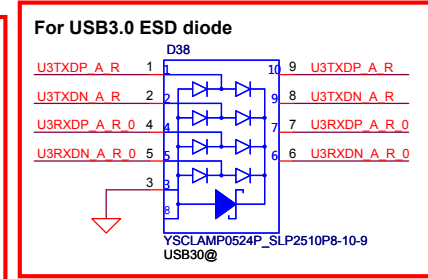
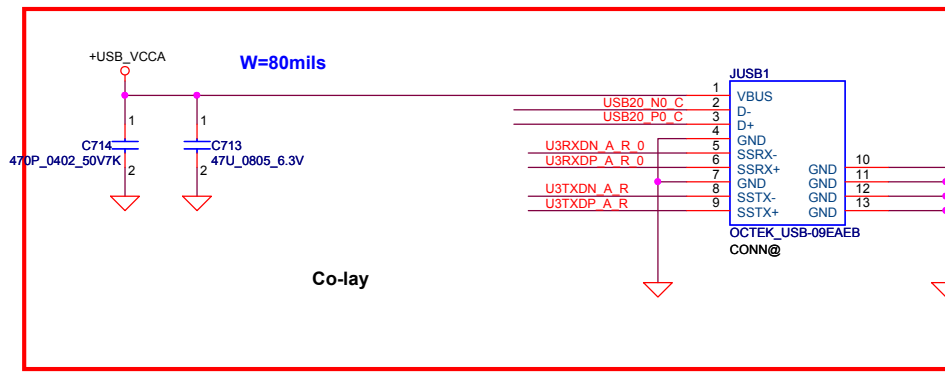
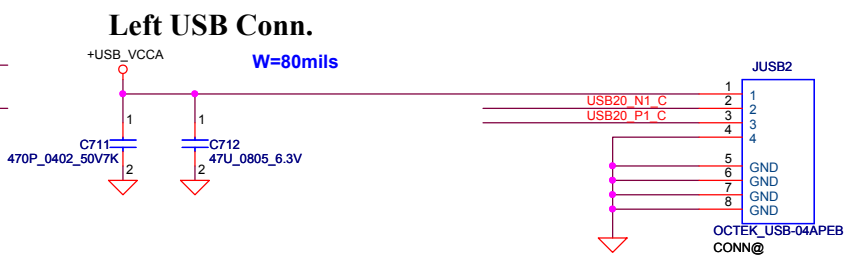
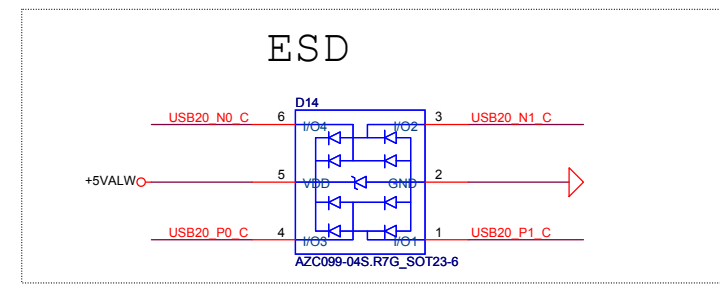


CONN PIN define need double check

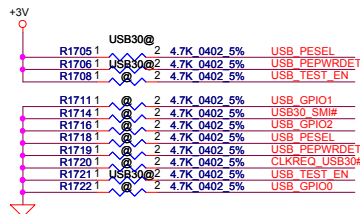
To TP/B Conn.



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Issued Date	2010/08/20	Deciphered Date	2012/06/30	P31-USB/BT/USBSusb				
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				Sheet	Document Number	Rev		
				Custom	LA7323P	0.22		
Date: Friday, March 04, 2011				Sheet	31	of	47	

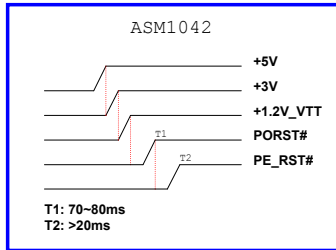


For WAKE Function

USB_PEPWRDET

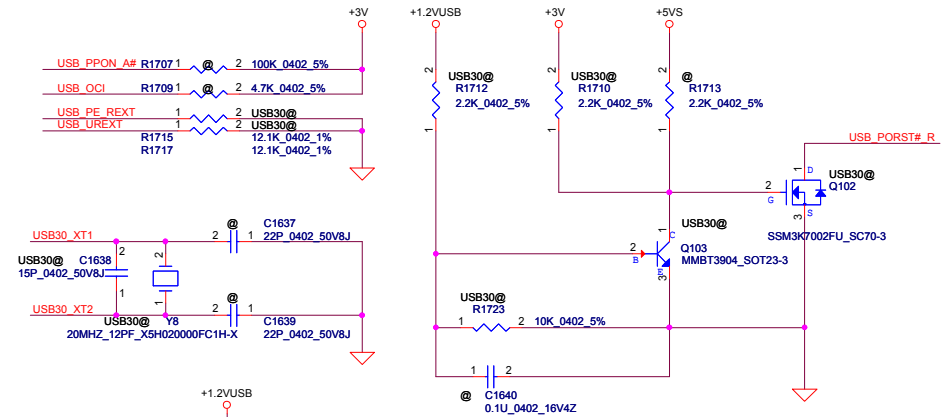
	R1719	R1706
S1	Mount	@
S3	@	Mount

Power Sequence

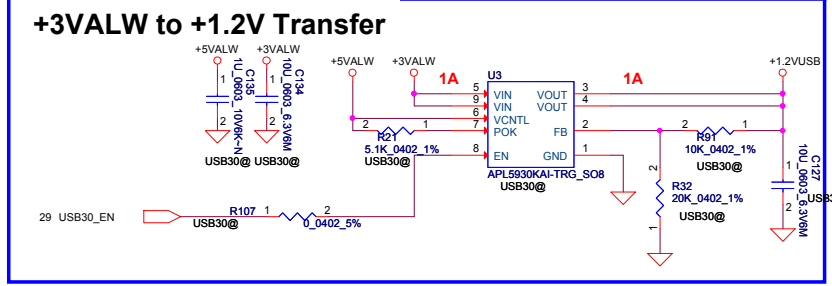
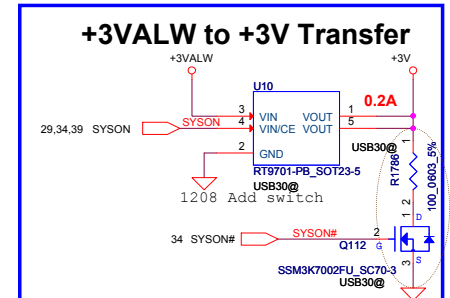
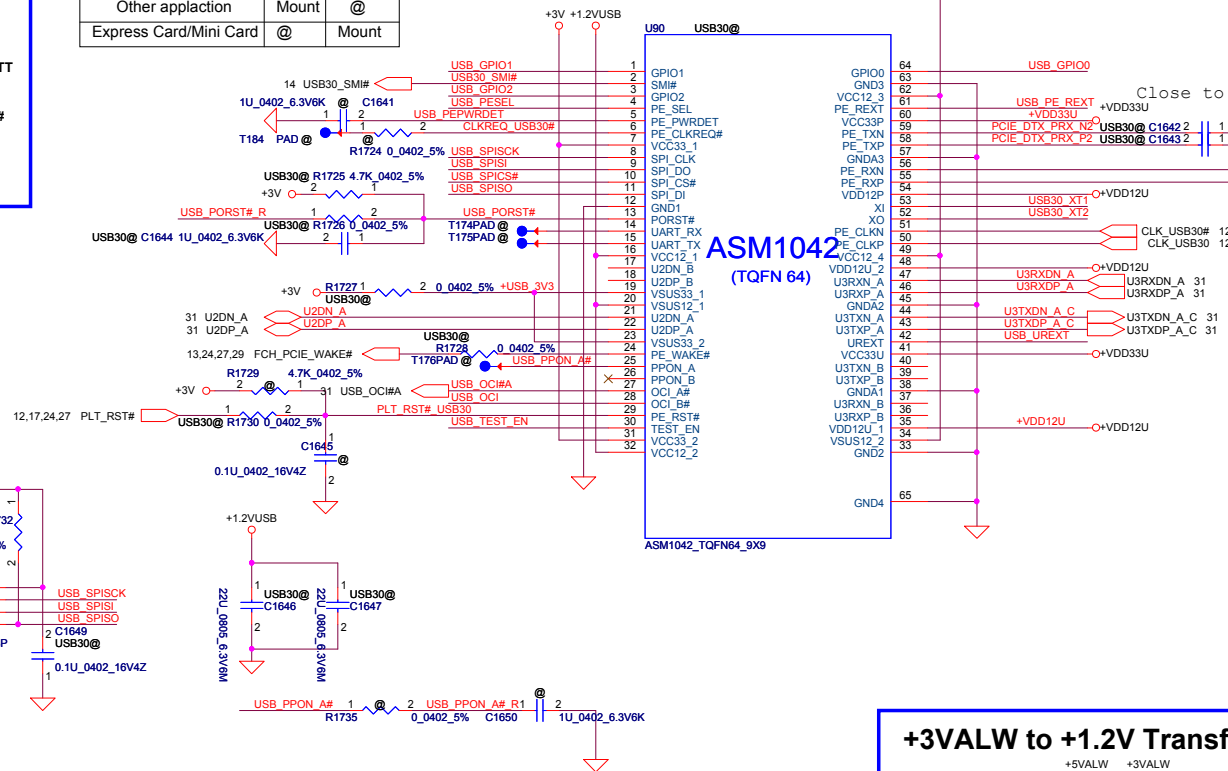


USB_PESSEL

	R808	R825
Other appclation	Mount	@
Express Card/Mini Card	@	Mount



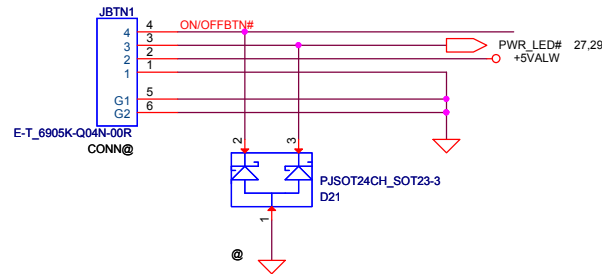
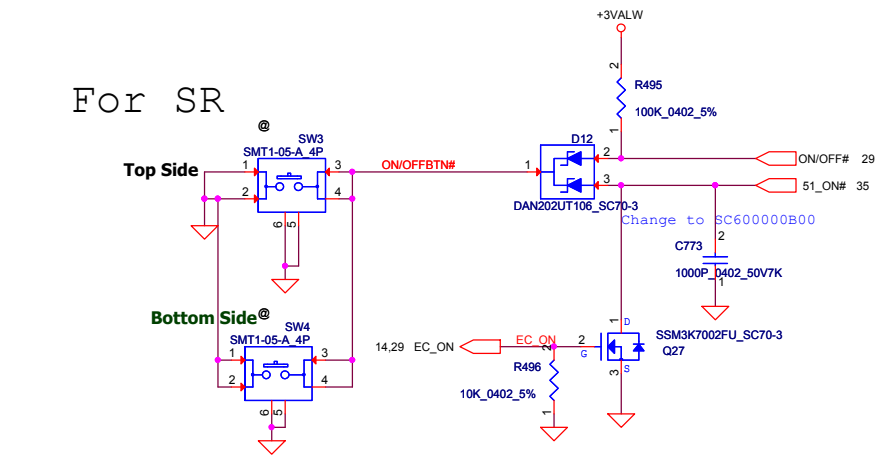
ASM1042
(TQFN 64)



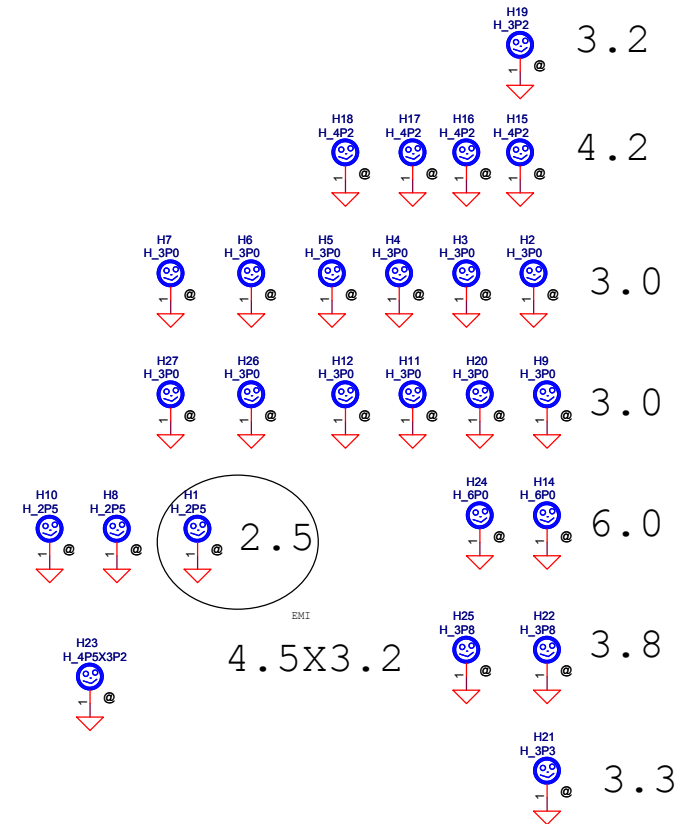
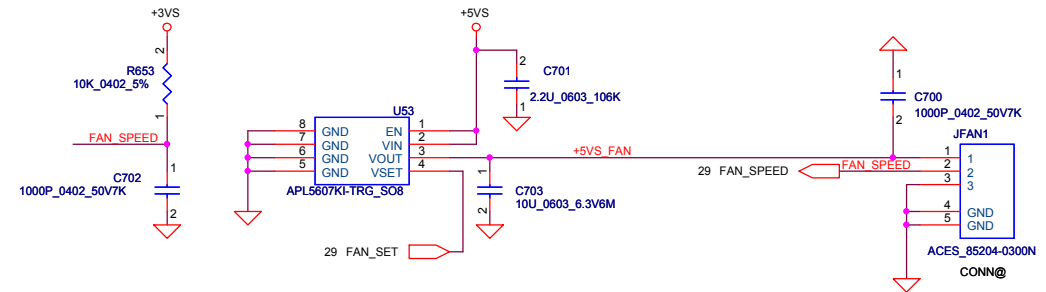
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Date: Friday, March 04, 2011		Sheet		32	of 47

ON/OFF switch **Power Button**

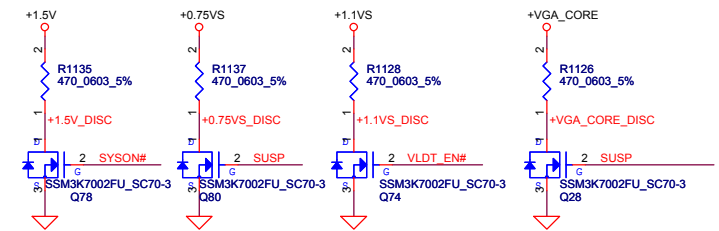
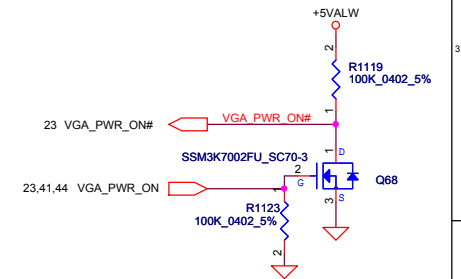
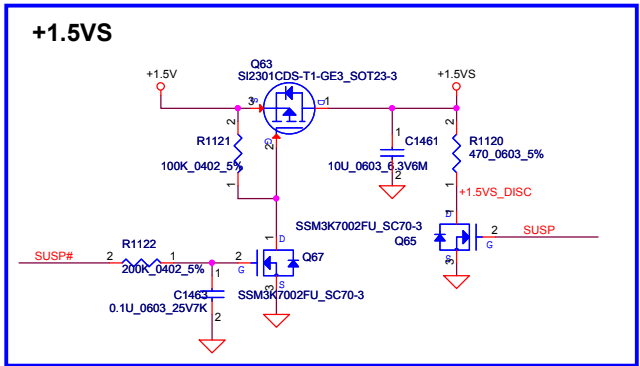
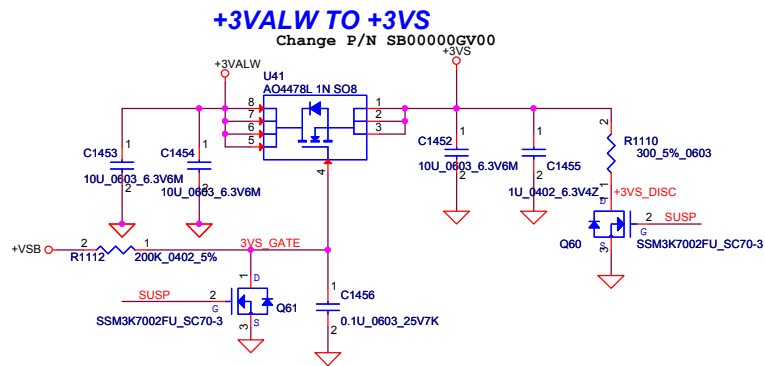
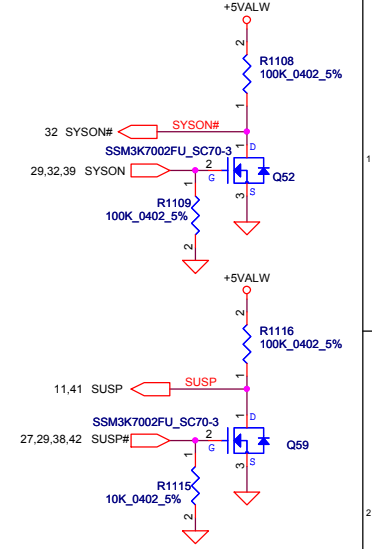
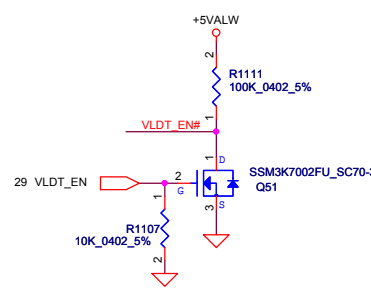
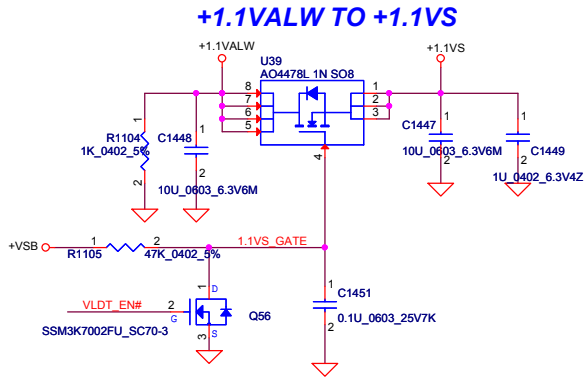
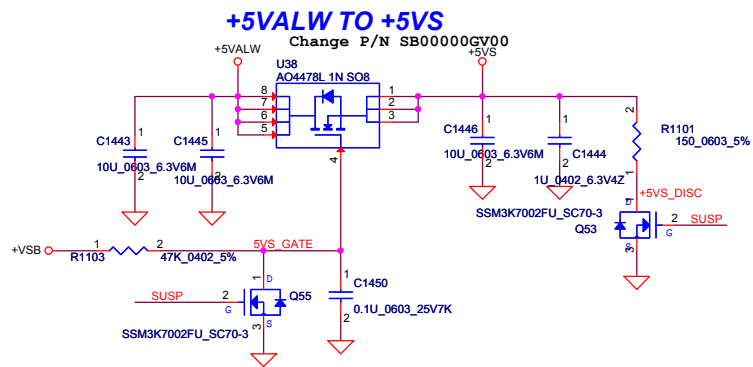
For SR



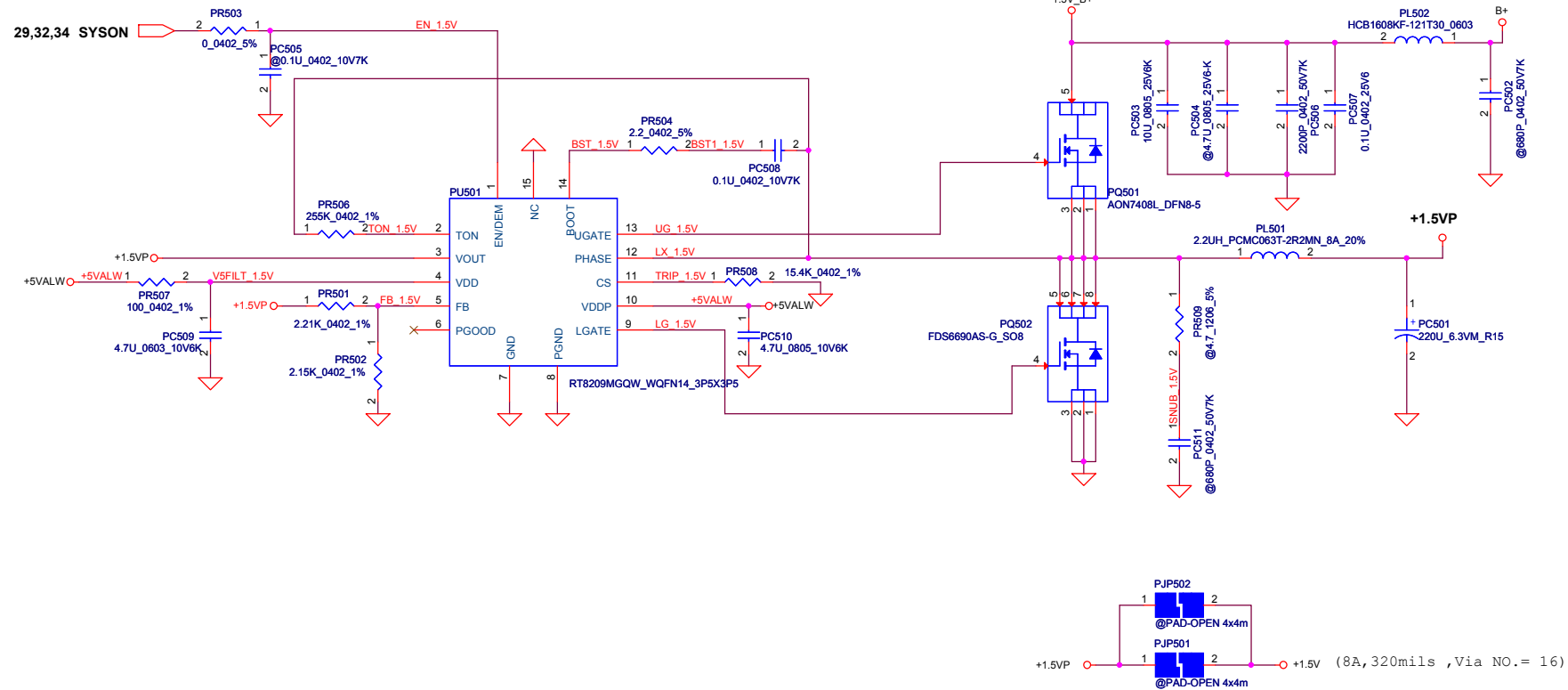
Fan Control Circuit



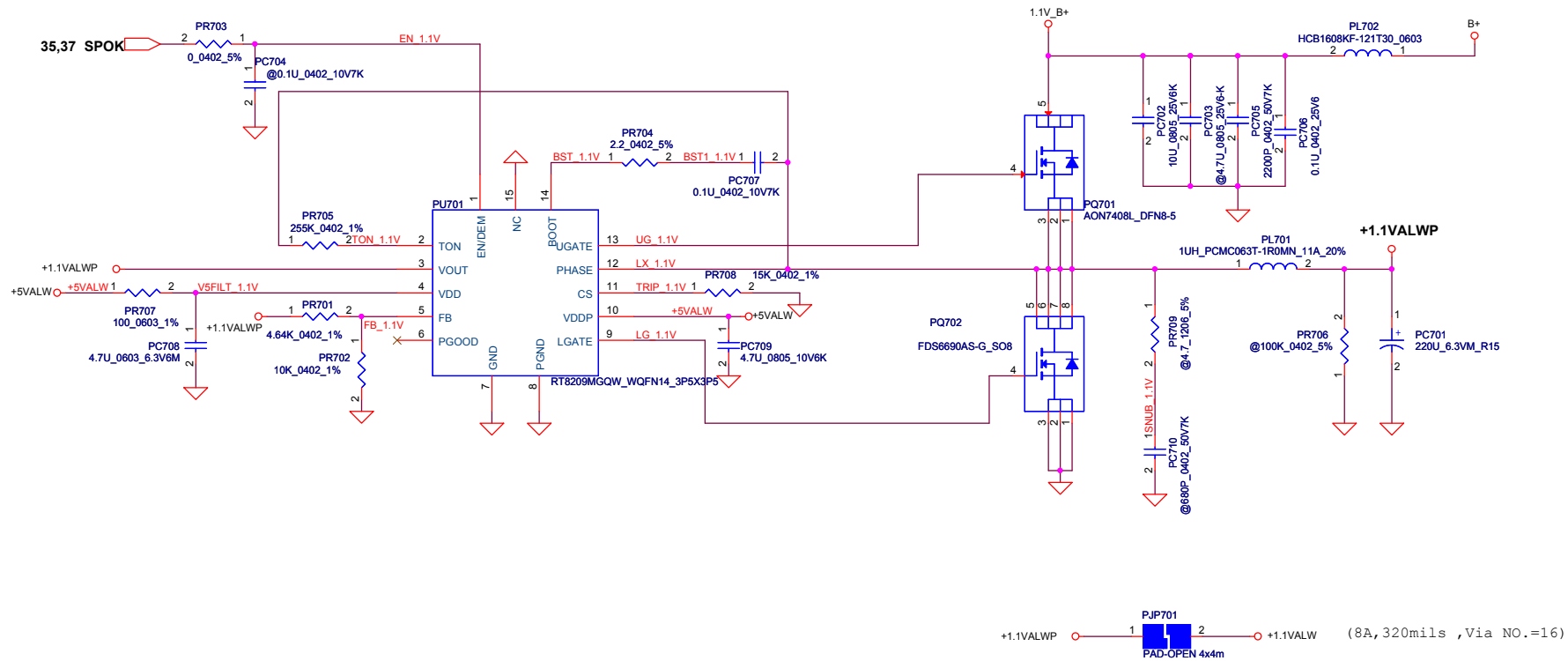
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Issued Date	2010/08/20	Deciphered Date	2012/06/30	Title P33-Other IO/USB (right)		
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				Document Number		Rev	
				LA7323P		0.22	
				Date:		Friday, March 04, 2011	

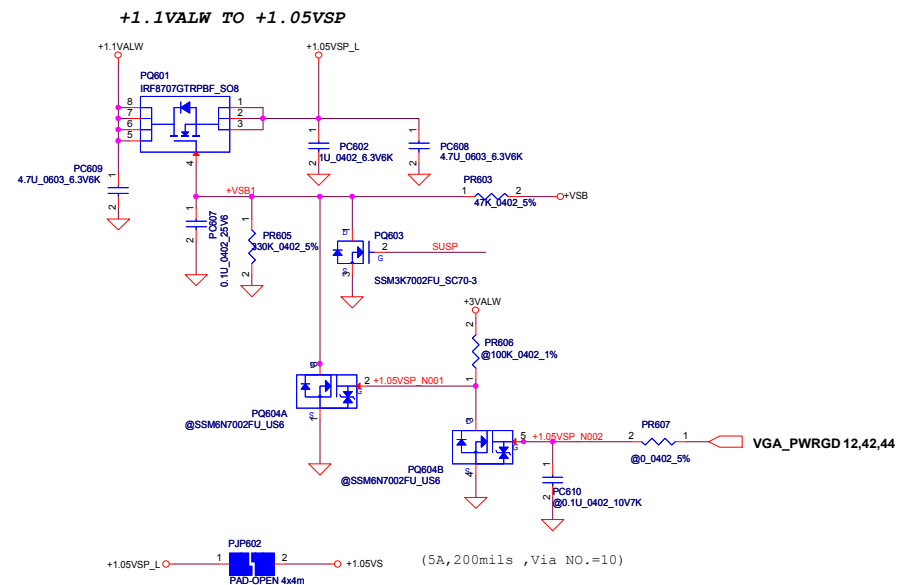
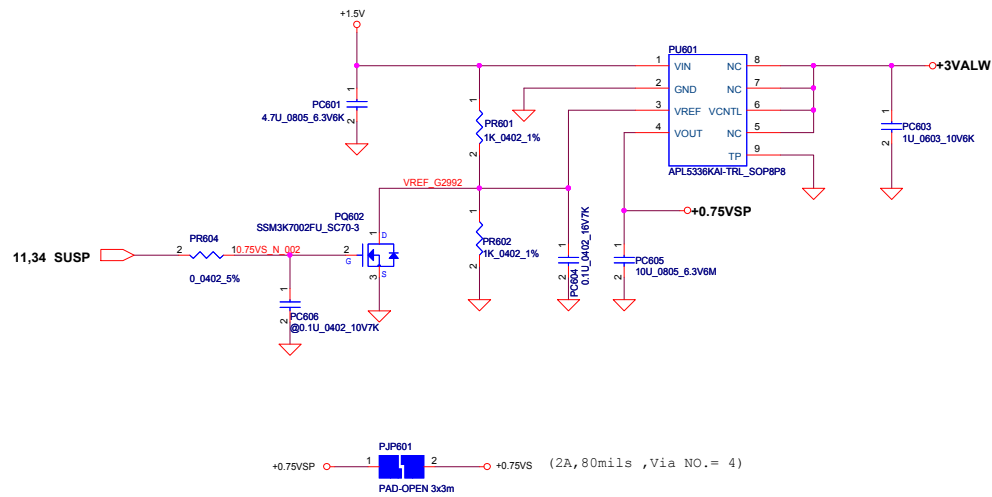


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				Date:	Friday, March 04, 2011
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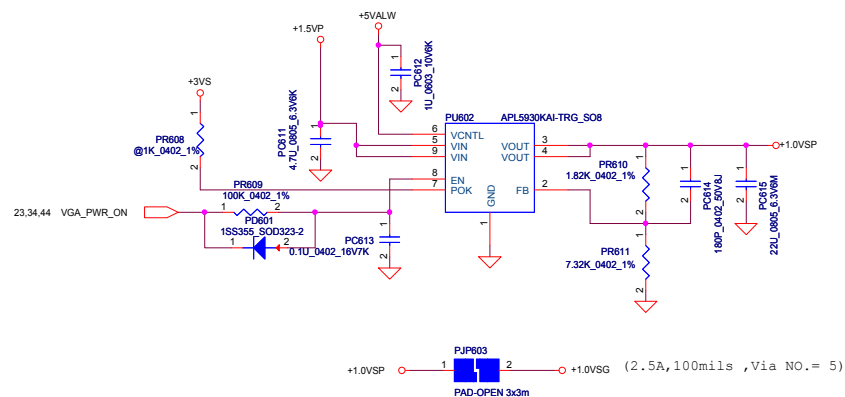


+1.1VALWP 1 PJP701 2 +1.1VALWP (8A, 320mils ,Via NO.=16)
PAD-OPEN 4x4m

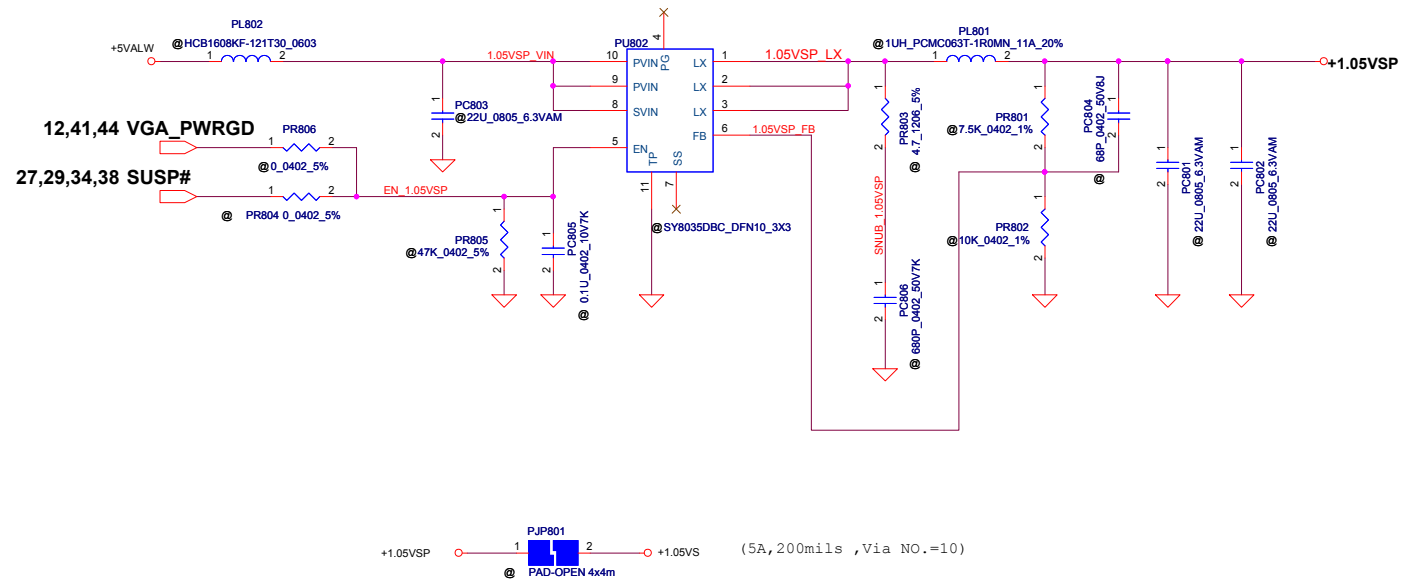
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				Date:	Friday, March 04, 2011
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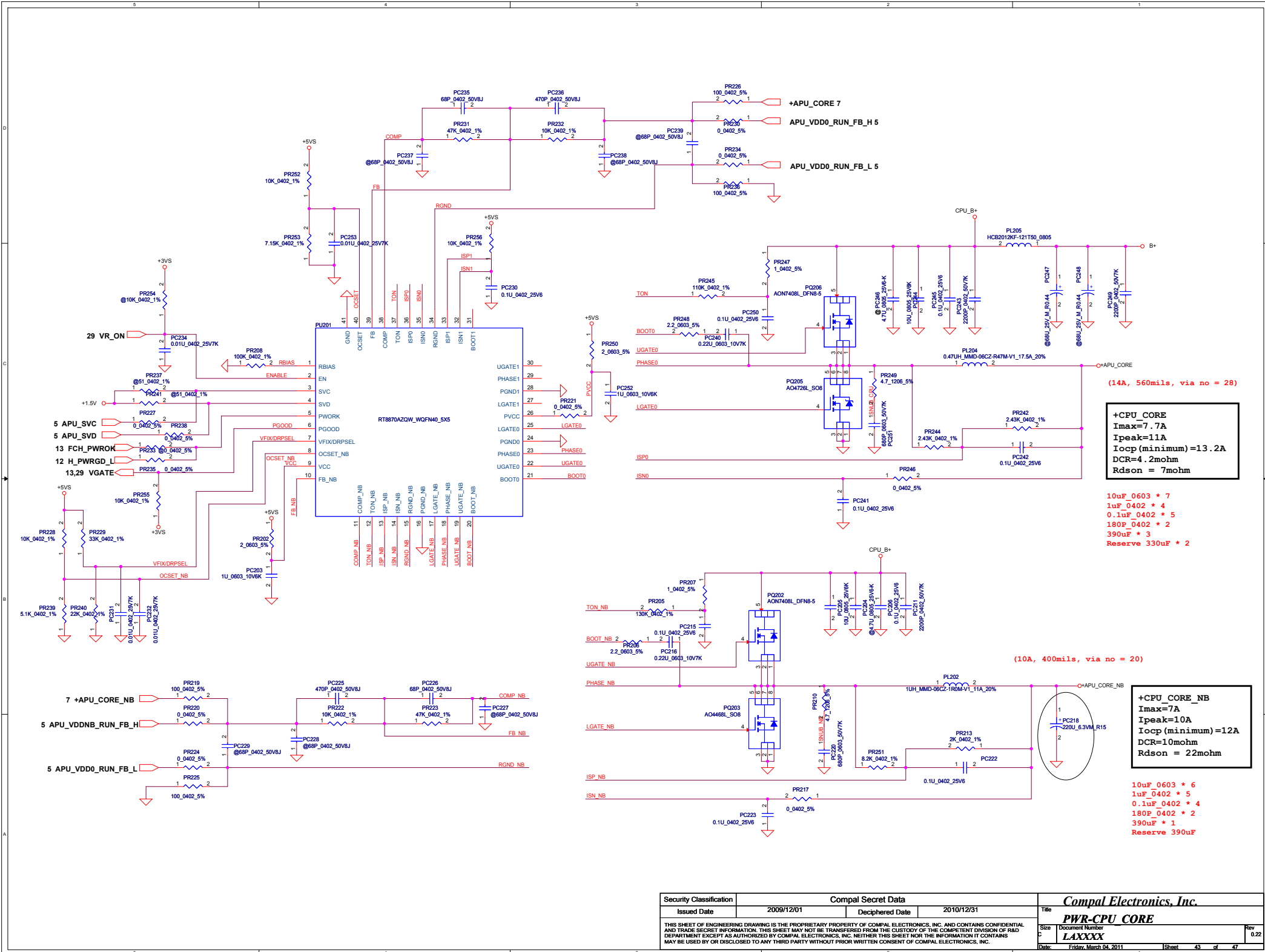
Need to confirm with HW power sequence.



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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title
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				Rev
				0.22
Date: Friday, March 04, 2011		Sheet 42 of 47		



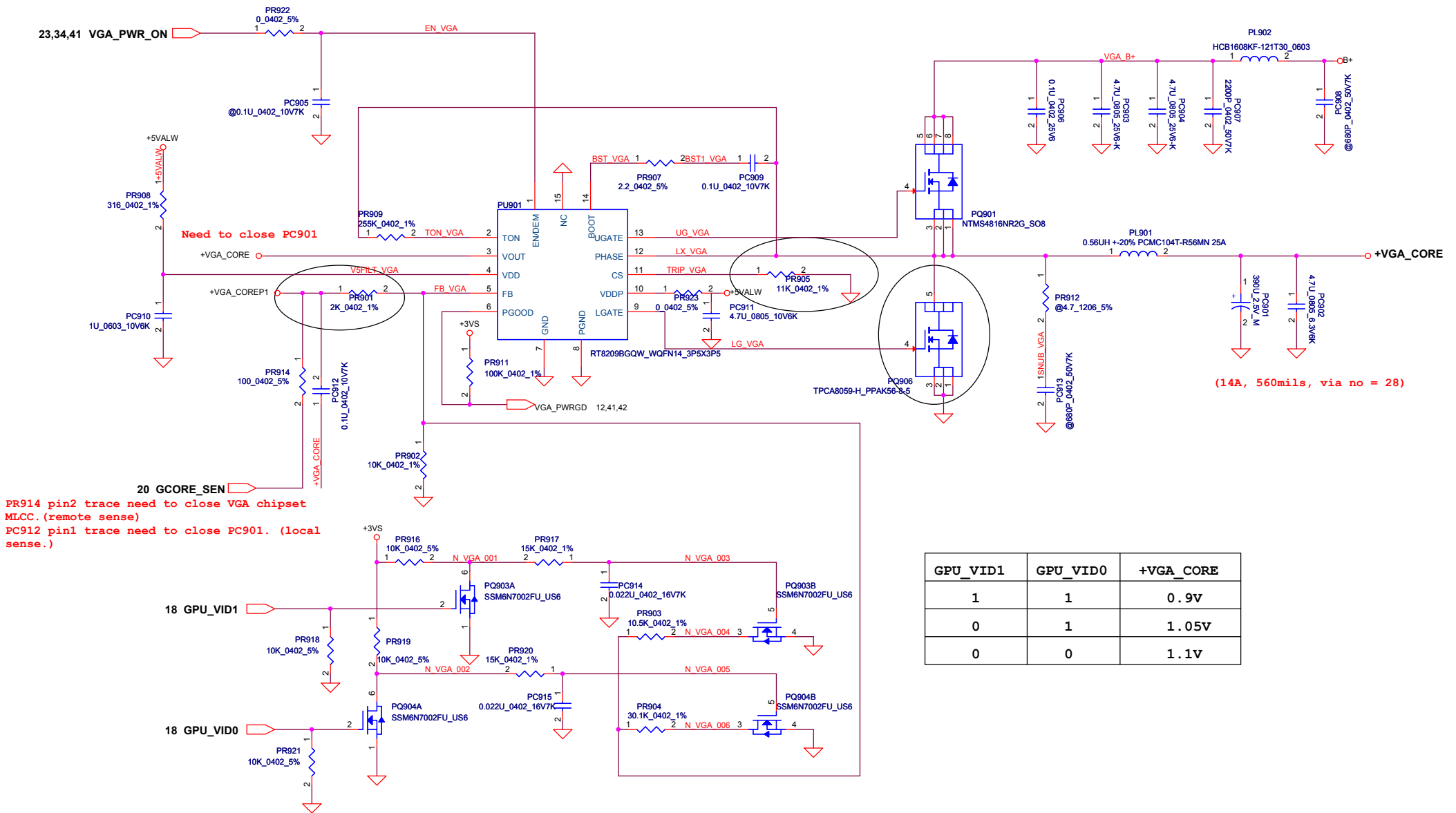
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Ipeak=11A
Iocp(minimum)=13.2A
DCR=4.2mohm
Rdson = 7mohm

10uF 0603 * 7
1uF 0402 * 4
0.1uF 0402 * 5
180P 0402 * 2
390uF * 3
Reserve 330uF * 2

+CPU_CORE_NB
Imax=7A
Ipeak=10A
Iocp(minimum)=12A
DCR=10mohm
Rdson = 22mohm

10uF 0603 * 6
1uF 0402 * 5
0.1uF 0402 * 4
180P 0402 * 2
390uF * 1
Reserve 390uF

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR-CPU CORE
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				Rev	0.22



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Compal Electronics, Inc. Changed-List History	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		DFB request	0.11	PG#10	change JLVS1 connector to 40 pin and add JCM1 6pin	12/17	ER
2		EC remove ext crystal	0.11	PG#29	Add R1787 and C1677	12/17	ER
3		DFB request for soldering	0.11	PG#30 PG#33	Change JTP1 and JBTN1 footprint	12/17	ER
4		JUSB2 no function	0.11	PG#31	Update JUSB2 symbol	12/17	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/17	ER
6		LID issue	0.11	PG#29	LID_SW# added a pull up 10Kohm. (R35)	12/17	ER
7		Update Broad ID	0.11	PG#29	Change R1606 to 154Kohm	12/17	ER
8		for BIOS crisis	0.12	PG#14	Add U11	12/17	ER
9		DDR3 SPD	0.12	PG#8	Reserve R152 , R155	12/17	ER
10		For discharge spec	0.13	PG#24	Add R1788 and Q113 discharge schematic	12/17	ER
11		For EMI test	0.2	PG#11	Remove Level Shifter schematic	12/17	ER
12		BIOS change to share ROM	0.2	PG#16 PG#29	Pop R594 and R602 , unpop R601 and R550 change U48 meterial	12/17	ER
13		Fix S3 resume black screen	0.21	PG#6	Add R1790 , R1791 68ohm pull down	02/18	PR
14		DFX request	0.21	PG#11	Update JDIMM2 footprint	02/18	PR
15		Fix S3 resume too long	0.21	PG#18	Add R1795 1M ohm	02/18	PR
16		Fix assembly issue	0.21	PG#29 PG#25	Update JKB1 and JAU1 footprint for ME connector	02/18	PR
17		EMI request	0.22	PG#11	pop L11~L14	02/22	PR
18							
19							
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27							

Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>				
Issued Date		2010/09/30	Deciphered Date	2010/12/31	Title			
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POWER SEQUENCE

