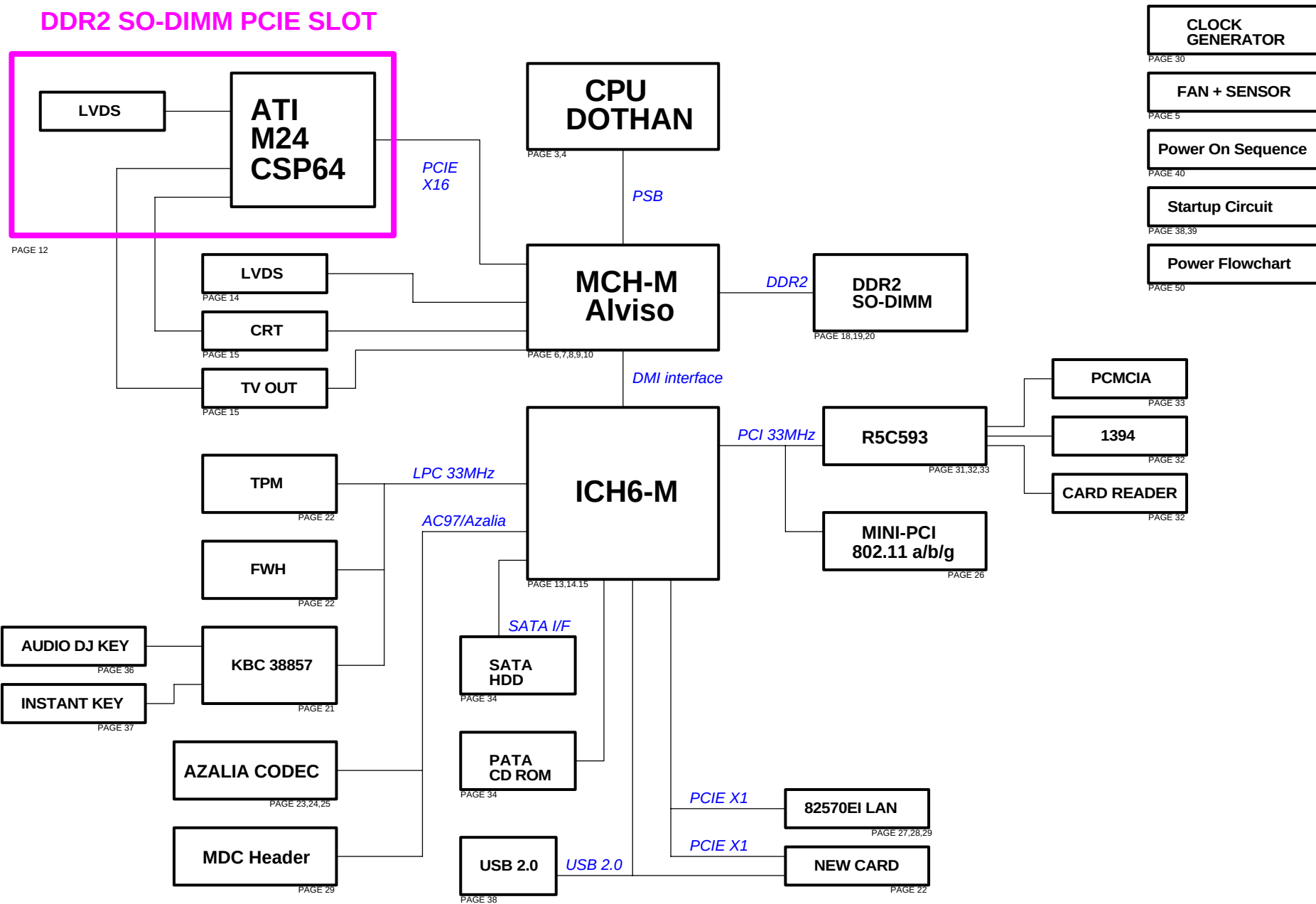


DDR2 SO-DIMM PCIE SLOT



REVISION LIST

R0.7	2003/10/13	Only chipset circuit but not including DC to DC power circuit
R0.8	2003/10/31	Add Intel 82570 chipset circuit and TPM socket
R0.9	2003/11/04	Add AZALIA CMI9880 chipset circuit and ALS I/F
R0.95	2003/11/10	Key Board changed to OKI HMB989-C Matrix

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT1_IN#_OC	I	+3.3V
BAT2_IN#_OC	I	+3.3V
CHG_EN_OC	I	+3.3V
CHG_LED	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SMCLK_BAT2	IO	+3.3V
SMDATA_BAT2	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.5A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
+1.5VSUS	1.5V	270 mA
+1.8V	1.8V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	390 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 22 mils
IN1/IN3 16 mils

37.5 OHM WIDTH

TOP/BOT 13.5 mils
IN1/IN3 10 mils

42 OHM WIDTH

TOP/BOT 11 mils
IN1/IN3 8.5 mils

55 OHM WIDTH

TOP/BOT 6 mils
IN1/IN3 5 mils

75 OHM WIDTH

TOP/BOT 2.5 mils
IN1/IN3 2 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 8 mils/ 4 mils
IN1/IN3 8 mils/ 3.5 mils

90 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 5 mils
IN1/IN3 5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 4 mils/ 6 mils
IN1/IN3 4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394 PCI_REQ#1
MINIPCI PCI_REQ#3

IDSEL

CB&1394 PCI_AD17
MINIPCI PCI_AD19

PCIE Device

PEG

ATI M24

PCIE Giga NIC

Intel 82570EI

PCB STACK-UP

PCB THICKNESS: 1.2 mm

- L1 TOP
- L2 GND1
- L3 IN1
- L4 IN2
- L5 VCC
- L6 IN3
- L7 GND2
- L8 BOT

PAGE 41

SIGNAL	IN:	VR_VID0 - 5 PM_DPRSLPVR STP_CPU# PM_PSI# IMVP_VR_ON
	OUT:	DELAY_VR_PWRGD VR_PWDGD_CK410#
POWER	IN:	AC_BAT_SYS +5V0 +3V0
	OUT:	+VCORE

PAGE 42

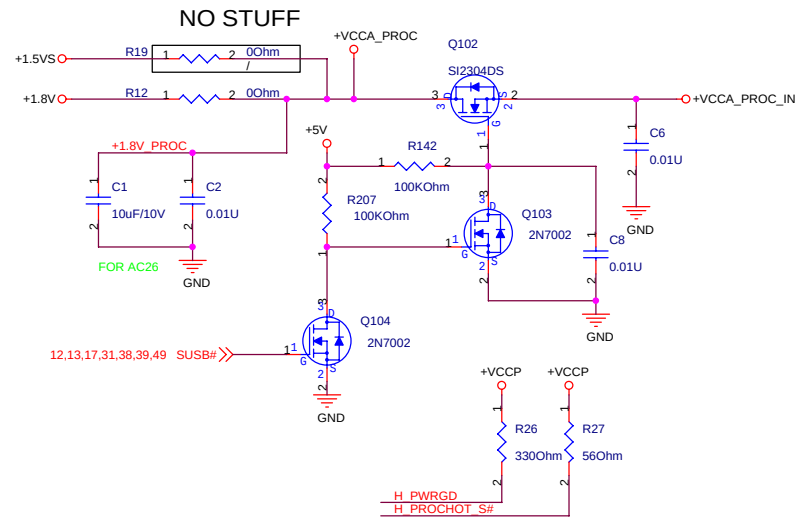
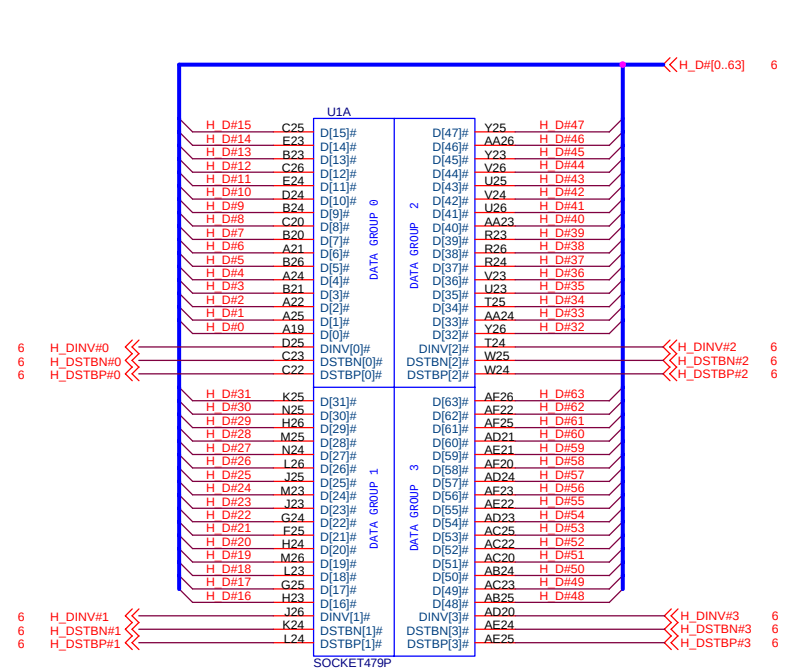
SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12V0 +3V0 +5V0

PAGE 43

SIGNAL	IN:	SUSB#_PWR SUSC#_PWR
POWER	IN:	AC_BAT_SYS +3V0
	OUT:	+1.8V +1.5V +2.5V +VCC_GMCH_CORE +5VALWAYS +3VALWAYS

PAGE 44

SIGNAL	IN:	SUSB#_PWR
	OUT:	VCC_MCH_VRPWRGD IMVP_VR_ON
POWER	IN:	+3VA +3V +1.8V +VCC_GMCH_CORE
	OUT:	+0.9VS +1.5VA +VCCP



The diagram illustrates the architecture of a 2D CNN. It starts with six input images labeled H_VID5, H_VID4, H_VID3, H_VID2, H_VID1, and H_VID0. These inputs are processed through a series of layers: RN1A, RN1B, RN1C, and RN1D. Each of these layers is followed by a pooling operation labeled 00hnm. The outputs of these layers are then processed by R9 and R10, which are also followed by pooling operations labeled 00hnm. The final outputs are VR_VID5, VR_VID4, VR_VID3, VR_VID2, VR_VID1, and VR_VID0. The diagram uses color-coded lines to show the flow of data: red for H_VID5, blue for H_VID4, green for H_VID3, purple for H_VID2, yellow for H_VID1, and pink for H_VID0. The pooling operations are represented by blue boxes with the label 00hnm. The final outputs are shown in red boxes.

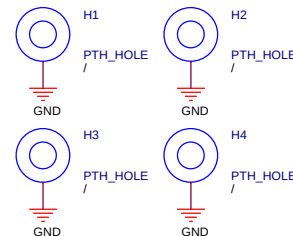
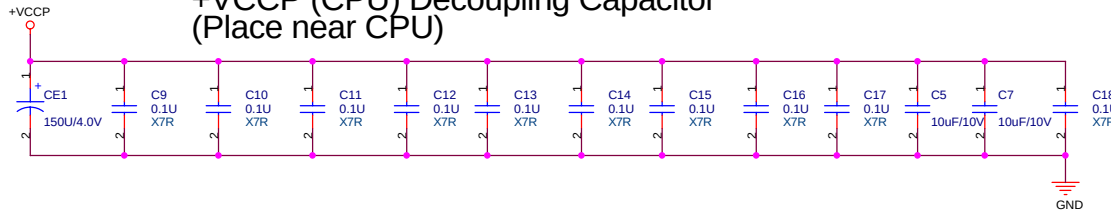
1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

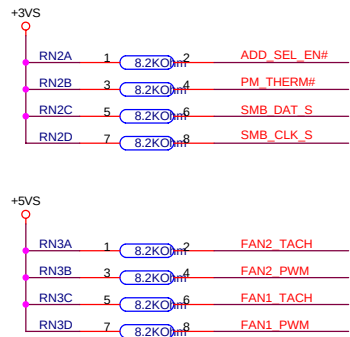
0.745V - 1.356V(+/- 1.5%)
C0: 27 A
C3: 7.59A
C4: 0.9A

VCC

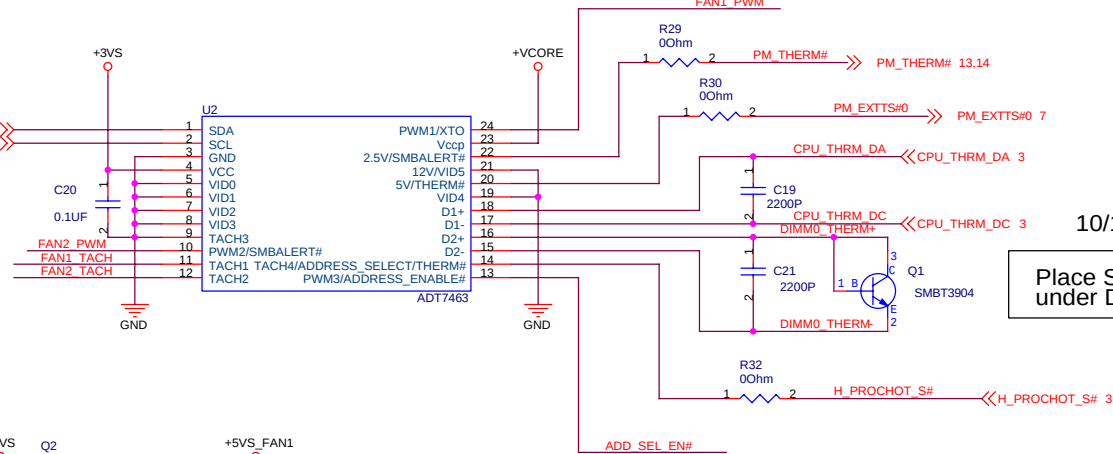
GND

+VCCP (CPU) Decoupling Capacitor
(Place near CPU)



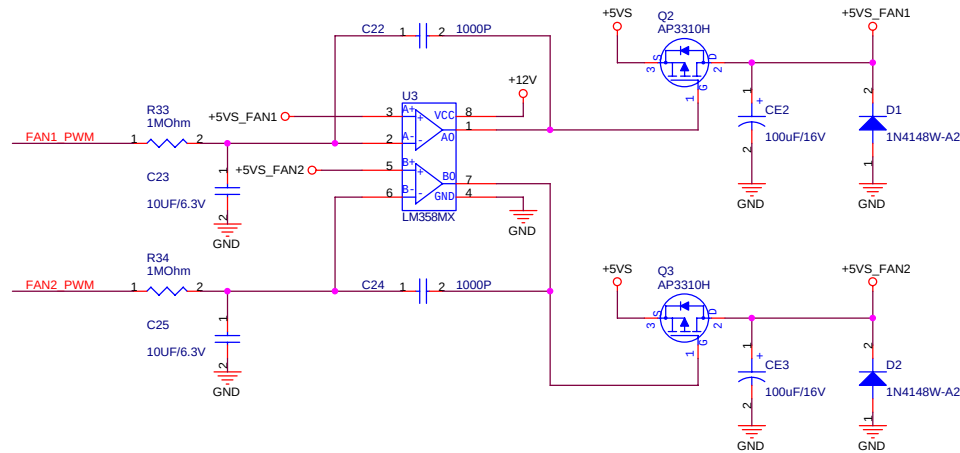


12,13,18,19,22,30 SMB_DAT_S
12,13,18,19,22,30 SMB_CLK_S

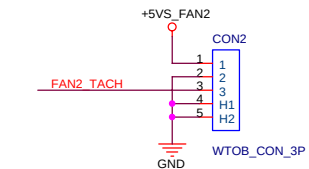
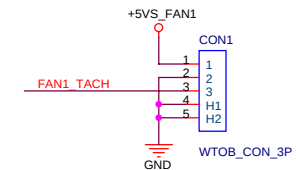


10/10/10 mil

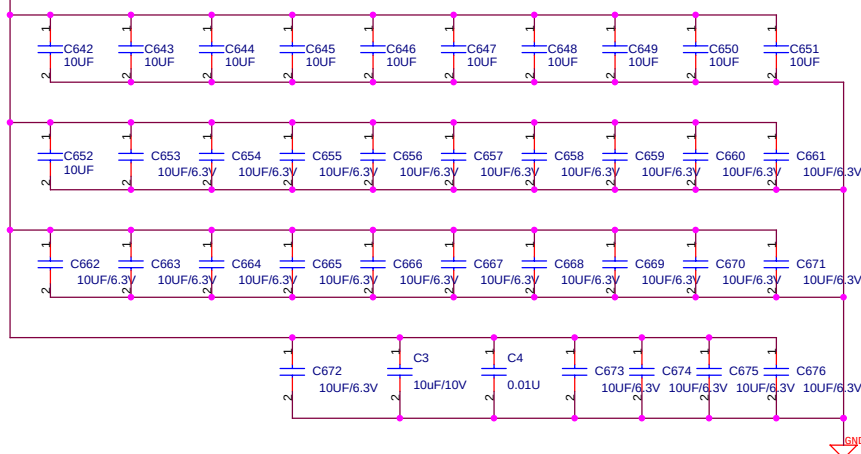
Place SMBT3904
under DIMM0



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58



CPU Vcore Decoupling Capacitor

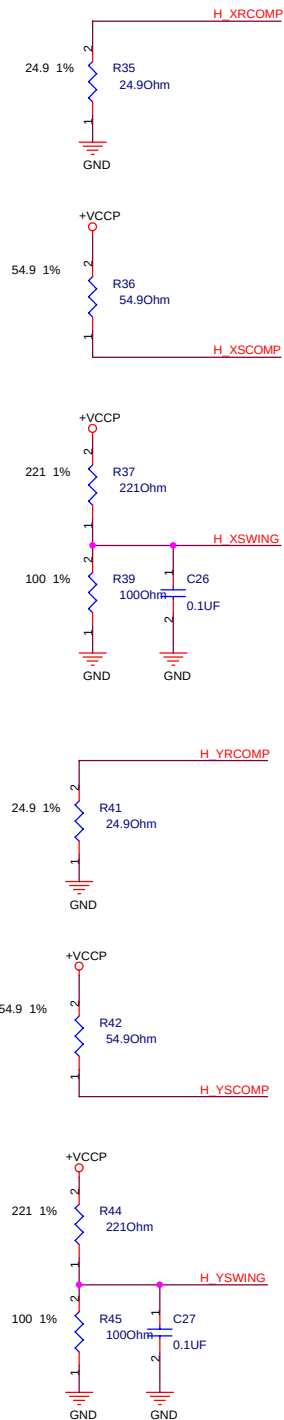


Mid Frequency
Decoupling (Place
around
Processor)

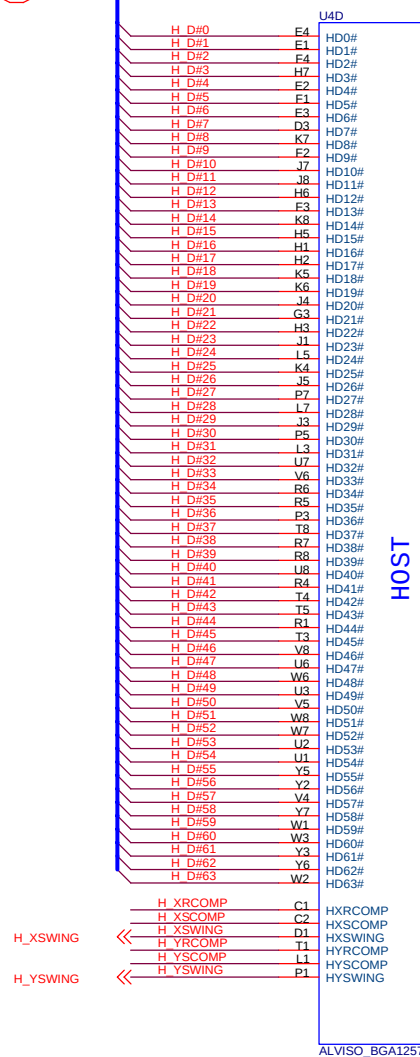
High Frequency
Decoupling (Place
underneath
Processor) using
10uF/6.3V X5R

+Vcore
Bulk
Decoupling

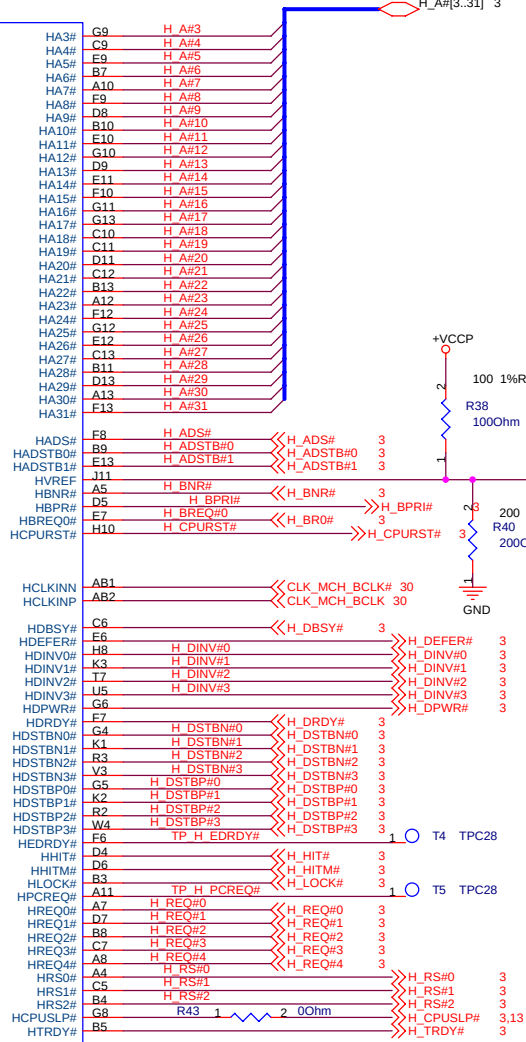
Four 200 uF are
located in
IMVP4



3 H_D#[0..63]

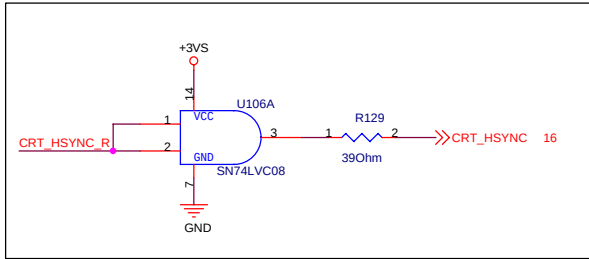


HOST

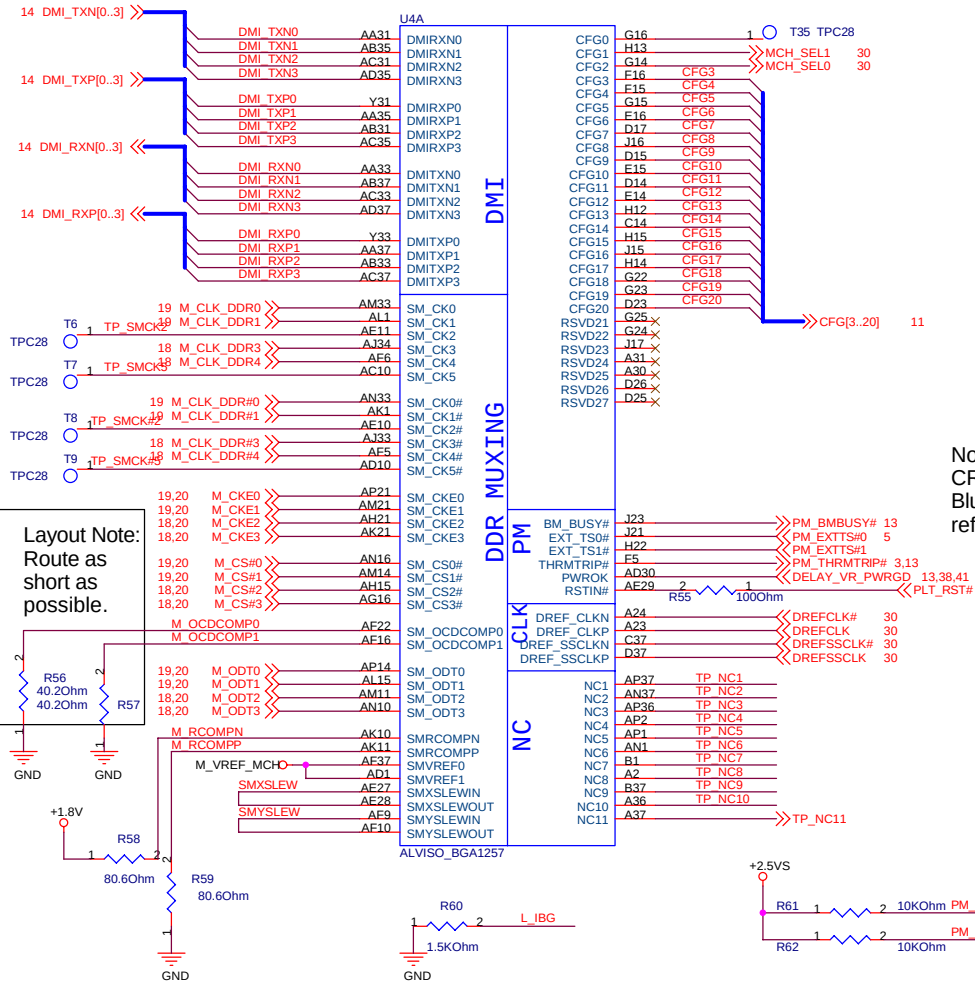
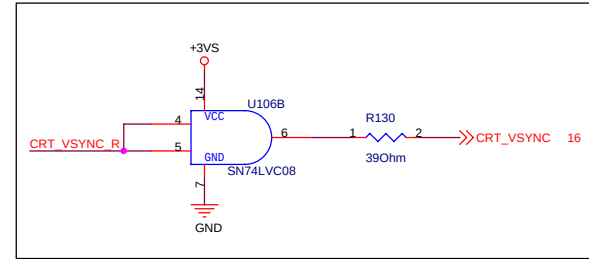


R43 NO STUFF

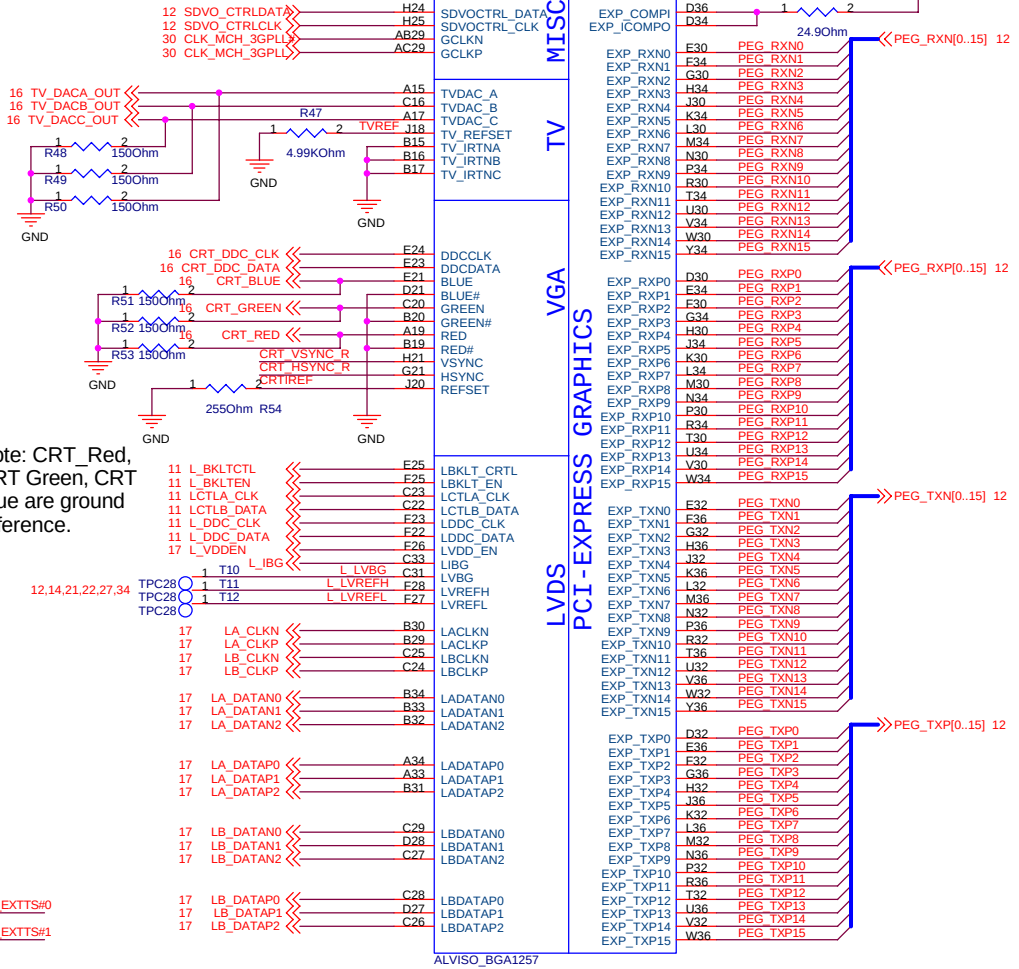
74LVC08 CLOSE to ALVISO



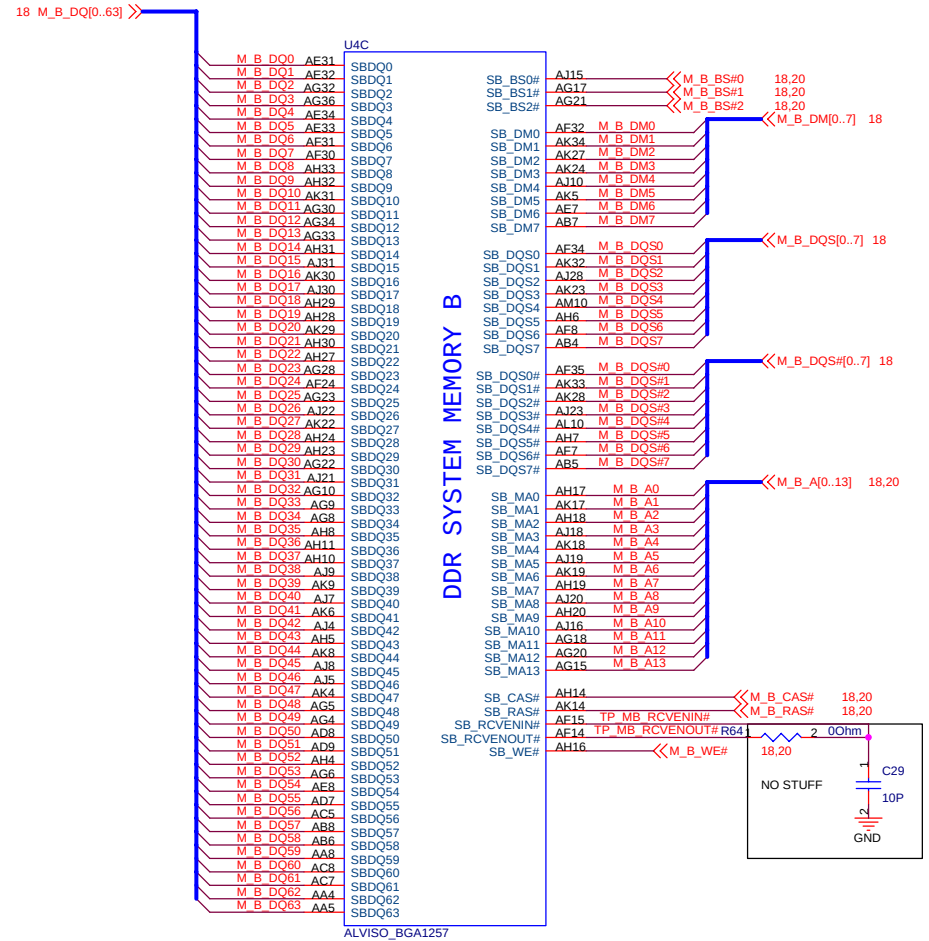
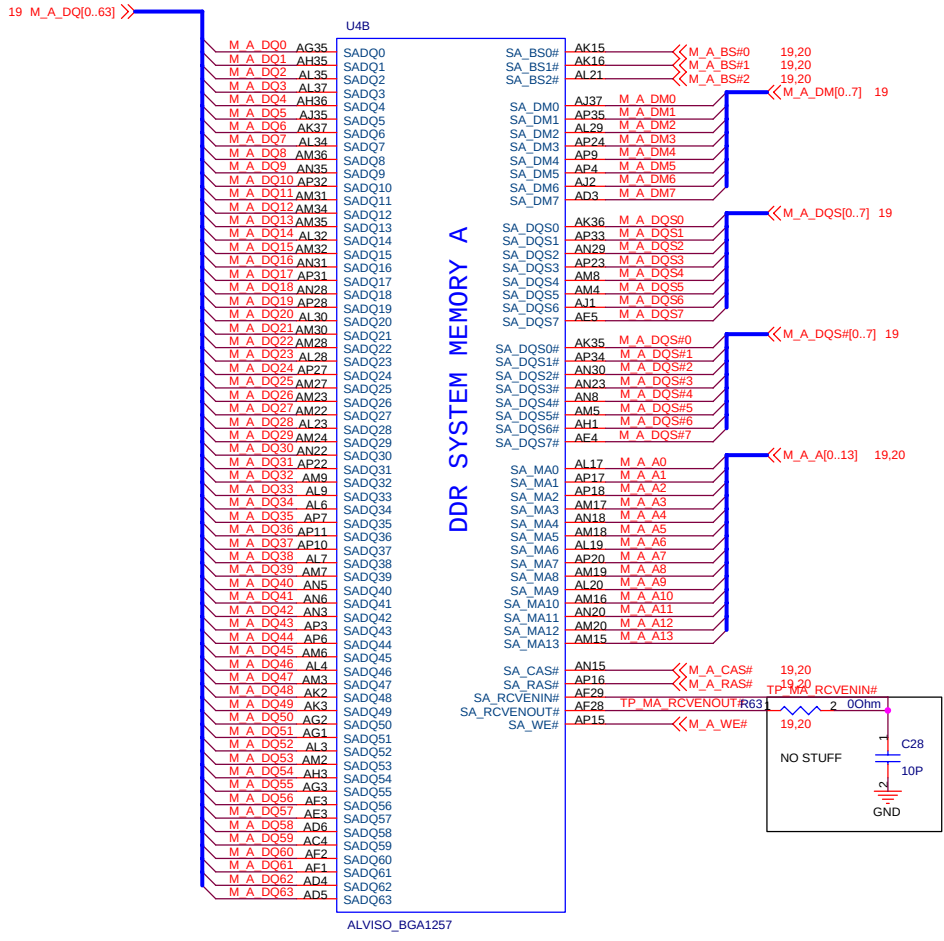
74LVC08 CLOSE to ALVISO

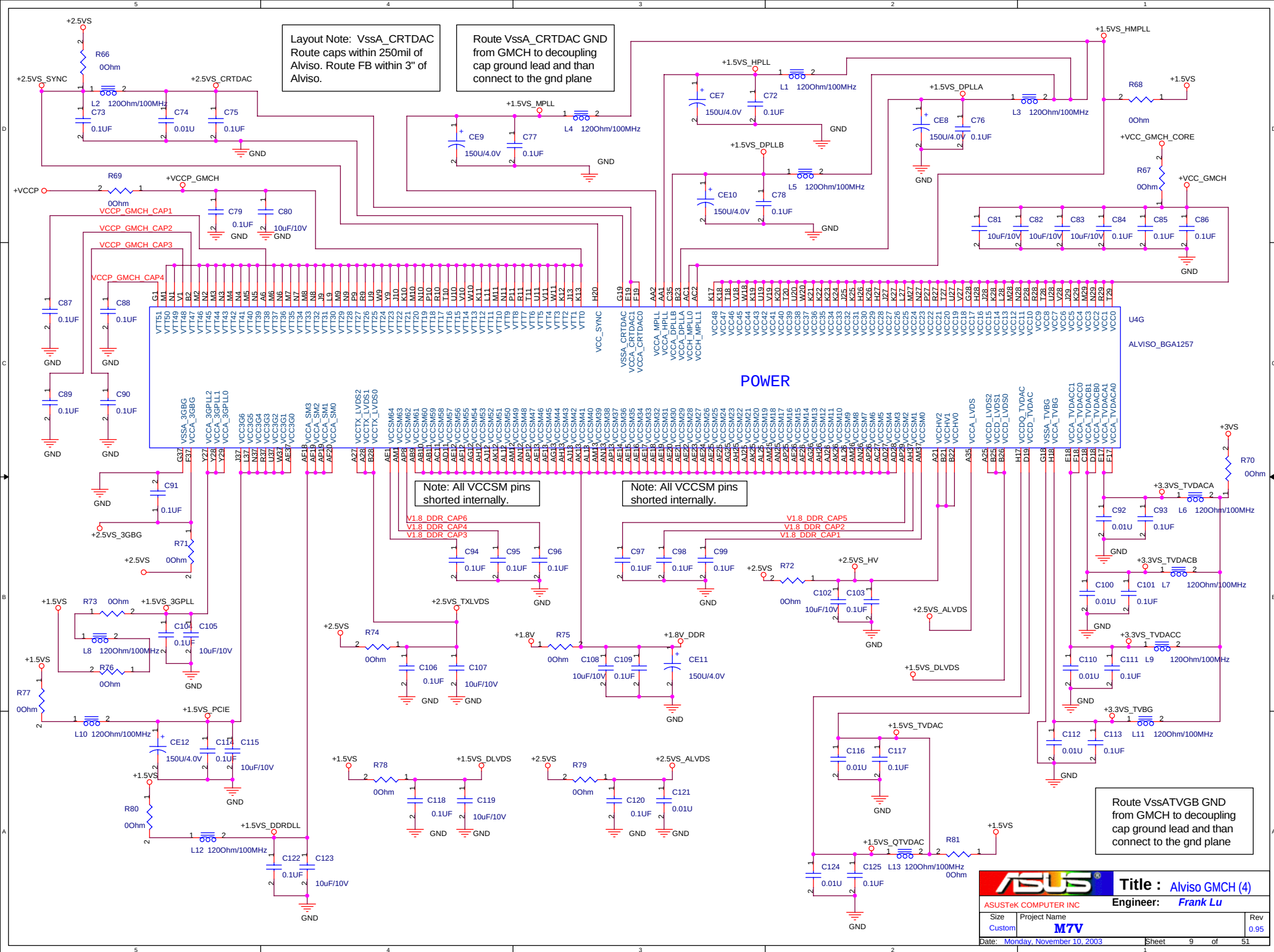


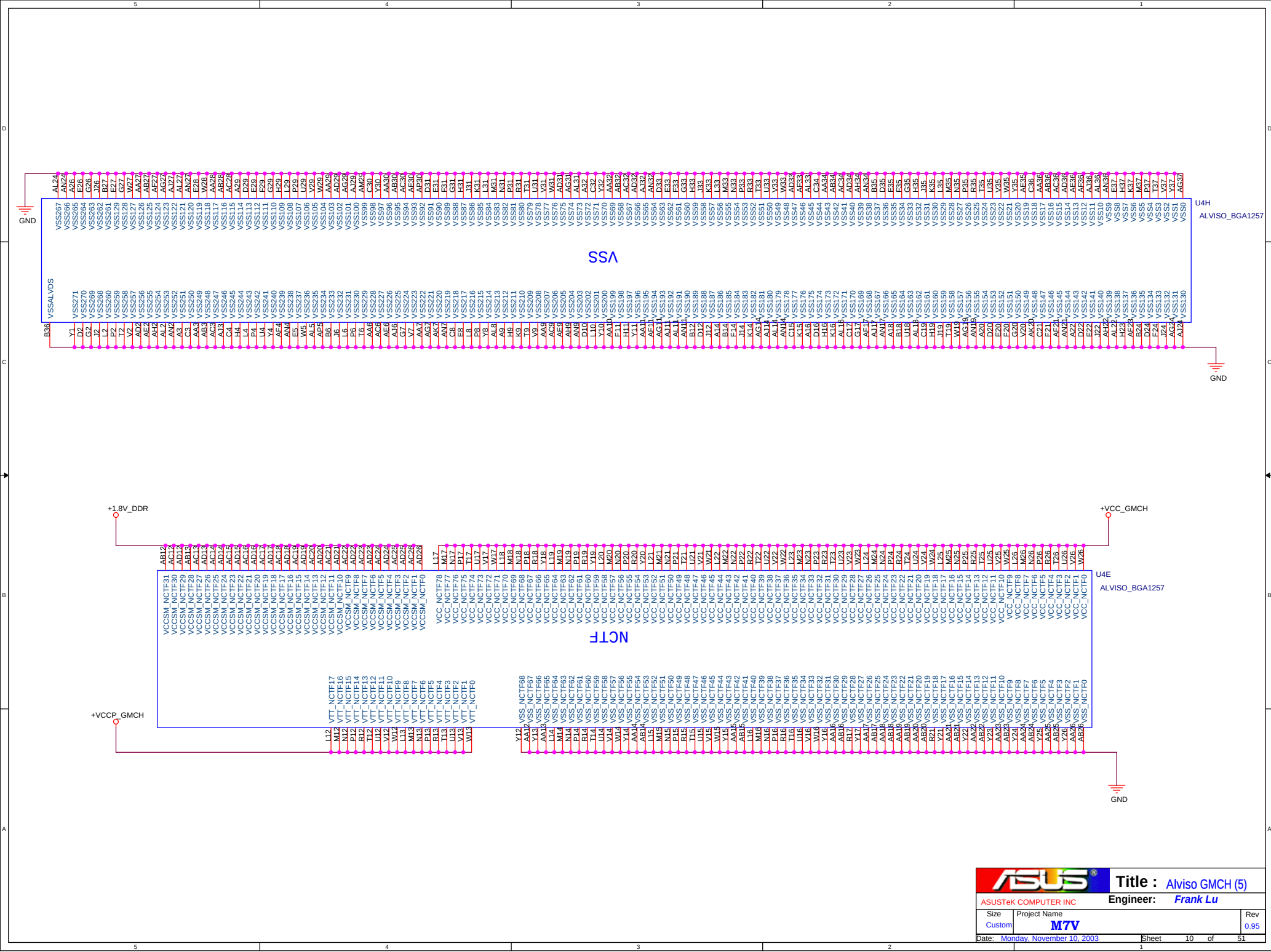
Note: CRT_Red, CRT Green, CRT Blue are ground reference.



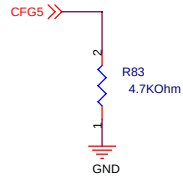
Layout Note:
Route as
short as
possible.



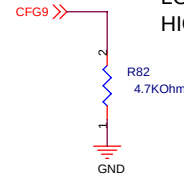




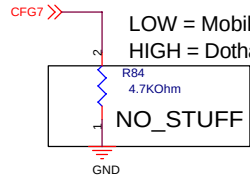
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



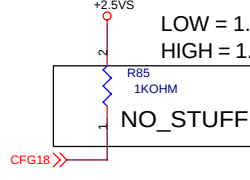
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



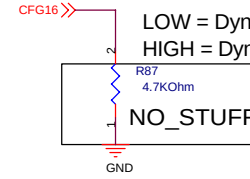
CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



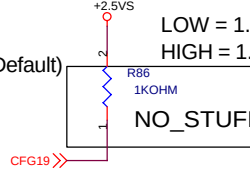
CFG18 : VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



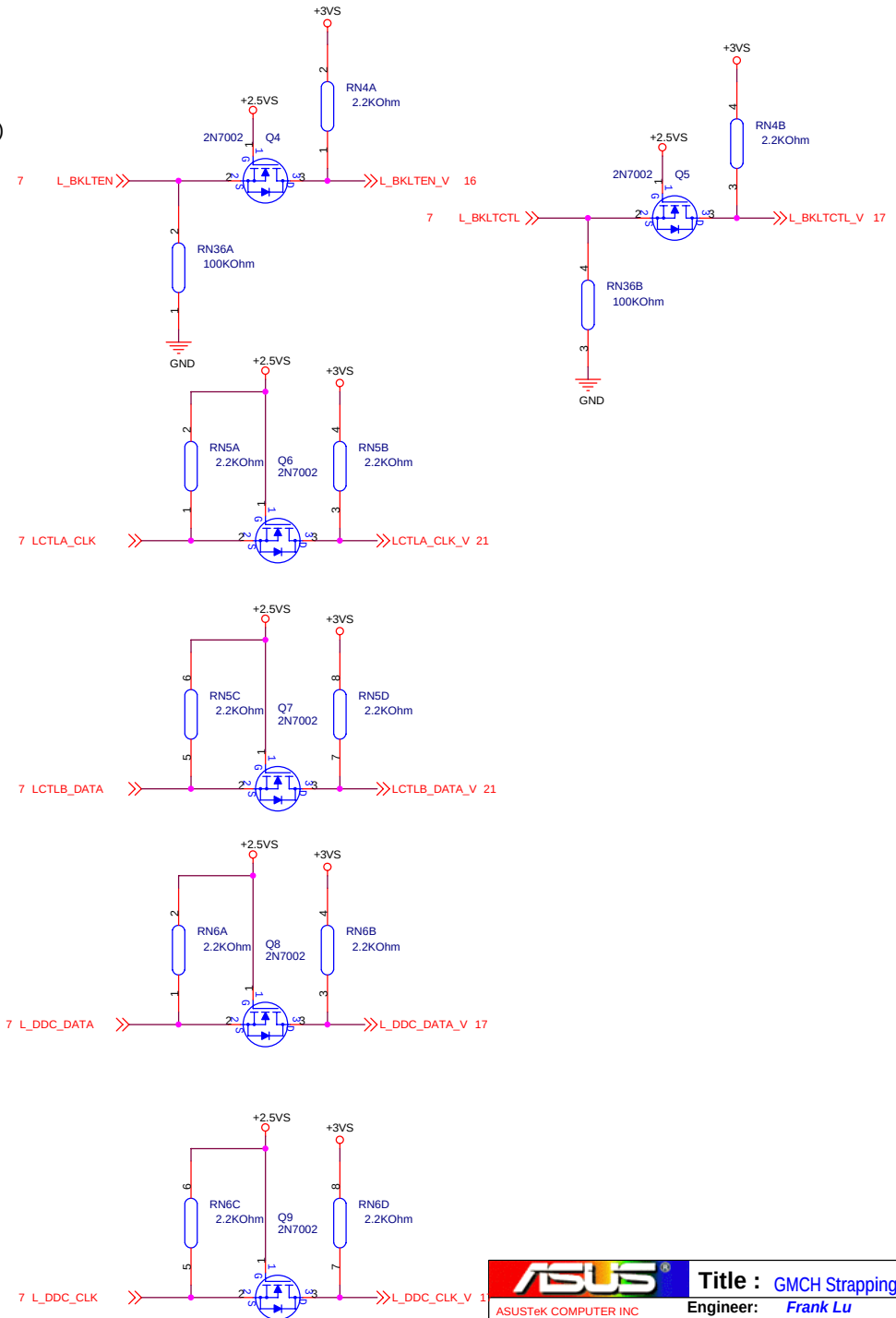
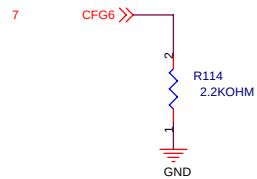
CFG19 : VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V



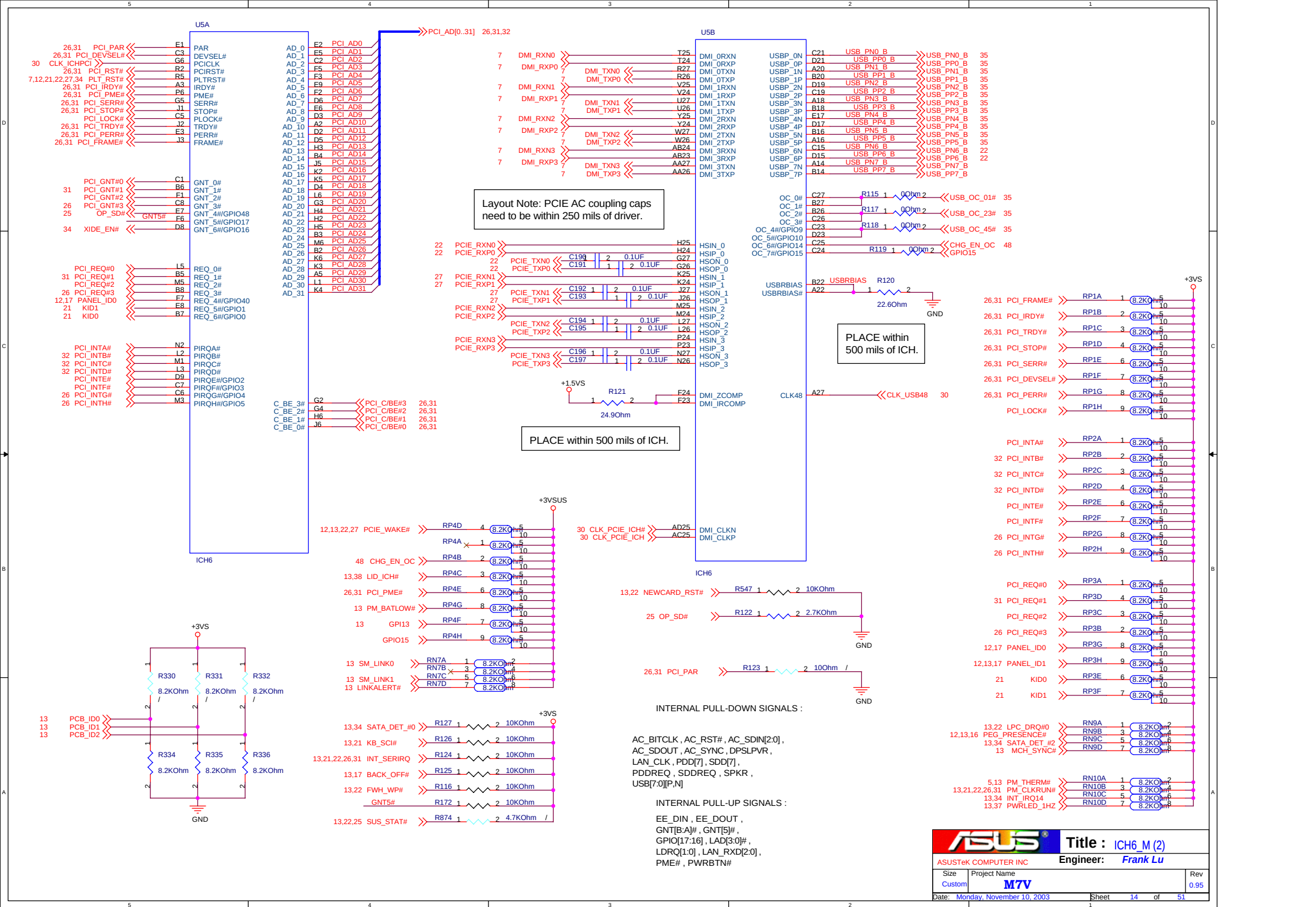
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.

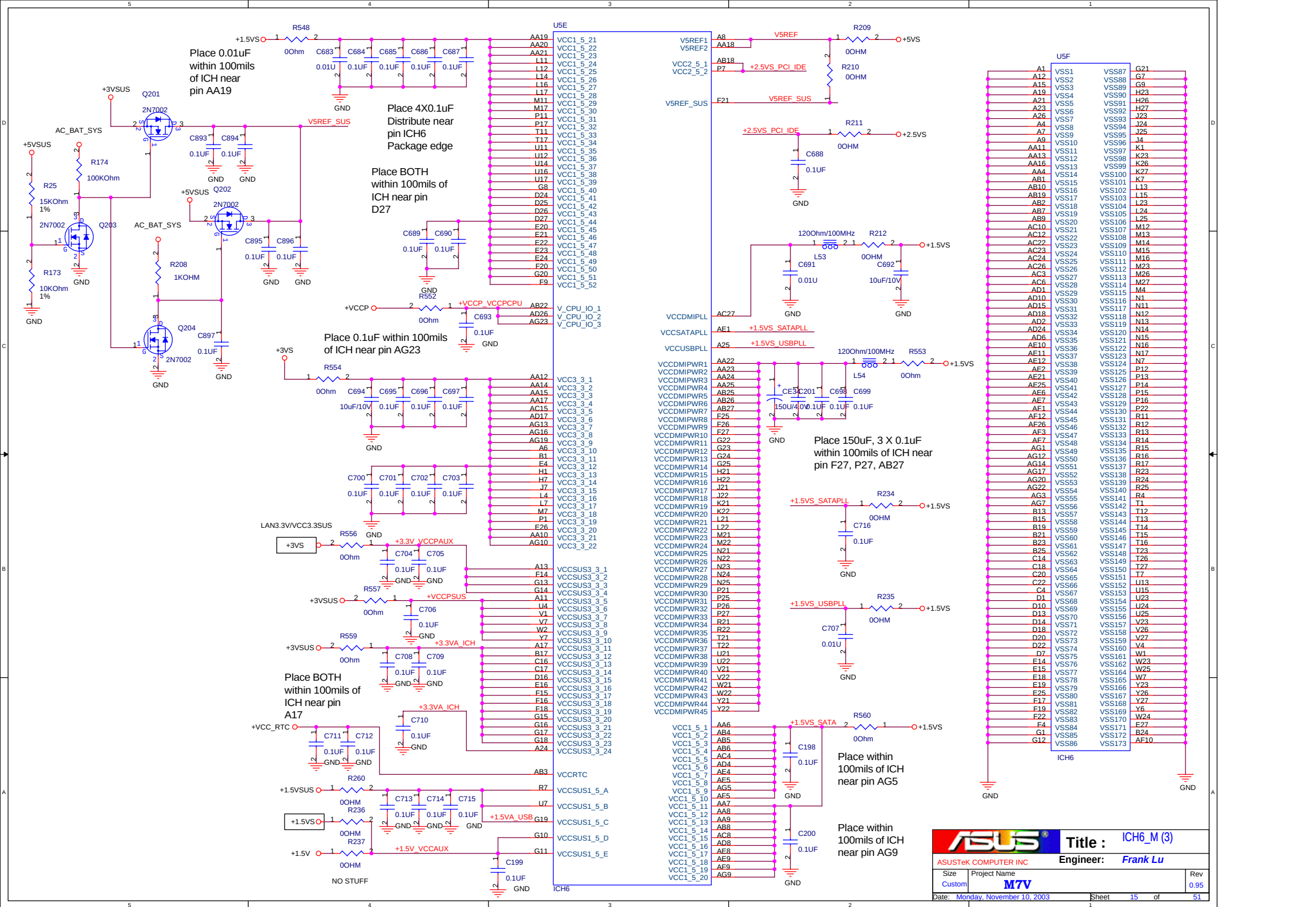
SDVOCRTL_DATA LOW = No SDVO device present (Default)

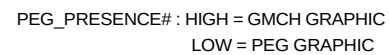
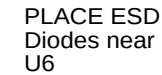
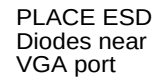
CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)









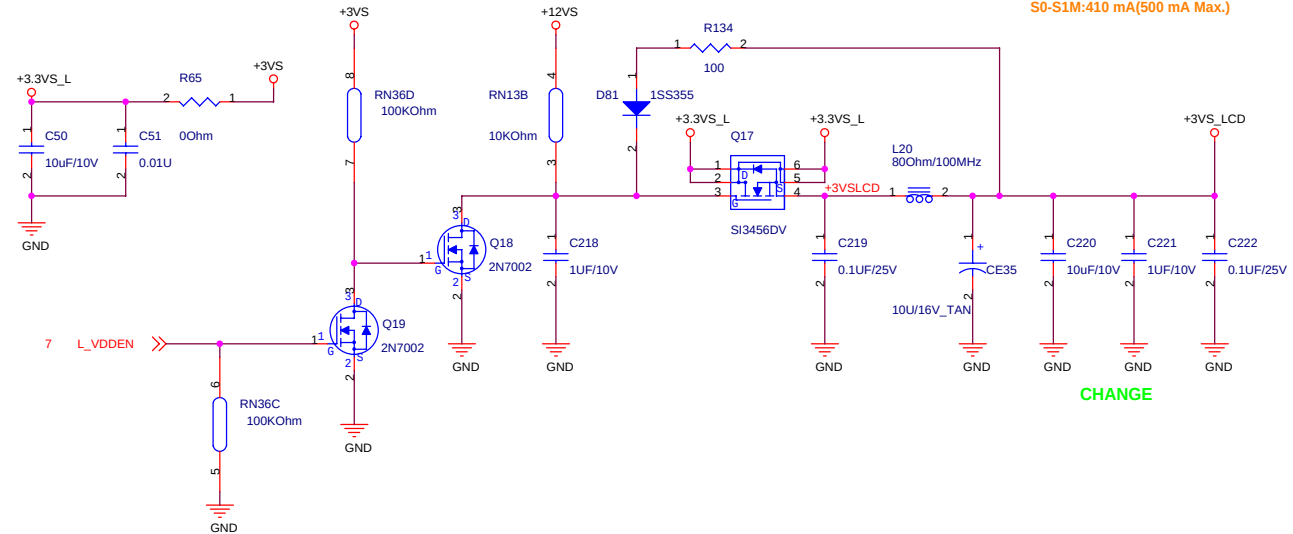


LCD Power

SI3865: US\$0.22

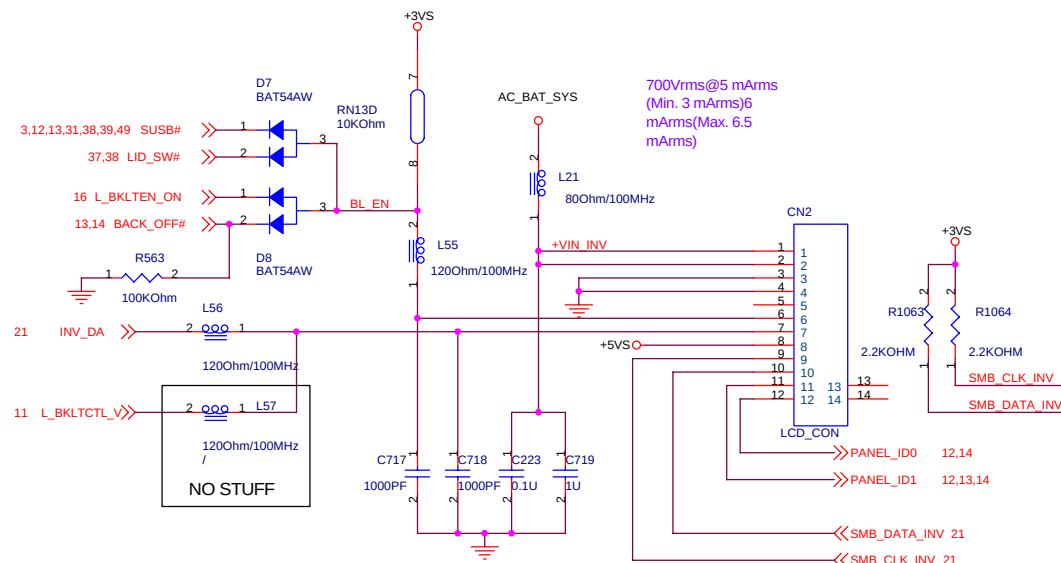
3-3.6V
S0-S1M:410 mA(500 mA Max.)

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800
PANEL ID0 RESERVE FOR VENDOR



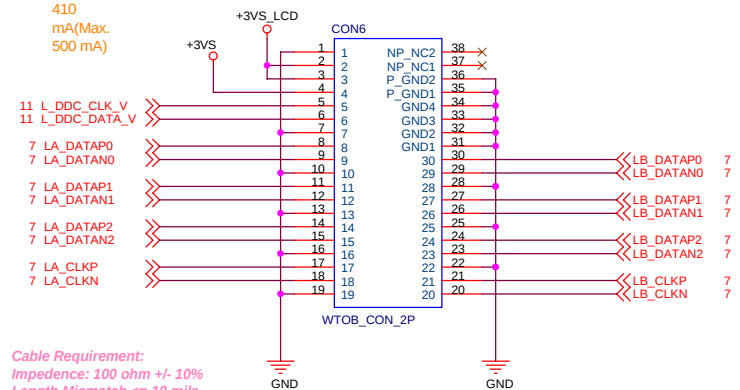
LCD Backlight Control

700Vrms@5 mArms
(Min. 3 mArms)6
mArms(Max. 6.5
mArms)



LCD LVDS Interface

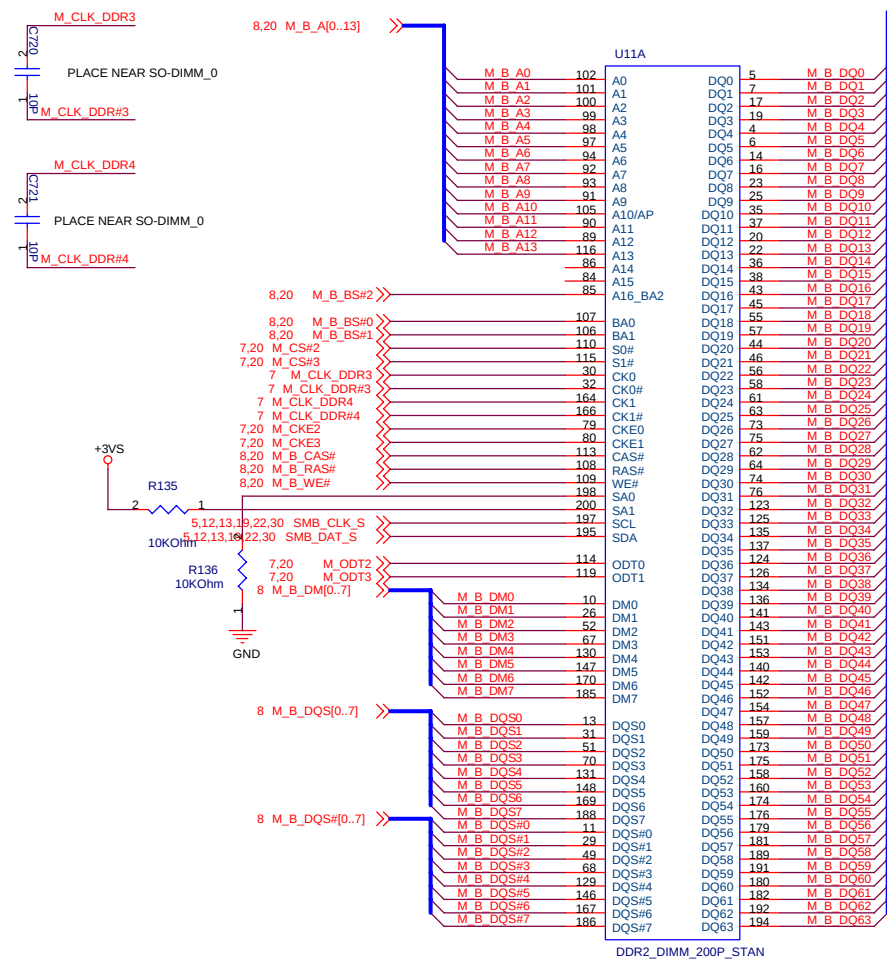
3V-3.6V
Full
Active:
410
mA(Max.
500 mA)



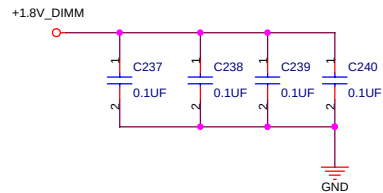
Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

ASL (SMB addr : 0x72)
(Ambient Light Sensor)

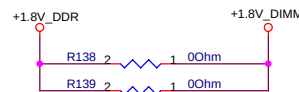
ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Frank Lu	
Size	Project Name	Rev	
Custom	M7V	0.95	
Date: Monday, November 10, 2003	Sheet	17	of 51



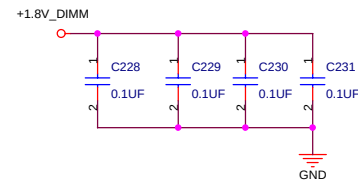
Layout Note: Place these High-Freq decoupling Caps near the GMCH



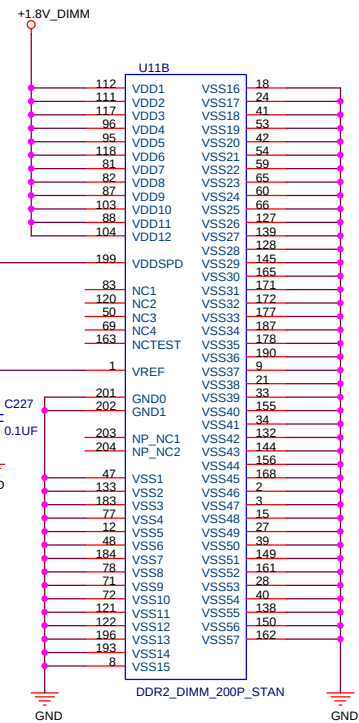
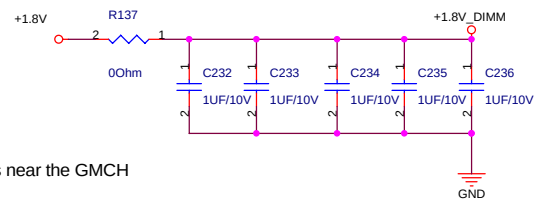
Layout Note: Place these resistors near the GMCH

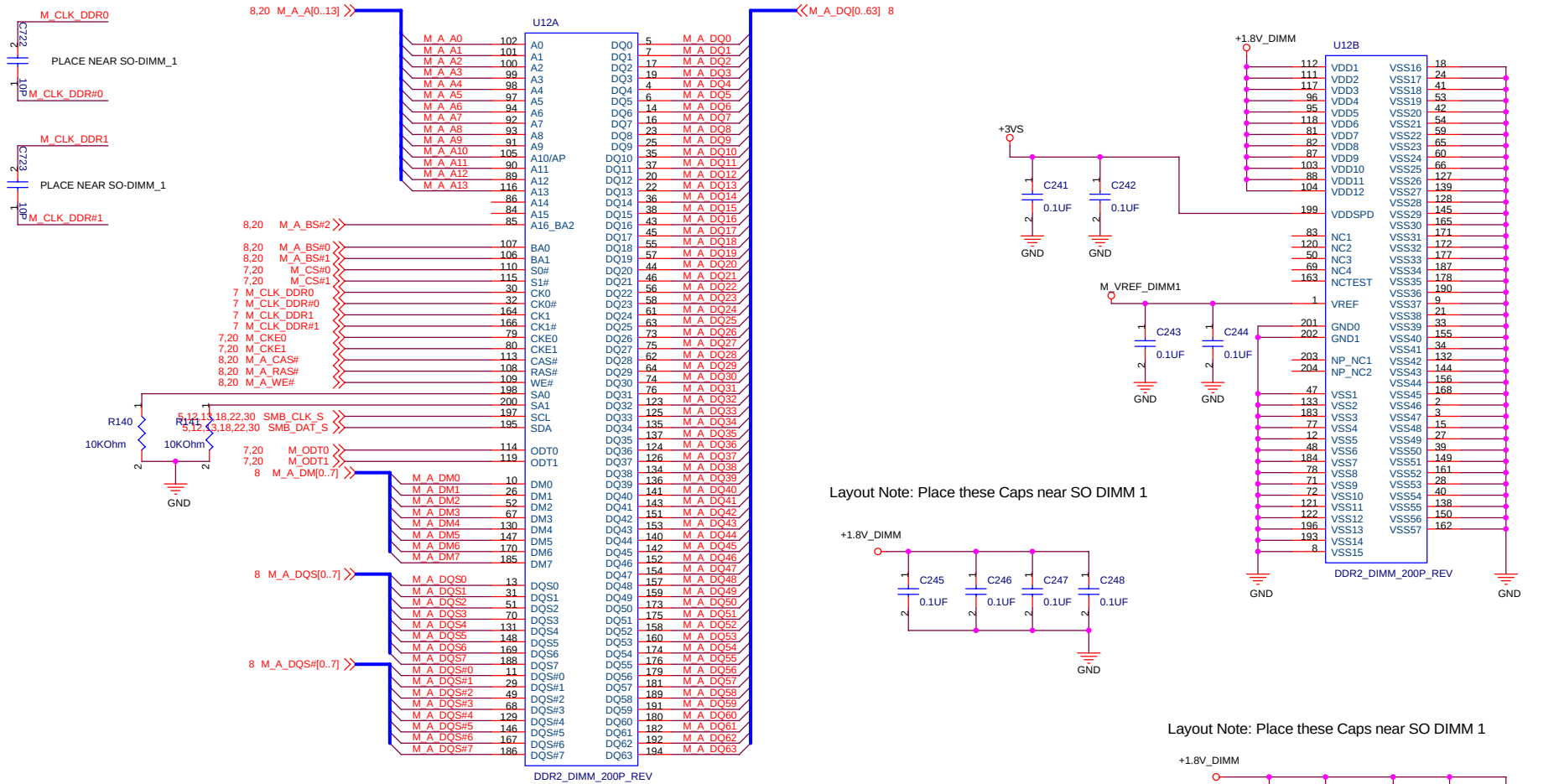


Layout Note: Place these Caps near SO DIMM 0

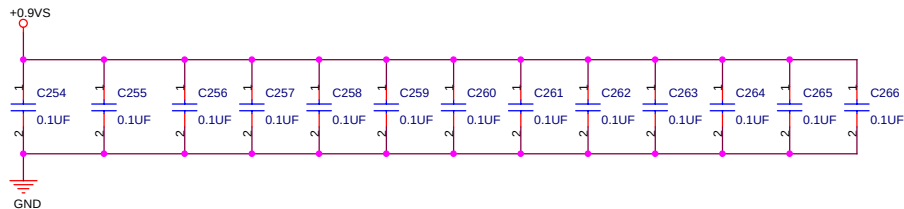
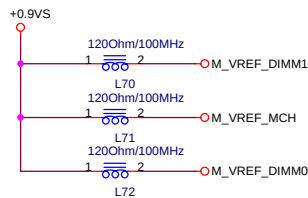


Layout Note: Place these Caps near SO DIMM 0

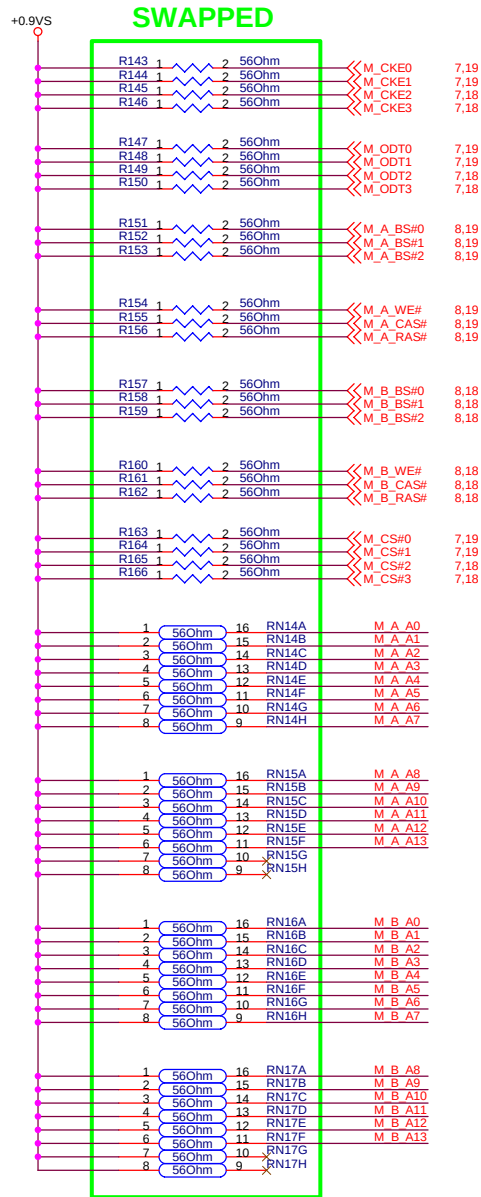
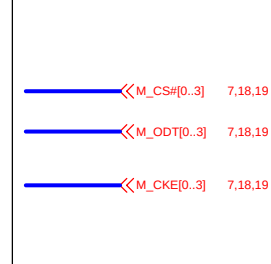
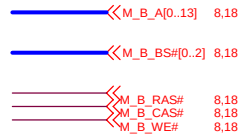
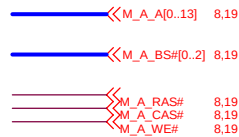
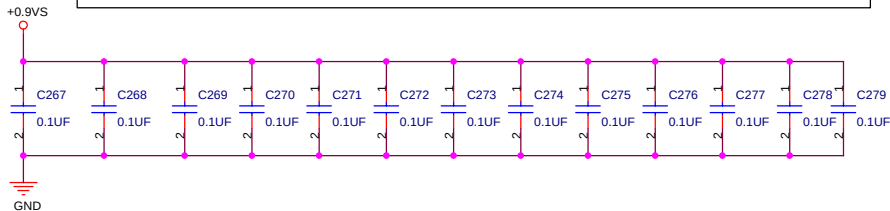


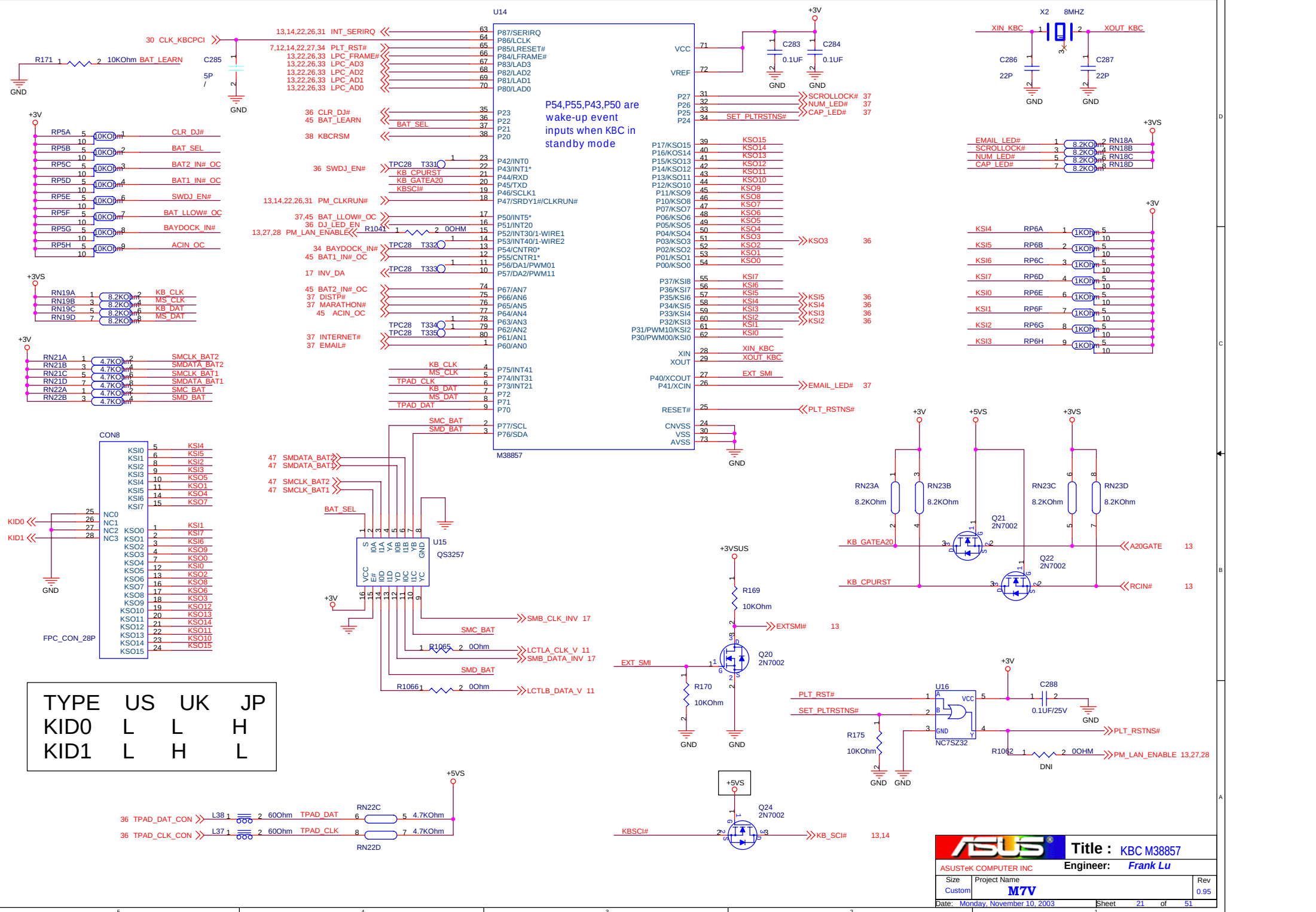


SO-DIMM 1 is placed father from
the GMCH than SO-DIMM 0

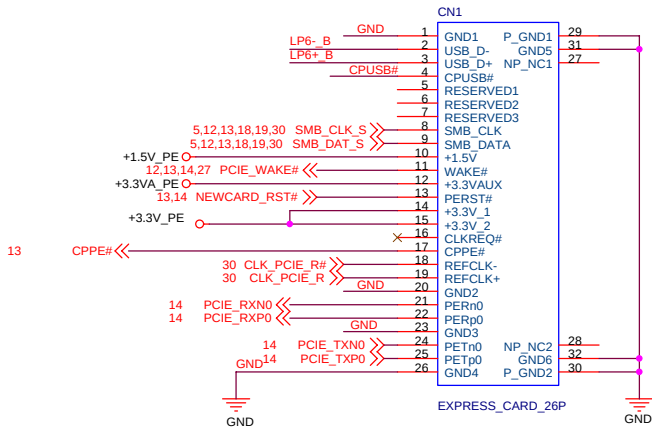


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

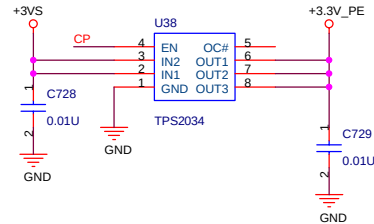
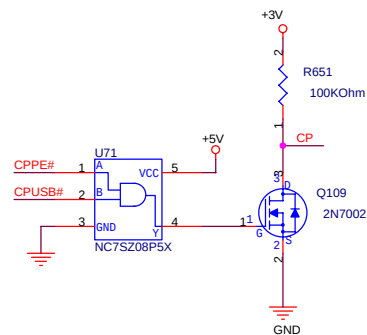
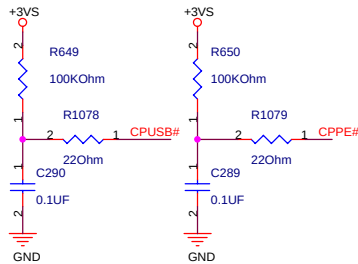
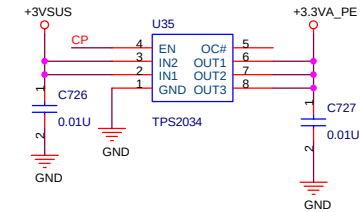
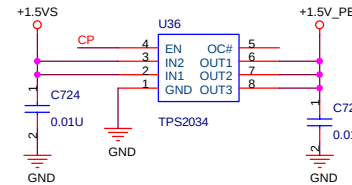
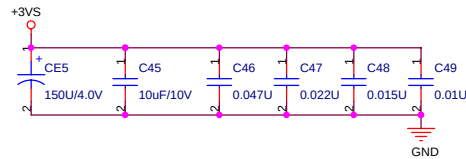
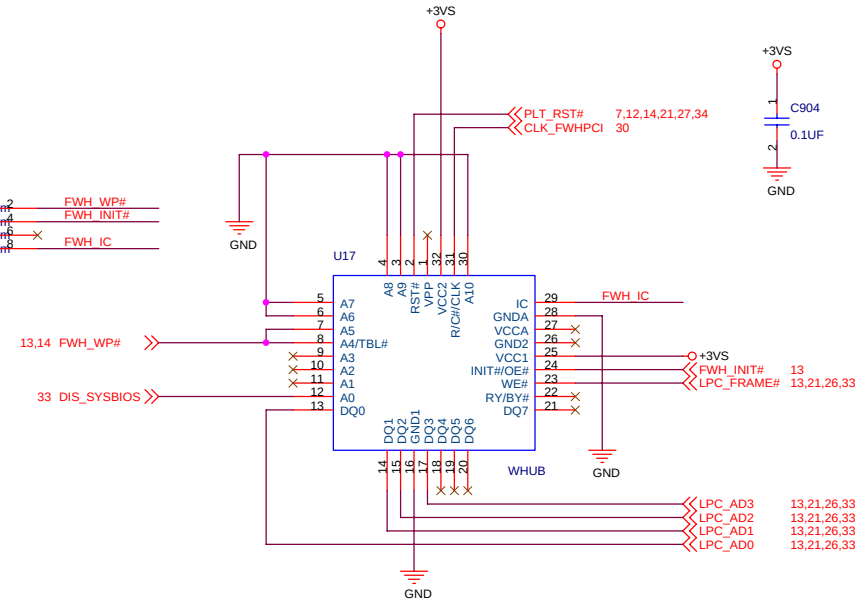




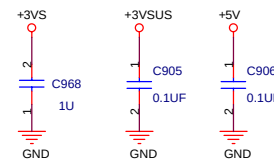
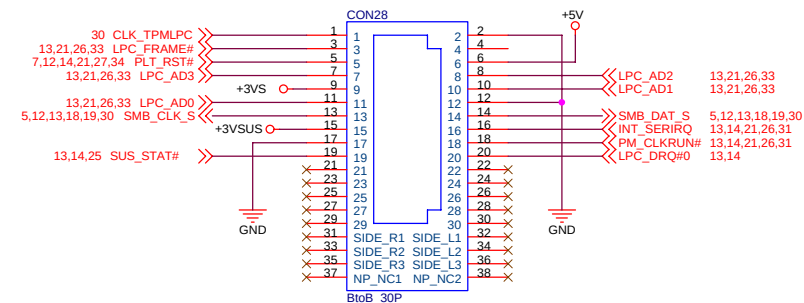
TYPE	US	UK	JP
KID0	L	L	H
KID1	L	H	L

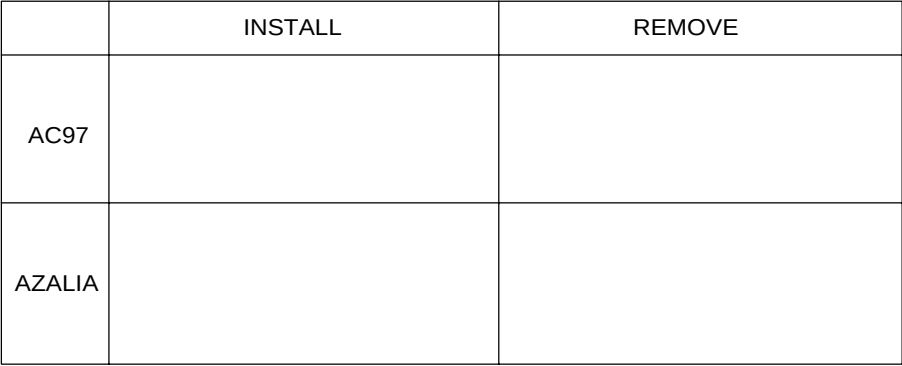


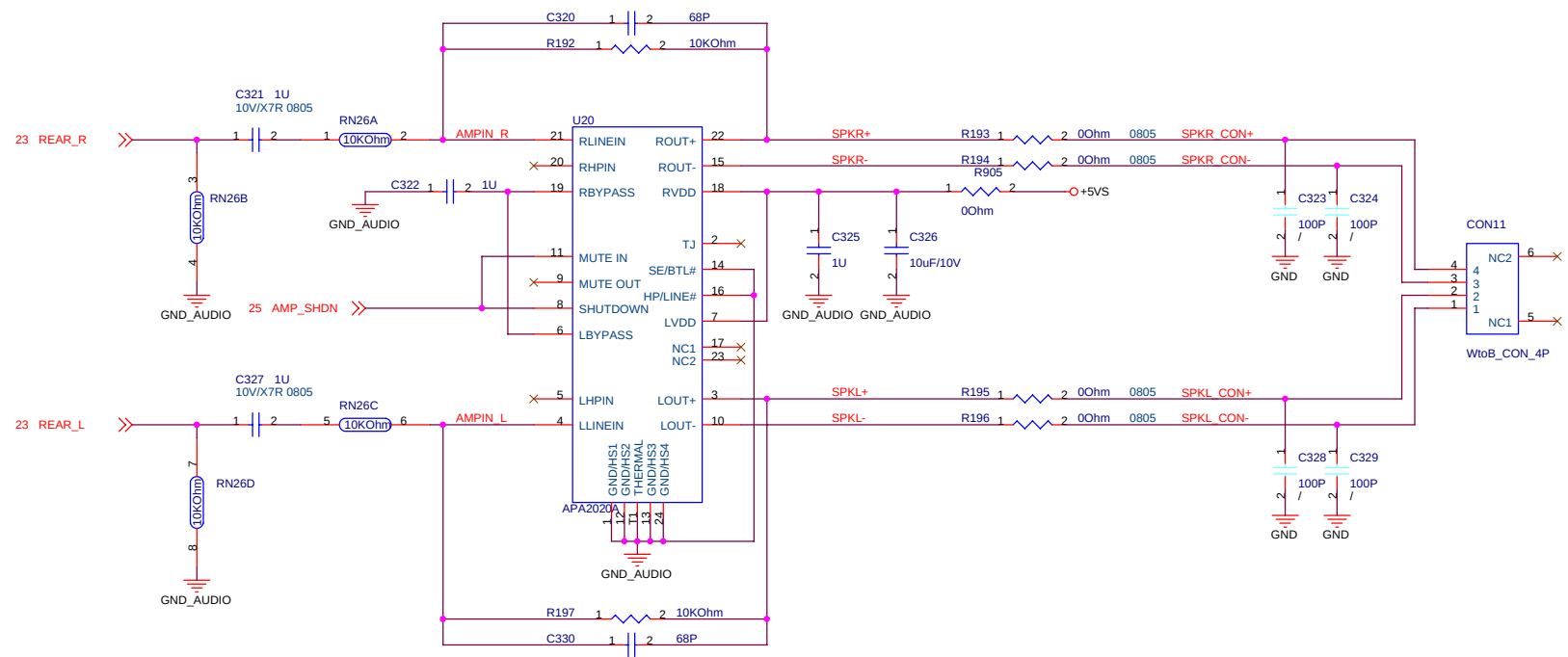
FOLLOW SST FWH SPEC

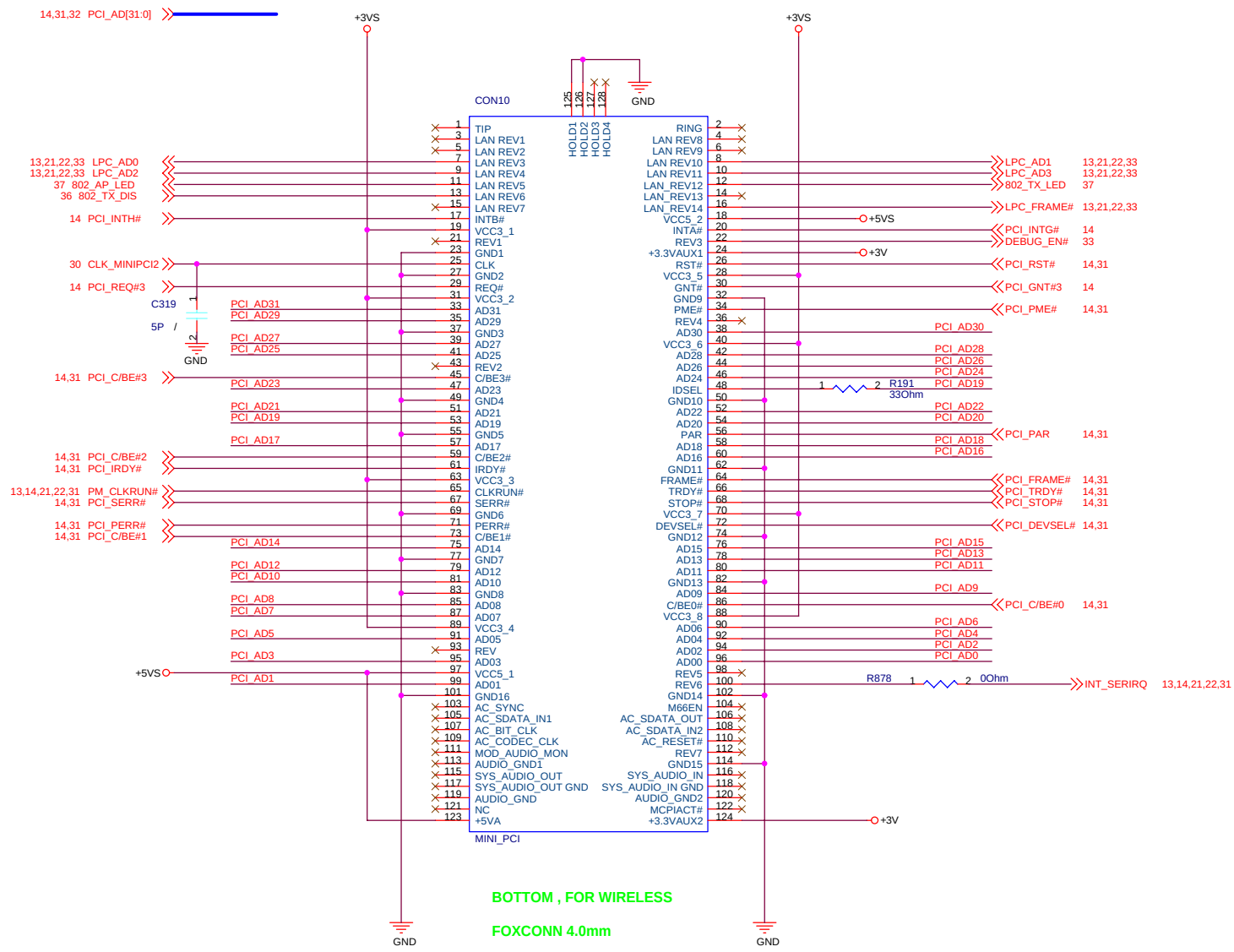


TPM B2B Connector

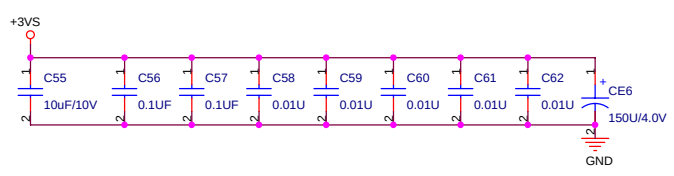


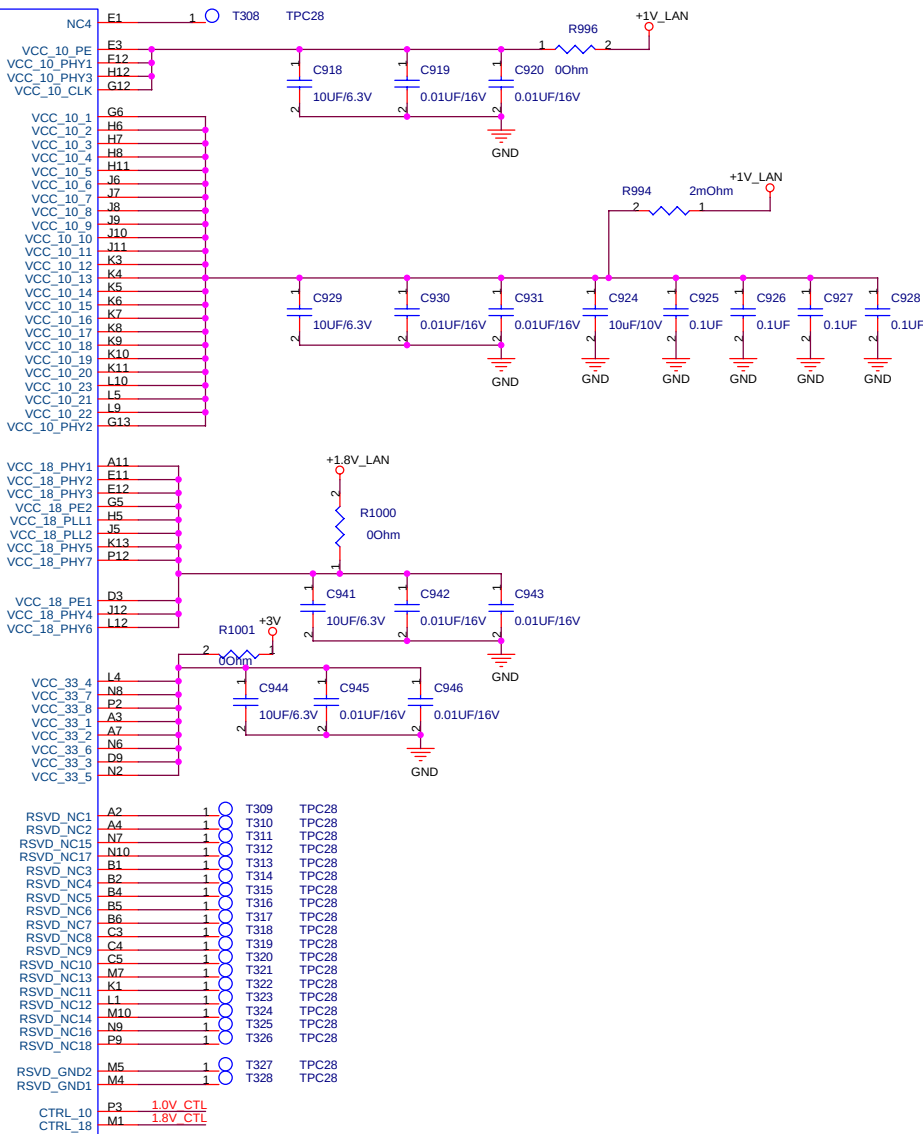
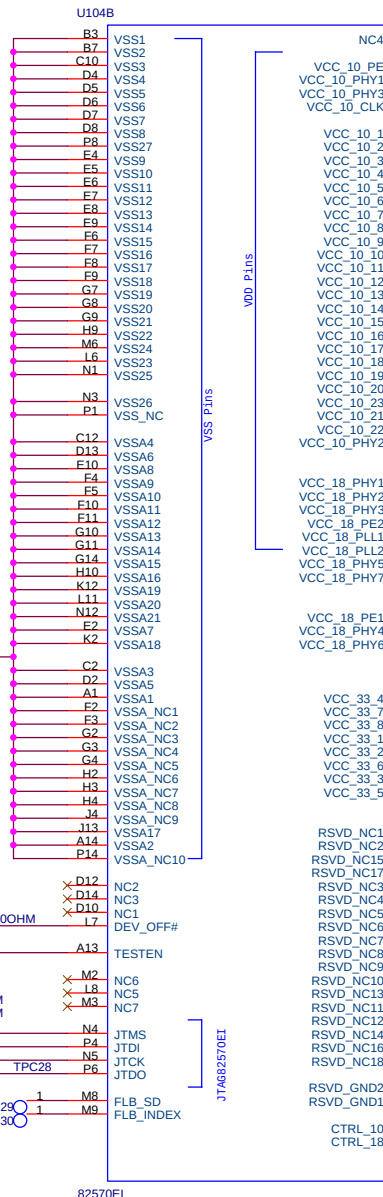
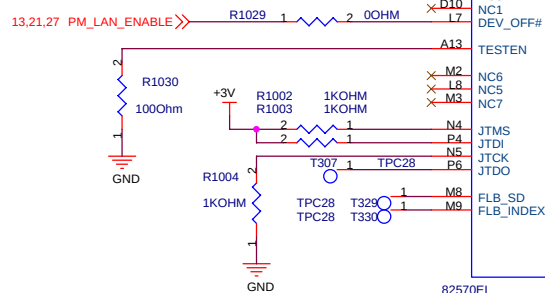
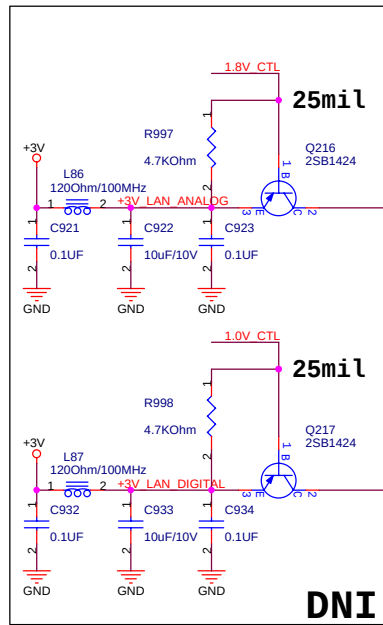




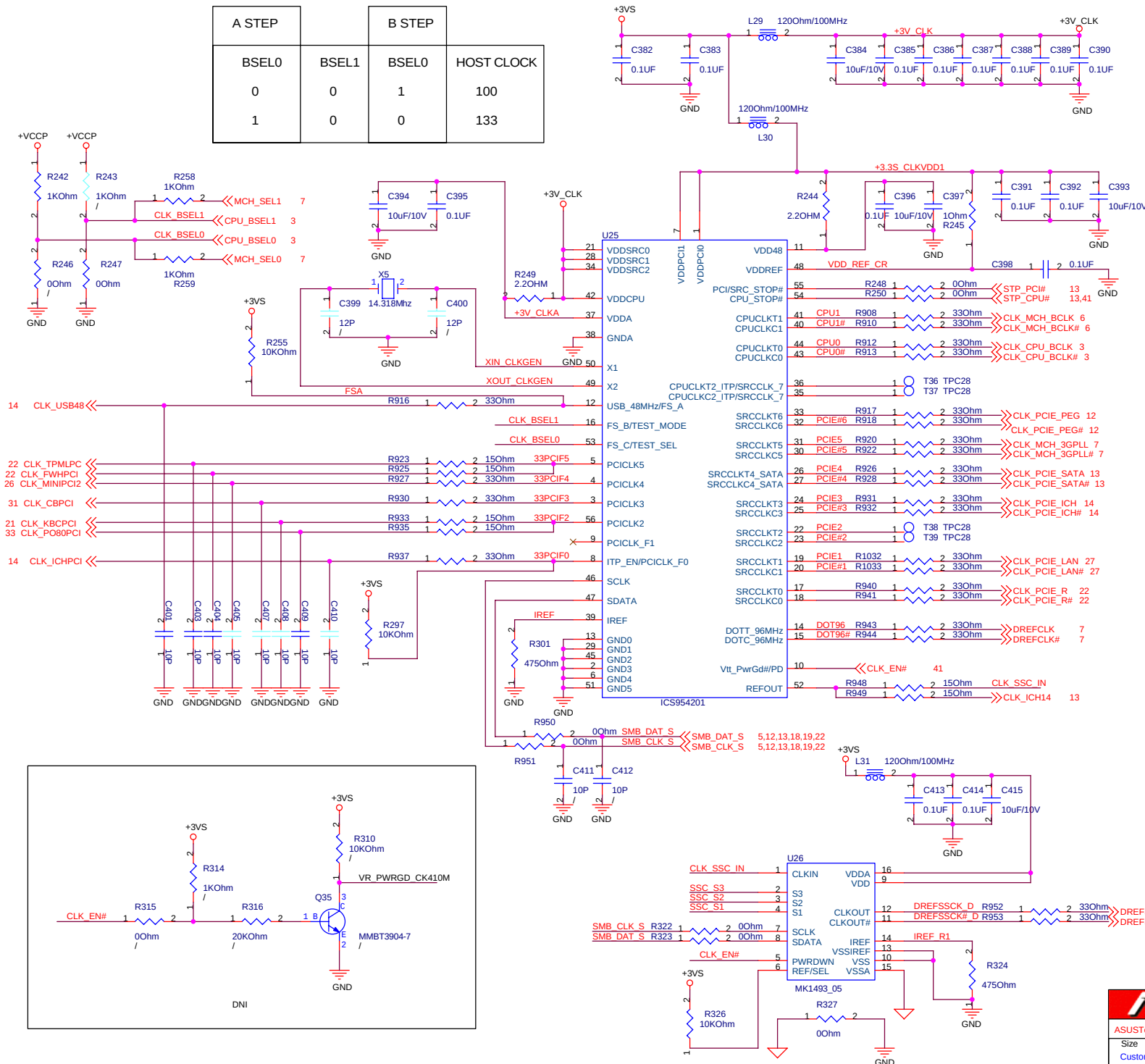


BOTTOM , FOR WIRELESS
FOXCONN 4.0mm

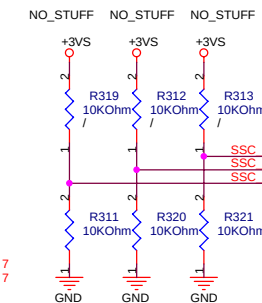
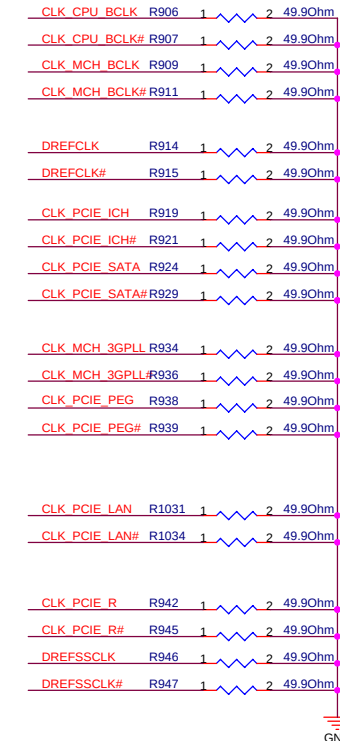


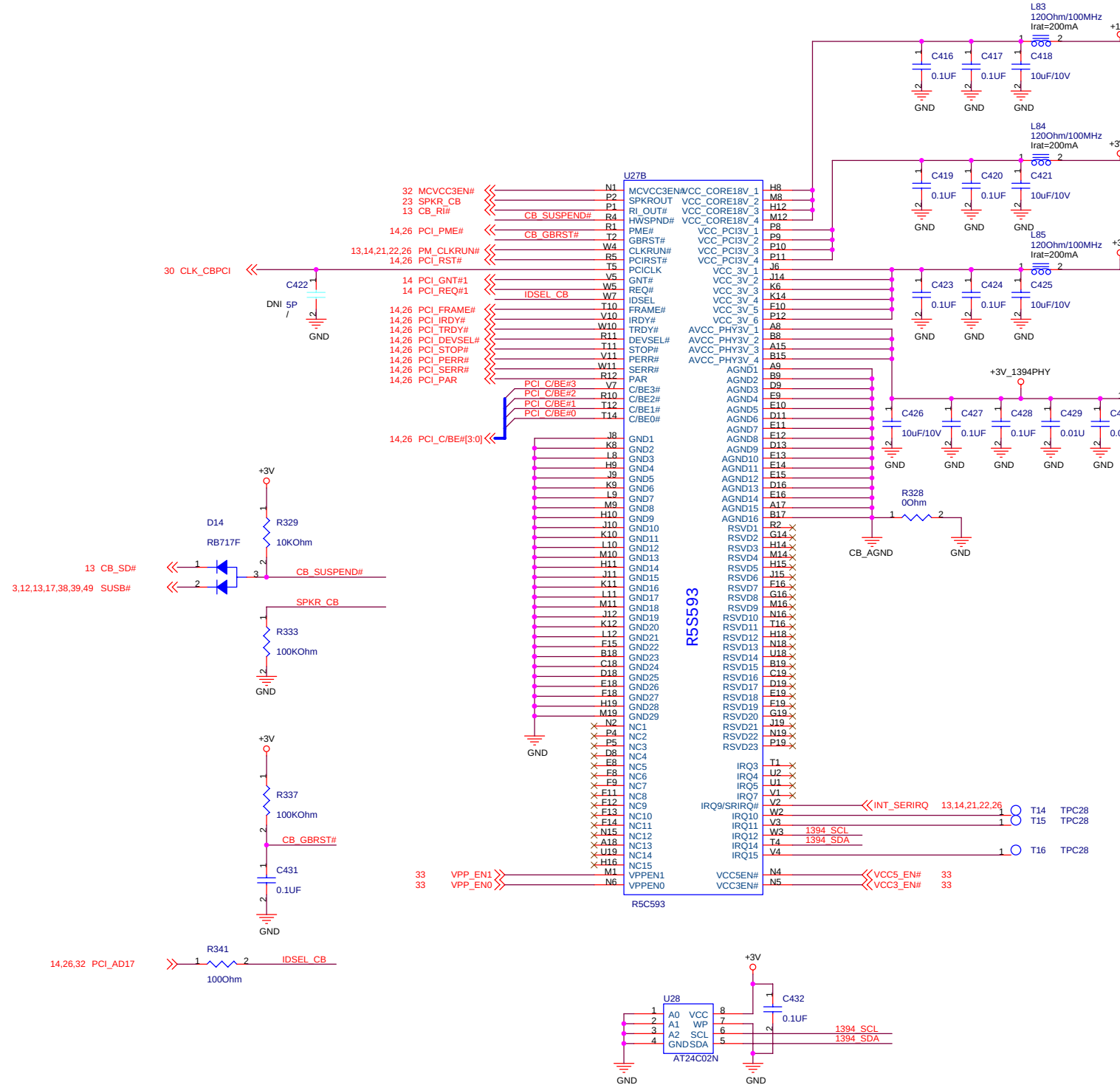


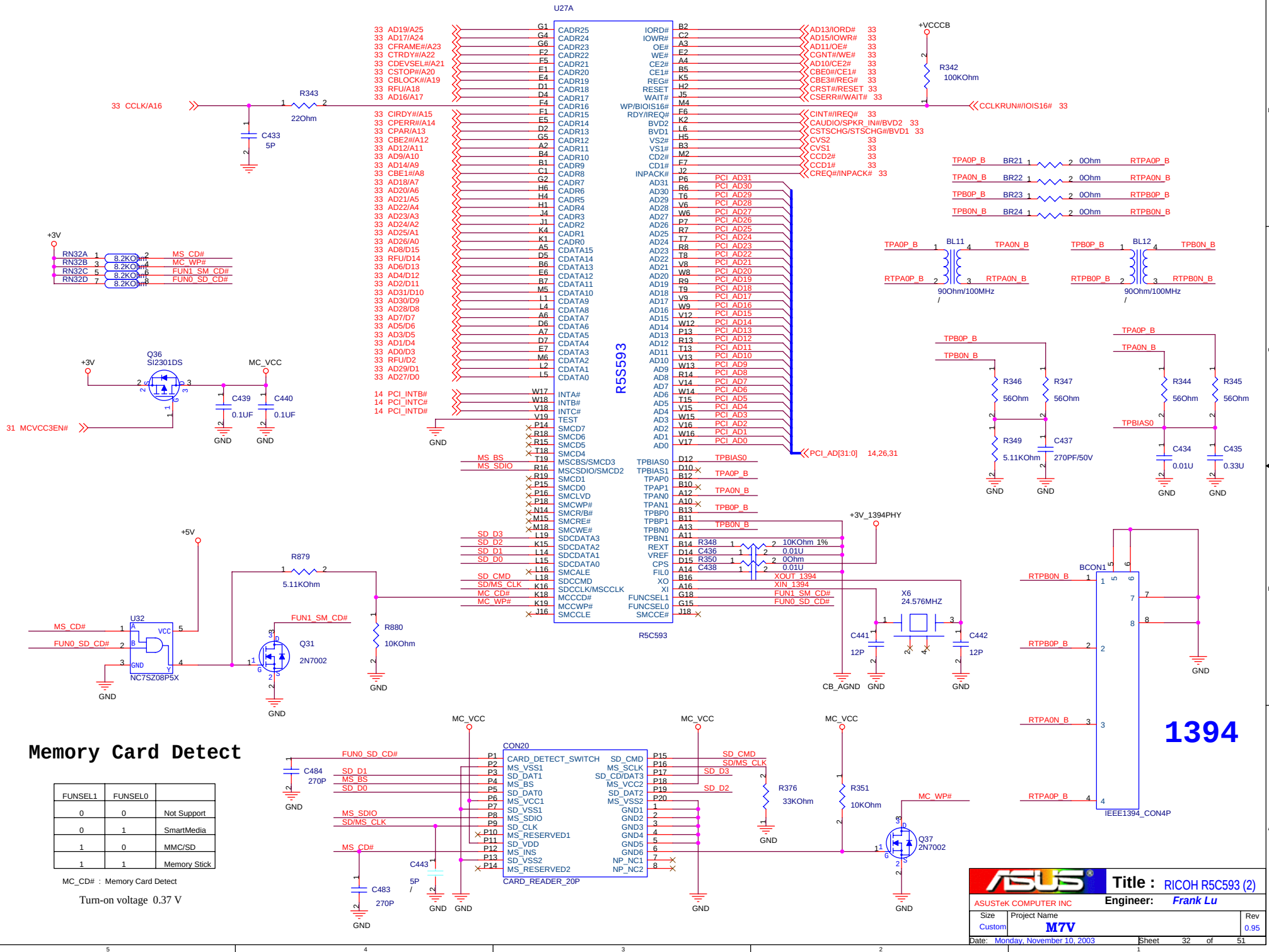
A STEP		B STEP	
BSEL0	BSEL1	BSEL0	HOST CLOCK
0	0	1	100
1	0	0	133

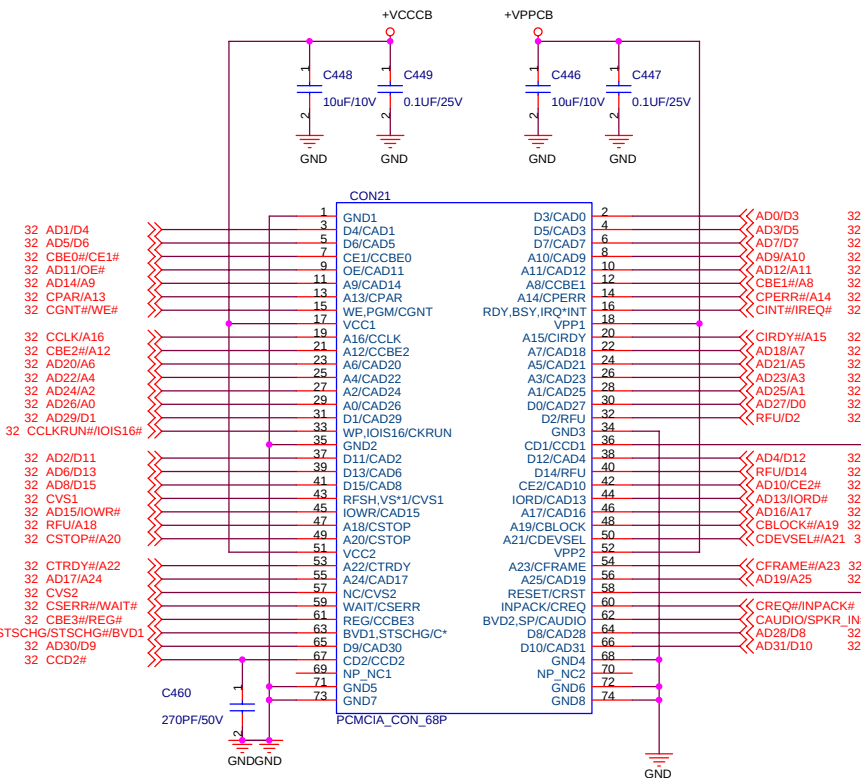
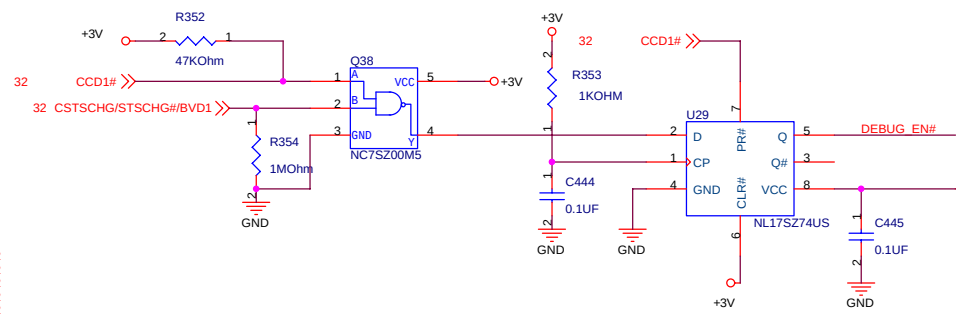
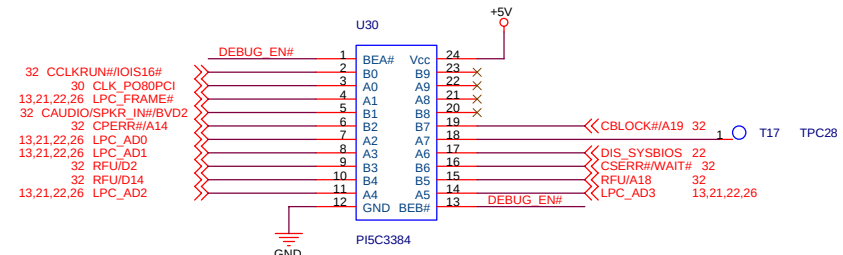
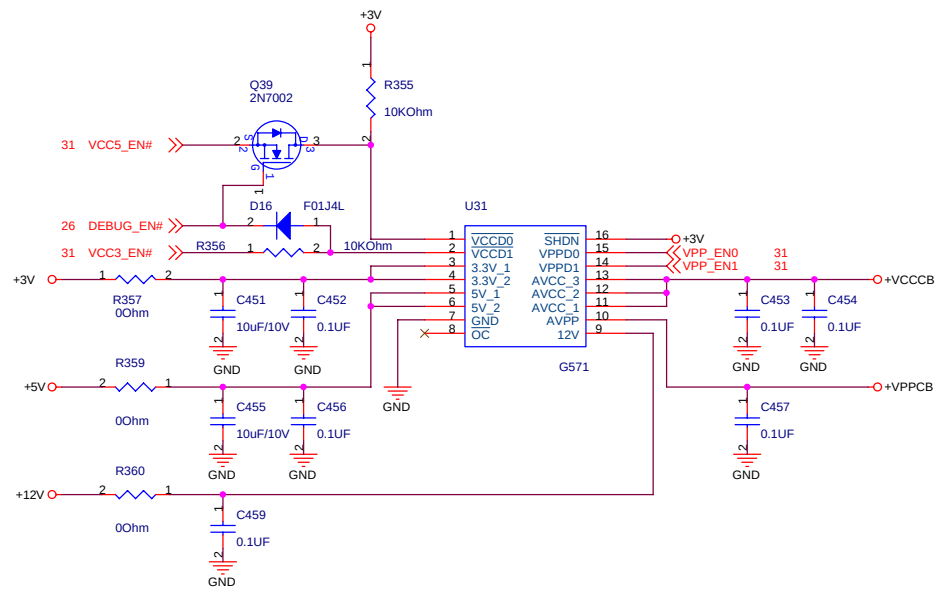


PLACE termination close to source IC

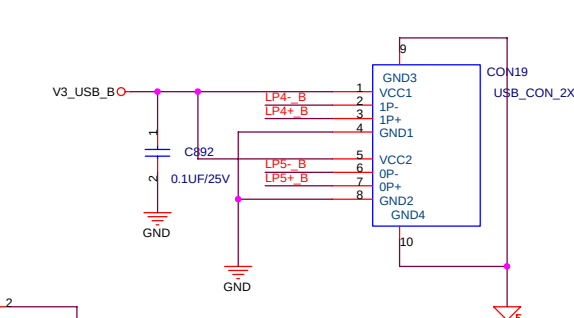
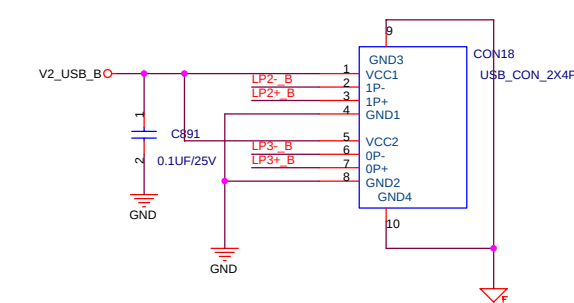
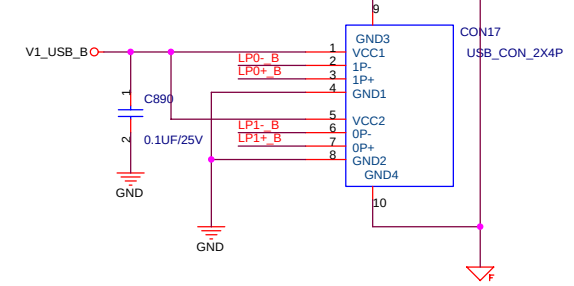
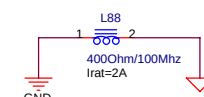
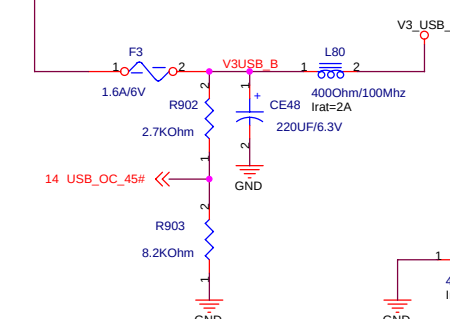
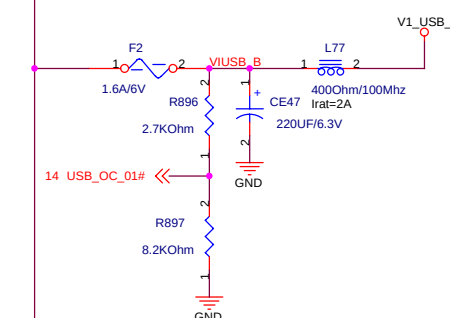
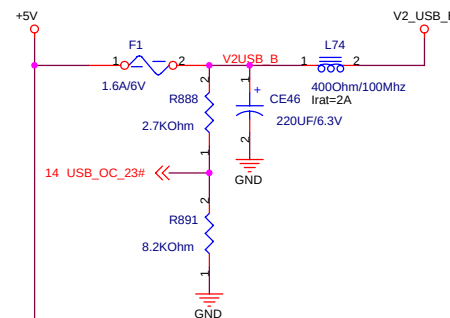




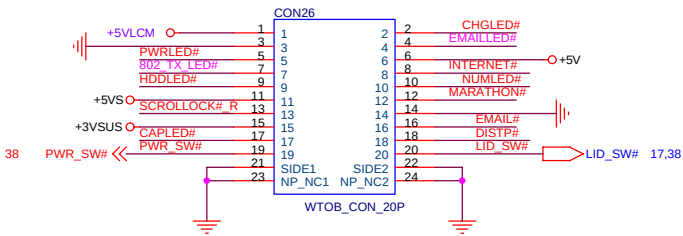




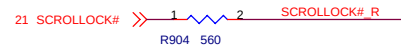
USB



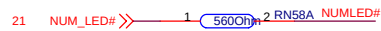
Indicator Connector



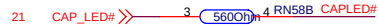
Scrollock LED(GREEN)



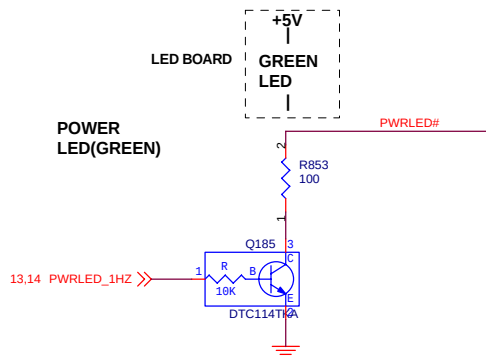
NUM LED(GREEN)



CAP LED(GREEN)

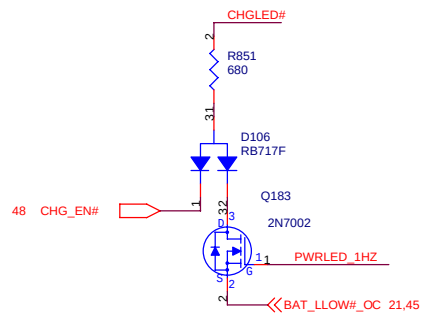


POWER LED(GREEN)

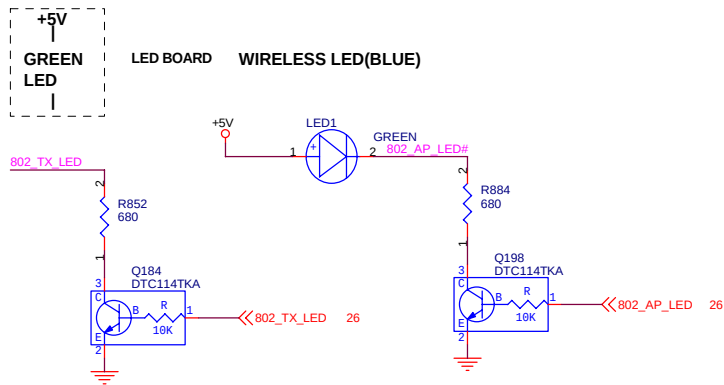


LED

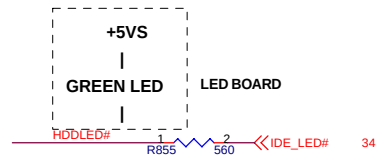
CHARGE LED(ORANGE)



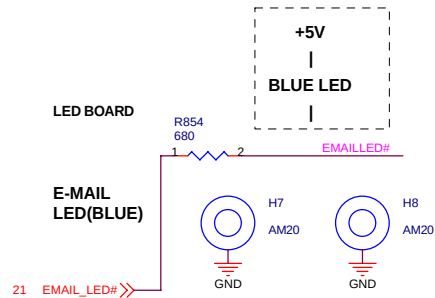
WIRELESS LED(BLUE)



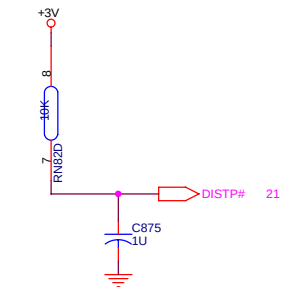
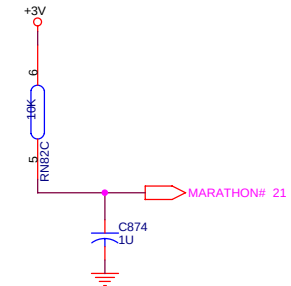
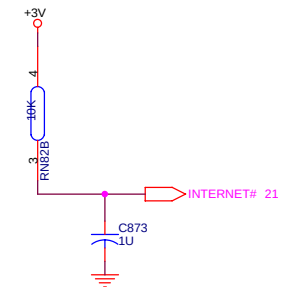
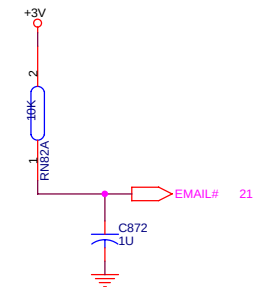
GREEN LED

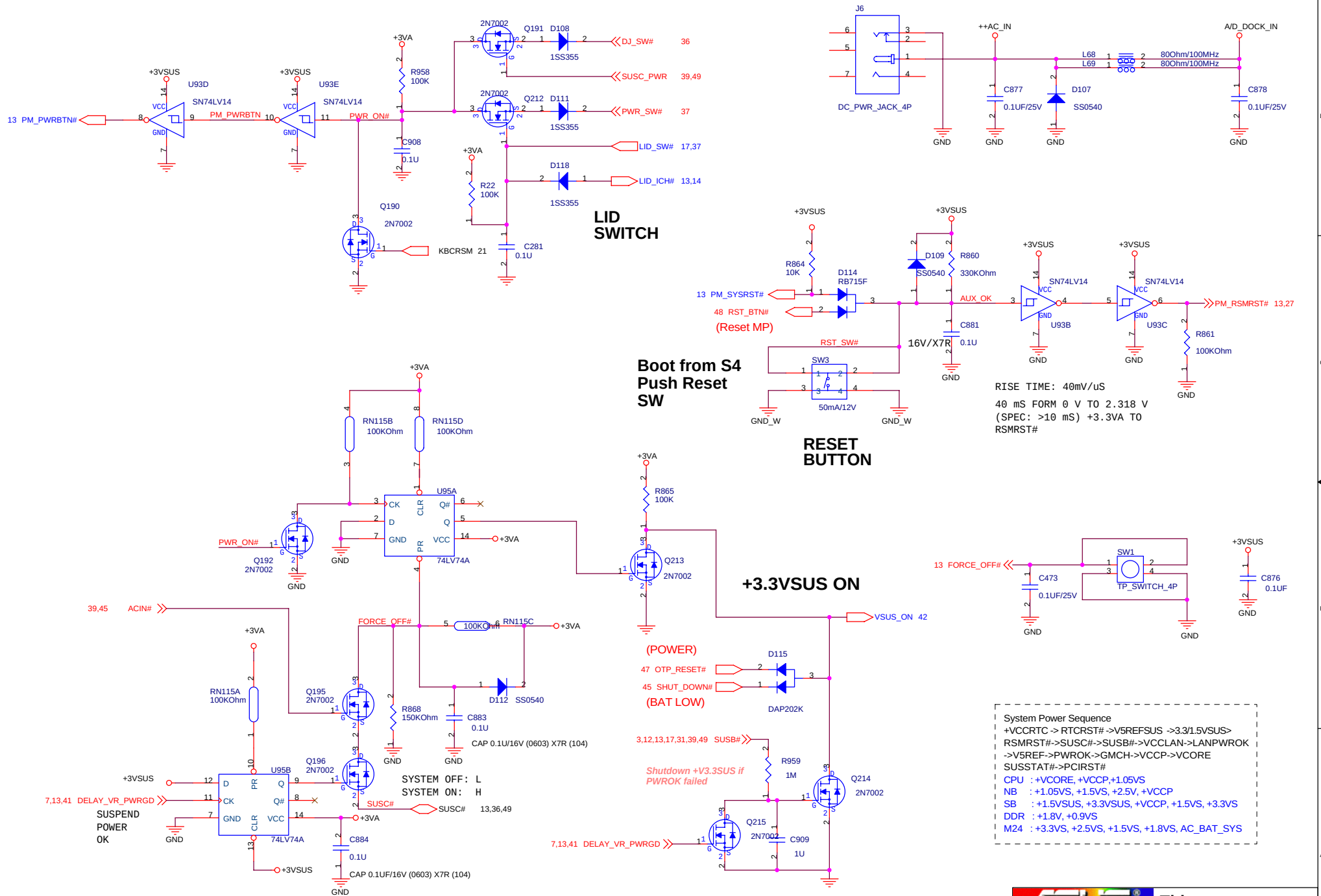


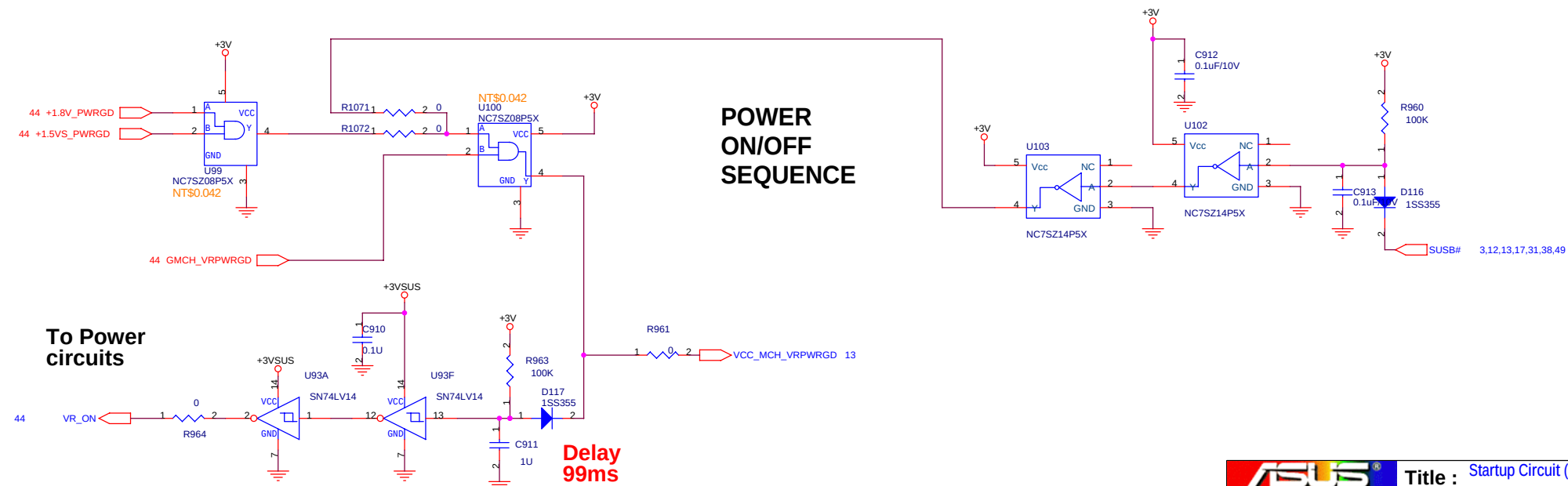
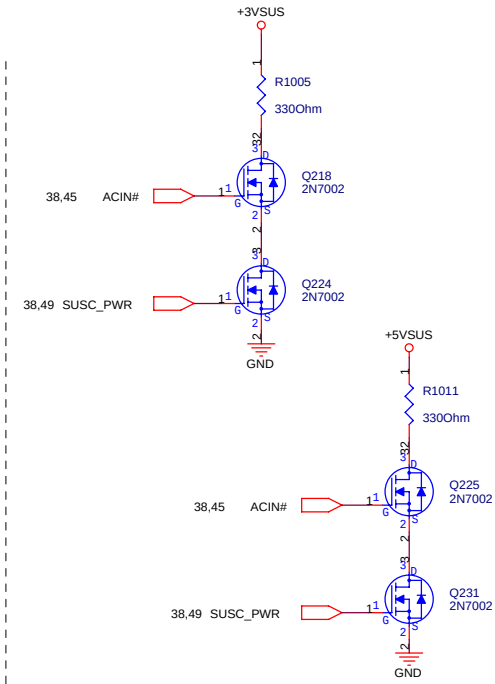
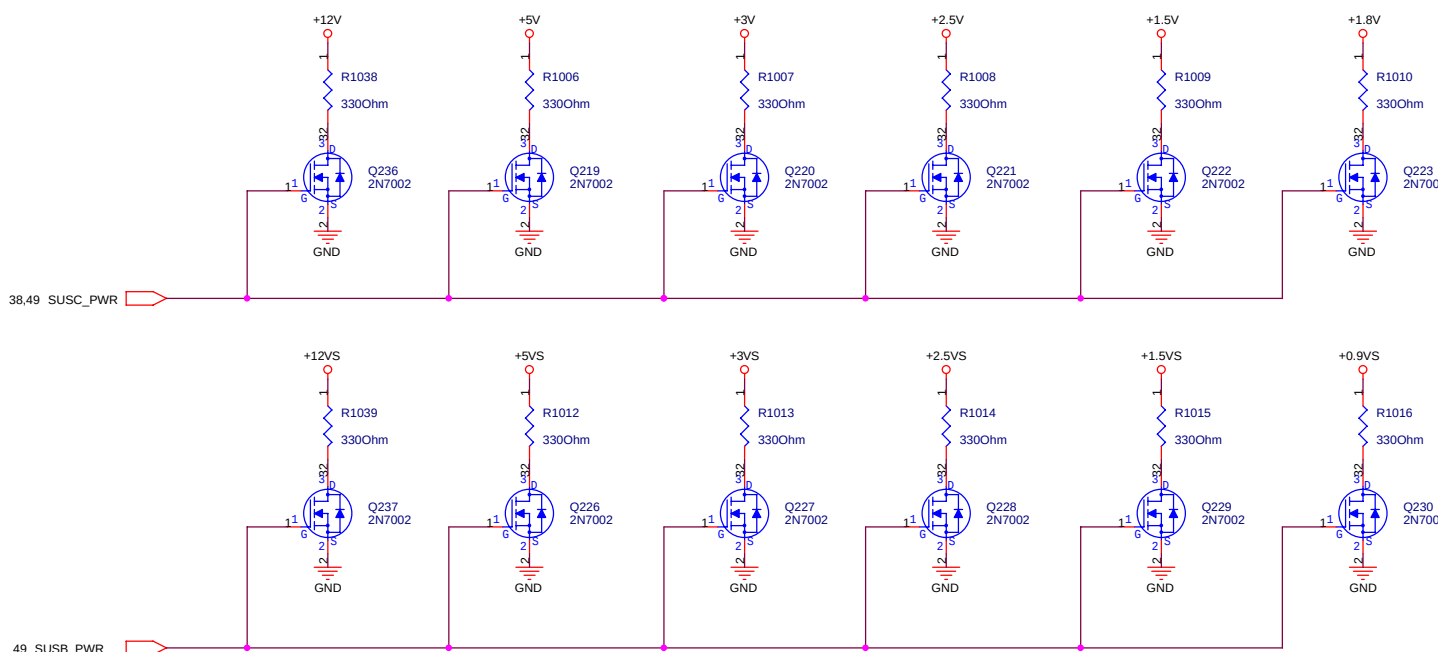
E-MAIL LED(BLUE)



INSTANT KEY



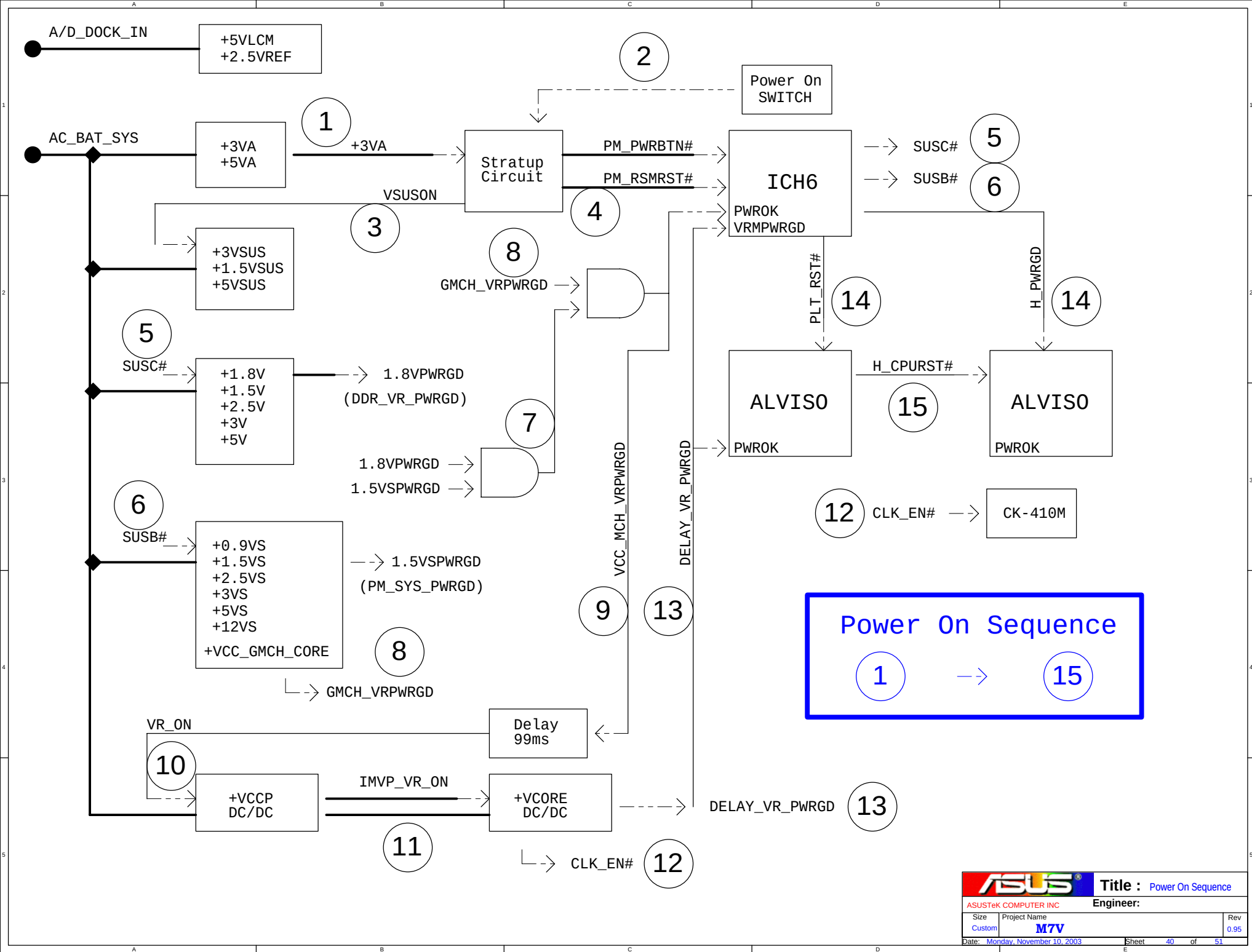


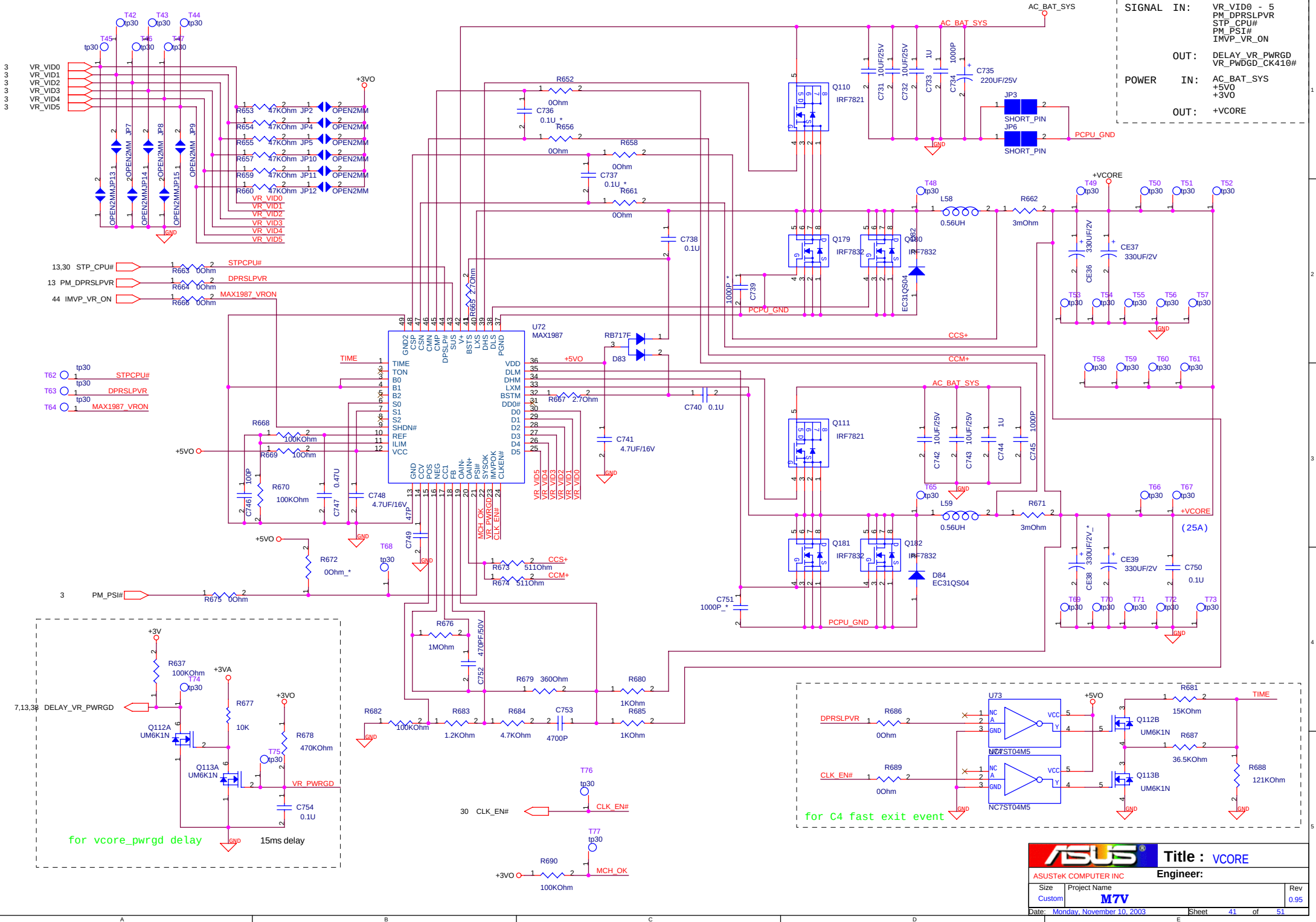


To Power
circuits

POWER ON/OFF SEQUENCE

Delay
99ms



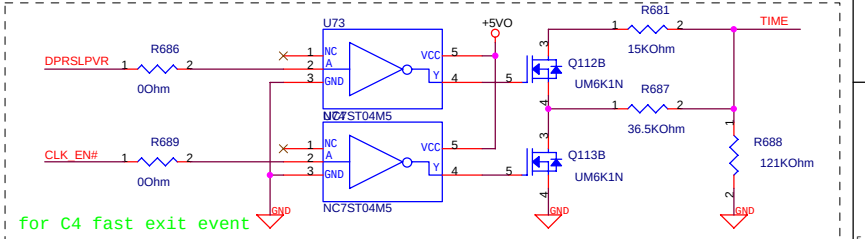


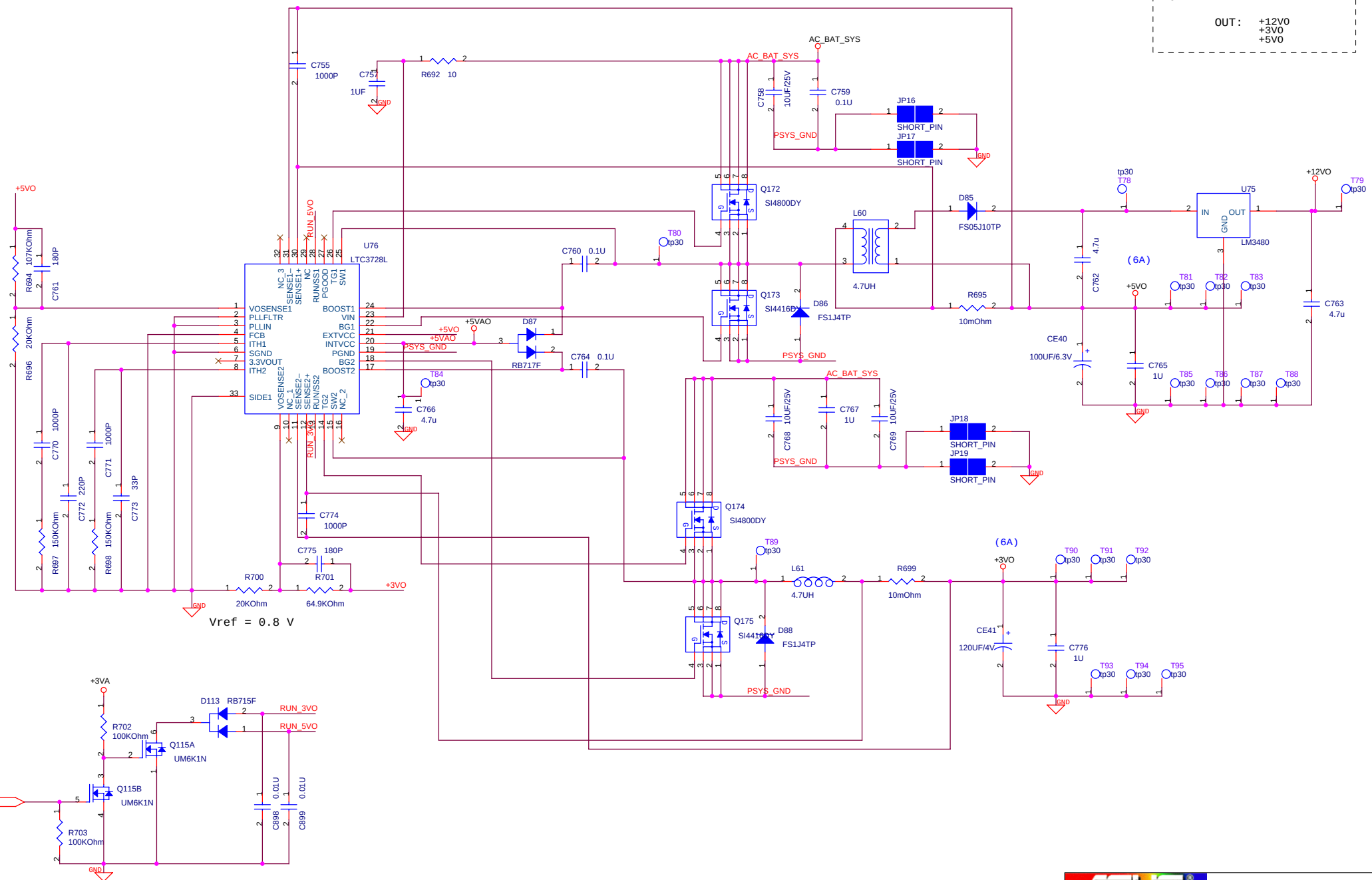
SIGNAL IN: VR_VID0 - 5
PM_DPRSLPVR
STP_CPU#
PM_PSI#
IMVP_VR_ON

OUT: DELAY_VR_PWRGD
VR_PWDGD_CK410#

POWER IN: AC_BAT_SYS
+5VO
+3VO

OUT: +Vcore

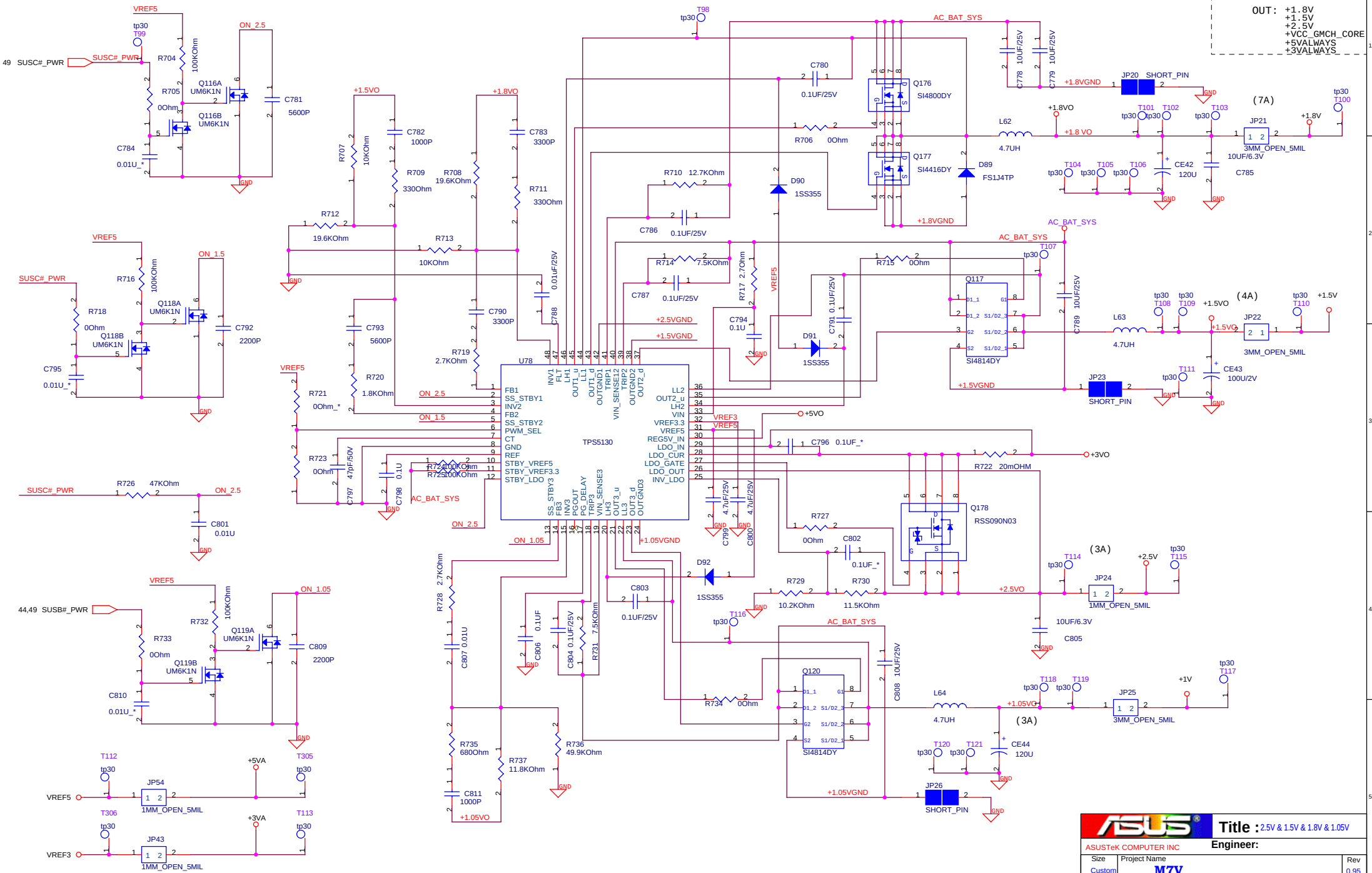


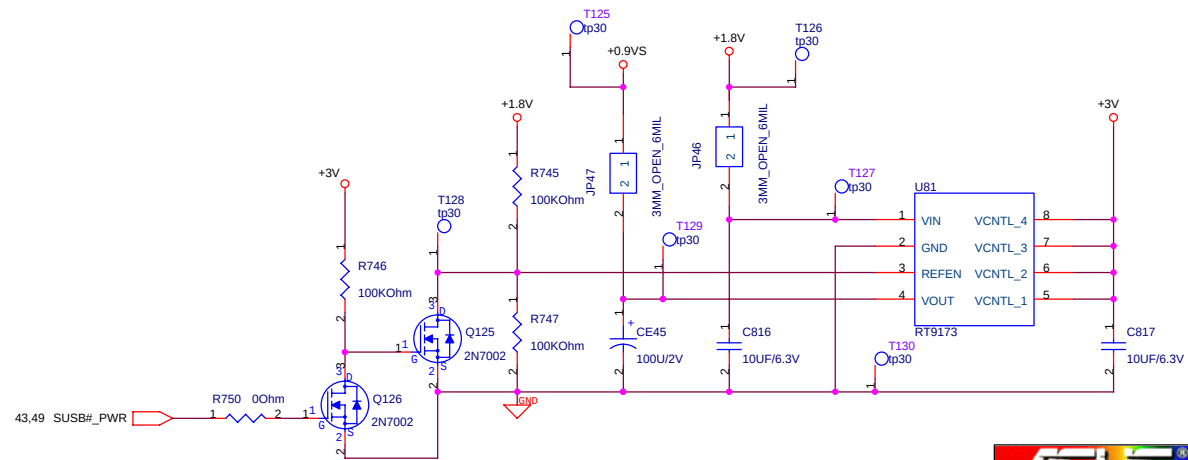
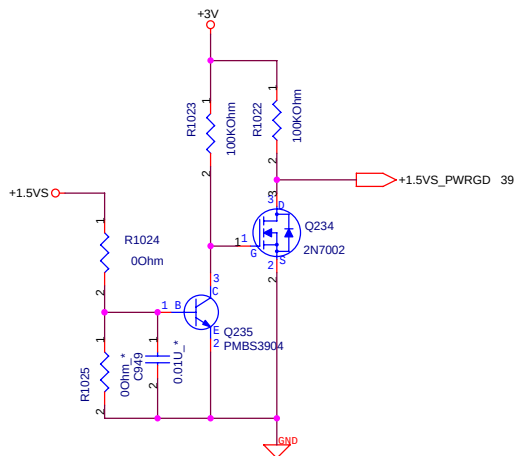
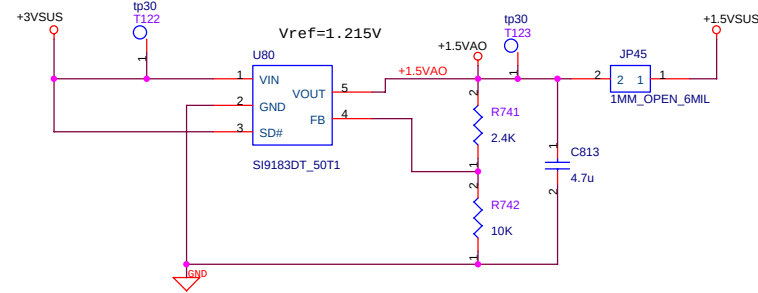
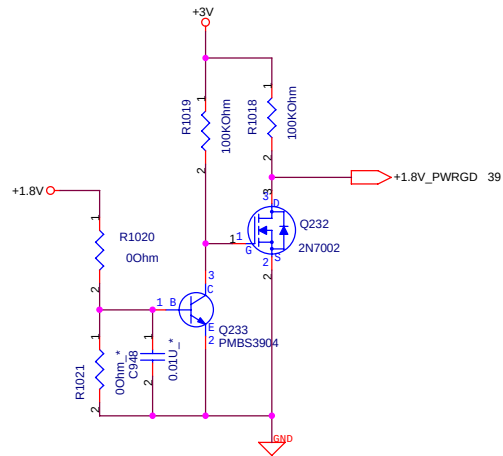
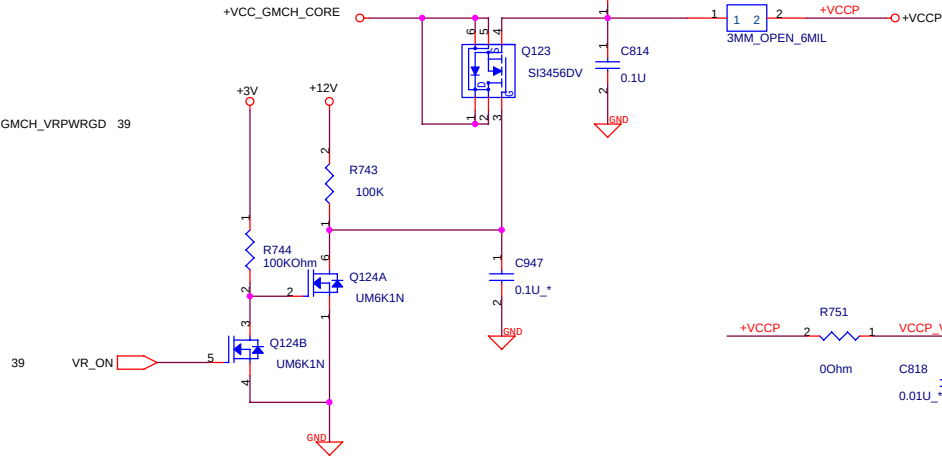
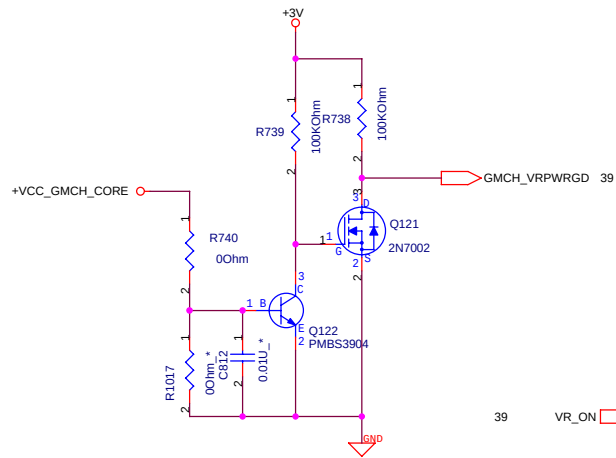


SIGNAL IN: SUSB#_PWR
SUSC#_PWR

POWER IN: AC_BAT_SYS
+3V0

OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS

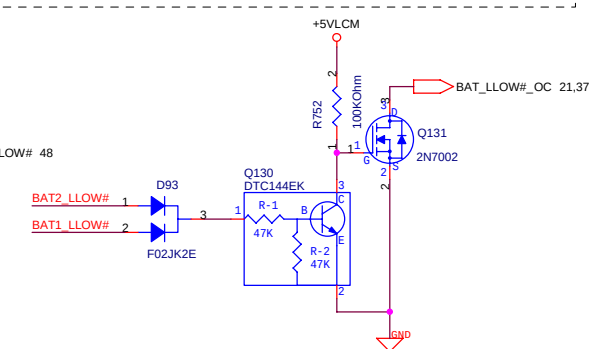
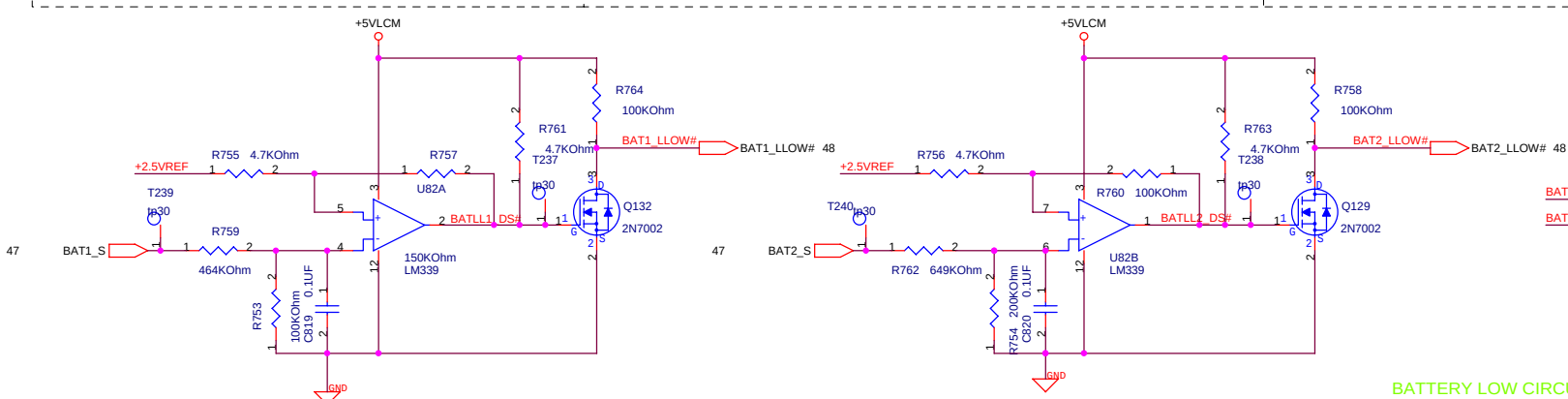
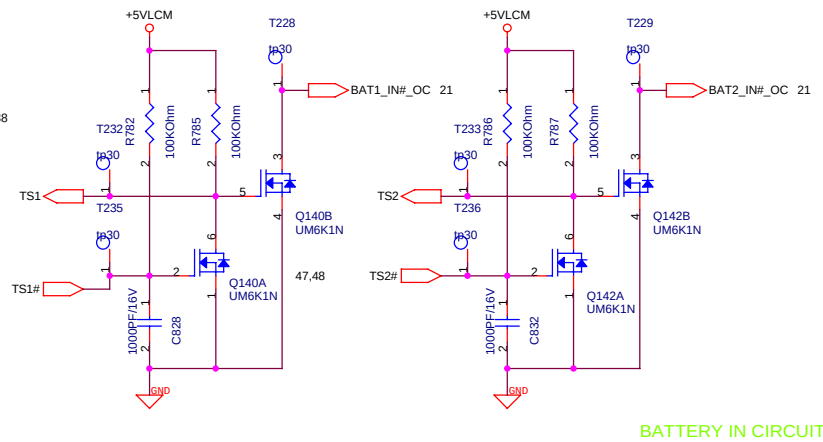
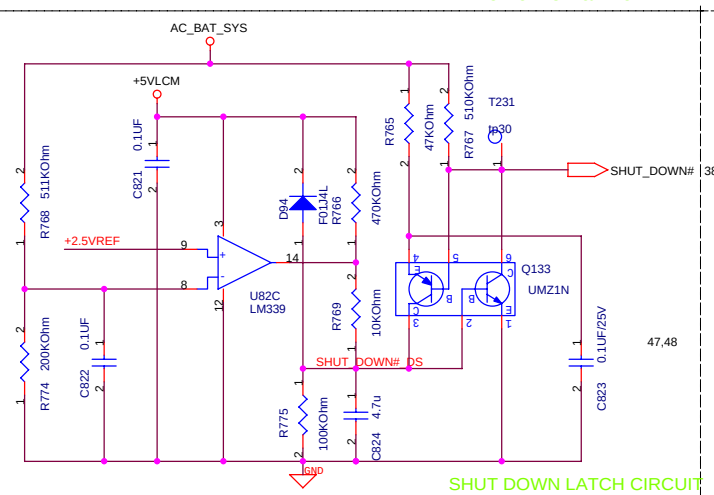
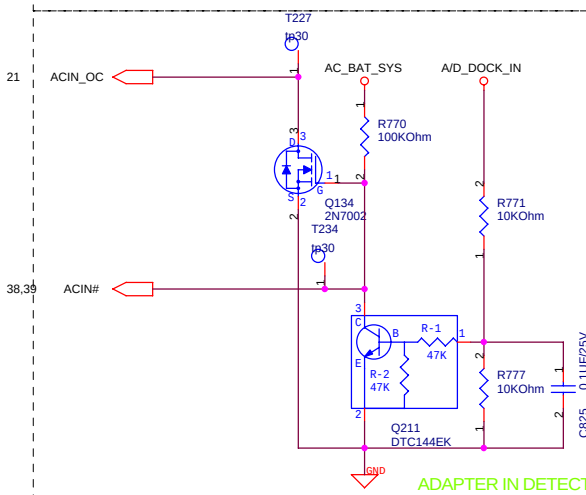
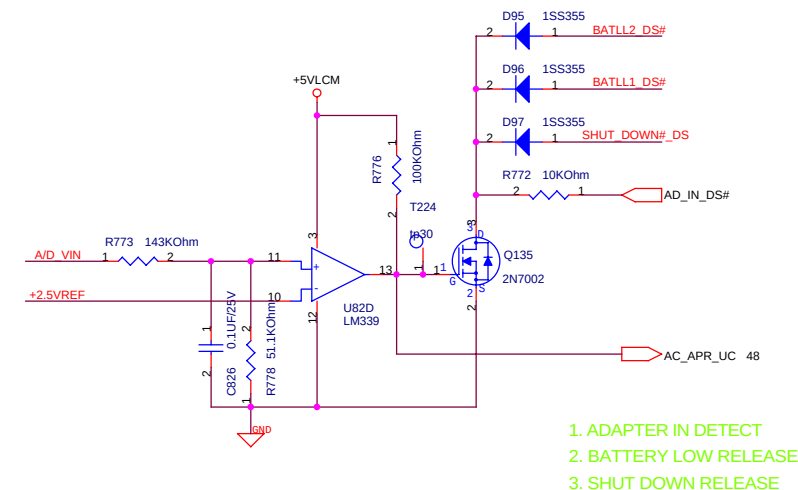
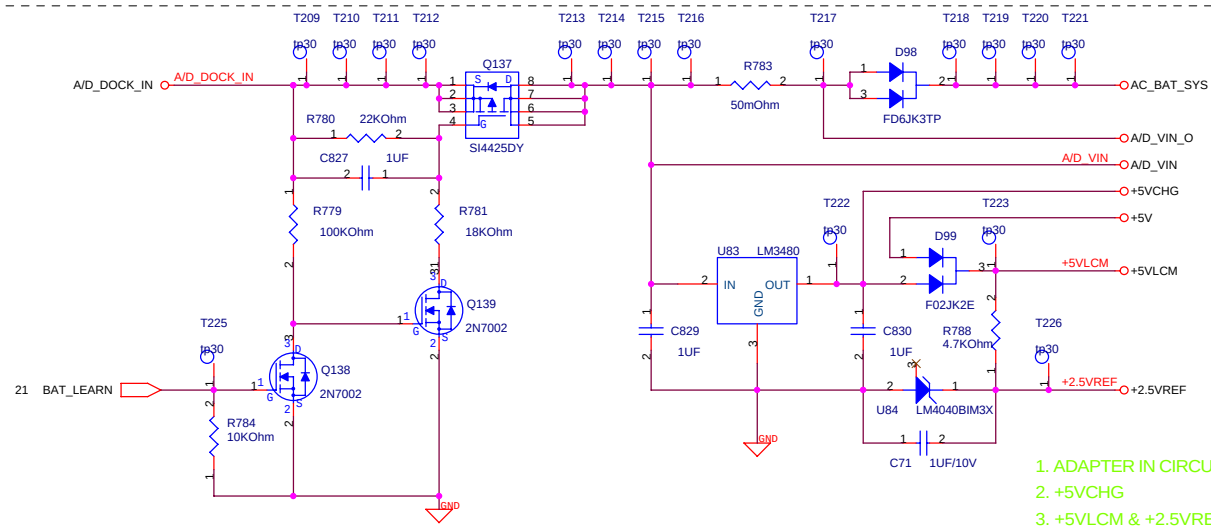


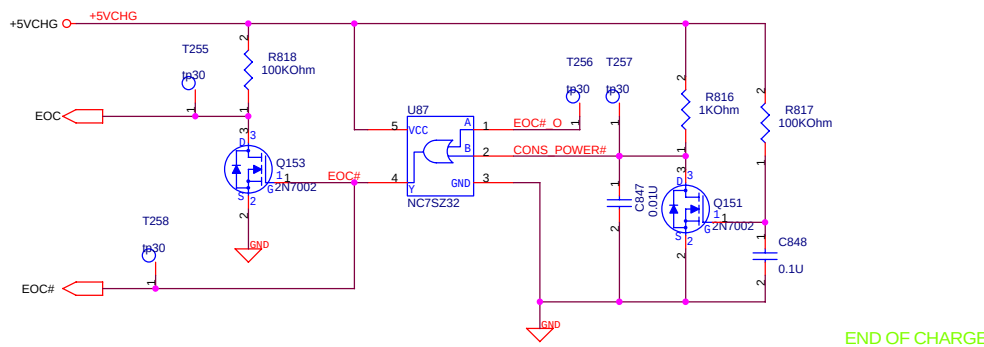
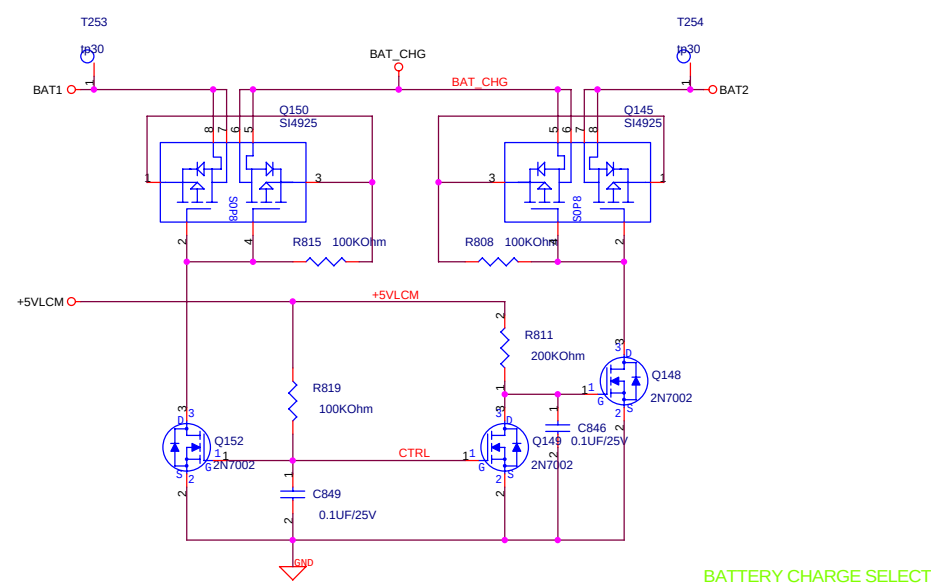
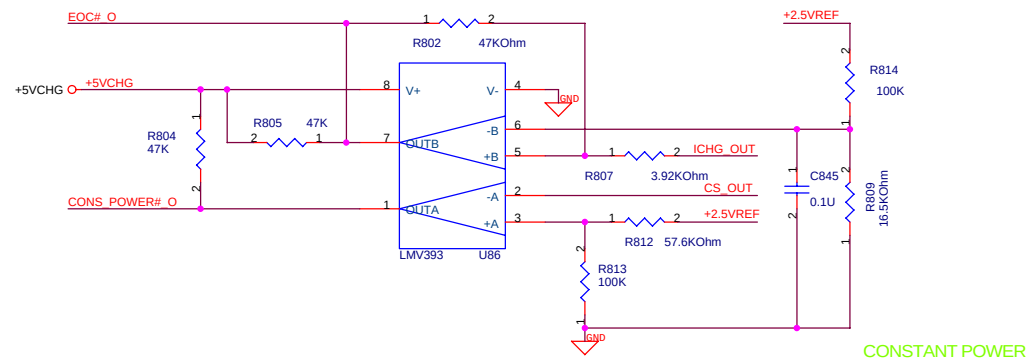
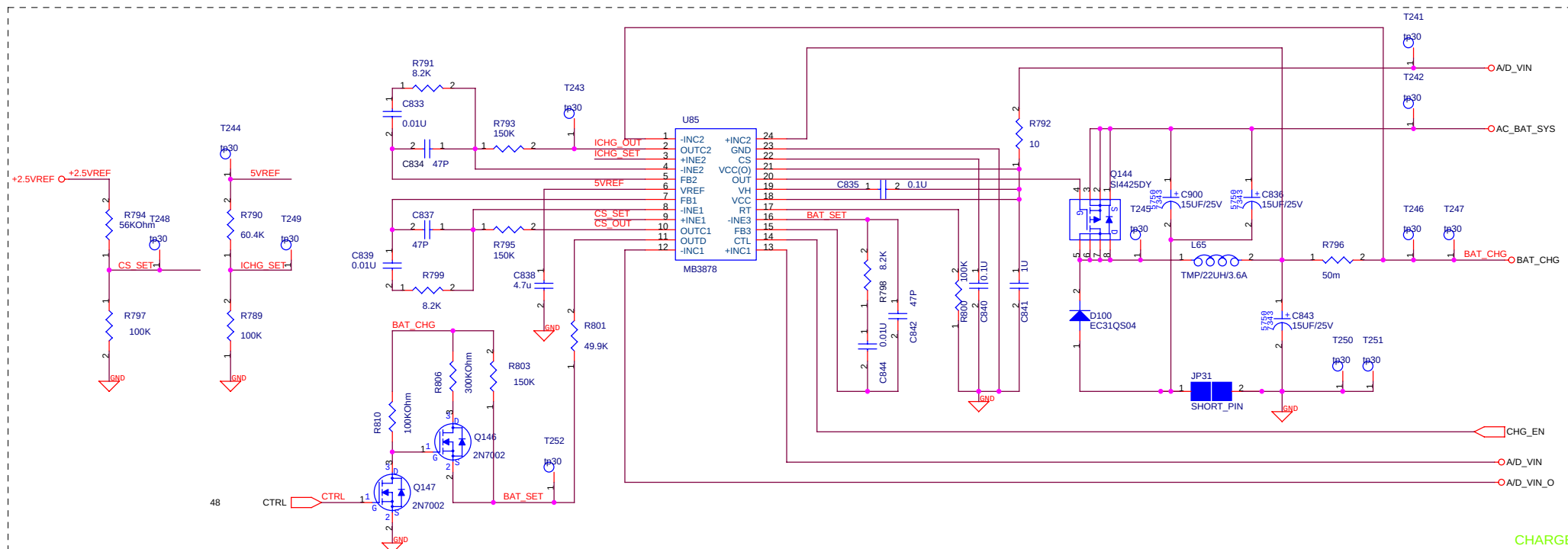


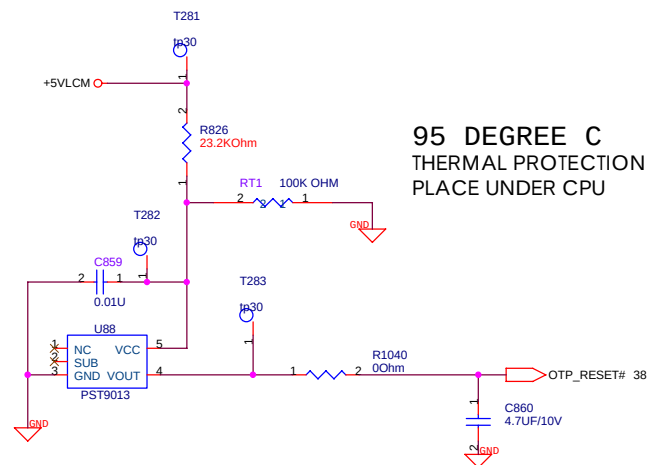
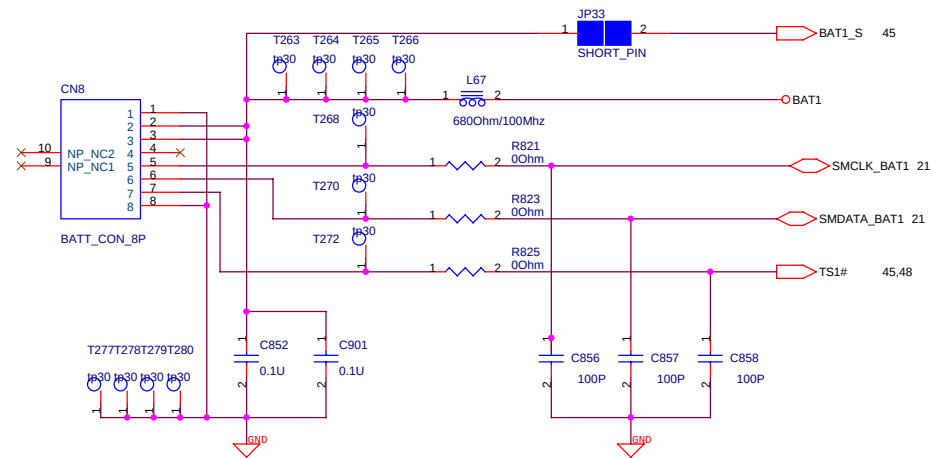
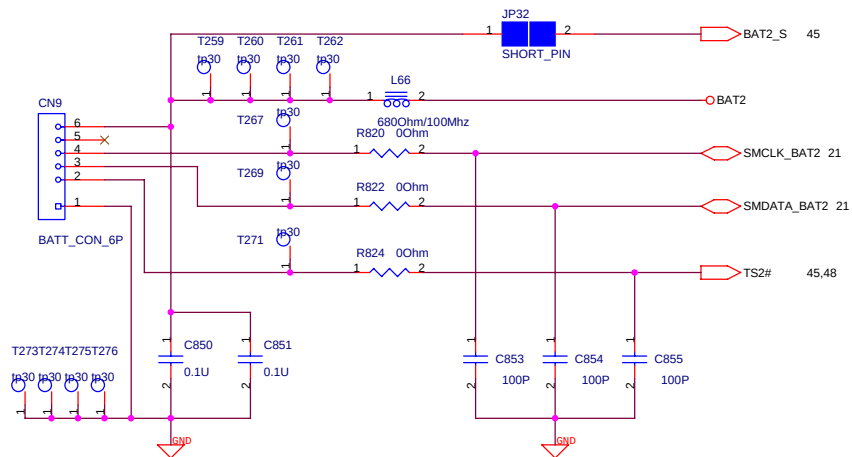
SIGNAL IN: SUSB#_PWR
OUT: VCC_MCH_VRPWRGD
IMVP_VR_ON

POWER IN: +3VA
+3V
+1.8V
+VCC_GMCH_CORE

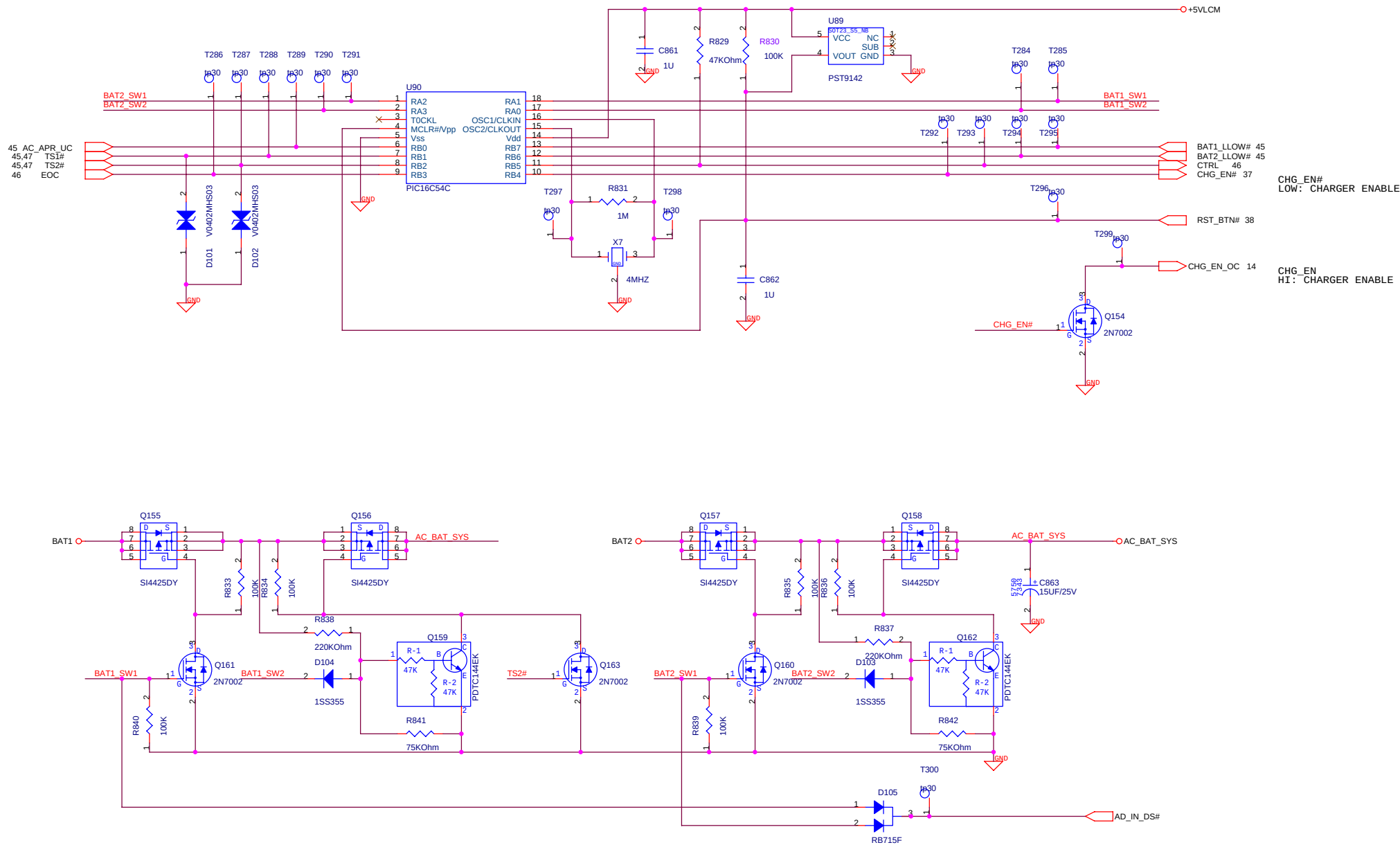
OUT: +0.9VS
+1.5VA
+VCCP

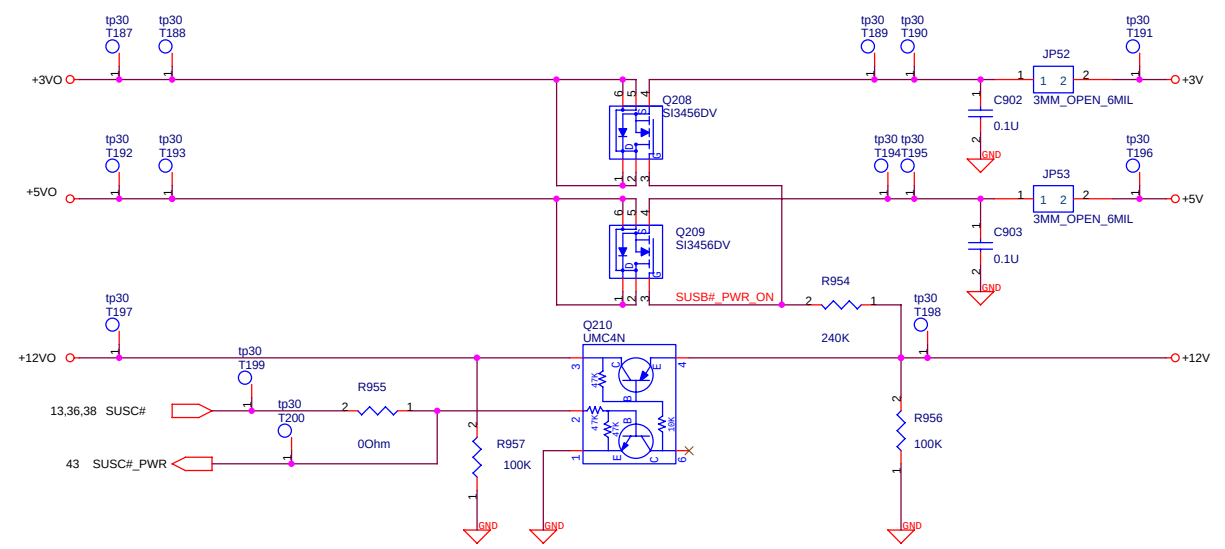
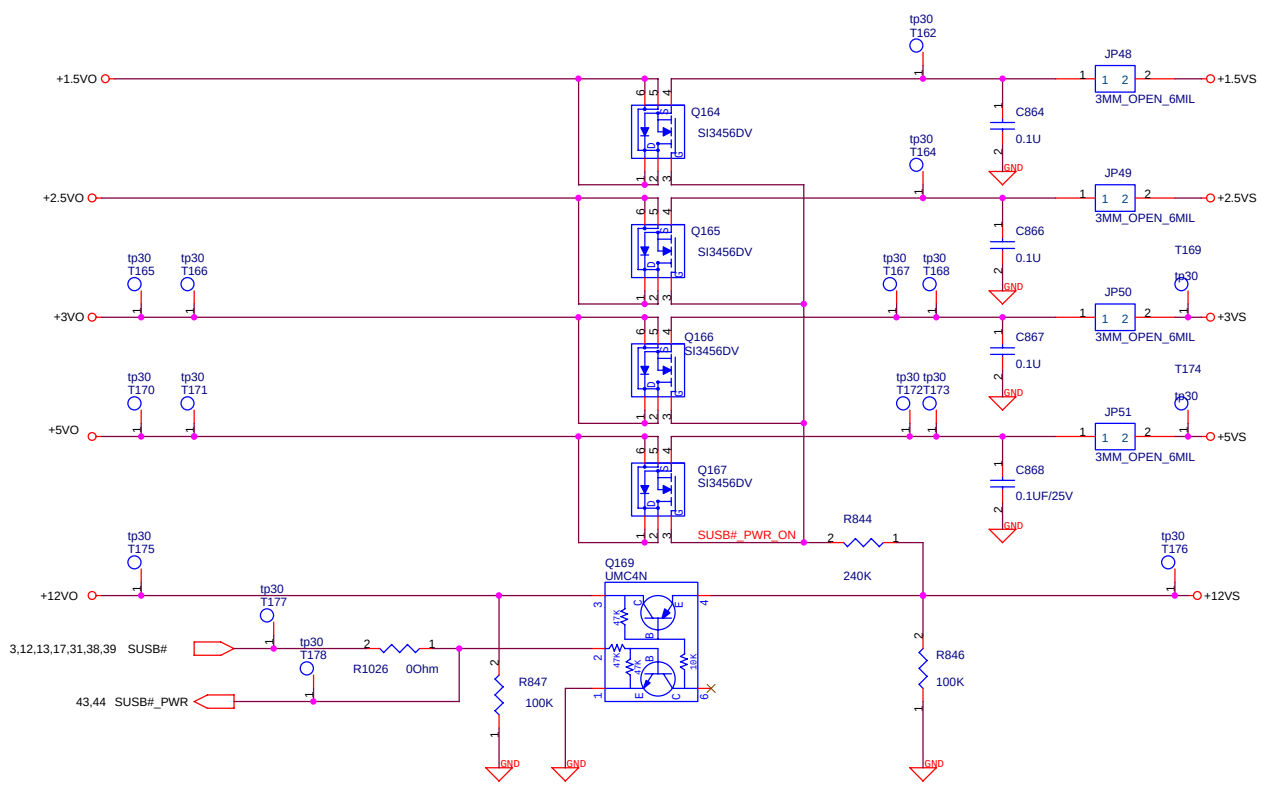
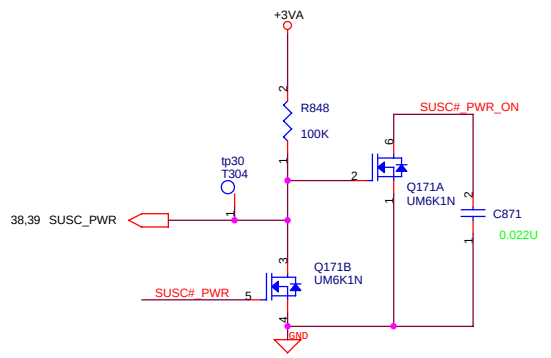
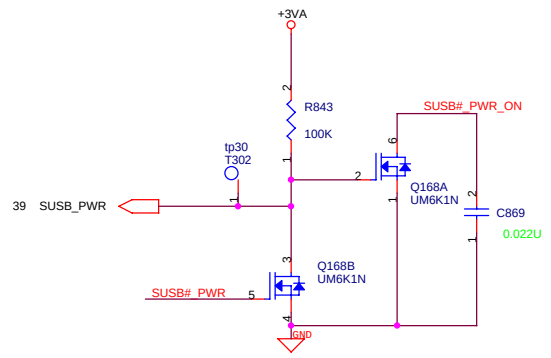
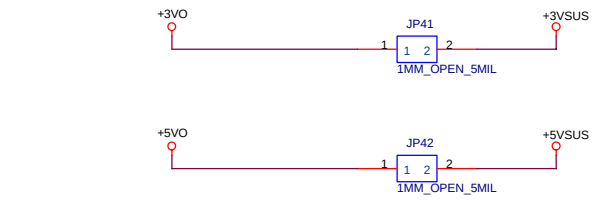


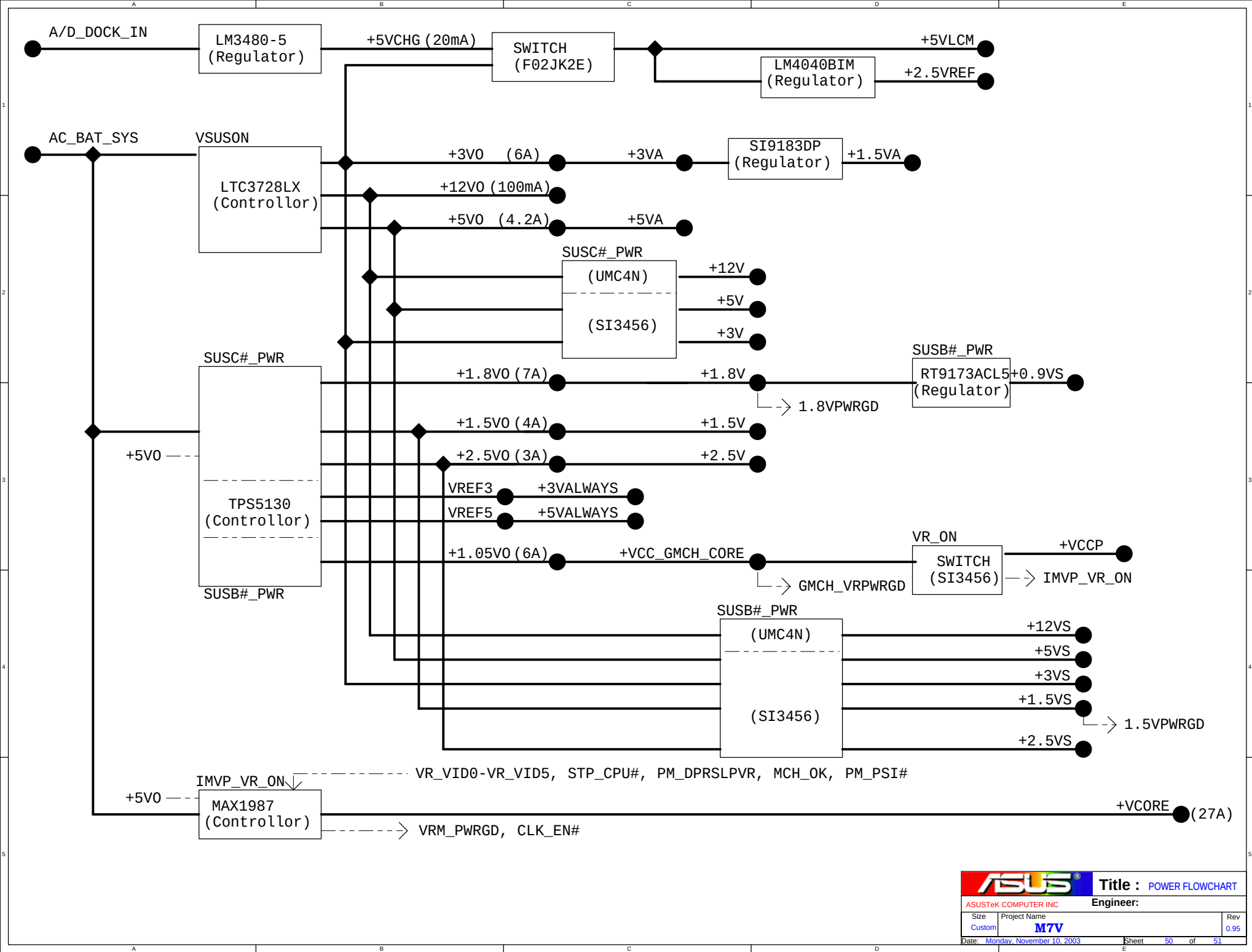




95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU







PCI Device	IDSEL#	REQ / GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)
Ambient Light Sensor	0111001x (72)

ICH6-M GPIO	M7V	W2	Volt
GPI 0	KID0	KID0	5VREF
GPI 1	KID1	KID1	5VREF
GPI 2			5VREF
GPI 3			5VREF
GPI 4			5VREF
GPI 5			5VREF
GPI 7	CPPE# (NEWCARD)		3V
GPI 8	EXTSMI#	EXTSMI#	3VSUS
GPI 11	LID_ICH#	LID_ICH#	3VSUS
GPI 12	KB_SCI#	KB_SCI#	3V
GPI 13			3VSUS
GPI 14	CHG_EN_OC	CHG_EN_OC	3VSUS
GPI 15			3VSUS
GPO 16	XIDE_EN#		3V
GPO 17			3V
GPO 19	PWRLED_1HZ	PWRLED_1HZ	3V
GPO 21	BACK_OFF#	BACK_OFF#	3V
GPO 23	FWH_WP#	FWH_WP#	3V
GPIO 24	NEWCARD_RST#		3VSUS
GPI 26	SATA_DET#0	SATA_DET#0	3V
GPIO 27	PCB_ID0	PCB_ID0	3VSUS
GPIO 28	PCB_ID1	PCB_ID1	3VSUS
GPI 29	PCB_ID2	PCB_ID2	3V
GPI 30			3V
GPI 31	PEG_PRESENT#		3V
GPIO 33	BAY_IN0		3V
GPIO 34	BAY_IN1		3V
GPI 40	PANEL_ID0	PANEL_ID0	5VREF
GPI 41	PANEL_ID1	PANEL_ID1	3V
GPO 48	OP_SD#	OP_SD#	3V
			3V
GPIO 25	CB_SD#	CB_SD#	3VSUS

KBC GPIO	M7V	W2
P23	CLR_DJ#	MSK_INSTKEY#
P22	BAT_LEARN	BAT_LEARN
P21	BAT_SEL	
P20	KBCRSM	KBCRSM
P42		(WATCHDOG)
P43	SWDJ_EN#	SWDJ_EN#
P44	KB_CPURST	KB_CPURST
P45	KB_GATEA20	KB_GATEA20
P46	KBCSCI	KBCSCI
P47	PM_CLKRUN#	PM_CLKRUN#
P50	BAT_LLOW#_OC	BAT_LLOW#_OC
P51	SWDJ_LED	SWDJ_LED
P52	PM_LAN_ENABLE **	PM_LAN_ENABLE **
P53		
P54	BAYDOCK_IN#	
P55	BAT1_IN#_OC	BAT1_IN_OC#
P56		(FAN_DA1)
P57	INV_DA	ADJ_BL
P67	BAT2_IN#_OC	
P66	PADLOCK#	PADLOCK#
P65	MARATHON#	MARATHON#
P64	ACIN_OC	ACIN_OC
P63		
P62		
P61	INTERNET#	INTERNET#
P60	EMAIL#	EMAIL#
P75		(KB_CLK)
P74		(MS_CLK)
P73	TPAD_CLK	TPAD_CLK
P72		(KB_DAT)
P71		(MS_DAT)
P70	TPAD_DAT	TPAD_DAT
P77	BAT_SMC	BAT_SMC
P76	BAT_SMD	BAT_SMD
P27	SCROLL_LED#	SCROLLLOCK#
P26	NUM_LED#	NUM_LED#
P25	CAP_LED#	CAP_LED#
P24	SET_PLTRSTNS#	SET_PLTRSTNS#
P40	EXT_SMI	KBC_EXTSMI
P41	EMAIL_LED#	EMAIL_LED#