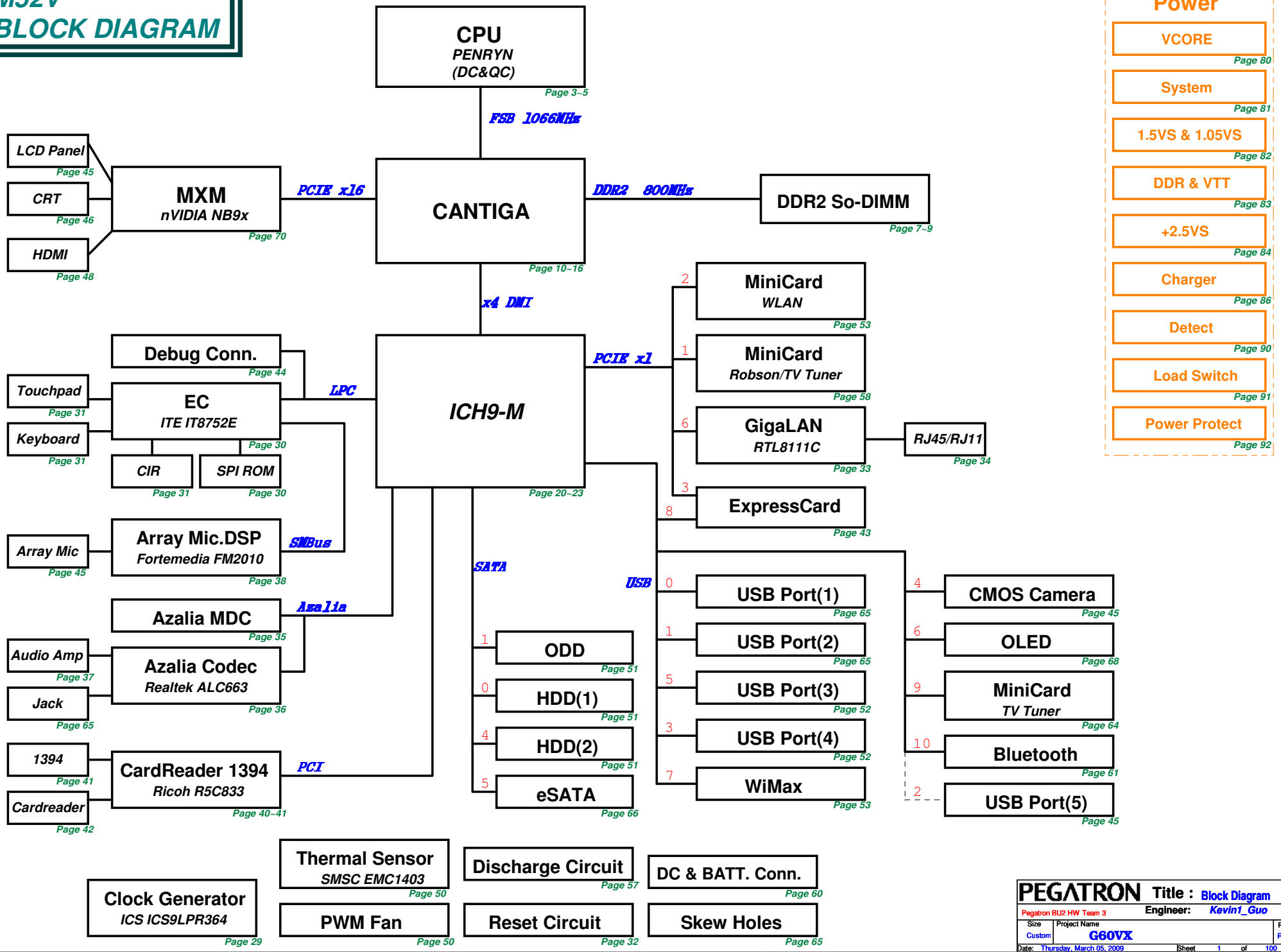
M52V BLOCK DIAGRAM



PEGATRON	Title : Block Diagram		
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo		
Size: Custom	Project Name: G60VX		Rev: R 1.2
Date: Thursday, March 05, 2009	Sheet 1 of 100		

ICH9-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIRQF#/GPIO3	PCI_INTF#	I/OD
F12	PIRQG#/GPIO4	PCI_INTG#	I/OD
B3	PIRQH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPIO8	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLGPIO1/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPIO12	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLGPIO2/GPIO14		
AE20	STP_PCI#/GPIO15	STP_PCI#	I/O
AJ14	DPRSLPVR/GPIO16	PM_DPRSLPVR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPIO18		
AJ10	GPIO19/SATA1GP		
AE11	GPIO20	BT_LED_ON	O
AJ12	SATA0GP/GPIO21		
AG10	SCLOCK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLGPIO0/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

EC IT8512E GPIO SETTING

Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O
29	PWM1/GPA1	CHG_LED_UP#	O
32	PWM2/GPA2		
33	PWM3/GPA3		
34	PWM4/GPA4	LCD_BL_PWM	O
35	PWM5/GPA5	FAN_PWM	O
36	PWM6/GPA6		
38	PWM7/GPA7		
122	RXD/GPB0	CHG_EN#	O
123	TXD/GPB1	PRECHG	O
139	CTX0/GPB2		
124	SMCLK0/GPB3	SMB0_CLK	I/O
125	SMDAT0/GPB4	SMB0_DAT	I/O
142	GA20/GPB5	A20GATE	O
4	KBRST#/GPB6	RC_IN#	O
126	GPB7	PM_RSMRST#	O
133	CRX0/GPC0	CRX0	I
129	SMCLK1/GPC1	SMB1_CLK	I/O
130	SMDAT1/GPC2	SMB1_DAT	I/O
64	GPC3	PM_PWRBTN#	O
136	WUI2/GPC4	AC_IN_OC#	I
65	GPC5	OP_SD#	O
140	WUI3/GPC6	BAT1_IN_OC#	I
20	GPC7	RFON_SW#	I
22	WUI0/GPD0	PWRLIMIT#	I
25	WUI1/GPD1	PM_SUSC#	I
26	WUI4/GPD2	BUF_PLT_RST#	I
27	ECSCI#/GPD3	EXT_SCI#	O
19	GPD4	EXT_SMI#	O
37	GPD5	LCD_BACKOFF#	O
53	TACH0 / GPD6	FAN0_TACH	I
54	GPD7		
23	GPE0	VSUS_ON	O
94	GPE1	SUSC_EC#	O
95	GPE2	SUSB_EC#	O
96	GPE3	CPU_VRON	O
141	PWRSW/GPE4	PWR_SW#	I
39	WUI5/GPE5	BAT2_IN_OC#	I
21	GPE6	LID_SW#	I
24	GPE7	INSTANT_ON#	I
97	PS2CLK0/GPF0		
98	PS2DAT0/GPF1	COLOREN#	I
99	PS2CLK1/GPF2	MARATHON#	I
100	PS2DAT1/GPF3	DISTP#	I
101	PS2CLK2/GPF4	TP_CLK	I/O
102	PS2DAT2/GPF5	TP_DAT	I/O
131	SMCLK2/GPF6	THRO_CPU	O
132	SMDAT2/GPF7	TP_LED	O
118	WUI7/GPG0		
121	GPG1	PM_SUSB#	I
112	GPG2		
116	GPG6		

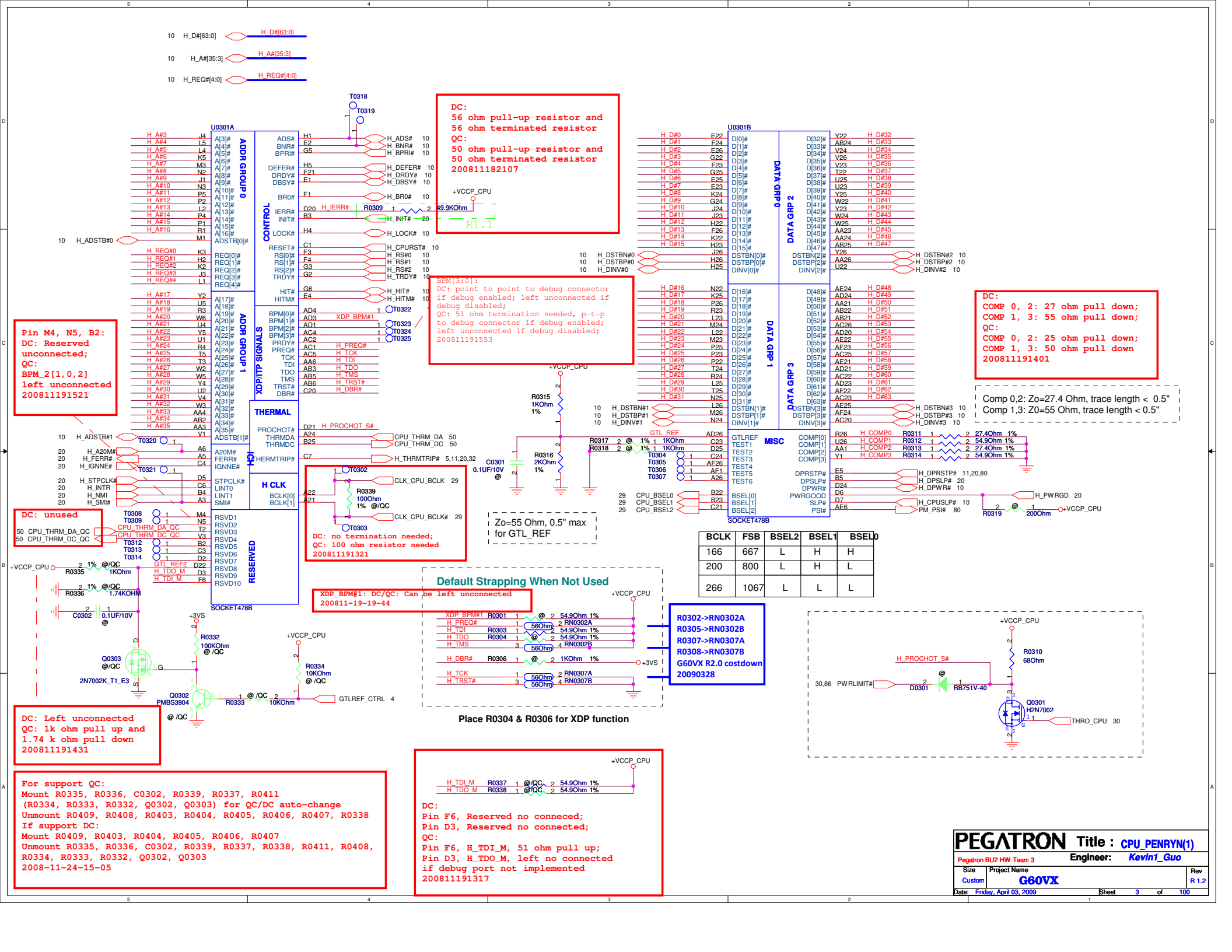
Pin	Pin Name	Signal Name	Type
105	CLKRUN#/GPH0	PM_CLKRUN#	I/O
106	CRX1/GPH1	3G_ON#	O
107	CTX1/GPH2	3G_LED_ON#	O
108	GPH3	BAT_LEARN	I/O
109	GPH4		
110	GPH5	NUM_LED	O
111	GPH6	CAP_LED	O
74	ADC0/GPI0	NV_OVERT#	I
75	ADC1/GPI1	SUS_PWRGD	I
76	ADC2/GPI2	ALL_SYS_PWRGD	I
77	ADC3/GPI3	CPU_PWRGD	I
78	ADC4/GPI4	PWR_MON	I
79	ADC5/GPI5	ALS_DA	I
80	ADC6/GPI6		
81	ADC7/GPI7		
84	DAC0/GPJ0	EC_CLK_EN	
85	DAC1/GPJ1	PM_PWROK	
86	DAC1/GPJ2		
87	DAC1/GPJ3		
88	DAC1/GPJ4		
89	DAC1/GPJ5		
15	GPK0		
16	GPK1		
17	GPK2		
18	GPK3		
48	GPK4		
49	GPK5		
62	GPK6		
63	GPK7		
90	GPL0		
91	GPL1		
92	GPL2		
93	GPL3		
119	GPL4		
120	GPL5		
134	GPL6		
135	GPL7		

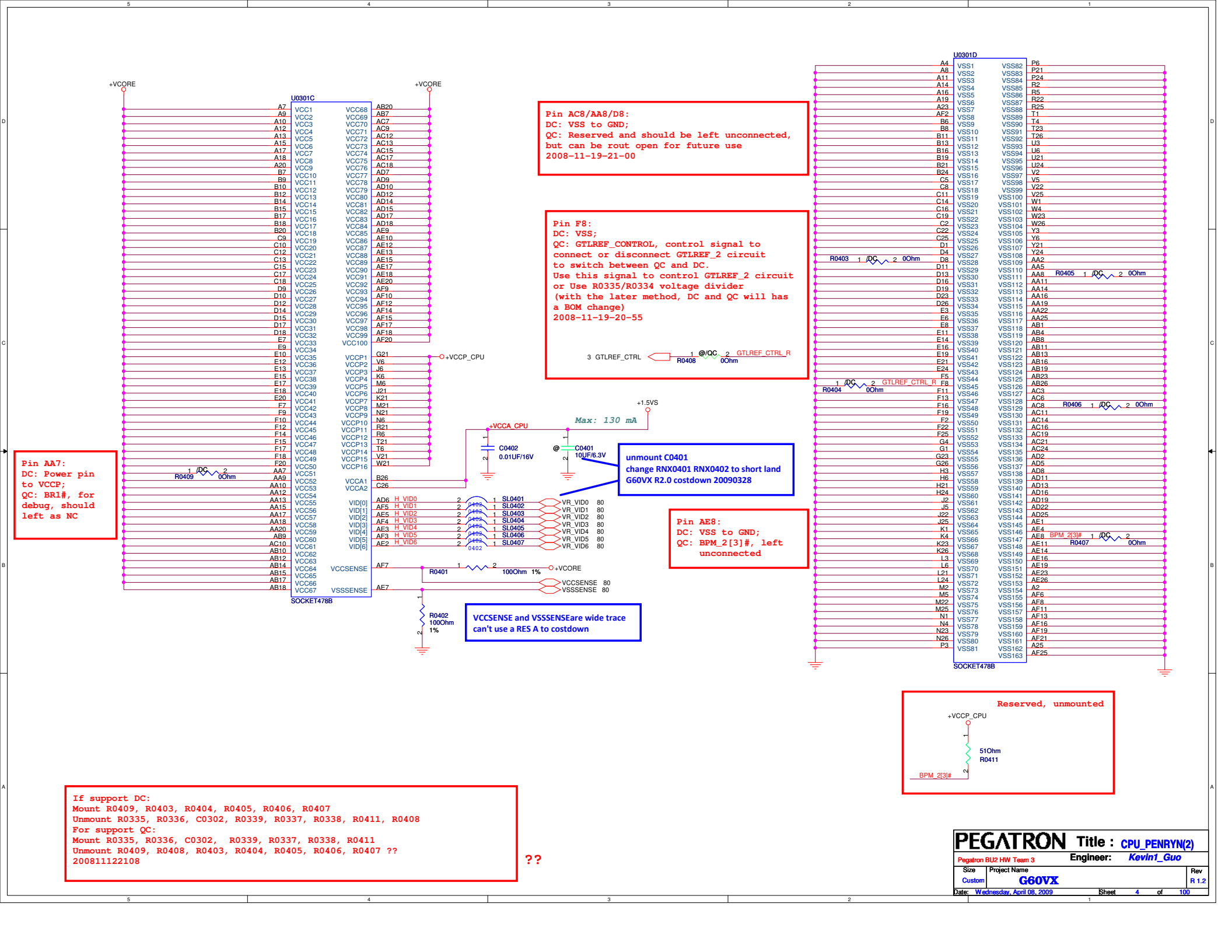
PEGATRON Title : System Setting

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

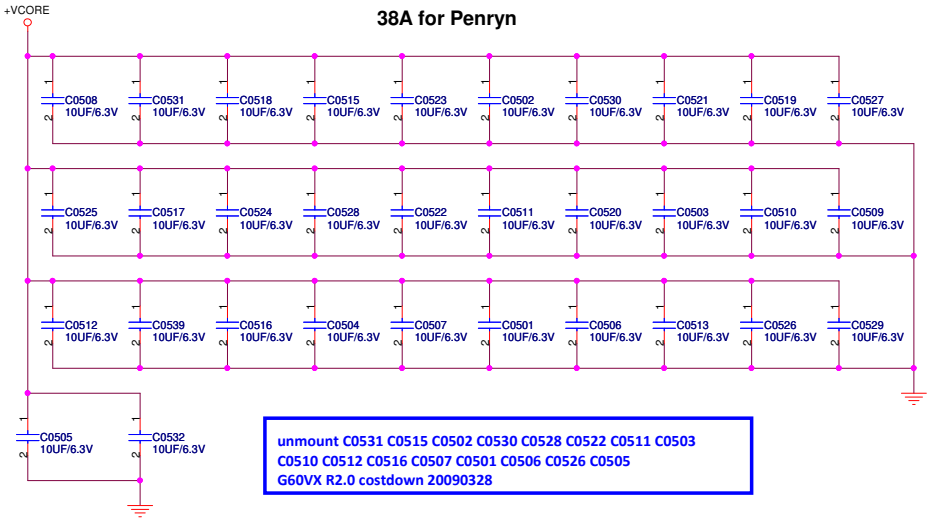
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 2 of 100


10 H_D#[63:0]
H_D#[63:0]
10 H_A#[35:3]
H_A#[35:3]
10 H_REQ#[4:0]
H_REQ#[4:0]
U0301A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
SOCKET478B
U0301B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
SOCKET478B
DC:
56 ohm pull-up resistor and
56 ohm terminated resistor
QC:
50 ohm pull-up resistor and
50 ohm terminated resistor
200811182107
+VCCP_CPU
R0309 49.9KOhm
R1.1
BPM[3:0]:
DC: point to point to debug connector
if debug enabled; left unconnected if
debug disabled;
QC: 51 ohm termination needed, p-t-p
to debug connector if debug enabled;
left unconnected if debug disabled;
200811191553
Pin M4, N5, B2:
DC: Reserved
unconnected;
QC:
BPM_2[1,0,2]
left unconnected
200811191521
DC:
COMP 0, 2: 27 ohm pull down;
COMP 1, 3: 55 ohm pull down;
QC:
COMP 0, 2: 25 ohm pull down;
COMP 1, 3: 50 ohm pull down
200811191401
Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Zo=55 Ohm, trace length < 0.5"
R0315 1KOhm 1%
R0316 2KOhm 1%
C0301 0.1UF/10V
R0317 1KOhm 1%
R0318 1KOhm 1%
Zo=55 Ohm, 0.5" max
for GTL_REF
DC: unused
DC: no termination needed;
QC: 100 ohm resistor needed
200811191321
R0339 100Ohm 1% @/QC
R0319 200Ohm
BCLK FSB BSEL2 BSEL1 BSEL0
166 667 L H H
200 800 L H L
266 1067 L L L
Default Strapping When Not Used
XDP_BPM#1: DC/QC: Can be left unconnected
200811-19-19-44
R0302->RN0302A
R0305->RN0302B
R0307->RN0307A
R0308->RN0307B
G60VX R2.0 costdown
20090328
Place R0304 & R0306 for XDP function
R0335 1KOhm
R0336 1.74KOHM
C0302 0.1UF/10V
R0332 100KOhm @/QC
R0334 10KOhm @/QC
R0333 10KOhm
Q0303 2N7002K_T1_E3
Q0302 PMBS3904
GTLREF_CTRL
DC: Left unconnected
QC: 1k ohm pull up and
1.74 k ohm pull down
200811191431
R0310 68Ohm
D0301 RB751V-40
Q0301 H2N7002
THRO_CPU
30,86 PWRLIMIT#
DC:
Pin F6, Reserved no conneced;
Pin D3, Reserved no connected;
QC:
Pin F6, H_TDI_M, 51 ohm pull up;
Pin D3, H_TDO_M, left no connected
if debug port not implemented
200811191317
For support QC:
Mount R0335, R0336, C0302, R0339, R0337, R0411
(R0334, R0333, R0332, Q0302, Q0303) for QC/DC auto-change
Unmount R0409, R0408, R0403, R0404, R0405, R0406, R0407, R0338
If support DC:
Mount R0409, R0403, R0404, R0405, R0406, R0407
Unmount R0335, R0336, C0302, R0339, R0337, R0338, R0411, R0408,
R0334, R0333, R0332, Q0302, Q0303
2008-11-24-15-05
PEGATRON
Title : CPU_PENRYN(1)
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size Custom
Project Name G60VX
Rev R 1.2
Date: Friday, April 03, 2009
Sheet 3 of 100

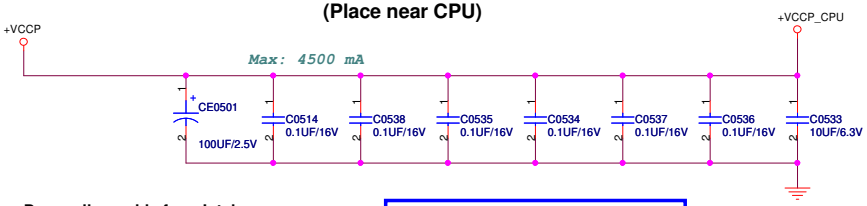

Pin AA7:
DC: Power pin to VCCP;
QC: BR1#, for debug, should left as NC
Pin AC8/AA8/D8:
DC: VSS to GND;
QC: Reserved and should be left unconnected, but can be rout open for future use
2008-11-19-21-00
Pin F8:
DC: VSS;
QC: GTLREF_CONTROL, control signal to connect or disconnect GTLREF_2 circuit to switch between QC and DC.
Use this signal to control GTLREF_2 circuit or Use R0335/R0334 voltage divider (with the later method, DC and QC will has a BOM change)
2008-11-19-20-55
Max: 130 mA
unmount C0401
change RNX0401 RNX0402 to short land
G60VX R2.0 costdown 20090328
Pin AE8:
DC: VSS to GND;
QC: BPM_2[3]#, left unconnected
VCCSENSE and VSSSENSEare wide trace
can't use a RES A to costdown
Reserved, unmounted
If support DC:
Mount R0409, R0403, R0404, R0405, R0406, R0407
Unmount R0335, R0336, C0302, R0339, R0337, R0338, R0411, R0408
For support QC:
Mount R0335, R0336, C0302, R0339, R0337, R0338, R0411
Unmount R0409, R0408, R0403, R0404, R0405, R0406, R0407 ??
200811122108
??
PEGATRON
Title : CPU_PENRYN(2)
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 4 of 100

38A for Penryn



unmount C0531 C0515 C0502 C0530 C0528 C0522 C0511 C0503
C0510 C0512 C0516 C0507 C0501 C0506 C0526 C0505
G60VX R2.0 costdown 20090328

+VCCP Decoupling Capacitor (Place near CPU)



unmount or delete C0538 C0537 C0536
G60VX R2.0 costdown 20090328

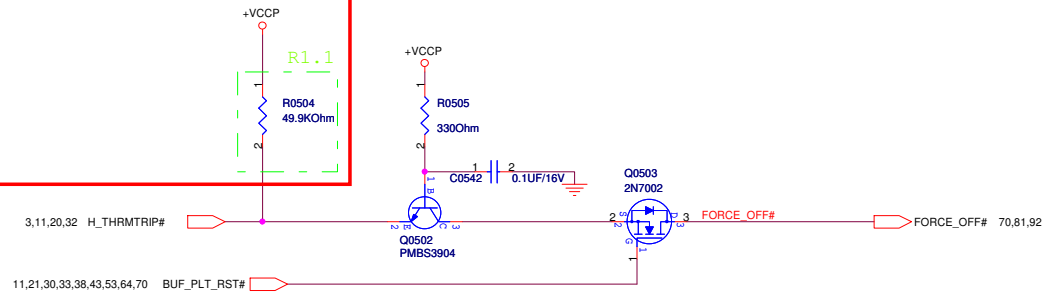
Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?

Checklist recomends THERMTRIP# pull up in the CPU side although functionality not used,
DC: 56 ohm pull up, 55 ohm terminate;
QC: 50 ohm pull up, 50 ohm terminate
200811190902

unmount R0504 R0505 C0542 Q0502 Q0503
connect H_THRMTRIP# to SB to costdown
G60VX R2.0 costdown 20090328



Thermal Trip signal (From CPU to ICH-9M and sequence)

PEGATRON Title : CPU_Capacitor

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, April 09, 2009 Sheet 5 of 100

Main Board

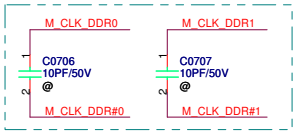
PEGATRON Title : CPU_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

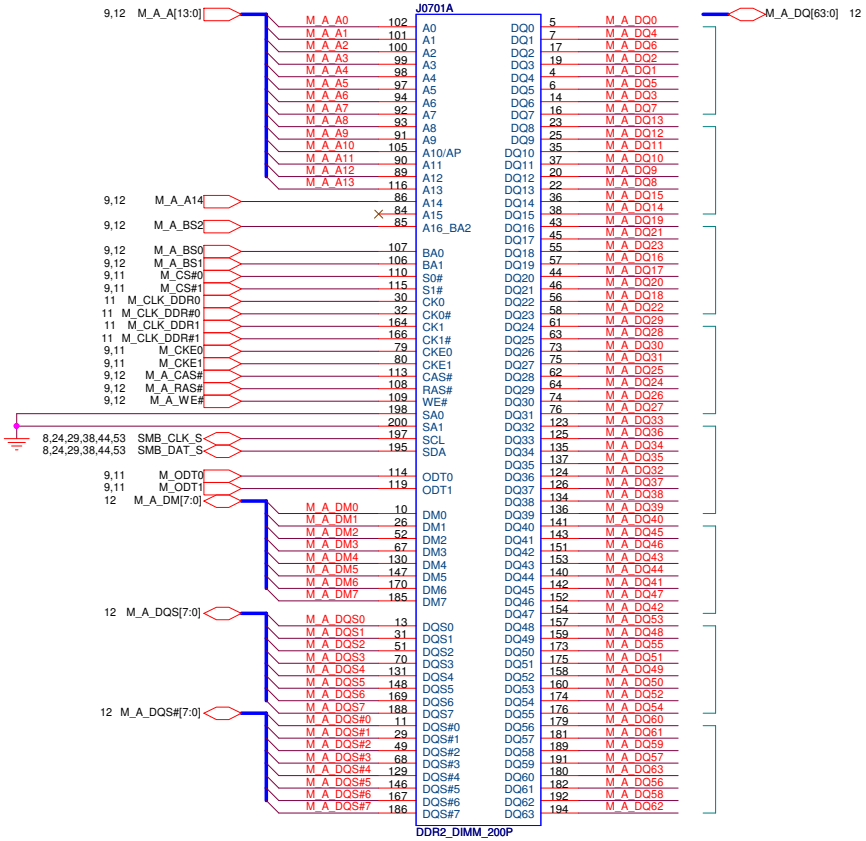
Size	Project Name	Rev
Custom	G60VX	R 1.2

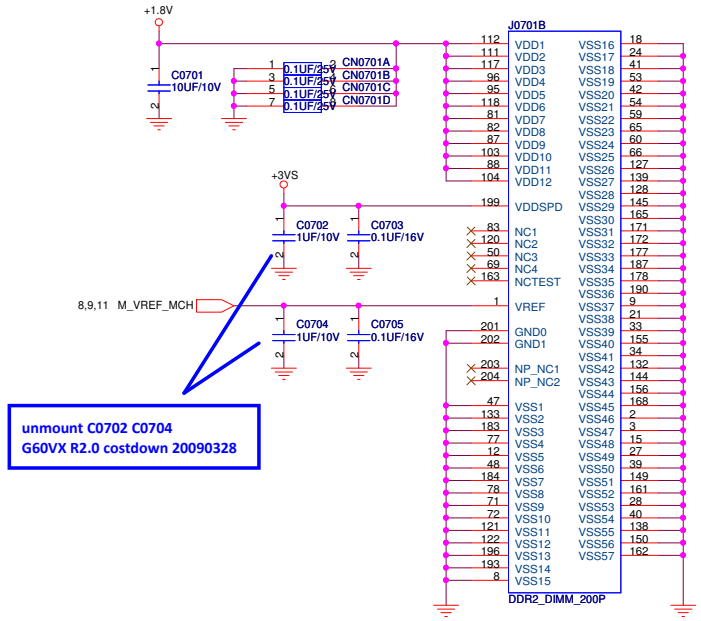
Date: Thursday, March 05, 2009 Sheet 6 of 100

Reserved for 3G



Reverse Type
H = 9.2 mm

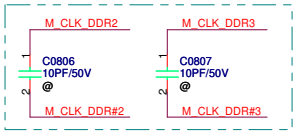




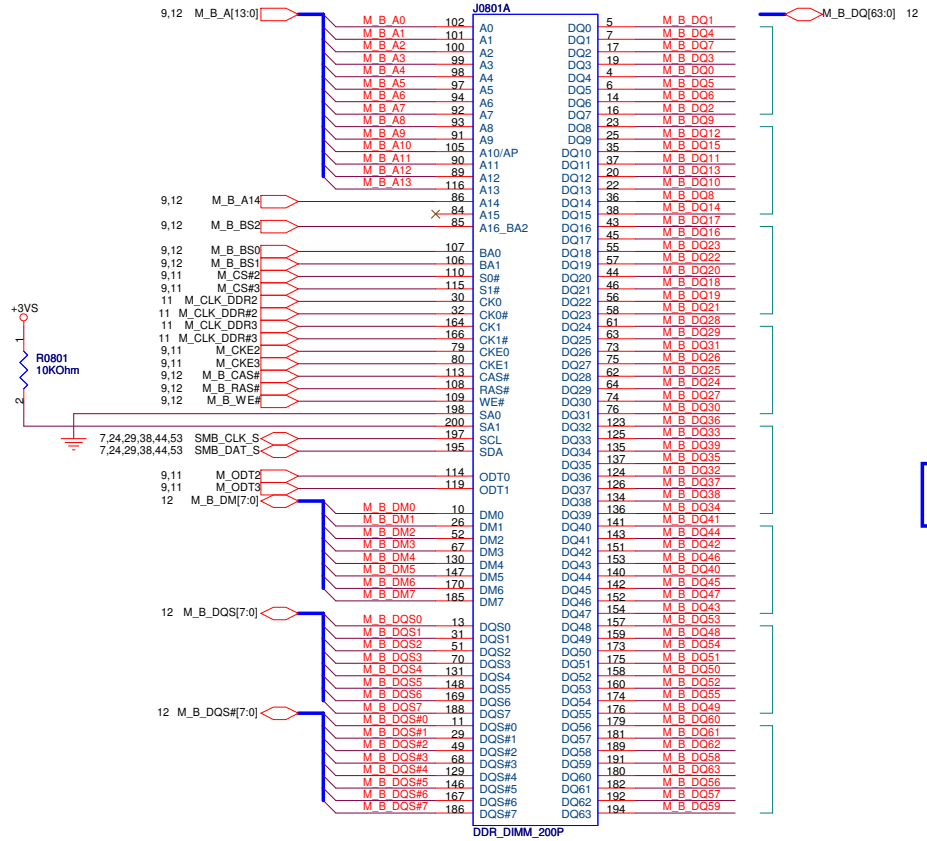
unmount C0702 C0704
G60VX R2.0 costdown 20090328

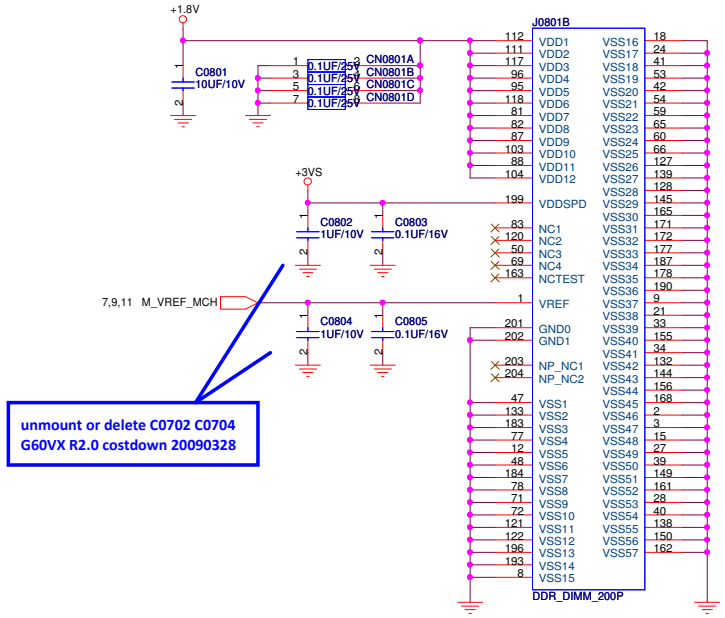
PEGATRON	Title : DIM_So-DIMM 0		
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo		
Size: Custom	Project Name: G60VX		Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 7 of 100		

Reserved for 3G



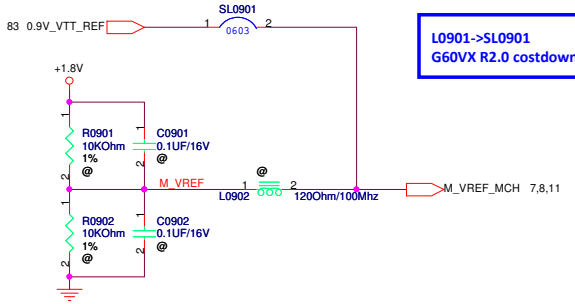
Reverse Type
H = 4.0 mm



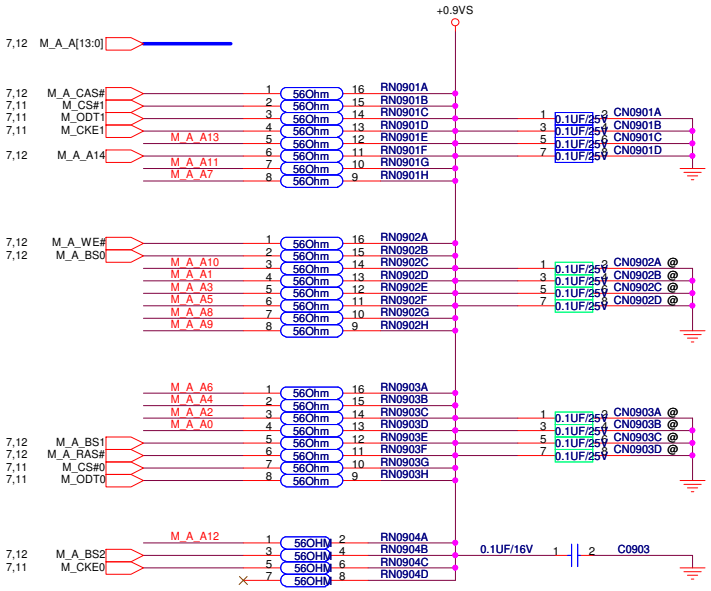


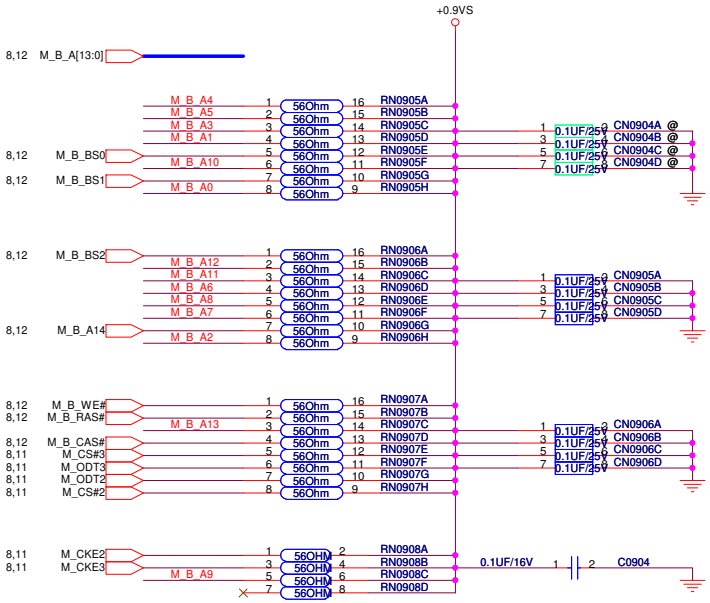
unmount or delete C0702 C0704
G60VX R2.0 costdown 20090328

PEGATRON	Title : DIM_So-DIMM 1		
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo		
Size: Custom	Project Name: G60VX		Rev: R 1.2
Date: Thursday, April 09, 2009	Sheet 8 of 100		



L0901->SL0901
G60VX R2.0 costdown 20090328





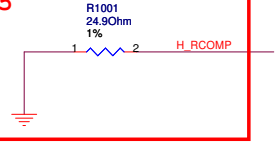
PEGATRON Title : DIM_DDR2 Termination

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

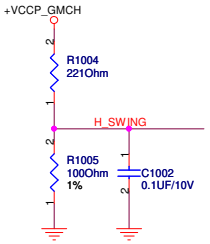
Size	Project Name	Rev
Custom	G60VX	R 1.2

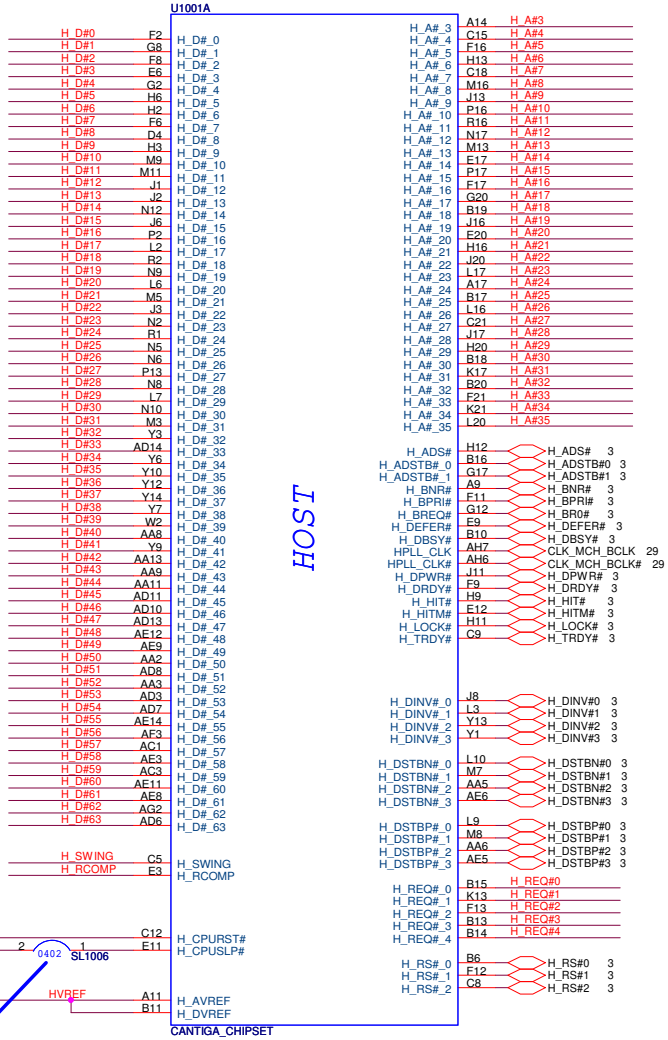
Date: Wednesday, April 08, 2009 Sheet 9 of 100

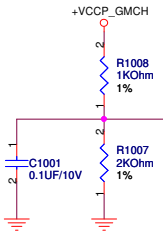
H_RCOMP:
DC: 25 ohm pull down;
QC: 17 ohm pull down
2008-11-19-20-25



H_SWING:
DC: 221 ohm pull up,
100 ohm pull down;
QC: 221 ohm pull up,
75 ohm pull down
2008-11-19-20-27





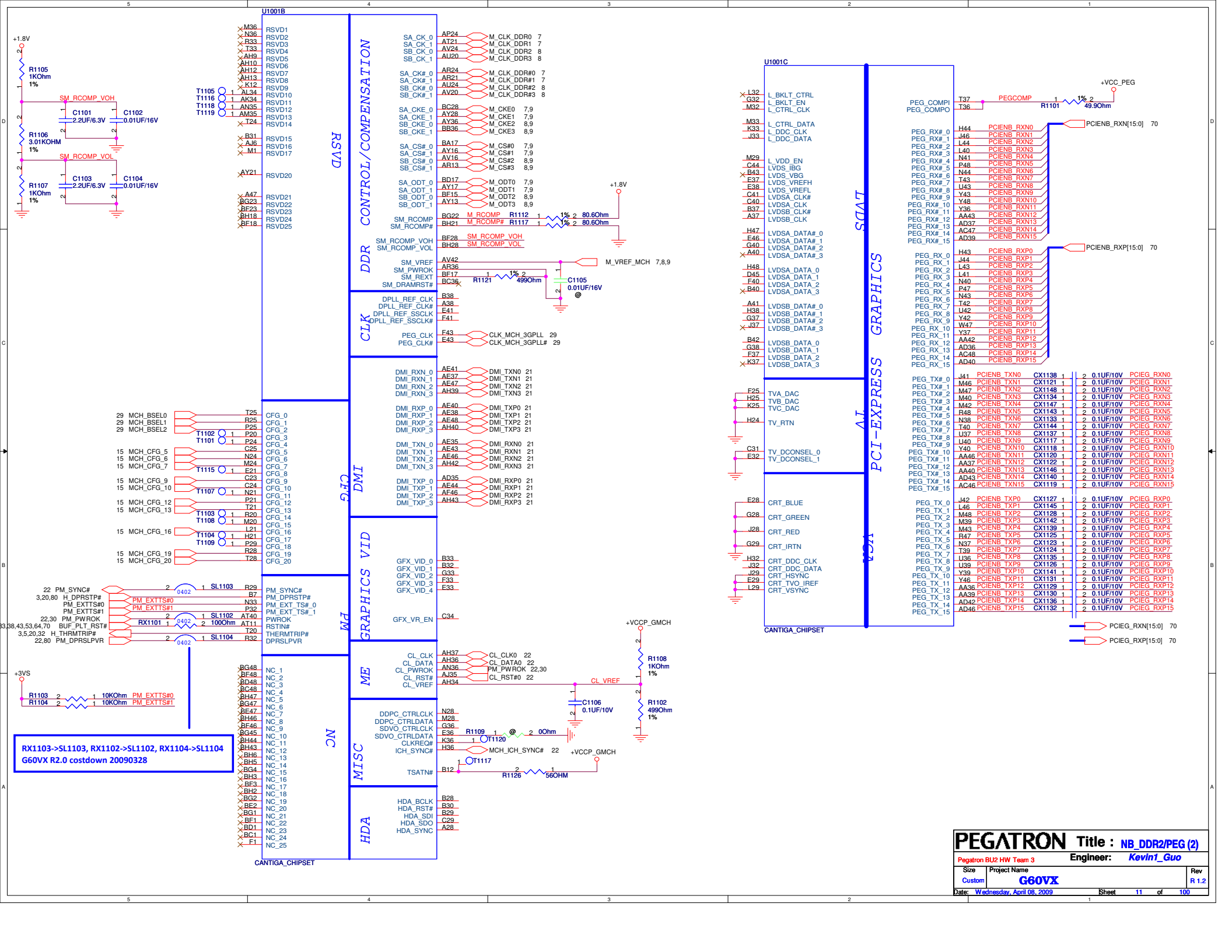


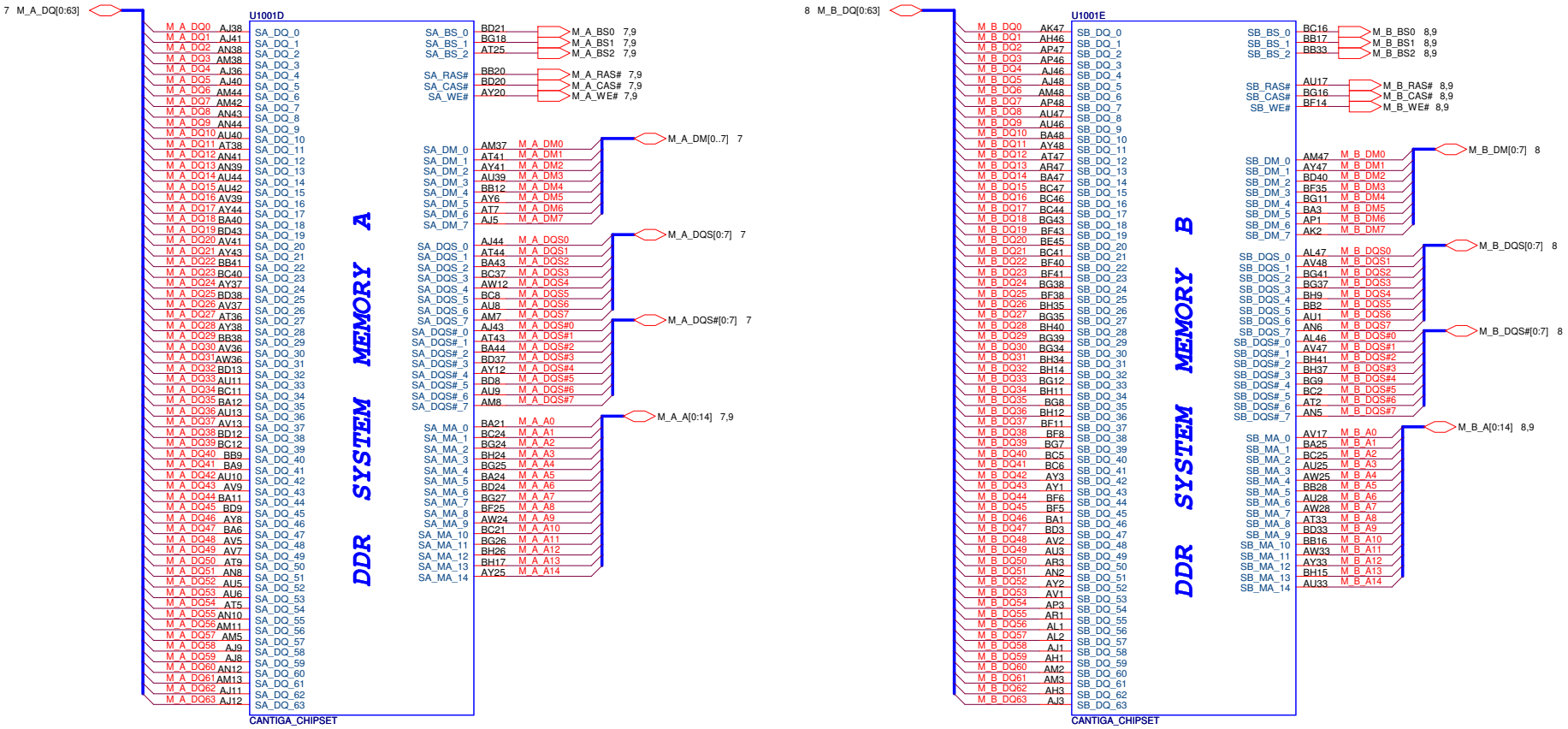
Cap 0.1uF within 100 mils from GMCH

RX1006->SL1006;
G60VX R2.0 costdown 20090405

3 H_A#[35:3] H_A#[35:3]
3 H_REQ#[4:0] H_REQ#[4:0]
3 H_D#[63:0] H_D#[63:0]

PEGATRON Title : NB_CPU (1)
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom | Project Name: G60VX | Rev: R 1.2
Date: Wednesday, April 08, 2009 | Sheet 10 of 100


U1001B
RSVD
CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
VID
GRAPHICS
PM
ME
MISC
NC
HDA
CANTIGA_CHIPSET
U1001C
LVDS
GRAPHICS
PCI-EXPRESS
AI
VGA
CANTIGA_CHIPSET
+1.8V
+3VS
+VCCP_GMCH
+VCC_PEG
SM_RCOMP_VOH
SM_RCOMP_VOL
R1105 1KOhm 1%
R1106 3.01KOHM 1%
R1107 1KOhm 1%
C1101 2.2UF/6.3V
C1102 0.01UF/16V
C1103 2.2UF/6.3V
C1104 0.01UF/16V
R1108 1KOhm 1%
R1102 499Ohm 1%
C1106 0.1UF/10V
R1109 0Ohm
R1126 56OHM
R1112 80.6Ohm
R1117 80.6Ohm
R1121 499Ohm
C1105 0.01UF/16V
R1101 49.9Ohm
PEGCOMP
M_VREF_MCH 7,8,9
CL_VREF
PCIENB_RXN[15:0] 70
PCIENB_RXP[15:0] 70
PCIEG_RXN[15:0] 70
PCIEG_RXP[15:0] 70
RX1103->SL1103, RX1102->SL1102, RX1104->SL1104
G60VX R2.0 costdown 20090328
PEGATRON
Title : NB_DDR2/PEG (2)
Engineer: Kevin1_Guo
Pegatron BU2 HW Team 3
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 11 of 100

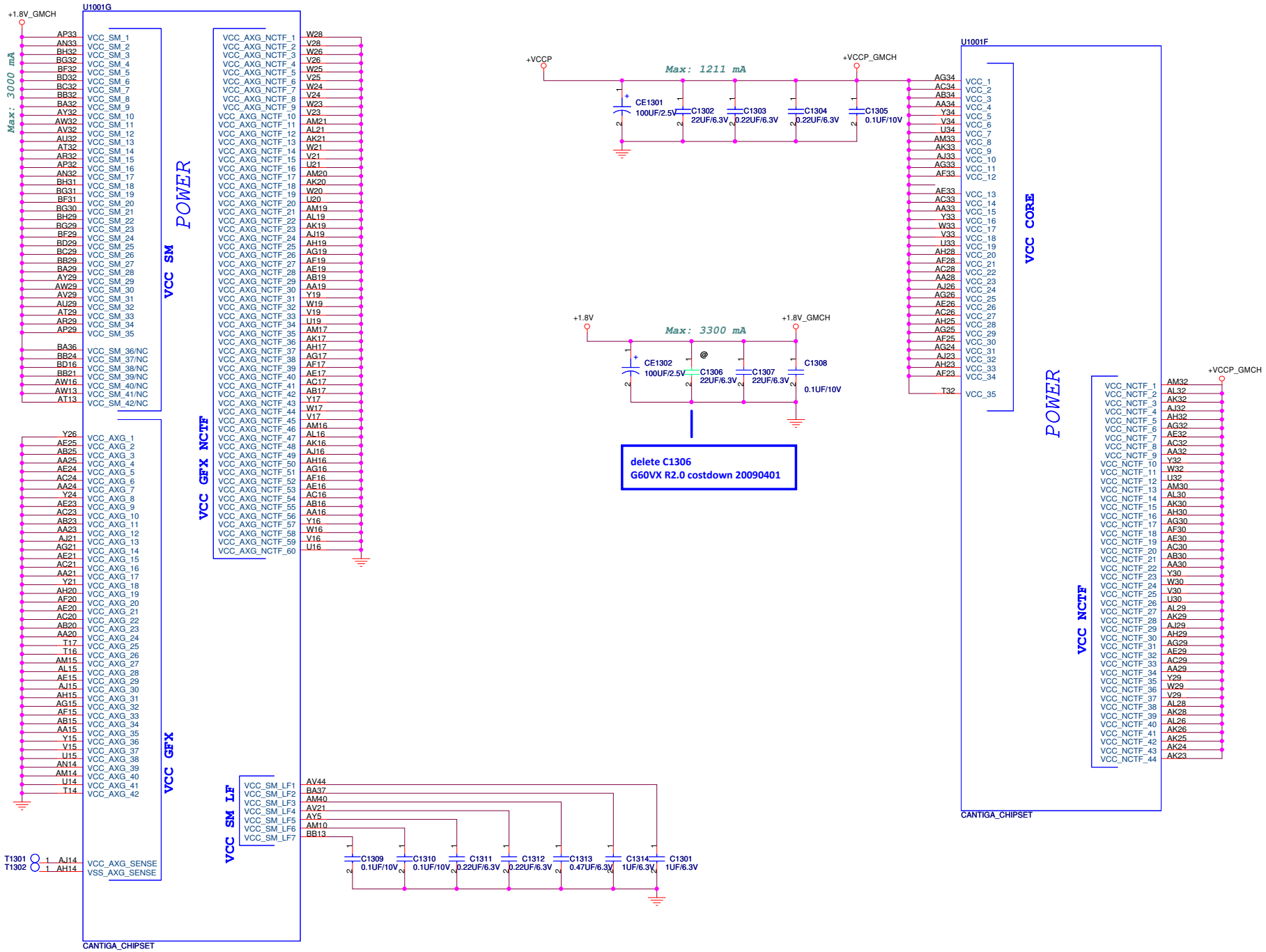


PEGATRON Title : NB_DDR2 bus (3)

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 12 of 100



PEGATRON Title : NB_POWER (4)

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Sunday, April 05, 2009 Sheet 13 of 100

R1415->SL1415;R1416->SL1416
R1406->SL1406;R1408->SL1408
R1410->SL1410; delete R1414
delete CE1407 C1442 C1449
R1405->SL1405->delete SL1405 Height limit;
R1401->SL1401;R1409->SL1409
R1404->SL1404;R1403->SL1403
Delete C1404
G60VX R2.0 costdown 20090401

+VCCP_GMCH
L1403 120Ohm/100Mhz SL1415 0603 +VCCP_PEGPLL
CE1404 10UF/6.3V C1412 0.1UF/10V
L1404 120Ohm/100Mhz +VCCP_HPLL
C1419 0.1UF/10V C1446 4.7UF/6.3V
L1405 120Ohm/100Mhz SL1416 0603 +VCCP_MPLL
C1427 22UF/6.3V C1426 0.1UF/10V

U1001H CANTIGA_CHIPSET

CRT: B27 VCCA_CRT_DAC_1, A26 VCCA_CRT_DAC_2, A25 VCCA_DAC_BG, B25 VSSA_DAC_BG
PLL: F47 VCC_DPLLA, L48 VCC_DPLLB, AD1 VCCA_HPLL (+VCCP_HPLL), AE1 VCCA_MPLL (+VCCP_MPLL) — 24mA / 140mA
A LVDS: J48 VCCA_LVDS, J47 VSSA_LVDS
A PEG: SL1406 0603 +1.5VS, AD48 VCCA_PEG_BG (+VCCA_PEG_GMCH), C1411 0.1UF/10V — 0.414mA; AA48 VCCA_PEG_PLL (+VCCP_PEGPLL) — 50mA
A SM: SL1408 0805 +VCCP_GMCH, +VCCASM_GMCH, CE1407 100UF/2.5V @, C1436 22UF/6.3V, C1445 4.7UF/6.3V, C1415 1UF/6.3V — DDR2: 720mA / DDR3: 748mA; RGB(0,255,128); AR20 VCCA_SM_1, AP20 VCCA_SM_2, AN20 VCCA_SM_3, AR17 VCCA_SM_4, AP17 VCCA_SM_5, AN17 VCCA_SM_6, AT16 VCCA_SM_7, AR16 VCCA_SM_8, AP16 VCCA_SM_9
A CK: SL1410 0805 +VCCP_GMCH, +VCCA_SM_CK, C1448 4.7UF/6.3V, C1438 22UF/6.3V, C1437 0.1UF/10V — DDR2: 26mA / DDR3: 38mA; AP28 VCCA_SM_CK_1, AN28 VCCA_SM_CK_2, AP25 VCCA_SM_CK_3, AN25 VCCA_SM_CK_4, AN24 VCCA_SM_CK_5, AM28 VCCA_SM_CK_NCTF_1, AM26 VCCA_SM_CK_NCTF_2, AM25 VCCA_SM_CK_NCTF_3, AL25 VCCA_SM_CK_NCTF_4, AM24 VCCA_SM_CK_NCTF_5, AL24 VCCA_SM_CK_NCTF_6, AM23 VCCA_SM_CK_NCTF_7, AL23 VCCA_SM_CK_NCTF_8
TV: B24 VCCA_TV_DAC_1, A24 VCCA_TV_DAC_2
HDA: A32 VCC_HDA
D TV/CRT: M25 VCCD_TVDAC, L28 VCCD_QDAC, AF1 VCCD_HPLL, AA47 VCCD_PEG_PLL
LVDS: M38 VCCD_LVDS_1, L37 VCCD_LVDS_2

POWER

+1.5VS L1406 120Ohm/100Mhz C1451 0.01UF/16V C1443 0.1UF/10V
Connect VCCD_TVDAC to GND, maintain VCCD_QDAC follow intel DG R2.2
G60VX R2.0 costdown 20090401
+VCCP_GMCH 158mA C1440 0.1UF/10V
+VCCP_PEGPLL C1441 0.1UF/10V

VTT: VTT_1 U13, VTT_2 T13, VTT_3 U12, VTT_4 T12, VTT_5 U11, VTT_6 T11, VTT_7 U10, VTT_8 T10, VTT_9 U9, VTT_10 T9, VTT_11 U8, VTT_12 T8, VTT_13 U7, VTT_14 T7, VTT_15 U6, VTT_16 T6, VTT_17 U5, VTT_18 T5, VTT_19 V3, VTT_20 U3, VTT_21 V2, VTT_22 U2, VTT_23 T2, VTT_24 V1, VTT_25 U1
+VCCP_GMCH_VTT — 852mA — C1450 4.7UF/6.3V, C1463 4.7UF/6.3V, C1404 0.47UF/6.3V @, SL1403 0805, CE1401 100UF/2.5V, +VCCP_GMCH

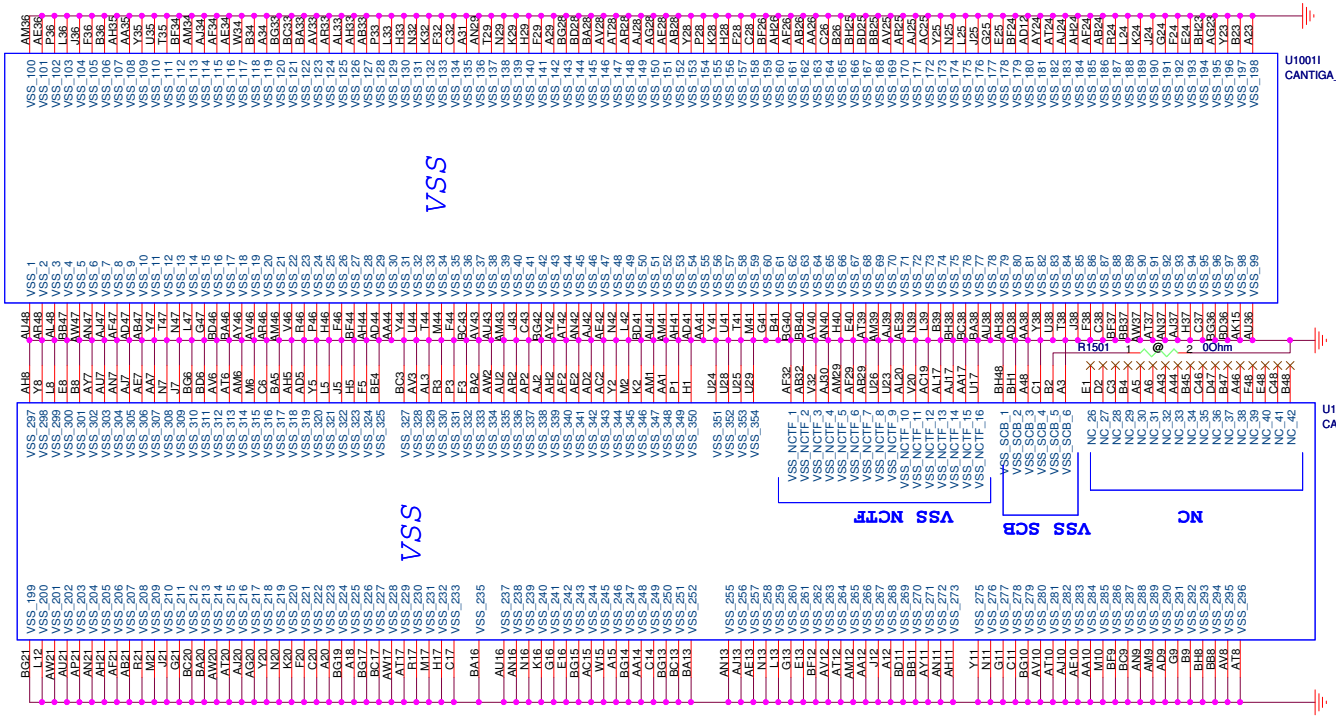
AXF: VCC_AXF_1 B22, VCC_AXF_2 B21, VCC_AXF_3 A21
+VCCAXF_GMCH — 322mA — C1406 1UF/6.3V, C1405 10UF/6.3V @, SL1404 0805, +VCCP_GMCH

SM CK: VCC_SM_CK_1 BF21, VCC_SM_CK_2 BH20, VCC_SM_CK_3 BG20, VCC_SM_CK_4 BF20
L1409 120Ohm/100Mhz +1.8V_GMCH — DDR2: 124mA / DDR3: 150mA
SL1409 0603, C1416 0.1UF/10V, C1418 10UF/6.3V
+VCCP_GMCH, D1401 BAT54C, R1402 10Ohm 1%, +3VS
106mA — SL1401 0603, +3VS_HV, C1417 0.1UF/10V

HV: VCC_TX_LVDS K47, VCC_HV_1 C35, VCC_HV_2 B35, VCC_HV_3 A35 — Max:106 mA
PEG: VCC_PEG_1 V48, VCC_PEG_2 U48, VCC_PEG_3 V47, VCC_PEG_4 U47, VCC_PEG_5 U46 — Max: 1782 mA
+VCC_PEG, R1.1, 0Ohm R1407, C1447 4.7UF/6.3V, C1444 22UF/6.3V, CE1406 100UF/2.5V, +VCCP_GMCH
DMI: VCC_DMI_1 AH48, VCC_DMI_2 AF48, VCC_DMI_3 AH47, VCC_DMI_4 AG47 — Max: 456 mA
+VCC_DMI, C1421 0.1UF/10V, +VCC_PEG
VTTLF: VTTLF1 A8, VTTLF2 L1, VTTLF3 AB2
C1433 0.47UF/6.3V, C1434 0.47UF/6.3V, C1435 0.47UF/6.3V

Change C1447 from 4.7UF/6.3V 0805 to 4.7UF/6.3V 0603 to satisfy the mechinal height strain
2008-11-26-14-22

PEGATRON Title : NB_POWER (5)
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom | Project Name: G60VX | Rev: R 1.2
Date: Wednesday, April 08, 2009 | Sheet 14 of 100



11 MCH_CFG_5

R1509 2.21KOhm @

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

11 MCH_CFG_6

R1514 2.21KOhm @

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

11 MCH_CFG_7

R1511 2.21KOhm @

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

11 MCH_CFG_9

R1512 2.21KOhm @

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

11 MCH_CFG_16

R1507 2.21KOhm @

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

11 MCH_CFG_10

R1508 2.21KOhm @

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

11 MCH_CFG_12

R1513 2.21KOhm @

11 MCH_CFG_13

R1510 2.21KOhm @

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

+3VS

R1503 4.02KOHM @

11 MCH_CFG_19

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

+3VS

R1506 4.02KOHM @

11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

PEGATRON Title : NB_GND/Strapping (6)

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 15 of 100

PEGATRON Title : NB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 16 of 100

Main Board

PEGATRON Title : NB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 17 of 100

Main Board

PEGATRON Title : NB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 18 of 100

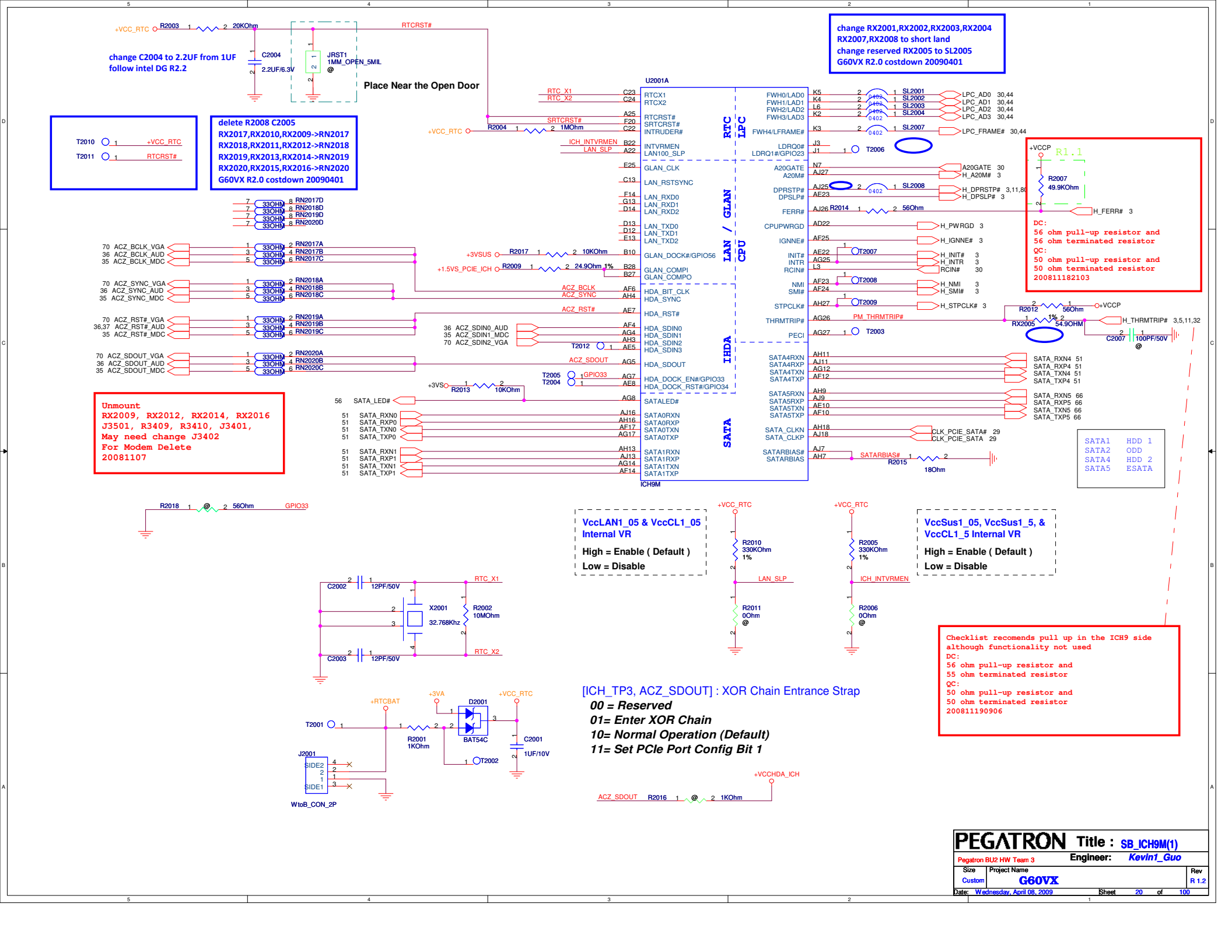
Main Board

PEGATRON Title : MEM_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 19 of 100


change C2004 to 2.2UF from 1UF
follow intel DG R2.2
Place Near the Open Door
change RX2001,RX2002,RX2003,RX2004
RX2007,RX2008 to short land
change reserved RX2005 to SL2005
G60VX R2.0 costdown 20090401
delete R2008 C2005
RX2017,RX2010,RX2009->RN2017
RX2018,RX2011,RX2012->RN2018
RX2019,RX2013,RX2014->RN2019
RX2020,RX2015,RX2016->RN2020
G60VX R2.0 costdown 20090401
Unmount
RX2009, RX2012, RX2014, RX2016
J3501, R3409, R3410, J3401,
May need change J3402
For Modem Delete
20081107
U2001A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
DC:
56 ohm pull-up resistor and
56 ohm terminated resistor
QC:
50 ohm pull-up resistor and
50 ohm terminated resistor
200811182103
SATA1 HDD 1
SATA2 ODD
SATA4 HDD 2
SATA5 ESATA
VccLAN1_05 & VccCL1_05
Internal VR
High = Enable (Default)
Low = Disable
VccSus1_05, VccSus1_5, &
VccCL1_5 Internal VR
High = Enable (Default)
Low = Disable
Checklist recomends pull up in the ICH9 side
although functionality not used
DC:
56 ohm pull-up resistor and
55 ohm terminated resistor
QC:
50 ohm pull-up resistor and
50 ohm terminated resistor
200811190906
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
WtoB_CON_2P
PEGATRON
Title : SB_ICH9M(1)
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 20 of 100

PCIE1 Robson/TV Tuner
PCIE2 MiniCard
PCIE3 NewCard
PCIE4 NC
PCIE5 SATA RAID
PCIE6 LAN

U2001B
PCI
Interrupt I/F
ICH9M

U2001D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M

SPI_MOSI
iTPM Enable
High = Enable
Low = Disable(Default)

Swap USB port 4 and port 8
G50VX R1.1 20090108

Delete the OLED connector,
Add TP to USBP9N/P
2008-11-25-15-05

Place within 500 mils of ICH

L<500mils
Place within 500 mils of ICH

USB0 External Port 1
USB1 External Port 2
USB2 External Port 3
USB3 External Port 4
USB4 CMOS Camera
USB5 External Port 5
USB6 OLED
USB7 WiMax
USB8 Newcard
USB9 TV-Tuner
USB10 Blue-Tooth
USB11 Finger Printer

ICH9 Boot BIOS select

		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

U2101
NC7SZ08P5X_NL
U2102
NC7SZ08P5X_NL
SL2111

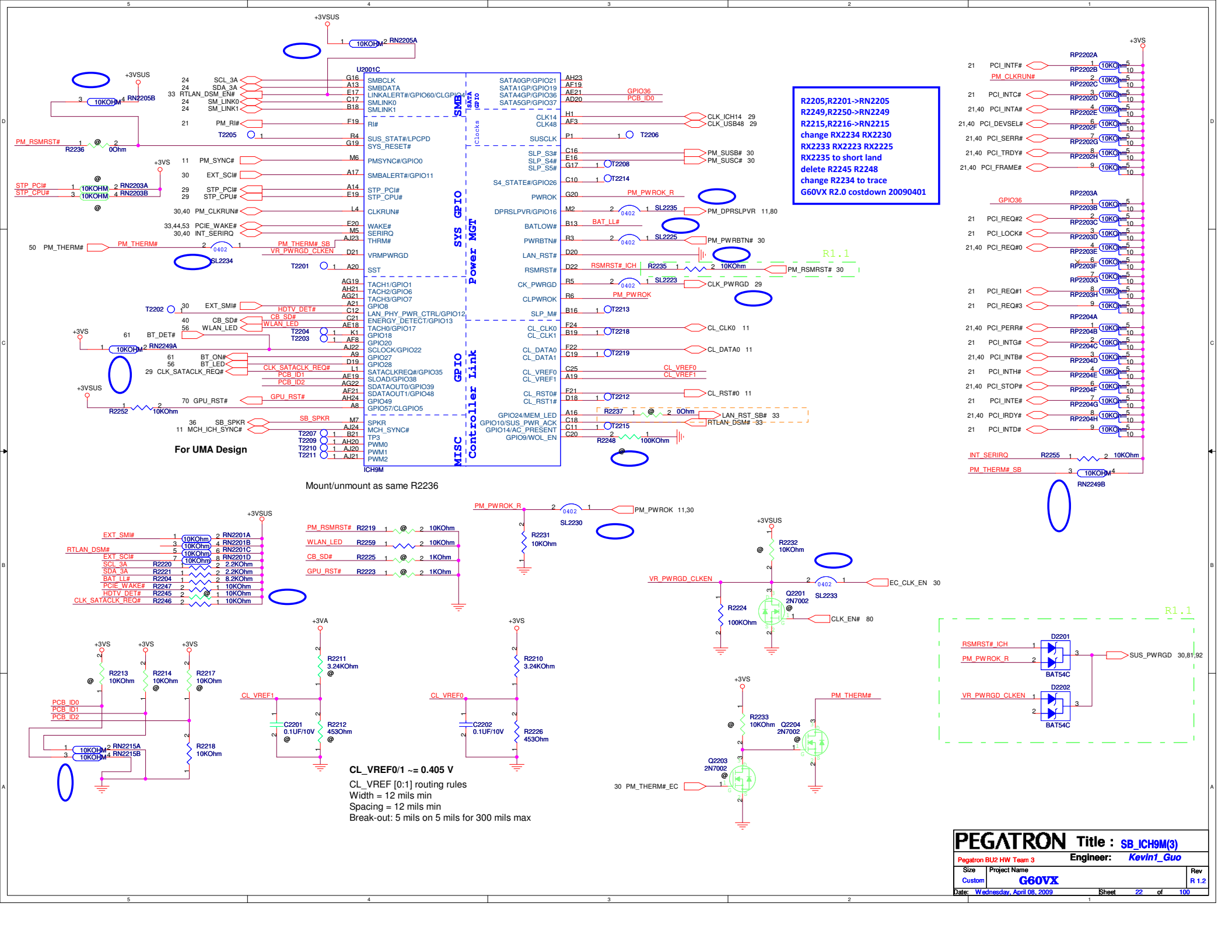
change R2111 to short land
G60VX R2.0 costdown 20090401

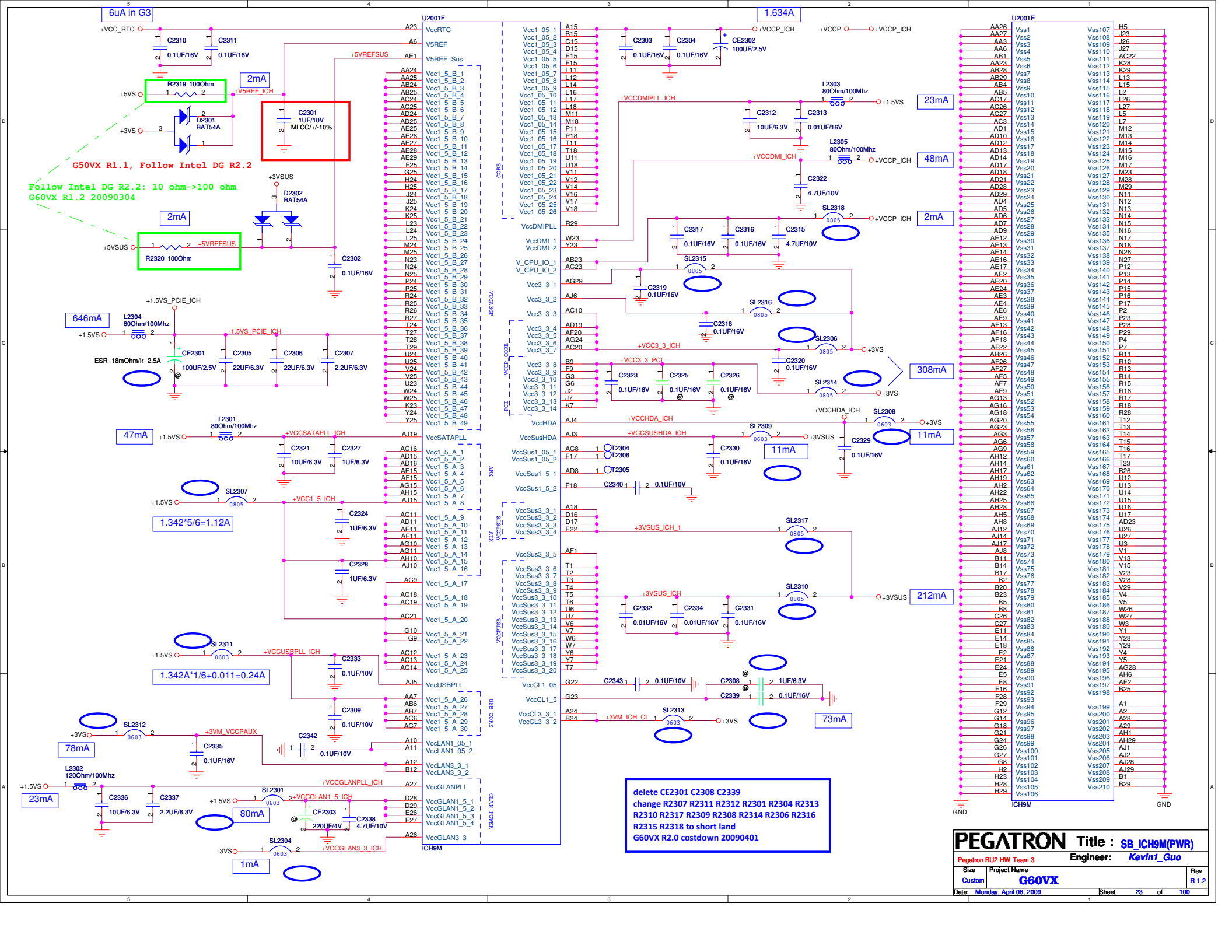
Reserved

When supporting CLK GEN Turbo PIN, UNI R2107.

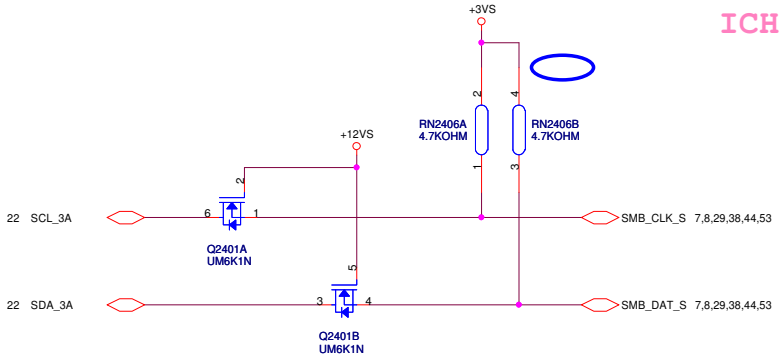
Mount R2107, R2108 in G50V

PEGATRON Title : SB_ICH9M(2)
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom Project Name: G60VX Rev: R 1.2
Date: Wednesday, April 08, 2009 Sheet 21 of 100

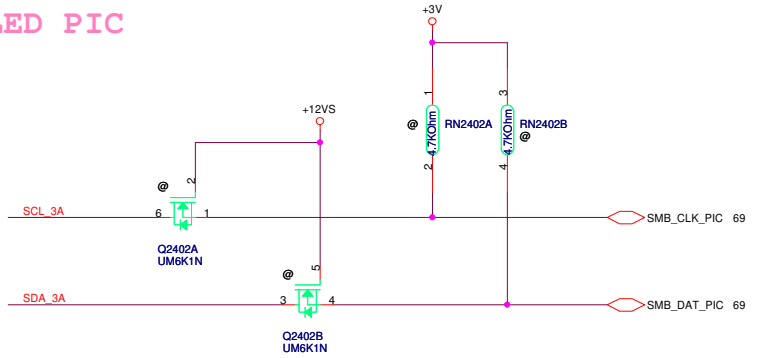

U2001C
ICH9M
SMB
GPIO
CLOCKS
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
R2205,R2201->RN2205
R2249,R2250->RN2249
R2215,R2216->RN2215
change RX2234 RX2230
RX2233 RX2223 RX2225
RX2235 to short land
delete R2245 R2248
change R2234 to trace
G60VX R2.0 costdown 20090401
R1.1
For UMA Design
Mount/unmount as same R2236
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
PEGATRON
Title : SB_ICH9M(3)
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 22 of 100

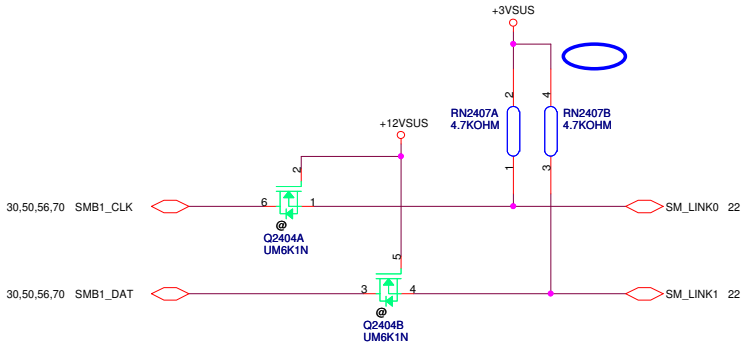

6uA in G3
2mA
G50VX R1.1, Follow Intel DG R2.2
Follow Intel DG R2.2: 10 ohm->100 ohm
G60VX R1.2 20090304
2mA
646mA
47mA
1.342*5/6=1.12A
1.342A*1/6+0.011=0.24A
78mA
23mA
80mA
1mA
1.634A
23mA
48mA
2mA
308mA
11mA
11mA
212mA
73mA
U2001F
ICH9M
U2001E
ICH9M
delete CE2301 C2308 C2339
change R2307 R2311 R2312 R2301 R2304 R2313
R2310 R2317 R2309 R2308 R2314 R2306 R2316
R2315 R2318 to short land
G60VX R2.0 costdown 20090401
PEGATRON
Title : SB_ICH9M(PWR)
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size Custom
Project Name G60VX
Rev R 1.2
Date: Monday, April 06, 2009
Sheet 23 of 100

ICH9-M



LED PIC





delete R2406 R2405; add RN2406
delete R2407 R2408; add RN2407
G60VX R2.0 costdown 20090401

PEGATRON	Title : SB_ICH9M-Other	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Thursday, April 02, 2009	Sheet 24 of 100	

Main Board

PEGATRON Title : SB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 25 of 100

Main Board

PEGATRON Title : SB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 26 of 100

Main Board

PEGATRON Title : SB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 27 of 100

Main Board

PEGATRON Title : SB_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 28 of 100

Main Board

unmount C2925,C2926 C2922
change R2901 to short land
G60VX R2.0 costdown 20090401

Latched Input Select

0 : Pin 17/18 = LCD_SSCG
1 : Pin 17/18 = PCIe_L0
33PCI3 R2907 10KOhm

0 : Pin 43/44 = SRC CLK
1 : Pin 43/44 = CPU_ITP CLK
33PCIF4 R2908 10KOhm

0 : Pin 14/15 = PCIe_L9
Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
Pin 17/18 = LCD_SSCG/PCIe_L0
33PCIF5 R2940 10KOhm, R2910 10KOhm

0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#
33PCI0 R2928 10KOhm, R2911 10KOhm

PEREQ1#:
PEREQ1# R2922 10KOhm

PEREQ2#:
PEREQ2# R2923 10KOhm

PEREQ3# : PCIEX2/4
PEREQ4# : PCIEX3/5/7

These two pins need to be latched in to select the source of PCICLKs and PCIECLKs:
high = SATA PLL
low = PCIEX PLL

For 364 Over-clocking
33PCI1 R2932 10KOhm, R2929 10KOhm
REF0 R2931 10KOhm, R2930 10KOhm

R1.2

Reserved for R1.0 Debug

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

U2901 ICS9LPR363DGLF-T

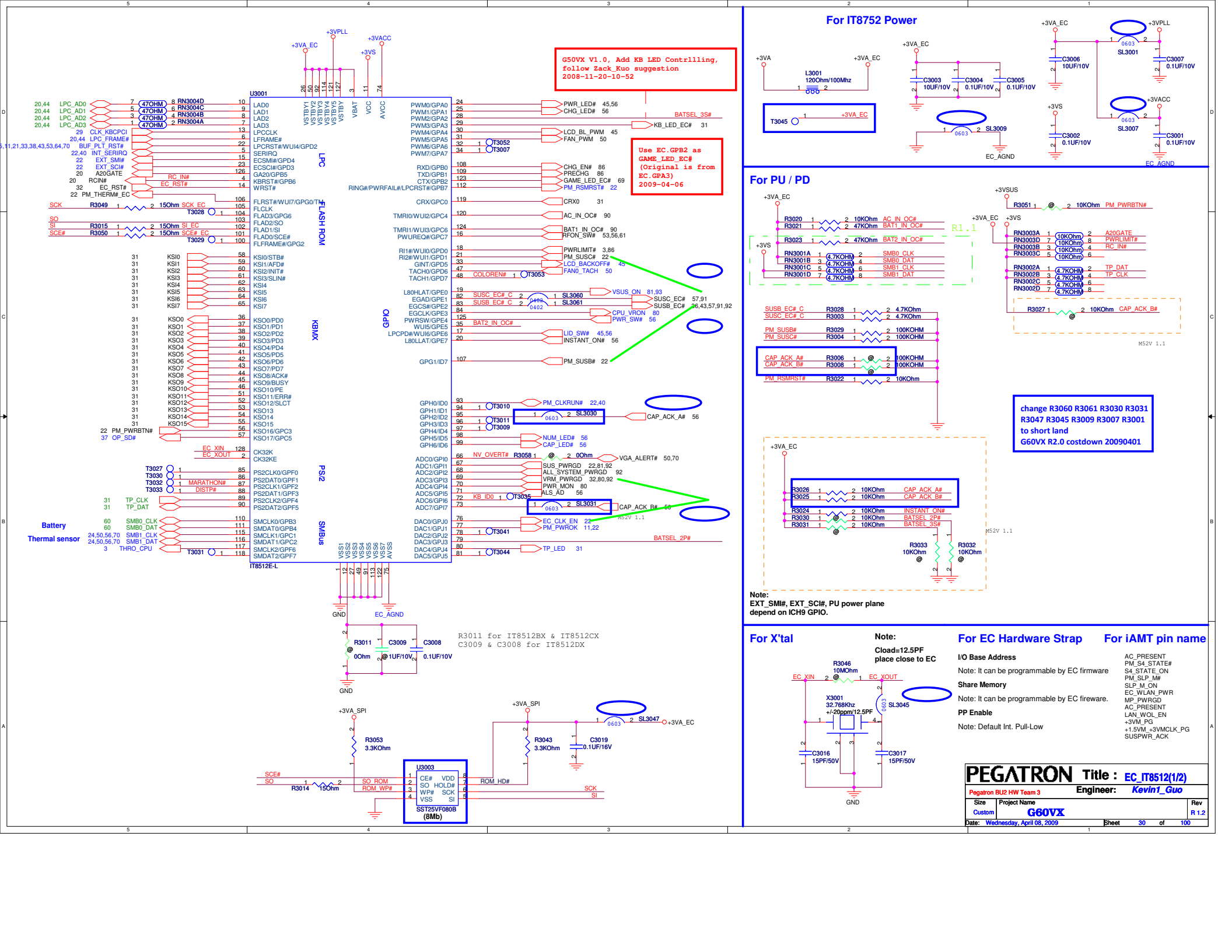
RX2901 RX2902->RN2901
RX2912 RX2913->RN2912
RX2914 RX2915->RN2914
RX2916 RX2917->RN2916
RX2918 RX2919->RN2918
RX2920 RX2921->RN2920
RX2922 RX2923->RN2922
RX2926 RX2927->RN2926
RX2924 RX2925->RN2924
RX2934 RX2933->RN2934
RX2928 RX2929->RN2928
R2918 R2919->short land

For 364 No Turbo Mount R2935, R2931 R2932, R2910, R2928, R2107, R2108
Unmount R2924, R2925, R2903, R2904 R2933, R2934, D2901, R2929, R2930 R2940, R2911
If 364 Turbo Mount R2904, R2925 based on above 200812141050

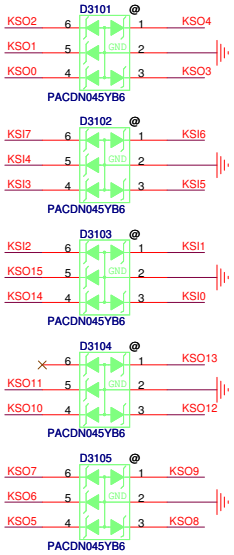
For 363: Mount: R2903, R2904 R2929, R2930, R2935, R2928
Unmount: R2924, R2925, R2934, R2933 D2901, R2931, R2932, R2940, R2911
2008-11-24-16-46

	R2903	R2904	R2925
363:VREF	1K	330	@
364:TURBO	@	10K	0
364:NO TURBO	@	@	@

PEGATRON Title : CLK_ICS9LPR363
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom Project Name: G60VX Rev: R 1.2
Date: Wednesday, April 08, 2009 Sheet 29 of 100

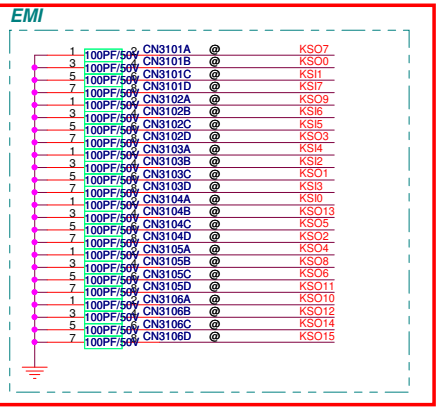

G50VX V1.0, Add KB LED Contrllling, follow Zack_Kuo suggestion 2008-11-20-10-52
Use EC.GPB2 as GAME_LED_EC# (Original is from EC.GPA3) 2009-04-06
U3001
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX
U3003
SST25VF080B (8Mb)
Battery
Thermal sensor
For IT8752 Power
For PU / PD
change R3060 R3061 R3030 R3031 R3047 R3045 R3009 R3007 R3001 to short land G60VX R2.0 costdown 20090401
Note: EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.
For X'tal
Note: Cload=12.5PF place close to EC
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC firmware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
PEGATRON
Title : EC_IT8512(1/2)
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 30 of 100

Main Board

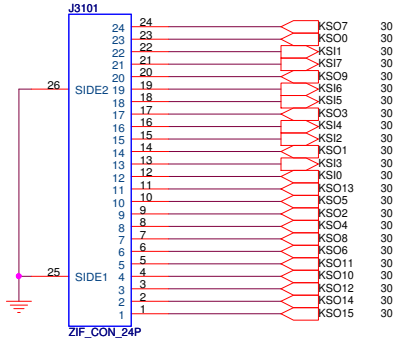


G50VX R1.1 Change back
20090113

EMI

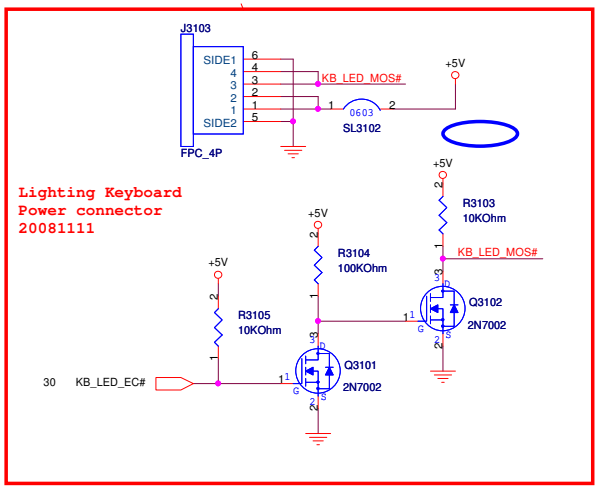


Keyboard



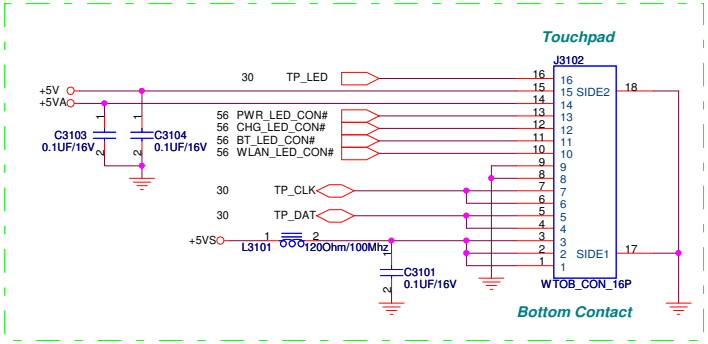
FPC_4P Reference P/N
12G183100402

change R3102 to 0603 short land
G60VX R2.0 costdown 20090401



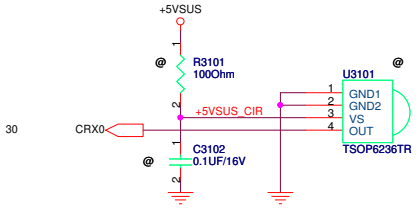
R1.1

Touchpad



Bottom Contact

CIR



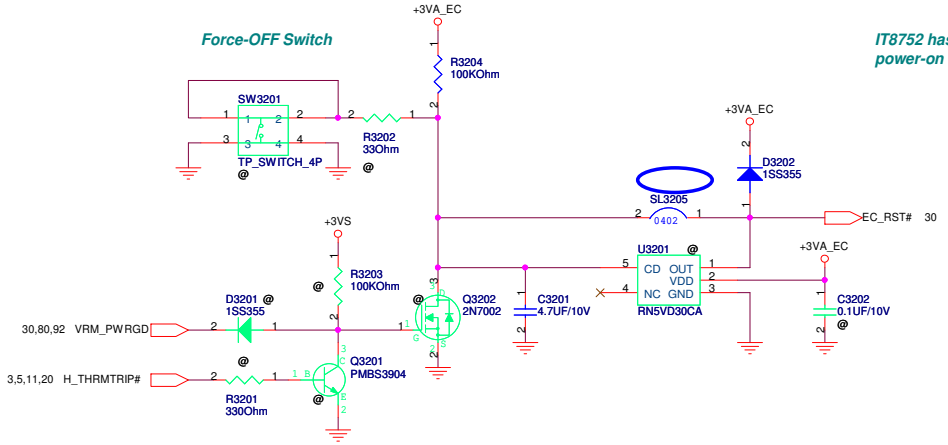
Unmount U3101
R3101, C3102 For
delete CIR
20081107

PEGATRON	Title : EC_IT8512(2/2)KB, TP & C	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 31 of 100	

unmount SW3201 D3201 R3201 R3202 R3203 Q3201 Q3202
change R3205 to short land
G60VX R2.0 costdown 20090401

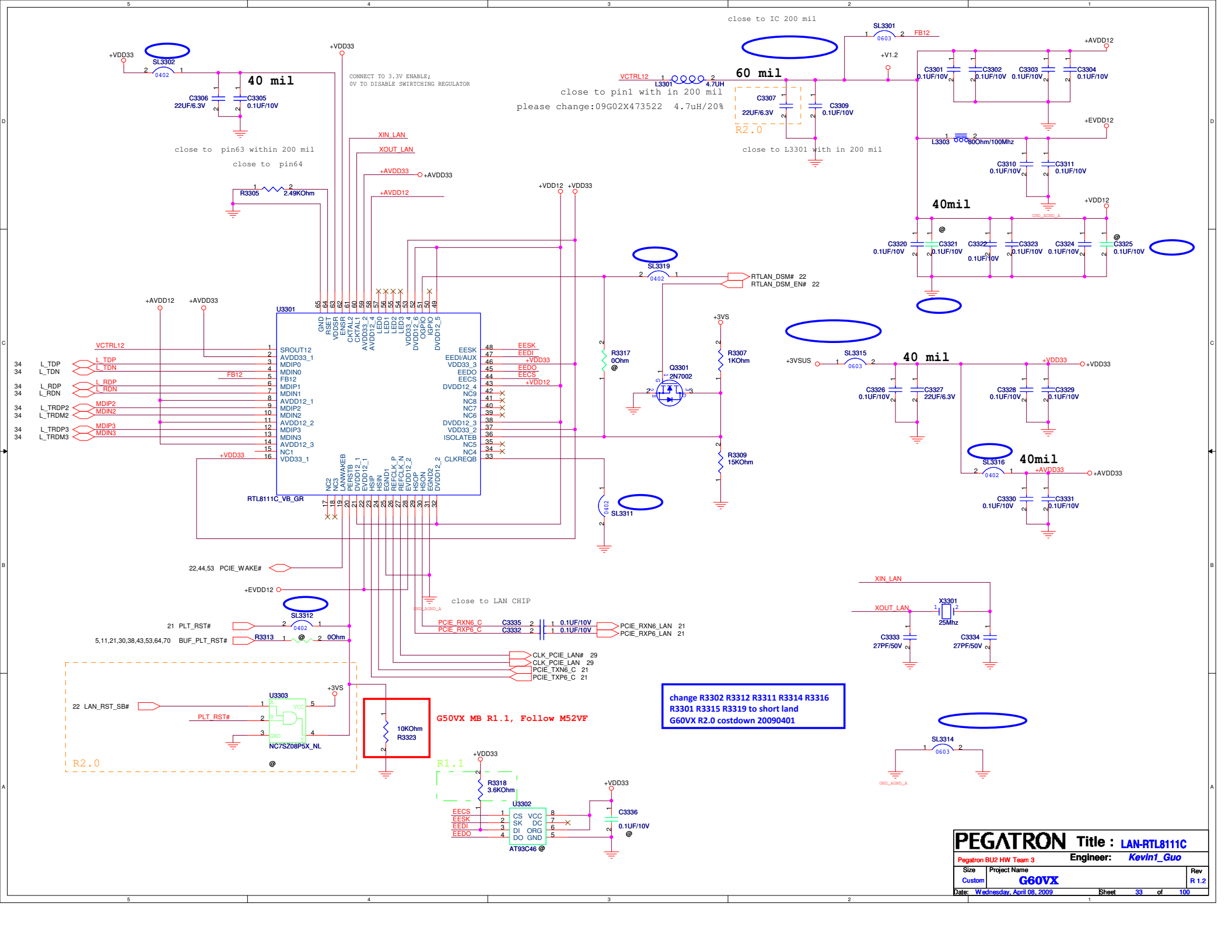
Force-OFF Switch

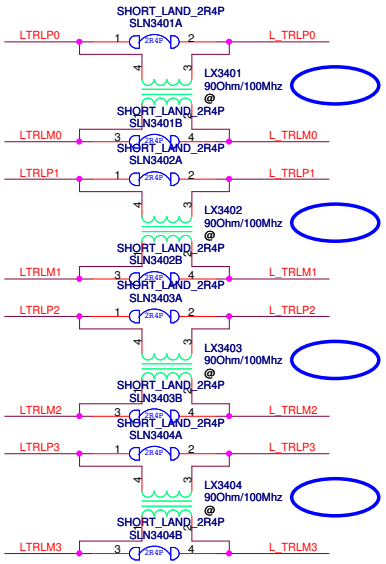
IT8752 has built-in level detection for power-on reset circuit

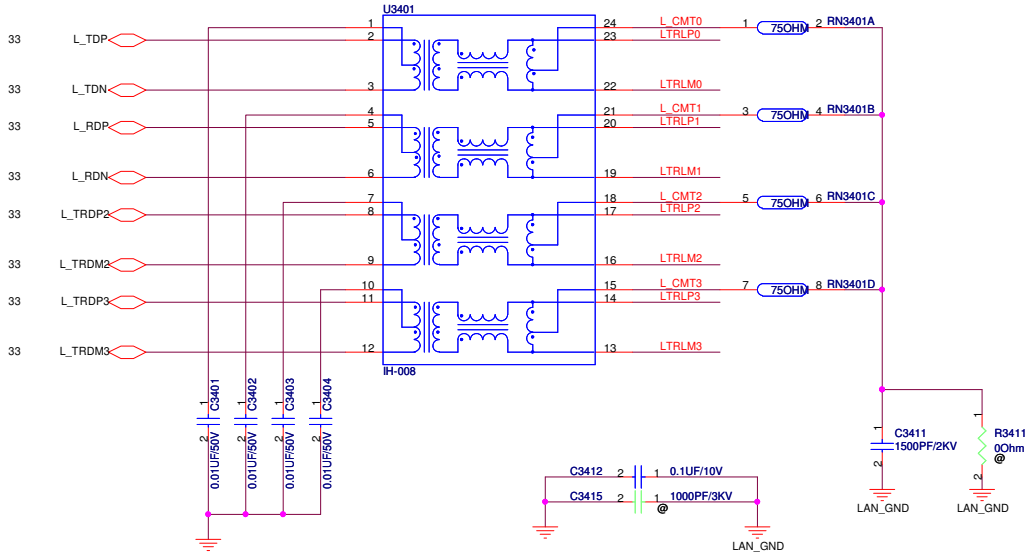


Reserve this part for protection
G60VX R1.2 20090305

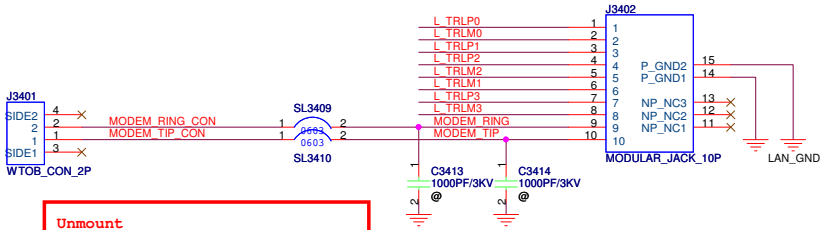
PEGATRON	Title : RST_Reset Circuit	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 32 of 100	


close to IC 200 mil
SL3301
0603
FB12
+V1.2
+AVDD12
VCTRL12
L3301
4.7UH
60 mil
close to pin1 with in 200 mil
please change:09G02X473522 4.7uH/20%
C3307
22UF/6.3V
R2.0
C3309
0.1UF/10V
close to L3301 with in 200 mil
C3301 0.1UF/10V
C3302 0.1UF/10V
C3303 0.1UF/10V
C3304 0.1UF/10V
+EVDD12
L3303
80Ohm/100Mhz
C3310 0.1UF/10V
C3311 0.1UF/10V
40mil
+VDD12
GND_AGND_A
C3320 0.1UF/10V
C3321 0.1UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
+VDD33
SL3302
0402
40 mil
C3306 22UF/6.3V
C3305 0.1UF/10V
CONNECT TO 3.3V ENABLE;
0V TO DISABLE SWIRTCHING REGULATOR
close to pin63 within 200 mil
close to pin64
XIN_LAN
XOUT_LAN
+AVDD33
+AVDD12
R3305
2.49KOhm
U3301
RTL8111C_VB_GR
SL3319
RTLAN_DSM# 22
RTLAN_DSM_EN# 22
R3317
0Ohm
Q3301
2N7002
R3307
1KOhm
R3309
15KOhm
SL3311
+3VS
+3VSUS
SL3315
40 mil
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 0.1UF/10V
C3329 0.1UF/10V
SL3316
40mil
C3330 0.1UF/10V
C3331 0.1UF/10V
VCTRL12
L_TDP
L_TDN
L_RDP
L_RDN
MDIP2
MDIN2
MDIP3
MDIN3
FB12
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
22,44,53 PCIE_WAKE#
+EVDD12
SL3312
21 PLT_RST#
5,11,21,30,38,43,53,64,70 BUF_PLT_RST#
R3313
@
0Ohm
close to LAN CHIP
PCIE_RXN6_C
PCIE_RXP6_C
C3335
C3332
0.1UF/10V
PCIE_RXN6_LAN 21
PCIE_RXP6_LAN 21
CLK_PCIE_LAN# 29
CLK_PCIE_LAN 29
PCIE_TXN6_C 21
PCIE_TXP6_C 21
XIN_LAN
XOUT_LAN
X3301
25Mhz
C3333 27PF/50V
C3334 27PF/50V
U3303
NC7SZ08P5X_NL
22 LAN_RST_SB#
PLT_RST#
10KOhm
R3323
G50VX MB R1.1, Follow M52VF
change R3302 R3312 R3311 R3314 R3316
R3301 R3315 R3319 to short land
G60VX R2.0 costdown 20090401
SL3314
0603
R1.1
R3318
3.6KOhm
U3302
AT93C46 @
C3336
0.1UF/10V
@
EECS
EESK
EEDI
EEDO
PEGATRON
Title : LAN-RTL8111C
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size
Custom
Project Name
G60VX
Rev
R 1.2
Date: Wednesday, April 08, 2009
Sheet 33 of 100





change RNX3401 RNX3402 RNX3403 RNX3404
to integrated short land;
change R3409 R3410 to short land
G60VX R2.0 costdown 20090402



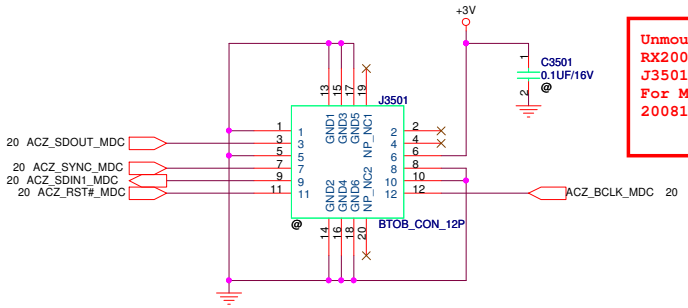
Unmount
RX2009, RX2012, RX2014, RX2016
J3501, R3409, R3410, J3401,
20081107

PEGATRON Title : LAN_RJ45 & RJ11

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 34 of 100



Unmount
RX2009, RX2012, RX2014, RX2016
J3501, R3409, R3410, J3401,
For Modem Delete
20081107

PEGATRON Title : LAN_MDC

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 35 of 100

If ALC662
Mount C3625, C3626, R3620, R3608, C3615, Q3702, CE3701, CE3702
Unmount R3611, R3612, R3621, C3636, C3638, R3618, R3705, R3706
If ALC663
Mount R3611, R3612, R3621, C3636, C3638, R3618, R3705, R3706
Unmount C3625, C3626, R3620, R3608, C3615, Q3702, CE3701, CE3702

change R3619 R3621 R3602
R3624 R3601 R3616 to short land;
change L3601 to short land;
unmount C3601 C3605 C3609;
G60VX R2.0 costdown 20090402

Audio Power

FOR ADJUST MODE:

Vo=1.25*(1+R3706/R3705)

=1.25*(1+ 100K/34.8K) = 4.84

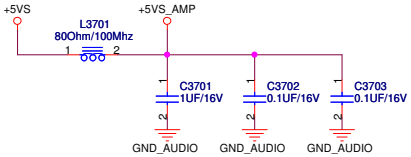
G50VX MB R1.1, Follow M52VF R2.0

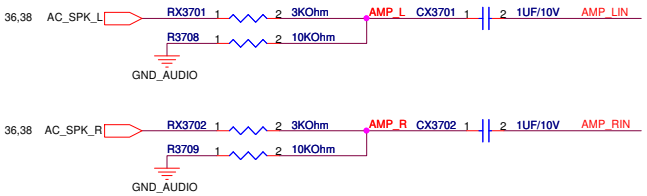
Input impedence:64K ohm(Typical)

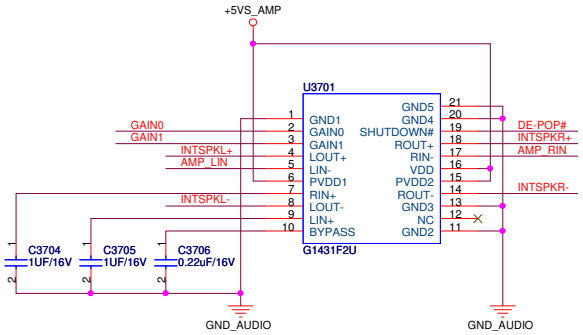
Try 0 ohm

PC BEEP

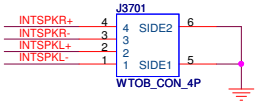
PEGATRON	Title : CODEC-ALC663
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo
Size: Custom	Project Name: G60VX
Rev: R 1.2	
Date: Wednesday, April 08, 2009	Sheet 36 of 100



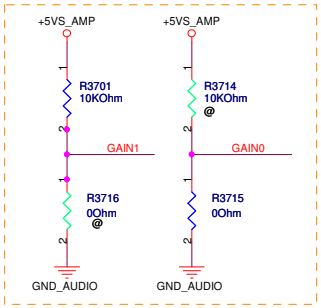




Internal Speaker Conn.

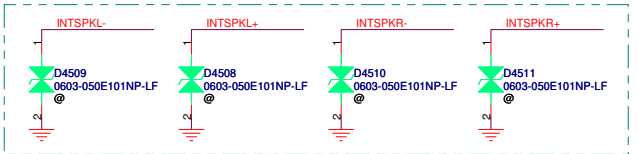


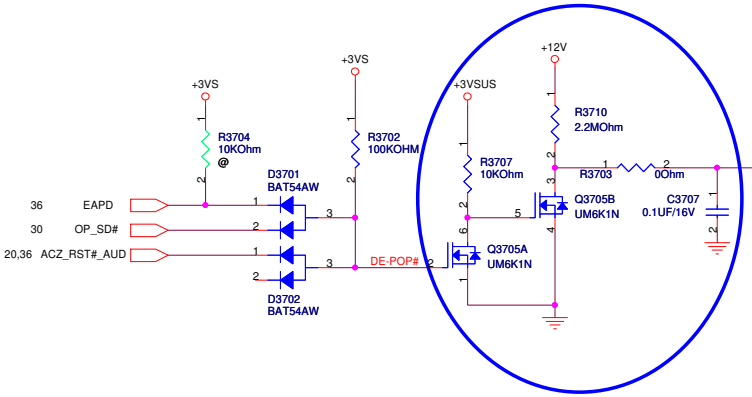
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

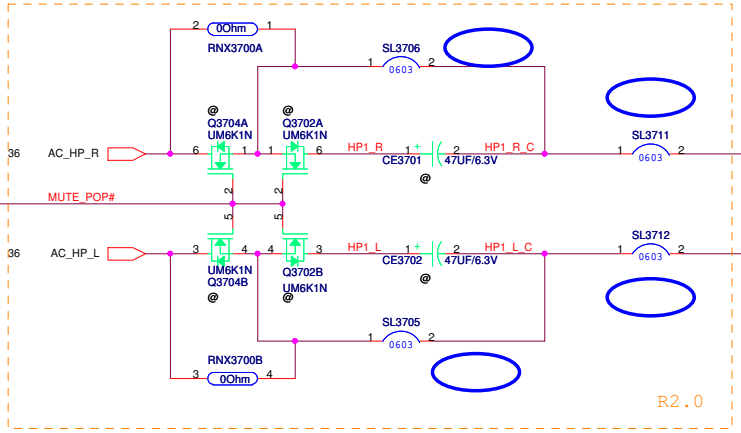


R2.0

Reserved for EMI



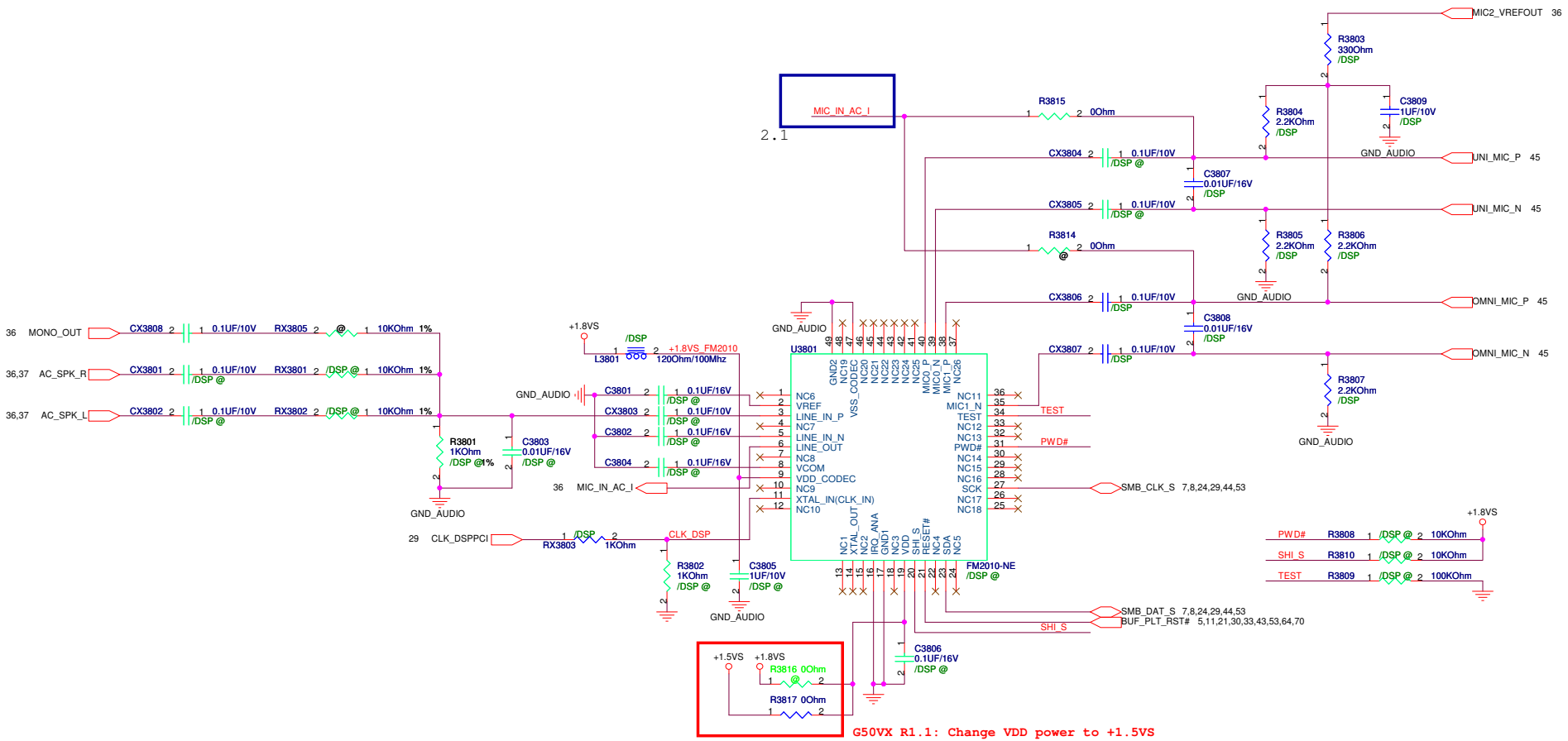




R2.0

unmount R3707 Q3705 R3710 R3703 C3707
change R3706 R3705 R3711 R3712 to short land
add SL3700 SL3701
G60VX R2.0 costdown 20090402

PEGATRON	Title : AUD_Amp & Jack	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 37 of 100	



Mount R4507, R508, R4509, R4510
U3801, R3803, C3809, R3804, CX3804, C3807, CX3805,
R3805, R3806, CX3806, CX3807, C3808, R3807
R3808, R3810, R3809, C3806, C3805, R3802, RX3803
C3804, C3802, CX3803, C3801, L3801, C3803, R3801
RX3801, RX3802, CX3801, CX3802

Unmount R3815, R3814, CX3808, RX3805
For supporting Array Mic
20081107

G50VX R1.1: Change VDD power to +1.5VS
to decrease the digital noise and for
less power consumption

PEGATRON Title : AUD_FM2010

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 38 of 100

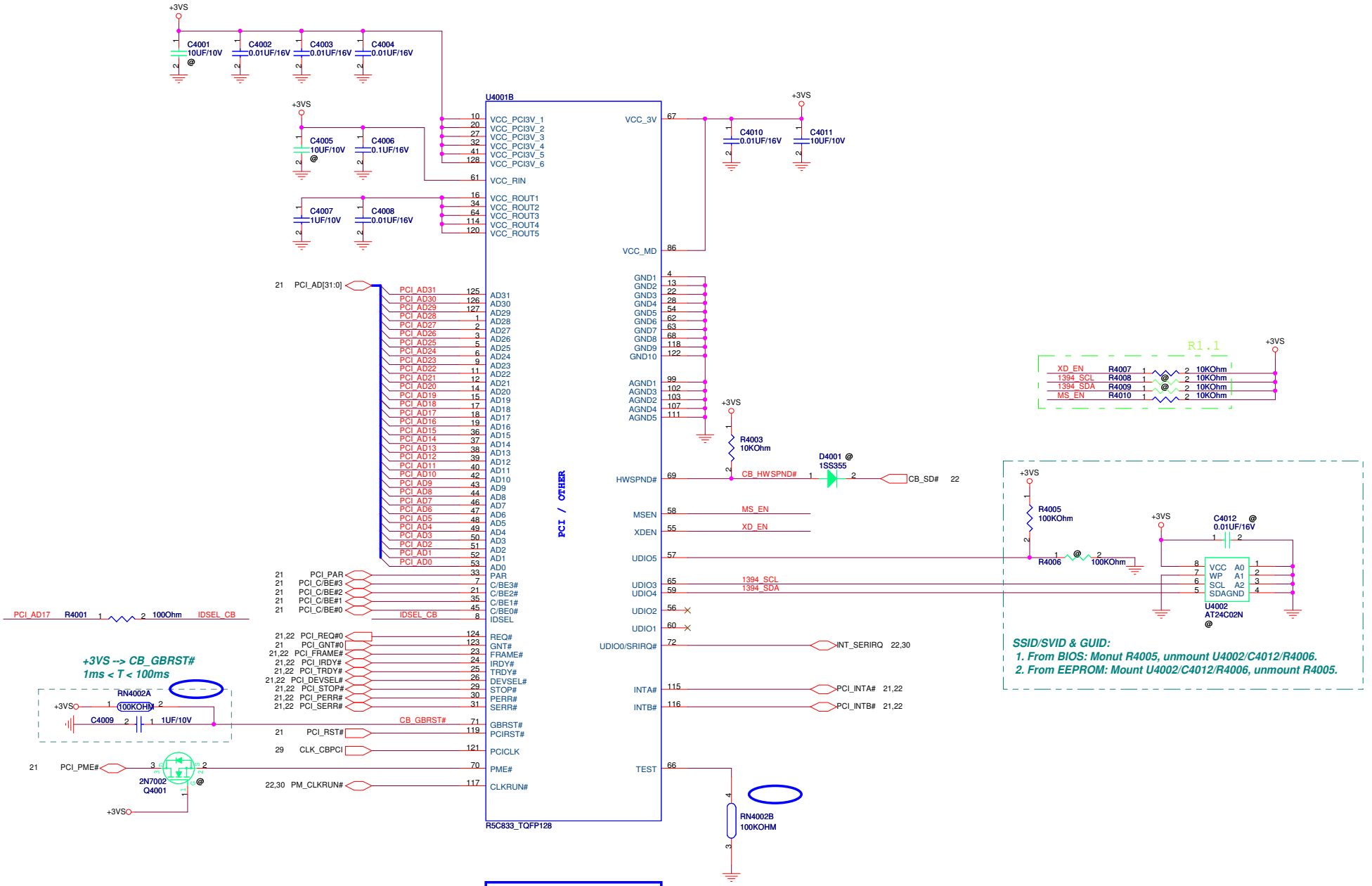
Main Board

PEGATRON Title : AUD_****

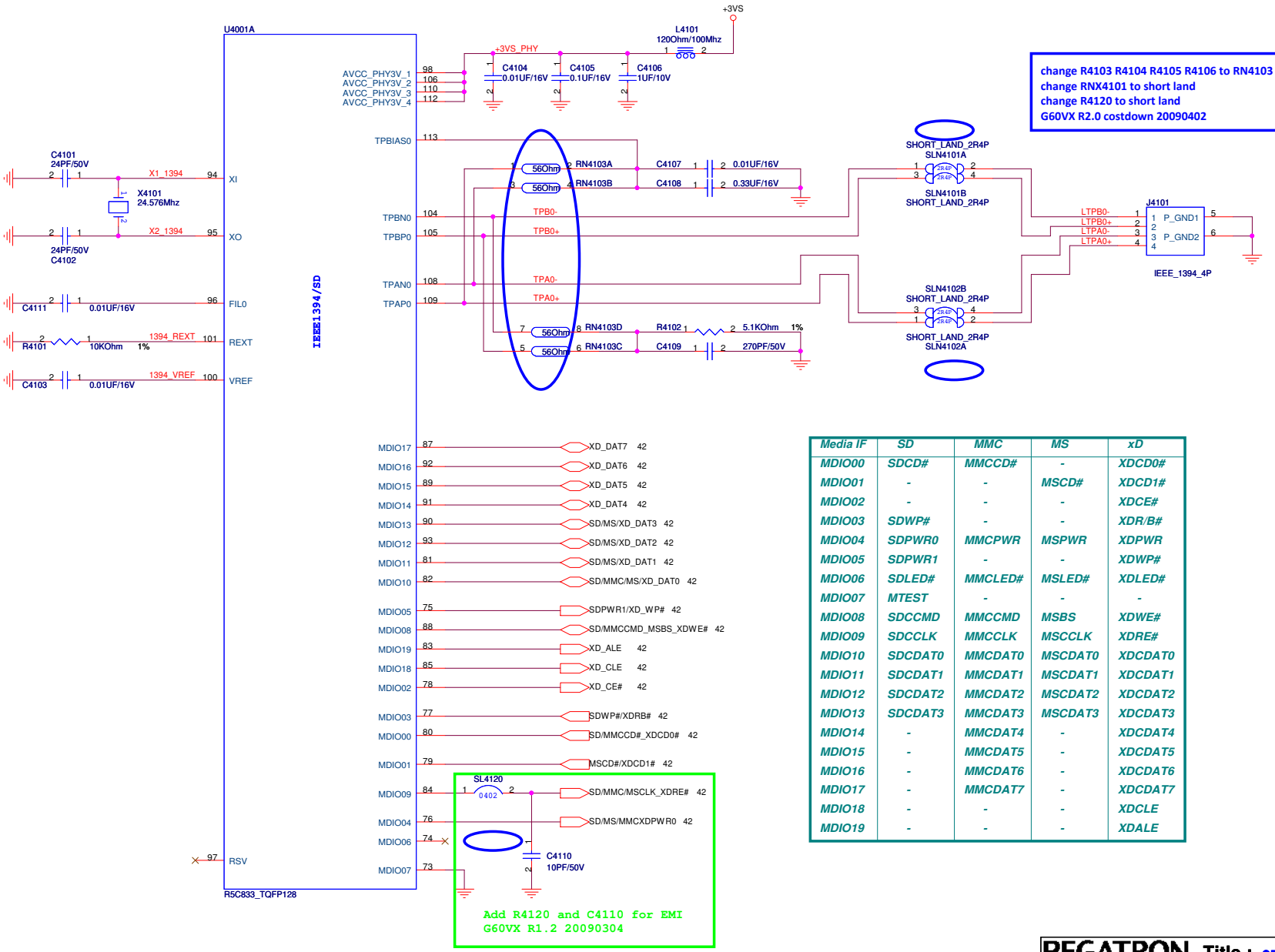
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 39 of 100



PEGATRON	Title : CB_R5C833		
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo		
Size: Custom	Project Name: G60VX		Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 40 of 100		



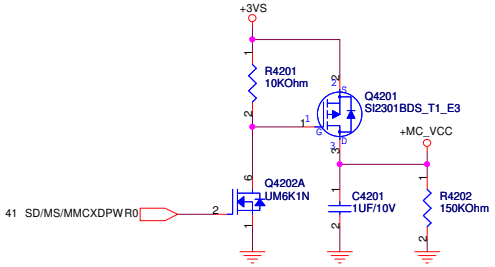
Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XDCLE
MDIO19	-	-	-	XDALE

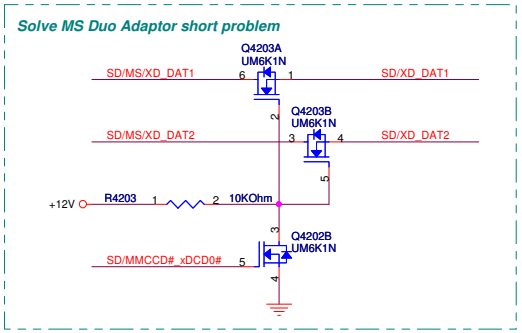
PEGATRON Title : CB_R5C833

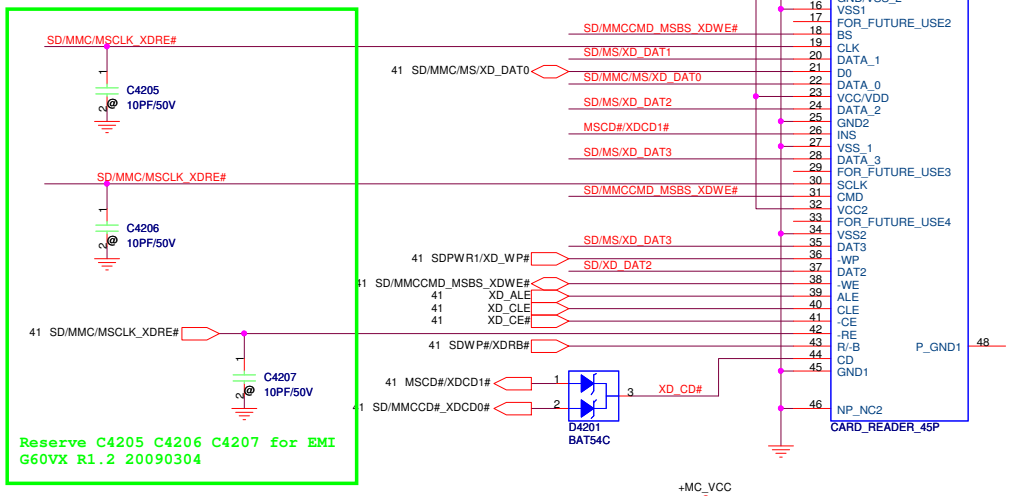
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

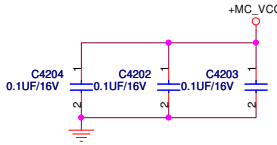
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 41 of 100







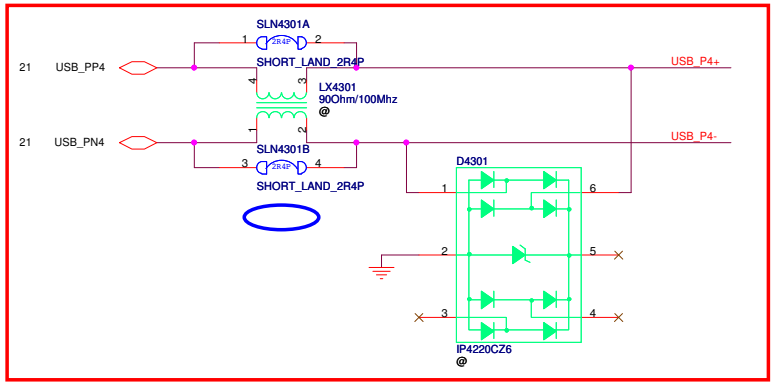


PEGATRON Title : CB_4in1 CardReader

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

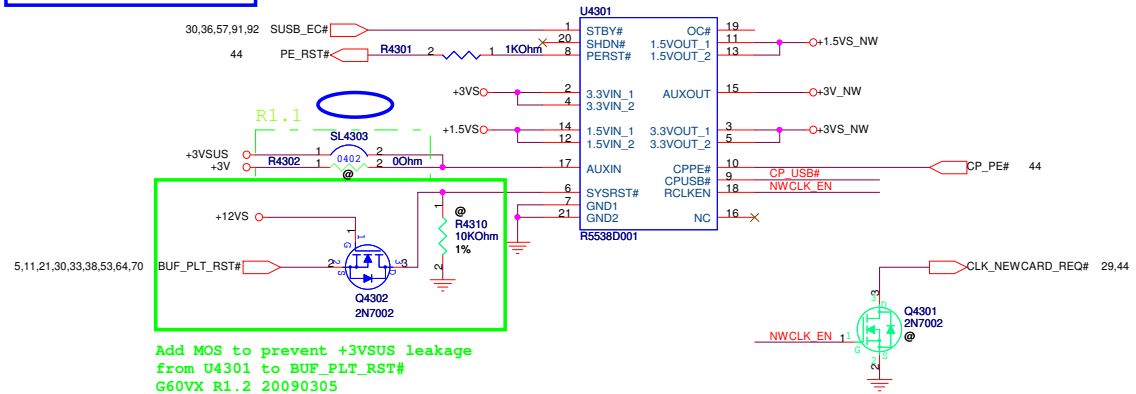
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 42 of 100



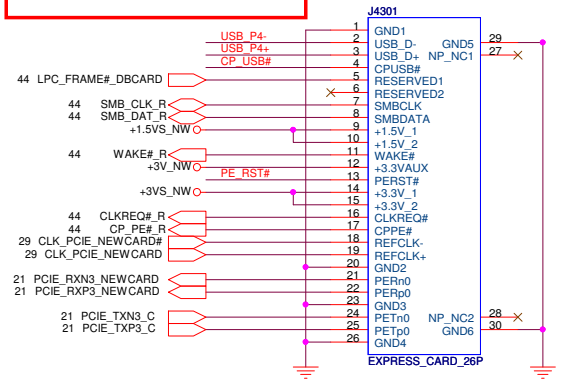
Change Newcard to USB port 4
G50VX R1.1 20090108

change RNX4301 to short land
chang R4303 to short land
G60VX R2.0 costdown 20090402

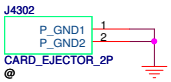


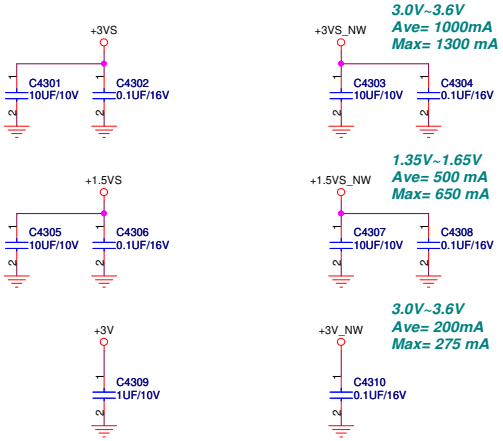
Add MOS to prevent +3VSUS leakage
from U4301 to BUF_PLT_RST#
G60VX R1.2 20090305

NewCard Header



NewCard Ejecter





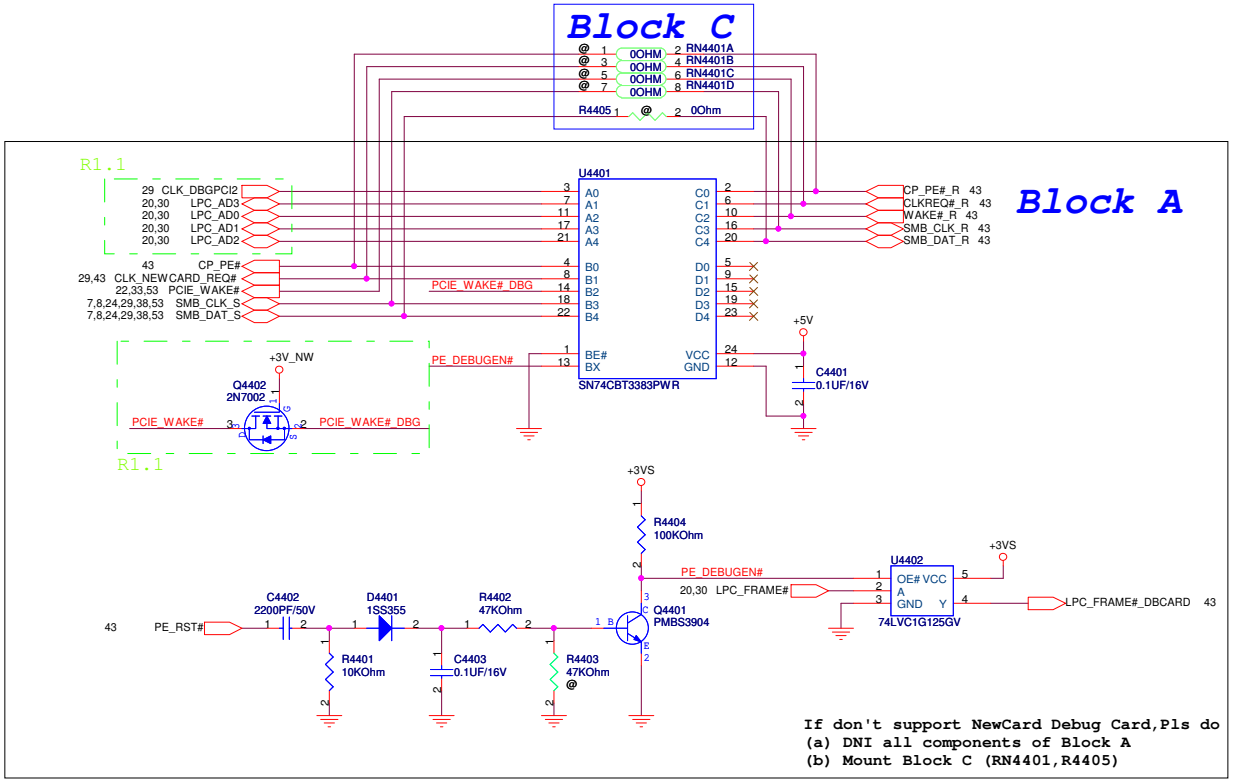
PEGATRON Title : CB_NewCard

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

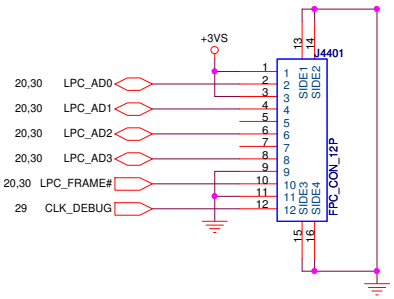
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 43 of 100

For NewCard Debug Card



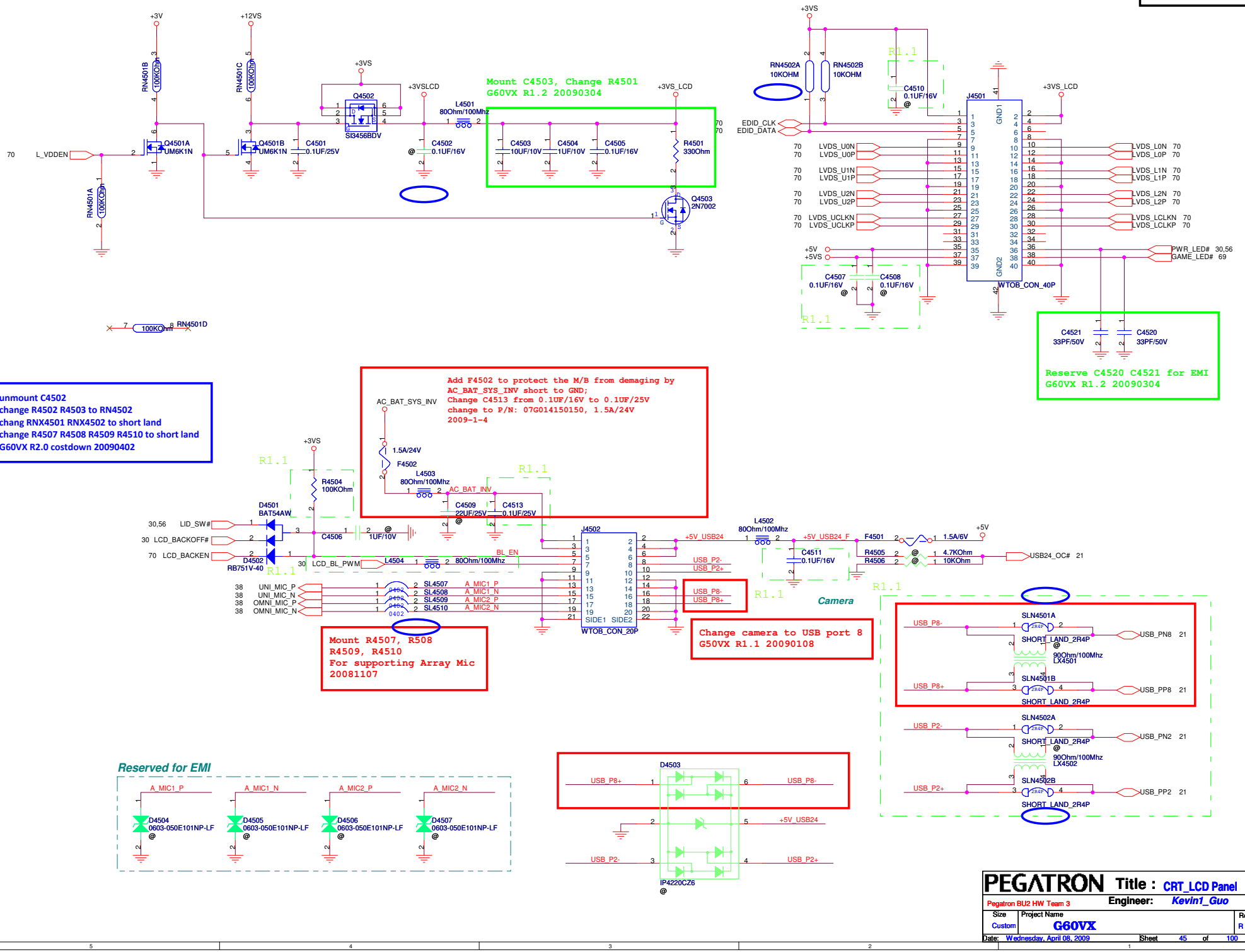
LPC Debug Port

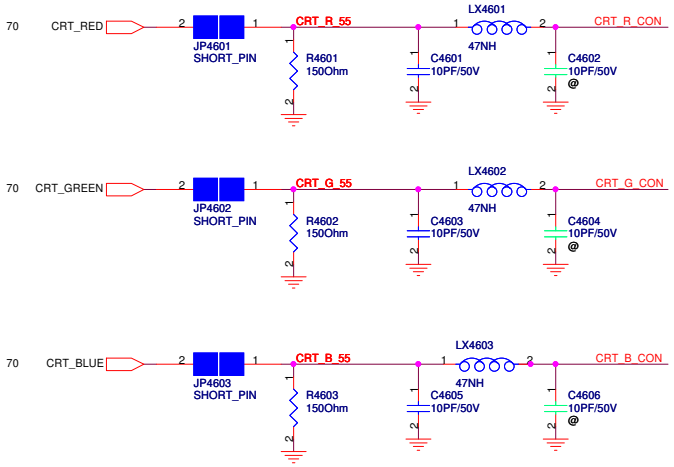


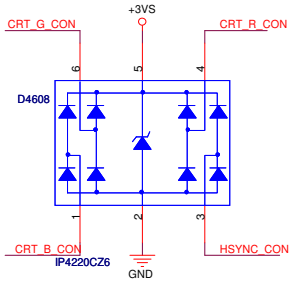
Mount Block A and LPC Debug Port in early stage
200811170917

PEGATRON	Title : BUG_Debug	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 44 of 100	

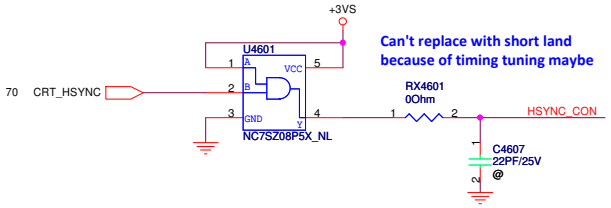
Main Board

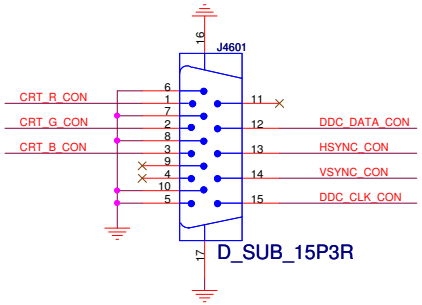

Mount C4503, Change R4501
G60VX R1.2 20090304
Reserve C4520 C4521 for EMI
G60VX R1.2 20090304
unmount C4502
change R4502 R4503 to RN4502
chang RNX4501 RNX4502 to short land
change R4507 R4508 R4509 R4510 to short land
G60VX R2.0 costdown 20090402
Add F4502 to protect the M/B from demaging by
AC_BAT_SYS_INV short to GND;
Change C4513 from 0.1UF/16V to 0.1UF/25V
change to P/N: 07G014150150, 1.5A/24V
2009-1-4
Mount R4507, R508
R4509, R4510
For supporting Array Mic
20081107
Change camera to USB port 8
G50VX R1.1 20090108
Camera
Reserved for EMI
PEGATRON
Title : CRT_LCD Panel
Pegatron BU2 HW Team 3
Engineer: Kevin1_Guo
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 45 of 100

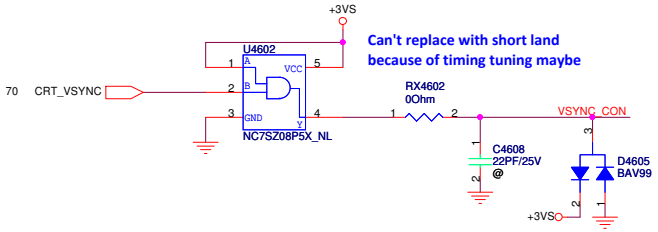


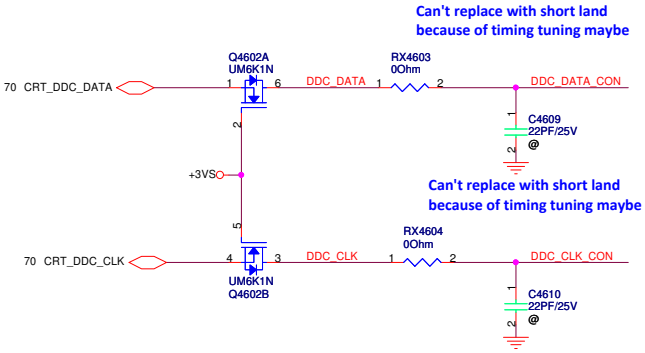


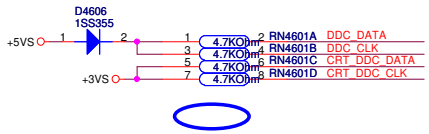
delete RX4605 RX4606 RX4607
delete D4601 D4602 D4603 D4604
add D4608
change RN4601 to 4R8P
delete RN4602
G60VX R2.0 costdown 20090402











PEGATRON Title : CRT_D-Sub

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

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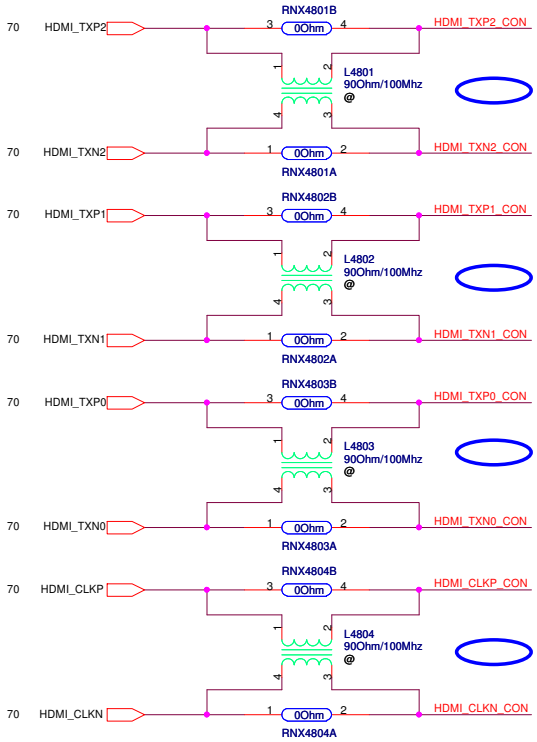
Main Board

PEGATRON Title : TV_****

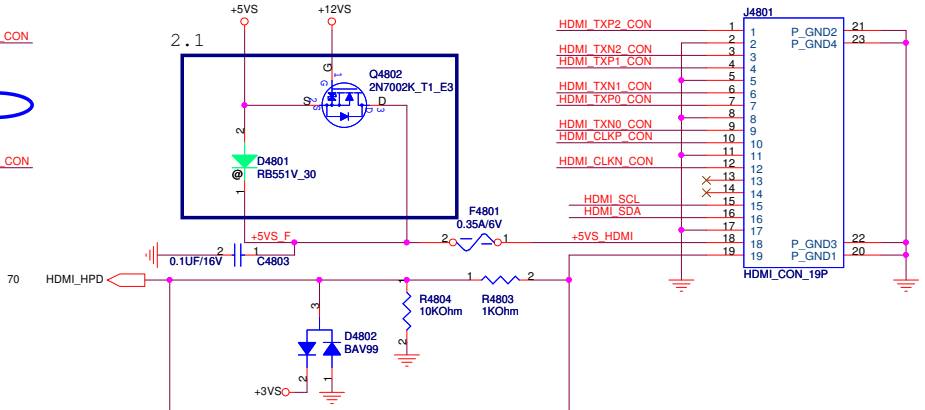
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

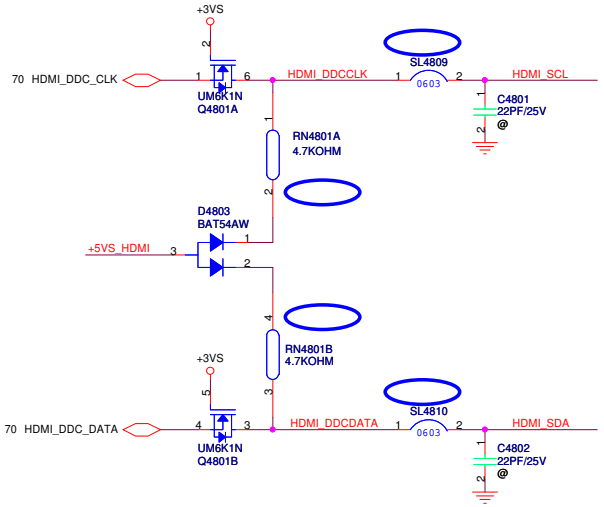
Size	Project Name	Rev
Custom	G60VX	R 1.2

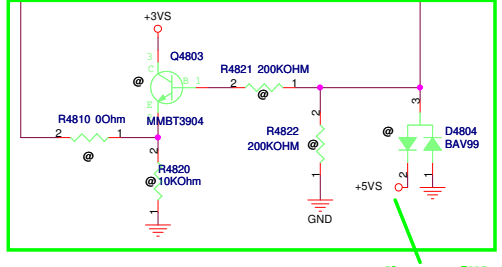
Date: Thursday, March 05, 2009 Sheet 47 of 100



Reserve RNX4801 RNX4802 RNX4803 RNX4804
delete RX4809 RX4810 / use short land;
delete R4801 R4802 / add RN4801
G60VX R2.0 costdown 20090402







Reserve schematic to prevent the
3.6-3.7V voltage to damage the GPU
NO STUFF! G60VX R1.2 20090304

Change +5VS from +3VS
G60VX R1.2 20090306

PEGATRON Title : TV_HDMI

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 48 of 100

Main Board

PEGATRON Title : TV_****

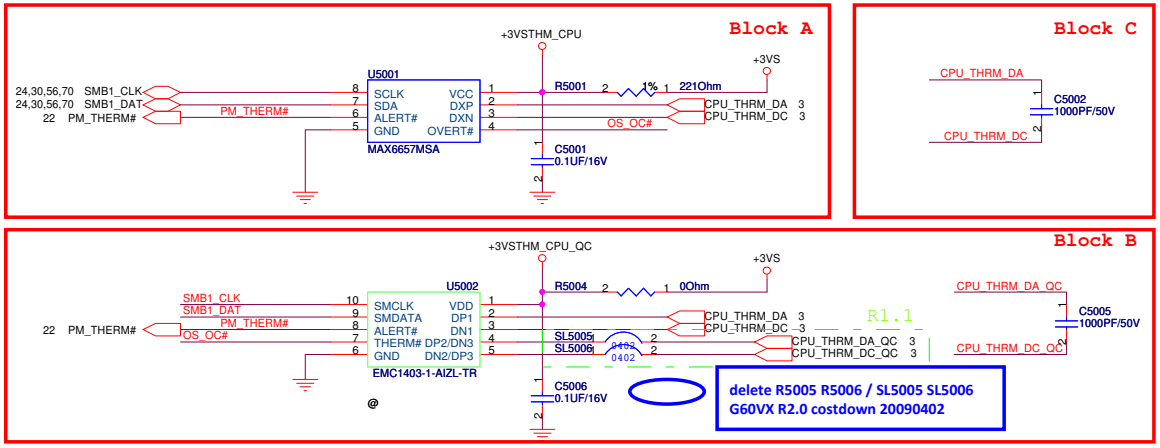
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 49 of 100

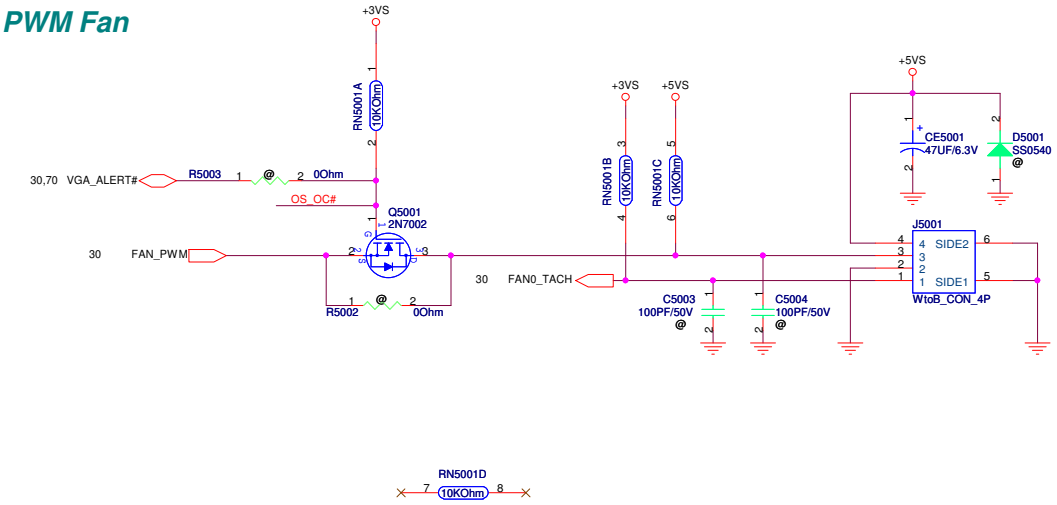
CPU Thermal Sensor

If support DC, Mount Block A and C, Unmount Block B;
If support QC, Mount Block B and C, Unmount Block A
200811121042



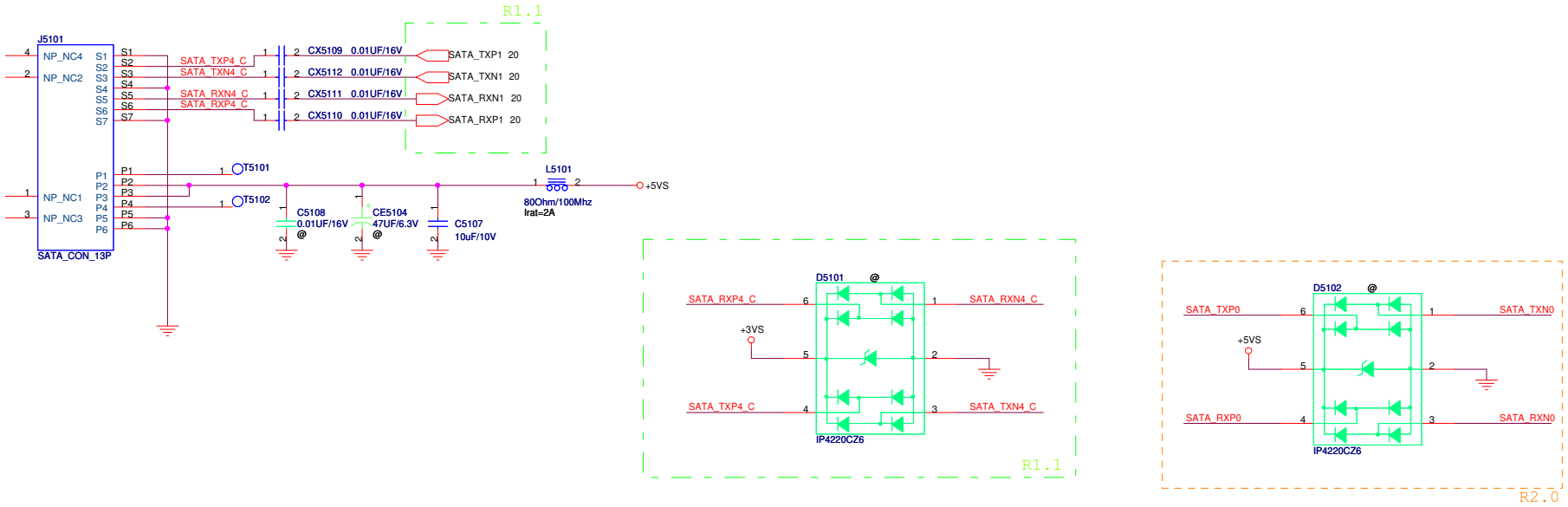
G50V and M52VF Mount R5004, R5005, R5006
C5005, C5006 although only support DC,
They can be cost down if only support DC

PWM Fan

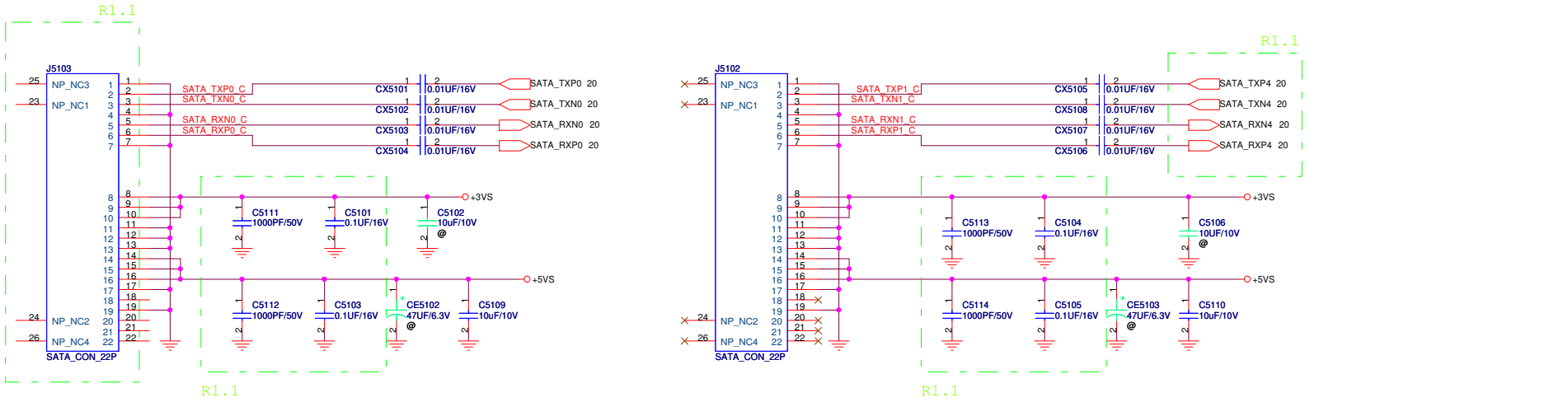


PEGATRON	Title : FAN_Fan & Sensor	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 50 of 100	

ODD



HDD



mount CE5102 C5103,unmount C5111
C5101 C5112 C5109
G60VX R2.0 costdown 20090402

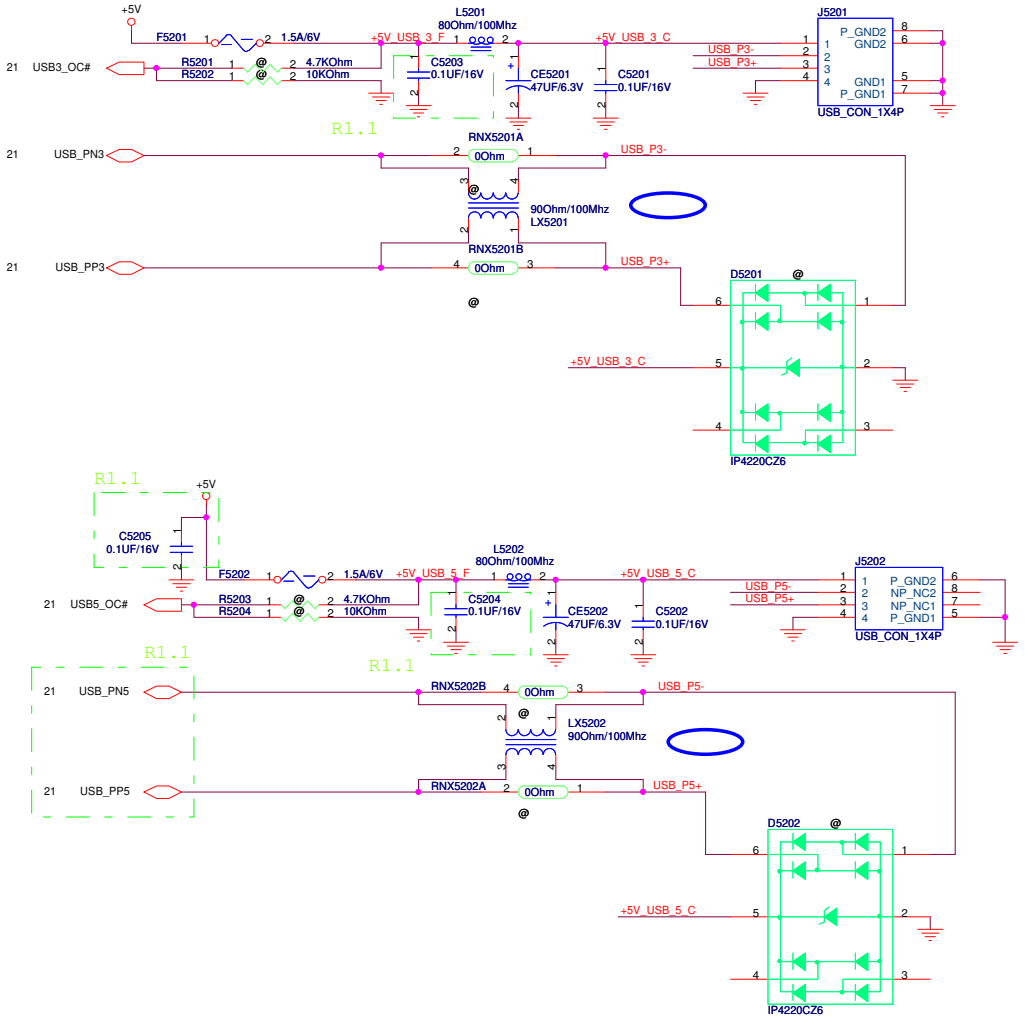
mount CE5103 C5105, unmount C5113
C5104 C5114 C5110
G60VX R2.0 costdown 20090402

PEGATRON Title : XDD_HDD & ODD

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 51 of 100

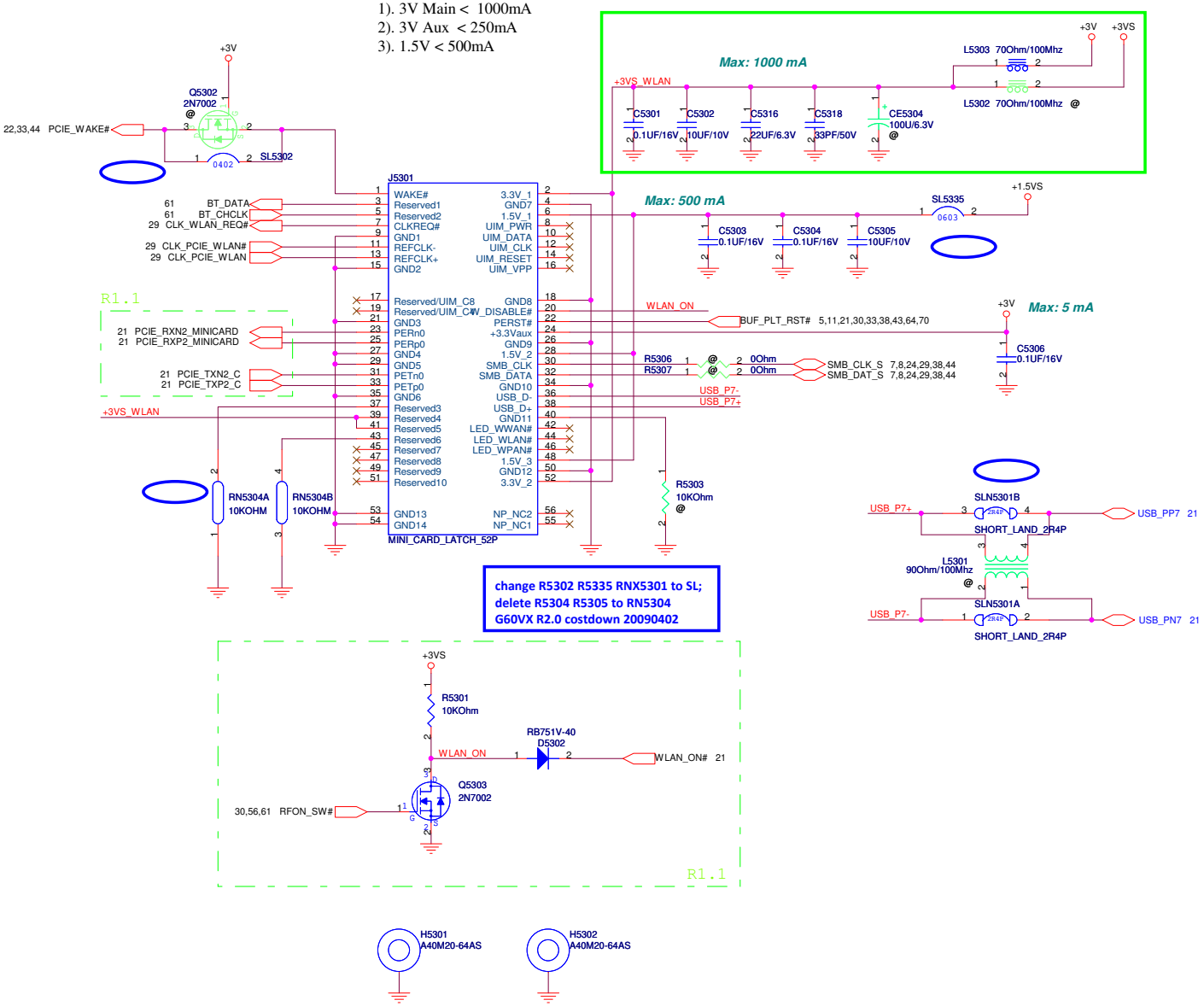


need Verification !
G60VX R2.0 costdown 20090402

PEGATRON	Title : USB_USB Port *2	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 52 of 100	

Follow H15HV R2.1 to accommodate large current
for Intel WiFi link 5300/5100 WLAN card
G60VX R1.2 20090305

POWER CONSUMPTION:
1). 3V Main < 1000mA
2). 3V Aux < 250mA
3). 1.5V < 500mA



PEGATRON	Title : PCI_WLAN	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 53 of 100	

Main Board

PEGATRON Title : BAR_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 54 of 100

Main Board

PEGATRON Title : SIO_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 55 of 100

Main Board

T5601 PWR_SW#
T5602 POWER_SW#
T5603 PWR_LED#
T5604 CHG_LED#
T5605 PWR_LED_CON#
T5606 CHG_LED_CON#

30 NUM_LED# — 33Ohm — RN5601A — NUM_LED_CON#
30 CAP_LED# — 33Ohm — RN5601B — CAP_LED_CON#

+3VA
RN5609A 10KOHM
30,45 LID_SW# — 33Ohm — RN5604B — LID_SW_CON#
C5602 0.1UF/10V

+3VA
RN5609B 10KOHM
30 PWR_SW# — 33Ohm — RN5604A — POWER_SW#
C5601 0.1UF/10V

J5601 FPC_20P
GND1 21
GND2 22
24,30,50,70 SMB1_CLK
24,30,50,70 SMB1_DAT
30 CAP_ACK_A#
+3VS
+5VS
HDD_LED_CON#
NUM_LED_CON#
+5VSUS
CAP_LED_CON#
+3VA
PWR_LED_CON#
LID_SW_CON#
POWER_SW#
GND
30 INSTANT_ON# — 0402 — SL5621
+5VA
CAP_ACK_B#
30 CAP_ACK_B#
30 ALS_AD — R5620 @ — 0Ohm

For Test

SW5602 TP_SWITCH_4P
R5623 0Ohm PWR_SW#
+5V
R5622 @ 330Ohm
LED5601 BLUE @
R5610 @ 0Ohm PWR_LED_CON#

delete R5609 R5607, add RN5609
delete R5621
delete R5619
delete R5614
delete R5617 R5616
G60VX R2.0 costdown 20090402

Power LED

+5V
R5618 10KOhm
30,45 PWR_LED# — Q5606A UM6K1N — Q5606B UM6K1N
PWR_LED_CON# — PWR_LED_CON# 31
R5641 @ 0Ohm
Reserve 0 OHM 0603

Charger LED

+5VA
R5613 10KOhm
30 CHG_LED# — Q5603A UM6K1N — Q5603B UM6K1N
CHG_LED_CON# 31
R5640 0Ohm @
Reserve 0 OHM 0603

+3VS
+3VA
R5615 10KOhm
R5611 10KOhm @
R5612 33Ohm
30,53,61 RFON_SW# — C5603 0.1UF/10V
SW5601 SLIDE_SWITCH_6P

HDD LED

+3VS
R5602 10KOhm
20 SATA_LED# — Q5601A UM6K1N — Q5601B UM6K1N
330Ohm R5603 HDD_LED_CON#
Can't remove R5603

WLAN LED

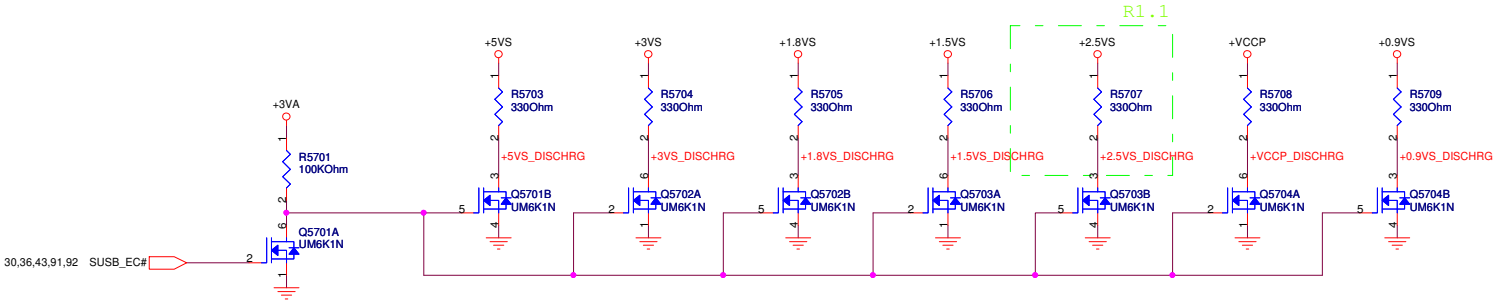
31 WLAN_LED_CON# — WLAN_LED_CON#
+3VS
R5604 10KOhm @
22 WLAN_LED — Q5605A UM6K1N

BT LED

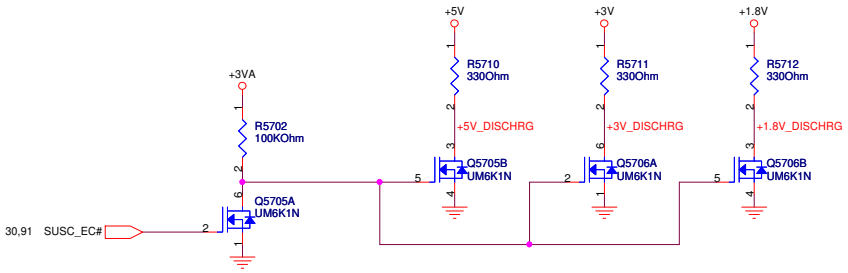
BT_LED_CON# — BT_LED_CON# 31
+3VS
R5605 10KOhm @
Q5605B UM6K1N — BT_LED 22

U80V doesn't costdown this MOS

PEGATRON Title : LED_Indicator
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom | Project Name: G60VX | Rev: R 1.2
Date: Wednesday, April 08, 2009 | Sheet 56 of 100



Need to verification!
G60VX R2.0 costdown 20090402



PEGATRON Title : DSG_Discharge

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 57 of 100

Main Board

PEGATRON Title : PCI_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 58 of 100

Main Board

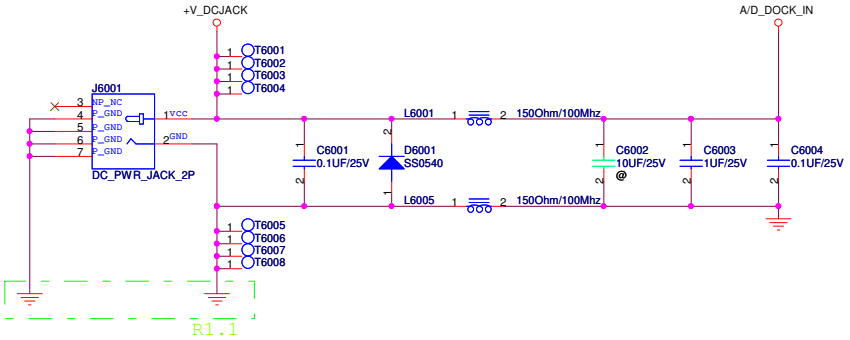
PEGATRON Title : DJ_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

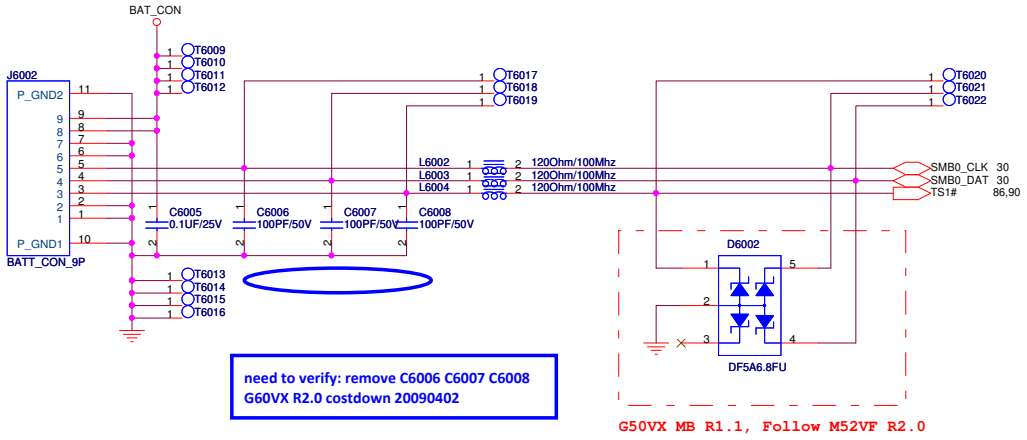
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 59 of 100

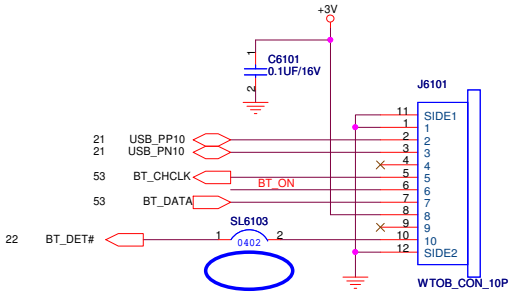
DC Jack



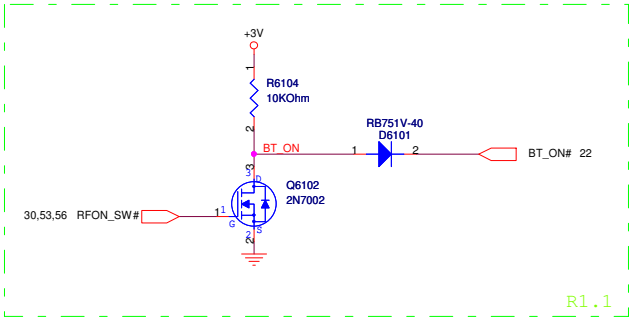
Battery Connector



PEGATRON	Title : DC_DC & BAT Conn	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Sunday, April 05, 2009	Sheet 60 of 100	



delete R6103
G60VX R2.0 costdown 20090402



PEGATRON	Title : BT_Bluetooth	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 61 of 100	

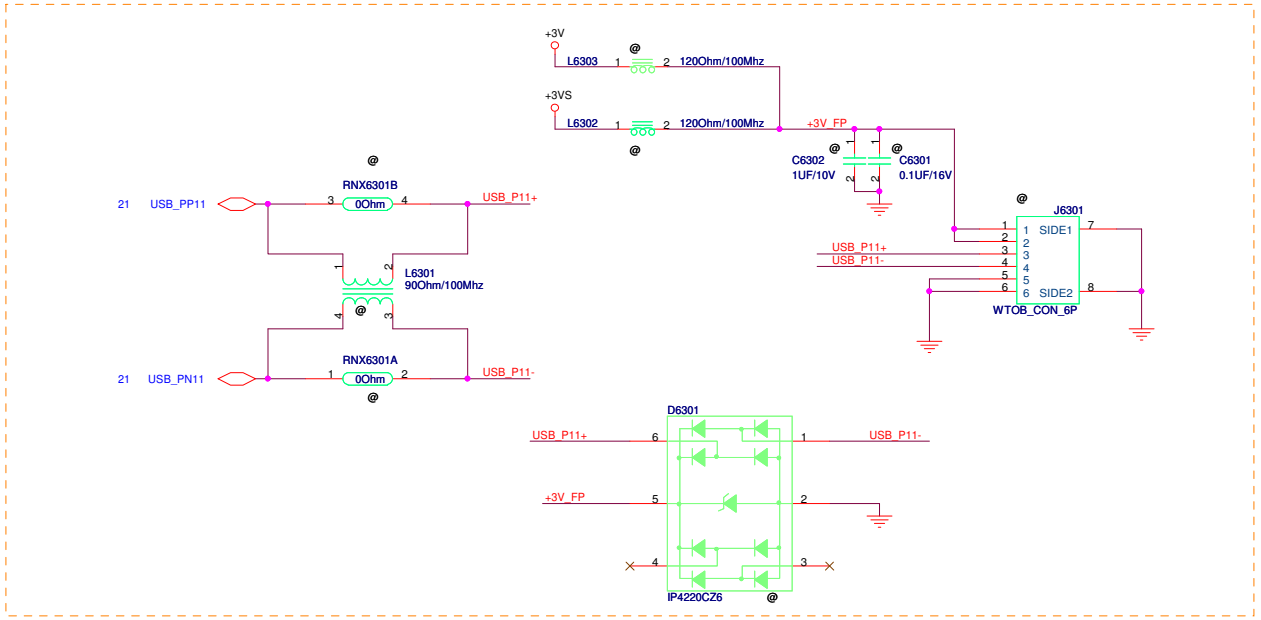
Main Board

PEGATRON Title : TPM_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

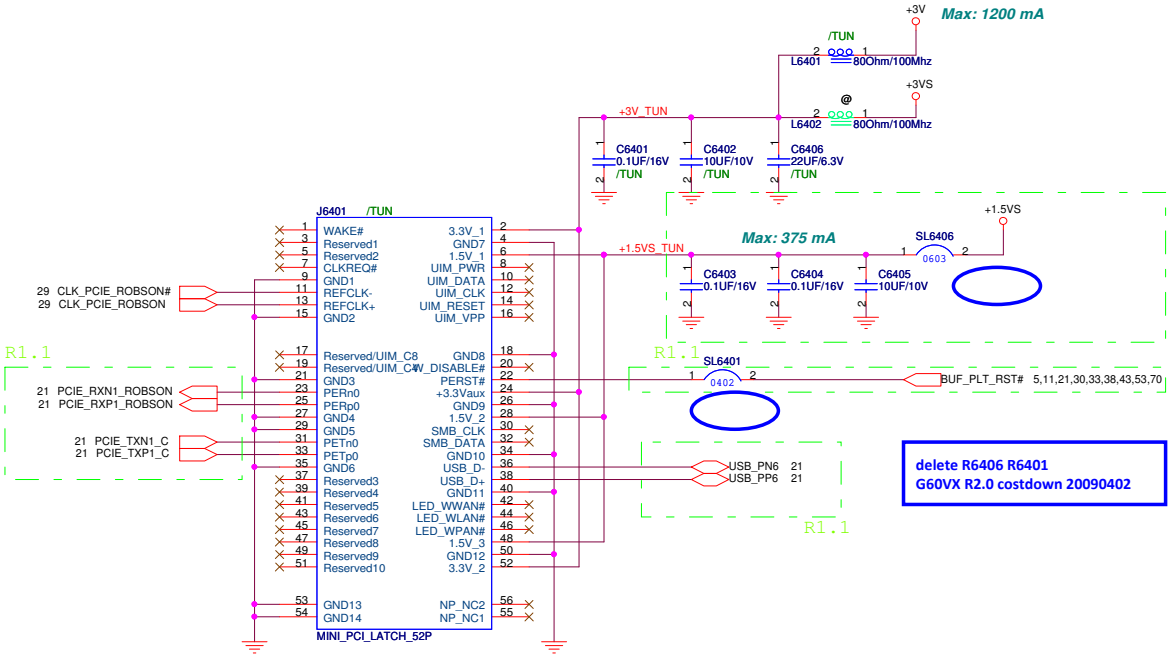
Date: Thursday, March 05, 2009 Sheet 62 of 100

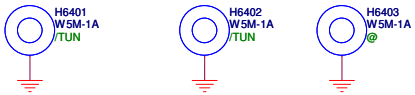


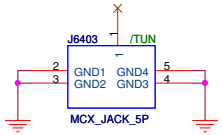
R2.0

Unmount J6301, C6301, C6302, L6302
RNX6301 for delete FP connector
L6303, L6301, D6301 is reserved
200811102025

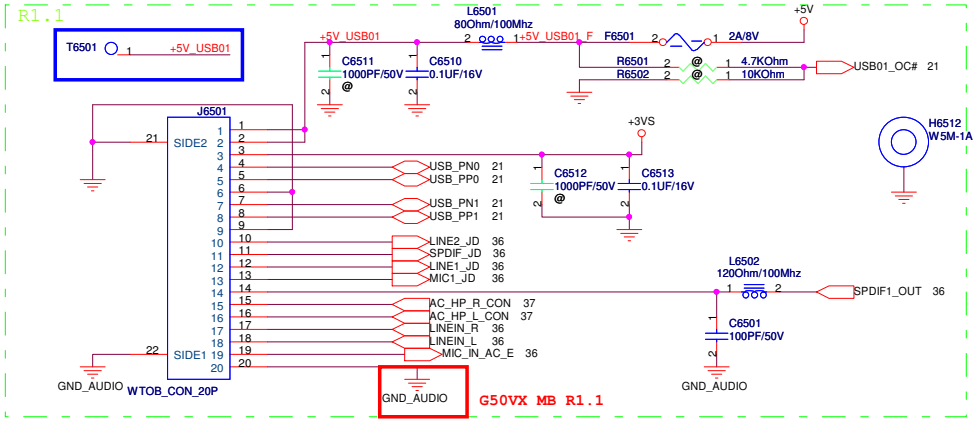
PEGATRON	Title : FP_FP Conn	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 63 of 100	

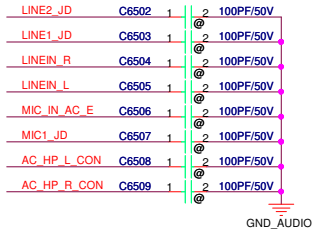


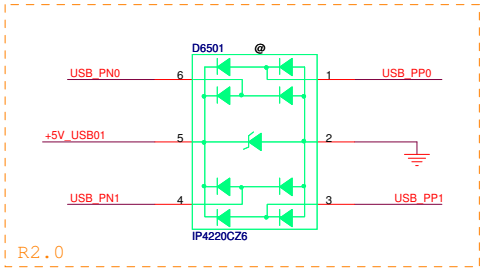


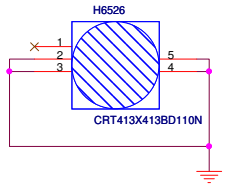


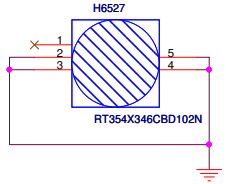
PEGATRON	Title : TUN_TV Tuner	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 64 of 100	

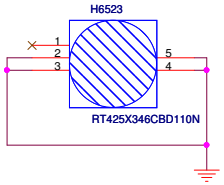


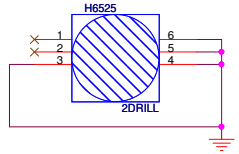


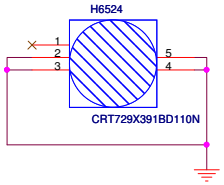


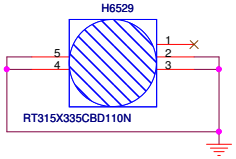


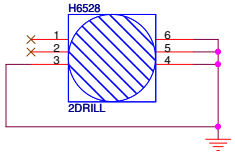




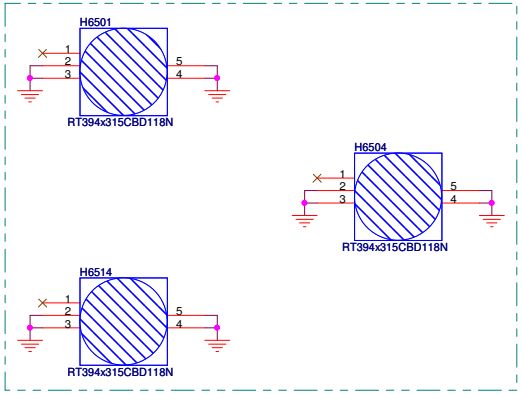




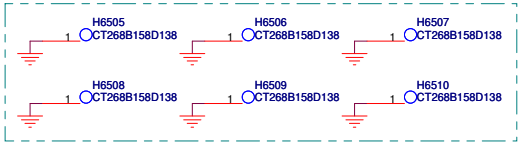




Screw Hole A



Screw Hole B



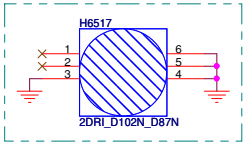
Screw Hole C

Screw Hole F

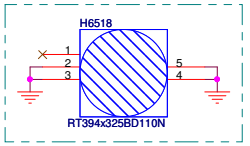
Screw Hole H

Screw Hole I

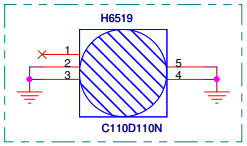
Screw Hole J



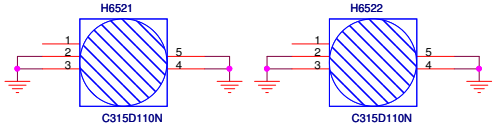
Screw Hole K



Screw Hole L



Screw Hole M

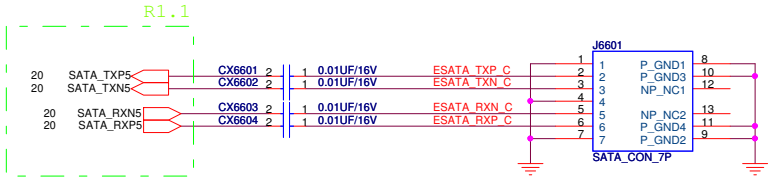


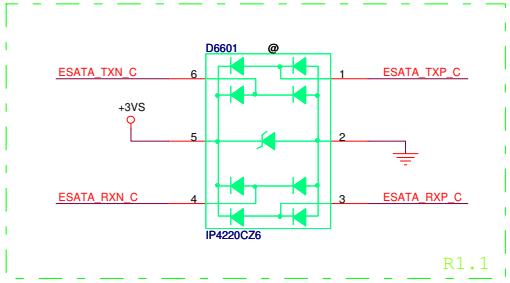
PEGATRON Title : ME_Conn & Skew Hole

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 65 of 100





PEGATRON	Title : ESA_ESATA	
Pegatron BU2 HW Team 3	Engineer: Kevin1_Guo	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Thursday, March 05, 2009	Sheet 66 of 100	

Main Board

PEGATRON Title : PCI_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

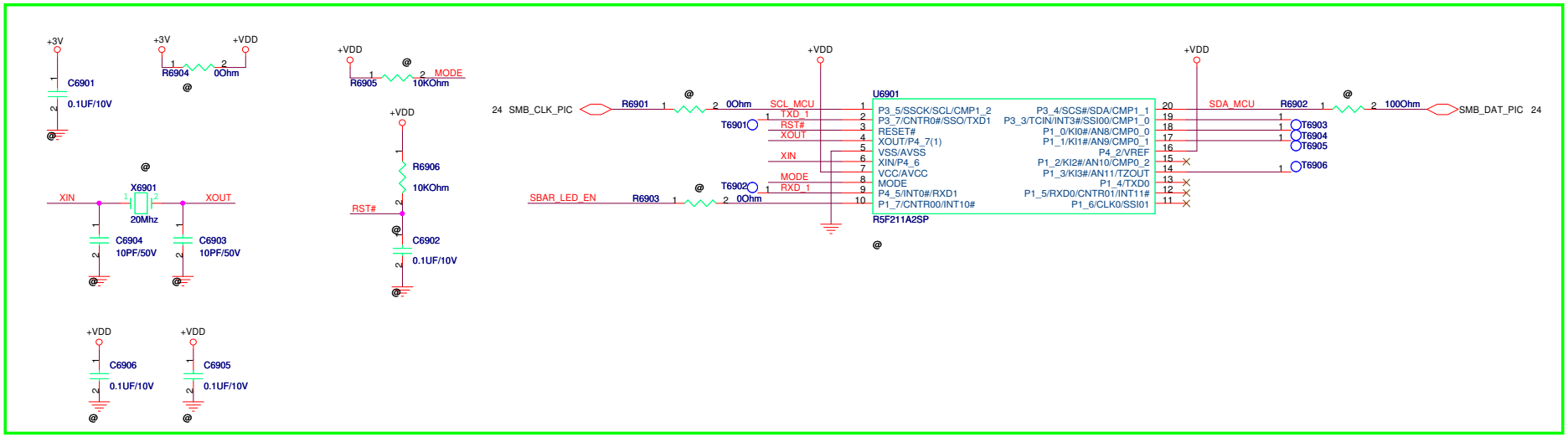
Date: Thursday, March 05, 2009 Sheet 67 of 100

PEGATRON Title : OTH_LCM

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

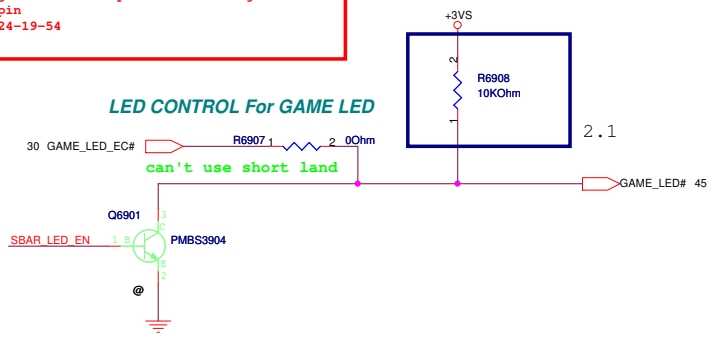
Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 68 of 100



Cause EC will control GAME_LED#
Mount R6907 R6908, unmount
all others and Q2402 RN2402
G60VX R1.2 20090305

G50VX V1.0, Change net GAME_LED_EC# from
conecting with EC.GPA3 pin to connecting with
EC.GPA6 pin
2008-11-24-19-54



PEGATRON Title : OTH_GAME-LED

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Wednesday, April 08, 2009 Sheet 69 of 100

Main Board

PCIENB_RXN[15:0] 11
PCIENB_RXP[15:0] 11
PCIEG_RXN[15:0] 11
PCIEG_RXP[15:0] 11

delete co-lay, reserved bead for EMI,
G60VX R2.0 20090408

J7001A

DVI
DVI_A_TX0
DVI_A_TX0#
DVI_A_TX1
DVI_A_TX1#
DVI_A_TX2
DVI_A_TX2#
DVI_A_CLK
DVI_A_CLK#
DVI_A_HPD
DVI_B_HPD/GND
DDCB_CLK
DDCB_DAT
DDCA_CLK
DDCA_DAT
48 HDMI_HPD
46 CRT_DDC_CLK
46 CRT_DDC_DATA

VGA
VGA_BLU
VGA_RED
VGA_GRN
VGA_HSYNC
VGA_VSYNC
46 CRT_BLUE
46 CRT_RED
46 CRT_GREEN
46 CRT_HSYNC
46 CRT_VSYNC

LVDS
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
LVDS_UTX0
LVDS_UTX0#
LVDS_UTX1
LVDS_UTX1#
LVDS_UTX2
LVDS_UTX2#
LVDS_UTX3
LVDS_UTX3#
LVDS_UCLK
LVDS_UCLK#
LVDS_LTX0
LVDS_LTX0#
LVDS_LTX1
LVDS_LTX1#
LVDS_LTX2
LVDS_LTX2#
LVDS_LTX3
LVDS_LTX3#
LVDS_LCLK
LVDS_LCLK#
45 L_VDDEN
45 LCD_BACKEN
45 LVDS_L0P
45 LVDS_L0N
45 LVDS_L1P
45 LVDS_L1N
45 LVDS_L2P
45 LVDS_L2N
45 LVDS_LCLKP
45 LVDS_LCLKN
45 LVDS_U0P
45 LVDS_U0N
45 LVDS_U1P
45 LVDS_U1N
45 LVDS_U2P
45 LVDS_U2N
45 LVDS_UCLKP
45 LVDS_UCLKN

IGP
+0.9VS
IGP_UTX0
IGP_UTX0#
IGP_UTX1
IGP_UTX1#
IGP_UTX2
IGP_UTX2#
36 SPDIF2_OUT
20 ACZ_RST#_VGA
20 ACZ_SDOUT_VGA
20 ACZ_SDIN2_VGA
20 ACZ_SYNC_VGA
20 ACZ_BCLK_VGA
IGP_UCLK
IGP_UCLK#
IGP_LTX0/DVI_B_TX0
IGP_LTX0#/DVI_B_TX0#
IGP_LTX1/DVI_B_TX1
IGP_LTX1#/DVI_B_TX1#
IGP_LTX2/DVI_B_TX2
IGP_LTX2#/DVI_B_TX2#
IGP_LCLK/DVI_B_CLK
IGP_LCLK#/DVI_B_CLK#
48 HDMI_TXP0
48 HDMI_TXN0
48 HDMI_TXP1
48 HDMI_TXN1
48 HDMI_TXP2
48 HDMI_TXN2
48 HDMI_CLKP
48 HDMI_CLKN
HDMI_TXP0
HDMI_TXN0
HDMI_TXP1
HDMI_TXN1
HDMI_TXP2
HDMI_TXN2
HDMI_CLKP
HDMI_CLKN

TV-OUT
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
T7001
T7002
T7003

SMBUS
DDCC_CLK
DDCC_DAT
SMB_CLK
SMB_DAT
45 EDID_CLK
45 EDID_DATA
24,30,50,56 SMB1_CLK
24,30,50,56 SMB1_DAT
RN7001A
RN7001B
0OHM

PEX
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
PCIEG_RXP0
PCIEG_RXN0
PCIENB_RXP0
PCIENB_RXN0
PCIEG_RXP1
PCIEG_RXN1
PCIENB_RXP1
PCIENB_RXN1
PCIEG_RXP2
PCIEG_RXN2
PCIENB_RXP2
PCIENB_RXN2
PCIEG_RXP3
PCIEG_RXN3
PCIENB_RXP3
PCIENB_RXN3
PCIEG_RXP4
PCIEG_RXN4
PCIENB_RXP4
PCIENB_RXN4
PCIEG_RXP5
PCIEG_RXN5
PCIENB_RXP5
PCIENB_RXN5
PCIEG_RXP6
PCIEG_RXN6
PCIENB_RXP6
PCIENB_RXN6
PCIEG_RXP7
PCIEG_RXN7
PCIENB_RXP7
PCIENB_RXN7
PCIEG_RXP8
PCIEG_RXN8
PCIENB_RXP8
PCIENB_RXN8
PCIEG_RXP9
PCIEG_RXN9
PCIENB_RXP9
PCIENB_RXN9
PCIEG_RXP10
PCIEG_RXN10
PCIENB_RXP10
PCIENB_RXN10
PCIEG_RXP11
PCIEG_RXN11
PCIENB_RXP11
PCIENB_RXN11
PCIEG_RXP12
PCIEG_RXN12
PCIENB_RXP12
PCIENB_RXN12
PCIEG_RXP13
PCIEG_RXN13
PCIENB_RXP13
PCIENB_RXN13
PCIEG_RXP14
PCIEG_RXN14
PCIENB_RXP14
PCIENB_RXN14
PCIEG_RXP15
PCIEG_RXN15
PCIENB_RXP15
PCIENB_RXN15
CLK_REQ#
PEX_RST#
PEX_REFCLK
PEX_REFCLK#

OTHER
THERM#
PRSNT1#
PRSNT2#
RUNPWROK
NP_NC1
NP_NC2
GND_1
GND_2
PRSNT2#
PWR_OK_VGA 92

R7014 SL7013 0402 0Ohm
GPU_RST# 22
BUF_PLT_RST# 5,11,21,30,33,38,43,53,64
CLK_PCIE_PEG 29
CLK_PCIE_PEG# 29
Q7003 2N7002
SL7001 0402
FORCE_OFF# 5,81,92
VGA_ALERT# 30,50
BUF_PLT_RST# 5,11,21,30,33,38,43,53,64

J7001B

AC_BAT_SYS
JP7001 3MM_OPEN_5MIL
JP7002 3MM_OPEN_5MIL
PWR_SRC1
PWR_SRC2
PWR_SRC3
PWR_SRC4
PWR_SRC5
PWR_SRC6
PWR_SRC7
PWR_SRC8
+1.5VS
1V8RUN_1
1V8RUN_2
1V8RUN_3
1V8RUN_4
1V8RUN_5
1V8RUN_6
1V8RUN_7
+3VS
3V3RUN_1
3V3RUN_2
3V3RUN_3
+2.5VS
5VRUN
2V5RUN
+5V
RSVD1
+12VS
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
AC/BATT#
48 HDMI_DDC_CLK
48 HDMI_DDC_DATA
29 CLK_GFX_SSC
29 CLK_GFX_NOSSC
SUSB#_PWR_VGA
+1.8VS
GND66
GND65
GND64
GND63
GND62
GND61
GND60
GND59
GND58
GND57
GND56
GND55
GND1
GND2
GND3
GND4
GND5
GND6
GND7
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GND36
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GND38
GND39
GND40
GND41
GND42
GND43
GND44
GND45
GND46
GND47
GND48
GND49
GND50
GND51
GND52
GND53
GND54
MXM_230P

U7001
+3VSUS
Vcc
NC
A
GND
Y
NC7SZ14P5_NL
SUSB#_PWR_VGA
G50VX MB R1.1
R7007 0Ohm
R7003 100KOhm
81,82,83,84,91,93 SUSB#_PWR
R7004 10KOhm
Q7001 PMBS3904
PRSNT2#
R7002 0Ohm
+12VSUS
R7005 100KOhm
R7006 100KOhm
Q7002 2N7002
ATI : Low
NV : High
C7005 0.1UF/16V

HDMI_TXP0 R7009 300Ohm
HDMI_TXN0 C7001 0.1UF/16V
HDMI_TXP1 R7010 300Ohm
HDMI_TXN1 C7002 0.1UF/16V
HDMI_TXP2 R7011 300Ohm
HDMI_TXN2 C7003 0.1UF/16V
HDMI_CLKP R7012 300Ohm
HDMI_CLKN C7004 0.1UF/16V

Please set them near
the MXM connector.

MXM Heatsink Stand-Off

H7001 CT217B67D47
H7002 CT217B67D47
H7003 U5F-M-EXPREE
H7004 U5F-M-EXPREE

no change

delete R7001 R7013
G60VX R2.0 costdown 20090402

PEGATRON Title : VGA_MXM
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom | Project Name: G60VX | Rev: R 1.2
Date: Wednesday, April 08, 2009 | Sheet 70 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 71 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 72 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

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Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 74 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 75 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 76 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 77 of 100

Main Board

PEGATRON Title : VGA_****

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 78 of 100

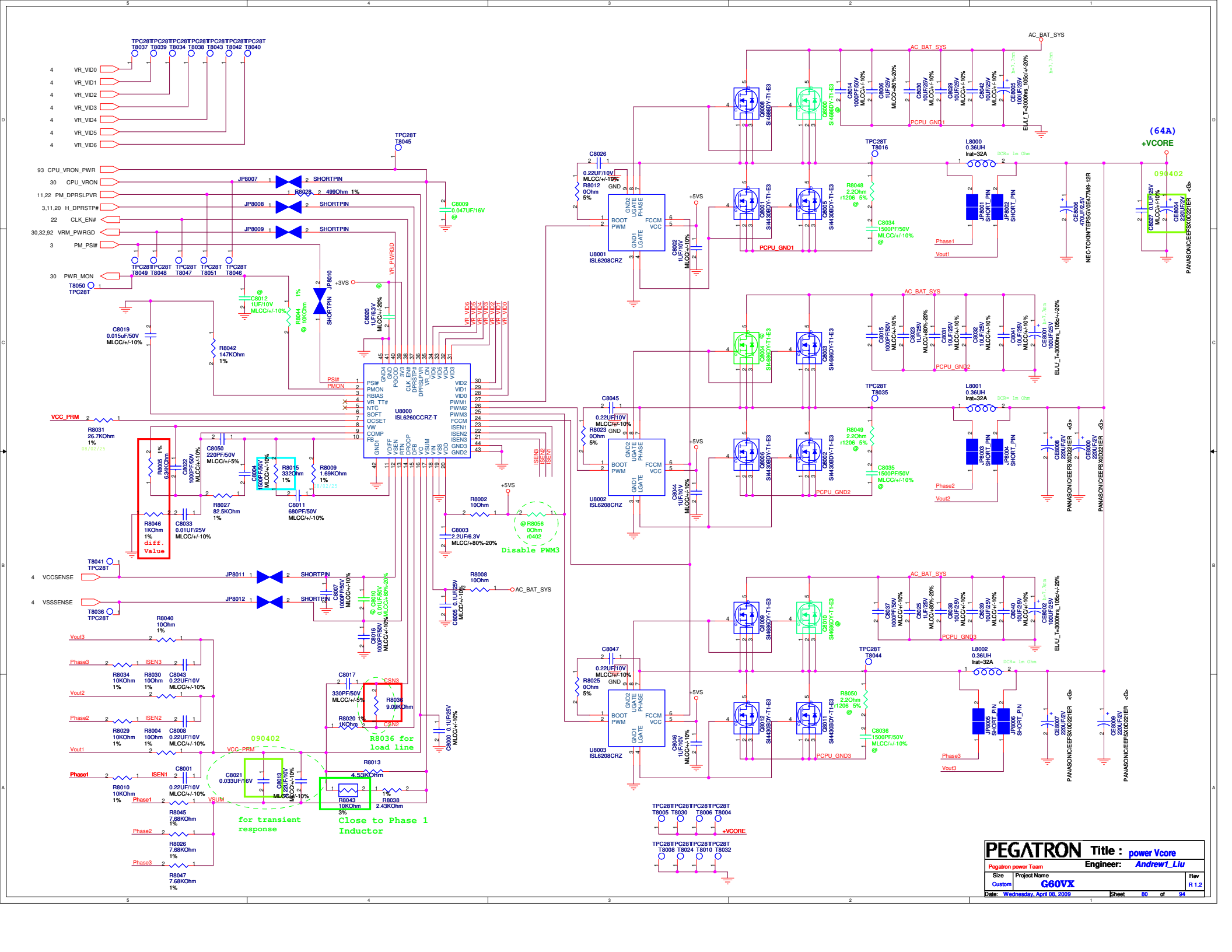
Main Board

PEGATRON Title : VGA_****

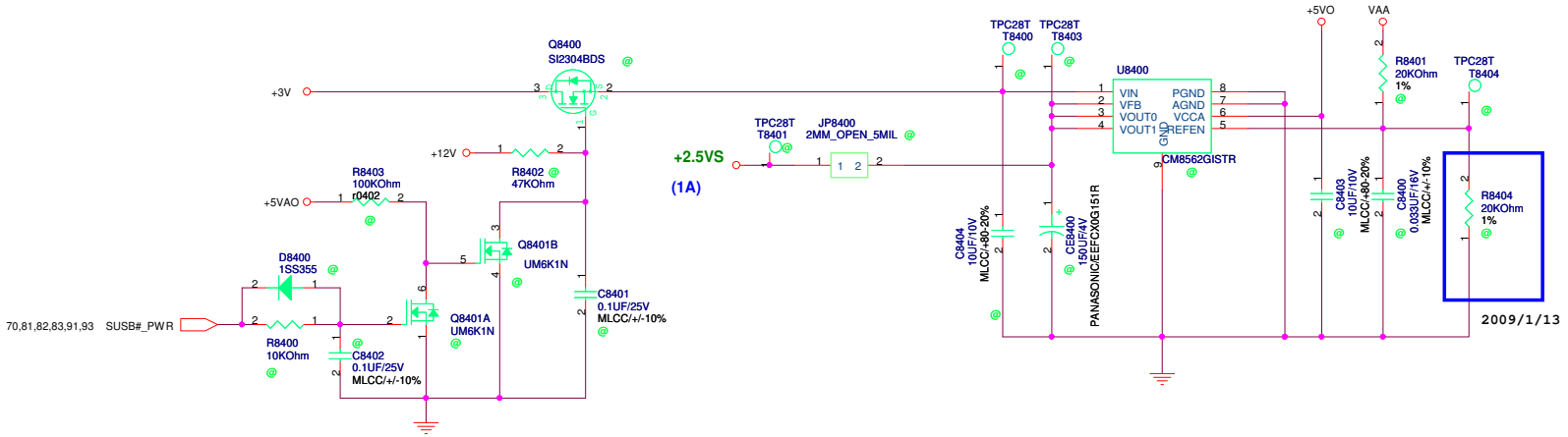
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

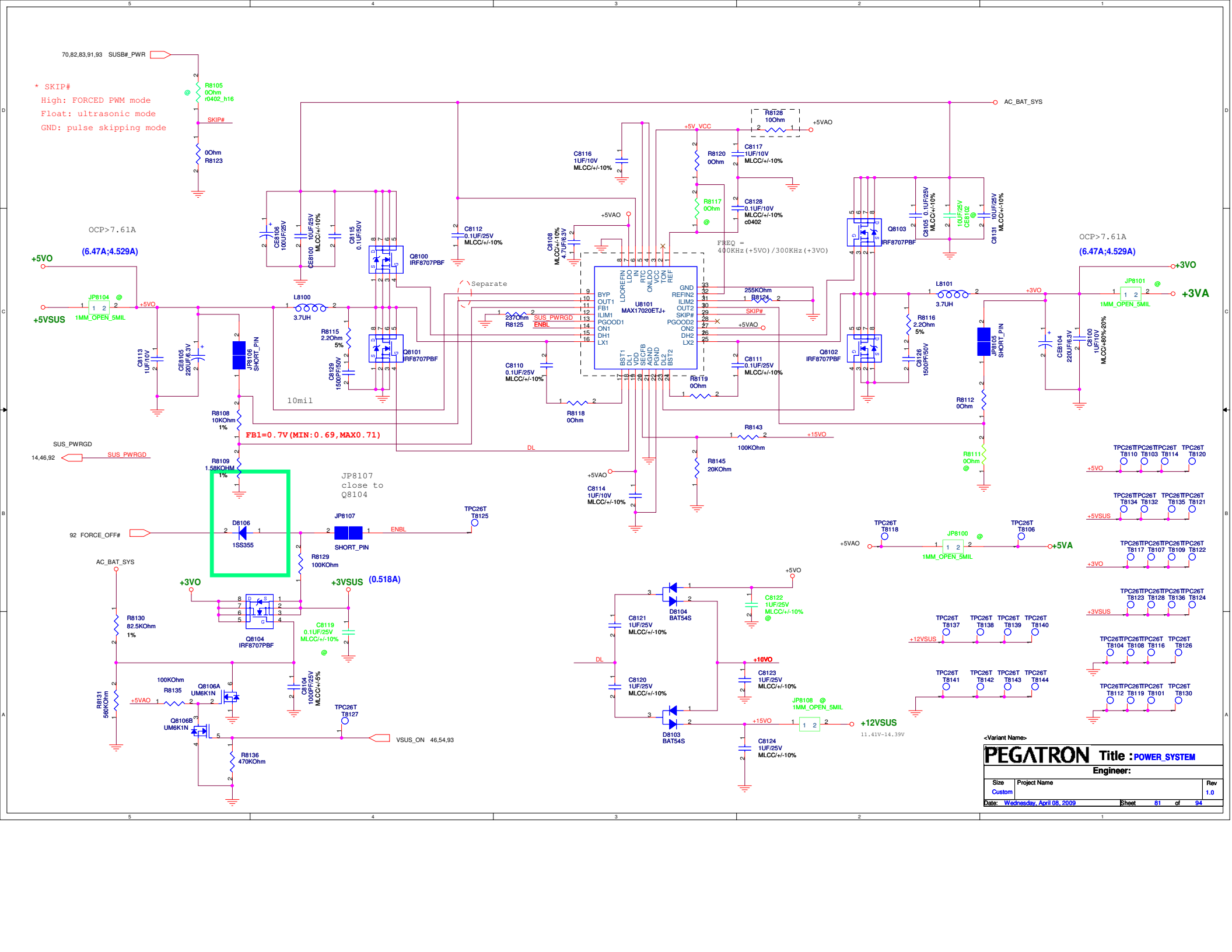
Date: Thursday, March 05, 2009 Sheet 79 of 100


U8000
ISL6260CCRZ-T
U8001
ISL6208CRZ
U8002
ISL6208CRZ
U8003
ISL6208CRZ
(64A)
+VCORE
090402
PCPU_GND1
PCPU_GND2
PCPU_GND3
AC_BAT_SYS
+5VS
+3VS
VCC_PRM
Disable PWM3
R8036 for load line
for transient response
Close to Phase 1 Inductor
PEGATRON
Title : power Vcore
Pegatron power Team
Engineer: Andrew1_Liu
Size: Custom
Project Name: G60VX
Rev: R 1.2
Date: Wednesday, April 08, 2009
Sheet 80 of 94

+2.5VS



PEGATRON	Title : POWER_I/O_+2.5VS	
Pegatron power Team	Engineer: Andrew1_Liu	
Size: Custom	Project Name: G60VX	Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 80 of 94	


70,82,83,91,93 SUSB#_PWR
* SKIP#
High: FORCED PWM mode
Float: ultrasonic mode
GND: pulse skipping mode
R8105 0Ohm r0402_h16
SKIP#
0Ohm R8123
OCP>7.61A
(6.47A;4.529A)
+5VO
+5VSUS
JP8104
1MM_OPEN_5MIL
L8100 3.7UH
CE8106 100UF/25V
CE8100 10UF/25V MLCC/+/-10%
C8115 0.1UF/50V
Q8100 IRF8707PBF
C8112 0.1UF/25V MLCC/+/-10%
Separate
C8113 1UF/10V
CE8105 220UF/6.3V
JP8106 SHORT_PIN
R8115 2.2Ohm 5%
C8129 1500PF/50V
Q8101 IRF8707PBF
10mil
R8108 10KOhm 1%
FB1=0.7V(MIN:0.69,MAX0.71)
SUS_PWRGD
14,46,92
SUS_PWRGD
R8109 1.58KOHM 1%
JP8107
close to
Q8104
D8106 1SS355
92 FORCE_OFF#
JP8107
SHORT_PIN
ENBL
TPC26T T8125
R8129 100KOhm
AC_BAT_SYS
+3VO
+3VSUS (0.518A)
R8130 82.5KOhm 1%
Q8104 IRF8707PBF
C8119 0.1UF/25V MLCC/+/-10%
100KOhm R8135
Q8106A UM6K1N
Q8106B UM6K1N
+5VAO
R8131 560KOhm
C8104 1000PF/25V MLCC/+/-5%
TPC26T T8127
VSUS_ON 46,54,93
R8136 470KOhm
C8108 MLCC/+/-10% 4.7UF/6.3V
+5VAO
+5V_VCC
R8126 10Ohm
+5VAO
C8116 1UF/10V MLCC/+/-10%
R8120 0Ohm
C8117 1UF/10V MLCC/+/-10%
R8117 0Ohm
C8128 0.1UF/10V MLCC/+/-10% c0402
FREQ = 400KHz(+5VO)/300KHz(+3VO)
U8101 MAX17020ETJ+
BYP OUT1 FB1 ILIM1 PGOOD1 ON1 DH1 LX1
LDOREFIN LDO IN RTC ONLDO VCC TON REF
GND REFIN2 ILIM2 OUT2 SKIP# PGOOD2 ON2 DH2 LX2
BST1 DL1 SECFB AGND PGND DL2 BST2
237Ohm R8125
SUS_PWRGD
ENBL
255KOhm R8124
SKIP#
+5VAO
C8110 0.1UF/25V MLCC/+/-10%
R8118 0Ohm
R8119 0Ohm
C8111 0.1UF/25V MLCC/+/-10%
Q8102 IRF8707PBF
Q8103 IRF8707PBF
C8105 0.1UF/25V MLCC/+/-10%
CE8102 10UF/25V
C8131 10UF/25V MLCC/+/-10%
AC_BAT_SYS
OCP>7.61A
(6.47A;4.529A)
+3VO
L8101 3.7UH
JP8101
+3VA
1MM_OPEN_5MIL
R8116 2.2Ohm 5%
C8126 1500PF/50V
JP8105 SHORT_PIN
CE8104 220UF/6.3V
C8100 1UF/10V MLCC+80%-20%
R8112 0Ohm
R8111 0Ohm
R8143 100KOhm
+15VO
R8145 20KOhm
+5VAO
C8114 1UF/10V MLCC/+/-10%
TPC26T T8118
JP8100
TPC26T T8106
+5VAO
+5VA
1MM_OPEN_5MIL
C8121 1UF/25V MLCC/+/-10%
D8104 BAT54S
C8122 1UF/25V MLCC/+/-10%
DL
C8120 1UF/25V MLCC/+/-10%
+10VO
C8123 1UF/25V MLCC/+/-10%
JP8108
1MM_OPEN_5MIL
D8103 BAT54S
+15VO
C8124 1UF/25V MLCC/+/-10%
+12VSUS
11.41V~14.39V
TPC26T T8110 T8103 T8114 T8120
+5VO
TPC26T T8134 T8132 T8135 T8121
+5VSUS
TPC26T T8117 T8107 T8109 T8122
+3VO
TPC26T T8123 T8128 T8136 T8124
+3VSUS
TPC26T T8137 T8138 T8139 T8140
+12VSUS
TPC26T T8104 T8108 T8116 T8126
TPC26T T8141 T8142 T8143 T8144
TPC26T T8112 T8119 T8101 T8130
<Variant Name>
PEGATRON
Title : POWER_SYSTEM
Engineer:
Size Custom
Project Name
Rev 1.0
Date: Wednesday, April 08, 2009
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* Rocset = Ioc * DRC / 10uA

+1.5VO: ROCSET = R8213 ; R8215 = R8213=10KOhm

+1.05VO: ROCSET = R8212 ; R8212=R8211=10KOhm

* VREF = 0.6V+-1%

+1.5VO = VREF * (R8206 + R8214) / R8214 =1.52V+-2.26%

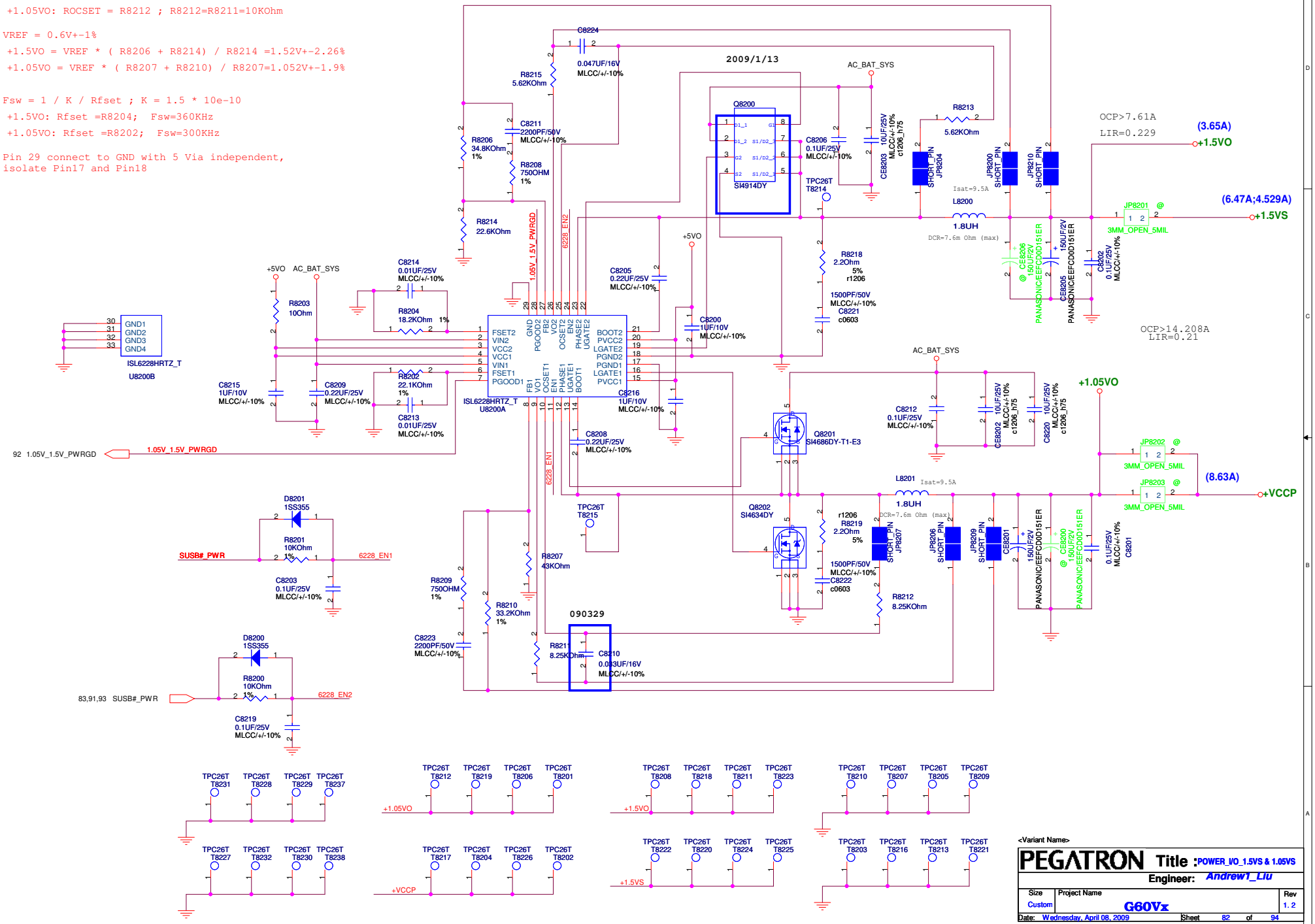
+1.05VO = VREF * (R8207 + R8210) / R8207=1.052V+-1.9%

* Fsw = 1 / K / Rfset ; K = 1.5 * 10e-10

+1.5VO: Rfset =R8204; Fsw=360KHz

+1.05VO: Rfset =R8202; Fsw=300KHz

* Pin 29 connect to GND with 5 Via independent, isolate Pin17 and Pin18



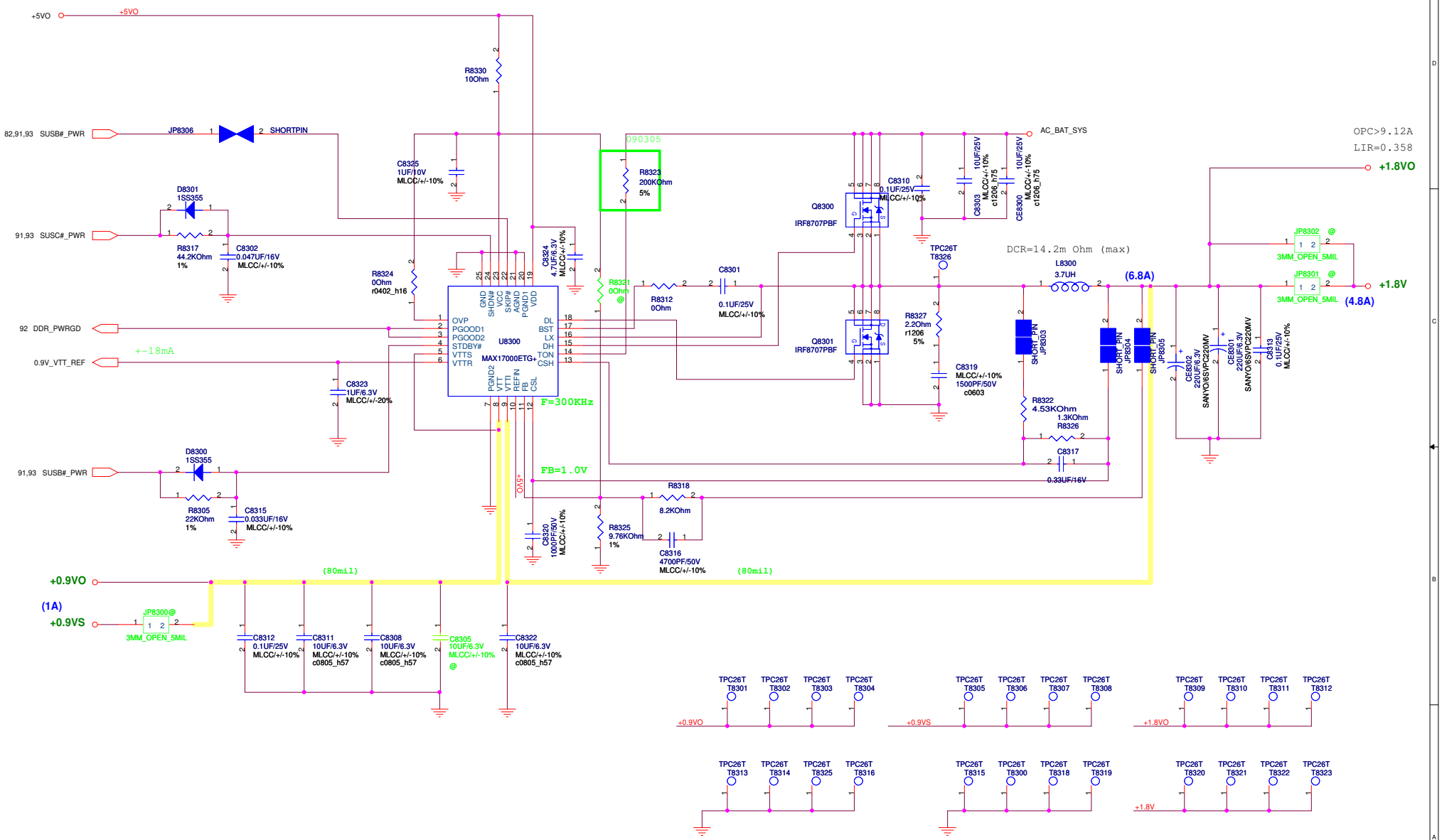
<Variant Name>

PEGATRON Title : POWER_I/O_1.5VS & 1.05VS

Engineer: Andrew1_Liu

Size	Project Name	Rev
Custom	G60Vx	1. 2

Date: Wednesday, April 08, 2009 Sheet 82 of 94



<Variant Name>

PEGATRON Title : POWER_I/O_DDR & VTT

Engineer: Andrew1_Liu

Size	Project Name	Rev
Custom	G60Vx	1.2

Date: Wednesday, April 08, 2009 Sheet 83 of 94

PEGATRON Title : N/A

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
C	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 85 of 100

POWER PATH & BAT_LEARN

120W&90W:R8801=15mOHM(10G21DR01515110)

65W: R8801=20mOHM(10G21DR02015110)

032108

080214 Snubber

1.10 Ohm,0.1uF/50V(p)
2.4.7Ohm,1uF/50V(s)
3.10 Ohm,1uF/50V

120W: R8832 = 1.82K
90W: R8832 = 6.98K
65W: R8832 = 17.8K

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

12/16 change

12/16 change

2008/09/12

090305

MAX17005=>R8813=1MOhm(@)
MAX17015=>R8813=0 Ohm

MAX17015 change MAX17005 List
R8805=100K 0.1%--->0 ohm
R8804=20K 0.1%--->@
R8813=0 ohm--->1.69M ohm
R8815=@--->130K ohm

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [60mV/Rsense(ADin)]*[1+(Rb/Ra)]
Rsense(ADin)=20m ohm
Ra=R8832=17.8K ohm;Rb=R8843=1K ohm
=> Iin(max)=3.168A
=> Constant Power = 19V * 3.168A = 60.2W

Charge Current Ichg = [240mV/Rsense(CHG)]*[VISET/VAA]
Rsense(CHG)=R8842=10m ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Precgarge current=150mA

2.4V<VCTL<4.2V=>3cell=>Vcell =4.2V+(4.2V-VVCTL)/6
3 cell=>VCTL= 3.9V => Vcell = 4.635V
0V<VCTL<1.8V=>4cell=>Vcell =4.2V+(VVCTL/6)
4 cell=>VCTL= 0.3V => Vcell = 4.635V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

VCTL = 3.9V; CHG VOLTAGE = 4.25/CELL(3 CELL)

PEGATRON	Title : POWER_CHARGER		
Pegatron power Team	Engineer: Andrew1_Liu		
Size: C	Project Name: G60VX		Rev: R1.2
Date: Wednesday, April 08, 2009	Sheet 86 of 94		

PEGATRON Title : N/A

Pegatron BU2 HW Team 3 Engineer:

Size	Project Name	Rev
A	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 87 of 100

PEGATRON Title : N/A

Pegatron BU2 HW Team 3 Engineer:

Size	Project Name	Rev
A	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 88 of 100

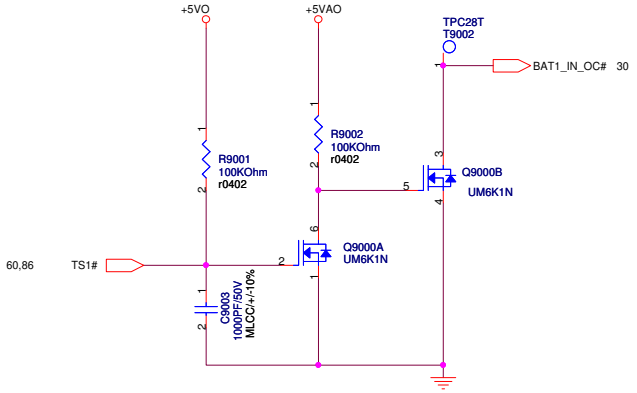
PEGATRON Title : N/A

Pegatron BU2 HW Team 3 Engineer:

Size	Project Name	Rev
A	G60VX	R 1.2

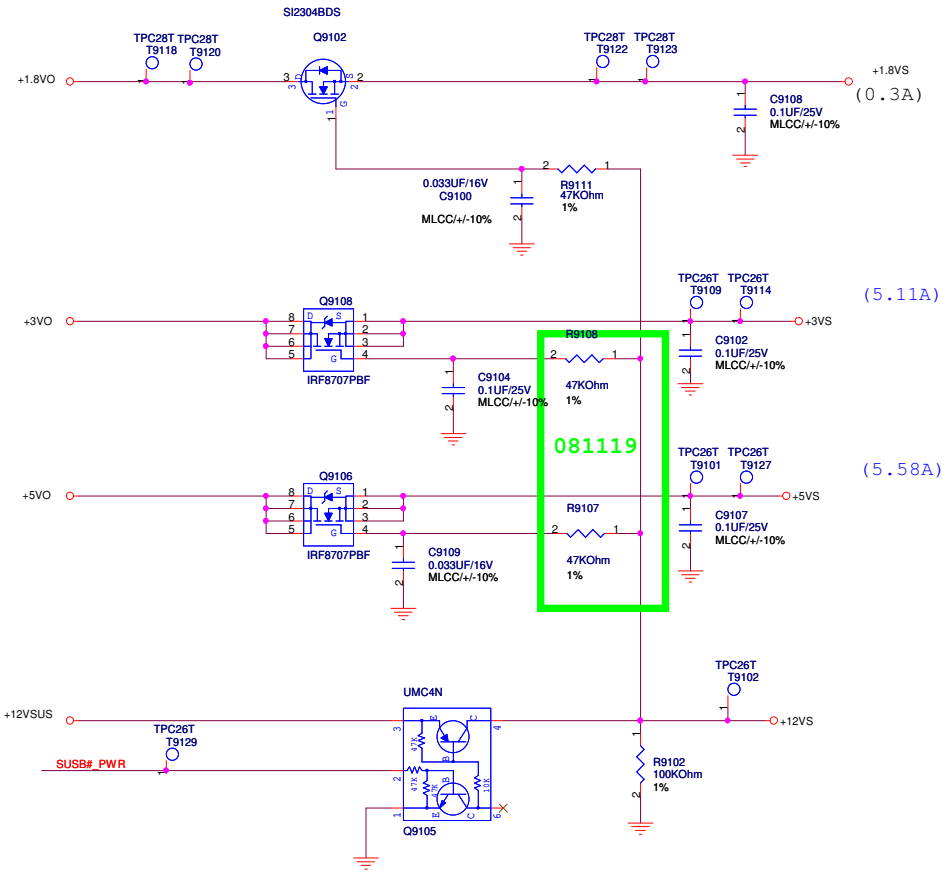
Date: Thursday, March 05, 2009 Sheet 89 of 100

BATTERY IN DETECT

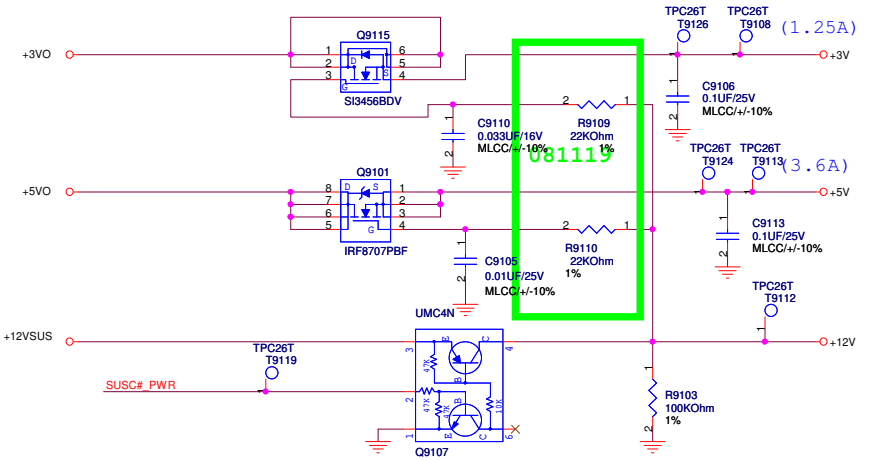


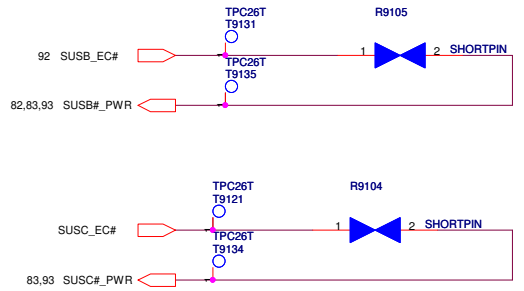
PEGATRON	Title : POWER_DETECT		
Pegatron power Team	Engineer: Andrew1_Liu		
Size: Custom	Project Name: G60VX		Rev: R 1.2
Date: Wednesday, April 08, 2009	Sheet 90 of 94		

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

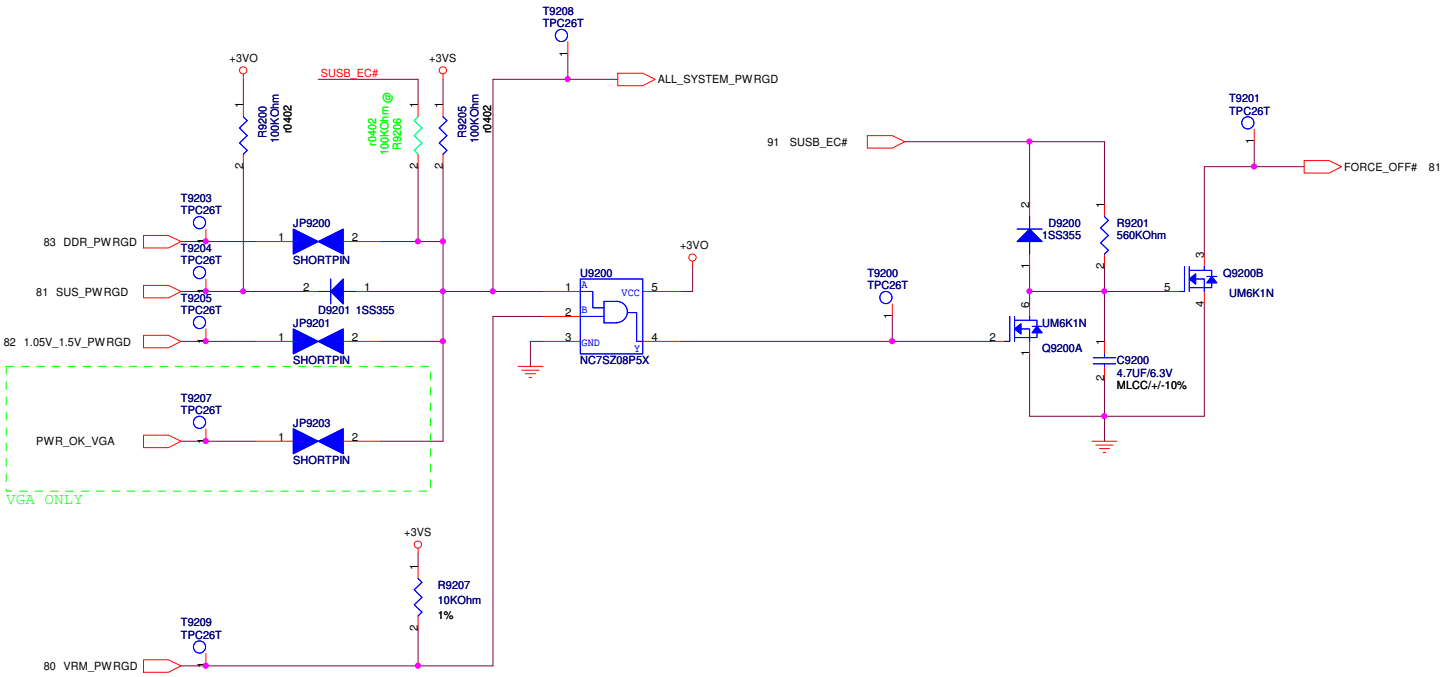
PEGATRON Title :POWER_LOAD SWITCH

Engineer: Andrew1_Liu

Size	Project Name	Rev
Custom	G60Vx	1.2

Date: Wednesday, April 08, 2009 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON Title :POWER_PROTECT

Engineer: Andrew1_Liu

Size	Project Name	Rev
Custom	G60Vx	1.2

Date: Wednesday, April 08, 2009 Sheet 92 of 94

AC_BAT_SYS — AC_BAT_SYS 80,81,82,83,88

BAT — BAT 88

BAT_CON — BAT_CON 88

+3VA — +3VA 81

+5VAO — +5VAO 81,90

+5VA — +5VA 81

+5VO — +5VO 81,82,83,90,91

+3VO — +3VO 81,91

+1.8VO — +1.8VO 83

+0.9VO — +0.9VO 83

+1.05VO — +1.05VO 80,82

+1.5VO — +1.5VO 82

+5VSUS — +5VSUS 81

+3VSUS — +3VSUS 81,92

+12VSUS — +12VSUS 81,91

+5V — +5V 91

+3V — +3V 91

+12V — +12V 91

+1.8V — +1.8V 83

+3VS — +3VS 80,91,92

+5VS — +5VS 80,91

+12VS — +12VS 91

+1.5VS — +1.5VS 82

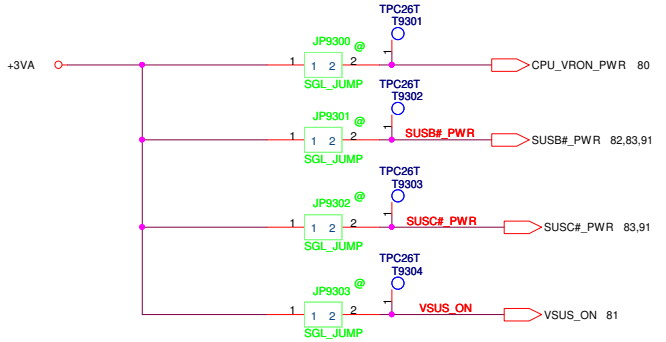
+0.9VS — +0.9VS 82

+1.8VS — +1.8VS 82

+VCCP — +VCCP 82

+VCORE — +VCORE 80

FOR POWER TEST



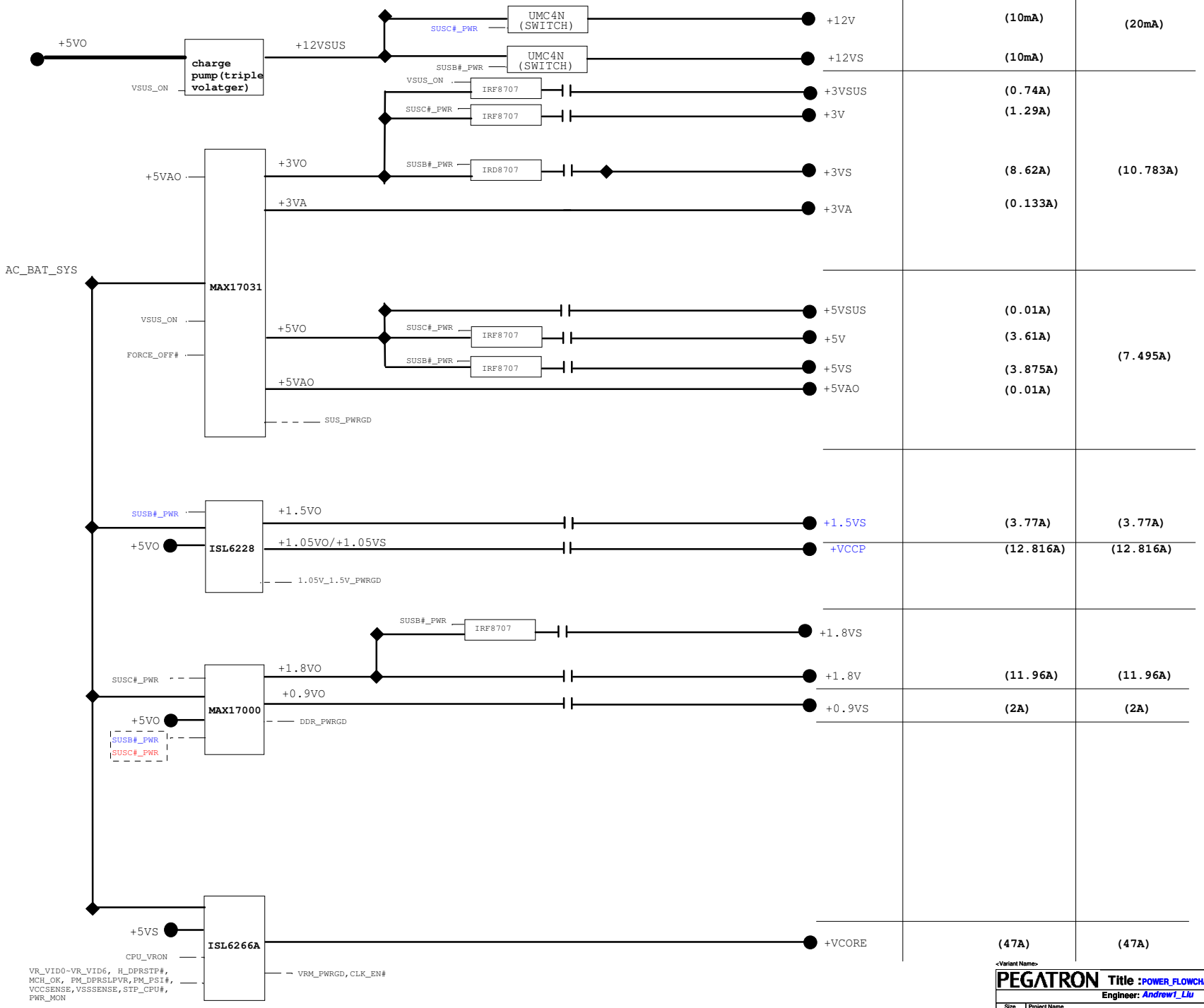
<Variant Name>

PEGATRON Title :POWER_SIGNAL

Engineer: Andrew1_Liu

Size	Project Name	Rev
Custom	G60Vx	1.2

Date: Wednesday, April 08, 2009 Sheet 93 of 94



<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: Andrew1_Liu

Size	Project Name	Rev
Custom	G60Vx	1.2

Date: Wednesday, April 08, 2009 Sheet 94 of 94

PEGATRON Title : N/A

Pegatron BU2 HW Team 3 Engineer:

Size	Project Name	Rev
A	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 95 of 100

Rev	Date	Description
R1.0		First Release!
R1.1		

Rev	Date	Description

PEGATRON Title : Revision History

Pegatron BU2 HW Team 3 Engineer:

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 96 of 100

R1.0

Item	Before	After	Reason	Owner	Date
	R8036:10.5k	R8036 change to 8.87k	To change VCORE load line to meet Intel spec.	Eve Kuo	2008/02/25
	R8015:0805	R8015 from 0805 --> 0603	0805 is common component to use.	Eve Kuo	2008/02/25
	Q8612, R8628, R8629	De-pop Q8612, R8628, R8629	G50V support 3S battery	Eve Kuo	2008/02/25

R1.1

Item	Before	After	Reason	Owner	Date
	JP8601,JP8606	Delete JP8601,JP8606	Due to the factory's requirement, the bead and jump won't be co-lay.		

R2.0

Item	Before	After	Reason	Owner	Date

PEGATRON Title : POWER_HISTORY

Pegatron BU2 HW Team 3 Engineer:

Size	Project Name	Rev
Custom	G60VX	R 1.2

Date: Thursday, March 05, 2009 Sheet 97 of 100

I/O Board

R1.1

+5V_USB_IO
+3VS_IO
IOJ101
WTOB_CON_20P
USB_PN0_IO
USB_PP0_IO
USB_PN1_IO
USB_PP1_IO
HP_JD_IO
SPDIF_JD_IO
LINE1_JD_IO
MIC_JD_IO
SPDIF1_OUT_IO
HP_R_IO
HP_L_IO
LINEIN_R_IO
LINEIN_L_IO
MIC_IO
SIDE1
SIDE2
GND_IO
IO_R117 0Ohm
GND_ADO

G50VX R1.1: Follow M52VF

USB_PN0_IO — IO_RNX101B 0Ohm — USB_PN0_IO_CON
USB_PP0_IO — IO_RNX101A 0Ohm — USB_PP0_IO_CON
IO_LX101 90Ohm/100Mhz

USB_PN1_IO — IO_RNX102B 0Ohm — USB_PN1_IO_CON
USB_PP1_IO — IO_RNX102A 0Ohm — USB_PP1_IO_CON
IO_LX102 90Ohm/100Mhz

USB Port 0

+5V_USB_IO — IO_R115 0Ohm — USB_PN0_IO_CON / USB_PP0_IO_CON
IO_CE101 47UF/6.3V
IO_C101 0.1UF/16V
IOJ102 USB_CON_1X4P (P_GND4, P_GND3, P_GND2, P_GND1)
IO_D102, IO_D101 0603-050E101NP-LF
GND_IO

USB Port 1

R2.0
+5V_USB_IO — IO_R116 0Ohm — USB_PN1_IO_CON / USB_PP1_IO_CON
IO_CE102 150UF/6.3V
IO_C102 0.1UF/16V
IOJ103 USB_CON_1X4P (P_GND4, P_GND3, P_GND2, P_GND1)
IO_D104, IO_D103 0603-050E101NP-LF
GND_IO

Headphone & S/PDIF Jack

R2.0
HP1_IN#_IO
JACK_IN#_IO
HP_R_IO — IO_R105 0Ohm — HP_R_CON_IO
HP_L_IO — IO_R106 0Ohm — HP_L_CON_IO
IO_C103 100PF/50V
IO_C104 100PF/50V
GND_ADO
+3VS_SPDIF_IO
SPDIF1_OUT_IO — IO_R107 0Ohm — IO_R108 0Ohm — SPDIFOUT_IO
IO_C105 0.1UF/16V
IO_C106 100PF/50V
IOJ104 PHONE_JACK_8P
0Ohm IO_R120
0Ohm IO_R119
GND_ADO GND_IO

+5V_USB_IO +5V_USB_IO +3VS_IO +3VS_SPDIF_IO
IO_R112 100KOhm
IO_R113 100KOhm
UMC4N
IO_Q103 2N7002
SPDIF_JD_IO
HP_JD_IO
IO_Q101A UM6K1N
IO_Q101B UM6K1N
HP1_IN#_IO
JACK_IN#_IO
IO_Q102
GND_IO

IO_D105 TVM0G5R5M411R
IO_C111 1000PF/50V
IO_C110 1000PF/50V
IO_D106 TVM0G5R5M411R
GND_ADO GND_IO

Add IO_D105, IO_D106 for ESD protection
Change IO_C111 and IO_C110 GND to GND_IO from GND_ADO for layout
G60VX R1.2 20090304

Line-in Jack

LINEIN_R_IO — IO_R109 0Ohm — LINEIN_R_CON_IO
LINEIN_L_IO — IO_R110 0Ohm — LINEIN_L_CON_IO
LINE1_JD_IO
IO_C107 100PF/50V
IO_C108 100PF/50V
IO_C112 1000PF/50V
IOJ105 AUDIO JACK PHONE_JACK_6P
GND_ADO

Left Screw Hole

IO_H1
2DRILL
GND_IO

Right Screw Hole

IO_H2
2DRILL
GND_IO

G50VX MB R1.1: change MIC_VREFOUTand pull high resistor form page98 to page36

MIC In Jack

MIC_IO — IO_R111 0Ohm — MIC_CON_IO
MIC_JD_IO
IO_C109 100PF/50V
IO_C113 1000PF/50V
IOJ106 AUDIO JACK PHONE_JACK_6P
GND_ADO

IO_R118 @ 0Ohm
IO_C114 1000PF/50V @
GND_ADO GND_IO

G50VX R1.1: Follow M52VF to isolate the digital noise from the audio device

PEGATRON Title : IO_USB & Audio Jack
Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo
Size: Custom | Project Name: G60VX | Rev: R 1.2
Date: Wednesday, March 11, 2009 | Sheet 98 of 100

R1.0

R1.1

2008/02/18	1. Change the port of SATA ODD and SATA HDD to meet design IP. (Page 51)
	2. Change SMBus of the Cap-sense Touch key from SMB0 to SMB1. (Page 56)
	3. Correct the signals of ESATA. (Page 66)
	4. Set R3318 as mount. (Page 33)
	5. Correct the signals of PCIE of WLAN. (Page 53)
	6. Correct the signals of PCIE of TV Tuner and add the reset signal for PCIE TV Tuner. Set the 1.5V power rail as mount. (Page 64)
	7. Unmount pull up resisters of 1394_SCL and 1394_SDA. (Page 40)
	8. Add common choke on CMOS for EMI requirement. (Page 45)
	9. Correct the signals of Newcard Debug Card. (Page 44)
	10. Change the R1407 to 1206 size. (Page 14)
2008/02/20	11. Change EC to 8512. (Page 30)
	12. Pull BAT2_IN_OC# up to fix CHARGER_LED bug. (Page 30)
2008/02/21	13. Delete the LCD_BL_DA signal which is designed for Light Sensor. (Page 45)
	14. Change the R4504 to 100K to fix LCD will display white screen when system boots. (Page 45)
	15. Add uP schematic to control the Game LED for PM request. (Page 69 & 24)
2008/03/05	16. Add discharge circuit for 2.5VS (Page 57)
	17. Change BT and WLAN ON/OFF control method (Page 53 and 61)
	18. Add ESD Protected Diode on SATA ODD and E-SATA(Page 51 and 66)
2008/03/11	19. Change PEG CLK Source on Clock Gen(Page 29)
2008/03/14	20. Change TouchPad Connector. (Page 31)
2008/03/18	21. Add 2 diodes to follow EC suggestion. (Page 22)
	22. Change the IO Connector. (Page 65, 98)
	23. Change Power Circuit. (Page 80-94)
	24. Exchange CLK_ICHPCI and CLK_KBCPCI to follow Design IP setting. (Page 30)
	25. Swap USB Ports to follow Design IP. (Page 45, 52, 64, 68,)
2008/03/19	26. Add 0OHM resistor between thermal sensor and CPU to follow Intel Design Guide. (Page 50)
	27. Add a N-MOS between U4401 and PCI_WAKE# to prevent system can't enter S4 which is waked by U4401. (Page 44)
2008/03/24	28. Add +3VSUS to NewCard Power Switch. (Page 43)
	29. Change the pull-up power source of SMB1 to +3VS. (Page 30)
2008/03/26	30. Change HDD Connector. (Page 51)
	31. Add EMI Solution on LVDS connector. (Page 45)
	32. Change the Ground of DC Jack for EMI. (Page 60)
	33. Add EMI Solution on USB connector. (Page 52)
	34. Add EMI Solution on HDMI connector. (Page 48)
	35. Add EMI Solution on IO connector. (Page 65)
	36. Add EMI Solution on HDD connector. (Page 51)
	37. Add EMI Solution on T/P connector. (Page 31)
2008/05/02	38. Correct the Headphone Jack Detect schematic. (Page 98)
	39. Change capacitor to MLCC. (Page 33)
2008/05/04	40. Add over-clock strapping. (Page 29)
2008/05/06	41. Reserve Finger Printer Schematic. (Page 63)
	42. Add Amplifer strapping. (Page 37)
	43. Remove the Capacitor of headphone. (Page 37)

G50VX

2008/11/17	3. Add comment for supporting Quad Core CPU. (Page 3)
	4. Reserve R0411 for support Quad Core, Add BOM option for DC/QC. (Page 4)
	5. Add comment for DC/QC. (Page 5)
	10. Add comment for DC/QC. (Page 10)
	20. Add comment for delete Modem function. (Page 20)
	21. Add comment for BOM option. (Page 21)
	29. Add comment for CLK Gen BOM option. (Page 29)
	30. Change: add Keyboard_LED conntrol signal. (Page 30)
	31. Add keyboard LED Power connector, Add comment for delete CIR BOM option (31)
	34. Add BOM option for delete RJ11 (34)
	35. Add BOM option for delete Modem function (35)
	36. Add BOM option for ALC662 and ALC663 co-lay (36)
	38. Add BOM option for supporting Array MIC (38)
	44. Add BOM option for supporting Debug Connector (44)
	45. Add BOM option for supporting Array MIC (45)
	50. Add BOM option for Thermal Sensor for QC and DC (50)
	63. Add BOM option for deleting FP function. (63)
	68. Add BOM option for deleting OLED connector. (68)
	69. Co-using of EC.GPA3 pin, for G50V reserved for controlling GAME_LED#. (69)
2008/11/24	31. Change J3103 Pin5, 6 GND name from GND_POWER to GND. (31)
	30. Change net GAME_LED_EC# from connecting with EC.GPA3 to EC.GPA6.(30)
	68. Delete all the content of page 68: OLED Connector.(68)
2008/11/25	21.Add TP to USBP9N/P.(21)
	45.Add F4502 to protect the M/B from demaging by AC_BAT_SYS_INV short to GND; Change C4513 from 0.1UF/16V to 0.1UF/25V.(45) 2008-11-25-21-06
2008/11/26	14.Change C1447 from 0805 to 0603 to satisfy the mechinical height constrain.(14)
2008/12/31	80.Change power solution, related page is 80-84, 86, 90-94
2009/1/2	60.Replace D6002,D6003,D6004 with integrated D6002 for improving the rise time
	70.Reserve R7007 for AMD M96 VGA card
	33.Add R3323 to reduce the LAN power consumption ?
2009/1/4	36.Change MIC_VREFOUT and 4.7k ohm pull high resistor from page98 to page36, related page is 98, 65, 36
	98.isolate the GND_AUDIO and GND_IO
	23.Folow Intel DG R2.2, change C2301 from 0.1UF/16V X7R-->1UF/10V X5R
	38.change the DSP VDD power to +1.5VS for better immunity of noise and less power
	31.change the keyboard connector pin define for chocolate keyboard
2009/1/8	21.Swap USB port 4 and 8, Camera use port 8, newcard use port 4, to decrease the EMI of camera when USB HDD is also used
	80.power team update the schematic
2009/1/13	31.Keyboard signal swap for capacitor layout
	30.Change EC pin GPH3/ID3 from BAT_LEARN to T3011, delete BAT_LEARN signal
	80,81,84. Add net CLK_EN#; Change U8101 symbol; Add R8404
	31.Keyboard connector signal change back

PEGATRON Title : System History 1

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

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G60VX R1.2

2009/03/05	Page 23: R2319, R2320 change to 100 ohm (Follow Intel DG R2.2)
	Page 32: Reserve Force_off# connect to EC_RST#
	page 41/42: Reserve 10pf capacitor for SD card CLK for EMI
	Page 43: Add MOS to prevent the leakage current from +3VSUS (U4301 pin 17) to BUF_PLT_RST#
	page 45: Reserve 33pf capacitor for PWR_LED#, GAME_LED# for EMI
	Page 45: Change R4501, mount C4503 to tune the falling time of +3VS_LCD
	Page 46: Follow M52V to change the schematic of RGB to tune the rise/fall time
	Page 46: Add schematic to protect the HSYNC/VSYNC from pulling low by CRT connector for M52VP
	Page 48: Reserve schematic for G50VX HDMI HPD signal level shift
	Page 48: Reserve pull high resistor and decoupling capacitor for TMDS signals
	Page 53: change WLAN pin 39,41 from NC to 3.3V power for full support Intel WiFi Link
	Page 69: Change GAME_LED# control from PIC MCU to EC
	Page 70: Reserve bead for MXM card for EMI
	Page 81: Reserve D8107 to prevent leakage from +3V, +3VS to +3VSUS and ENBL when VSUS_ON accidentally pulled low
	Page 98: Reserve VPORT (varistor) on signal HP1_IN#_IO and JACK_IN#_IO for ESD protection

PEGATRON Title : System History 2

Pegatron BU2 HW Team 3 Engineer: Kevin1_Guo

Size	Project Name	Rev
Custom	G60VX	R 1.2

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