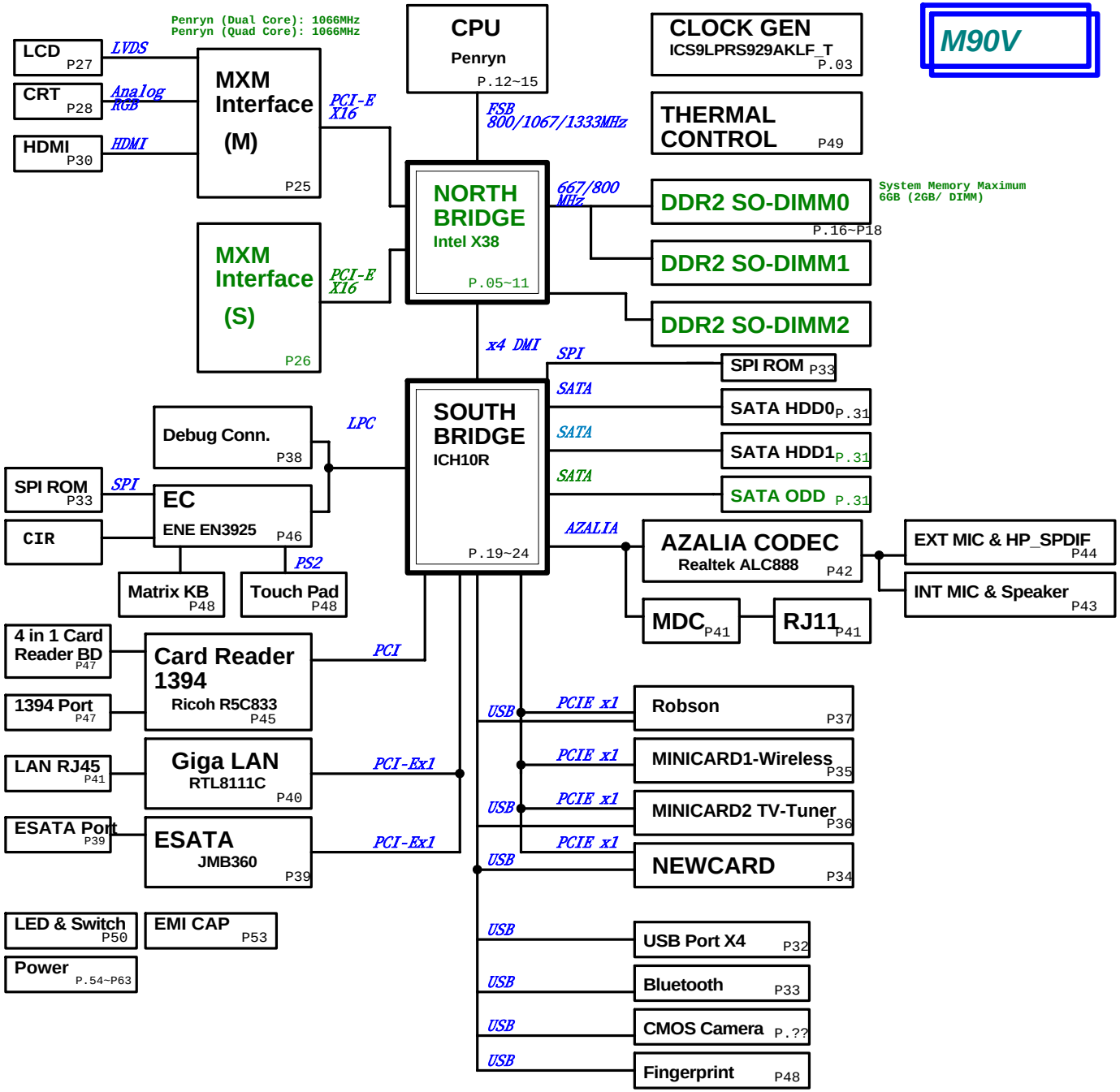
M90V

2.0G
2008_0519



<Variant Name>

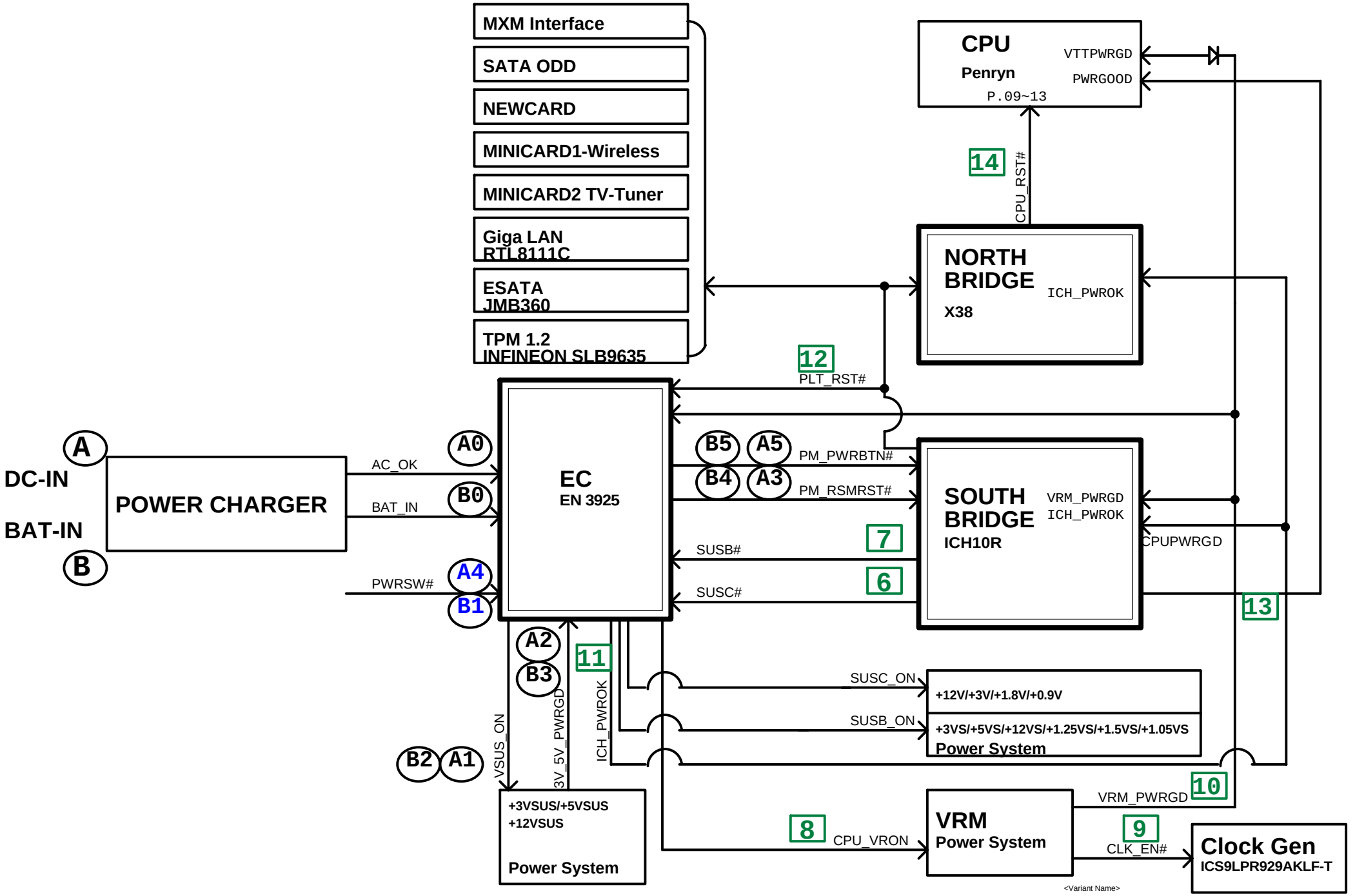
ASUSTek Computer Inc.

Title : Block Diagram

Engineer: Alan Chen

Size	Project Name	Rev
Custom	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 1 of 65



<Variant Name>

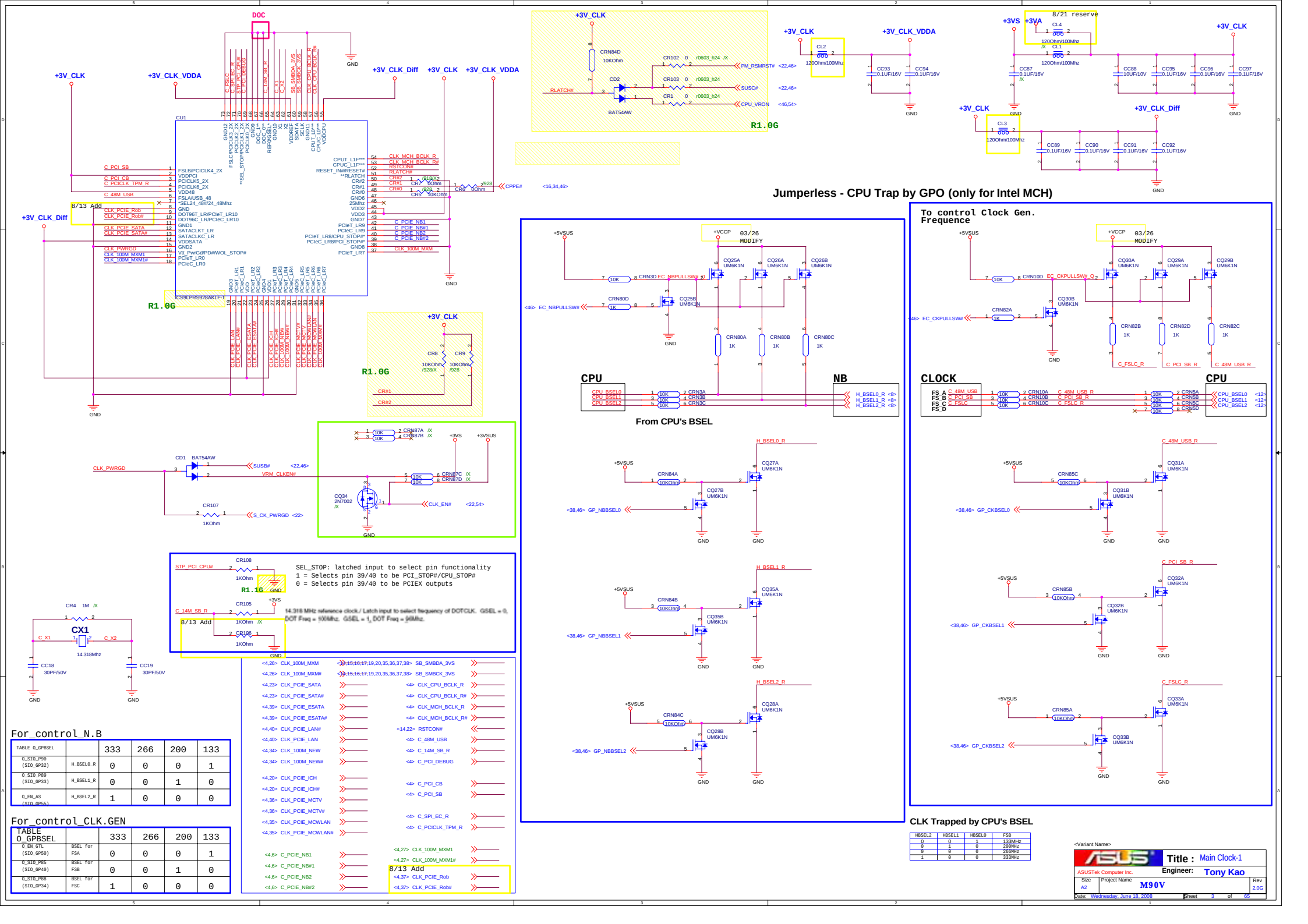
ASUSTek Computer Inc.

Title : Power Sequence

Engineer: Alan_Chen

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 2 of 65



For_control_N.B

TABLE 0_GPBSEL		333	266	200	133
0_SIO_P90 (SIO_GP32)	H_BSEL0_R	0	0	0	1
0_SIO_P89 (SIO_GP33)	H_BSEL1_R	0	0	1	0
0_EN_AS (SIO_GP55)	H_BSEL2_R	1	0	0	0

For_control_CLK.GEN

TABLE 0_GPBSEL		333	266	200	133
0_EN_GTL (SIO_GP50)	BSEL for FSA	0	0	0	1
0_SIO_P85 (SIO_GP40)	BSEL for FSB	0	0	1	0
0_SIO_P88 (SIO_GP34)	BSEL for FSC	1	0	0	0

CLK Trapped by CPU's BSEL

HBSEL2	HBSEL1	HBSEL0	FSB
0	0	1	133MHz
0	1	0	200MHz
0	0	0	266MHz
1	0	0	333MHz

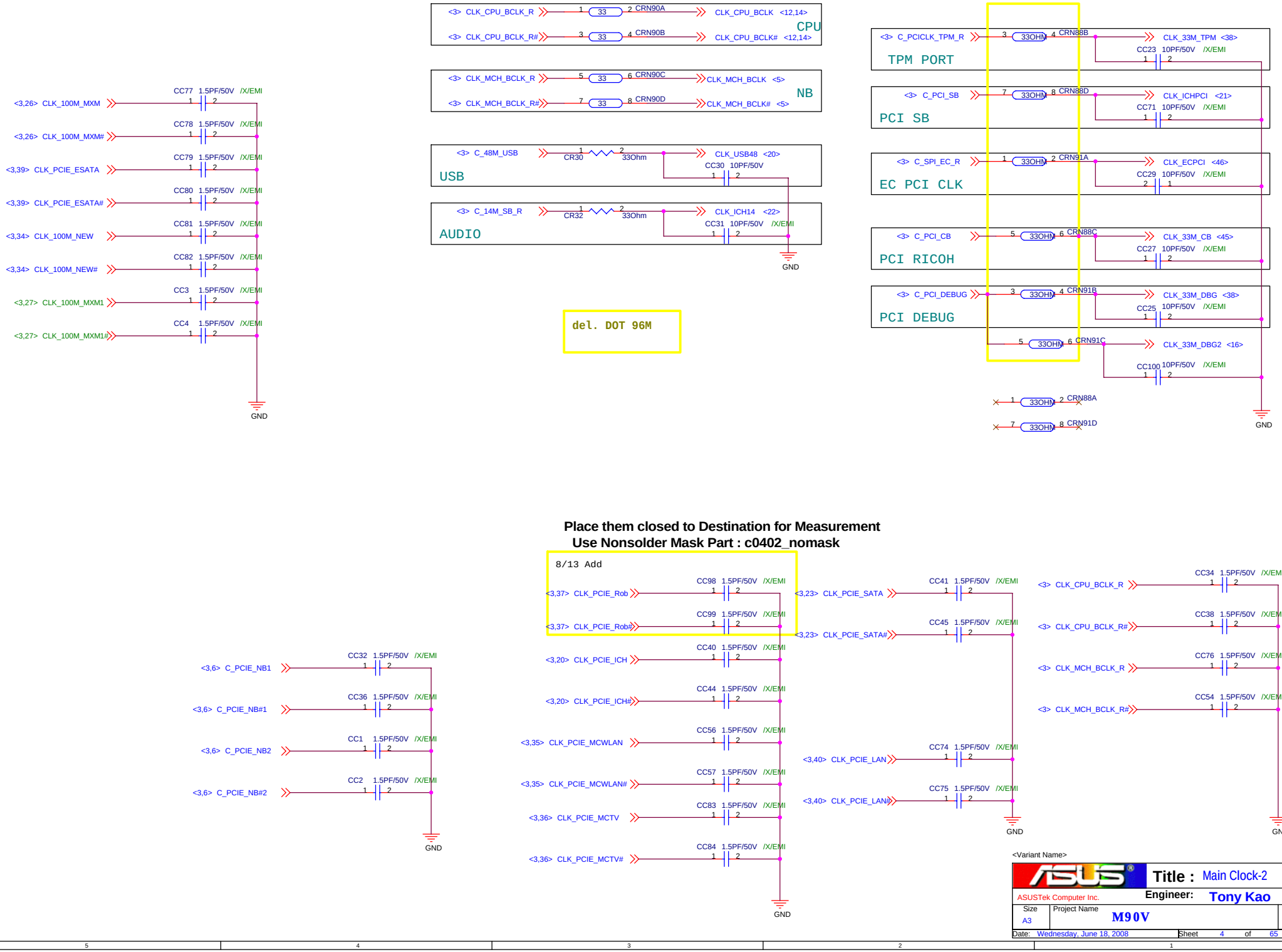
<Variant Name>

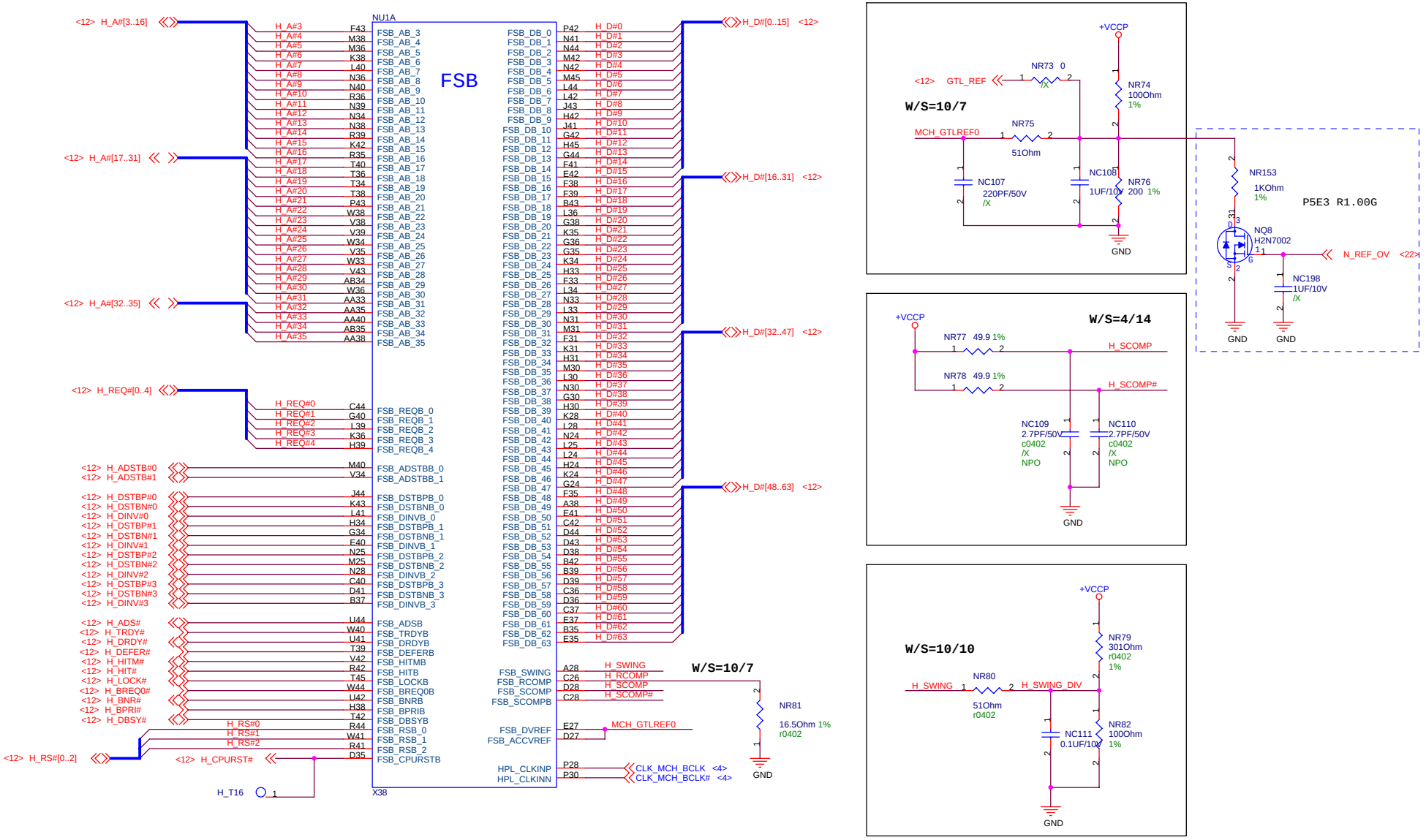
Title : Main Clock-1

ASUSTek Computer Inc. Engineer: Tony Kao

Size A2 | Project Name M90V | Rev 2.0G

Date: Wednesday, June 18, 2008 | Sheet 3 of 65


CPU
NB
USB
AUDIO
TPM PORT
PCI SB
EC PCI CLK
PCI RICOH
PCI DEBUG
del. DOT 96M
Place them closed to Destination for Measurement
Use Nonsolder Mask Part : c0402_nomask
8/13 Add
GND
<Variant Name>
Title : Main Clock-2
ASUSTek Computer Inc.
Engineer: Tony Kao
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 4 of 65



<Variant Name>

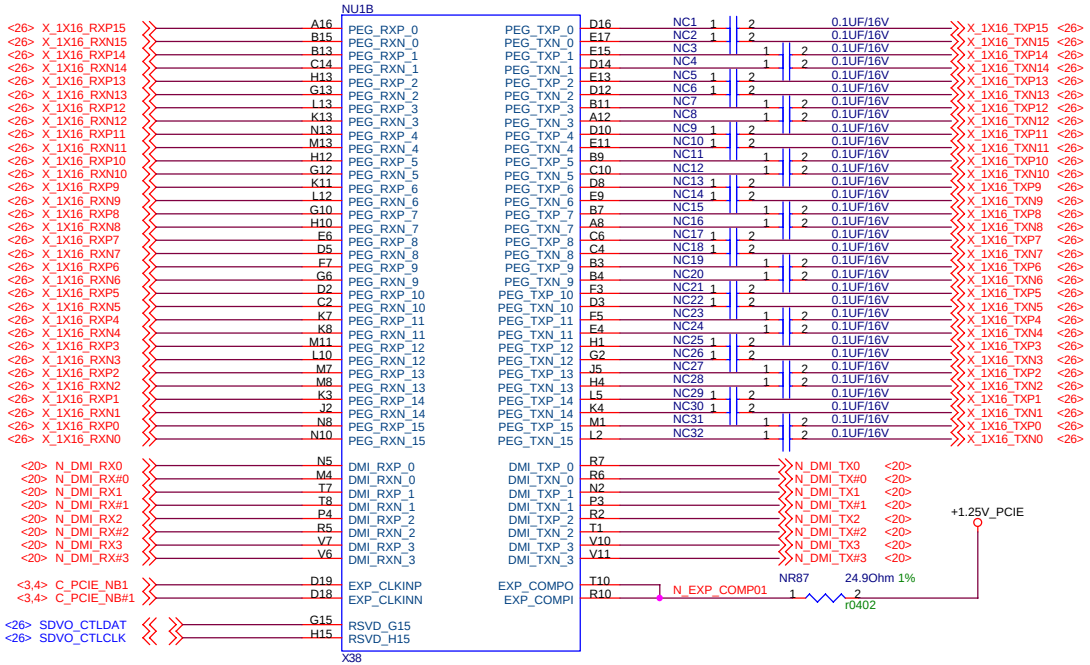
Title : BEARLAKE-X-1

ASUSTek Computer Inc.

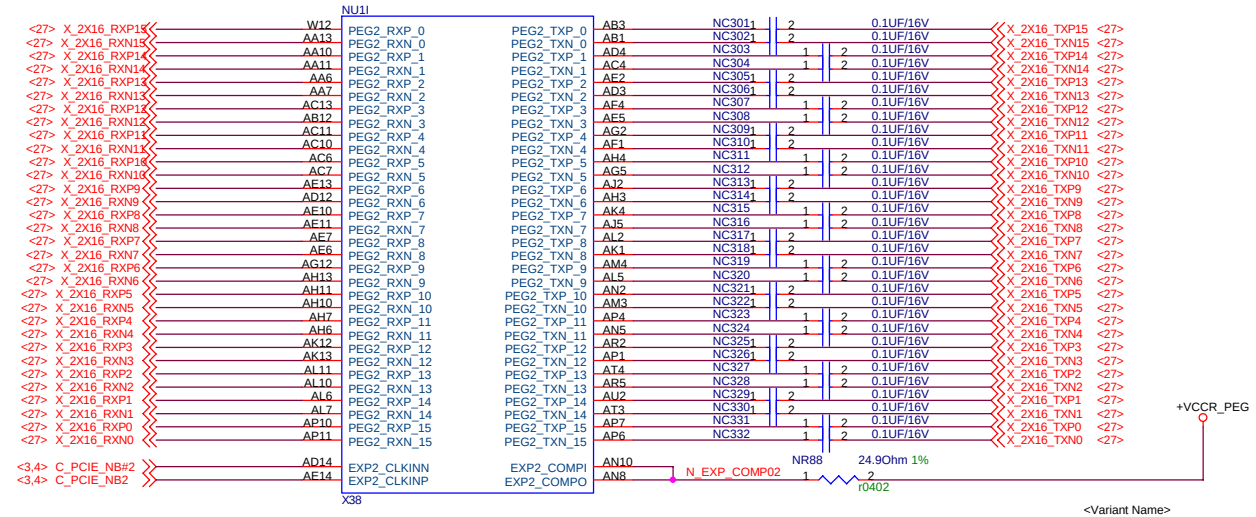
Engineer: Rex Chang

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 5 of 65



PCIEX16



<Variant Name>

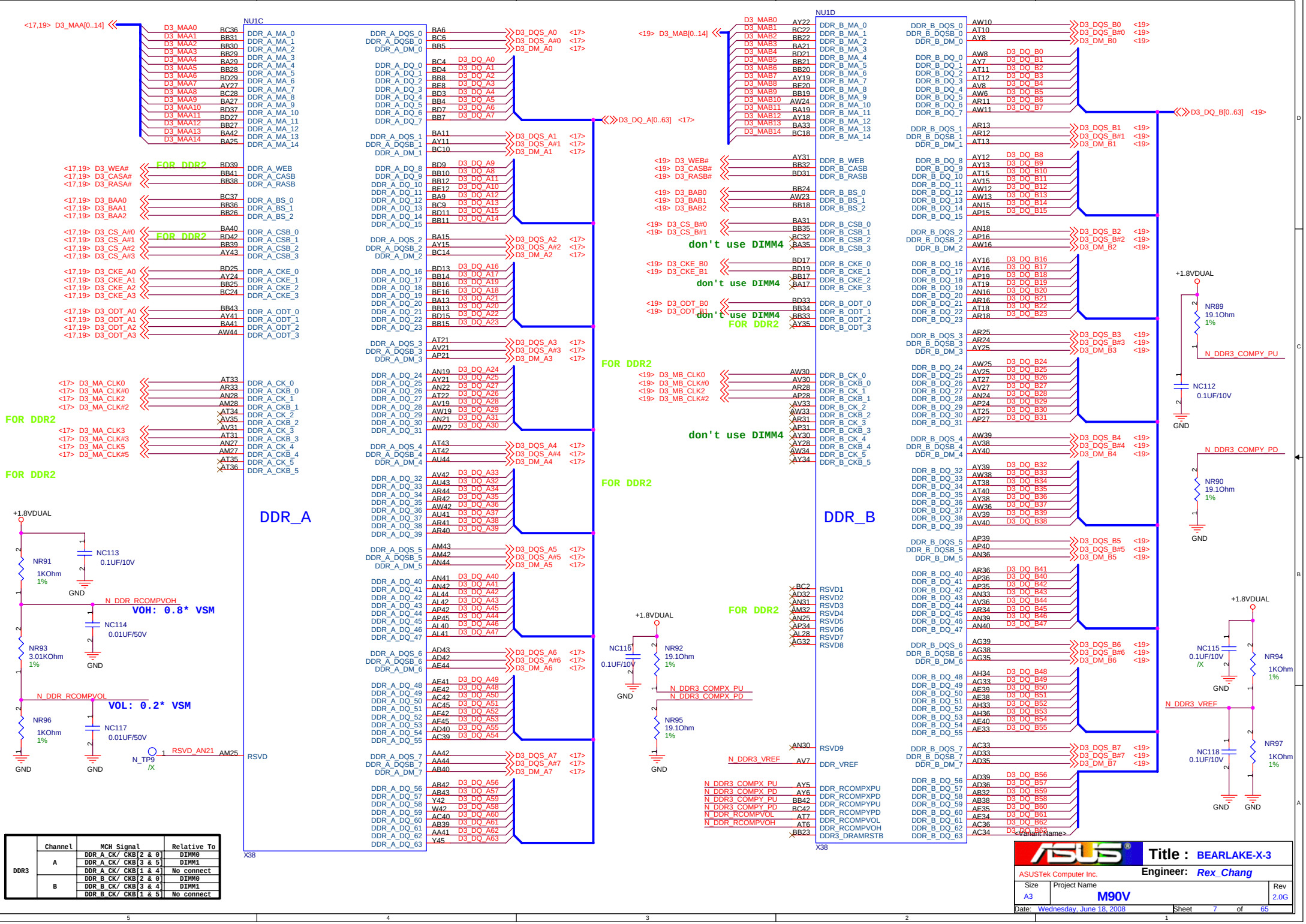
ASUSTek Computer Inc.

Title : BEARLAKE-X-2

Engineer: Rex Chang

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 6 of 65



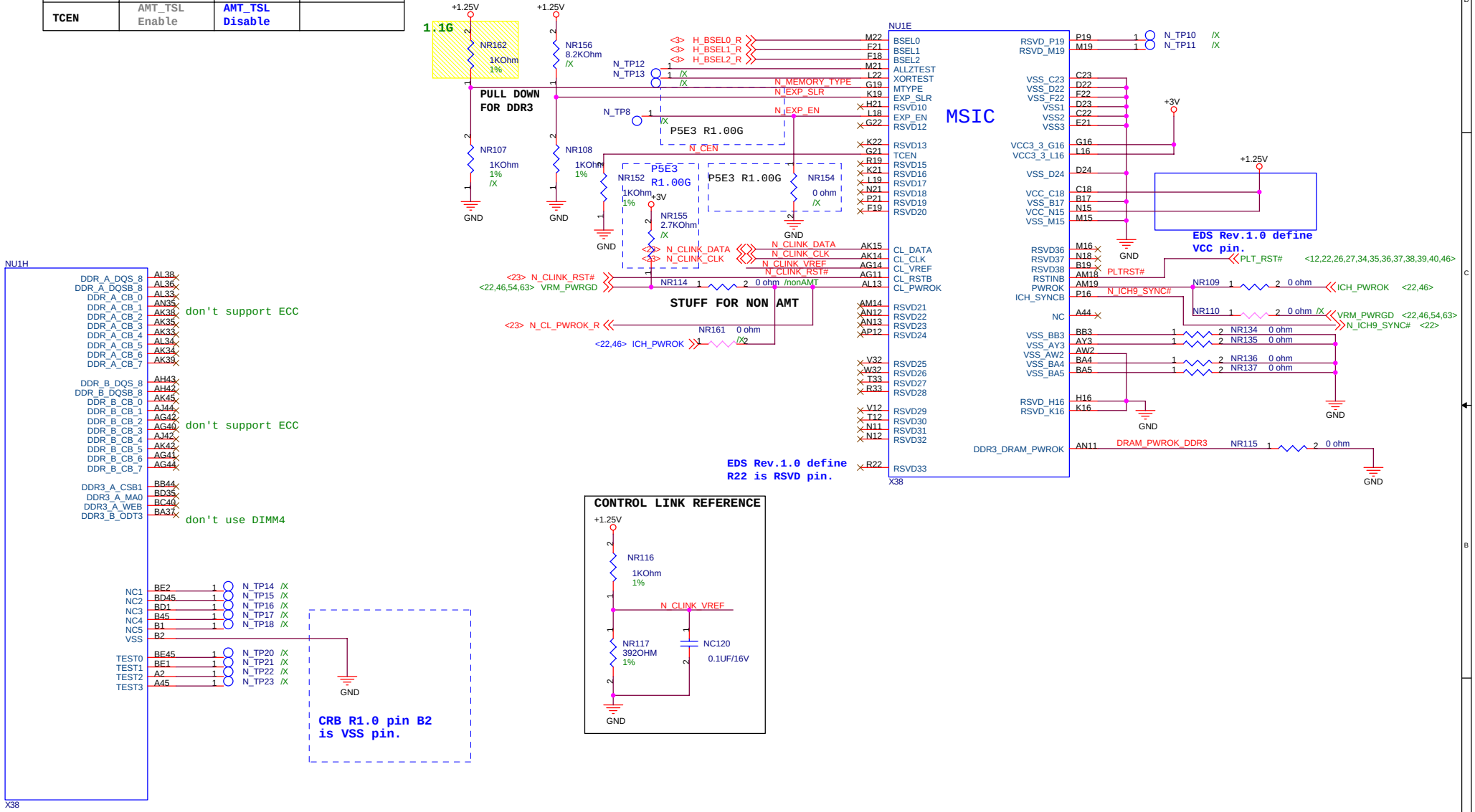
DDR3	Channel	MCH Signal	Relative To
	A	DDR_A_CK/ CKB[2 & 0]	DIMM0
		DDR_A_CK/ CKB[3 & 5]	DIMM1
		DDR_A_CK/ CKB[1 & 4]	No connect
	B	DDR_B_CK/ CKB[2 & 0]	DIMM0
		DDR_B_CK/ CKB[3 & 4]	DIMM1
		DDR_B_CK/ CKB[1 & 5]	No connect

ASUSTek Computer Inc.	Title : BEARLAKE-X-3	
	Engineer: Rex_Chang	
Size: A3	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 7 of 65	

Net Name	H	L	Description
MTYPE	DDR2	DDR3	Memory Type select
EXP_SLR	Norm (For ATX)	Reverse (For uBTX)	PCI-E LANE Reversal
EXP_EN	Concurrent	Non-Concurrent	PCI-E / SDVO Co-existence
TCEN	AMT_TSL Enable	AMT_TSL Disable	

MCH BSEL TABLE

BSEL2	BSEL1	BSEL0	FSB Frequency
0	0	0	267MHz (1067)
0	1	0	200MHz (800)
1	0	0	333MHz (1333)



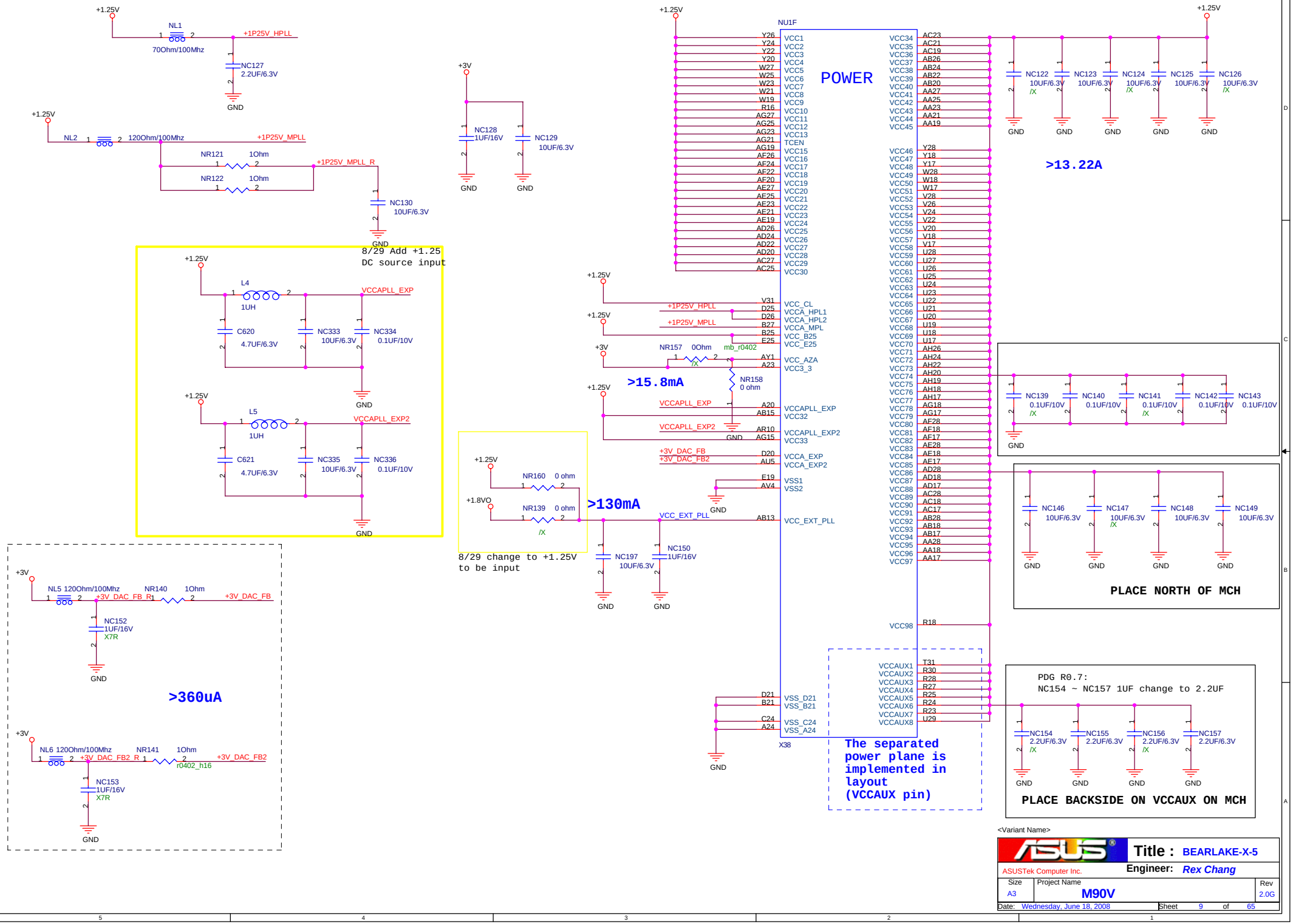
<Variant Name>

Title : BEARLAKE-X-4

ASUSTek Computer Inc. Engineer: Rex Chang

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 8 of 65


+1.25V
NL1
70Ohm/100Mhz
+1P25V_HPLL
NC127
2.2UF/6.3V
GND
NL2
120Ohm/100Mhz
+1P25V_MPLL
NR121
1Ohm
NR122
1Ohm
+1P25V_MPLL_R
NC130
10UF/6.3V
8/29 Add +1.25
DC source input
L4
1UH
VCCAPLL_EXP
C620
4.7UF/6.3V
NC333
10UF/6.3V
NC334
0.1UF/10V
L5
1UH
VCCAPLL_EXP2
C621
4.7UF/6.3V
NC335
10UF/6.3V
NC336
0.1UF/10V
+3V
NL5 120Ohm/100Mhz
+3V_DAC_FB_R
NR140
1Ohm
+3V_DAC_FB
NC152
1UF/16V
X7R
>360uA
NL6 120Ohm/100Mhz
+3V_DAC_FB2_R
NR141
1Ohm
+3V_DAC_FB2
r0402_h16
NC153
1UF/16V
X7R
NC128
1UF/16V
NC129
10UF/6.3V
+1.8VO
NR160
0 ohm
NR139
0 ohm
/X
>130mA
8/29 change to +1.25V
to be input
NC197
10UF/6.3V
NC150
1UF/16V
NU1F
POWER
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
TCEN
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC_CL
VCCA_HPL1
VCCA_HPL2
VCCA_MPL
VCC_B25
VCC_E25
VCC_AZA
VCC3_3
VCCAPLL_EXP
VCCAPLL_EXP2
VCC32
VCC33
VCCA_EXP
VCCA_EXP2
VSS1
VSS2
VCC_EXT_PLL
VSS_D21
VSS_B21
VSS_C24
VSS_A24
X38
VCC34
VCC35
VCC36
VCC37
VCC38
VCC39
VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCC49
VCC50
VCC51
VCC52
VCC53
VCC54
VCC55
VCC56
VCC57
VCC58
VCC59
VCC60
VCC61
VCC62
VCC63
VCC64
VCC65
VCC66
VCC67
VCC68
VCC69
VCC70
VCC71
VCC72
VCC73
VCC74
VCC75
VCC76
VCC77
VCC78
VCC79
VCC80
VCC81
VCC82
VCC83
VCC84
VCC85
VCC86
VCC87
VCC88
VCC89
VCC90
VCC91
VCC92
VCC93
VCC94
VCC95
VCC96
VCC97
VCC98
R18
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
The separated
power plane is
implemented in
layout
(VCCAUX pin)
NR157
0Ohm
mb_r0402
/X
NR158
0 ohm
>15.8mA
NC122
10UF/6.3V
NC123
10UF/6.3V
NC124
10UF/6.3V
NC125
10UF/6.3V
NC126
10UF/6.3V
>13.22A
NC139
0.1UF/10V
NC140
0.1UF/10V
NC141
0.1UF/10V
NC142
0.1UF/10V
NC143
0.1UF/10V
PLACE NORTH OF MCH
NC146
10UF/6.3V
NC147
10UF/6.3V
NC148
10UF/6.3V
NC149
10UF/6.3V
PLACE NORTH OF MCH
PDG R0.7:
NC154 ~ NC157 1UF change to 2.2UF
NC154
2.2UF/6.3V
NC155
2.2UF/6.3V
NC156
2.2UF/6.3V
NC157
2.2UF/6.3V
PLACE BACKSIDE ON VCCAUX ON MCH
<Variant Name>
Title : BEARLAKE-X-5
ASUSTek Computer Inc.
Engineer: Rex Chang
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 9 of 65

MOW WW50_2006:
Intel's platform power-delivery simulation analysis has resulted in the removal of back-side decoupling caps for VCC_Core.

PLACE BACKSIDE

CLOSE TO NR17 ON SIGNAL N_DDR3_COMPY_PU

Layout used big shapes cover NJP1 pin1 and pin2

Layout used big shapes cover NJP2 pin1 and pin2

PWR CL

>0.98A

>3.93A

>6.25A

>2.63A

>1.73A

>350mA

CRB R1.0 pin W31 is VSS pin.

9/4 reserve

70Ohm/100Mhz
Irat > 350mA

<Variant Name>

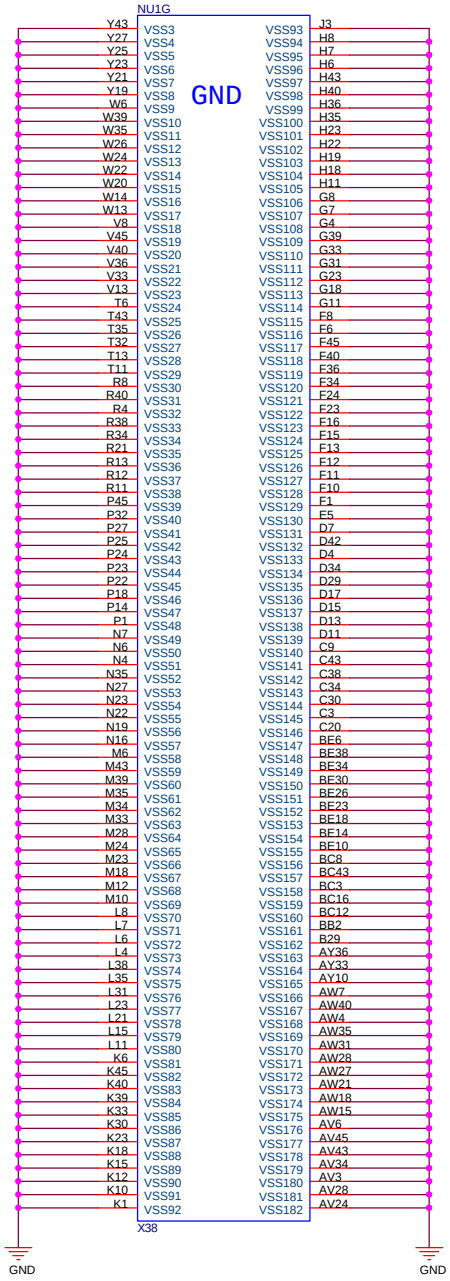
Title : BEARLAKE-X-6

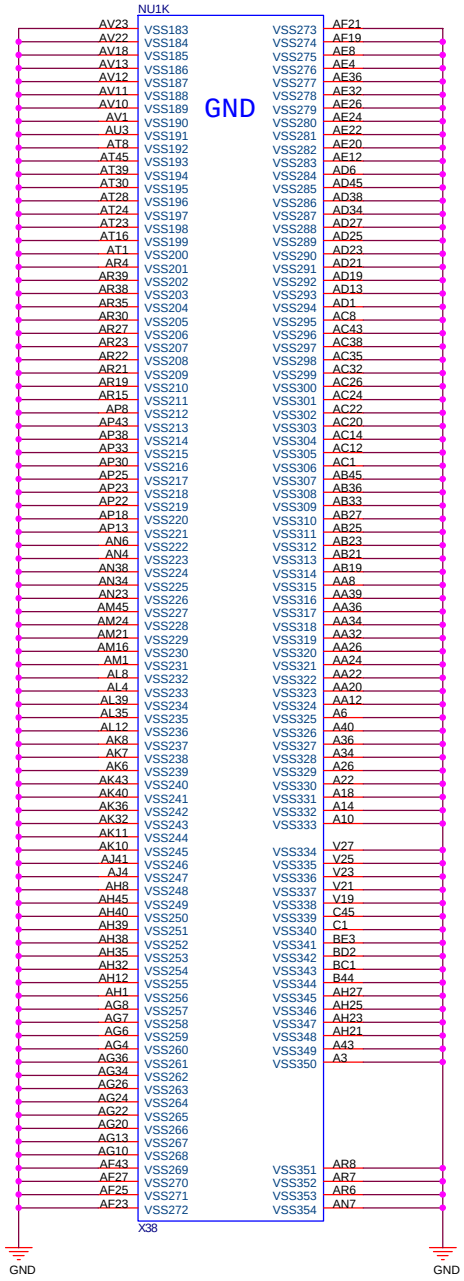
ASUSTek Computer Inc.

Engineer: Rex Chang

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 10 of 65





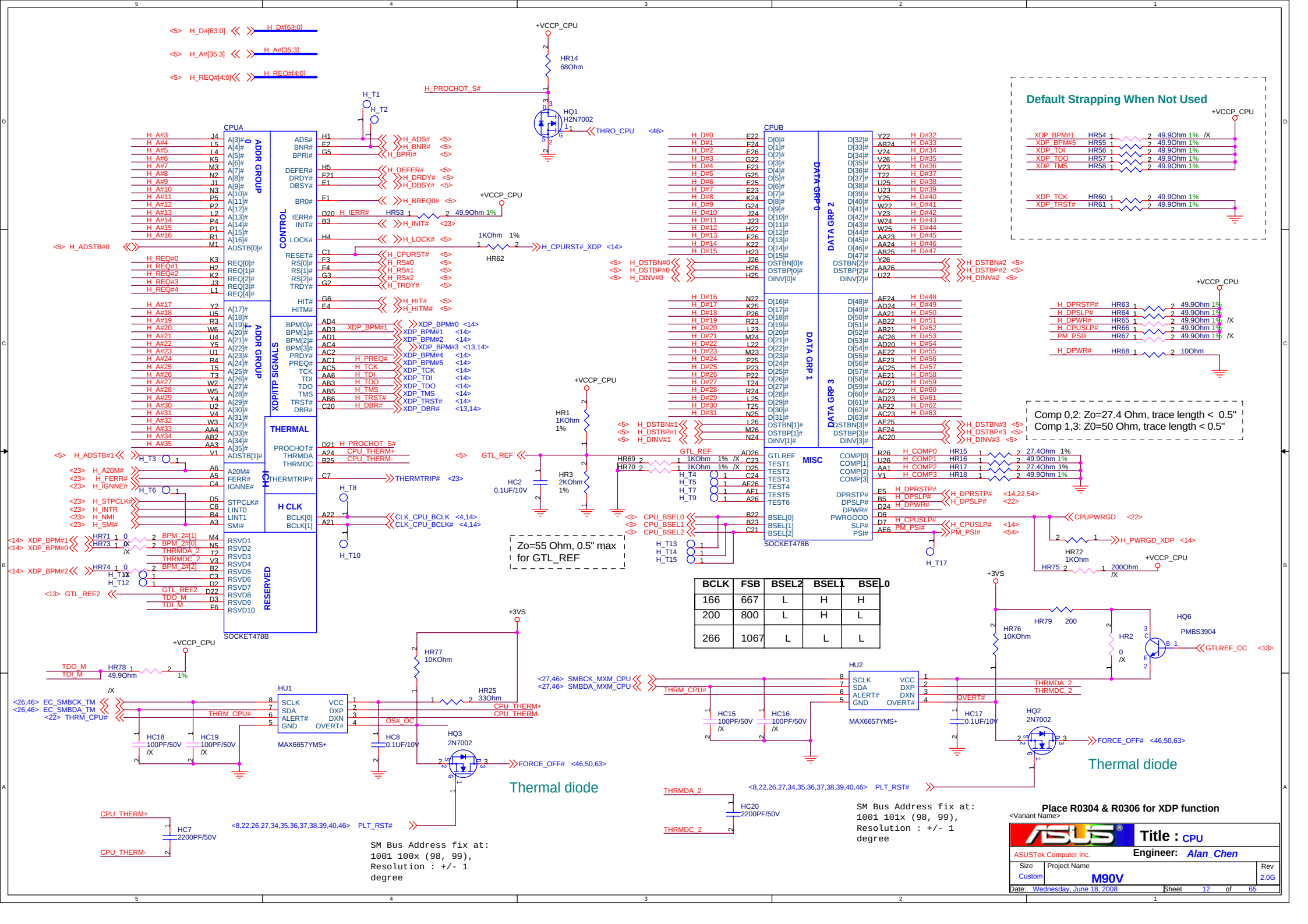
<Variant Name>

Title : BEARLAKE-X-7

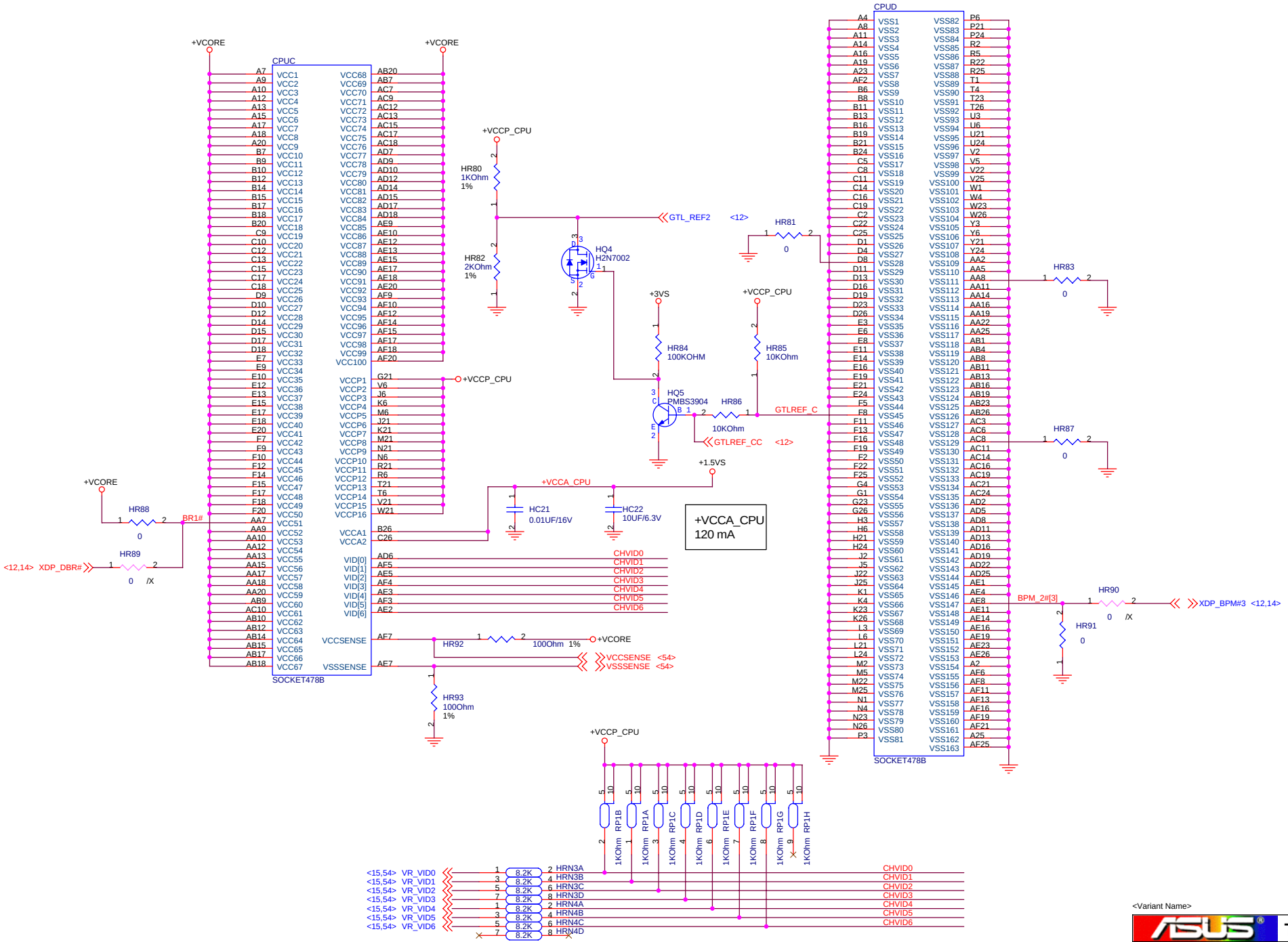
ASUSTek Computer Inc. Engineer: Rex Chang

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 11 of 65



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L



<Variant Name>

ASUSTek Computer Inc.

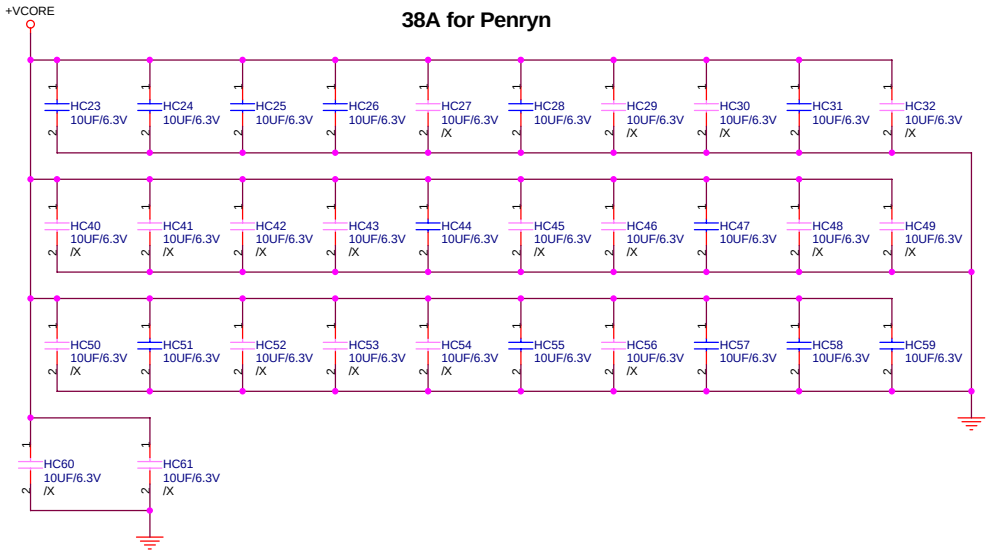
Title : CPU

Engineer: Alan_Chen

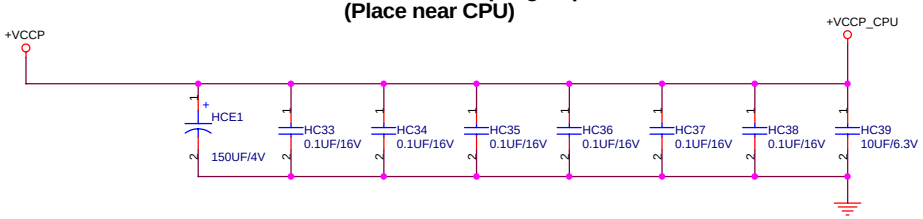
Size	Project Name	Rev
Custom	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 13 of 65

38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from Intel

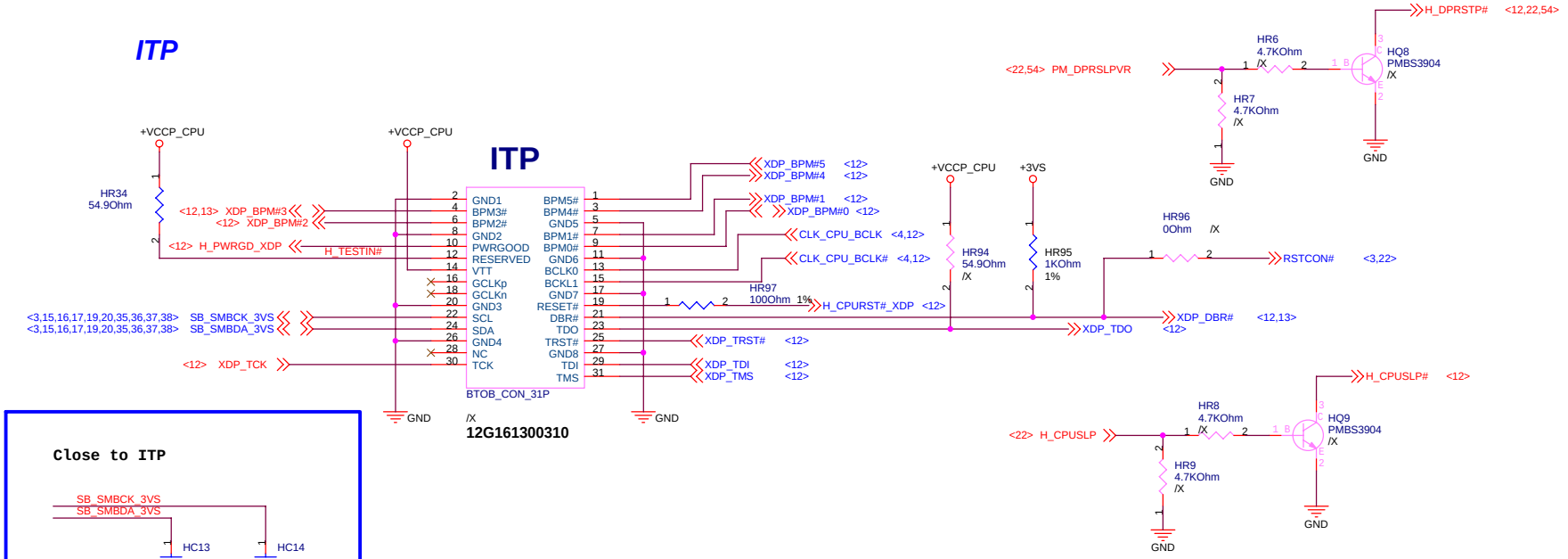
VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs

?

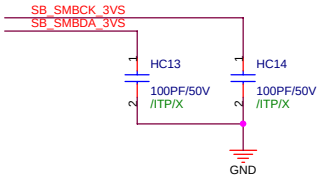
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?

+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?

ITP

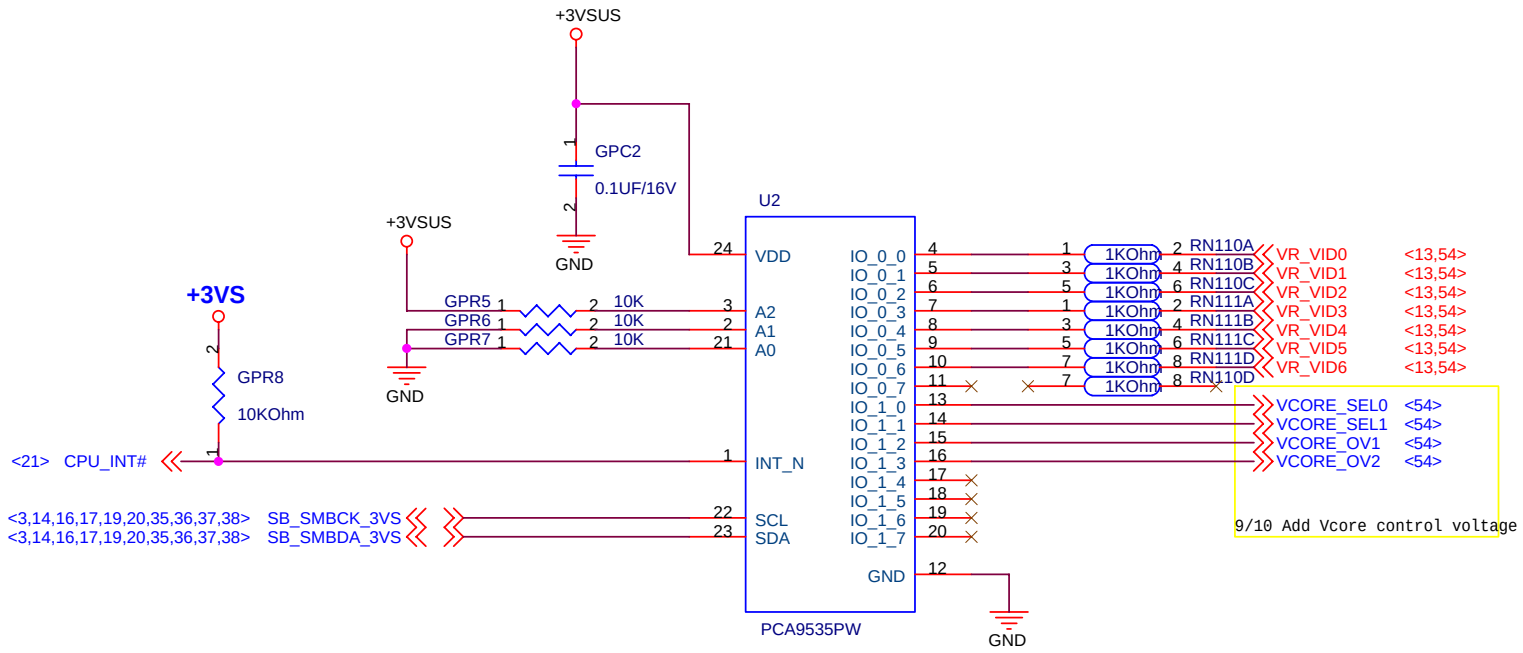


Close to ITP



<Variant Name>

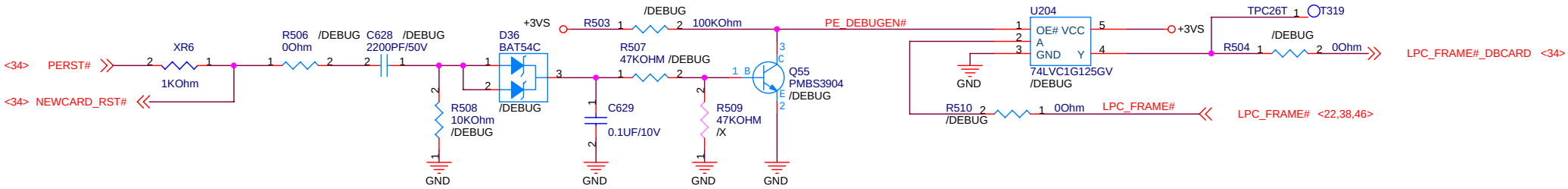
ASUSTek Computer Inc.	Title : CPU	
	Engineer: Alan_Chen	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 14 of 65	



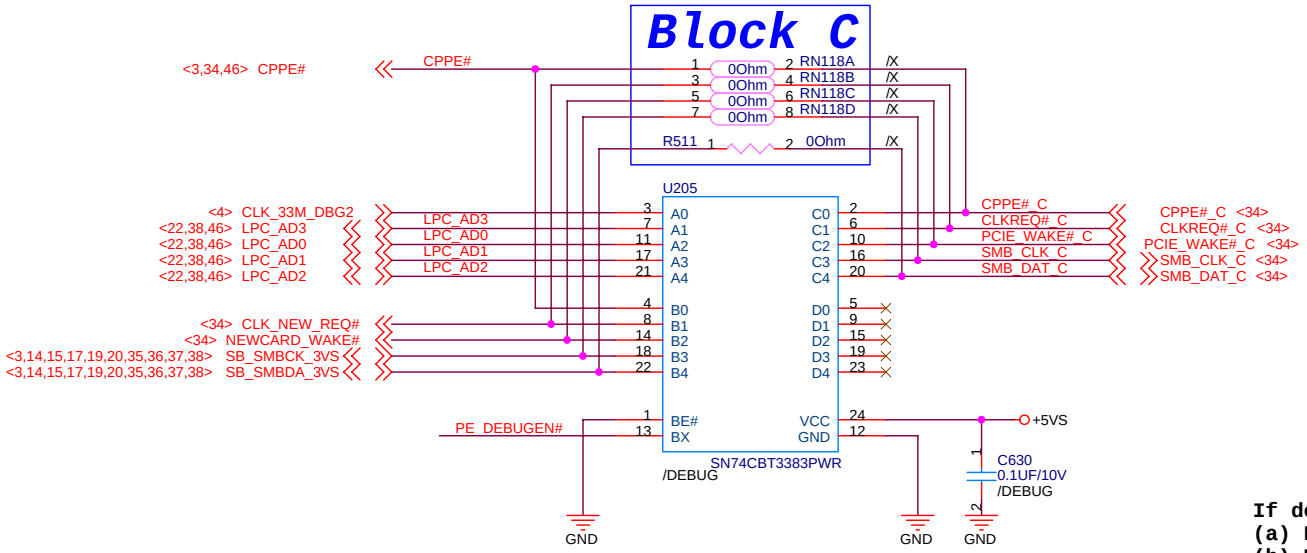
<Variant Name>

ASUSTek Computer Inc.	Title : VID	
	Engineer: Rex Chang	
Size: A4	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 15 of 65	

Block A



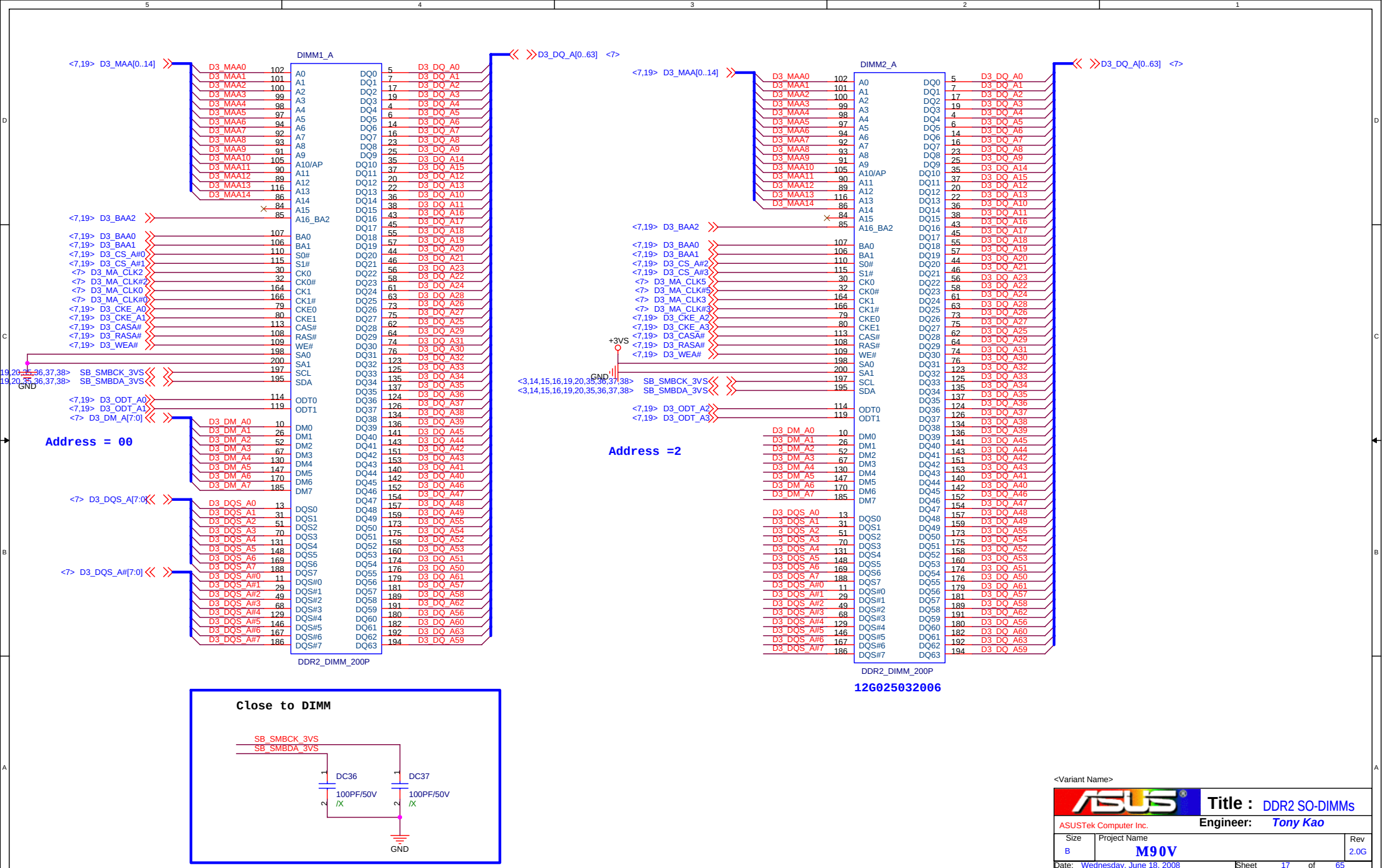
Block C

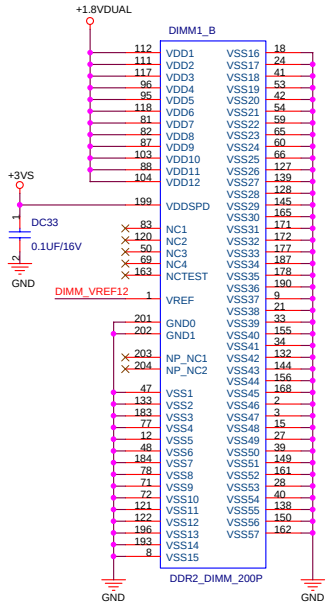


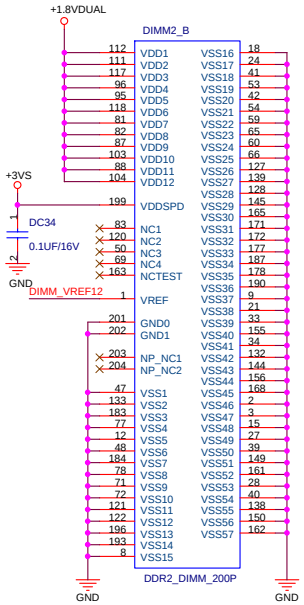
If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

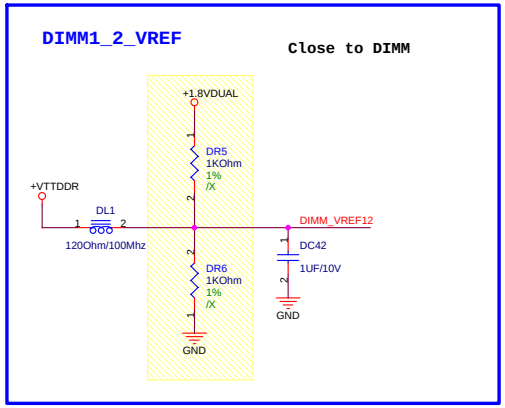
<Variant Name>

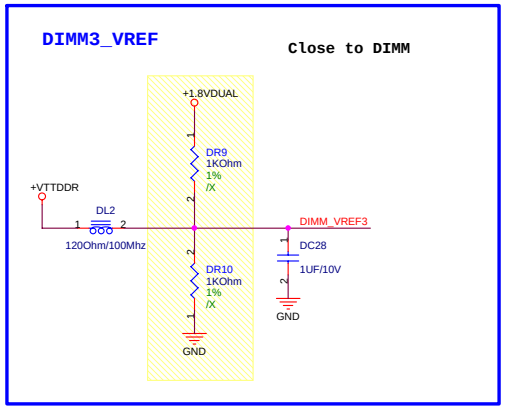
ASUSTek Computer Inc.	Title : DEBUG CARD	
	Engineer: Alan_chen	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 16 of 65	

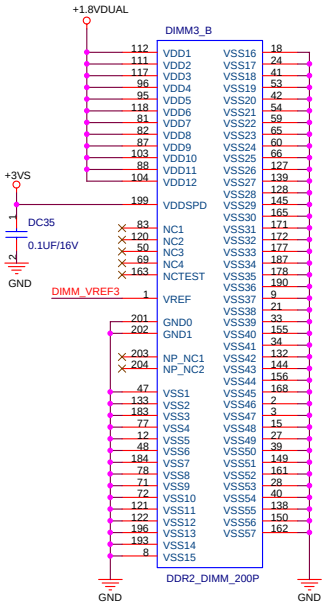

DIMM1_A
DIMM2_A
DDR2_DIMM_200P
Address = 00
Address =2
12G025032006
Close to DIMM
SB_SMBCK_3VS
SB_SMBDA_3VS
DC36
DC37
100PF/50V
/X
GND
+3VS
<Variant Name>
Title : DDR2 SO-DIMMs
ASUSTek Computer Inc.
Engineer: Tony Kao
Size B
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 17 of 65

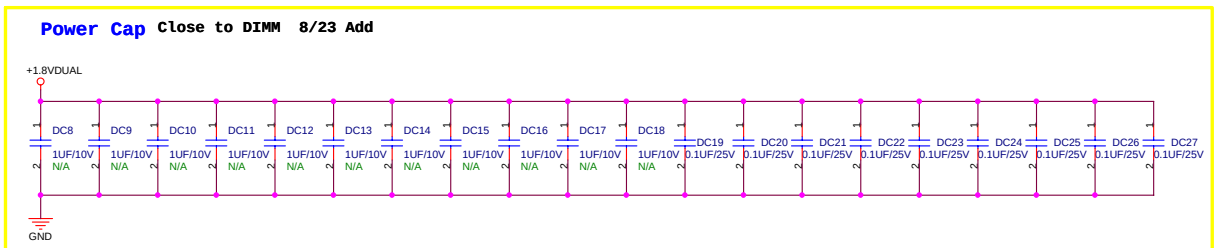


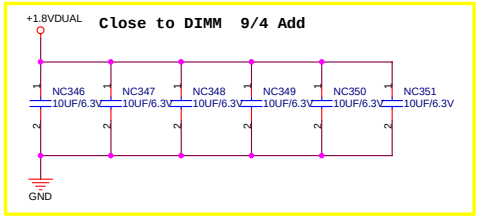


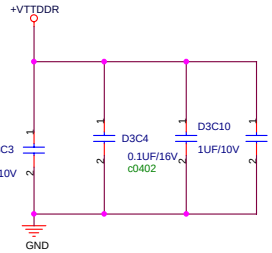






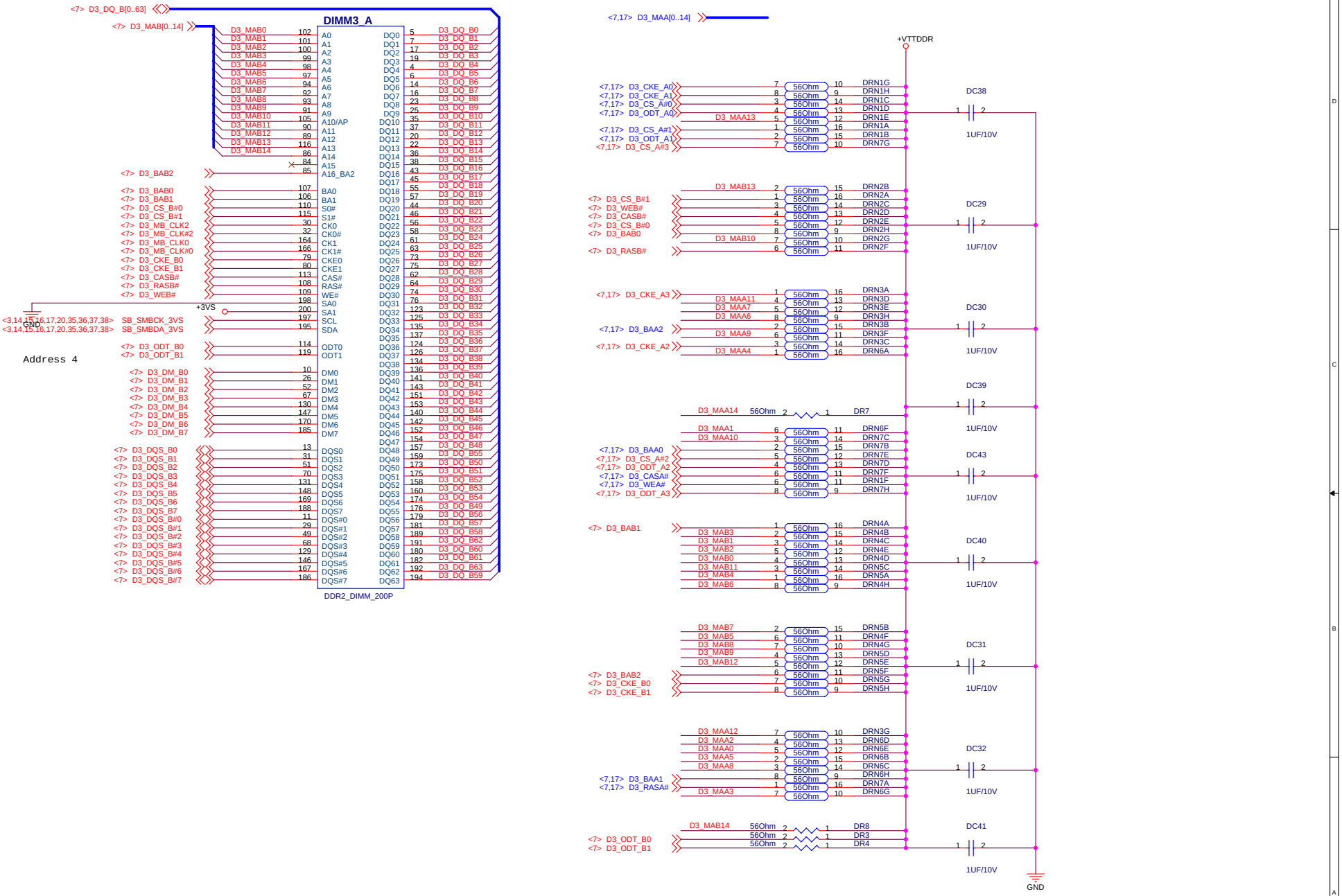






<variant_name>

ASUSTek Computer Inc.	Title : DDR2 TERMINATION	
	Engineer: Tony Kao	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 18 of 65	



<Variant Name>

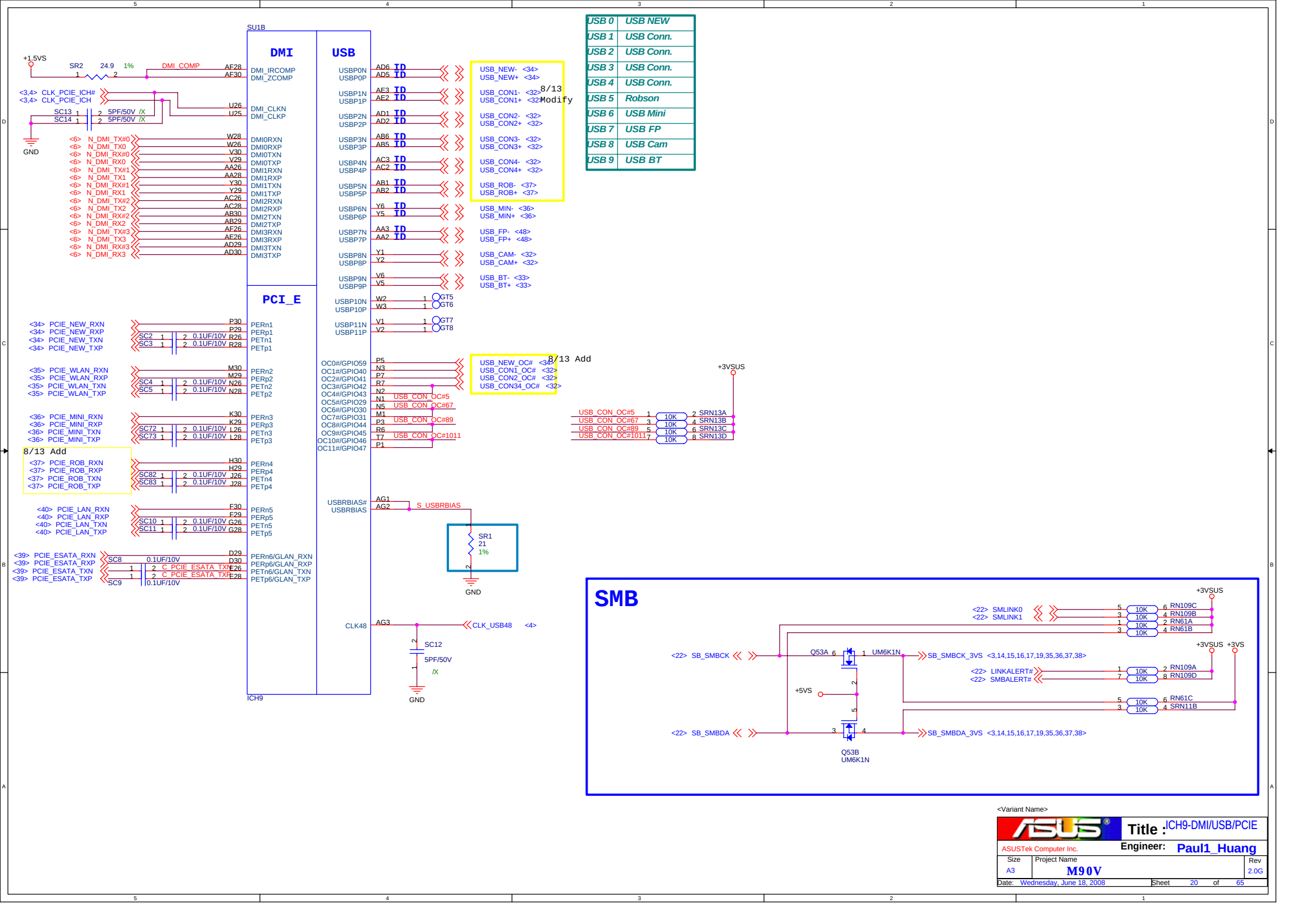
ASUSTek Computer Inc.

Title : DDR2 SO-DIMMs

Engineer: Tony Kao

Size	Project Name	Rev
Custom	M90V	2.0G

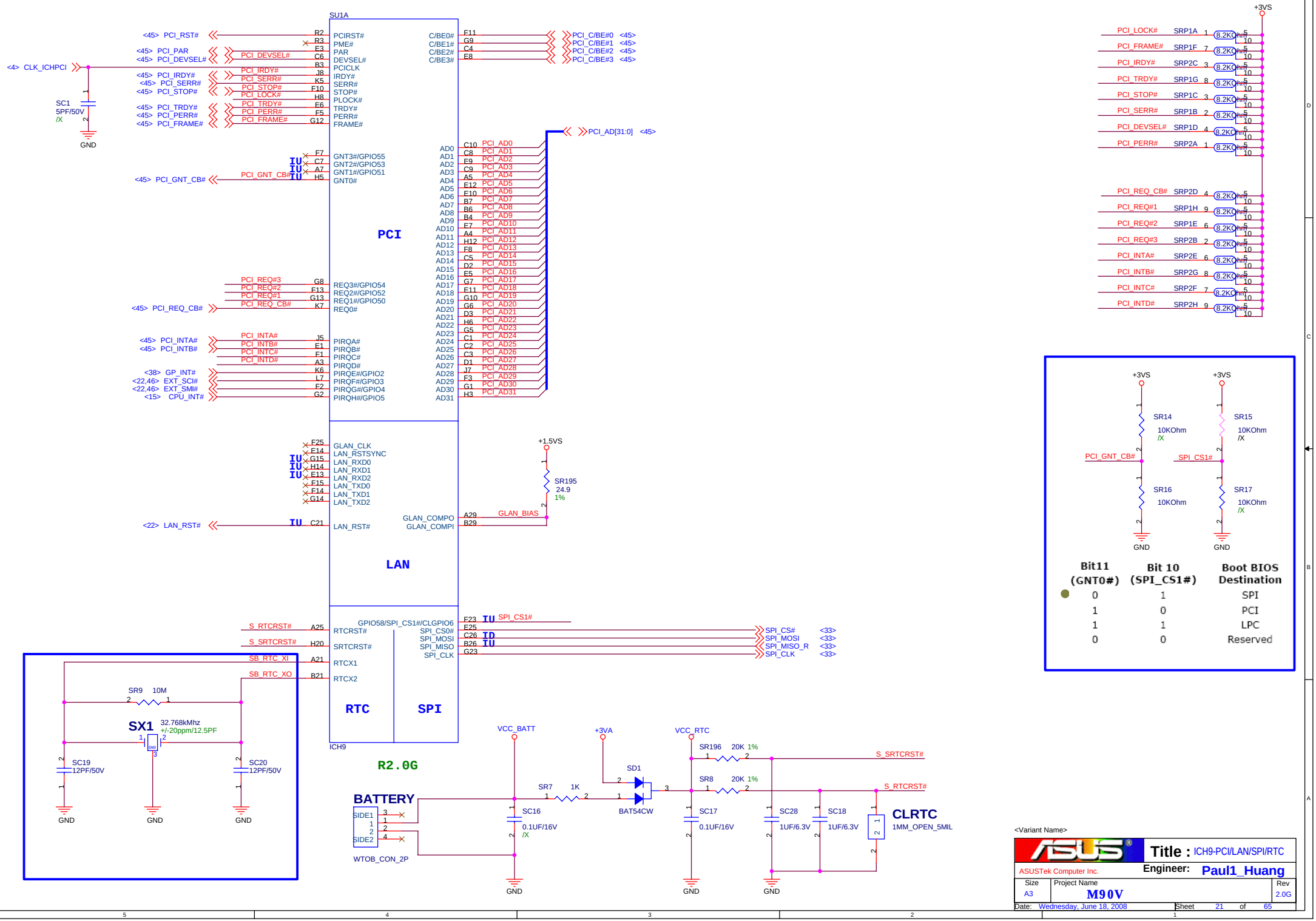
Date: Wednesday, June 18, 2008 Sheet 19 of 65

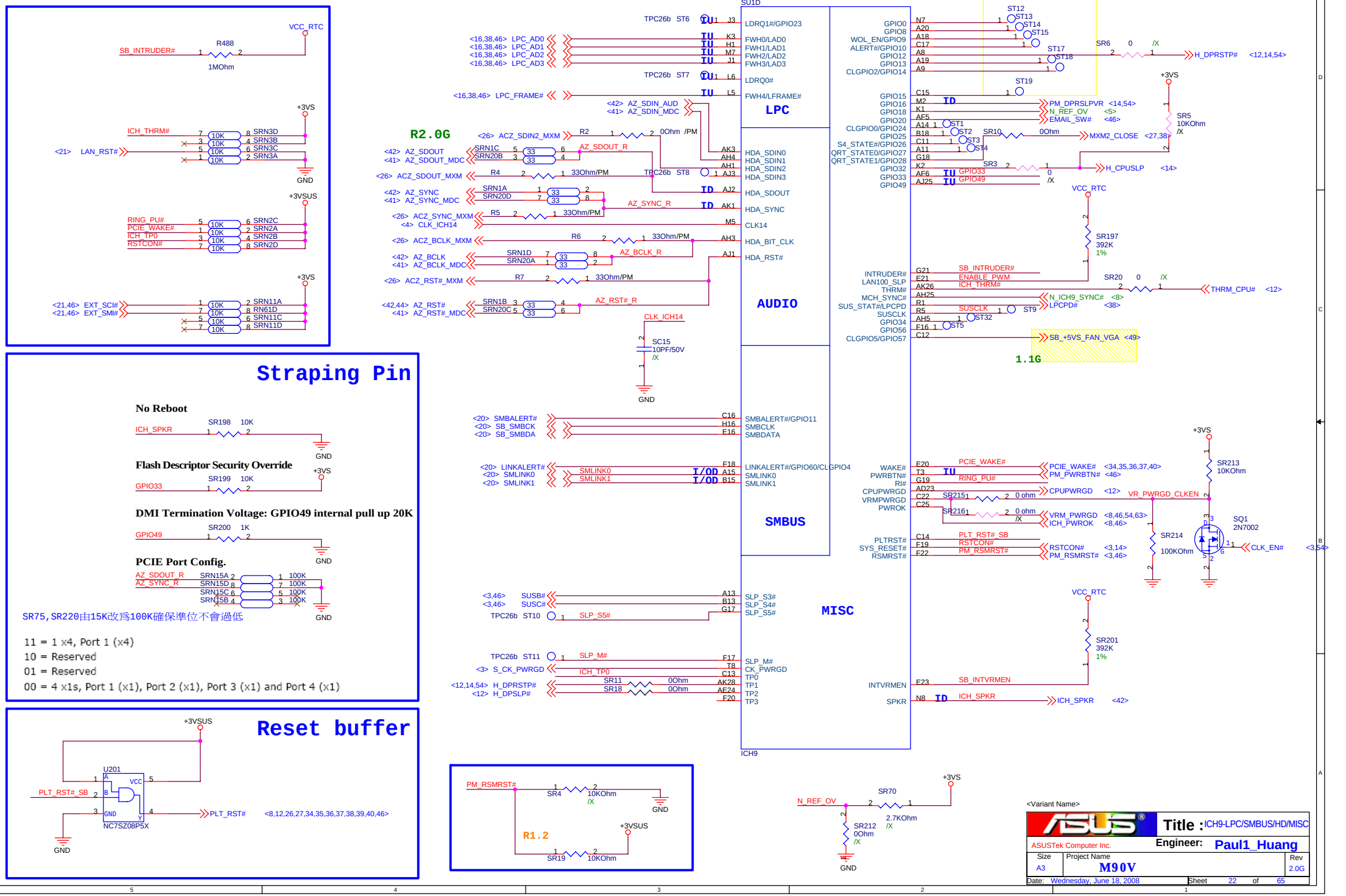


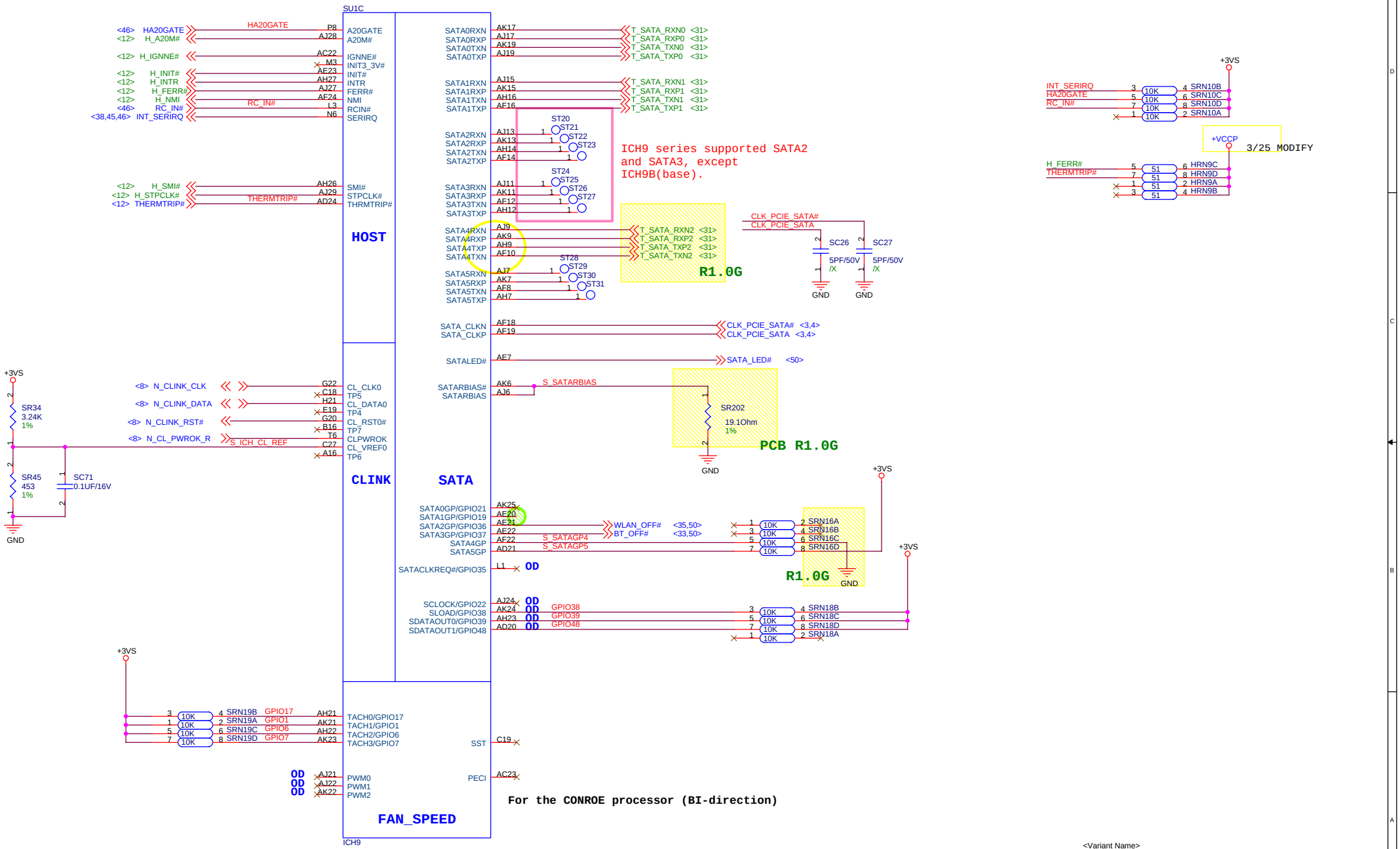
USB 0	USB NEW
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB Conn.
USB 5	Robson
USB 6	USB Mini
USB 7	USB FP
USB 8	USB Cam
USB 9	USB BT

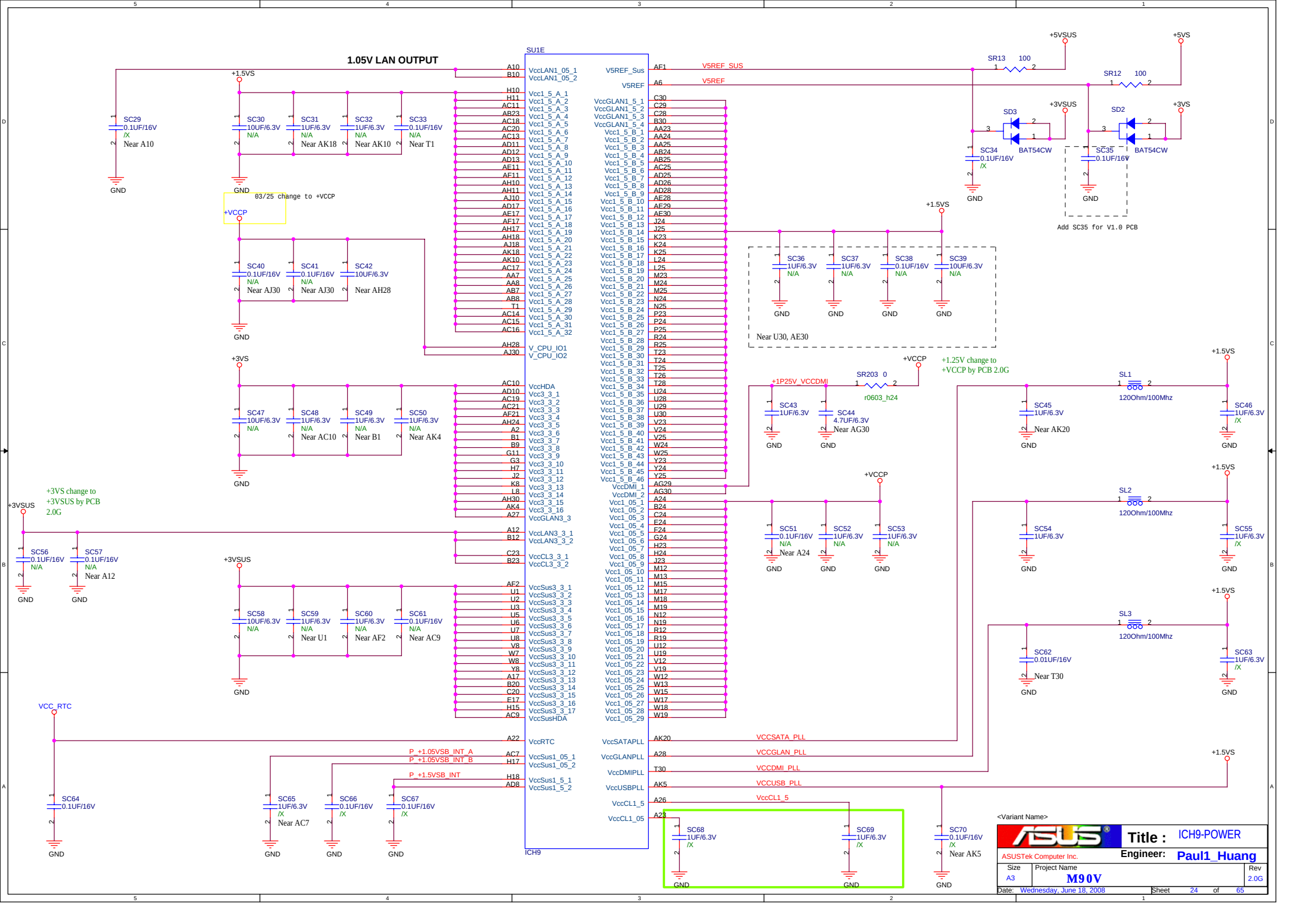
<Variant Name>

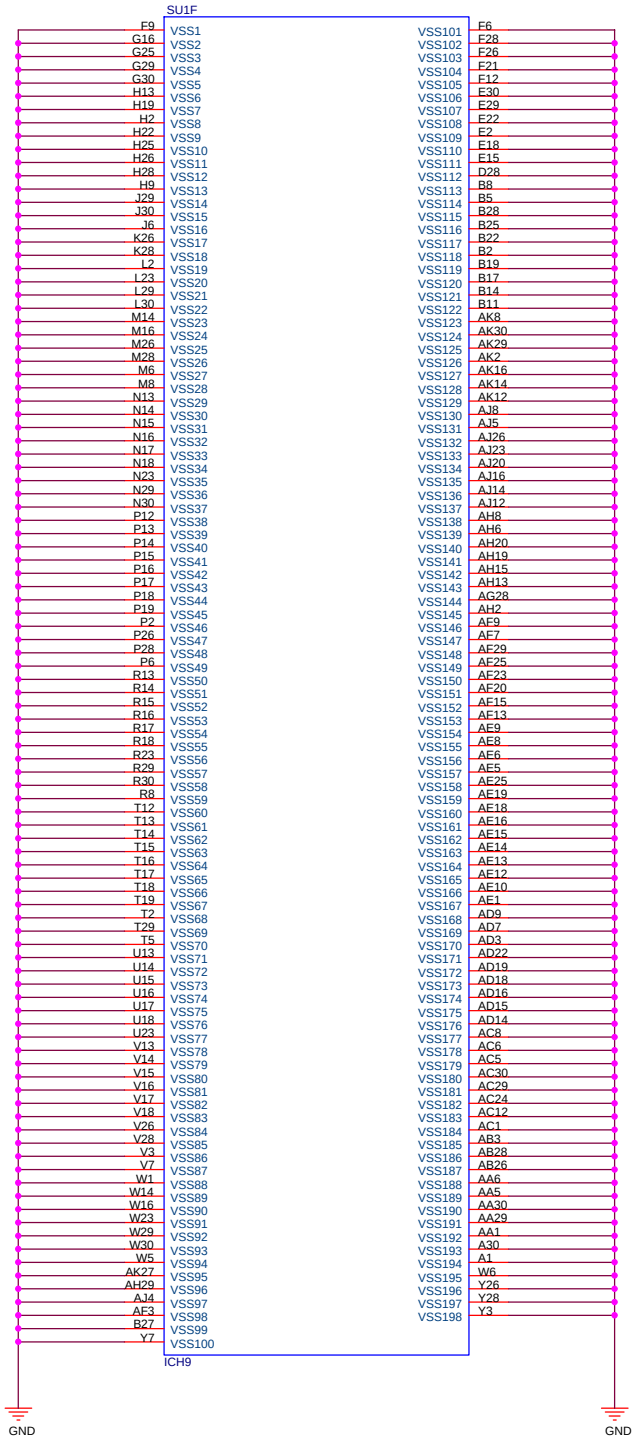
ASUSTek Computer Inc.	Title : ICH9-DMI/USB/PCIE	
	Engineer: Paul1_Huang	
Size: A3	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 20 of 65	


SU1A
PCI
LAN
RTC
SPI
ICH9
R2.0G
BATTERY
CLRTC
SX1 32.768kMhz +/-20ppm/12.5PF
Bit11 (GNT0#) Bit 10 (SPI_CS1#) Boot BIOS Destination
0 1 SPI
1 0 PCI
1 1 LPC
0 0 Reserved
Title : ICH9-PCI/LAN/SPI/RTC
ASUSTek Computer Inc.
Engineer: Paul1_Huang
M90V
Date: Wednesday, June 18, 2008
Sheet 21 of 65


Straping Pin
No Reboot
ICH_SPKR
SR198 10K
GND
Flash Descriptor Security Override
GPIO33
SR199 10K
+3VS
DMI Termination Voltage: GPIO49 internal pull up 20K
GPIO49
SR200 1K
PCIE Port Config.
AZ_SDOUT_R
AZ_SYNC_R
SRN15A
SRN15D
SRN15C
SRN15B
100K
SR75,SR220由15K改爲100K確保準位不會過低
11 = 1 x4, Port 1 (x4)
10 = Reserved
01 = Reserved
00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1) and Port 4 (x1)
Reset buffer
+3VSUS
U201
NC7SZ08P5X
PLT_RST#_SB
PLT_RST#
<8,12,26,27,34,35,36,37,38,39,40,46>
R488
1MOhm
SB_INTRUDER#
VCC_RTC
ICH_THRM#
LAN_RST#
SRN3D
SRN3B
SRN3C
SRN3A
RING_PU#
PCIE_WAKE#
ICH_TP0
RSTCON#
SRN2C
SRN2A
SRN2B
SRN2D
EXT_SCI#
EXT_SMI#
SRN11A
RN61D
SRN11C
SRN11D
SU1D
ICH9
LPC
AUDIO
SMBUS
MISC
LDRQ1#/GPIO23
LDRQ0#
FWH4/LFRAME#
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_SYNC
CLK14
HDA_BIT_CLK
HDA_RST#
SMBALERT#/GPIO11
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
SLP_S3#
SLP_S4#
SLP_S5#
SLP_M#
CK_PWRGD
TP0
TP1
TP2
TP3
R2.0G
R1.2
1.1G
9/4 reserve GPIO pin
GPIO0
GPIO8
WOL_EN/GPIO9
ALERT#/GPIO10
GPIO12
GPIO13
CLGPIO2/GPIO14
GPIO15
GPIO16
GPIO18
GPIO20
CLGPIO0/GPIO24
GPIO25
S4_STATE#/GPIO26
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
GPIO32
GPIO33
GPIO49
H_DPRSTP#
PM_DPRSLPVR
N_REF_OV
EMAIL_SW#
MXM2_CLOSE
H_CPUSLP
SR5
10KOhm
SR10
0Ohm
SR3
SR197
392K
1%
INTRUDER#
LAN100_SLP
THRM#
MCH_SYNC#
SUS_STAT#/LPCPD
SUSCLK
GPIO34
GPIO56
CLGPIO5/GPIO57
SB_INTRUDER#
ENABLE_PWM
ICH_THRM#
N_ICH9_SYNC#
LPCPD#
SUSCLK
SB_+5VS_FAN_VGA
THRM_CPU#
SR20
SR213
10KOhm
SR214
100KOhm
SQ1
2N7002
CLK_EN#
WAKE#
PWRBTN#
RI#
CPUPWRGD
VRMPWRGD
PWROK
PCIE_WAKE#
RING_PU#
PM_PWRBTN#
CPUPWRGD
VR_PWRGD_CLKEN
VRM_PWRGD
ICH_PWROK
PLTRST#
SYS_RESET#
RSMRST#
PLT_RST#_SB
RSTCON#
PM_RSMRST#
SR201
392K
1%
INTVRMEN
SB_INTVRMEN
SPKR
ICH_SPKR
SR70
2.7KOhm
SR212
0Ohm
PM_RSMRST#
SR4
10KOhm
SR19
10KOhm
CLK_ICH14
SC15
10PF/50V
AZ_SDOUT_R
AZ_SYNC_R
AZ_BCLK_R
AZ_RST#_R
R2
R4
R5
R6
R7
0Ohm /PM
33Ohm/PM
SRN1A
SRN20D
SRN1C
SRN20B
SRN1D
SRN20A
SRN1B
SRN20C
33
SUSB#
SUSC#
SLP_S5#
SLP_M#
ICH_TP0
S_CK_PWRGD
H_DPSLP#
TPC26b ST6
TPC26b ST7
TPC26b ST8
TPC26b ST10
TPC26b ST11
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
AZ_SDIN_AUD
AZ_SDIN_MDC
ACZ_SDIN2_MXM
AZ_SDOUT
AZ_SDOUT_MDC
ACZ_SDOUT_MXM
AZ_SYNC
AZ_SYNC_MDC
ACZ_SYNC_MXM
CLK_ICH14
ACZ_BCLK_MXM
AZ_BCLK
AZ_BCLK_MDC
ACZ_RST#_MXM
AZ_RST#
AZ_RST#_MDC
SMBALERT#
SB_SMBCK
SB_SMBDA
LINKALERT#
SMLINK0
SMLINK1
SUSB#
SUSC#
SLP_S5#
SLP_M#
ICH_TP0
H_DPRSTP#
H_DPSLP#
SR11
SR18
0Ohm
+3VS
+3VSUS
GND
<Variant Name>
Title : ICH9-LPC/SMBUS/HD/MISC
ASUSTek Computer Inc.
Engineer: Paul1_Huang
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 22 of 65


SU1C
HOST
CLINK
SATA
FAN_SPEED
ICH9
ICH9 series supported SATA2 and SATA3, except ICH9B(base).
R1.0G
PCB R1.0G
R1.0G
3/25 MODIFY
For the CONROE processor (BI-direction)
<Variant Name>
Title : ICH9-CLINK/SATA/FAN/CPU
ASUSTek Computer Inc.
Engineer: Paul1_Huang
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 23 of 65


1.05V LAN OUTPUT
SU1E
ICH9
+1.5VS
+VCCP
+3VS
+3VSUS
+5VSUS
+5VS
GND
03/25 change to +VCCP
+3VS change to +3VSUS by PCB 2.0G
+1.25V change to +VCCP by PCB 2.0G
Near U30, AE30
Add SC35 for V1.0 PCB
VCC_RTC
V5REF_SUS
V5REF
+1P25V_VCCDMI
VCCSATA_PLL
VCCGLAN_PLL
VCCDMI_PLL
VCCUSB_PLL
VccCL1_5
P_+1.05VSB_INT_A
P_+1.05VSB_INT_B
P_+1.5VSB_INT
<Variant Name>
Title : ICH9-POWER
ASUSTek Computer Inc.
Engineer: Paul1_Huang
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 24 of 65



<Variant Name>

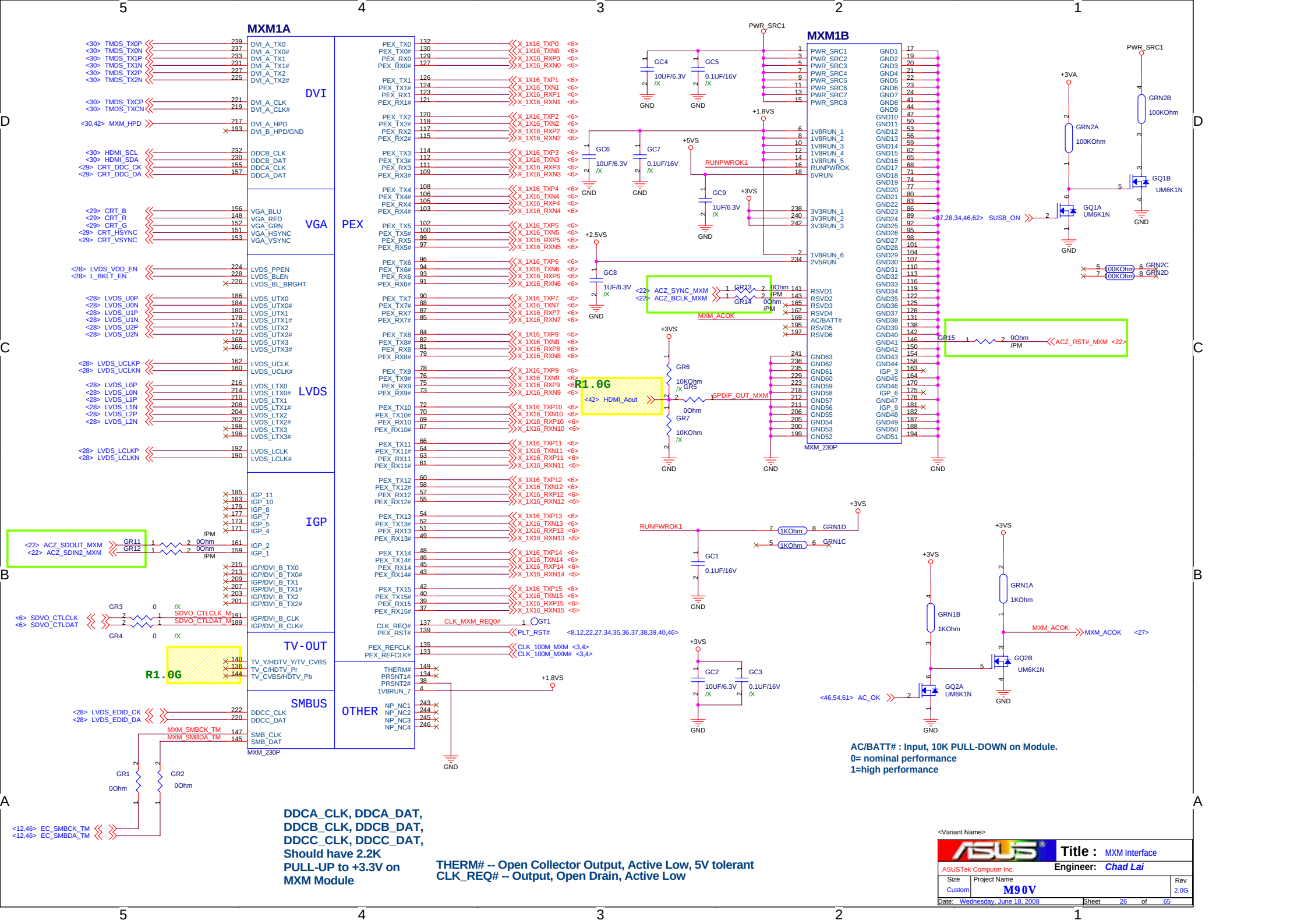
Title : ICH9-GND

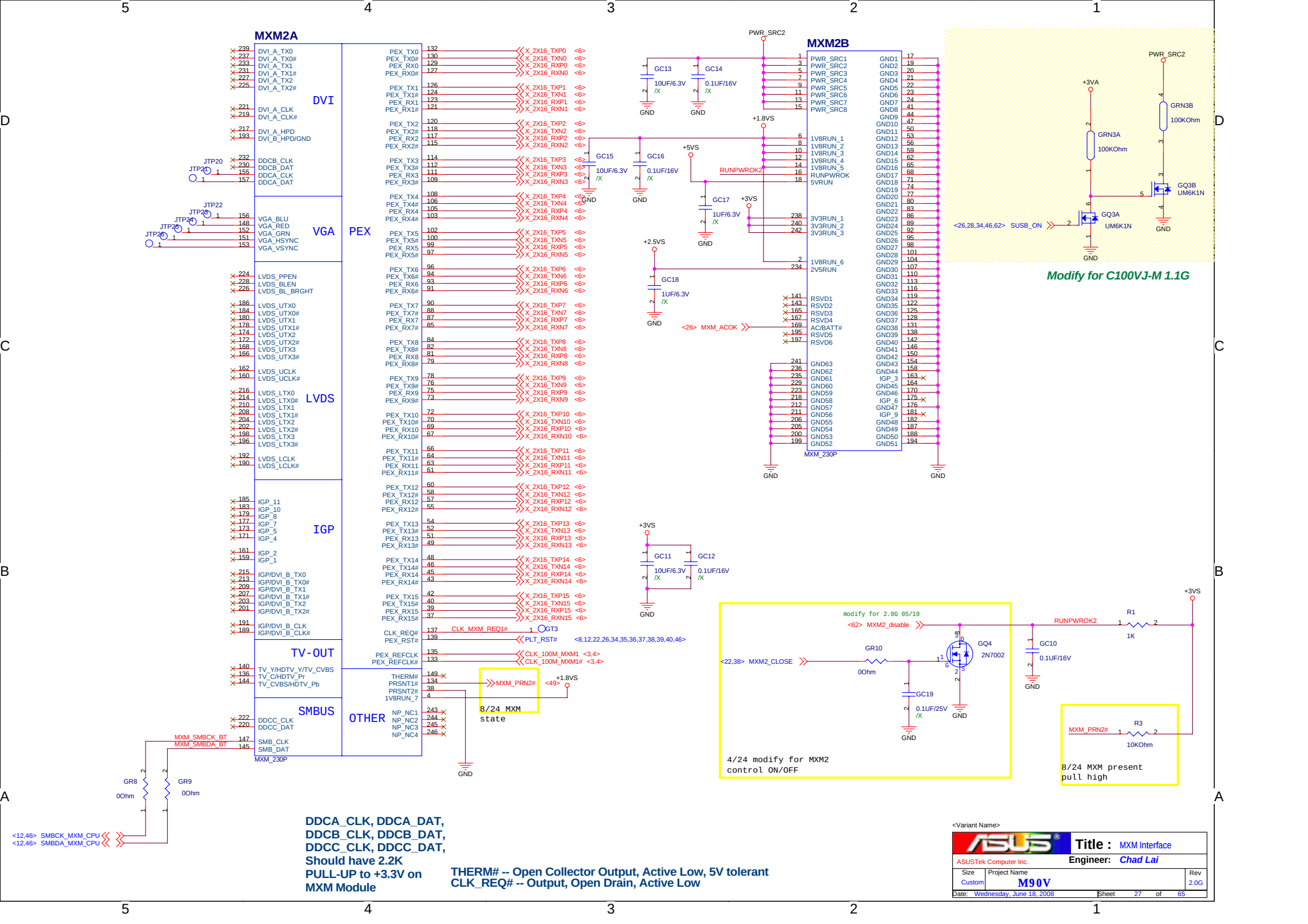
ASUSTek Computer Inc.

Engineer: Paul1_Huang

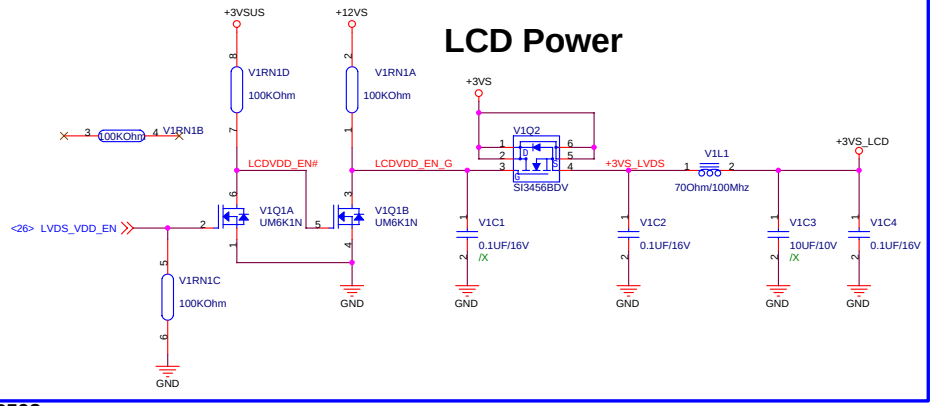
Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 25 of 65


MXM1A
DVI
VGA
LVDS
IGP
TV-OUT
SMBUS
PEX
OTHER
MXM_230P
MXM1B
MXM_230P
R1.0G
R1.0G
DDCA_CLK, DDCA_DAT,
DDCB_CLK, DDCB_DAT,
DDCC_CLK, DDCC_DAT,
Should have 2.2K
PULL-UP to +3.3V on
MXM Module
THERM# -- Open Collector Output, Active Low, 5V tolerant
CLK_REQ# -- Output, Open Drain, Active Low
AC/BATT# : Input, 10K PULL-DOWN on Module.
0= nominal performance
1=high performance
<Variant Name>
Title : MXM Interface
ASUSTek Computer Inc.
Engineer: Chad Lai
Size Custom
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 26 of 65


MXM2A
DVI
VGA
PEX
LVDS
IGP
TV-OUT
SMBUS
OTHER
MXM_230P
MXM2B
MXM_230P
PWR_SRC2
+1.8VS
+5VS
+3VS
+2.5VS
GND
RUNPWROK2
MXM_ACOK
SUSB_ON
MXM_PRN2#
CLK_MXM_REQ1#
PLT_RST#
CLK_100M_MXM1
CLK_100M_MXM1#
MXM_SMBCK_BT
MXM_SMBDA_BT
<12,46> SMBCK_MXM_CPU
<12,46> SMBDA_MXM_CPU
Modify for C100VJ-M 1.1G
modify for 2.0G 05/19
<62> MXM2_disable
<22,38> MXM2_CLOSE
4/24 modify for MXM2
control ON/OFF
8/24 MXM
state
8/24 MXM present
pull high
DDCA_CLK, DDCA_DAT,
DDCB_CLK, DDCB_DAT,
DDCC_CLK, DDCC_DAT,
Should have 2.2K
PULL-UP to +3.3V on
MXM Module
THERM# -- Open Collector Output, Active Low, 5V tolerant
CLK_REQ# -- Output, Open Drain, Active Low
<Variant Name>
Title : MXM Interface
ASUSTek Computer Inc.
Engineer: Chad Lai
Size Custom
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 27 of 65

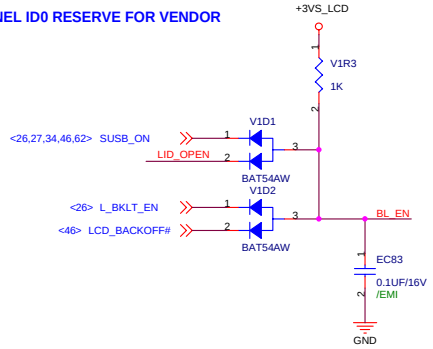
LCD Power

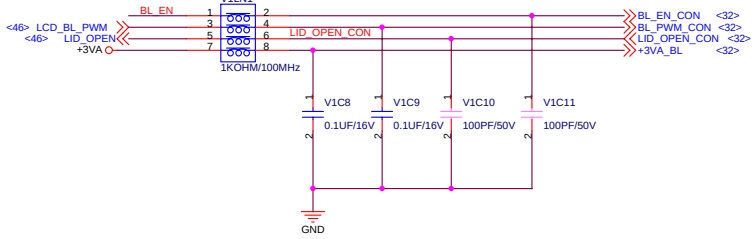


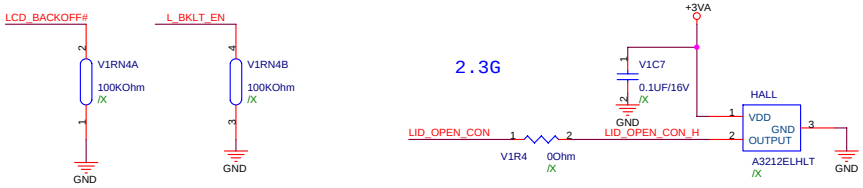
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

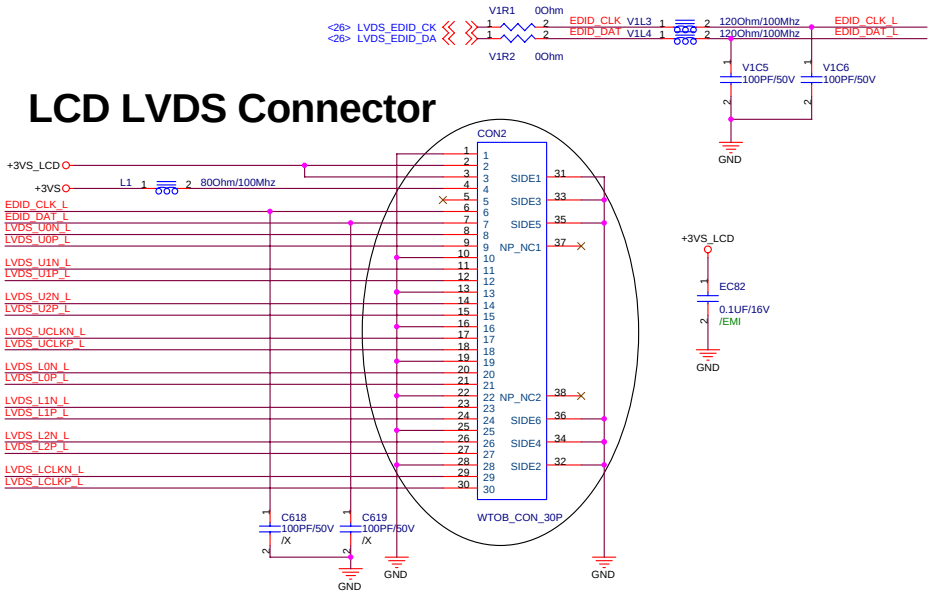
PANEL ID0 RESERVE FOR VENDOR

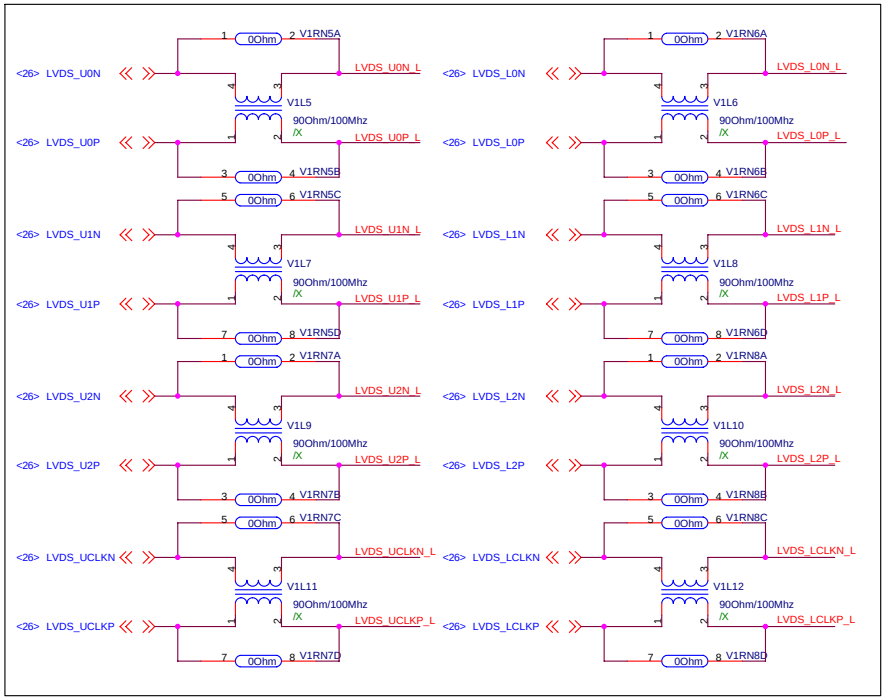






LCD LVDS Connector





<Variant Name>

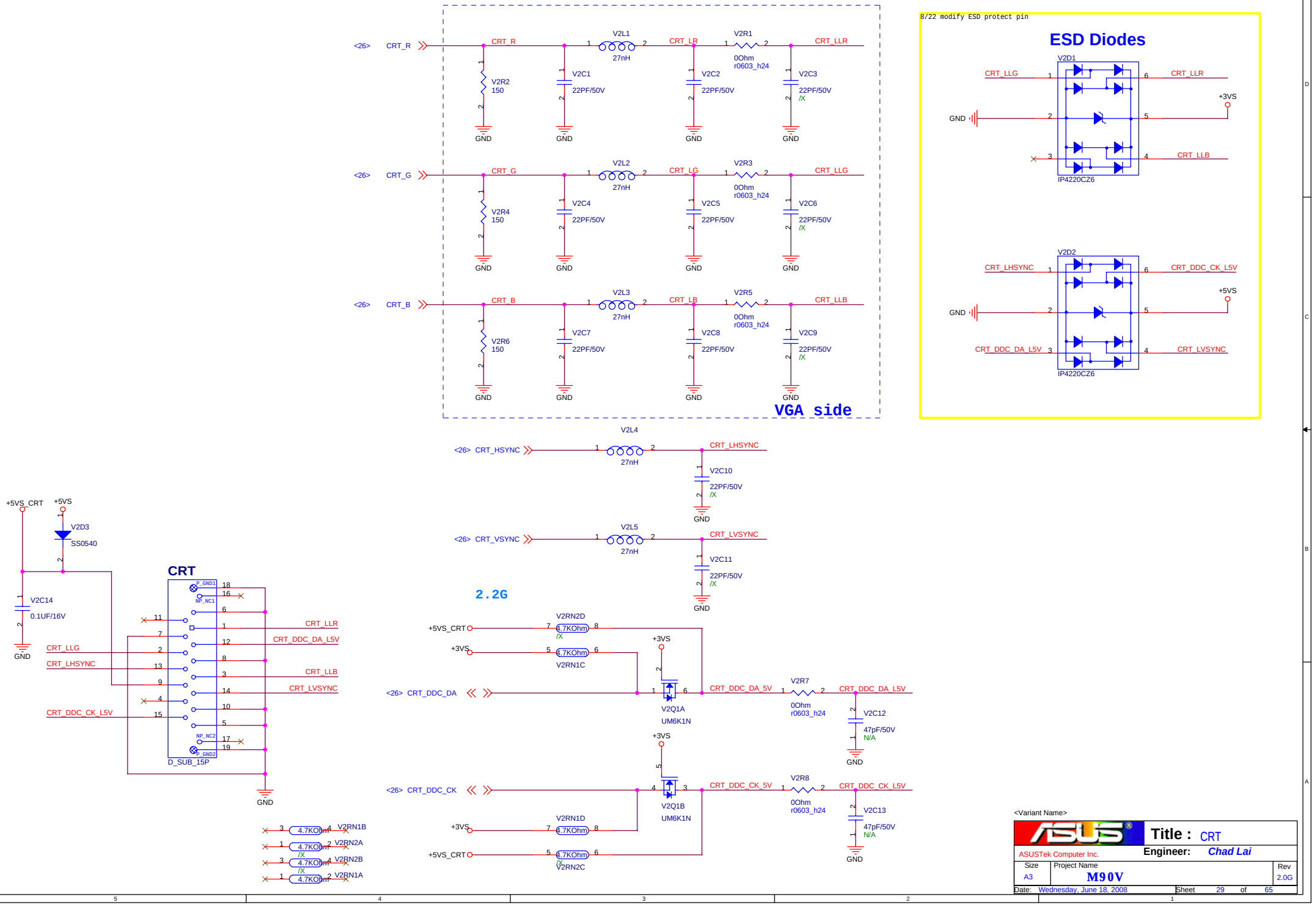
ASUSTek Computer Inc.

Title : LVDS & INVERTER

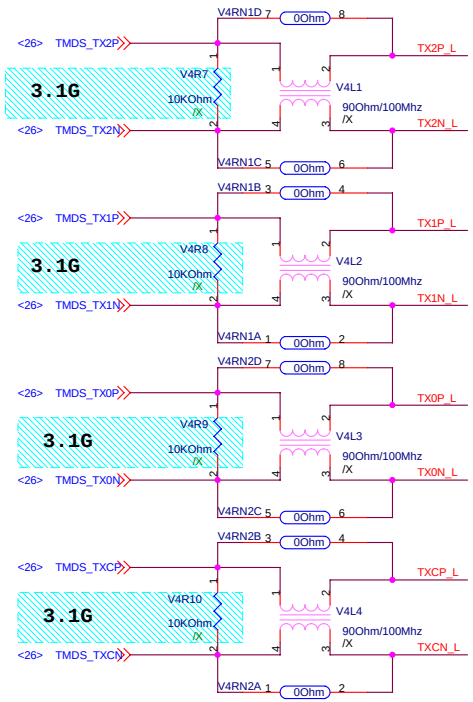
Engineer: *Chad Lai*

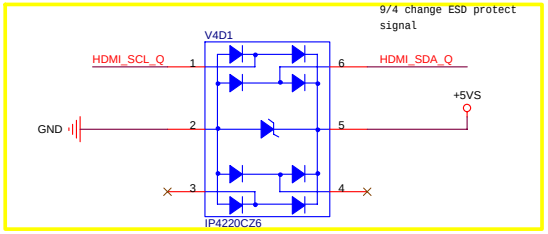
Size	Project Name	Rev
Custom	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 28 of 65

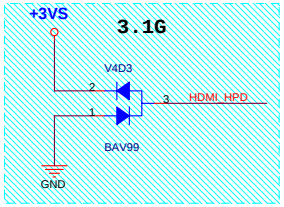

8/22 modify ESD protect pin
ESD Diodes
V2D1
IP4220CZ6
V2D2
IP4220CZ6
VGA side
2.2G
CRT
D_SUB_15P
V2D3
SS0540
V2C14
0.1UF/16V
V2L1
V2L2
V2L3
V2L4
V2L5
27nH
V2R1
V2R2
V2R3
V2R4
V2R5
V2R6
0Ohm
r0603_h24
150
V2C1
V2C2
V2C3
V2C4
V2C5
V2C6
V2C7
V2C8
V2C9
V2C10
V2C11
22PF/50V
/X
V2RN1A
V2RN1B
V2RN1C
V2RN1D
V2RN2A
V2RN2B
V2RN2C
V2RN2D
4.7KOhm
V2Q1A
V2Q1B
UM6K1N
V2R7
V2R8
V2C12
V2C13
47pF/50V
N/A
<Variant Name>
Title : CRT
ASUSTek Computer Inc.
Engineer: Chad Lai
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 29 of 65

Choke : TDK ACM2012 prefered

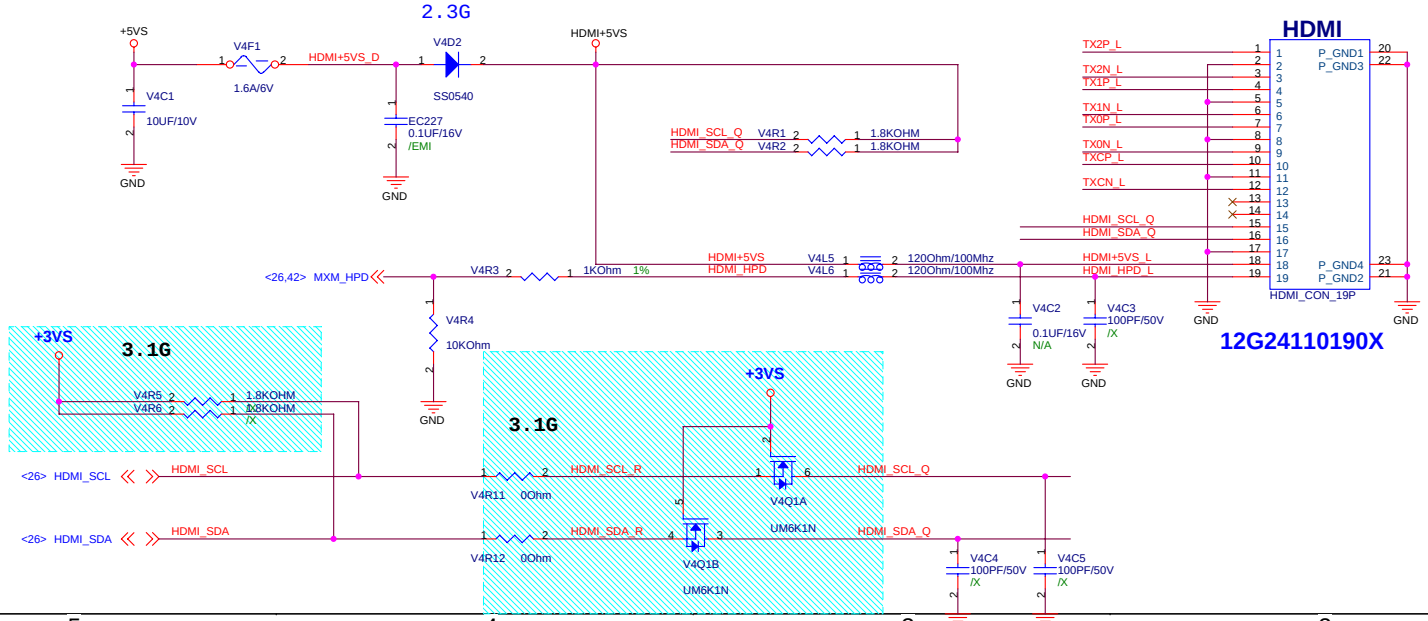




ESD Diode, Place close to Connector

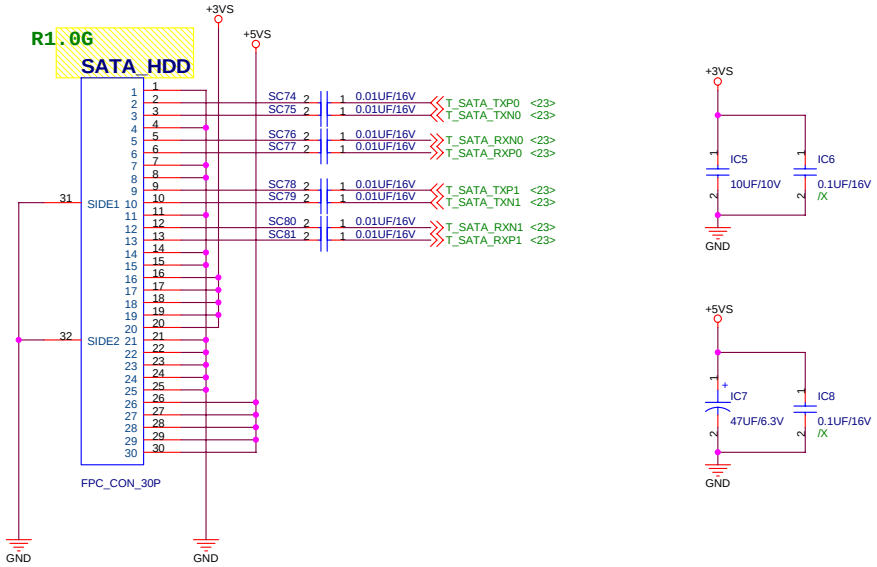


HDMI Connector

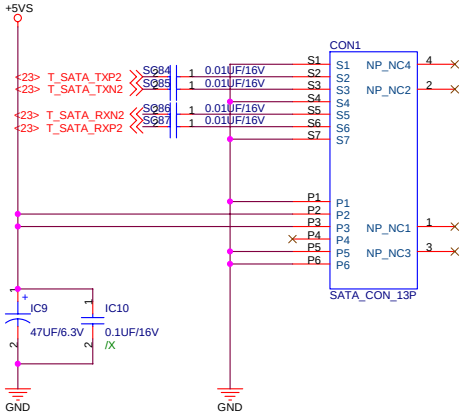


<Variant Name>

ASUSTek Computer INC.	Title : HDMI Connector	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 30 of 65	



SATA ODD



<Variant Name>

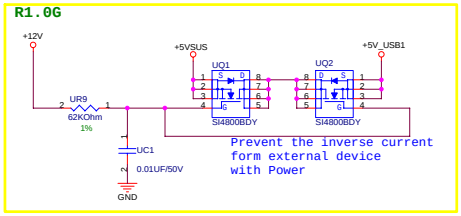
Title : SATA-HDD & ODD

ASUSTek Computer Inc.

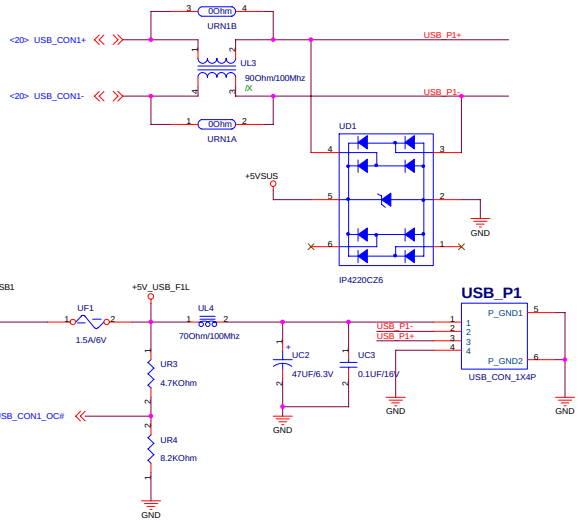
Engineer: Chad Lai

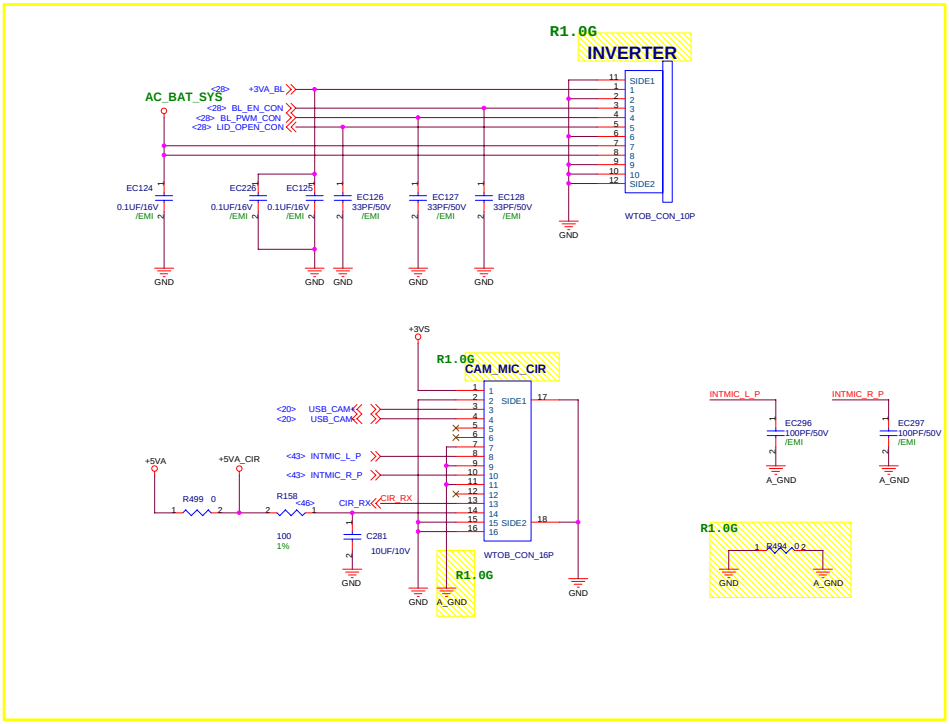
Size	Project Name	Rev
Custom	M90V	2.0G

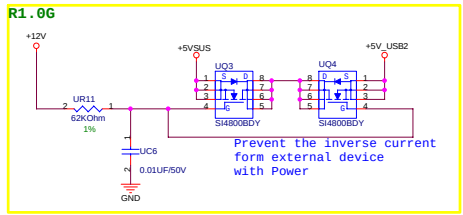
Date: Wednesday, June 18, 2008 Sheet 31 of 65



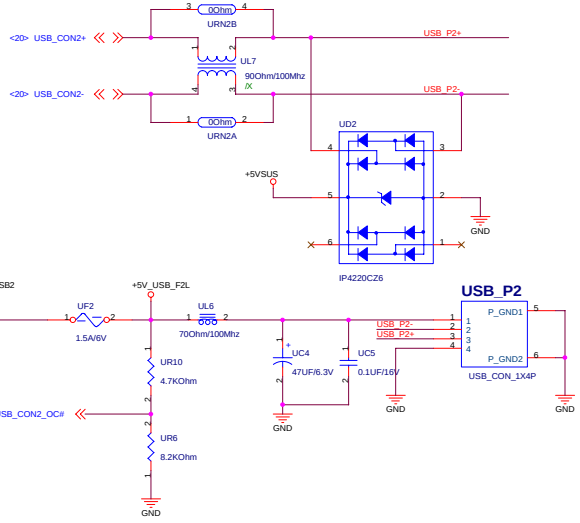
All close to USB connectors

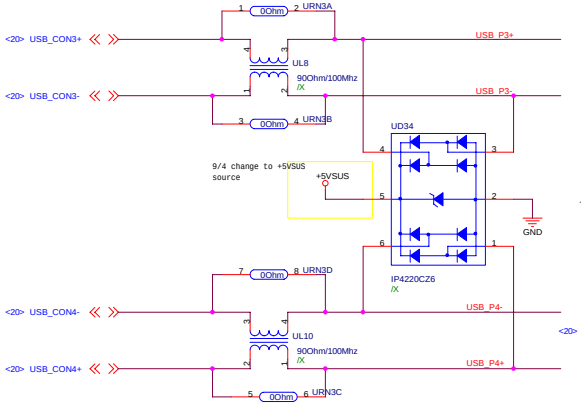


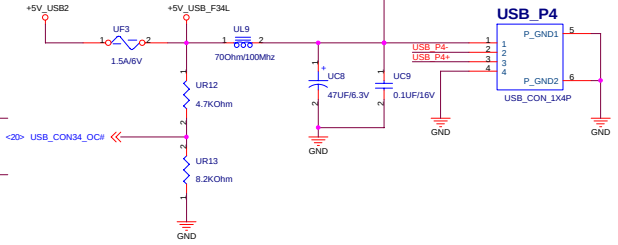




All close to USB connectors



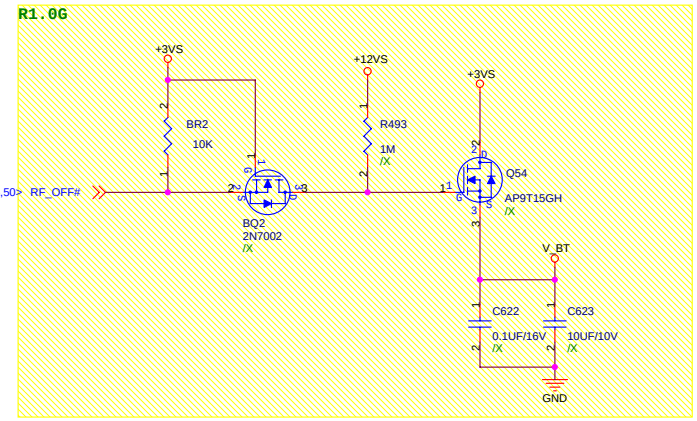


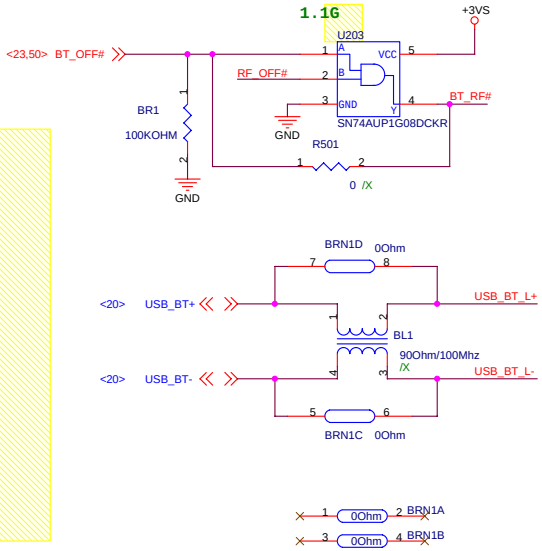


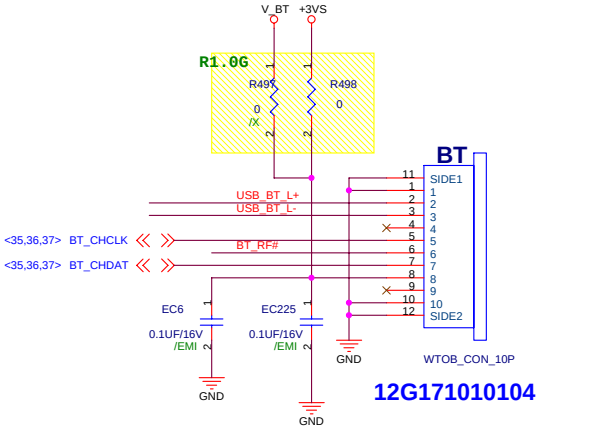
<Variant Name>

ASUSTek Computer Inc.	Title : USB CONN	
	Engineer: Chad Lai	
Size: A2	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 32 of 65	

Bluetooth Connector

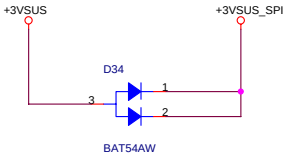


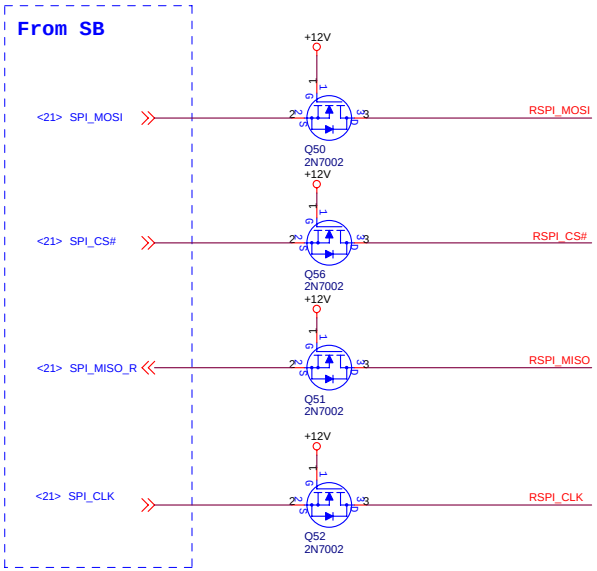


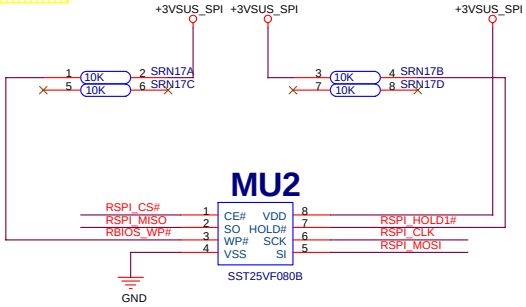


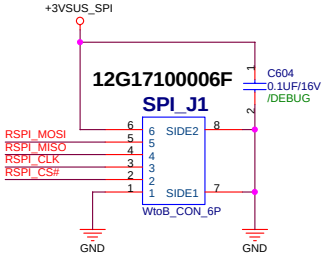
BT_OFF# : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

SPI Close To ICH9





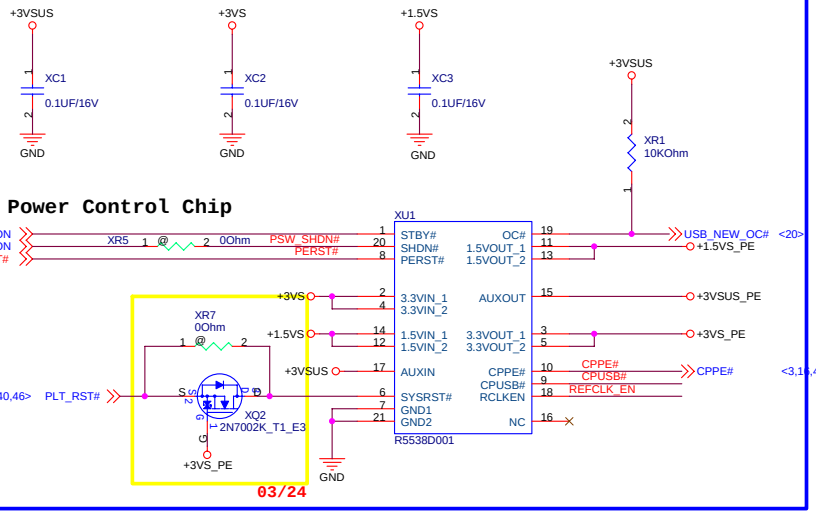




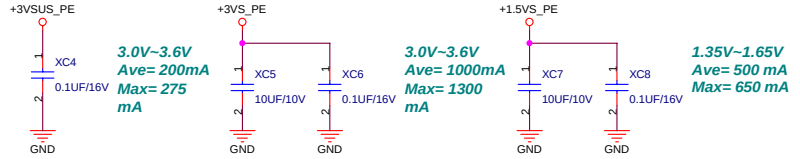
<Variant Name>

ASUSTek Computer Inc.	Title : Blue Tooth & SPI	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 33 of 65	

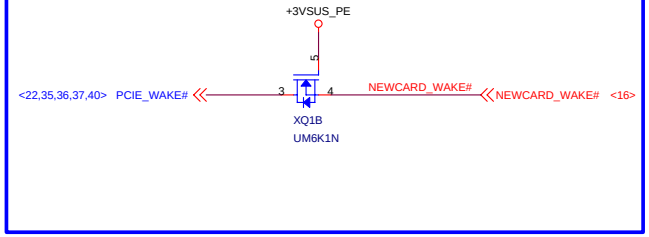
Decouple Cap. (Near XU1)



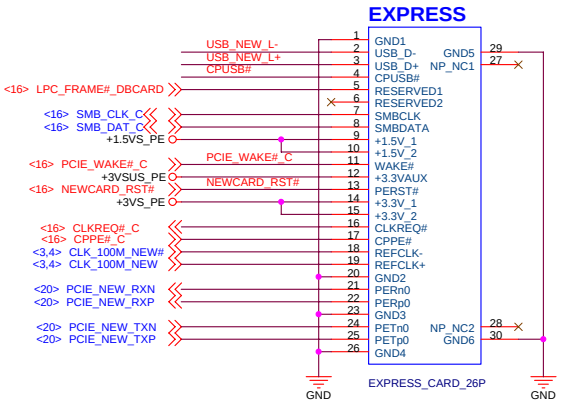
Decouple Cap. (Near Express connector)



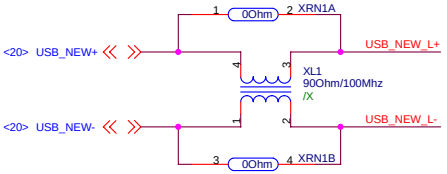
NEWCARD Wake#

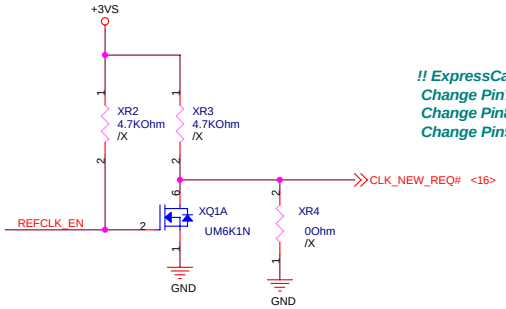


EXPRESS



USB CHOKE FOR EMI





!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

EJECTOR

12G21C20000P

<Variant Name>

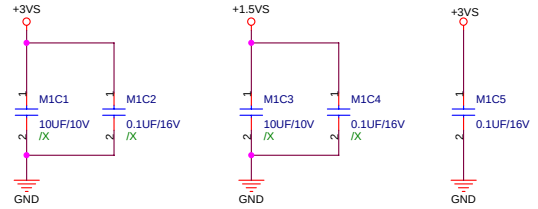
ASUSTek Computer Inc.	Title : NEWCARD	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 34 of 65	

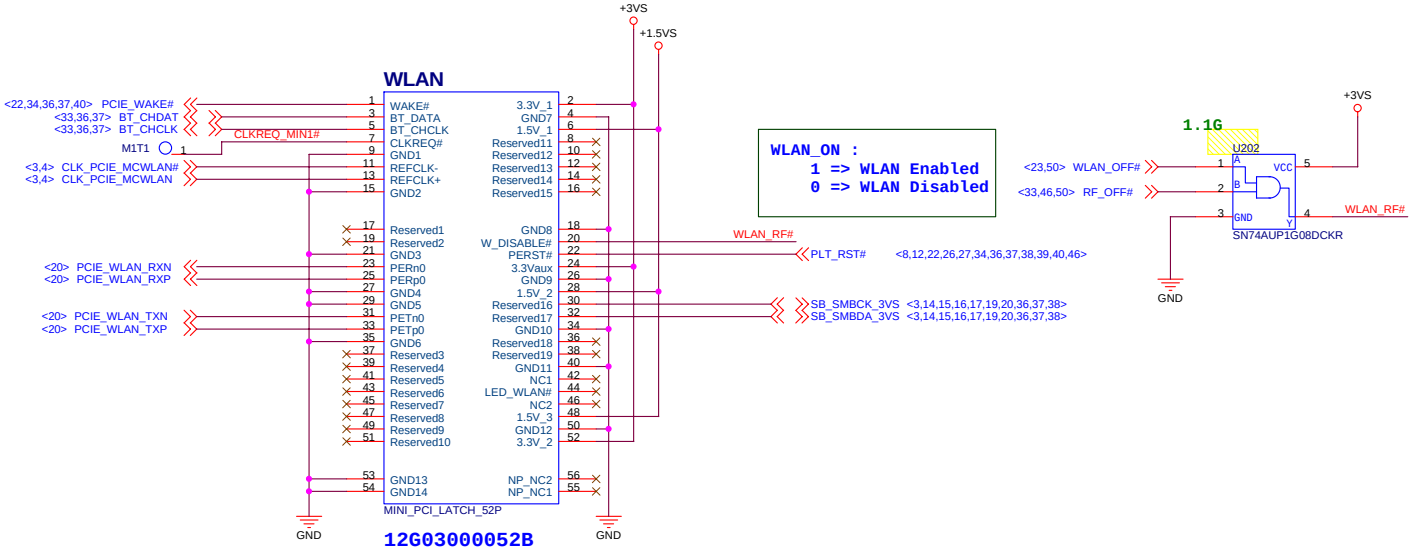
Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA





<Variant Name>

Title : MINI CARD

ASUSTek Computer Inc. **Engineer:** *Chad Lai*

Size	Project Name	Rev
Custom	M90V	2.0G

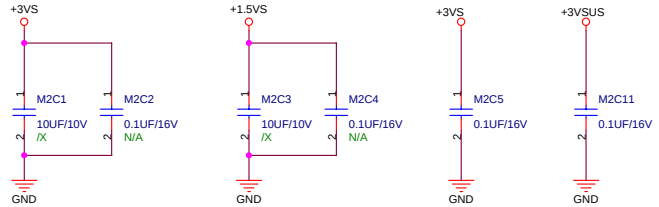
Date: Wednesday, June 18, 2008 Sheet 35 of 65

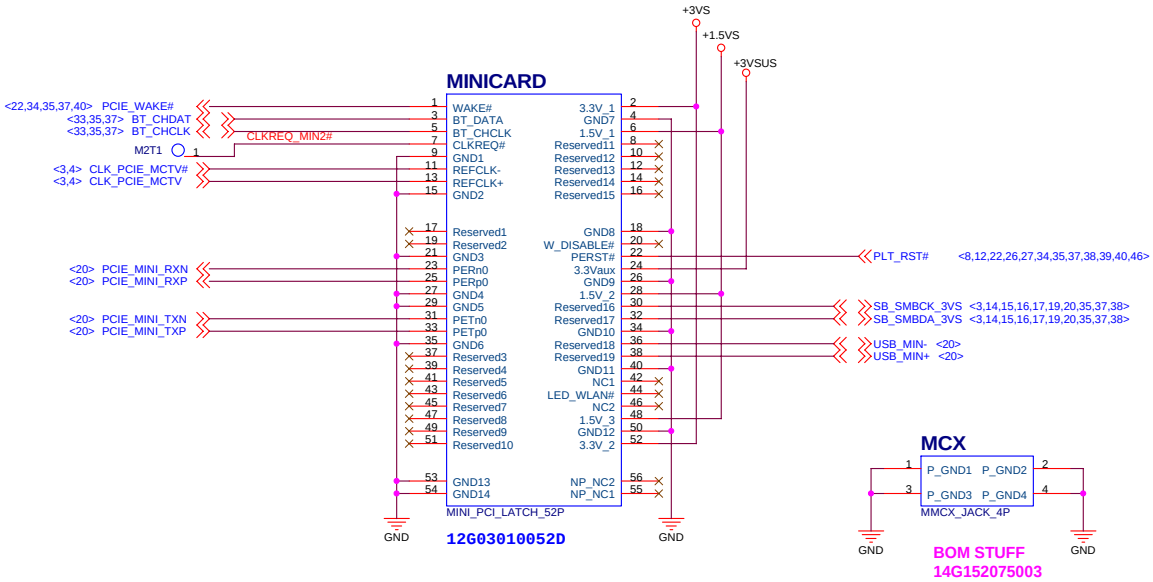
Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA





<Variant Name>

ASUSTek Computer Inc.

Title : MINI CARD

Engineer: *Chad Lai*

Size	Project Name	Rev
Custom	M90V	2.0G

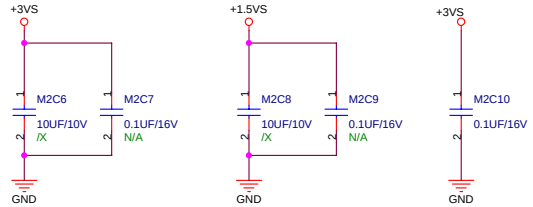
Date: Wednesday, June 18, 2008 Sheet 36 of 65

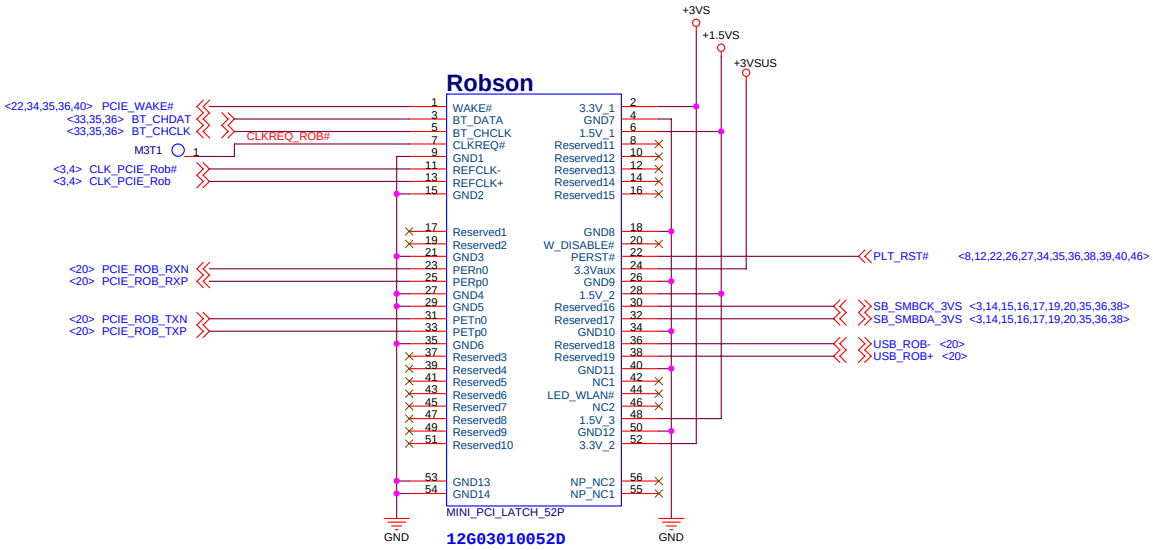
Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

+3.003V~+3.597V
Max= 250 mA

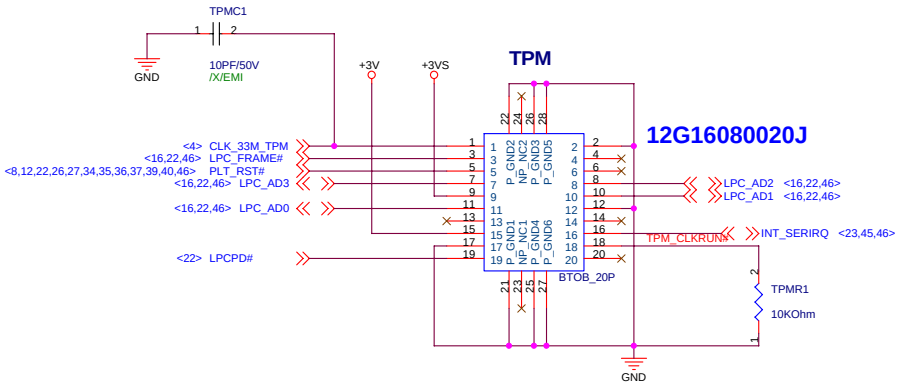




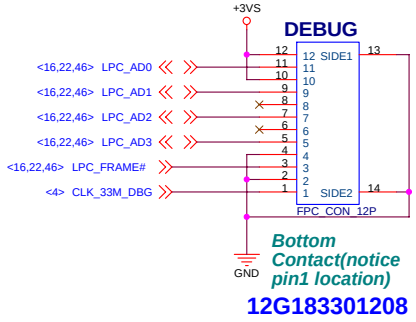
<Variant Name>

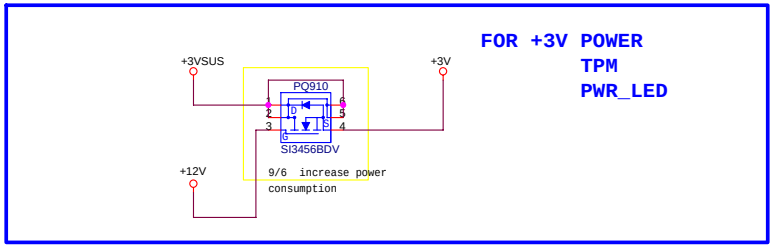
ASUSTek Computer Inc.	Title : MINI CARD	
	Engineer: *Chad Lai*	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 37 of 65	

TPM Connector

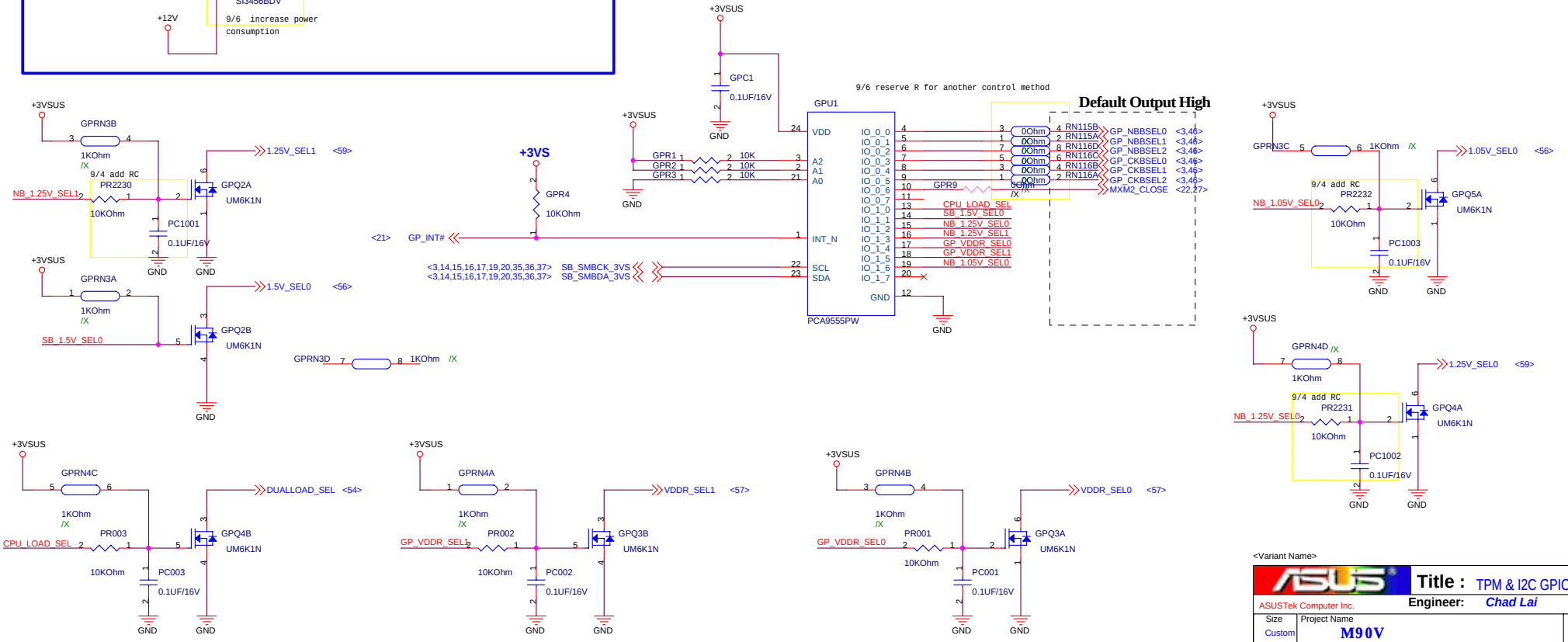


Debug Connector





I2C GPIO Controller



<Variant Name>

ASUSTek Computer Inc.	Title : TPM & I2C GPIO Controller	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 38 of 65	

Decouple Cap. (Near RU1)

ESATA+1.8VS (Total 260 mA)

ESATA+1.8VA

RL1 120Ohm/100Mhz

RC1 10UF/10V — Must

RC2 0.1UF/16V /X — Cost down

RC3 0.1UF/16V /X — Cost down

RC4 0.1UF/16V

RC5 0.1UF/16V

RC6 0.1UF/16V

+3VS 40 mA)

RC7 0.1UF/16V /X — Cost down

RC8 0.1UF/16V /X — Cost down

RC9 0.1UF/16V /X — Cost down

GND

R1.1 BOM update

RR1 10MOhm

RX1 25Mhz

ESATA_XI — ESATA_XO

RC10 22PF/50V

RC11 22PF/50V

GND

R1.1 - Layout

+3VS

RRN1A 4.7KOhm

RRN1B 4.7KOhm

RRN1C 4.7KOhm

RRN1D 4.7KOhm

ESATA+1.8VA

ESATA+1.8VS +3VS

ESATA_LED# <50>

PLT_RST# <8,12,22,26,27,34,35,36,37,38,40,46>

ZSMBCLK

ZSMBDAT

RU1

JMB360

DG18_1, XRSTn, ZSMBDAT, XSMBCLK, DV33_2, DG33_2, DG18_2, DV18_3, YHDTEDn, XTEST, DG18_3, ZGPIO3

DV18_1, APCLKN, APCLKP, APVDD, APGND, APREXT, APRXP, APRXN, APV18, APG18, APTXN, APTXP

ZGPIO2, ZGPIO1, ZGPIO0, DV18_2, DV33_1, DG33_1, NC2, NC3, NC4, NC5, NC6, NC7

NC1, ASXIN, ASXOUT, ASV33, ASG33, ASREXT, ASRXP, ASRXN, ASV18, ASG18, ASTXN, ASTXP

<3,4> CLK_PCIE_ESATA#

<3,4> CLK_PCIE_ESATA

<20> PCIE_ESATA_TXP

<20> PCIE_ESATA_TXN

<20> PCIE_ESATA_RXN

<20> PCIE_ESATA_RXP

RC12 0.1UF/16V — C_PCIE_ESATA_RXN

RC13 0.1UF/16V — C_PCIE_ESATA_RXP

ESATA_XI

ESATA_XO

ESATA_RX0

ESATA_RX0#

ESATA_TX0#

ESATA_TX0

PCIE_STRAP

ESATA_STRAP

GND

Power Solution for E-SATA !!

Date : 09/01/2006

ESATA+1.8VS

Io=0.5A

+1.8VS

RL2 120Ohm/100Mhz /X

ESATA+1.8VS

+3VS

T1PQ1 ADJ/GND, OUT, Vout, IN — GS1117AXF

T1PR1 120Ohm 1%

T1PR2 56.2Ohm 1%

T1PC1 0.1UF/16V

T1PC2 0.1UF/16V /X

T1PCE1 100UF/2.5V

P_1.8VSATA_ADJ_10

PL_CAP

GND

Vout=Vref(1+T1PR2/T1PR1)=1.25*(1+56.2/120)=1.835V*

ESATA Connector

BOM stuff 12G15110007P

ESATA_TX0 — RC14 0.01UF/16V — ESATA_TX0_C

ESATA_TX0# — RC15 0.01UF/16V — ESATA_TX0#_C

ESATA_RX0# — RC16 0.01UF/16V — ESATA_RX0#_C

ESATA_RX0 — RC17 0.01UF/16V — ESATA_RX0_C

Place near connector

ESATA

GND1, TX+, TX-, GND2, RX-, RX+, GND3, P_GND1, P_GND2, P_GND3, P_GND4, NP_NC1, NP_NC2

SATA_CON_7P

GND

12G15110007M

PCIE_STRAP

RR4 8.2KOhm

PCB R1.0 BOM update

Place RR4 close to pin 6

ESATA_STRAP

RR5 12KOhm 1%

Place RR5 close to pin 18

<Variant Name>

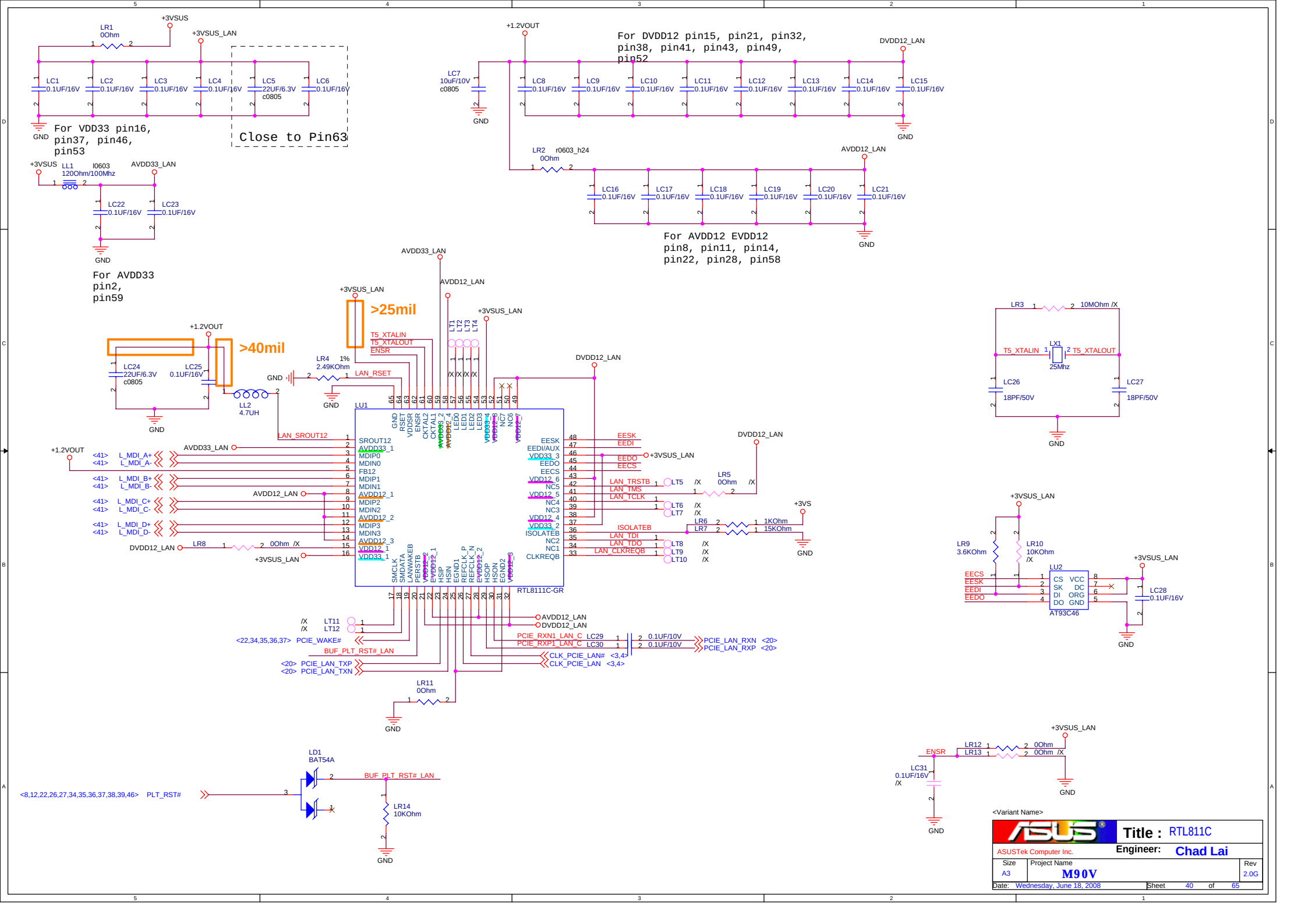
ASUSTek Computer INC.

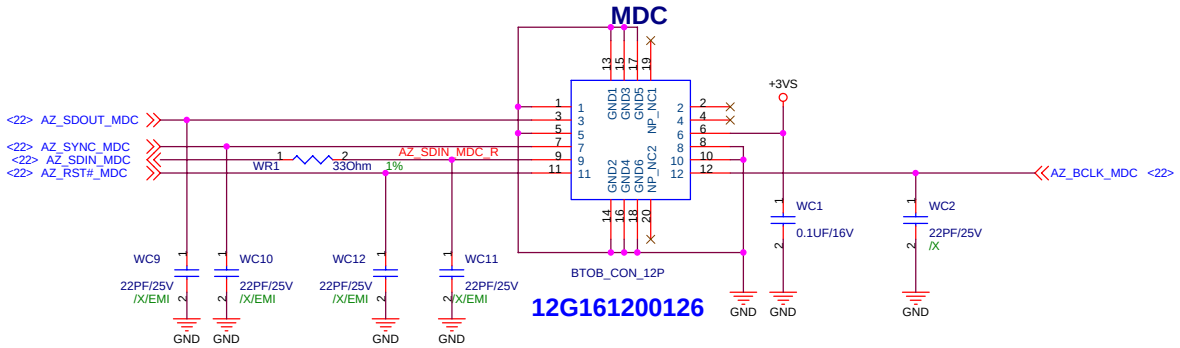
Title : ESATA-JMB360

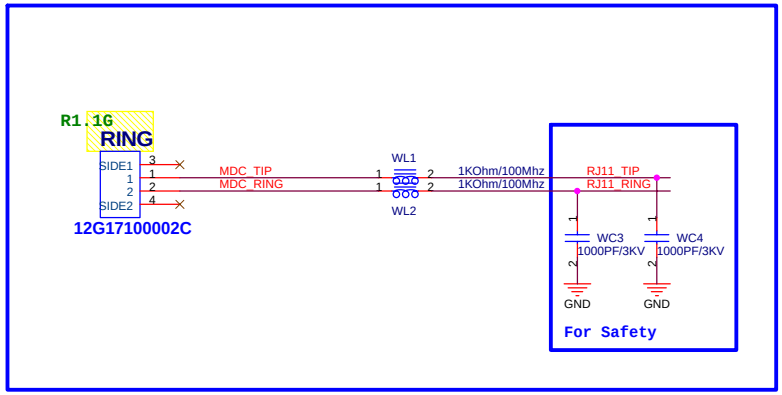
Engineer: Chad Lai

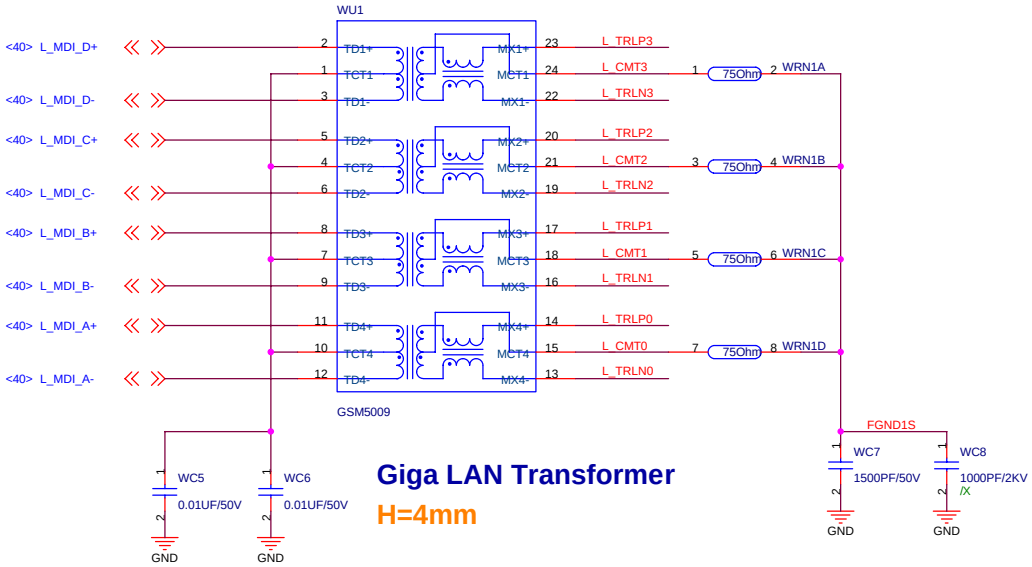
Size	Project Name	Rev
A3	M90V	2.0G

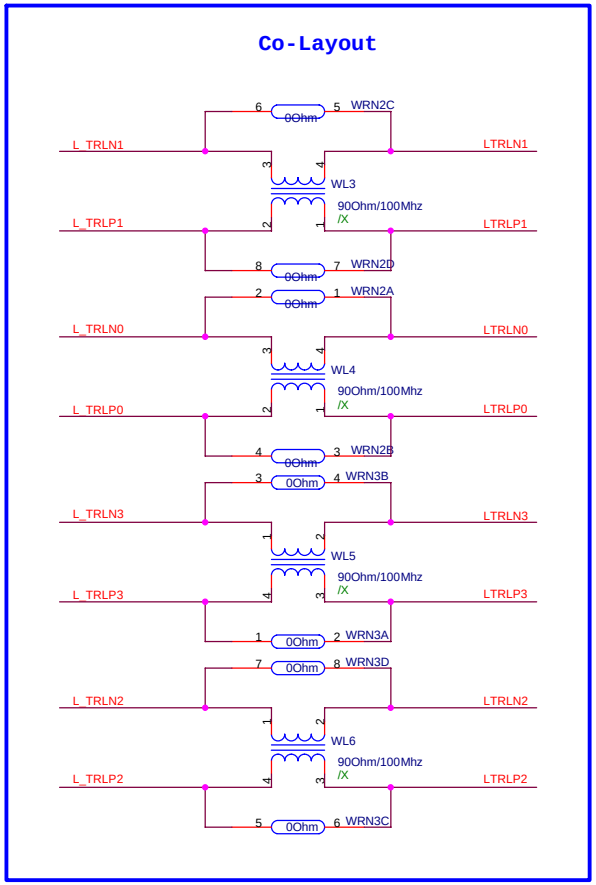
Date: Wednesday, June 18, 2008 Sheet 39 of 65

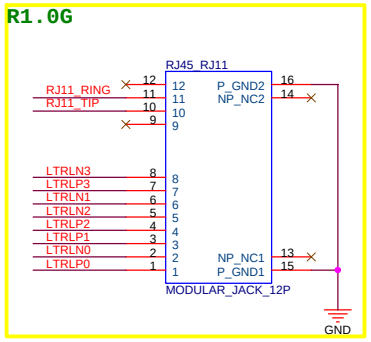

+3VSUS
LR1 0Ohm
+3VSUS_LAN
LC1 0.1UF/16V
LC2 0.1UF/16V
LC3 0.1UF/16V
LC4 0.1UF/16V
LC5 22UF/6.3V c0805
LC6 0.1UF/16V
GND
For VDD33 pin16, pin37, pin46, pin53
Close to Pin63
+1.2VOUT
For DVDD12 pin15, pin21, pin32, pin38, pin41, pin43, pin49, pin52
DVDD12_LAN
LC7 10uF/10V c0805
LC8 0.1UF/16V
LC9 0.1UF/16V
LC10 0.1UF/16V
LC11 0.1UF/16V
LC12 0.1UF/16V
LC13 0.1UF/16V
LC14 0.1UF/16V
LC15 0.1UF/16V
LL1 120Ohm/100Mhz l0603
AVDD33_LAN
LC22 0.1UF/16V
LC23 0.1UF/16V
LR2 0Ohm r0603_h24
AVDD12_LAN
LC16 0.1UF/16V
LC17 0.1UF/16V
LC18 0.1UF/16V
LC19 0.1UF/16V
LC20 0.1UF/16V
LC21 0.1UF/16V
For AVDD12 EVDD12 pin8, pin11, pin14, pin22, pin28, pin58
For AVDD33 pin2, pin59
>25mil
>40mil
LC24 22UF/6.3V c0805
LC25 0.1UF/16V
LL2 4.7UH
LR4 2.49KOhm 1%
LAN_RSET
LU1
RTL8111C-GR
LAN_SROUT12
T5_XTALIN
T5_XTALOUT
ENSR
LR3 10MOhm /X
LX1 25Mhz
LC26 18PF/50V
LC27 18PF/50V
L_MDI_A+
L_MDI_A-
L_MDI_B+
L_MDI_B-
L_MDI_C+
L_MDI_C-
L_MDI_D+
L_MDI_D-
LR8 0Ohm /X
LR5 0Ohm /X
LR6 1KOhm
LR7 15KOhm
LR9 3.6KOhm
LR10 10KOhm /X
LU2 AT93C46
LC28 0.1UF/16V
EESK
EEDI
EEDO
EECS
LAN_TRSTB
LAN_TMS
LAN_TCLK
ISOLATEB
LAN_TDI
LAN_TDO
LAN_CLKREQB
PCIE_WAKE#
BUF_PLT_RST#_LAN
PCIE_RXN1_LAN_C LC29 0.1UF/10V
PCIE_RXP1_LAN_C LC30 0.1UF/10V
PCIE_LAN_RXN
PCIE_LAN_RXP
CLK_PCIE_LAN#
CLK_PCIE_LAN
PCIE_LAN_TXP
PCIE_LAN_TXN
LR11 0Ohm
LD1 BAT54A
PLT_RST#
LR14 10KOhm
LR12 0Ohm
LR13 0Ohm /X
LC31 0.1UF/16V /X
<Variant Name>
Title : RTL811C
ASUSTek Computer Inc.
Engineer: Chad Lai
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 40 of 65





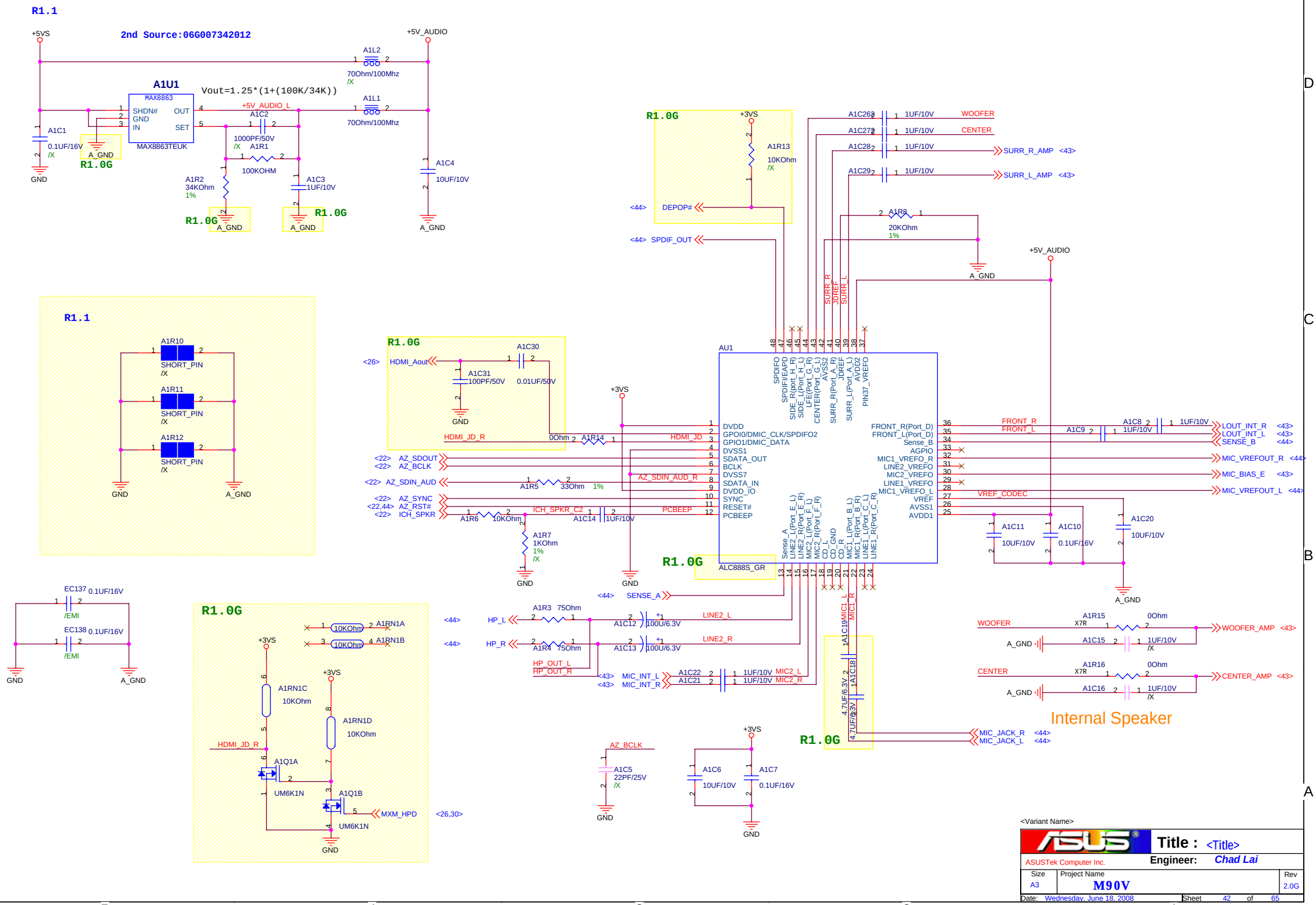


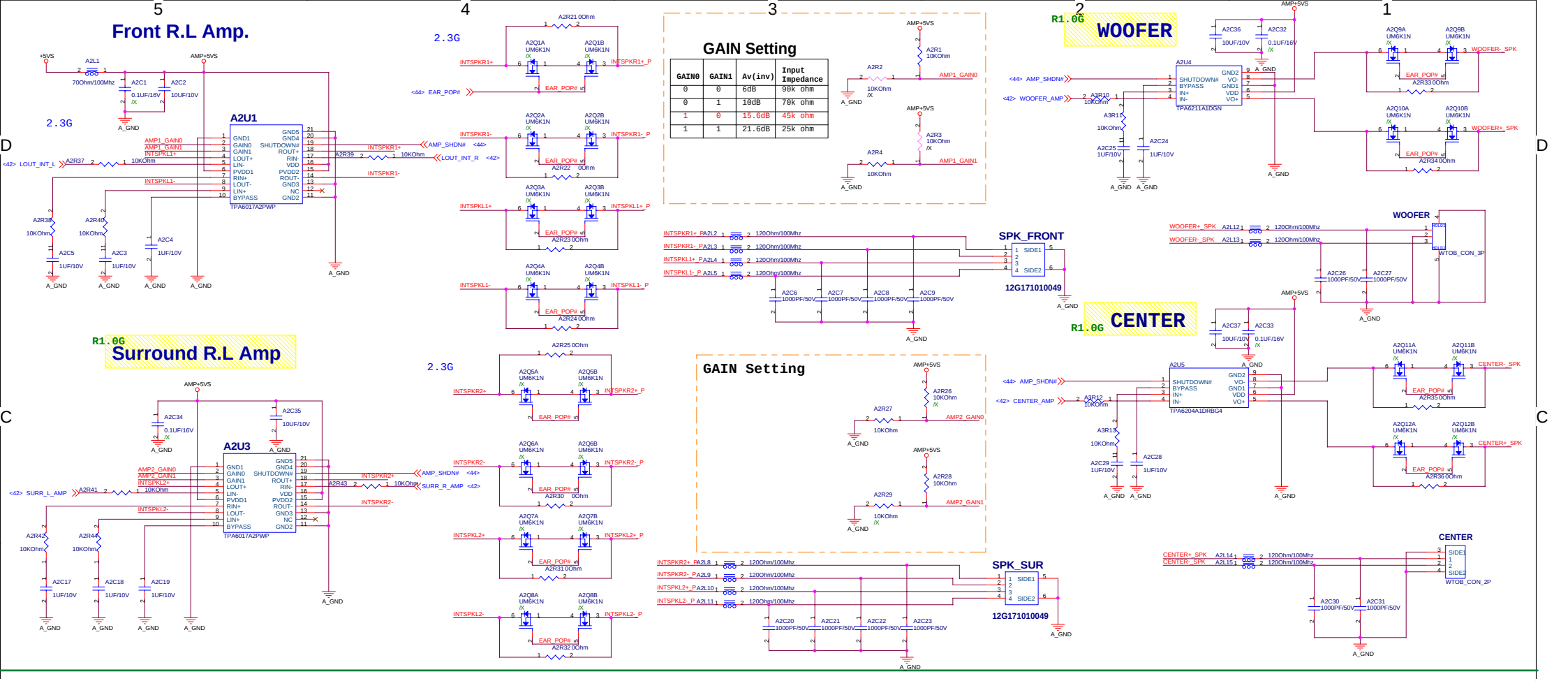




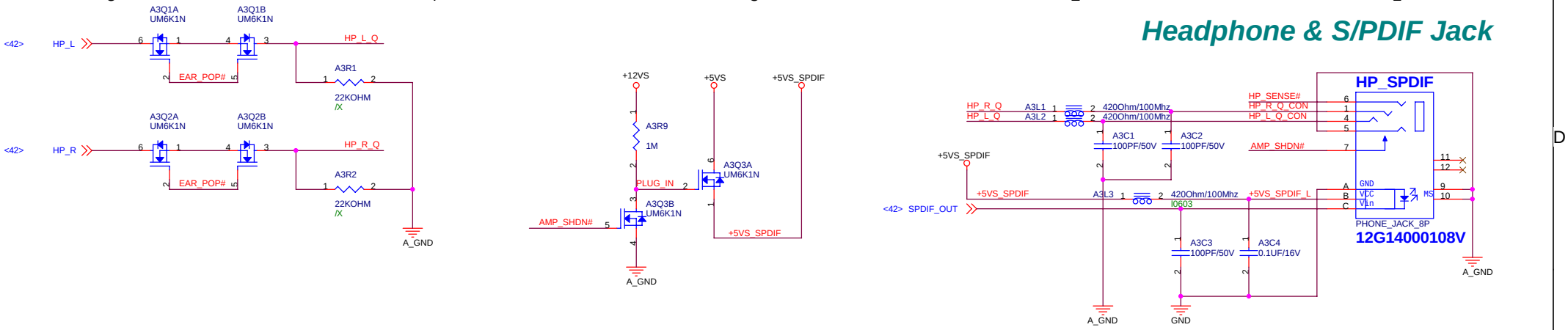
<Variant Name>

ASUSTek Computer Inc.	Title : MDC / RJ45	
	Engineer: Chad Lai	
Size: A3	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 41 of 65	


R1.1
2nd Source:06G007342012
+5VS
+5V_AUDIO
A1U1
MAX8863
Vout=1.25*(1+(100K/34K))
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
+5V_AUDIO_L
A1L2
A1L1
70Ohm/100Mhz
/X
A1C1
0.1UF/16V
A1C2
1000PF/50V
A1R1
100KOHM
A1R2
34KOhm
1%
A1C3
1UF/10V
A1C4
10UF/10V
A_GND
R1.0G
R1.1
A1R10
A1R11
A1R12
SHORT_PIN
R1.0G
+3VS
A1R13
10KOhm
DEPOP#
SPDIF_OUT
A1C26
A1C27
A1C28
A1C29
1UF/10V
WOOFER
CENTER
SURR_R_AMP
SURR_L_AMP
A1R8
20KOhm
HDMI_Aout
A1C30
A1C31
100PF/50V
0.01UF/50V
HDMI_JD_R
0Ohm
A1R14
HDMI_JD
AU1
DVDD
GPOI0/DMIC_CLK/SPDIFO2
GPIO1/DMIC_DATA
DVSS1
SDATA_OUT
BCLK
DVSS7
SDATA_IN
DVDD_IO
SYNC
RESET#
PCBEEP
SPDIFO
SPDIF/EAPD
SIDE_R(port_H_R)
SIDE_L(Port_H_L)
LFE(Port_G_R)
CENTER(Port_G_L)
AVSS2
SURR_R(Port_A_R)
JDREF
SURR_L(Port_A_L)
AVDD2
PIN37_VREFO
FRONT_R(Port_D)
FRONT_L(Port_D)
Sense_B
AGPIO
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
LINE1_VREFO
MIC1_VREFO_L
VREF
AVSS1
AVDD1
AZ_SDOUT
AZ_BCLK
AZ_SDIN_AUD
AZ_SYNC
AZ_RST#
ICH_SPKR
ICH_SPKR_C2
A1R5
33Ohm
AZ_SDIN_AUD_R
A1R6
10KOhm
A1C14
A1R7
1KOhm
ALC888S_GR
SENSE_A
HP_L
HP_R
A1R3
75Ohm
A1R4
A1C12
A1C13
100U/6.3V
LINE2_L
LINE2_R
HP_OUT_L
HP_OUT_R
MIC_INT_L
MIC_INT_R
A1C22
A1C21
MIC2_L
MIC2_R
FRONT_R
FRONT_L
A1C9
A1C8
LOUT_INT_R
LOUT_INT_L
SENSE_B
MIC_VREFOUT_R
MIC_BIAS_E
MIC_VREFOUT_L
VREF_CODEC
A1C11
A1C10
A1C20
10UF/10V
0.1UF/16V
EC137
EC138
/EMI
A1R1A
A1R1B
A1R1C
A1R1D
A1Q1A
A1Q1B
UM6K1N
HDMI_JD_R
MXM_HPD
<26,30>
AZ_BCLK
A1C5
22PF/25V
A1C6
A1C7
WOOFER
CENTER
A1R15
A1R16
X7R
0Ohm
A1C15
A1C16
WOOFER_AMP
CENTER_AMP
Internal Speaker
MIC_JACK_R
MIC_JACK_L
<Variant Name>
Title : <Title>
ASUSTek Computer Inc.
Engineer: Chad Lai
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 42 of 65

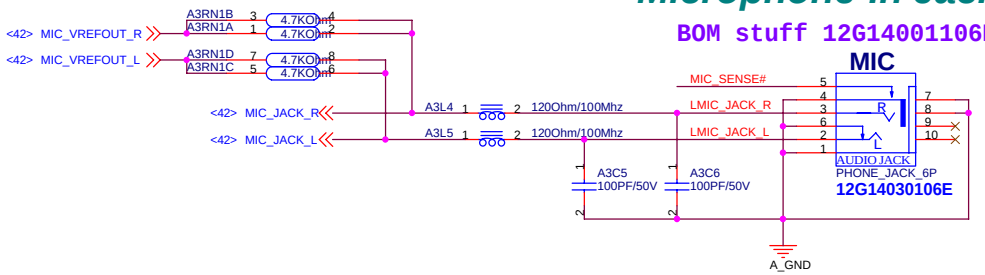

Front R.L Amp.
2.3G
A2U1
TPA6017A2PWP
GAIN Setting
GAIN0 GAIN1 Av(inv) Input Impedance
0 0 6dB 90k ohm
0 1 10dB 70k ohm
1 0 15.6dB 45k ohm
1 1 21.6dB 25k ohm
SPK_FRONT
12G171010049
WOOFER
R1.0G
TPA6211A1DGN
CENTER
TPA6204A1DRBG4
Surround R.L Amp
A2U3
GAIN Setting
SPK_SUR
12G171010049
Internal MIC Amp.
FL = 33.86Hz, FH = 22.5kHz
Place Near INTMIC Connector
A2U2
LMV358IDR
R1.1
R1.2

Headphone & S/PDIF Jack

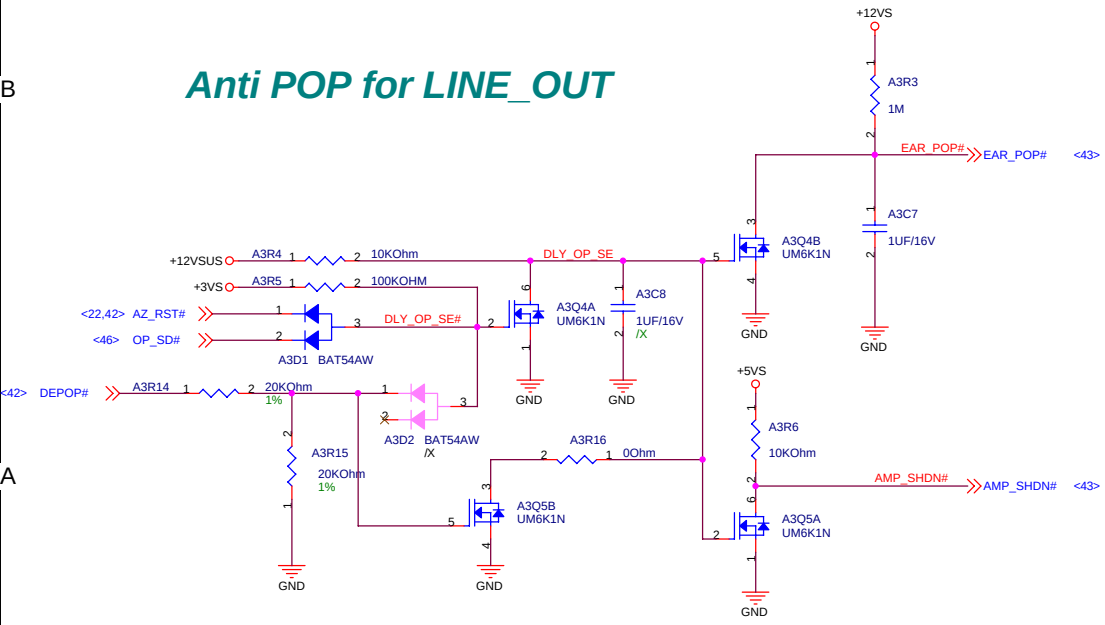


Microphone-In Jack

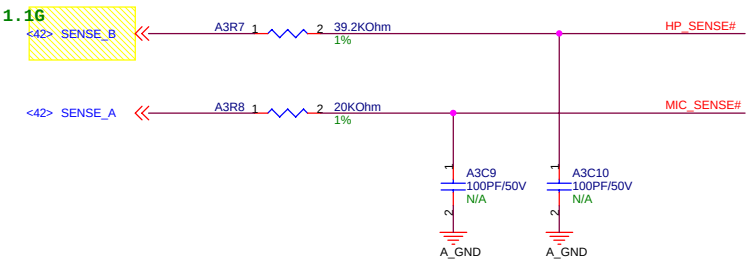
BOM stuff 12G14001106M



Anti POP for LINE_OUT



Jack Plug-in Detection



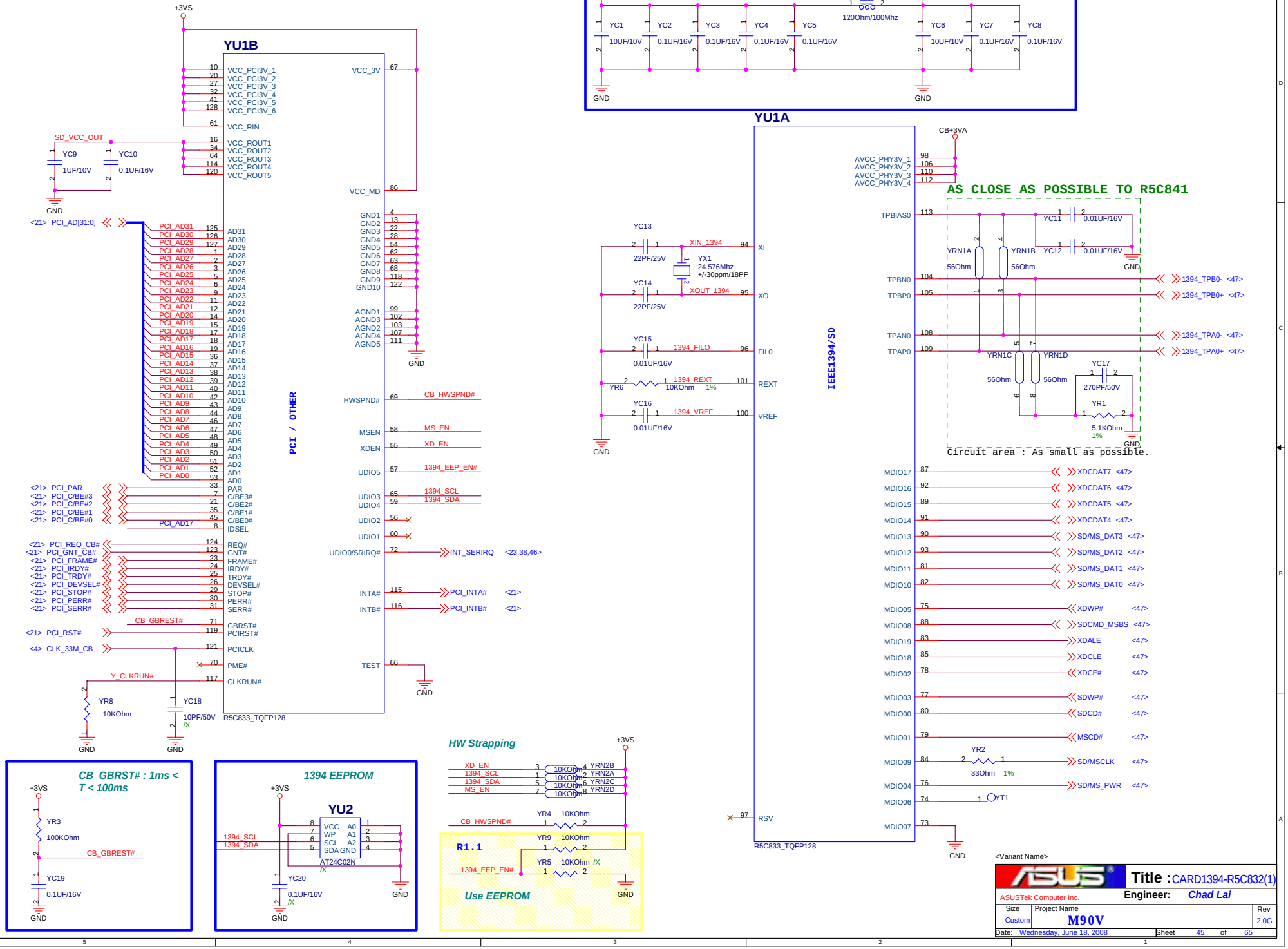
<Variant Name>

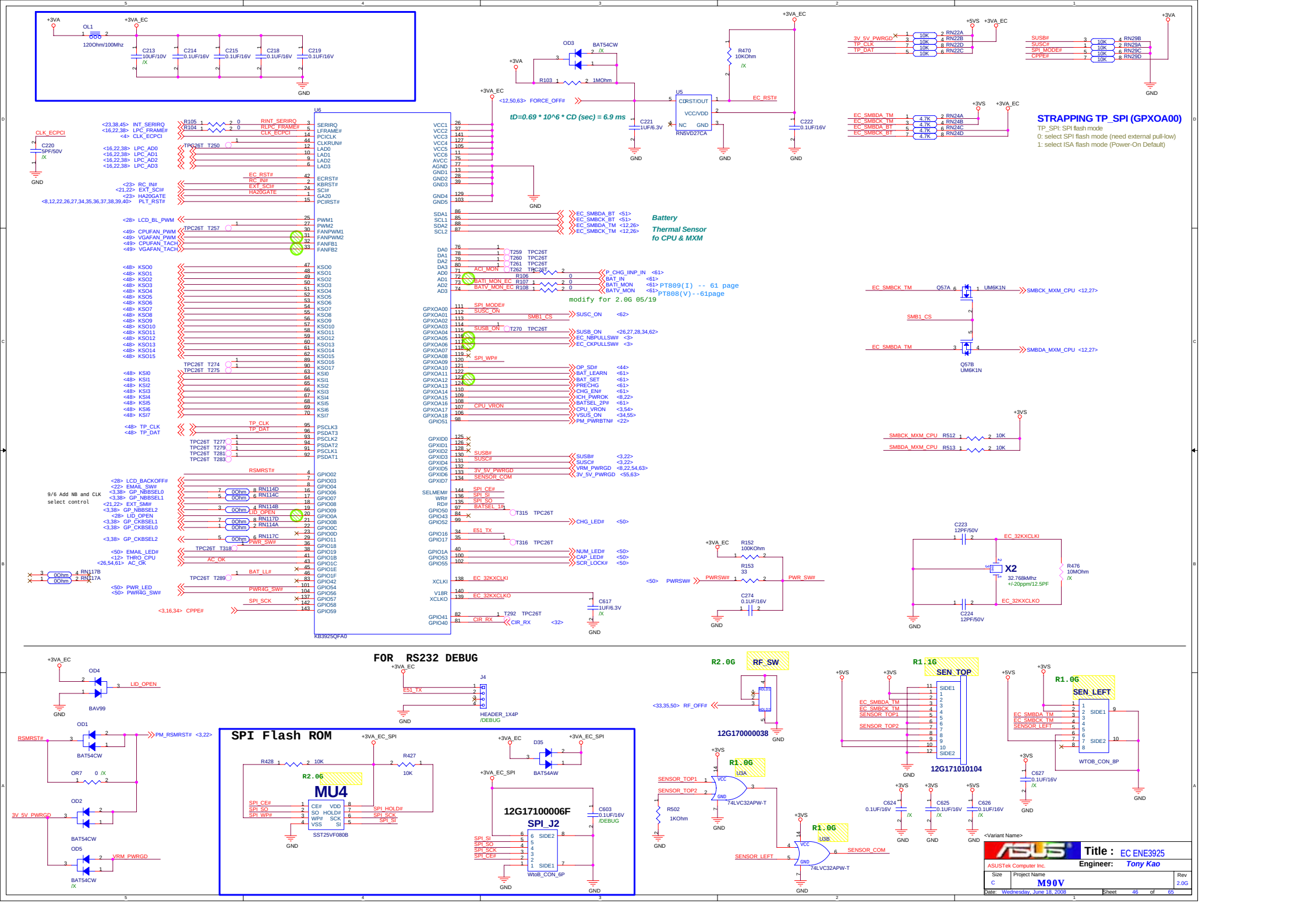
Title : SCH page name

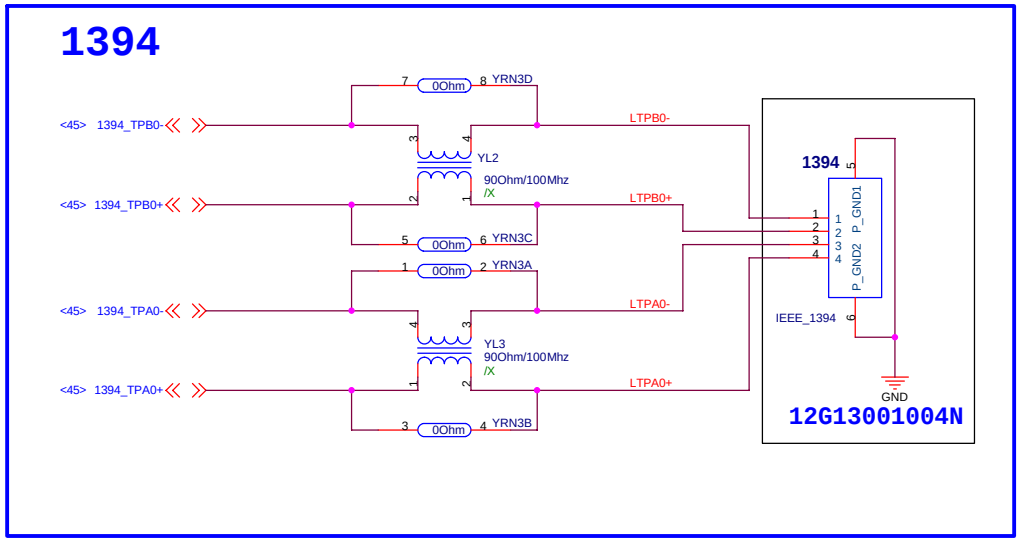
ASUSTek Computer Inc. Engineer: Chad Lai

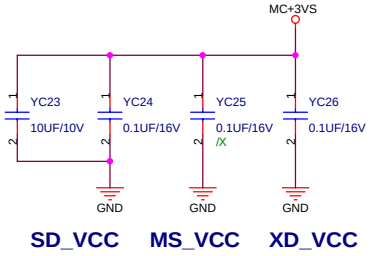
Size	Project Name	Rev
A3	M90V	2.0G

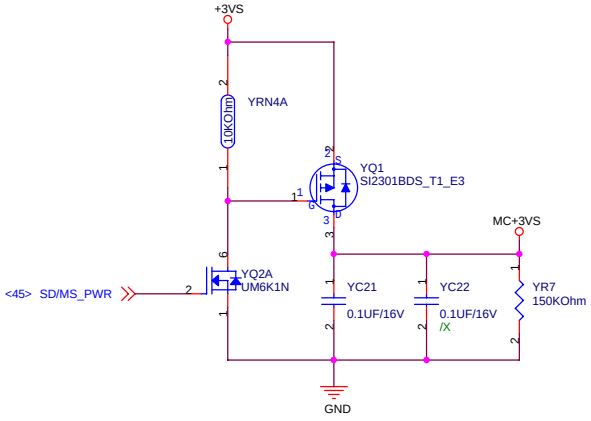
Date: Wednesday, June 18, 2008 Sheet 44 of 65

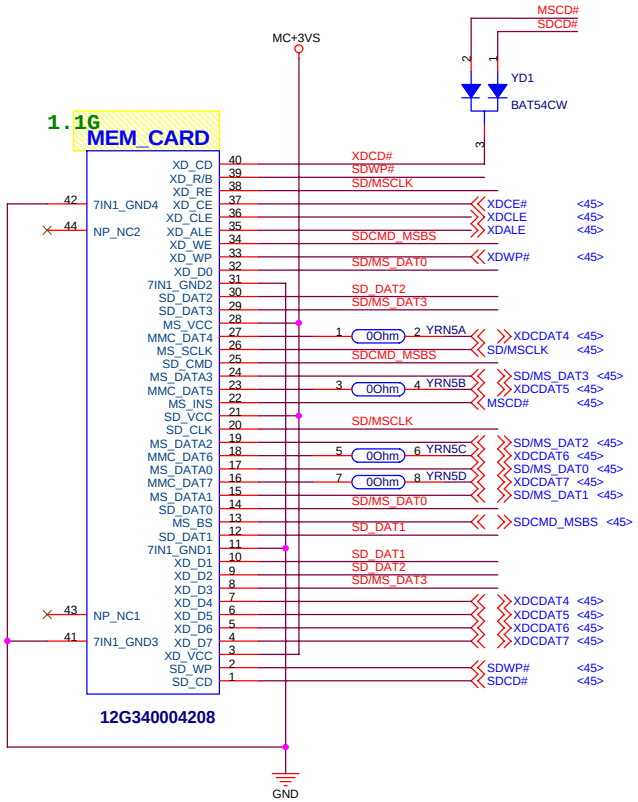

Decouple Cap. (Near YU1)
+3VS
CB+3VA
YL1
120Ohm/100Mhz
YC1 10UF/10V
YC2 0.1UF/16V
YC3 0.1UF/16V
YC4 0.1UF/16V
YC5 0.1UF/16V
YC6 10UF/10V
YC7 0.1UF/16V
YC8 0.1UF/16V
GND
YU1B
PCI / OTHER
VCC_PCI3V_1
VCC_PCI3V_2
VCC_PCI3V_3
VCC_PCI3V_4
VCC_PCI3V_5
VCC_PCI3V_6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
SD_VCC_OUT
YC9 1UF/10V
YC10 0.1UF/16V
<21> PCI_AD[31:0]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
<21> PCI_PAR
<21> PCI_C/BE#3
<21> PCI_C/BE#2
<21> PCI_C/BE#1
<21> PCI_C/BE#0
PCI_AD17
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
<21> PCI_REQ_CB#
<21> PCI_GNT_CB#
<21> PCI_FRAME#
<21> PCI_IRDY#
<21> PCI_TRDY#
<21> PCI_DEVSEL#
<21> PCI_STOP#
<21> PCI_PERR#
<21> PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
CB_GBREST#
<21> PCI_RST#
GBRST#
PCIRST#
<4> CLK_33M_CB
PCICLK
PME#
Y_CLKRUN#
CLKRUN#
YR8 10KOhm
YC18 10PF/50V /X
R5C833_TQFP128
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND3
AGND2
AGND4
AGND5
HWSPND#
CB_HWSPND#
MSEN
MS_EN
XDEN
XD_EN
UDIO5
1394_EEP_EN#
UDIO3
UDIO4
1394_SCL
1394_SDA
UDIO2
UDIO1
UDIO0/SRIRQ#
INT_SERIRQ
<23,38,46>
INTA#
PCI_INTA#
INTB#
PCI_INTB#
TEST
YU1A
IEEE1394/SD
XIN_1394
XOUT_1394
YC13 22PF/25V
YC14 22PF/25V
YX1 24.576Mhz +/-30ppm/18PF
YC15 0.01UF/16V
YC16 0.01UF/16V
1394_FILO
1394_REXT
1394_VREF
YR6 10KOhm 1%
XI
XO
FIL0
REXT
VREF
RSV
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
AS CLOSE AS POSSIBLE TO R5C841
TPBIAS0
YC11 0.01UF/16V
YC12 0.01UF/16V
YRN1A 56Ohm
YRN1B 56Ohm
TPBN0
TPBP0
TPAN0
TPAP0
YRN1C 56Ohm
YRN1D 56Ohm
YC17 270PF/50V
YR1 5.1KOhm 1%
1394_TPB0- <47>
1394_TPB0+ <47>
1394_TPA0- <47>
1394_TPA0+ <47>
Circuit area : As small as possible.
MDIO17 XDCDAT7 <47>
MDIO16 XDCDAT6 <47>
MDIO15 XDCDAT5 <47>
MDIO14 XDCDAT4 <47>
MDIO13 SD/MS_DAT3 <47>
MDIO12 SD/MS_DAT2 <47>
MDIO11 SD/MS_DAT1 <47>
MDIO10 SD/MS_DAT0 <47>
MDIO05 XDWP# <47>
MDIO08 SDCMD_MSBS <47>
MDIO19 XDALE <47>
MDIO18 XDCLE <47>
MDIO02 XDCE# <47>
MDIO03 SDWP# <47>
MDIO00 SDCD# <47>
MDIO01 MSCD# <47>
MDIO09 SD/MSCLK <47>
MDIO04 SD/MS_PWR <47>
MDIO06
MDIO07
YR2 33Ohm 1%
YT1
CB_GBRST# : 1ms < T < 100ms
YR3 100KOhm
YC19 0.1UF/16V
1394 EEPROM
YU2
AT24C02N /X
YC20 0.1UF/16V /X
HW Strapping
XD_EN
1394_SCL
1394_SDA
MS_EN
YRN2B 10KOhm
YRN2A 10KOhm
YRN2C 10KOhm
YRN2D 10KOhm
YR4 10KOhm
YR9 10KOhm
YR5 10KOhm /X
R1.1
Use EEPROM
<Variant Name>
Title : CARD1394-R5C832(1)
ASUSTek Computer Inc.
Engineer: Chad Lai
Size Custom
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 45 of 65

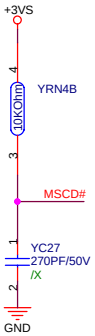

STRAPPING TP_SPI (GPXOA00)
TP_SPI: SPI flash mode
0: select SPI flash mode (need external pull-low)
1: select ISA flash mode (Power-On Default)
Battery
Thermal Sensor
fo CPU & MXM
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
modify for 2.0G 05/19
PT809(I) -- 61 page
PT808(V)--61page
FOR RS232 DEBUG
SPI Flash ROM
MU4
SST25VF080B
12G17100006F
SPI_J2
12G170000038
12G171010104
R2.0G
R1.0G
R1.1G
SEN_TOP
SEN_LEFT
RF_SW
KB3925QFA0
Title : EC ENE3925
Engineer: Tony Kao
ASUSTek Computer Inc.
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 46 of 65



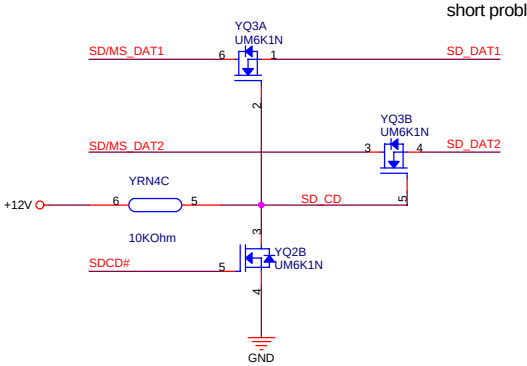








Solve MS Duo Adaptor short problem



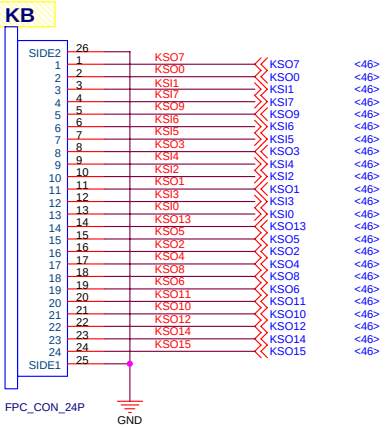
<variant_name>

ASUSTek Computer Inc.	Title : 1394 CON	
	Engineer: Chad Lai	
Size: A3	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 47 of 65	

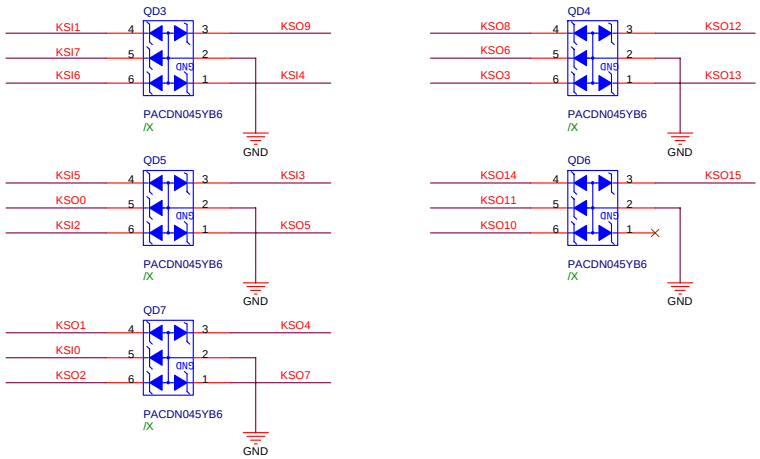
ISA ROM

Keyboard Connector

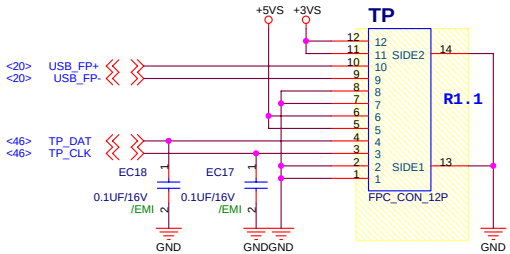
R1.0G



FOR EMI/ESD



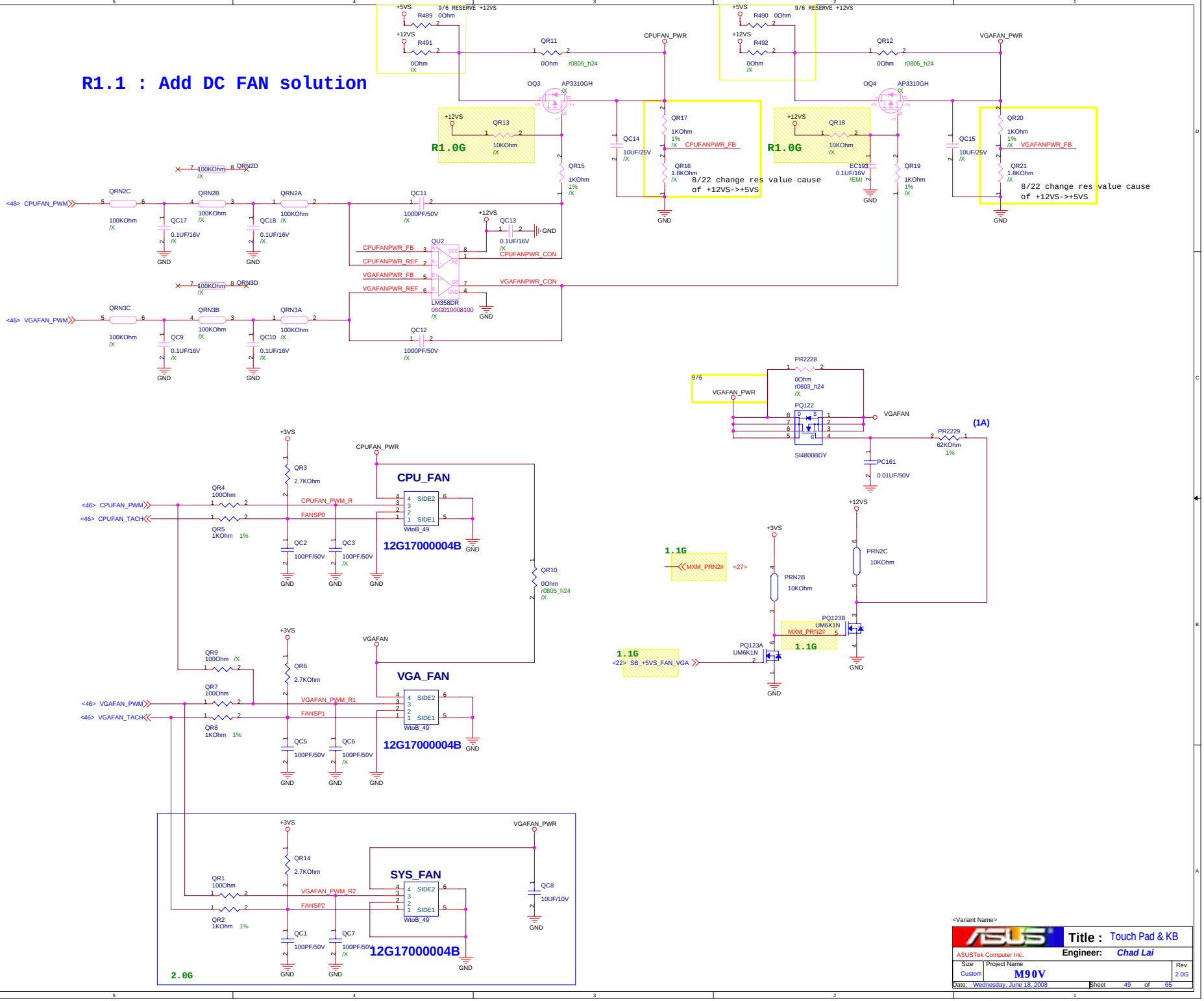
Fingerprint & TouchPad Connector



<Variant Name>

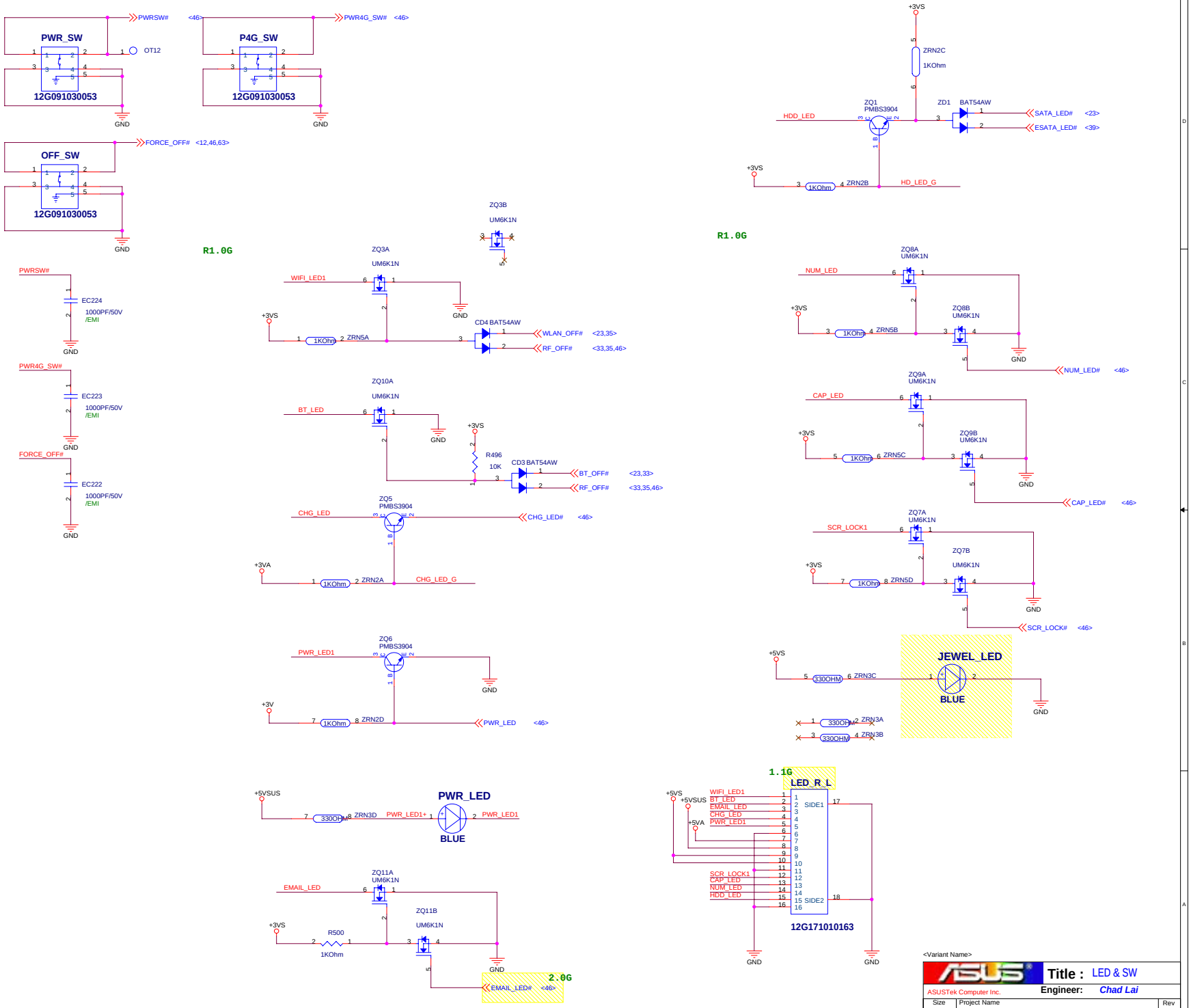
ASUSTek Computer Inc.	Title : ISA FLASH ROM	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 48 of 65	

R1.1 : Add DC FAN solution



<Variant Name>

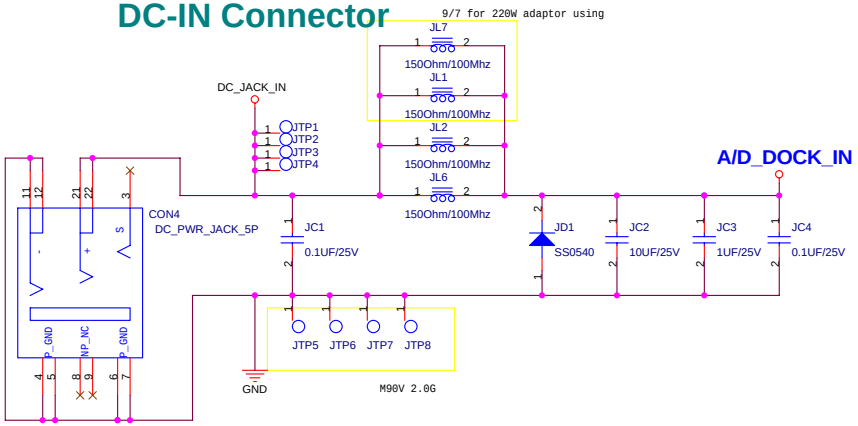
ASUSTek Computer Inc.	Title : Touch Pad & KB	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 49 of 65	



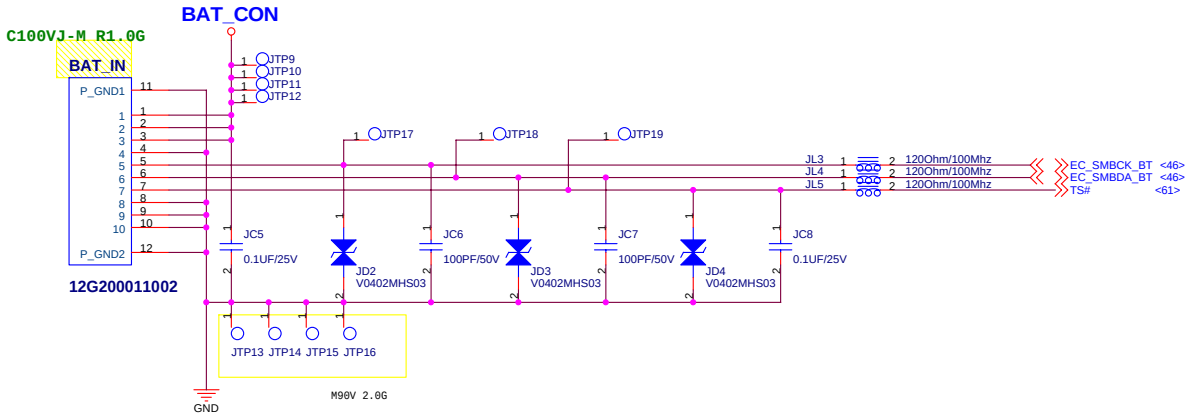
<Variant Name>

ASUSTek Computer Inc.	Title : LED & SW	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 50 of 65	

DC-IN Connector

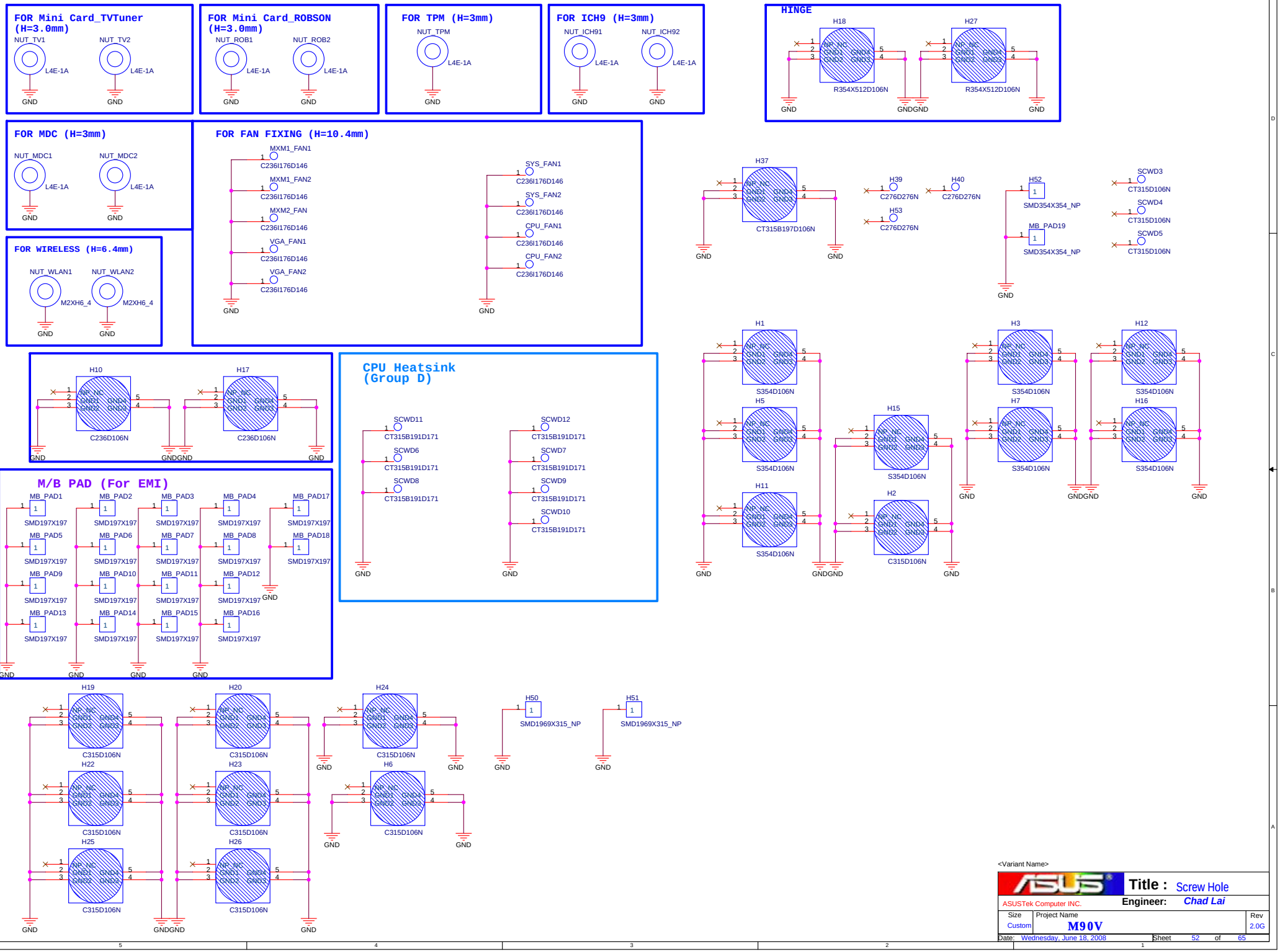


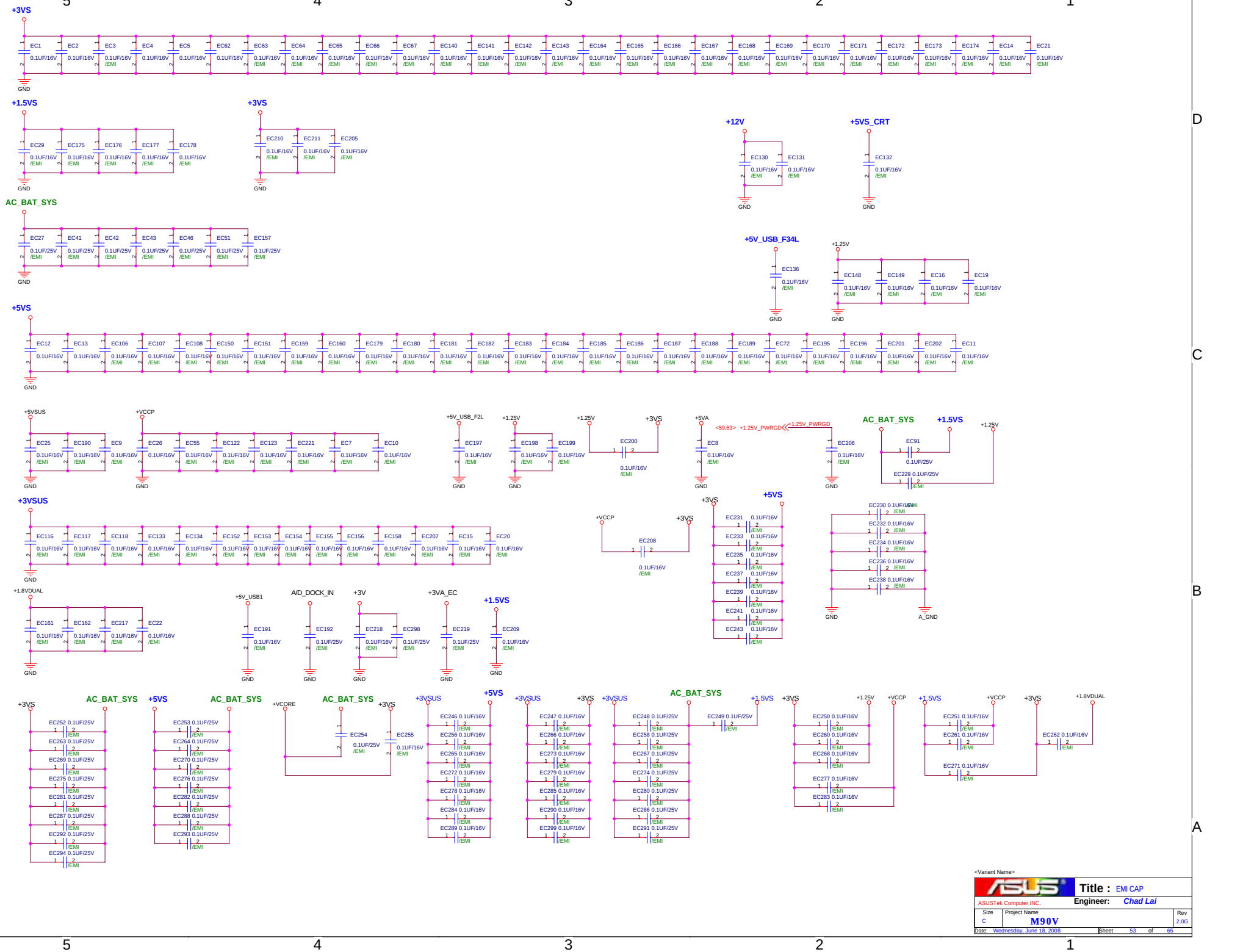
BAT-IN Connector



<Variant Name>

ASUSTek Computer INC.	Title : DC IN & BAT IN	
	Engineer: Chad Lai	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 51 of 65	


FOR Mini Card_TVTuner (H=3.0mm)
NUT_TV1
NUT_TV2
L4E-1A
GND
FOR Mini Card_ROBSON (H=3.0mm)
NUT_ROB1
NUT_ROB2
FOR TPM (H=3mm)
NUT_TPM
FOR ICH9 (H=3mm)
NUT_ICH91
NUT_ICH92
HINGE
H18
H27
R354X512D106N
FOR MDC (H=3mm)
NUT_MDC1
NUT_MDC2
FOR FAN FIXING (H=10.4mm)
MXM1_FAN1
MXM1_FAN2
MXM2_FAN
VGA_FAN1
VGA_FAN2
SYS_FAN1
SYS_FAN2
CPU_FAN1
CPU_FAN2
C236I176D146
FOR WIRELESS (H=6.4mm)
NUT_WLAN1
NUT_WLAN2
M2XH6_4
H37
CT315B197D106N
H39
H40
H53
C276D276N
H52
SMD354X354_NP
MB_PAD19
SCWD3
SCWD4
SCWD5
CT315D106N
H10
H17
C236D106N
H1
H3
H12
H5
H7
H16
H11
H15
H2
S354D106N
C315D106N
CPU Heatsink (Group D)
SCWD11
SCWD6
SCWD8
SCWD12
SCWD7
SCWD9
SCWD10
CT315B191D171
M/B PAD (For EMI)
MB_PAD1
MB_PAD2
MB_PAD3
MB_PAD4
MB_PAD17
MB_PAD5
MB_PAD6
MB_PAD7
MB_PAD8
MB_PAD18
MB_PAD9
MB_PAD10
MB_PAD11
MB_PAD12
MB_PAD13
MB_PAD14
MB_PAD15
MB_PAD16
SMD197X197
H19
H20
H24
H22
H23
H6
H25
H26
H50
H51
SMD1969X315_NP
GND
<Variant Name>
Title : Screw Hole
ASUSTek Computer INC.
Engineer: Chad Lai
Size Custom
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 52 of 65



<variant_name>

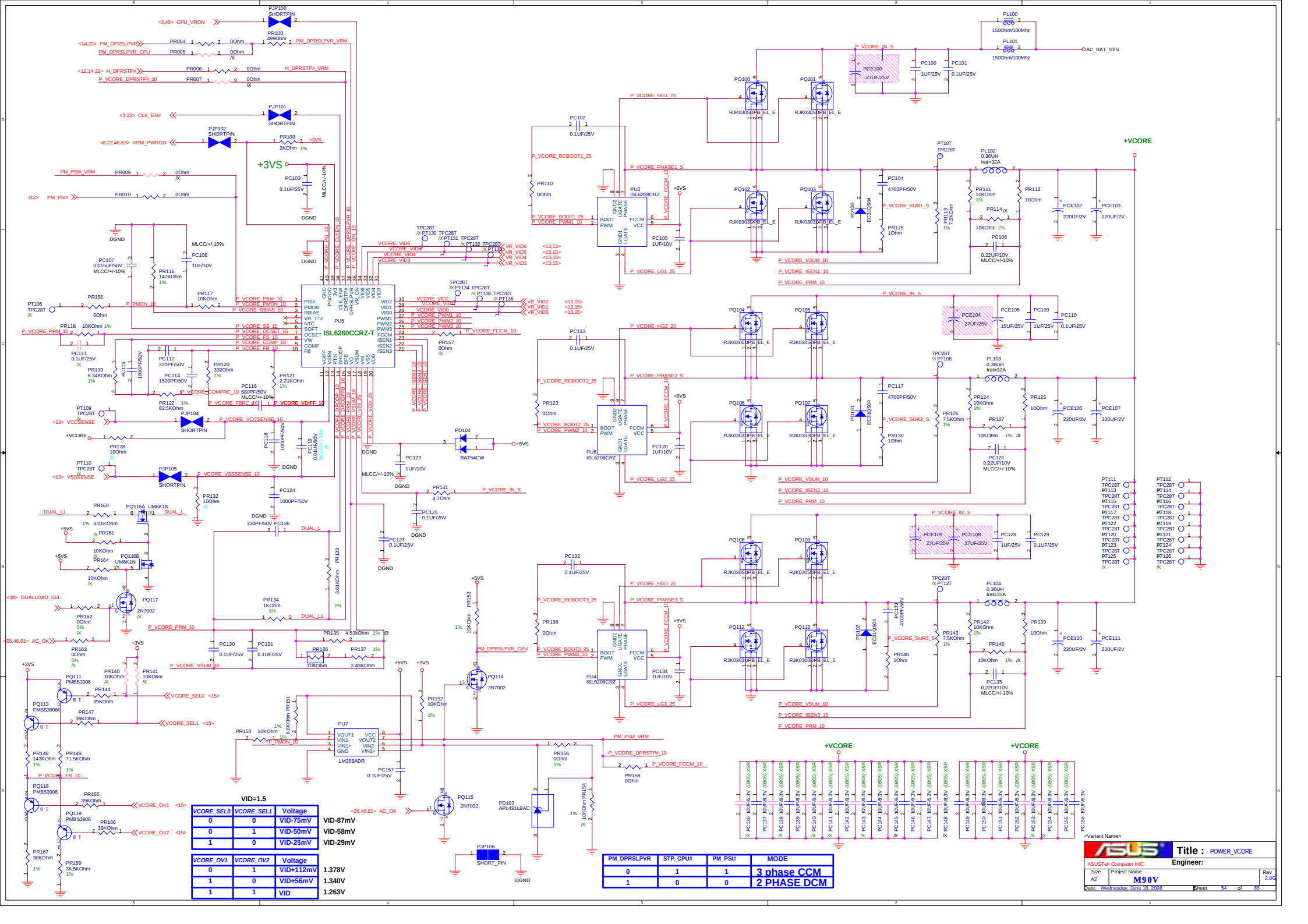
ASUSTek Computer INC.

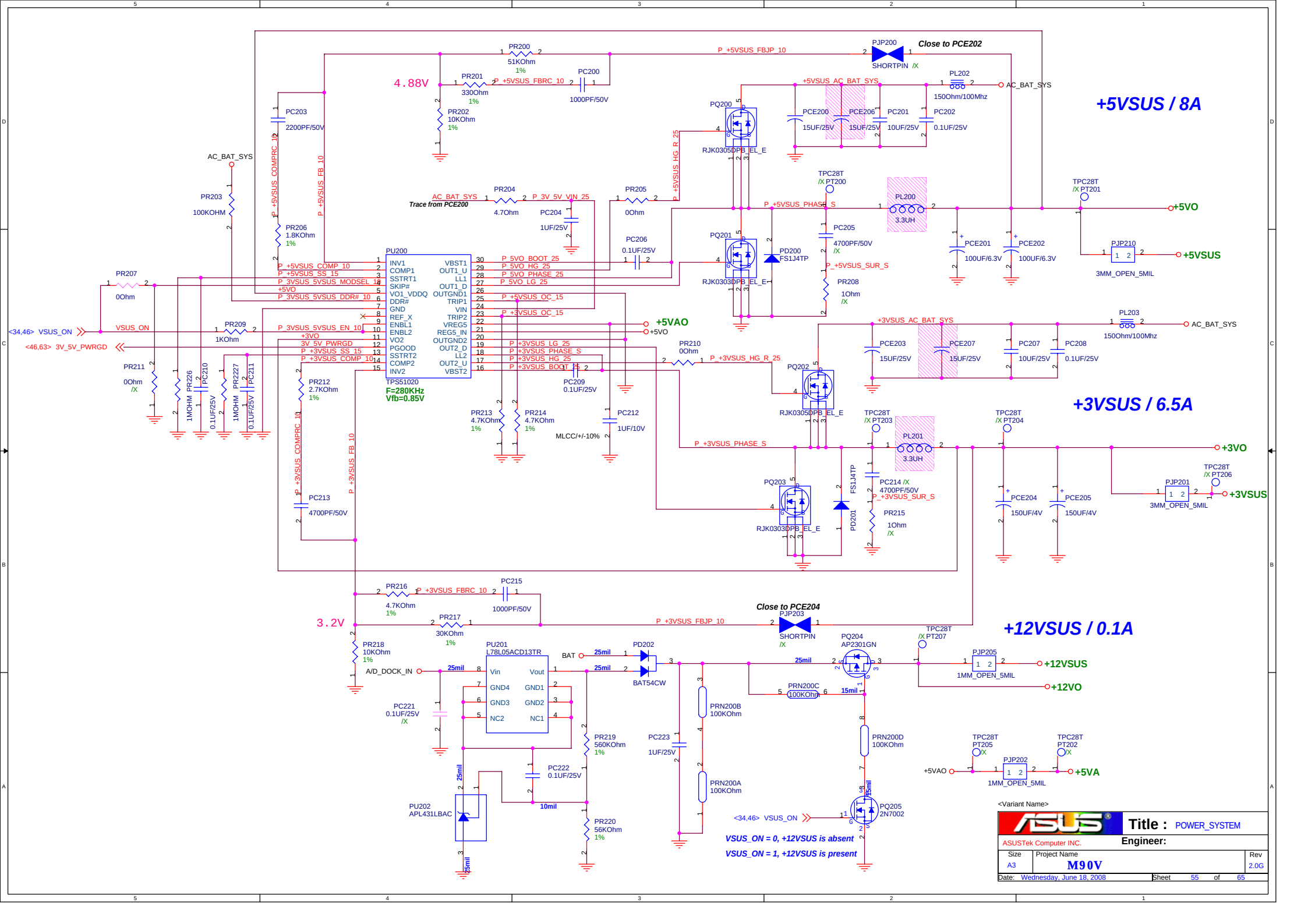
Title : EMI CAP

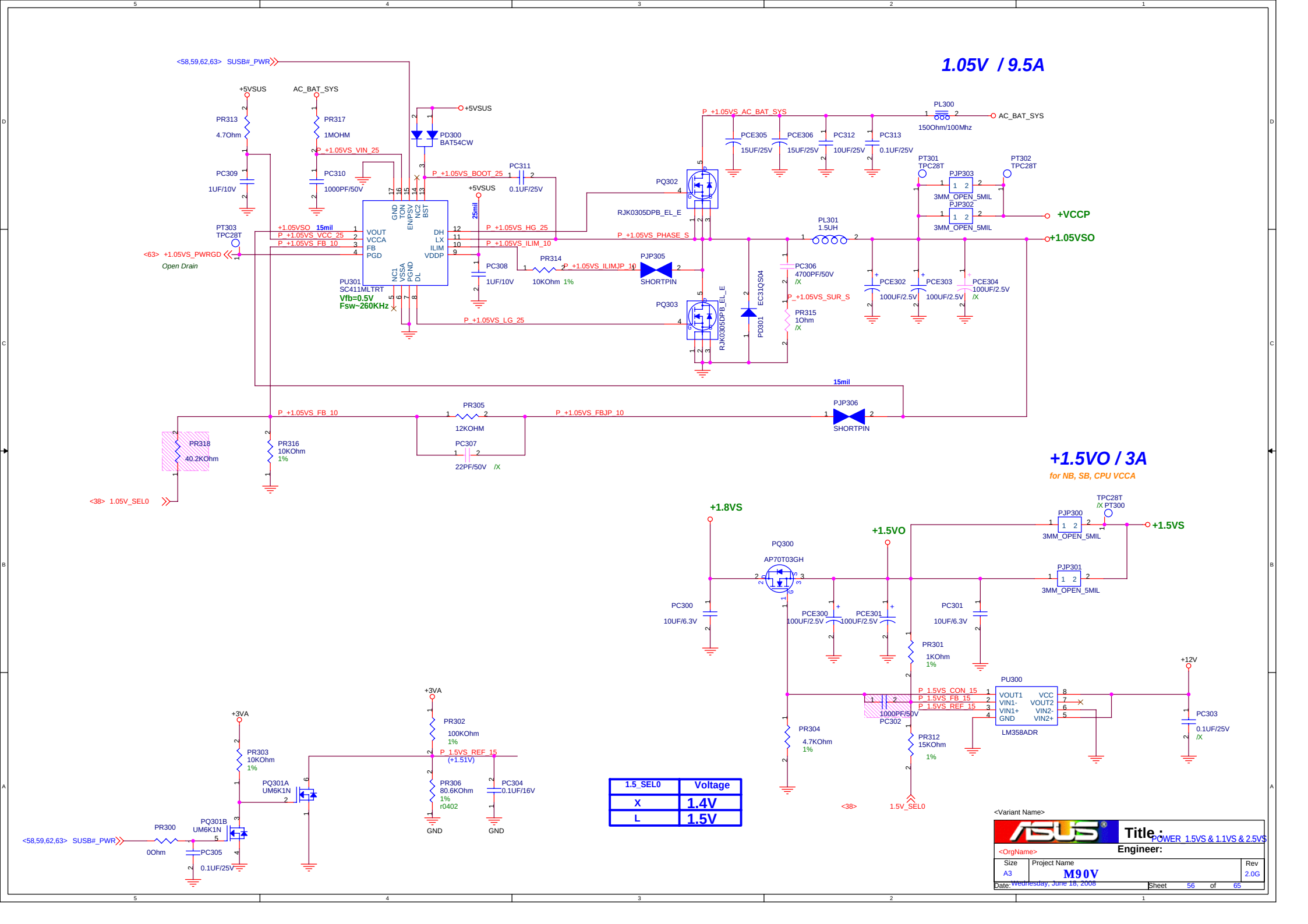
Engineer: Chad Lai

Size	Project Name	Rev
C	M90V	2.0G

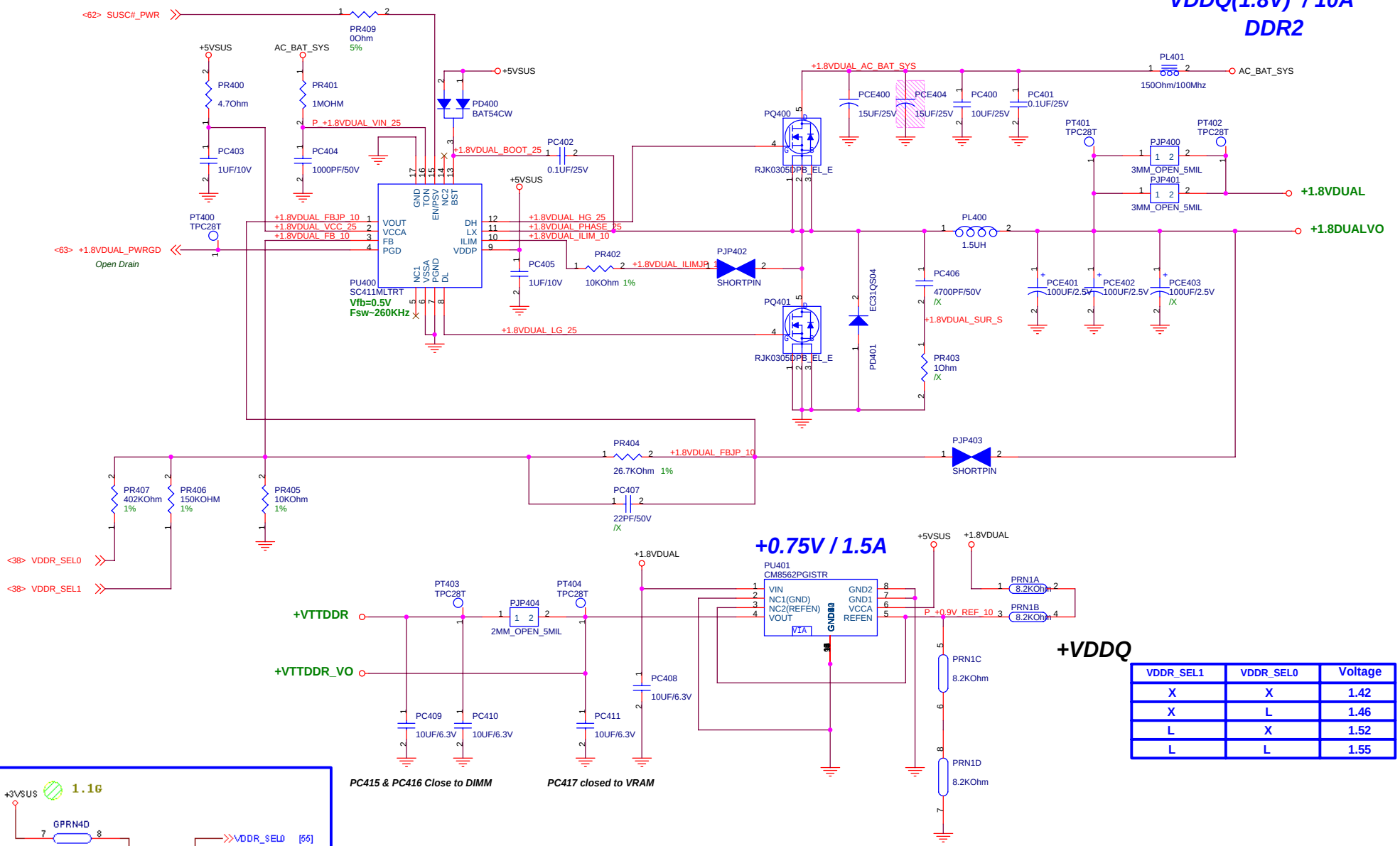
Date: Wednesday, June 18, 2008 Sheet 53 of 65


ISL6260CCRZ-T
PU5
PU3 ISL6208CRZ
PU4 ISL6208CRZ
PU6 ISL6208CRZ
PU7
LM358ADR
+VCORE
+3VS
+5VS
DGND
AC_BAT_SYS
VID=1.5
VCORE_SEL0 VCORE_SEL1 Voltage
0 0 VID-75mV
0 1 VID-50mV
1 0 VID-25mV
1 1 VID
VID-87mV
VID-58mV
VID-29mV
VCORE_OV1 VCORE_OV2 Voltage
0 1 VID+112mV 1.378V
1 0 VID+56mV 1.340V
1 1 VID 1.263V
PM_DPRSLPVR STP_CPU# PM_PSI# MODE
0 1 1 3 phase CCM
1 0 0 2 PHASE DCM
Title : POWER_VCORE
ASUSTek Computer INC.
Engineer:
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 54 of 65

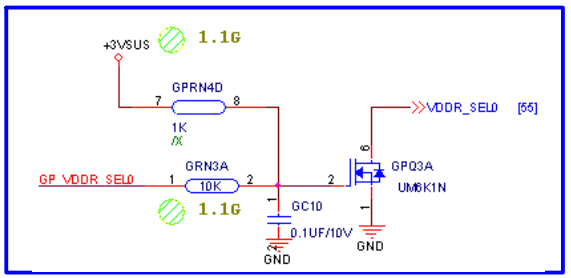

+5VSUS / 8A
+3VSUS / 6.5A
+12VSUS / 0.1A
4.88V
3.2V
PU200
TPS51020
F=280KHz
Vfb=0.85V
PU201
L78L05ACD13TR
PU202
APL431LBAC
PJP200
SHORTPIN /X
Close to PCE202
PJP203
Close to PCE204
PQ200
PQ201
PQ202
PQ203
PQ204
AP2301GN
PQ205
2N7002
RJK0305DPB_EL_E
RJK0303DPB_EL_E
PD200
FS1J4TP
PD201
PD202
BAT54CW
AC_BAT_SYS
+5VSUS_AC_BAT_SYS
+3VSUS_AC_BAT_SYS
+5VO
+5VSUS
+3VO
+3VSUS
+12VSUS
+12VO
+5VA
+5VAO
+5VO
VSUS_ON
3V_5V_PWRGD
A/D_DOCK_IN
BAT
Trace from PCE200
VSUS_ON = 0, +12VSUS is absent
VSUS_ON = 1, +12VSUS is present
<Variant Name>
Title : POWER_SYSTEM
ASUSTek Computer INC.
Engineer:
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 55 of 65


1.05V / 9.5A
<58,59,62,63> SUSB#_PWR
+5VSUS
AC_BAT_SYS
PR313 4.7Ohm
PR317 1MOHM
P_+1.05VS_VIN_25
PC309 1UF/10V
PC310 1000PF/50V
PD300 BAT54CW
P_+1.05VS_BOOT_25
PC311 0.1UF/25V
PT303 TPC28T
+1.05VSO 15mil
P_+1.05VS_VCC_25
P_+1.05VS_FB_10
<63> +1.05VS_PWRGD
Open Drain
PU301 SC411MLTRT
Vfb=0.5V
Fsw~260KHz
VOUT VCCA FB PGD VDDP ILIM LX DH NCL VSSA PGND DL EN/PSV TON GND NC2 BST
25mil
P_+1.05VS_HG_25
P_+1.05VS_ILIM_10
P_+1.05VS_LG_25
PC308 1UF/10V
PR314 10KOhm 1%
P_+1.05VS_ILIMJP_10
PJP305 SHORTPIN
PQ302 RJK0305DPB_EL_E
PQ303 RJK0305DPB_EL_E
P_+1.05VS_AC_BAT_SYS
PCE305 15UF/25V
PCE306 15UF/25V
PC312 10UF/25V
PC313 0.1UF/25V
PL300 150Ohm/100Mhz
PT301 TPC28T
PT302 TPC28T
PJP303 3MM_OPEN_5MIL
PJP302 3MM_OPEN_5MIL
+VCCP
PL301 1.5UH
+1.05VSO
P_+1.05VS_PHASE_S
PC306 4700PF/50V /X
P_+1.05VS_SUR_S
PR315 1Ohm /X
PD301 EC31QS04
PCE302 100UF/2.5V
PCE303 100UF/2.5V
PCE304 100UF/2.5V /X
15mil
PJP306 SHORTPIN
P_+1.05VS_FB_10
PR305 12KOHM
P_+1.05VS_FBJP_10
PR318 40.2KOhm
PR316 10KOhm 1%
PC307 22PF/50V /X
<38> 1.05V_SEL0
+1.5VO / 3A
for NB, SB, CPU VCCA
+1.8VS
PQ300 AP70T03GH
PC300 10UF/6.3V
PCE300 100UF/2.5V
PCE301 100UF/2.5V
PC301 10UF/6.3V
PR301 1KOhm 1%
TPC28T /X PT300
PJP300 3MM_OPEN_5MIL
+1.5VS
PJP301 3MM_OPEN_5MIL
PU300 LM358ADR
VOUT1 VIN1- VIN1+ GND VCC VOUT2 VIN2- VIN2+
P_1.5VS_CON_15
P_1.5VS_FB_15
P_1.5VS_REF_15
PC302 1000PF/50V
PR304 4.7KOhm 1%
PR312 15KOhm 1%
+12V
PC303 0.1UF/25V /X
<38> 1.5V_SEL0
+3VA
PR303 10KOhm 1%
PQ301A UM6K1N
PQ301B UM6K1N
PR300 0Ohm
<58,59,62,63> SUSB#_PWR
PC305 0.1UF/25V
PR302 100KOhm 1%
P_1.5VS_REF_15 (+1.51V)
PR306 80.6KOhm 1% r0402
PC304 0.1UF/16V
GND
1.5_SEL0 | Voltage
X | 1.4V
L | 1.5V
<Variant Name>
Title : POWER 1.5VS & 1.1VS & 2.5VS
<OrgName>
Engineer:
Size A3
Project Name M90V
Rev 2.0G
Date: Wednesday, June 18, 2008
Sheet 56 of 65

VDDQ(1.8V) / 10A
DDR2



VDDR_SEL1	VDDR_SEL0	Voltage
X	X	1.42
X	L	1.46
L	X	1.52
L	L	1.55



CHECK RC DELAY FOR EC(OV PIN)

<Variant Name>

ASUS

Title :

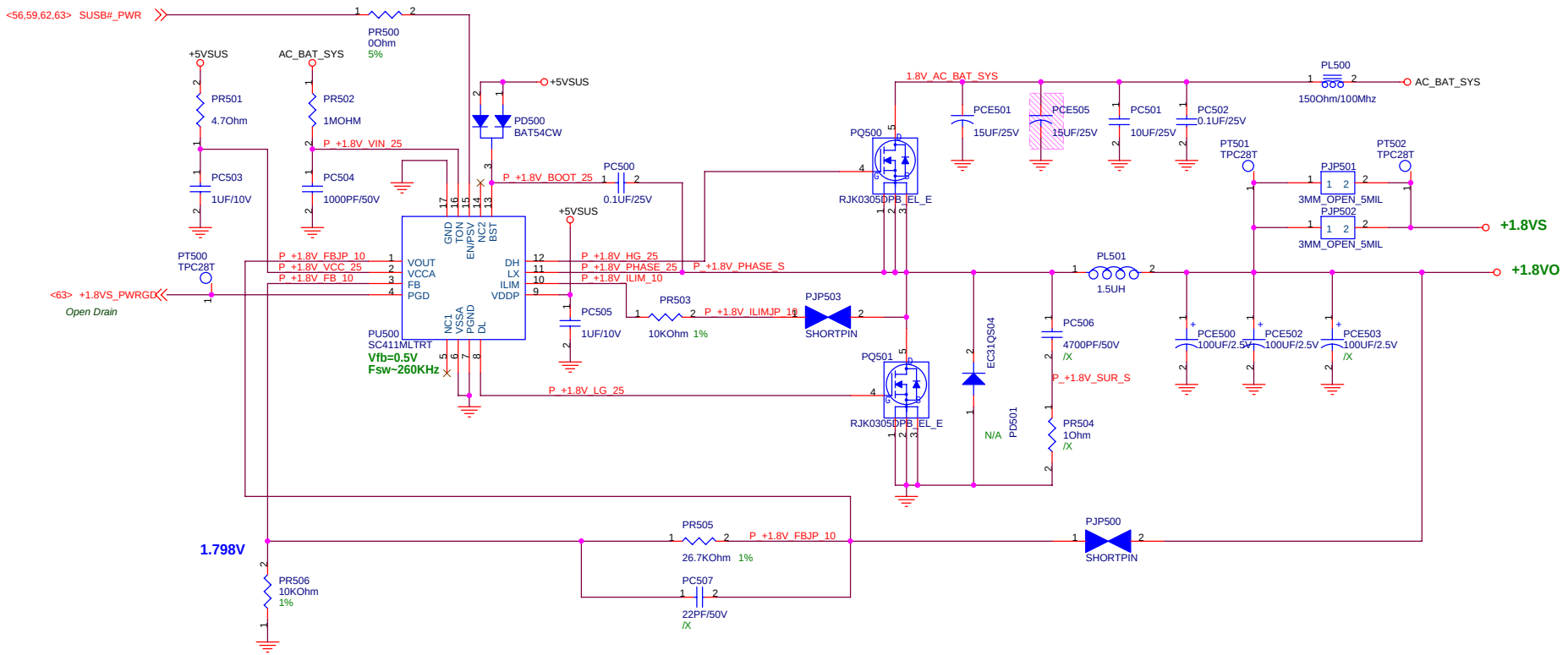
<OrgName>

Engineer:

Size	Project Name	Rev
A3		2.0G

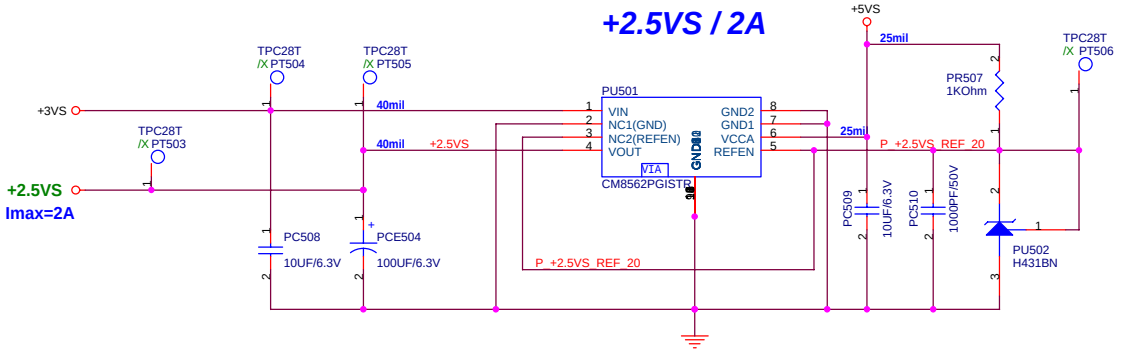
Date: Wednesday, June 18, 2008 Sheet 57 of 65

MXM / 6A



MXM

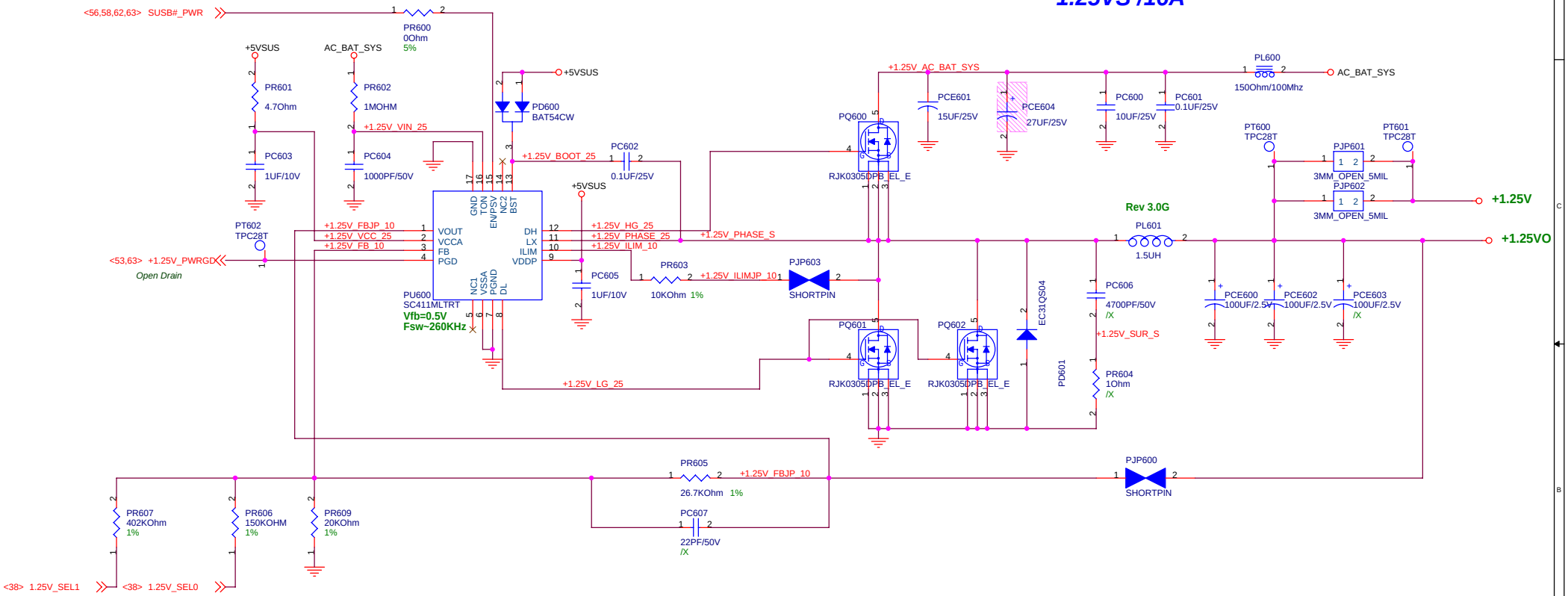
+2.5VS / 2A



<Variant Name>

Title :	
<OrgName>	Engineer:
Size: A3	Project Name
Rev: 2.0G	
Date: Wednesday, June 18, 2008	Sheet 58 of 65

1.25VS /16A

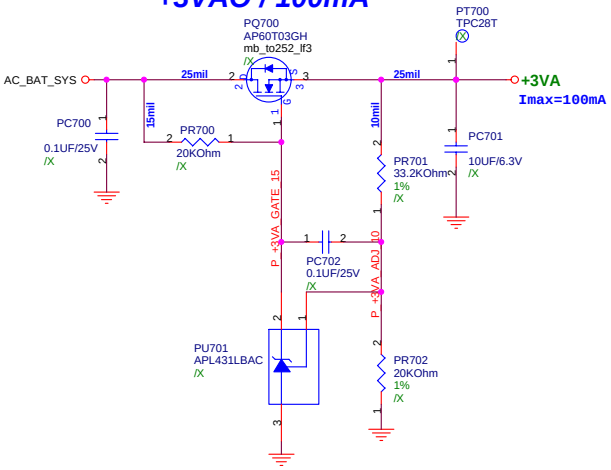


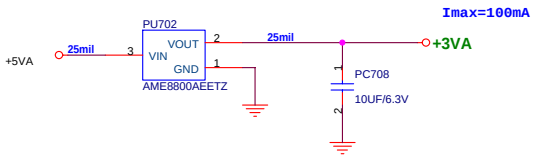
1.25V_SEL1	1.25V_SEL0	Voltage
X	X	1.14
X	L	1.17
L	X	1.23
L	L	1.263

<Variant Name>

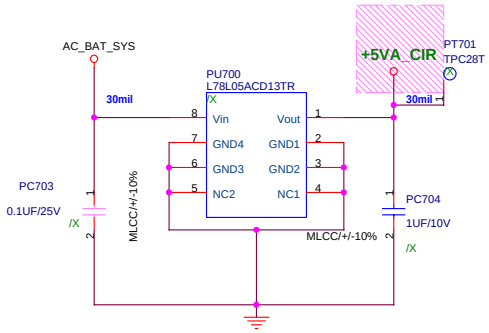
ASUS	Title :	
<OrgName>	Engineer:	
Size: A3	Project Name	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 59 of 65	

+3VAO / 100mA





For CIR Power



<Variant Name>

Title : POWER_I/O_+3VA & +2.5V

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
Custom	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 60 of 65

Setting the Adapter Input Current Limit

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 3.30V

Adaptor Max. Current :

PR805=20K PR812 = 71.5K; Ilimit = 11.72A; 220W

PR805=20K PR812 = 178K; Ilimit = 4.5A; 81W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }

VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

Victl = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Victl = 2.084V

=> Icharge = 1.6933A

BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V

=> Icharge = 2.9329A

PR806=120K PR813 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

BATSEL= 1, 2600(2400) mAH

BATSEL= 0, 2800 mAH

BATSEL_2P# = 1, 3 Cells

BATSEL_2P# = 0, 6 or 9 Cells

PRECHG = 1, Pre-Charging Mode

Charging Current = 156mA

CHG_EN# = 1, Charger Disabled

CHG_EN# = 0, Charger Enabled

AC_OK = 1, Adaptor is present

AC_OK = 0, Adaptor is absent

BAT_LEARN = 1, Battery discharges

BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

For EC monitor Adapter

TS# = 1; Battery absence

TS# = 0; Battery Plug-in

BAT_IN_OC# = 1; Battery absence

BAT_IN_OC# = 0; Battery Plug-in

<Variant Name>

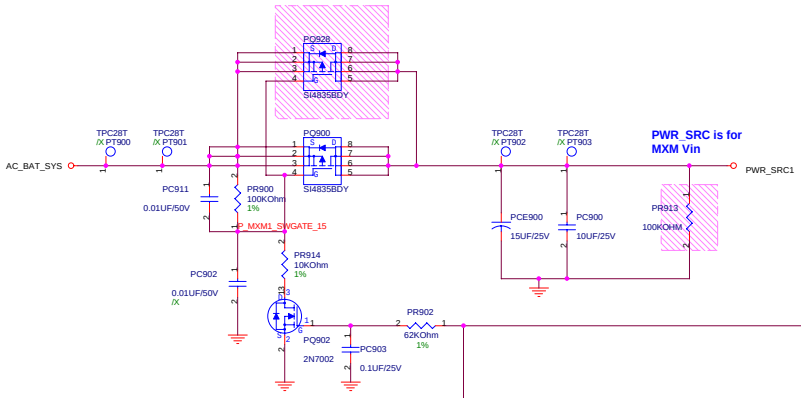
Title : POWER_CHARGER

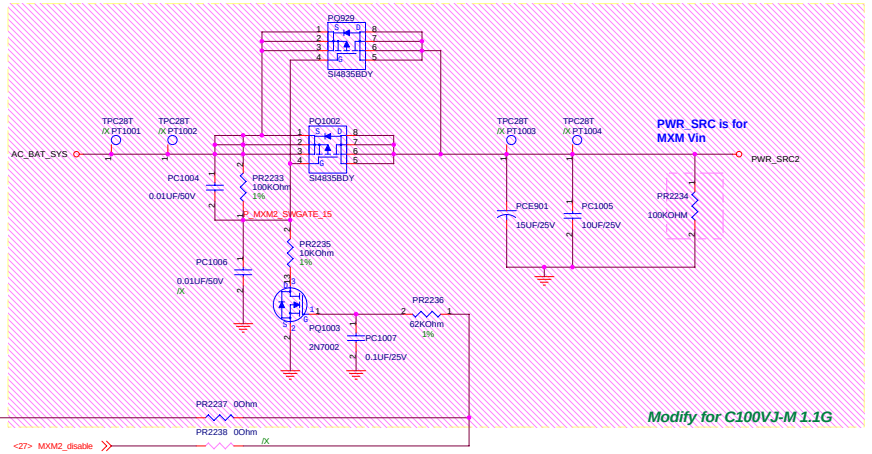
ASUSTek Computer INC. Engineer:

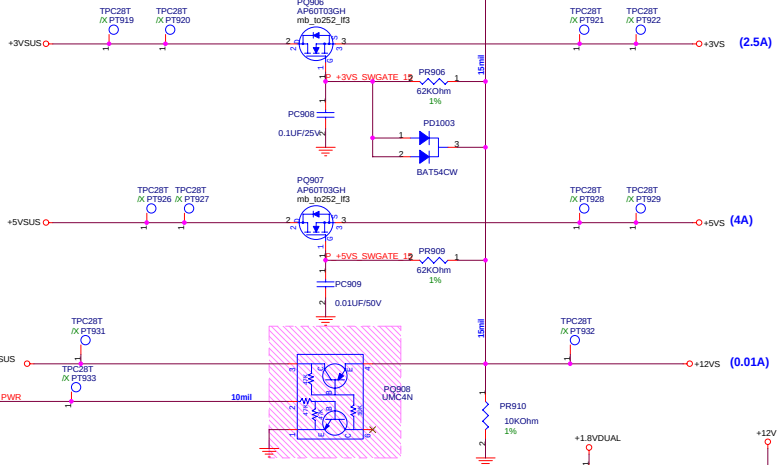
Size: C | Project Name: M90V | Rev: 2.0G

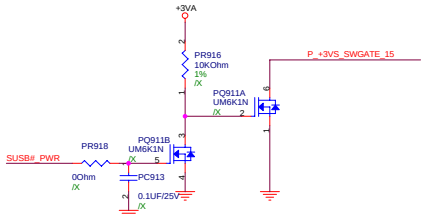
Date: Wednesday, June 18, 2008 | Sheet 61 of 65

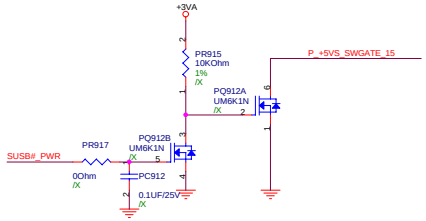
SUSB#_PWR POWER



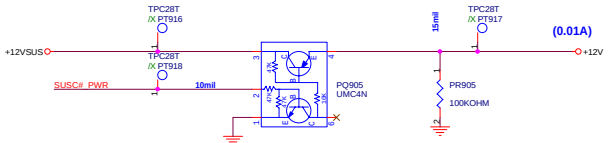


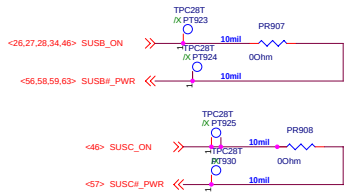


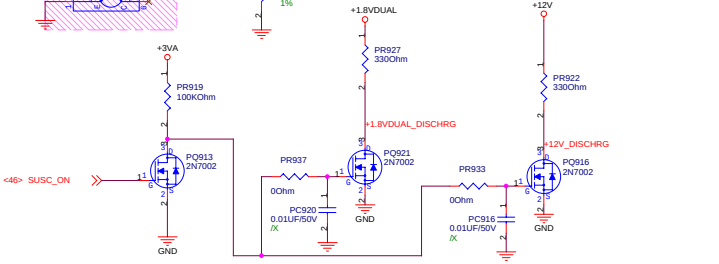


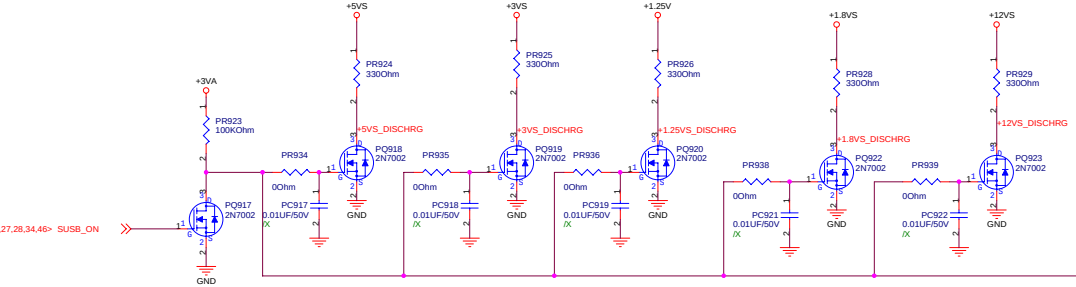


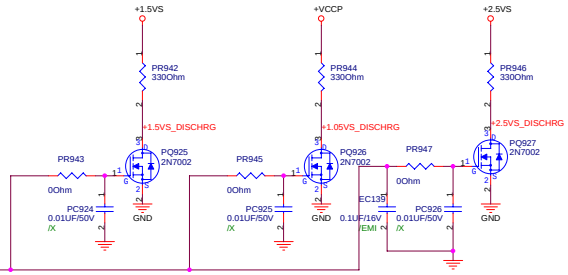
SUSC#_PWR POWER











<Variant Name>

Title : POWER_LOAD SWITCH

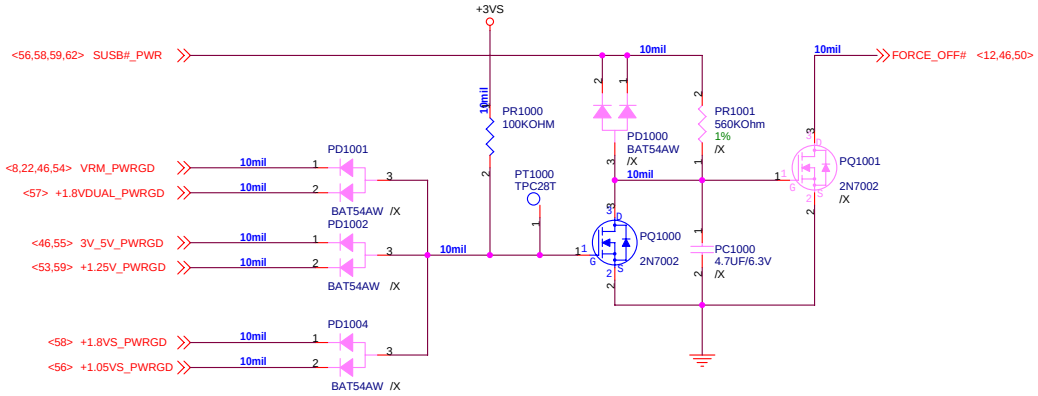
ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
A2	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 62 of 65

Power Good Detecter



<Variant Name>

ASUSTek Computer INC.	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: M90V	Rev: 2.0G
Date: Wednesday, June 18, 2008	Sheet 63 of 65	

8/10
1. Change new power circuit from P53 to P62
2. Use single ESATA to replace the combination of ESATA
and USB port (P38)
3. Add button, inverter and camera boards (P32)

8/13
1. Add Robson function (P37)
2. Remove LED (P50)
3. Because use SATA ODD(audio is digitsal signal), delete
Audio analog single pin (P42)

8/15
1. Change DDR3 SO-Dimm; DIMM1 H4, DIMM2 H8,DIMM3 H12(P16~P18)
2. Add USB port (P32)
3. Change LVDS connector to 17" panel

8/16
1. Change MXM1 and MXM2 connectors to H16 (P25,
P26)

8/20
1. MXM data pin change back to standard (P6, P8)
2. Change DC_IN jack
3. Change DDR3 Dimm3 to H8 temporary

8/21
1. Clock Gen. 3VA reserve (P3)
2. USB change to dual in one
connector (P32)

8/22
1. Add VGA Fan control pin and change Fan voltage from +12VS to +5VS
(P49)
2. Add ESATA voltage ESATA+1.8VS (P39)
3. Add for ESATA+1.8V power (P40)

8/23
1. Change RJ11-45 Conn. (P42)
2. change 1394 Conn. (P48)

8/28
1. Add
control (P14)

8/29
1. Add LC FILTER==>VCCAPLL_EXP and VCCAPLL_EXP2 (P9)
2. VCC_EXT_PLL pin change to +1.25V

9/4
1. Reserve CAP (P10)(P15)(P18)
2. Add couple CAP (P32)
3. Add RC filter (P39)

9/6
1. Reserve GPIO Res for another control method (P39)
2. Change 2N7002 to SI3456BDV for power consumption
3. Add CPU frequency control (P47)
4. Add GPIO for VGA and System fan control (P47)
5. Add detection of MXM present pin (P47)
6. Add wireless lan LED control (P47)
7. modify fan control method and reserve +5V and +12V fan
type

10/31
1. clock GEN change to 928 (P3)
2. change battery hold (P21)
3. Add audio singnal on MDC device (P22)
4. Move SATA ODD to port SATA4 and pull low the interlock switch (P23)
5. Remove S-singal pin on MXM (P26)
6. Change net name from SPDIF_OUT to HDMI_Aout(P26)
7. Modify USB circuit for different side application (P32)
8. Set E-SATA+1.8VS to /X on regulator side (P39)
9. Change ALC883 to ALC888S (P42)
10. Add audio AMP on SURR, Center and Woofer (P43)
11. Modify FAN control on MOSFET switch (P49)

11/1
1. DDR3 change to reverse type

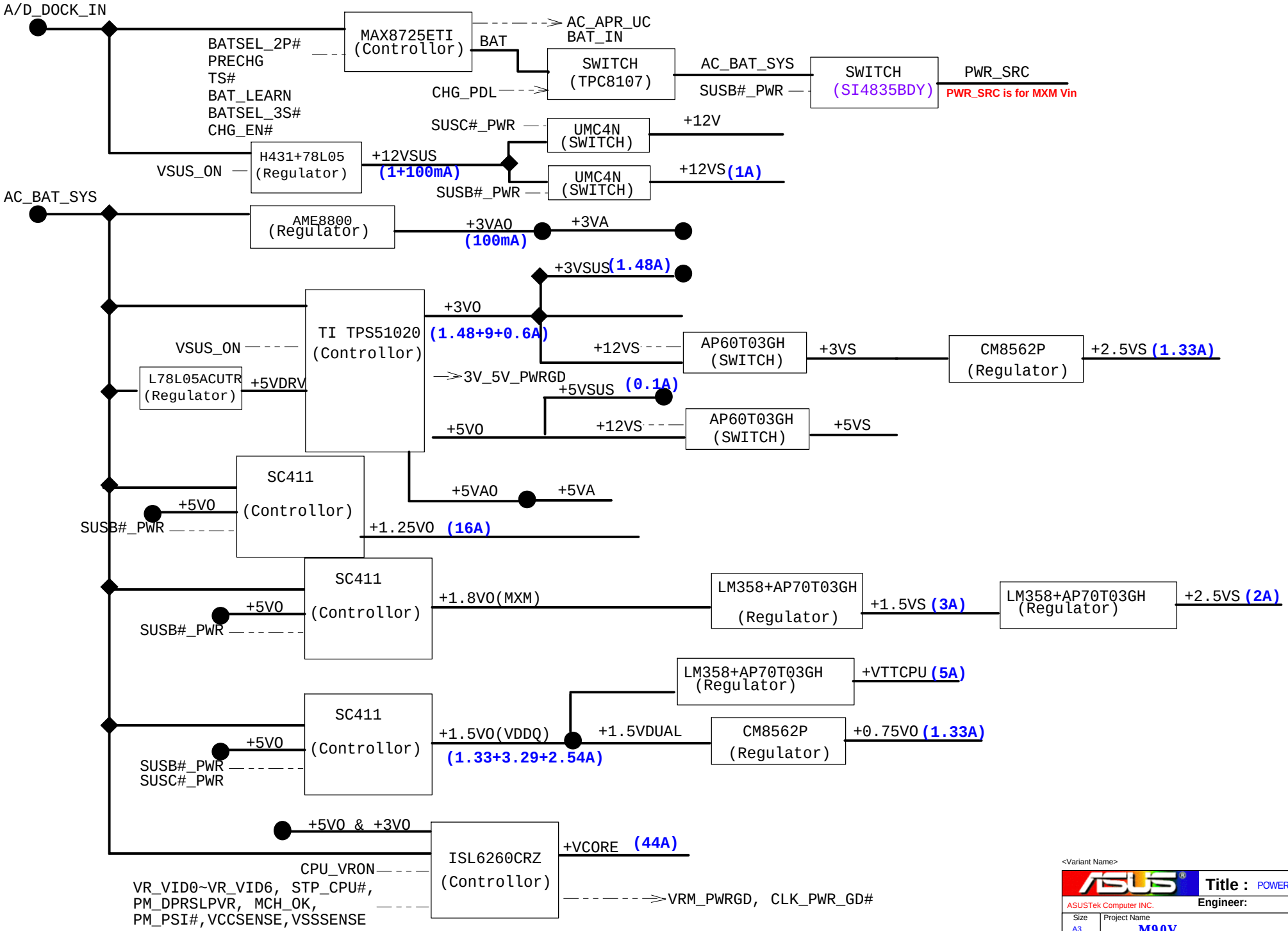
<Variant Name>

Title : Notice

ASUSTek computer INC. Engineer: <OrgAddr1>

Size	Project Name	Rev
	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 64 of 65



<Variant Name>

ASUSTek Computer INC.

Title : POWER_FLOWCHART

Engineer:

Size	Project Name	Rev
A3	M90V	2.0G

Date: Wednesday, June 18, 2008 Sheet 65 of 65