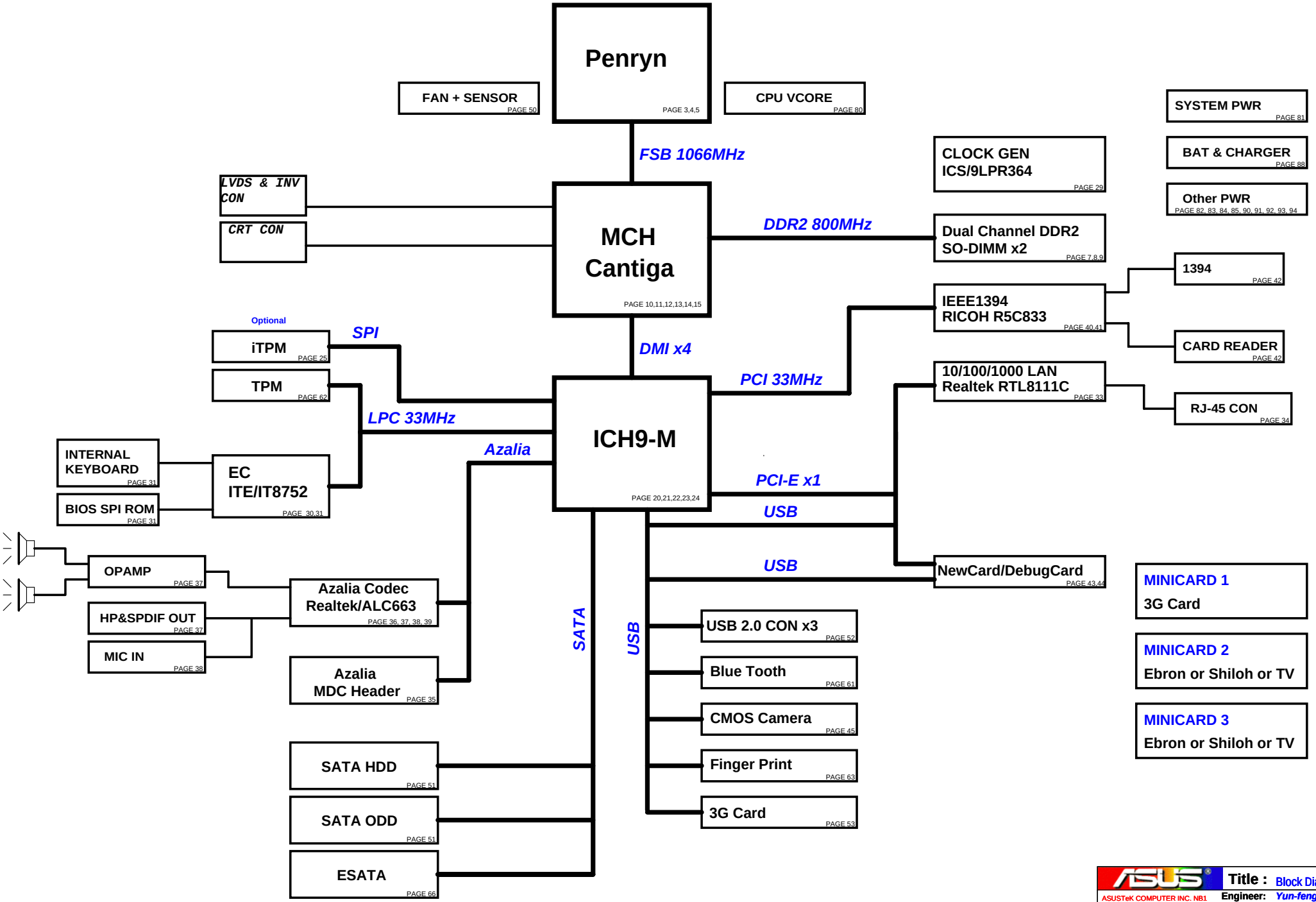
N50A/N51A Montevina Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 1 of 79	

N50A Schematic Index

Page	System page Ref.
01	Block Diagram
02	Schematic Information
03-05	CPU-Penryn
07-09	DDR II SO-DIMM
10-15	Cantiga
20-24	ICH9M
25	SPI ROM
29	CLK-ICS9LPR363CGLF-T
30-31	EC_IT8752
32	POWER-ON SEQUENCE
33	Realtek RTL8111C
34	RJ45 + RJ11
35	MDC
36	ALC663 Codec
37	AUDIO_G1431 & HP
38	MICROPHONE & Array MIC
~~39~~	~~FM2010 DSP~~
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & 4 IN1 CON
43	NewCard PWR SW & CON
44	Debug
45	LVDS & INVERTER CONNECTOR
46	CRT
48	HDMI
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port x 3
53	MINICARD(Ebron/Robson/3G/TV)
~~54~~	~~PORT Docking~~
~~55~~	~~Super I/O & FIR~~
56	LED/TP/SW
57	DISCHARGE
58	UMB
60	DC power jack, Batter conn.
61	Blue Tooth
62	TPM
63	Finger Print
65	MDC NUT & Hinksink NUT
66	E-SATA
68	XDP
70-77	VGA (nVidia NB9P-GE)
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.5V & 1.05VM
83	POWER_I/O_DDR & VTT
84	NONE
85	POWER_VGA_VCORE & 1.1VO
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

GPIO33 Internal Pull High, Go Low= Flash_ _ _
Descriptor Security will be overriden

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]# EXT PU	+5VS
GPIO 06	GPI	- EXT PU	+3VS
GPIO 07	GPI	- EXT PU	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	- INT PD*	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	NEWCARD_OC#	+3VSUS
GPIO 30	Native	USB_OC3467#	+3VSUS
GPIO 31	Native	USB_OC3467#	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3467#	+3VSUS
GPIO 43	Native	USB_OC3467#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	WLAN_ON	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	**+3VS**
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

INT PU*: PU or PD in special time

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	

ASUSTeK COMPUTER INC. NB1

Title : Schematic Information

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Thursday, July 24, 2008 Sheet 2 of 79

12G010059478G

CPU Debug Port

Default Strapping When Not Used

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

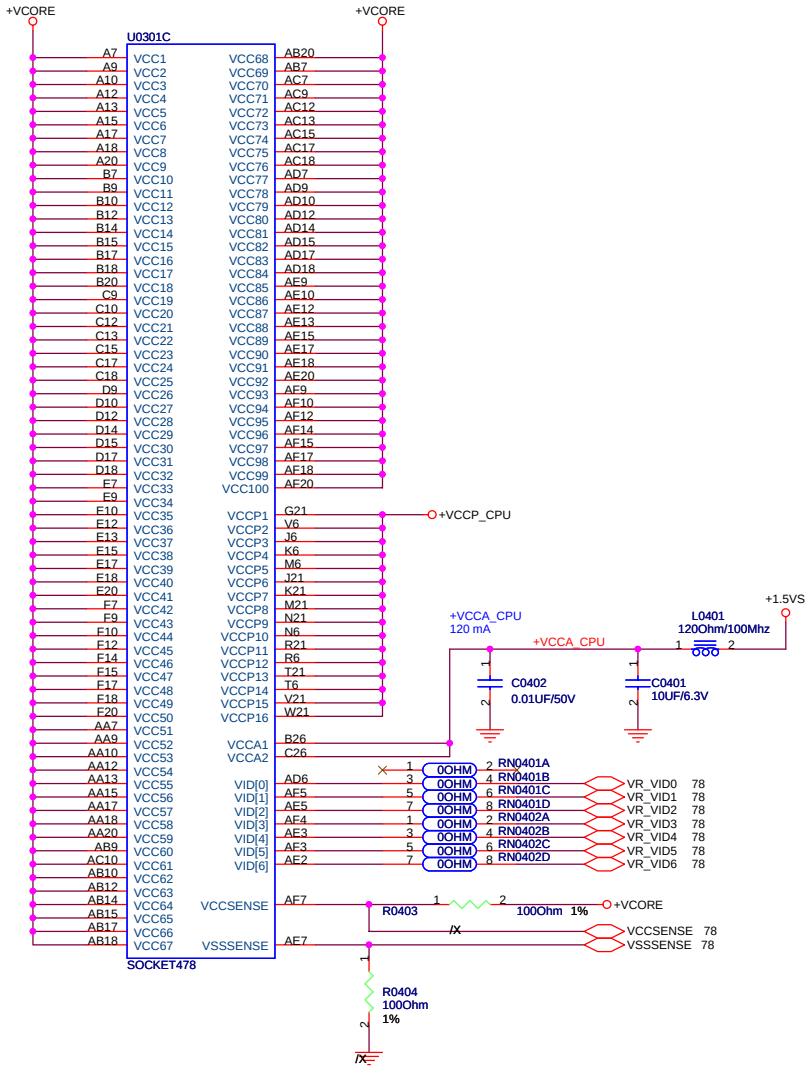
Zo=55 Ohm, 0.5" max for GTL_REF

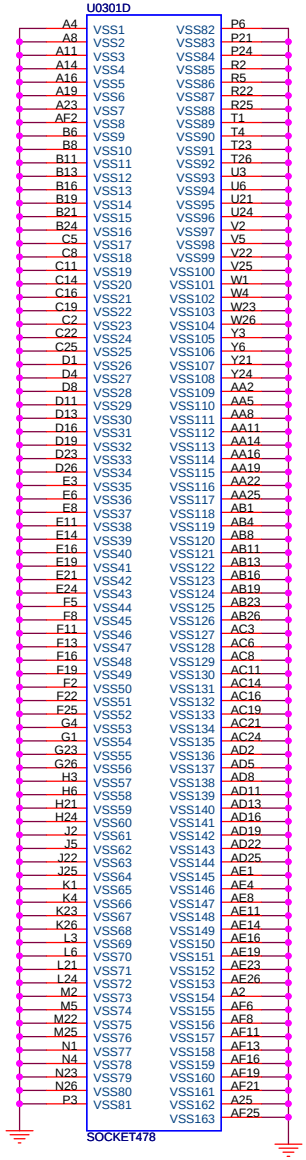
I(ITP_CPURST#) < 0.5"
I(H_CPURST#) < 6.0"

R1.1_(49)

2008-07-16

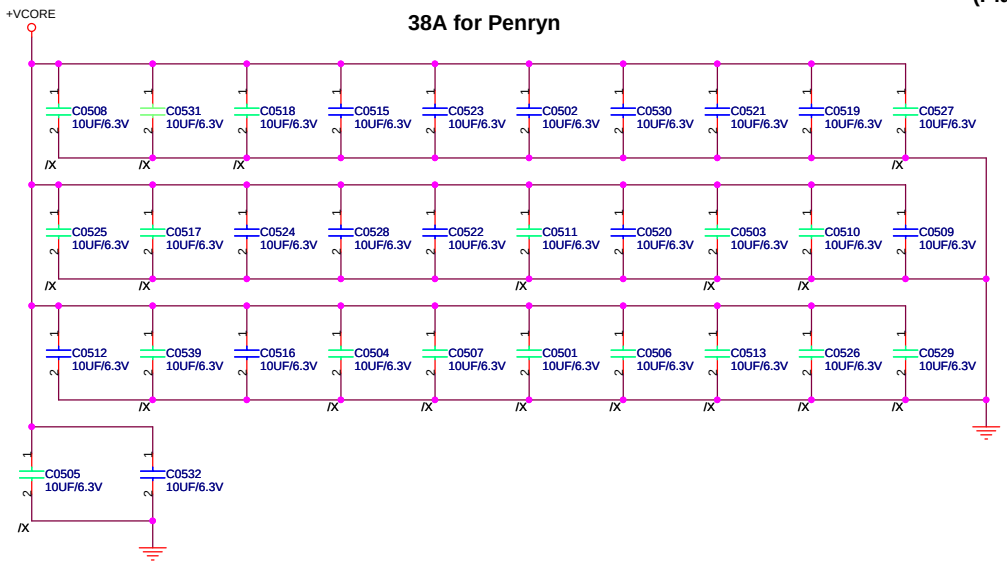
Title :	CPU-Penryn(1)
ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan
Size: Custom	Project Name: N50A/N51A
Rev: 1.0	
Date: Wednesday, August 06, 2008	Sheet 3 of 79





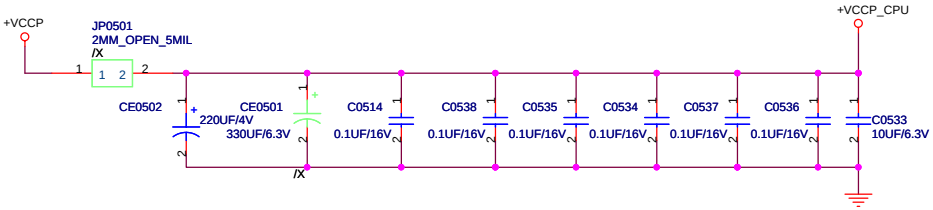
ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn(2)	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 4 of 79	

38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)

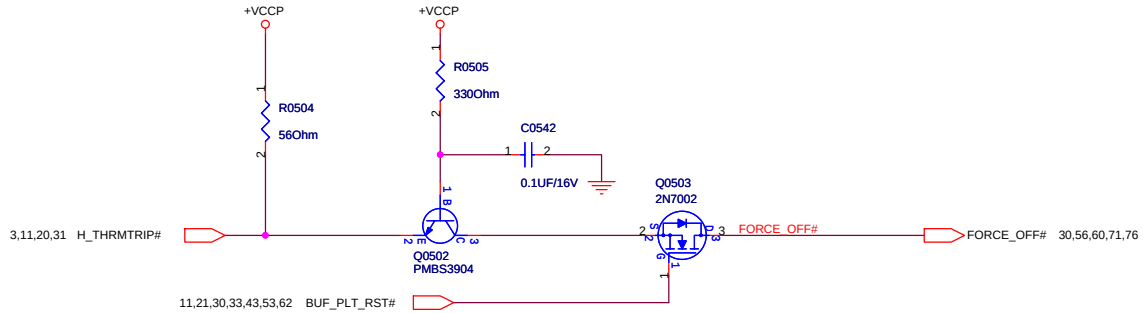
因爲CE0501與ME干涉,CE0501要移遠一點,而預留CE0502在原本CE0501位置



Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?



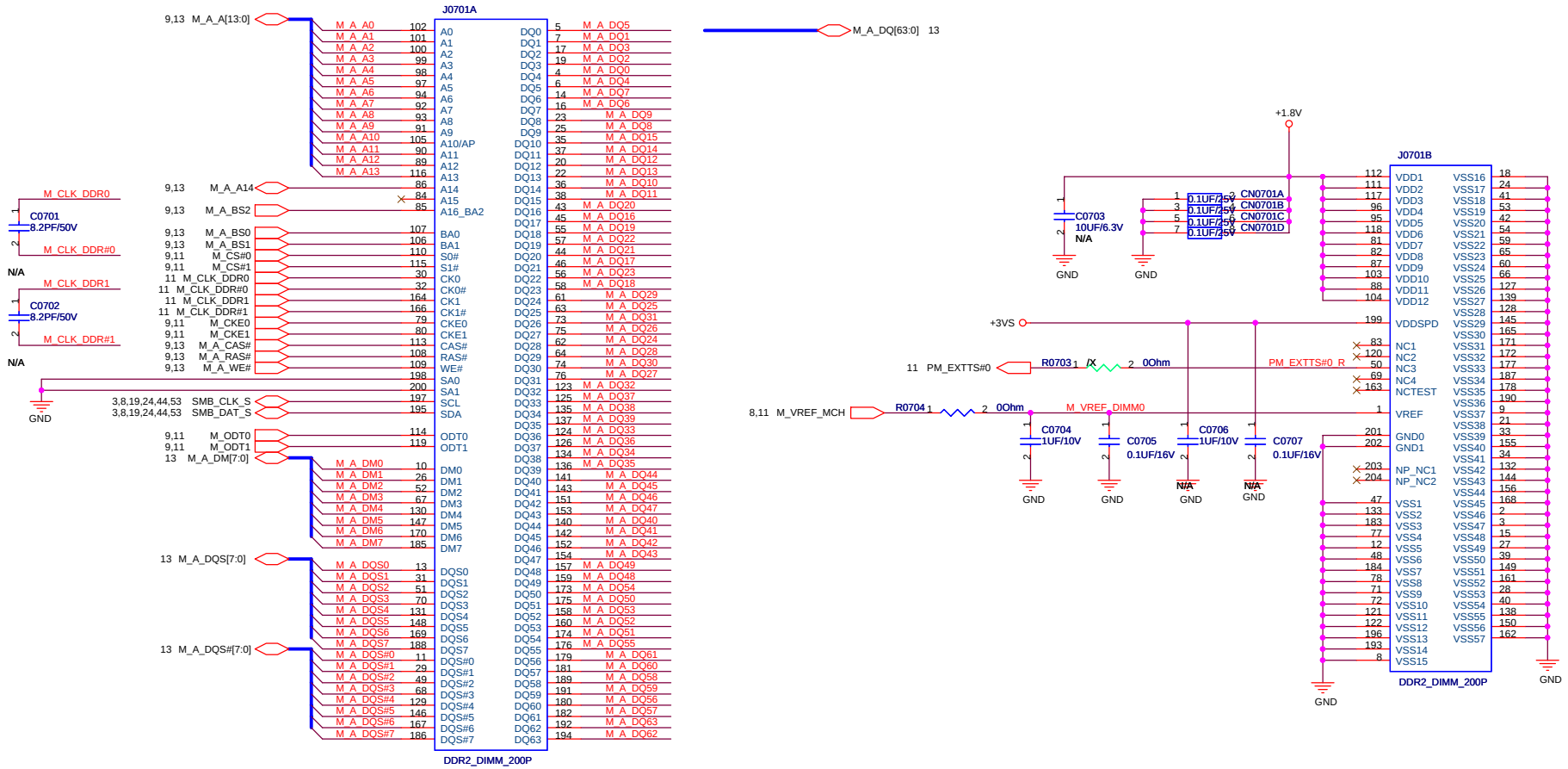
Thermal Trip signal (From CPU to ICH-9M and sequence)

Thermal trip control circit

ASUSTeK COMPUTER INC. NB1	Title : CPU CAPS	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 5 of 79	

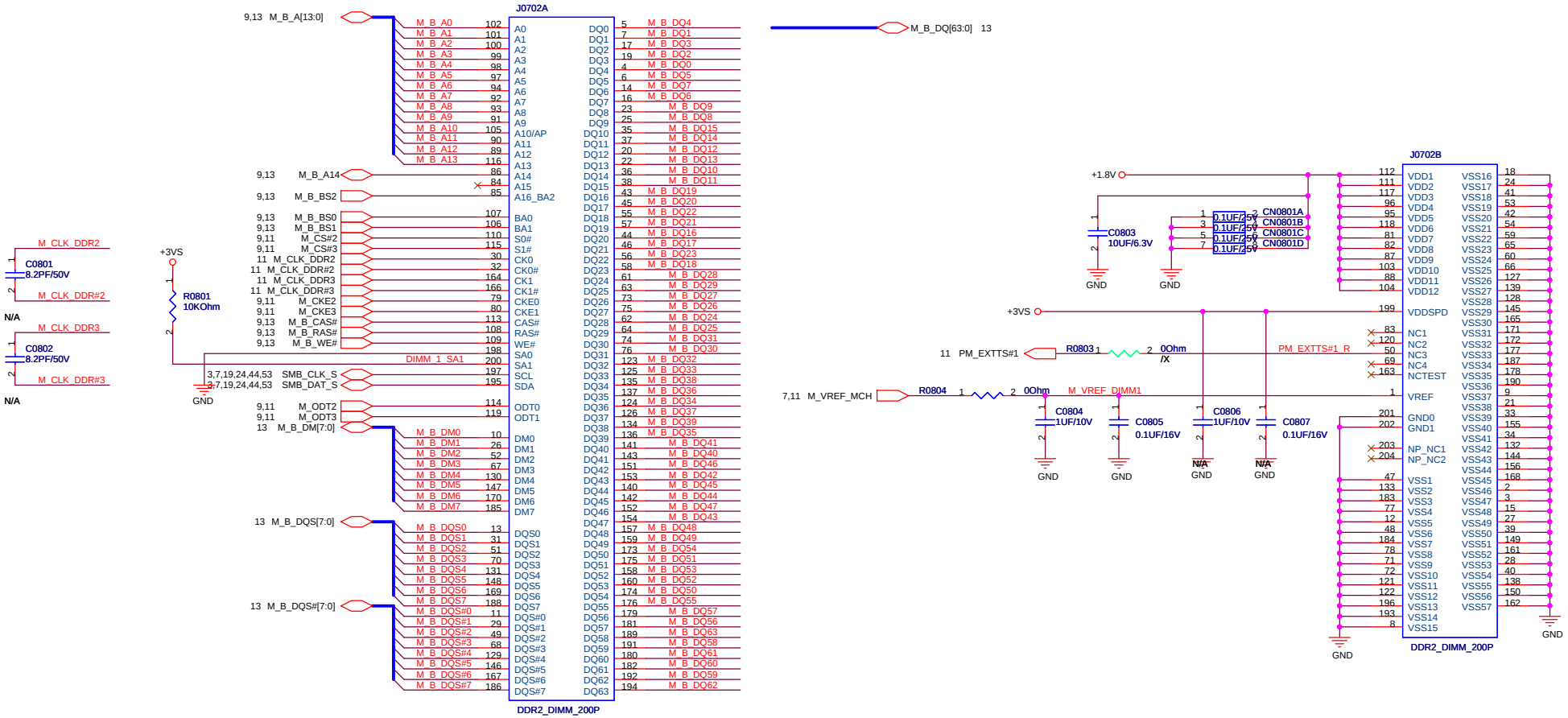
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: *yun-feng_yan*	
Size: A	Project Name: **N50A/N51A**	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 6 of 79	

REV Type



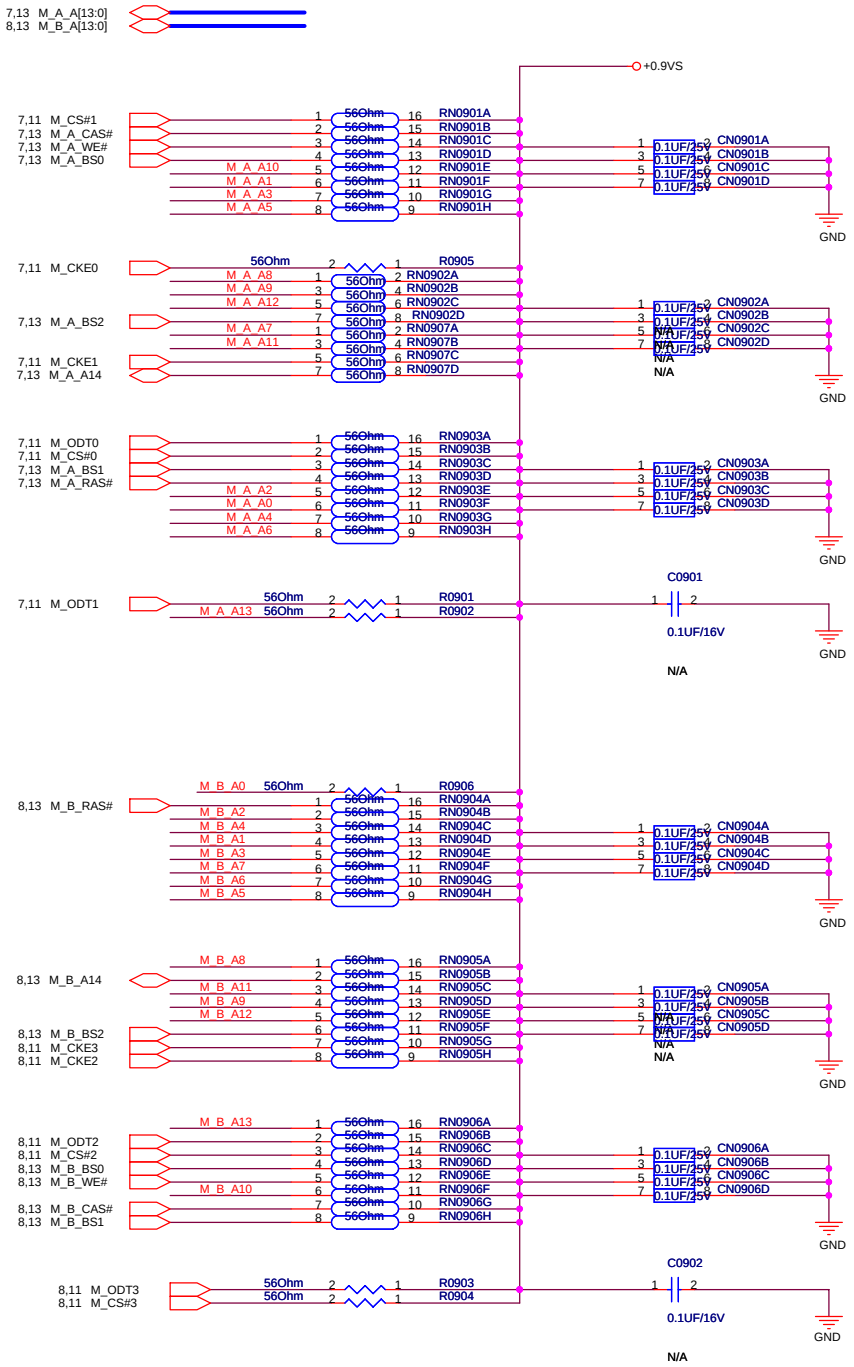
ASUSTeK COMPUTER INC. NB1	Title DDR2 SO-DIMM_0		
	Engineer: yun-feng_yan		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 7 of 79		

STD Type

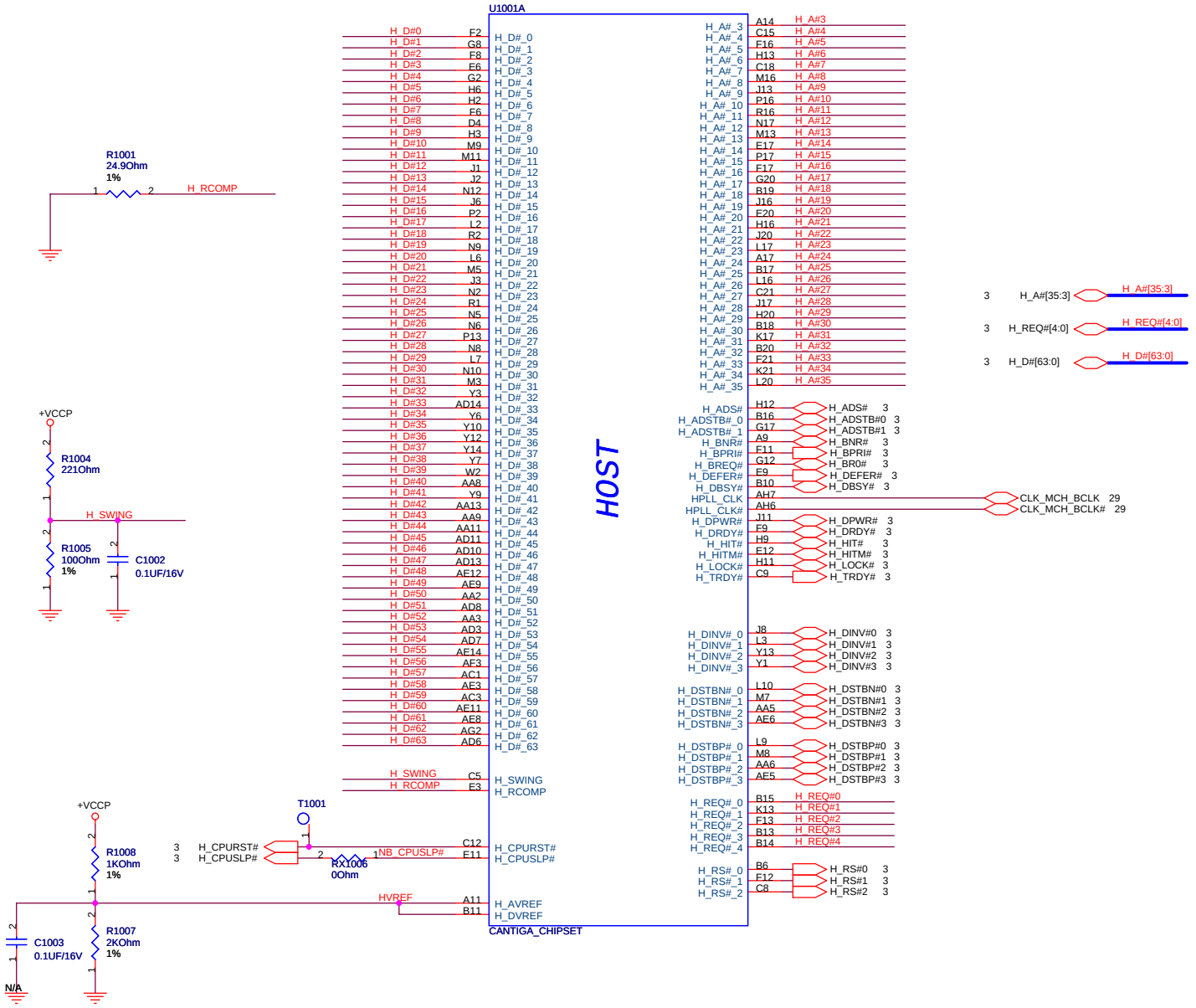


ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 8 of 79		

Title :DDR2 SO-DIMM_1



ASUSTeK COMPUTER INC. NB1	Title DDR2 termination	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 9 of 79	



Cap 0.1uF within 100 mils from GMCH

ASUSTeK COMPUTER INC. NB1	Title : Cantiga -- CPU (1)	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 10 of 79	

U1001B

RSVD

CONTROL/COMPENSATION

DDR

CLK

CFG

DMI

GRAPHICS VID

PM

ME

MISC

HDA

NC

CANTIGA_CHIPSET

ME JTAG PORT

T1122 ME_JTAG_TCK
T1123 ME_JTAG_TDI
T1124 ME_JTAG_TDO
T1125 ME_JTAG_TMS
T1126

R1130 0Ohm /X

2008-07-16

SDVO_CTRL_DATA : SDVO/iHDMI/DP Interface Present

0 = SDVO/iHDMI/DP Disabled (D)
1 = SDVO/iHDMI/DP Enabled

HDMI_SDA — R1149 /X — +3VS — 4.02KOHM 1%

DDPC_CTRLDATA : SDVO/iHDMI/DP Device Present

0 = No SDVO/iHDMI/DP (D)
1 = SDVO/iHDMI/DP Present

DDPC_CTRLDATA — R1150 /X — +3VS — 4.02KOHM 1%

+1.8V
R1105 1KOhm 1%
SM_RCOMP_VOH
C1101 2.2UF/10V
C1102 0.01UF/50V
R1106 3.01KOHM
SM_RCOMP_VOL
R1107 1KOhm 1%
C1103 2.2UF/10V
C1104 0.01UF/50V

+3VS
R1103 10KOhm
R1104 10KOhm
PM_EXTTS#0 7
PM_EXTTS#1 8
R1111 N/A 10KOhm MCH_CLKREQ#

+1.8V
R1109 1KOhm 1% N/A
M_VREF_MCH 7,8
R1110 1KOhm 1% N/A
C1107 0.1UF/16V
GND GND

+VCCP
R1108 1KOhm 1%
R1102 499Ohm 1%
C1106 0.1UF/16V
11/02
PM_PWROK_MCH
CL_VREF

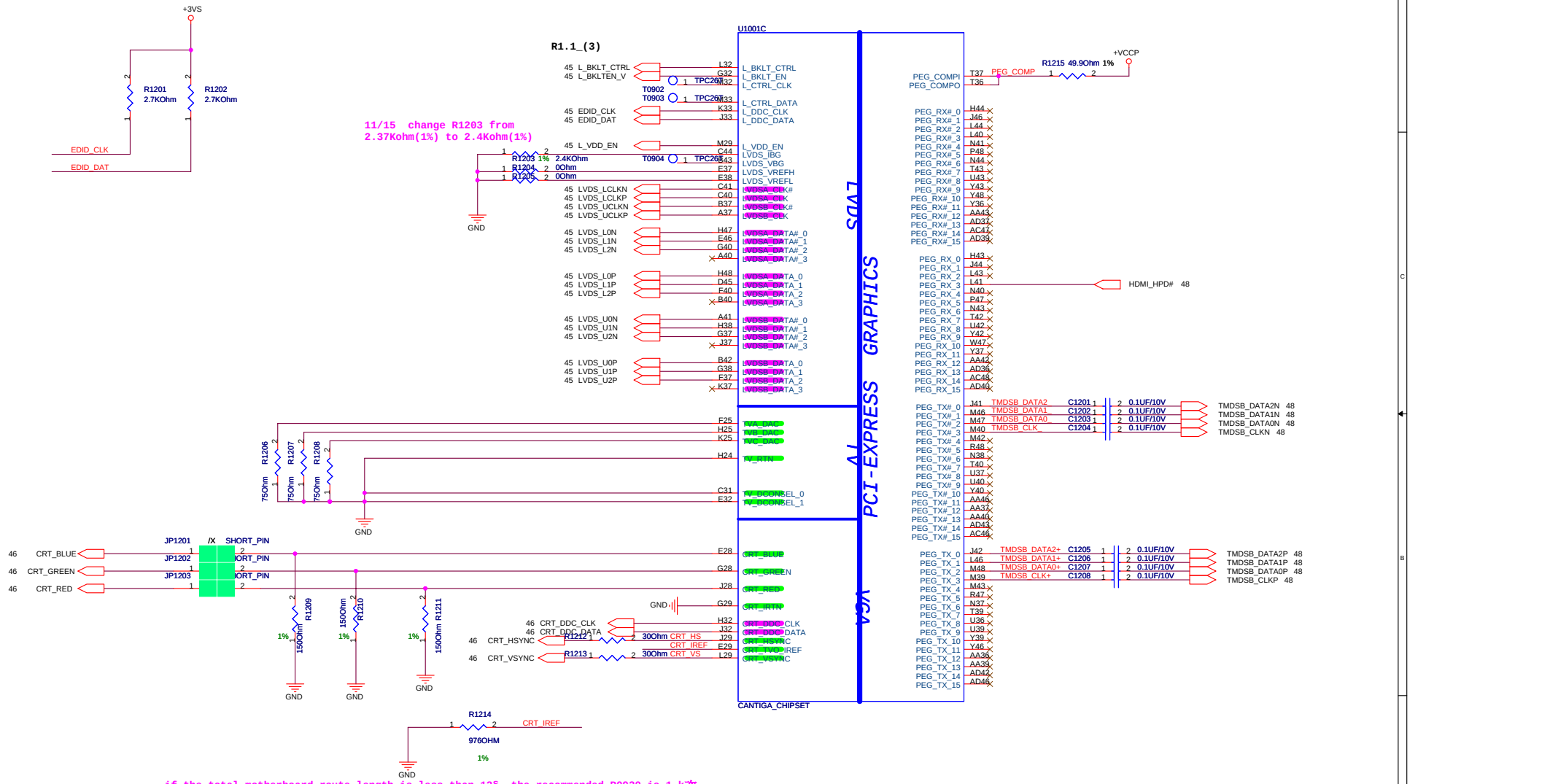
+1.8V
R1112 80.6Ohm 1%
R1117 80.6Ohm 1%
M_RCOMP
M_RCOMP#
SM_RCOMP_VOH
SM_RCOMP_VOL

M_VREF_MCH
C1105 0.01UF/50V /X
MCH_SM_REXT 499Ohm R1121 1%

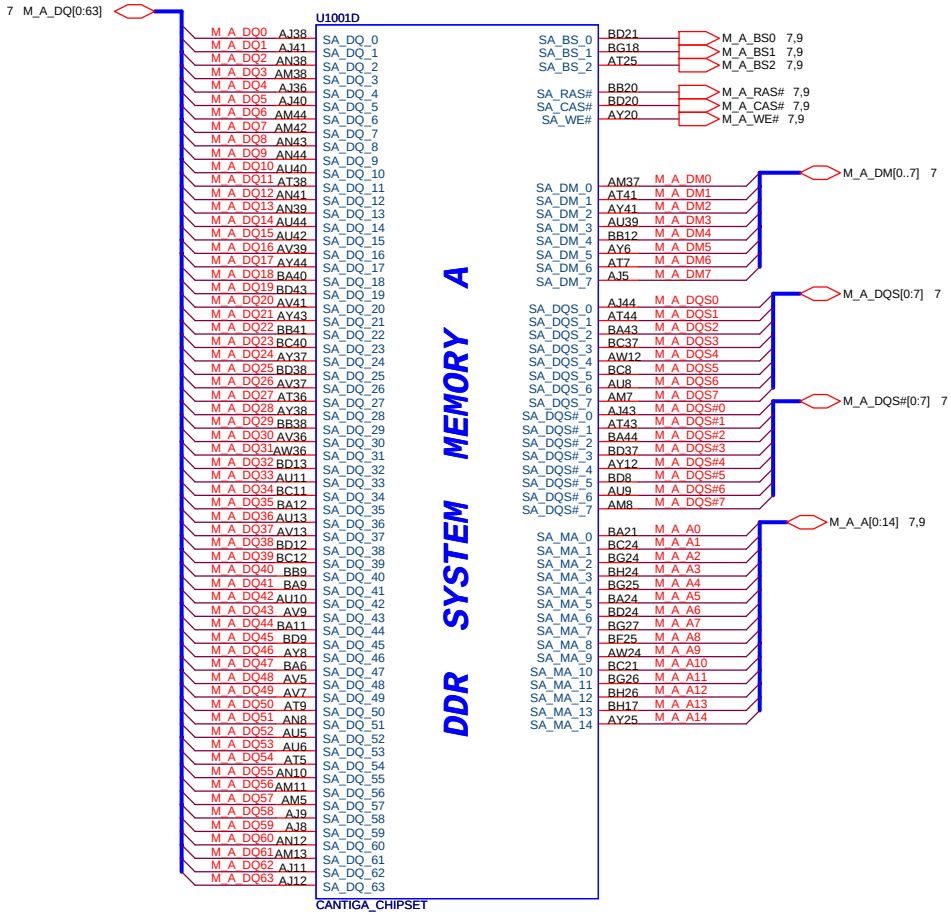
+VCCP
R1126 56Ohm
TSATN#

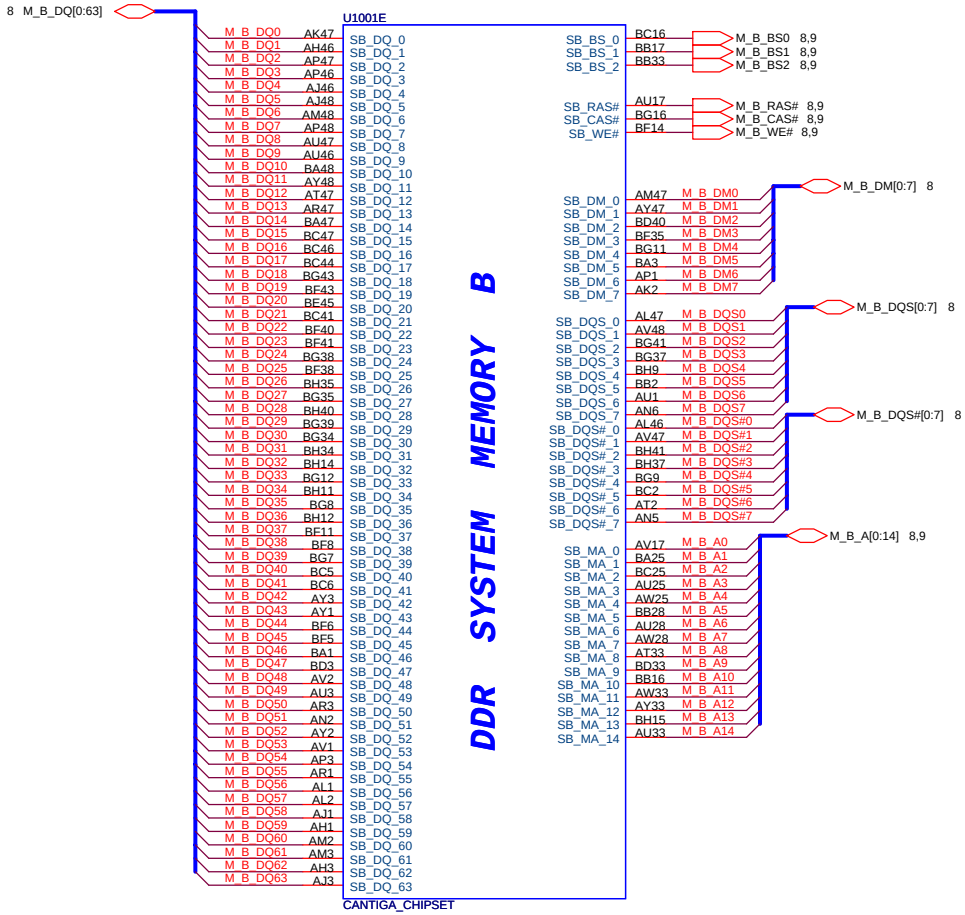
ACZ_BCLK_NB_R 49
ACZ_RST#_NB_R 49
R1174 33Ohm
ACZ_SDIN2_R 49
ACZ_SDOUT_NB_R 49
ACZ_SYNC_NB_R 49
For HDMI

Title :	Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan
Size: Custom	Project Name: N50A/N51A
Rev:	1.0
Date: Wednesday, August 06, 2008	Sheet 11 of 79



ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 12 of 79		





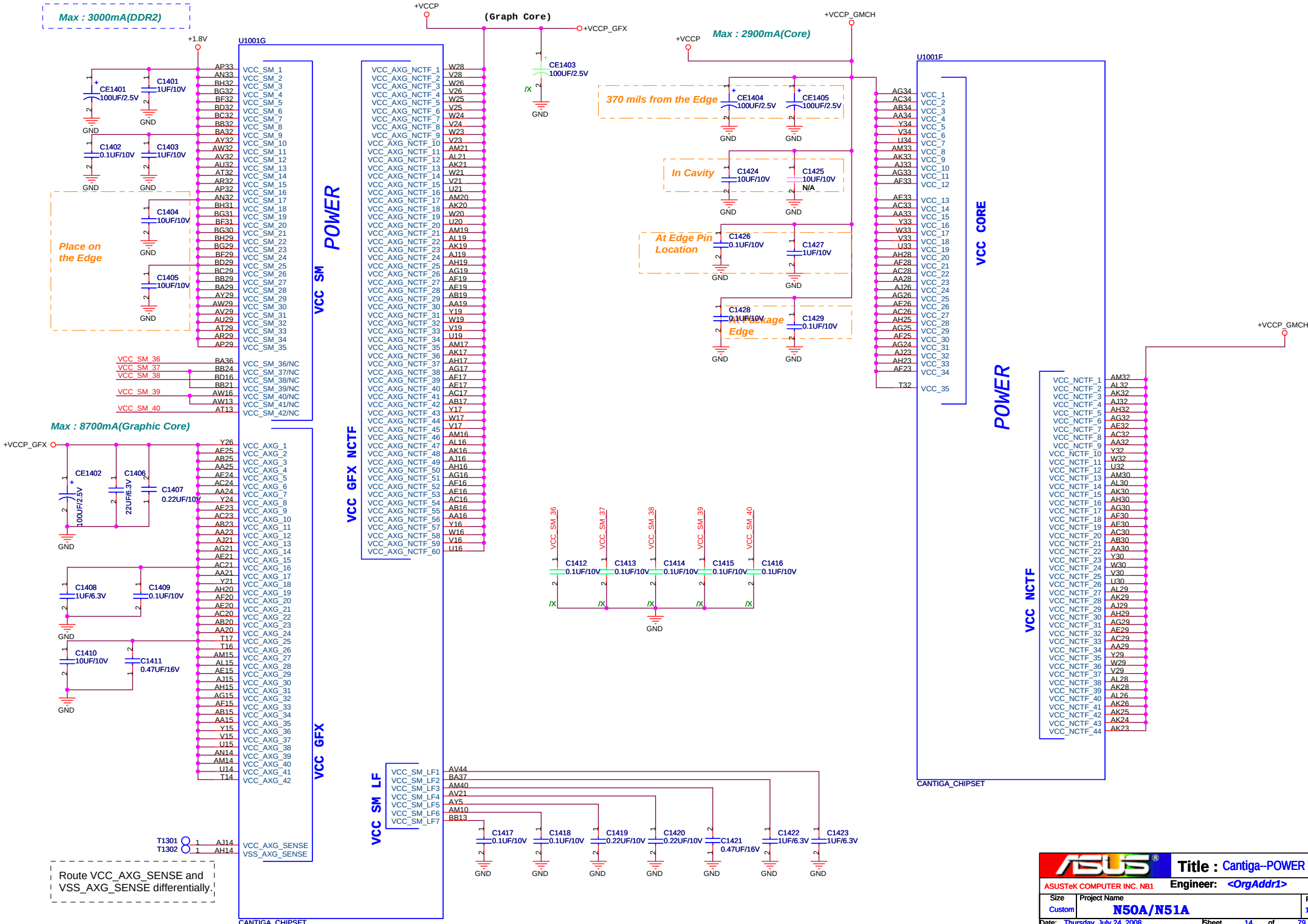
ASUSTeK COMPUTER INC. NB1

Title : Cantiga--DDR2 bus (3)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 13 of 79


Max : 3000mA(DDR2)
+1.8V
U1001G
CE1401 100UF/2.5V
C1401 1UF/10V
C1402 0.1UF/10V
C1403 1UF/10V
C1404 10UF/10V
C1405 10UF/10V
Place on the Edge
GND
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
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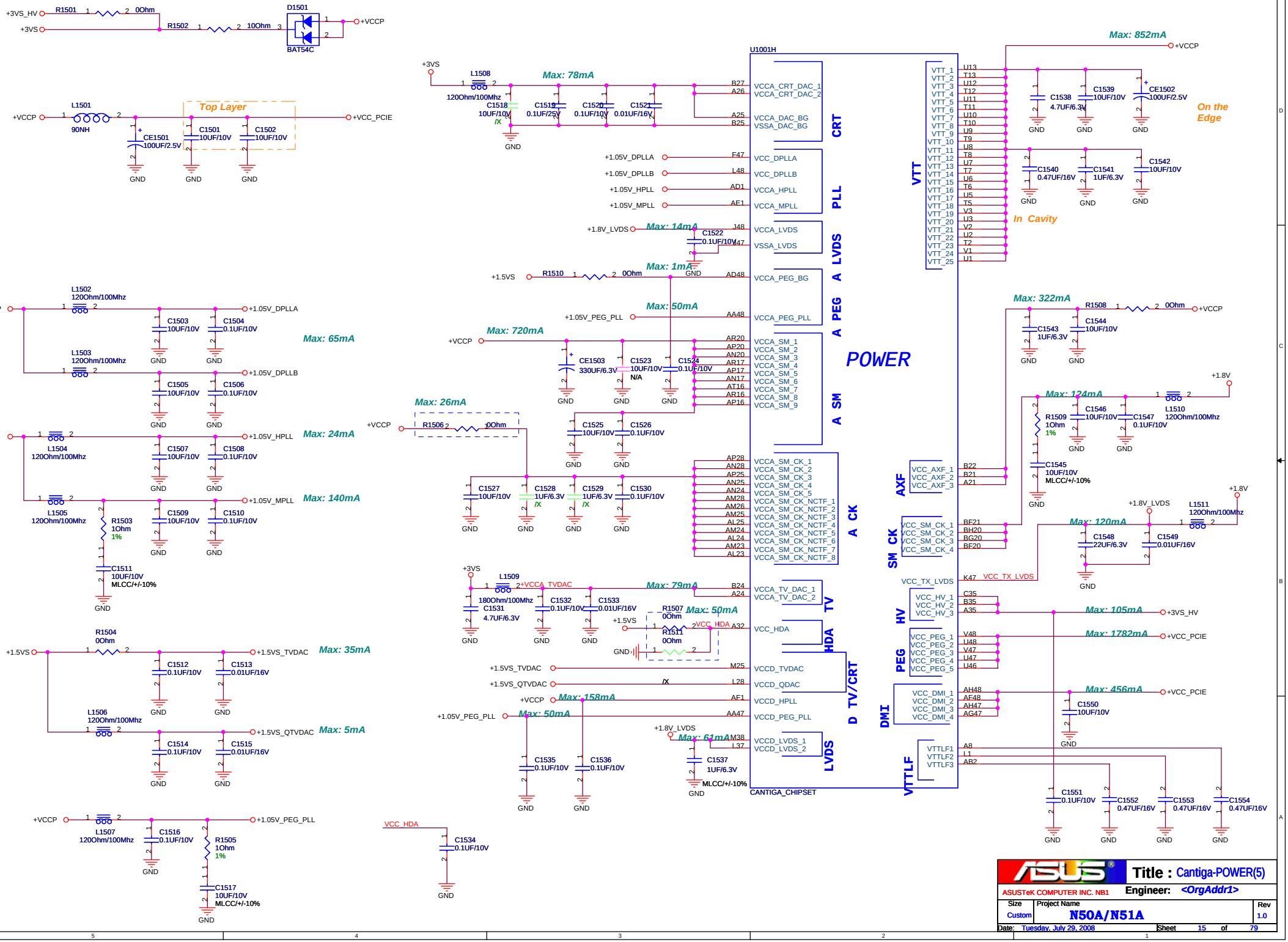
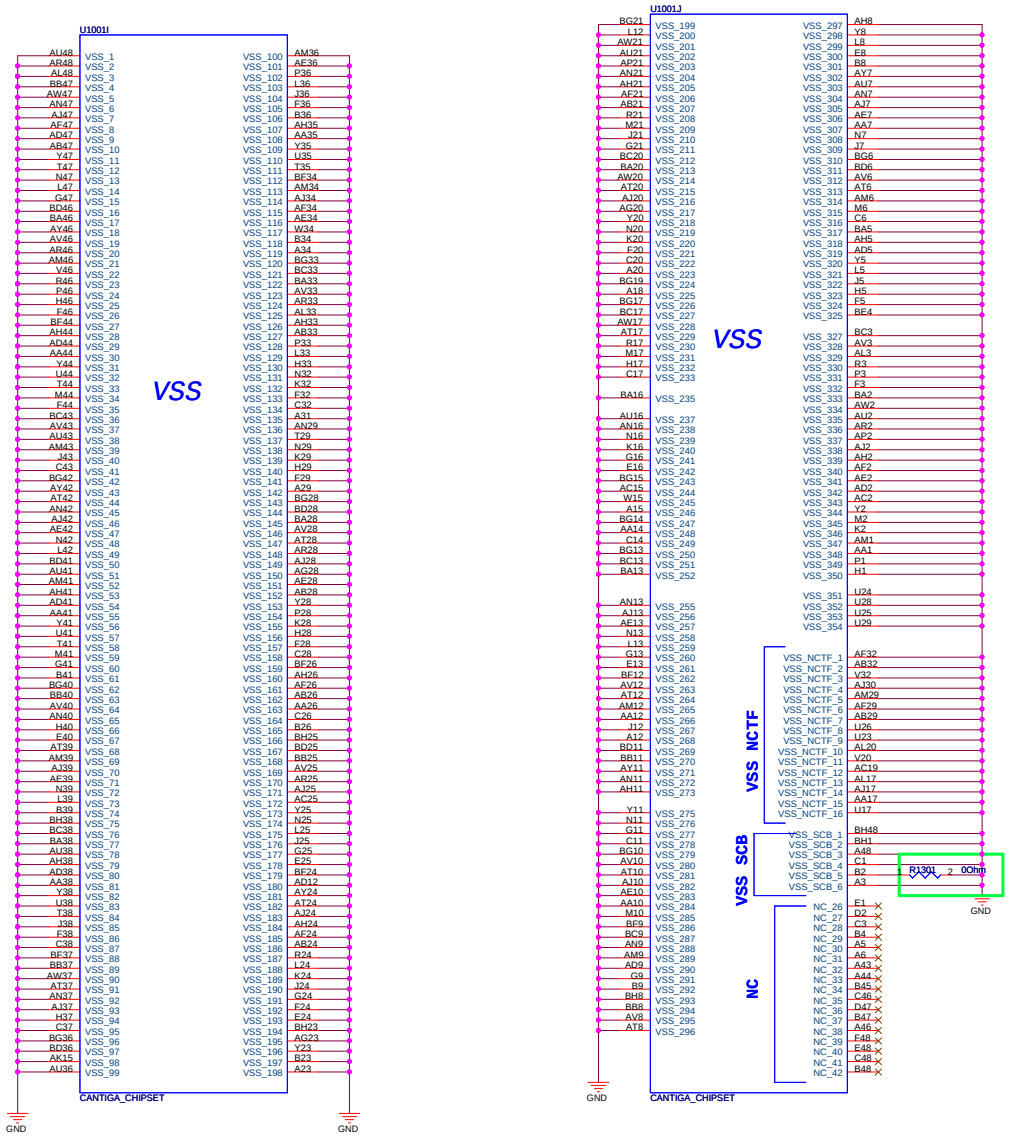
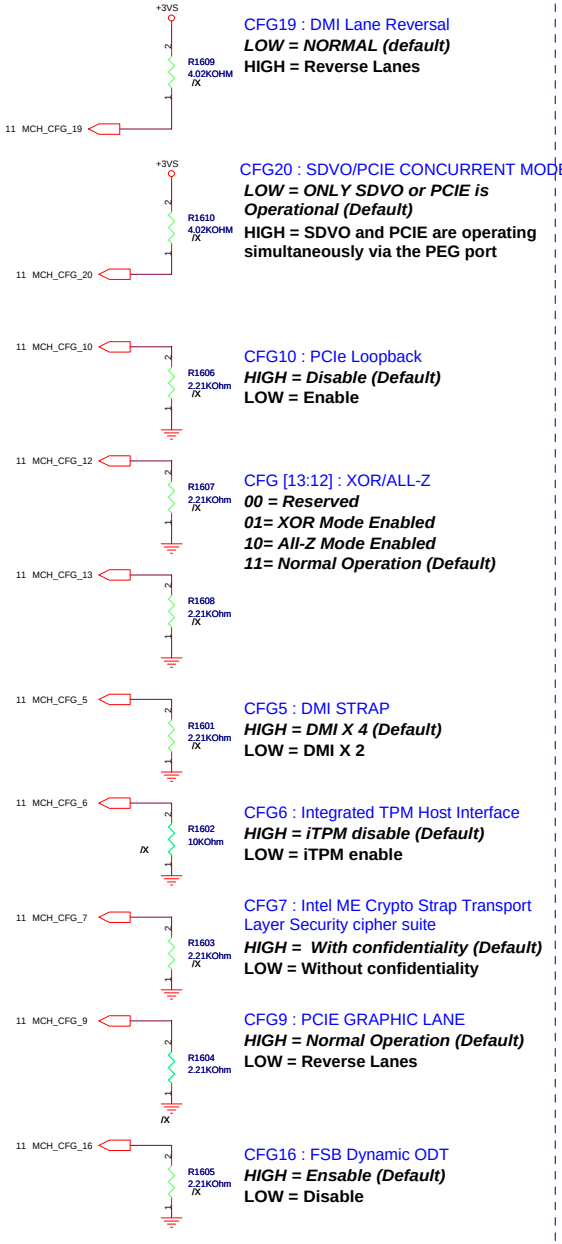
VCC_SM_34
VCC_SM_35
VCC_SM_36
VCC_SM_37
VCC_SM_38
VCC_SM_39
VCC_SM_40
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
Max : 8700mA(Graphic Core)
+VCCP_GFX
CE1402 100UF/2.5V
C1406 22UF/6.3V
C1407 0.22UF/10V
C1408 1UF/6.3V
C1409 0.1UF/10V
C1410 10UF/10V
C1411 0.47UF/16V
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC GFX
T1301
T1302
VCC_AXG_SENSE
VSS_AXG_SENSE
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.
CANTIGA_CHIPSET
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
+VCCP
(Graph Core)
+VCCP_GFX
CE1403 100UF/2.5V
/X
GND
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
C1417 0.1UF/10V
C1418 0.1UF/10V
C1419 0.22UF/10V
C1420 0.22UF/10V
C1421 0.47UF/16V
C1422 1UF/6.3V
C1423 1UF/6.3V
VCC SM LF
VCC_SM_36
VCC_SM_37
VCC_SM_38
VCC_SM_39
VCC_SM_40
C1412 0.1UF/10V
C1413 0.1UF/10V
C1414 0.1UF/10V
C1415 0.1UF/10V
C1416 0.1UF/10V
+VCCP_GMCH
+VCCP
Max : 2900mA(Core)
370 mils from the Edge
CE1404 100UF/2.5V
CE1405 100UF/2.5V
In Cavity
C1424 10UF/10V
C1425 10UF/10V N/A
At Edge Pin Location
C1426 0.1UF/10V
C1427 1UF/10V
At Package Edge
C1428 0.1UF/10V
C1429 0.1UF/10V
U1001F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
T32
VCC CORE
POWER
+VCCP_GMCH
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
CANTIGA_CHIPSET
ASUSTeK COMPUTER INC. NB1
Title : Cantiga--POWER (4)
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Thursday, July 24, 2008
Sheet 14 of 79


+3VS_HV
+3VS
R1501 0Ohm
R1502 10Ohm
D1501
BAT54C
+VCCP
L1501
90NH
Top Layer
+VCC_PCIE
CE1501 100UF/2.5V
C1501 10UF/10V
C1502 10UF/10V
GND
U1001H
CANTIGA_CHIPSET
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
VCCA_DAC_BG
VSSA_DAC_BG
VCC_DPLLA
VCC_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
VCCA_TV_DAC_1
VCCA_TV_DAC_2
VCC_HDA
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1
VCCD_LVDS_2
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
VCC_TX_LVDS
VCC_HV_1
VCC_HV_2
VCC_HV_3
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
VTTLF1
VTTLF2
VTTLF3
+1.05V_DPLLA
+1.05V_DPLLB
+1.05V_HPLL
+1.05V_MPLL
+1.05V_PEG_PLL
+1.5VS
+1.5VS_TVDAC
+1.5VS_QTVDAC
+1.8V_LVDS
+1.8V
+VCCA_TVDAC
VCC_TX_LVDS
Max: 852mA
Max: 322mA
Max: 124mA
Max: 120mA
Max: 105mA
Max: 1782mA
Max: 456mA
Max: 78mA
Max: 14mA
Max: 1mA
Max: 50mA
Max: 720mA
Max: 26mA
Max: 65mA
Max: 24mA
Max: 140mA
Max: 79mA
Max: 50mA
Max: 158mA
Max: 61mA
Max: 35mA
Max: 5mA
On the Edge
In Cavity
Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Tuesday, July 29, 2008
Sheet 15 of 79



R1.1_(4)



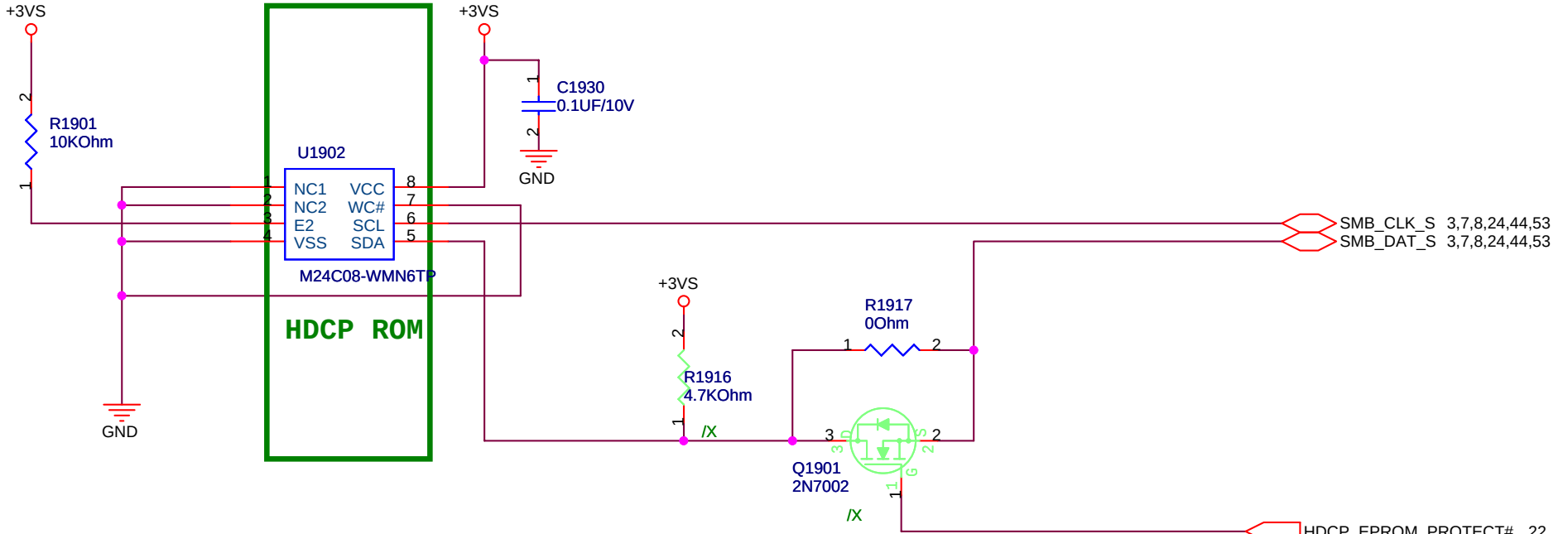
ASUSTeK COMPUTER INC. NB1	Title : Cantiga-GND	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 16 of 79	

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 17 of 79	

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: B	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 18 of 79

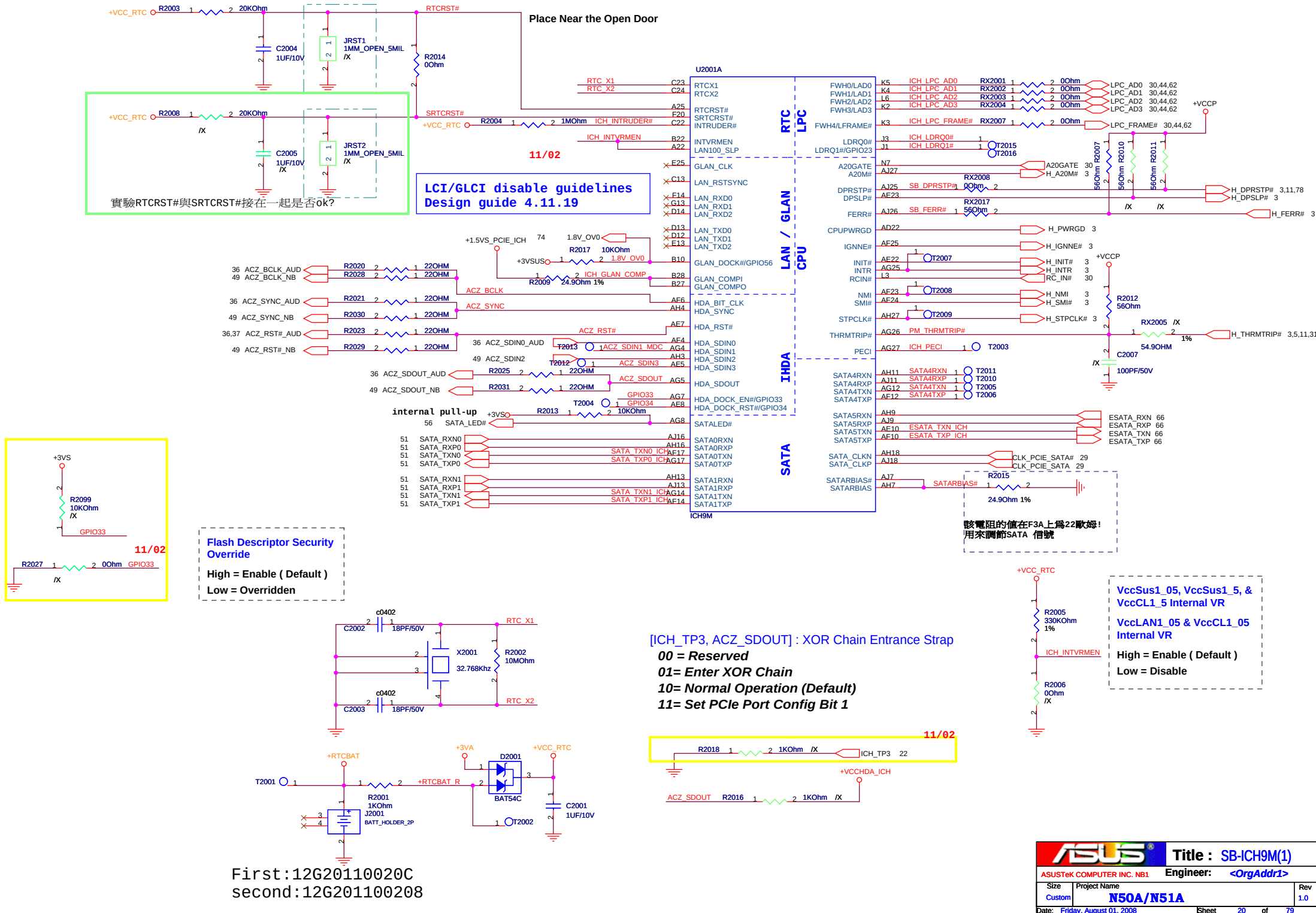
R1.1_(11)

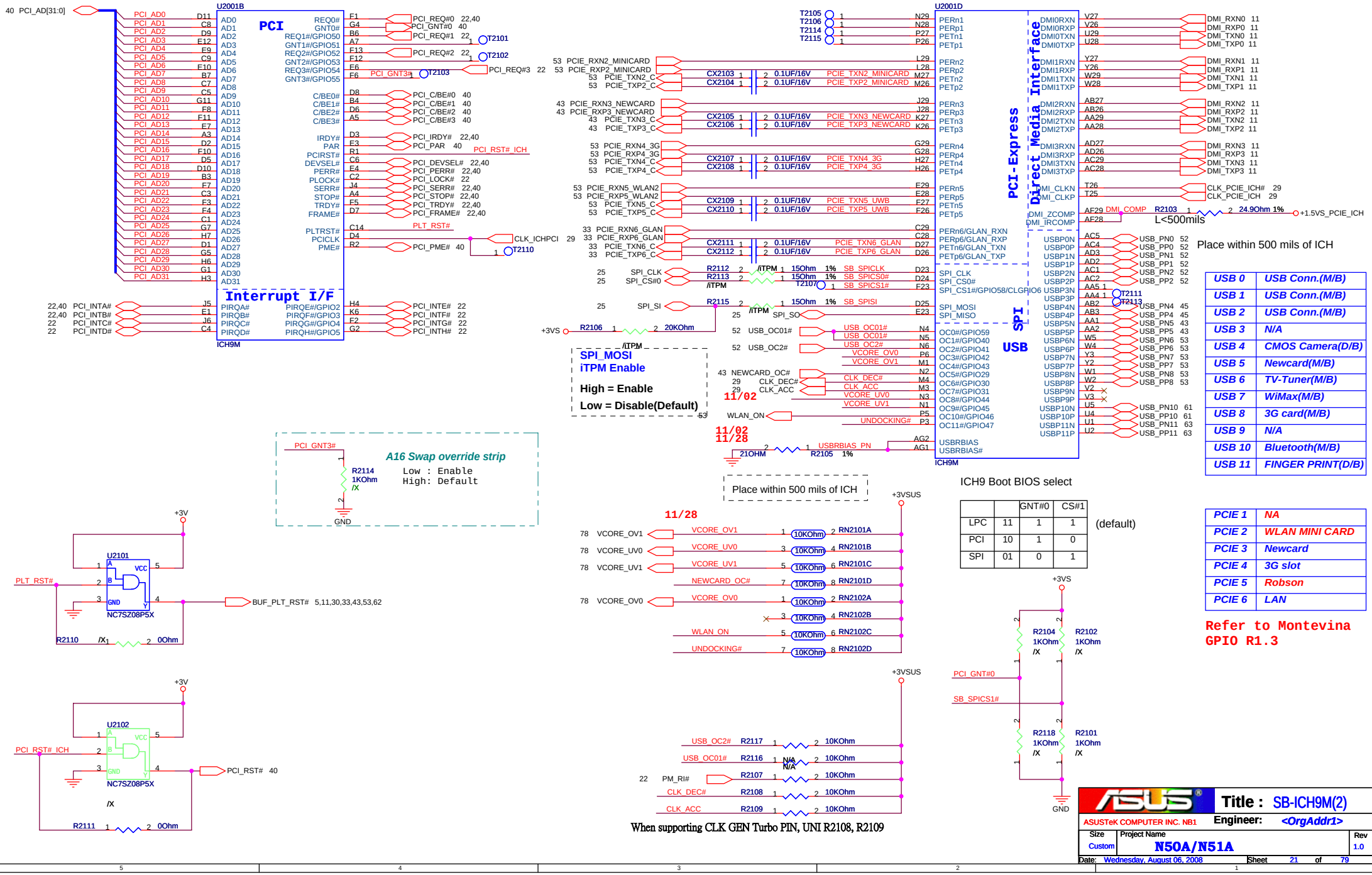
R1.1_(42)



S:05G020600010

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 19 of 79	

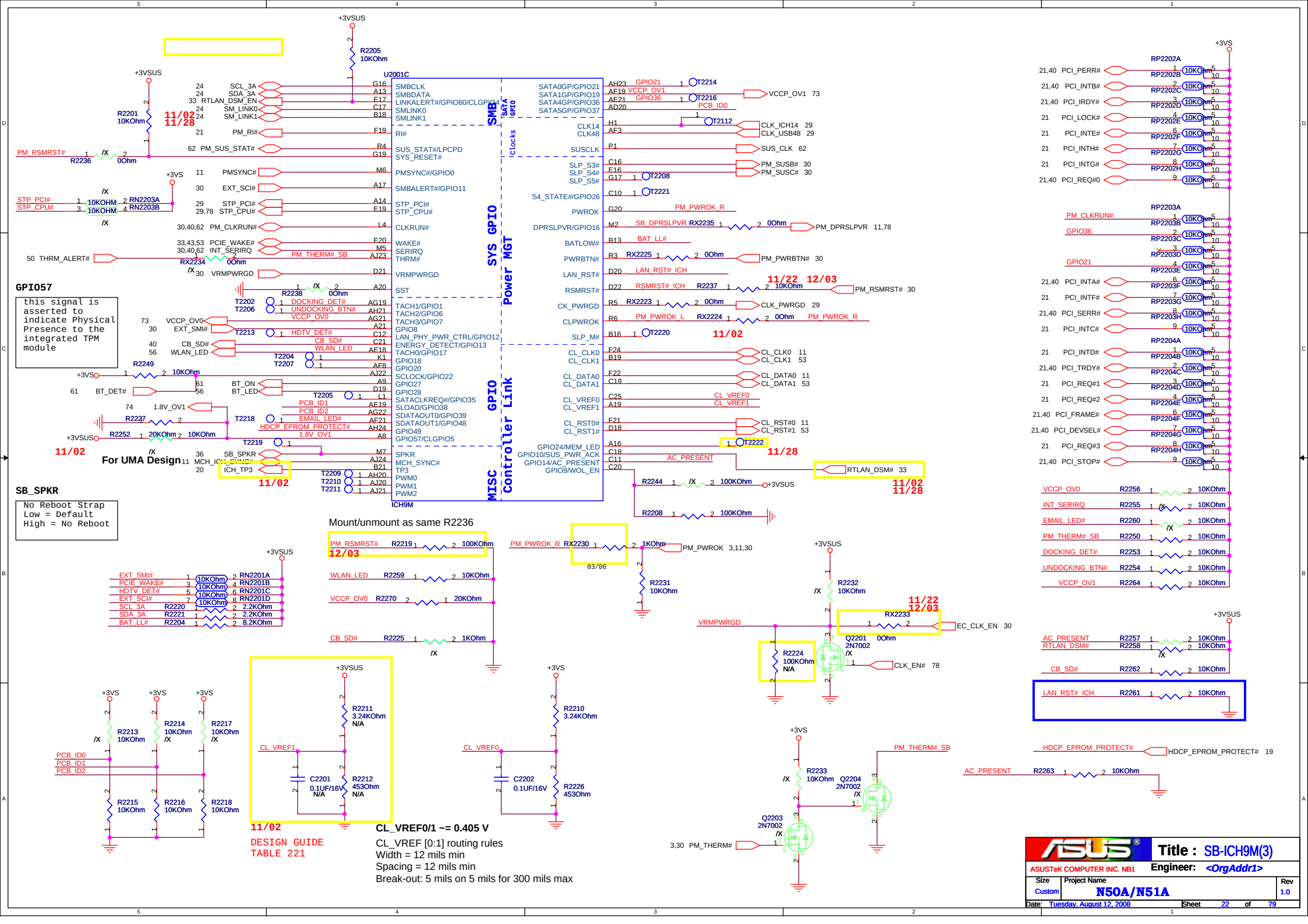

Place Near the Open Door
11/02
實驗RTCRST#與SRTCRST#接在一起是否ok?
LCI/GLCI disable guidelines
Design guide 4.11.19
U2001A
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
ICH9M
internal pull-up
Flash Descriptor Security Override
High = Enable (Default)
Low = Overridden
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
11/02
R2018 1 2 1KOhm /X ICH_TP3 22
+VCCHDA_ICH
ACZ_SDOUT R2016 1 2 1KOhm /X
R2005 330KOhm 1% ICH_INTVRMEN R2006 0Ohm /X
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
R2099 10KOhm /X GPIO33
R2027 1 2 0Ohm GPIO33 /X
11/02
該電阻的值在F3A上爲22歐姆!
用來調節SATA 信號
R2015 24.9Ohm 1%
First:12G20110020C
second:12G201100208
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
Sheet 20 of 79

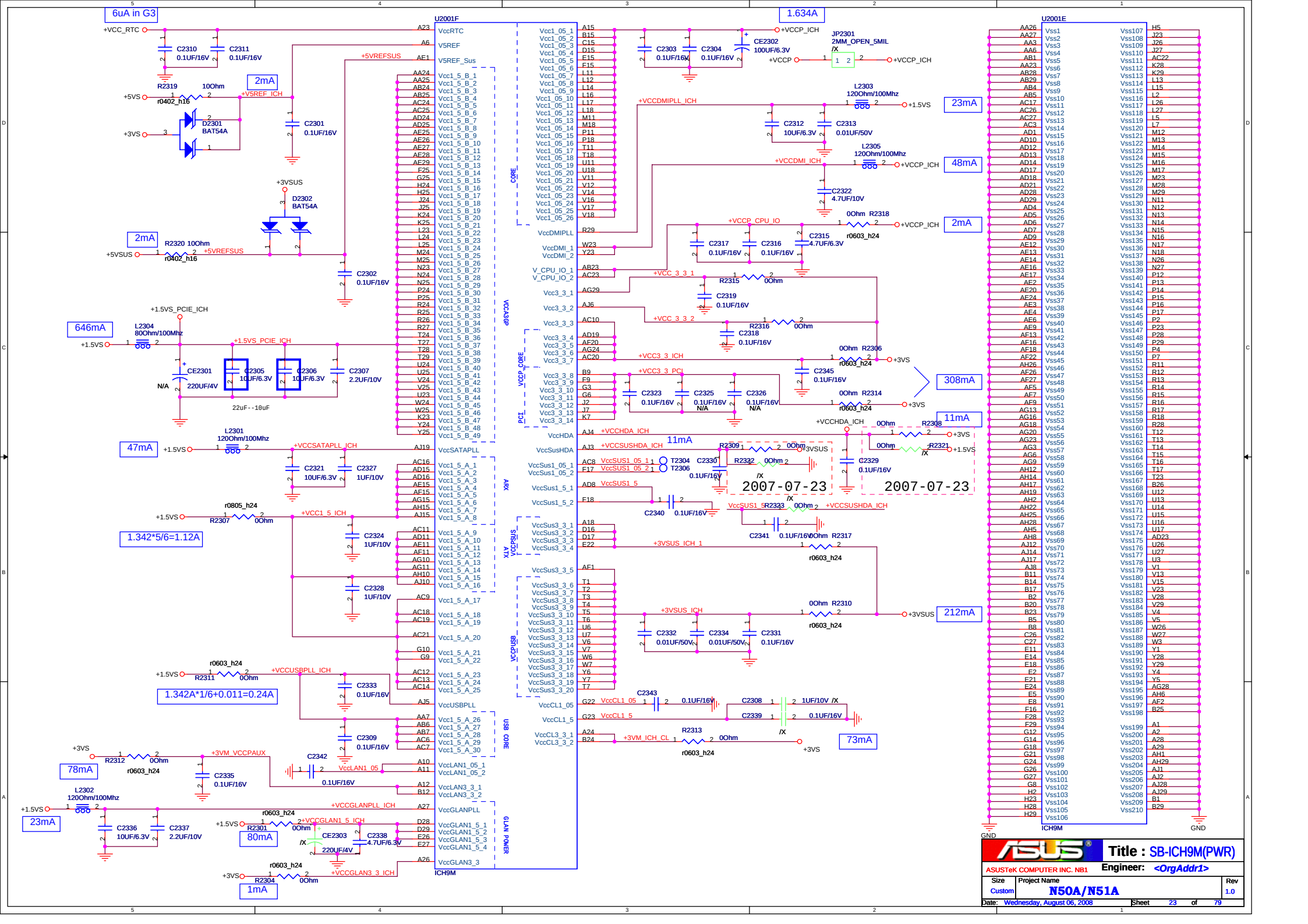


		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

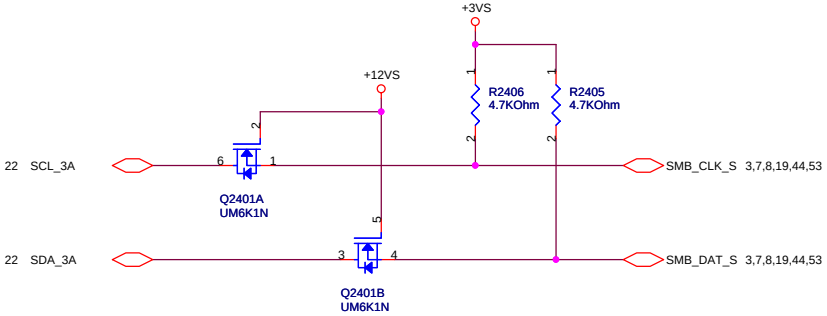
USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	N/A
USB 4	CMOS Camera(D/B)
USB 5	Newcard(M/B)
USB 6	TV-Tuner(M/B)
USB 7	WiMax(M/B)
USB 8	3G card(M/B)
USB 9	N/A
USB 10	Bluetooth(M/B)
USB 11	FINGER PRINT(D/B)

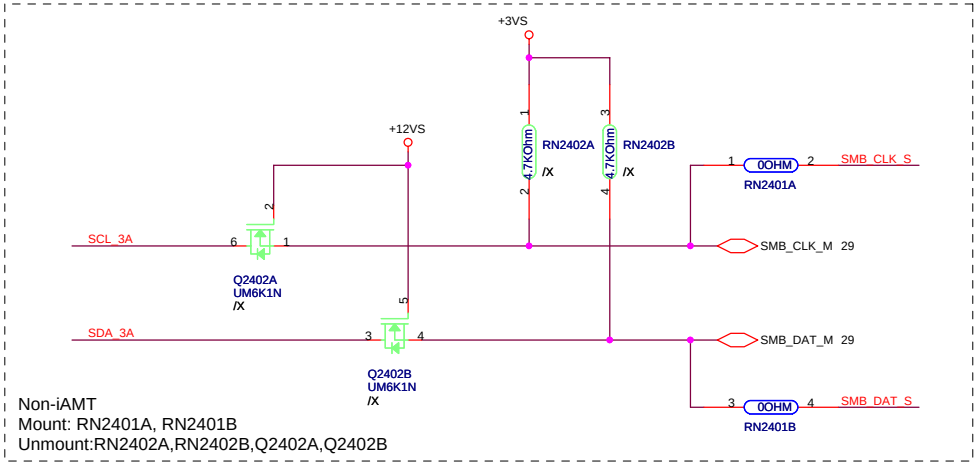
PCIE 1	NA
PCIE 2	WLAN MINI CARD
PCIE 3	Newcard
PCIE 4	3G slot
PCIE 5	Robson
PCIE 6	LAN


U2001C
ICH9M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
GPIO57
this signal is asserted to indicate Physical Presence to the integrated TPM module
SB_SPKR
No Reboot Strap
Low = Default
High = No Reboot
For UMA Design
Mount/unmount as same R2236
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
DESIGN GUIDE
TABLE 221
ASUSTeK COMPUTER INC. NB1
Title : SB-ICH9M(3)
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Tuesday, August 12, 2008
Sheet 22 of 79


6uA in G3
1.634A
U2001F
U2001E
ICH9M
+VCC_RTC
C2310 0.1UF/16V
C2311 0.1UF/16V
2mA
R2319 10Ohm
r0402_h16
+5VS
+3VS
D2301 BAT54A
C2301 0.1UF/16V
+5VREFSUS
+5VREF_ICH
+3VSUS
D2302 BAT54A
R2320 10Ohm
+5VSUS
C2302 0.1UF/16V
+1.5VS_PCIE_ICH
646mA
L2304 80Ohm/100Mhz
+1.5VS
CE2301 220UF/4V
C2305 10UF/6.3V
C2306 10UF/6.3V
C2307 2.2UF/10V
22uF--10uF
47mA
L2301 120Ohm/100Mhz
+VCCSATAPLL_ICH
C2321 10UF/6.3V
C2327 1UF/10V
r0805_h24
R2307 0Ohm
+VCC1_5_ICH
1.342*5/6=1.12A
C2324 1UF/10V
C2328 1UF/10V
r0603_h24
R2311 0Ohm
+VCCUSBPLL_ICH
1.342A*1/6+0.011=0.24A
C2333 0.1UF/16V
C2309 0.1UF/16V
78mA
R2312 0Ohm
+3VM_VCCPAUX
C2335 0.1UF/16V
C2342 0.1UF/16V
VccLAN1_05
23mA
L2302 120Ohm/100Mhz
C2336 10UF/6.3V
C2337 2.2UF/10V
+VCCGLANPLL_ICH
80mA
R2301 0Ohm
+VCCGLAN1_5_ICH
CE2303 220UF/4V
C2338 4.7UF/6.3V
1mA
R2304 0Ohm
+VCCGLAN3_3_ICH
+VCCP_ICH
JP2301 2MM_OPEN_5MIL
CE2302 100UF/6.3V
C2303 0.1UF/16V
C2304 0.1UF/16V
+VCCP
+VCCDMIPLL_ICH
L2303 120Ohm/100Mhz
+1.5VS
23mA
C2312 10UF/6.3V
C2313 0.01UF/50V
+VCCDMI_ICH
L2305 120Ohm/100Mhz
48mA
C2322 4.7UF/10V
+VCCP_CPU_IO
0Ohm R2318
C2317 0.1UF/16V
C2316 0.1UF/16V
C2315 4.7UF/6.3V
2mA
+VCC_3_3_1
R2315 0Ohm
C2319 0.1UF/16V
+VCC_3_3_2
R2316 0Ohm
C2318 0.1UF/16V
+VCC3_3_ICH
0Ohm R2306
C2345 0.1UF/16V
+VCC3_3_PCI
C2323 0.1UF/16V
C2325 0.1UF/16V
C2326 0.1UF/16V
N/A
0Ohm R2314
308mA
+VCCHDA_ICH
0Ohm R2308
11mA
+VCCSUSHDA_ICH
R2309 0Ohm
R2321 /X
T2304
T2306
C2330 0.1UF/16V
R2332 0Ohm
C2329 0.1UF/16V
2007-07-23
VccSUS1_5
C2340 0.1UF/16V
R2333 0Ohm
C2341 0.1UF/16V
R2317 0Ohm
+3VSUS_ICH_1
+3VSUS_ICH
0Ohm R2310
212mA
C2332 0.01UF/50V
C2334 0.01UF/50V
C2331 0.1UF/16V
C2343 0.1UF/16V
C2308 1UF/10V /X
C2339 0.1UF/16V
+3VM_ICH_CL
R2313 0Ohm
73mA
GND
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Title : SB-ICH9M(PWR)
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Wednesday, August 06, 2008
Sheet 23 of 79

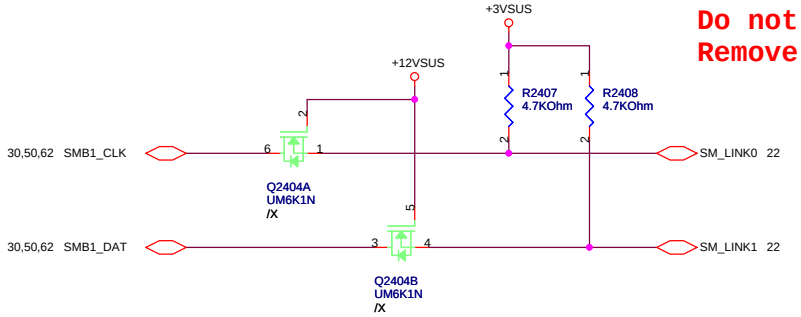
ICH9-M





Non-iAMT
Mount: RN2401A, RN2401B
Unmount:RN2402A,RN2402B,Q2402A,Q2402B

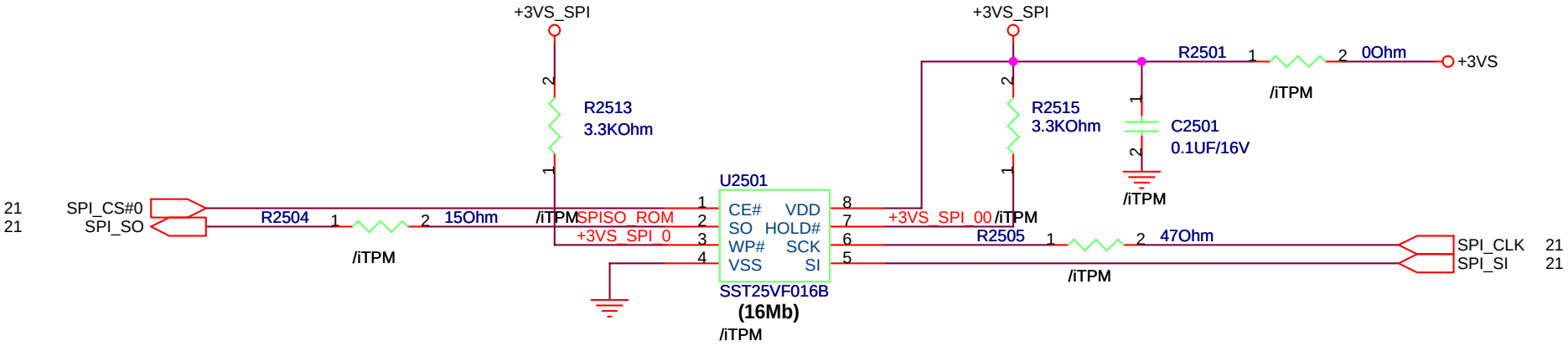
EC-IT8752



Do not support iAMT
Remove ME-EC smbus

Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S SMB_DAT_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card B. SMB_CLK_M SMB_DAT_M → CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor

ASUSTeK COMPUTER INC. NB1 — Title : ICH9M-Other
Engineer: <OrgAddr1>
Size: Custom | Project Name: N50A/N51A | Rev: 1.0
Date: Friday, August 01, 2008 | Sheet 24 of 79



FOR iTPM
8Mb 05G00120A010

ASUSTeK COMPUTER INC. NB1	Title : SPI ROM	
	Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 25 of 79	

ASUSTeK COMPUTER INC. NB1	Title :			
	Engineer: <OrgAddr1>			
Size: A	Project Name: N50A/N51A			Rev: 1.0
Date: Thursday, July 24, 2008		Sheet 26 of 79		

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 27 of 79	

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 28 of 79	

2 source:RTM875T-363 06G011501020

U2901

ICS9LPR363EGLF-T

PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled

PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled

PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled

PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled

Latched Input Select

Decide pin 43/44
0 = SRC CLK
1 = CPU_ITP CLK
(Pin8)
ITP_EN

Decide pin 17/18
0 = LCDCLK
1 = PCIEX
(Pin5)
SELPCIE0_LCD#

Decide pin 40/41
0 = PCIECLK
1 = PEREQ#
(Pin64)
REQ_SEL#

Decide pin 17/18
SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS
SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0
(Pin9)

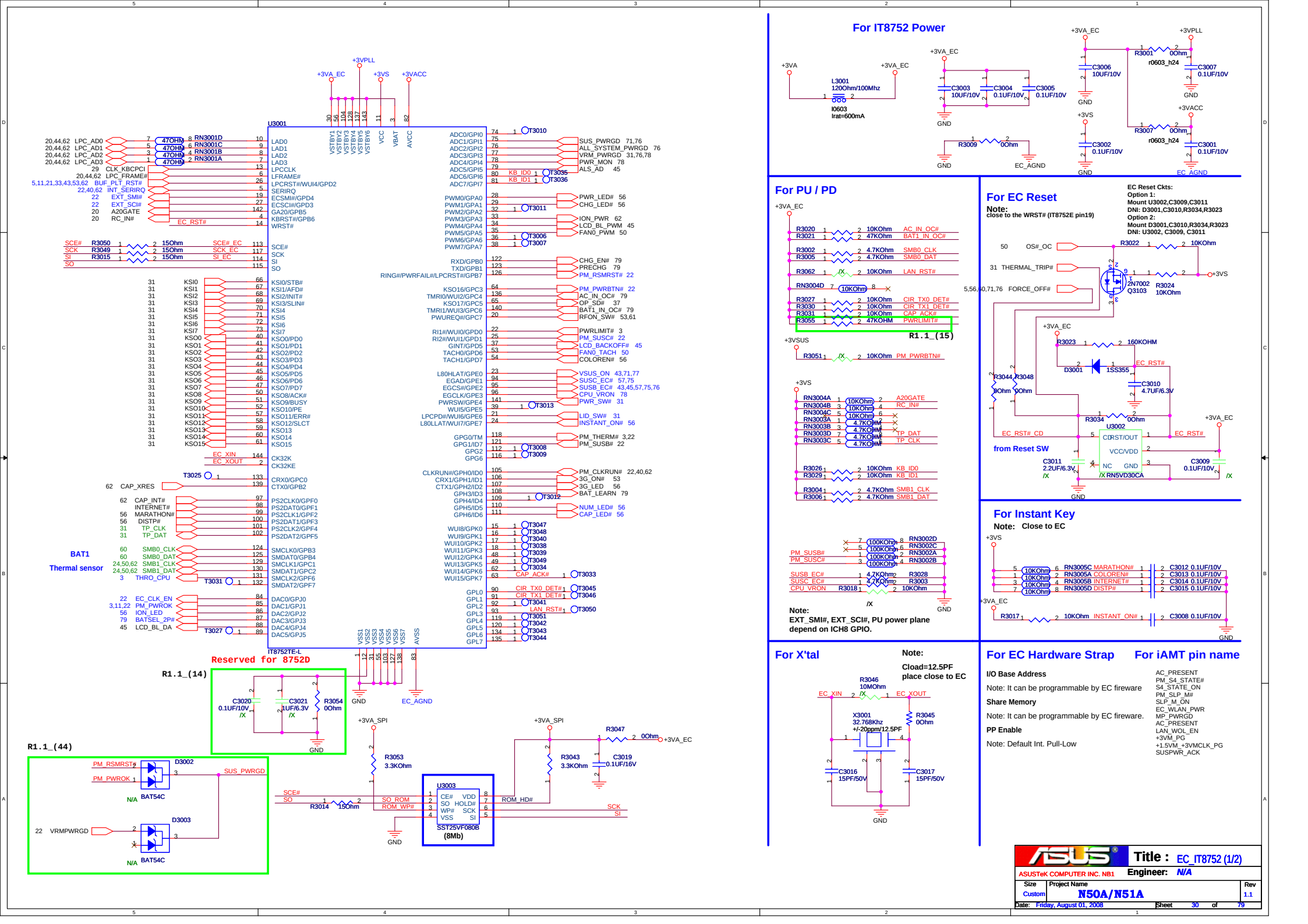
BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO	UNI	10K	0
364:NO TBO	UNI	UNI	UNI

Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9	27FIXSS
	SELLCD_27#=1	DOT96	LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=0	PCIEX9	PCIEX0
	SELLCD_27#=1	DOT96	PCIEX0

ASUSTeK COMPUTER INC. NB1
Title : CLOCK GEN
Engineer: <OrgAddr1>
Size: Custom
Project Name: N50A/N51A
Rev: 1.0
Date: Tuesday, August 05, 2008
Sheet 29 of 79


U3001
IT8752TE-L
+3VPLL
+3VA_EC
+3VS
+3VACC
LAD0
LAD1
LAD2
LAD3
LPCCLK
LFRAME#
LPCRST#/WUI4/GPD2
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
GA20/GPB5
KBRST#/GPB6
WRST#
SCE#
SCK
SI
SO
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
CK32K
CK32KE
CRX0/GPC0
CTX0/GPB2
PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7
DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7
RXD/GPB0
TXD/GPB1
RING#/PWRFAIL#/LPCRST#/GPB7
KSO16/GPC3
TMRI0/WUI2/GPC4
KSO17/GPC5
TMRI1/WUI3/GPC6
PWUREQ#/GPC7
RI1#/WUI0/GPD0
RI2#/WUI1/GPD1
GINT/GPD5
TACH0/GPD6
TACH1/GPD7
L80HLAT/GPE0
EGAD/GPE1
EGCS#/GPE2
EGCLK/GPE3
PWRSW/GPE4
WUI5/GPE5
LPCPD#/WUI6/GPE6
L80LLAT/WUI7/GPE7
GPG0/TM
GPG1/ID7
GPG2
GPG6
CLKRUN#/GPH0/ID0
CRX1/GPH1/ID1
CTX1/GPH2/ID2
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
WUI8/GPK0
WUI9/GPK1
WUI10/GPK2
WUI11/GPK3
WUI12/GPK4
WUI13/GPK5
WUI14/GPK6
WUI15/GPK7
GPL0
GPL1
GPL2
GPL3
GPL4
GPL5
GPL6
GPL7
VSTBY1
VSTBY2
VSTBY3
VSTBY4
VSTBY5
VSTBY6
VCC
VBAT
AVCC
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
AVSS
RN3001D
RN3001C
RN3001B
RN3001A
47OHM
EC_RST#
R3050
R3049
R3015
15Ohm
SCE# EC
SCK EC
SI EC
T3025
CAP_XRES
CAP_INT#
INTERNET#
MARATHON#
DISTP#
TP_CLK
TP_DAT
BAT1
Thermal sensor
SMB0_CLK
SMB0_DAT
SMB1_CLK
SMB1_DAT
THRO_CPU
T3031
EC_CLK_EN
PM_PWROK
ION_LED
BATSEL_2P#
LCD_BL_DA
T3027
EC_XIN
EC_XOUT
Reserved for 8752D
R1.1_(14)
C3020
0.1UF/10V
/X
C3021
1UF/6.3V
/X
R3054
0Ohm
GND
EC_AGND
R1.1_(44)
D3002
BAT54C
N/A
D3003
BAT54C
N/A
PM_RSMRST#
PM_PWROK
SUS_PWRGD
VRMPWRGD
+3VA_SPI
R3053
3.3KOhm
R3014
15Ohm
SCE#
SO
SO_ROM
ROM_WP#
U3003
SST25VF080B
(8Mb)
ROM_HD#
SCK
SI
R3047
0Ohm
R3043
3.3KOhm
C3019
0.1UF/16V
T3010
T3035
T3036
T3011
T3006
T3007
T3013
T3012
T3047
T3048
T3040
T3038
T3039
T3049
T3034
T3033
T3045
T3046
T3041
T3050
T3051
T3042
T3043
T3044
SUS_PWRGD 71,76
ALL_SYSTEM_PWRGD 76
VRM_PWRGD 31,76,78
PWR_MON 78
ALS_AD 45
KB_ID0
KB_ID1
PWR_LED# 56
CHG_LED# 56
ION_PWR 62
LCD_BL_PWM 45
FAN0_PWM 50
CHG_EN# 79
PRECHG 79
PM_RSMRST# 3
PM_PWRBTN# 22
AC_IN_OC# 79
OP_SD# 37
BAT1_IN_OC# 79
RFON_SW# 53,61
PWRLIMIT# 3
PM_SUSC# 22
LCD_BACKOFF# 45
FAN0_TACH 50
COLOREN# 56
VSUS_ON 43,71,77
SUSC_EC# 57,75
SUSB_EC# 43,45,57,75,76
CPU_VRON 78
PWR_SW# 31
LID_SW# 31
INSTANT_ON# 56
PM_THERM# 3,22
PM_SUSB# 22
PM_CLKRUN# 22,40,62
3G_ON# 53
3G_LED 56
BAT_LEARN 79
NUM_LED# 56
CAP_LED# 56
CAP_ACK#
CIR_TX0_DET#
CIR_TX1_DET#
LAN_RST#
For IT8752 Power
+3VA
L3001
120Ohm/100Mhz
I0603
Irat=600mA
C3003
10UF/10V
C3004
0.1UF/10V
C3005
0.1UF/10V
R3009
0Ohm
EC_AGND
C3006
10UF/10V
R3001
0Ohm
r0603_h24
C3007
0.1UF/10V
C3002
0.1UF/10V
R3007
0Ohm
r0603_h24
C3001
0.1UF/10V
For PU / PD
R3020
10KOhm
AC_IN_OC#
R3021
47KOhm
BAT1_IN_OC#
R3002
4.7KOhm
SMB0_CLK
R3005
4.7KOhm
SMB0_DAT
R3062
10KOhm
LAN_RST#
RN3004D
10KOhm
R3027
10KOhm
CIR_TX0_DET#
R3030
10KOhm
CIR_TX1_DET#
R3031
10KOhm
CAP_ACK#
R3055
47KOHM
PWRLIMIT#
R1.1_(15)
+3VSUS
R3051
10KOhm
PM_PWRBTN#
RN3004A
RN3004B
RN3004C
RN3003A
RN3003B
RN3003D
RN3003C
10KOhm
4.7KOhm
A20GATE
RC_IN#
TP_DAT
TP_CLK
R3026
10KOhm
KB_ID0
R3029
10KOhm
KB_ID1
R3004
4.7KOhm
SMB1_CLK
R3006
4.7KOhm
SMB1_DAT
PM_SUSB#
PM_SUSC#
SUSB_EC#
SUSC_EC#
CPU_VRON
R3018
100KOhm
RN3002D
RN3002C
RN3002A
RN3002B
4.7KOhm
R3028
R3003
10KOhm
/X
Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.
For EC Reset
Note:
close to the WRST# (IT8752E pin19)
EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011
OS#_OC
THERMAL_TRIP#
FORCE_OFF#
5,56,70,71,76
R3022
10KOhm
2N7002
Q3103
R3024
10KOhm
+3VS
R3023
160KOHM
D3001
1SS355
EC_RST#
C3010
4.7UF/6.3V
R3044
R3048
0Ohm
R3034
0Ohm
U3002
CRST/OUT
VCC/VDD
NC
GND
EC_RST# CD
EC_RST#
from Reset SW
C3011
2.2UF/6.3V
/X
/X RN5VD30CA
C3009
0.1UF/10V
/X
For Instant Key
Note: Close to EC
+3VS
RN3005C MARATHON#
RN3005A COLOREN#
RN3005B INTERNET#
RN3005D DISTP#
10KOhm
C3012 0.1UF/10V
C3013 0.1UF/10V
C3014 0.1UF/10V
C3015 0.1UF/10V
+3VA_EC
R3017
10KOhm
INSTANT_ON#
C3008 0.1UF/10V
For X'tal
Note:
Cload=12.5PF
place close to EC
R3046
10MOhm
EC_XIN
EC_XOUT
X3001
32.768Khz
+/-20ppm/12.5PF
R3045
0Ohm
C3016
15PF/50V
C3017
15PF/50V
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
Title : EC_IT8752 (1/2)
ASUSTeK COMPUTER INC. NB1
Engineer: N/A
Size Custom
Project Name N50A/N51A
Rev 1.1
Date: Friday, August 01, 2008
Sheet 30 of 79

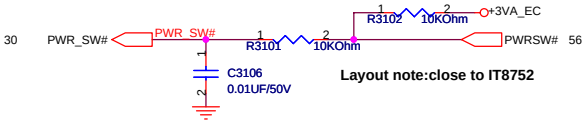
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

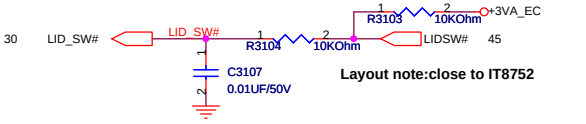
In Page 60

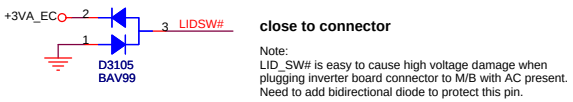
For Switch

PWR SWITCH



LID SWITCH

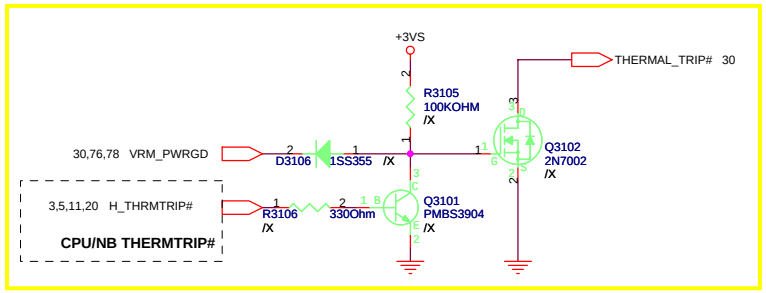




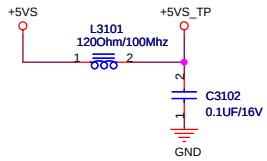
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

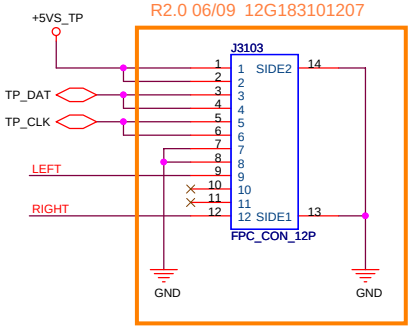
For Thermal Control Method

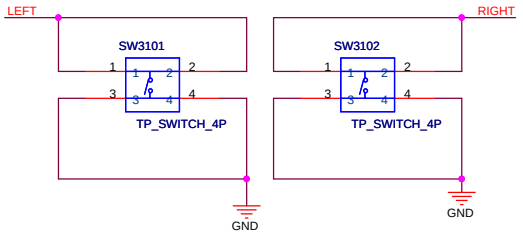
11/20 Remove redundant components

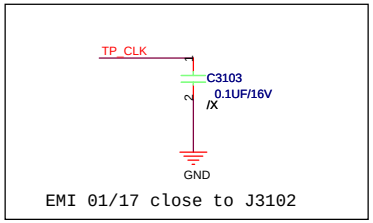


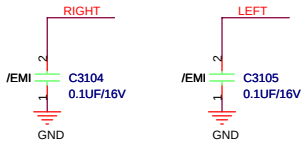
Touchpad Connector



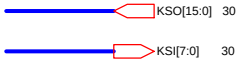




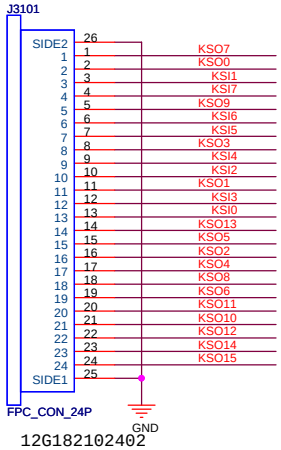




Keyboard Connector

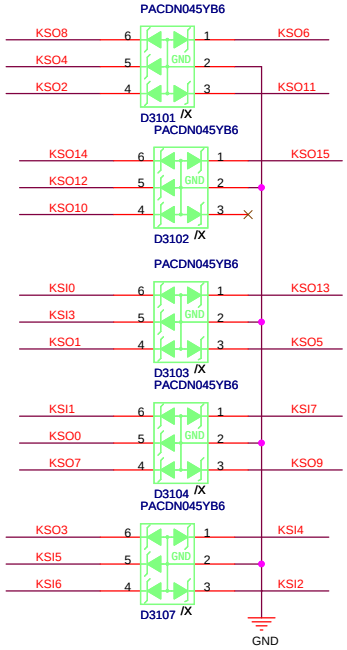


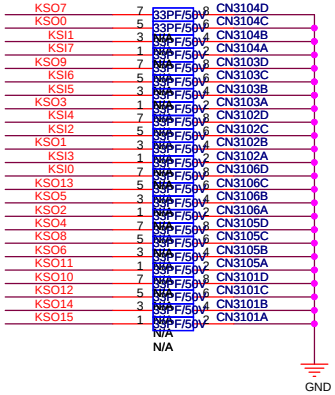
F7/N1 Keyboard



12G182102402

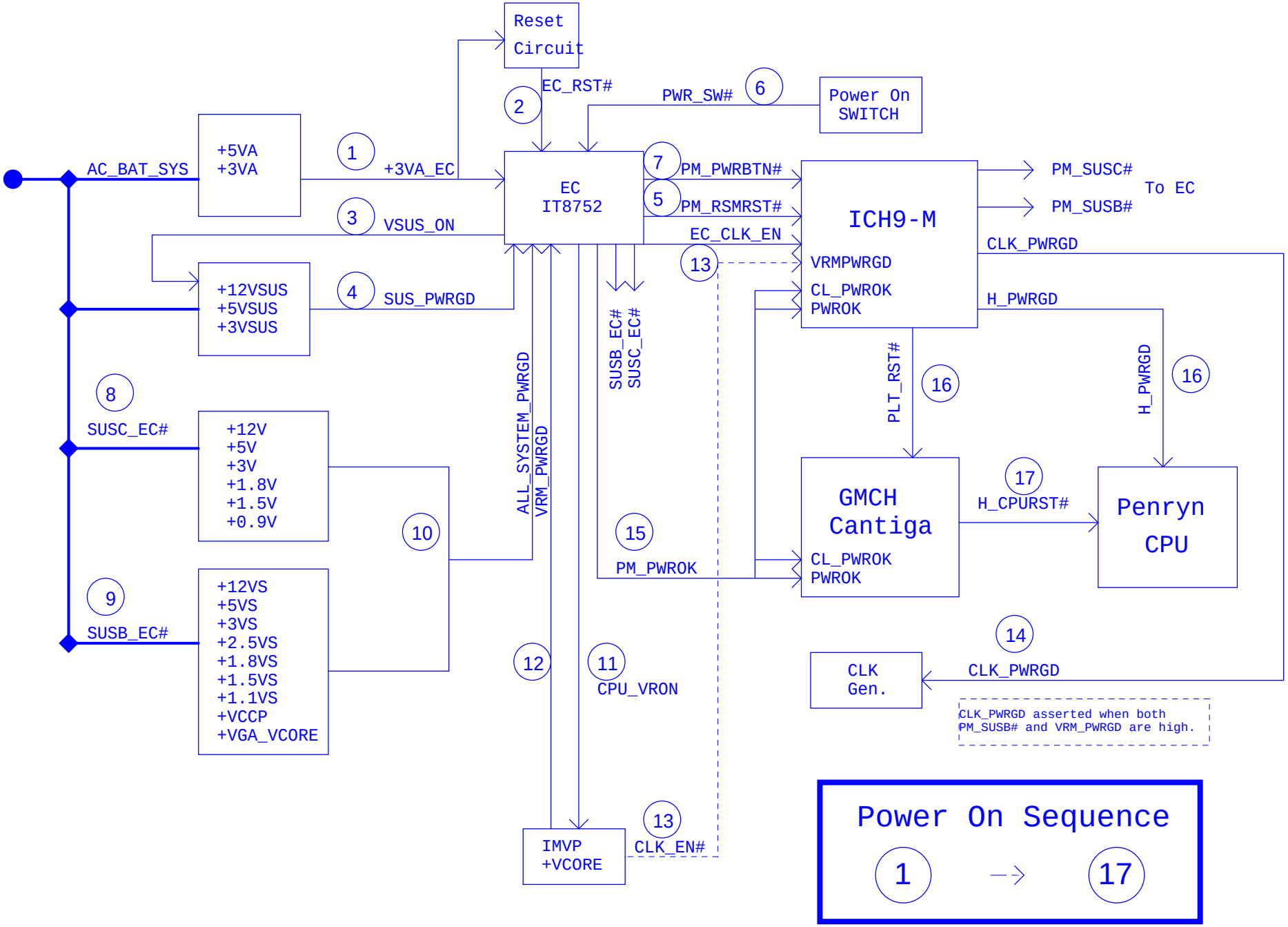
11/02



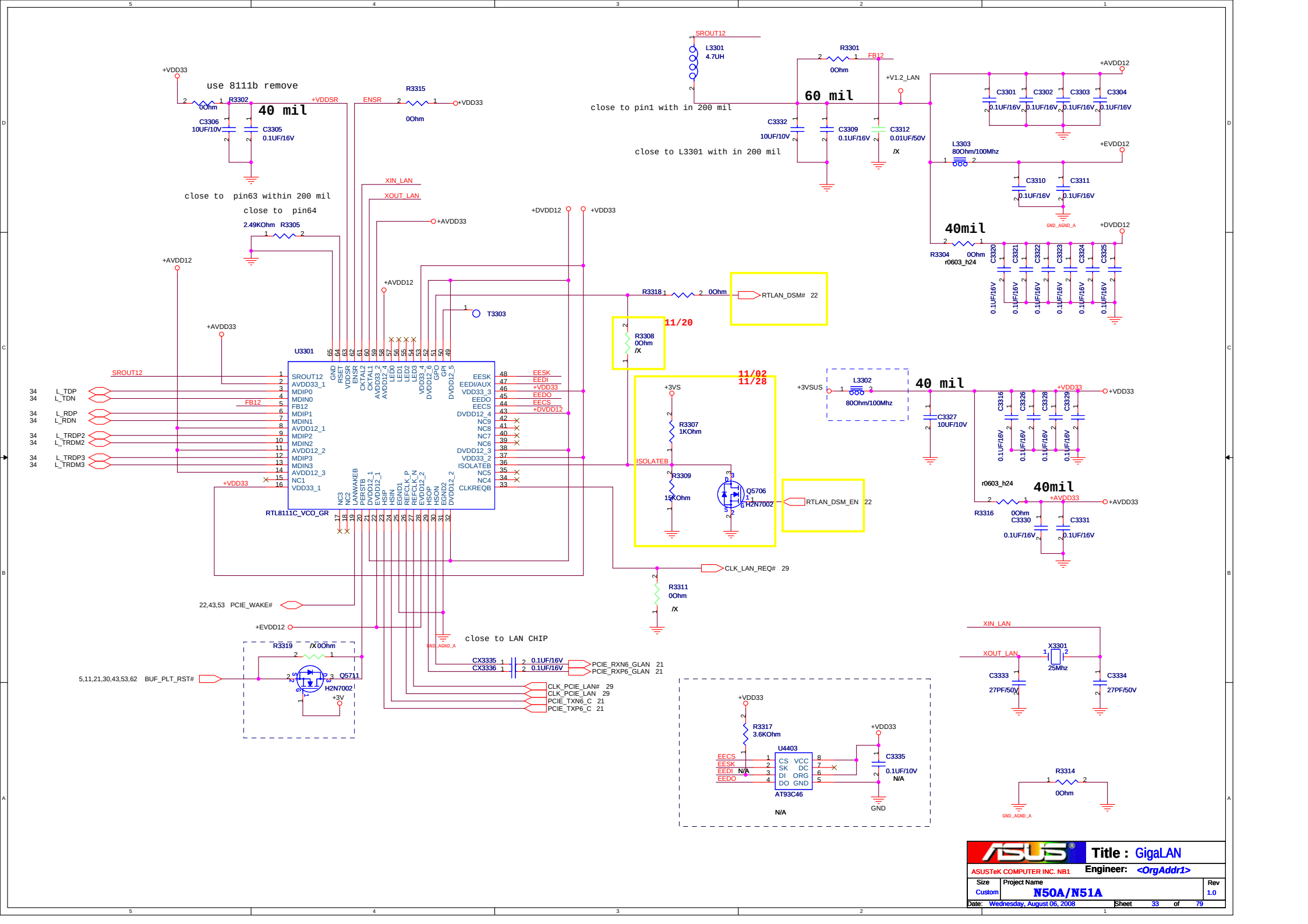


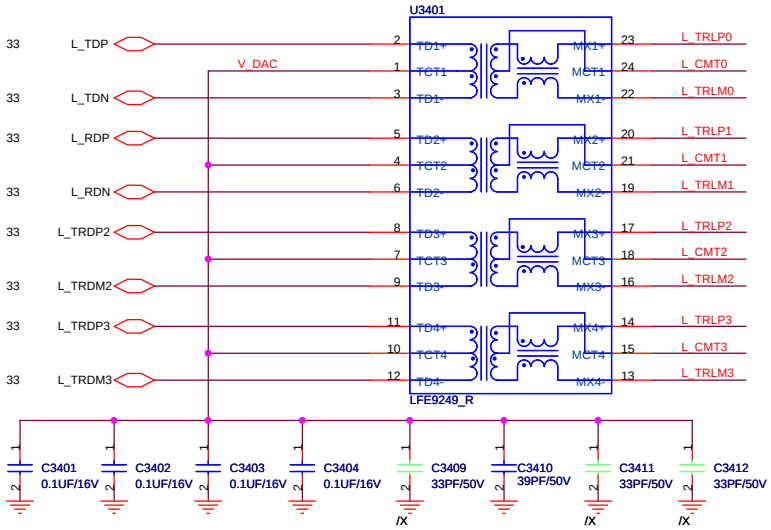
12G09103004P

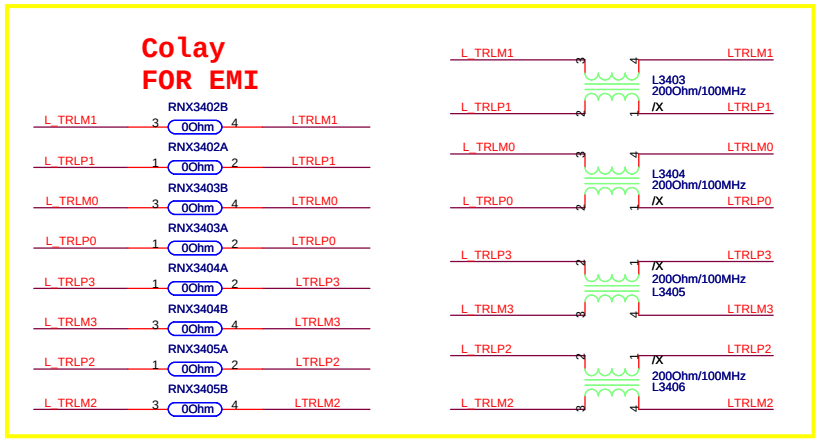
ASUSTeK COMPUTER INC. NB1	Title : EC_IT8511 (2/2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 31 of 79	

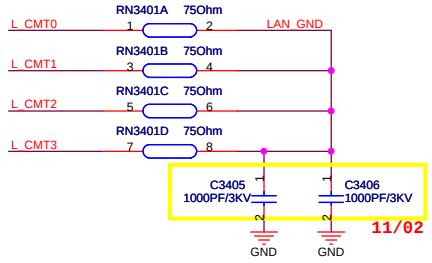


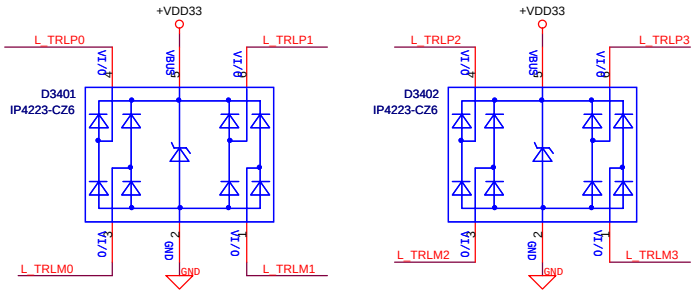
ASUSTeK COMPUTER INC. NB1	Title : POWER-ON SEQUENCE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 32 of 79	

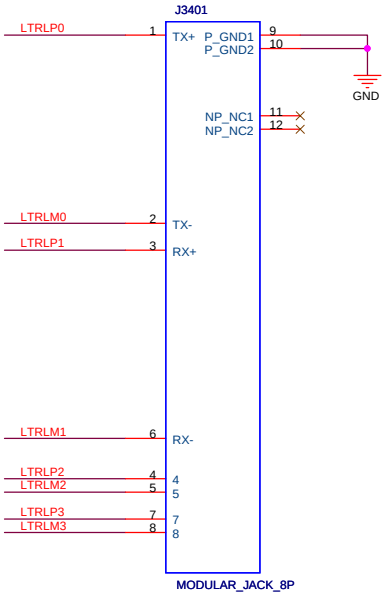

use 8111b remove
40 mil
close to pin1 with in 200 mil
60 mil
close to L3301 with in 200 mil
close to pin63 within 200 mil
close to pin64
close to LAN CHIP
40mil
11/20
11/02
11/28
RTL8111C_VCO_GR
U3301
U4403
AT93C46
Q5706
H2N7002
Q5711
T3303
X3301
25Mhz
Title : GigaLAN
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Wednesday, August 06, 2008
Sheet 33 of 79









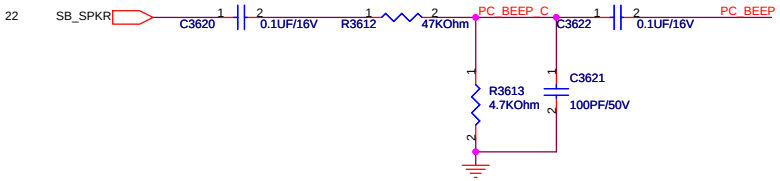


12G142111083

ASUSTeK COMPUTER INC. NB1	Title : RJ45	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 34 of 79	

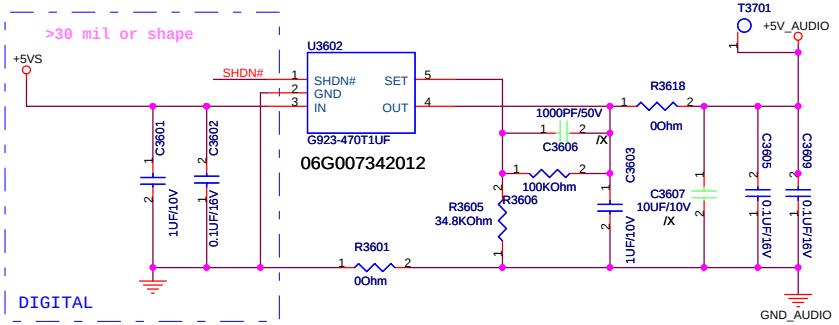
Title :	MDC
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 35 of 79

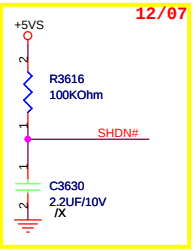
PC BEEP

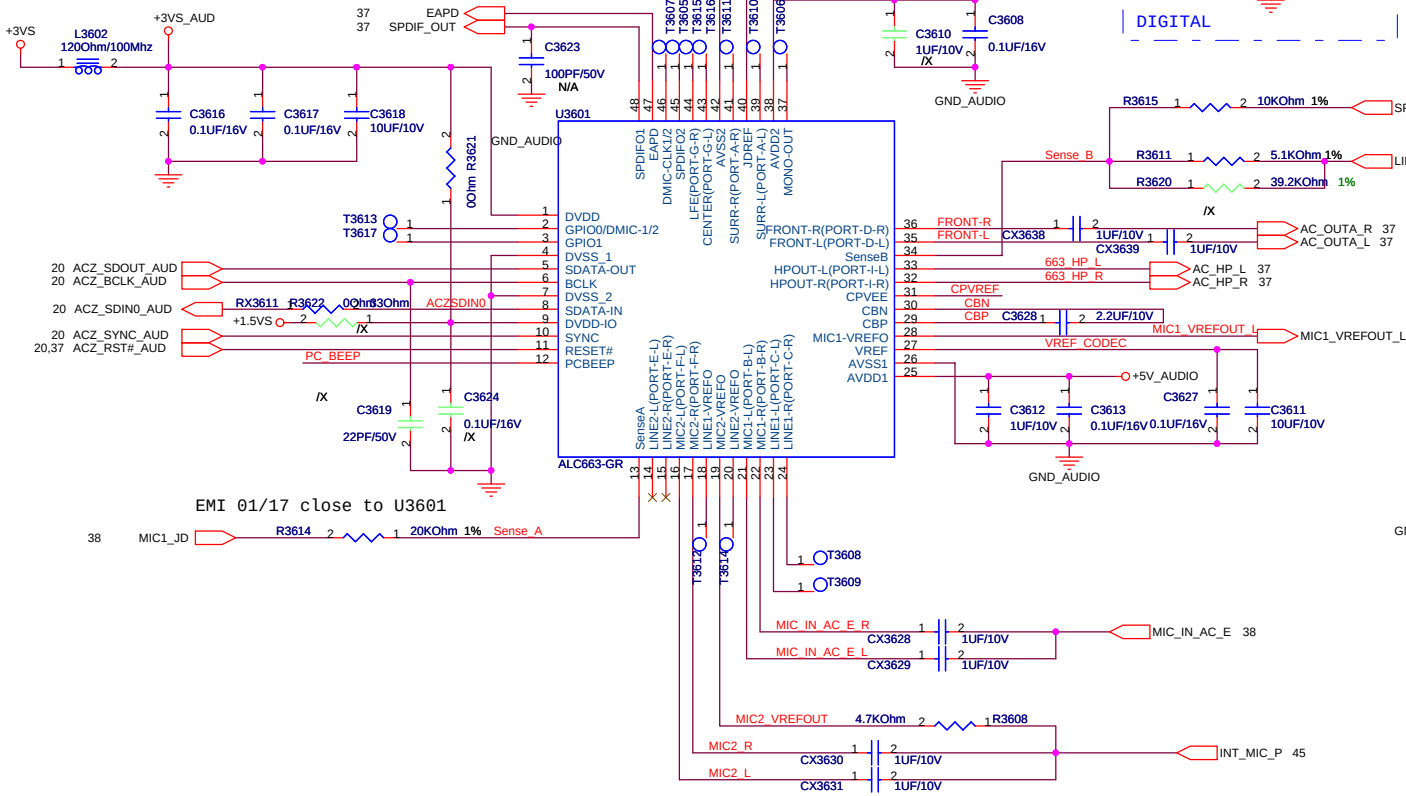


Audio Power

FOR ADJUST MODE:
Vo=1.25*(1+R3706/R3705)
= 1.25*(1+ 100K/34.8K) = 4.84





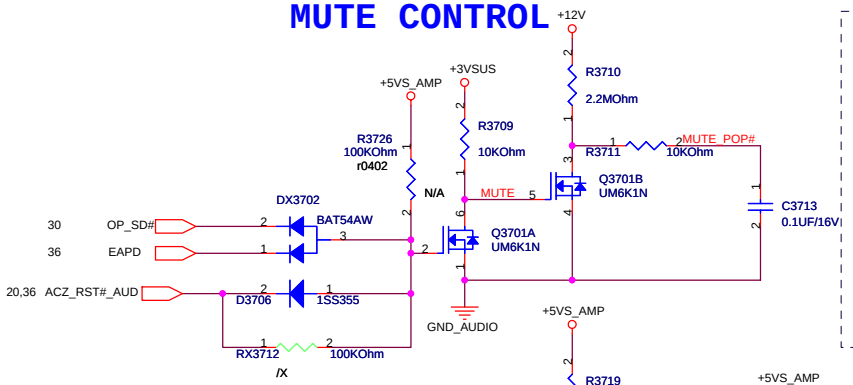


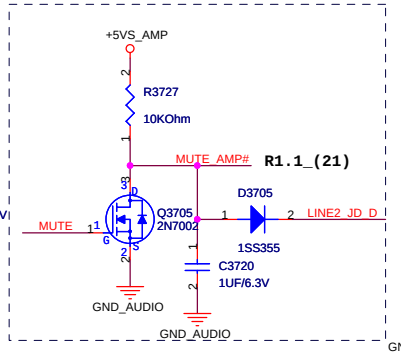
Input impedence:64K ohm(Typical)

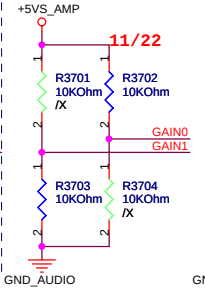
12/07 ALC663 CHARGE PUMP

ASUSTeK COMPUTER INC. NB1	Title : CODEC ALC663	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 36 of 79	

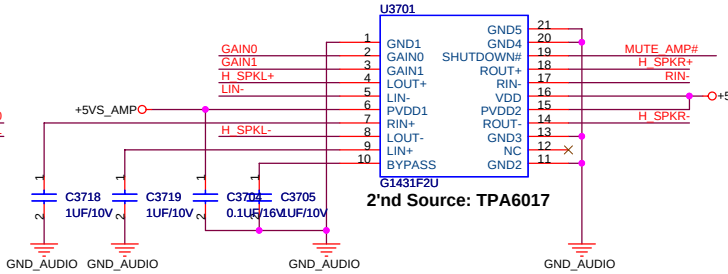
MUTE CONTROL



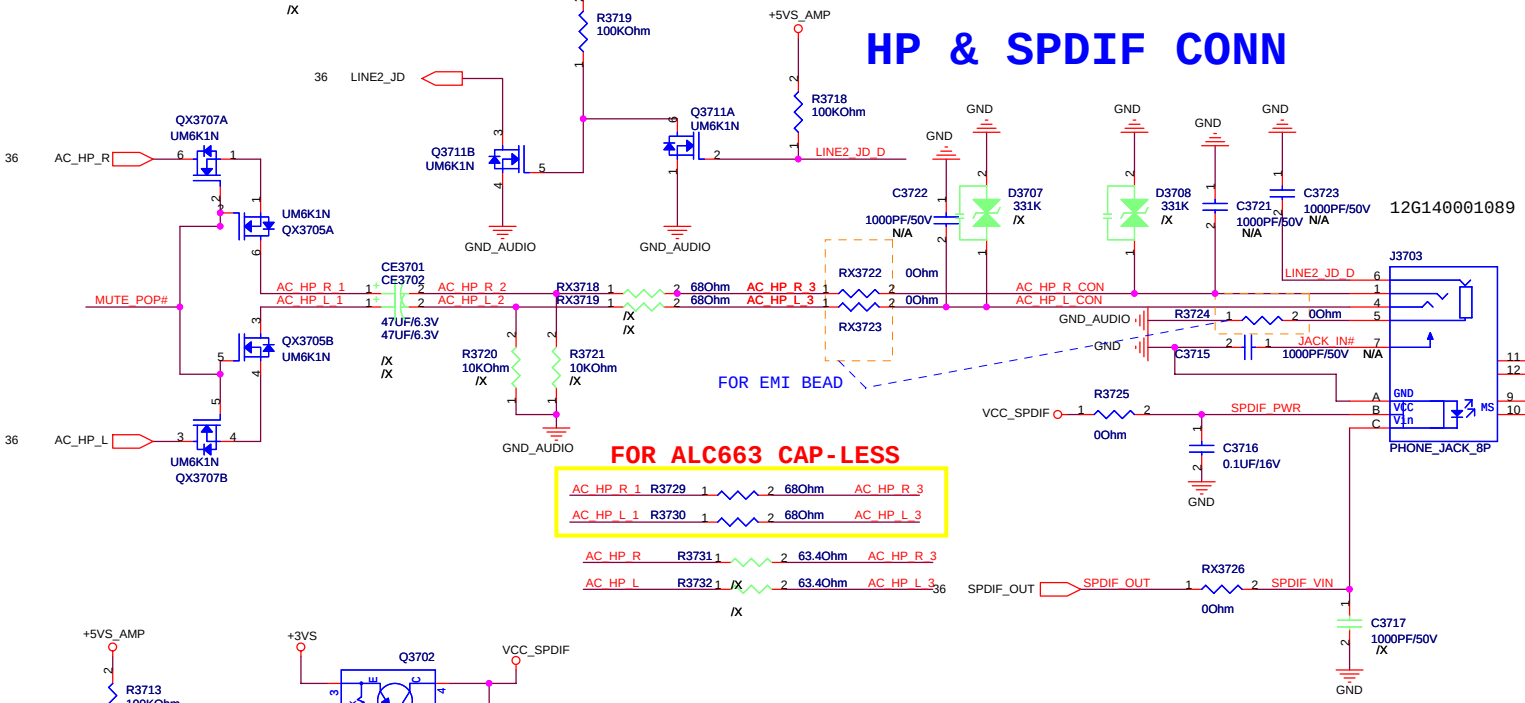




SPEAKER AMP

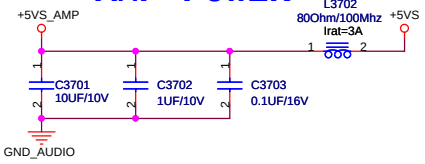


HP & SPDIF CONN

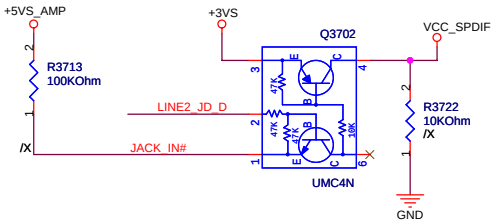


GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

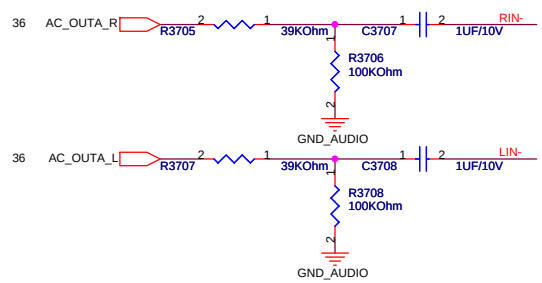
AMP POWER



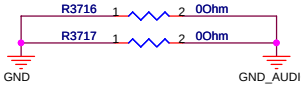
FOR ALC663 CAP-LESS

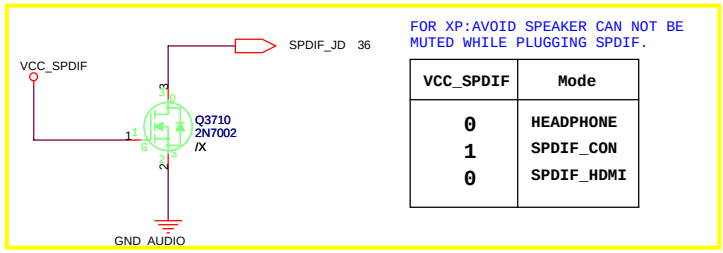


JACK_IN#	LINE2_JD_D	Mode
0	1	SPDIF_CON
0	0	HEADPHONE,SPDIF_HDMI
1	1	SPDIF_HDMI



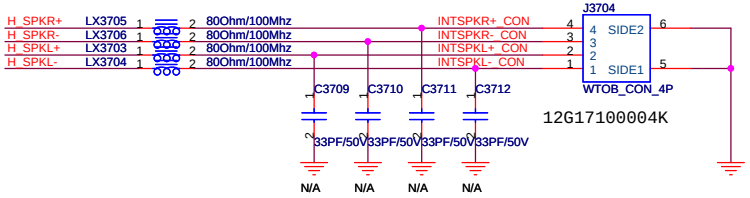
JACK GND

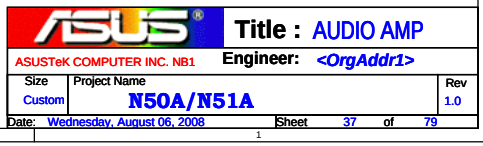




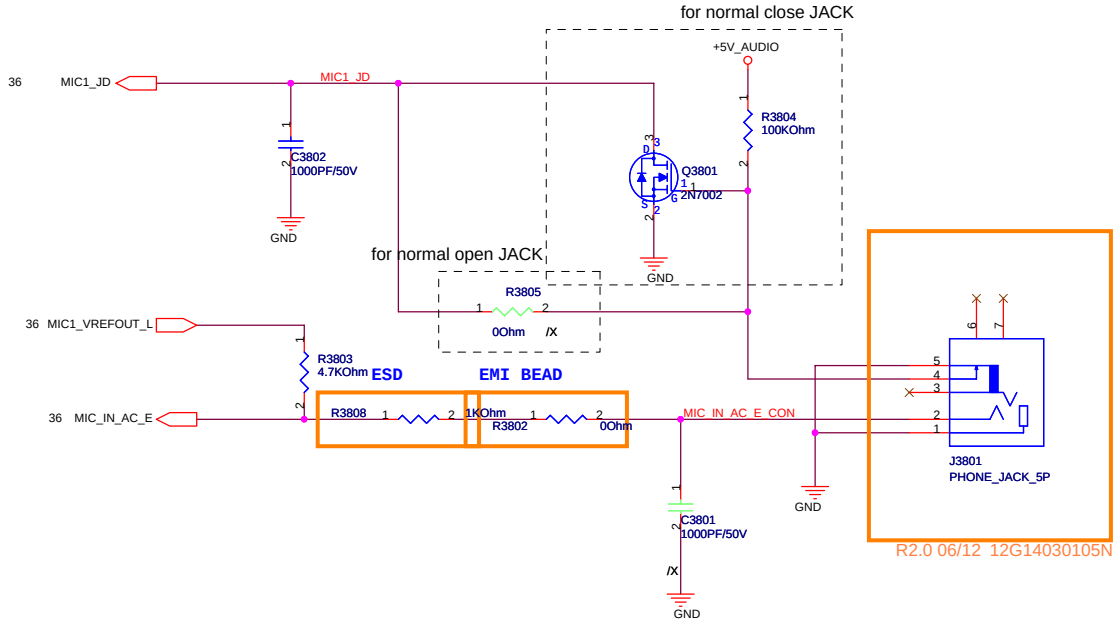
VCC_SPDIF	Mode
0	HEADPHONE
1	SPDIF_CON
0	SPDIF_HDMI

SPEAKER CONNECTOR(2W)



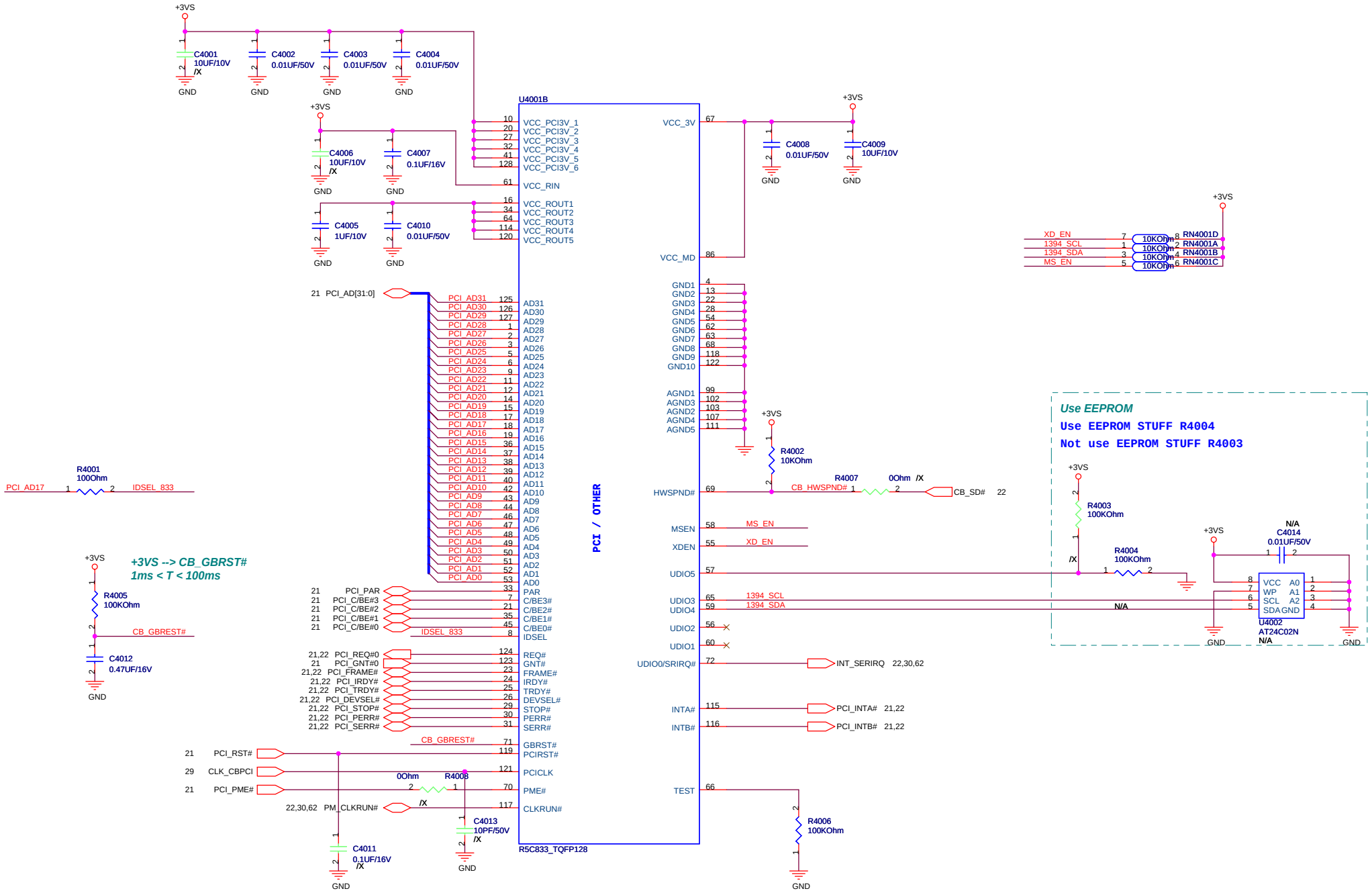


EXTERNAL MICROPHONE

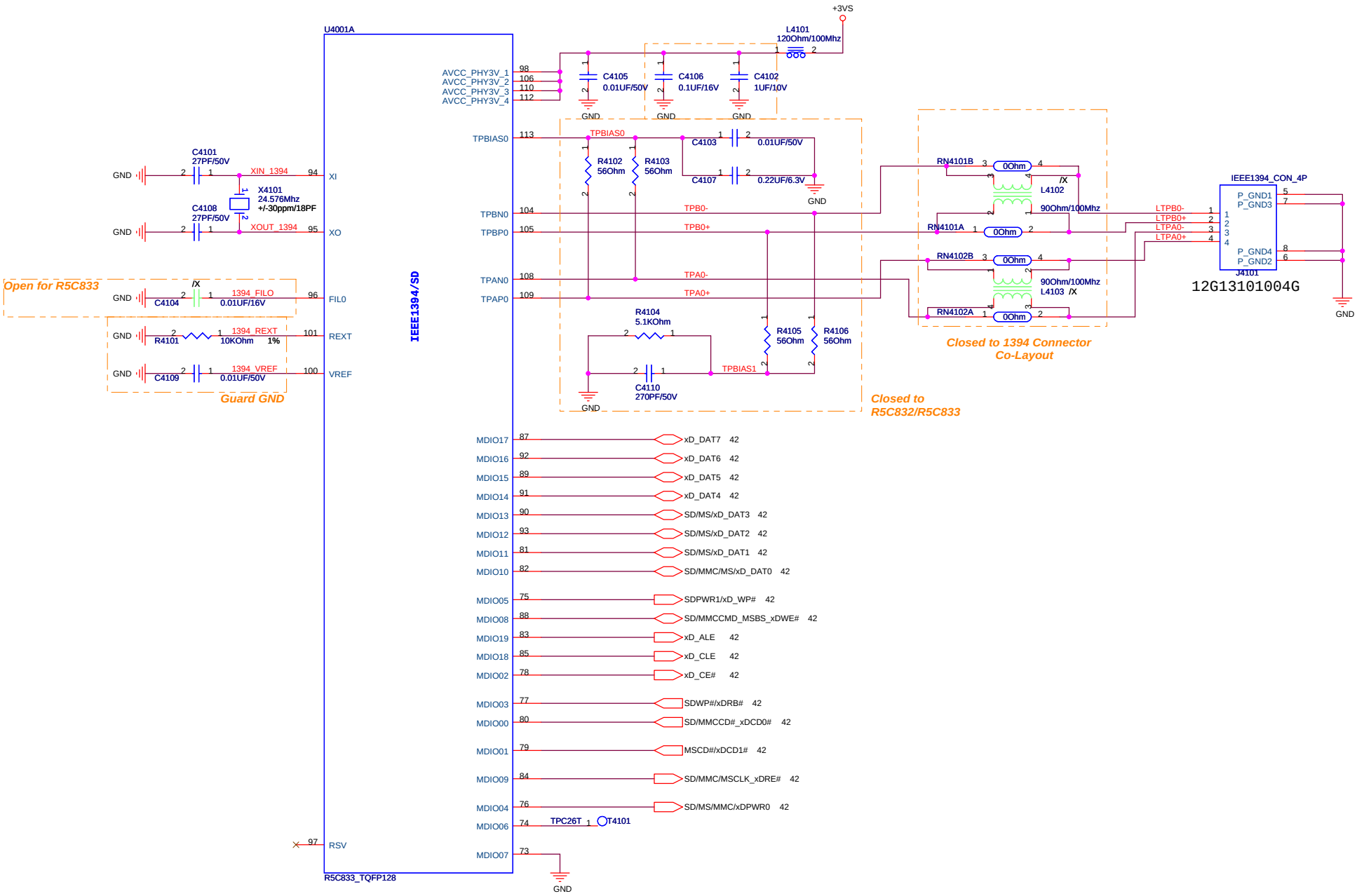


ASUSTeK COMPUTER INC. NB1	Title : MIC&LINEIN		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Friday, August 01, 2008	Sheet 38 of 79		

ASUSTeK COMPUTER INC. NB1	Title : DSP		
	Engineer: <OrgAddr1>		
Size: A	Project Name: N50A/N51A		Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 39 of 79		

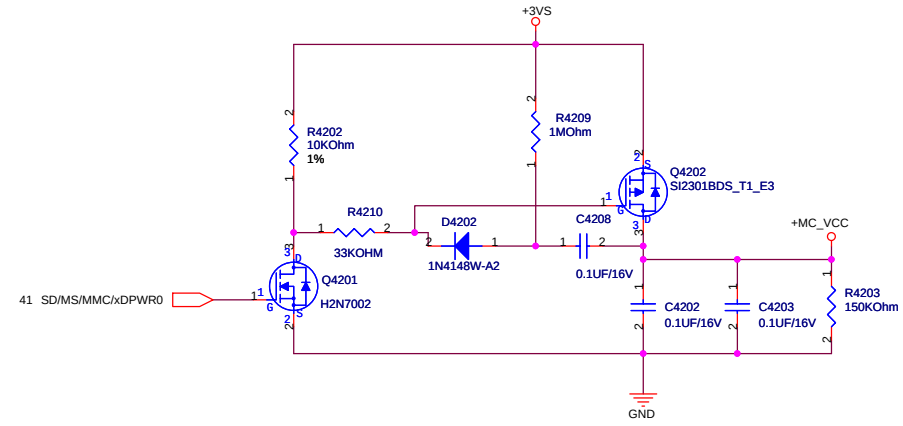


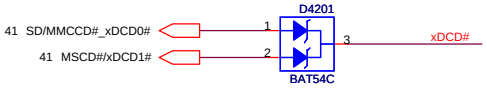
ASUSTeK COMPUTER INC. NB1	Title : CARDBUS R5C833 (1)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Tuesday, August 12, 2008	Sheet 40 of 79		

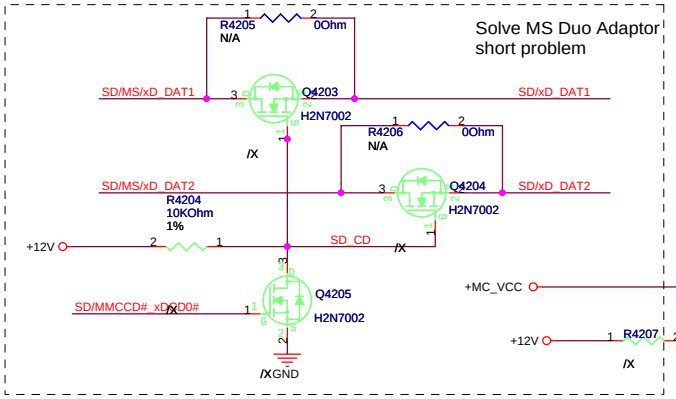


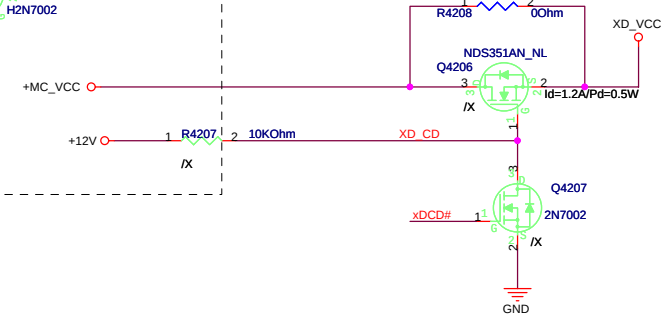
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, August 07, 2008	Sheet 41 of 79	

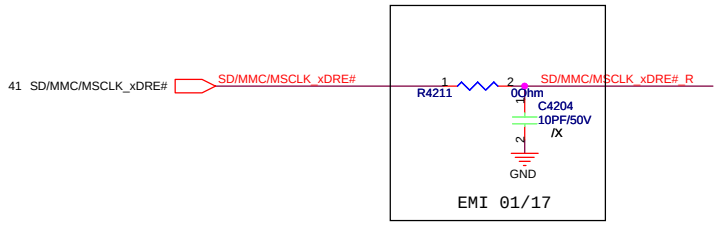
Title :CARDBUS R5C833 (2)

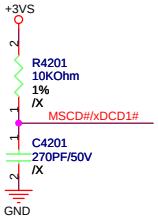


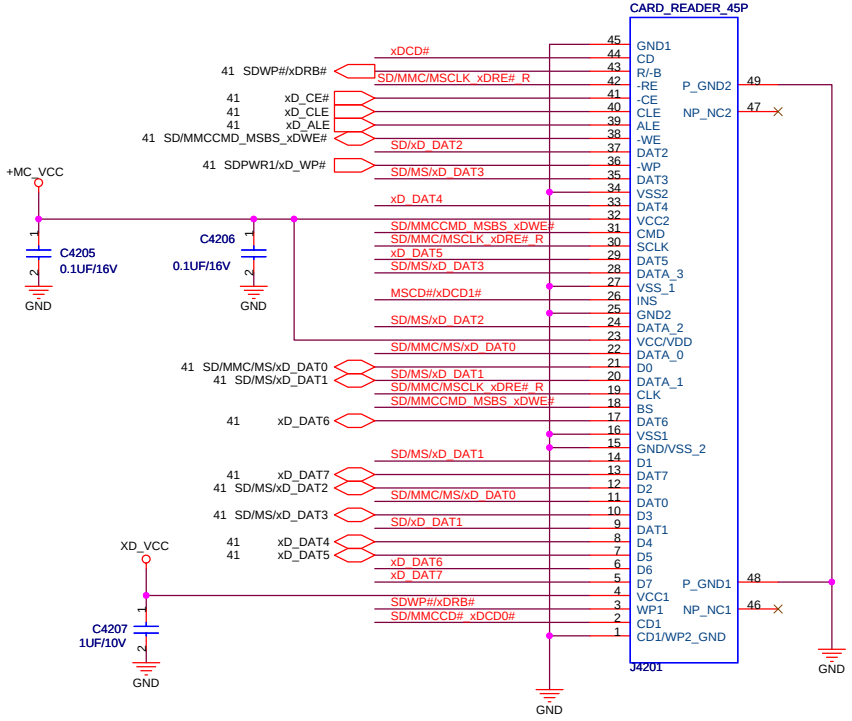












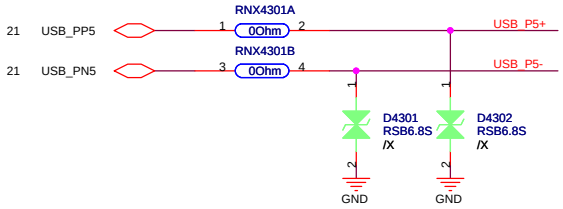
ASUSTeK COMPUTER INC. NB1

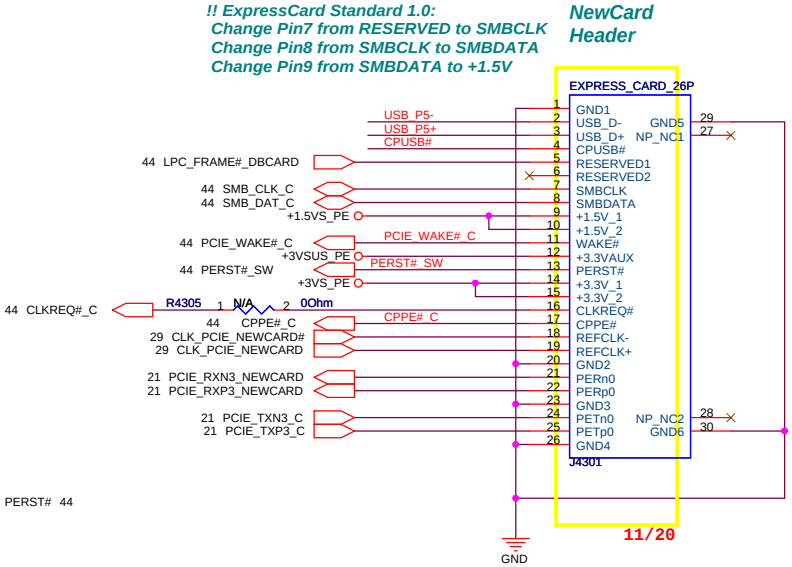
Title : 1394&CardReader CON

Engineer: <Enginner Name>

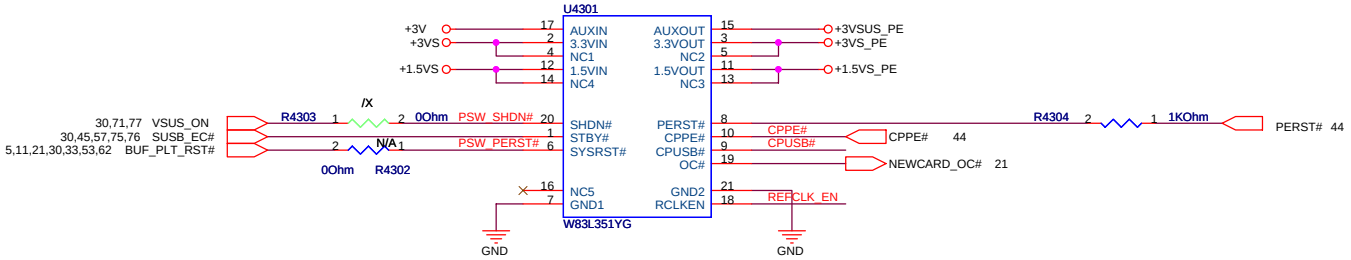
Size	Project Name	Rev
Custom	N50A/N51A	1.0

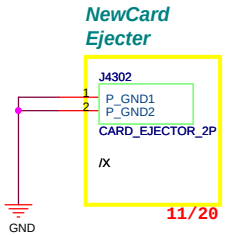
Date: Monday, August 11, 2008 Sheet 42 of 79





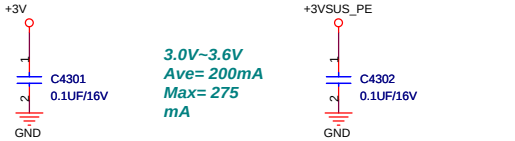
1st source:06G030091010

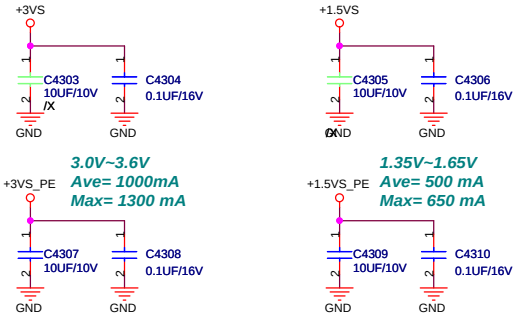


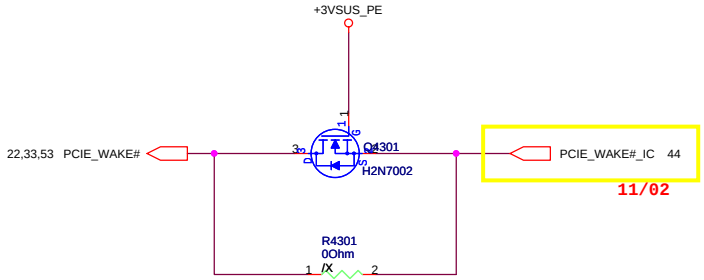


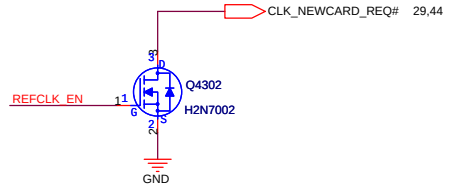
12G161300261

12G21C102604



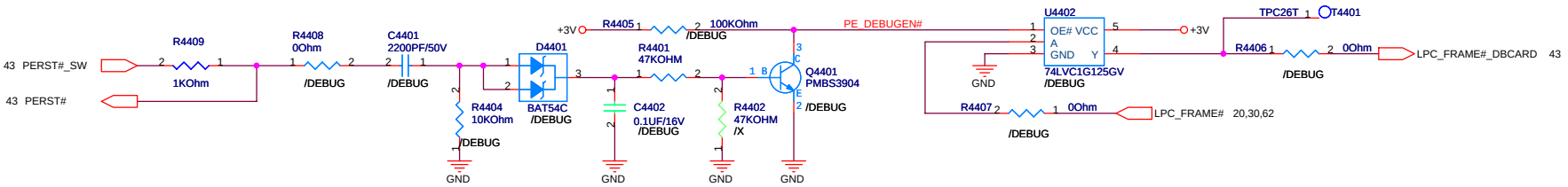


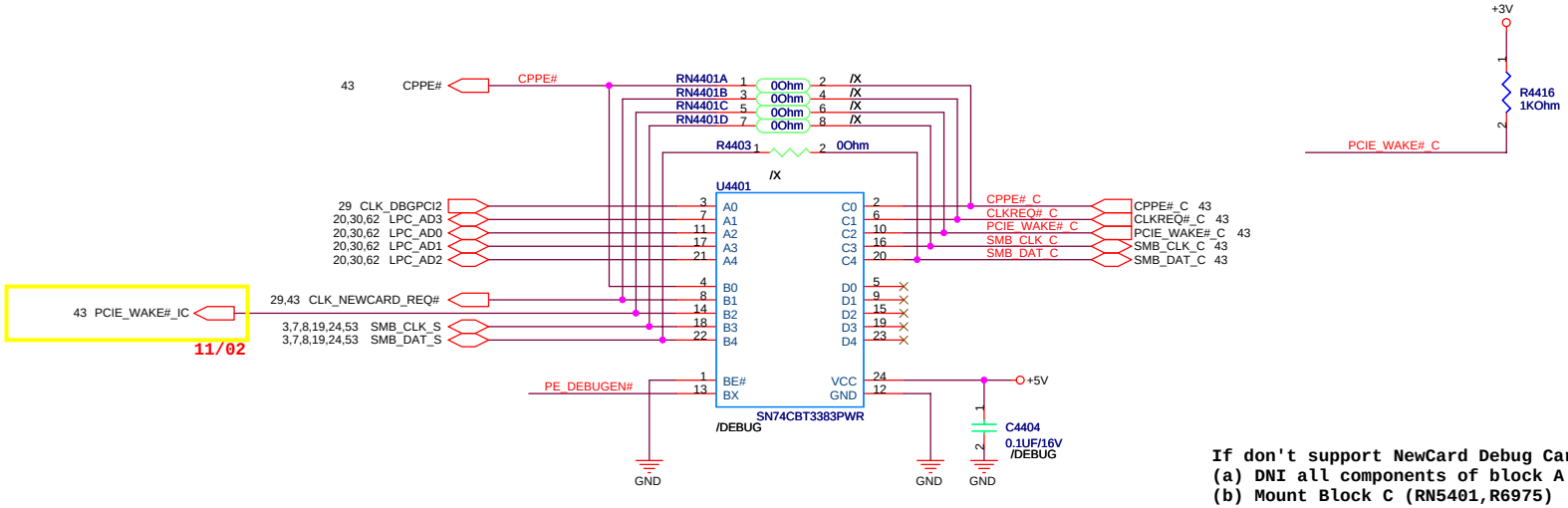




ASUSTeK COMPUTER INC. NB1	Title : NEW CARD	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 43 of 79	

Block A

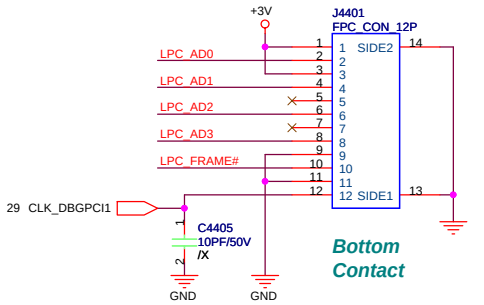


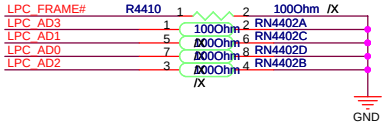


If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.





ASUSTeK COMPUTER INC. NB1

Title : DEBUG

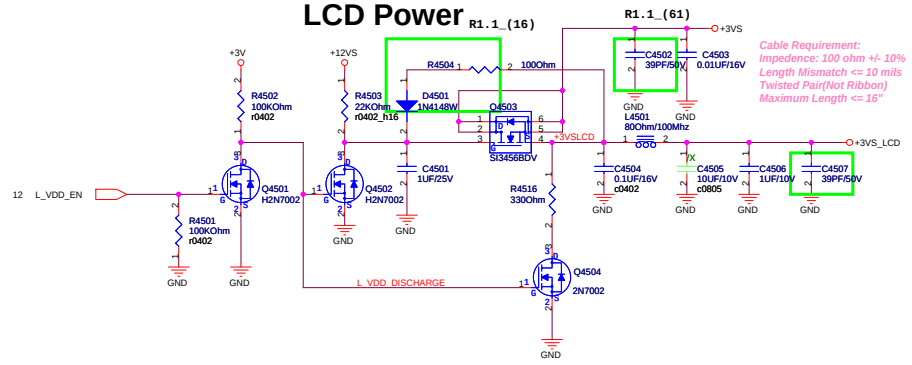
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Monday, August 04, 2008 Sheet 44 of 79

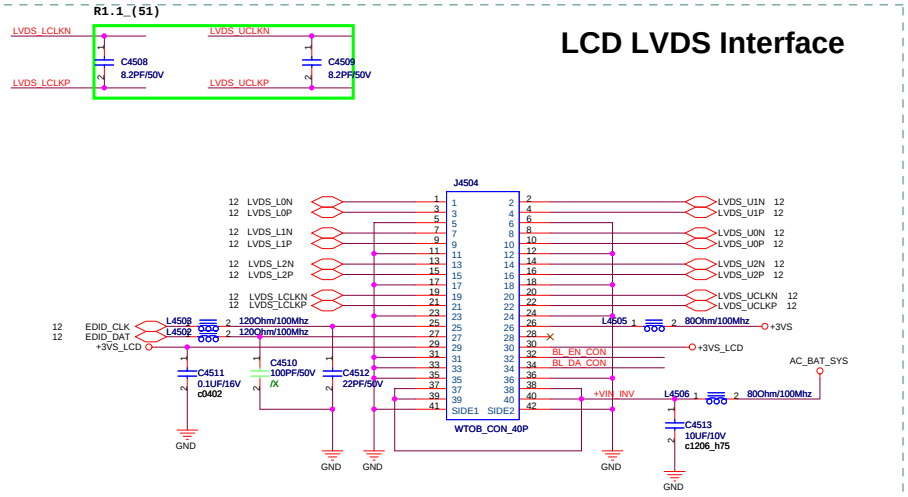
LCD Backlight Control

LCD Power

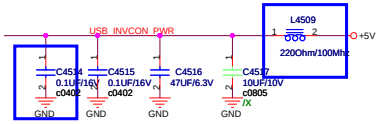


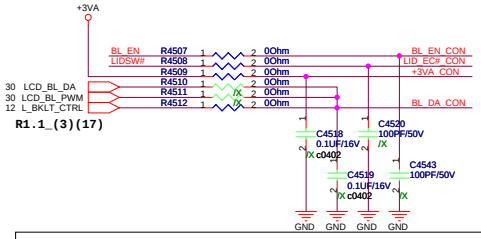
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

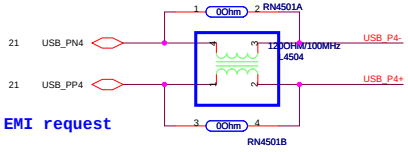
LCD LVDS Interface



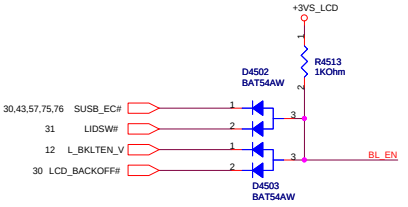
Inverter Interface/Speaker CONN.

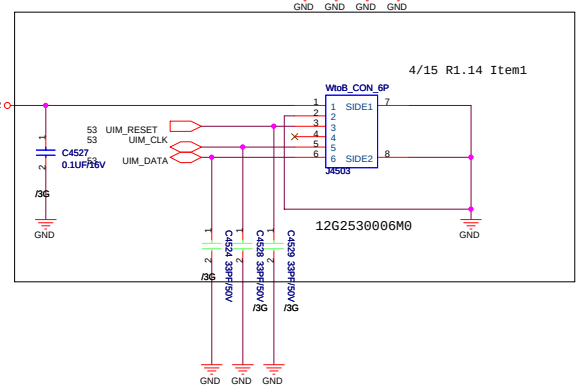


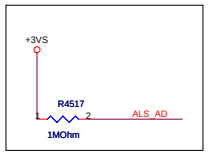


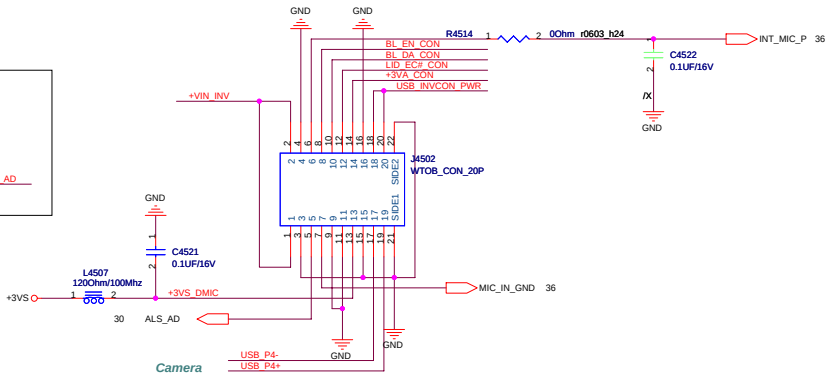


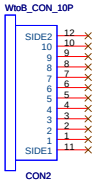
R1.1_(59) change for EMI request



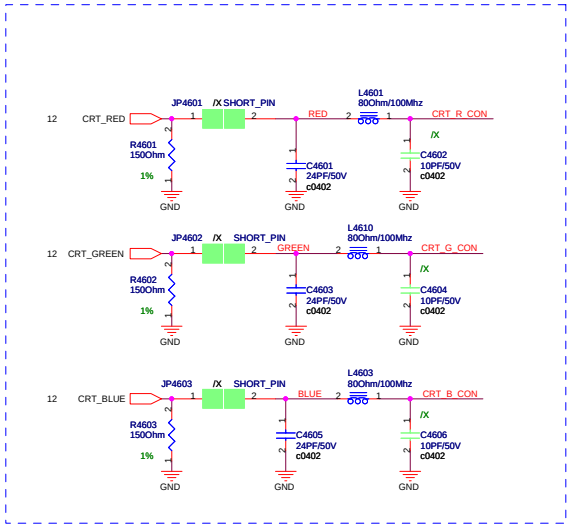


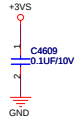




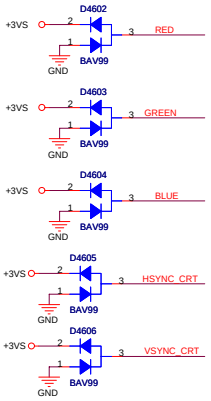


ASUSTeK COMPUTER INC. NB1	Title : LVDS	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50A/N51A	Rev: 1.0
Date: Monday, August 11, 2008	Sheet 45 of 79	

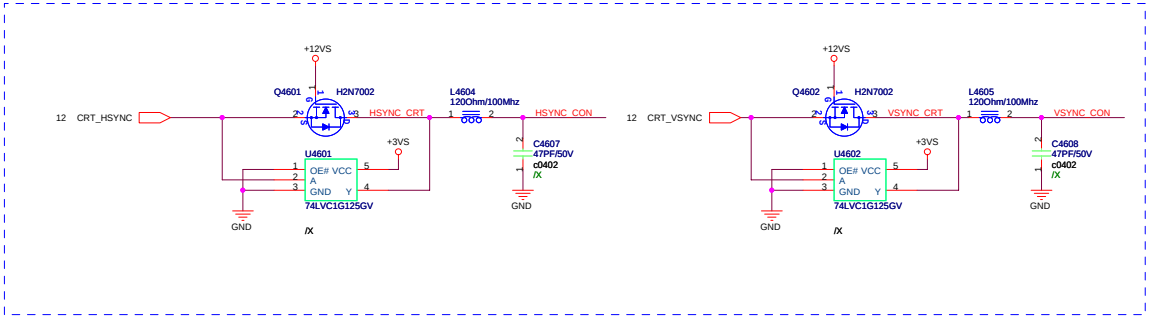


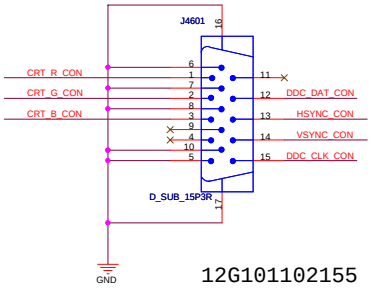


Place a 0.1uF CAP across the ESD Diode close

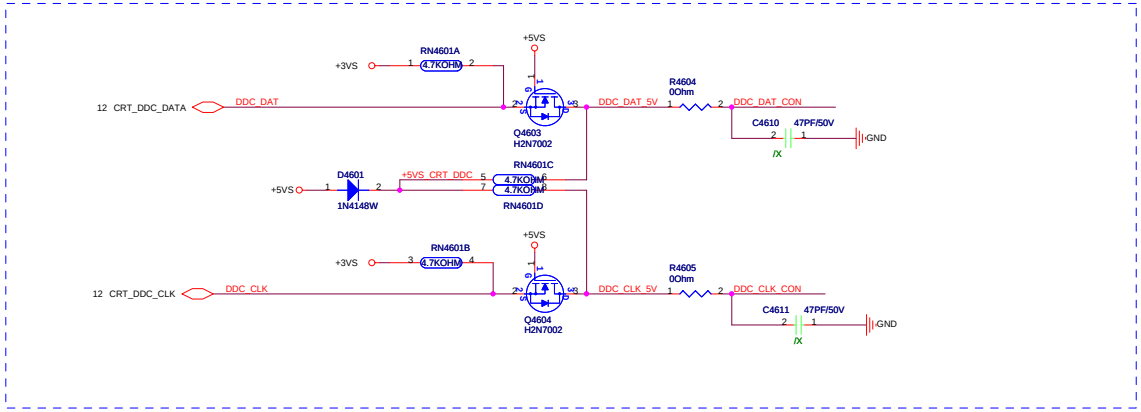


PLACE ESD Diodes near VGA port



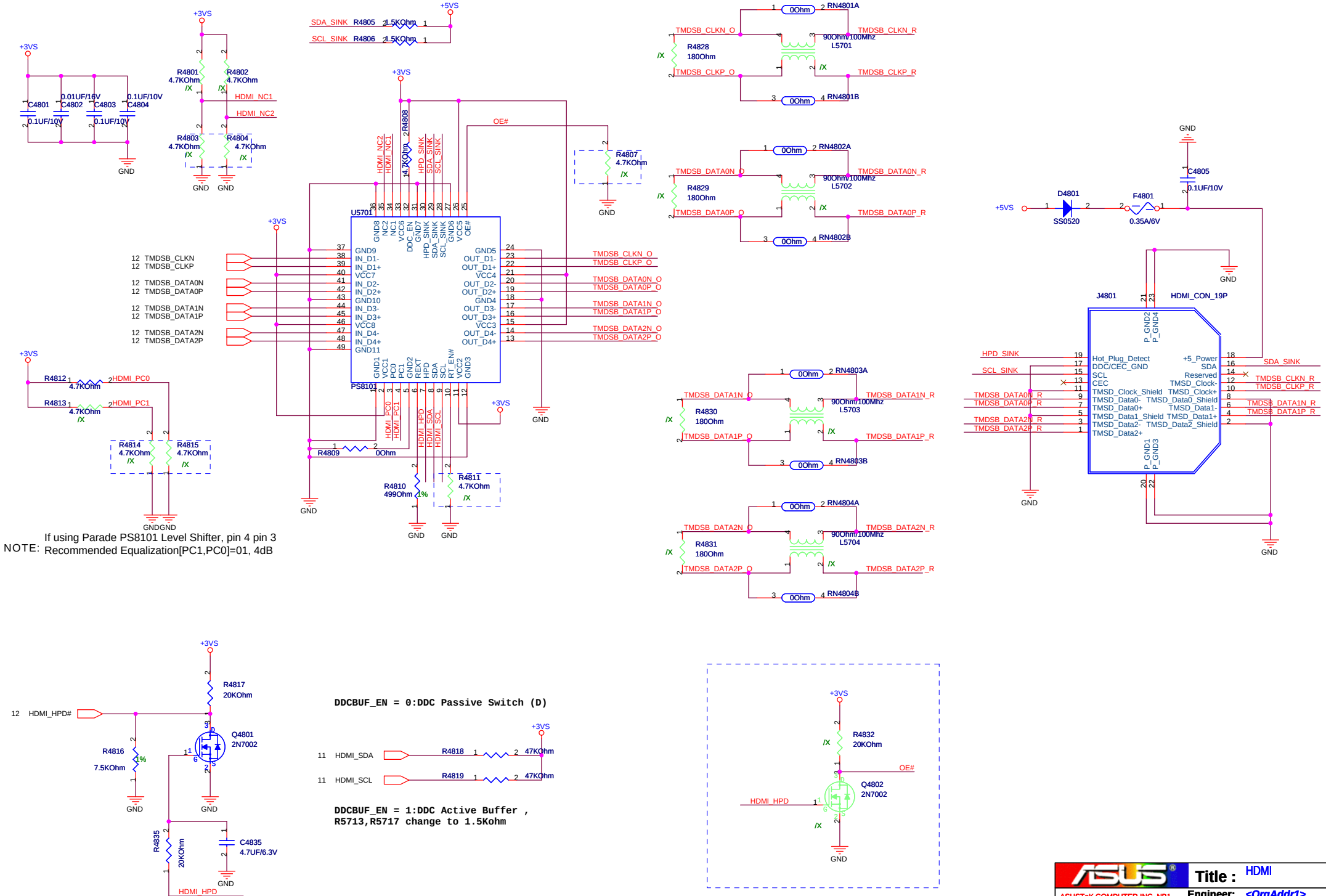


12G101102155



ASUSTeK COMPUTER INC. NB1	Title : CRT	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 46 of 79	

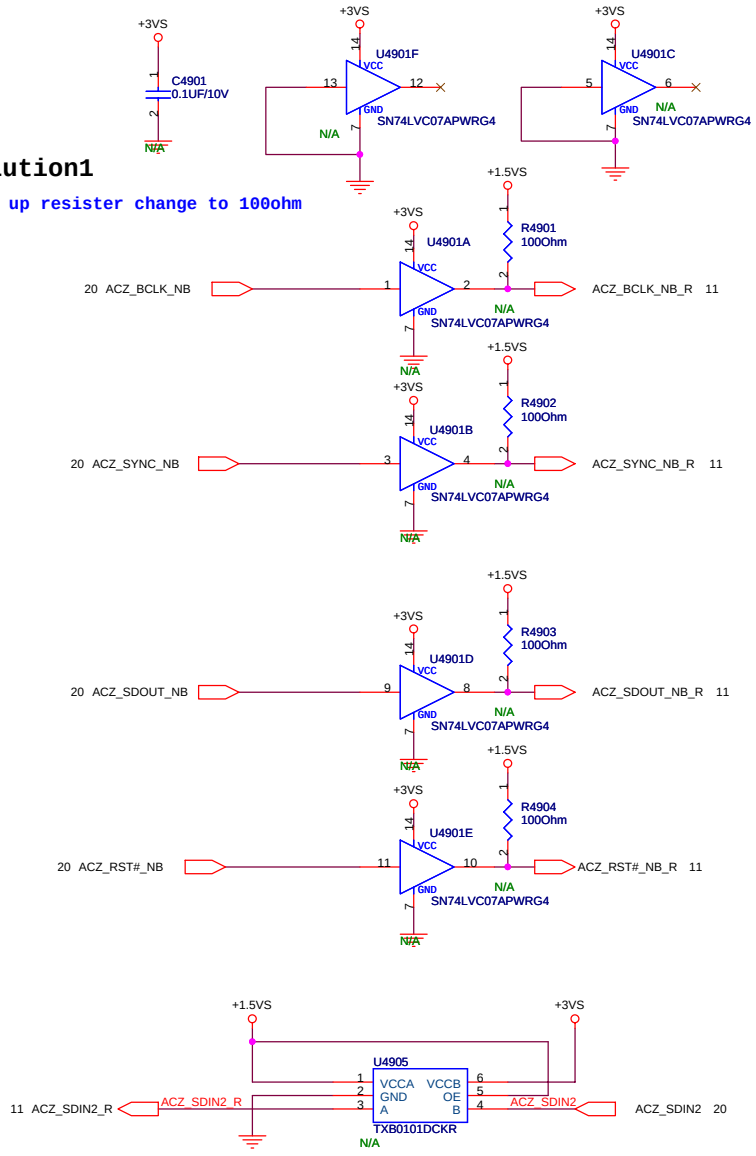
Title : DVI	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 47 of 79



ASUSTeK COMPUTER INC. NB1	Title : HDMI	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 48 of 79	

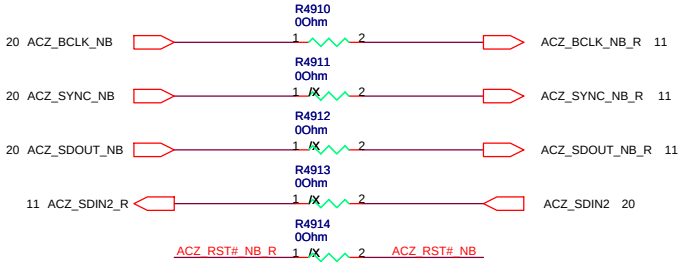
Solution1

pull up resister change to 100ohm



Solution2

for 1.5V HDA



/X

ASUSTeK COMPUTER INC. NB1

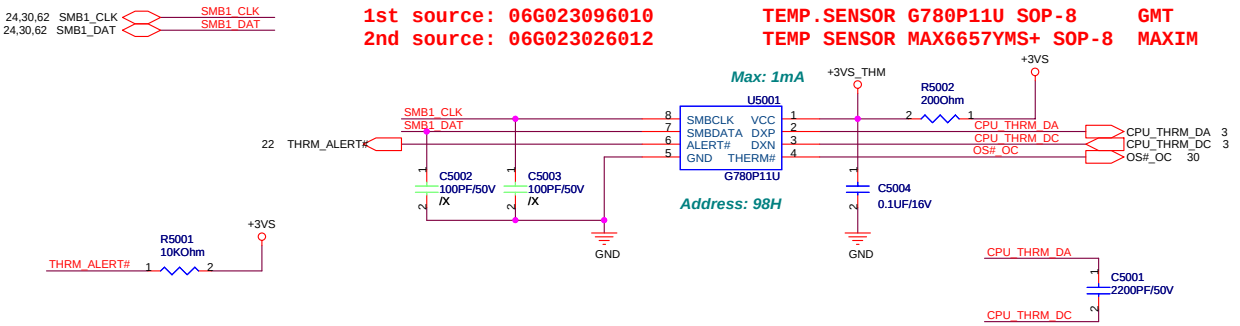
Title :

Engineer: <OrgAddr1>

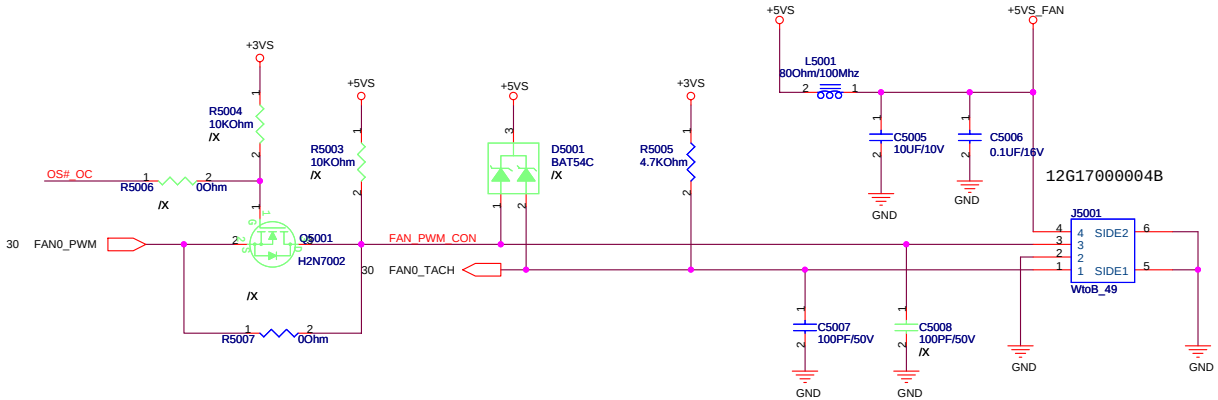
Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 49 of 79

Thermal Sensor

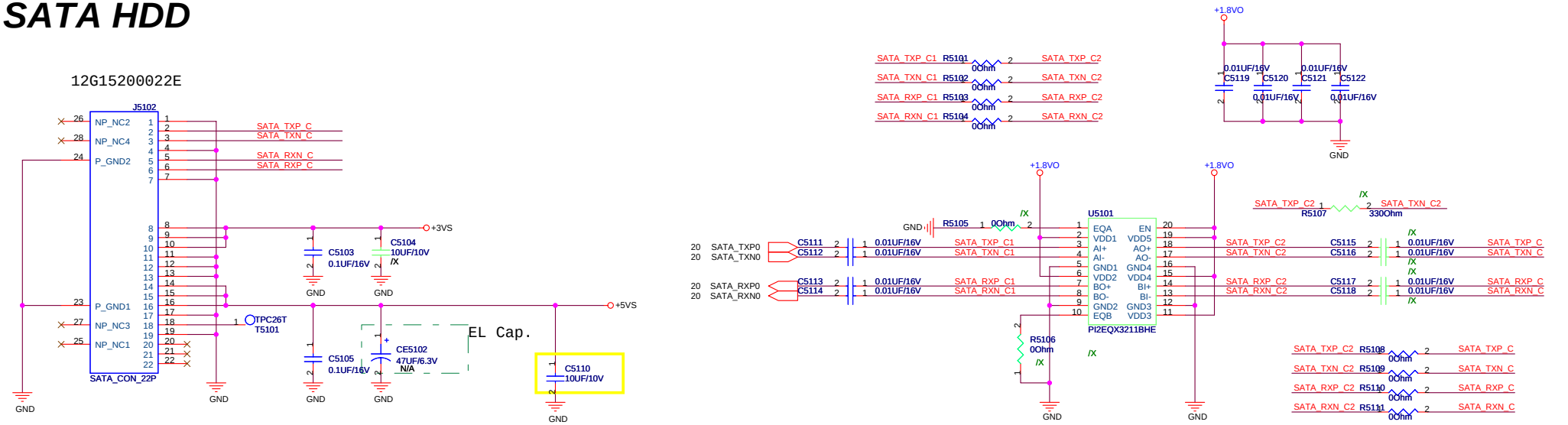


DC FAN Control

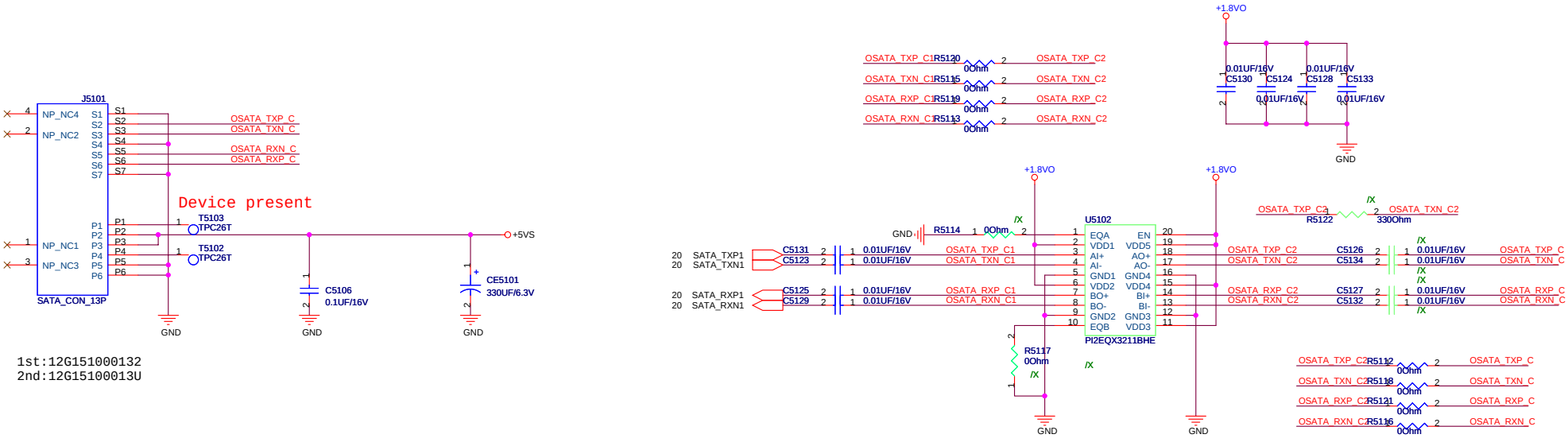


ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 50 of 79		

SATA HDD

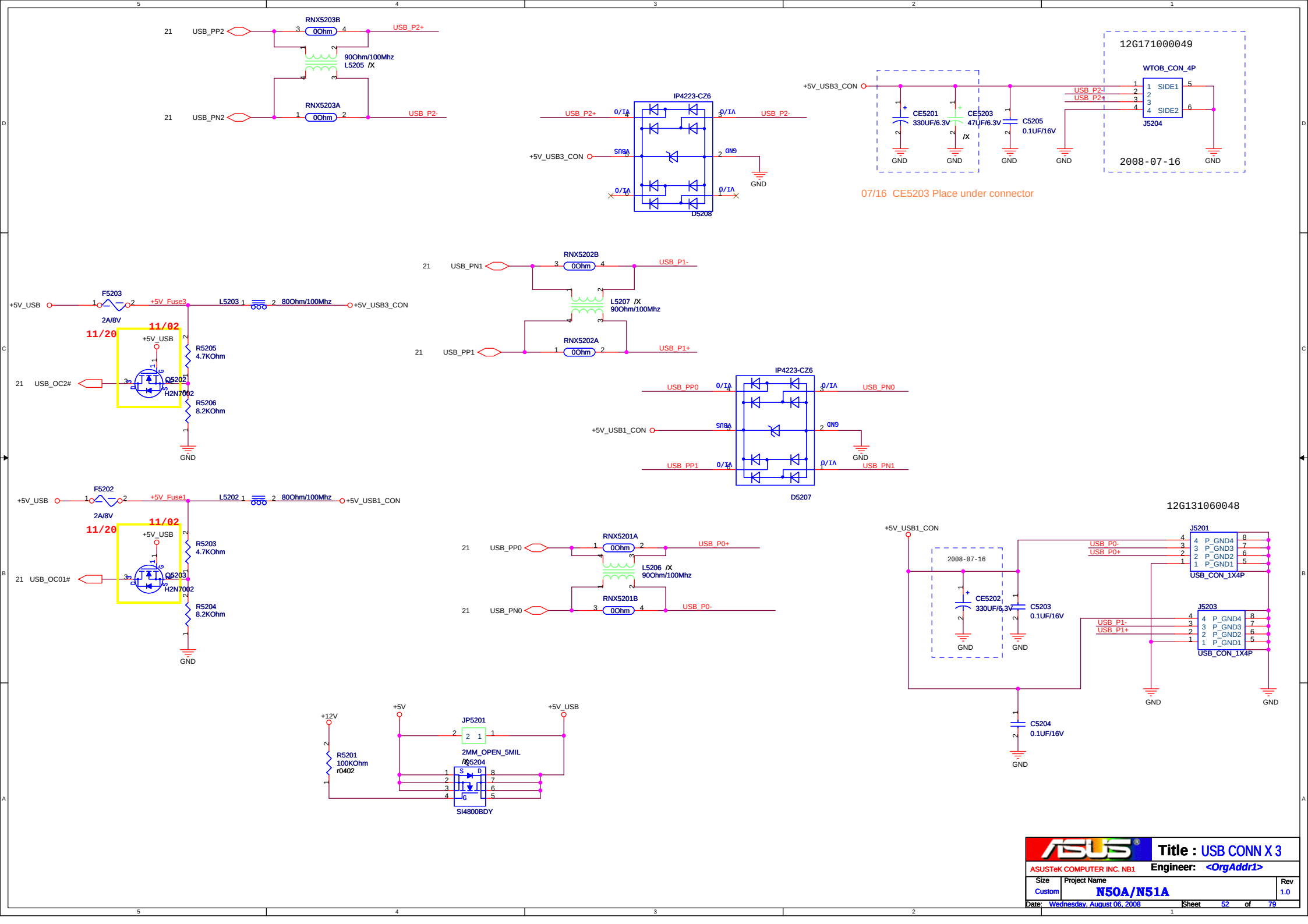


ODD

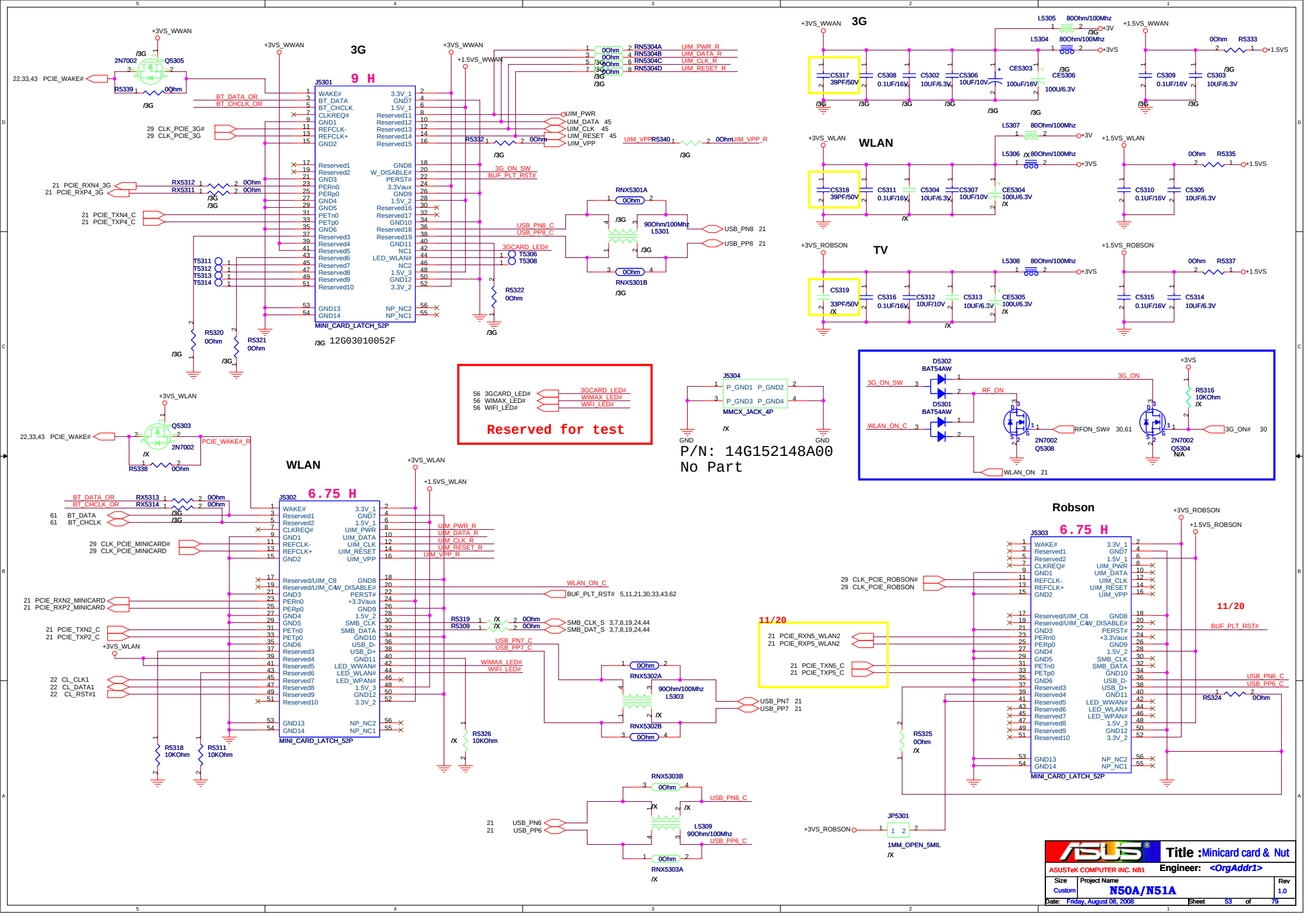


1st:12G151000132
2nd:12G15100013U

ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 51 of 79	



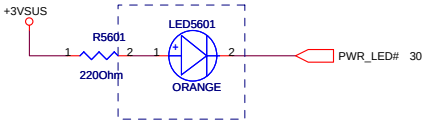
ASUSTeK COMPUTER INC. NB1	Title : USB CONN X 3		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 52 of 79		


3G
J5301
9 H
MINI_CARD_LATCH_52P
12G03010052F
WLAN
J5302
6.75 H
MINI_CARD_LATCH_52P
Reserved for test
P/N: 14G152148A00
No Part
Robson
J5303
6.75 H
MINI_CARD_LATCH_52P
11/20
TV
Title :Minicard card & Nut
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
N50A/N51A
Date: Friday, August 08, 2008
Sheet 53 of 79

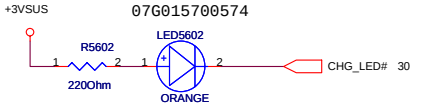
Title :	Port Docking
ASUSTeK COMPUTER INC. NB1	Engineer: *<OrgAddr1>*
Size: A	Project Name: **N50A/N51A**
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 54 of 79

Title :	Super I/O & FIR
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 55 of 79

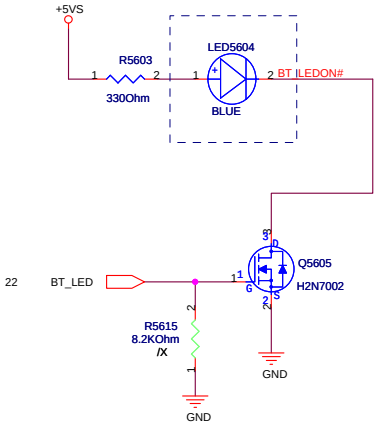
For Power LED



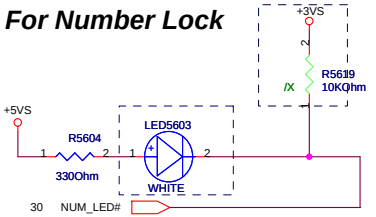
For Battery LED



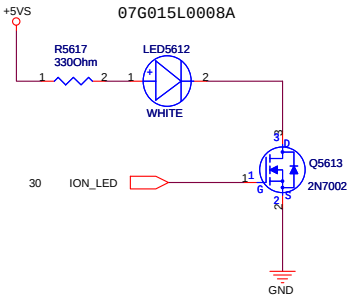
For BT LED



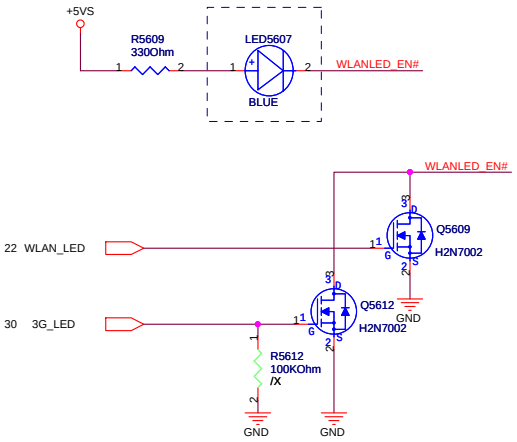
For Number Lock



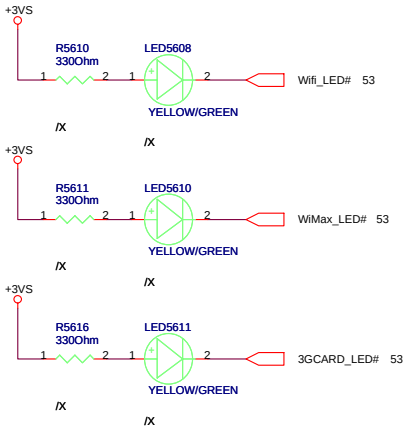
For Ionizer



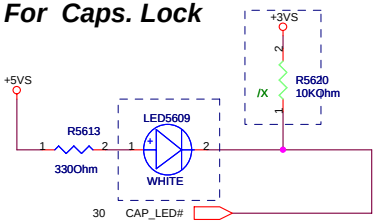
For WireLess LED



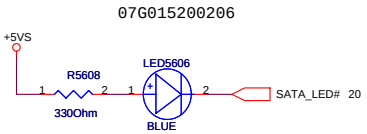
LEDs for testing

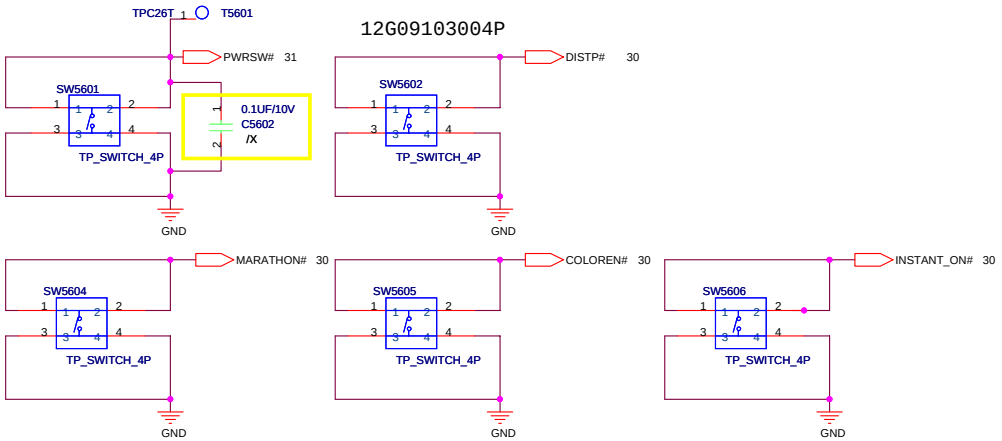


For Caps. Lock

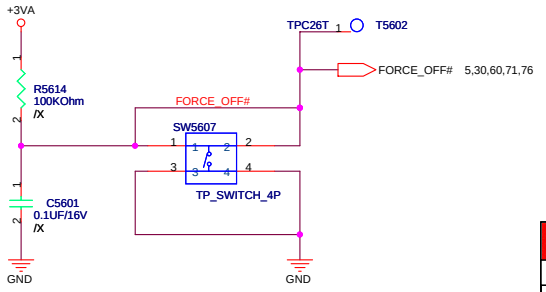


For SATA/IDE LED

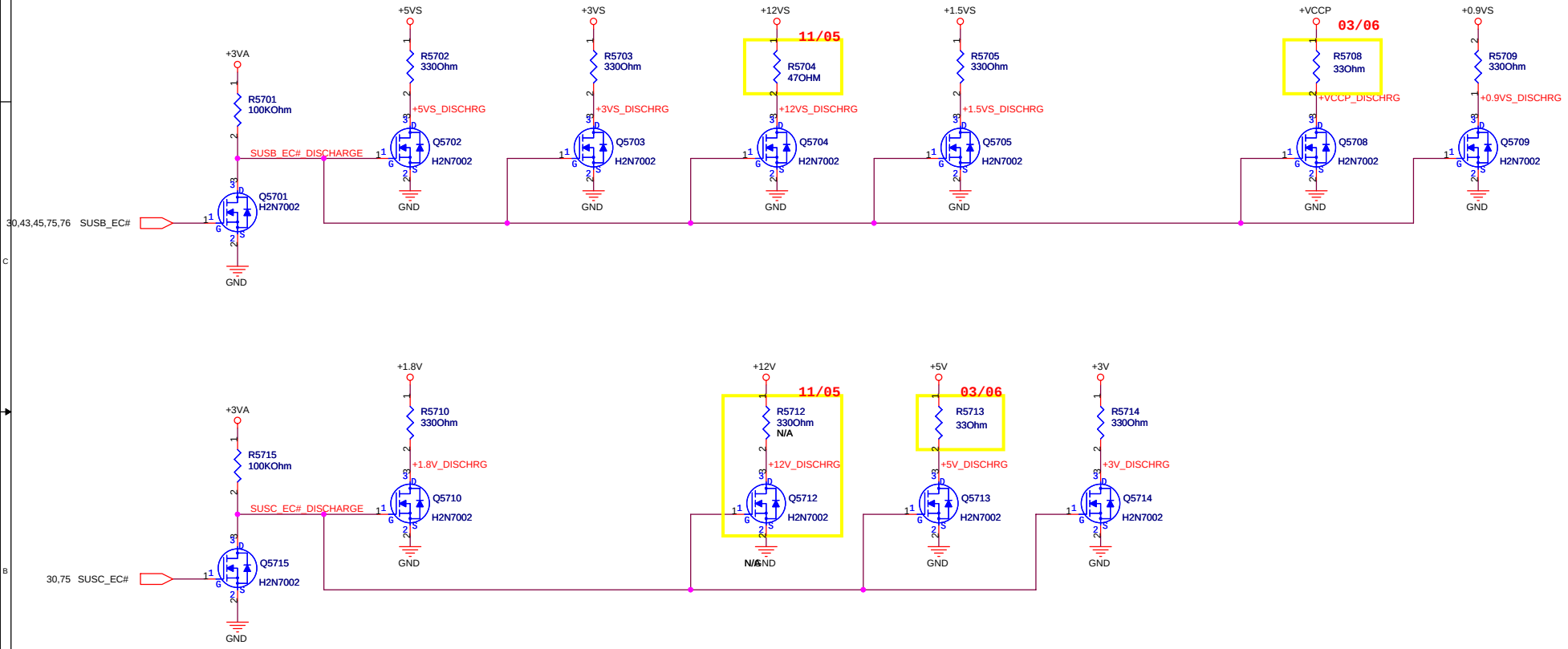




SHUT_DOWN#



ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 56 of 79	



ASUSTeK COMPUTER INC. NB1

Title : DISCHARGE

Engineer: <OrgAddr1>

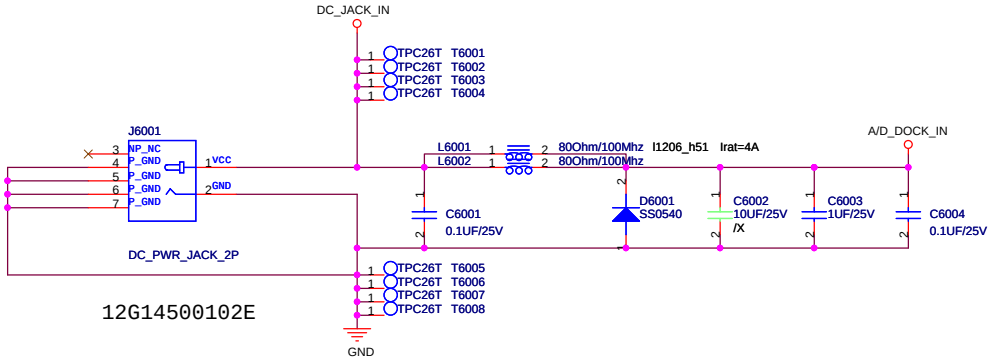
Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Wednesday, August 06, 2008 Sheet 57 of 79

Title :	UWB Minicard card
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: N50A/N51A
Rev: 1.0	
Date: Wednesday, August 06, 2008	Sheet 58 of 79

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 59 of 79

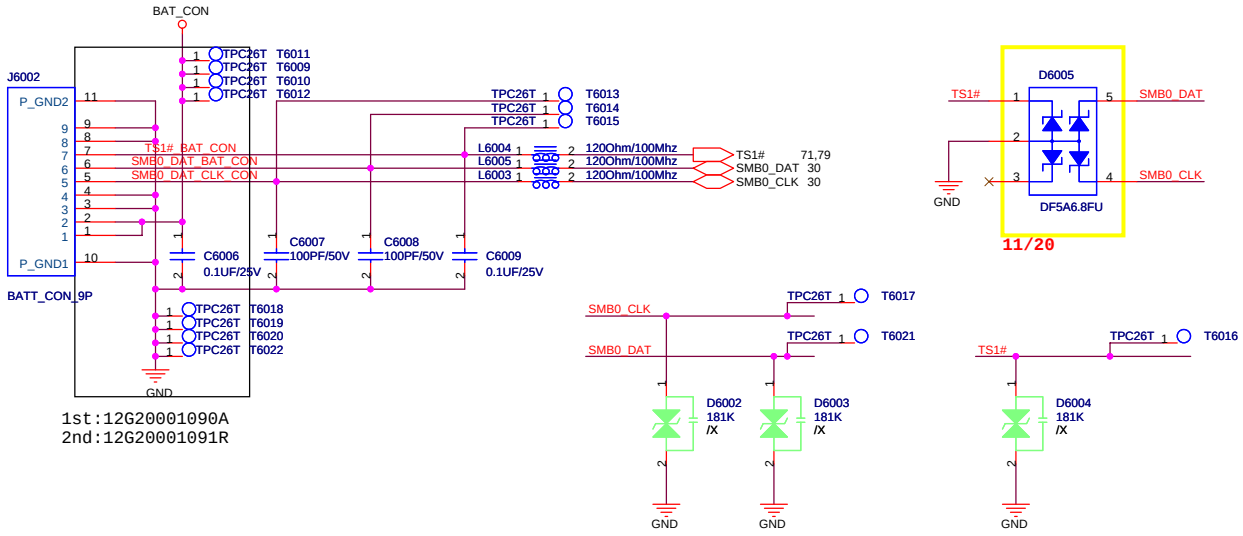
DC IN



12G14500102E

BAT IN

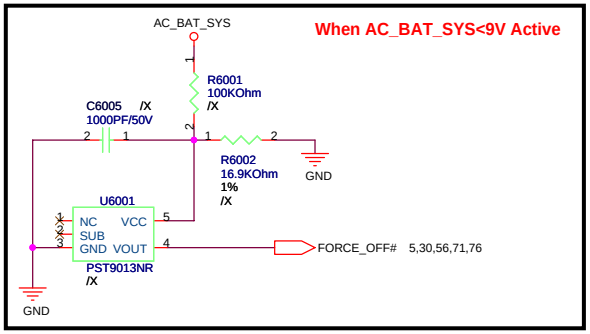
3/11 Pin define follow Battery protection board



1st:12G20001090A
2nd:12G20001091R

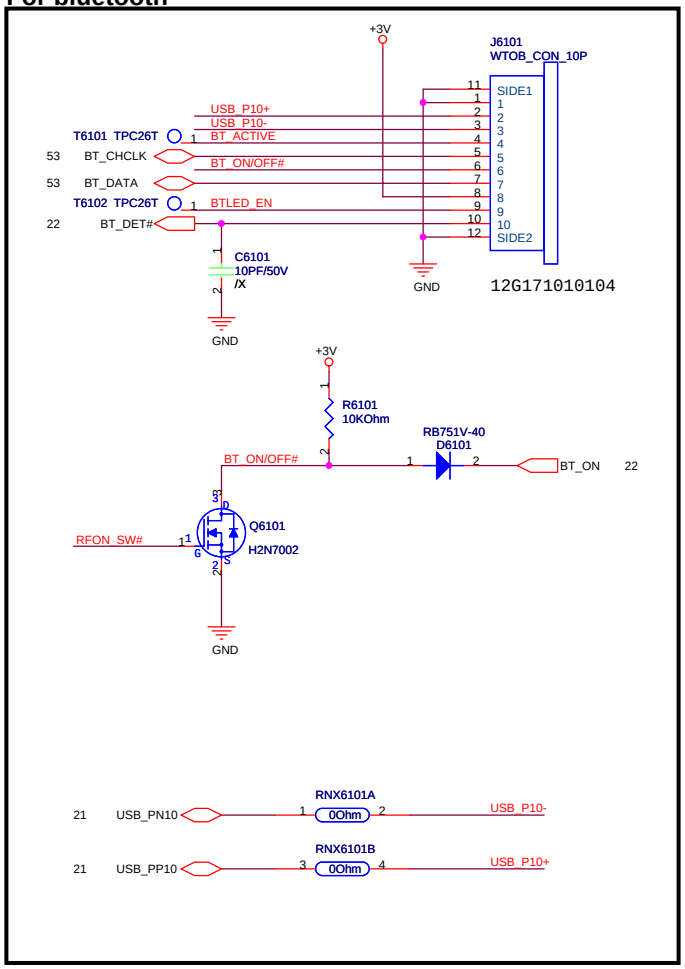
11/20

Without Battery & Pull out Adapter



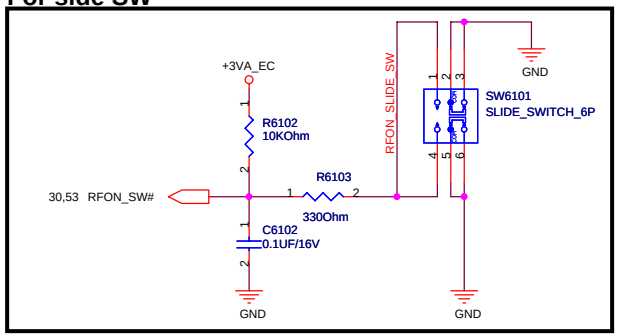
ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 60 of 79	

For bluetooth



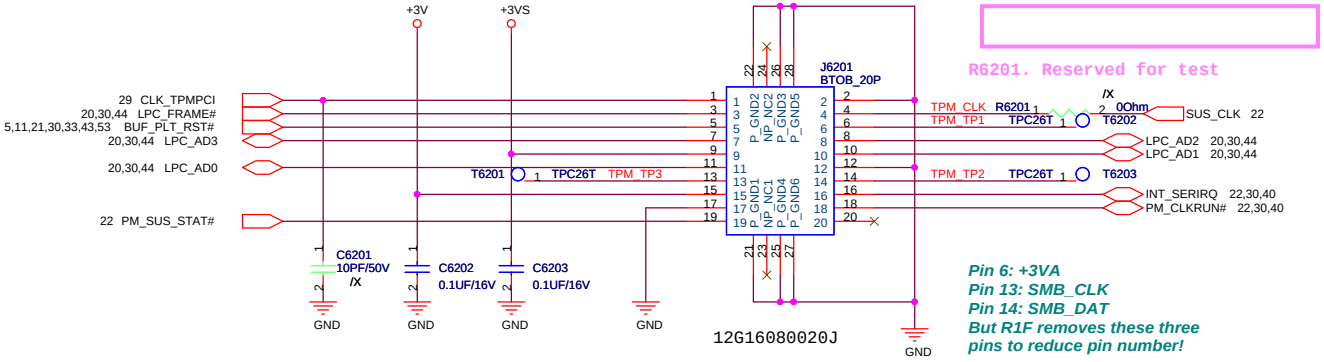
For side SW

12G090070063



ASUSTeK COMPUTER INC. NB1	Title : BlueTooth	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 61 of 79	

For TPM module

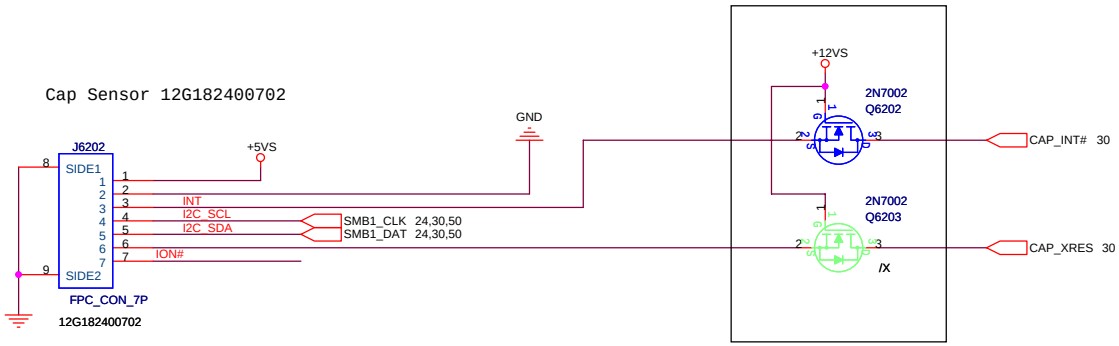


R6201. Reserved for test

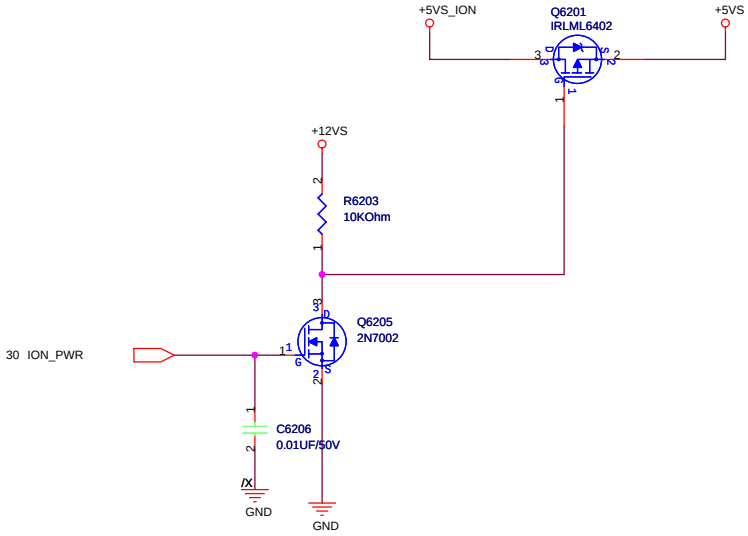
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

R1.10 04/08 Item1 level shift

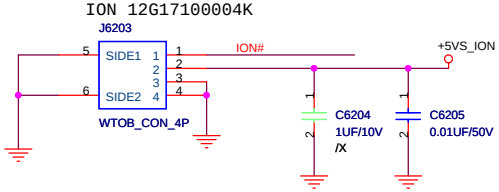
Cap Sensor 12G182400702



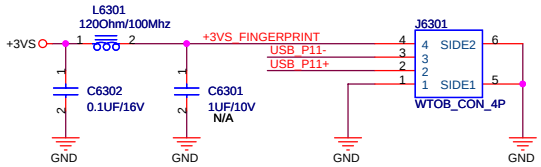
R1.10 04/08 Item2 Ion Power control schematic

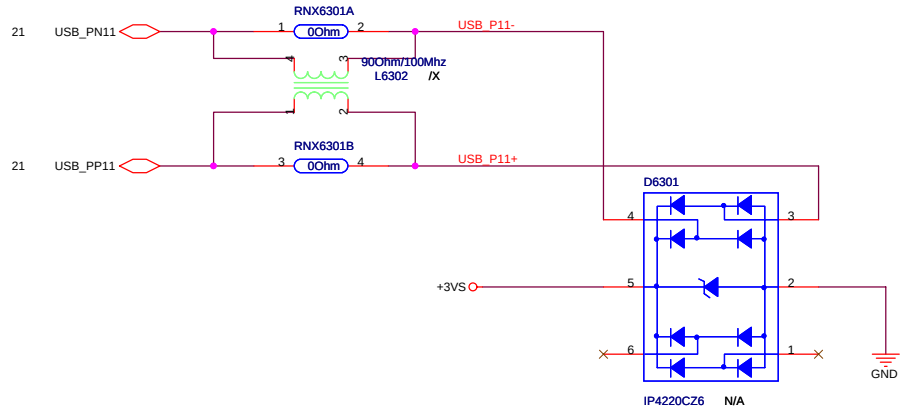


ION 12G17100004K



ASUSTeK COMPUTER INC. NB1	Title : TPM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 62 of 79	





ASUSTeK COMPUTER INC. NB1	Title : Fingerprint		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 63 of 79		

Title : TUN

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
B	N50A/N51A	1.0

Date: Thursday, July 24, 2008 Sheet 64 of 79

R1.11 04/10 EMI

U6501 EMI_SPRING_PAD

U6502 EMI_SPRING_PAD

U6503 EMI_SPRING_PAD

/EMI

R2.0 06/18 reserve for EMI

固定孔

H6527

C79D79N

/X

H6524 S335D91N

H6525 /X S335D91N

H6526 /X S335D91N

/X

FOR SCREW HOLE

H6514 S335D91N

H6518 /X S335D91N

H6523 /X S335D91N

H6501 S335D91N

H6505 /X S335D91N

H6528 /X CR226X236D91N

H6511 /X S335D91N

H6502 S335D91N

H6507 /X S335D91N

H6509 /X S335D91N

H6512 /X S335D91N

H6503 S335D91N

H6506 /X S335D91N

H6510 /X S335D91N

H6513 /X S335D91N

FOR TPM (BOT) 13GN7510M270 FOR MDC (TOP)

H6201 L4E_1A

FOR CPU

H6516 CT268B158D138

H6520 /X CT268B158D138

H6521 /X CT268B158D138

H6522 /X CT268B158D138

/X

13G021029050

FOR 3G (BOT)

H5301 A40M20-64AS

H5302 A40M20-64AS

FOR ROBSON (BOT)

H5303 CT217B67D47

H5304 CT217B67D47

FOR WLAN (BOT)

13G021043050

FOR UWB (BOT)

H5801 CT217B67D47

H5802 CT217B67D47

MINI PCI-E CON

FAN NUT

H5306 CT256B315ID146

GND

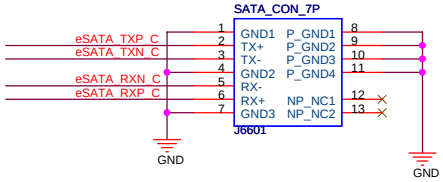
Title MDC NUT & Hinksink NUT

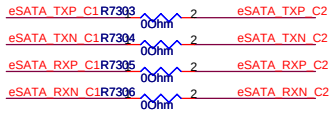
ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>

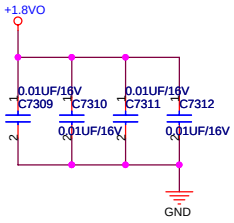
Size Custom | Project Name N50A/N51A | Rev 1.0

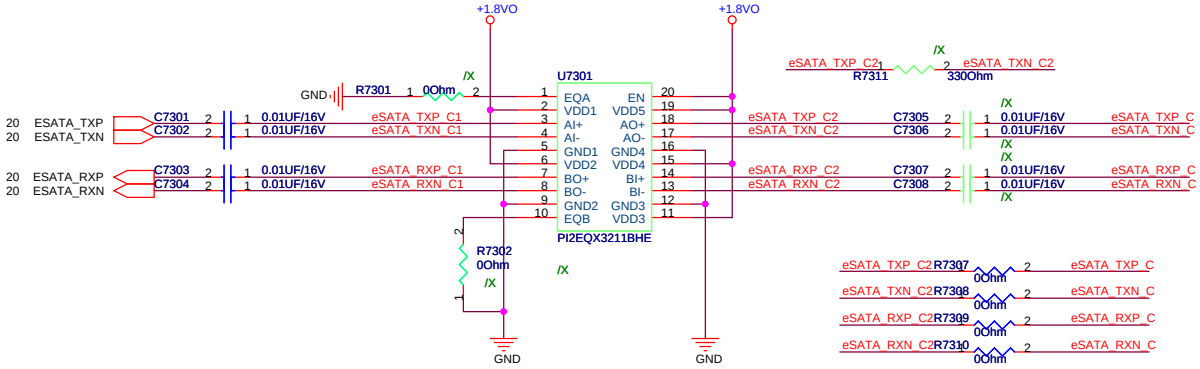
Date: Wednesday, August 06, 2008 | Sheet 65 of 79

12G15110007M

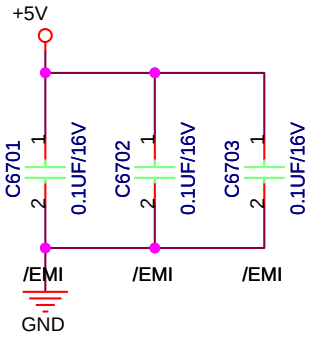


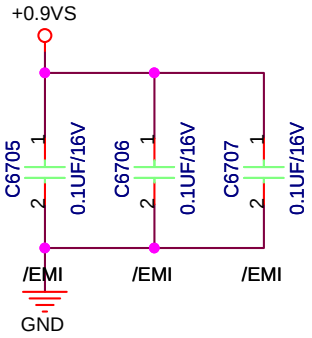


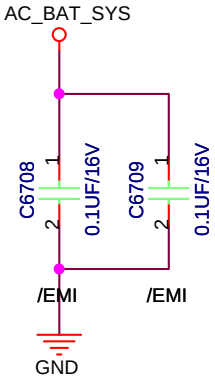


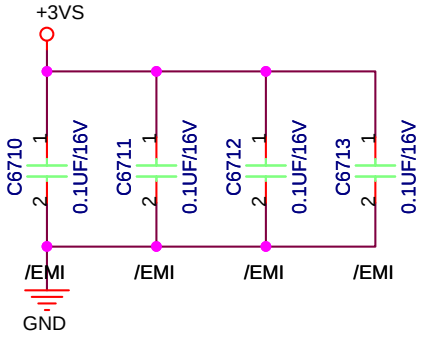


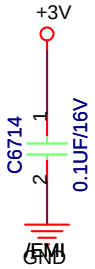
ASUSTeK COMPUTER INC. NB1	Title : E-SATA	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 66 of 79	

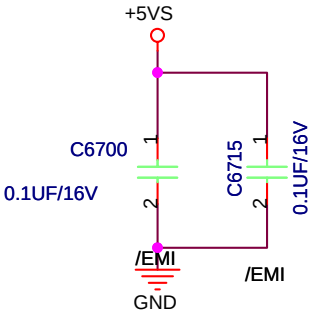


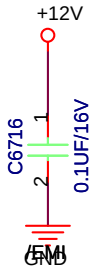












ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 67 of 79	

Title :	XDP
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: N50A/N51A
Rev: 1.0	
Date: Wednesday, August 06, 2008	Sheet 68 of 79

N50Vm Revision History

Rev	Date	Description
1.0	2007-07-28	Add R4835、C4835 、R2323
	2007/11/22	

Rev	Date	Description

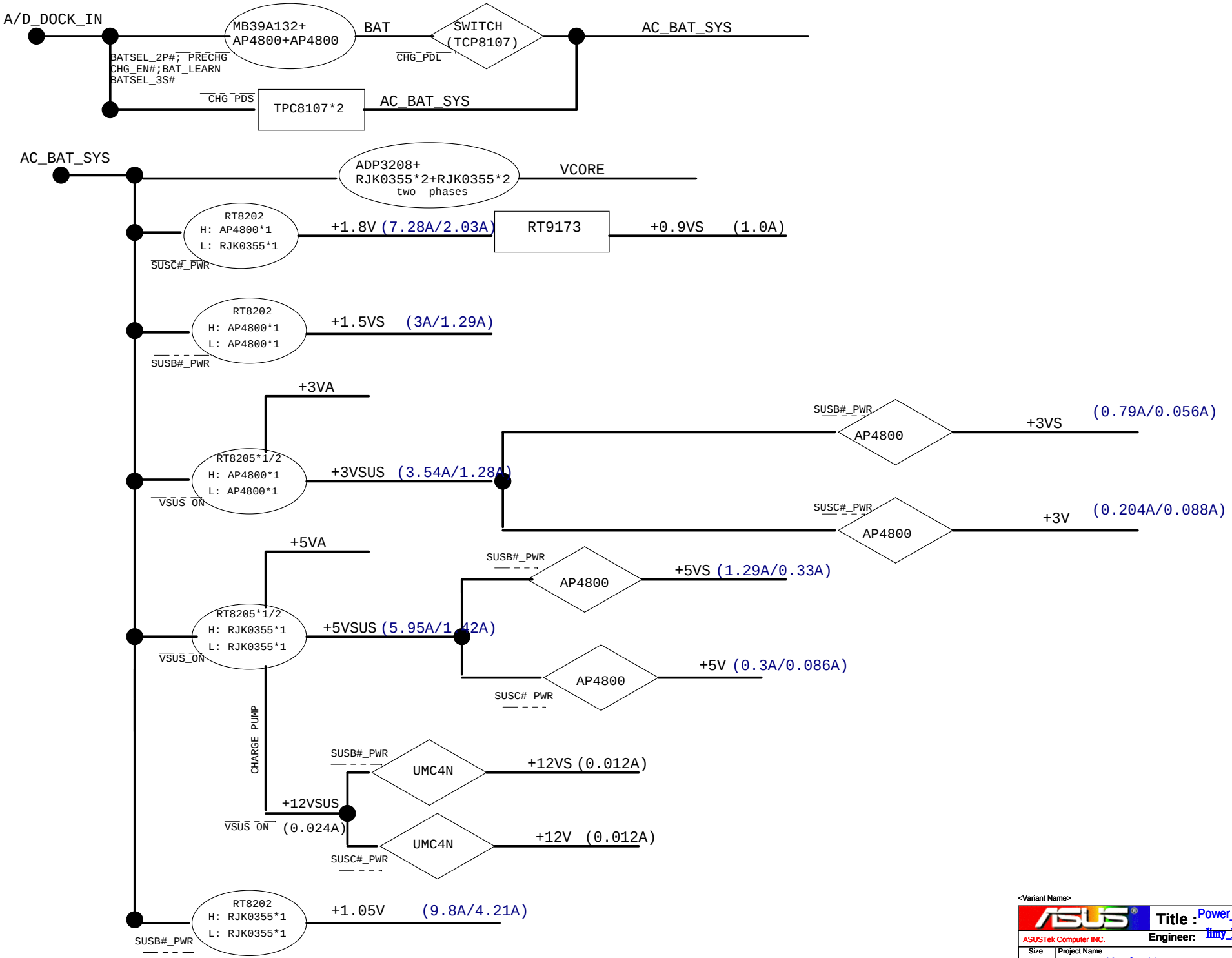
ASUSTeK COMPUTER INC. NB1

Title : HISTORY

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Monday, July 28, 2008 Sheet 69 of 79



<Variant Name>

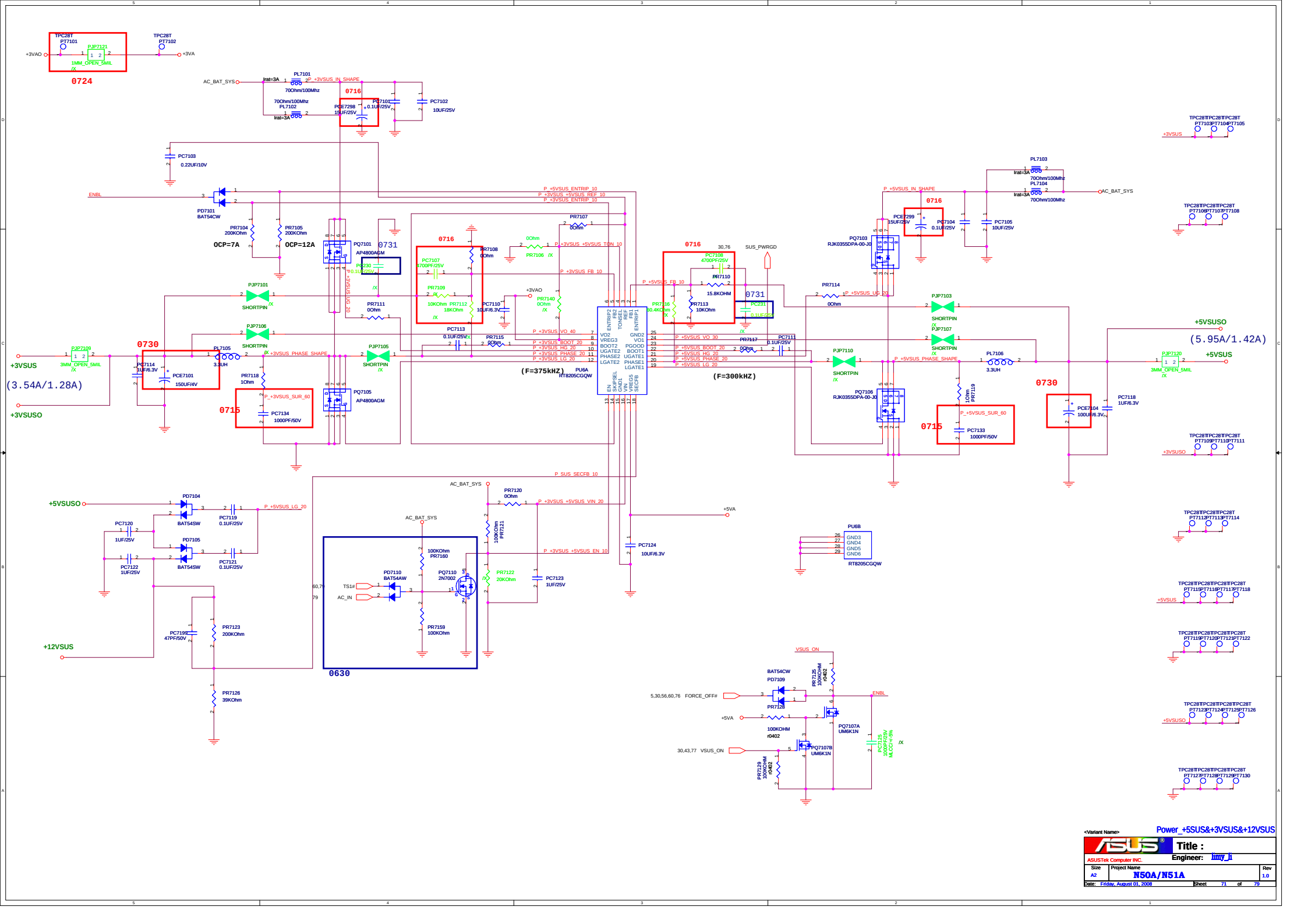
ASUSTek Computer INC.

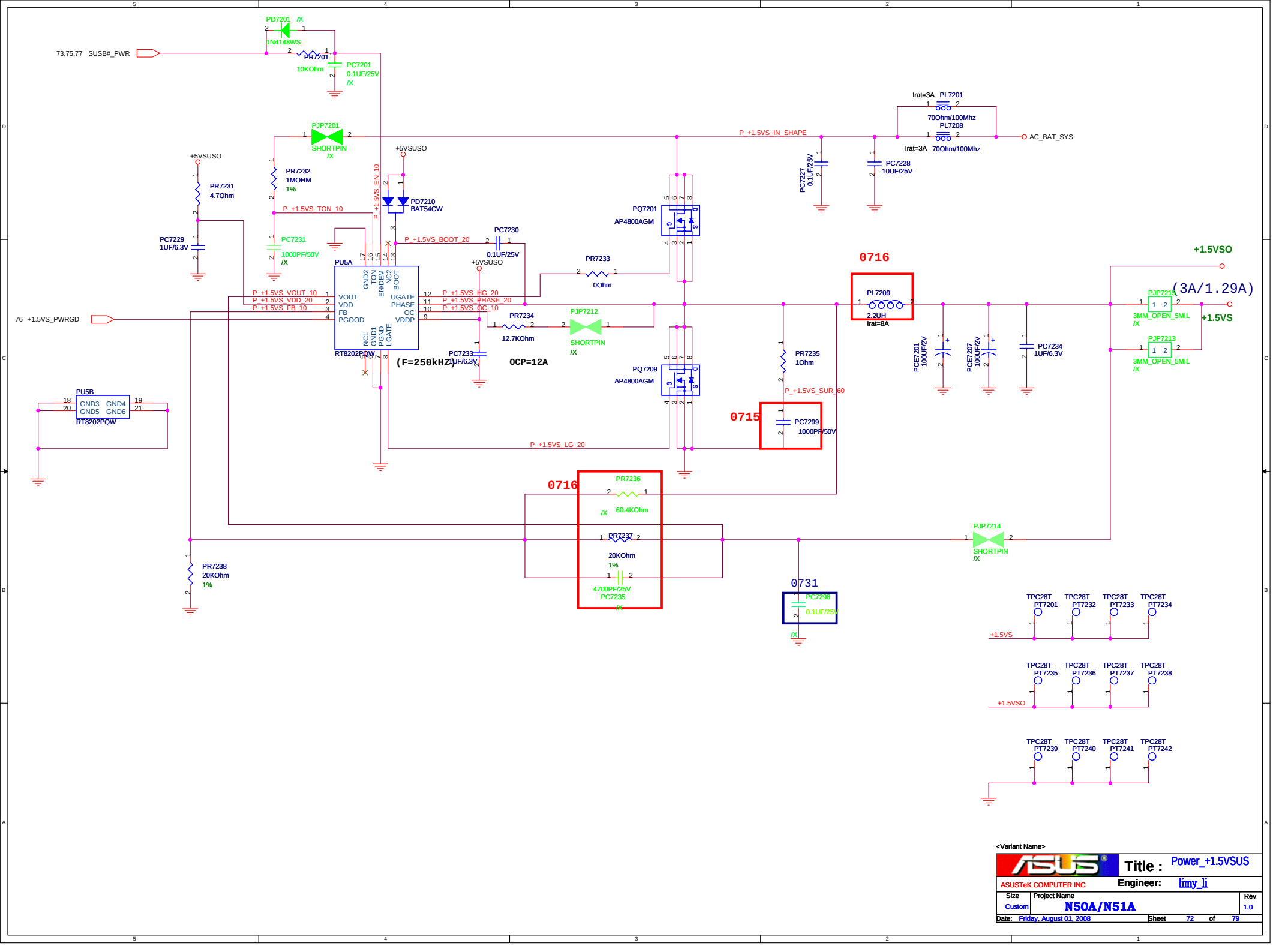
Title : Power_Flow

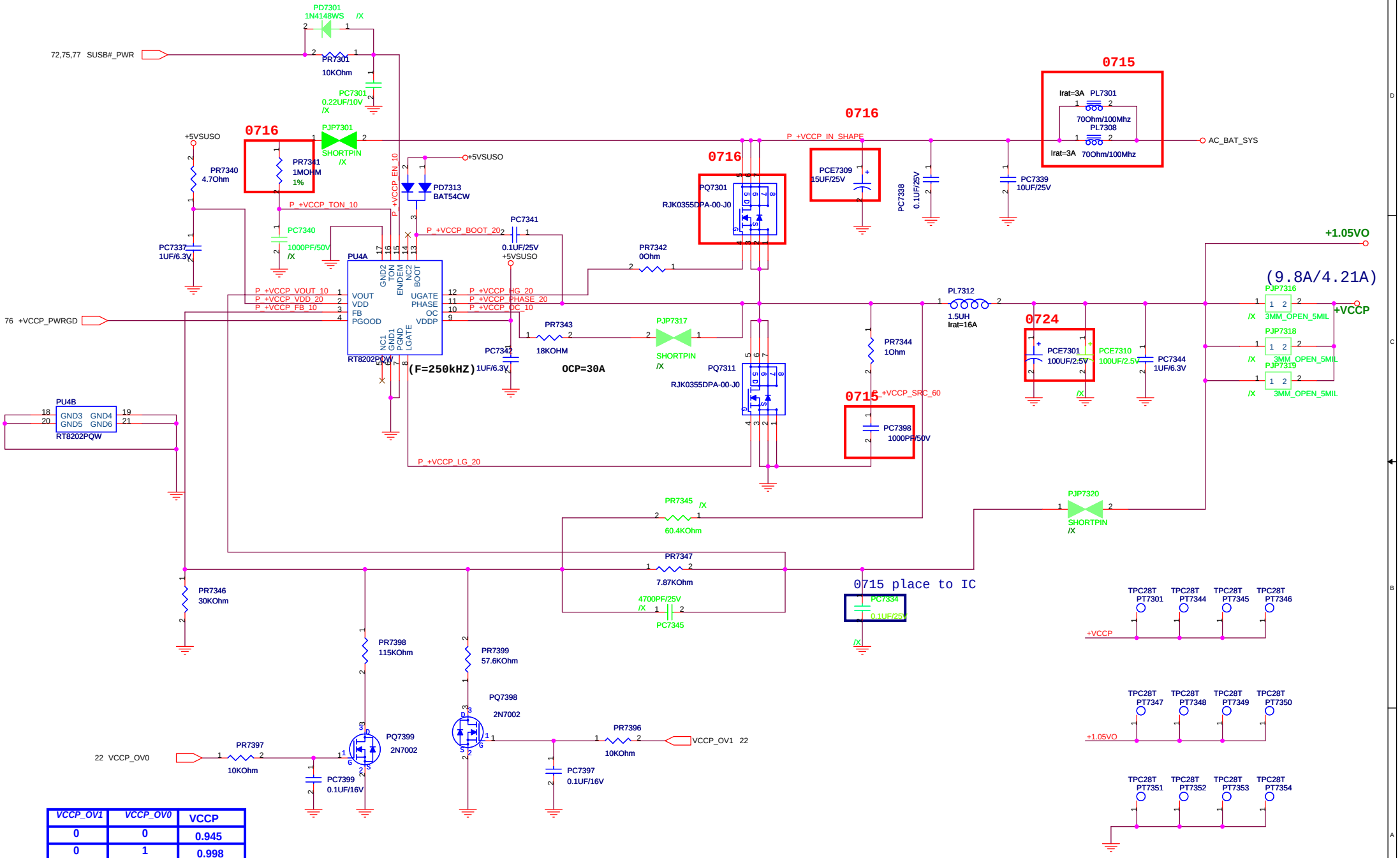
Engineer: limy_li

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 70 of 79


+3VSUS
(3.54A/1.28A)
+3VSUSO
+5VSUSO
(5.95A/1.42A)
+5VSUS
+12VSUS
+3VAO
+5VA
AC_BAT_SYS
ENBL
VSUS_ON
SUS_PWRGD
OCP=7A
OCP=12A
(F=375kHZ)
(F=300kHZ)
PU6A RT8205CGQW
PU6B RT8205CGQW
0724
0730
0731
0716
0715
0630
PJP7101 SHORTPIN
PJP7103 SHORTPIN
PJP7105 SHORTPIN
PJP7106 SHORTPIN
PJP7107 SHORTPIN
PJP7110 SHORTPIN
PJP7109 3MM_OPEN_5MIL
PJP7120 3MM_OPEN_5MIL
PJP7121 1MM_OPEN_5MIL
PL7101 70Ohm/100Mhz
PL7102 70Ohm/100Mhz
PL7103 70Ohm/100Mhz
PL7104 70Ohm/100Mhz
PL7105 3.3UH
PL7106 3.3UH
PD7101 BAT54CW
PD7104 BAT54SW
PD7105 BAT54SW
PD7109 BAT54CW
PD7110 BAT54AW
PQ7101 AP4800AGM
PQ7105 AP4800AGM
PQ7103 RJK0355DPA-00-J0
PQ7106 RJK0355DPA-00-J0
PQ7110 2N7002
PQ7107A UM6K1N
PQ7107B UM6K1N
PCE7298 15UF/25V
PCE7299 15UF/25V
PCE7101 150UF/4V
PCE7104 100UF/6.3V
PC7101 0.1UF/25V
PC7102 10UF/25V
PC7103 0.22UF/10V
PC7104 0.1UF/25V
PC7105 10UF/25V
PC7106 0.1UF/25V
PC7107 4700PF/25V
PC7108 4700PF/25V
PC7109 0.1UF/25V
PC7110 10UF/6.3V
PC7111 0.1UF/25V
PC7113 0.1UF/25V
PC7114 1UF/6.3V
PC7118 1UF/6.3V
PC7119 0.1UF/25V
PC7120 1UF/25V
PC7121 0.1UF/25V
PC7122 1UF/25V
PC7123 1UF/25V
PC7124 10UF/6.3V
PC7125 1000PF/25V
PC7126 1000PF/50V
PC7133 1000PF/50V
PC7134 1000PF/50V
PC7199 47PF/50V
PC7230 0.1UF/25V
PC7231 0.1UF/25V
PR7101 0Ohm
PR7102 0Ohm
PR7103 0Ohm
PR7104 200KOhm
PR7105 200KOhm
PR7106 0Ohm
PR7107 0Ohm
PR7108 0Ohm
PR7109 10KOhm
PR7110 15.8KOHM
PR7111 0Ohm
PR7112 18KOhm
PR7113 10KOhm
PR7114 0Ohm
PR7115 0Ohm
PR7116 30.4KOhm
PR7117 0Ohm
PR7118 10Ohm
PR7119 10Ohm
PR7120 0Ohm
PR7121 100KOhm
PR7122 20KOhm
PR7123 200KOhm
PR7125 100KOHM
PR7126 39KOhm
PR7127 10KOHM
PR7128 100KOHM
PR7159 100KOhm
PR7160 100KOhm
TPC28T PT7101
TPC28T PT7102
TPC28T PT7103 PT7104 PT7105
TPC28T PT7106 PT7107 PT7108
TPC28T PT7109 PT7110 PT7111
TPC28T PT7112 PT7113 PT7114
TPC28T PT7115 PT7116 PT7117 PT7118
TPC28T PT7119 PT7120 PT7121 PT7122
TPC28T PT7123 PT7124 PT7125 PT7126
TPC28T PT7127 PT7128 PT7129 PT7130
ENTRIP2 FB2 TONSEL REF RB1 ENTRIP1
VO2 VREG3 BOOT2 UGATE2 PHASE2 LGATE2
GND2 VO1 PGOOD BOOT1 UGATE1 PHASE1 LGATE1
EN SKIPSEL SWD1 VIN VREG5 SECFB
GND3 GND4 GND5 GND6
P_+3VSUS_+5VSUS_REF_10
P_+3VSUS_+5VSUS_TON_10
P_+3VSUS_FB_10
P_+3VSUS_VO_40
P_+3VSUS_BOOT_20
P_+3VSUS_HG_20
P_+3VSUS_PHASE_20
P_+3VSUS_LG_20
P_+5VSUS_ENTRIP_10
P_+5VSUS_FB_10
P_+5VSUS_VO_30
P_+5VSUS_BOOT_20
P_+5VSUS_HG_20
P_+5VSUS_PHASE_20
P_+5VSUS_LG_20
P_+5VSUS_UG_20
P_SUS_SECFB_10
P_+3VSUS_+5VSUS_VIN_20
P_+3VSUS_+5VSUS_EN_10
P_+5VSUS_IN_SHAPE
+3VSUS_PHASE_SHAPE
+5VSUS_PHASE_SHAPE
+3VSUS_SUR_60
+5VSUS_SUR_60
+5VSUS_LG_20
5,30,56,60,76 FORCE_OFF#
30,43,77 VSUS_ON
TS1#
AC_IN
60,79
Irat=3A
<Variant Name>
Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTek Computer INC.
Engineer: Jimy_li
Size A2
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
Sheet 71 of 79


PD7201 /X
1N4148WS
73,75,77 SUSB#_PWR
PR7201
10KOhm
PC7201
0.1UF/25V
/X
PJP7201
SHORTPIN
/X
+5VSUSO
PR7231
4.7Ohm
PC7229
1UF/6.3V
PR7232
1MOHM
1%
PC7231
1000PF/50V
/X
P_+1.5VS_TON_10
P_+1.5VS_EN_10
PD7210
BAT54CW
P_+1.5VS_BOOT_20
PC7230
0.1UF/25V
PU5A
RT8202PQW
P_+1.5VS_VOUT_10
P_+1.5VS_VDD_20
P_+1.5VS_FB_10
P_+1.5VS_HG_20
P_+1.5VS_PHASE_20
P_+1.5VS_OC_10
P_+1.5VS_LG_20
76 +1.5VS_PWRGD
PR7233
0Ohm
PR7234
12.7KOhm
PJP7212
SHORTPIN
/X
PC7233
1UF/6.3V
(F=250kHZ)
OCP=12A
PQ7201
AP4800AGM
PQ7209
AP4800AGM
P_+1.5VS_IN_SHAPE
Irat=3A PL7201
70Ohm/100Mhz
PL7208
Irat=3A 70Ohm/100Mhz
AC_BAT_SYS
PC7227
0.1UF/25V
PC7228
10UF/25V
0716
PL7209
2.2UH
Irat=8A
0715
PR7235
1Ohm
P_+1.5VS_SUR_60
PC7299
1000PF/50V
PCE7201
100UF/2V
PCE7207
100UF/2V
PC7234
1UF/6.3V
+1.5VSO
(3A/1.29A)
PJP7211
3MM_OPEN_5MIL
/X
+1.5VS
PJP7213
3MM_OPEN_5MIL
/X
0716
PR7236
/X
60.4KOhm
PR7237
20KOhm
1%
4700PF/25V
PC7235
/X
PR7238
20KOhm
1%
PJP7214
SHORTPIN
/X
0731
PC7298
0.1UF/25V
/X
PU5B
RT8202PQW
TPC28T PT7201
TPC28T PT7232
TPC28T PT7233
TPC28T PT7234
+1.5VS
TPC28T PT7235
TPC28T PT7236
TPC28T PT7237
TPC28T PT7238
+1.5VSO
TPC28T PT7239
TPC28T PT7240
TPC28T PT7241
TPC28T PT7242
<Variant Name>
Title : Power_+1.5VSUS
ASUSTeK COMPUTER INC
Engineer: limy_li
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
Sheet 72 of 79



VCCP_OV1	VCCP_OV0	VCCP
0	0	0.945
0	1	0.998
1	0	1.049
1	1	1.1005

<Variant Name>

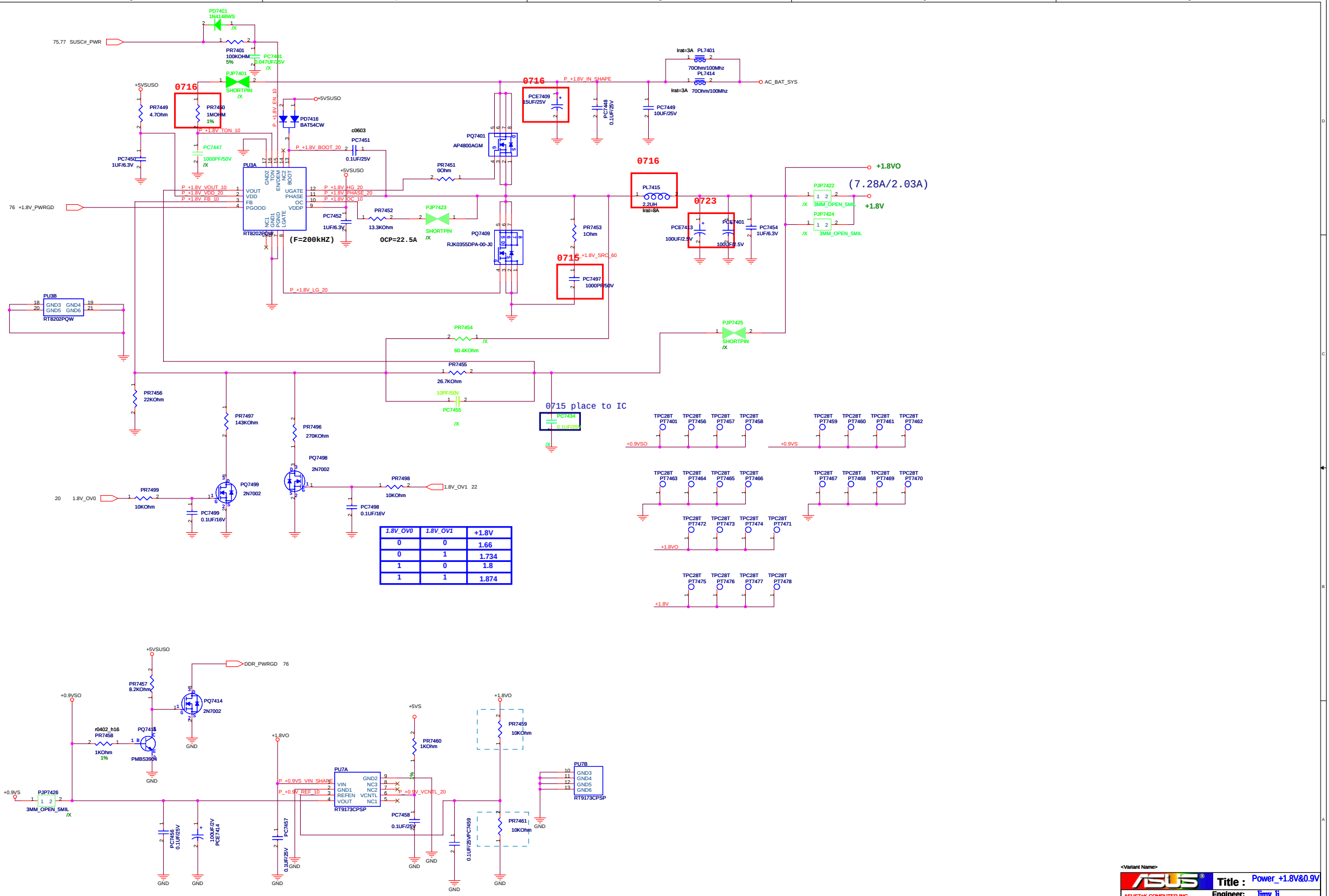
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer: limy_li

Size	Project Name	Rev
A3	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 73 of 79



1.8V_OV0	1.8V_OV1	+1.8V
0	0	1.66
0	1	1.734
1	0	1.8
1	1	1.874

<Variant Name>

ASUSTeK COMPUTER INC

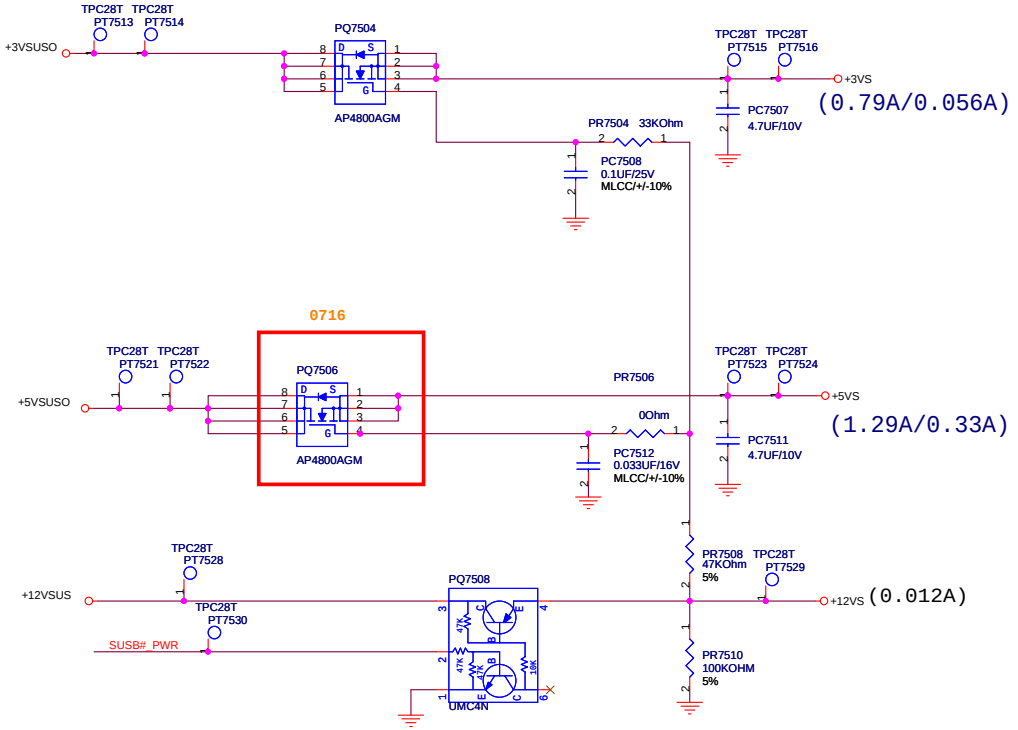
Title : Power_+1.8V&0.9V

Engineer: Jimy_Ji

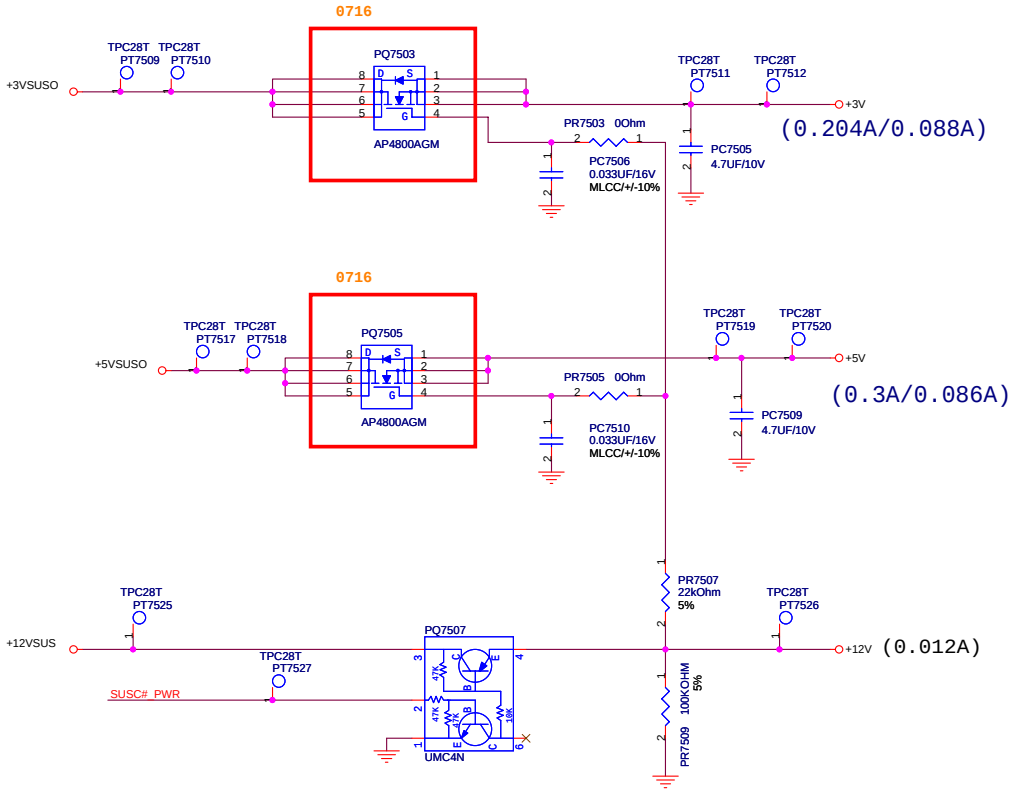
Size	Project Name	Rev
A2	N50A/N51A	1.0

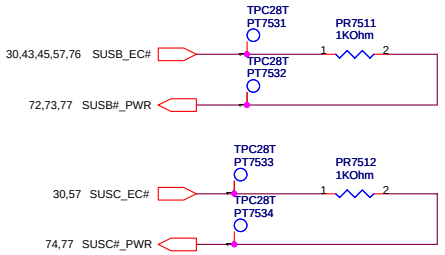
Date: Friday, August 01, 2008 Sheet 74 of 79

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

ASUSTeK COMPUTER INC

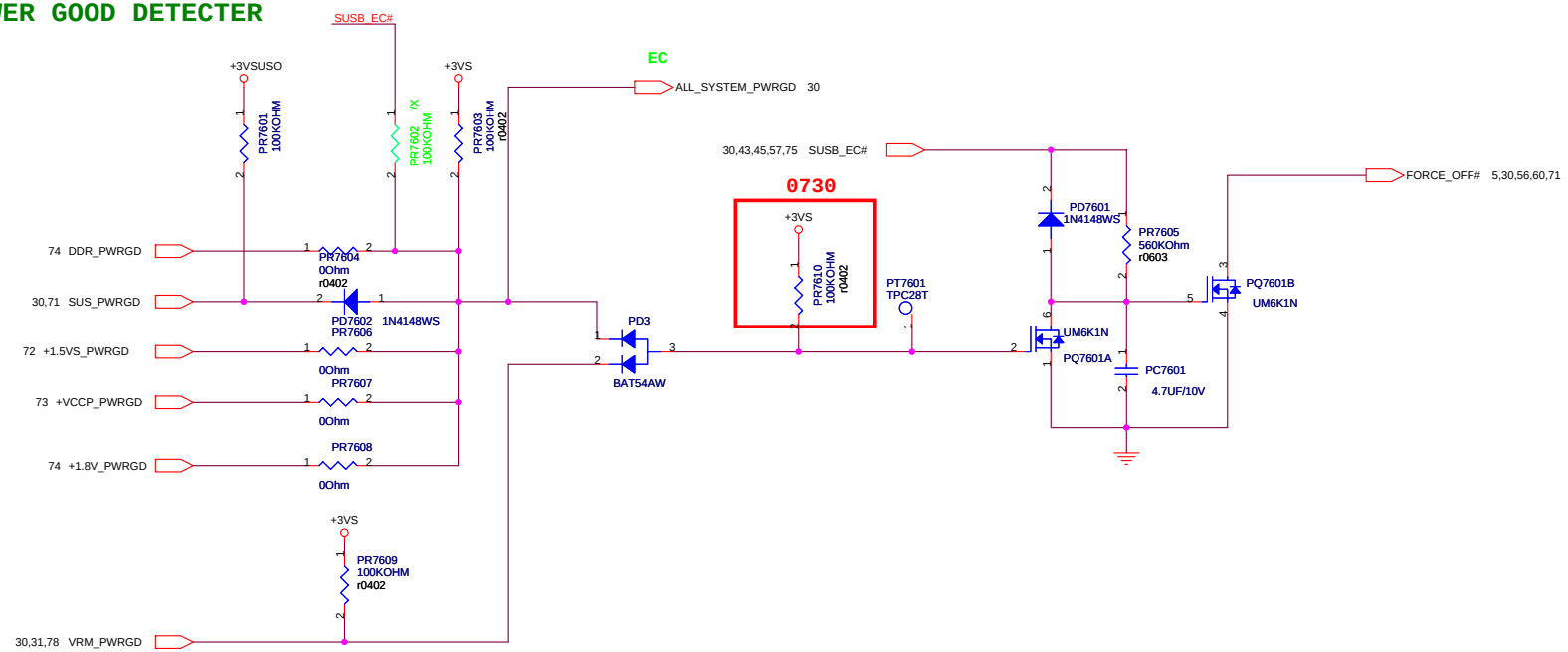
Title : Power_Load_Switch

Engineer: limy_li

Size	Project Name	Rev
Custom	N50A/N51A	1.0

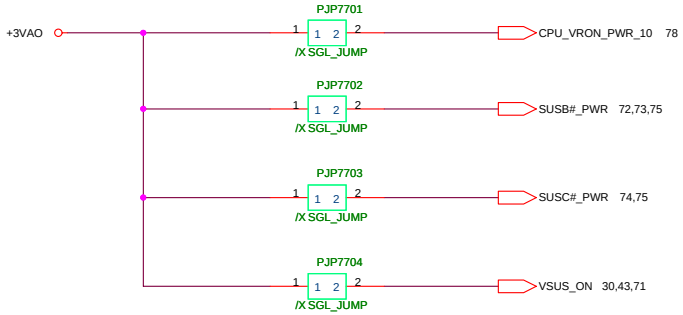
Date: Tuesday, August 05, 2008 Sheet 75 of 79

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC	Title: Power_good_detecter	
	Engineer: limy_li	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 76 of 79	



<Variant Name>

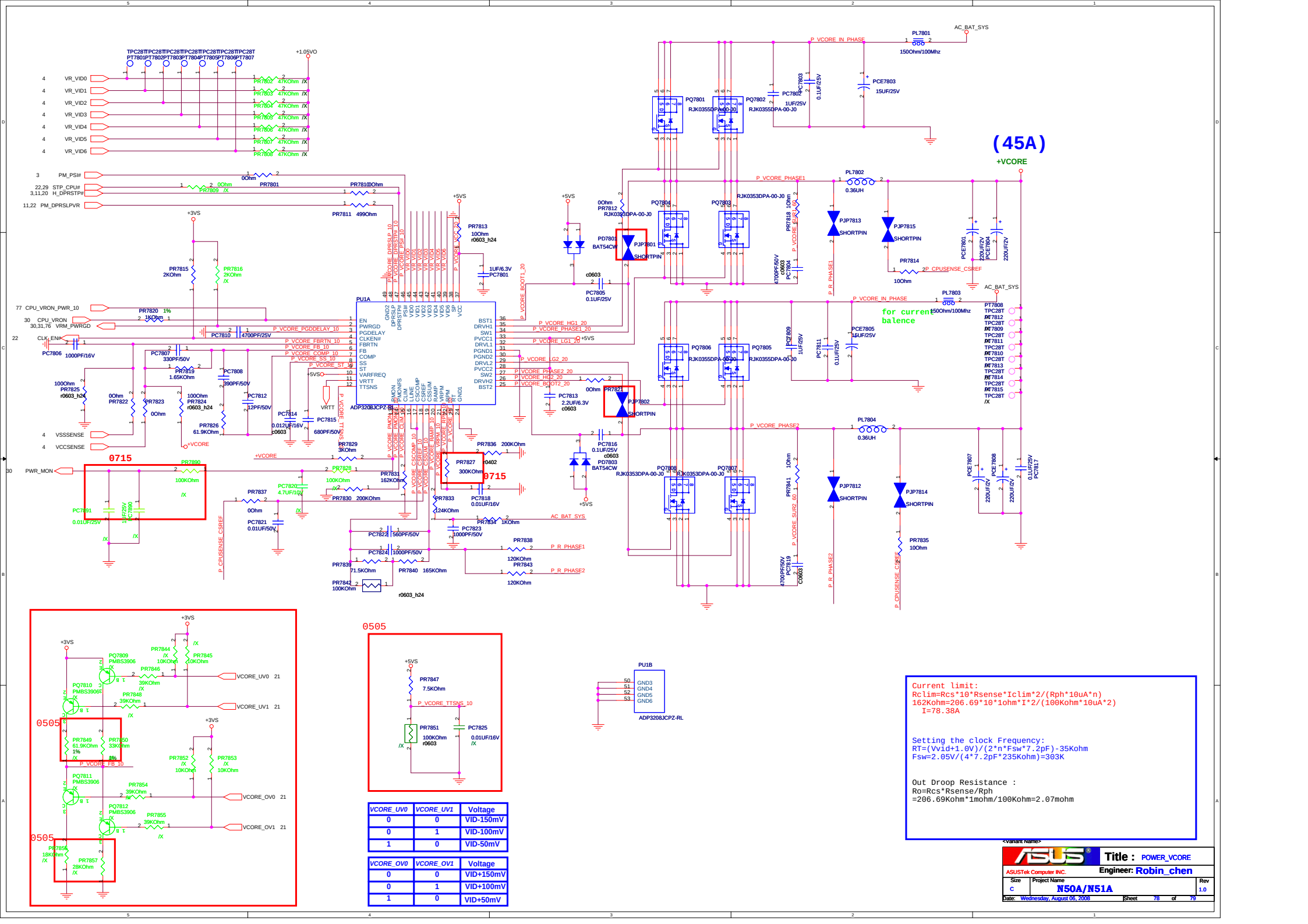
ASUSTeK COMPUTER INC

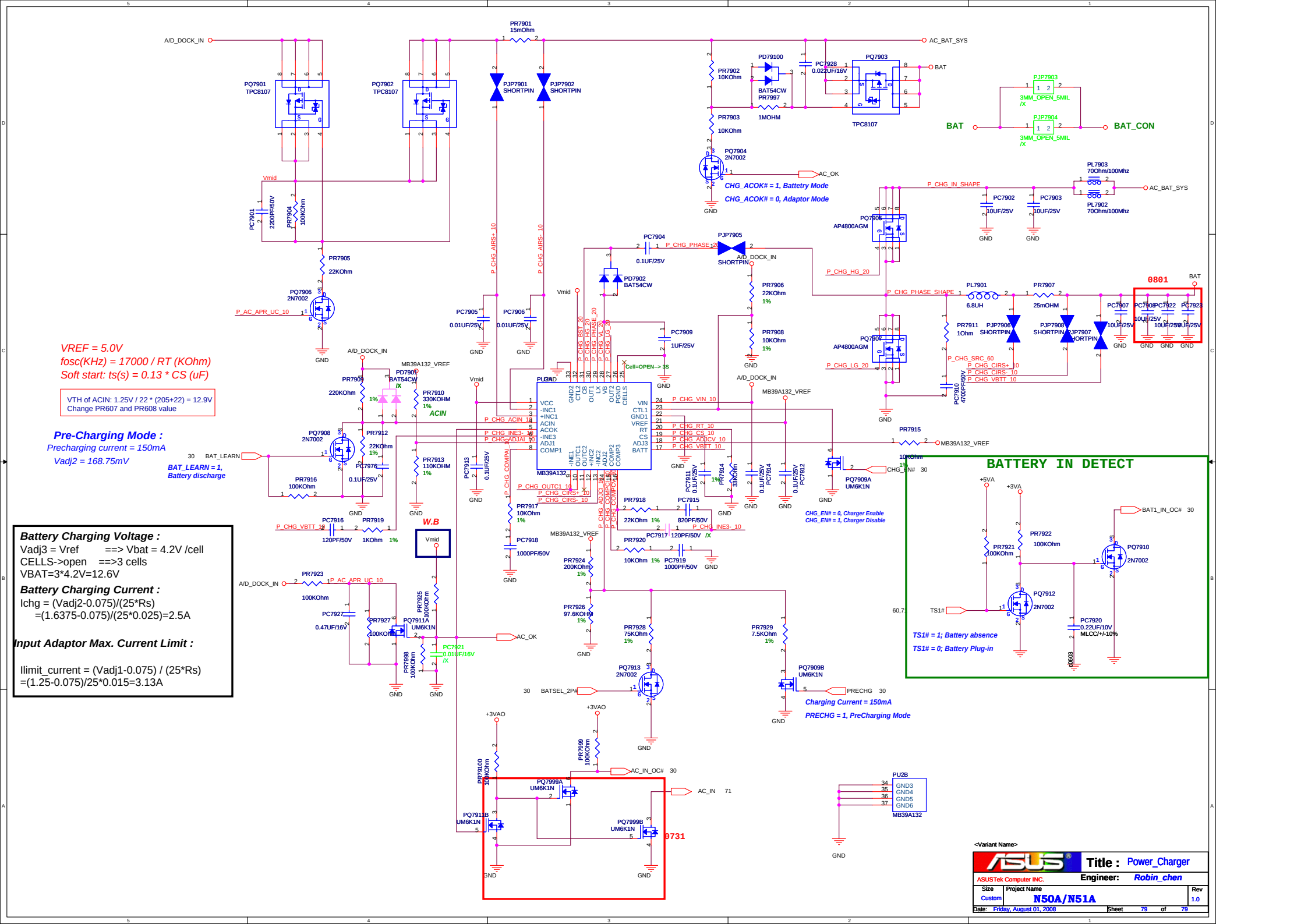
Title : Power_for_test

Engineer: Robin_chen

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 77 of 79


(45A)
+VCORE
ADP3208JCPZ-RL
PU1A
PU1B
for current balence
0715
0505
Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
I=78.38A
Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K
Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm
VCORE_UV0 VCORE_UV1 Voltage
0 0 VID-150mV
0 1 VID-100mV
1 0 VID-50mV
VCORE_OV0 VCORE_OV1 Voltage
0 0 VID+150mV
0 1 VID+100mV
1 0 VID+50mV
Title : POWER_VCORE
ASUSTek Computer INC.
Engineer: Robin_chen
Size C
Project Name N50A/N51A
Rev 1.0
Date: Wednesday, August 06, 2008
Sheet 78 of 79


VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
VTH of ACIN: 1.25V / 22 * (205+22) = 12.9V
Change PR607 and PR608 value
Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV
BAT_LEARN = 1,
Battery discharge
Battery Charging Voltage :
Vadj3 = Vref ==> Vbat = 4.2V /cell
CELLS->open ==>3 cells
VBAT=3*4.2V=12.6V
Battery Charging Current :
Ichg = (Vadj2-0.075)/(25*Rs)
=(1.6375-0.075)/(25*0.025)=2.5A
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.25-0.075)/25*0.015=3.13A
BATTERY IN DETECT
TS1# = 1; Battery absence
TS1# = 0; Battery Plug-in
CHG_EN# = 0, Charger Enable
CHG_EN# = 1, Charger Disable
Charging Current = 150mA
PRECHG = 1, PreCharging Mode
CHG_ACOK# = 1, Battetry Mode
CHG_ACOK# = 0, Adaptor Mode
0801
0731
Title : Power_Charger
ASUSTek Computer INC.
Engineer: Robin_chen
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
Sheet 79 of 79