N50Tr SCHEMATIC R110

SYSTEM PAGE REF.

POWER PAGE REF.

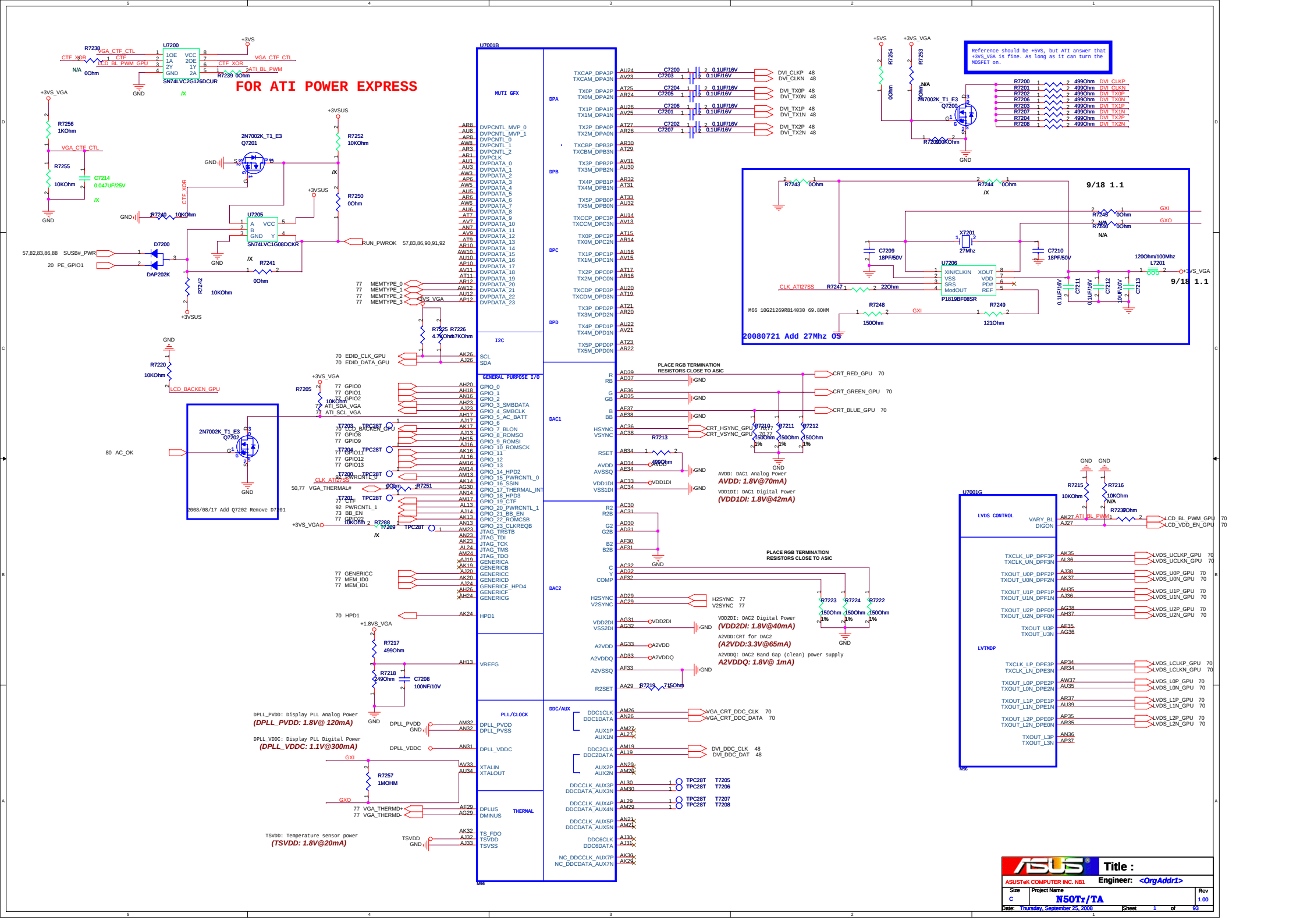
ASUSTeK COMPUTER INC. NB1

Title : Page Reference

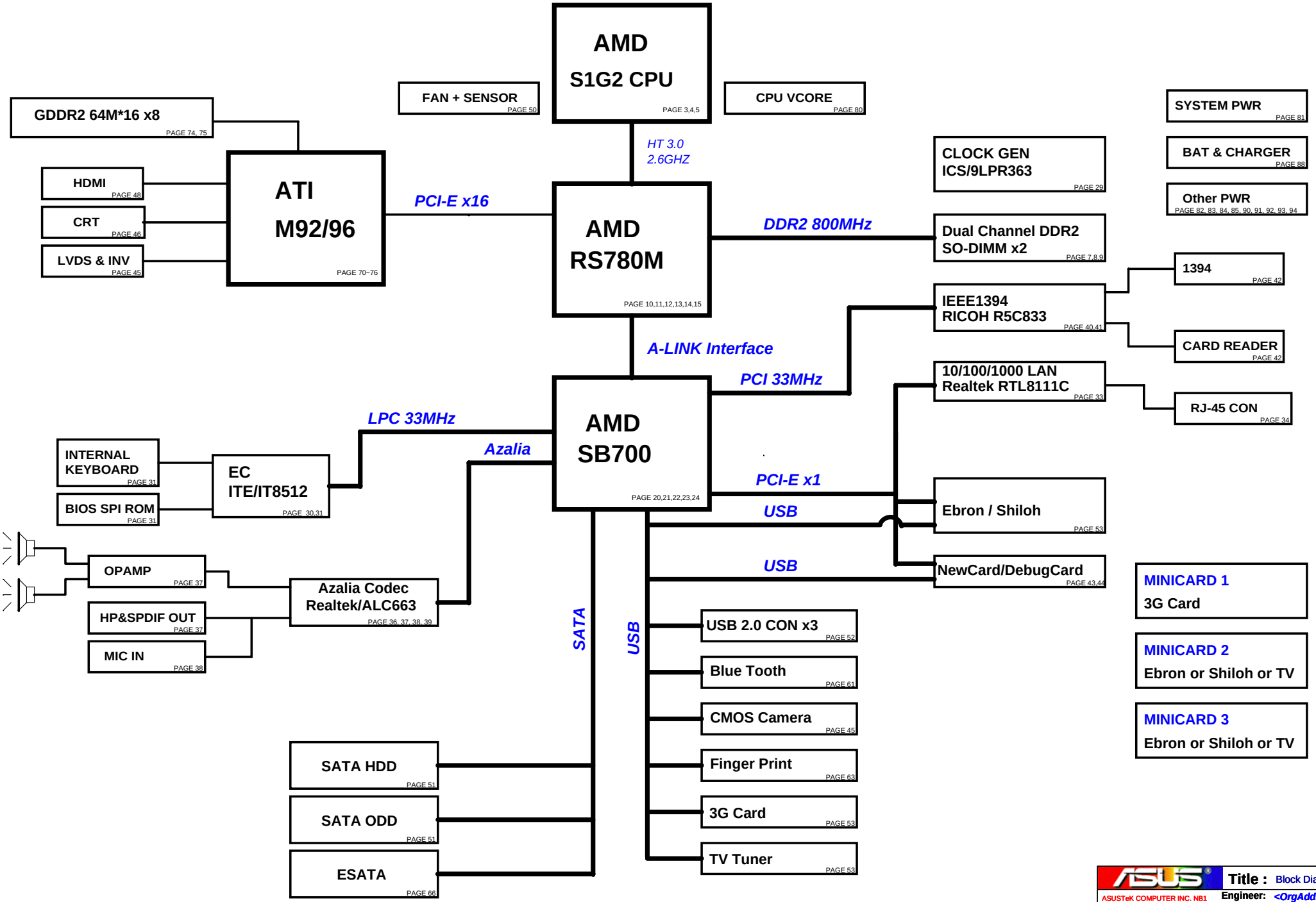
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50Tr/Ta	1.00

Date: Thursday, September 25, 2008 Sheet 1 of 93

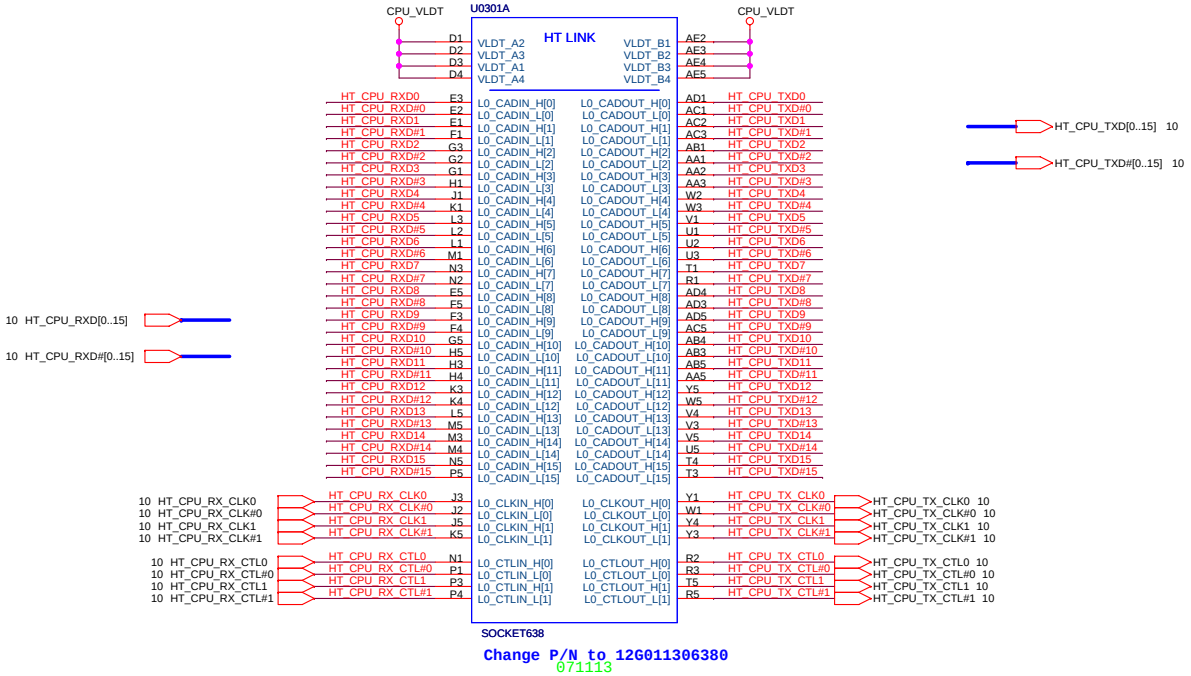

FOR ATI POWER EXPRESS
U7001B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
U7001G
LVDS CONTROL
LVTMDP
PLACE RGB TERMINATION RESISTORS CLOSE TO ASIC
9/18 1.1
20080721 Add 27Mhz OS
2008/08/17 Add Q7202 Remove D7201
Reference should be +5VS, but ATI answer that +3VS_VGA is fine. As long as it can turn the MOSFET on.
AVDD: DAC1 Analog Power
AVDD: 1.8V@70mA)
VDD1DI: DAC1 Digital Power
(VDD1DI: 1.8V@42mA)
VDD2DI: DAC2 Digital Power
(VDD2DI: 1.8V@40mA)
A2VDD:CRT for DAC2
(A2VDD:3.3V@65mA)
A2VDDQ: DAC2 Band Gap (clean) power supply
A2VDDQ: 1.8V@ 1mA)
DPLL_PVDD: Display PLL Analog Power
(DPLL_PVDD: 1.8V@ 120mA)
DPLL_VDDC: Display PLL Digital Power
(DPLL_VDDC: 1.1V@300mA)
TSVDD: Temperature sensor power
(TSVDD: 1.8V@20mA)
Title :
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size C
Project Name N50Tr/TA
Rev 1.00
Date: Thursday, September 25, 2008
Sheet 1 of 93

N50Tr Puma Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/Ta	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 2 of 93	

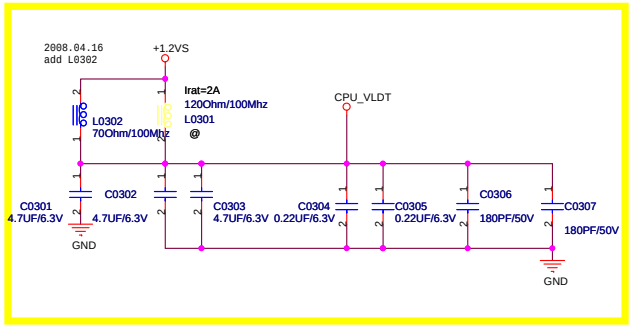
1.5A



Change P/N to 12G011306380

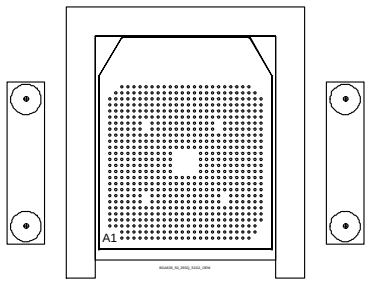
071113

Do not cross plane.



Place close to socket

*** If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**

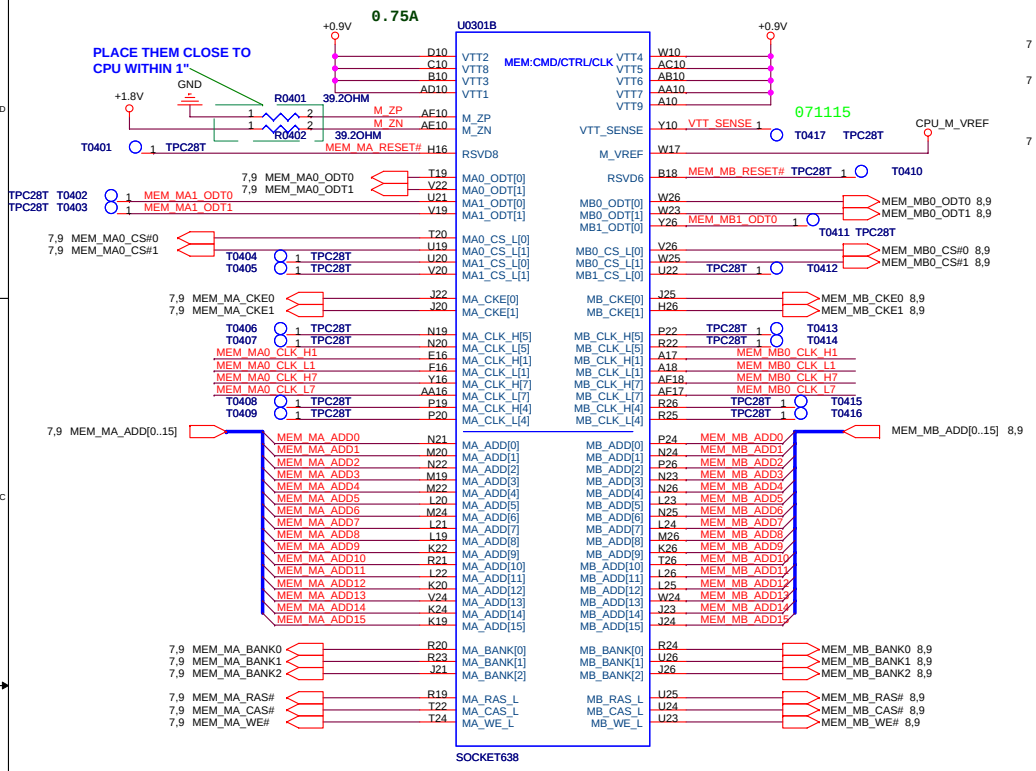


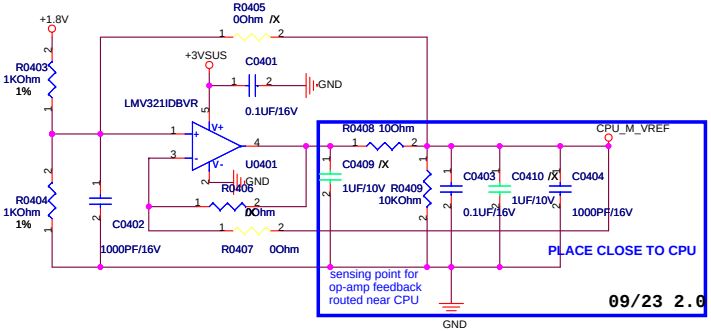
ASUSTeK COMPUTER INC. NB1	Title : Griffin HT I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/Ta	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 3 of 93	

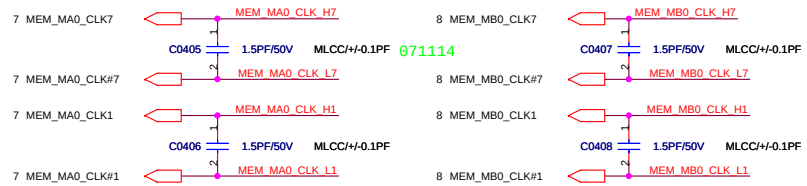
Processor Memory Interface

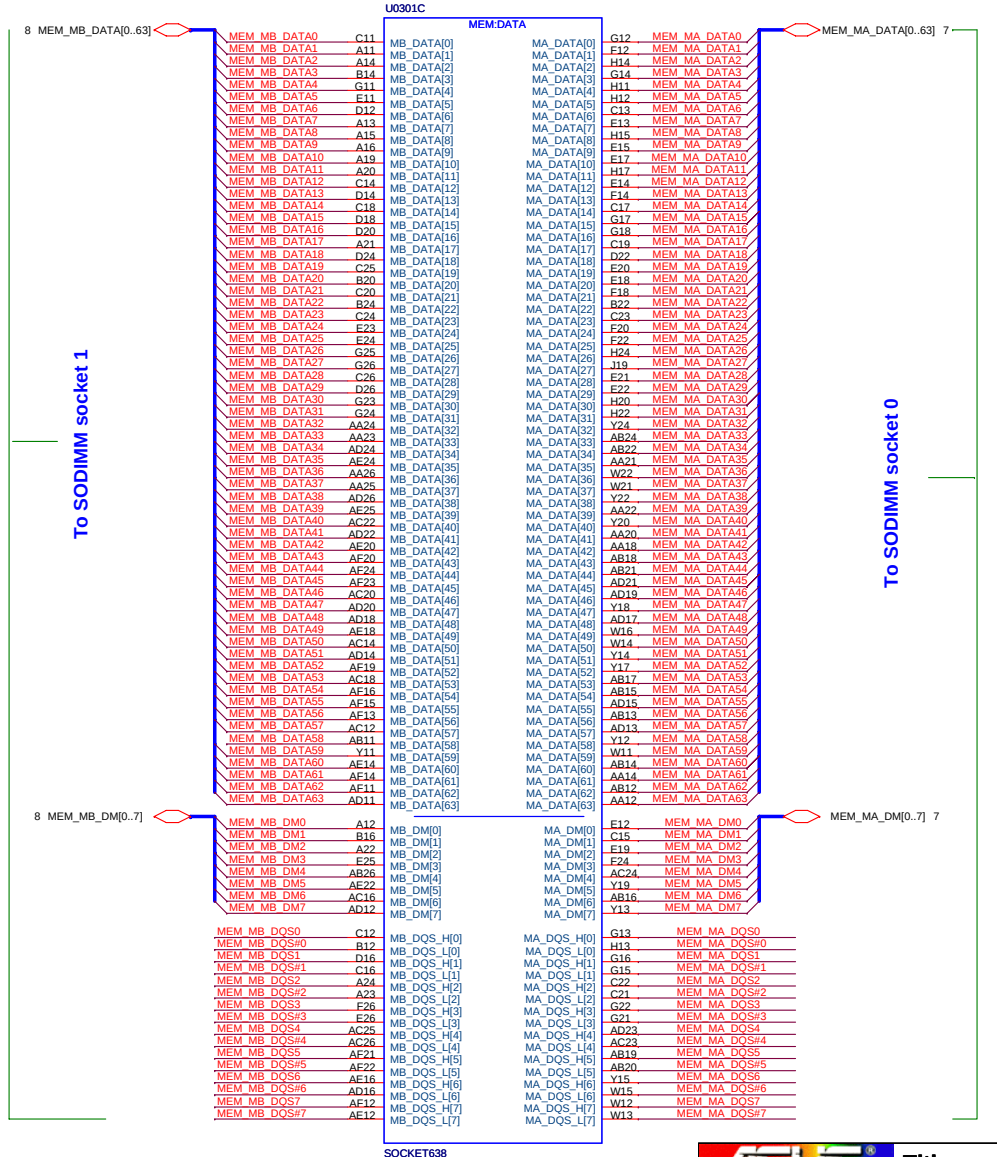
place close to PROCESSOR within 1.5 inch

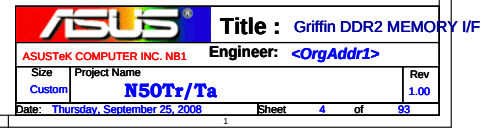
place close to PROCESSOR within 1.5 inch

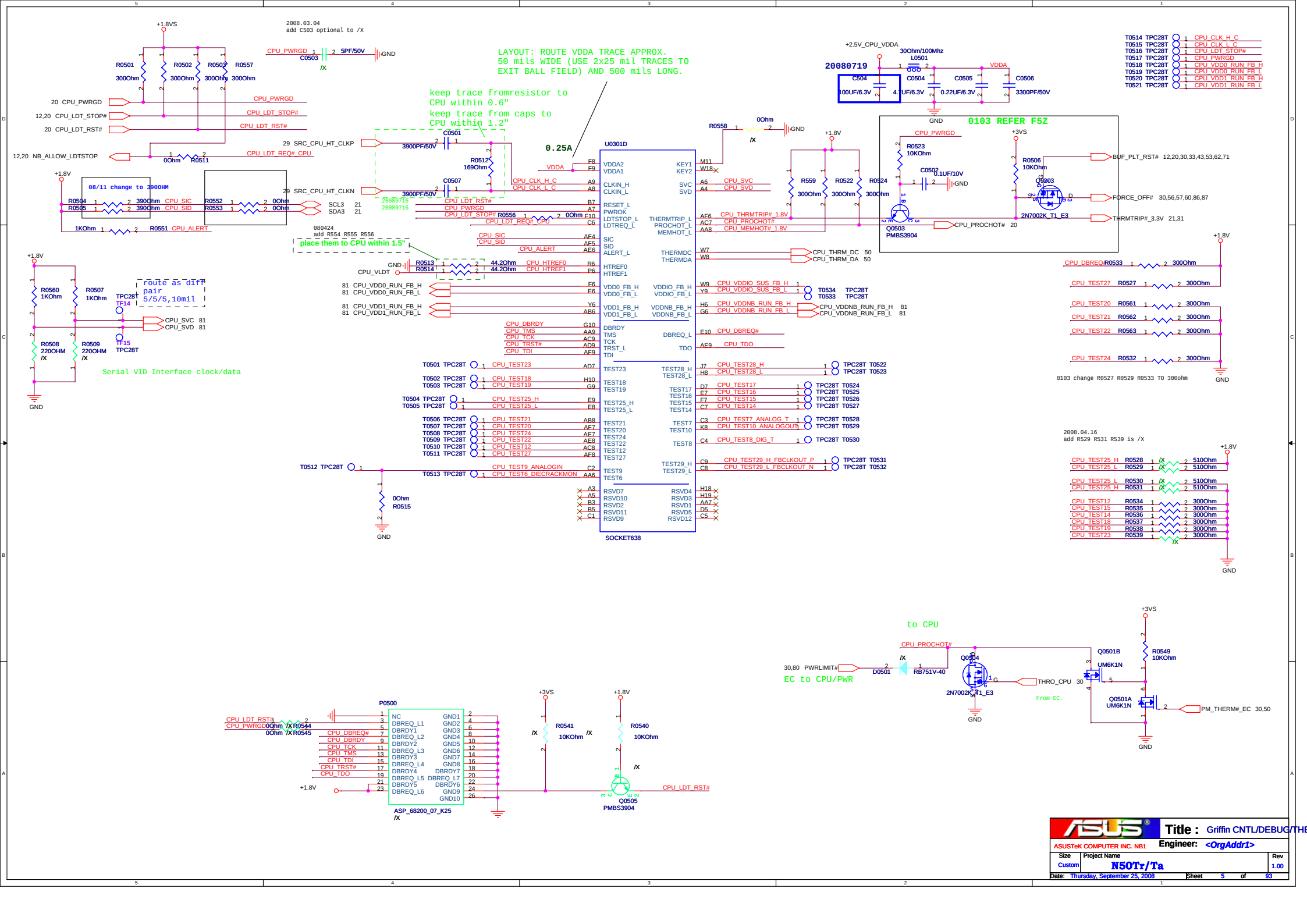


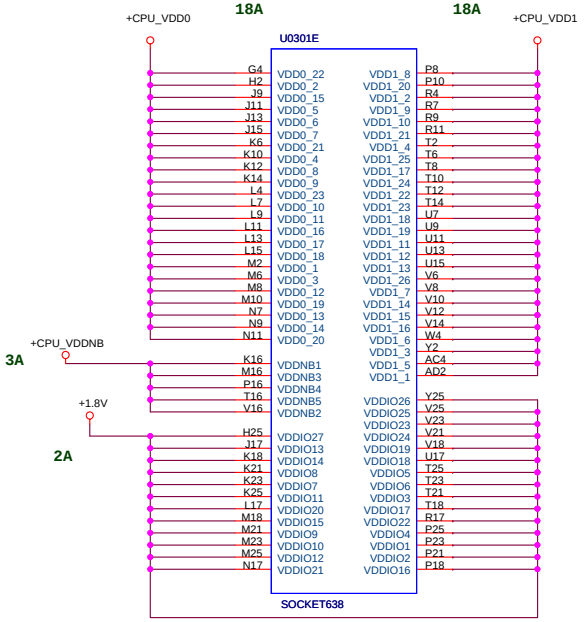


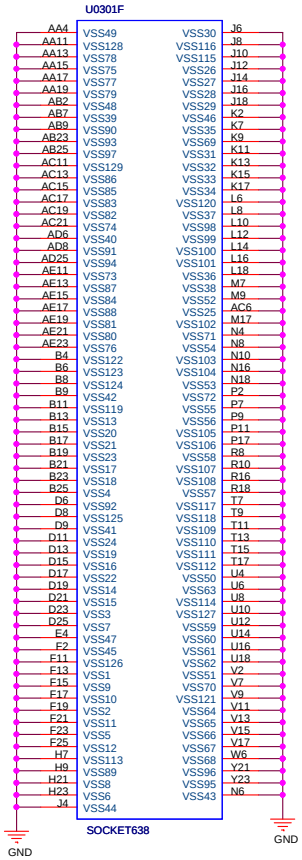


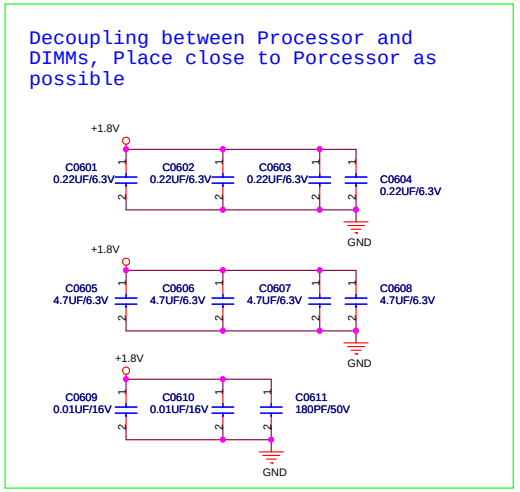


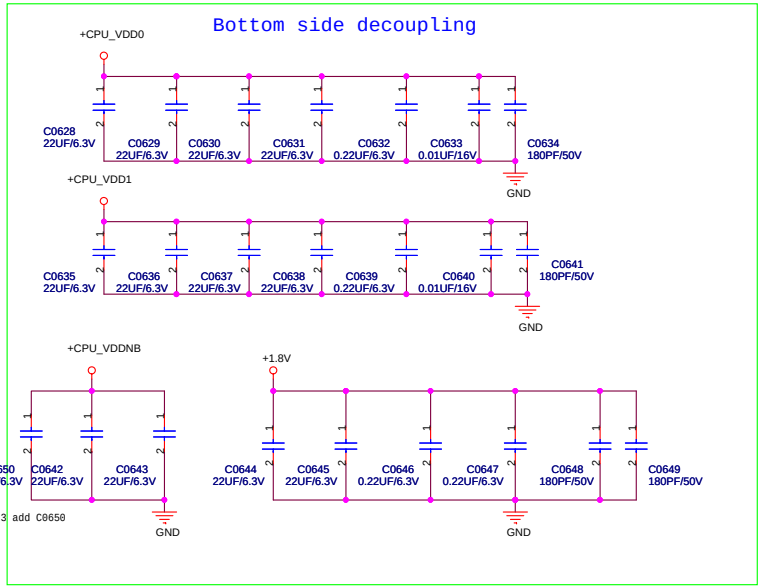


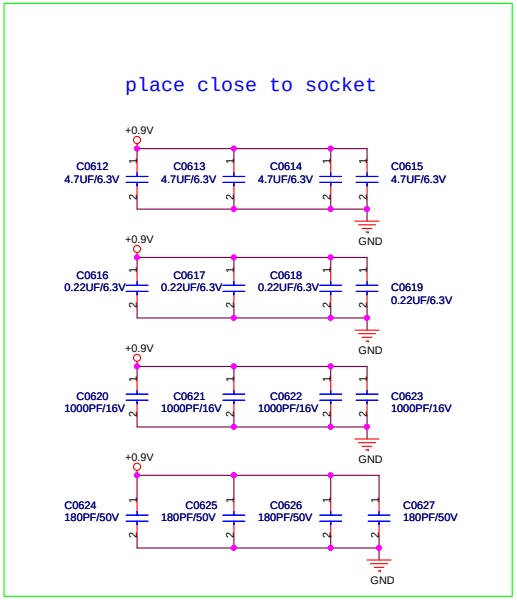

+1.8VS
R0501 300Ohm
R0502 300Ohm
R0503 300Ohm
R0557 300Ohm
20 CPU_PWRGD
12,20 CPU_LDT_STOP#
20 CPU_LDT_RST#
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
12,20 NB_ALLOW_LDTSTOP
R0511 0Ohm
CPU_LDT_REQ#_CPU
2008.03.04
add C503 optional to /X
CPU_PWRGD
C0503 5PF/50V
GND
/X
LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
0.25A
+2.5V_CPU_VDDA
30Ohm/100Mhz
L0501
20080719
C504 100UF/6.3V
C0504 4.7UF/6.3V
C0505 0.22UF/6.3V
C0506 3300PF/50V
VDDA
GND
0103 REFER F5Z
T0514 TPC28T CPU_CLK_H_C
T0515 TPC28T CPU_CLK_L_C
T0516 TPC28T CPU_LDT_STOP#
T0517 TPC28T CPU_PWRGD
T0518 TPC28T CPU_VDD0_RUN_FB_H
T0519 TPC28T CPU_VDD0_RUN_FB_L
T0520 TPC28T CPU_VDD1_RUN_FB_H
T0521 TPC28T CPU_VDD1_RUN_FB_L
29 SRC_CPU_HT_CLKP
29 SRC_CPU_HT_CLKN
C0501 3900PF/50V
C0507 3900PF/50V
R0512 169Ohm
20080716
20080716
CPU_CLK_H_C
CPU_CLK_L_C
CPU_LDT_RST#
CPU_PWRGD
CPU_LDT_STOP#
R0556 0Ohm
CPU_LDT_REQ#_CPU
U0301D
VDDA
VDDA2
VDDA1
CLKIN_H
CLKIN_L
RESET_L
PWROK
LDTSTOP_L
LDTREQ_L
SIC
SID
ALERT_L
HTREF0
HTREF1
VDD0_FB_H
VDD0_FB_L
VDD1_FB_H
VDD1_FB_L
DBRDY
TMS
TCK
TRST_L
TDI
TEST23
TEST18
TEST19
TEST25_H
TEST25_L
TEST21
TEST20
TEST24
TEST22
TEST12
TEST27
TEST9
TEST6
RSVD7
RSVD10
RSVD2
RSVD11
RSVD9
KEY1
KEY2
SVC
SVD
THERMTRIP_L
PROCHOT_L
MEMHOT_L
THERMDC
THERMDA
VDDIO_FB_H
VDDIO_FB_L
VDDNB_FB_H
VDDNB_FB_L
DBREQ_L
TDO
TEST28_H
TEST28_L
TEST17
TEST16
TEST15
TEST14
TEST7
TEST10
TEST8
TEST29_H
TEST29_L
RSVD4
RSVD3
RSVD1
RSVD5
RSVD12
SOCKET638
R0558 0Ohm
+1.8V
R559 300Ohm
R0522 300Ohm
R0524 300Ohm
CPU_THRMTRIP# 1.8V
CPU_PROCHOT#
CPU_MEMHOT# 1.8V
CPU_THRM_DC 50
CPU_THRM_DA 50
CPU_VDDIO_SUS_FB_H
CPU_VDDIO_SUS_FB_L
T0534 TPC28T
T0533 TPC28T
CPU_VDDNB_RUN_FB_H
CPU_VDDNB_RUN_FB_L
CPU_VDDNB_RUN_FB_H 81
CPU_VDDNB_RUN_FB_L 81
CPU_DBREQ#
CPU_TDO
T0522 TPC28T
T0523 TPC28T
T0524 TPC28T
T0525 TPC28T
T0526 TPC28T
T0527 TPC28T
T0528 TPC28T
T0529 TPC28T
T0530 TPC28T
T0531 TPC28T
T0532 TPC28T
R0523 10KOhm
C0502 0.1UF/10V
R0506 10KOhm
+3VS
Q0503 PMBS3904
BUF_PLT_RST# 12,20,30,33,43,53,62,71
FORCE_OFF# 30,56,57,60,86,87
2N7002K_T1_E3
THRMTRIP#_3.3V 21,31
CPU_PROCHOT# 20
08/11 change to 390OHM
R0504 390Ohm CPU_SIC
R0505 390Ohm CPU_SID
R0552 0Ohm
R0553 0Ohm
SCL3 21
SDA3 21
1KOhm R0551 CPU_ALERT
080424
add R554 R555 R556
place them to CPU within 1.5"
CPU_SIC
CPU_SID
CPU_ALERT
R0513 44.2Ohm CPU_HTREF0
R0514 44.2Ohm CPU_HTREF1
CPU_VLDT
81 CPU_VDD0_RUN_FB_H
81 CPU_VDD0_RUN_FB_L
81 CPU_VDD1_RUN_FB_H
81 CPU_VDD1_RUN_FB_L
R0560 1KOhm
R0507 1KOhm
TPC28T TF14
TPC28T TF15
R0508 220OHM /X
R0509 220OHM /X
route as diff pair 5/5/5,10mil
CPU_SVC 81
CPU_SVD 81
Serial VID Interface clock/data
CPU_DBREQ R0533 300Ohm
CPU_TEST27 R0527 300Ohm
CPU_TEST20 R0561 300Ohm
CPU_TEST21 R0562 300Ohm
CPU_TEST22 R0563 300Ohm
CPU_TEST24 R0532 300Ohm
0103 change R0527 R0529 R0533 TO 300ohm
2008.04.16
add R529 R531 R539 is /X
CPU_TEST25_H R0528 510Ohm
CPU_TEST25_L R0529 510Ohm
CPU_TEST25_L R0530 510Ohm
CPU_TEST25_H R0531 510Ohm
CPU_TEST12 R0534 300Ohm
CPU_TEST15 R0535 300Ohm
CPU_TEST14 R0536 300Ohm
CPU_TEST18 R0537 300Ohm
CPU_TEST19 R0538 300Ohm
CPU_TEST23 R0539 300Ohm
T0501 TPC28T CPU_TEST23
T0502 TPC28T CPU_TEST18
T0503 TPC28T CPU_TEST19
T0504 TPC28T CPU_TEST25_H
T0505 TPC28T CPU_TEST25_L
T0506 TPC28T CPU_TEST21
T0507 TPC28T CPU_TEST20
T0508 TPC28T CPU_TEST24
T0509 TPC28T CPU_TEST22
T0510 TPC28T CPU_TEST12
T0511 TPC28T CPU_TEST27
T0512 TPC28T
T0513 TPC28T CPU_TEST9_ANALOGIN
CPU_TEST6_DIECRACKMON
0Ohm R0515
to CPU
CPU_PROCHOT#
30,80 PWRLIMIT#
D0501 RB751V-40
EC to CPU/PWR
Q0501A UM6K1N
Q0501B UM6K1N
2N7002K_T1_E3
THRO_CPU 30
From EC.
R0549 10KOhm
PM_THERM#_EC 30,50
P0500
ASP_68200_07_K25
CPU_LDT_RST#
CPU_PWRGD
0Ohm /X R0544
0Ohm /X R0545
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
R0541 10KOhm /X
R0540 10KOhm /X
Q0505 PMBS3904
CPU_LDT_RST#
ASUSTeK COMPUTER INC. NB1
Title : Griffin CNTL/DEBUG/THE
Engineer: <OrgAddr1>
Size Custom
Project Name N50Tr/Ta
Rev 1.00
Date: Thursday, September 25, 2008
Sheet 5 of 93





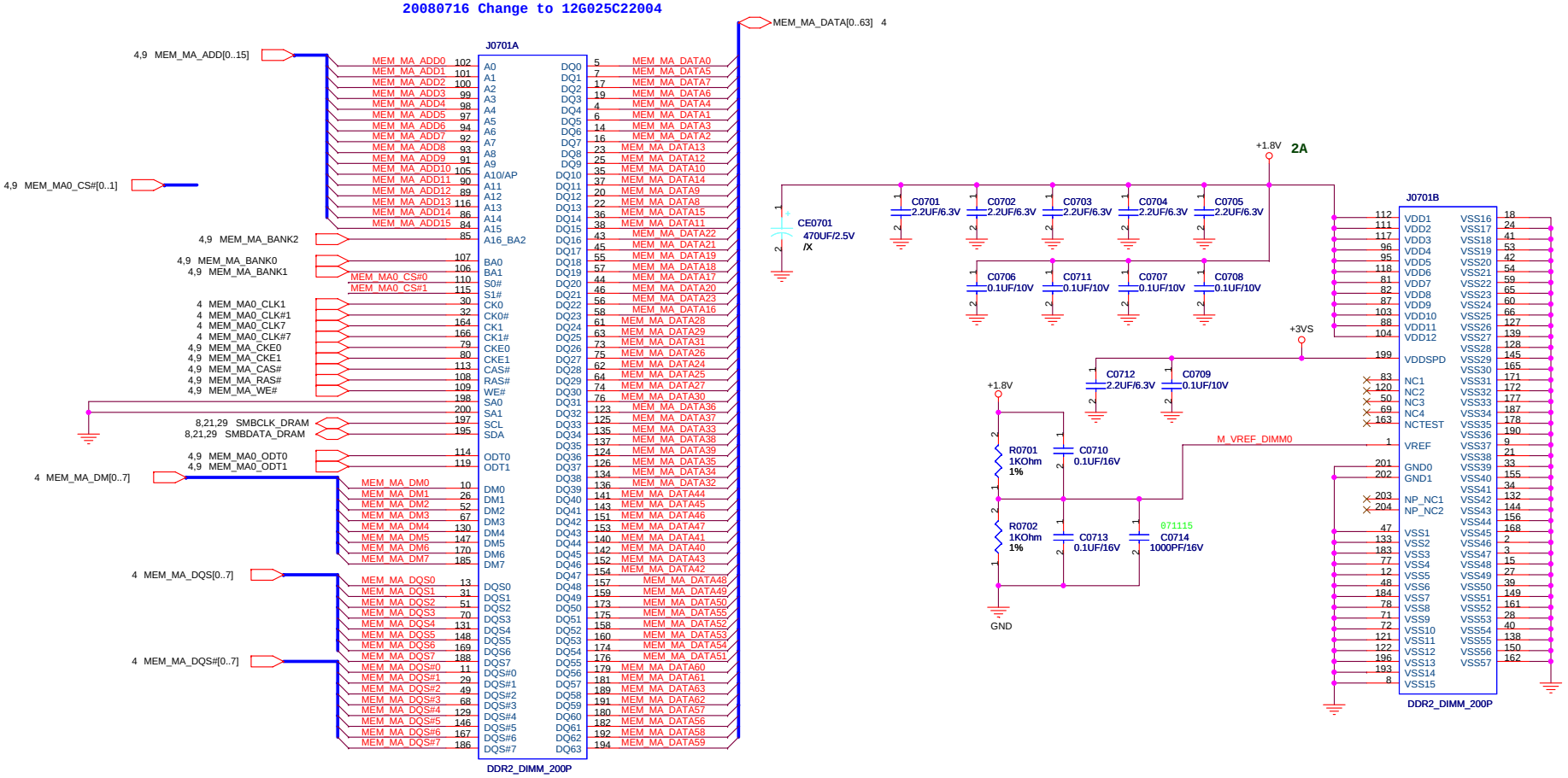




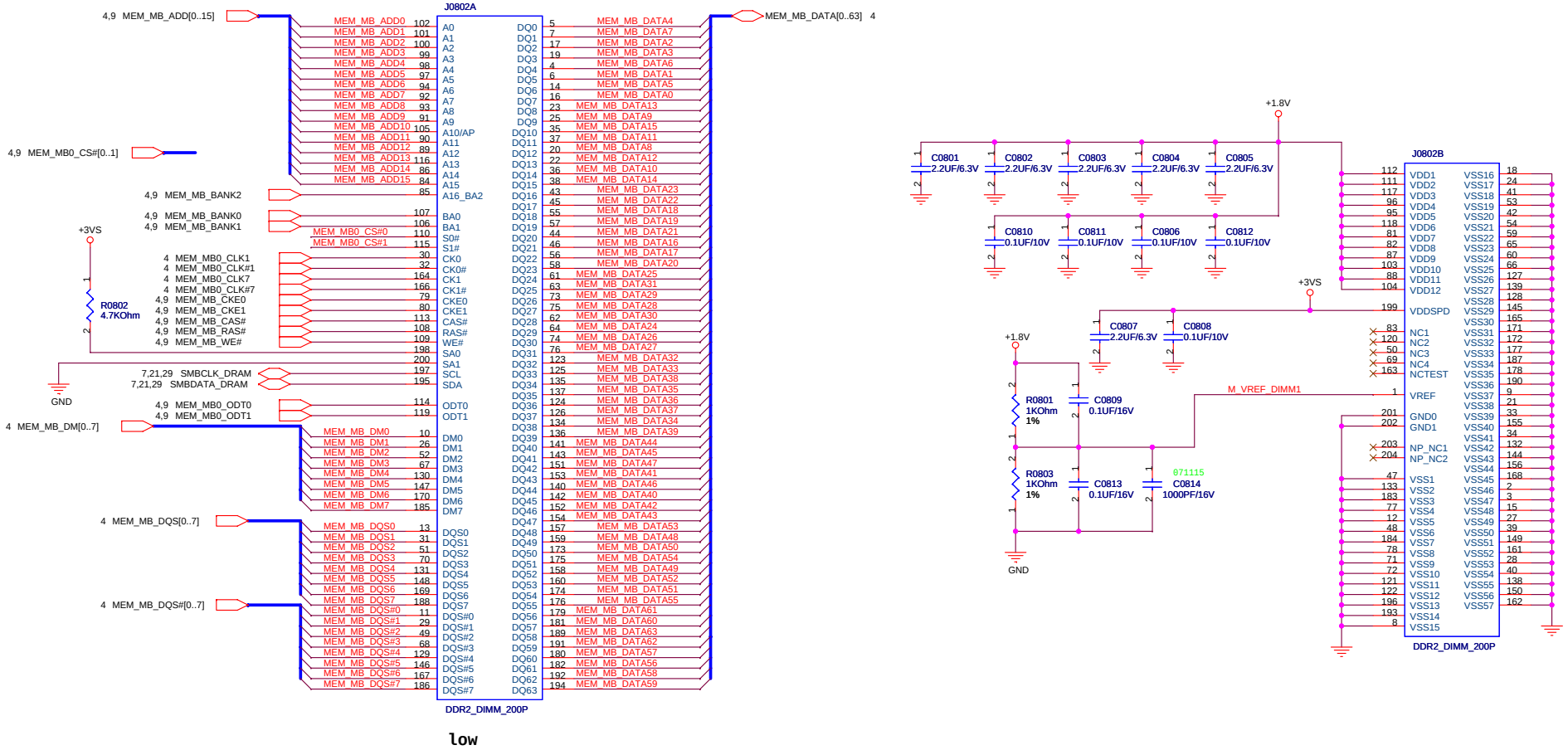


ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/Ta	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 6 of 93	

20080716 Change to 12G025C22004

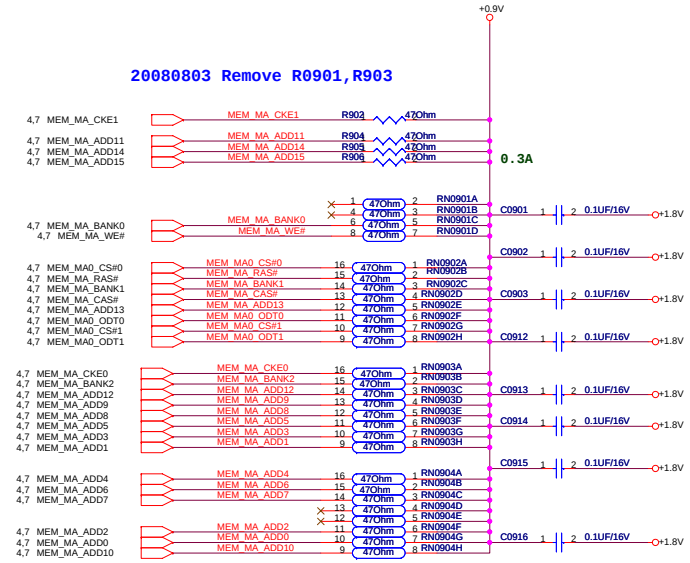


Title : DDR2 SO-DIMM0			
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50Tr/Ta		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 7 of 93		

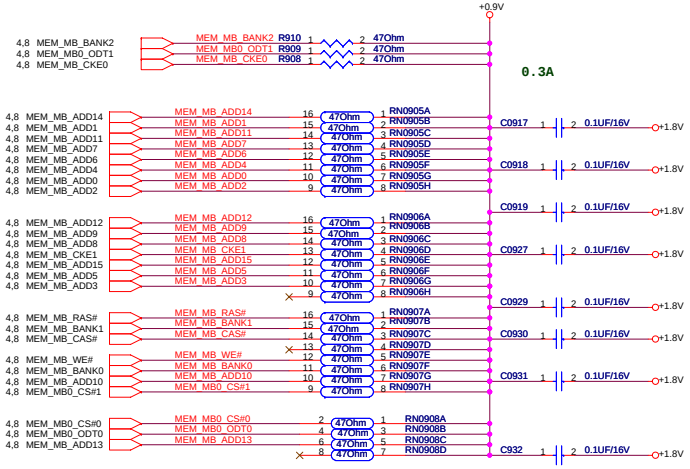


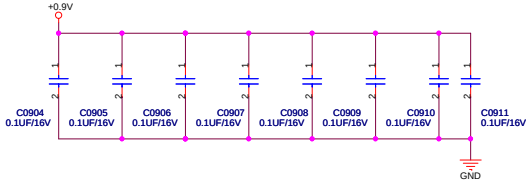
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50Tr/Ta		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 8 of 93		

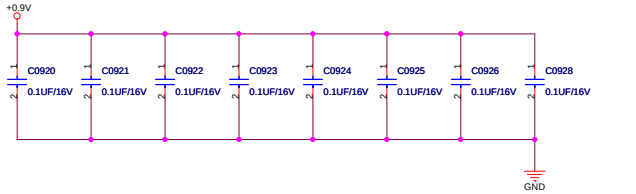
20080803 Remove R0901,R903

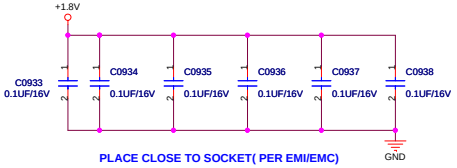


20080803 Remove R907



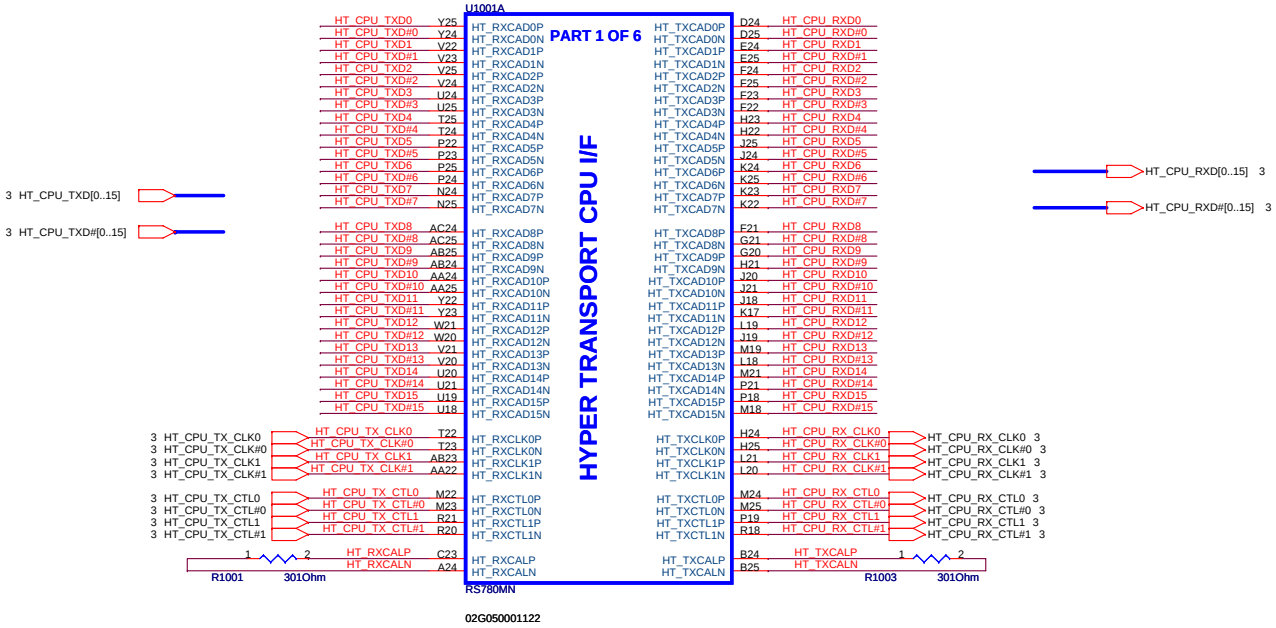






PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC. NB1	Title : DDR2_TERMINATIONS		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50Tr/Ta		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 9 of 93		



02G050001122

ASUSTeK COMPUTER INC. NB1	Title : RS780M-HT LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/Ta	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 10 of 93	

PCI-E:
0~3 HDMI@ RS780M
4~7 NC
8~15 VGA8x

Refer to RS780M datasheet Table 3-10

Caps on VGA card

PCIENB_RXN[0..15] 71
PCIENB_RXP[0..15] 71

U1001B

PART 2 OF 6

PCIE I/F GFX

PCIENB_RXP15 D4 GFX_RX0P
PCIENB_RXN15 C4 GFX_RX0N
PCIENB_RXP14 A3 GFX_RX1P
PCIENB_RXN14 B3 GFX_RX1N
PCIENB_RXP13 C2 GFX_RX2P
PCIENB_RXN13 C1 GFX_RX2N
PCIENB_RXP12 E5 GFX_RX3P
PCIENB_RXN12 F5 GFX_RX3N
PCIENB_RXP11 G5 GFX_RX4P
PCIENB_RXN11 G6 GFX_RX4N
PCIENB_RXP10 H5 GFX_RX5P
PCIENB_RXN10 H6 GFX_RX5N
PCIENB_RXP9 J6 GFX_RX6P
PCIENB_RXN9 J5 GFX_RX6N
PCIENB_RXP8 J7 GFX_RX7P
PCIENB_RXN8 J8 GFX_RX7N
PCIENB_RXP7 L5 GFX_RX8P
PCIENB_RXN7 L6 GFX_RX8N
PCIENB_RXP6 M8 GFX_RX9P
PCIENB_RXN6 L8 GFX_RX9N
PCIENB_RXP5 P7 GFX_RX10P
PCIENB_RXN5 M7 GFX_RX10N
PCIENB_RXP4 P5 GFX_RX11P
PCIENB_RXN4 M5 GFX_RX11N
PCIENB_RXP3 R8 GFX_RX12P
PCIENB_RXN3 P8 GFX_RX12N
PCIENB_RXP2 R6 GFX_RX13P
PCIENB_RXN2 R5 GFX_RX13N
PCIENB_RXP1 P4 GFX_RX14P
PCIENB_RXN1 P3 GFX_RX14N
PCIENB_RXP0 T4 GFX_RX15P
PCIENB_RXN0 T3 GFX_RX15N

GFX_TX0P A5 PCIENB_TXP15
GFX_TX0N B5 PCIENB_TXN15
GFX_TX1P A4 PCIENB_TXP14
GFX_TX1N B4 PCIENB_TXN14
GFX_TX2P C3 PCIENB_TXP13
GFX_TX2N B2 PCIENB_TXN13
GFX_TX3P D1 PCIENB_TXP12
GFX_TX3N D2 PCIENB_TXN12
GFX_TX4P E2 PCIENB_TXP11
GFX_TX4N E1 PCIENB_TXN11
GFX_TX5P F4 PCIENB_TXP10
GFX_TX5N F3 PCIENB_TXN10
GFX_TX6P F1 PCIENB_TXP9
GFX_TX6N F2 PCIENB_TXN9
GFX_TX7P H4 PCIENB_TXP8
GFX_TX7N H3 PCIENB_TXN8
GFX_TX8P H1 PCIENB_TXP7
GFX_TX8N H2 PCIENB_TXN7
GFX_TX9P J2 PCIENB_TXP6
GFX_TX9N J1 PCIENB_TXN6
GFX_TX10P K4 PCIENB_TXP5
GFX_TX10N K3 PCIENB_TXN5
GFX_TX11P K1 PCIENB_TXP4
GFX_TX11N K2 PCIENB_TXN4
GFX_TX12P M4 PCIENB_TXP3
GFX_TX12N M3 PCIENB_TXN3
GFX_TX13P M1 PCIENB_TXP2
GFX_TX13N M2 PCIENB_TXN2
GFX_TX14P N2 PCIENB_TXP1
GFX_TX14N N1 PCIENB_TXN1
GFX_TX15P P1 PCIENB_TXP0
GFX_TX15N P2 PCIENB_TXN0

PCIENB_TXN0 C1142 2 1 0.1UF/10V PCIEG_RXN0
PCIENB_TXN1 C1144 2 1 0.1UF/10V PCIEG_RXN1
PCIENB_TXN2 C1141 2 1 0.1UF/10V PCIEG_RXN2
PCIENB_TXN3 C1148 2 1 0.1UF/10V PCIEG_RXN3
PCIENB_TXN4 C1145 2 1 0.1UF/10V PCIEG_RXN4
PCIENB_TXN5 C1147 2 1 0.1UF/10V PCIEG_RXN5
PCIENB_TXN6 C1143 2 1 0.1UF/10V PCIEG_RXN6
PCIENB_TXN7 C1146 2 1 0.1UF/10V PCIEG_RXN7
PCIENB_TXN8 C1119 2 1 0.1UF/10V PCIEG_RXN8
PCIENB_TXN9 C1120 2 1 0.1UF/10V PCIEG_RXN9
PCIENB_TXN10 C1121 2 1 0.1UF/10V PCIEG_RXN10
PCIENB_TXN11 C1122 2 1 0.1UF/10V PCIEG_RXN11
PCIENB_TXN12 C1123 2 1 0.1UF/10V PCIEG_RXN12
PCIENB_TXN13 C1124 2 1 0.1UF/10V PCIEG_RXN13
PCIENB_TXN14 C1125 2 1 0.1UF/10V PCIEG_RXN14
PCIENB_TXN15 C1126 2 1 0.1UF/10V PCIEG_RXN15

71 PCIEG_RXN[0..15]

PCIENB_TXP0 C1149 2 1 0.1UF/10V PCIEG_RXP0
PCIENB_TXP1 C1150 2 1 0.1UF/10V PCIEG_RXP1
PCIENB_TXP2 C1151 2 1 0.1UF/10V PCIEG_RXP2
PCIENB_TXP3 C1156 2 1 0.1UF/10V PCIEG_RXP3
PCIENB_TXP4 C1152 2 1 0.1UF/10V PCIEG_RXP4
PCIENB_TXP5 C1155 2 1 0.1UF/10V PCIEG_RXP5
PCIENB_TXP6 C1153 2 1 0.1UF/10V PCIEG_RXP6
PCIENB_TXP7 C1154 2 1 0.1UF/10V PCIEG_RXP7
PCIENB_TXP8 C1133 2 1 0.1UF/10V PCIEG_RXP8
PCIENB_TXP9 C1134 2 1 0.1UF/10V PCIEG_RXP9
PCIENB_TXP10 C1135 2 1 0.1UF/10V PCIEG_RXP10
PCIENB_TXP11 C1136 2 1 0.1UF/10V PCIEG_RXP11
PCIENB_TXP12 C1137 2 1 0.1UF/10V PCIEG_RXP12
PCIENB_TXP13 C1138 2 1 0.1UF/10V PCIEG_RXP13
PCIENB_TXP14 C1139 2 1 0.1UF/10V PCIEG_RXP14
PCIENB_TXP15 C1140 2 1 0.1UF/10V PCIEG_RXP15

71 PCIEG_RXP[0..15]

PCIE I/F GPP

53 PCIE_RXP0_TV AE3 GPP_RX0P
53 PCIE_RXN0_TV AD4 GPP_RX0N
33 PCIE_RXP1_LAN AE2 GPP_RX1P
33 PCIE_RXN1_LAN AD3 GPP_RX1N
53 PCIE_RXP3_WLAN AD1 GPP_RX2P
53 PCIE_RXN3_WLAN AD2 GPP_RX2N
43 PCIE_RXP2_NEWCARD V5 GPP_RX3P
43 PCIE_RXN2_NEWCARD W6 GPP_RX3N
U5 GPP_RX4P
U6 GPP_RX4N
U8 GPP_RX5P
U7 GPP_RX5N

GPP_TX0P AC1 GPP_TX0P_C C1101 2 1 0.1UF/10V C1103 2 1 0.1UF/10V PCIE_TXP0_TV 53
GPP_TX0N AC2 GPP_TX0N_C PCIE_TXN0_TV 53
GPP_TX1P AB4 GPP_TX1P_C C1102 2 1 0.1UF/10V C1105 2 1 0.1UF/10V PCIE_TXP1_LAN 33
GPP_TX1N AB3 GPP_TX1N_C PCIE_TXN1_LAN 33
GPP_TX2P AA2 GPP_TX3P_C C1128 2 1 0.1UF/10V C1129 2 1 0.1UF/10V PCIE_TXP3_WLAN 53
GPP_TX2N AA1 GPP_TX3N_C PCIE_TXN3_WLAN 53
GPP_TX3P Y1 GPP_TX2P_C C1104 2 1 0.1UF/10V C1106 2 1 0.1UF/10V PCIE_TXP2_NEWCARD 43
GPP_TX3N Y2 GPP_TX2N_C PCIE_TXN2_NEWCARD 43
GPP_TX4P Y4
GPP_TX4N Y3
GPP_TX5P V1
GPP_TX5N V2

PCIE I/F SB

20 PCIE_SB_NB_RX0P AA8 SB_RX0P
20 PCIE_SB_NB_RX0N Y8 SB_RX0N
20 PCIE_SB_NB_RX1P AA7 SB_RX1P
20 PCIE_SB_NB_RX1N Y7 SB_RX1N
20 PCIE_SB_NB_RX2P AA5 SB_RX2P
20 PCIE_SB_NB_RX2N AA6 SB_RX2N
20 PCIE_SB_NB_RX3P W5 SB_RX3P
20 PCIE_SB_NB_RX3N Y5 SB_RX3N

SB_TX0P AD7 A_TX0P_C C1107 2 1 0.1UF/10V C1109 2 1 0.1UF/10V PCIE_NB_SB_TX0P 20
SB_TX0N AE7 A_TX0N_C PCIE_NB_SB_TX0N 20
SB_TX1P AE6 A_TX1P_C C1108 2 1 0.1UF/10V C1112 2 1 0.1UF/10V PCIE_NB_SB_TX1P 20
SB_TX1N AD6 A_TX1N_C PCIE_NB_SB_TX1N 20
SB_TX2P AB6 A_TX2P_C C1110 2 1 0.1UF/10V C1114 2 1 0.1UF/10V PCIE_NB_SB_TX2P 20
SB_TX2N AC6 A_TX2N_C PCIE_NB_SB_TX2N 20
SB_TX3P AD5 A_TX3P_C C1111 2 1 0.1UF/10V C1116 2 1 0.1UF/10V PCIE_NB_SB_TX3P 20
SB_TX3N AE5 A_TX3N_C PCIE_NB_SB_TX3N 20

AC8 1.27KOHM 1 2 R1101
AB8 2KOHM 1 2 R1102 +1.1V_NB

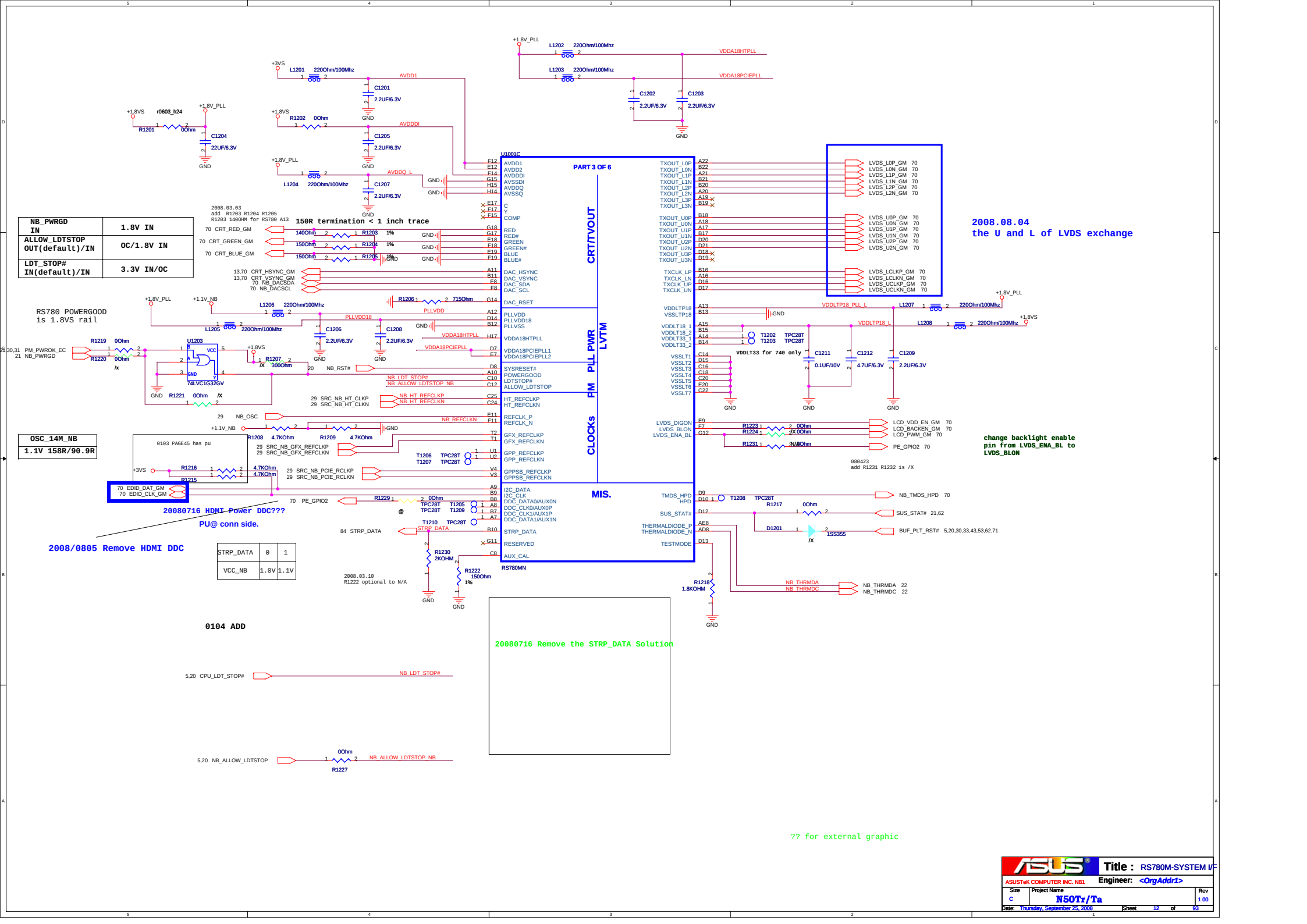
PCE_CALRP
PCE_CALRN

GND

RS780MN

080712 ADD 3G
0427:change wlan and newcard lane

ASUSTeK COMPUTER INC. NB1	Title : RS780M-PCIE LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50Tr/Ta		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 11 of 93		



NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

OSC_14M_NB
1.1V 158R/90.9R

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

2008.03.03
add R1203 R1204 R1205
R1203 1480HM for RS780 A13

150R termination < 1 inch trace

RS780 POWERGOOD
is 1.8VS rail

0103 PAGE45 has pu

2008.03.10
R1222 optional to N/A

2008.08.04
the U and L of LVDS exchange

change backlight enable
pin from LVDS_ENA_BL to
LVDS_BLON

080423
add R1231 R1232 is /X

20080716 HDMI Power DDC???
PU@ conn side.

2008/0805 Remove HDMI DDC

0104 ADD

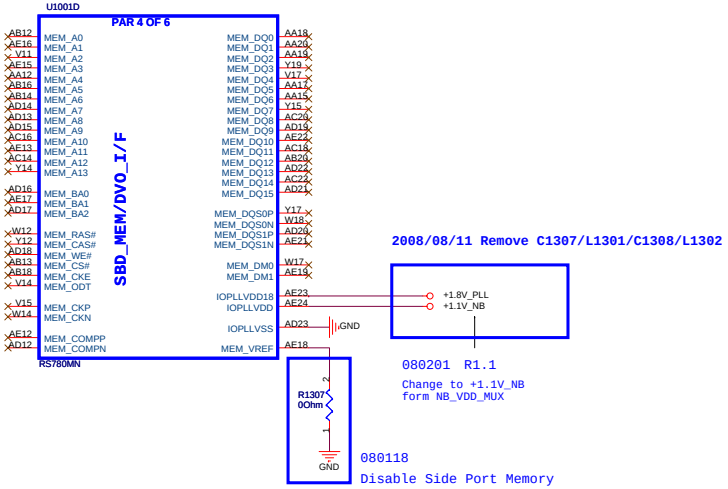
20080716 Remove the STRP_DATA Solution

?? for external graphic

Title : RS780M-SYSTEM I/F		
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: C	Project Name: N50Tr/Ta	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 12 of 93	

R1.11 080319

Change the NB Part number to RS780 (A13)



2008/08/11 Remove C1307/L1301/C1308/L1302

080201 R1.1

Change to +1.1V_NB
form NB_VDD_MUX

080118

Disable Side Port Memory

R1.1

DFT_GPIO1: LOAD_EEPROM_STRAPS

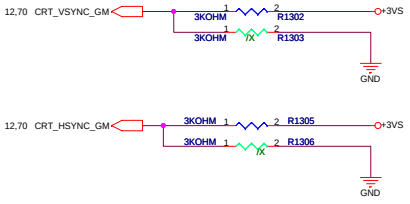
```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

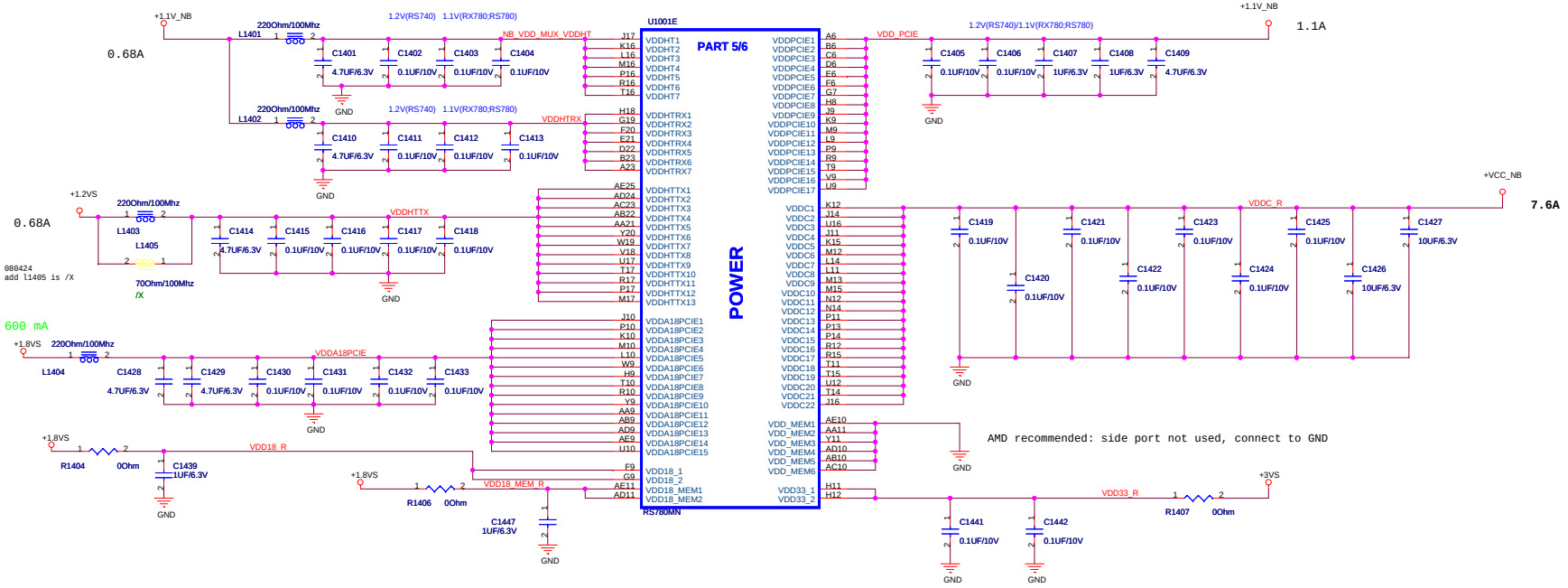
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

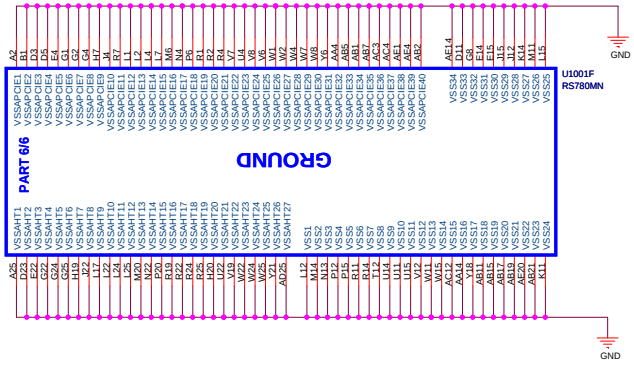
```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



ASUSTeK COMPUTER INC. NB1	Title : RS780M-SPMEM/STRAPS	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50Tr/Ta	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 13 of 93	



3.3V rails ramp high relative to 1.8V
Display and PLL rails. max 2.1V



ASUSTeK COMPUTER INC. NB1	Title : RS780M-POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name: N50Tr/Ta		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 14 of 93		

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 15 of 93	

ASUSTeK COMPUTER INC		Title : BLANK			
		Engineer:			
Size	Project Name				Rev
A	N50Tr/TA				1.00
Date: Thursday, September 25, 2008			Sheet 16 of 93		

ASUSTeK COMPUTER INC	Title : BLANK			
	Engineer:			
Size: A	Project Name: N50Tr/TA			Rev: 1.00
Date: Thursday, September 25, 2008		Sheet 17 of 93		

Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:	
Size A	Project Name **N50Tr/TA**	Rev 1.00
Date: Thursday, September 25, 2008	Sheet 18 of 93	

Title : BLANK

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A	N50Tr/TA	1.00

Date: Thursday, September 25, 2008 Sheet 19 of 93

2008/08/11 AMD Review

PCI_AD23 1 T2044 TPC28T
PCI_AD24 1 T2047 TPC28T
PCI_AD25 1 T2049 TPC28T
PCI_AD26 1 T2050 TPC28T
PCI_AD27 1 T2051 TPC28T
PCI_AD28 1 T2052 TPC28T

0108 change R2008 TO 22 ohm

REMOVE TPM FUNCTION

T2048 TPC28T

A_RST# R2029 0Ohm N2

U2001A

SB700
Part 1 of 5

A_RST#

11 PCIE_SB_NB_RX0P C2001 0.1UF/10V A_RX0P_C V23
11 PCIE_SB_NB_RX0N C2008 0.1UF/10V A_RX0N_C V22
11 PCIE_SB_NB_RX1P C2007 0.1UF/10V A_RX1P_C V24
11 PCIE_SB_NB_RX1N C2002 0.1UF/10V A_RX1N_C V25
11 PCIE_SB_NB_RX2P C2009 0.1UF/10V A_RX2P_C U25
11 PCIE_SB_NB_RX2N C2003 0.1UF/10V A_RX2N_C U24
11 PCIE_SB_NB_RX3P C2010 0.1UF/10V A_RX3P_C T23
11 PCIE_SB_NB_RX3N C2004 0.1UF/10V A_RX3N_C T22

PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N

11 PCIE_NB_SB_TX0P U22
11 PCIE_NB_SB_TX0N U21
11 PCIE_NB_SB_TX1P U19
11 PCIE_NB_SB_TX1N V19
11 PCIE_NB_SB_TX2P R20
11 PCIE_NB_SB_TX2N R21
11 PCIE_NB_SB_TX3P R18
11 PCIE_NB_SB_TX3N R17

PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N

+1.2VS
220Ohm/100Mhz
L2001
0104 CHANGE P/N

PCIE_VDDR R2005 1% 562Ohm PCIE_CALRP T25
GND R2004 2.05KOHM 1% PCIE_CALRN T24

PCIE_CALRP PCIE_CALRN

PCIE_PVDD_L P24
C2005 10UF/6.3V C2006 1UF/6.3V P25

PCIE_PVDD PCIE_PVSS

PCI EXPRESS INTERFACE

PCI CLKS

PCICLK0 P4 CLK_TPMPCI_R R2002 22Ohm CLK_TPMPCI 62
PCICLK1 P3 CLK_KBCPCI_R R2003 22Ohm CLK_CBPCI 40
PCICLK2 P1 CLK_DBGPCI2_R R2009 0Ohm CLK_SIOPCI 24
PCICLK3 P2 CLK_DBGPCI1_R R2008 22Ohm PCI_CLK3 24,44
PCICLK4 T4 PCI_CLK4_R R2036 0Ohm PCI_CLK4 24
PCICLK5/GPIO41 T3 PCI_CLK5_R R2037 0Ohm PCI_CLK5 24

2008.03.05
R2009 R2036 R2037 PN to 10G212000004010

PCIRST# N1 R2034 33Ohm PCI_RST# 40

PCI_AD[31:0] 40

AD0 U2 PCI_AD0
AD1 P7 PCI_AD1
AD2 V4 PCI_AD2
AD3 T1 PCI_AD3
AD4 V3 PCI_AD4
AD5 U1 PCI_AD5
AD6 V1 PCI_AD6
AD7 V2 PCI_AD7
AD8 T2 PCI_AD8
AD9 W1 PCI_AD9
AD10 T9 PCI_AD10
AD11 R6 PCI_AD11
AD12 R7 PCI_AD12
AD13 R5 PCI_AD13
AD14 U8 PCI_AD14
AD15 U5 PCI_AD15
AD16 Y7 PCI_AD16
AD17 W8 PCI_AD17
AD18 V9 PCI_AD18
AD19 Y8 PCI_AD19
AD20 AA8 PCI_AD20
AD21 Y4 PCI_AD21
AD22 Y3 PCI_AD22
AD23 Y2 PCI_AD23
AD24 AA2 PCI_AD24
AD25 AB4 PCI_AD25
AD26 AA1 PCI_AD26
AD27 AB3 PCI_AD27
AD28 AB2 PCI_AD28
AD29 AC1 PCI_AD29
AD30 AC2 PCI_AD30
AD31 AD1 PCI_AD31

PCI_C/BE#[3:0] PCI_C/BE#[3:0] 40

CBE0# W2 PCI_C/BE#0
CBE1# U7 PCI_C/BE#1
CBE2# AA7 PCI_C/BE#2
CBE3# Y1 PCI_C/BE#3

FRAME# AA6 PCI_FRAME# PCI_FRAME# 40
DEVSEL# W5 PCI_DEVSEL# PCI_DEVSEL# 40
IRDY# AA5 PCI_IRDY# PCI_IRDY# 40
TRDY# Y5 PCI_TRDY# PCI_TRDY# 40
PAR U6 PCI_PAR PCI_PAR 40
STOP# W6 PCI_STOP# PCI_STOP# 40
PERR# W4 PCI_PERR# PCI_PERR# 40
SERR# V7 PCI_SERR# PCI_SERR# 40

REQ0# AC3 PCI_REQ#0 PCI_REQ#0 40
REQ1# AD4 PCI_REQ#1 T2042 TPC28T
REQ2# AB7 PCI_REQ#2 T2043 TPC28T R2038
REQ3#/GPIO70 AE6
REQ4#/GPIO71 AB6 PCI_REQ#4 T2045 TPC28T

INT_VGA_TV_EN# 70
08.07.22

GNT0# AD2 PCI_GNT#0
GNT1# AE4 PCI_GNT#1 T2038 TPC28T
GNT2# AD5 PCI_GNT#2 T2039 TPC28T 20080716 ADD PE_GPIO1
GNT3#/GPIO72 AC6
GNT4#/GPIO73 AE5 PCI_GNT#4 T2041 TPC28T
CLKRUN# AD6 PM_CLKRUN# T2037 TPC28T
LOCK# V5

PCI_GNT#0 40
PE_GPIO1 72
PM_CLKRUN# 30,40,62

internal Pull Up 8.2K

INTE#/GPIO33 AD3 PCI_INTA#
INTF#/GPIO34 AC4 PCI_INTB#
INTG#/GPIO35 AE2 PCI_INTC# T2046 TPC28T
INTH#/GPIO36 AE3 PCI_INTD#

PCI_INTA# 40
PCI_INTB# 40
20080716 ADD PE_GPIO0
PE_GPIO0 71

+3VS
PCI_INTA# R2007 2.2kOHM
PCI_INTB# R2006 2.2kOHM

PCI INTERFACE

C2017 15PF/50V CLK_TPMPCI
C2018 15PF/50V CLK_CBPCI
C2019 15PF/50V CLK_SIOPCI
C2020 15PF/50V PCI_CLK3
C2021 15PF/50V LPC_CLKDEBUG
C2022 15PF/50V LPC_CLKEC
GND

0109

2008.03.11
C2018之C2019之C2020之C2017之C2021之 C2022 change to 15pf,optional is N/A

29 SRC_SB_PCIE_RCLKP N25 PCIE_RCLKP/NB_LNK_CLKP
29 SRC_SB_PCIE_RCLKN N24 PCIE_RCLKN/NB_LNK_CLKN

T2017 TPC28T T2018 TPC28T K23 NB_DISP_CLKP K22 NB_DISP_CLKN
T2019 TPC28T T2020 TPC28T M24 NB_HT_CLKP M25 NB_HT_CLKN
T2021 TPC28T T2022 TPC28T P17 CPU_HT_CLKP M18 CPU_HT_CLKN
T2023 TPC28T T2024 TPC28T M23 SLT_GFX_CLKP M22 SLT_GFX_CLKN
T2025 TPC28T T2026 TPC28T J19 GPP_CLK0P J18 GPP_CLK0N
T2027 TPC28T T2028 TPC28T L20 GPP_CLK1P L19 GPP_CLK1N
T2029 TPC28T T2030 TPC28T M19 GPP_CLK2P M20 GPP_CLK2N
T2031 TPC28T T2032 TPC28T N22 GPP_CLK3P P22 GPP_CLK3N
T2033 TPC28T L18 25M_48M_66M_OSC
T2034 TPC28T J21 25M_X1
T2035 TPC28T J20 25M_X2

CLOCK GENERATOR

32K_XIN A3 X1
32K_XOUT B3 X2

RTC XTAL

LPCCLK0 G22 LPC_CLK0_R R2023 22Ohm LPC_CLKDEBUG 24,44
LPCCLK1 E22 LPC_CLK1_R R2025 22Ohm LPC_CLKEC 24,30
LAD0 H24 LPC_AD0 30,44,62
LAD1 H23 LPC_AD1 30,44,62
LAD2 J25 LPC_AD2 30,44,62
LAD3 J24 LPC_AD3 30,44,62
LFRAME# H25 LPC_FRAME# 30,44,62
LDRQ0# H22 TPC28T T2036
LDRQ1#/GNT5#/GPIO68 AB8 TPC28T T2014
BMREQ#/REQ5#/GPIO65 AD7 GPIO65 TPC28T T2015
SERIRQ V15 INT_SERIRQ 30,40,62

LPC

+VCC_RTC
R2024 1MOhm
INTRUDER_ALERT#

RTCCLK C3 RTC_CLK 24
INTRUDER_ALERT# C2 INTRUDER_ALERT#
VBAT B2

+VCC_RTC
R2026 510Ohm
C2013 0.1UF/10V
C2014 1UF/6.3V
TPC28T T2016
TF1 TPC28T
JRST1 SGL_JUMP
GND

D2001
+3VA
+RTCBAT
RB715F

R2022 1KOhm 0110 add for safety

R2035 0Ohm

2008.03.03
D2001 R2022 optional change to /X, R2035 change to N/A

J2001 BATT_HOLDER_2P

First:12G20110020C
second:12G201100208
20080723 Change Battery PN

RTC

5 CPU_PWRGD

81 HT_CPU_PWRGD

PMBS3904 Q2000

R2021 10KOhm @
R2020 1KOhm @
+3VS +1.8VS

5,12 NB_ALLOW_LDTSTOP F23 ALLOW_LDTSTP
5 CPU_PROCHOT# F24 PROCHOT# 20080716
F22 LDT_PG
5,12 CPU_LDT_STOP# G25 LDT_STP#
5 CPU_LDT_RST# G24 LDT_RST# 20080716

CPU

080424
add R2042 R2041 R2040

+3V +3VS
R2043 100KOhm
R2039 100KOhm /X
Q2001B UM6K1N
Q2001A UM6K1N

32K_XIN
32K_XOUT
R2027 20MOHM /X
X2001 32.768KHZ SIDE
07G010N23272
R2028 20MOHM
C2015 18PF/50V
C2016 18PF/50V

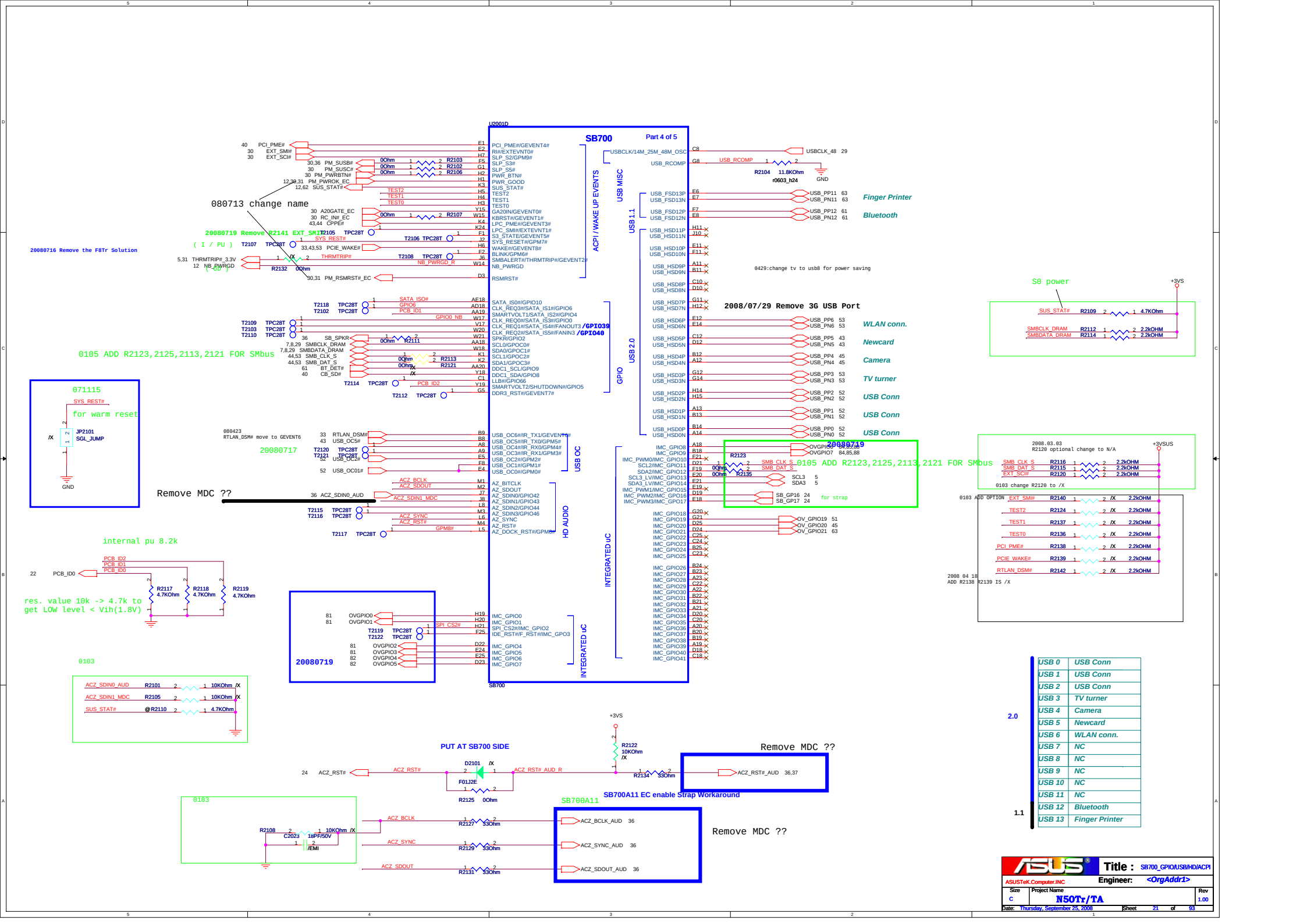
080423
ADD R2039 Q2001

R2030 0Ohm /X
+3VSUS
U2002 74LVC1G17GW
A_RST#
R2031 33Ohm NB_RST# 12
R2033 33Ohm BUF_PLT_RST# 5,12,30,33,43,53,62,71
R2032 8.2KOhm
GND

NB_RST#
C2024 0.1UF/10V @
GND

2008/0805 Add C2024 for NB_RST# Glitch

ASUSTeK.COMPUTER.INC	Title : SB700_CPU/PCIE/LPC/CLK		
	Engineer: <OrgAddr1>		
Size: C	Project Name: N50Tr/TA	Rev: 1.00	
Date: Thursday, September 25, 2008	Sheet 20 of 93		


SB700
Part 4 of 5
U2001D
SB700
080713 change name
20080719 Remove R2141 EXT_SMI#
20080716 Remove the F8Tr Solution
0105 ADD R2123,2125,2113,2121 FOR SMbus
071115
for warm reset
JP2101
SGL_JUMP
Remove MDC ??
20080717
internal pu 8.2k
res. value 10k -> 4.7k to get LOW level < Vih(1.8V)
0103
20080719
PUT AT SB700 SIDE
SB700A11 EC enable Strap Workaround
SB700A11
Remove MDC ??
2008/07/29 Remove 3G USB Port
0429:change tv to usb8 for power saving
S0 power
2008.03.03
R2120 optional change to N/A
0103 change R2120 to /X
0103 ADD OPTION
2008 04 18
ADD R2138 R2139 IS /X
Finger Printer
Bluetooth
WLAN conn.
Newcard
Camera
TV turner
USB Conn
USB Conn
USB Conn
USB 0 USB Conn
USB 1 USB Conn
USB 2 USB Conn
USB 3 TV turner
USB 4 Camera
USB 5 Newcard
USB 6 WLAN conn.
USB 7 NC
USB 8 NC
USB 9 NC
USB 10 NC
USB 11 NC
USB 12 Bluetooth
USB 13 Finger Printer
2.0
1.1
Title : SB700_GPIO/USB/HD/ACPI
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name N50Tr/TA
Rev 1.00
Date: Thursday, September 25, 2008
Sheet 21 of 93

2008.03.03
R2208 R2209 R2210 R2211 R2212 R2213 from 4.99OHM to 0OHM

2008/08/11 Remove R2208/R2209/R2210/R2211/R2212/R2213

for SATA HDD

for SATA ODD

for E- SATA

U2001B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

SB700

Place SATA_CAL
RES very close
to ball of SB700

R2201 1KOhm 1% 1% SATA_CAL

R2205 10MOhm

X2201 25Mhz

C2209 10PF/50V

C2210 10PF/50V

C2211 close
to the ball
of SB700

L2202 220Ohm/100Mhz

C2211 2.2UF/6.3V

C2212 2.2UF/6.3V

C2213 0.1UF/10V

080423
C2211 C2212 TO 2.2U(0603)

L2203 220Ohm/100Mhz

C2216 close
to the ball
of SB700

C2216 1UF/10V

C2217 0.1UF/10V

WLAN_ON# ----> WLAN_ON

BT_ON 61

080712

20080711

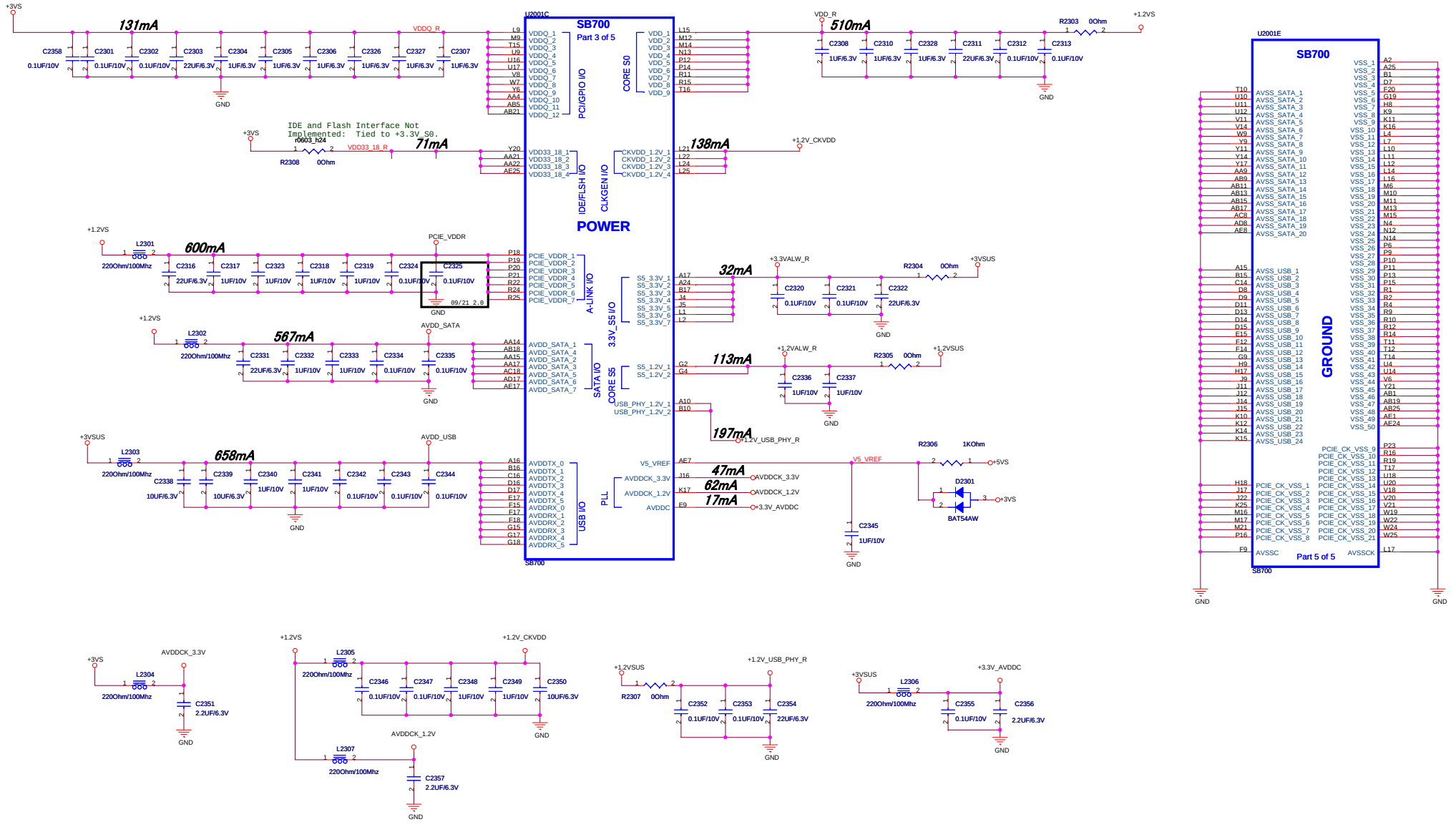
080424
add R2218 R2222 IS /X

C2214 0.1UF/16V

C2215 2.2UF/10V

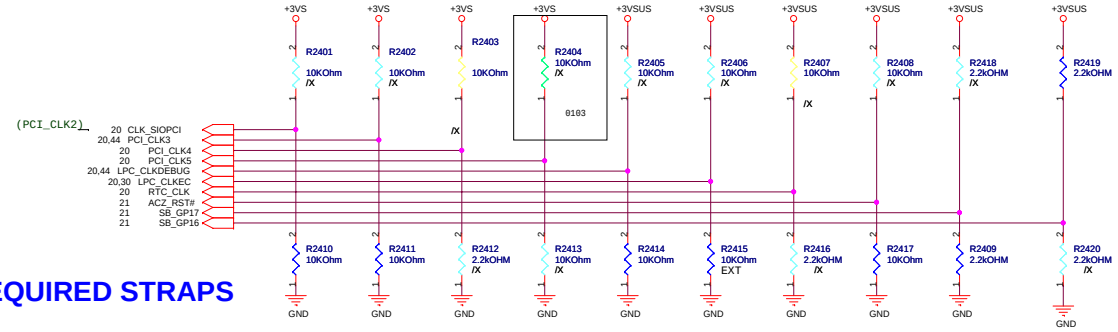
GND trace at
least 10mil
wide

Title :	SB700_PATA/SATA
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>
Size: C	Project Name: N50Tr/TA
Rev: 1.00	
Date: Thursday, September 25, 2008	Sheet 22 of 93



ASUSTeK.COMPUTER.INC	Title : SB700_POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 23 of 93		

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

ASUSTeK.Computer.INC

Title : SB700_STRAP

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	N50Tr/TA	1.00

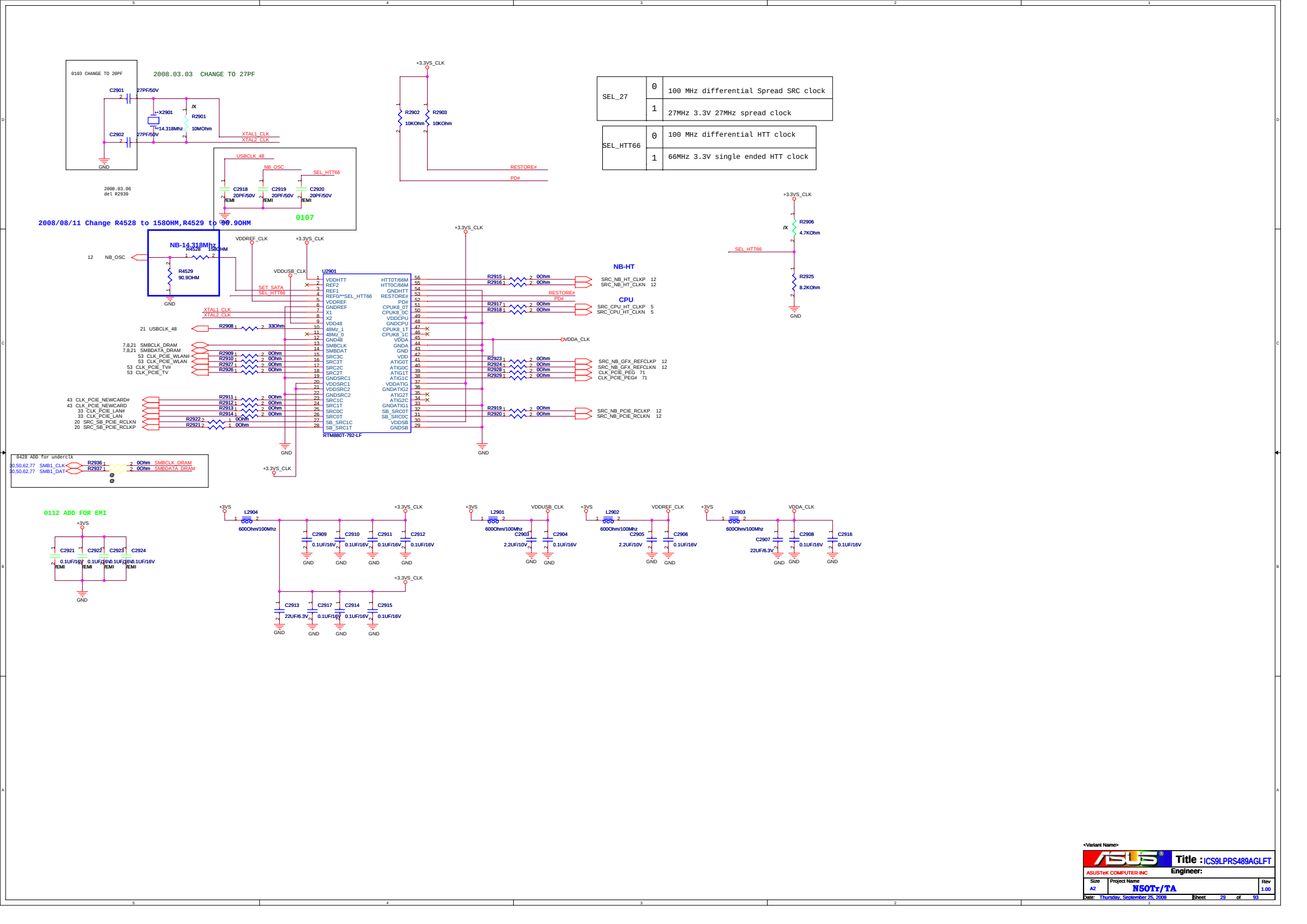
Date: Thursday, September 25, 2008 Sheet 24 of 93

ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 25 of 93	

Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:	
Size: A	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 26 of 93	

ASUS	Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:		
Size A	Project Name N50Tr/TA		Rev 1.00
Date: Thursday, September 25, 2008	Sheet 27 of 93		

ASUSTeK COMPUTER INC		Title : BLANK			
		Engineer:			
Size	Project Name				Rev
A	N50Tr/TA				1.00
Date: Thursday, September 25, 2008		Sheet 28 of 93			



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICS9LPRS489AGLFT

Engineer:

Size	Project Name	Rev
A2	N50Tr/TA	1.00

Date: Thursday, September 25, 2008 Sheet 29 of 93

R2.05

Change RNX3001 from 47 ohm to 0 ohm .The RNX3001 with modification of RN4401 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

080131 R1.1
Check EC power

080130
R1.1
Change EC from IT8752 to IT8512

U3001

LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus

080712 Internet

Batt1
Thermal sensor

R2.0 080401
Un-mount C3018 for ITE suggestion

080204 R1.1
IT8512 I~J

For IT8512 Power

R2.0 080327
Add test point for factory ICT test

R2.01 080411
Change P/N to 09G013120103

For PU / PD

080215 R1.1
change 4.7K P/N from 10G2124720040 to 10G2124720010

080130 R1.1 GPL3

Change pull up resistor from 10K to 47K ohm

071115

080215 change P/N

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

Note:
close to the WRST# (IT8752E pin19)

R2.0 080327
Follow the design IP

11/05

071115
New Thermal Process

For Instant Key

Note: Close to EC

Del COLOREN# Pin at RN3002B 071113

080713 Add Coloren#

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low

R2.0 080327
EPSON advise to use 100K ohm

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

20080717 Vcore Sense

071116
Reserve for current leakage issue (Reference to F5R)

Q3001A
UM6K1N
R3008 33Ohm
Q3001B
UM6K1N
R3010 33Ohm

071129
071120
Decision by resistor

R2.02 080519
Un-Mount R3059 and Q3002 for cost down

071207
AMD review

Q3002
BSS138

U3005
74LVC1G32GV

071116
(Reference to F7KR)

080713 ?????

EC Check (AC Auto Boot Issue)

071113
Change Net name from PM_RSMRST#

080123 R1.1
D3002 1SS355
1KOhm R3052

071113
Change Net name from PM_RSMRST#_EC

071113
Change Net name from PM_PWROK

071203
refer page31.

071113
Change Net name from PM_PWROK_EC

071116
Reserve "Auto power on" solution for ATI Chipset

ASUSTeK COMPUTER INC. NB1
Title : EC_IT8512 (1/2)
Engineer: <OrgAddr1>
Size: Custom
Project Name: N50Tr/TA
Rev: 1.00
Date: Thursday, September 25, 2008
Sheet 30 of 93

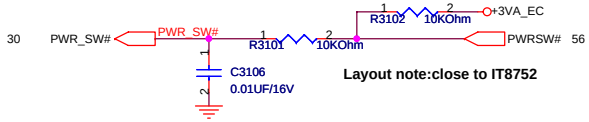
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

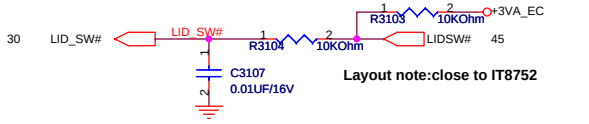
In Page 60

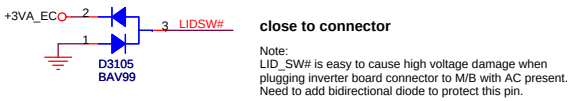
For Switch

PWR SWITCH



LID SWITCH



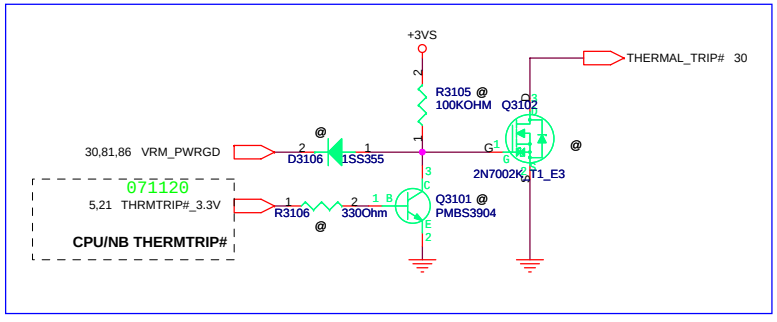


Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

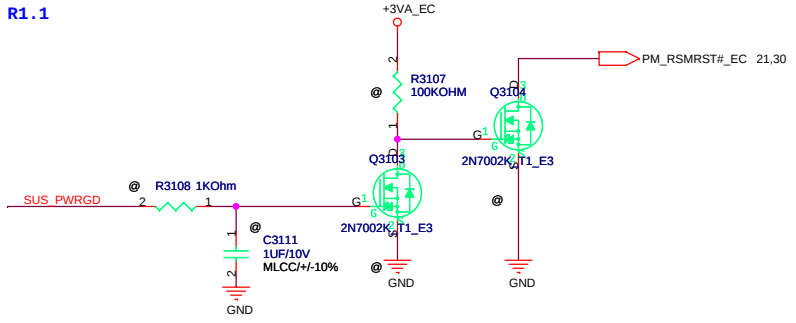
For Thermal Control Method

R2.0 080325

Unmount Thermal_trip component
D3106,R3105,R3106,Q3101, and Q3102, for cost down

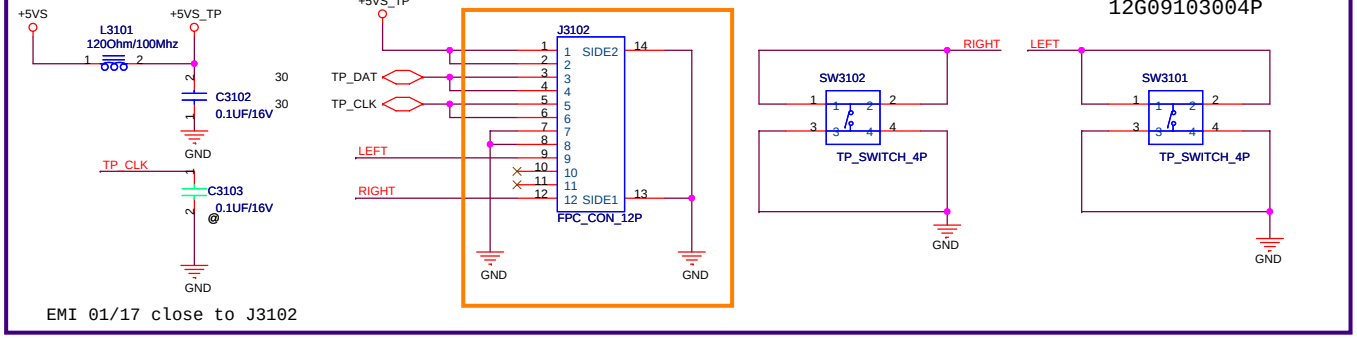


R1.1



080121 Q3103 & Q3104 pin2 and pin3 Reverse
080123 Reserve for SB700 interface

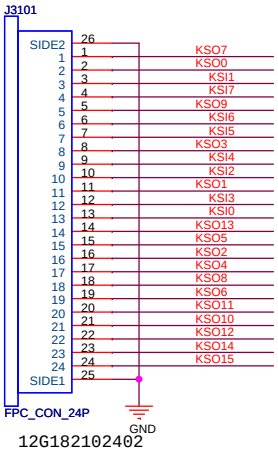
Touchpad Connector



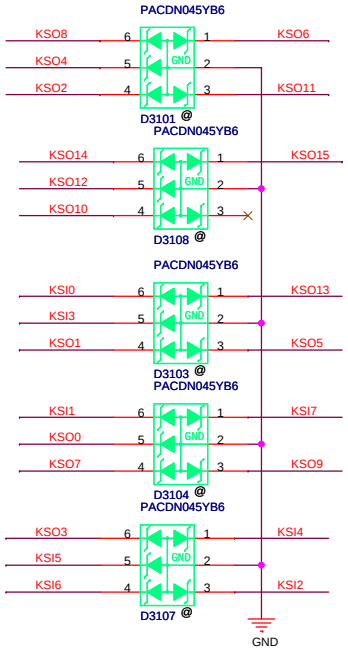
EMI 01/17 close to J3102

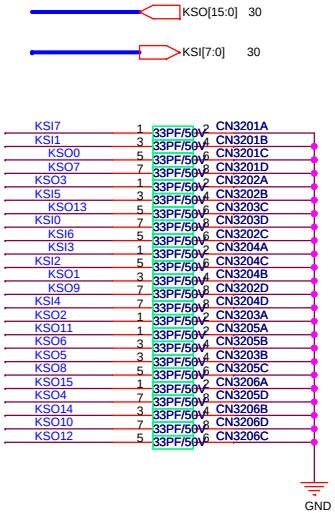
Keyboard Connector

F7/N1 Keyboard



11/02





ASUSTeK COMPUTER INC. NB1

Title : EC_IT8512 (2/2)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50Tr/TA	1.00

Date: Thursday, September 25, 2008 Sheet 31 of 93

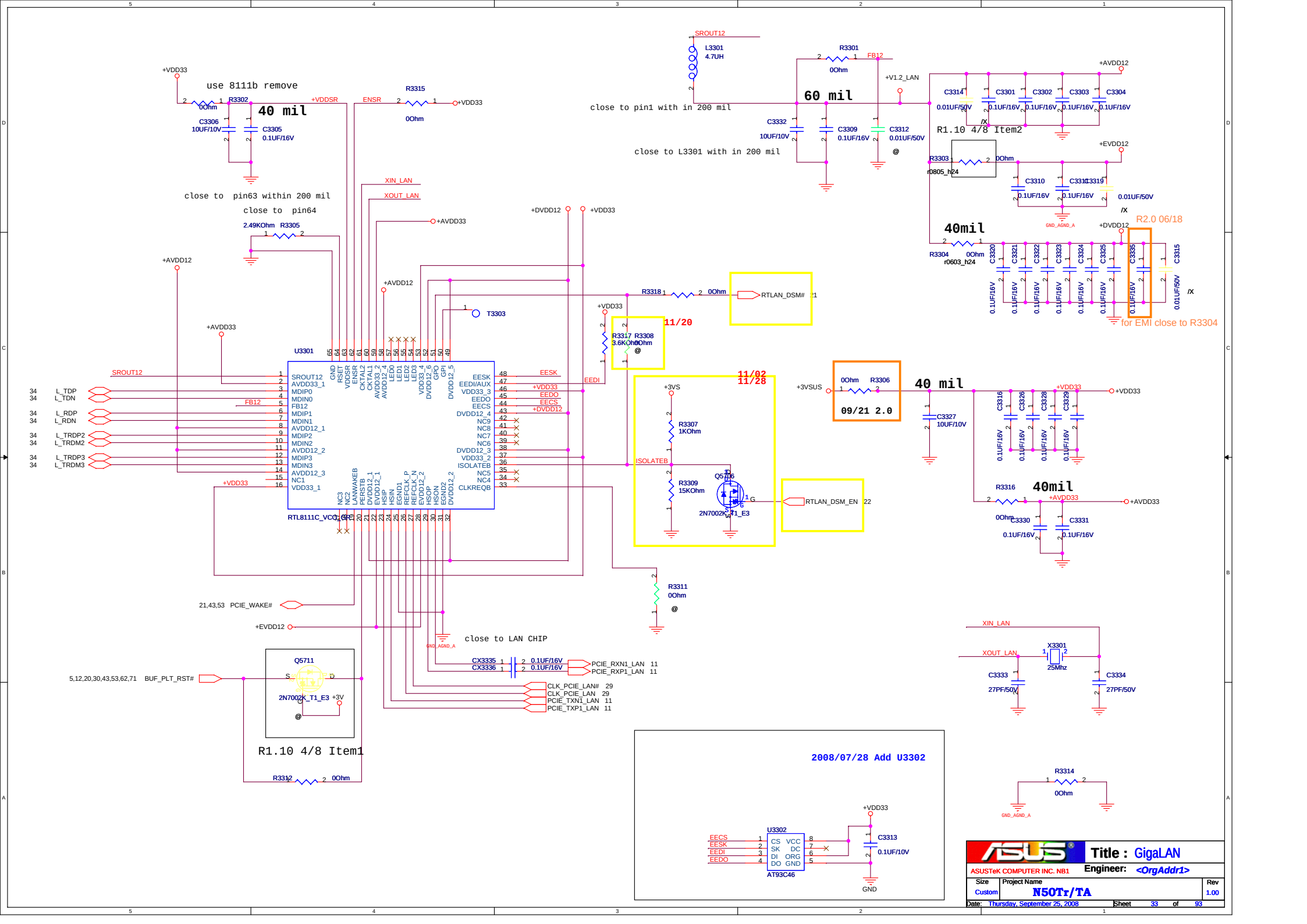
Title : POWER-ON SEQUENCE

ASUSTeK COMPUTER INC. NB1

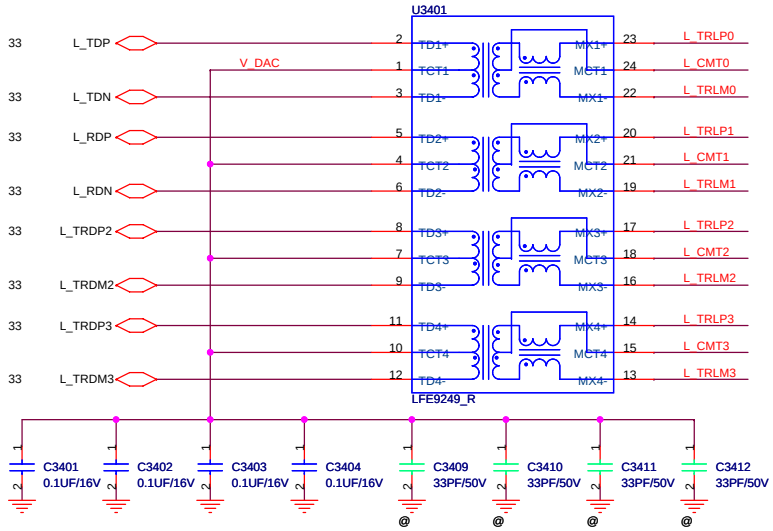
Engineer: <OrgAddr1>

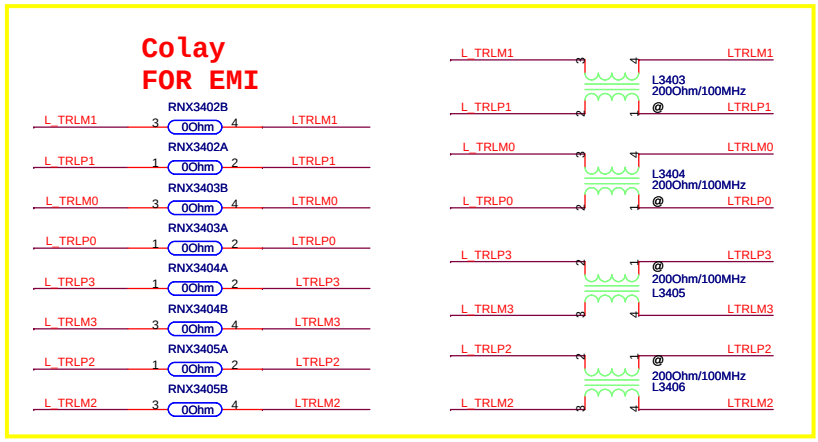
Size	Project Name	Rev
Custom	N50Tr/TA	1.00

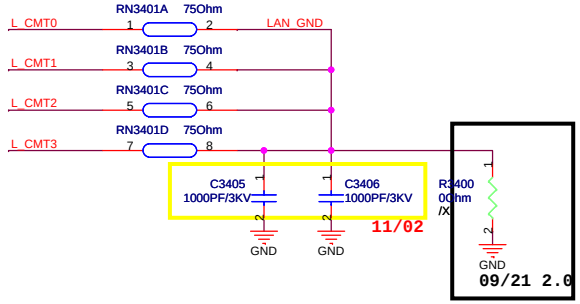
Date: Thursday, September 25, 2008 Sheet 32 of 93

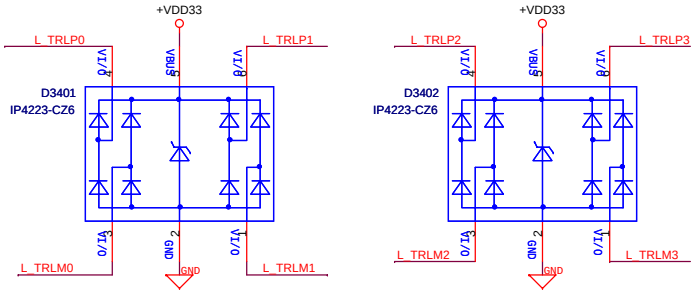

use 8111b remove
40 mil
close to pin63 within 200 mil
close to pin64
close to pin1 with in 200 mil
60 mil
close to L3301 with in 200 mil
R1.10 4/8 Item2
40mil
R2.0 06/18
for EMI close to R3304
11/20
11/02
11/28
09/21 2.0
40 mil
40mil
close to LAN CHIP
R1.10 4/8 Item1
2008/07/28 Add U3302
RTL8111C_VC0_GR
U3301
U3302
Q5706
Q5711
T3303
AT93C46
Title : GigaLAN
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Project Name N50Tr/TA
Rev 1.00
Date: Thursday, September 25, 2008
Sheet 33 of 93

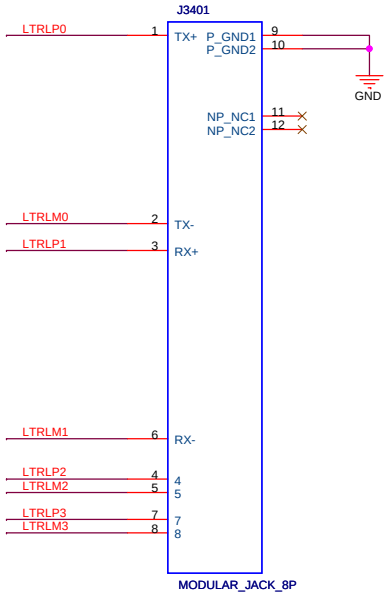
2nd source:09G051059055 GST5009 LF











12G142111083

ASUSTeK COMPUTER INC. NB1		Title : RJ45	
		Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008		Sheet 34 of 93	

R2.0 06/11 remove MDC

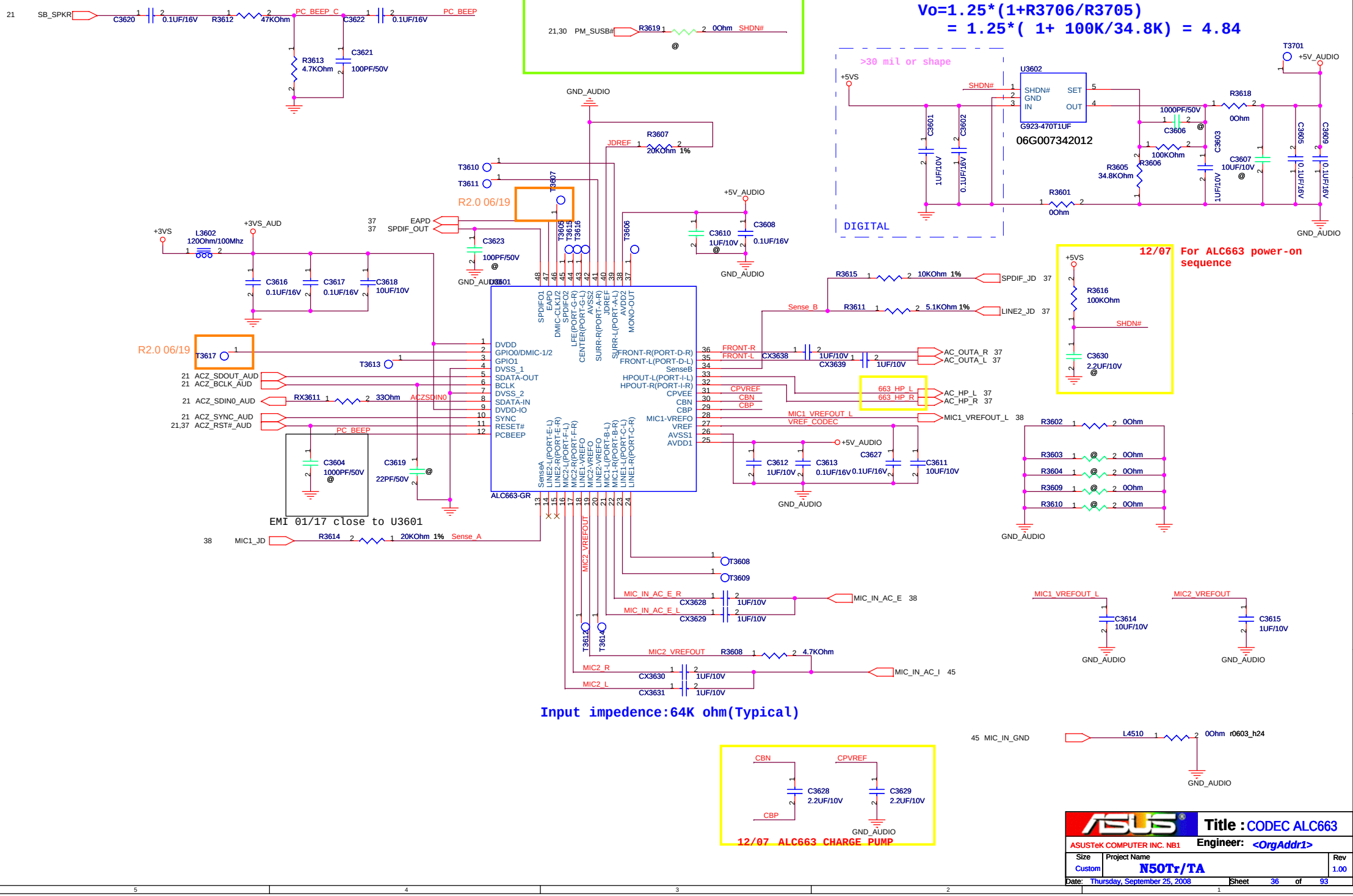
ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 35 of 93	

PC BEEP

update 08/0714

Audio Power

FOR ADJUST MODE:
Vo=1.25*(1+R3706/R3705)
= 1.25*(1+ 100K/34.8K) = 4.84



ASUSTeK COMPUTER INC. NB1

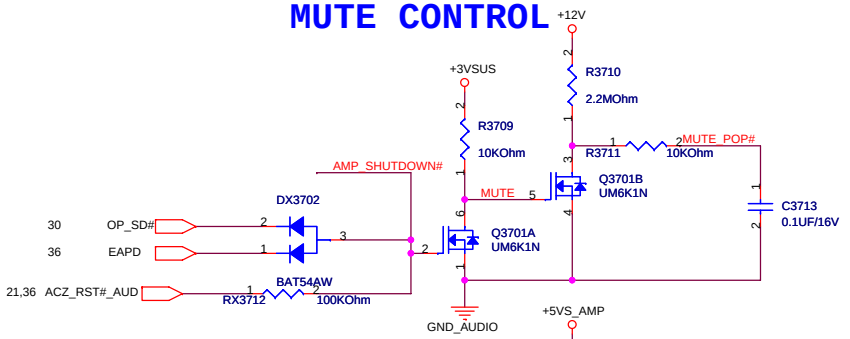
Title : CODEC ALC663

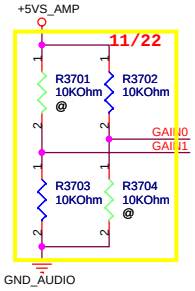
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50Tr/TA	1.00

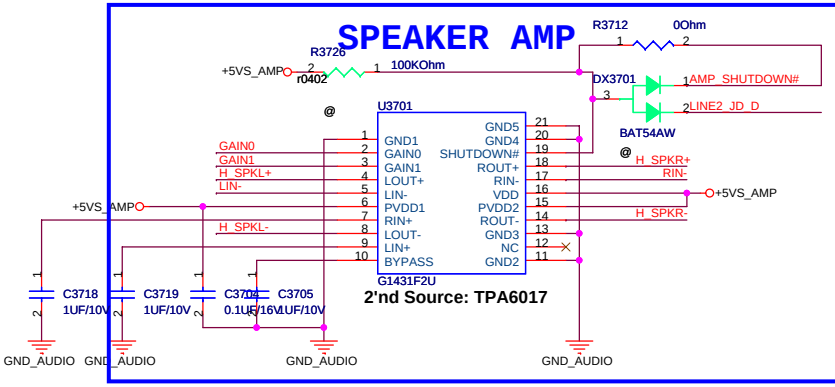
Date: Thursday, September 25, 2008 Sheet 36 of 93

MUTE CONTROL



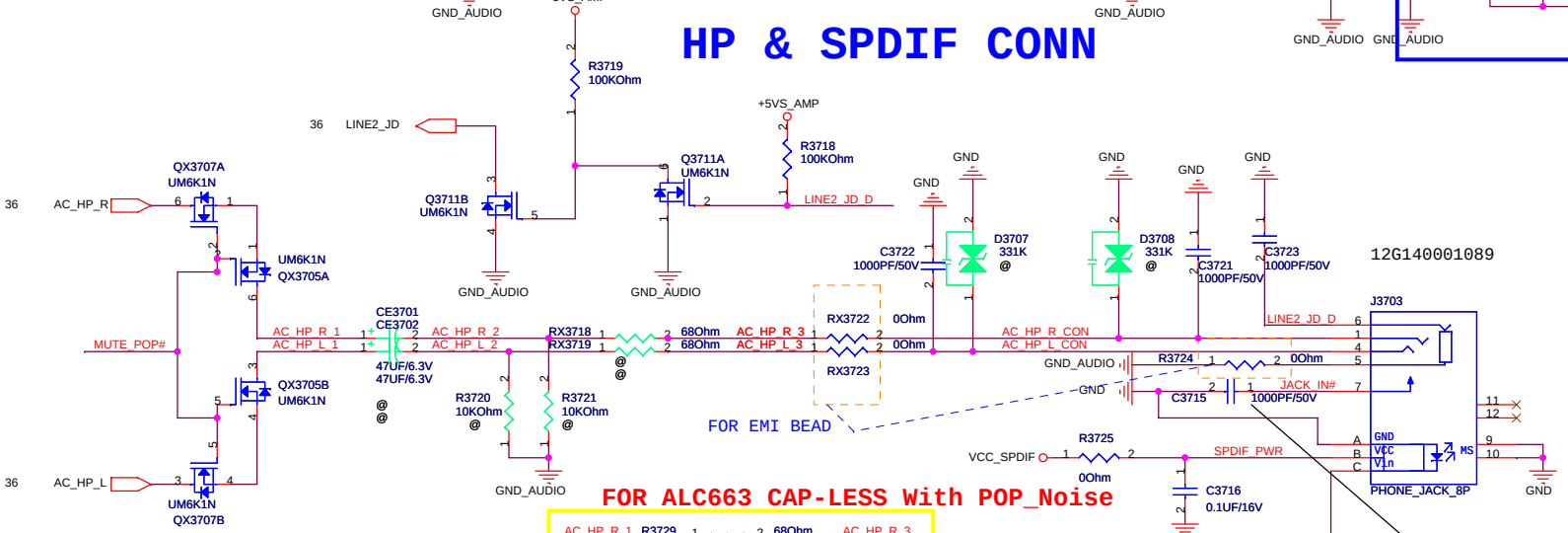


SPEAKER AMP

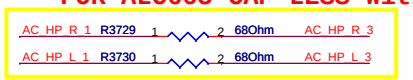


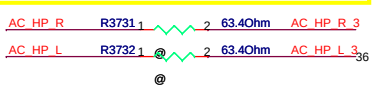
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

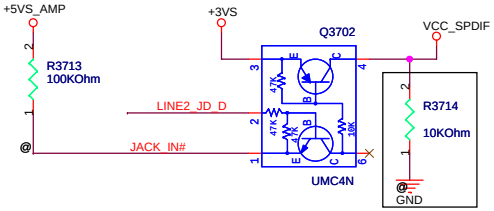
HP & SPDIF CONN



FOR ALC663 CAP-LESS With POP_Noise

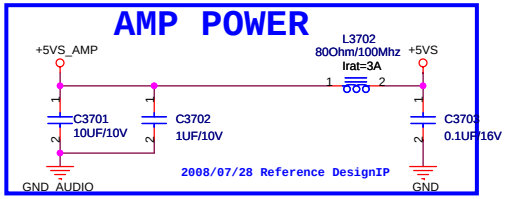


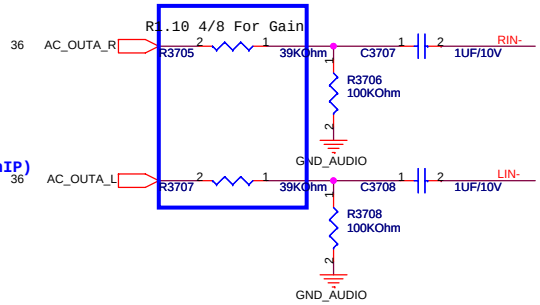




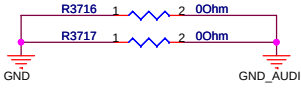
JACK_IN#	LINE2_JD_D	Mode
0	1	SPDIF_CON
0	0	HEADPHONE,SPDIF_HDMI
1	1	SPDIF_HDMI

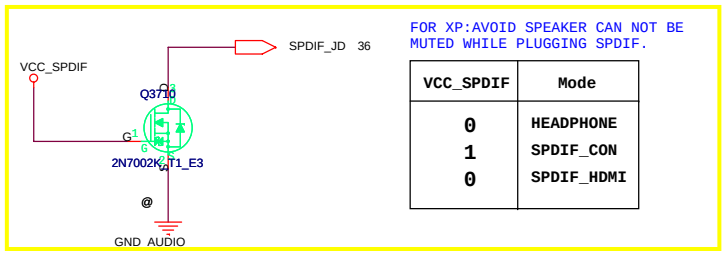
AMP POWER





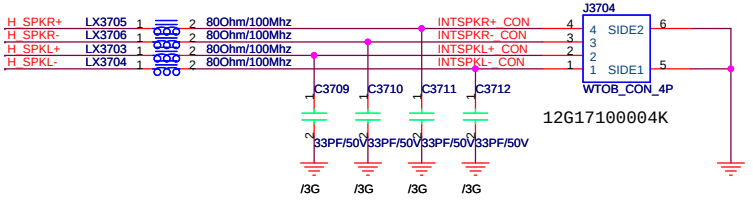
JACK GND



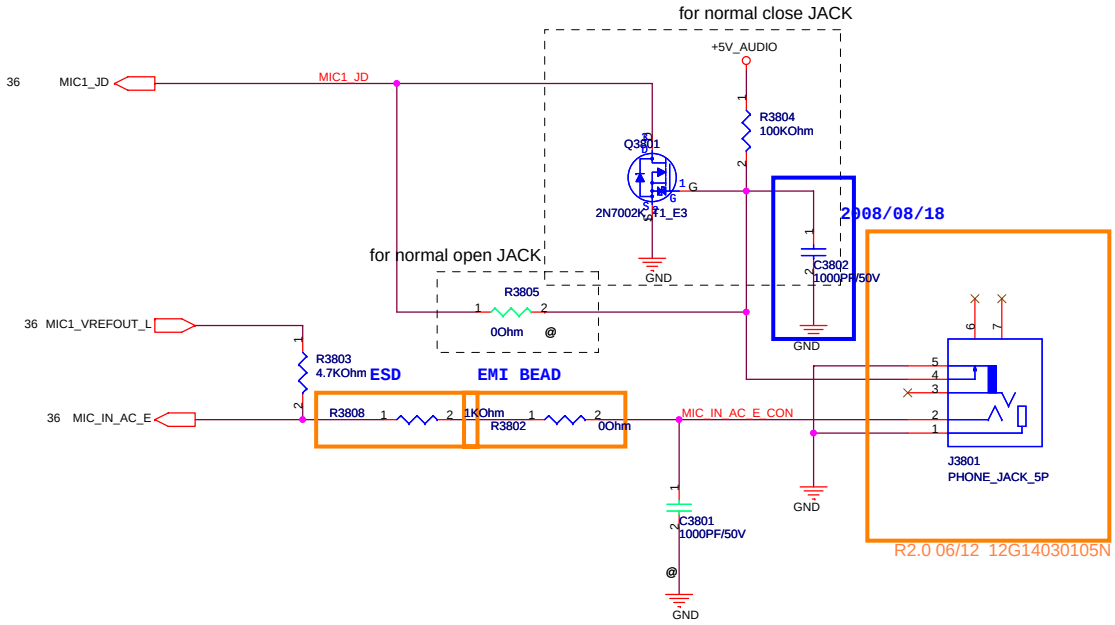


VCC_SPDIF	Mode
0	HEADPHONE
1	SPDIF_CON
0	SPDIF_HDMI

SPEAKER CONNECTOR(2W)

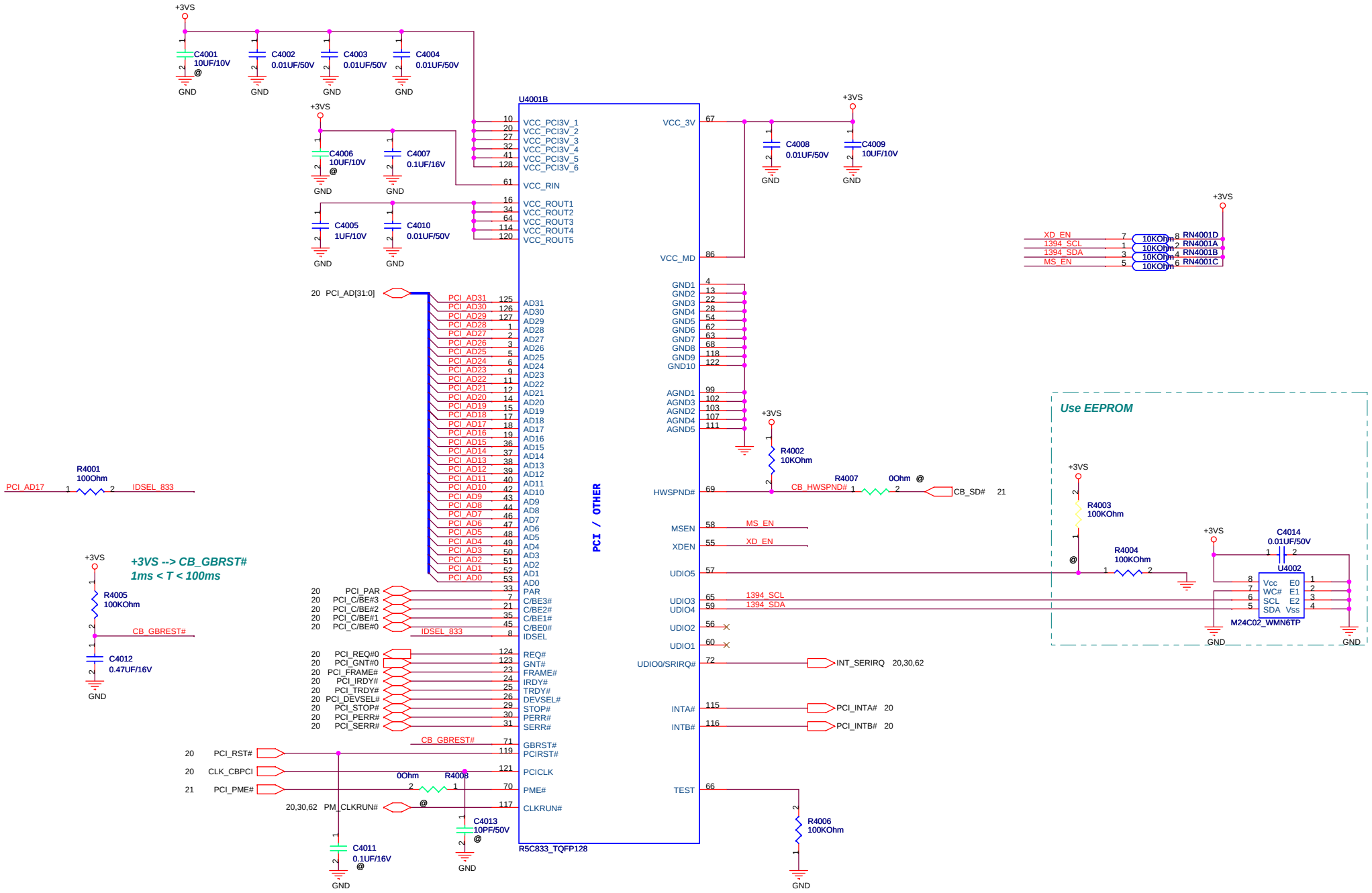


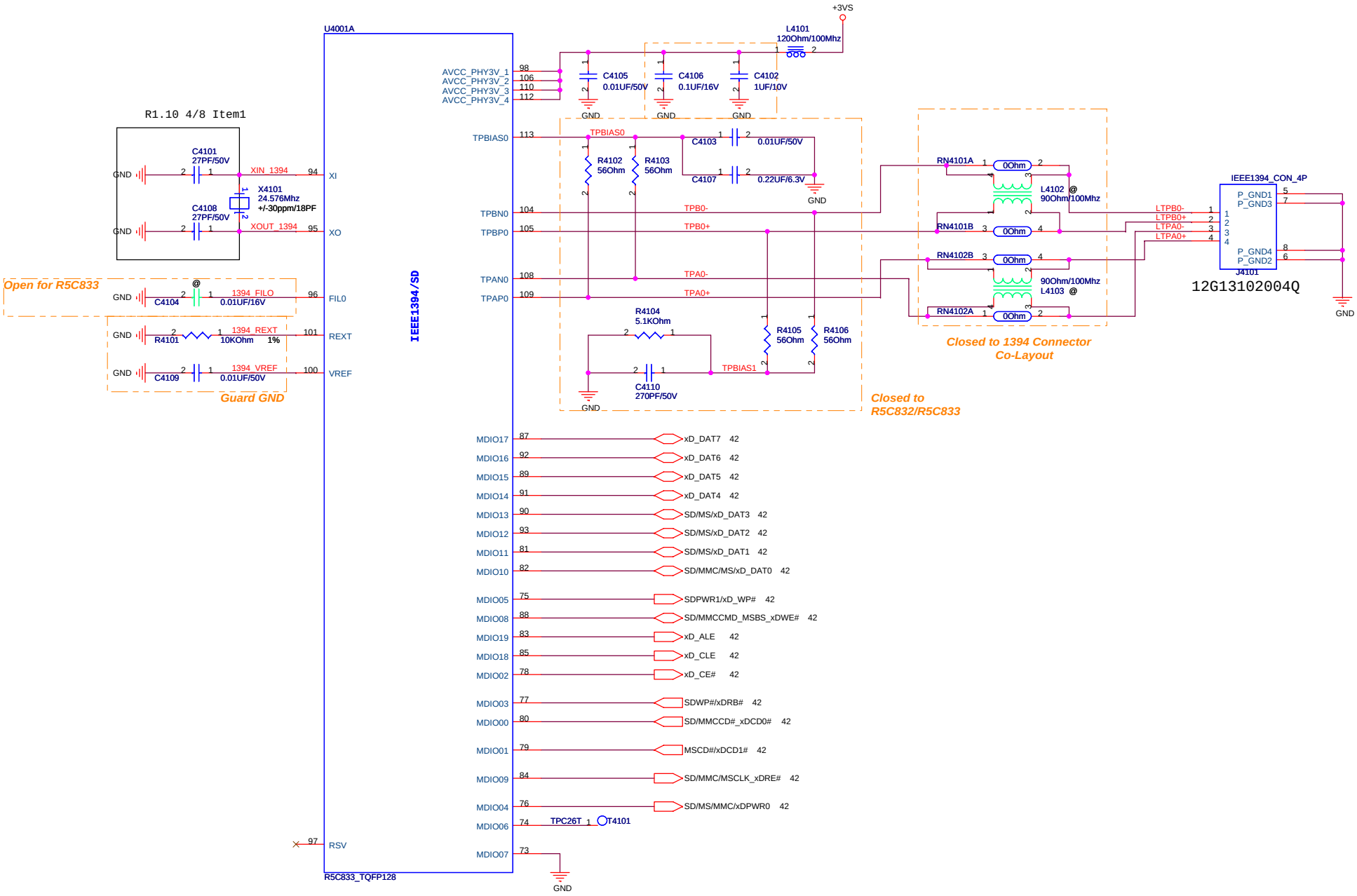
EXTERNAL MICROPHONE



ASUSTeK COMPUTER INC. NB1	Title : MIC&LINEIN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 38 of 93	

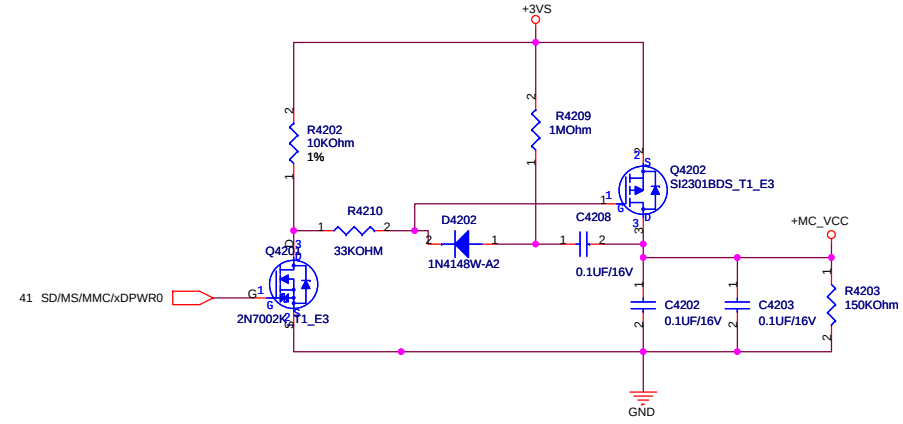
ASUSTeK COMPUTER INC	Title : BLANK			
	Engineer:			
Size: A	Project Name: N50Tr/TA			Rev: 1.00
Date: Thursday, September 25, 2008		Sheet 39 of 93		

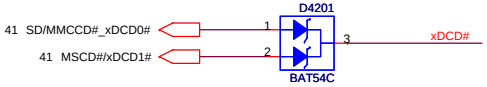

U4001B
PCI / OTHER
R5C833_TQFP128
+3VS
GND
C4001 10UF/10V @
C4002 0.01UF/50V
C4003 0.01UF/50V
C4004 0.01UF/50V
C4005 1UF/10V
C4006 10UF/10V @
C4007 0.1UF/16V
C4008 0.01UF/50V
C4009 10UF/10V
C4010 0.01UF/50V
C4011 0.1UF/16V @
C4012 0.47UF/16V
C4013 10PF/50V @
C4014 0.01UF/50V
R4001 100Ohm
R4002 10KOhm
R4003 100KOhm
R4004 100KOhm
R4005 100KOhm
R4006 100KOhm
R4007 0Ohm @
R4008 0Ohm @
RN4001A RN4001B RN4001C RN4001D 10KOhm
XD_EN
1394_SCL
1394_SDA
MS_EN
PCI_AD[31:0]
PCI_AD17
IDSEL_833
CB_HWSPND#
CB_SD# 21
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
INT_SERIRQ 20,30,62
INTA# PCI_INTA# 20
INTB# PCI_INTB# 20
TEST
PCI_PAR
PCI_C/BE#3
PCI_C/BE#2
PCI_C/BE#1
PCI_C/BE#0
PCI_REQ#0
PCI_GNT#0
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_DEVSEL#
PCI_STOP#
PCI_PERR#
PCI_SERR#
PCI_RST#
CLK_CBPCI
PCI_PME#
PM_CLKRUN#
CB_GBREST#
+3VS --> CB_GBRST#
1ms < T < 100ms
Use EEPROM
U4002
M24C02_WMN6TP
Vcc E0
WC# E1
SCL E2
SDA Vss
ASUSTeK COMPUTER INC. NB1
Title :CARDBUS R5C833 (1)
Engineer: <OrgAddr1>
Size Custom
Project Name N50Tr/TA
Rev 1.00
Date: Thursday, September 25, 2008
Sheet 40 of 93

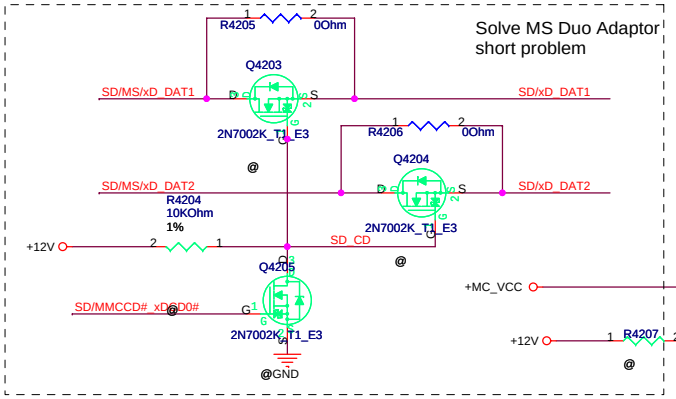


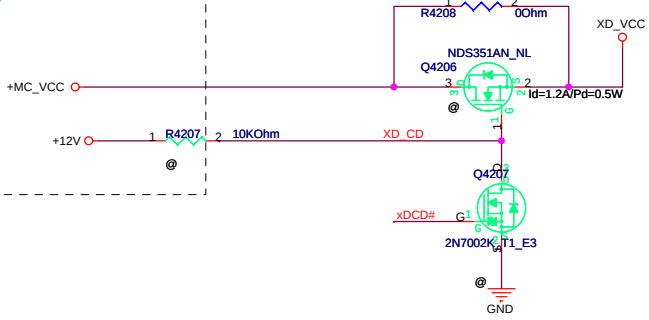
ASUSTeK COMPUTER INC. NB1	Title : CARDBUS R5C833 (2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 41 of 93	

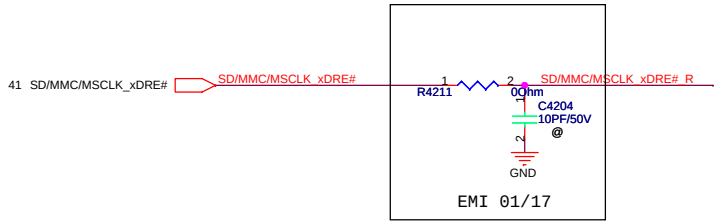
R1.10 4/8 Item1

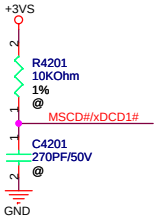


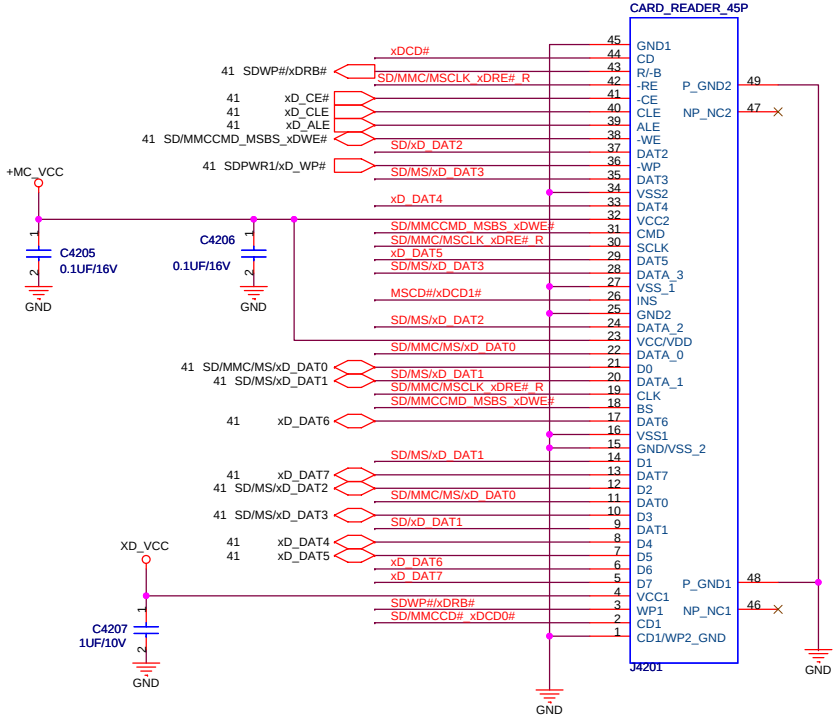


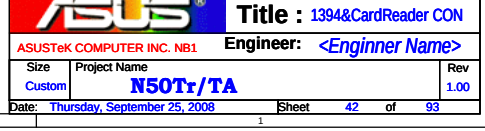


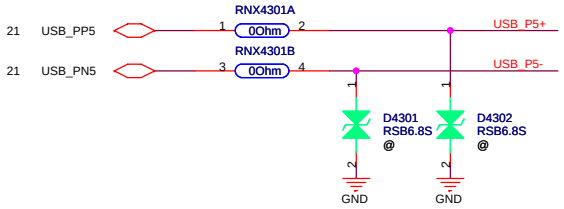






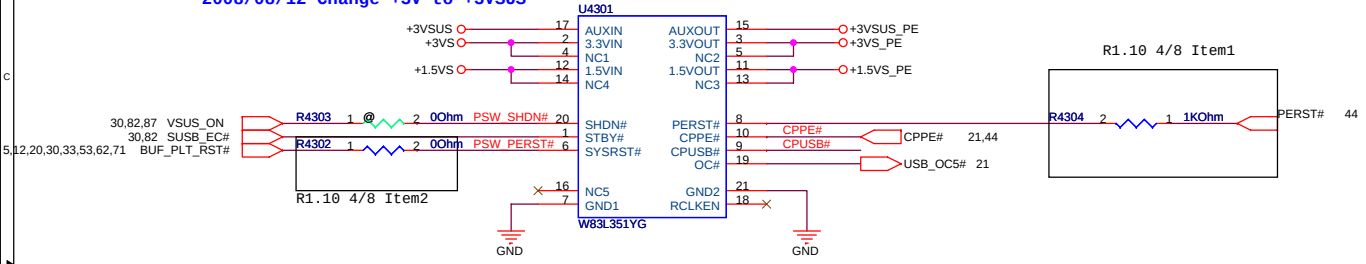






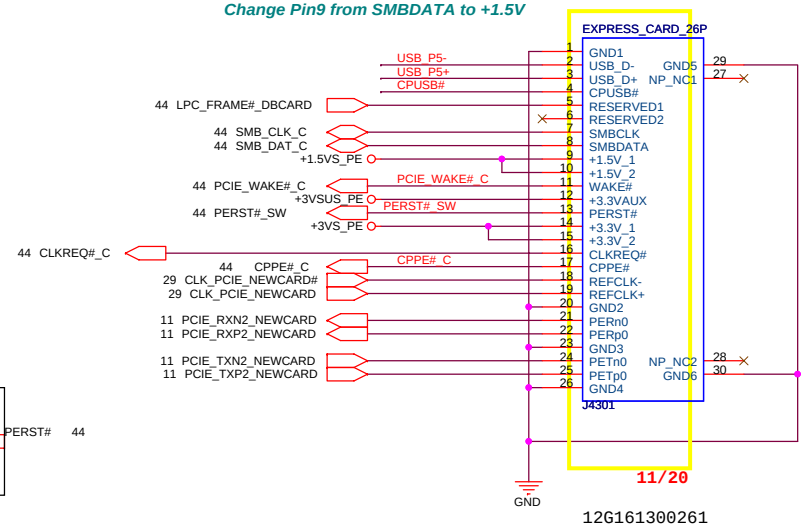
1st source:06G030091010

2008/08/12 Change +3V to +3VSUS



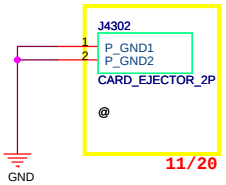
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Header

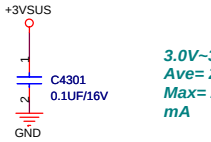


12G161300261

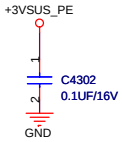
NewCard Ejecter

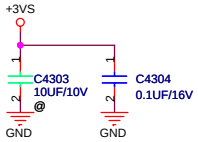


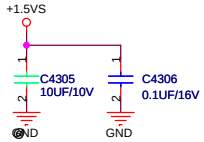
12G21C102604



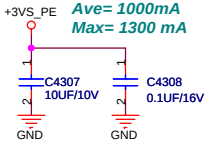
3.0V~3.6V
Ave= 200mA
Max= 275 mA



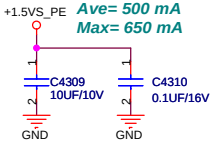


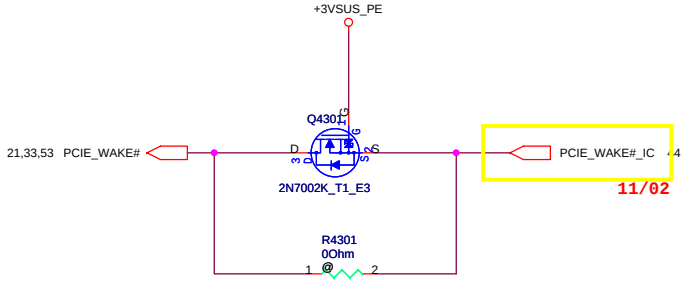


3.0V~3.6V
Ave= 1000mA
Max= 1300 mA



1.35V~1.65V
Ave= 500 mA
Max= 650 mA



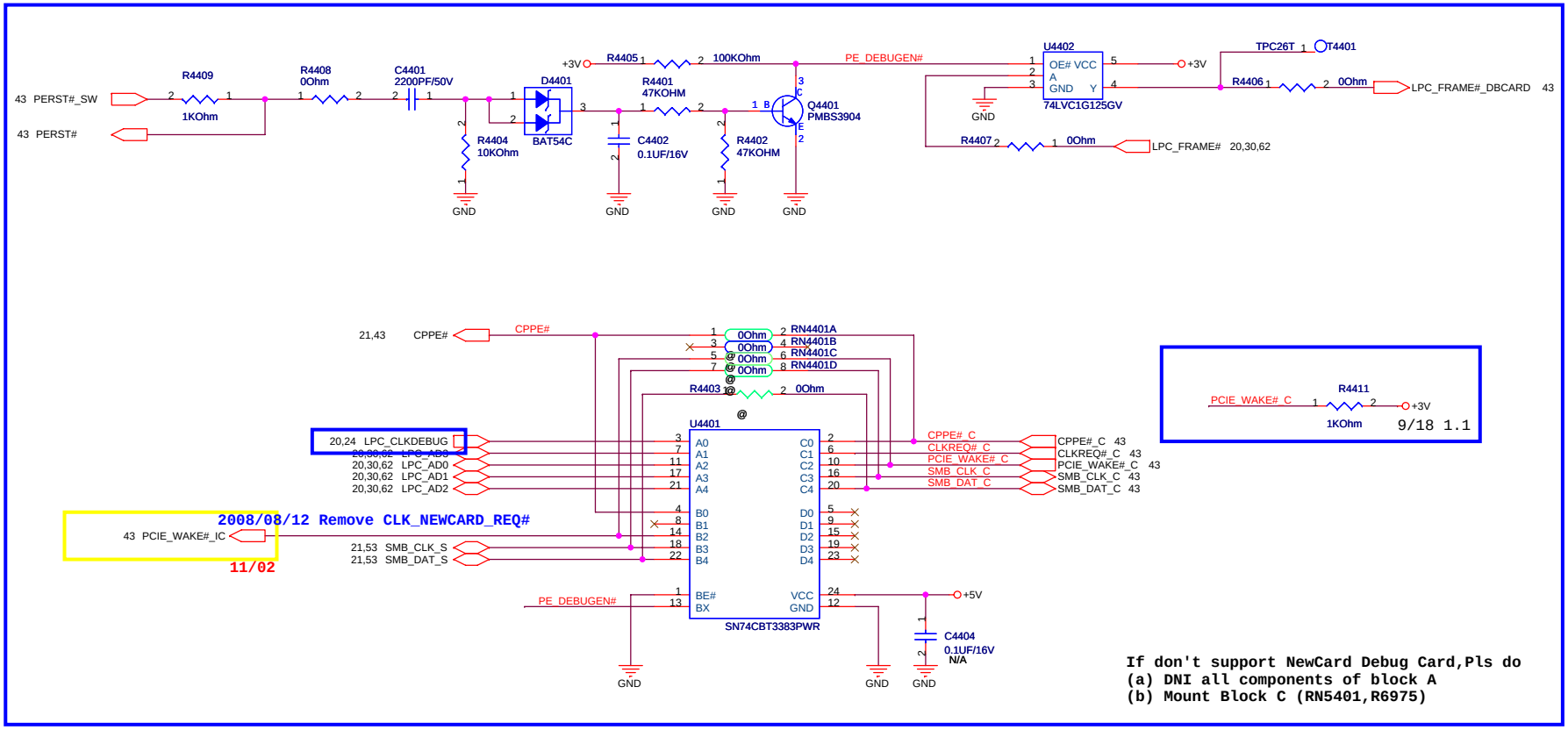


2008/08/12 Remove Q4302 for REFCLK_EN

2008/07/28 ????

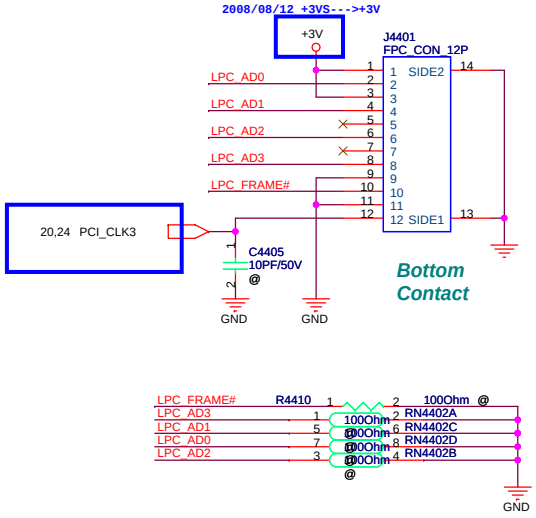
ASUSTeK COMPUTER INC. NB1	Title : NEW CARD	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 43 of 93	

Block A



For PCMCIA Debug Card

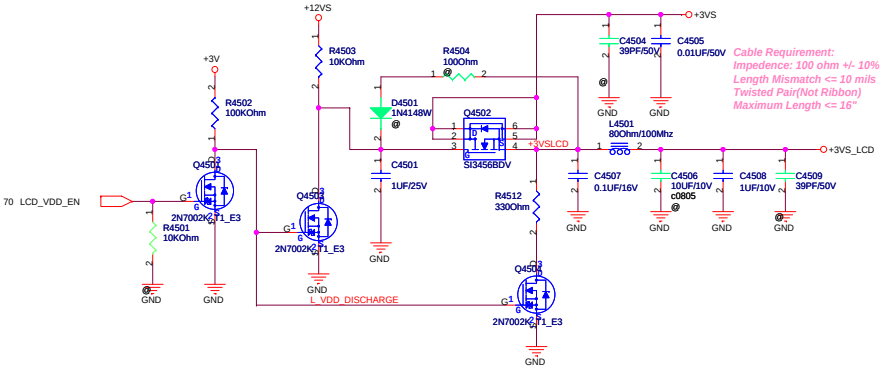
If support NewCard Debug Card,
Pls don't mount all components.



ASUSTeK COMPUTER INC. NB1	Title : DEBUG	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 44 of 93	

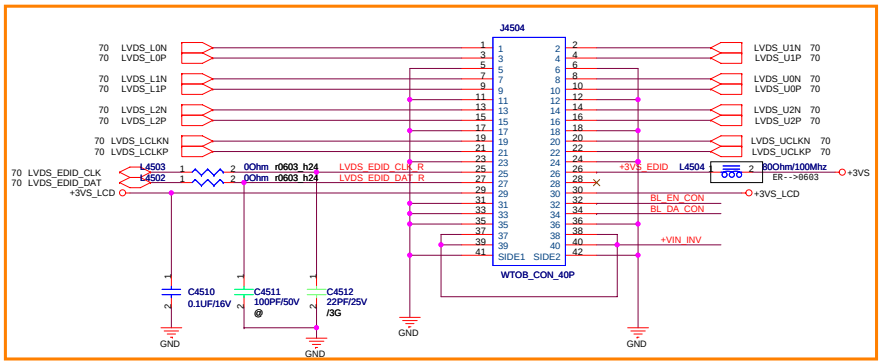
LCD Backlight Control

LCD Power

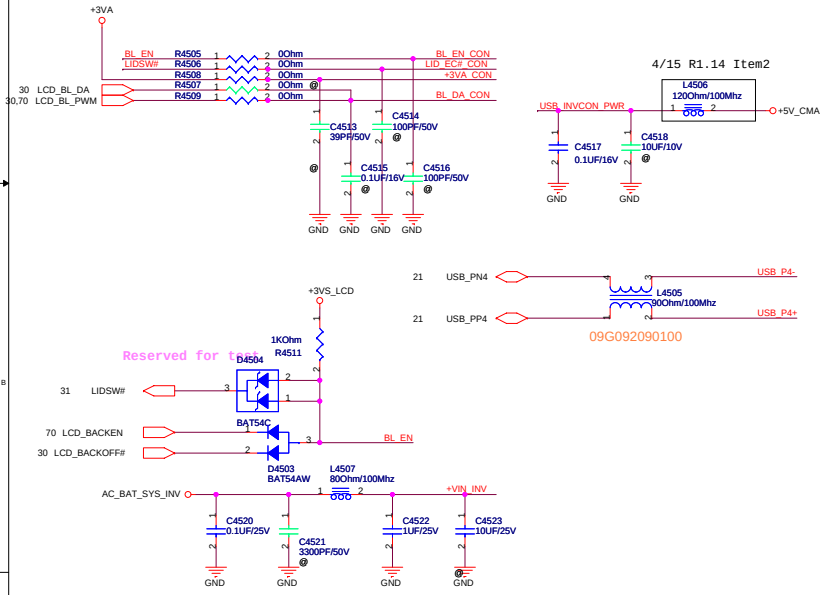


LCD LVDS Interface

R2.0 06/09 12G171010405

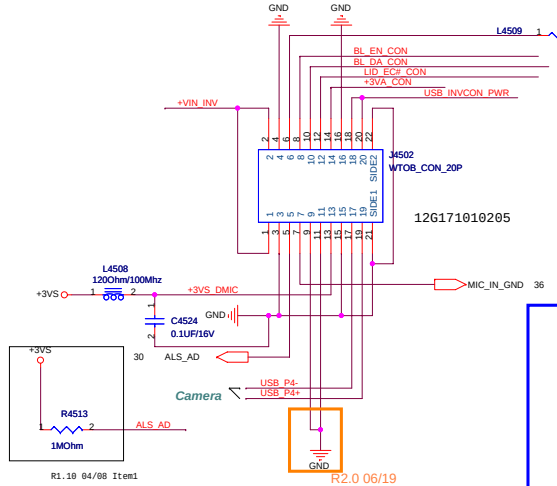


INVERTER
Interface/Speaker CONN.

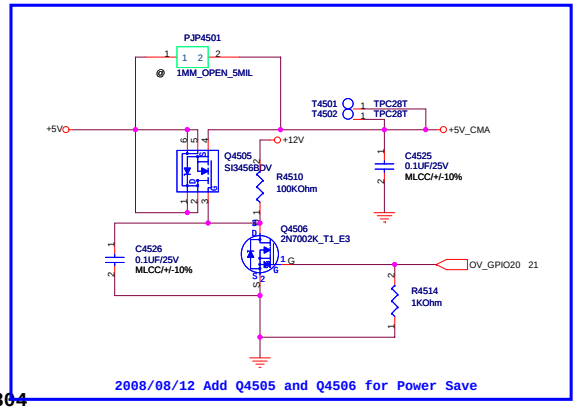


4/15 R1.14 Item2

09G092090100



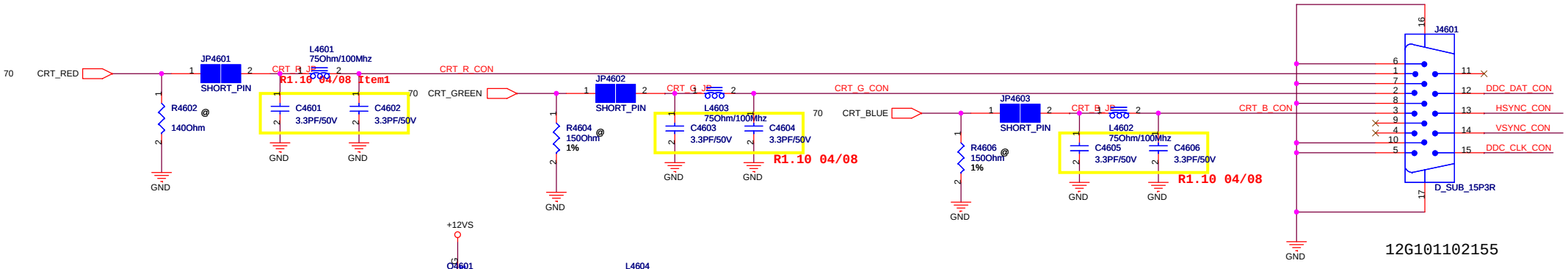
R2.0 06/19 unmount for mic background noise issue



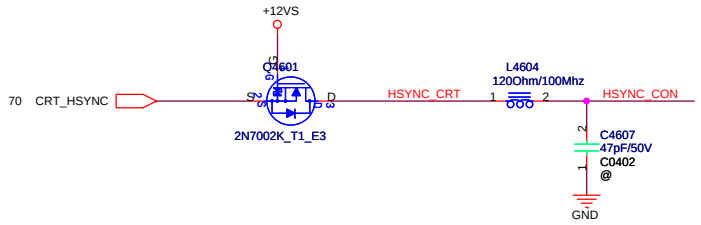
2008/08/12 Add Q4505 and Q4506 for Power Save

delete sim card function 20080804

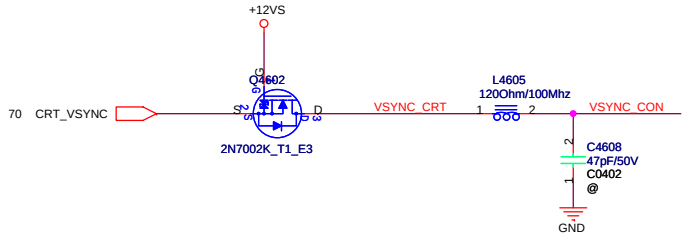
ASUSTeK COMPUTER INC. NB1	Title: LVDS & Inverter CON	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 45 of 93	

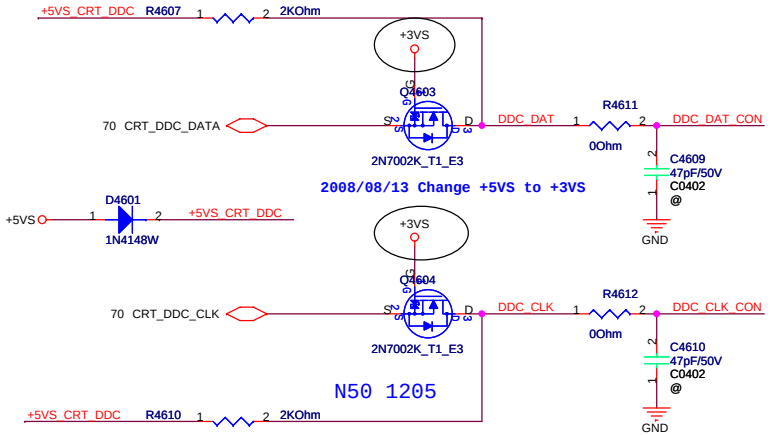


12G101102155

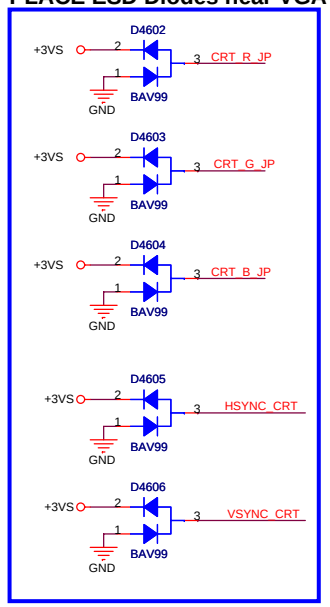


2008/0807 Remove U4601/U4602





PLACE ESD Diodes near VGA port



ASUSTeK COMPUTER INC. NB1	Title : CRT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 46 of 93	

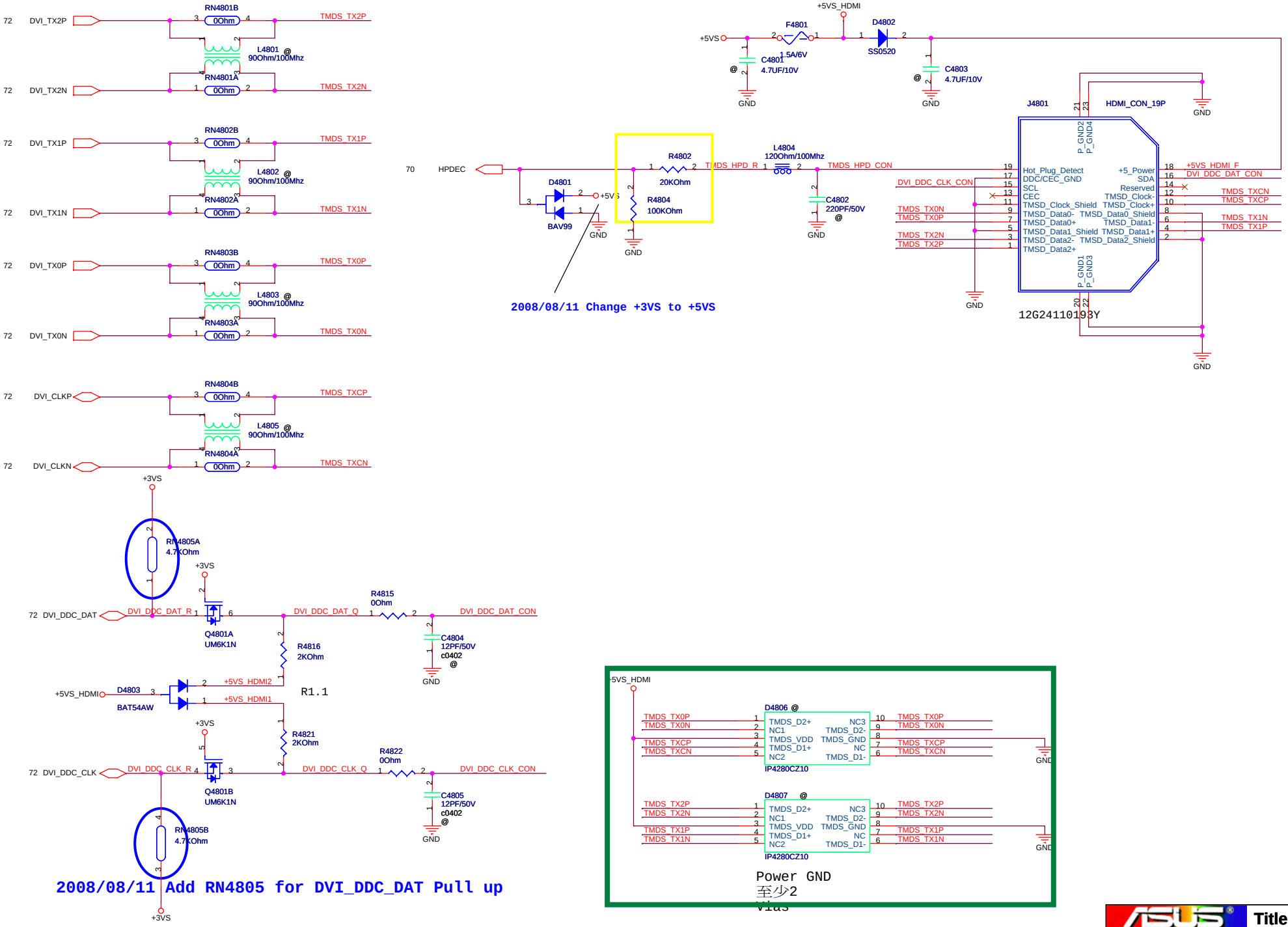
Title : BLANK

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A	N50Tr/TA	1.00

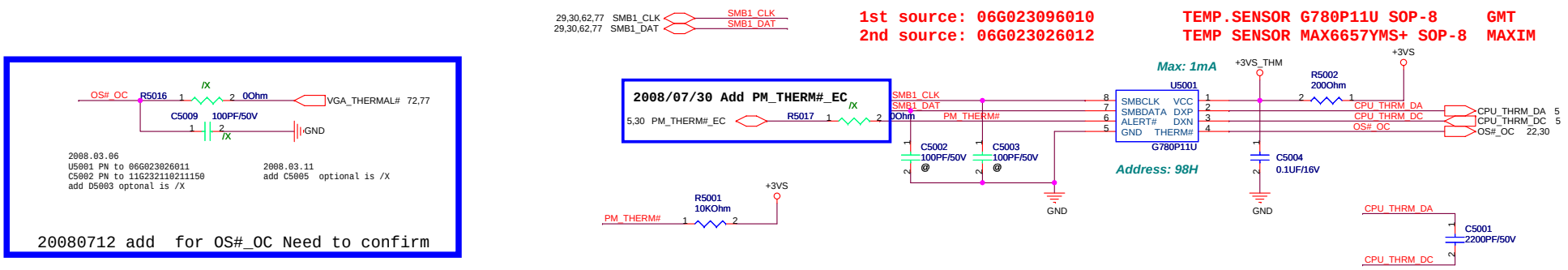
Date: Thursday, September 25, 2008 Sheet 47 of 93



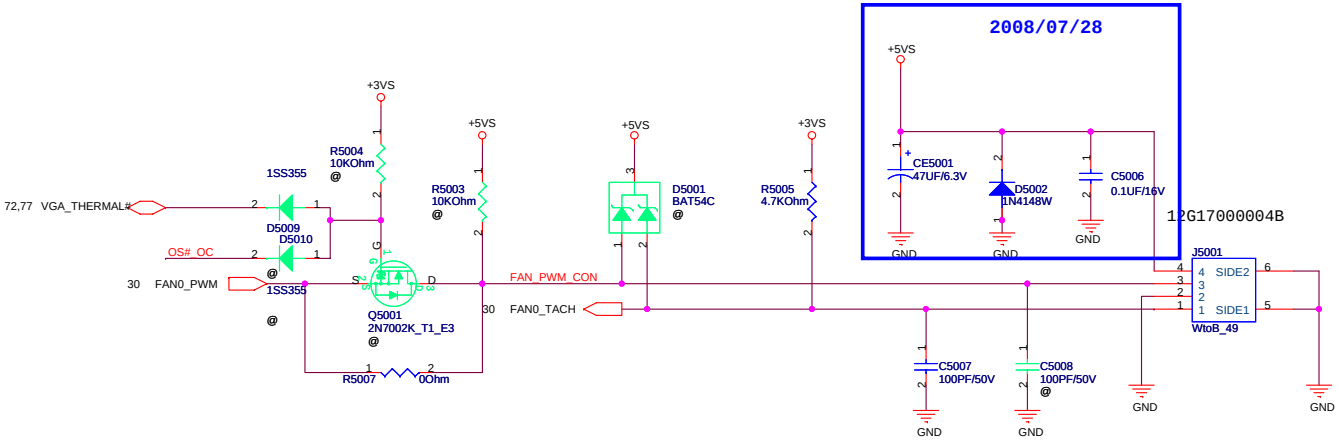
Title : HDMI			
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 48 of 93		

ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 49 of 93	

Thermal Sensor



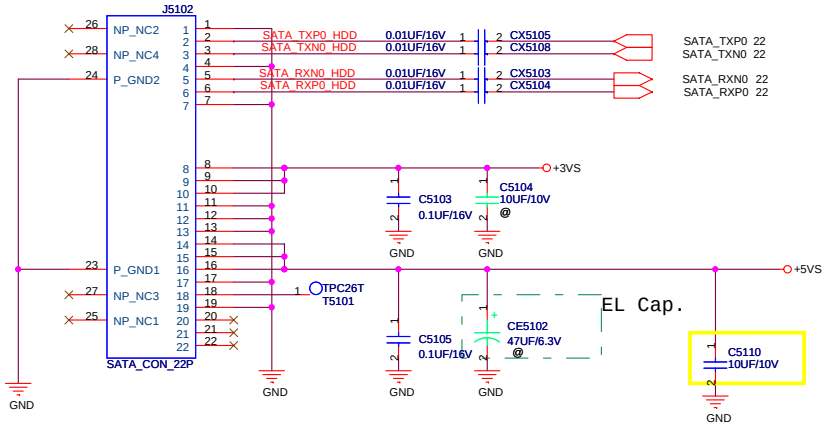
DC FAN Control

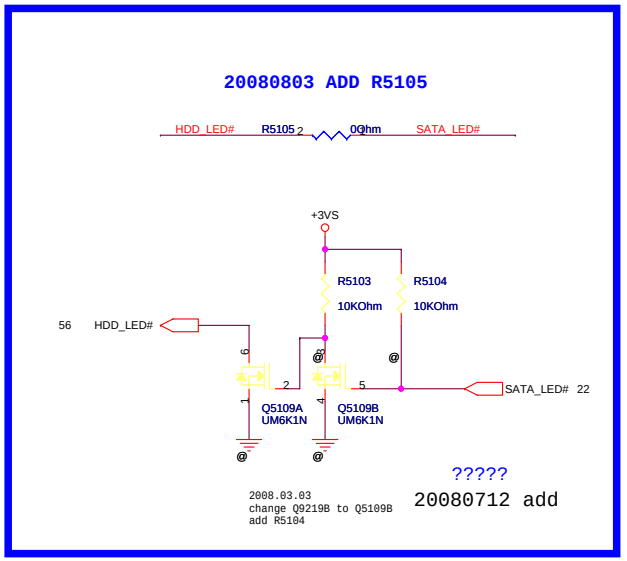


ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 50 of 93		

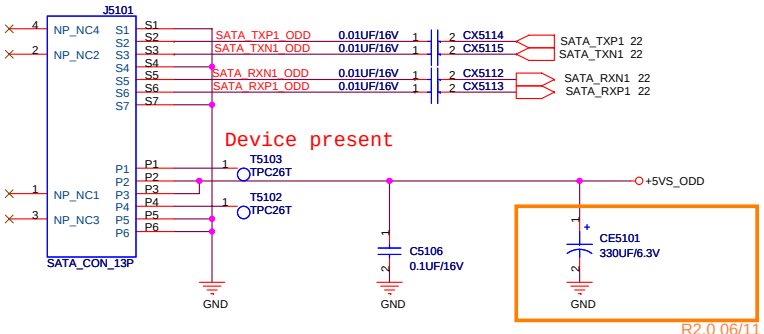
SATA HDD

12G15200022E

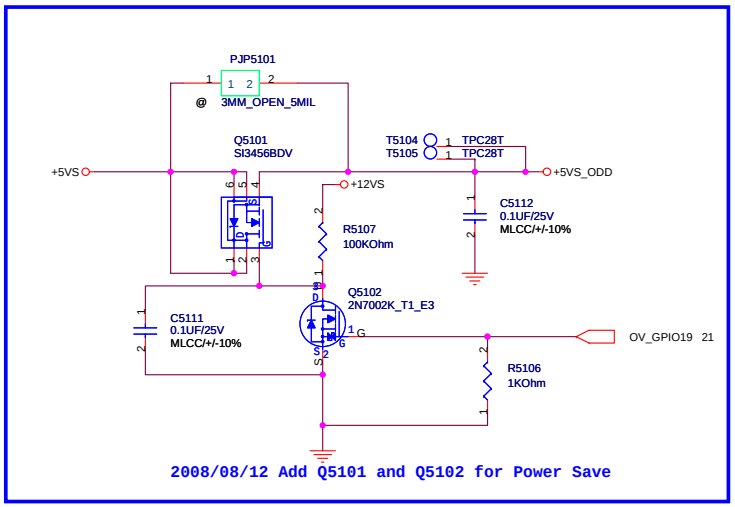




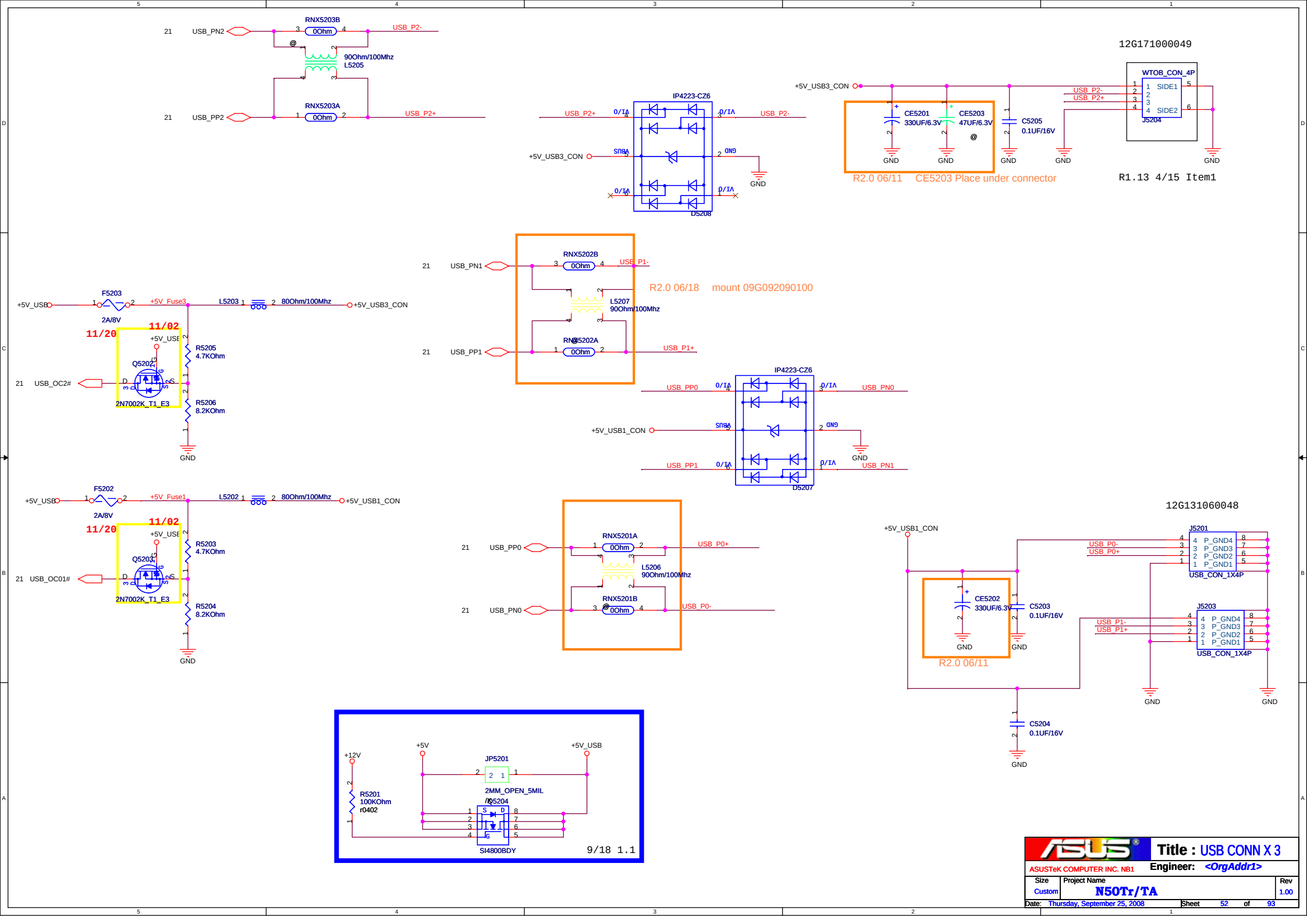
ODD



1st:12G151000132
2nd:12G15100013U

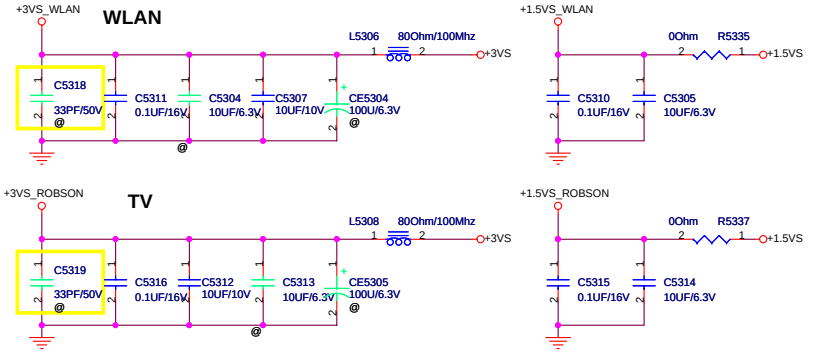


ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 51 of 93	


RNX5203B
0Ohm
USB_PN2
USB_P2-
90Ohm/100Mhz
L5205
RNX5203A
0Ohm
USB_PP2
USB_P2+
IP4223-CZ6
USB_P2+
USB_P2-
+5V_USB3_CON
D5208
12G171000049
+5V_USB3_CON
CE5201
330UF/6.3V
CE5203
47UF/6.3V
C5205
0.1UF/16V
WTOB_CON_4P
SIDE1
SIDE2
J5204
R2.0 06/11 CE5203 Place under connector
R1.13 4/15 Item1
F5203
+5V_USB
+5V_Fuse3
L5203
80Ohm/100Mhz
+5V_USB3_CON
2A/8V
11/02
11/20
R5205
4.7KOhm
Q5202
2N7002K_T1_E3
USB_OC2#
R5206
8.2KOhm
RNX5202B
0Ohm
USB_PN1
USB_P1-
L5207
90Ohm/100Mhz
RNX5202A
0Ohm
USB_PP1
USB_P1+
R2.0 06/18 mount 09G092090100
IP4223-CZ6
USB_PP0
USB_PN0
+5V_USB1_CON
USB_PP1
USB_PN1
D5207
F5202
+5V_USB
+5V_Fuse1
L5202
80Ohm/100Mhz
+5V_USB1_CON
2A/8V
11/02
11/20
R5203
4.7KOhm
Q5203
2N7002K_T1_E3
USB_OC01#
R5204
8.2KOhm
RNX5201A
0Ohm
USB_PP0
USB_P0+
L5206
90Ohm/100Mhz
RNX5201B
0Ohm
USB_PN0
USB_P0-
12G131060048
+5V_USB1_CON
CE5202
330UF/6.3V
C5203
0.1UF/16V
R2.0 06/11
J5201
USB_P0-
USB_P0+
P_GND4
P_GND3
P_GND2
P_GND1
USB_CON_1X4P
J5203
USB_P1-
USB_P1+
C5204
0.1UF/16V
+12V
+5V
+5V_USB
JP5201
2MM_OPEN_5MIL
/Q5204
R5201
100KOhm
r0402
SI4800BDY
9/18 1.1
Title : USB CONN X 3
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size
Custom
Project Name
N50Tr/TA
Rev
1.00
Date: Thursday, September 25, 2008
Sheet 52 of 93

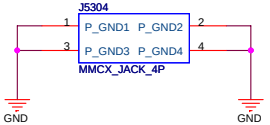
2008/08/04 Remove SIM Schematic

2008/07/29 Remove 3G

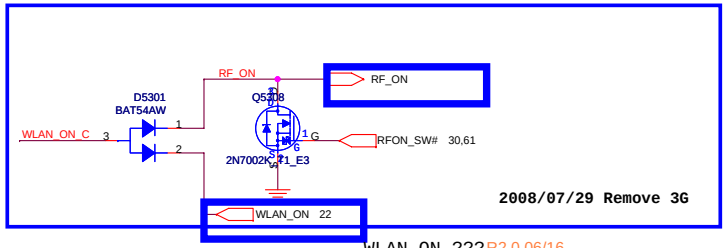


56 WIMAX_LED#
56 WIFI_LED#
WIMAX_LED#
WIFI_LED#

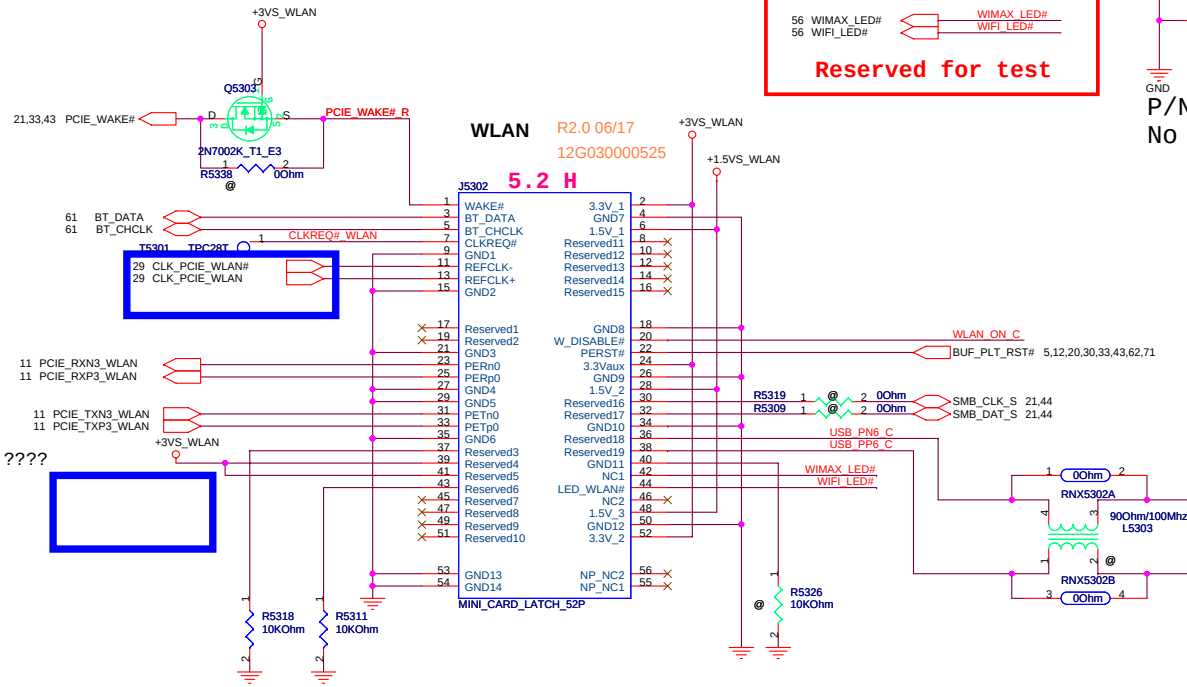
Reserved for test

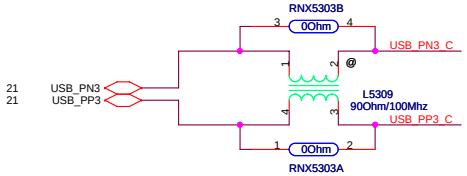


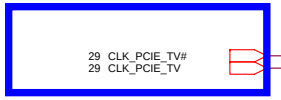
P/N: 14G152148A00
No Part

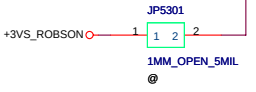


WLAN_ON ??? R2.0 06/16









ASUSTeK COMPUTER INC. NB1	Title : Minicard card & Nut	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 53 of 93	

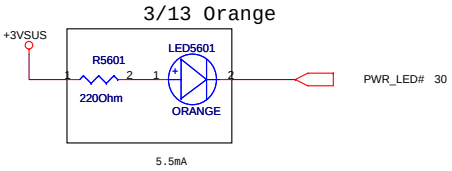
ASUSTeK COMPUTER INC			Title : BLANK		
			Engineer:		
Size	Project Name				Rev
A	N50Tr/TA				1.00
Date: Thursday, September 25, 2008			Sheet 54 of 93		

Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:

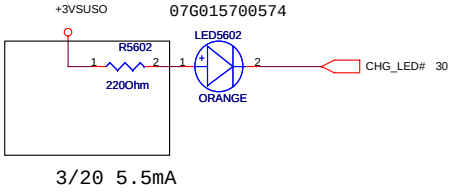
Size	Project Name	Rev
A	N50Tr/TA	1.00

Date: Thursday, September 25, 2008 Sheet 55 of 93

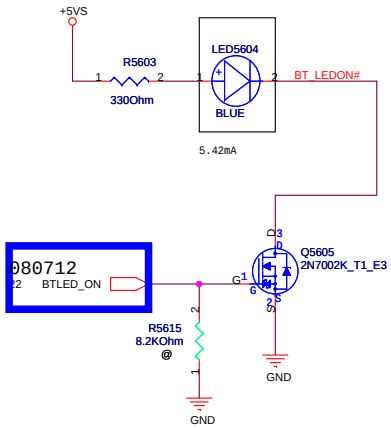
For Power LED



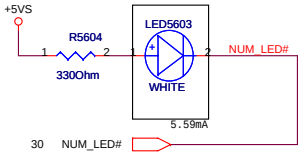
For Battery LED



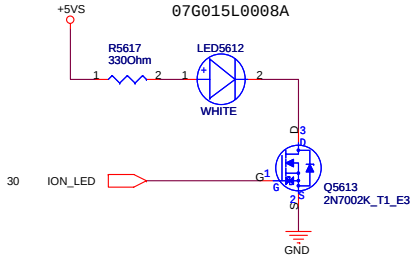
For BT LED



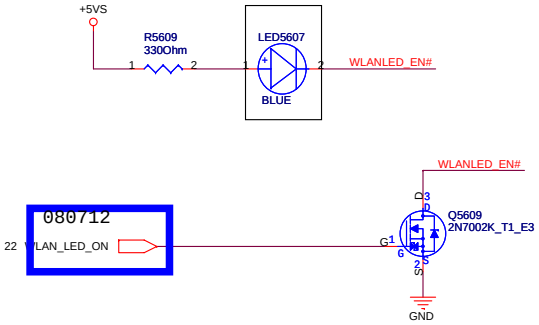
For Number Lock



For Ionizer

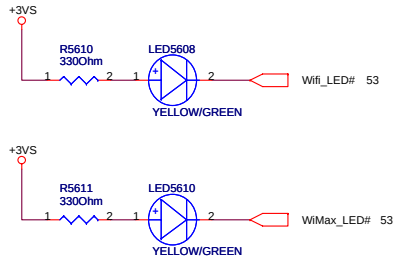


For WireLess LED



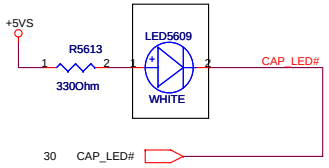
2008/07/30 Remove 3G Function

LEDs for testing

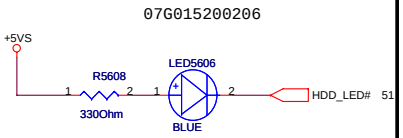


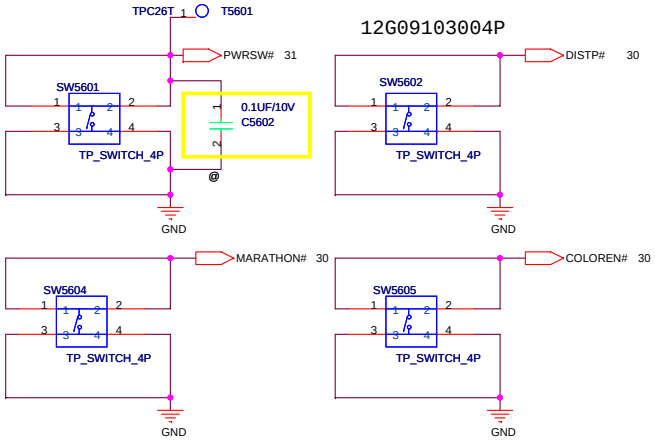
2008/07/29 Remove 3G LED

For Caps. Lock

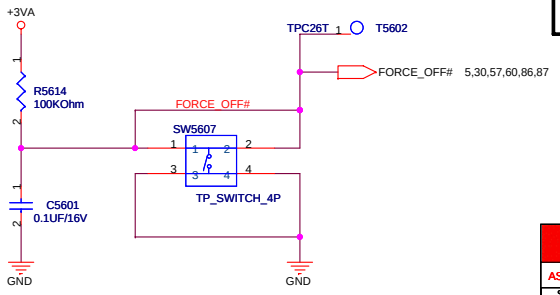


For SATA/IDE LED

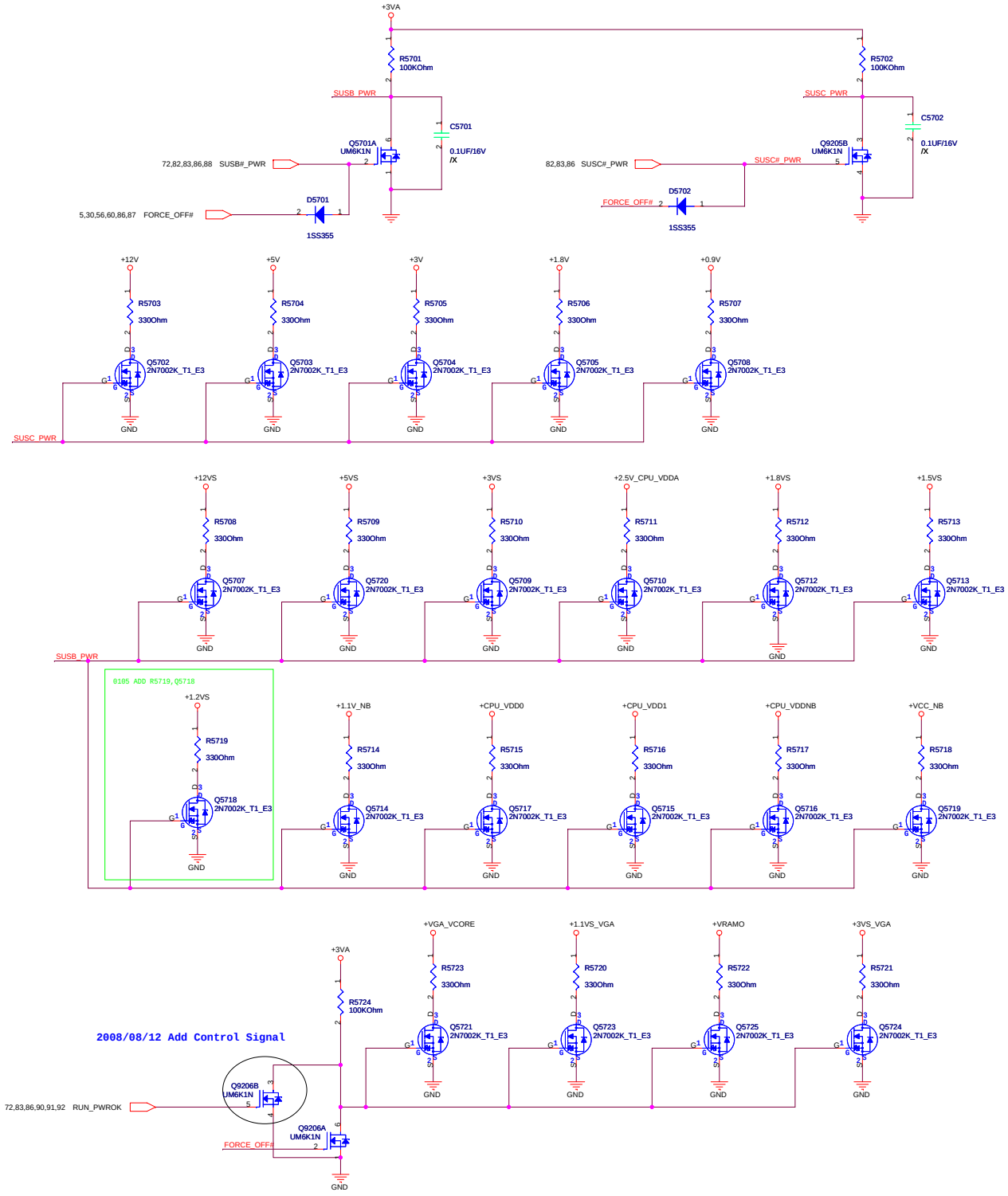




SHUT_DOWN#



ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 56 of 93	



ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 57 of 93	

Title : UWB Minicard card

ASUSTeK COMPUTER INC. NB1

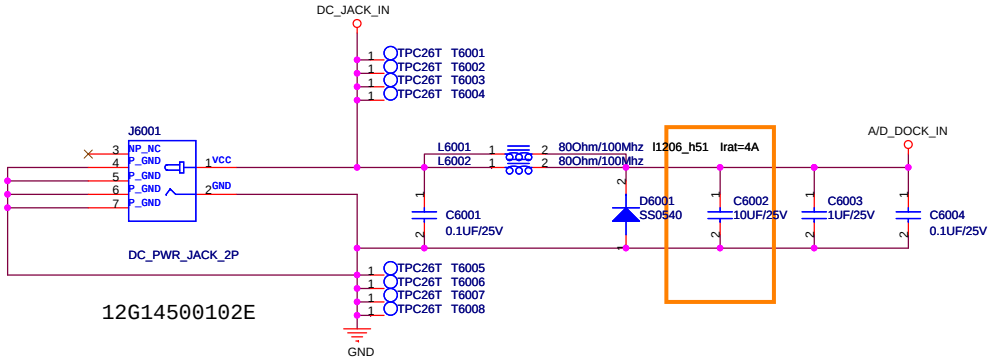
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50Vm/Vc	1.1

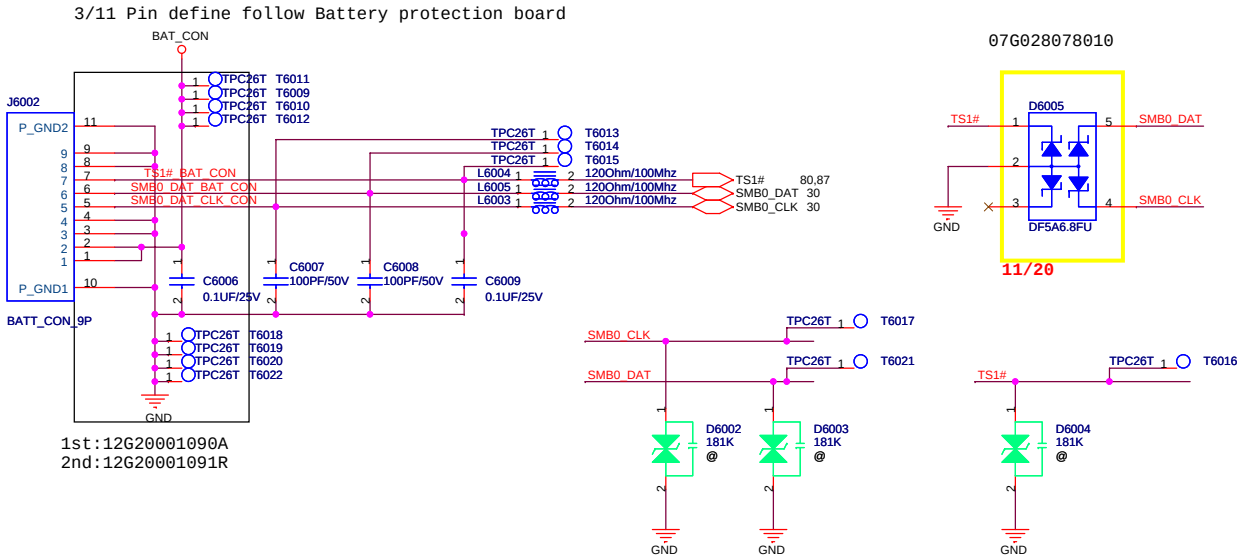
Date: Thursday, September 25, 2008 Sheet 58 of 93

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 59 of 93		

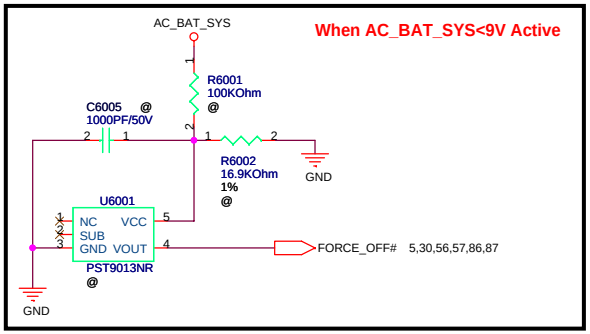
DC IN



BAT IN

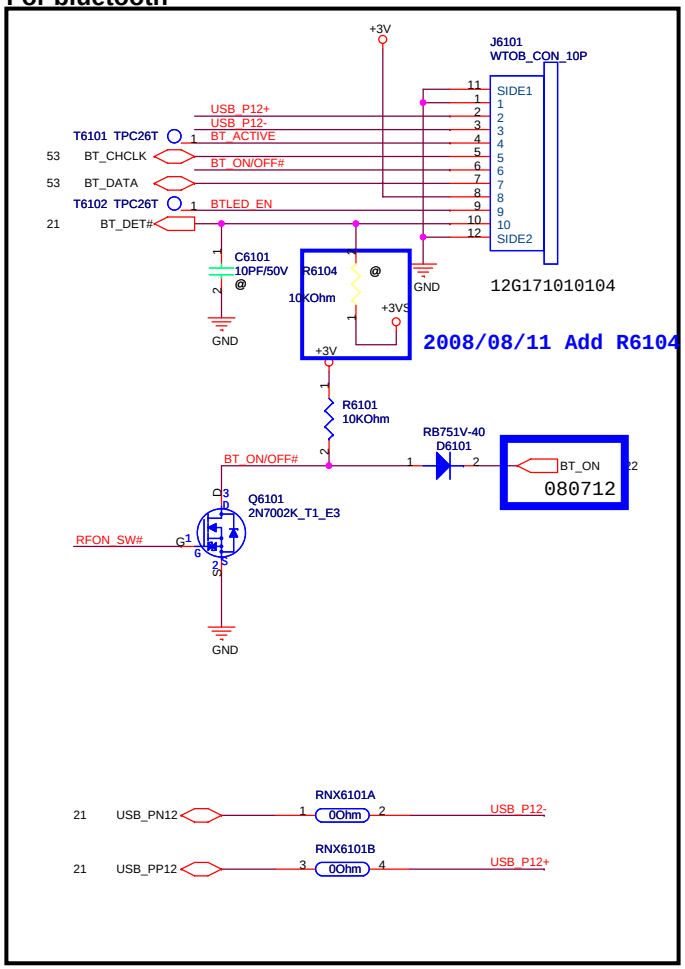


Without Battery & Pull out Adapter



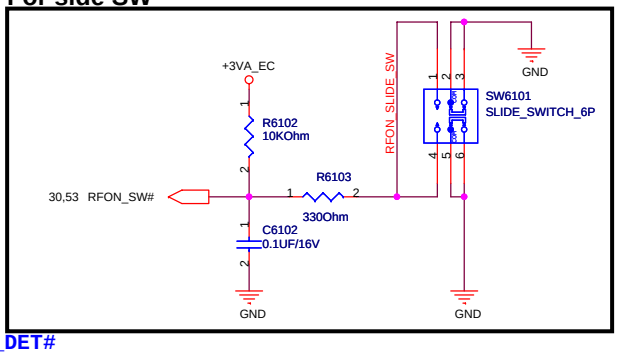
ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 60 of 93	

For bluetooth



For side SW

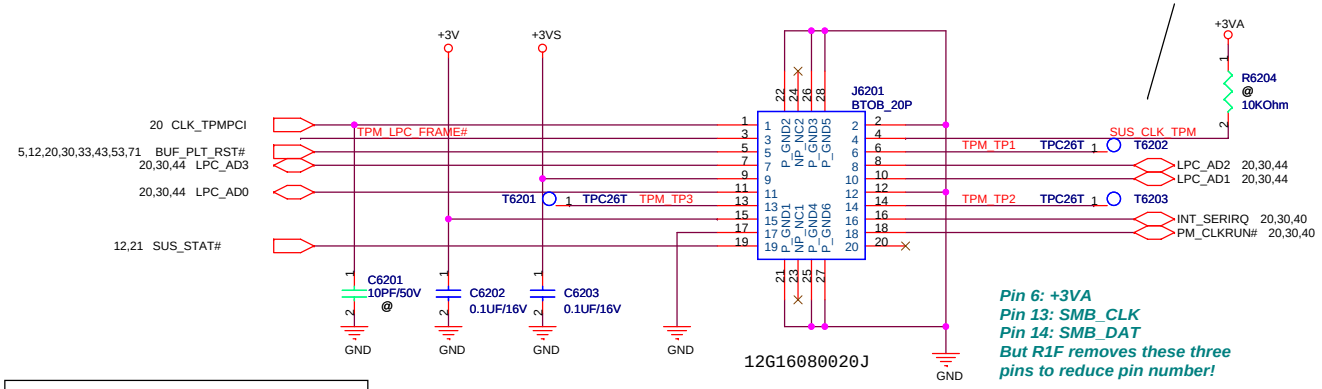
12G090070063



ASUSTeK COMPUTER INC. NB1	Title : BlueTooth	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 61 of 93	

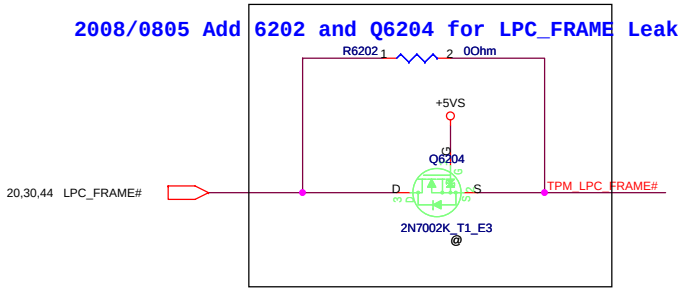
For TPM module

080805
TPM module has internal crystal

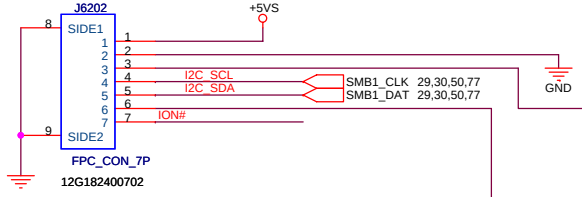


Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

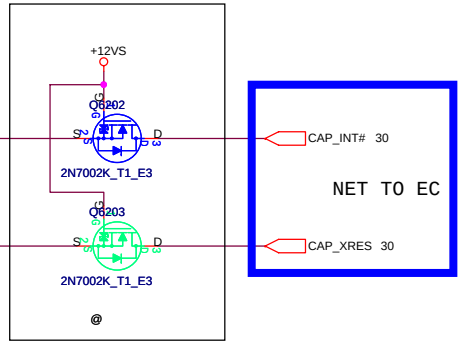
2008/0805 Add 6202 and Q6204 for LPC_FRAME Leak Current from TPM



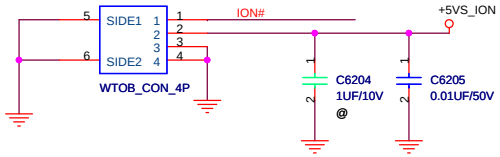
Cap Sensor 12G182400702



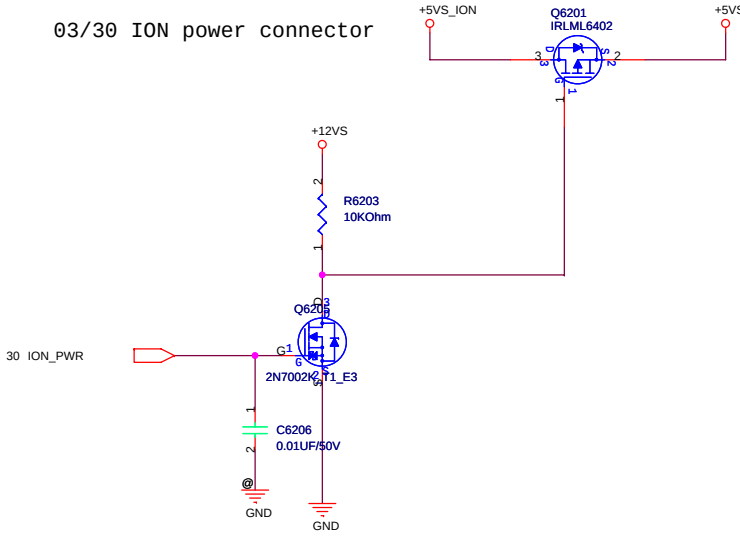
03/21 Cap sensor



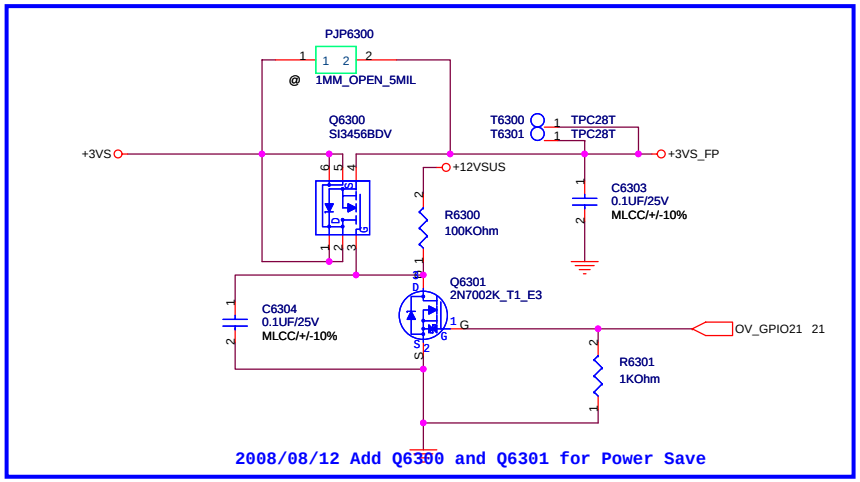
ION 12G17100004K

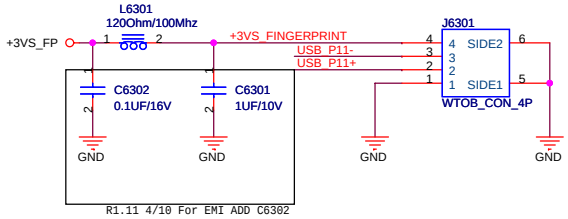


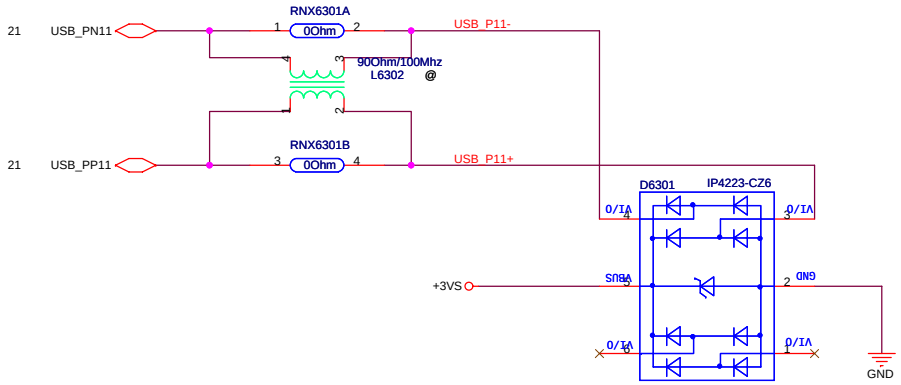
03/30 ION power connector



ASUSTeK COMPUTER INC. NB1	Title : TPM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 62 of 93	







ASUSTeK COMPUTER INC. NB1	Title : Fingerprint	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 63 of 93	

Title : BLANK

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
D	N50Tr/TA	1.00

Date: Thursday, September 25, 2008 Sheet 64 of 63

R1.11 04/10 EMI

U6501 EMI_SPRING_PAD

U6502 EMI_SPRING_PAD

U6503 EMI_SPRING_PAD

R2.0 06/18 reserve for EMI

固定孔

H6527 C79D79N

FOR SCREW HOLE

H6524 H6525 H6526 H6514 H6518 H6523 H6501 H6505 H6528 H6511 H6502 H6507 H6509 H6512 H6503 H6506 H6510 H6513

S335D91N

CR226X236D91N

GND

FOR TPM (BOT) 13GN7510M270 FOR MDC (TOP)

H6201 L4E_1A

R2.0 06/11 MDC nuts removed

FOR CPU

H6516 H6520 H6521 H6522 CT268B158D138

FOR VGA

H6515 H6517 H6519 CT268B158D138

FOR ROBSON (BOT) R2.0 06/17 FOR WLAN (BOT) FOR UWB (BOT)

13G021043011

H5303 H5304 CT217B67D47

H5801 H5802 CT217B67D47

2008/07/29 Remove 3G

20080723 Remove H5305

MINI PCI-E CON

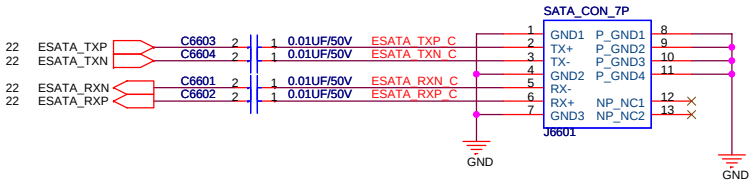
R1.13 4/15 Item1

FAN NUT

H5306 CT256B315ID146

Title	MDC NUT & Hinksink NUT	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 65 of 93	

12G15110007M



ASUSTeK COMPUTER INC. NB1	Title : E-SATA	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 66 of 93	

ASUSTeK COMPUTER INC	Title : BLANK			
	Engineer:			
Size: A	Project Name: N50Tr/TA			Rev: 1.00
Date: Thursday, September 25, 2008		Sheet 67 of 93		

Title : XDP

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50Tr/TA	1.00

Date: Thursday, September 25, 2008 Sheet 68 of 93

N50Vm Revision History

Rev	Date	Description
1.0	2008/7/24	Swap DDR0/DD1 DATA Signal
1.0	2008/8/03	ADD R5105 for SATA_LED#
1.0	2008/8/03	86_Power_GOOD_DETECTER ，Change +VCC_NB_PWRGD Signal
1.0	2008/8/03	Add U1203.. For AMD PowerGood Glitch
1.0	2008/8/03	Remove R0901,R903,R907
1.0	2008/8/03	Add R3619 for PM_SUSB#
1.0	2008/8/04	1, To support Express Card at E/R,mount Block A except RN4401 & R4403. 2, Unmount C4523 3, Unmount D5009 & 5010 4, Remove L5205,L5206,L5207 and mount RNX5201,RNX5202,RNX5203. 5, Remove CE5203 6, Remove Sim Card:unmount RN5304,R5340,J4503,C4527,C4528,C4529,C4519 7, Mount LED for Test:LED5608,LED5610,R5610,R5611 8, Mount Switch for E/R:SW5601,SW5602,SW5607,SW5605,SW5604 and R5614,C5601
1.0	2008/8/04	Page 70 ADD Q7009,Q7010 FOR leak Current Remove Co-Lay 0 OHM
1.0	2008/8/04	Page 12 the U and L of LVDS exchange
1.0	2008/8/05	Page 80 Add PJP8009 for AC_BAT_SYS_INV
1.0	2008/8/05	Page 70 Exchange LCD_BACKEN and LCD_VDD_EN
1.0	2008/8/05	Page20 Add C2024 for NB_RST# Glitch
1.0	2008/8/05	Page 62 Add 6202 and Q6204 for LPC_FRAME Leak Current from TPM
1.0	2008/8/05	Page 62 Add R6204 for SUS_CLK_TPM
1.0	2008/8/05	Page 72 Add R7253 and R7254
1.0	2008/8/07	Page 70 Add R7039,R7040,R7041,R7042
1.0	2008/8/07	Page 46 Remove U4601/U4602
1.0	2008/8/07	Page 46 Add JP2101 for Warm Reset
1.0	2008/8/07	Page 21 Remove R2144,R2143
1.0	2008/8/11	Page 73,76 PCIE_VDDR Change to PCIE_VDDR_G
1.0	2008/8/11	Page61 Add R6104 for BT_DET#
1.0	2008/8/11	Page30 Add T3010,T3011
1.0	2008/8/11	Page70 Remove RN7009,RN7010,RN7011,RN7012,R7034,R7036
1.0	2008/8/11	Page 77Add R7732/R7731/R7730/R7729/R7735/R7734/R7733/R7728
1.0	2008/8/11	Page 76 Add RN4805 for DVI_DDC_DAT/DVI_DDC_CLK Pull up
1.0	2008/8/11	Page13 Remove C1307/L1301/C1308/L1302

Rev	Date	Description
1.0	2008/8/12	Page70 AMD Review Add Q7011,Q7012,Q7013,Q7014
1.0	2008/8/12	Page53 Remove Q5309
1.0	2008/8/12	Page45 Add Q4505 and Q4506 for Power Save
1.0	2008/8/12	Page51 Add Q5101 and Q5102 for Power Save
1.0	2008/8/12	Page53 Add Q6300 and Q6301 for Power Save
1.0	2008/8/17	Page72 Add Q7202 Remove D7201

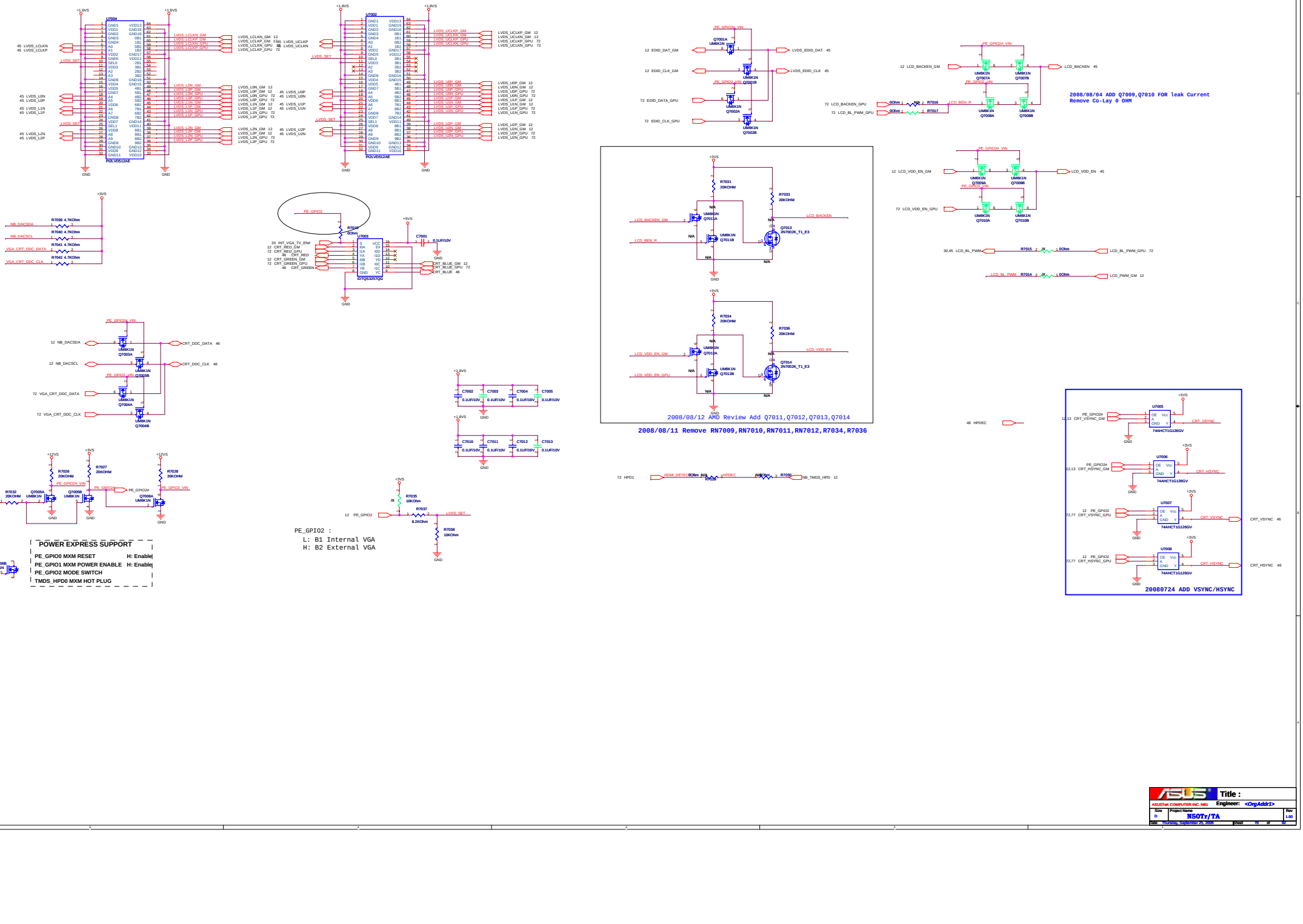
ASUSTeK COMPUTER INC. NB1

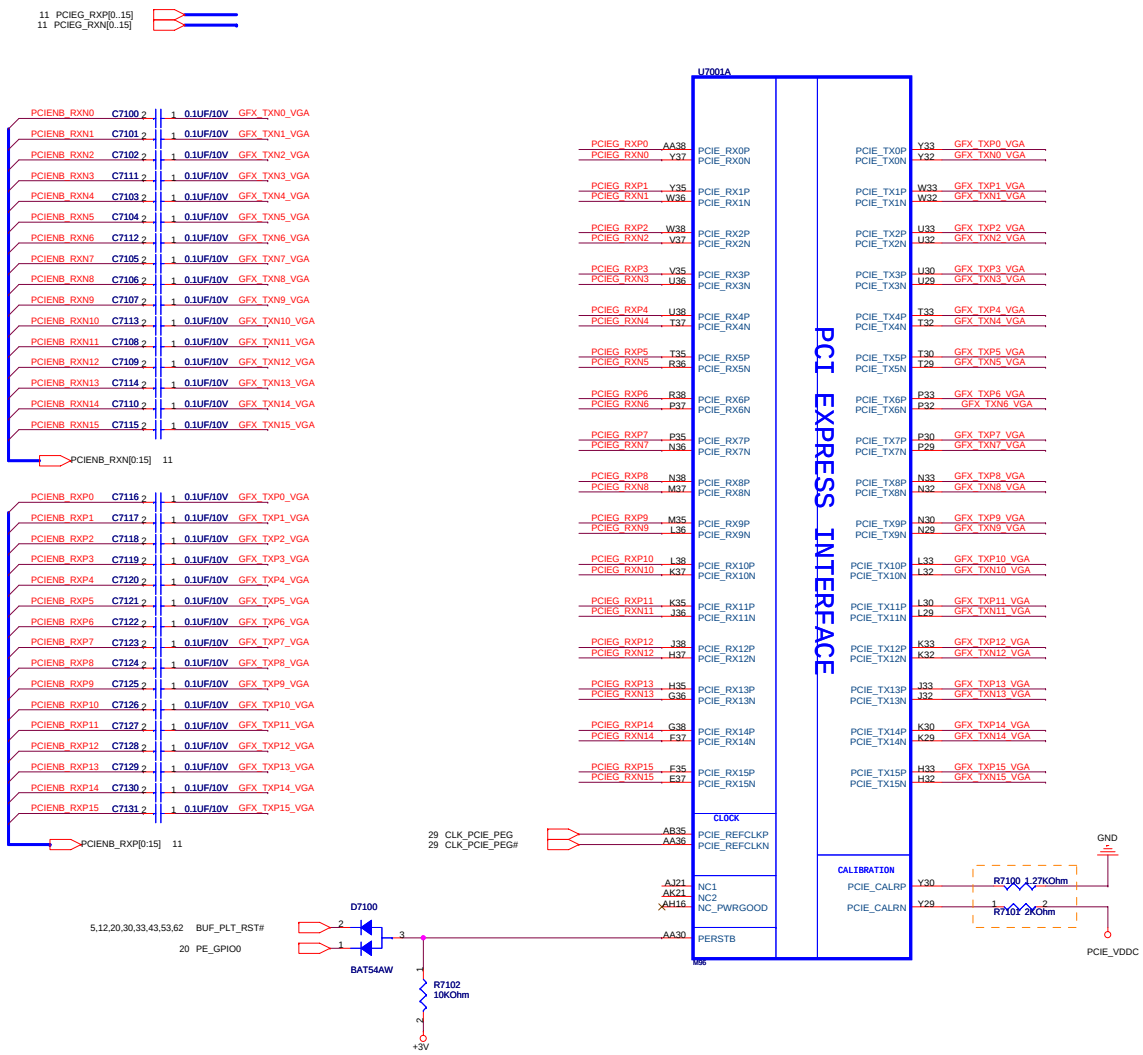
Title : HISTORY

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50Tr/TA	1.00

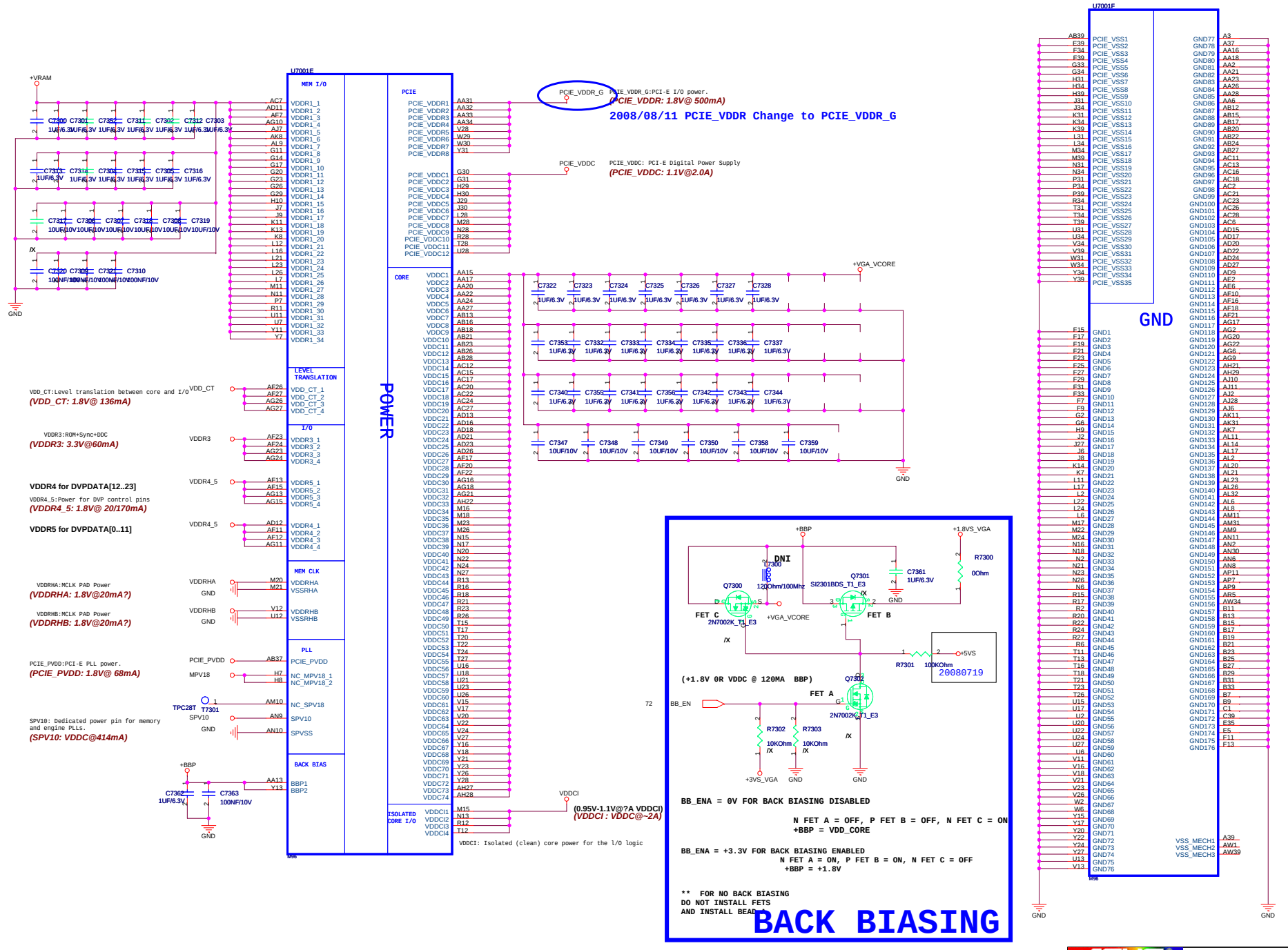
Date: Thursday, September 25, 2008 Sheet 69 of 93

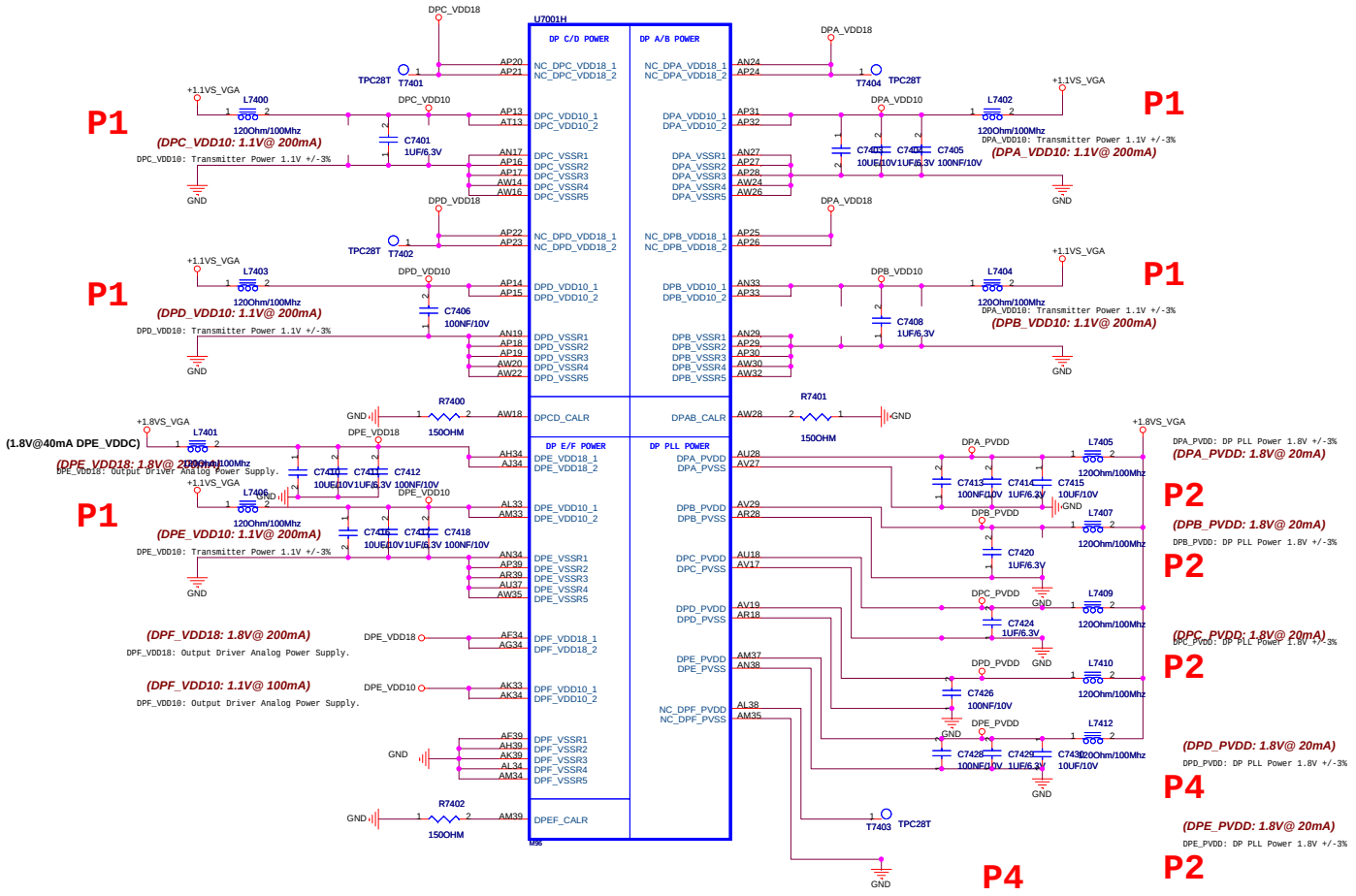

U7004
PI2LVD512AE
U7002
PI2LVD512AE
LVDS_SET
LVDS_LCLKN_GM
LVDS_LCLKP_GM
LVDS_LCLKN_GPU
LVDS_LCLKP_GPU
LVDS_L0N_GM
LVDS_L0P_GM
LVDS_L0N_GPU
LVDS_L0P_GPU
LVDS_L1N_GM
LVDS_L1P_GM
LVDS_L1N_GPU
LVDS_L1P_GPU
LVDS_L2N_GM
LVDS_L2P_GM
LVDS_L2N_GPU
LVDS_L2P_GPU
LVDS_U0N_GM
LVDS_U0P_GM
LVDS_U0N_GPU
LVDS_U0P_GPU
LVDS_U1N_GM
LVDS_U1P_GM
LVDS_U1N_GPU
LVDS_U1P_GPU
LVDS_U2N_GM
LVDS_U2P_GM
LVDS_U2N_GPU
LVDS_U2P_GPU
+1.8VS
GND
PE_GPIO2_VIN
Q7001A
Q7001B
Q7002A
Q7002B
UM6K1N
12 EDID_DAT_GM
12 EDID_CLK_GM
72 EDID_DATA_GPU
72 EDID_CLK_GPU
LVDS_EDID_DAT 45
LVDS_EDID_CLK 45
PE_GPIO2# VIN
Q7007A
Q7007B
Q7008A
Q7008B
12 LCD_BACKEN_GM
72 LCD_BACKEN_GPU
72 LCD_BL_PWM_GPU
0Ohm
R7016
R7017
LCD_BEN_R
LCD_BACKEN 45
2008/08/04 ADD Q7009,Q7010 FOR leak Current
Remove Co-Lay 0 OHM
+3VS
R7031
20KOHM
R7033
20KOHM
R7034
20KOHM
R7036
20KOHM
Q7011A
Q7011B
Q7012A
Q7012B
Q7013
Q7014
2N7002K_T1_E3
LCD_BACKEN_GM
LCD_BEN_R
LCD_VDD_EN_GM
LCD_VDD_EN_GPU
LCD_BACKEN
LCD_VDD_EN
N/A
2008/08/12 AMD Review Add Q7011,Q7012,Q7013,Q7014
2008/08/11 Remove RN7009,RN7010,RN7011,RN7012,R7034,R7036
12 LCD_VDD_EN_GM
72 LCD_VDD_EN_GPU
LCD_VDD_EN 45
30,45 LCD_BL_PWM
R7015
LCD_BL_PWM_GPU 72
LCD_BL_PWM
R7014
LCD_PWM_GM 12
R7039 4.7KOhm
R7040 4.7KOhm
R7041 4.7KOhm
R7042 4.7KOhm
NB_DACSDA
NB_DACSCL
VGA_CRT_DDC_DATA
VGA_CRT_DDC_CLK
12 NB_DACSDA
12 NB_DACSCL
72 VGA_CRT_DDC_DATA
72 VGA_CRT_DDC_CLK
CRT_DDC_DATA 46
CRT_DDC_CLK 46
Q7003A
Q7003B
Q7004A
Q7004B
PE_GPIO2
PE_GPIO2 :
L: B1 Internal VGA
H: B2 External VGA
U7003
Q7TQS3257QG
R7018
50hm
C7001
0.1UF/10V
20 INT_VGA_TV_EN#
12 CRT_RED_GM
72 CRT_RED_GPU
46 CRT_RED
12 CRT_GREEN_GM
72 CRT_GREEN_GPU
46 CRT_GREEN
CRT_BLUE_GM 12
CRT_BLUE_GPU 72
CRT_BLUE 46
C7002
C7003
C7004
C7005
C7010
C7011
C7012
C7013
0.1UF/10V
R7026
20KOHM
R7027
20KOHM
R7028
20KOHM
R7032
20KOHM
Q7005A
Q7005B
Q7006A
Q7006B
+12VS
+3VS
R7035
10KOhm
R7037
8.2KOhm
R7038
10KOhm
12 PE_GPIO2
LVDS_SET
POWER EXPRESS SUPPORT
PE_GPIO MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
Q7008B
72 HPD1
HDMI_DETECT
80hm
N/A
R7029
HPDEC
R7030
NB_TMDS_HPD 12
48 HPDEC
U7005
U7006
U7007
U7008
74AHCT1G126GV
PE_GPIO2#
12,13 CRT_VSYNC_GM
12,13 CRT_HSYNC_GM
12 PE_GPIO2
72,77 CRT_VSYNC_GPU
72,77 CRT_HSYNC_GPU
CRT_VSYNC
CRT_HSYNC
CRT_VSYNC 46
CRT_HSYNC 46
20080724 ADD VSYNC/HSYNC
ASUSTeK COMPUTER INC. NB1
Title :
Engineer: <OrgAddr1>
Size: D
Project Name: N50Tr/TA
Rev: 1.00
Date: Thursday, September 25, 2008
Sheet 70 of 82



2008/08/12 Change +3V to +3VS_VGA

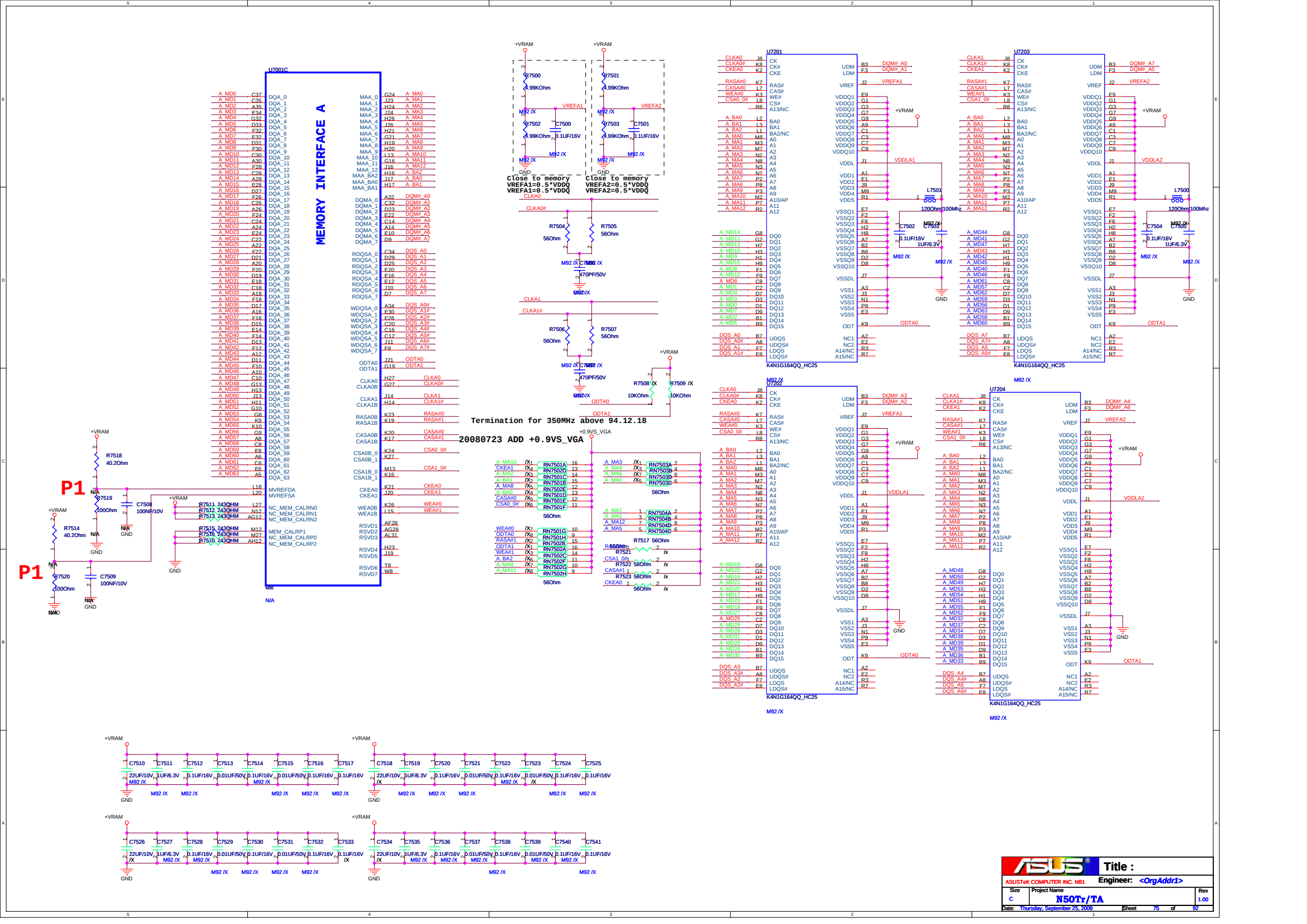
ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: C	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 71 of 92		


U7001E
MEM I/O
PCIE
POWER
CORE
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
ISOLATED CORE I/O
PCIE_VDDR_G
PCIE_VDDR_G:PCI-E I/O power.
(PCIE_VDDR: 1.8V@ 500mA)
2008/08/11 PCIE_VDDR Change to PCIE_VDDR_G
PCIE_VDDC
PCIE_VDDC: PCI-E Digital Power Supply
(PCIE_VDDC: 1.1V@2.0A)
+VGA_VCORE
VDD_CT:Level translation between core and I/O
(VDD_CT: 1.8V@ 136mA)
VDDR3:ROM+Sync+DDC
(VDDR3: 3.3V@60mA)
VDDR4 for DVPDATA[12..23]
VDDR4_5:Power for DVP control pins
(VDDR4_5: 1.8V@ 20/170mA)
VDDR5 for DVPDATA[0..11]
VDDRHA:MCLK PAD Power
(VDDRHA: 1.8V@20mA?)
VDDRHB:MCLK PAD Power
(VDDRHB: 1.8V@20mA?)
PCIE_PVDD:PCI-E PLL power.
(PCIE_PVDD: 1.8V@ 68mA)
SPV10: Dedicated power pin for memory and engine PLLs.
(SPV10: VDDC@414mA)
VDDCI
(0.95V-1.1V@?A VDDCI)
(VDDCI : VDDC@~2A)
VDDCI: Isolated (clean) core power for the I/O logic
(+1.8V 0R VDDC @ 120MA BBP)
BB_ENA = 0V FOR BACK BIASING DISABLED
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.8V
** FOR NO BACK BIASING
DO NOT INSTALL FETS
AND INSTALL BEAD
BACK BIASING
GND
U7001F
GND
Title :
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size: C
Project Name: N50Tr/TA
Rev: 1.00
Date: Thursday, September 25, 2008
Sheet 73 of 92



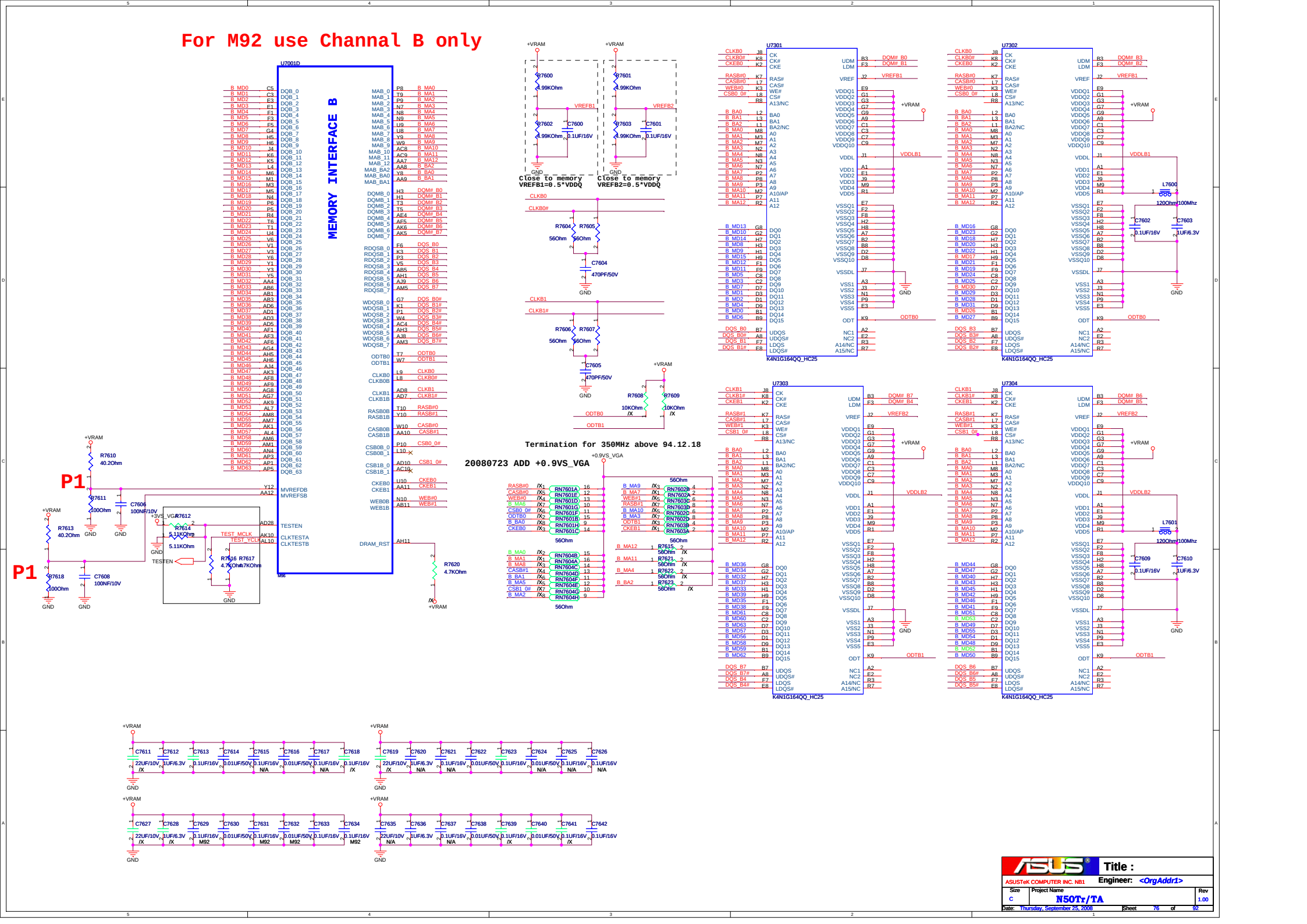
For Placement: P1 is Priority 1, P2 Second Priority and so on.....

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 74 of 92	

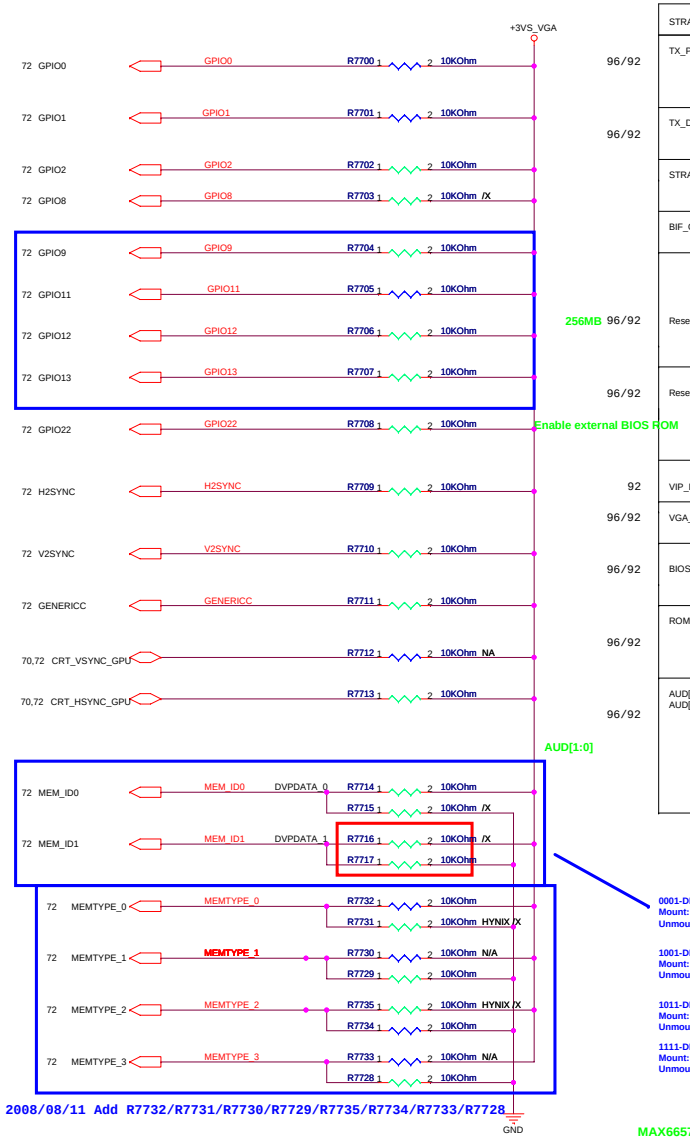


ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: C	Project Name: N50Tr/TA		Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 75 of 92		

For M92 use Channal B only



OPTION STRAPS



2008/08/11 Add R7732/R7731/R7730/R7729/R7735/R7734/R7733/R7728

M96/M92M Straps

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT	RECOMMEND
TX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)	
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 -----Disable 1------Enable	0 (internal pull-down)	
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0	
Reserved	H2SYNC	ATI internal use only . Other logic must not affect this signal during RESET Reconnended to 0	0 (internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
Reserved	GPIO_21_BB_EN GENERICC	Internal use only. INTERNALPULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
VIP_DEVICE_STRAP_EN	V2SYNC	0 - Ignore VIP device straps 1 - Use VIP device straps	0 (internal pull-down)	
VGA_DIS	GPIO_9_ROMSI	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)	
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0	
ROMIDCFG(3:0)	GPIO(9,13:11)	If BIOS_ROM_EN=1,then Config[3:0]defines the ROM type. If BIOS_ROM_EN=0,then Config[2:0]defines the primary memoru apeture size. 128MB---x000 32MB---x011 2GB---x110 256MB---x001 512MB--x100 4GB---x111 64MB----x010 1GB-----x101	0000 (internal pull-down)	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort and HDMI if adapter is detected; 10 - Audio for DisplayPort only; 11 - Audio for both DisplayPort and HDMI.	0 (internal pull-down) 0 (internal pull-down)	Design dependent.

0001-DDR2 Infineon(32MX16)
Mount: VR31, VR41, VR22, VR353
Unmount: VR27, VR40, VR21, VR352

1001-DDR2 Hynix(32MX16)
Mount: VR31, VR41, VR22, VR352
Unmount: VR27, VR40, VR21, VR353

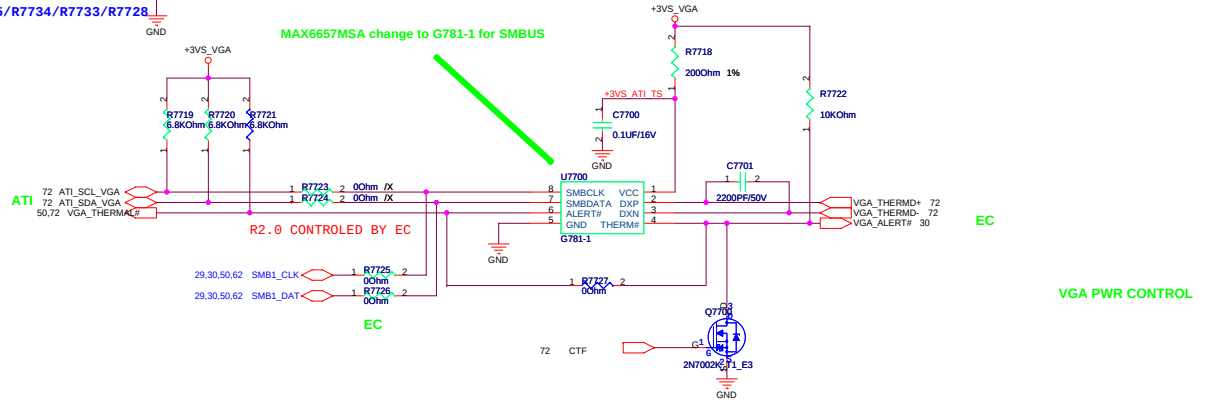
1011-DDR2 Hynix(64MX16)
Mount: VR31, VR40, VR22, VR352
Unmount: VR27, VR41, VR21, VR353

1111-DDR2 Micron(64MX16)
Mount: VR31, VR40, VR21, VR352
Unmount: VR27, VR41, VR22, VR353

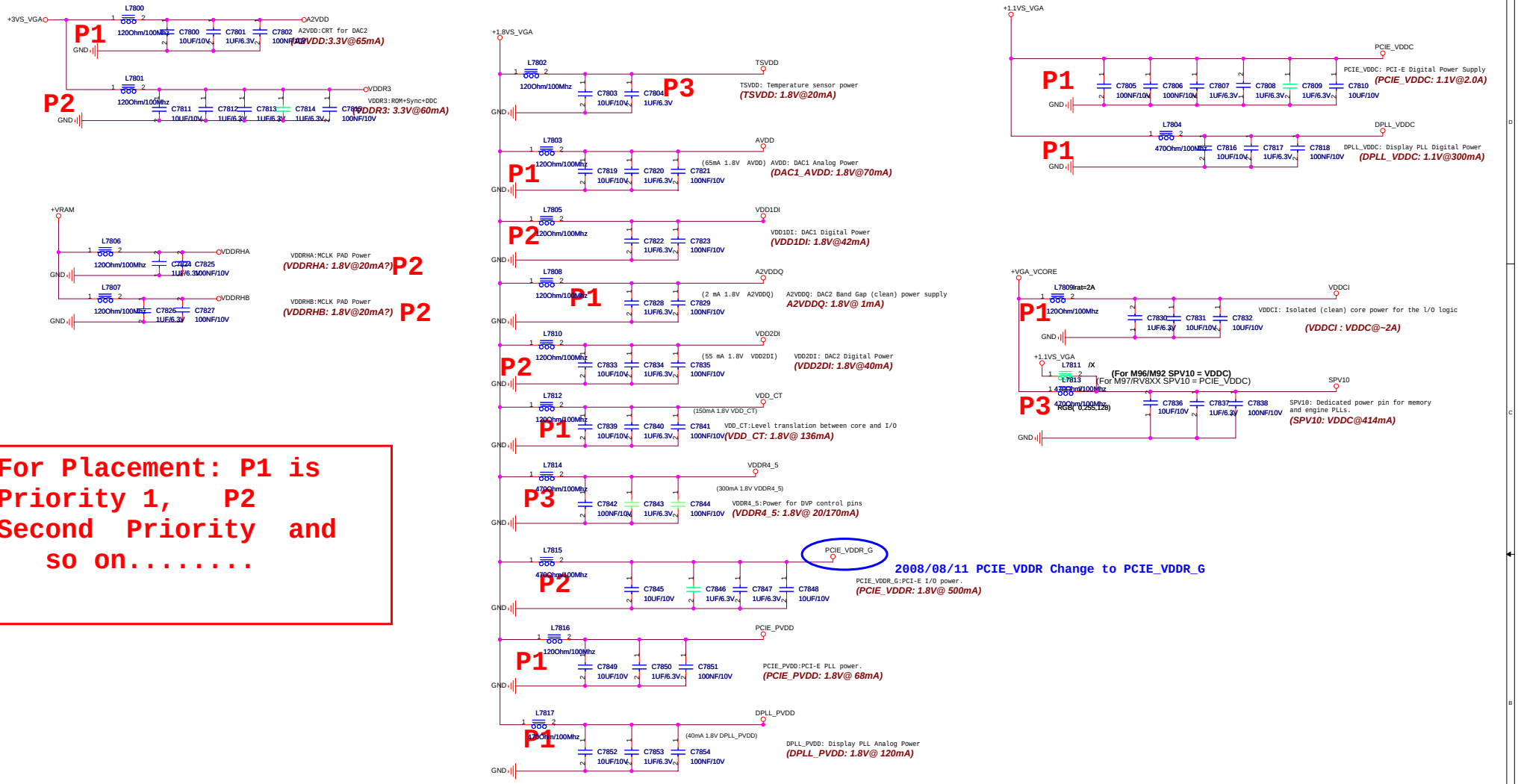
Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)		ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	F8Va	0	32M*16 (256M)	A channel
	0001		1	32M*16 (512M)	2-AB channel
	0010		2	64M*16 (512M)	A channel
	0011		3	64M*16 (1G)	2-AB channel
	0100		4	16M*16 (128M)	A channel
	0101		5	16M*16 (256M)	2-AB channel
Samsung	0110		6	32M*16 (256MB)	A channel
	0111		7	32M*16 (512MB)	2-AB channel
Hynix	1000		8	32M*16 (256M)	A channel
	1001	F8Va	9	32M*16 (512M)	2-AB channel
	1010		10	64M*16 (512M)	A channel
	1011	F8Va	11	64M*16 (1G)	2-AB channel
	1100		12	16M*16 (128M)	A channel
	1101		13	16M*16 (256M)	2-AB channel
	1110		14		
Micron	1111	F8Va	15	64M*16 (1G)	2-AB channel

MAX6657MSA change to G781-1 for SMBUS



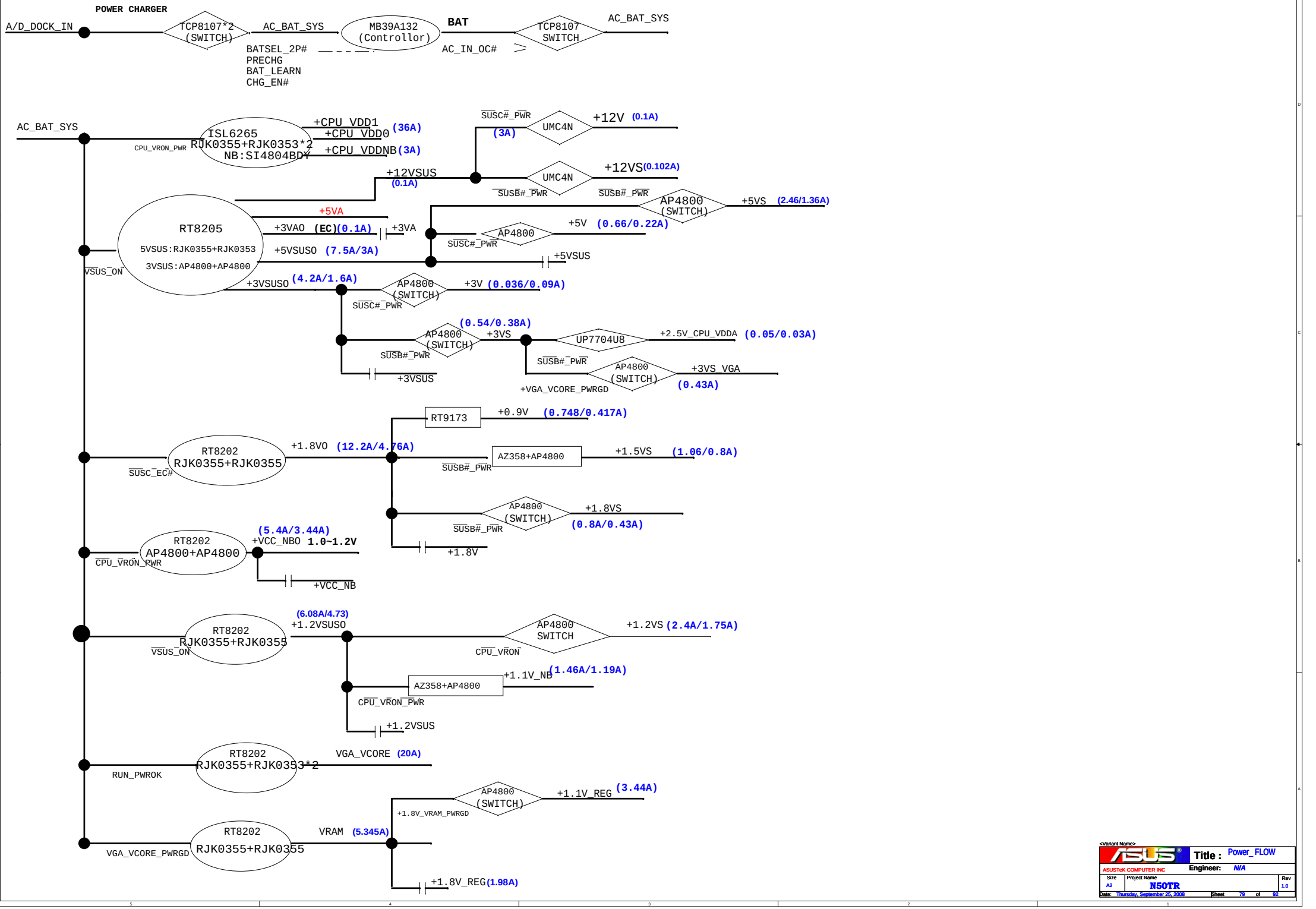
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 77 of 92	



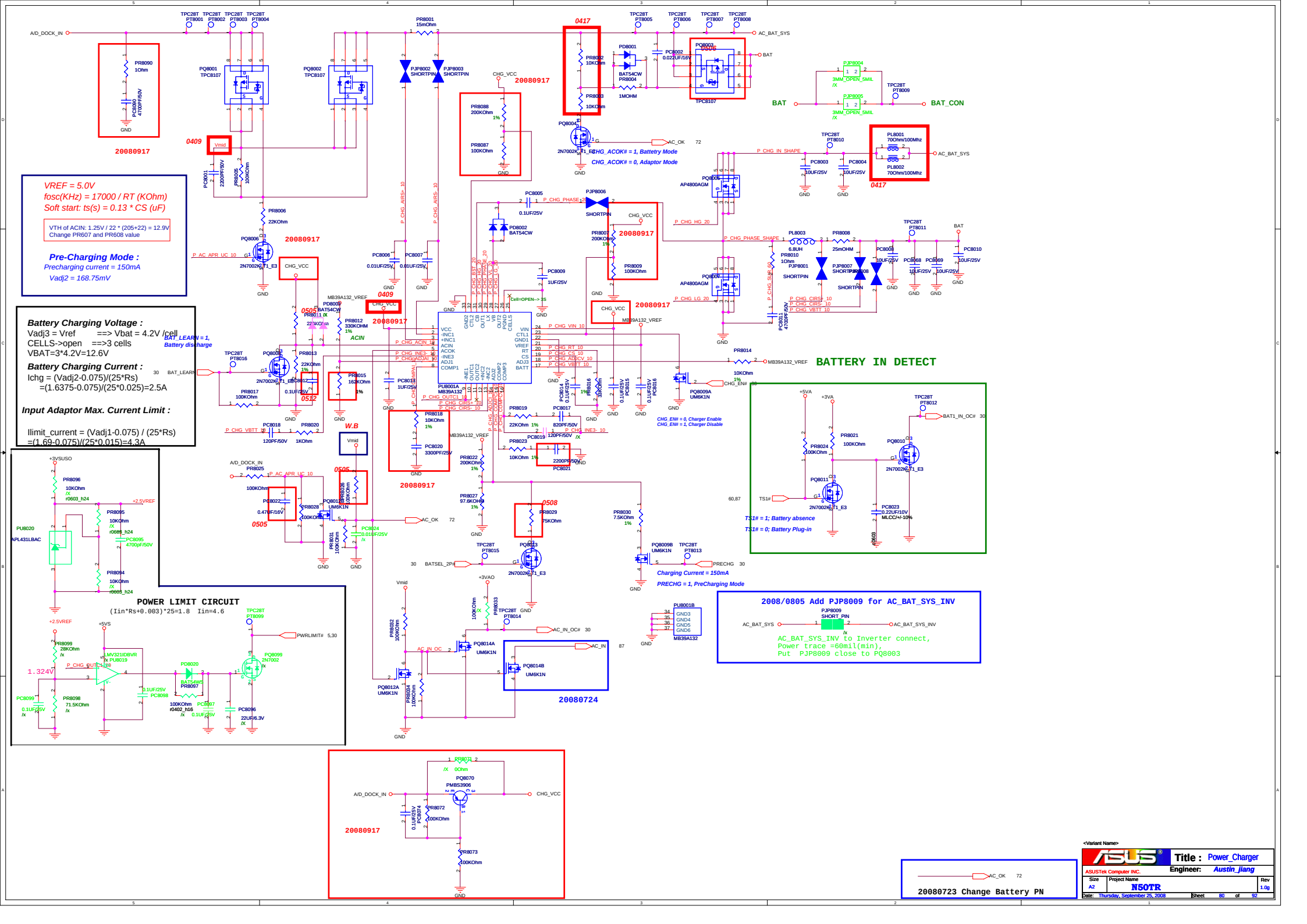
For Placement: P1 is Priority 1, P2 Second Priority and so on.....

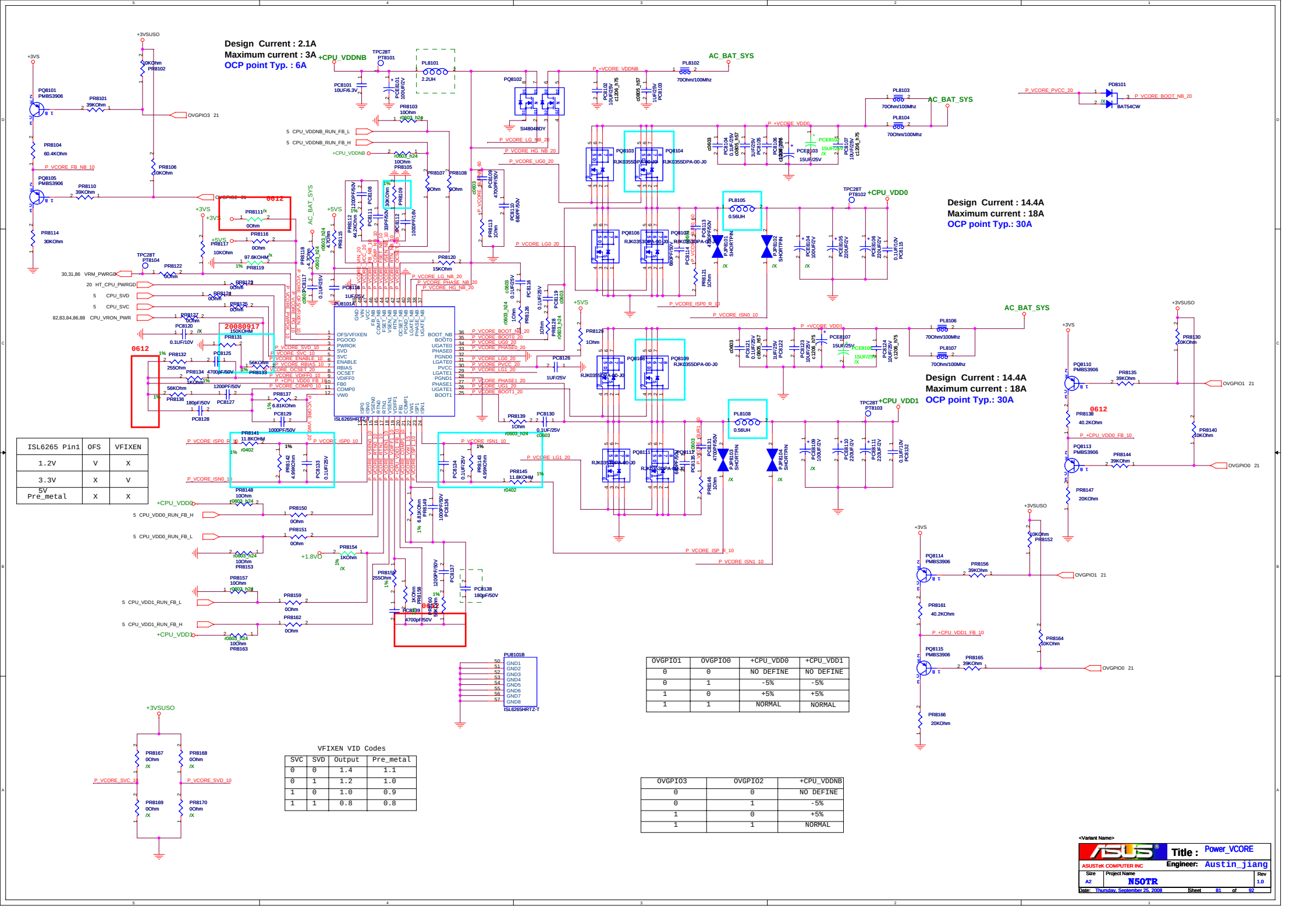
2008/08/11 PCIE_VDDR Change to PCIE_VDDR_G

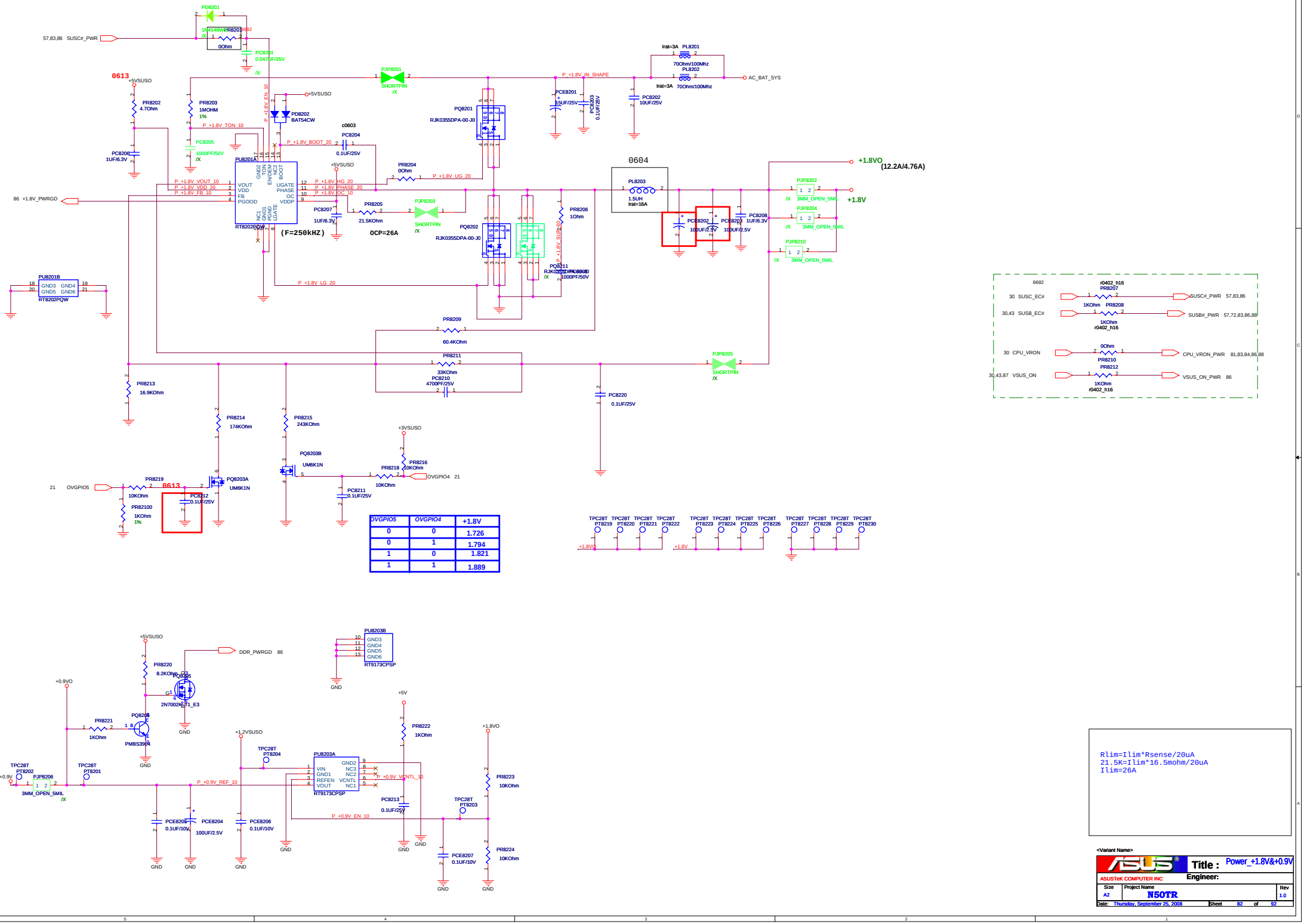
ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50Tr/TA	Rev: 1.00
Date: Thursday, September 25, 2008	Sheet 78 of 92	

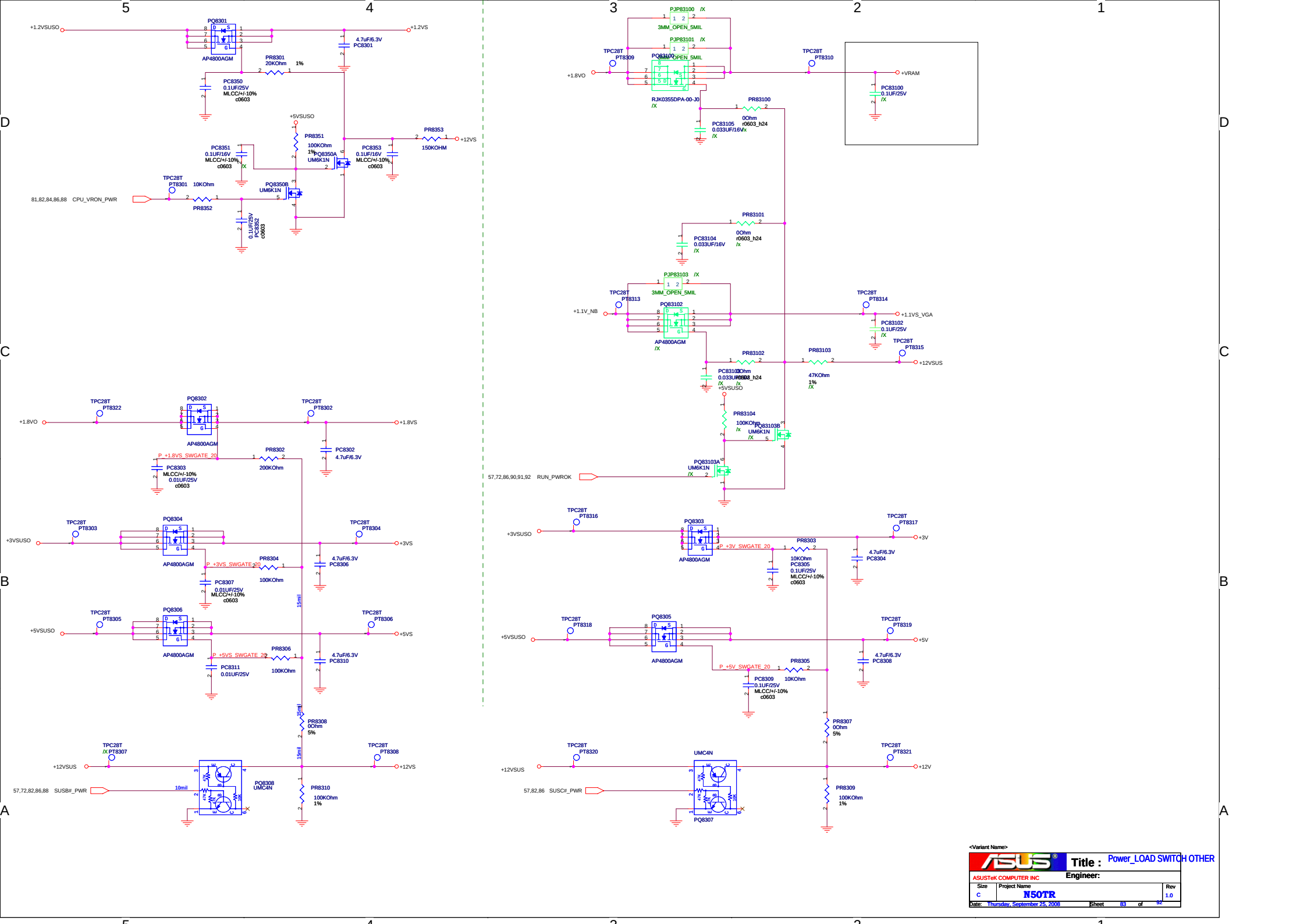


<Variant Name>
ASUSTeK COMPUTER INC
Title : Power_FLOW
Engineer: N/A
Size A2
Project Name N50TR
Rev 1.0
Date: Thursday, September 25, 2008
Sheet 79 of 92


VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
VTH of ACIN: 1.25V / 22 * (205+22) = 12.9V
Change PR607 and PR608 value
Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV
Battery Charging Voltage :
Vadj3 = Vref ==> Vbat = 4.2V /cell
CELLS->open ==>3 cells
VBAT=3*4.2V=12.6V
Battery Charging Current :
Ichg = (Vadj2-0.075)/(25*Rs)
=(1.6375-0.075)/(25*0.025)=2.5A
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.69-0.075)/(25*0.015)=4.3A
BAT_LEARN = 1, Battery discharge
ACIN
CHG_ACOK# = 1, Battery Mode
CHG_ACOK# = 0, Adaptor Mode
BATTERY IN DETECT
CHG_EN# = 0, Charger Enable
CHG_EN# = 1, Charger Disable
TS1# = 1; Battery absence
TS1# = 0; Battery Plug-in
Charging Current = 150mA
PRECHG = 1, PreCharging Mode
POWER LIMIT CIRCUIT
(Iin*Rs+0.003)*25=1.8 Iin=4.6
2008/0805 Add PJP8009 for AC_BAT_SYS_INV
AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put PJP8009 close to PQ8003
20080724
20080723 Change Battery PN
Title : Power_Charger
Engineer: Austin_Jiang
ASUSTek Computer INC.
N50TR
Thursday, September 25, 2008
Sheet 80 of 92

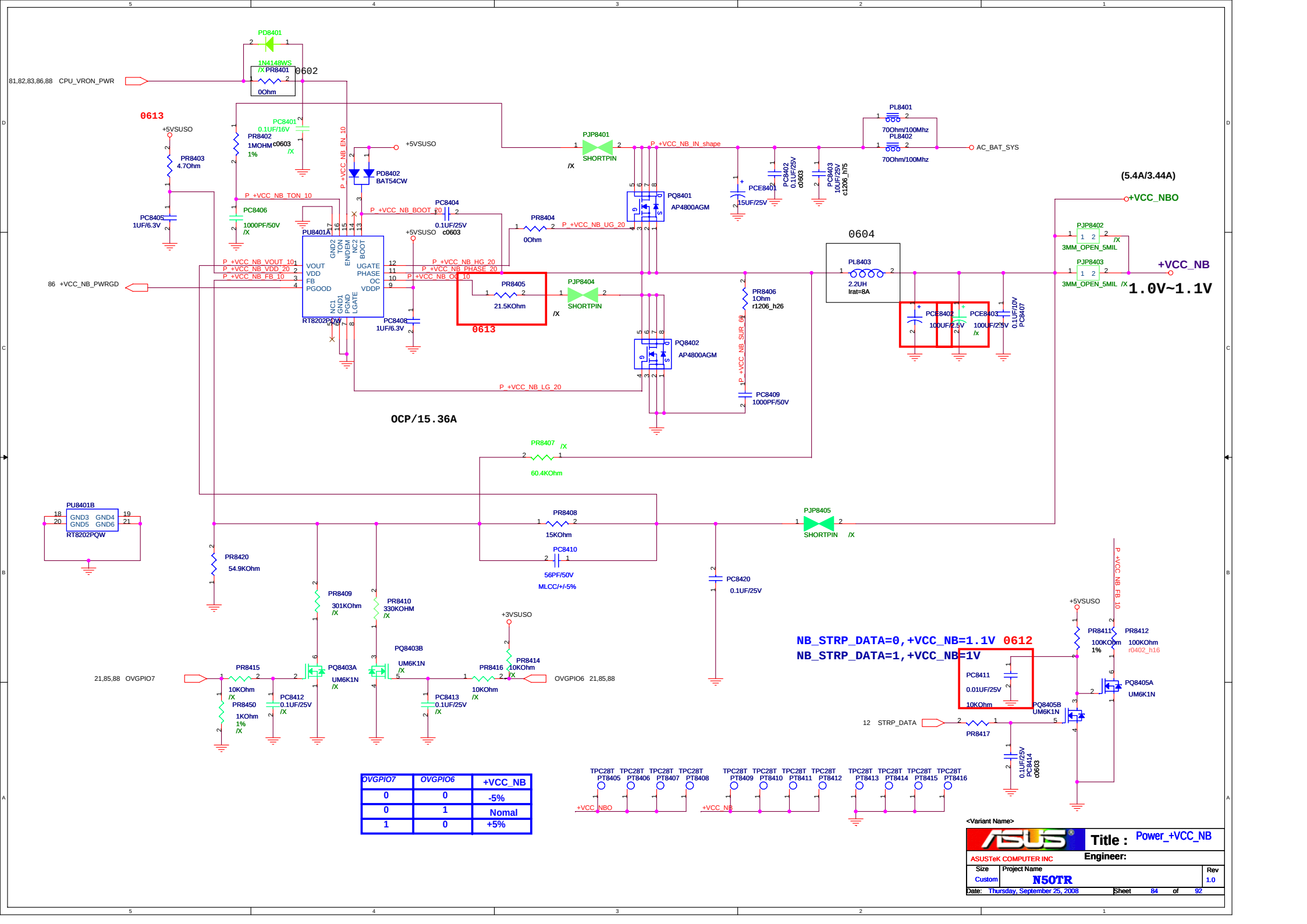

Design Current : 2.1A
Maximum current : 3A
OCP point Typ. : 6A
Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 30A
Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 30A
+CPU_VDDNB
+CPU_VDD0
+CPU_VDD1
AC_BAT_SYS
ISL6265HRTZ-T
0612
20080917
VFIXEN VID Codes
SVC SVD Output Pre_metal
0 0 1.4 1.1
0 1 1.2 1.0
1 0 1.0 0.9
1 1 0.8 0.8
ISL6265 Pin1 OFS VFIXEN
1.2V V X
3.3V X V
5V Pre_metal X X
OVGPIO1 OVGPIO0 +CPU_VDD0 +CPU_VDD1
0 0 NO DEFINE NO DEFINE
0 1 -5% -5%
1 0 +5% +5%
1 1 NORMAL NORMAL
OVGPIO3 OVGPIO2 +CPU_VDDNB
0 0 NO DEFINE
0 1 -5%
1 0 +5%
1 1 NORMAL
Title : Power_VCORE
ASUSTeK COMPUTER INC
Engineer: Austin_jiang
Project Name N50TR
Date: Thursday, September 25, 2008
Sheet 81 of 92


PD8201
1N4148WS
PR8201
0Ohm
PC8201
0.047UF/25V
57,83,86 SUSC#_PWR
0613
+5VSUSO
PR8202
4.7Ohm
PR8203
1MOHM
1%
P +1.8V_TON 10
PC8205
1000PF/50V
PC8206
1UF/6.3V
PD8202
BAT54CW
P +1.8V_EN 10
c0603
PC8204
0.1UF/25V
P +1.8V_BOOT 20
PJP8201
SHORTPIN
P +1.8V_IN_SHAPE
Irat=3A PL8201
70Ohm/100Mhz
PL8202
Irat=3A 70Ohm/100Mhz
AC_BAT_SYS
PQ8201
RJK0355DPA-00-J0
PCE8201
150UF/25V
PC8203
0.1UF/25V
PC8202
10UF/25V
PU8201A
RT8202PQW
VOUT
VDD
FB
PGOOD
LGATE
PHASE
OC
VDDP
BOOT
UGATE
ENDEM
PGND
P +1.8V_VOUT 10
P +1.8V_VDD 20
P +1.8V_FB 10
P +1.8V_HG 20
P +1.8V_PHASE 20
P +1.8V_OC 10
P +1.8V_UG 20
P +1.8V_LG 20
PR8204
0Ohm
PR8205
21.5KOhm
PC8207
1UF/6.3V
PJP8203
SHORTPIN
PQ8202
RJK0355DPA-00-J0
PR8206
1Ohm
PQ8211
RJK0355DPA-00-J0
PC8211
1000PF/50V
(F=250kHZ)
0CP=26A
0604
PL8203
1.5UH
Irat=16A
PCE8202
100UF/2.5V
PCE8203
100UF/2.5V
PC8208
1UF/6.3V
+1.8VO
(12.2A/4.76A)
+1.8V
PJP8202
PJP8204
PJP8210
3MM_OPEN_5MIL
86 +1.8V_PWRGD
PU8201B
RT8202PQW
PR8209
60.4KOhm
PR8211
33KOhm
PC8210
4700PF/25V
PJP8205
SHORTPIN
PR8213
16.9KOhm
PC8220
0.1UF/25V
PR8214
174KOhm
PR8215
243KOhm
PQ8203B
UM6K1N
PR8216
10KOhm
PR8218
10KOhm
PC8211
0.1UF/25V
+3VSUSO
21 OVGPIO5
PR8219
10KOhm
PR82100
1KOhm
1%
PQ8203A
UM6K1N
PC8212
0.1UF/25V
OVGPIO4 21
0602
r0402_h16
PR8207
30 SUSC_EC#
1KOhm
SUSC#_PWR 57,83,86
PR8208
30,43 SUSB_EC#
SUSB#_PWR 57,72,83,86,88
30 CPU_VRON
0Ohm
PR8210
CPU_VRON_PWR 81,83,84,86,88
PR8212
30,43,87 VSUS_ON
VSUS_ON_PWR 86
OVGPIO5
OVGPIO4
+1.8V
0
0
1.726
0
1
1.794
1
0
1.821
1
1
1.889
TPC28T PT8219
TPC28T PT8220
TPC28T PT8221
TPC28T PT8222
TPC28T PT8223
TPC28T PT8224
TPC28T PT8225
TPC28T PT8226
TPC28T PT8227
TPC28T PT8228
TPC28T PT8229
TPC28T PT8230
+0.9VO
+1.8V
+5VSUSO
DDR_PWRGD 86
PR8220
8.2KOhm
PQ8205
2N7002KW_T1_E3
PU8203B
RT9173CPSP
GND
+0.9VO
PR8221
1KOhm
PQ8204
PMBS3904
+1.2VSUSO
TPC28T PT8204
PU8203A
RT9173CPSP
VIN
GND1
REFEN
VOUT
GND2
NC3
NC2
VCNTL
NC1
P +0.9V_VCNTL_10
P +0.9V_REF_10
P +0.9V_EN 10
+5V
PR8222
1KOhm
PC8213
0.1UF/25V
TPC28T PT8203
PR8223
10KOhm
PR8224
10KOhm
PCE8207
0.1UF/10V
TPC28T PT8202
TPC28T PT8201
PJP8206
3MM_OPEN_5MIL
+0.9V
PCE8205
0.1UF/10V
PCE8204
100UF/2.5V
PCE8206
0.1UF/10V
Rlim=Ilim*Rsense/20uA
21.5K=Ilim*16.5mohm/20uA
Ilim=26A
<Variant Name>
Title : Power_+1.8V&+0.9V
ASUSTeK COMPUTER INC
Engineer:
Size A2
Project Name N50TR
Rev 1.0
Date: Thursday, September 25, 2008
Sheet 82 of 92



<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_LOAD SWITCH OTHER	
	Engineer:	
Size: C	Project Name: N50TR	Rev: 1.0
Date: Thursday, September 25, 2008	Sheet 83 of 92	



OVGPIO7	OVGPIO6	+VCC_NB
0	0	-5%
0	1	Nomal
1	0	+5%

<Variant Name>

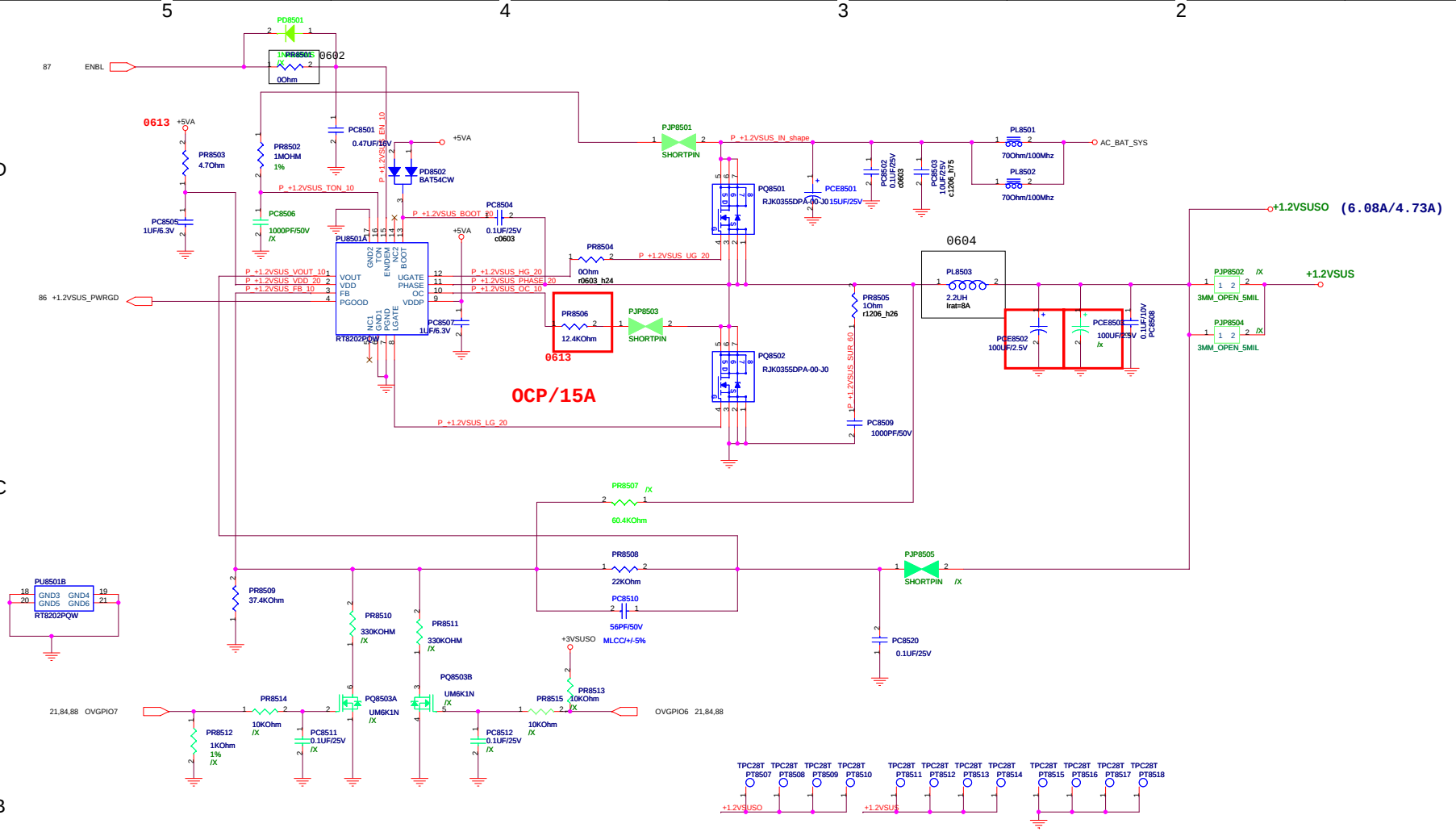
Title : Power_+VCC_NB

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 84 of 92



OVGPIO7	OVGPIO6	+1.2VSUS
0	0	1.15
0	1	1.2
1	0	1.2
1	1	1.25

<Variant Name>

ASUSTeK COMPUTER INC

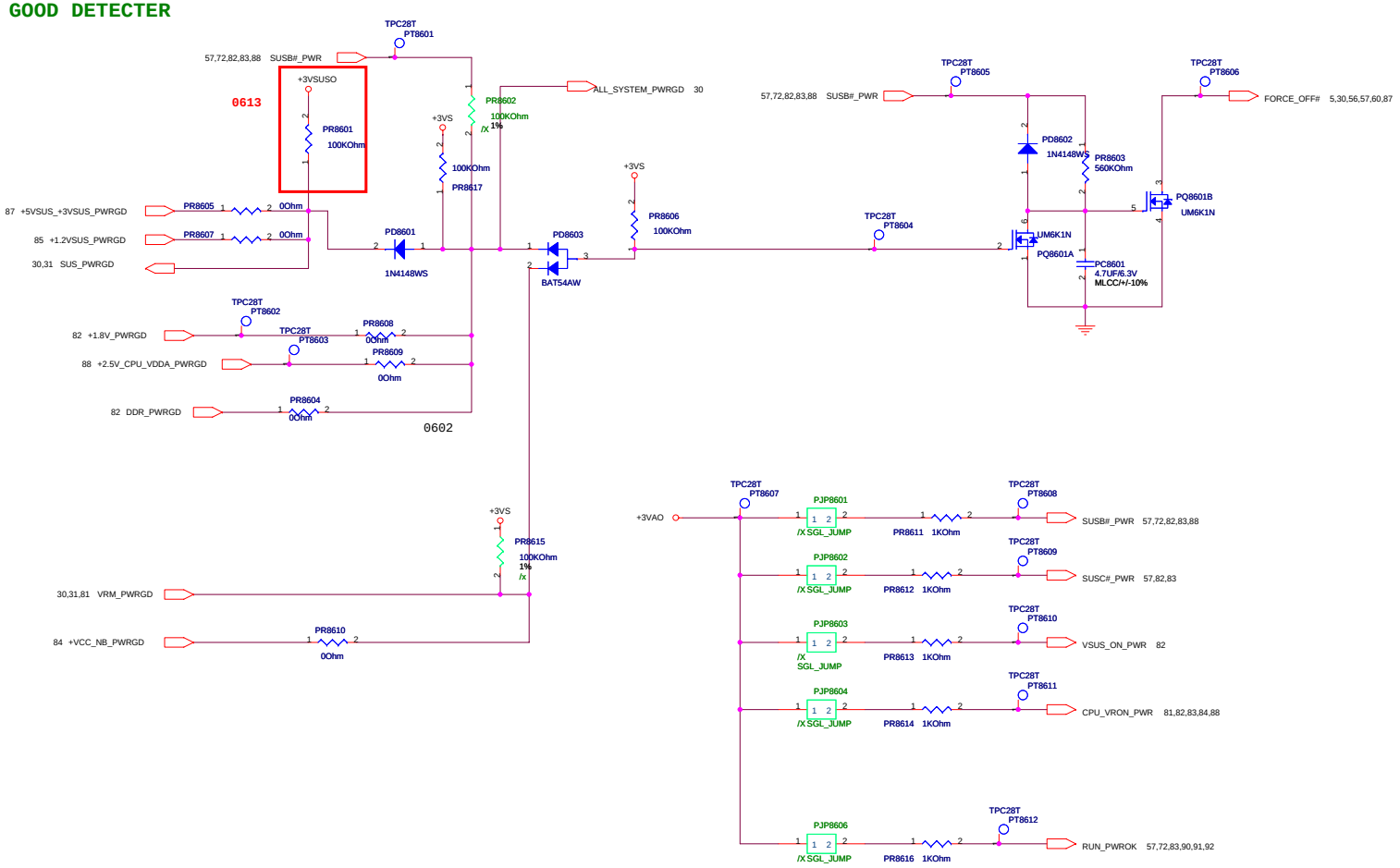
Title : Power_1.2VSUS

Engineer:

Size	Project Name	Rev
C	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 85 of 92

POWER GOOD DETECTER



<Variant Name>

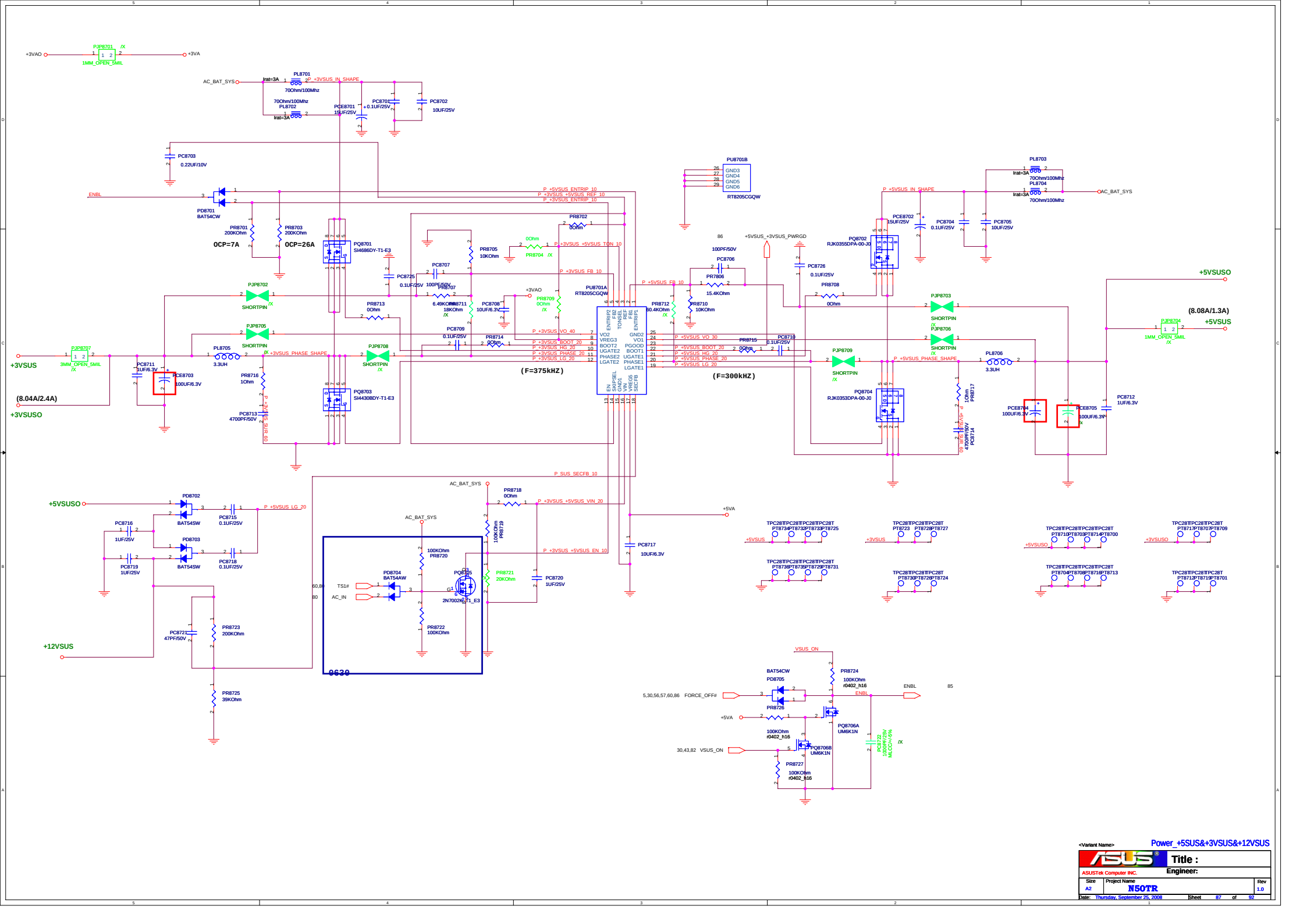
ASUSTeK COMPUTER INC

Title : Power_GOOD_DETECTER

Engineer:

Size	Project Name	Rev
C	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 86 of 92



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Power_+5SUS&+3VSUS&+12VSUS

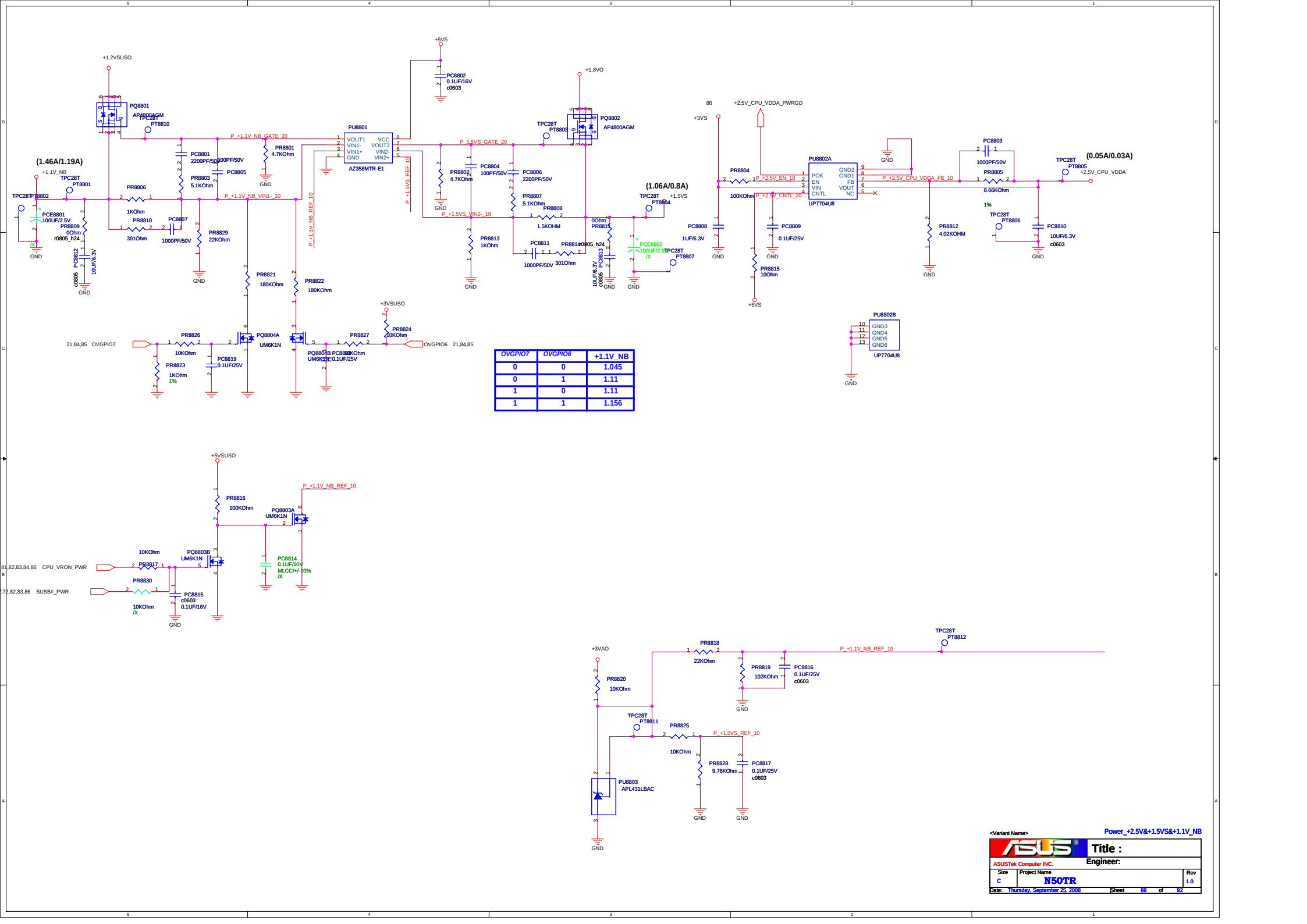
ASUSTek Computer INC.

Title :

Engineer:

Size	Project Name	Rev
A2	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 87 of 92



OVGPIO7	OVGPIO6	+1.1V_NB
0	0	1.045
0	1	1.11
1	0	1.11
1	1	1.156

<Variant Name>

Power_+2.5V&+1.5VS&+1.1V_NB

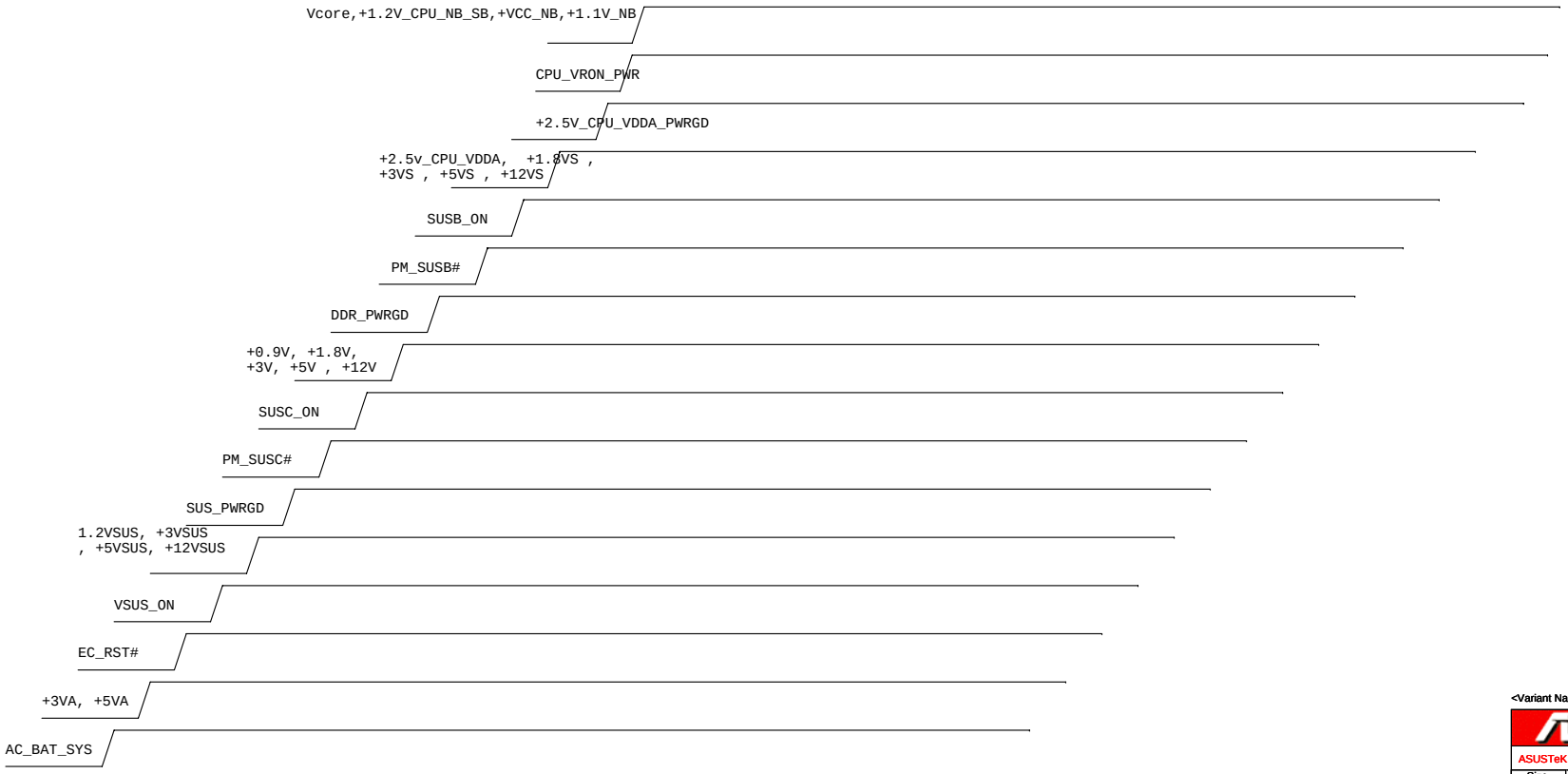
ASUSTek Computer INC.

Title :

Engineer:

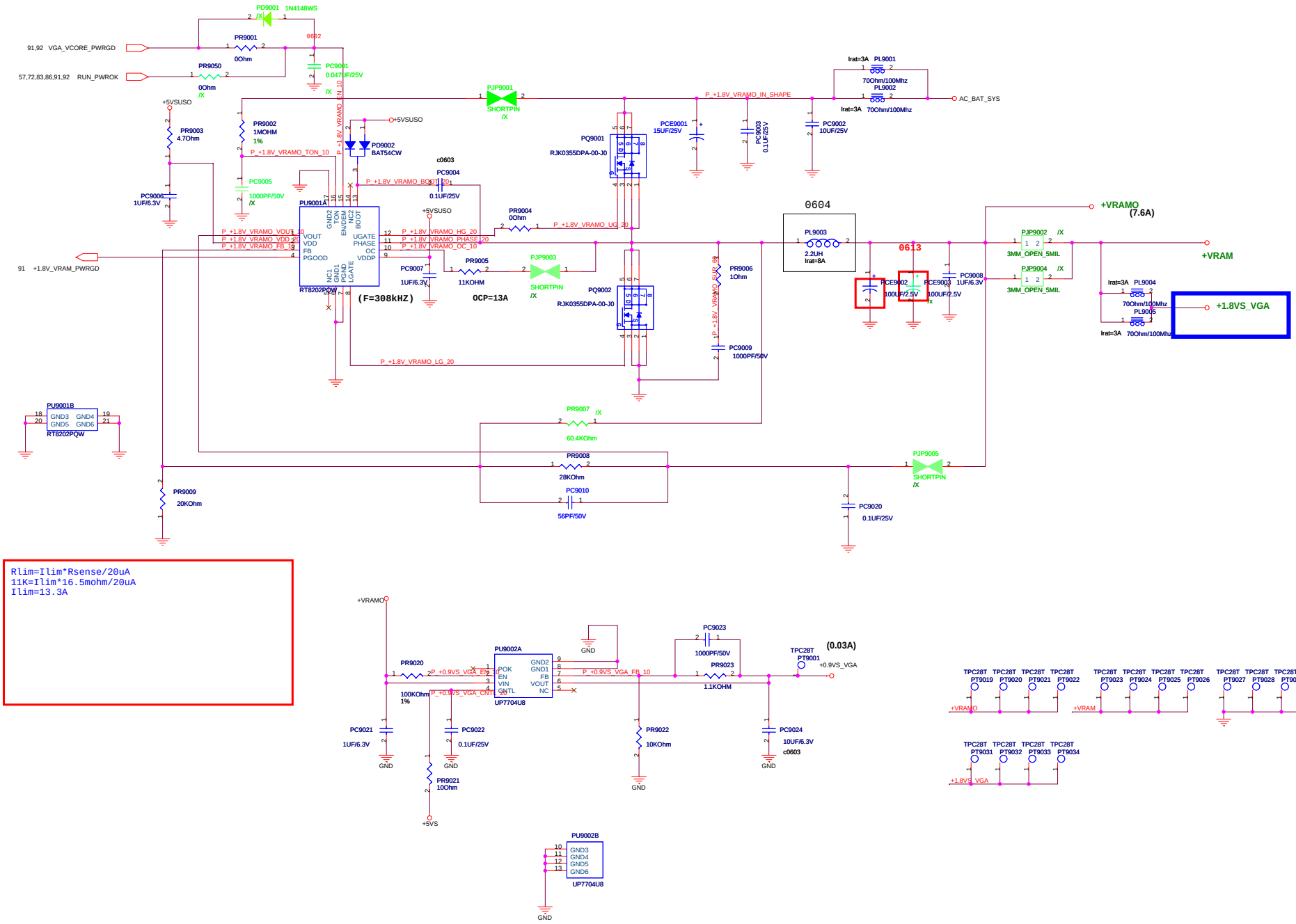
Size	Project Name	Rev
C	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 88 of 92



<Variant Name>

ASUSTeK COMPUTER INC	Title : Power SEQUENCE	
	Engineer: N/A	
Size: Custom	Project Name: N50TR	Rev: 1.0
Date: Thursday, September 25, 2008	Sheet 89 of 92	



<Variant Name>

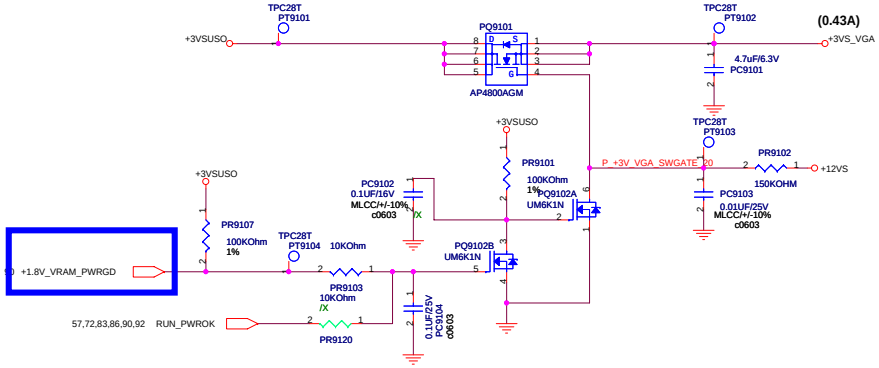
ASUSTeK COMPUTER INC

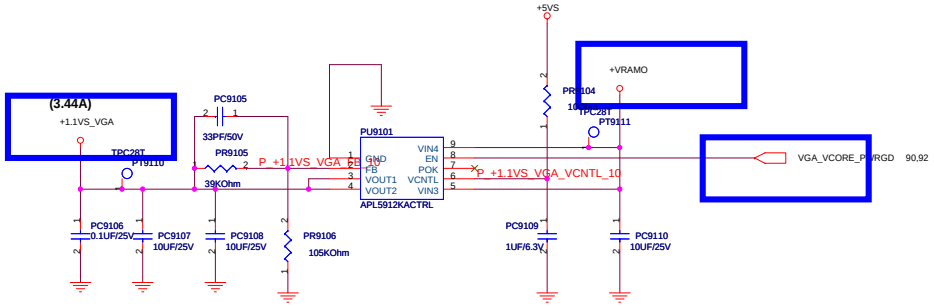
Title : Power 1.8V REG&+1.8V_VRAM

Engineer: N/A

Size	Project Name	Rev
C	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 90 of 92





<variant_name>
Power _3VS_VGA&+1.1V_REG

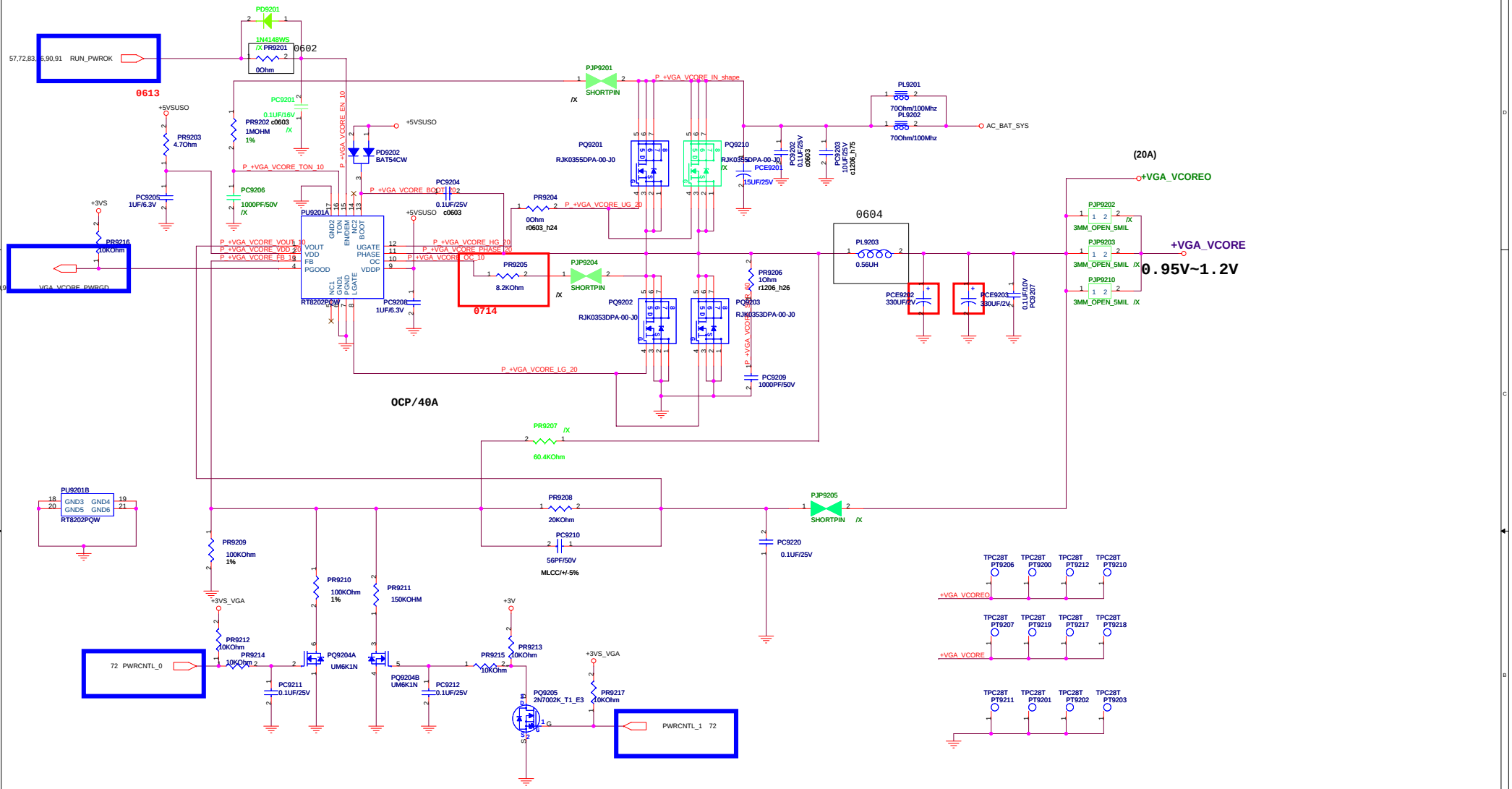
Title :

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
C	N50TR	1.0

Date: Thursday, September 25, 2008 Sheet 91 of 92
</variant_name>



PWRCNTL_0	PWRCNTL_1	VGA_VCORE
0	0	1.0
0	1	0.9
1	0	1.15
1	1	1.05

Rlim=Ilim*Rsense/20uA
8K=Ilim*3.9mohm/20uA
Ilim=41A

<Variant Name>

ASUSTeK COMPUTER INC

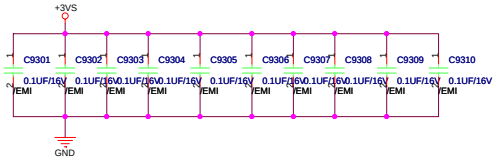
Title : Power_+VGA_VCORE

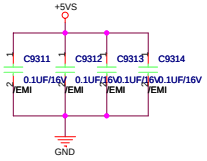
Engineer:

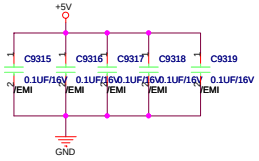
Size	Project Name	Rev
C	N50TR	1.0

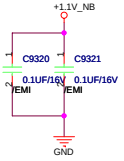
Date: Thursday, September 25, 2008 Sheet 92 of 92

0814 ADD FOR EMI









<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_+VGA_VCORE	
	Engineer:	
Size: C	Project Name: N50TR	Rev: 1.0
Date: Thursday, September 25, 2008	Sheet 93 of 93	