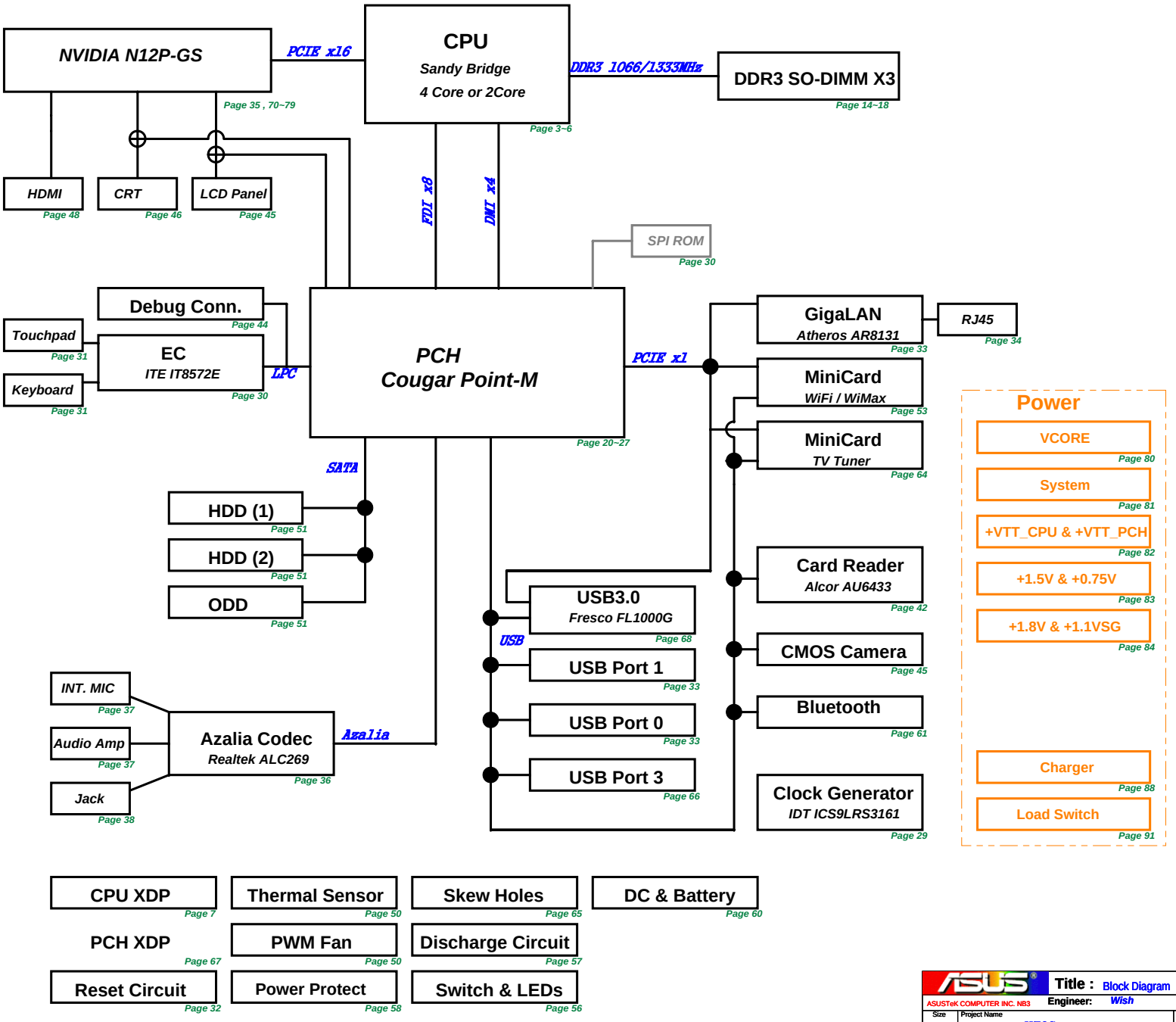
N73Sv Block Diagram



ASUSTeK COMPUTER INC. NB3	Title : Block Diagram	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 1 of 95	

PCH GPIO

PCH_IBEX GPIO	Use As	Signal Name	Int.& Ext Pull up / down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPI	NC_TP	EXT PU	+3VS
GPIO 07	GPI	USB3_SMI#	EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	INT PD	+3VSUS
GPIO 14	Native	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1_TV#	EXT PD	+3VS
GPIO 19	GPI	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2_WLAN#	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	-	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3_NEWCARD#	EXT PD	+3VSUS
GPIO 26	GPI	CLKREQ4_USB3#	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	-	+3VSUS
GPIO 29	Native		-	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT_PCH	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPI	SATA_CLK_REQ#_R	EXT PD	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PD	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PD	+3VS
GPIO 38	GPI	PCB_ID0	EXT PU / PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PU / PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	-	+3VSUS
GPIO 46	Native	NC_TP	-	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	DGPU_PWM_SELECT#_R	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PD	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU (Diode)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	GPO	EDID_SELECT#	INT TBD	+3VS
GPIO 67	Native	CLK_CR48	INT TBD	+3VS
GPIO 72	GPO	PM_BATLOW#	INT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC IT8572 GPIO

EC GPIO	Use As	Signal Name
GPA0	OD	PWR_LED#
GPA1	OD	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3	O	MUTE_LED#
GPA4	ALT	LCD_BL_PWM
GPA5	ALT	FAN_PWM
GPA6	ALT	VOLUME_LED#
GPA7	O	MEDIA_KEY_LED#
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT
GPB3	ALT	SMB0_CLK
GPB4	ALT	SMB0_DAT
GPB5	OD	A20GATE
GPB6	OD	RC_IN#
GPB7	O	PM_RSMRST#
GPC0		CLK_UC
GPC1	ALT	SMB1_CLK
GPC2	ALT	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	ALT	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	ALT	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	ALT	BUF_PLT_RST#
GPD3	OD	EXT_SCI#
GPD4	OD	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	ALT	FAN0_TACH
GPD7	OD	EXP_GATE_LED#
GPE0	O	-
GPE1	I/PU	-
GPE2	I/PU	-
GPE3		-
GPE4	ALT	PWR_SW#
GPE5	ALT	CLK_OC#
GPE6	I	LID_SW#
GPE7	I	EXP_GATE#
GPF0	ALT	OS_LED#
GPF1	O	VSUS_ON
GPF2	I	VCCP_DV0
GPF3	I	VCCP_DV1
GPF4	ALT	TP_CLK
GPF5	ALT	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck
GPG1	I	PM_SUSB#
GPG2		CLK_STRAP0
GPG6		CLK_STRAP1
GPH0	ALT	PM_CLKRUN#
GPH1		GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	OD	NUM_LED#
GPH6	OD	CAP_LED#
GPI0		HDMI_HPD
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5		-
GPI6		IDLE_HPD_INT#
GPI7		-
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	ALT	VSET_EC
GPJ3	ALT	ISET_EC
GPJ4		CPU_DV0
GPJ5	O	CPU_DV1

Design IP Source:N73JF

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LRS3197)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
VID Controller(ASM8272)	0011011x (36)	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
CPU Thermal Sensor(G781)	1001100x (9A)	
VGA Thermal IC(G781-1)	1001101x (9E)	

PCI Express

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	USB 3.0
PCIE 5	Card Reader
PCIE 6	GLAN
PCIE 7	
PCIE 8	

USB Port

USB 0	USB Port 0
USB 1	USB Port 1
USB 2	USB Port 2
USB 3	USB Port 3
USB 4	Minicard TV Tuner
USB 5	NewCard
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	

SATA Port

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

Device Identification

CPU Thermal Senser		
1st	06G023048011	G781F
2nd		

VGA Thermal Senser		
1st	06G023048010	G781-1
2nd		

Clock Gen		
1st	06G011614010	ICS9LVS3161
2nd		

ASUSTeK COMPUTER INC. NB3

Title : System Setting

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 2 of 95

Main Board

FDI disable: (For discrete graphic)

1. NC:
   FDI_TX#[0:7],FDI_TX[0:7],VCC_AXGSENSE,VSS_AXGSENSE
2. Pull-down to GND via 1KΩ ± 5% resistor:
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving
3. Connected to GND:
   VCCAXG
4. Can be connected to GND directly:
   DPLL_REF_CLK,DPLL_REF_CLK#
5. Connect to +V1.05S rail:
   VCCFDIPLL

eDP disable/Enable

CFG[4]:
Enable: Mount R0503, R0303=1K
Disable: un-mount R0503, R0303=10Kohm

CPU socket P/N change to 12G011909893

U0301A

DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP

SOCKET989

Huron River PCIE support
2.5 GT/s, 5 GT/s and 8 GT/s

PCIE AC Coupling Capacitors:
1. 436735 PDG Page 39, 75nF~200nF
2. 431433 EMERALD LAKE Schematic 220nF
3. 436735 PDG Page 41, 180nF~265nF

修改CPU Reset,分壓沒辦法meet Rise and fall time spec

U0303 74LVC1G07GW

SKTOCC# (Socket Occupied): pulled to ground on the processor package

PROCHOT#: 0.15ns<Trf<0.44nS, 0.1ns<Tf<0.45ns (measured between 0.7*VCCP and 0.3*VCCP

CATERR#: This signal indicates that the system has experienced a catastrophic error and can't continue to operate

connected 43pF close to the IMVP

RNX0301 close to CPU, C0301 and C0302 Close to RNX0301

100 MHz, Come form PCH

For eDP 120MHz

Follow 436715_4_sodimm_Rev0.9

MISC
CLOCKS
THERMAL
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT

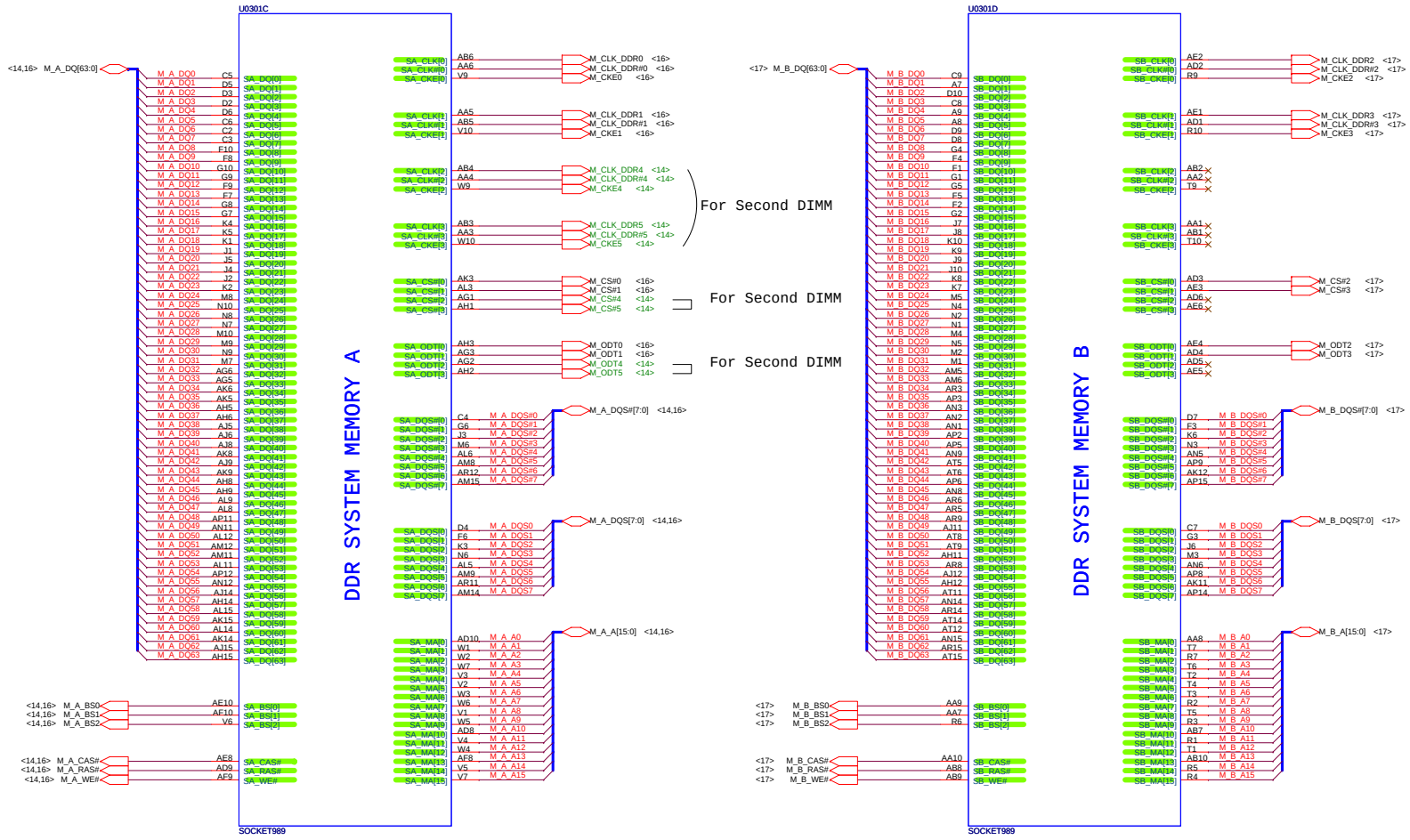
PM_DRAMPWROK: 0.15nS<Trf<0.42nS, 0.09ns<Tf<0.36ns (measured between 0.7*VCCP and 0.3*VCCP

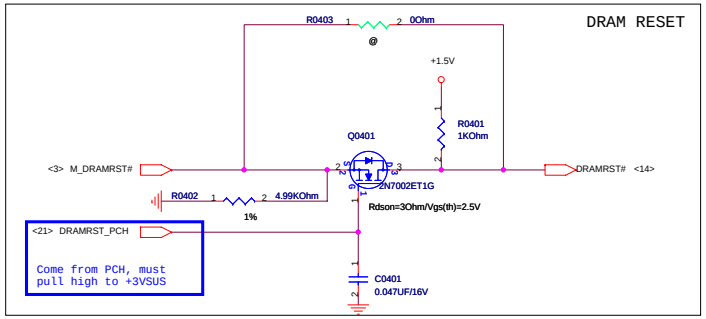
CPU_RST#: 0.25nS<Trf<0.42nS, 0.09ns<Tf<0.36ns (measured between 0.7*VCCP and 0.3*VCCP

修改CPU Reset,分壓沒辦法meet Rise and fall time spec

U0302 74LVC1G07GW

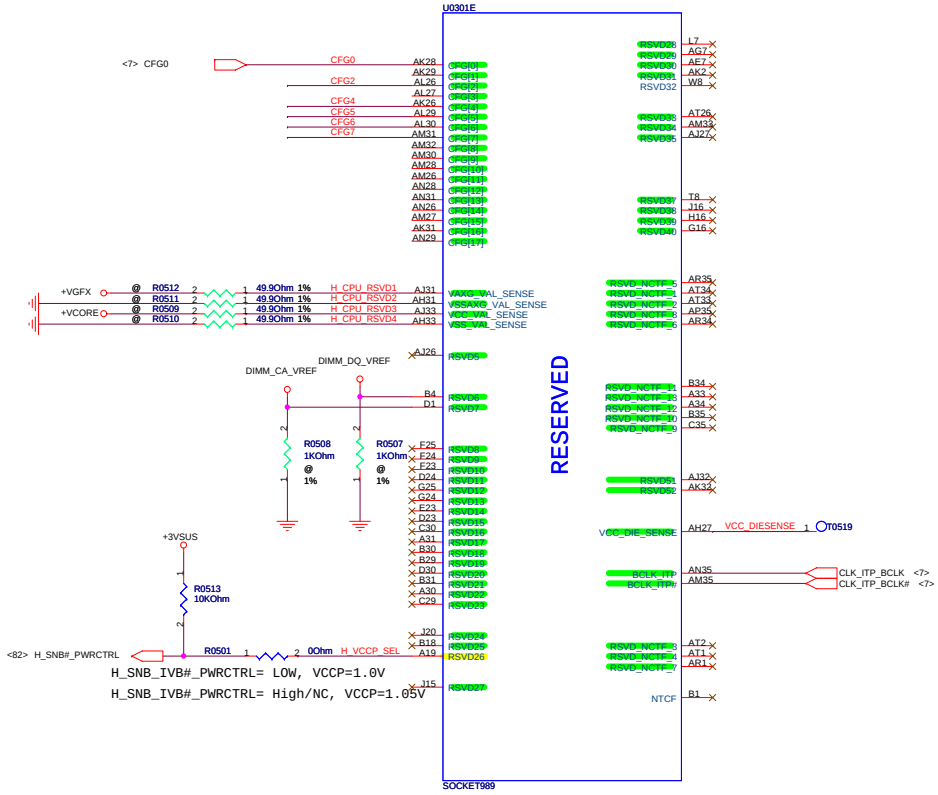
ASUSTeK COMPUTER INC. NB3	Title : CPU_DMI,PEG,FDI,CLK,MISC		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 3 of 95		

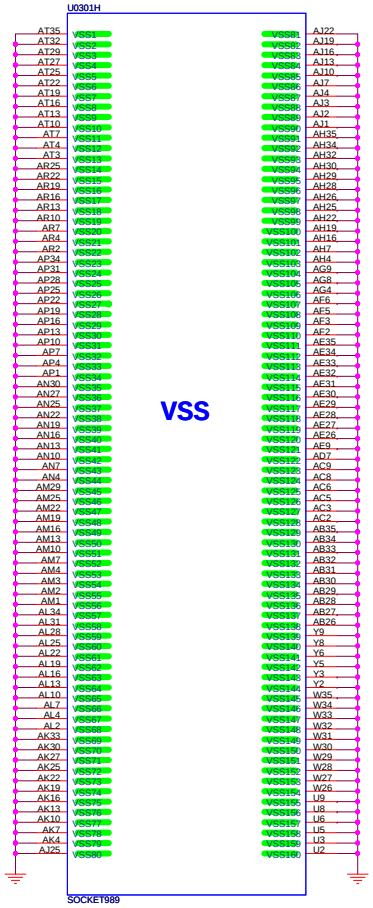


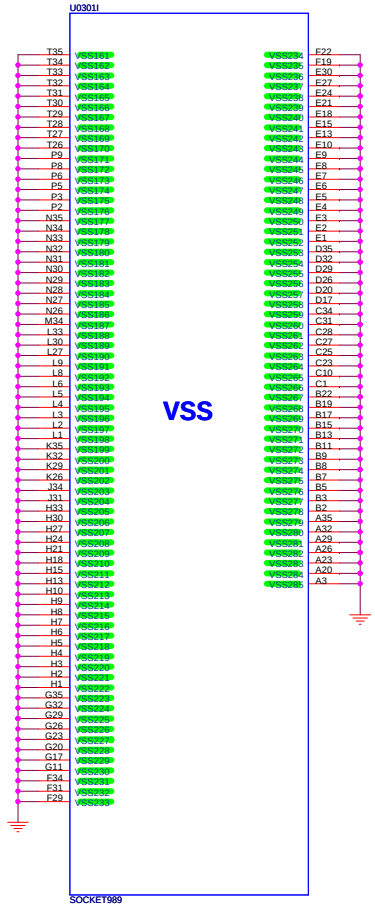


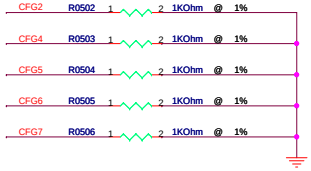
ASUSTeK COMPUTER INC. NB3	Title : CPU_DDR3		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 4 of 95		

1，拿掉測點,以需有Via 2，拿掉net
CFG1,CFG3,CFG8~CFG17,以防止layout后處理一直報錯。









CFG strapping information:

CFG[2]: PEG Static Lane Reversal (For the 16X)

- 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

CFG[4]: Display Port Presence Strap

- 1 : (Default) Disable; No Physical Display Port attached to Embedded Display Port
- 0 : Enable; An external Display Port device is connected to the Embeded Display port

CFG[6:5]: PCIE Port Bifurcation Straps

- 11 : (Default) X16 - Device 1 functions 1 and 2 disable
- 10 : X8, X8 - Device 1 function 1 enabled; Function 2 disable
- 01 : Reserved - (Device 1 Function 1 disable ; Function 2 enable
- 00 : X8, X4 X4 - Device 1 function 1 and 2 enabled

CFG[7]: Defer Training

-1: (Default) PEG Train immediately following xxRESETB de assertion

-0: PEG Wait for BIOS for training

ASUSTeK COMPUTER INC. NB3

Title : CPU_CFG,RSVD,GND

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 5 of 95

POWER

2C (35W) : 52A
4C (45W) : 78A

U0301F

CORE SUPPLY

PEG AND DDR

+VCORE_CPU

+VTT_CPU 10A

C0604 22UF/6.3V, C0605 22UF/6.3V
C0607 22UF/6.3V, C0608 22UF/6.3V, C0609 22UF/6.3V, C0610 22UF/6.3V
C0614 22UF/6.3V, C0615 22UF/6.3V
C0617 22UF/6.3V, C0618 22UF/6.3V, C0619 22UF/6.3V, C0620 22UF/6.3V
CE0601 330UF/2V, CE0602 330UF/2V

+VTT_CPU
C0677 0.1UF/16V, C0678 0.1UF/16V, C0679 0.1UF/16V

SVID

VIDALERT#, VIDSCLK, VIDSOUT

+VTT_CPU
R0605 75Ohm
R0602 43Ohm
R0604 130Ohm 1%

AJ29 H_CPU_SVIDALRT#
AJ30 H_CPU_SVIDCLK
AJ28 H_CPU_SVIDDAT

VR_SVID_ALERT# <80>
VR_SVID_CLK <80>
VR_SVID_DATA <80>

SENSE LINES

VCCSENSE, VSSSENSE
AJ35, AJ34
SL0604, SL0605 8482

VCCSENSE <80>
VSSSENSE <80>

VCCIO_SENSE, VSSIO_SENSE
B10, A10
T0601

VCCP_SENSE <82>
VSSP_SENSE <82>

SOCKET989

Power stuff
220uF*2,so EE only
reserve *1

100ohm R0606 & R0607 delete,Power stuff

PC8071,PC8072 change to 10uF,so its can be in CPU socket

+VCORE
In CPU socket
PC8070 22UF/6.3V c0805
PC8071 10UF/6.3V c0603
PC8072 10UF/6.3V c0603
PC8073 22UF/6.3V c0805
PC8074 22UF/6.3V c0805
PC8075 22UF/6.3V c0805
PC8076 22UF/6.3V c0805
PC8077 22UF/6.3V c0805
PC8078 22UF/6.3V c0805
PC8079 22UF/6.3V c0805

+VCORE
close CPU socket
PC8080 22UF/6.3V c0805
PC8081 22UF/6.3V c0805
PC8082 22UF/6.3V c0805
PC8083 22UF/6.3V c0805
PC8084 22UF/6.3V c0805
PC8085 22UF/6.3V c0805
PC8086 22UF/6.3V c0805
PC8087 22UF/6.3V c0805
PC8088 22UF/6.3V c0805
PC8089 22UF/6.3V c0805

+VGFX_CORE, +VGFX
+1.05VS, +VTT_CPU

POWER

U0301G

GRAPHICS

+VGFX 33A

C0628 22UF/6.3V, C0629 22UF/6.3V, C0630 22UF/6.3V
C0631 22UF/6.3V, C0632 22UF/6.3V, C0633 22UF/6.3V
C0634 22UF/6.3V
CE0604 330UF/2V
C0635 22UF/6.3V, C0636 22UF/6.3V, C0637 22UF/6.3V
C0638 22UF/6.3V, C0639 22UF/6.3V, C0640 22UF/6.3V
C0643 22UF/6.3V

SENSE LINES

VAXG_SENSE, VSSAXG_SENSE
AK35, AK34
VCC_AXG_SENSE <80>
VSS_AXG_SENSE <80>

VREF

SM_VREF
AL1 +V_SM_VREF_CNT

+V_SM_VREF should have 10 mils trace width

0930: R0617, R0618 Change to 1K

+VDDQ
R0617 1KOhm 1%
R0618 1KOhm 1%

DDR3 -1.5V RAILS

+VDDQ 5A

C0647 10UF/6.3V, C0648 10UF/6.3V, C0649 10UF/6.3V
C0650 10UF/6.3V, C0651 10UF/6.3V, C0652 10UF/6.3V
CE0607 330UF/2V

+1.5VS

1009 change +1.5V to +1.5VS for energy star

SA RAIL

+0.8VS 6A

VCCSA
C0653 10UF/6.3V, C0654 10UF/6.3V, C0655 10UF/6.3V, C0656 10UF/6.3V
CE0608 330UF/2V

1.8V RAIL

+1.8VS
SL0607 6805
C0644 10UF/6.3V, C0645 1UF/6.3V, C0646 1UF/6.3V
1A
VCCPLL
CE0605 330UF/2V

MISC

VCCSA_SENSE
R0610 100Ohm 1%
T0602
VCCSA_SEL0 <87>
VCCSA_SEL1 <87>
R0608 1KOhm
R0609 1KOhm

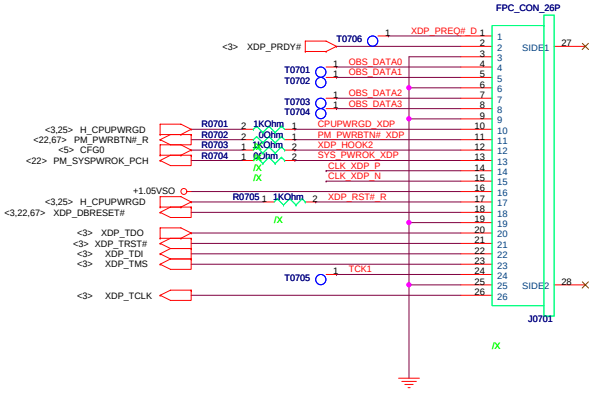
SOCKET989

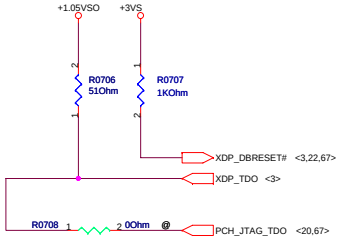
It must be min 100ns after to +1.5Vs reaches 80%

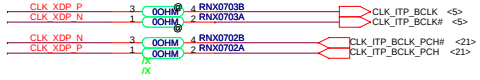
VCCSA_SEL0	VCCSA_SEL1	VCCSA_SEL
L	L	0.9V
L	H	0.8V
H	L	0.75V
H	H	0.65V

ASUSTeK COMPUTER INC. NB3

Title : CPU_PWR
Engineer: Wish
Size: C
Project Name: N73Sv
Rev: 1.0
Date: Wednesday, October 13, 2010
Sheet 6 of 95







ASUSTeK COMPUTER INC. NB3	Title : CPU_XDP	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 7 of 95	

Main Board

ASUSTeK COMPUTER INC. NB3	Title : NB_****		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 8 of 95		

ASUSTeK COMPUTER INC. NB3	Title : NB_****	
	Engineer: *Wish*	
Size: A	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 9 of 95	

Title :	NB_****
ASUSTeK COMPUTER INC. NB3	Engineer: Wish
Size: A	Project Name: N73Sv
Rev: 1.0	
Date: Wednesday, October 13, 2010	Sheet 10 of 95

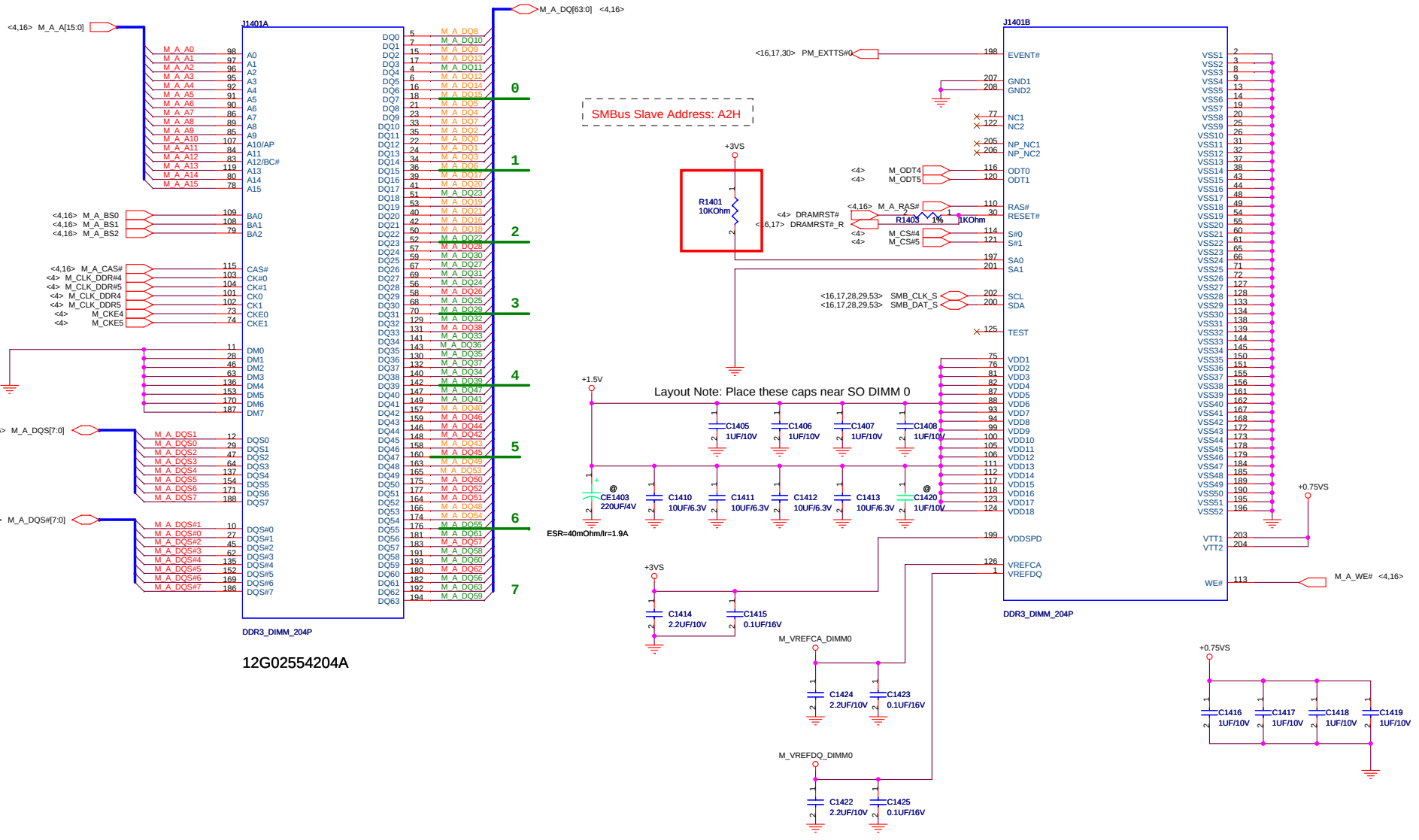
Title :	NB_****
ASUSTeK COMPUTER INC. NB3	Engineer: Wish
Size: A	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 11 of 95

Main Board

ASUSTeK COMPUTER INC. NB3	Title : NB_****	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 12 of 95	

ASUSTeK COMPUTER INC. NB3		Title : NB_****	
		Engineer: Wish	
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010		Sheet 13 of 95	

CH-A-4mm-TOP

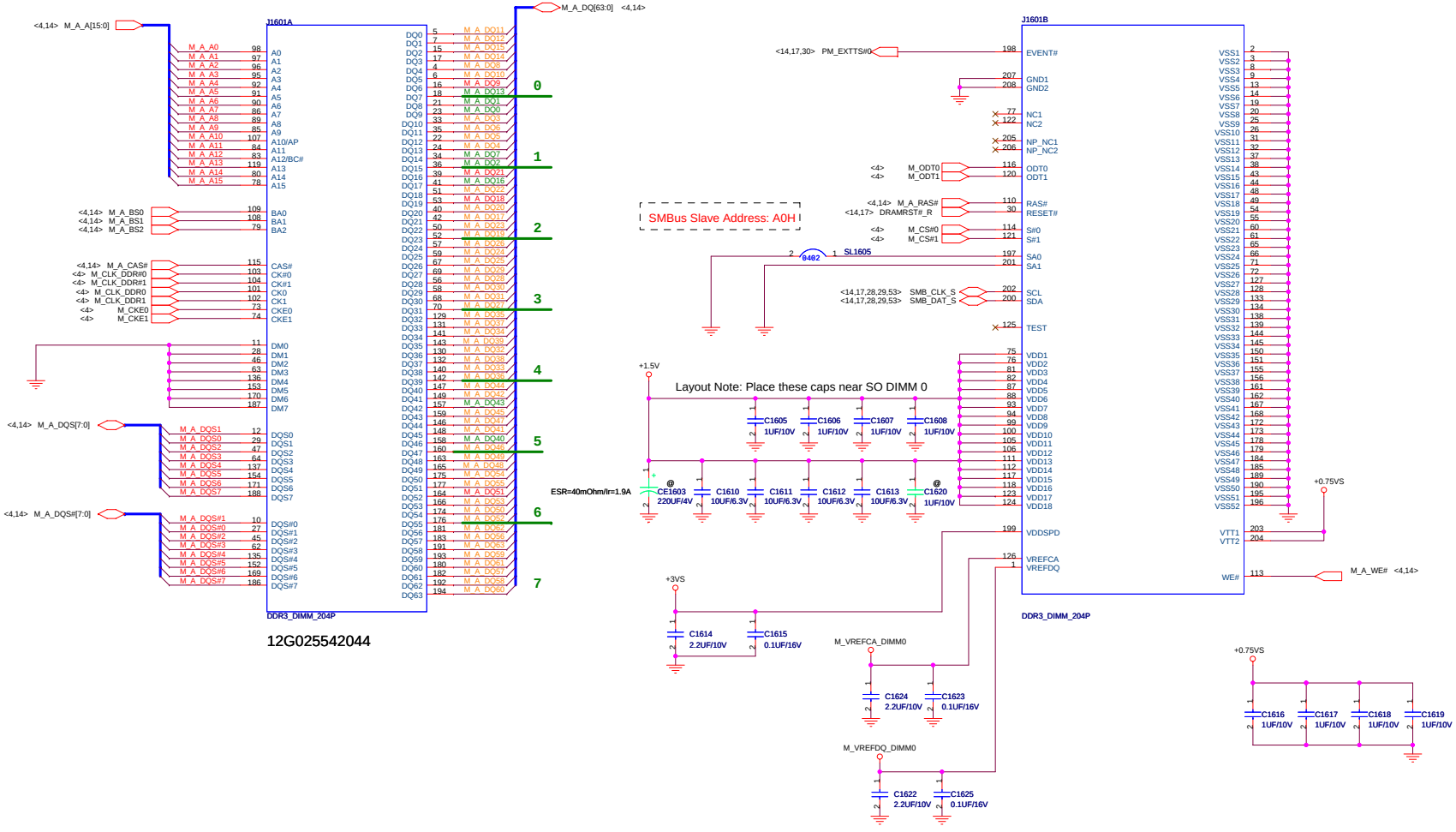


Title	DDR3 SO-DIMM_0
ASUSTeK COMPUTER INC. NB6	Engineer: Wish
Size: Custom	Project Name: N73Sv
Rev	1.0
Date: Wednesday, October 13, 2010	Sheet 14 of 95

Main Board

ASUSTeK COMPUTER INC. NB3	Title : DDR3_****		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 15 of 95		

CH-A-5.2mm-BOT

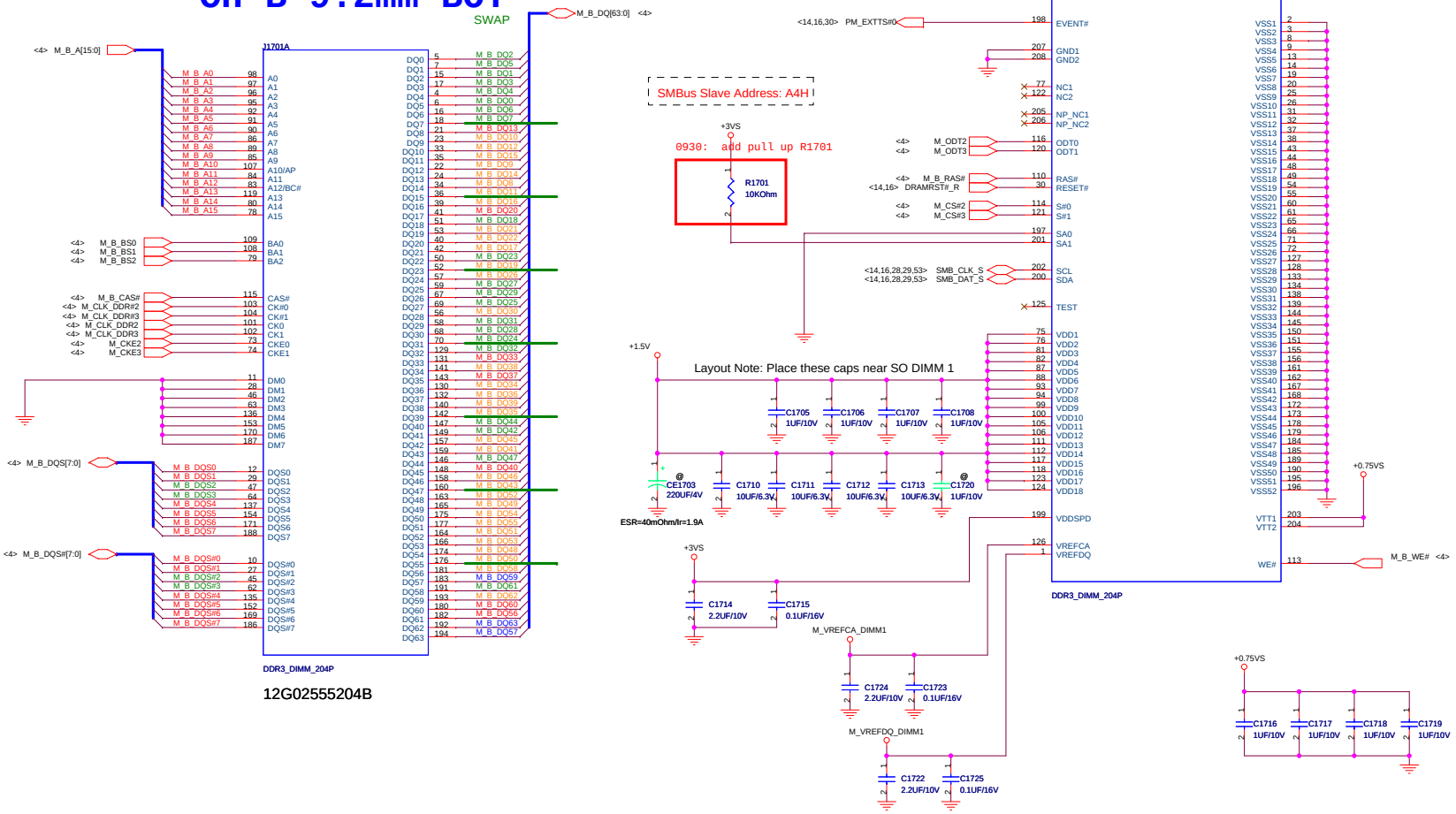


12G025542044

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_0	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 16 of 95	

CH-B-9.2mm-BOT

SWAP



12G02555204B

SMBus Slave Address: A4H

+3VS

0930: add pull up R1701

R1701 10KOhm

+1.5V

Layout Note: Place these caps near SO DIMM 1

C1705 1UF/10V
C1706 1UF/10V
C1707 1UF/10V
C1708 1UF/10V
@ CE1703 220UF/4V
ESR=40mOhm/Ir=1.9A
C1710 10UF/6.3V
C1711 10UF/6.3V
C1712 10UF/6.3V
C1713 10UF/6.3V
@ C1720 1UF/10V

+0.75VS

+3VS

C1714 2.2UF/10V
C1715 0.1UF/16V

M_VREFCA_DIMM1

C1724 2.2UF/10V
C1723 0.1UF/16V

M_VREFDQ_DIMM1

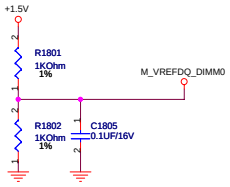
C1722 2.2UF/10V
C1725 0.1UF/16V

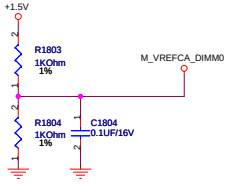
+0.75VS

C1716 1UF/10V
C1717 1UF/10V
C1718 1UF/10V
C1719 1UF/10V

ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1		
	Engineer: Wish		
Size C	Project Name N73Sv		Rev 1.0
Date: Wednesday, October 13, 2010	Sheet 17 of 95		

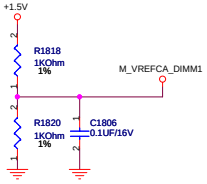
For DDR3_VREF command & address.

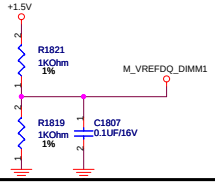




M1

M1: Fixed SO-DIMM VREF_DQ (Default Stuffing)





ASUSTeK COMPUTER INC. NB3	Title : DIM_CA/DQ Voltage	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 18 of 95	

Main Board

ASUSTeK COMPUTER INC. NB3

Title : CPU_VID Controller_*

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 19 of 95

RTC battery

BATT HOLDER @ IO BOARD 2

PCH P/N : 02G010027100

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Stuff For Moff

HDA_SYNC(On-Die PLL VR voltage select):
Rising edge of RSMRST# pin
High:1.5V, Low:1.8V (default)

stuff R2027 for 1.5V +VCCAFDI

reserve for power noise

HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achive the Vihmin at PCH input.Therefore, platform may need to isolate this signal from the codec during the strap phase.

SATA 0	Main HD
SATA 1	2nd HD
SATA 2	ODD
SATA 3	
SATA 4	
SATA 5	

Boot BIOS Strap:GNT1#(BBS0), SATA1GP(BBS1)

ACZ_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V (2) ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V

0930: Maunt for ME firmware update

HD Audio

JTAG

For PU/PD

SPKR:No Reboot strap

GPIO33 is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : Disable, LOW : Enable

DPDG(P.28):510hm, CRB:4.7KOhm

stuff ??

Boundary Scan TP (PCH)

PCH_JTAG_TCK T2008
PCH_JTAG_TMS T2009
PCH_JTAG_TDI T2010
PCH_JTAG_TDO T2011
RTCRST# T2013
INTVRMEN T2015
SRTCRST# T2016

Intel Anti-Theft Technology: Enable=High

SATALED#: O.D. 6mA

Title	C8_IBEX(1)SATA,IHDA,RTC,LPC
ASUSTeK COMPUTER INC.	Engineer: Wish
Size: C	Project Name: N73Sv
Rev	1.0
Date: Wednesday, October 13, 2010	Sheet 20 of 95

If support PCIE 3.0, pls change all 0.1uF to 0.22uF

PCIE1: TV
PCIE2: WLAN
PCIE4: USB3.0
PCIE6: LAN

U2001B

PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS

COUGARPOINT-H

Check BIOS
Programmable output clock

PCH CLKREQ Setting:

C2108與C2109換成10pF

R2108: For Xtal measurement

stuff:Integrated clock mode

ASUSTeK COMPUTER INC.	Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 21 of 95	

SUSACK#:
SUSACK# and SUSWARN# can be tied together if EC does not want to involve in handshake mechanism for the Deep Sleep state entry and exit.

APWROK:
For platform not supporting iAMT it can be connected to PWROK.

SUSPWRDNACK (PCH to EC):
This pin requires a pull-up to +3VSUS. Platforms are not expected to use this signal when the PCH's Deep S4/S5 feature is used.

SUSWARN# (PCH to EC):
This pin aserts low when PCH is planning to enter the DeepSx power state and remove Suspend power(using SLP_SUS#)

Entry Into Deep S4/S5
A combination of condition is required for entry into Deep S4/S5
All of the following must be met:
-Intel ME in Moff.
-AND either "a" or "b"(EDS R0.7v1 p.186).

ASW Power well stable for at least 1ms before platform logic asserts APWROK

Have Pull up Res. in CPU side

DSWVRMEN:
High -> DSW On-Die VR Enable
Low -> DSW On-Die VR disable

DPWROK:
This input is tied together with RSMRST# in platforms that do not support DeepSx

VCCDSW stable to DPWROK assertion is 10ms (min)

Delete R2222, R2228, U2201, R2230, R2233, C2201 and D2203, Deeper sleeper要拿掉

PMSYNCH is Low in C6/C7 states only

CHECK PULL-UP OR DOWN

reserve for powr noise

Power failure solution (S0-->G3,S5-->G3):

PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

09'MoW04:
Optional if ME FW is Ignition FW

D2207: Prevent EC drive hign, SUS_PWRGD sink low in S5-->G3.

For PU/PD

CRB:8.2K Ohm

DG:Pull-up 10K Ohm to 3.3V(Core)
CRB:NO Pull-up or down resistor

Strap high is GPIO mode

Internal PU 15K to 40K

Boundary Scan TP (PCH)

PM_RSMRST#_PCH	T2217
PM_PWROK_PCH	T2211
APWROK_R	T2215
PM_SYSPWROK_PCH	T2216

ASUSTeK COMPUTER INC.

Title : PCH_IBEX(3)_FDI,DMI,SYS PWR

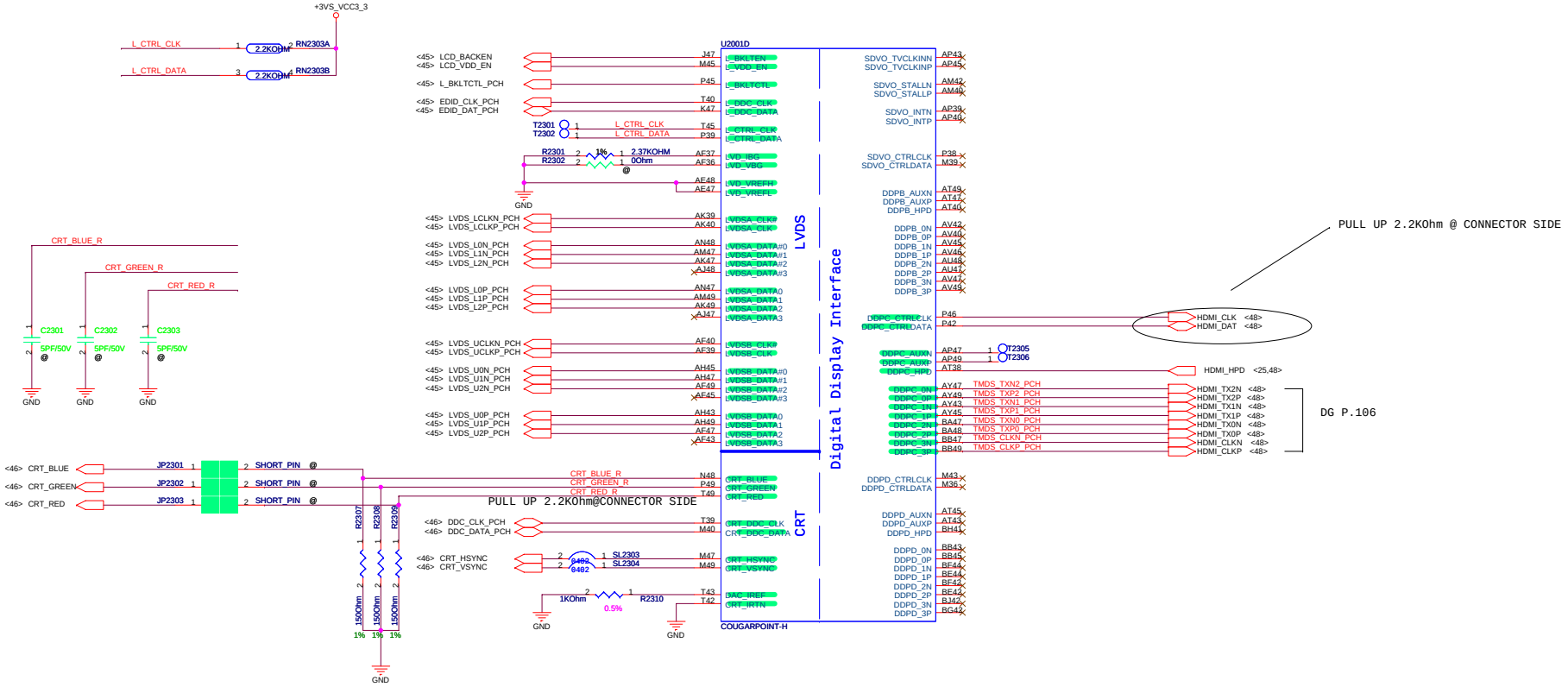
Engineer: Wish

Size: C | Project Name: N73Sv | Rev: 1.0

Date: Wednesday, October 13, 2010 | Sheet 22 of 95

PORT	STRAP	ENABLE PORT	DISABLE PORT
LVDS	L_DDC_DATA	Pull up to 3.3(V) with 2.2k Ohm	NC
PORT B	SDVO_CTRLDATA		
PORT C	DDPC_CTRLDATA		
PORT D	DDPD_CTRLDATA		

DG P.105,168



ASUSTeK COMPUTER INC.	Title : PCH_IBEX(4)_DP,LVDS,CRT		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 23 of 95		

Tacoma Pass(NVRAM) Disabling and termination guidelines(DG R0.7 p.322)
If the tacoma Pass interface is not used,
the interface signals, incuding NV_RCOMP,
can be left as No connects with few exceptions.
VccpNAND, NV_ALE, NV_CLE

PCB ID

+3VS_VCC3_3 +3VS_VCC3_3

R2501 10KOhm @ — PCB_ID0
R2502 10KOhm @ — PCB_ID1
R2503 10KOhm
R2504 10KOhm
GND GND

U2001E

RSVD: BG26 BJ26 BH25 BJ16 BG16 AH38 AH37 AK43 AK45 C18 N30 H3 AH12 AM4 AM5 Y13 K24 L24 AB46 AB45 B21 M20 AY16 BG46 BE28 BC30 BE32 BJ32 BC28 BE30 BF32 BG32 AV26 BB26 AU28 AY30 AU26 AY26 AV28 W30

NVRAM: AY7 AY7 AU3 BG4 AT10 BC8 AU2 AT4 AT3 AT1 AY3 AT5 AV3 AV1 BB1 BA3 BB5 BB3 BB7 BE8 BD4 BF6 AV5 AY1 AV10 AT8 AY5 BA2 AT12 BF3

NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3 NV_DQS0 NV_DQS1
NV_DQ0 / NV_IO0 … NV_DQ15 / NV_IO15
NV_ALE NV_CLE NV_RCOMP NV_RB# NV_RE#_WRB0 NV_RE#_WRB1 NV_WE#_CK0 NV_WE#_CK1

NV_CLE → T2401 (1)
NV_RCOMP → T2402 (1)
R2420 2 — 1 1KOhm
+V_NVRAM_VCCPNAND
R2418 2.2kOHM
T2403 (1)
H_SNB_INV# <3>

DMI & FDI Termination Voltage

NV_CLE	LOW : Set to Vss
	HIGH : Set to Vcc

CRB

USB: C24 A24 C25 B25 C26 A26 K28 H28 E28 D28 C28 A28 C29 B29 N28 M28 L30 K30 G30 E30 C30 A30 L32 K32 G32 E32 C32 A32

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USB_PN0 <33> USB_PP0 <33> USB_PN1 <33> USB_PP1 <33> USB_PN2 <66> USB_PP2 <66> USB_PN3 <69> USB_PP3 <69> USB_PN4 <54> USB_PP4 <54>
USB_PN8 <53> USB_PP8 <53> USB_PN9 <45> USB_PP9 <45>
USB_PN11 <42> USB_PP11 <42> USB_PN12 <61> USB_PP12 <61>

USB 0	USB Port (LAN BD)
USB 1	USB Port (LAN BD)
USB 2	USB Port
USB 3	USB 3.0 Port
USB 4	TV Tuner
USB 5	
USB 6	
USB 7	
USB 8	WiFi / WiMax
USB 9	Camera
USB 10	
USB 11	Card Reader
USB 12	Bluetooth
USB 13	

PCI: K40 K38 H38 G38 C46 C44 E40 D47 E42 F46 G42 G40 C42 D44 K10 C6 H49 H43 J48 K42 H40

PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD# *IRQA *IRQB *IRQC *IRQD
GPU_RST# STP_27M PCI_GNT1# DGPU_PWM_SELECT# STP_A16OVR PCI_INTE# PCB_ID0 PCB_ID1 PCI_PME# PLT_RST# CLKOUT_PCI0

REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54 GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55 *IRQE# / GPIO2 *IRQF# / GPIO3 *IRQG# / GPIO4 *IRQH# / GPIO5 *PME# *PLTRST# CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

<70> GPU_RST# <29> STP_27M <70> DGPU_PWR_EN# — 5V — 5V
T2408 (1)
<51> SATA_ODD_DA#
T2407 (1)
T2413 (1)
<21> CLK_PCI_FB <30> CLK_KBCPCI_PCH <44> CLK_DEBUG
R2428 22Ohm CLK_PCI_FB_R
R2429 39Ohm CLK_KBCPCI_PCH_R
R2430 22Ohm CLK_DEBUG_R

USB: C33 B33 A14 K20 B17 C16 L16 A16 D14 C14

USBRBIAS# USBRBIAS
USBRBIAS_PN — R2406 22.6Ohm 1% — GND
OC#0 OC#1 OC#2 OC#3 OC#4 OC#5 OC#6 OC#7
OC0# / GPIO39 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO44 OC6# / GPIO10 OC7# / GPIO14

COUGARPOINT-H

+3VSUS_ORG
OC#0 RP2403A 1 10KOhm 5 10
OC#7 RP2403B 2 10KOhm 5 10
OC#3 RP2403C 3 10KOhm 5 10
OC#5 RP2403D 4 10KOhm 5 10
OC#1 RP2403E 6 10KOhm 5 10
OC#2 RP2403F 7 10KOhm 5 10
OC#6 RP2403G 8 10KOhm 5 10
OC#4 RP2403H 9 10KOhm 5 10

+3VS_VCC3_3
PCI_INTA# RP2401A 1 10KOhm 5 10
PCI_INTB# RP2401B 2 10KOhm 5 10
PCI_INTC# RP2401C 3 10KOhm 5 10
RP2401D 4 10KOhm 5 10
SATA_ODD_DA# RP2401E 6 10KOhm 5 10
PCI_INTD# RP2401F 7 10KOhm 5 10
PCI_INTE# RP2401G 8 10KOhm 5 10
RP2401H 9 10KOhm 5 10
STP_27M R2427 10KOhm
SATA_ODD_DA# R2421 10KOhm @
DGPU_PWR_EN# R2422 10KOhm @
GPU_RST# R2423 10KOhm
STP_27M R2424 10KOhm @
GND

Boot BIOS Strap : GNT1#, SATA1GP

Boot BIOS Strap		
GNT1#(BBS1)	SATA1GP(BBS0)	Boot BIOS Location
0	1	Reserved
1	0	PCI
1	1	SPI (PCH)
0	0	LPC

Sampled on rising edge of PWROK.

+3VS_VCC3_3
Default PU 20K OHM
R2409 10KOhm R2410 10KOhm
<20> SATA1GP — R2411 1KOhm @
PCI_GNT1# — R2412 1KOhm @
GND

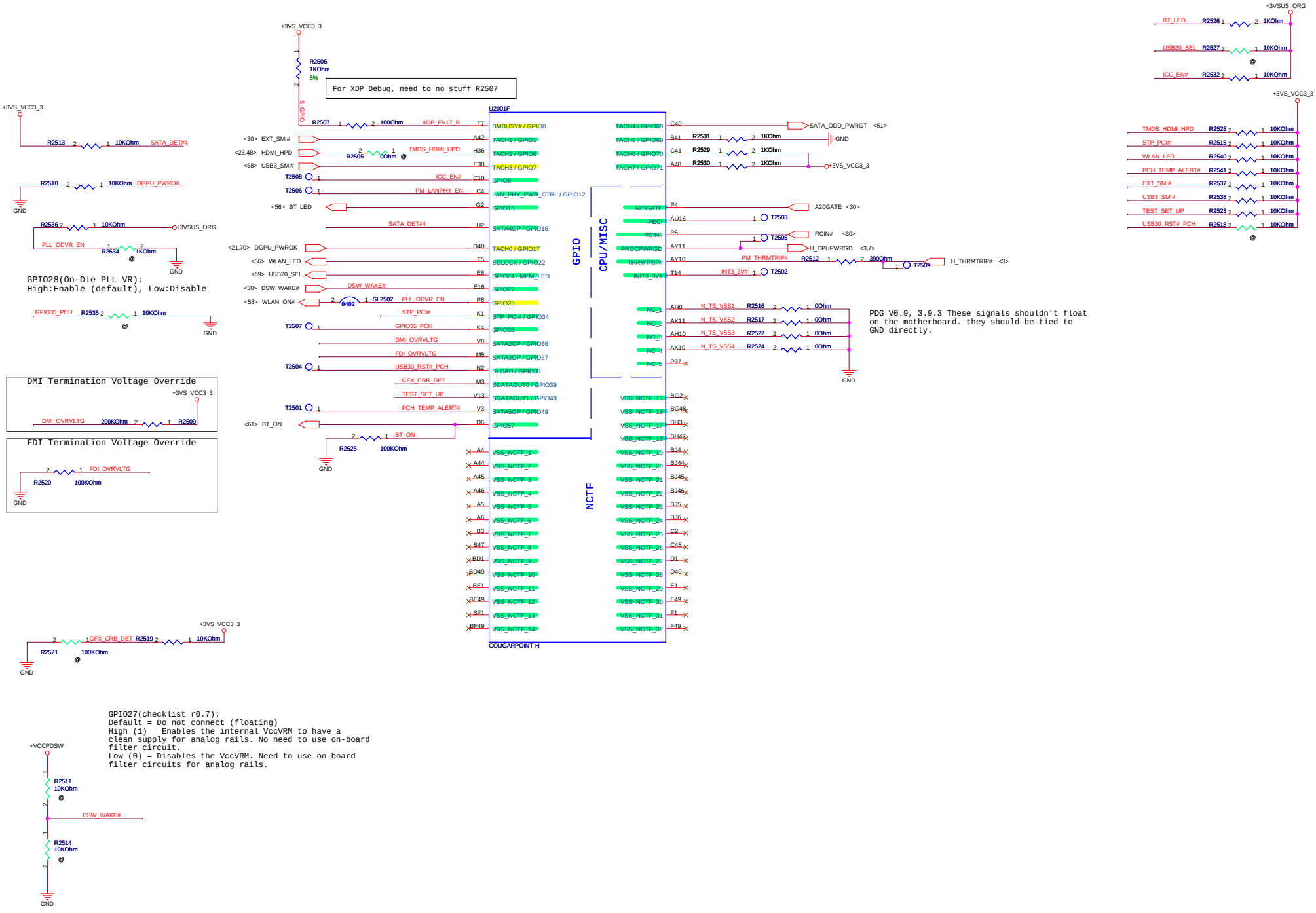
GNT3#: A16 swap override Strap/ Top-Block swap override jumper

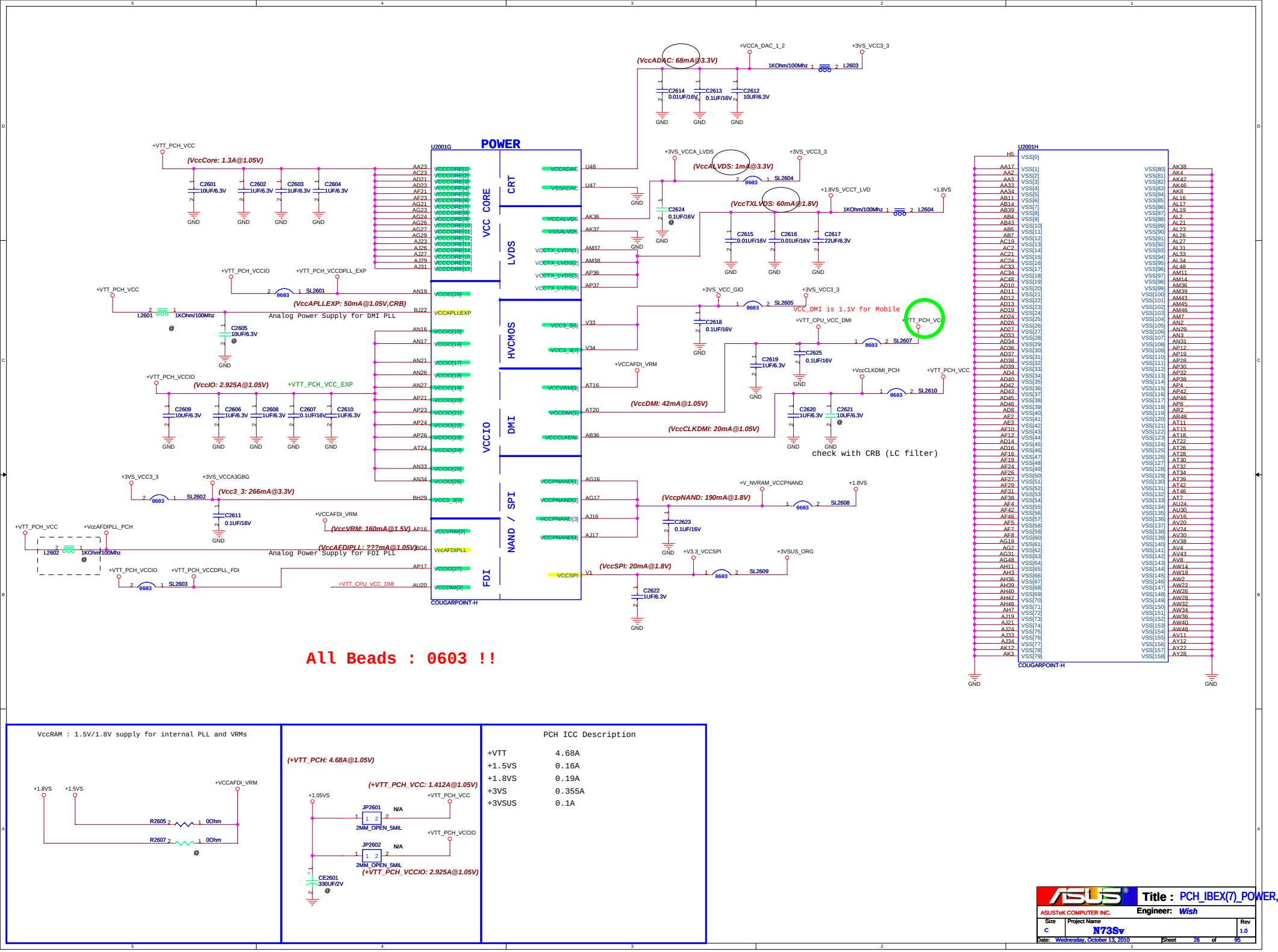
Low=Enabled A16 swap override/ Top-Block swap override
High=Default

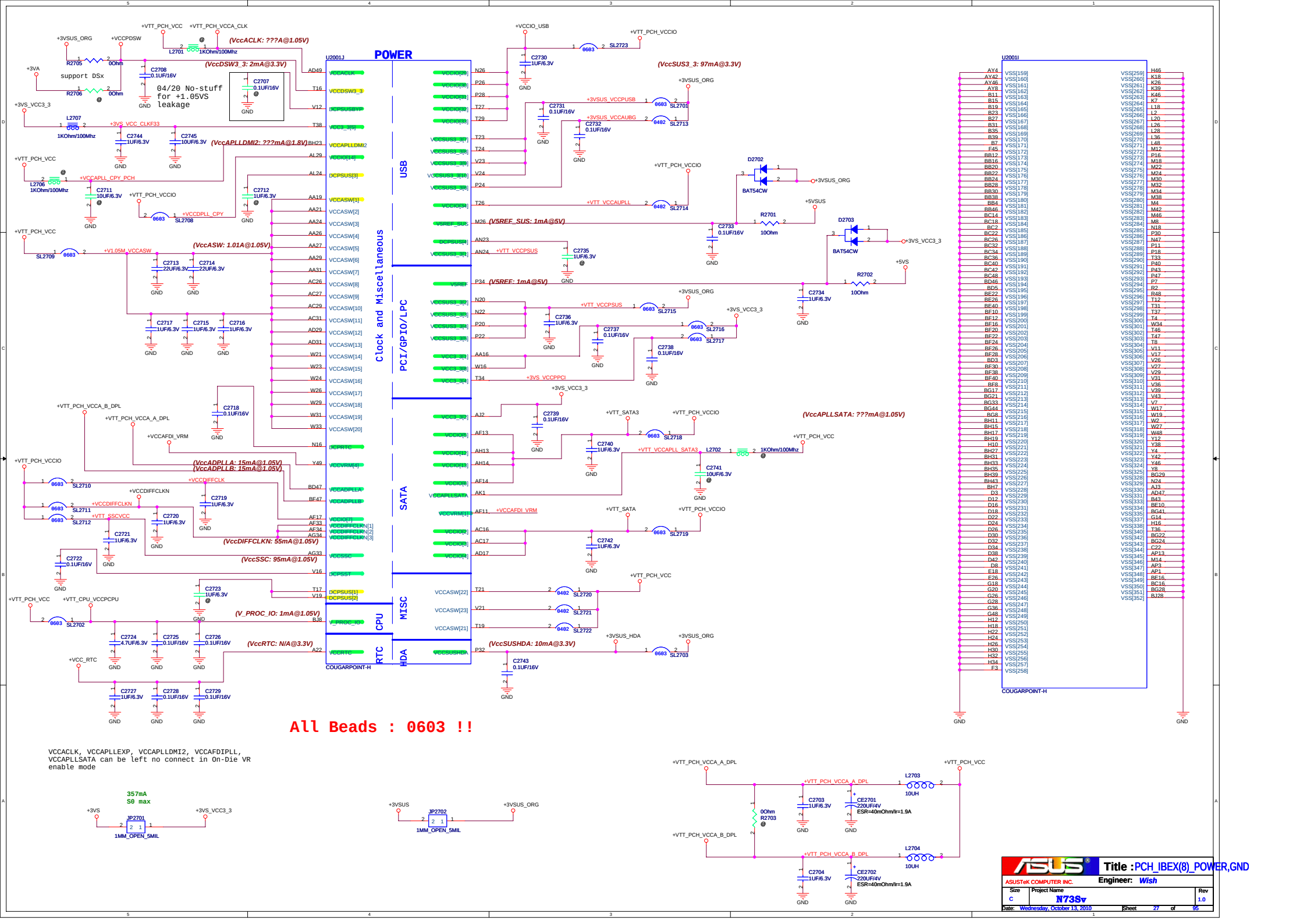
STP_A16OVR — R2413 1KOhm @ — GND

+3V
U2401 74LVC1G08GW (INB, INA, GND, VCC, OUTY)
<32> PLT_RST# — BUF_PLT_RST# <3,30,33,42,45,53,54,68,70>
R2414 0Ohm @
GND

Title : PCH_IBEX(5)_PCI,NVRAM,USB		
ASUSTeK COMPUTER INC.	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 24 of 95	


+3VS_VCC3_3
R2506 1KOhm 5%
For XDP Debug, need to no stuff R2507
U2001F
R2507 100Ohm XDP_FN17_R
BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
GPIO24 / MEM_LED
GPIO27
GPIO28
STP_PCI# / GPIO34
GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SATA5GP / GPIO49
GPIO57
GPIO
CPU/MISC
NCTF
COUGARPOINT-H
TACH4 / GPIO68
TACH5 / GPIO69
TACH6 / GPIO70
TACH7 / GPIO71
A20GATE
PECI
RCIN#
PROCPWRGD
THRMTRIP#
INIT3_3V#
SATA_ODD_PWRGT <51>
A20GATE <30>
RCIN# <30>
H_CPUPWRGD <3,7>
H_THRMTRIP# <3>
PM_THRMTRIP# R2512 390Ohm
INT3_3V# T2502
T2503
T2505
T2509
N_TS_VSS1 R2516 0Ohm
N_TS_VSS2 R2517 0Ohm
N_TS_VSS3 R2522 0Ohm
N_TS_VSS4 R2524 0Ohm
PDG V0.9, 3.9.3 These signals shouldn't float on the motherboard. they should be tied to GND directly.
+3VSUS_ORG
BT_LED R2526 1KOhm
USB20_SEL R2527 10KOhm
ICC_EN# R2532 10KOhm
TMDS_HDMI_HPD R2528 10KOhm
STP_PCI# R2515 10KOhm
WLAN_LED R2540 10KOhm
PCH_TEMP_ALERT# R2541 10KOhm
EXT_SMI# R2537 10KOhm
USB3_SMI# R2538 10KOhm
TEST_SET_UP R2523 10KOhm
USB30_RST#_PCH R2518 10KOhm
R2513 10KOhm SATA_DET#4
R2510 10KOhm DGPU_PWROK
R2536 10KOhm
PLL_ODVR_EN R2534 1KOhm
GPIO28(On-Die PLL VR):
High:Enable (default), Low:Disable
GPIO35_PCH R2535 10KOhm
DMI Termination Voltage Override
DMI_OVRVLTG 200KOhm R2509
FDI Termination Voltage Override
FDI_OVRVLTG R2520 100KOhm
GFX_CRB_DET R2519 10KOhm
R2521 100KOhm
GPIO27(checklist r0.7):
Default = Do not connect (floating)
High (1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.
Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.
+VCCPDSW
R2511 10KOhm
DSW_WAKE#
R2514 10KOhm
GND
Title : PCH_IBEX(6)CPU,GPIO,MISC
ASUSTeK COMPUTER INC.
Engineer: Wish
Size C
Project Name N73Sv
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 25 of 95


POWER
U2001G
VCC CORE
CRT
LVDS
HVCMOS
DMI
VCCIO
SPI
NAND
FDI
COUGARPOINT-H
U2001H
(VccADAC: 68mA@3.3V)
(VccCore: 1.3A@1.05V)
(VccALVDS: 1mA@3.3V)
(VccTXLVDS: 60mA@1.8V)
(VccAPLLEXP: 50mA@1.05V,CRB)
Analog Power Supply for DMI PLL
(VccIO: 2.925A@1.05V)
(Vcc3_3: 266mA@3.3V)
(VccVRM: 160mA@1.5V)
(VccAFDIPLL: ???mA@1.05V)
Analog Power Supply for FDI PLL
(VccDMI: 42mA@1.05V)
(VccCLKDMI: 20mA@1.05V)
(VccNAND: 190mA@1.8V)
(VccSPI: 20mA@1.8V)
VCC_DMI is 1.1V for Mobile
check with CRB (LC filter)
All Beads : 0603 !!
VccRAM : 1.5V/1.8V supply for internal PLL and VRMs
(+VTT_PCH: 4.68A@1.05V)
(+VTT_PCH_VCC: 1.412A@1.05V)
(+VTT_PCH_VCCIO: 2.925A@1.05V)
PCH ICC Description
+VTT 4.68A
+1.5VS 0.16A
+1.8VS 0.19A
+3VS 0.355A
+3VSUS 0.1A
Title : PCH_IBEX(7)_POWER,GND
ASUSTeK COMPUTER INC.
Engineer: Wish
Size C
Project Name N73Sv
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 26 of 95


POWER
U2001J
COUGARPOINT-H
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
U2001I
COUGARPOINT-H
(VccACLK: ???A@1.05V)
(VccDSW3_3: 2mA@3.3V)
(VccAPLLDMI2: ???mA@1.8V)
(VccASW: 1.01A@1.05V)
(VccADPLLA: 15mA@1.05V)
(VccADPLLB: 15mA@1.05V)
(VccDIFFCLKN: 55mA@1.05V)
(VccSSC: 95mA@1.05V)
(V_PROC_IO: 1mA@1.05V)
(VccRTC: N/A@3.3V)
(VccSUS3_3: 97mA@3.3V)
(V5REF_SUS: 1mA@5V)
(V5REF: 1mA@5V)
(VccAPLLSATA: ???mA@1.05V)
(VccSUSHDA: 10mA@3.3V)
04/20 No-stuff for +1.05VS leakage
support DSx
All Beads : 0603 !!
VCCACLK, VCCAPLLEXP, VCCAPLLDMI2, VCCAFDIPLL, VCCAPLLSATA can be left no connect in On-Die VR enable mode
357mA
S0 max
1MM_OPEN_5MIL
Title :PCH_IBEX(8)_POWER,GND
ASUSTeK COMPUTER INC.
Engineer: Wish
Size C
Project Name N73Sv
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 27 of 95

PCH SPI ROM

Reserve +3VA

+3VA +3VSUS_ORG +3VM_SPI

R2834 1 2 0Ohm
R2835 1 2 0Ohm @

D2801
BAT54CW

R2847 2 1 0Ohm @

Put near U2801

SPI FLASH TOOL CON

+3VM_SPI

J2802

SPI_CS#_CON
SPI_SO_CON
SPI_CLK_CON
SPI_SI_CON

HEADER_2X4P_K8

12G06100008K

SPI_CLK_CON

EC2801 0.1UF/16V @

SLN2801B SLN2801A SLN2802B SLN2802A

+3VM_SPI

T2807

T2801 T2802

<20> SPI_CS#0
<20> SPI_SO

R2837 33Ohm
R2838 33Ohm

R2833 3.3KOhm
R2831 3.3KOhm
C2802 0.1UF/16V

T2806

U2801

CE# VDD
SO HOLD#
WP# SCK
VSS SI

+3VM_SPI_WP08
+3VM_SPI_00
SPICLK0
SPISI0

SST25VF032B
(32Mb)

R2866 0Ohm
R2869 0Ohm
T2805
T2808

R2867 0Ohm
R2868 0Ohm

R2840 33Ohm
R2841 33Ohm

T2803
T2804

SPI_CLK <20>
SPI_SI <20>

<30> EC_SCE#_PCH
<30> EC_SO_PCH

EC_SCK_PCH <30>
EC_SI_PCH <30>

PCH

+3VS +12VS

4.7KOhm R2802
4.7KOhm R2803

<21> SCL_3A
<21> SDA_3A

Q2801A UM6K1N
Q2801B UM6K1N

SMB_CLK_S <14,16,17,29,53>
SMB_DAT_S <14,16,17,29,53>

EC

<30> SMB1_CLK
<30> SMB1_DAT

+12VSUS

Q2802A UM6K1N
Q2802B UM6K1N

PCH

SML1_CLK <21>
SML1_DAT <21>

+12VS +3VS

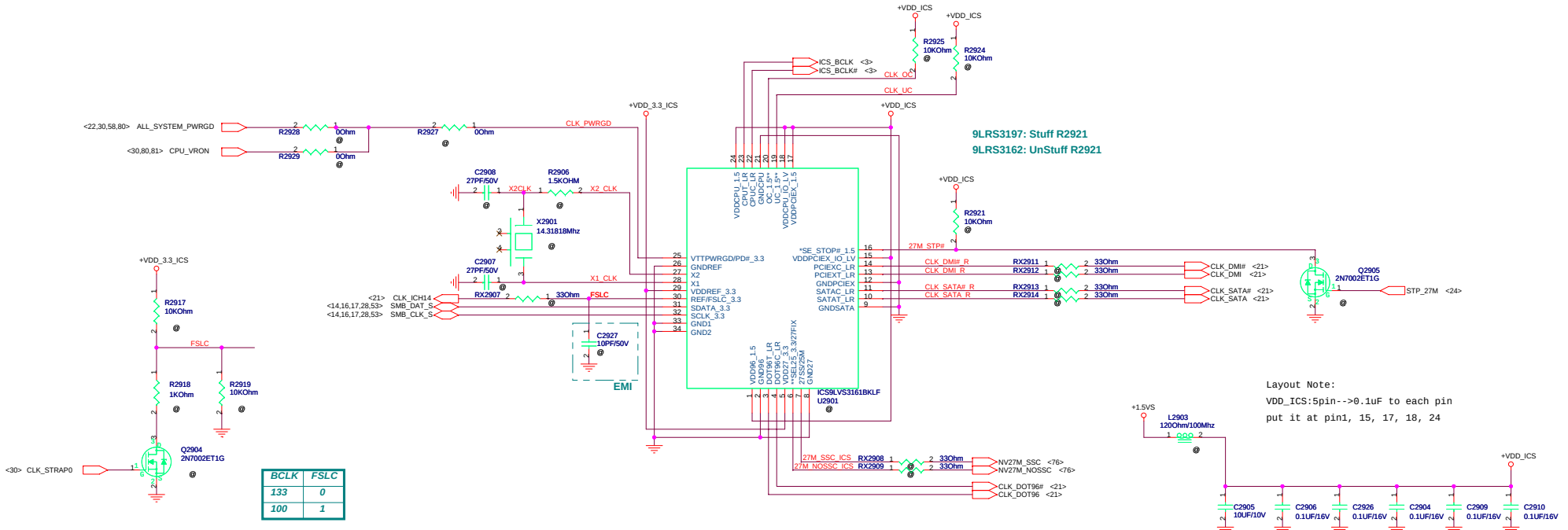
4.7KOhm R2809
4.7KOhm R2808

Q2804A UM6K1N
Q2804B UM6K1N

SMB1_CLK_S <50,75,88>
SMB1_DAT_S <50,75,88>

CPU,Thermal

ASUSTeK COMPUTER INC.	Title : PCH_SPI ROM,OTH	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 28 of 95	



BCLK	FSLC
133	0
100	1

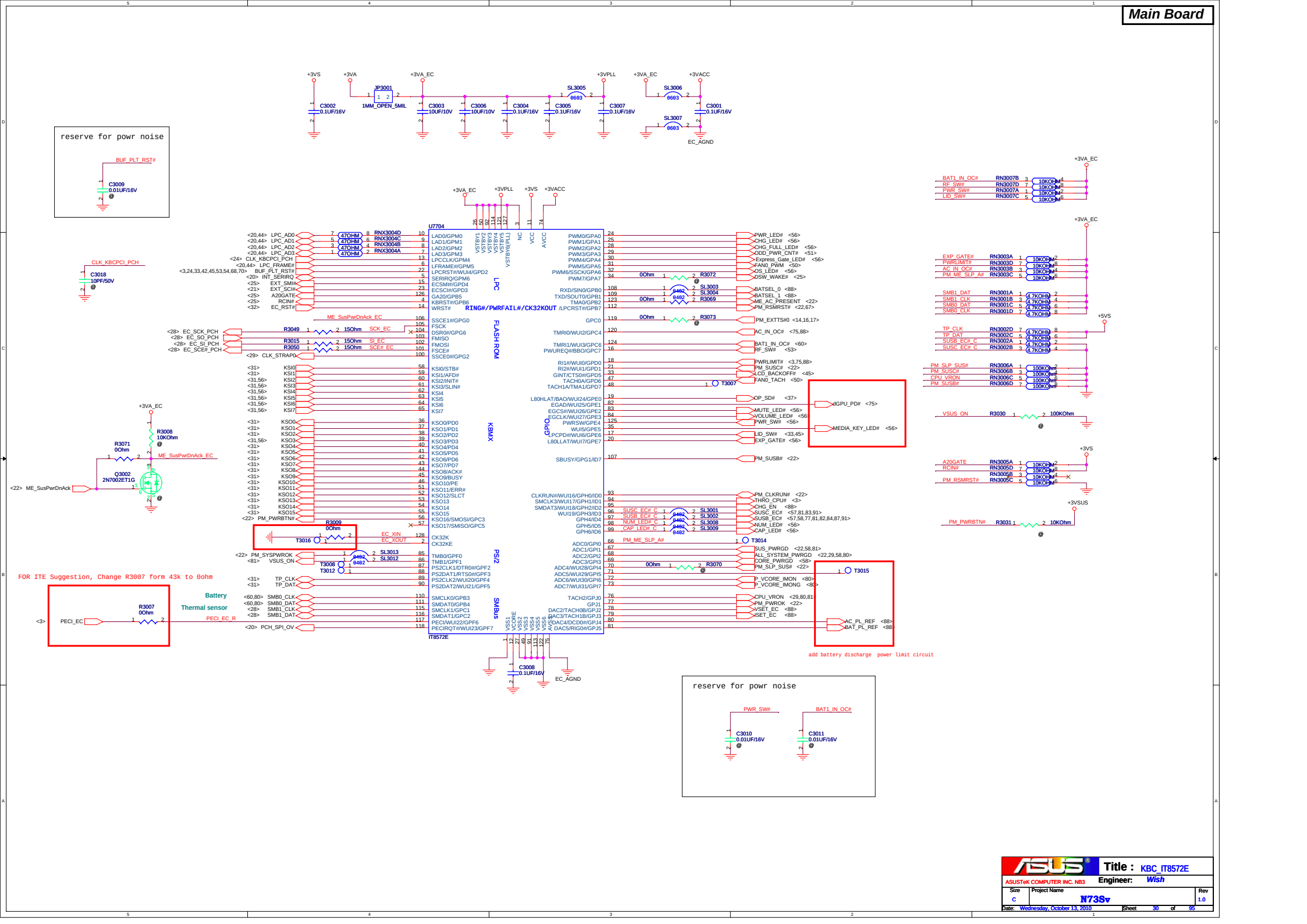
Layout Note:
VDD_ICS:5pin-->0.1uF to each pin
put it at pin1, 15, 17, 18, 24

Total Power Consumption 104mW

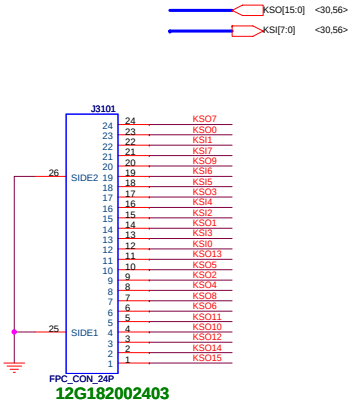
Layout Note:
27M_NOSSC length must short
27M_NOSSC=L, 27M_SSC=27M
27M_NOSSC=H, 27M_SSC=25M

Layout Note:
VDD_3.3_ICS:5pin-->0.1uF to each pin
put it at pin5,29

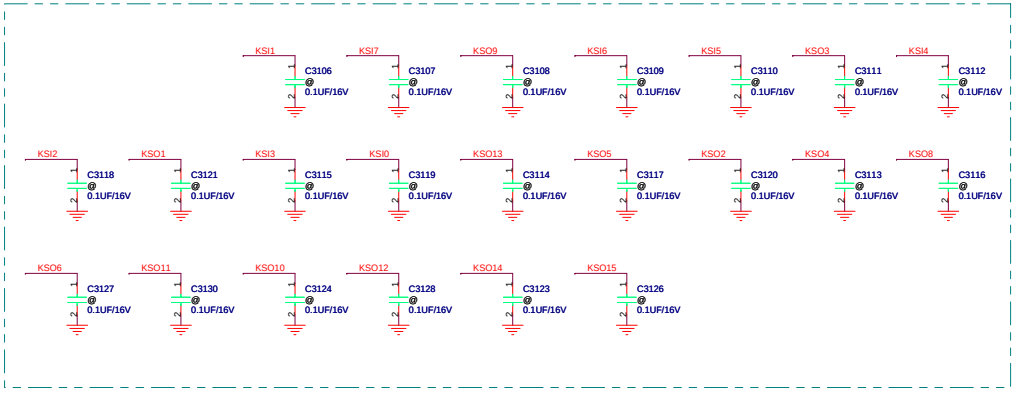
ASUSTeK COMPUTER INC. NB3	Title : CLK_ICS9LRS3197		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 29 of 95		


reserve for powr noise
BUF_PLT_RST#
C3009 0.01UF/16V @
+3VS
+3VA
+3VA_EC
+3VPLL
+3VACC
JP3001 1MM_OPEN_5MIL
C3002 0.1UF/16V
C3003 10UF/10V
C3006 10UF/10V
C3004 0.1UF/16V
C3005 0.1UF/16V
C3007 0.1UF/16V
C3001 0.1UF/16V
SL3005 0603
SL3006 0603
SL3007 0603
EC_AGND
U7704
IT8572E
LPC
FLASH ROM
KBMX
PS/2
SMBus
GPIO
RING#/PWRFAIL#/CK32KOUT
/LPCRST#/GPB7
CLK_KBCPCI_PCH
C3018 10PF/50V @
R3049 15Ohm SCK_EC
R3015 15Ohm SI_EC
R3050 15Ohm SCE#_EC
ME_SusPwrDnAck_EC
R3008 10KOhm @
R3071 0Ohm
Q3002 2N7002ET1G
R3009 0Ohm
T3016
EC_XIN
EC_XOUT
SL3013 0402
SL3012 0402
T3008
T3012
R3007 0Ohm
PECI_EC_R
Battery
Thermal sensor
FOR ITE Suggestion, Change R3007 form 43k to 0ohm
R3073 0Ohm
R3069 0Ohm
R3072 0Ohm
R3070 0Ohm
SL3003 0402
SL3004 0402
SL3001 0402
SL3002 0402
SL3008 0402
SL3009 0402
T3007
T3014
T3015
dGPU_PD# <75>
MEDIA_KEY_LED# <56>
add battery discharge power limit circuit
C3008 0.01UF/16V
reserve for powr noise
C3010 0.01UF/16V @
C3011 0.01UF/16V @
PWR_SW#
BAT1_IN_OC#
RN3007B 10KOHM
RN3007D 10KOHM
RN3007A 10KOHM
RN3007C 10KOHM
RN3003A 10KOHM
RN3003D 10KOHM
RN3003B 10KOHM
RN3003C 10KOHM
RN3001A 4.7KOHM
RN3001B 4.7KOHM
RN3001C 4.7KOHM
RN3001D 4.7KOHM
RN3002D 4.7KOHM
RN3002C 4.7KOHM
RN3002A 4.7KOHM
RN3002B 4.7KOHM
RN3006A 100KOhm
RN3006B 100KOhm
RN3006C 100KOhm
RN3006D 100KOhm
R3030 100KOhm @
RN3005A 10KOHM
RN3005D 10KOHM
RN3005B 10KOHM
RN3005C 10KOHM
R3031 10KOhm @
+5VS
+3VSUS
ASUSTeK COMPUTER INC. NB3
Title : KBC_IT8572E
Engineer: Wish
Size C
Project Name N73Sv
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 30 of 95

Keyboard Connector

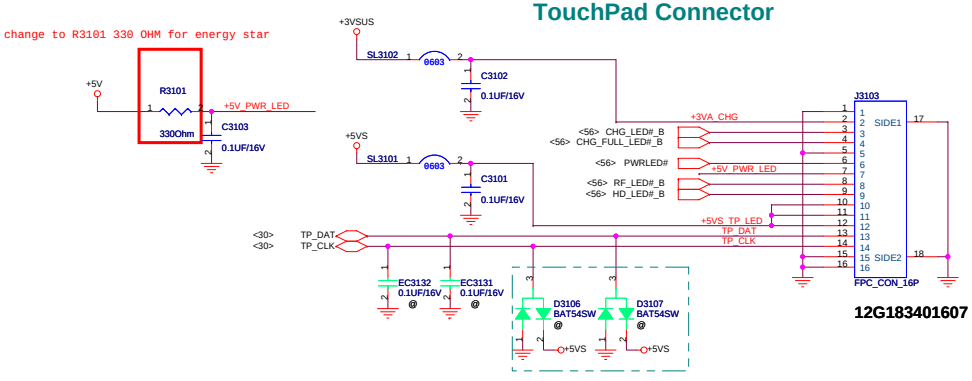


12G182002403



Reserved for EMI

TouchPad Connector

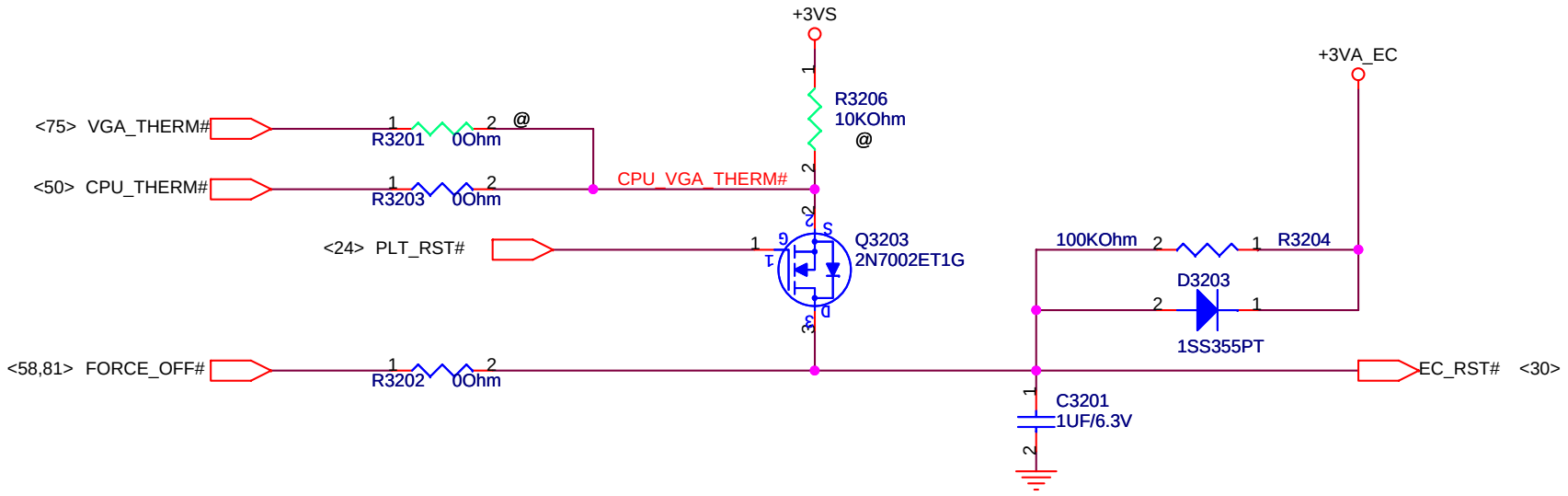


12G183401607

Reserved for EMI

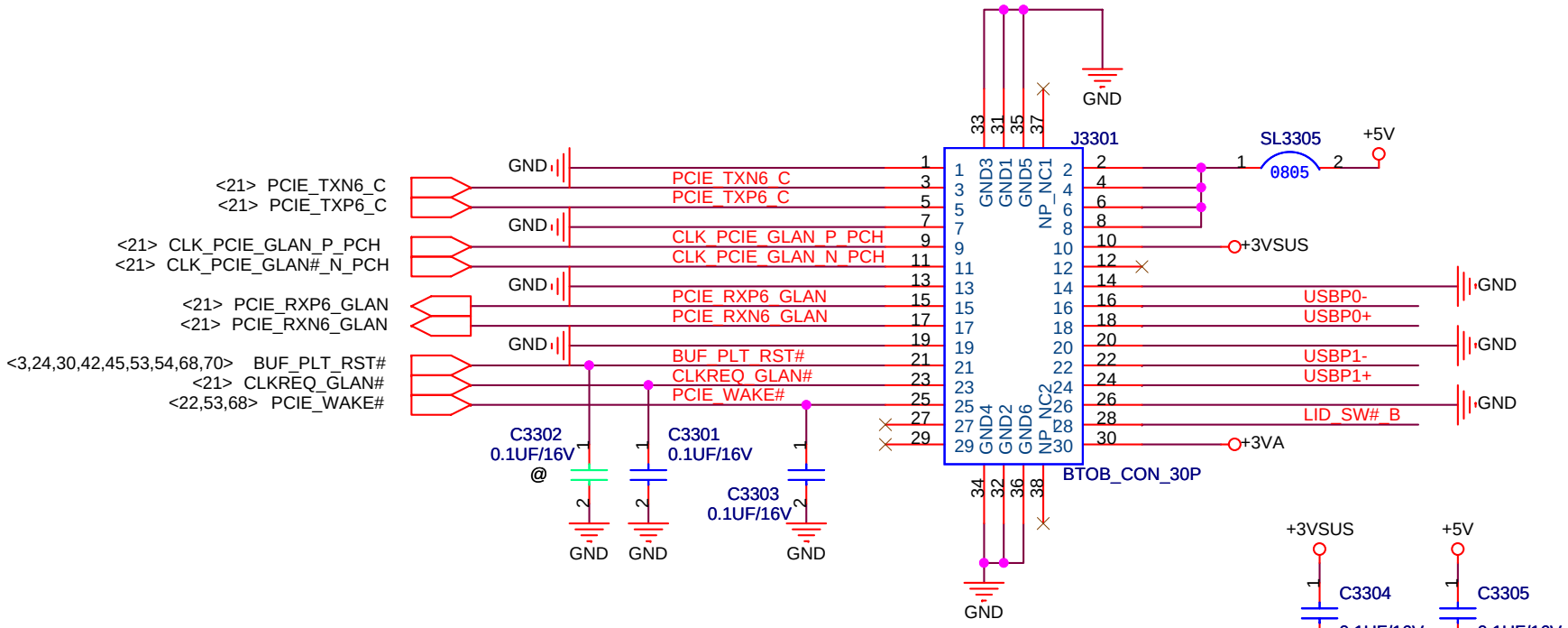
ASUSTeK COMPUTER INC. NB3	Title : KBC_KB & TP	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 31 of 95	

Main Board

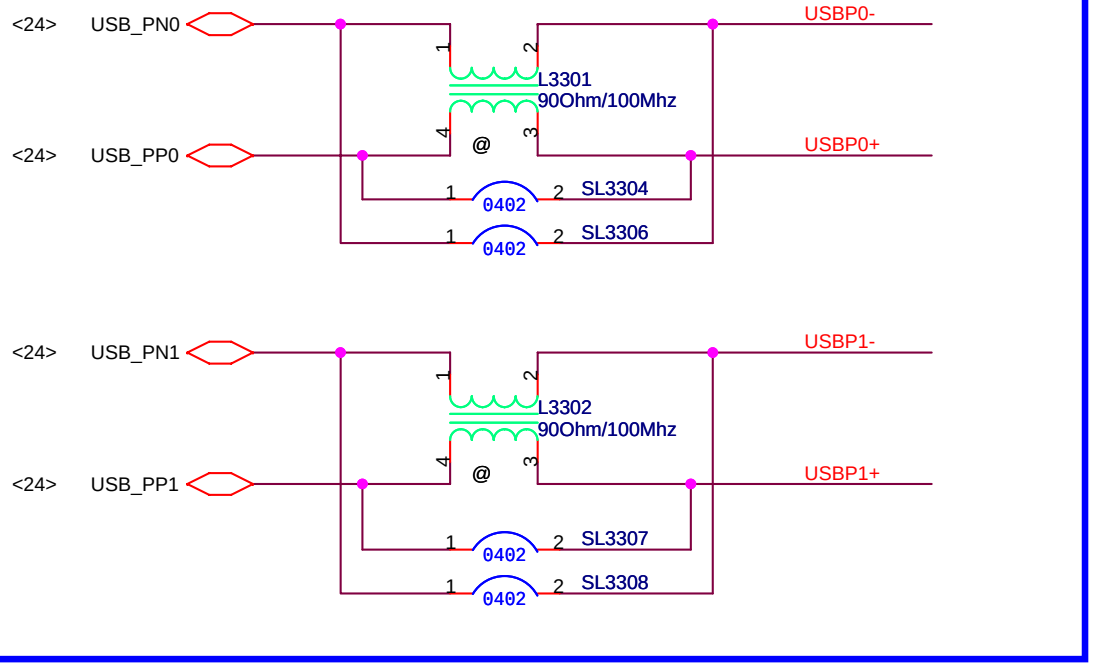


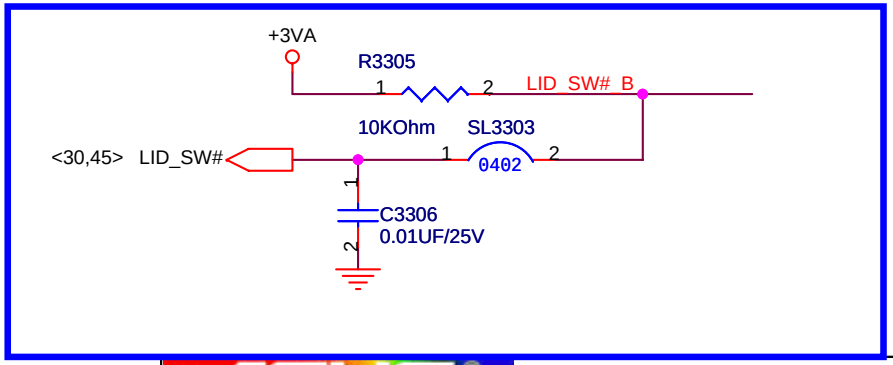
Check it! ITE說C3201可以不用加

ASUSTeK COMPUTER INC. NB3	Title : RST_Reset Circuit	
	Engineer: Wish	
Size: A	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 32 of 95	



EMI RESERVE
recommand stuff





ASUSTeK COMPUTER INC. NB3	Title : LAN_AR8131	
	Engineer: Wish	
Size: A	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 33 of 95	

Main Board

Title : LAN_RJ45 Conn.

ASUSTeK COMPUTER INC. NB3

Engineer: Wish

Size	Project Name	Rev
B	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 34 of 95

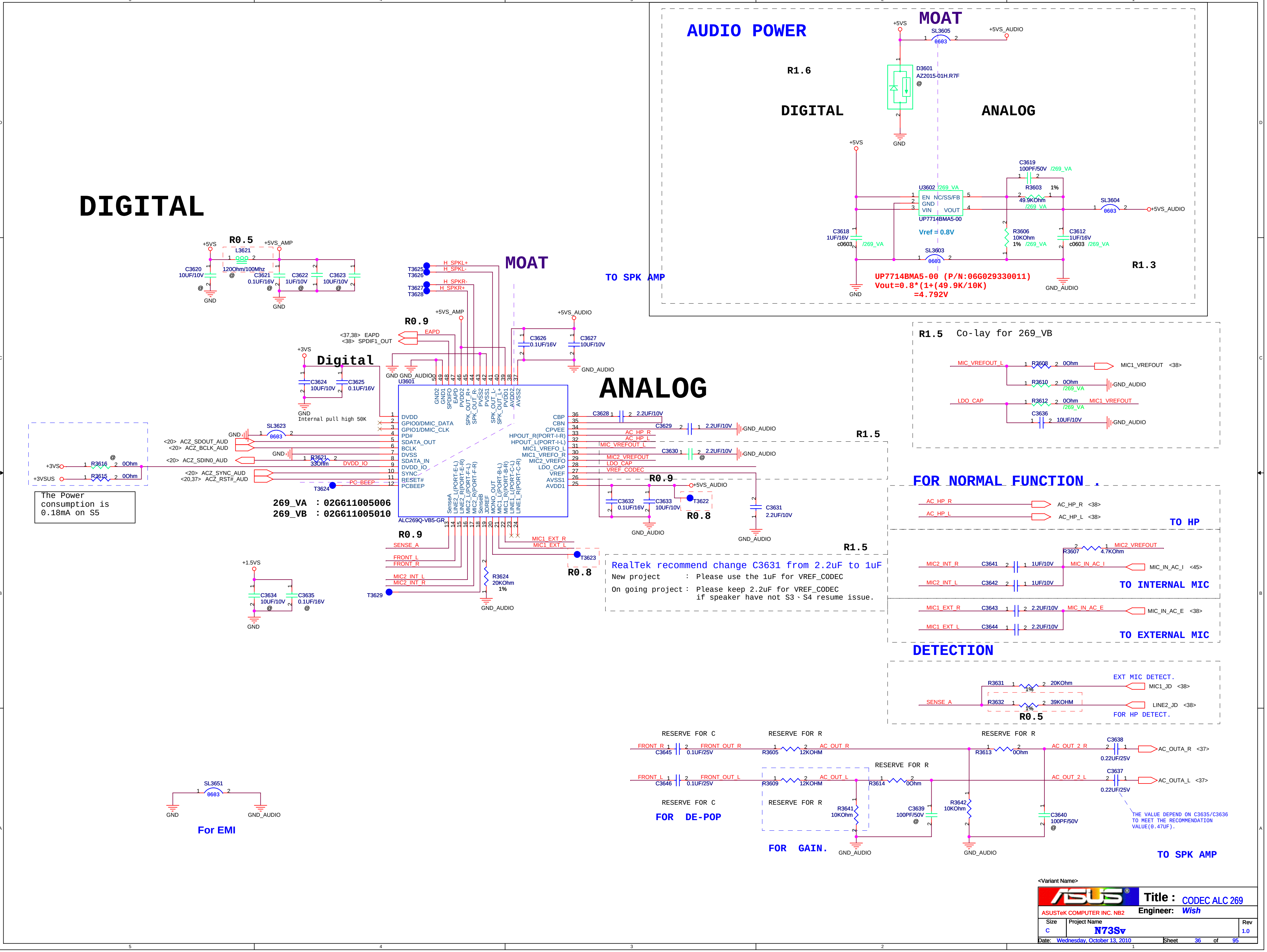
ASUSTeK COMPUTER INC. NB6

Title : ****

Engineer: Wish

Size	Project Name	Rev
Custom	N73Sv	1.0

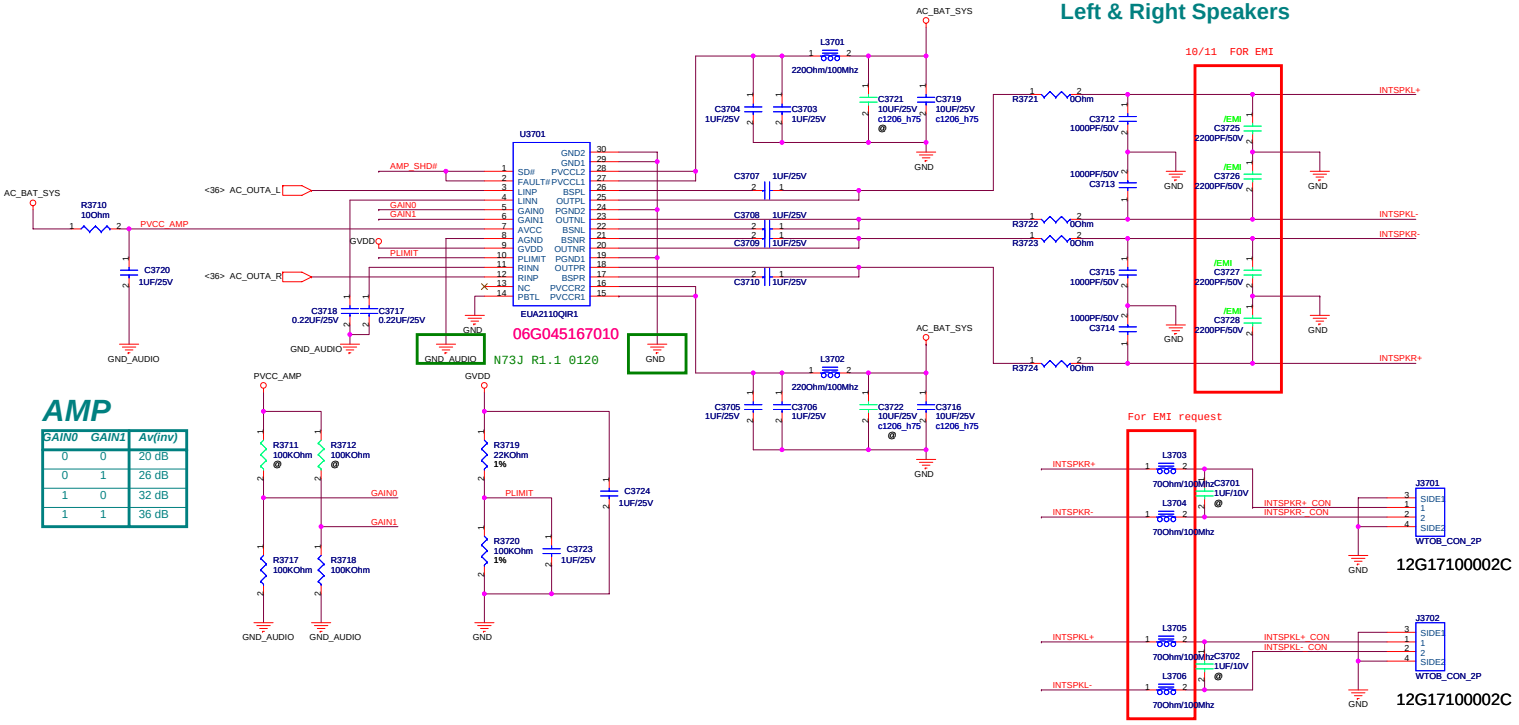
Date: Wednesday, October 13, 2010 Sheet 35 of 95



AUDIO POWER
MOAT
R1.6
DIGITAL
ANALOG
D3601 AZ2015-01H.R7F
SL3605 0603
+5VS
+5VS_AUDIO
GND
U3602 UP7714BMA5-00
EN NC/SS/FB
GND
VIN VOUT
Vref = 0.8V
C3619 100PF/50V /269_VA
R3603 1% 49.9KOhm /269_VA
R3606 10KOhm 1% /269_VA
C3612 1UF/16V c0603 /269_VA
C3618 1UF/16V c0603 /269_VA
SL3603 0603
SL3604 0603
GND_AUDIO
R1.3
UP7714BMA5-00 (P/N:06G029330011)
Vout=0.8*(1+(49.9K/10K)
=4.792V
DIGITAL
R0.5
L3621 120Ohm/100Mhz
C3620 10UF/10V
C3621 0.1UF/16V
C3622 1UF/10V
C3623 10UF/10V
+5VS_AMP
MOAT
TO SPK AMP
H_SPKL+
H_SPKL-
H_SPKR-
H_SPKR+
T3625 T3626 T3627 T3628
R0.9
EAPD
<37,38> EAPD
<38> SPDIF1_OUT
Digital
+3VS
C3624 10UF/10V
C3625 0.1UF/16V
Internal pull high 50K
C3626 0.1UF/16V
C3627 10UF/10V
U3601
ALC269Q-VB5-GR
ANALOG
DVDD
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD#
SDATA_OUT
BCLK
DVSS
SDATA_IN
DVDD_IO
SYNC
RESET#
PCBEEP
CBP
CBN
CPVEE
HPOUT_R(PORT-I-R)
HPOUT_L(PORT-I-L)
MIC1_VREFO_L
MIC1_VREFO_R
MIC2_VREFO
LDO_CAP
VREF
AVSS1
AVDD1
SL3623 0603
<20> ACZ_SDOUT_AUD
<20> ACZ_BCLK_AUD
<20> ACZ_SDIN0_AUD
R3621 33Ohm
<20> ACZ_SYNC_AUD
<20,37> ACZ_RST#_AUD
PC_BEEP
T3624
+3VS
+3VSUS
R3616 0Ohm
R3615 0Ohm
The Power consumption is 0.18mA on S5
269_VA : 02G611005006
269_VB : 02G611005010
C3628 2.2UF/10V
C3629 2.2UF/10V
C3630 2.2UF/10V
AC_HP_R
AC_HP_L
MIC_VREFOUT_L
MIC2_VREFOUT
LDO_CAP
VREF_CODEC
R1.5
R0.9
C3632 0.1UF/16V
C3633 10UF/10V
T3622
R0.8
C3631 2.2UF/10V
R0.9
SENSE_A
FRONT_L
FRONT_R
MIC2_INT_L
MIC2_INT_R
MIC1_EXT_R
MIC1_EXT_L
T3623
R0.8
R3624 20KOhm 1%
T3629
+1.5VS
C3634 10UF/10V
C3635 0.1UF/16V
R1.5
RealTek recommend change C3631 from 2.2uF to 1uF
New project : Please use the 1uF for VREF_CODEC
On going project : Please keep 2.2uF for VREF_CODEC if speaker have not S3、S4 resume issue.
R1.5 Co-lay for 269_VB
MIC_VREFOUT_L
R3608 0Ohm
MIC1_VREFOUT <38>
R3610 0Ohm /269_VA
LDO_CAP
R3612 0Ohm /269_VA
MIC1_VREFOUT
C3636 10UF/10V
FOR NORMAL FUNCTION .
AC_HP_R <38>
AC_HP_L <38>
TO HP
R3607 4.7KOhm
MIC2_VREFOUT
C3641 1UF/10V
C3642 1UF/10V
MIC_IN_AC_I <45>
TO INTERNAL MIC
C3643 2.2UF/10V
C3644 2.2UF/10V
MIC_IN_AC_E <38>
TO EXTERNAL MIC
DETECTION
EXT MIC DETECT.
R3631 20KOhm 1%
MIC1_JD <38>
R3632 39KOHM 1%
LINE2_JD <38>
FOR HP DETECT.
R0.5
RESERVE FOR C
RESERVE FOR R
C3645 0.1UF/25V
FRONT_OUT_R
R3605 12KOHM
AC_OUT_R
R3613 0Ohm
AC_OUT_2_R
C3638 0.22UF/25V
AC_OUTA_R <37>
C3646 0.1UF/25V
FRONT_OUT_L
R3609 12KOHM
AC_OUT_L
R3614 0Ohm
AC_OUT_2_L
C3637 0.22UF/25V
AC_OUTA_L <37>
R3641 10KOhm
C3639 100PF/50V
R3642 10KOhm
C3640 100PF/50V
FOR DE-POP
FOR GAIN.
THE VALUE DEPEND ON C3635/C3636 TO MEET THE RECOMMENDATION VALUE(0.47UF).
TO SPK AMP
SL3651 0603
For EMI
<Variant Name>
Title : CODEC ALC 269
ASUSTeK COMPUTER INC. NB2
Engineer: Wish
Size C
Project Name N73Sv
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 36 of 95

Main Board

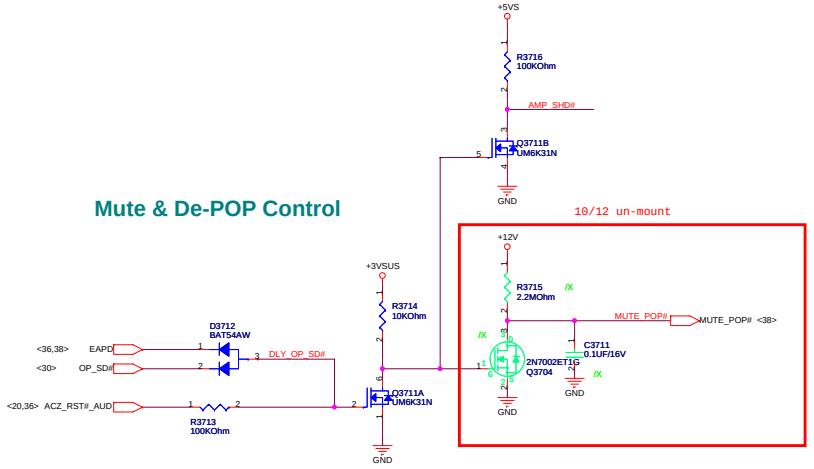
Left & Right Speakers

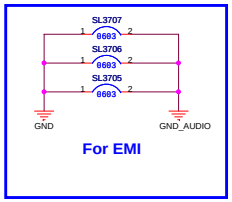


AMP

GAIN0	GAIN1	Av(inv)
0	0	20 dB
0	1	26 dB
1	0	32 dB
1	1	36 dB

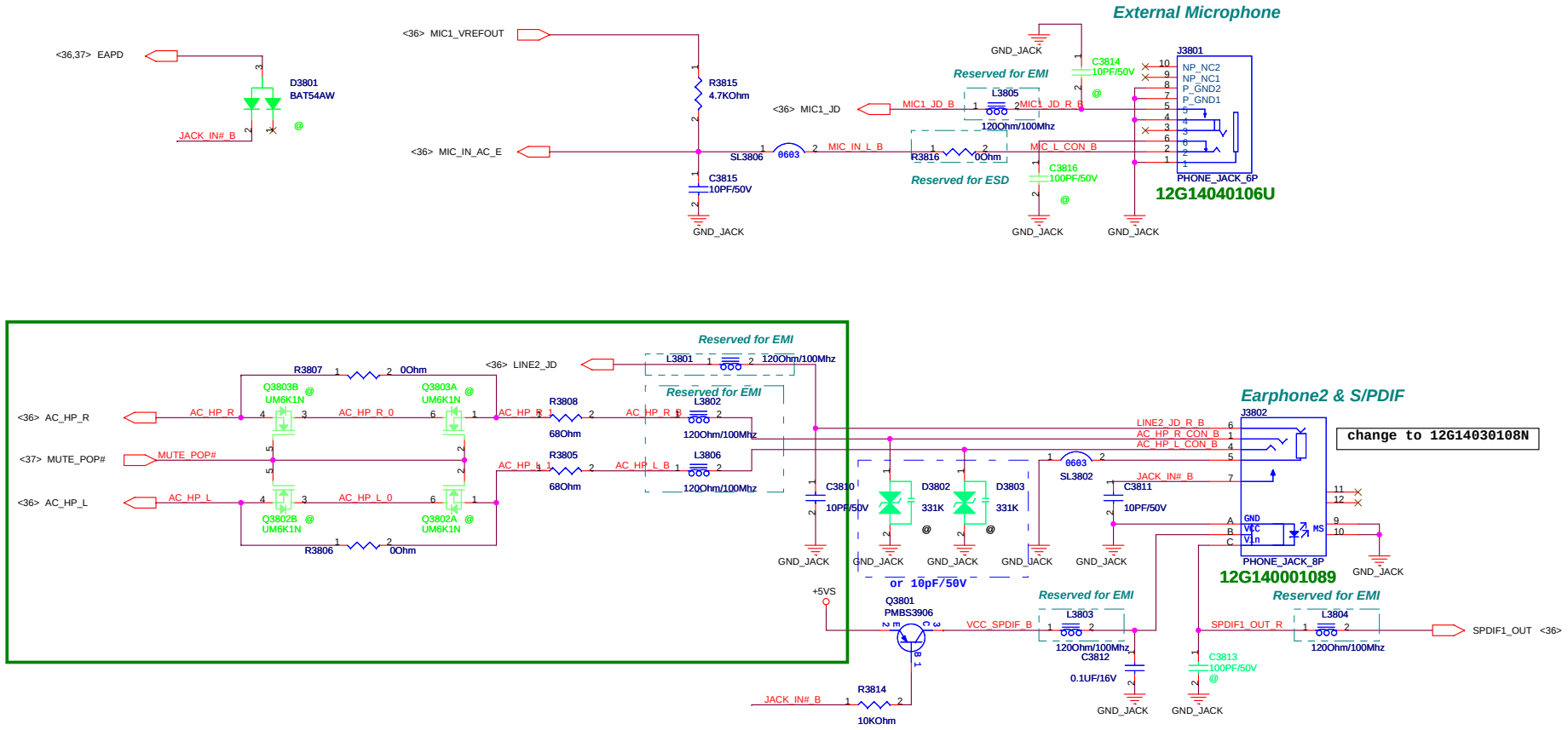
Mute & De-POP Control



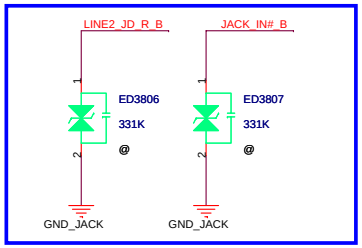


Title :	AUD_SPKR,Woofer,Mic
ASUSTeK COMPUTER INC. NB3	Engineer: Wish
Size: Custom	Project Name: N73Sv
Rev: 1.0	
Date: Wednesday, October 13, 2010	Sheet 37 of 95

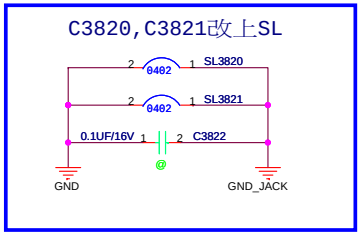
AUDIO



For EMI Reserve



For EMI Reserve



<Variant Name>

ASUSTeK COMPUTER INC. NB2	Title : MIC&LINEIN	
	Engineer: Wish	
Size: Custom	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 38 of 95	

Title :	AUD_****
ASUSTeK COMPUTER INC. NB3	Engineer: Wish
Size: A	Project Name: N73Sv
Rev: 1.0	
Date: Wednesday, October 13, 2010	Sheet 39 of 95

Title :	Audio IO Conn.
ASUSTeK COMPUTER INC	Engineer: Wish
Size: A	Project Name: N73Sv
Rev: 1.0	
Date: Wednesday, October 13, 2010	Sheet 40 of 95

Title :	Audio IO Conn.
ASUSTeK COMPUTER INC	Engineer: Wish
Size: A	Project Name: N73Sv
Rev: 1.0	
Date: Wednesday, October 13, 2010	Sheet 41 of 95

1009 reserve R4218 (+3VS) for energy star

Pin2 has internal pu 75K to +3V.

Reserve for Eye Diagram

Ref Schematic:
+3V_CR: 4.7Ux2
0.1Ux1
+1.8V: 2.2Ux1
+3V_CARD:4.7Ux1

Close to chip

SD write protect
1:decided by SDWP(Default)
0:letting SD always write-enable

Clock source select
1:For 48mMHz (Default)
0:For 12MHz

power saving mode
1:For enable (Default)
0:For disable

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

IC side

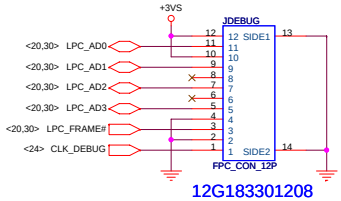
CON side

ASUSTeK COMPUTER INC. NB3	Title : AU6433	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 42 of 95	

Main Board

ASUSTeK COMPUTER INC. NB3	Title : CB_NewCard	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 43 of 95	

LPC Debug Port

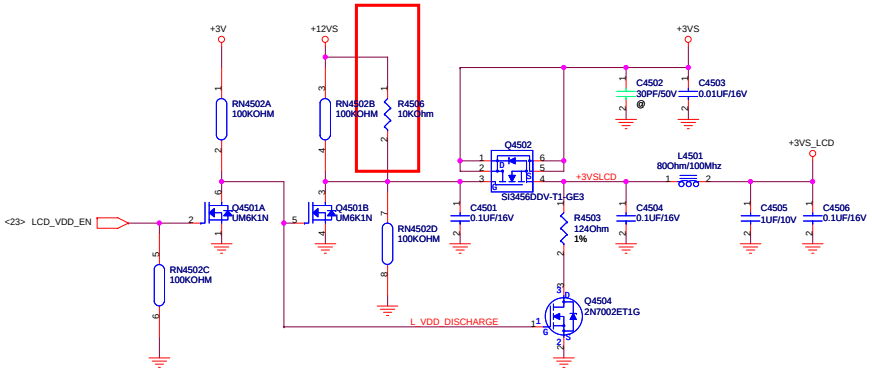


12G183301208

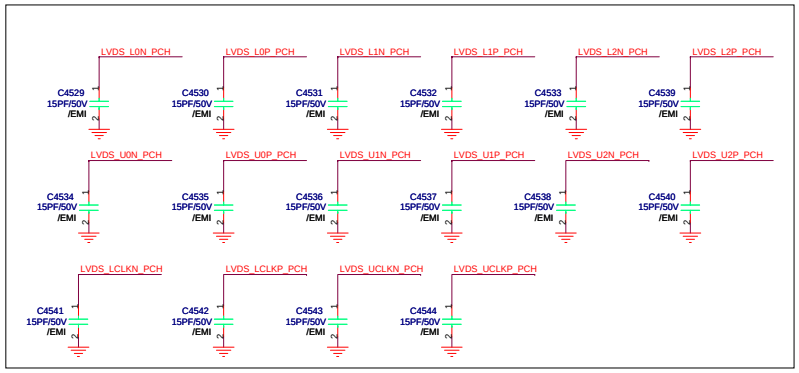
ASUSTeK COMPUTER INC. NB3	Title : BUG_NewCard & LPC	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 44 of 95	

LCD Power

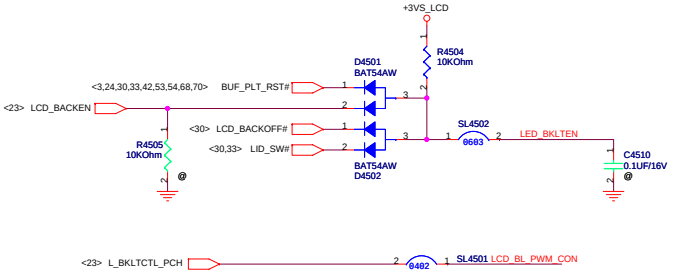
0930: 峭湮Q4502襞莨掷

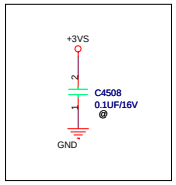


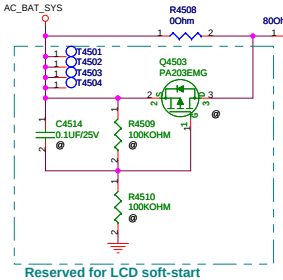
for EMI



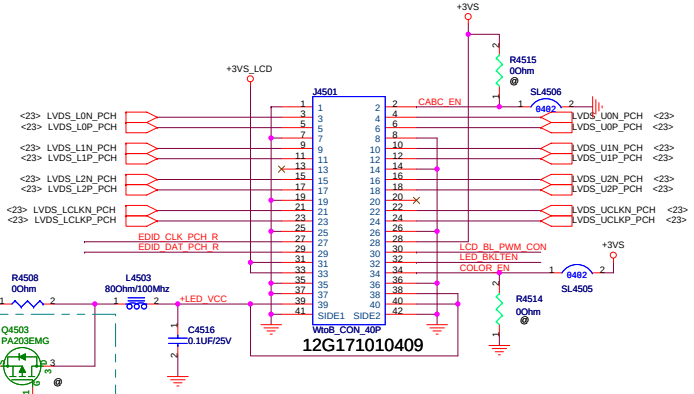
Panel Connector



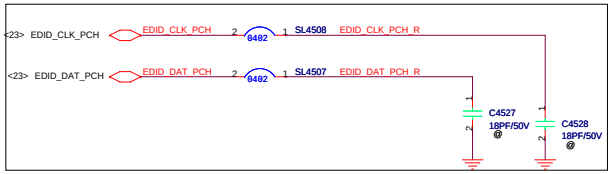




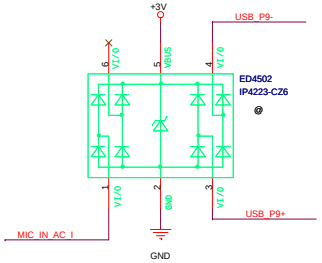
Reserved for LCD soft-start

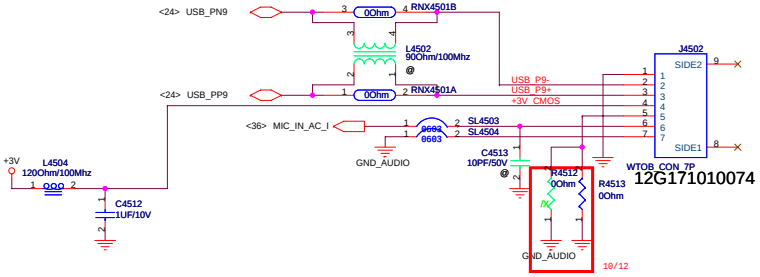


for EMI



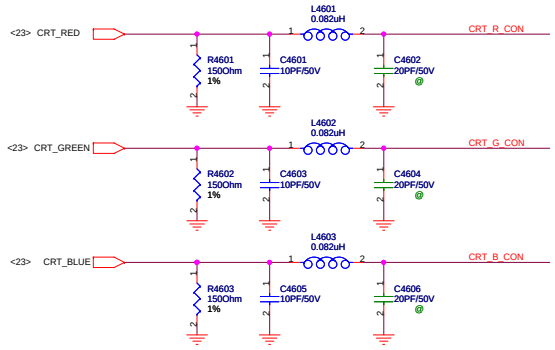
CMOS & Int. Mic.

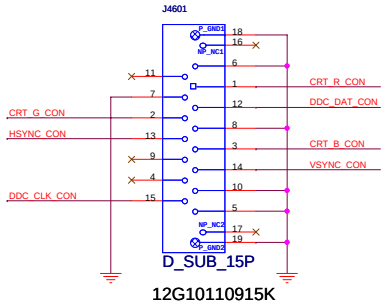


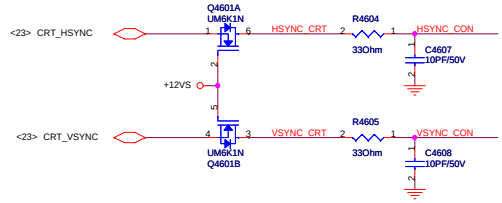


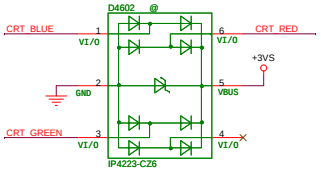
10/12

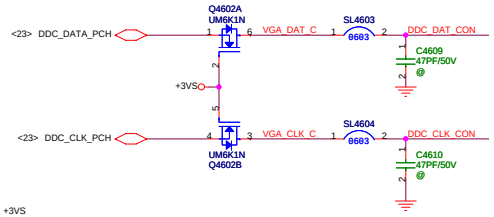
ASUSTeK COMPUTER INC. NB3	Title : CRT_LVDS & CMOS	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 45 of 95	

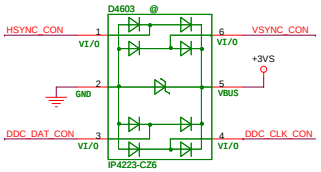


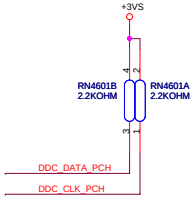








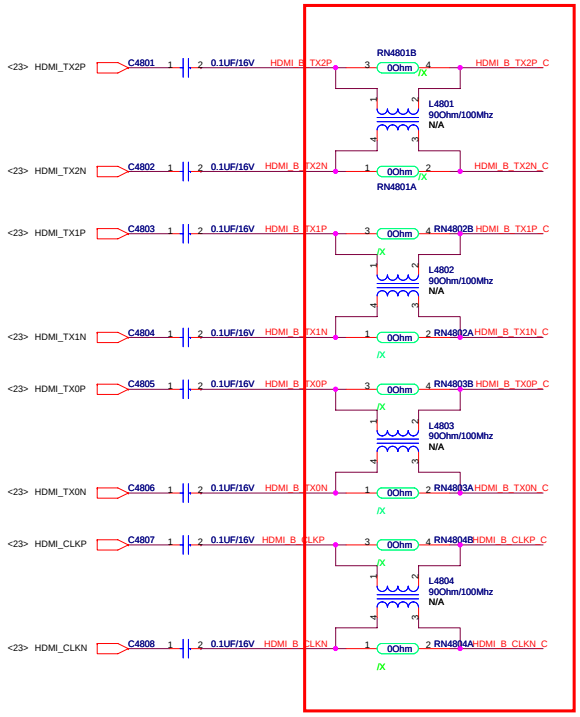


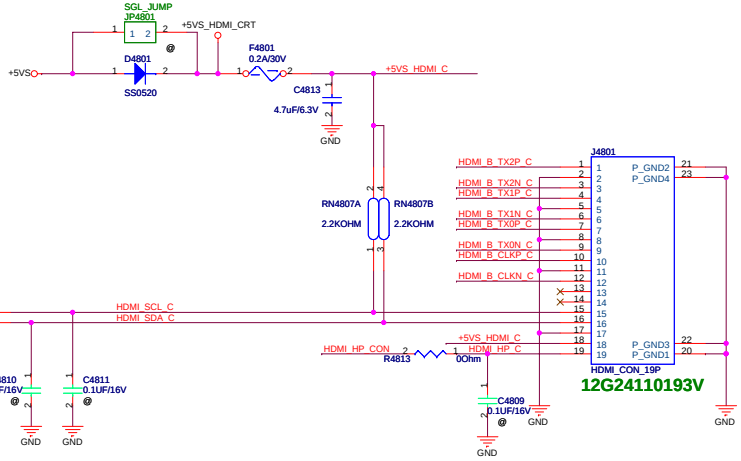


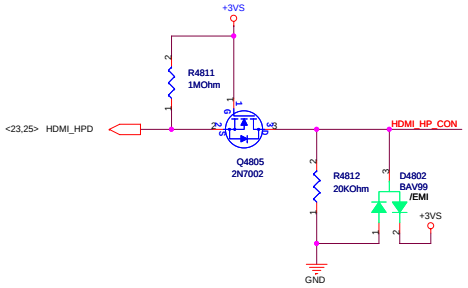
ASUSTeK COMPUTER INC. NB3	Title : CRT_D-Sub	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 46 of 95	

Main Board

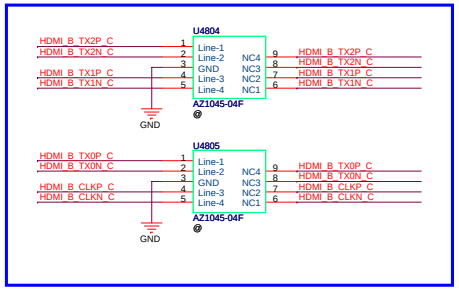
ASUSTeK COMPUTER INC. NB3	Title : CRT_****	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 47 of 95	

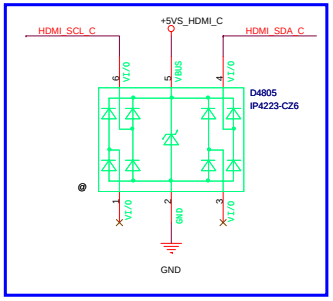


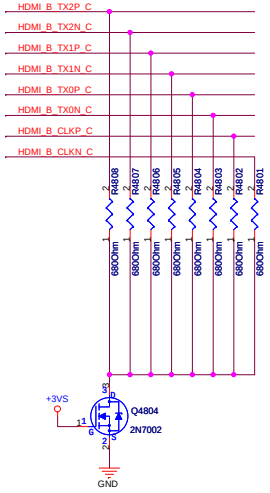


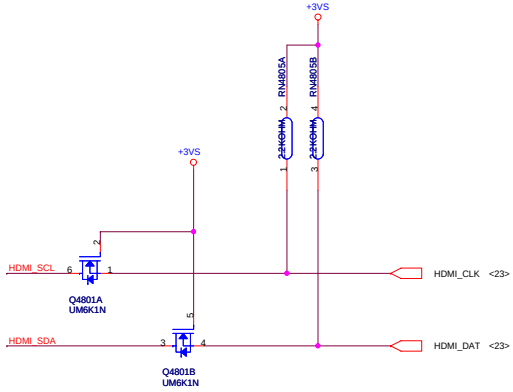


Keep R4809/R4810 = 100K/10K and mount D4802 in case of HPD input is 5V or 3.3V and chip has internal pull down resistor.









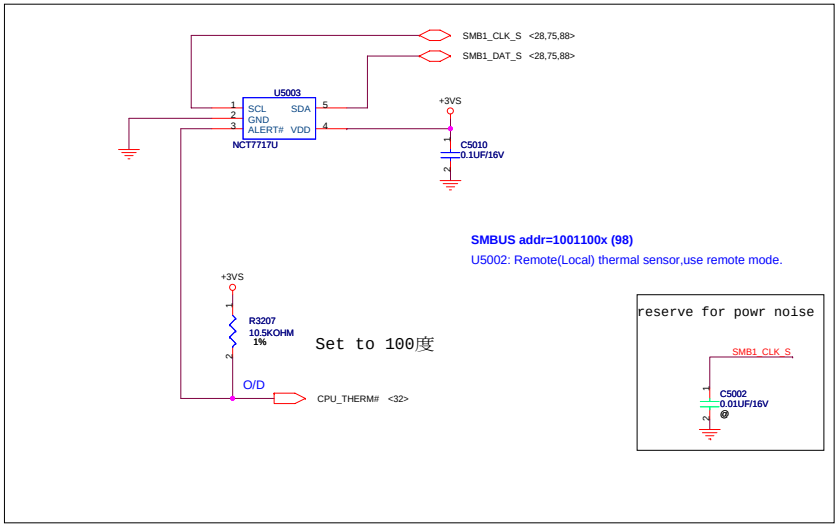
ASUSTeK COMPUTER INC. NB3	Title : CRT_HDMI		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 48 of 95		

Main Board

ASUSTeK COMPUTER INC. NB3	Title : HDMI_****	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 49 of 95	

CPU Thermal Sensor

change Thermal sensor solution

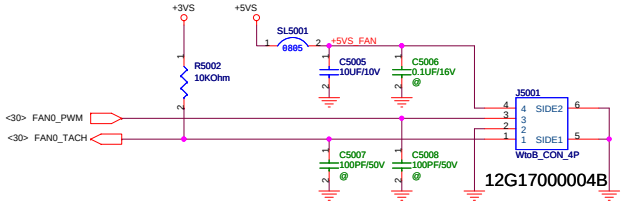


Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

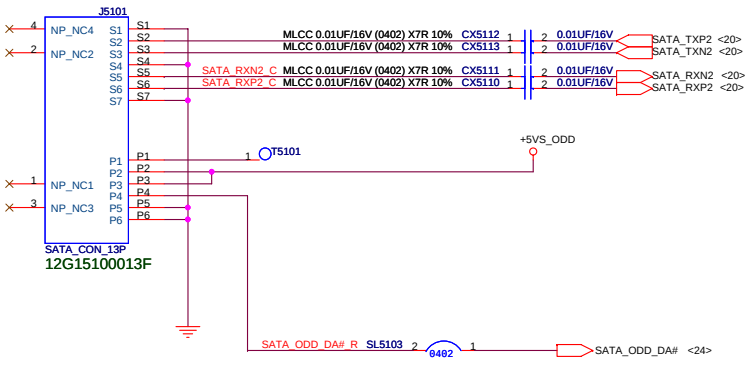
DC FAN Control



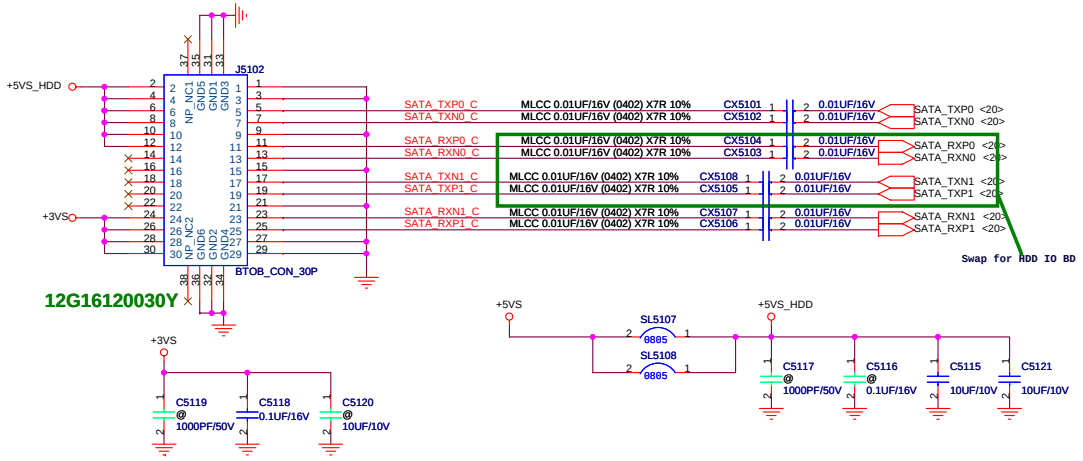
ASUSTeK COMPUTER INC. NB3	Title : FAN_Thermal Sensor & Fan	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 50 of 95	

Main Board

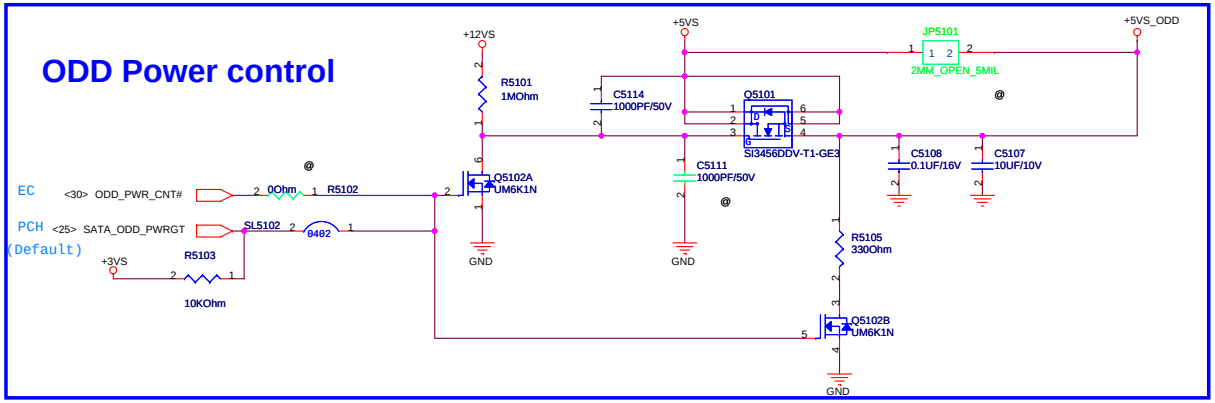
ODD



HDD

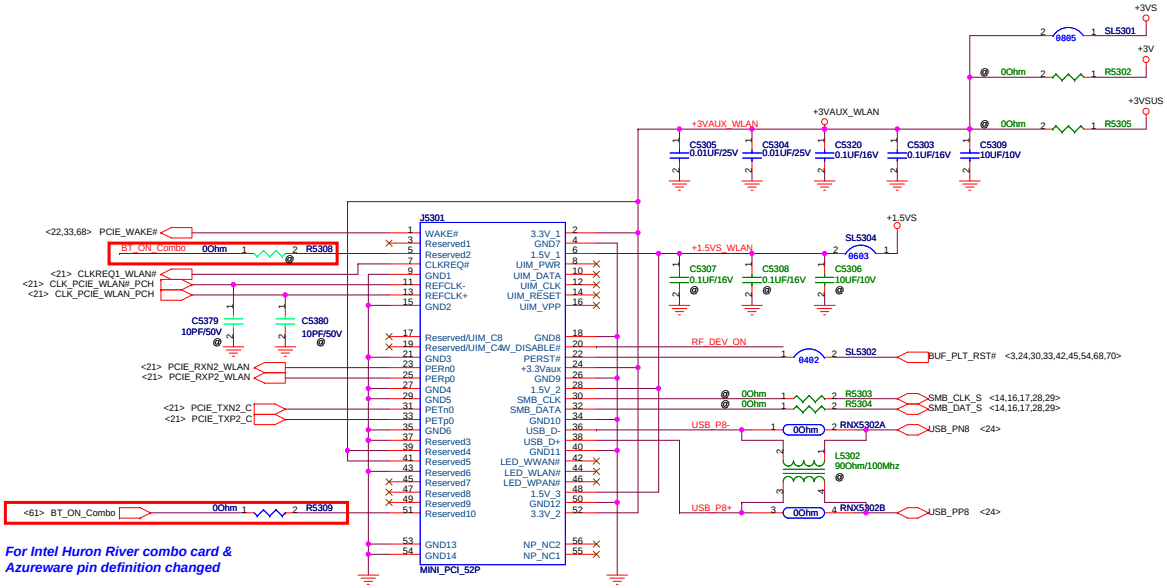


ODD Power control



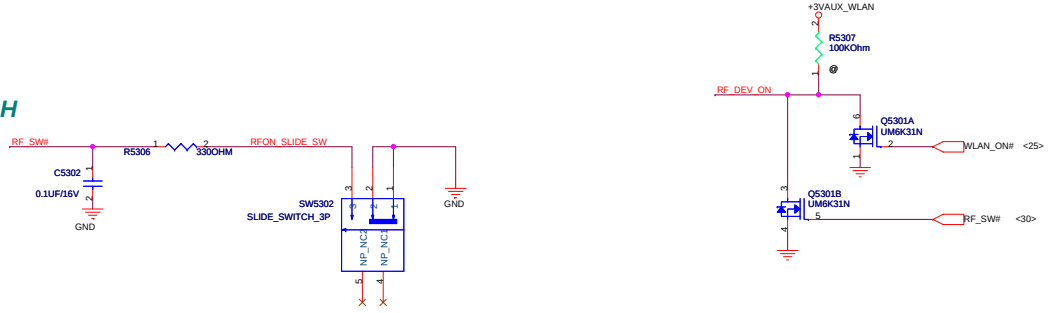
ASUSTeK COMPUTER INC. NB3	Title : XDD_HDD & ODD Conn.	
	Engineer: Wish	
Size: Custom	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 51 of 95	

ASUSTeK COMPUTER INC. NB3	Title : Empty Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 52 of 95	



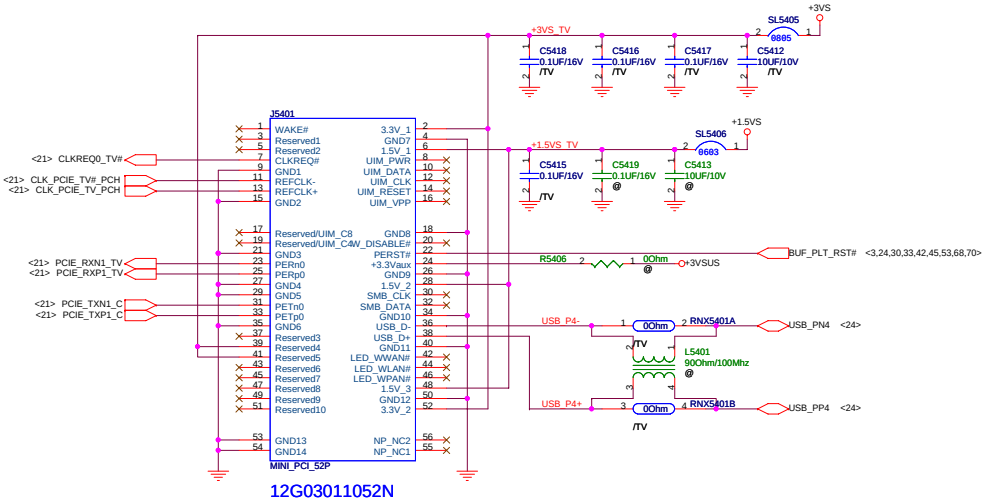
12G03011052N

RF SWITCH



12G09107003D

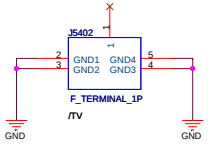
ASUSTeK COMPUTER INC. NB3	Title : PCI_WiFi/WiMax		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 53 of 95		



12G03011052N

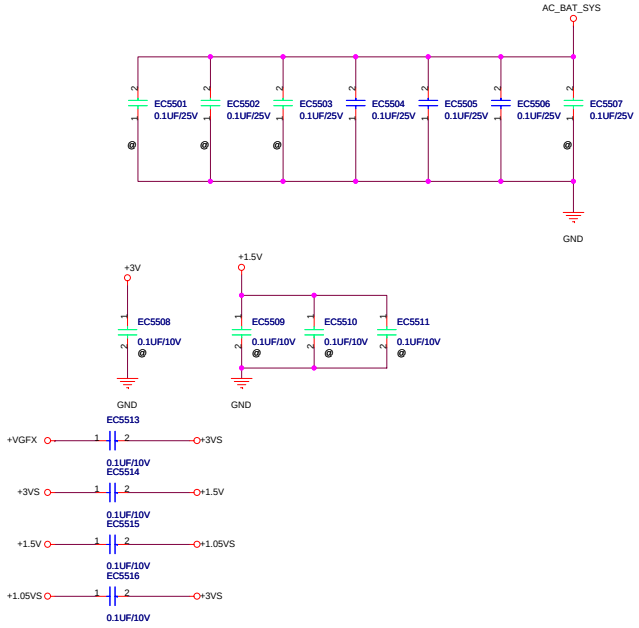
/TV

TV Conn.



14G152158000

ASUSTeK COMPUTER INC. NB3	Title : TUN_TV Tuner	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 54 of 95	

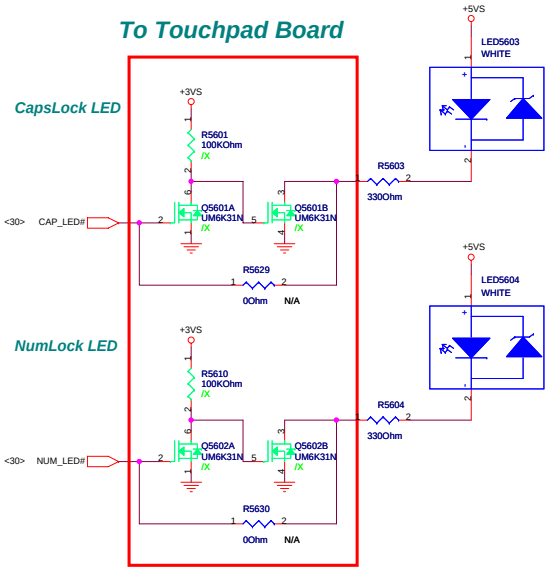


ASUSTeK COMPUTER INC. NB3	Title : Empty	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 55 of 95	

Main Board

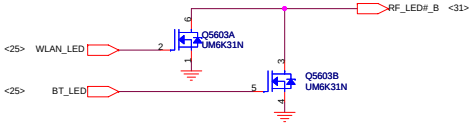
To Touchpad Board

CapsLock LED

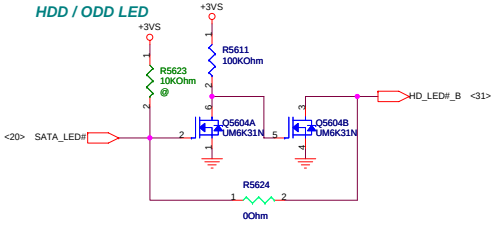


NumLock LED

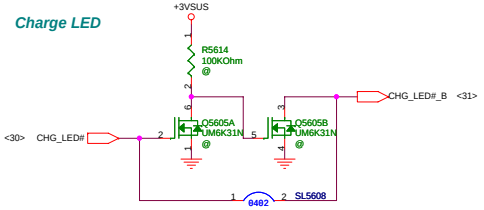
Wireless ON LED



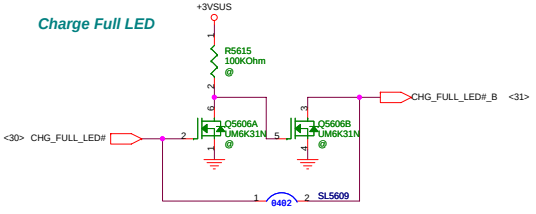
HDD / ODD LED



Charge LED

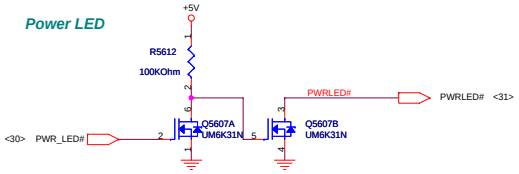


Charge Full LED

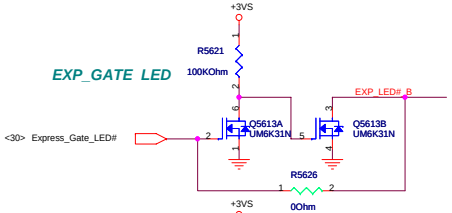


delete dGPU/iGPU LED

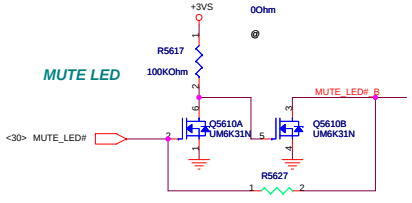
Power LED



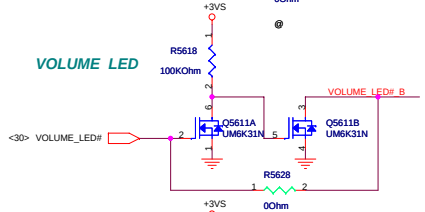
EXP_GATE LED



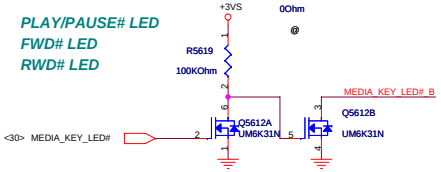
MUTE LED

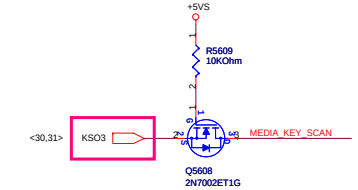


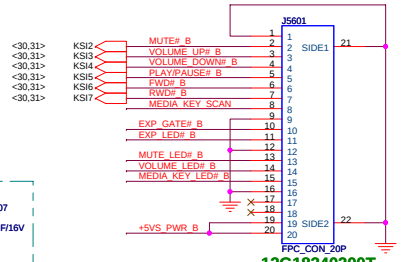
VOLUME LED

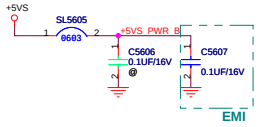


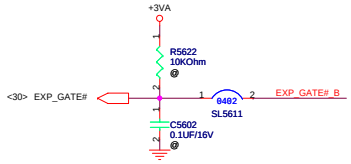
PLAY/PAUSE# LED
FWD# LED
RWD# LED

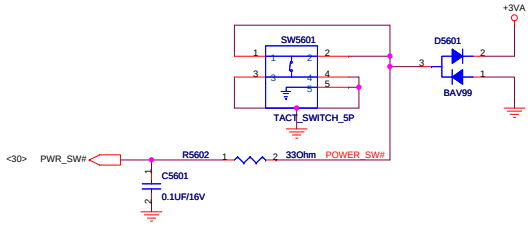




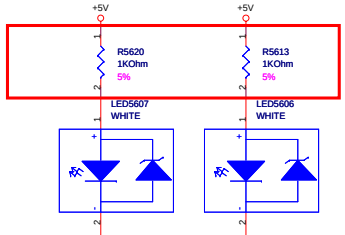




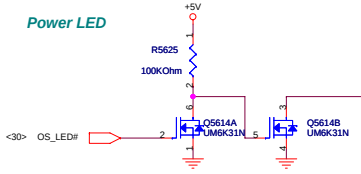




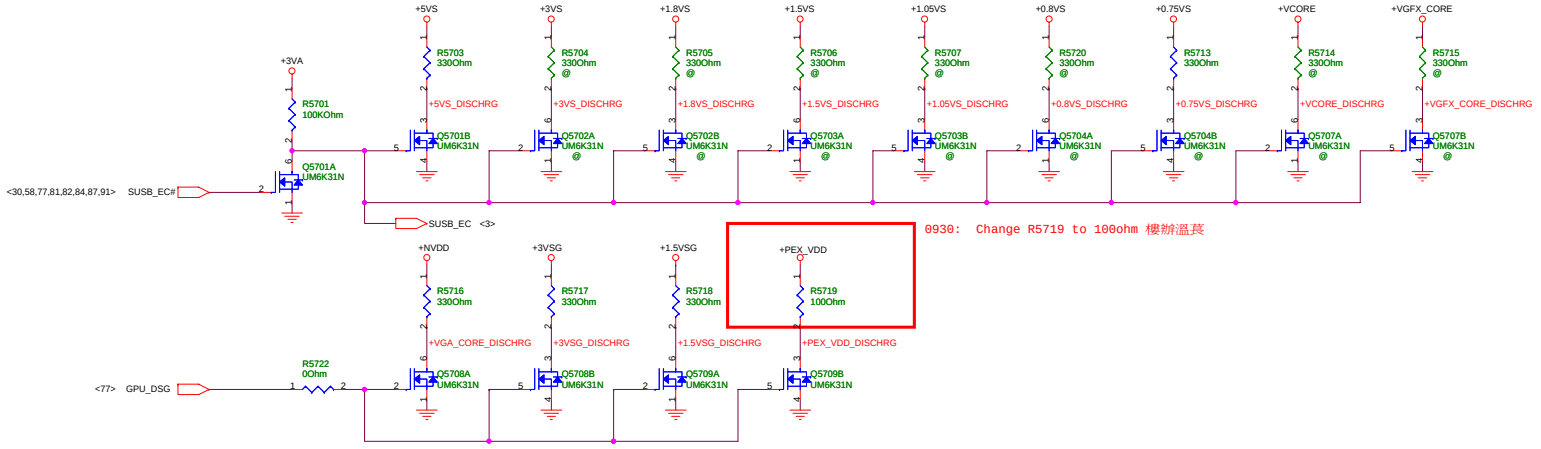
change R5620 R5613 to 1k for energy star



Power LED

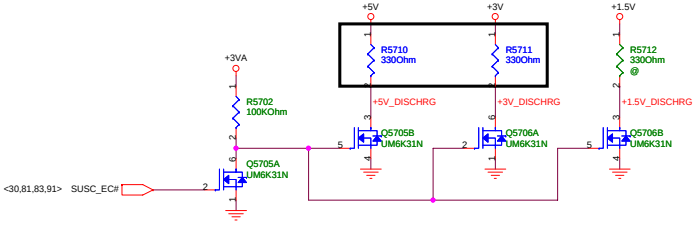


ASUSTeK COMPUTER INC. NB3	Title : LED_LED & Switch	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 56 of 95	

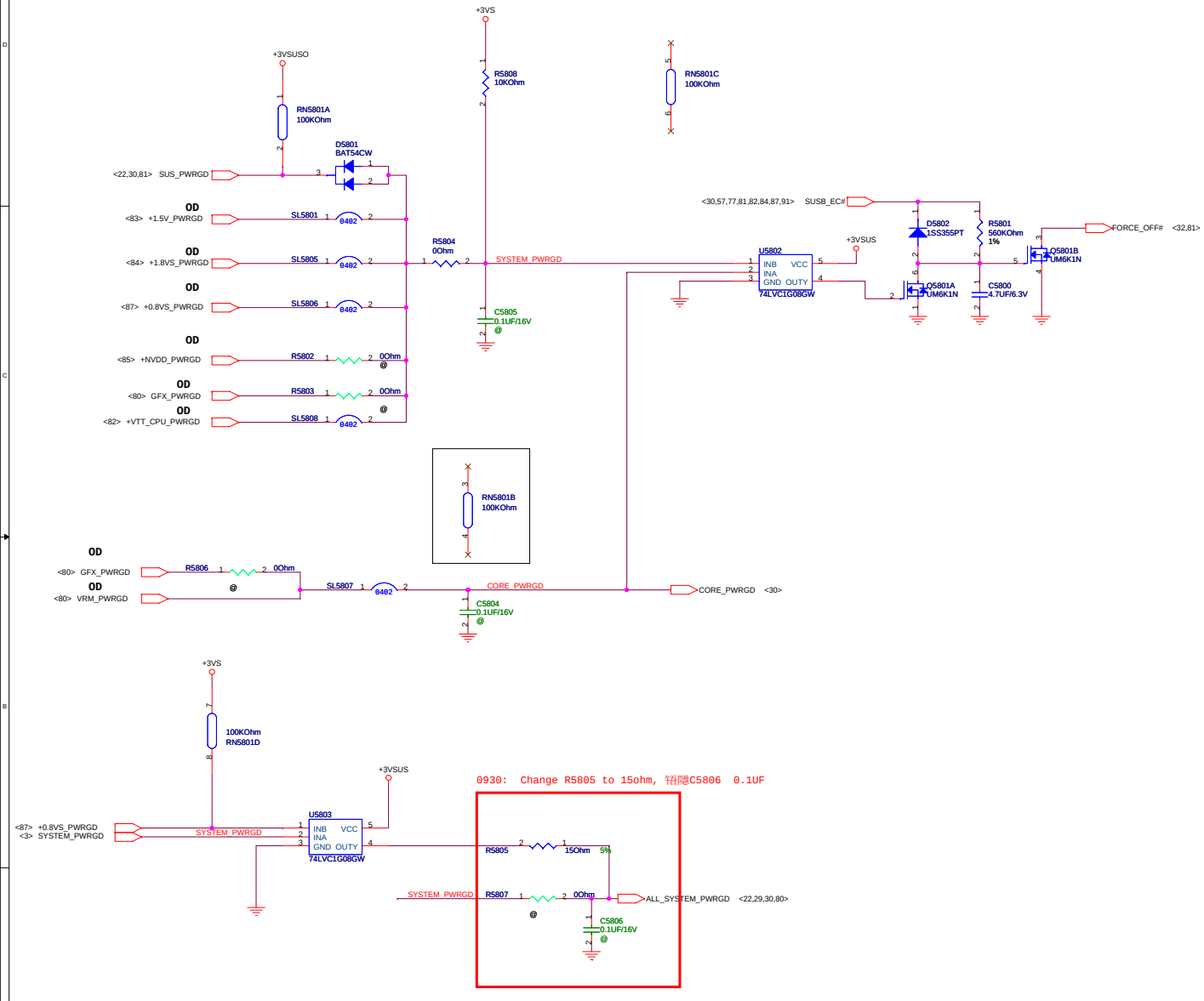


0930: Change R5719 to 100ohm 樓辦溫蔑

Stuff R5710 and R5711



ASUSTeK COMPUTER INC. NB3	Title : DSG_Discharge	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 57 of 95	



ASUSTeK COMPUTER INC. NB3	Title : PRO_Protect	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 58 of 95	

Title : Dynamic Vcore Ctrl

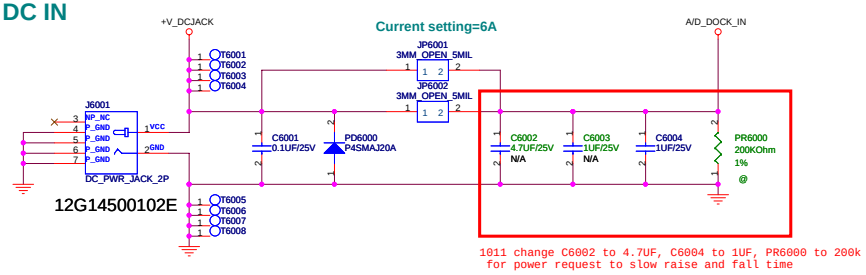
ASUSTeK COMPUTER INC. NB3

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

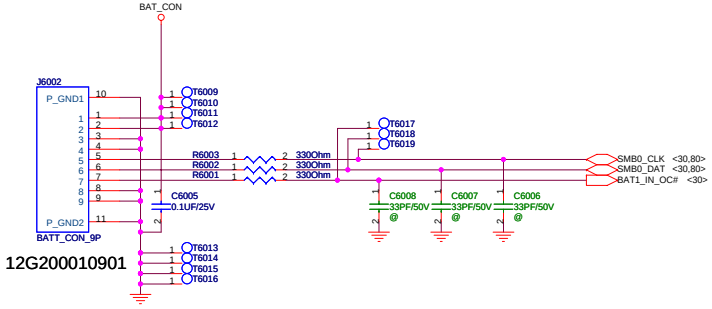
Date: Wednesday, October 13, 2010 Sheet 59 of 95

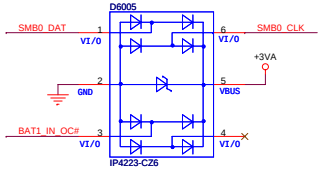
DC IN



1011 change C6002 to 4.7UF, C6004 to 1UF, PR6000 to 200k
for power request to slow raise and fall time

BAT IN



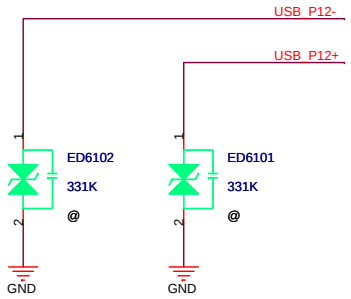


ASUSTeK COMPUTER INC. NB3	Title : DC_DC & BAT IN	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 60 of 95	

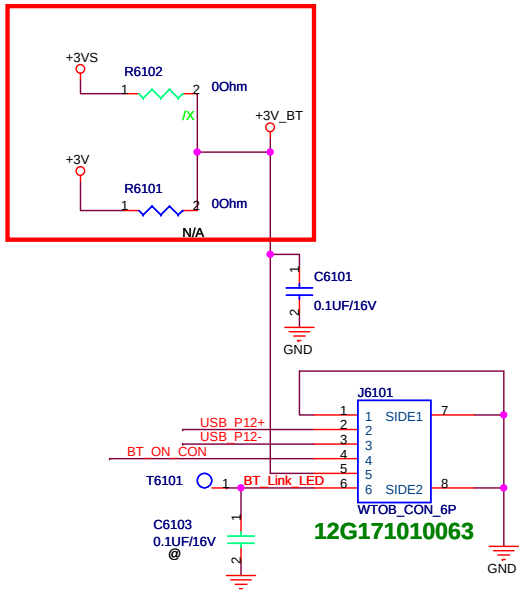
Main Board

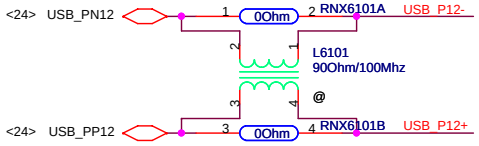
BLUETOOTH

Reserve for EMI

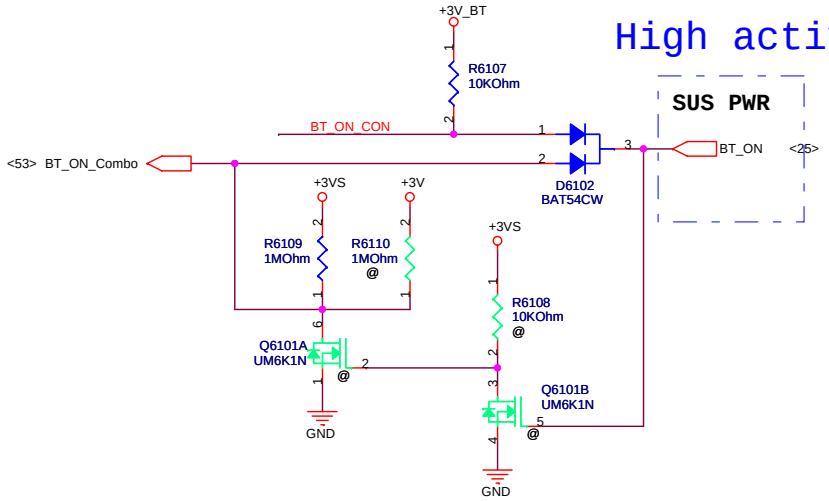


10/12 Reserve R6102 For Energy Satr





High active



ASUSTeK COMPUTER INC. NB3	Title : BT_Bluetooth	
	Engineer: Wish	
Size: B	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 61 of 95	

Main Board

ASUSTeK COMPUTER INC. NB3

Title : TPM_****

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 62 of 95

Main Board

ASUSTeK COMPUTER INC. NB3

Title : FP ****

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 63 of 95

Main Board

ASUSTeK COMPUTER INC. NB3	Title : BAR_****	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 64 of 95	

Main Board

Screw D x 2 for ODD

H6551 s04335 — NP_NC, GND1 GND4, GND2 GND3 — CT197D91N

H6552 s04335 — NP_NC, GND1 GND4, GND2 GND3 — CT197D91N

Screw E x 4

H6555 s04492 — NP_NC, GND1 GND4, GND2 GND3 — C315D110N

H6557 s04492 — NP_NC, GND1 GND4, GND2 GND3 — C315D110N

H6558 s04492 — NP_NC, GND1 GND4, GND2 GND3 — C315D110N

Screw F x 10

H6559 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6561 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6563 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6565 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6567 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6560 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6562 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6564 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6566 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

H6568 s04493 — NP_NC, GND1 GND4, GND2 GND3 — CRT315X354B315D110N

Screw B x 4 *CPU Bracket*

H6505 — C276D138

H6506 — C276D138

H6507 — C276D138

H6508 — C276D138

Screw H x 1

H6571 s04504 — NP_NC, GND1 GND4, GND2 GND3 — CT315CB394D110N

Screw C x 4 *GPU Bracket*

H6523 — CT156CRB299X327D136

H6522 — CT156CRB299X327D136

H6524 — CT156CRB299X327D136

H6521 — CT156CRB299X327D136

H6569 — C110D110N

H6572 — O315X433DO197X315

H6570 — DO126X114N

MiniCard (Wifi) Stand-Off

HMC

H6501 — CT217B67D47 — 13GNJA10M060-1

H6502 — CT217B67D47 — 13GNJA10M060-1

MiniCard (TV) Stand-Off

MC

H6531 — CT217B67D47 — /TV — 13GNJA10M060-1

H6532 — CT217B67D47 — /TV — 13GNJA10M060-1

FAN Stand-Off

H6535 — U5F-M-EXPREE — 13G021036001

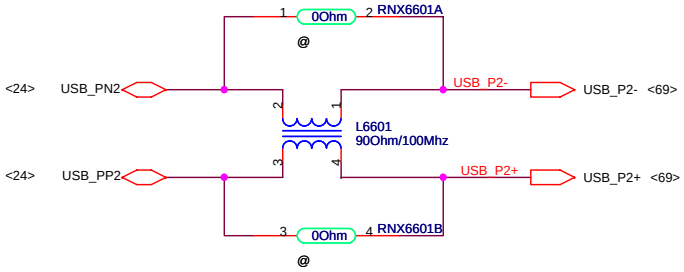
H6536 — A40M20-64AS — 13G021029050

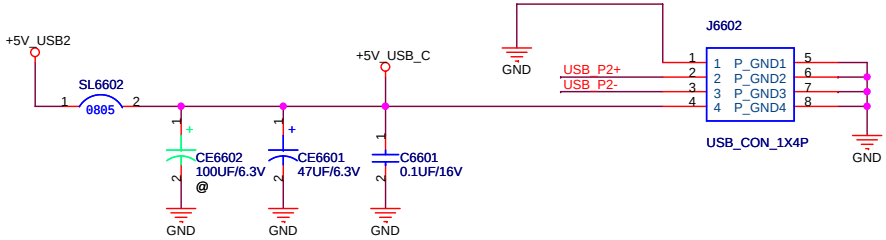
HDD Stand-Off

H6573 — CT236SB354ID146 — 13G021043060

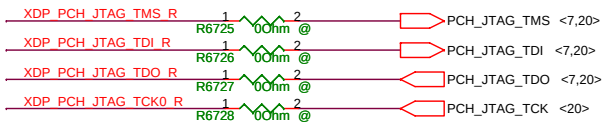
H6574 — CT236SB354ID146 — 13G021043060

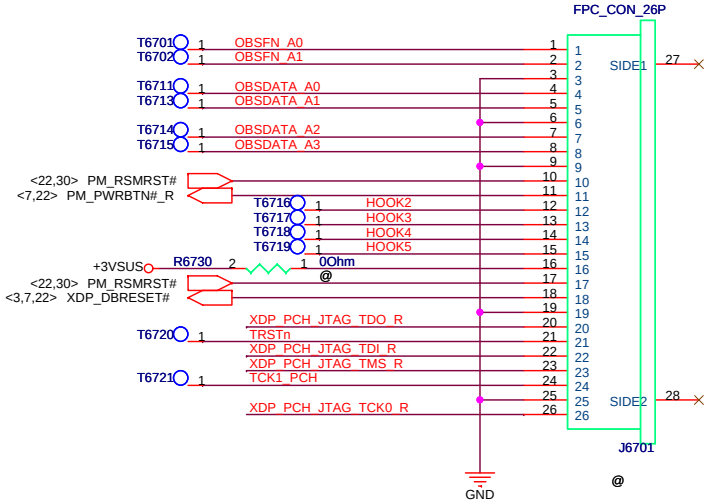
ASUSTeK COMPUTER INC. NB3	Title : ME_W2B conn. & NUT	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 65 of 95	



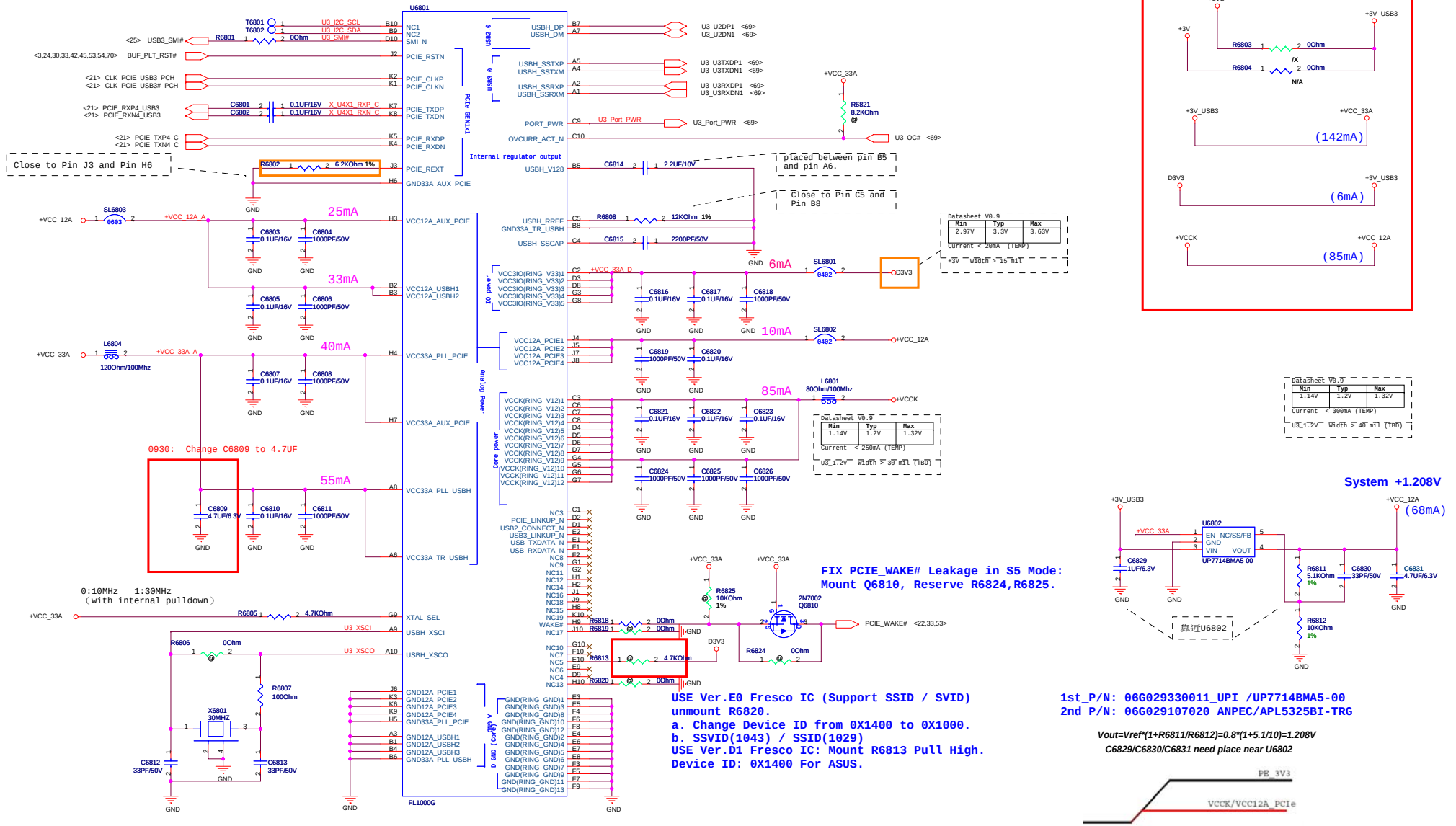


ASUSTeK COMPUTER INC. NB3	Title : USB2.0 Port	
	Engineer: Wish	
Size: B	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 66 of 95	





ASUSTeK COMPUTER INC. NB3	Title : OTH_PCH_XDP	
	Engineer: Wish	
Size: B	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 67 of 95	



reserve +3VS for USB3.0 for energy star

1st_P/N: 06G029330011_UPI /UP7714BMA5-00
2nd_P/N: 06G029107020_ANPEC/APL5325BI-TRG

Vout=Vref(1+R6811/R6812)=0.8*(1+5.1/10)=1.208V*
C6829/C6830/C6831 need place near U6802

Remove the power-up sequence

USE XTAL 30MHz(Size:3225)
Mount C6812,C6813= 33pF/50V, Mount R6805 Pull High.
1st_P/N: 07G010213002_TXC/7V30000001
2nd_P/N: 07G010713000_FUJICOM/FSX3M30.000000M20FAO

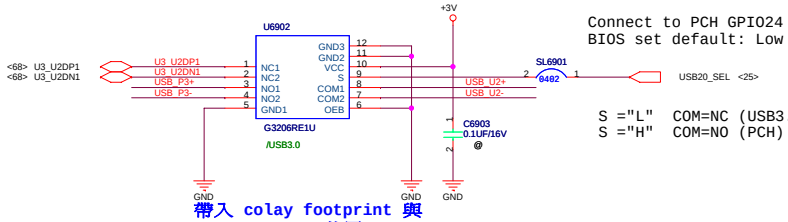
USE XTAL 10MHz(Size:5032)
Mount C6812,C6813= 22pF/50V,Unmount R6805.
P/N: 07G010201002_TXC/7A10000028

USE Vendor Ver.E0_P/N: 02G165000120
FRESCO FL1000G (E0) TFBGA100 (ES)
to replace Ver.D1_P/N: 02G165000110
FRESCO FL1000G (D1) TFBGA100 (MP)

(1) ADD S3 remove wake-up Function .
(2) Support to write SSID/SSVID.

ASUSTeK COMPUTER INC. NB1	Title : USB 3.0_FRESCO		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 68 of 95		

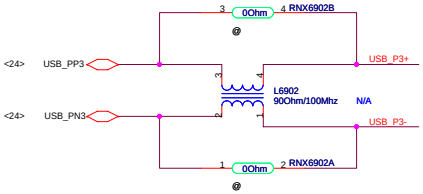
USB ports



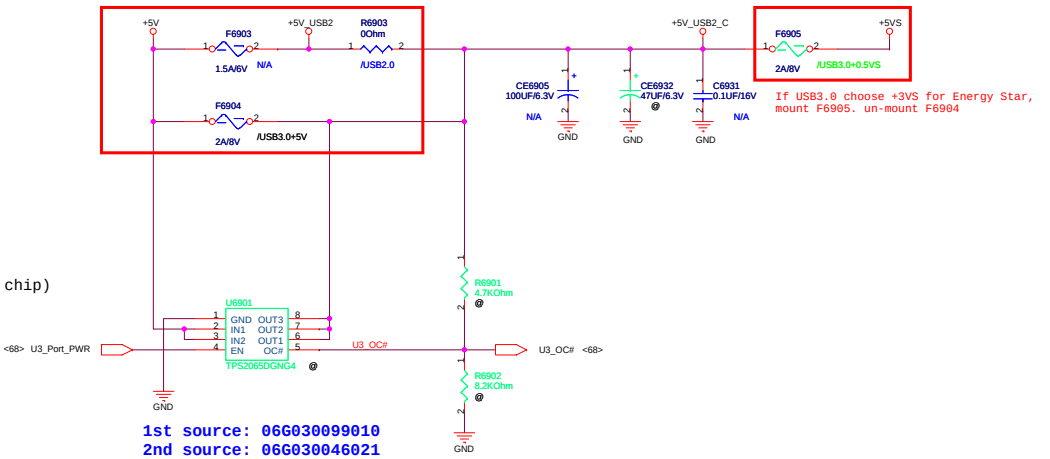
Connect to PCH GPIO24
BIOS set default: Low

S ="L" COM=NC (USB3.0 chip)
S ="H" COM=NO (PCH)

帶入 colay footprint 與
06G114005020 共用



0930: USB 2.0 改F6903 & R6903乙USB 3.0改F6903 & F6904,祥改R6903



1st source: 06G030099010
2nd source: 06G030046021

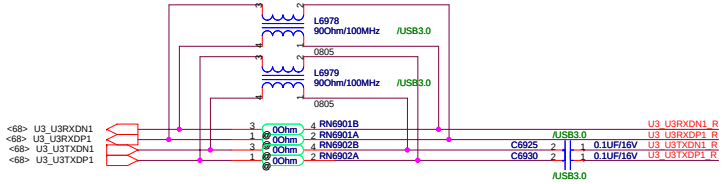
Fresco USB3.0 VBUS Contorl Circuit

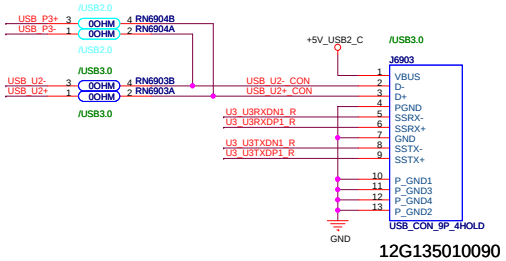
Follow USB3.0 Logo 認證 (必要條件：a. S3 Wake up; b. VBUS Control Circuit)
需搭配 Ver. E0 Fresco Chipset IC 才採PWR SW方式上件，目前(Ver. D1)採Poly Fuse方式上件

1. Unmount R6819,U6901. Mount F6903,R6903,R6904 for Poly Fuse in Ver. D1 Fresco Chipset IC.

2. Mount R6819,U6901. Unmount F6903,R6903,R6904 for PWR SW in Ver. E0 Fresco Chipset IC.

USB3.0 EMI-Protection

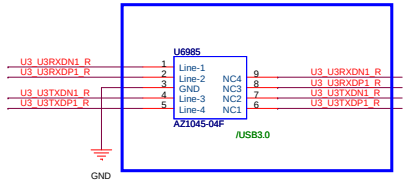




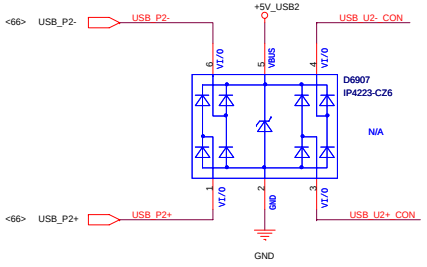
12G135010090

If BOM w/USB2.0,then
stuff 12G131090046

USB3.0/USB 2.0 ESD-Protection

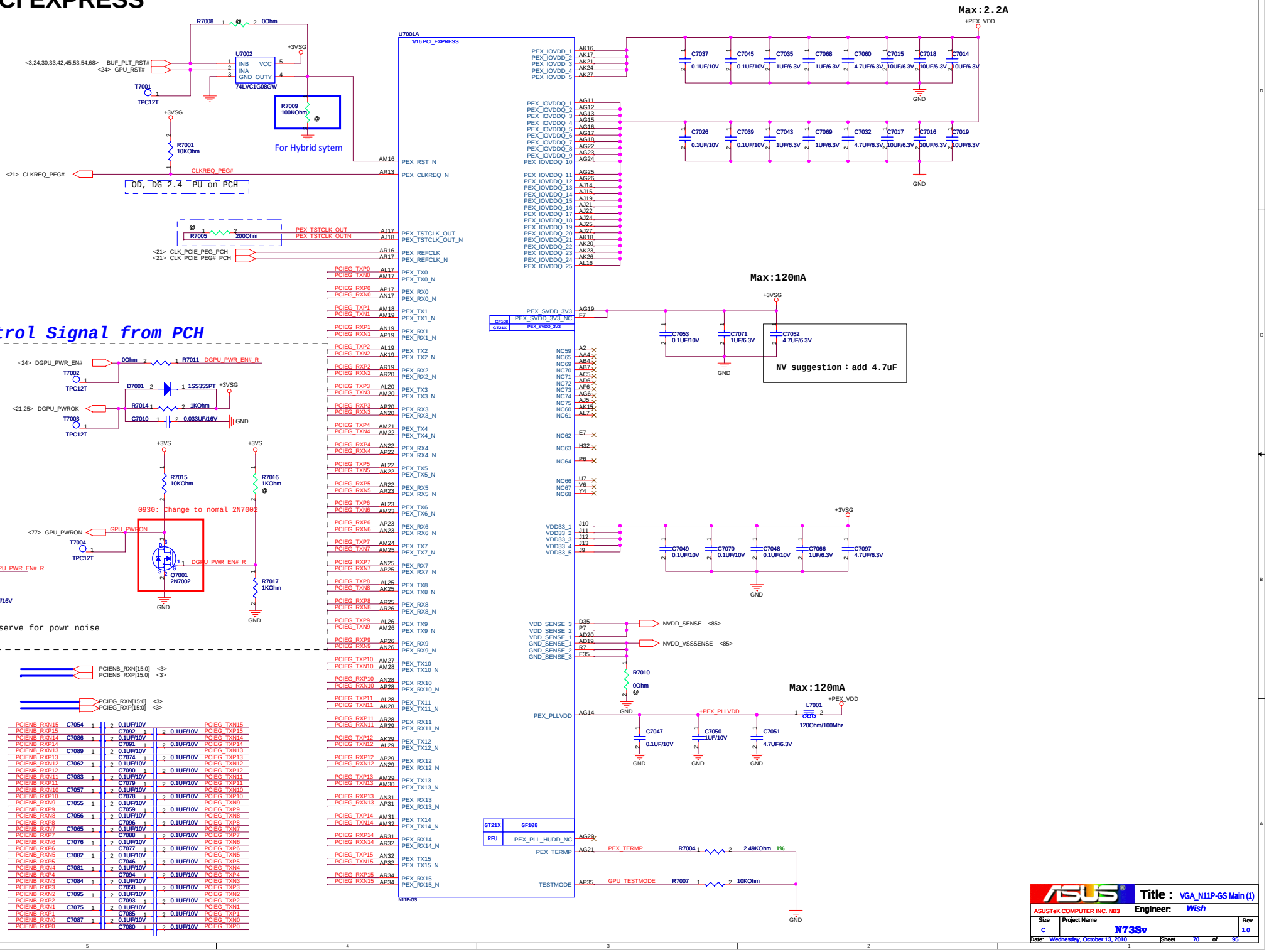


走線請直接由 U1485 穿過至零件另一側之對應 pin
勿成分枝狀走線



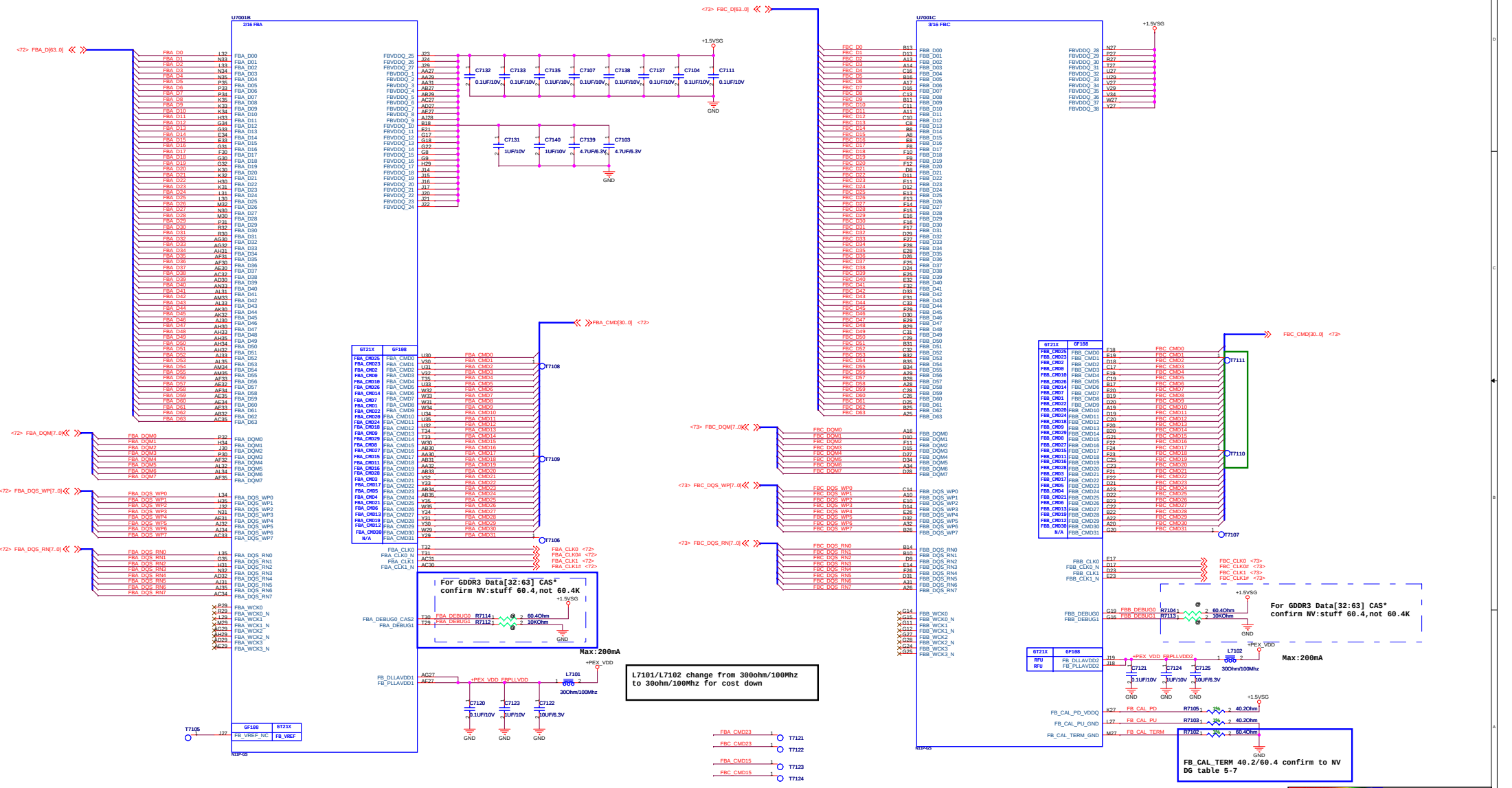
ASUSTeK COMPUTER INC. NB4	Title : USB3.0 Port	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 69 of 95	

PCI EXPRESS

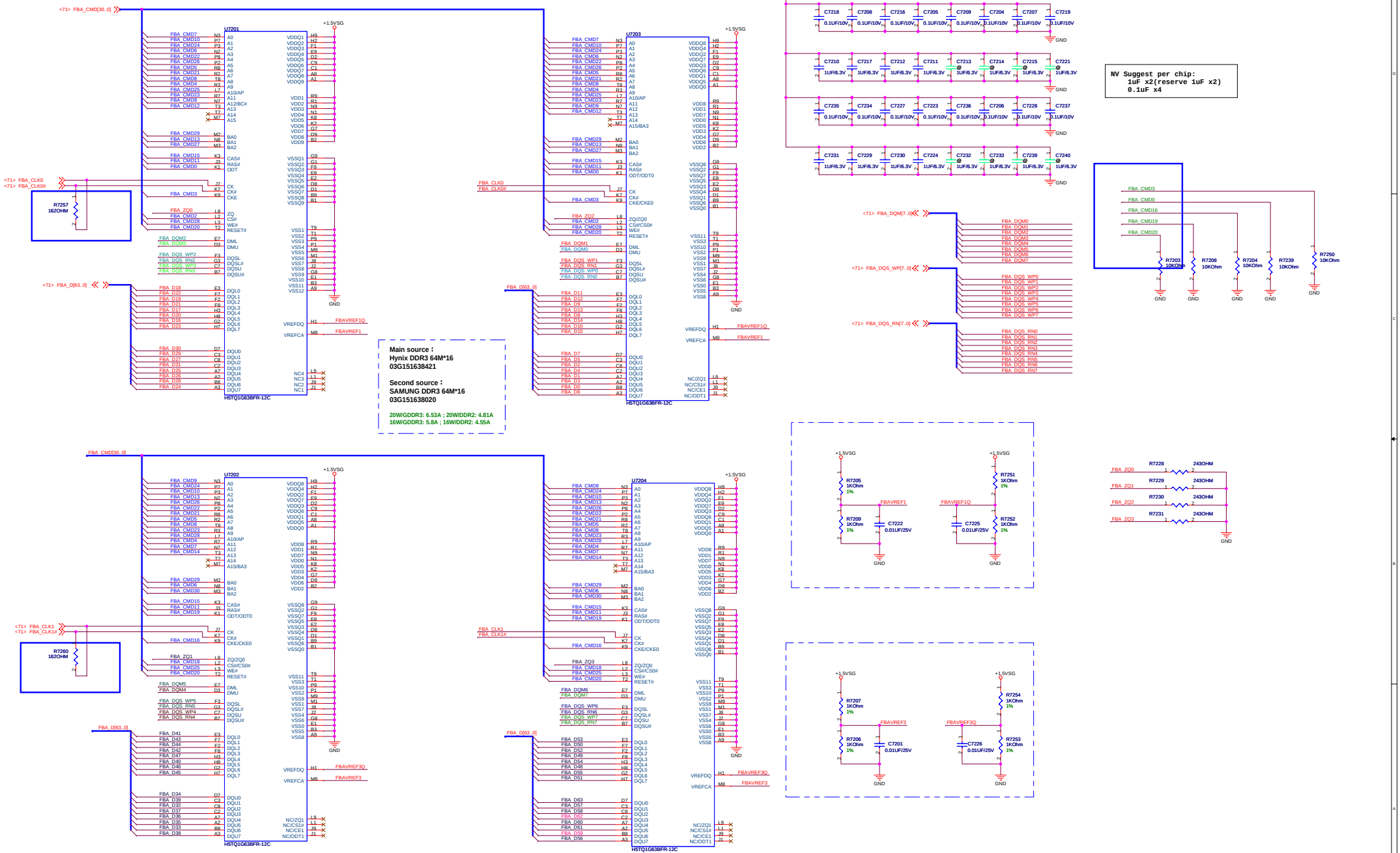

Max:2.2A
Max:120mA
Max:120mA
Control Signal from PCH
GPI054
GPI017
U7001A
1/16 PCI_EXPRESS
N11P-GS
For Hybrid sytem
OD, DG 2.4 PU on PCH
0930: Change to nomal 2N7002
reserve for powr noise
NV suggestion：add 4.7uF
Title : VGA_N11P-GS Main (1)
ASUSTeK COMPUTER INC. NB3
Engineer: Wish
Project Name N73Sv
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 70 of 95

GPU MEMORY INTERFACE: PARTITION A

GPU MEMORY INTERFACE: PARTITION C

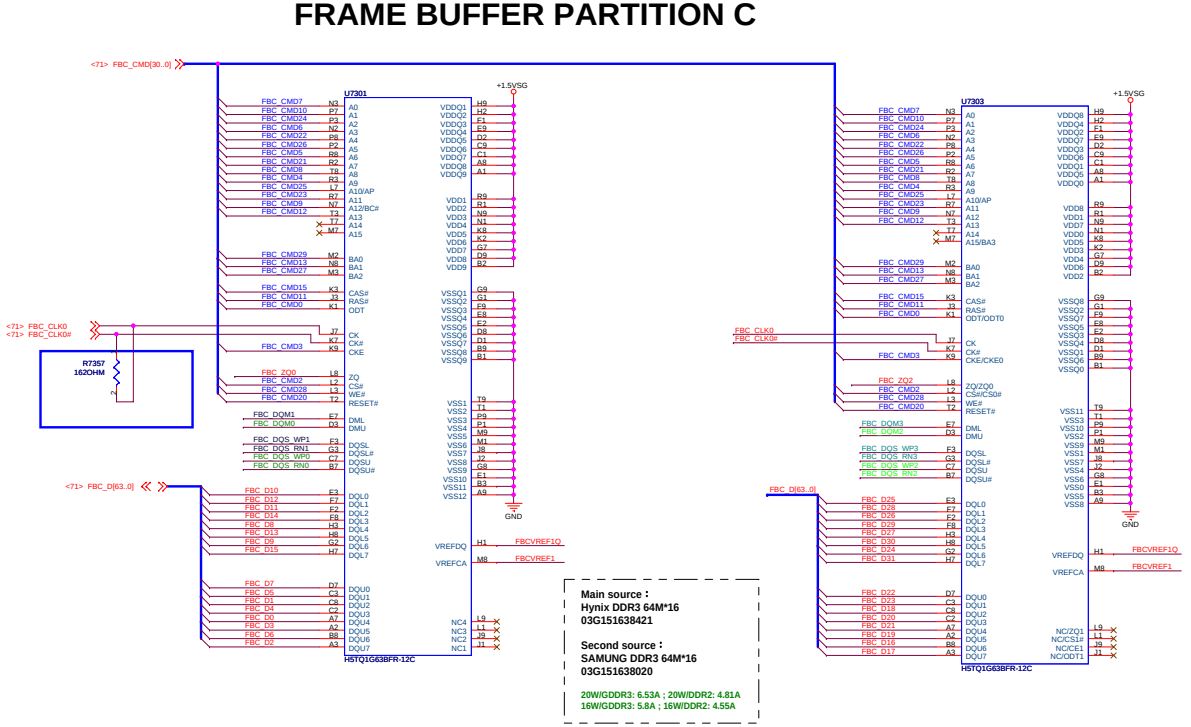


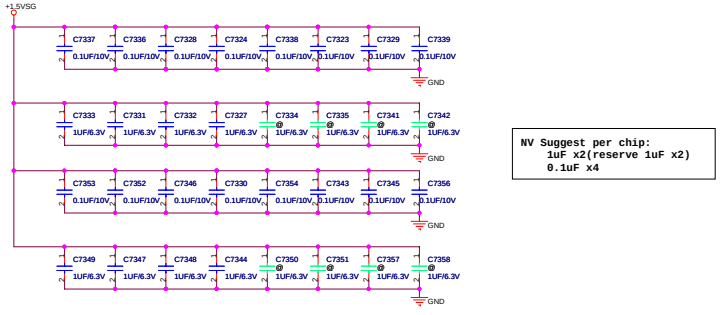
FRAME BUFFER PARTITION A



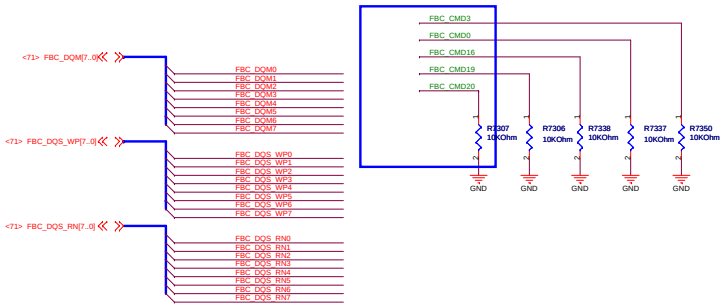
ASUSTeK COMPUTER INC.	Title : VGA VRAM CH_A		
	Engineer: Wish		
Size: Custom	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 72 of 95		

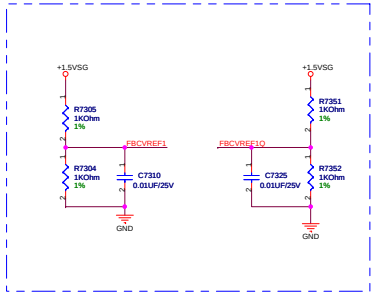
FRAME BUFFER PARTITION C

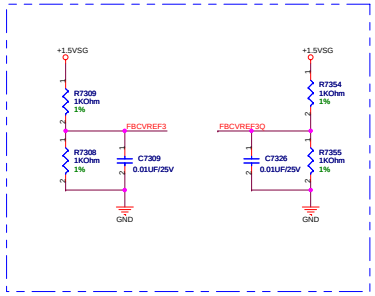


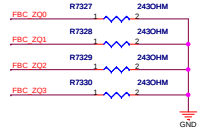


NV Suggest per chip:
1uF x2(reserve 1uF x2)
0.1uF x4

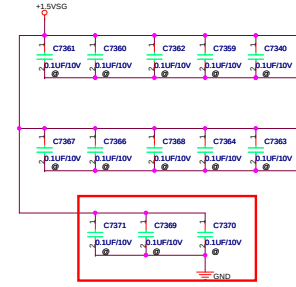






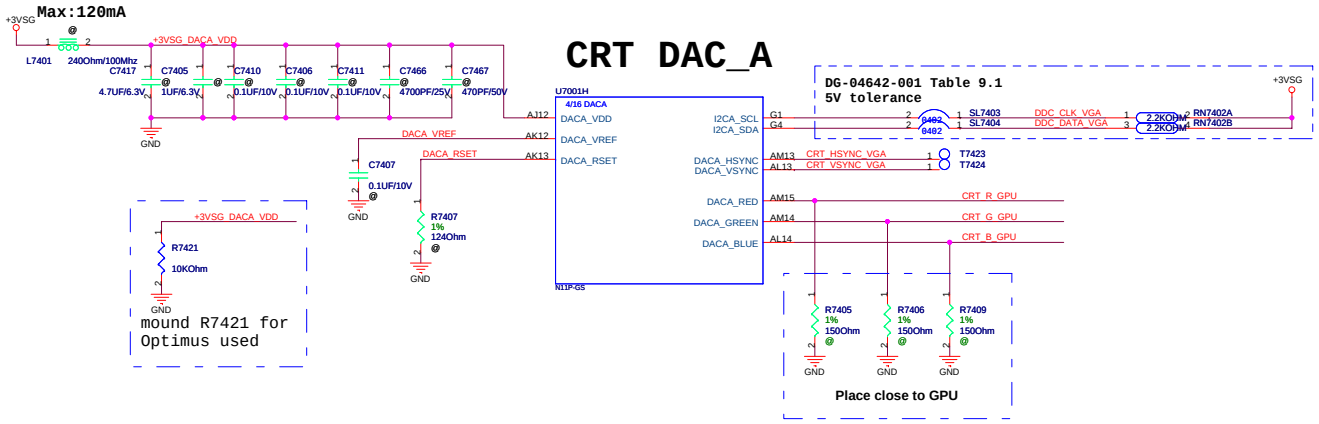


NV Suggestion close to MEM_CMD near.

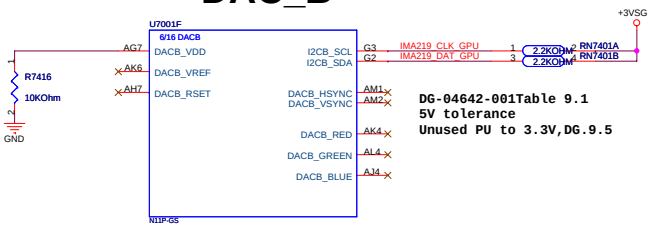


ASUSTeK COMPUTER INC.	Title : VGA VRAM CH_C		
	Engineer: Wish		
Size: Custom	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 73 of 95		

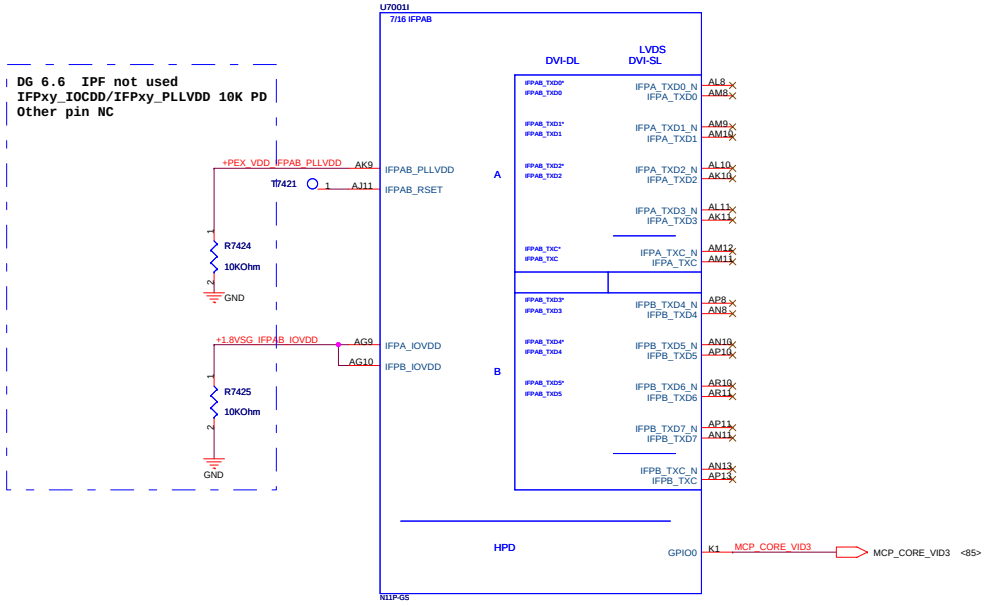
CRT DAC_A



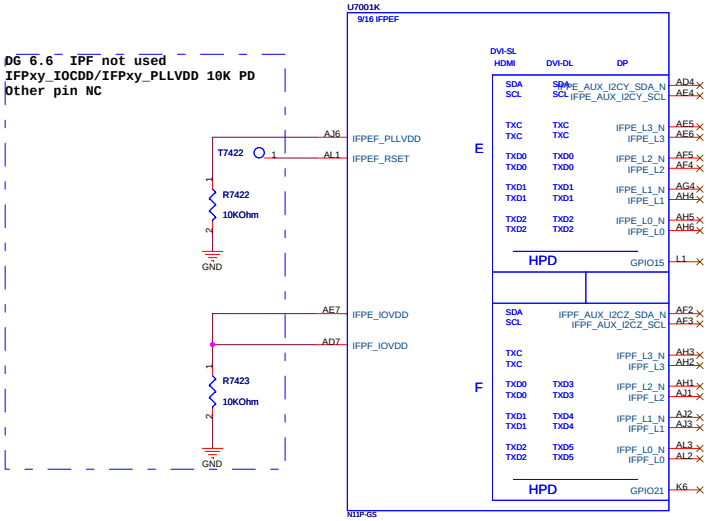
DAC_B



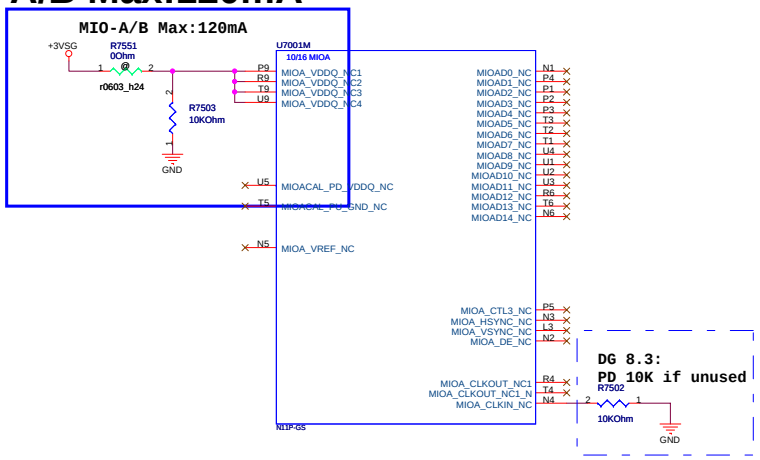
LVDS

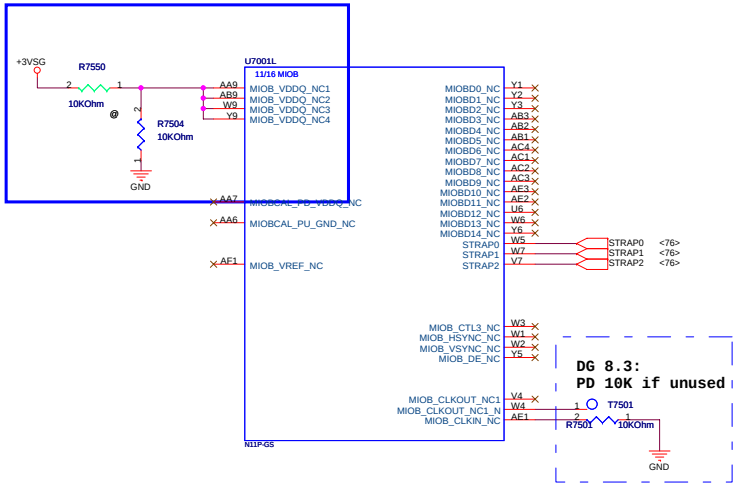


IFP_E/F



MIO-A/B Max:120mA





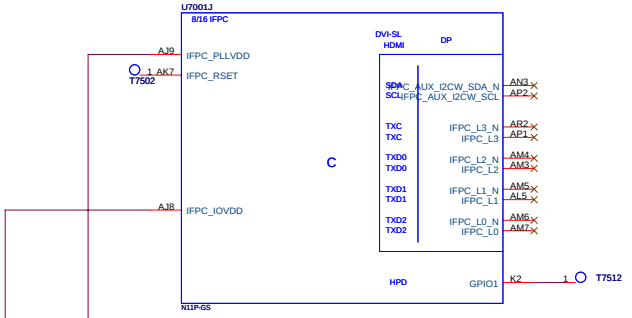
GPIO ASSIGNMENTS

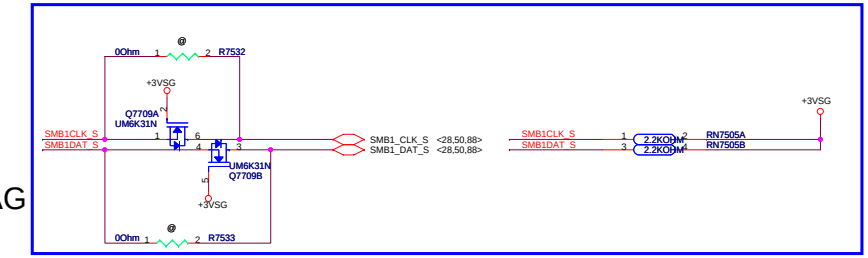
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	IFPC HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	NVVDD VID 2
8	I/O	LOW	OVER THERMAL
9	I/O	LOW	THERMAL ALERT
10	OUT	N/A	FBVREF SELECT
11	I/O	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	MEM_VID/PWR Control
14	OUT	N/A	PWR Control

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
15	IN	N/A	IFPE HOTPLUG (HDMI)
16	OUT	N/A	FAN PWM CONTROL
17	IN	N/A	RESERVED
18	IN	N/A	RESERVED
19	IN	N/A	IFPD HOTPLUG
20	IN	N/A	RESERVED
21	IN	N/A	IFPF HOTPLUG
22	IN	N/A	SLI Swap Ready Signal
23	I/O	N/A	STEREO

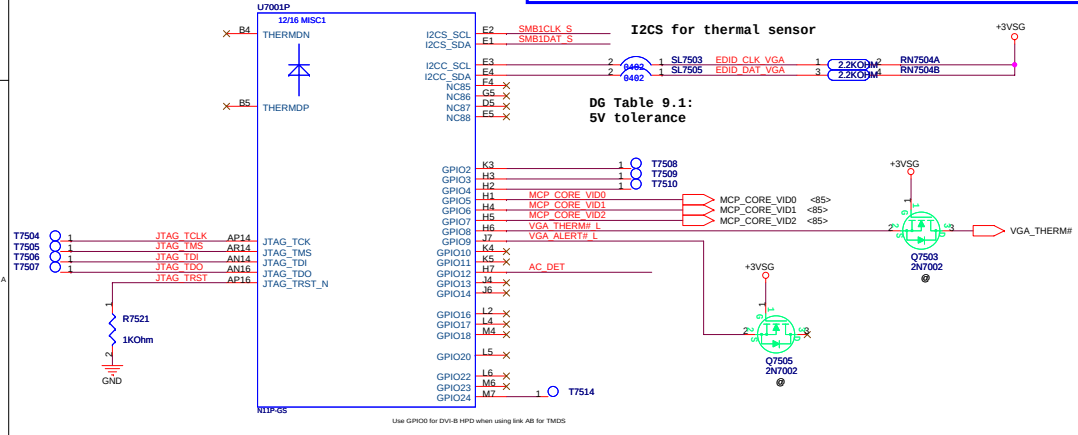
HDMI(link C)



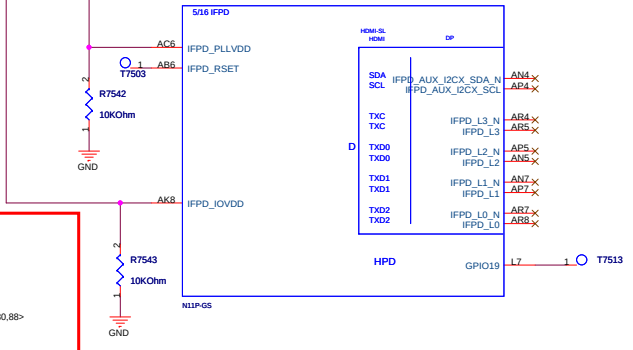


GPIO, TEMP SENSOR, JTAG

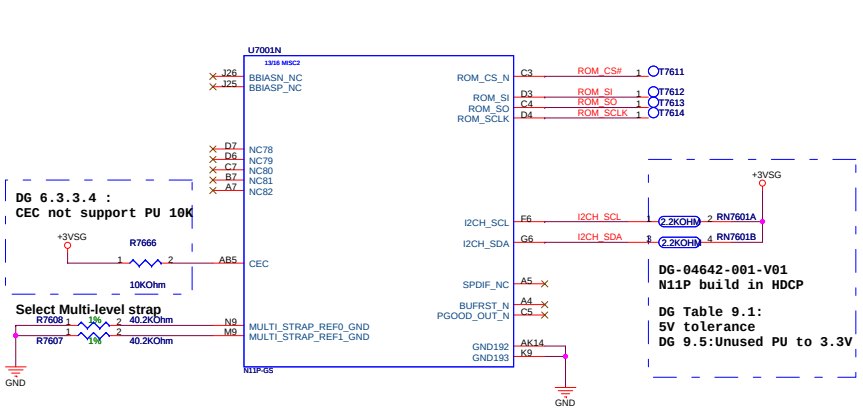
I2C ADDRESS: 0x9AH

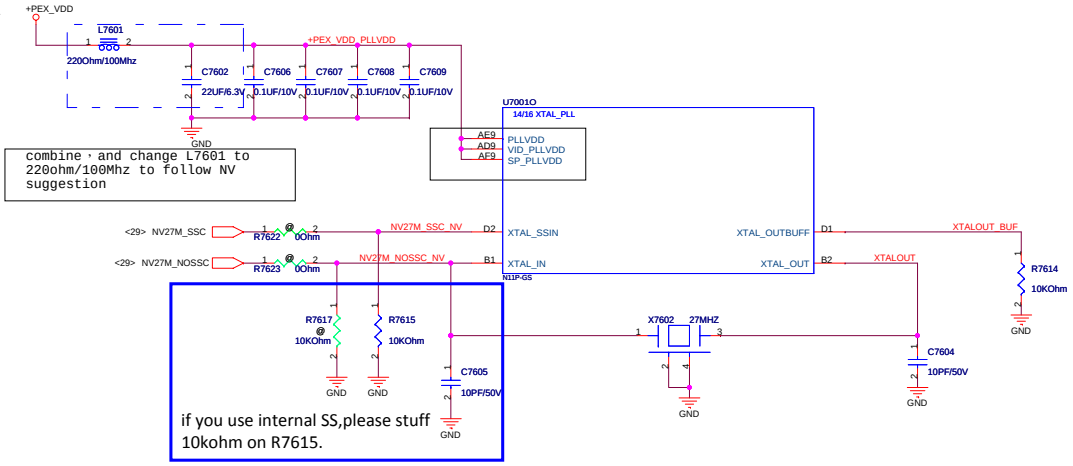


DVI(link D)

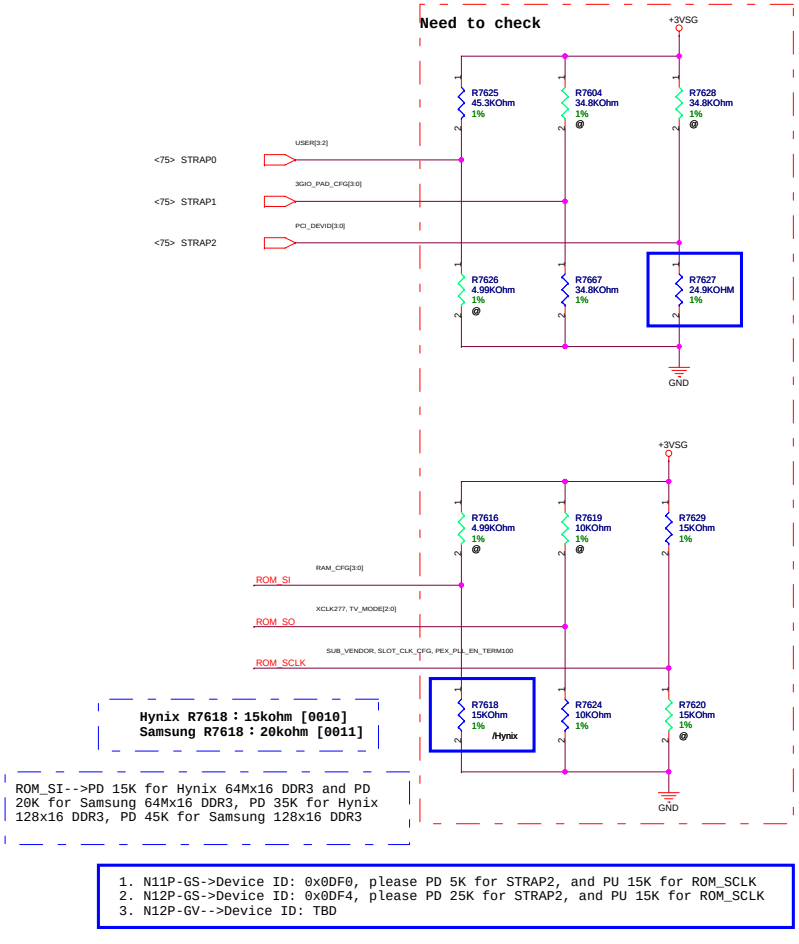


Title : VGA_N11P-GS Main (6)			
ASUSTeK COMPUTER INC. NB3	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 75 of 95		





STRAPPING OPTIONS



	3V3	GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0

USER_BIT0
USER_BIT1
USER_BIT2
USER_BIT3

STRAP1

3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1
3GIO_PADCFG_LUT_ADR2
3GIO_PADCFG_LUT_ADR3

0x0: Desktop default (normal swing) - 5k PD
0x1: Mobile default (low swing) - 10k PD
acc. to //hw/tesla_g98b/manuals/dev_ext_devices.ref

STRAP2

PCI_DEVID_0 — all 4 bits set by HW strapping
PCI_DEVID_1 — 0x0A35 : 30K ohm PD (N11P-GV1)
PCI_DEVID_2
PCI_DEVID_3

ROM_SO

VGA_DEVICE — 0:3D DEVICE; 1: VGA DEVICE(default)
SMB_ALT_ADDR — 0:0x9E(default) — 0x1=10K PD
FB_0BAR_SIZE — 0:256M(default)
XCLK_417 — 0: 277MHZ(Default)

ROM_SI

RAM_CFG_0 — 1GB (8pcs.64Mx16)
RAM_CFG_1 — RAM_CFG[3:0] Definitions
RAM_CFG_2
RAM_CFG_3

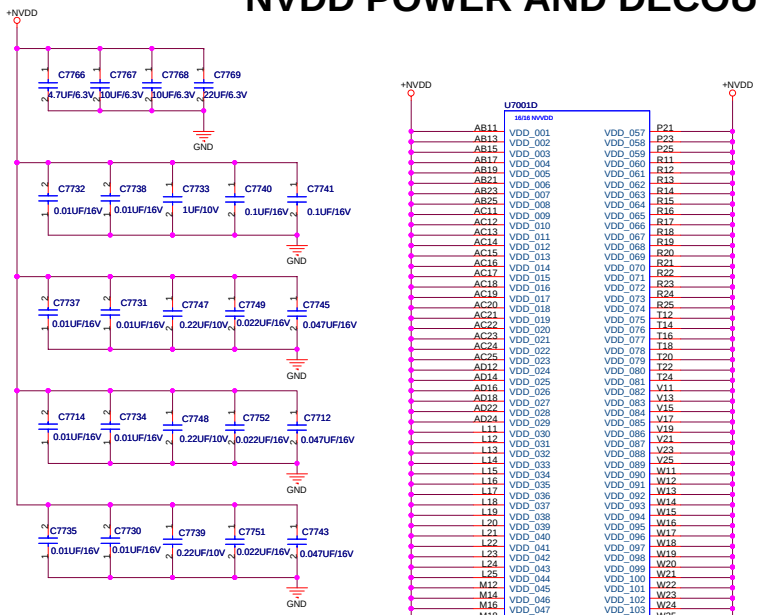
ROM_SCLK

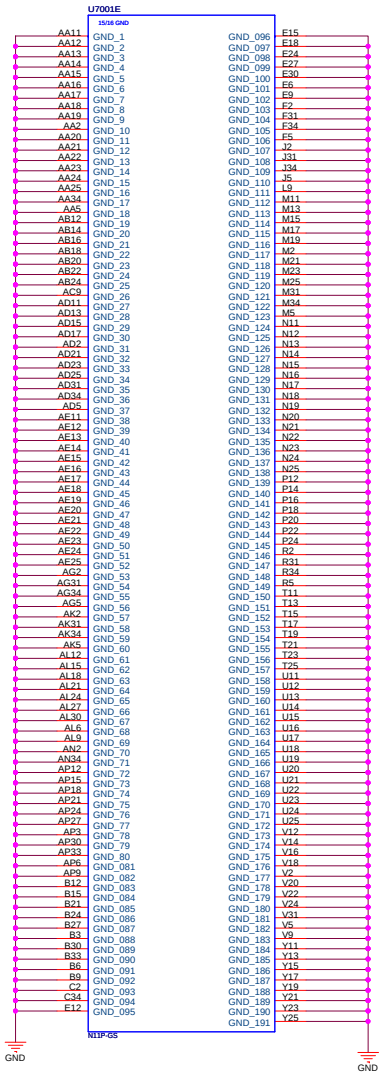
PEX_PLL_EN_TERM — 0: Default
SLOT_CLK_CONFIG — 1: GPU and MCH COMMON REFCLK
SUB_VENDOR — 0: VBIOS ROM is not present, default "1" — 35K PU
PCI_DEVID_4 — 0: 0x0A28(PCDEVID[4]=0) for MP, 0x0A3D(PCDEVID[4]=1 for ER

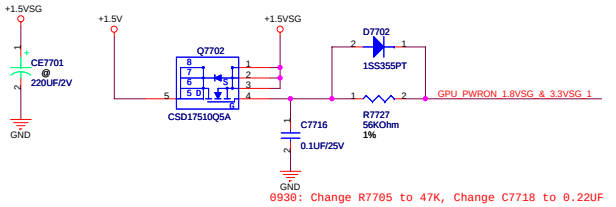
1. N11P-GS->Device ID: 0x0DF0, please PD 5K for STRAP2, and PU 15K for ROM_SCLK
2. N12P-GS->Device ID: 0x0DF4, please PD 25K for STRAP2, and PU 15K for ROM_SCLK
3. N12P-GV-->Device ID: TBD

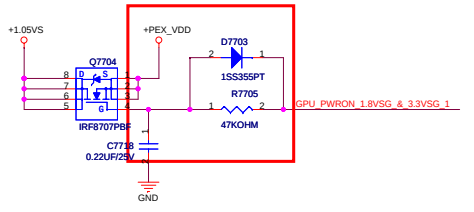
ASUSTeK COMPUTER INC. NB3 | Title : VGA_N11P-GS Main (7) | Engineer: Wish | Size: C | Project Name: N73Sv | Rev: 1.0 | Date: Wednesday, October 13, 2010 | Sheet 76 of 95

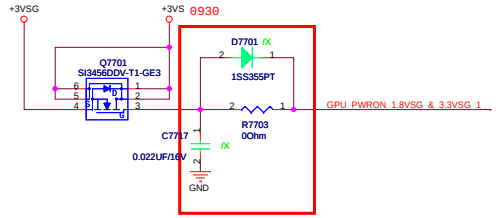
NVDD POWER AND DECOUPLING NVDD GROUND

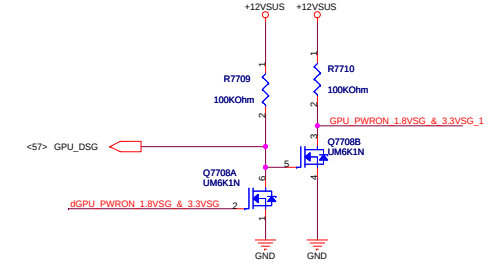


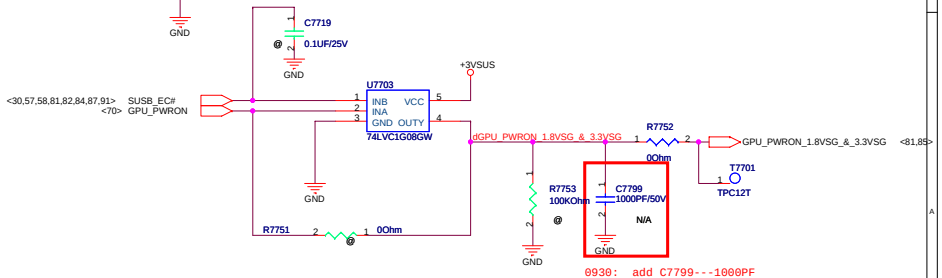












ASUSTeK COMPUTER INC. NB3	Title : VGA_N11P-GS Main (8)	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 77 of 95	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : **	
	Engineer: Wish	
Size: Custom	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 78 of 95	

Rev	Date	Description
1.1	2010/08	(1)Page3 & 20 & 70 ：CPU socket P/N change to 12G011909893; PCH P/N as 02G010027100; GPU P/N change to 02G190018200; change VRAM to Hynix H5TQ1G63DFR-11C & SAMSUNG/K4W1G1646E-HC11 (2)Page3/80 ：link SNB_SKTOCC# to VRM controller (3)Page3 ：reserve 0.01uF(C0335/C0336/C0337) for H_CPUPWRGD/PM_SYNC#/H_SNB_INV# (4)Page3/7 ：un-link XDP_PREQ# to XDP for saving layout space, and add test point on XDP connector side. (5)Page6 ：change +VDDQ power source from +1.5VS to +1.5V, so delete JP0601&JP0602 (6)Page6/80 ：add R0602 serial R & R0605 pull-up R for VR_SVID_ALERT#, and change PR8071 to 0ohm, un-mount PR8063 (7)Page6 ：un-mount CE0601 for factory DFM (8)Page26/27 ：change SL0402 to SL0603 for SL2601/SL2602/SL2603/SL2702/SL2703/SL2708/SL2710/SL2711/SL2712/SL2717/SL2718/SL2719 (9)Page29 ：un-mount Clock Gen. & others interrelated components (10)Page30 : 10.1 change net name from FAN_PWM to FAN0_PWM(page 50) 10.2 DSW_WAKE# changed to no function 10.3 PM_EXTTS#0 changed to no function 10.4 changed net name from RFON_SW# to RF_SW#(page 53) 10.5 OP_SD# changed from GPC5 to GPE0, and VOLUME_LED# changed from GPE0 to GPE3 10.6 THRO_CPU change from GPE5 to GPH1, and changed net name from THRO_CPU to THRO_CPU#,and correct THRO_CPU# control, R0307 changed from 62ohm to 200ohm(page 3); 10.7 PM_SLP_SUS# changed to no function (11)Page33 : delete +3VS power & SL3310 for LAN chip changed to AR8151 (12)Page33 : un-mount C3302 for BUF_PLT_RST# glitch issue (13)Page36 : change C3631 from 1UF/10V to 2.2UF/10V for EA test failed (14)Page36/20 : change DVDD_IO power source to +3VSUS, and then un-mount U2002 & R2028 and stuff R2024 (15)Page37 : ex-change MUTE_POP# & AMP_SHD# MOS (16)Page42 : change the Card Reader chip to AU6437-GDL (17)Page44 : change J4401 to JDEBUG1 for BU request (18)Page46 : unstuff C4602/C4604/C4606 for EA test failed (19)Page68 : change FRESCO FL1000G (D1) TFBGA100 (MP) to FRESCO FL1000G (E0) TFBGA100 (ES) (20)Page66/69 : change CE6602 & CE6932 to c3528 size (21)Page76 : change R7627 value for N12P-GS and pay attention to R7618 value (22)Page77 : change Q7702 to CSD17507Q5A for high Rdson (23)Page77 : change R7703 to 0ohm (24)Page55 : mount stitich Caps EC5513~EC5516, and delete EC5512 (25)Page : change RNX4501、RNX5302、RNX5401、RNX6101、RNX6601、RNX6902、RN6901、RN6902 from 0402 size to 0603 size (26)Page6 ：un-mount CE0601 for factory DFM (27)Page26 : reserve CE2601 for +1.05VS (28)Page68 : add R6801 for GPIO "USB3_SMI#"

Rev	Date	Description
2.0	2010/09/30	1: Page 69, USB 2.0 mount F6903 & R6903てUSB 3.0 mount F6903 & F6904, un-mount R6903 2 : Page 68, unmount R6813 3 : Page 45, Mount R4506, increase Q4502 Vgs 4 : Page 20, Mount R2008 for ME firmware update 5 : Page 85, Change PR8556 to 91K, Change C7716 to 0.22UF and add D8501 for discharge 6 : Page 20, Mount R2008 for ME firmware update 7 : Page 77, Change R7705 to 47K, Change C7718 to 0.22UF 8 : Page 6, R0617, R0618 Change to 1K 9 : Page 82, Change PR8201 to 360K, Change PC8201 to 0.01UF 10 : Page 77, Add C7799---1000PF 11 : Page 58, Change R5805 to 15ohm, reserve C5806 0.1UF 12 : Page 70, Change GPU to N12P山 02G190018204 13 : Page 38, Change J3802 to 12G14030108N 14 : Page 20, Change PCH to 02G010027500 15 : Page 68, Change C6809 to 4.7UF 16 : Page 57, Change R5719 to 100ohm for quick discharge 17 : Page 17,14, add pull up R1701, R1401 18 : Page 44, JDEBUG connector Power change to +3VS 19 : Page 70/77,change U7002 & U7703 from NC7SZ08P5X_NL to 74LVC1G08GW for saving the variety of component. 20 : Page 80, un-stuff PCE8008，mount PCE8007
	2010/10/06	21 : Page 48, For EMI, mount L4801, L4802, L4803, L4804,un-mount RN4801, RN4802, RN4803, RN4804 22 : Page 30, Change GPE1 to dGPU_PD#, Change GPE5 to MEDIA_KEY_LED# 23 : Page 75, Add D7501 for PWRLIMIT#
	2010/10/07	24 : Page 56, For EC +3v reference, mount R5601 R5610 Q5601 Q5602---> change it back (2010/10/11) 25 : Page 30, FOR ITE Suggestion, Change R3007 form 43k to 0ohm 26 : Page 30, Change SL3010 to R3009 0ohm prevent EC version change. 27 : Page 07, un-mount XDP: J0701, R0701, R0702 , R0703, R0704, R0705, RNX0702 28 : Page 30, add battery discharge power limit circuit
	2010/10/09	29 : Page 06, change +1.5V to +1.5VS for energy star 30 : Page 42, Reserve R4218 (+3VS) for energy star 31 : Page 31, SL3101 change to R3101 330 OHM for energy star 32 : Page 56, change R5620 R5613 to 1k for energy star 32 : Page 68, Reserve +3VS for USB3.0 for energy star and remove JP6801 JP6802 JP6803
	2010/10/11	33 : Page 60, Change C6002 to 4.7UF, C6004 to 1UF, PR6000 to 200k for power request to slow raise and fall time 34 : Page 91, Change PQ9113 to 07G005B19010 for large current 35 : Page 37, Reserve C3725 C3726 C3727 C3728 FOR EMI
	2010/10/12	36 : Page 61, Reserve R6102 For Energy Satr 37 : Page 45, Add R4513 to change J4502 PIN5 from GND_AUDIO to GND 38 : Page 60, mount C6002 C6003 for POWER suggestion 39 : update power circuit for BOM 40 : Page 37 Page 03, unmount R3715 Q3704 C3711 R0303
	2010/10/13	41 : Page 69, reserve R6905 for leakage, If USB3.0 choose +3VS for Energy Star, mount F6905, un-mount F6904 42 : Page 03, Mount Q0302 R0335 For DRAMPWROK quick discharge 43 : Page 69, Change F6904 F6905 from 07G012200130 to 07G014200020 43 : Page 37, For EMI request, Change jump to bead (L3703, L3704, L3705, L3706)

ASUSTeK COMPUTER INC. NB4

Title : change list

Engineer: Wish

Size	Project Name	Rev
C	N73Sv	1.0

Date: Wednesday, October 13, 2010 Sheet 79 of 95

IMVP7 CPU VCORE REGULATOR

PR8090 = 500hm for OC
PR8090 = 0Ohm for Normal

PC8094 close to CPU

PR8078 & PC8019 close to IC

Layout Note:
VR_SVID_DATA, VR_SVID_ALERT#, VR_SVID_CLK, tracke is 5mil, distance is 15mil

Layout Note:
place PR8071(43ohm),PR8063(75ohm) put the middle of CPU & VR
place PR8069(130ohm),PR8068(54.9ohm) close to VR

Close to VCORE Hot_Spot

105C and 93C

Close to +VGFX Hot_Spot

PU8003 UP6262M8-B2

PU8001 close to PU8000

Close to Phase 1 Inductor PL8001

Ocp = 168A

PR8044 2.61KOhm
PR8043 11KOhm
PC8044 0.068UF/10V
PC8043 0.47UF/10V
PR8042 1.4KOHM r0402
PR8045 10KOHM r0603
PC8045 0.1UF/16V
PC8006 330PF/50V
PR8046 100Ohm

PR8089 = 500hm for OC
PR8089 = 0Ohm for Normal

PC8093 close to CPU

PU8000 ISL95831HRTZ-T

OCP = 40A
Imax = 33A

LL=3.9mohm

Imax = 91A

LL = 1.97 mohm

Close to Hi-MOS

(Range: 0.3V~1.3V)
MAX:41.0A
RMS:33.0A

PL8004 0.56UH 10x10x4mm 950mil
PL8003 0.36UH 10x10x4mm 950mil
PL8002 0.36UH 10x10x4mm 950mil
PL8001 0.36UH 10x10x4mm 950mil

PQ8001 CSD17507Q5A
PQ8002 CSD17510Q5A
PQ8003 CSD17510Q5A
PQ8004 CSD17507Q5A
PQ8005 CSD17510Q5A
PQ8006 CSD17510Q5A
PQ8007 CSD17507Q5A
PQ8008 CSD17510Q5A
PQ8009 CSD17510Q5A
PQ8010 CSD17507Q5A
PQ8011 CSD17510Q5A
PQ8012 CSD17510Q5A
PQ8013 CSD17507Q5A
PQ8014 CSD17507Q5A

PU8001 ISL6208CRZ

PU8003 UP6262M8-B2

PU8000 ISL95831HRTZ-T

PJ8010 PJ8011 PJ8012 3MM_OPEN_5MIL

PT8000 PT8001 PT8002 PT8003 PT8011 PT8012 PT8013 PT8015 PT8016 PT8017 PT8018 PT8019 PT8020 PT8021 PT8022 PT8023 PT8024 PT8025 PT8026 PT8027 PT8028 PT8029 PT8030 PT8031 TPC28T

1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =3.9A

2. Ripple Current:
Iripple=7A

3. Voltage & Current:
0.3V~1.3V : 55A

4.ripple voltage:
Ipeak=(vin-vo)*D/(L*Fsw)=8.8A
ESR=9/3=3mohm
V=26.4mV

5. Frequency:
Rfset = (T -0.29) *2.65
Frequency= 300KHZ

For 35W CPU:
PR8014 = 5.62K for Vboot=0V/49A; PR8053 = 9.53K for 105C/25A
For 45W CPUs:
PR8014 = 590Ohm for Vboot=0V/91A; PR8053 = 6.65K for 105C/33A

<Variant Name>

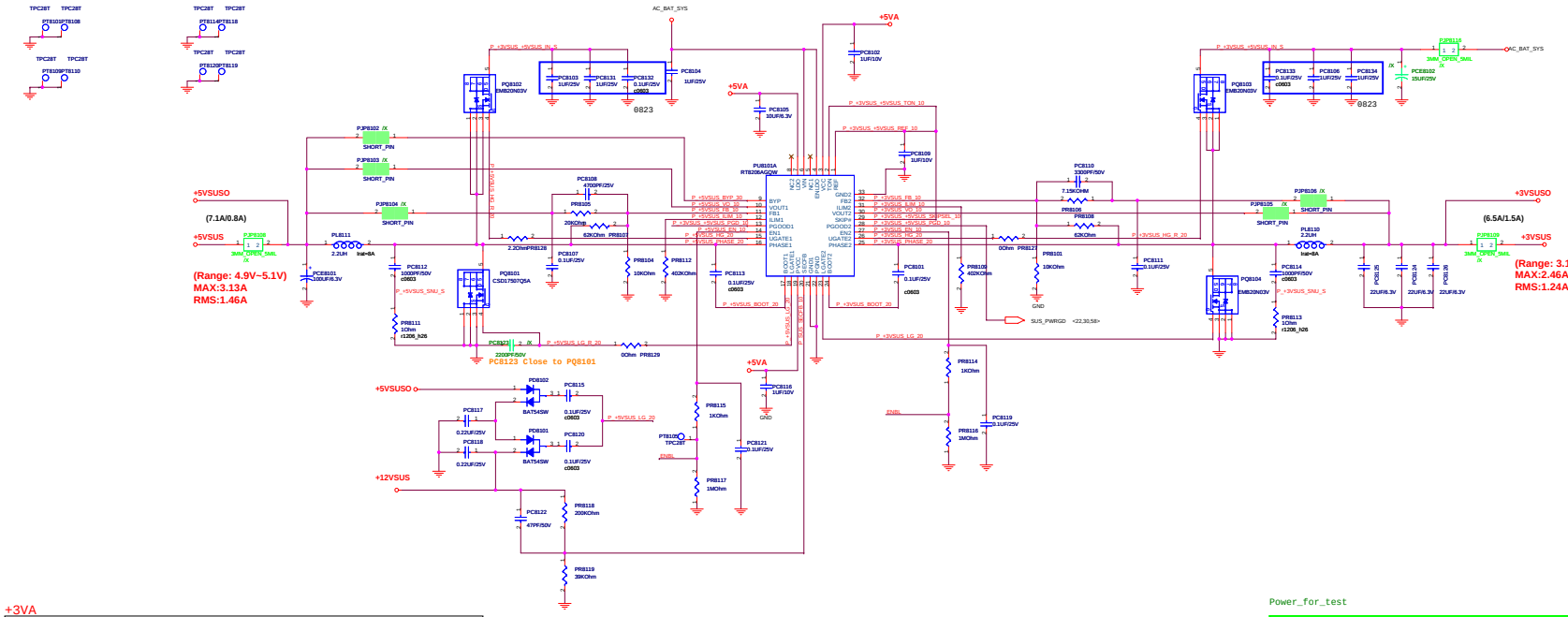
ASUSTeK COMPUTER INC. NB1

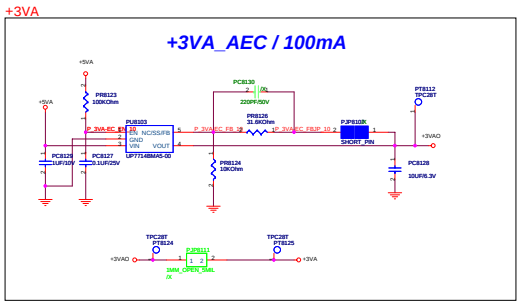
Title : +VCORE

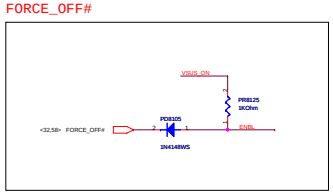
Engineer: VC

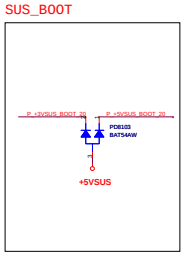
Size	Project Name	Rev
Custom	U53S	1.0

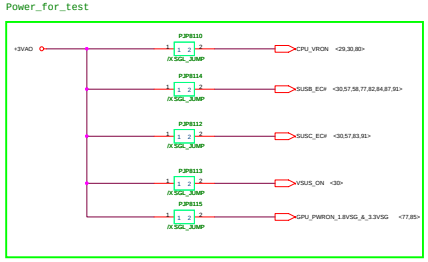
Date: Wednesday, October 13, 2010 Sheet 80 of 92











Power information +5VSUS

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =2.082A

2. Ripple Current:

I rip =1.012A
I spec=2.5A ×1
pcs

3. Dynamic:

Ipeak=(vin-vo)*D/(L*Fsw)=2.58A
ESR / 1 pcs =15 mohm
△V =38.72mV

1. Voltage & Current:

+5VSUS=5V@3.13A

2. Frequency:

fosc=300KHz

3. OCP:

Set PR8112=402Kohm
Iocp=14A

Power information +3VSUS

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =1.375A

2. Ripple Current:

I rip =1.152A
I spec=2.5A ×1
pcs

3. Dynamic:

Ipeak=(vin-vo)*D/(L*Fsw)=1.55A
ESR / 1 pcs =15mohm
△V =23.25mV

1. Voltage & Current:

+3VSUS=3.3V@2.46A

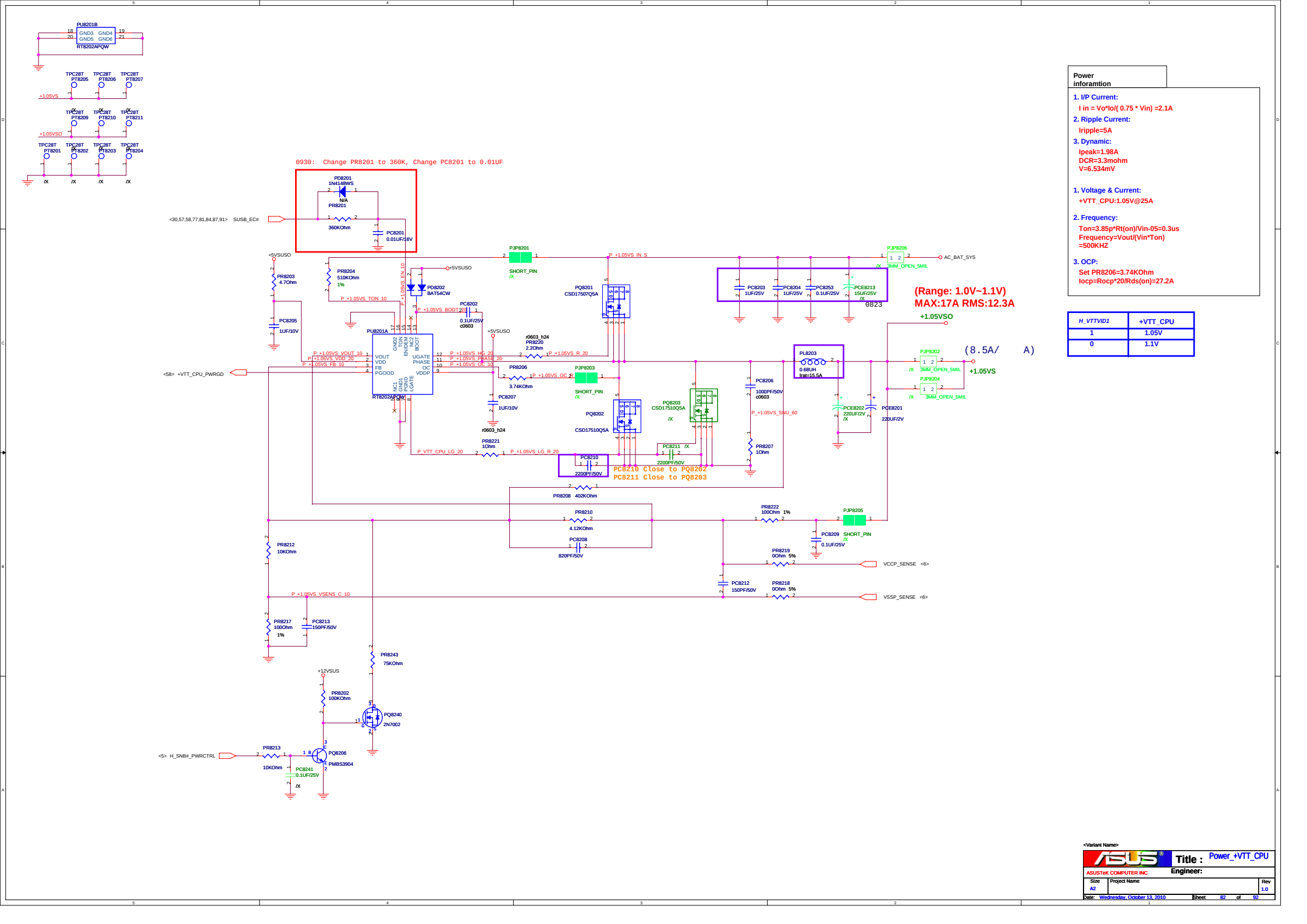
2. Frequency:

fosc=375KHz

3. OCP:

Set PR8109=402Kohm
Iocp=8.74A

ASUSTeK Computer INC.	Title : Power +5SUS&+3VSUS&+12VSUS		
	Engineer: ZHI-KUN_LIU		
Size	Project Name		Rev
Custom	M61JV		1.0
Date: Wednesday, October 14, 2015		Sheet 33 of 50	



Power inforamtion

1. I/P Current:

I in = Vo*Io/(0.75 * Vin) =2.1A

2. Ripple Current:

Iripple=5A

3. Dynamic:

Ipeak=1.98A
DCR=3.3mohm
V=6.534mV

1. Voltage & Current:

+VTT_CPU:1.05V@25A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:

Set PR8206=3.74KOhm
Iocp=Rocp*20/Rds(on)=27.2A

H_VTTVID1	+VTT_CPU
1	1.05V
0	1.1V

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VTT_CPU

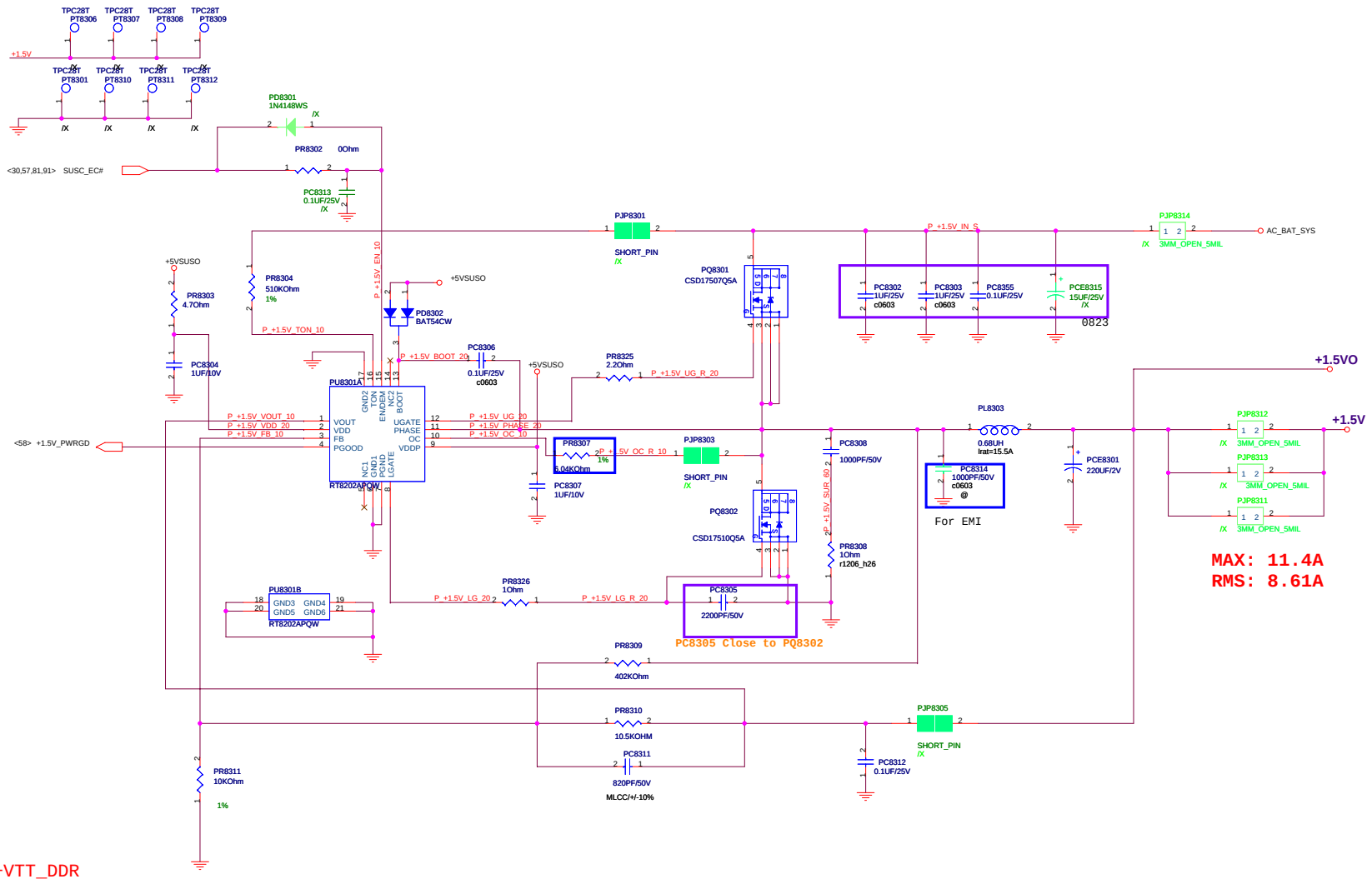
Engineer:

Size	Project Name	Rev
A2		1.0

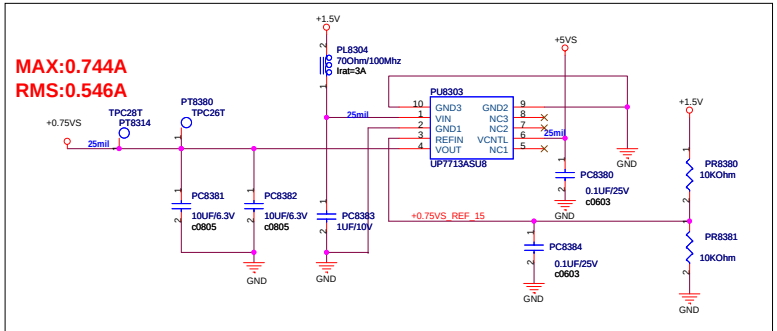
Date: Wednesday, October 13, 2010 Sheet 82 of 92

Power information

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =3.6A
2. Ripple Current:
   Iripple=5A
3. ripple voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=2.07A
   DCR=10mohm
   V=20.7mV
1. Voltage & Current:
   1.5V: 16.45A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8307=4.7kohm
   Iocp=Rocp*20/Rds(on)=17A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A



+VTT_DDR



<Variant Name>

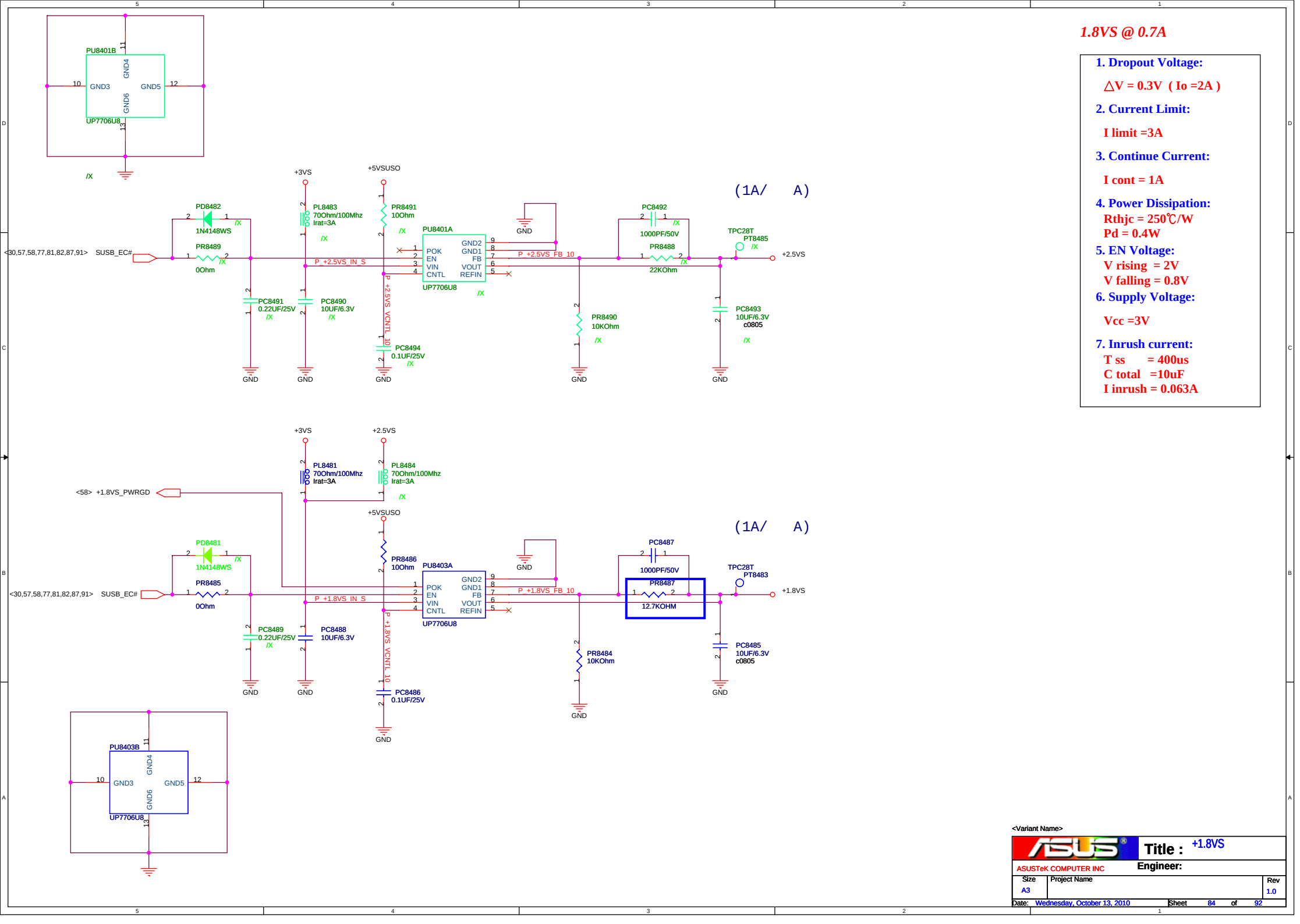
ASUSTeK COMPUTER INC

Title : +1.5V

Engineer:

Size	Project Name	Rev
C		1.0

Date: Wednesday, October 13, 2010 Sheet 83 of 92



1.8VS @ 0.7A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =3A

3. Continue Current:

I cont = 1A

4. Power Dissipation:

Rthjc = 250℃/W
Pd = 0.4W

5. EN Voltage:

V rising = 2V
V falling = 0.8V

6. Supply Voltage:

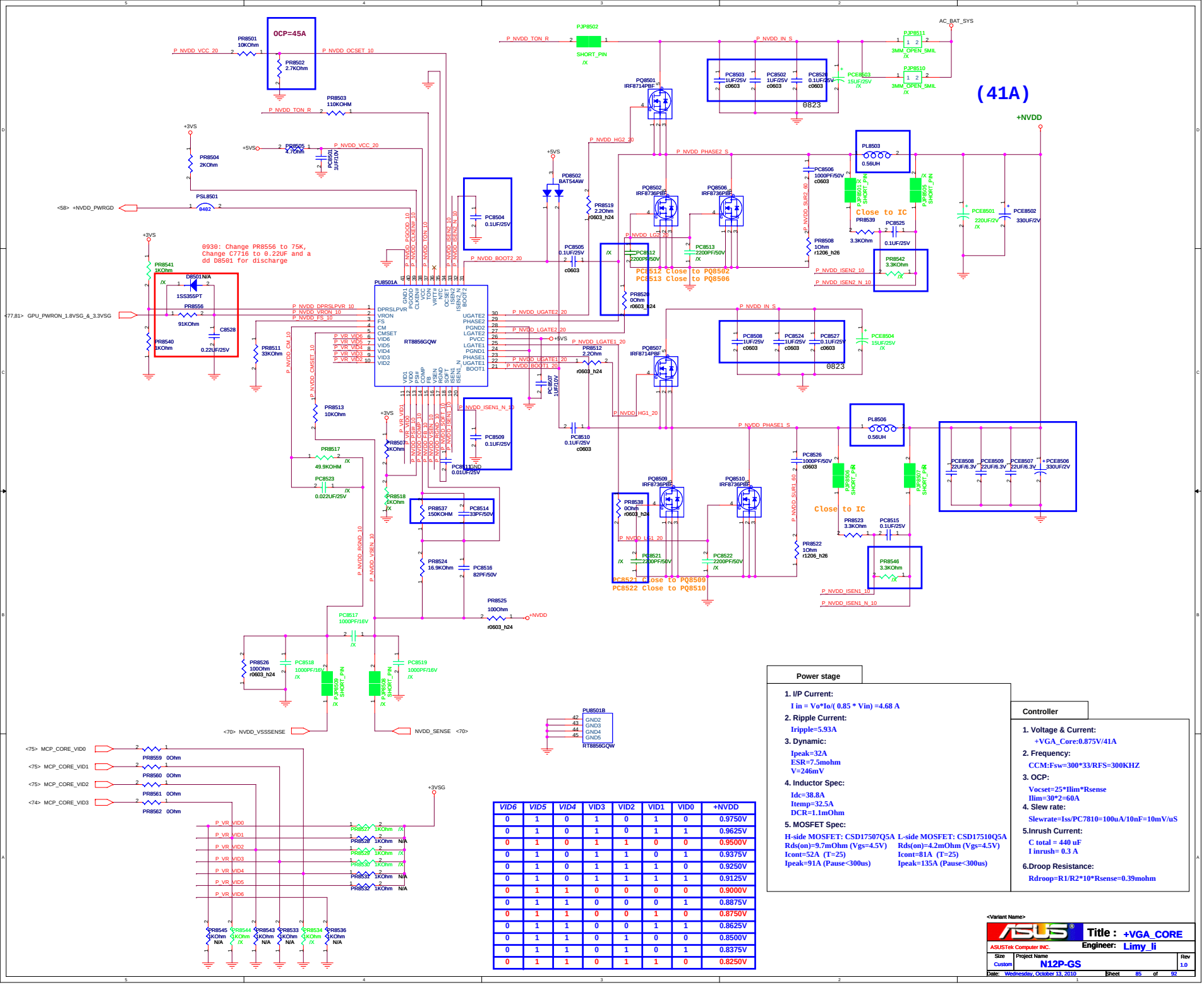
Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush = 0.063A

<Variant Name>

ASUSTeK COMPUTER INC	Title : +1.8VS	
	Engineer:	
Size: A3	Project Name	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 84 of 92	



Power stage

1. I/P Current:
   I in = Vo*Io/(0.85 * Vin) =4.68 A
2. Ripple Current:
   Iripple=5.93A
3. Dynamic:
   Ipeak=32A
   ESR=7.5mohm
   V=246mV
4. Inductor Spec:
   Idc=38.8A
   Itemp=32.5A
   DCR=1.1mOhm
5. MOSFET Spec:
   H-side MOSFET: CSD17507Q5A
   Rds(on)=9.7mOhm (Vgs=4.5V)
   Icont=52A (T=25)
   Ipeak=91A (Pause<300us)
   L-side MOSFET: CSD17510Q5A
   Rds(on)=4.2mOhm (Vgs=4.5V)
   Icont=81A (T=25)
   Ipeak=135A (Pause<300us)

Controller

1. Voltage & Current:
   +VGA_Core:0.875V/41A
2. Frequency:
   CCM:Fsw=300*33/RFS=300KHZ
3. OCP:
   Vocset=25*Ilim*Rsense
   Ilim=30*2=60A
4. Slew rate:
   Slewrate=Iss/PC7810=100uA/10nF=10mV/uS
5. Inrush Current:
   C total = 440 uF
   I inrush= 0.3 A
6. Droop Resistance:
   Rdroop=R1/R2*10*Rsense=0.39mohm

VID6	VID5	VID4	VID3	VID2	VID1	VID0	+NVDD
0	1	0	1	0	1	0	0.9750V
0	1	0	1	0	1	1	0.9625V
0	1	0	1	1	0	0	0.9500V
0	1	0	1	1	0	1	0.9375V
0	1	0	1	1	1	0	0.9250V
0	1	0	1	1	1	1	0.9125V
0	1	1	0	0	0	0	0.9000V
0	1	1	0	0	0	1	0.8875V
0	1	1	0	0	1	0	0.8750V
0	1	1	0	0	1	1	0.8625V
0	1	1	0	1	0	0	0.8500V
0	1	1	0	1	0	1	0.8375V
0	1	1	0	1	1	0	0.8250V

<Variant Name>

Title : +VGA_CORE

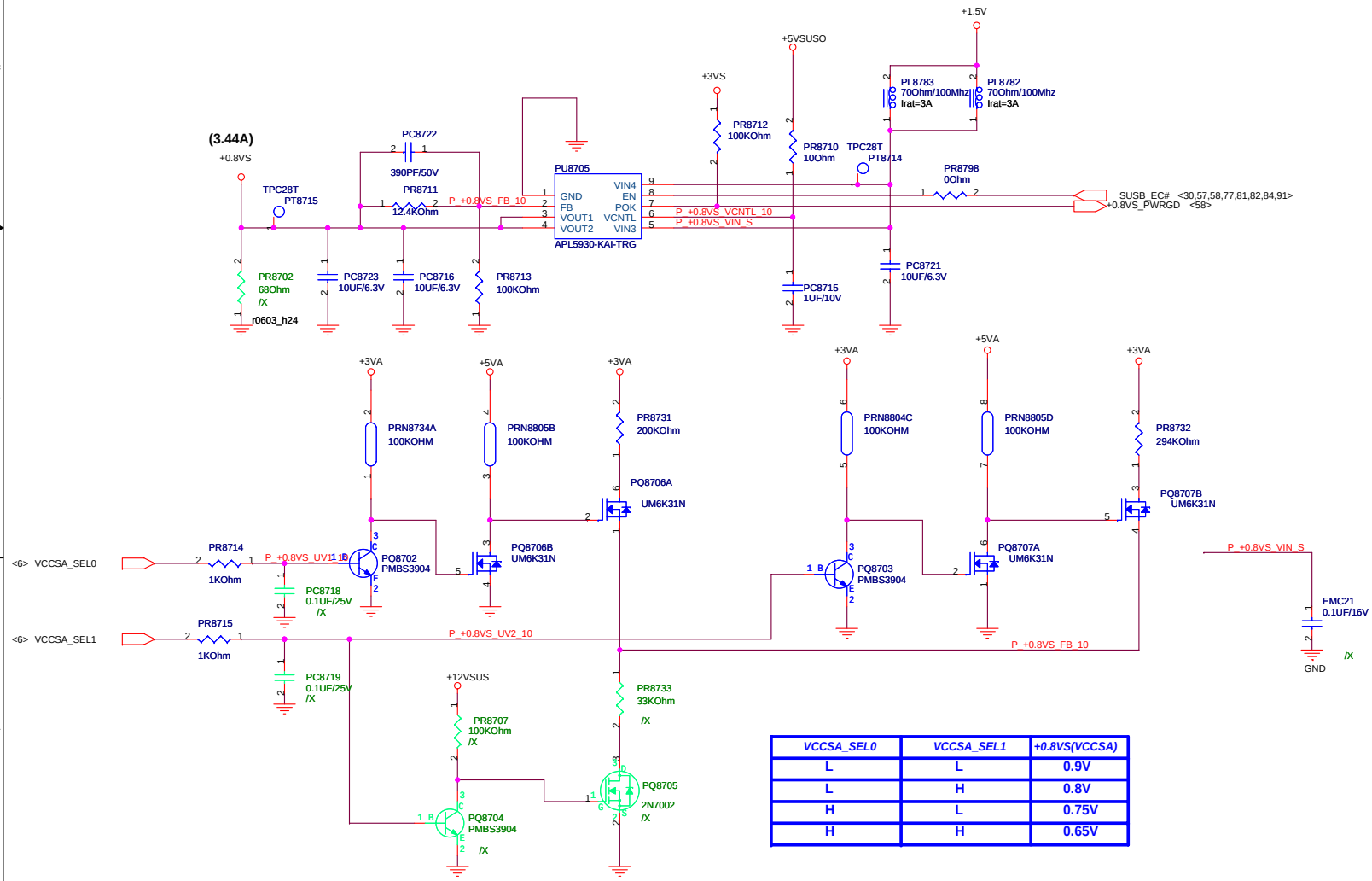
ASUSTek Computer INC.

Engineer: Limy_li

Size	Project Name	Rev
Custom	N12P-GS	1.0

Date: Wednesday, October 13, 2010 Sheet 85 of 92

ASUSTeK COMPUTER INC. NB3	Title :	
	Engineer:	
Size: A2	Project Name: Design_IP	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 86 of 92	



VCCSA_SEL0	VCCSA_SEL1	+0.8VS(VCCSA)
L	L	0.9V
L	H	0.8V
H	L	0.75V
H	H	0.65V

<Variant Name>

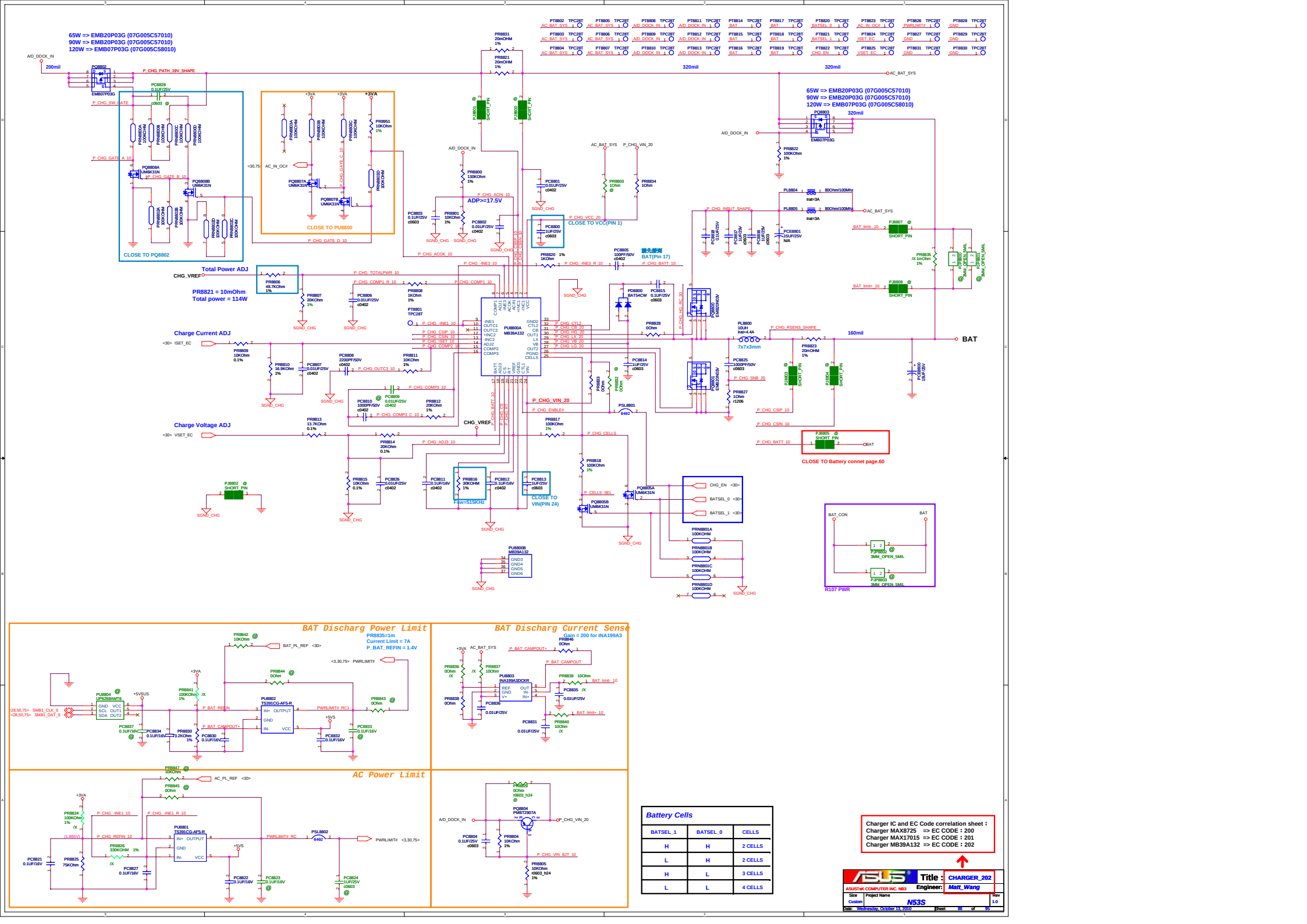
Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom		1.0

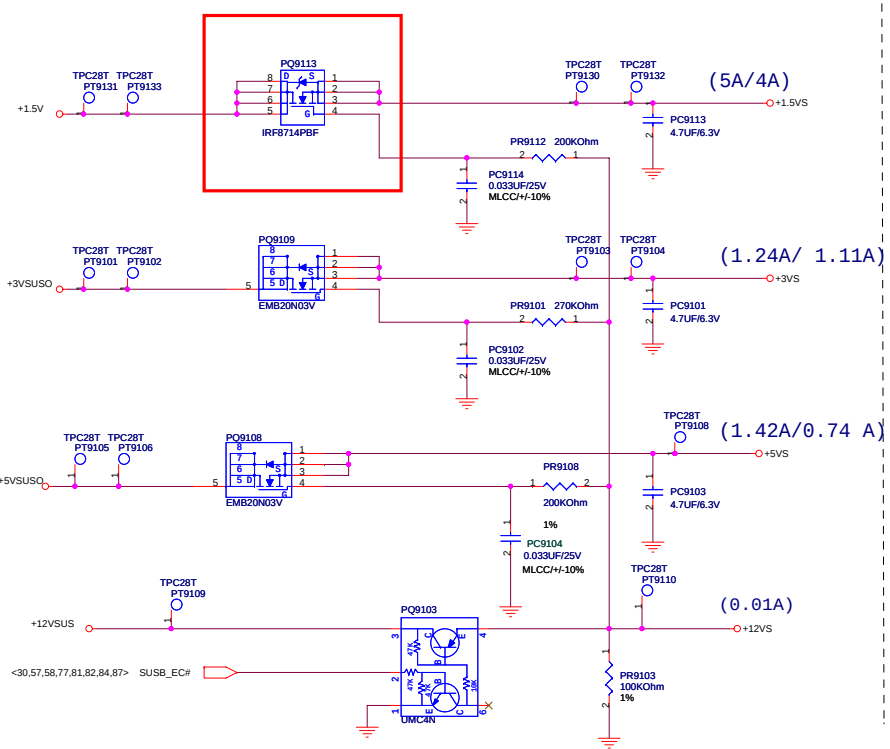
Date: Wednesday, October 13, 2010 Sheet 87 of 92


65W => EMB20P03G (07G005C57010)
90W => EMB20P03G (07G005C57010)
120W => EMB07P03G (07G005C58010)
A/D_DOCK_IN
200mil
P_CHG_PATH_19V_SHAPE
320mil
AC_BAT_SYS
CLOSE TO PQ8802
CLOSE TO PU8800
ADP>=17.5V
CLOSE TO VCC(PIN 1)
BAT(Pin 17)
Total Power ADJ
CHG_VREF
PR8821 = 10mOhm
Total power = 114W
Charge Current ADJ
ISET_EC
Charge Voltage ADJ
VSET_EC
CHG_VREF
P_CHG_VIN_20
160mil
BAT
CLOSE TO Battery connet page.60
R107 PWR
BAT Discharg Power Limit
PR8835=1m
Current Limit = 7A
P_BAT_REFIN = 1.4V
BAT Discharg Current Sense
Gain = 200 for INA199A3
AC Power Limit
Battery Cells
BATSEL_1
BATSEL_0
CELLS
H H 2 CELLS
L H 2 CELLS
H L 3 CELLS
L L 4 CELLS
Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202
Title : CHARGER_202
Engineer: Matt_Wang
ASUSTeK COMPUTER INC. NB3
Project Name N53S
Rev 1.0
Date: Wednesday, October 13, 2010
Sheet 88 of 95

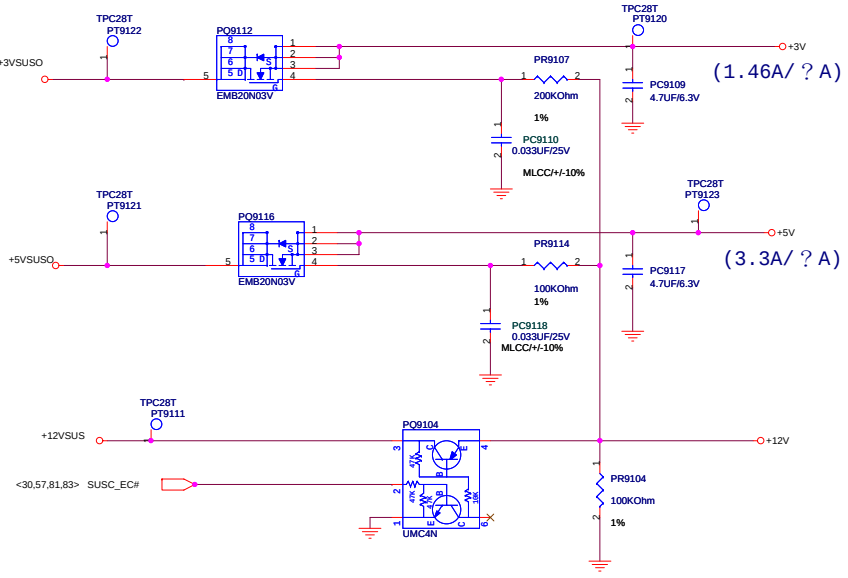
Title :	
ASUSTeK COMPUTER INC. NB3	Engineer:
Size: Custom	Project Name: Design_IP
Rev: 1.0	
Date: Wednesday, October 13, 2010	Sheet 89 of 92

ASUSTeK COMPUTER INC. NB3	Title :
	Engineer:
Size: A	Project Name: Design_IP
	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 90 of 92

SUSB#_PWR POWER



SUSC#_PWR POWER



<Variant Name>

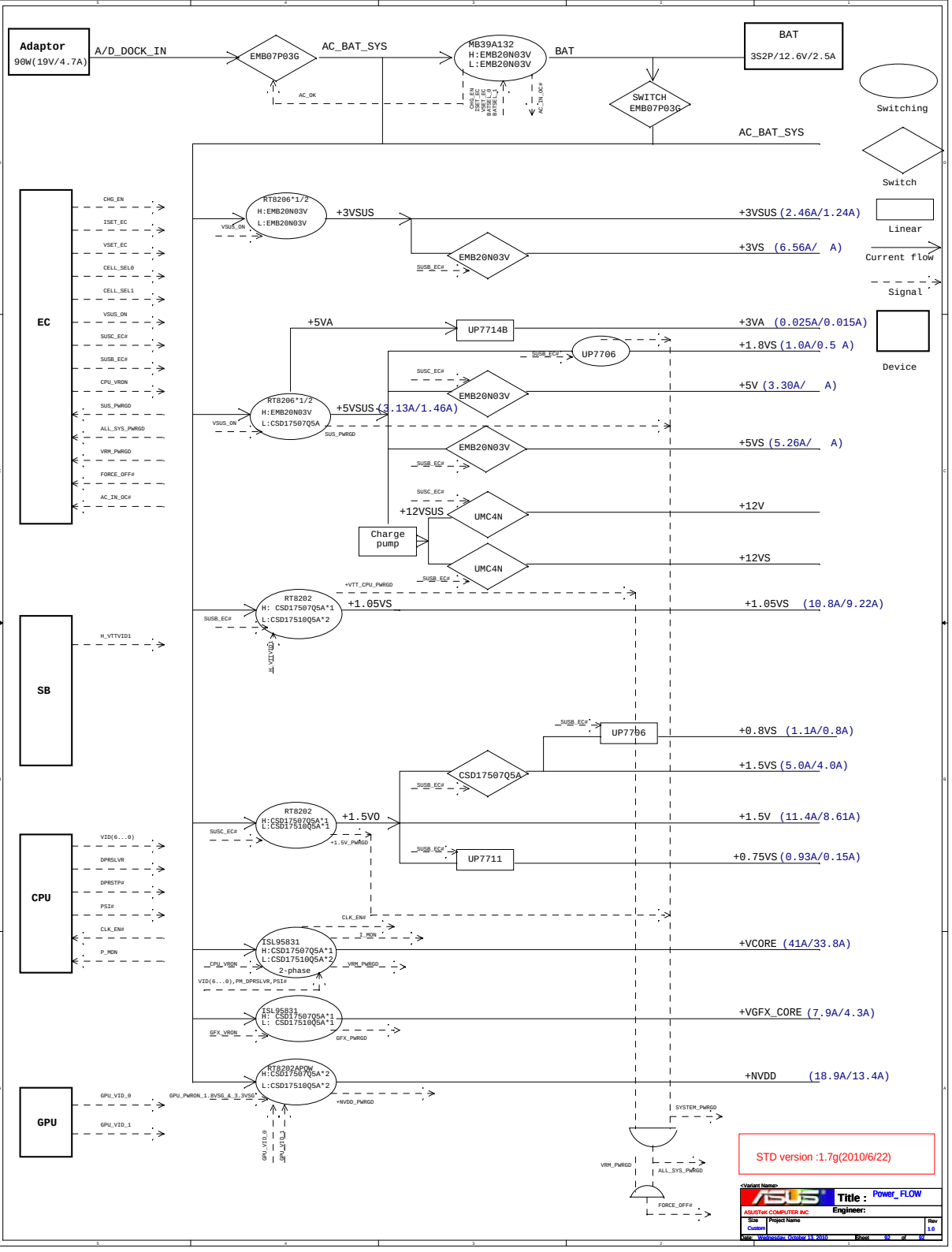
ASUSTeK COMPUTER INC

Title : Power_Load_Switch

Engineer:

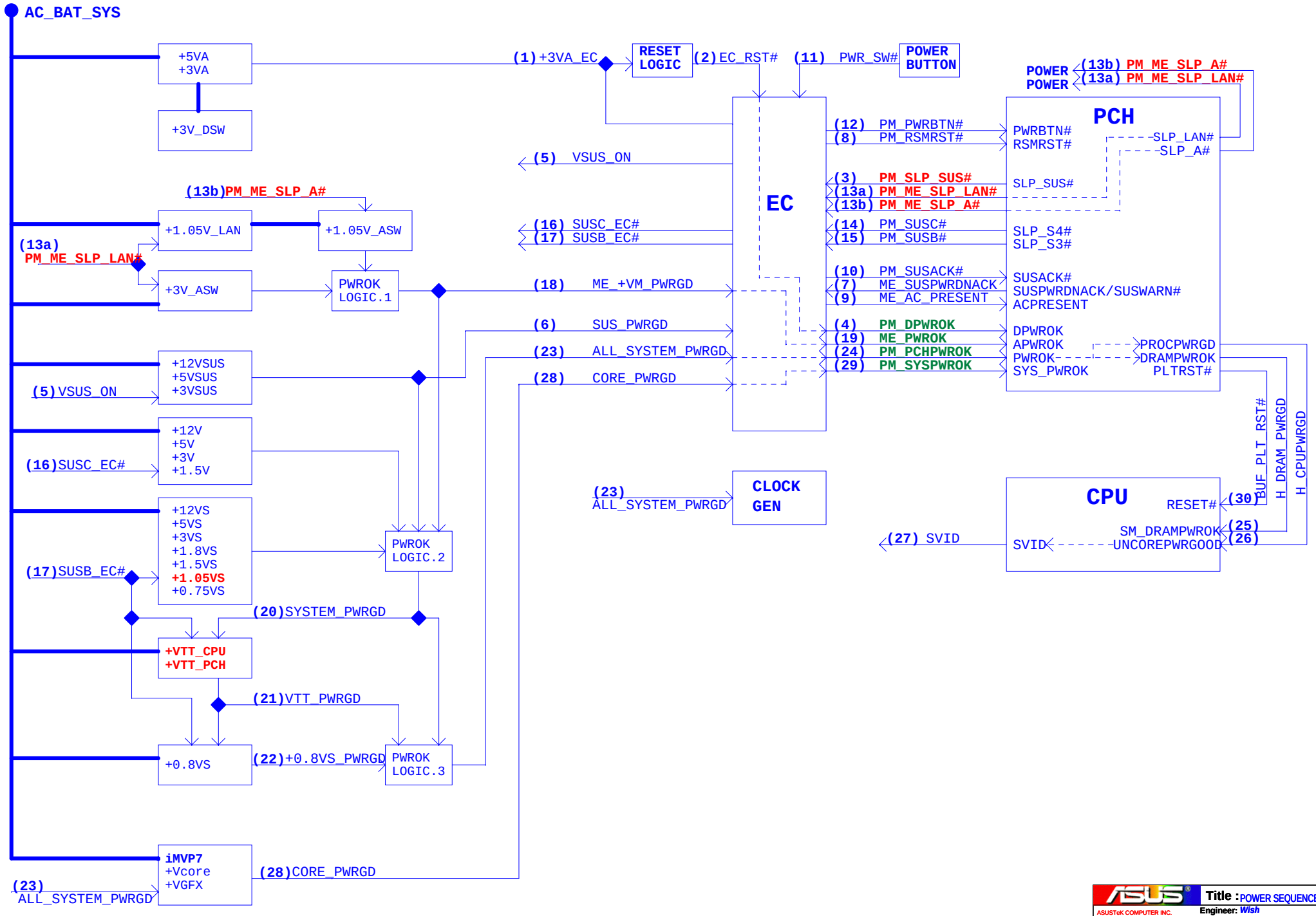
Size	Project Name	Rev
Custom		1.0

Date: Wednesday, October 13, 2010 Sheet 91 of 92


Adaptor
90W(19V/4.7A)
A/D_DOCK_IN
EMB07P03G
AC_BAT_SYS
MB39A132
H:EMB20N03V
L:EMB20N03V
BAT
BAT
3S2P/12.6V/2.5A
SWITCH
EMB07P03G
AC_BAT_SYS
Switching
Switch
Linear
Current flow
Signal
Device
EC
SB
CPU
GPU
CHG_EN
ISET_EC
VSET_EC
CELL_SEL0
CELL_SEL1
VSUS_ON
SUSC_EC#
SUSB_EC#
CPU_VRON
SUS_PWRGD
ALL_SYS_PWRGD
VRM_PWRGD
FORCE_OFF#
AC_IN_OC#
H_VTTVID1
VID(6...0)
DPRSLVR
DPRSTP#
PSI#
CLK_EN#
P_MON
GPU_VID_0
GPU_VID_1
RT8206*1/2
H:EMB20N03V
L:EMB20N03V
+3VSUS
+3VSUS (2.46A/1.24A)
EMB20N03V
+3VS (6.56A/ A)
+5VA
UP7714B
+3VA (0.025A/0.015A)
UP7706
+1.8VS (1.0A/0.5 A)
+5V (3.30A/ A)
RT8206*1/2
H:EMB20N03V
L:CSD17507Q5A
+5VSUS (3.13A/1.46A)
+5VS (5.26A/ A)
+12VSUS
Charge pump
UMC4N
+12V
+12VS
RT8202
H: CSD17507Q5A*1
L:CSD17510Q5A*2
+1.05VS
+1.05VS (10.8A/9.22A)
UP7706
+0.8VS (1.1A/0.8A)
CSD17507Q5A
+1.5VS (5.0A/4.0A)
RT8202
H:CSD17507Q5A*1
L:CSD17510Q5A*1
+1.5VO
+1.5V (11.4A/8.61A)
UP7711
+0.75VS (0.93A/0.15A)
ISL95831
H:CSD17507Q5A*1
L:CSD17510Q5A*2
2-phase
+VCORE (41A/33.8A)
ISL95831
H: CSD17507Q5A*1
L: CSD17510Q5A*1
+VGFX_CORE (7.9A/4.3A)
RT8202APQW
H:CSD17507Q5A*2
L:CSD17510Q5A*2
+NVDD (18.9A/13.4A)
SYSTEM_PWRGD
VRM_PWRGD
ALL_SYS_PWRGD
FORCE_OFF#
STD version :1.7g(2010/6/22)
Title : Power_FLOW
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name
Rev: 1.0
Date: Wednesday, October 13, 2010
Sheet 92 of 92

AC-IN Mode

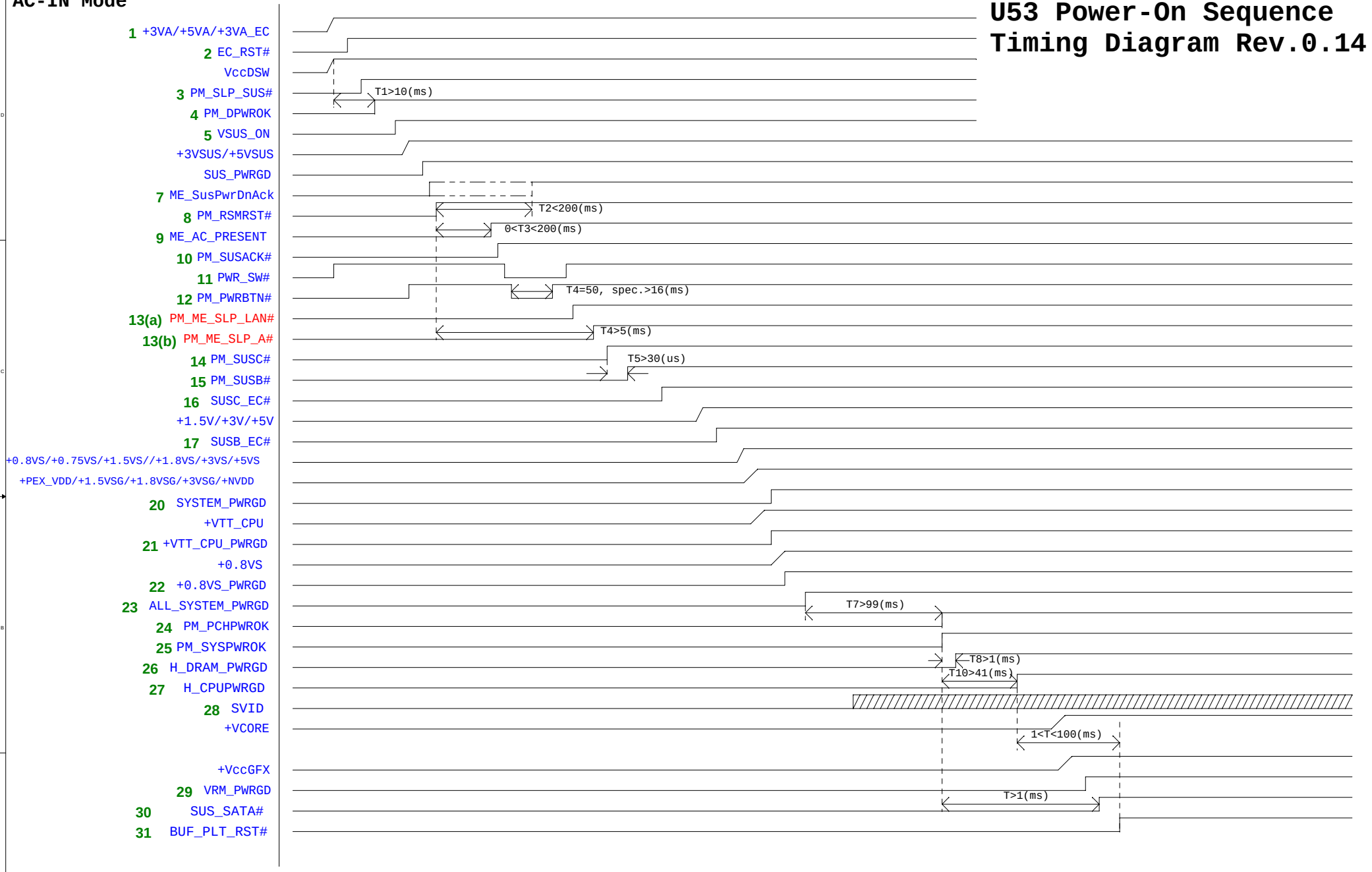
U53 Power On Sequence Diagram Rev.0.14



ASUSTeK COMPUTER INC.	Title : POWER SEQUENCE	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 93 of 95	

AC-IN Mode

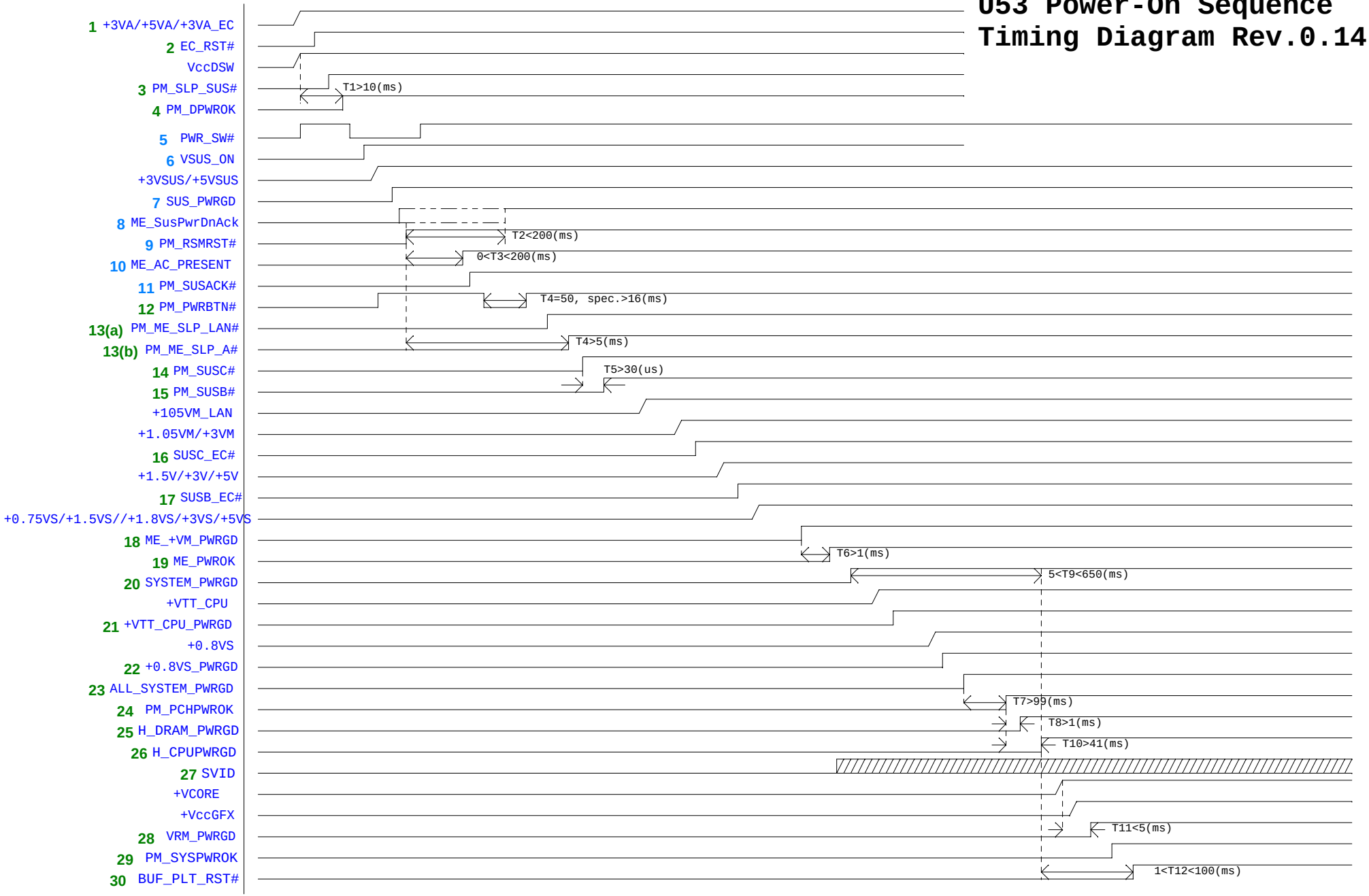
U53 Power-On Sequence Timing Diagram Rev.0.14



ASUSTeK COMPUTER INC.	Title : Power On Timing	
	Engineer: Wish	
Size: C	Project Name: N73Sv	Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 94 of 95	

DC-IN Mode

U53 Power-On Sequence Timing Diagram Rev.0.14



ASUSTeK COMPUTER INC.	Title : Power On Timing		
	Engineer: Wish		
Size: C	Project Name: N73Sv		Rev: 1.0
Date: Wednesday, October 13, 2010	Sheet 95 of 95		