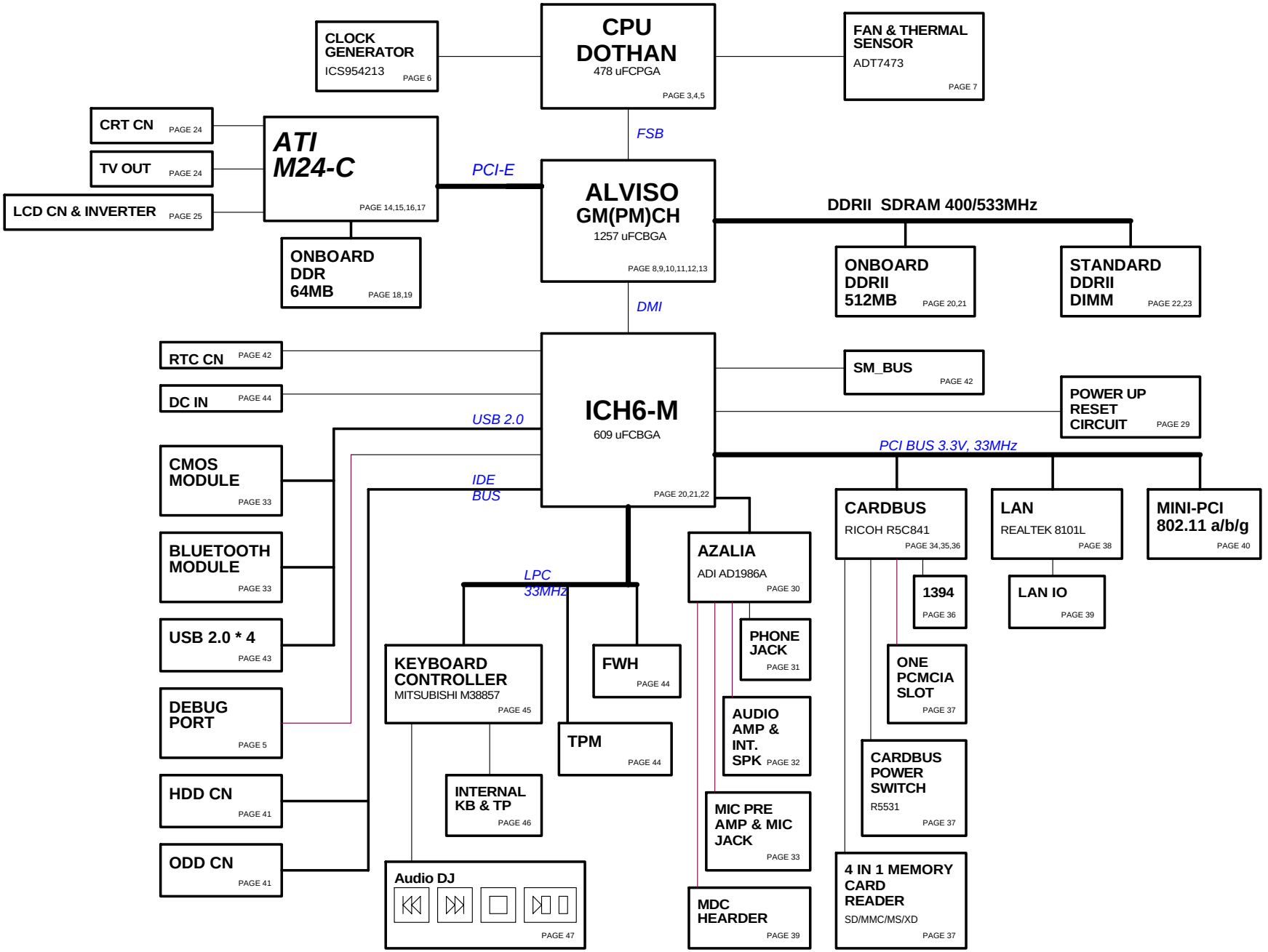
DOTHAN/ALVISO-GM(PM)/ATI M24 BLOCK DIAGRAM

SUB-BOARD

- INSTANT KEY BOARD
- AUDIO DJ BOARD
- MIC BOARD

POWER

- VCORE PAGE 48
- SYSTEM 3VO/5VO PAGE 49
- 1.2V/1.5V/1.8V/1.05V PAGE 50
- 1.5VA/0.9VS PAGE 51
- BATLOW/SD# PAGE 52
- CHARGE PAGE 53
- BAT CON PAGE 54
- PIC16C54 PAGE 55
- LOAD Switch PAGE 56
- VGA VCORE PAGE 57



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME : <Doc>
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DESIGN ENGINEER :

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35	CardBus RICOH 5C841/PCI_A		
36	CardBus RICOH 5C841/PCI_C		
37	Cardbus & CardReader & PwrSw		
38	LAN RealTek-RTL8101L		
39	LAN IO & MDC		
40	MiniPCI		
41	HDD CN & CDROM CN		
42	SM_BUS & RTC CN		
43	4*USB2.0 Conn		
44	DCIN JACK & FWH & TPM		
45	Keyboard Controller (M3885)		
46	LEDs & Internal KB & TP		
47	Audio DJ		
48	VCORE		
49	SYSTEM		
50	2.5V & 1.5V & 1.8V & 1.05V		
51	1.5VA & DDR2 & 3VALWAYS_P		
52	BATLOW/SD#		

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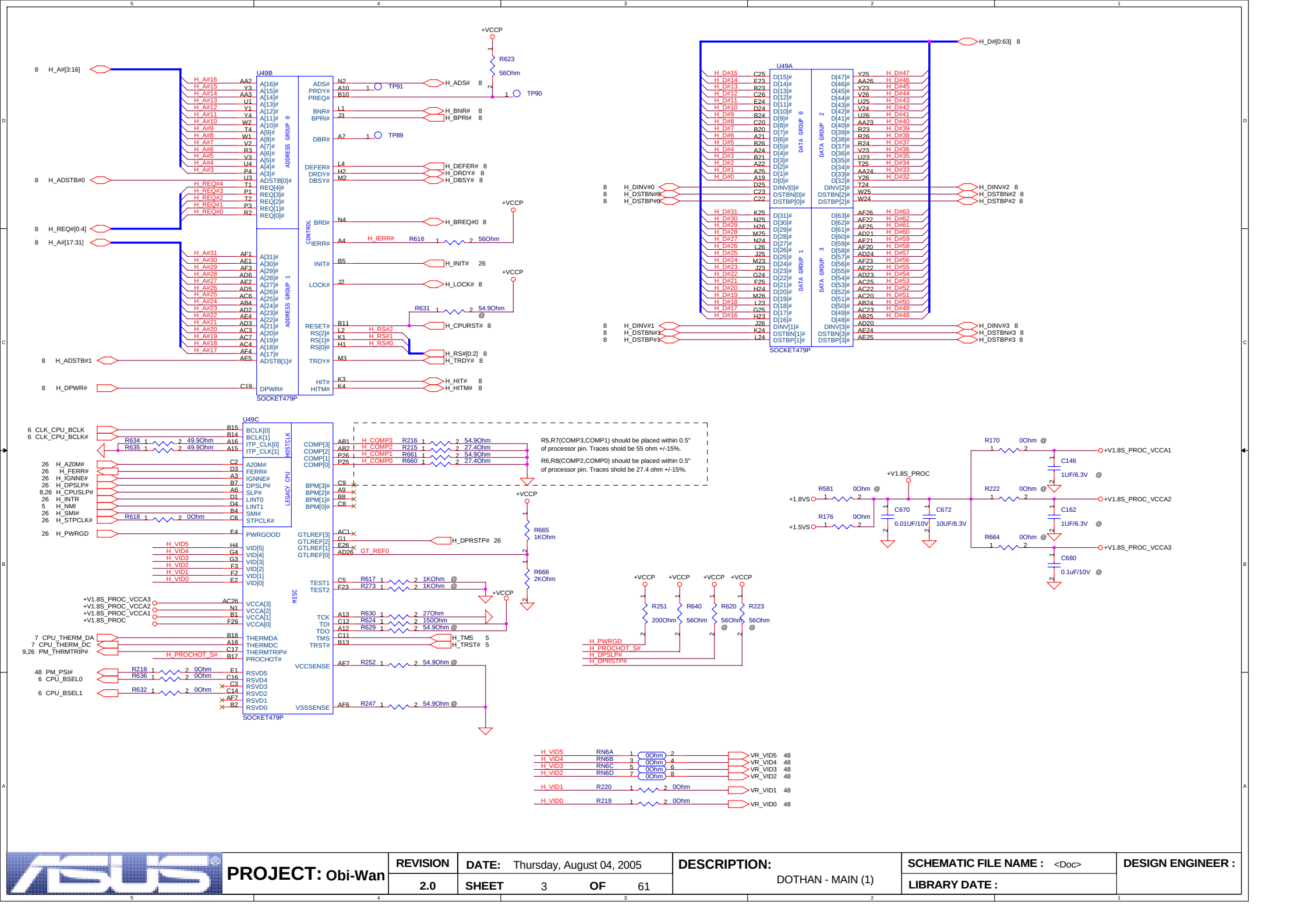

PROJECT: Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** DOTHAN - MAIN (1)	**SCHEMATIC FILE NAME :** <Doc>
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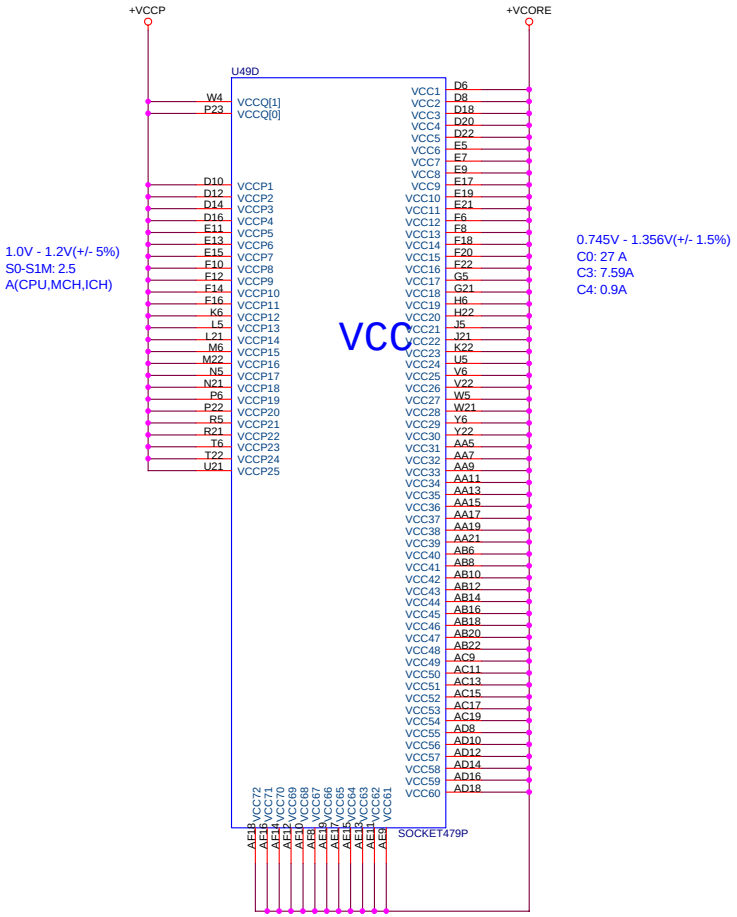
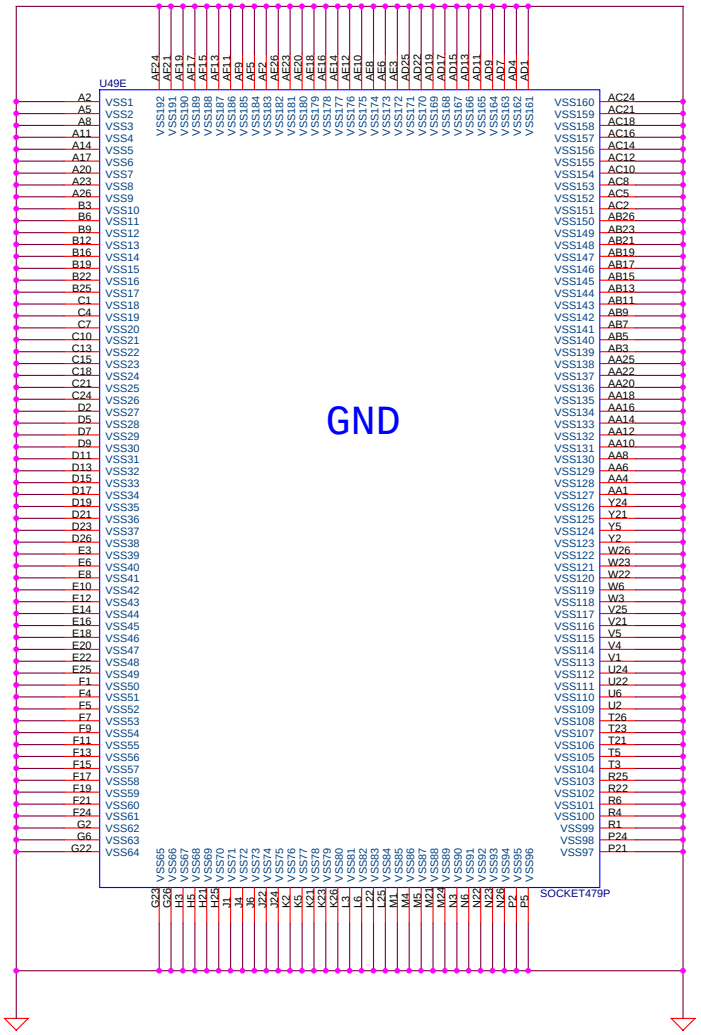
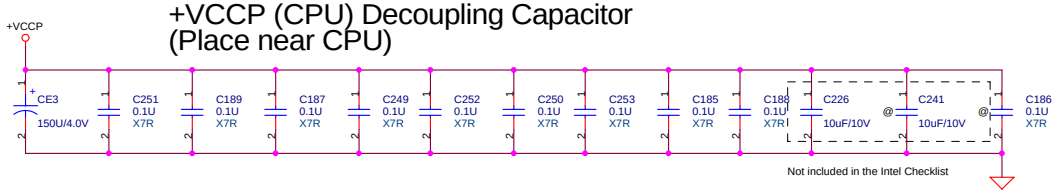
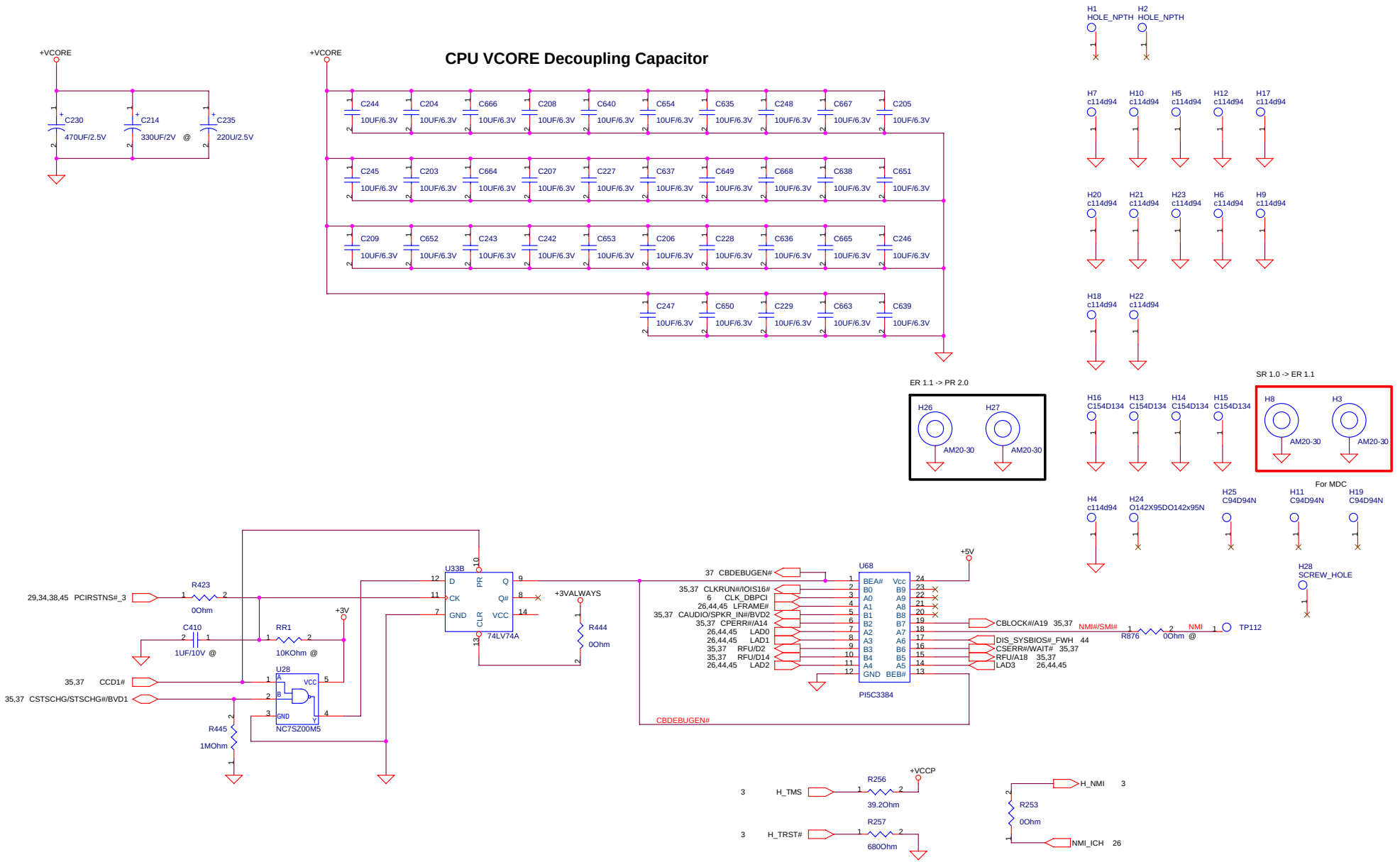
DESIGN ENGINEER :





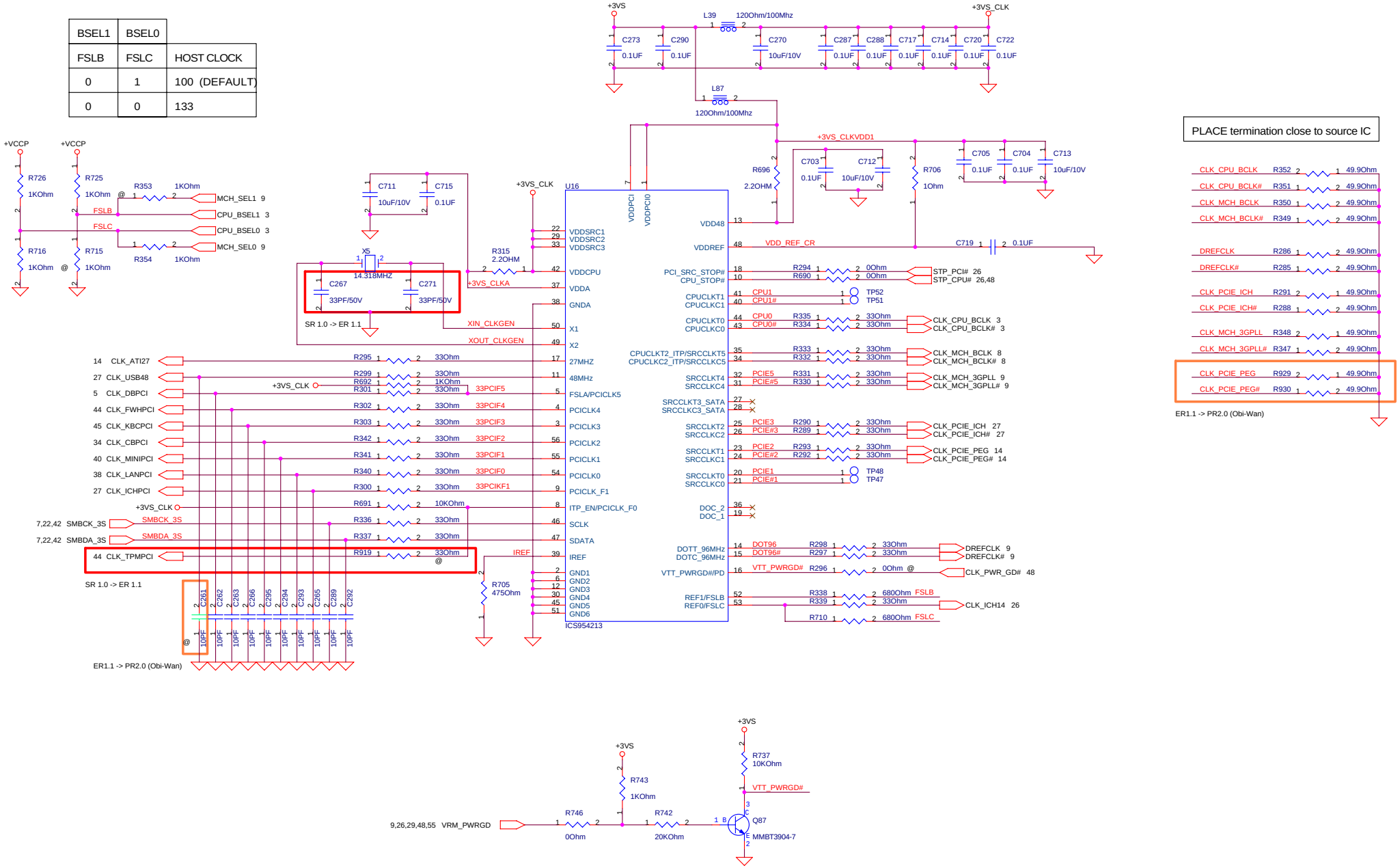


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: DOTHAN - POWER&GND (2)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 4 OF 61		LIBRARY DATE :	



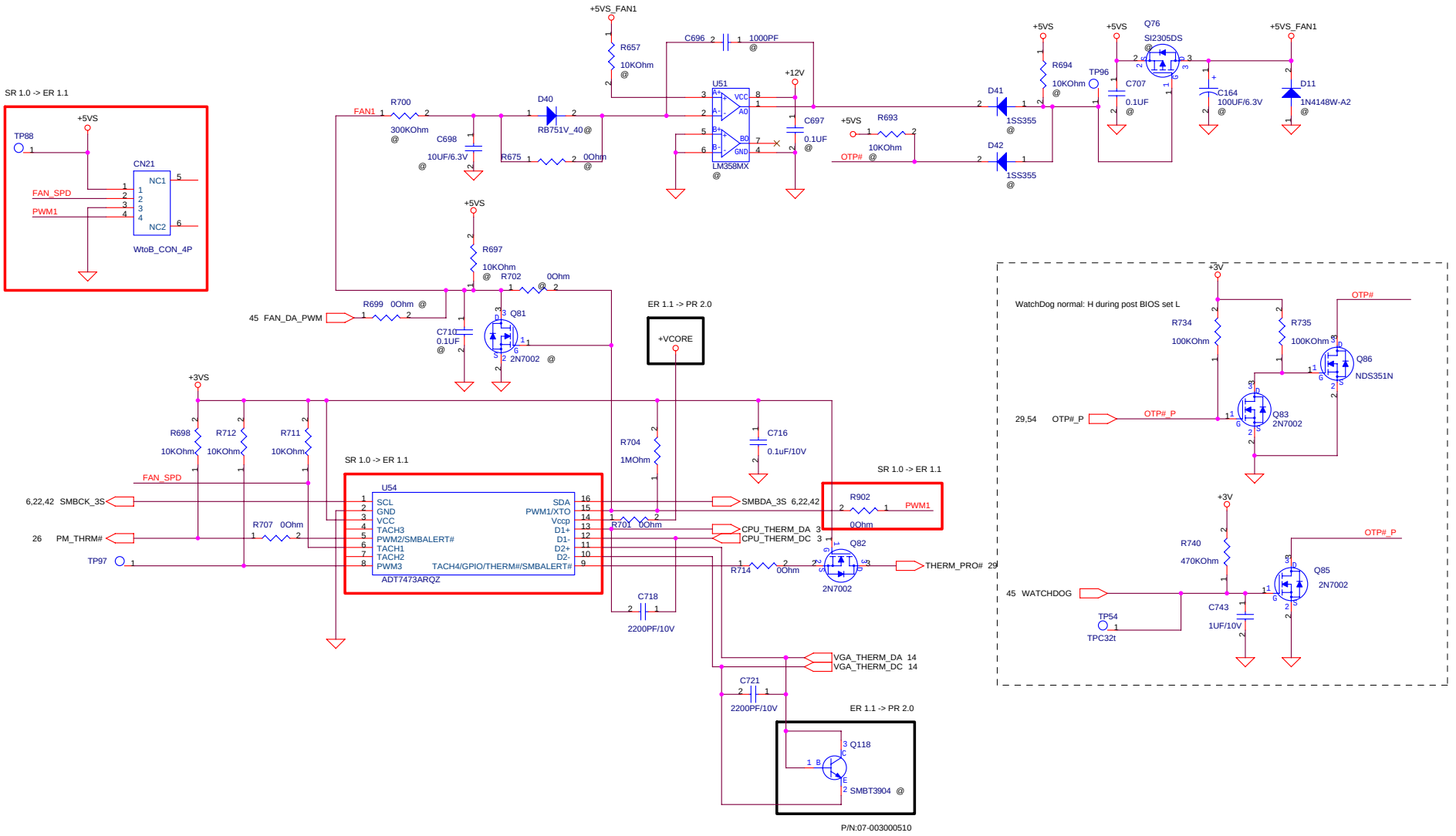
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: CPU CAPS& DEBUG CARD	SCHEMATIC FILE NAME : <Doc>
		SHEET 5 OF 61		LIBRARY DATE :
				DESIGN ENGINEER :

BSEL1	BSEL0	
FSLB	FSLC	HOST CLOCK
0	1	100 (DEFAULT)
0	0	133

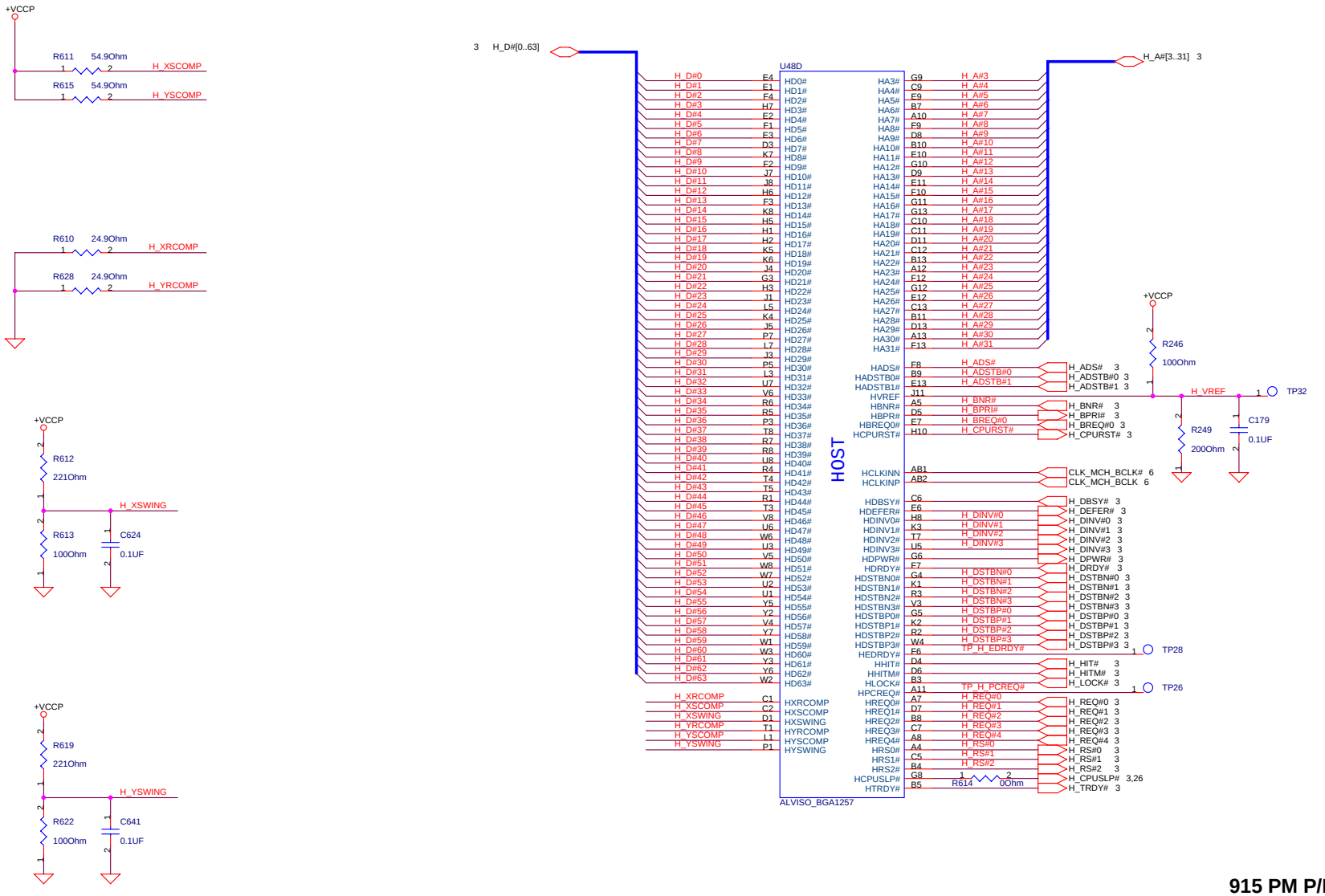


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: CLOCK GENERATOR	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 6 OF 61		LIBRARY DATE :	

FAN



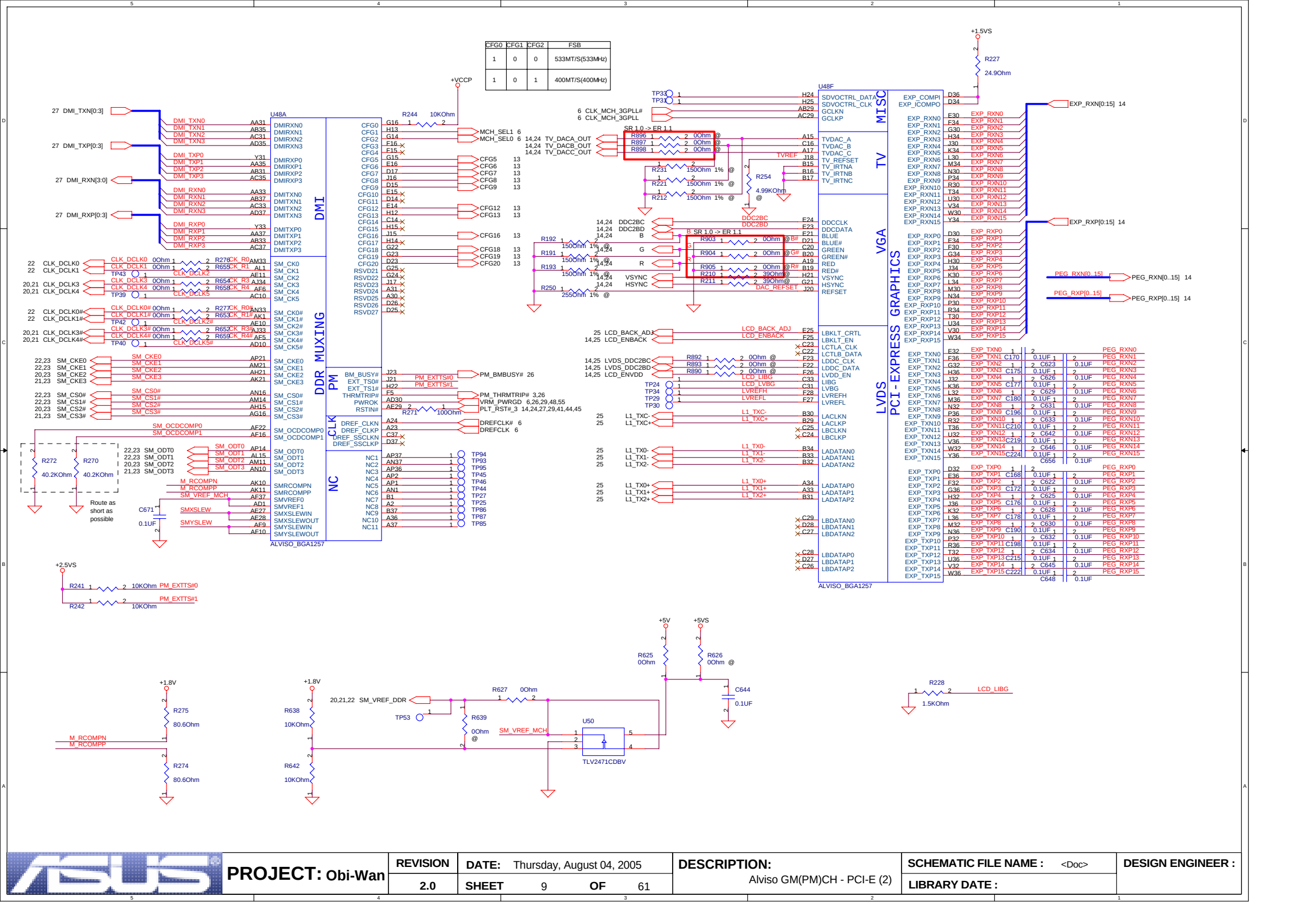
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: FAN & THERMAL SENSOR	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 7 OF 61		LIBRARY DATE :	



915 PM P/N is 02-010000791HQ

915 GM P/N is 02-010002640

PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: Alviso GM(PM)CH - HOST (1)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 8 OF 61		LIBRARY DATE :	



PROJECT: Obi-Wan	REVISION: 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: Alviso GM(PM)CH - PCI-E (2)
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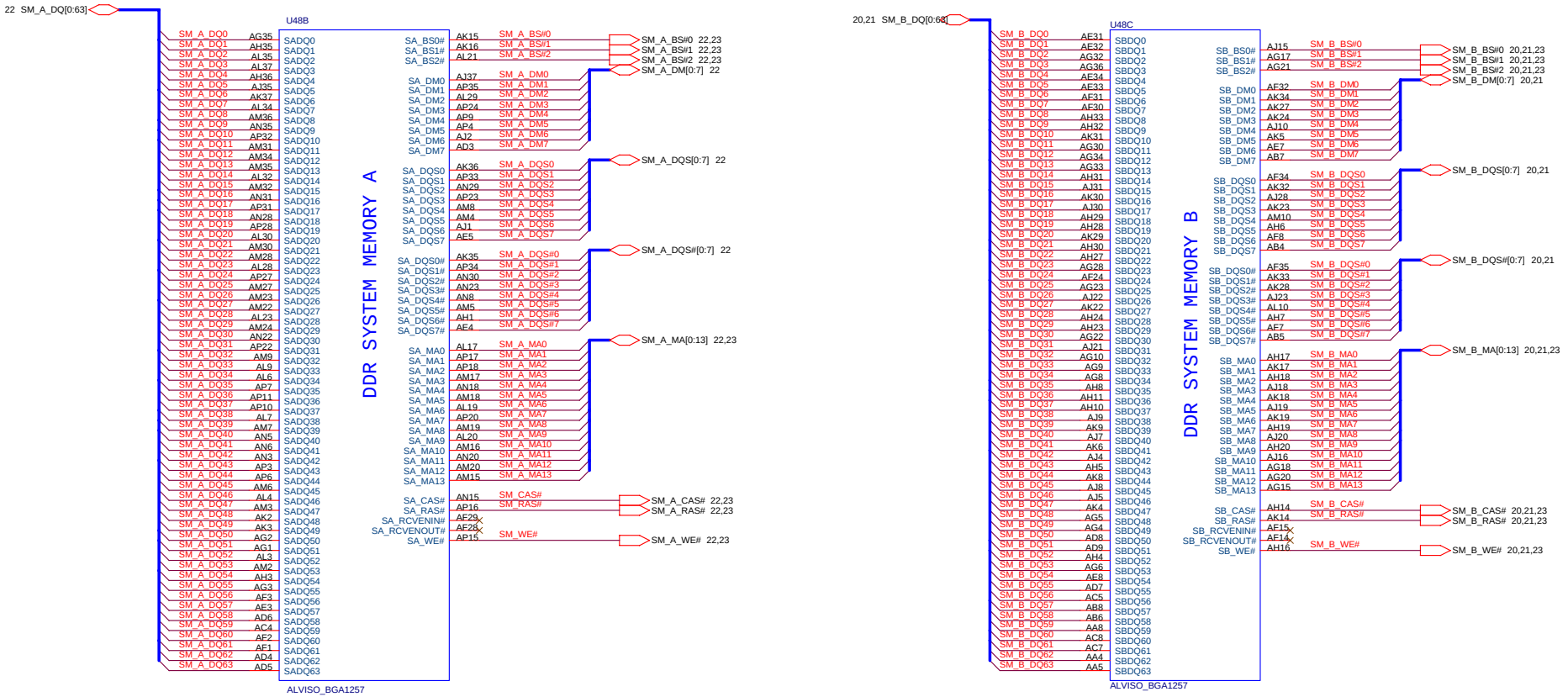

PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: Alviso GM(PM)CH - DDR (3)	SCHEMATIC FILE NAME : <Doc>
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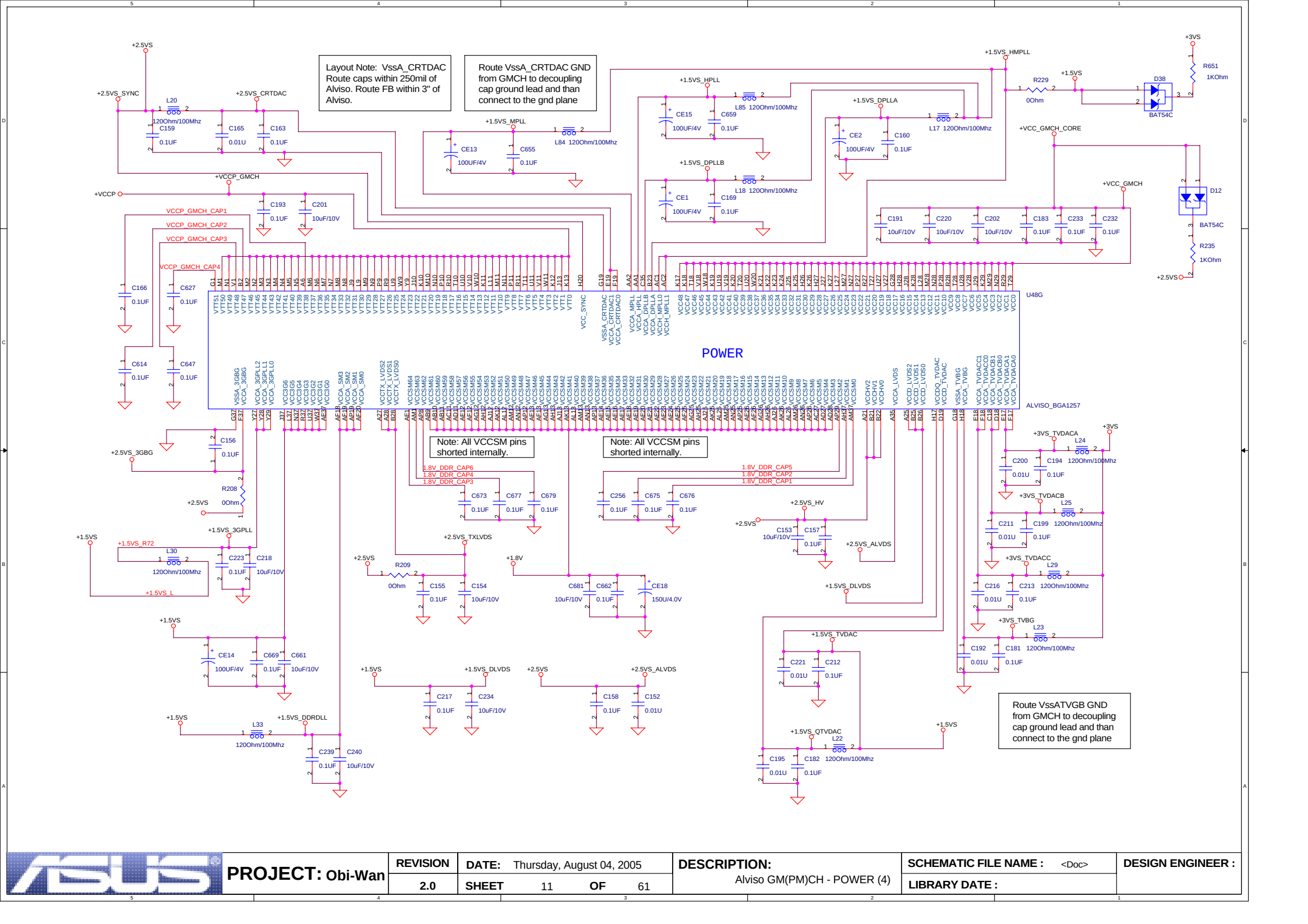
Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
POWER
U48G
ALVISO_BGA1257
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
+2.5VS
+2.5VS_SYNC
+2.5VS_CRTDAC
+2.5VS_3GBG
+2.5VS_HV
+2.5VS_ALVDS
+1.5VS
+1.5VS_HMPLL
+1.5VS_HPLL
+1.5VS_MPLL
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_3GPLL
+1.5VS_TVDAC
+1.5VS_QTVDAC
+1.5VS_DLVDS
+1.5VS_DDRDLL
+2.5VS_TXLVDS
+1.8V
+3VS
+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
+3VS_TVBG
+VCCP
+VCCP_GMCH
+VCC_GMCH_CORE
+VCC_GMCH
VCCP_GMCH_CAP1
VCCP_GMCH_CAP2
VCCP_GMCH_CAP3
VCCP_GMCH_CAP4
1.8V_DDR_CAP6
1.8V_DDR_CAP4
1.8V_DDR_CAP3
1.8V_DDR_CAP5
1.8V_DDR_CAP2
1.8V_DDR_CAP1
L20 120Ohm/100Mhz
L85 120Ohm/100Mhz
L84 120Ohm/100Mhz
L17 120Ohm/100Mhz
L18 120Ohm/100Mhz
L30 120Ohm/100Mhz
L33 120Ohm/100Mhz
L24 120Ohm/100Mhz
L25 120Ohm/100Mhz
L29 120Ohm/100Mhz
L23 120Ohm/100Mhz
L22 120Ohm/100Mhz
R651 1KOhm
R229 0Ohm
R208 0Ohm
R209 0Ohm
R235 1KOhm
D38 BAT54C
D12 BAT54C
C159 0.1UF
C165 0.01U
C163 0.1UF
CE15 100UF/4V
C659 0.1UF
CE13 100UF/4V
C655 0.1UF
CE2 100UF/4V
C160 0.1UF
CE1 100UF/4V
C169 0.1UF
C193 0.1UF
C201 10uF/10V
C191 10uF/10V
C220 10uF/10V
C202 10uF/10V
C183 0.1UF
C233 0.1UF
C232 0.1UF
C166 0.1UF
C627 0.1UF
C614 0.1UF
C647 0.1UF
C156 0.1UF
C673 0.1UF
C677 0.1UF
C679 0.1UF
C256 0.1UF
C675 0.1UF
C676 0.1UF
C153 10uF/10V
C157 0.1UF
C223 0.1UF
C218 10uF/10V
C155 0.1UF
C154 10uF/10V
C681 10uF/10V
C662 0.1UF
CE18 150U/4.0V
CE14 100UF/4V
C669 0.1UF
C661 10uF/10V
C217 0.1UF
C234 10uF/10V
C158 0.1UF
C152 0.01U
C239 0.1UF
C240 10uF/10V
C200 0.01U
C194 0.1UF
C211 0.01U
C199 0.1UF
C216 0.01U
C213 0.1UF
C192 0.01U
C181 0.1UF
C221 0.01U
C212 0.1UF
C195 0.01U
C182 0.1UF
PROJECT: Obi-Wan
REVISION 2.0
DATE: Thursday, August 04, 2005
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DESCRIPTION: Alviso GM(PM)CH - POWER (4)
SCHEMATIC FILE NAME : <Doc>
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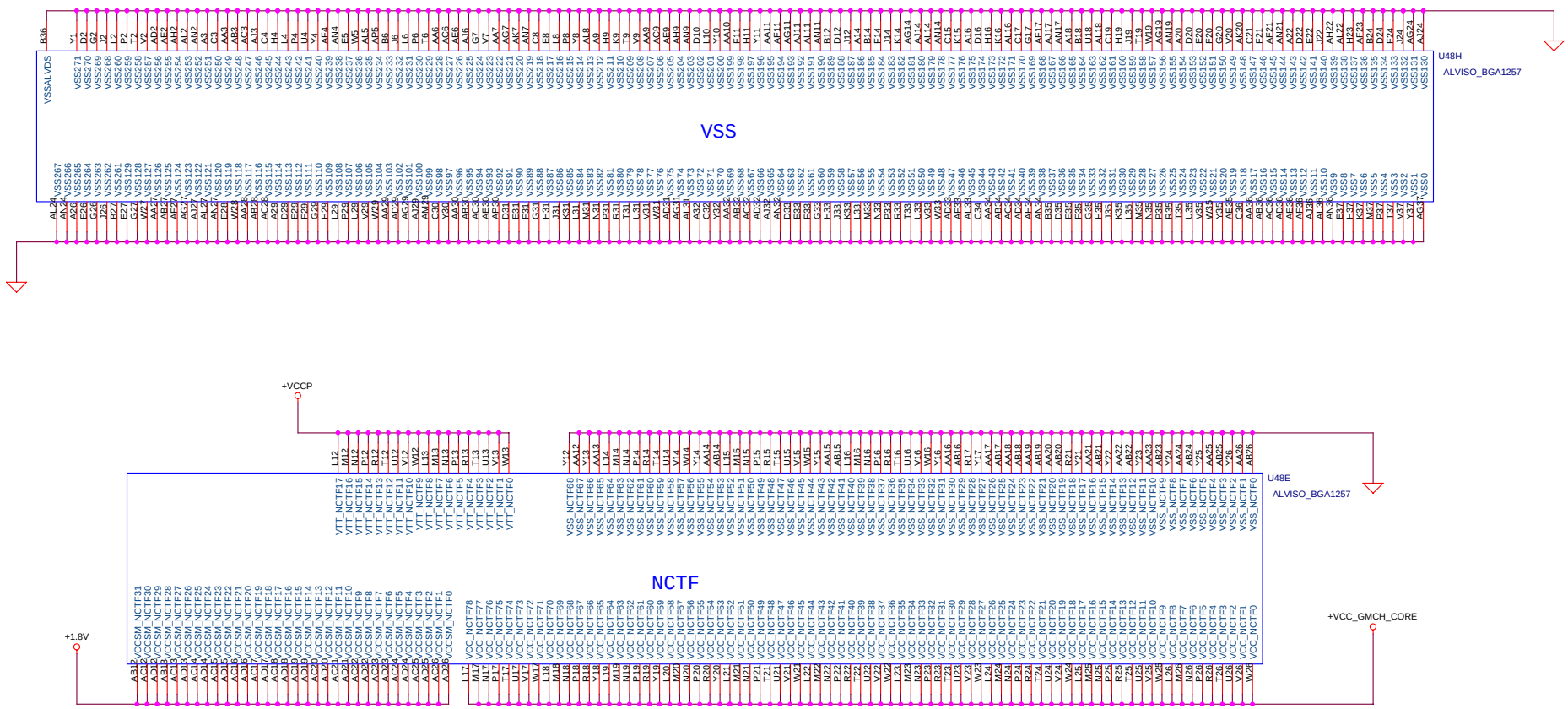
DESIGN ENGINEER :



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: Alviso GM(PM)CH - GND (5)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
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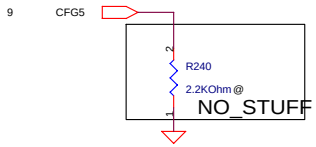
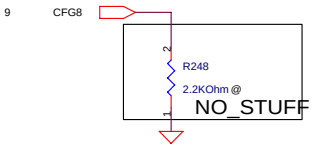
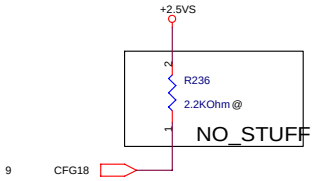
CFG5 : DMI x2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



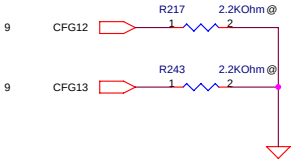
CFG8 : PCI-X POWER SAVING
LOW = PCI-X Power Saving
HIGH = (Default)



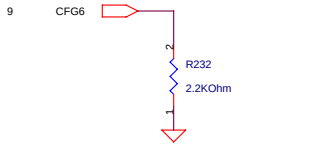
CFG18 : GMCH core VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V



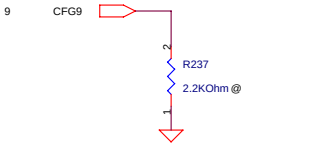
CFG12 : XOR/ALL Z test straps
CFG13 : XOR/ALL Z test straps
LOW LOW = Reserved
LOW HIGH = XOR Mode Enabled
HIGH LOW = All Z Mode Enabled
HIGH HIGH = Normal Operation (Default)



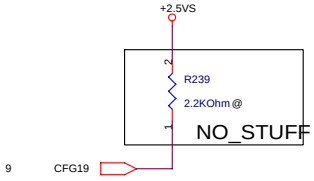
CFG6 : DDR vs DDR2 select
LOW = DDR2
HIGH = DDR (Default)



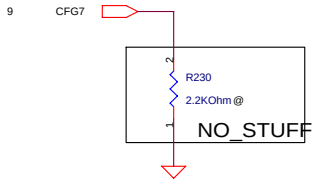
CFG9 : PCI Express Graphic Lane Reversal
LOW = Reverse Lane
HIGH = Normal Operation (Default)



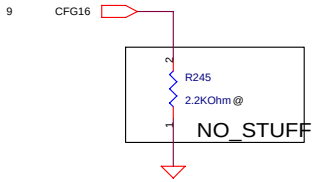
CFG19 : CPU VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V



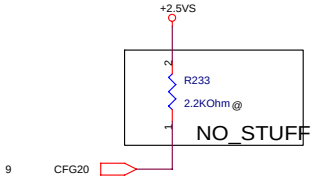
CFG7 : CPU Strap
LOW = Reserved
HIGH = Dothan (Default)



CFG16 : FSB Dynamic ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG20 : SDVO Present
LOW = No SDVO device present (Default)
HIGH = SDVO device present



CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.

SDVOCRTL_DATA LOW = No SDVO device present (Default)

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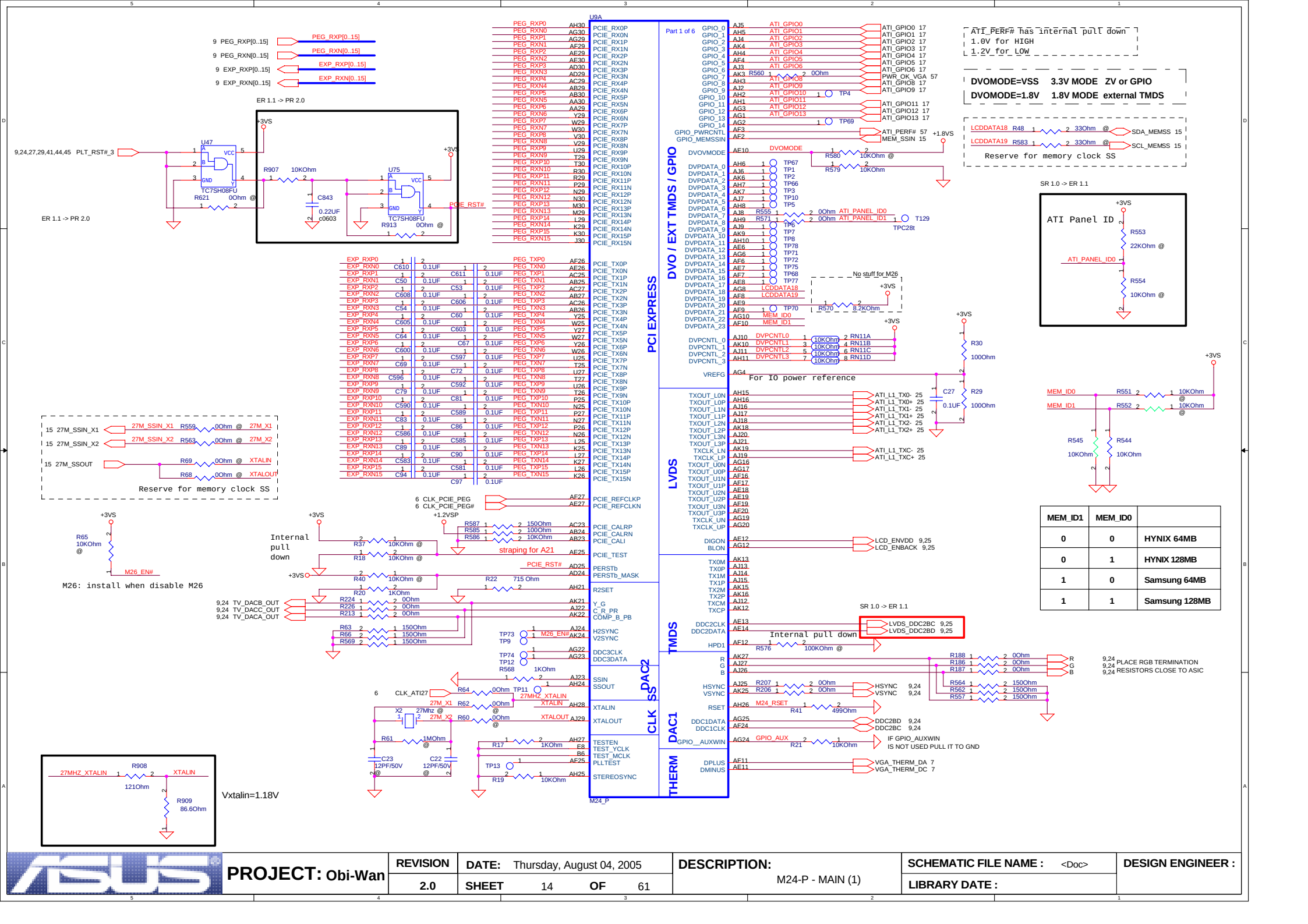
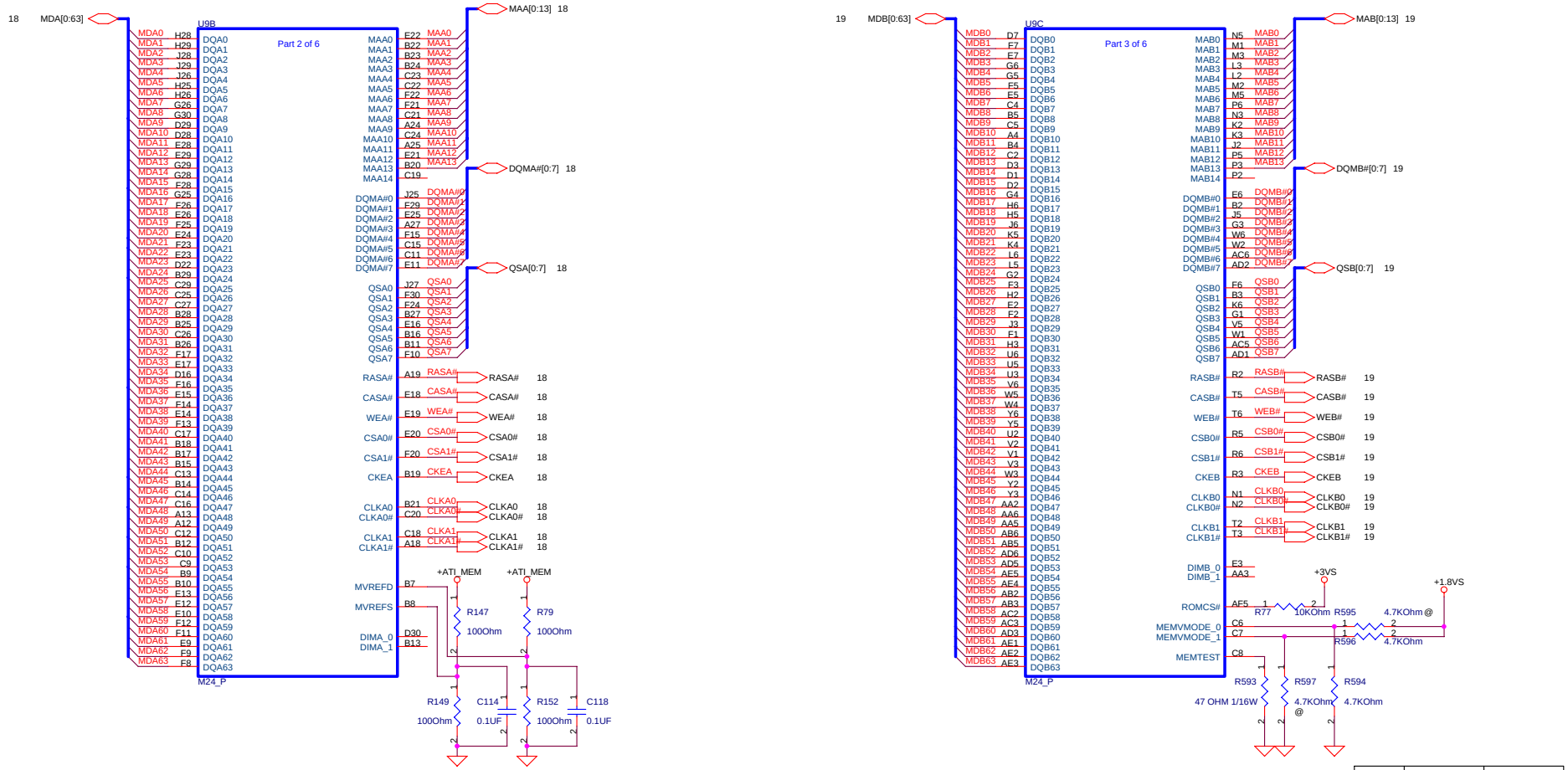
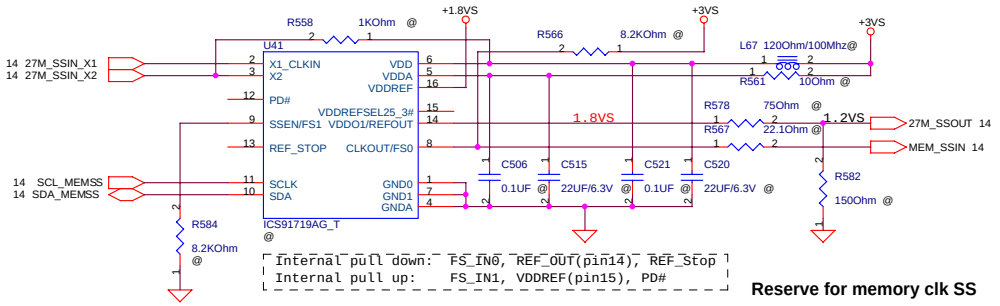

U9A
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCI EXPRESS
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PERSTb
PERSTb_MASK
R2SET
Y_G
C_R_PR
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
SSIN
SSOUT
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
M24_P
Part 1 of 6
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_PWRCNTL
GPIO_MEMSSIN
DVO / EXT TMDS / GPIO
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
For IO power reference
LVDS
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXCLK_UN
TXCLK_UP
DIGON
BLON
TMDS
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
GPIO__AUXWIN
DAC2
CLK
DAC1
THERM
DPLUS
DMINUS
ATI_GPIO0
ATI_GPIO1
ATI_GPIO2
ATI_GPIO3
ATI_GPIO4
ATI_GPIO5
ATI_GPIO6
ATI_GPIO8
ATI_GPIO9
ATI_GPIO10
ATI_GPIO11
ATI_GPIO12
ATI_GPIO13
ATI_PERF#
MEM_SSIN
DVOMODE
ATI_PANEL_ID0
ATI_PANEL_ID1
LCDDATA18
LCDDATA19
MEM_ID0
MEM_ID1
DVPCNTL0
DVPCNTL1
DVPCNTL2
DVPCNTL3
LCD_ENVDD
LCD_ENBACK
LVDS_DDC2BC
LVDS_DDC2BD
HSYNC
VSYNC
M24_RSET
DDC2BD
DDC2BC
GPIO_AUX
VGA_THERM_DA
VGA_THERM_DC
ATI_PERF# has internal pull down
1.0V for HIGH
1.2V for LOW
DVOMODE=VSS 3.3V MODE ZV or GPIO
DVOMODE=1.8V 1.8V MODE external TMDS
Reserve for memory clock SS
SR 1.0 -> ER 1.1
ATI Panel ID
No stuff for M26
Internal pull down
straping for A21
PCIE_RST#
M26_EN#
M26: install when disable M26
ER 1.1 -> PR 2.0
Vxtalin=1.18V
PLACE RGB TERMINATION RESISTORS CLOSE TO ASIC
IF GPIO_AUXWIN IS NOT USED PULL IT TO GND
MEM_ID1 MEM_ID0
0 0 HYNIX 64MB
0 1 HYNIX 128MB
1 0 Samsung 64MB
1 1 Samsung 128MB
PROJECT: Obi-Wan
REVISION 2.0
DATE: Thursday, August 04, 2005
SHEET 14 OF 61
DESCRIPTION: M24-P - MAIN (1)
SCHEMATIC FILE NAME : <Doc>
LIBRARY DATE :
DESIGN ENGINEER :



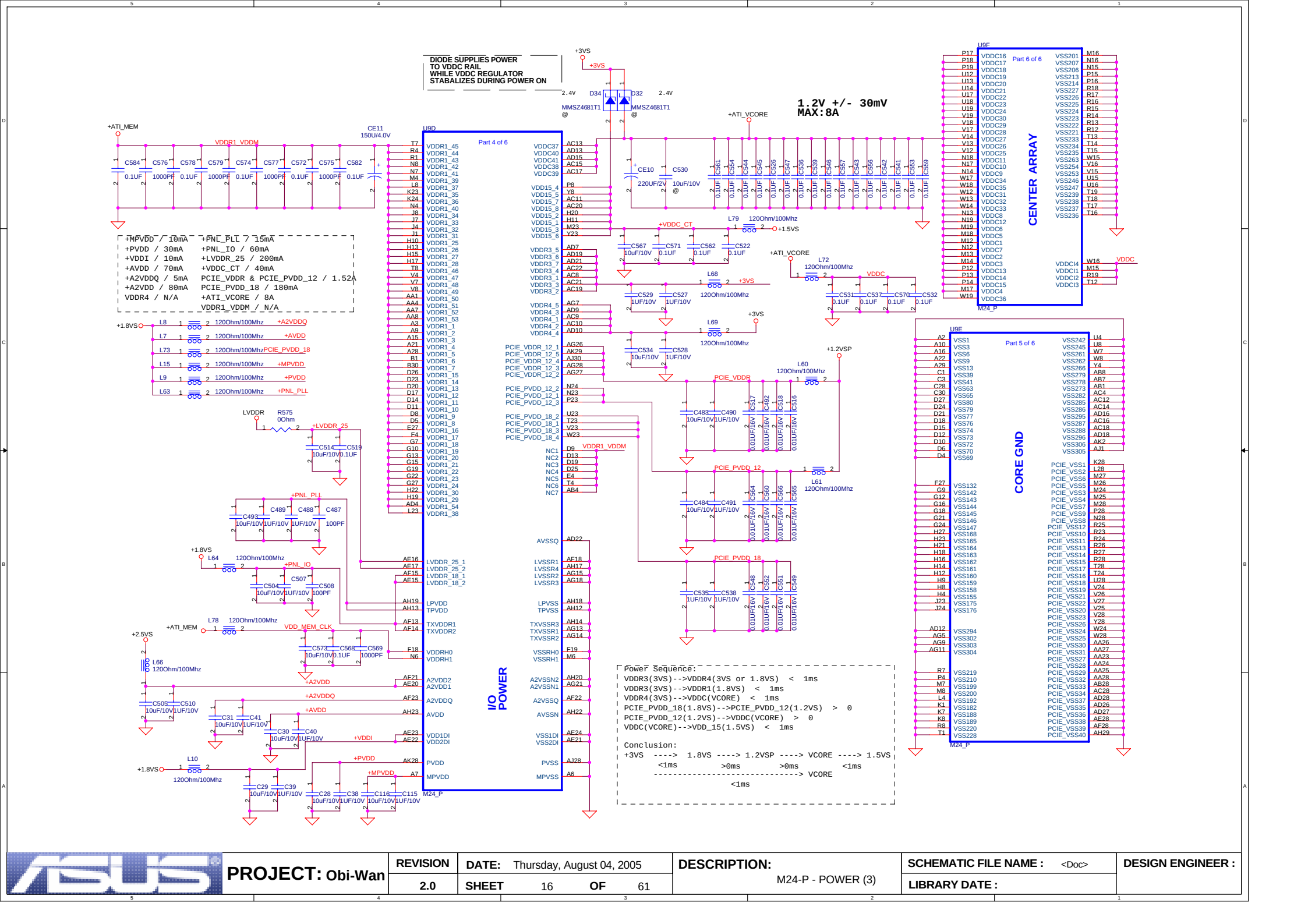
VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+1.8VS
2.5V	+1.8VS	GND



Reserve for memory clk SS

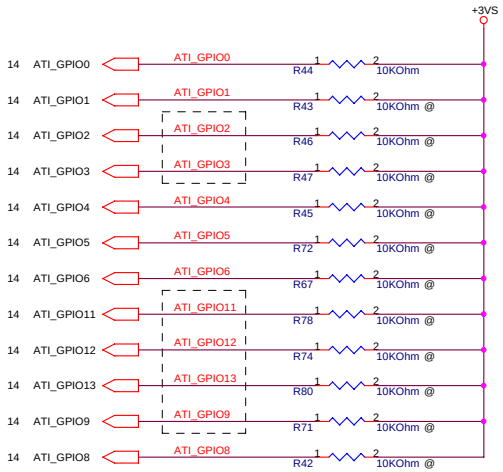
ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** M24-P - MEMORY INTERFACE (2)	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 15 **OF** 61		**LIBRARY DATE :**

DESIGN ENGINEER :



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: M24-P - POWER (3)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 16 OF 61		LIBRARY DATE :	

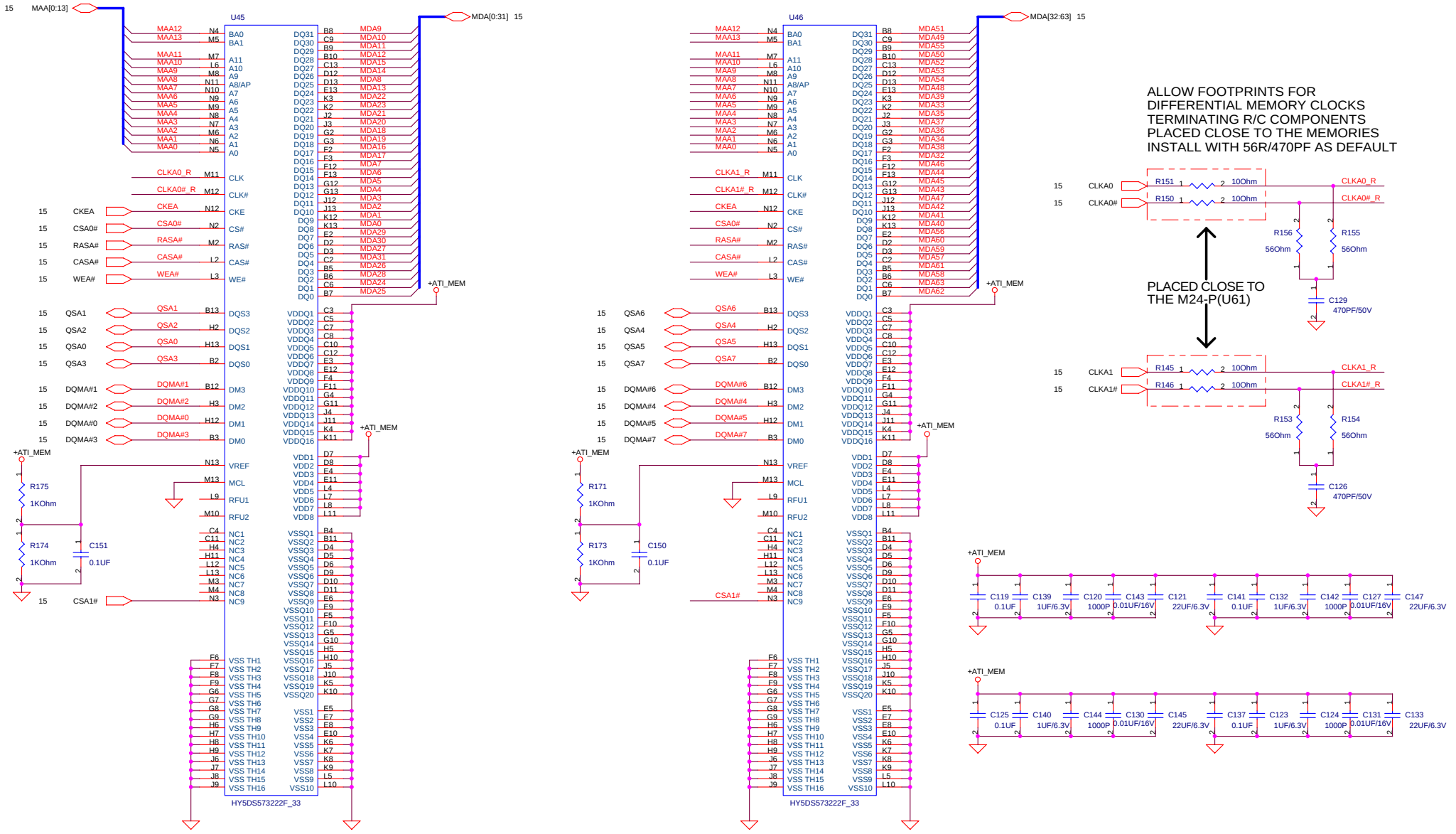
OPTION STRAPS



GPIO[0:13] : Internal PD

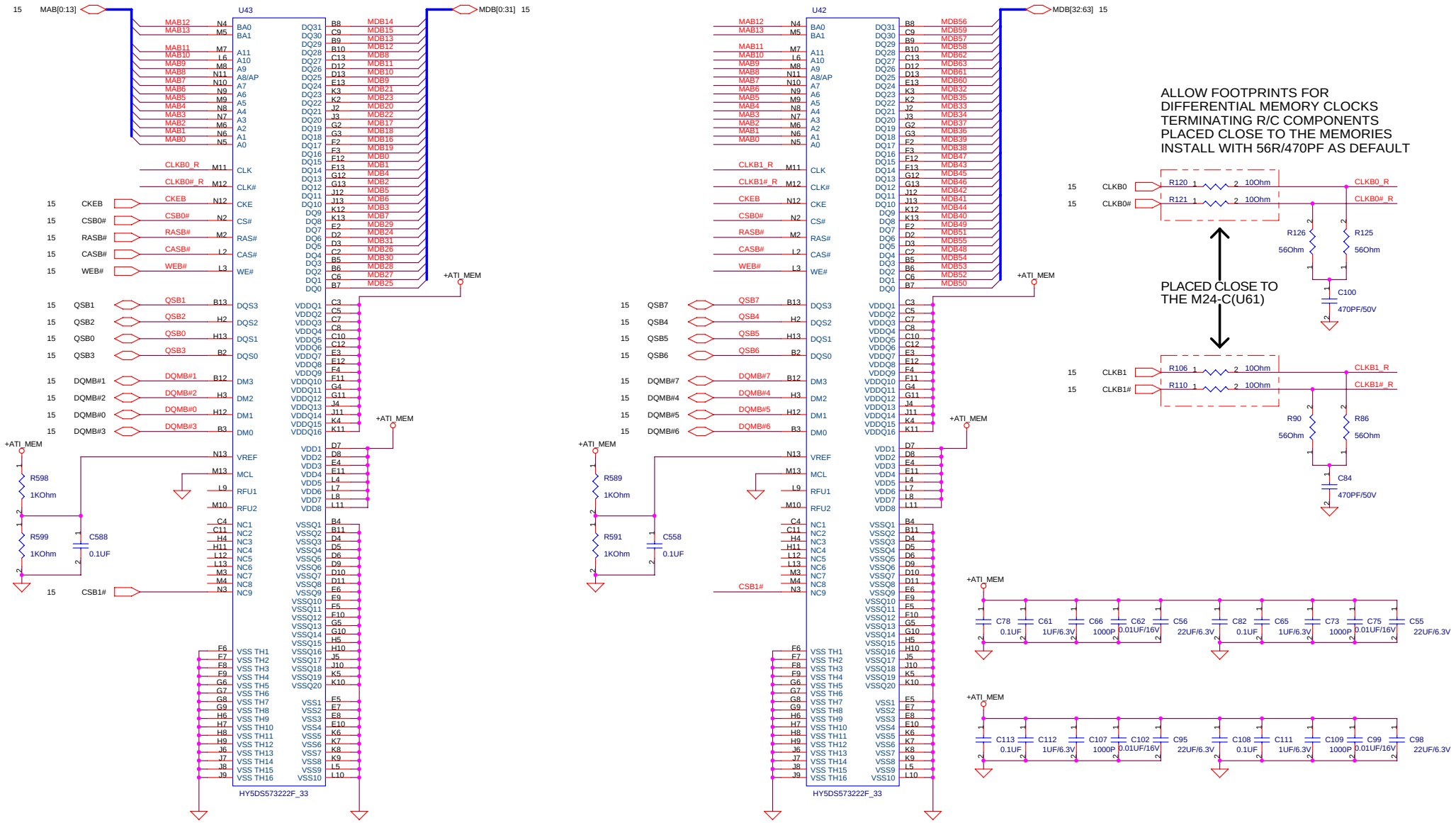
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disable for mobile mode 1: Tx de_emphasis enable	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal	00
B_PTX_IEXT	GPIO4	**0: normal mode** **1: extra current in Tx output stage**	0
FORCE_COMPLIANCE	GPIO5	Force chip to go to compliance state quickly for test purposes	0
B_PPLL_BW	GPIO6	0: Full PLL Bandwidth 1: Reduce PLL Bandwidth	0
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	0000
	DVPDATA_20	0: Slave VIP host port device peesent 1: No slave VIP host port device	0

M26: GPIO11 is memory aperture (0=128M 1=256M)

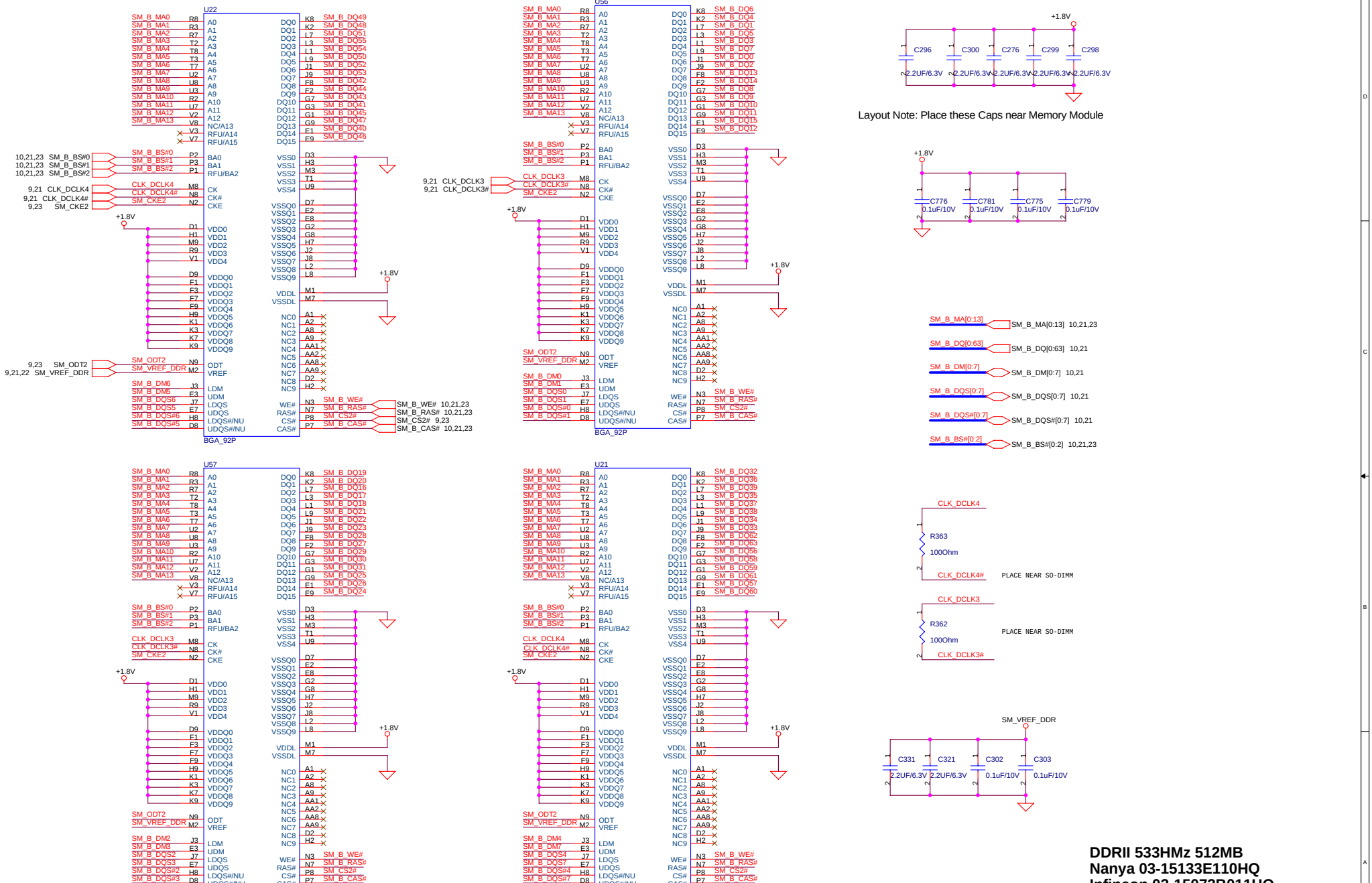


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: M24-C - DDR MEMORY A	SCHEMATIC FILE NAME : <Doc>
		SHEET 18 OF 61		LIBRARY DATE :

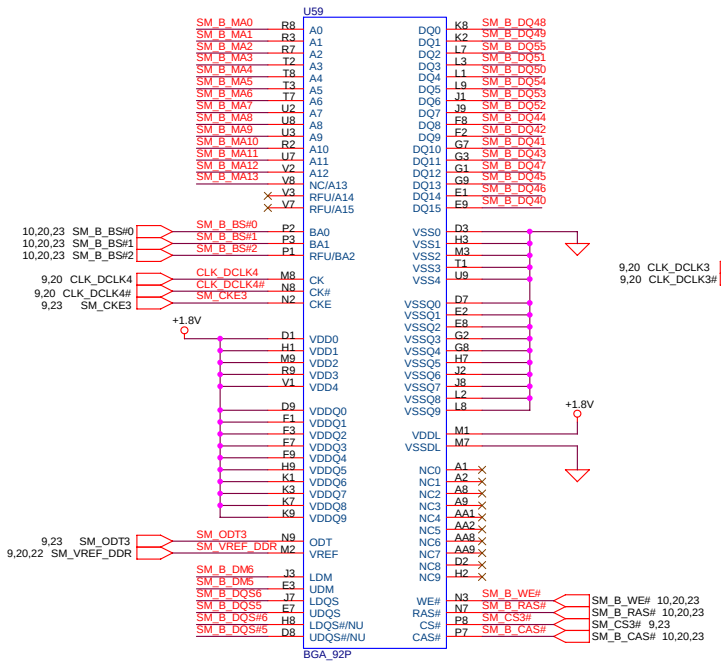
DESIGN ENGINEER :

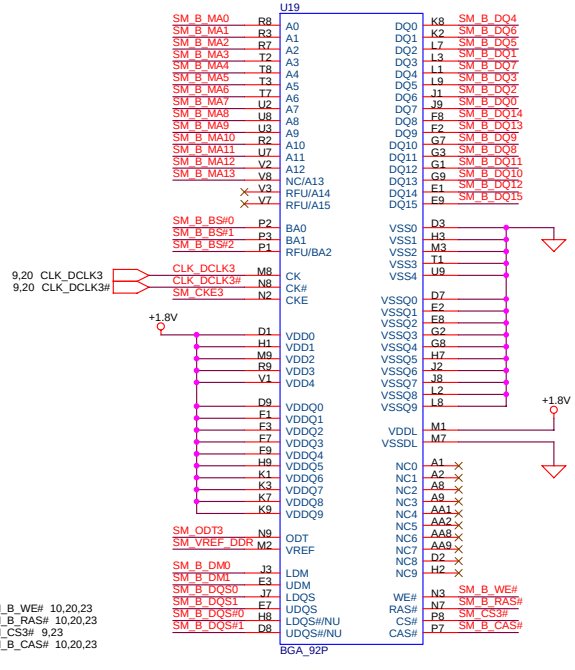


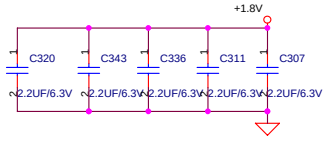
PROJECT: Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** M24-C - DDR MEMORY B	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 19 **OF** 61		**LIBRARY DATE :**	



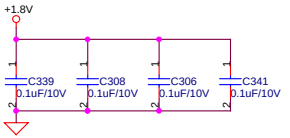
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: DDR2 (1)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 20 OF 61		LIBRARY DATE :	

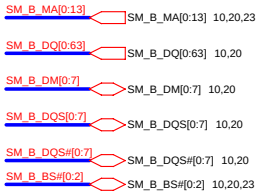


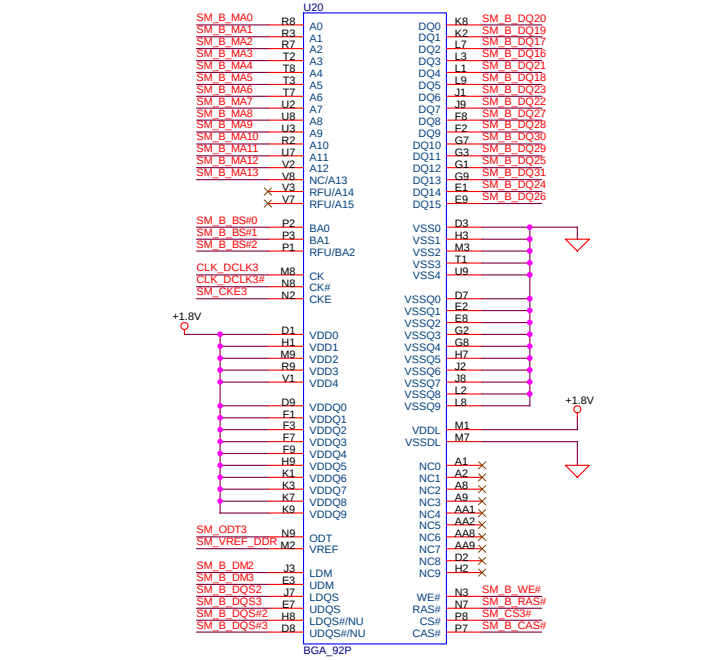


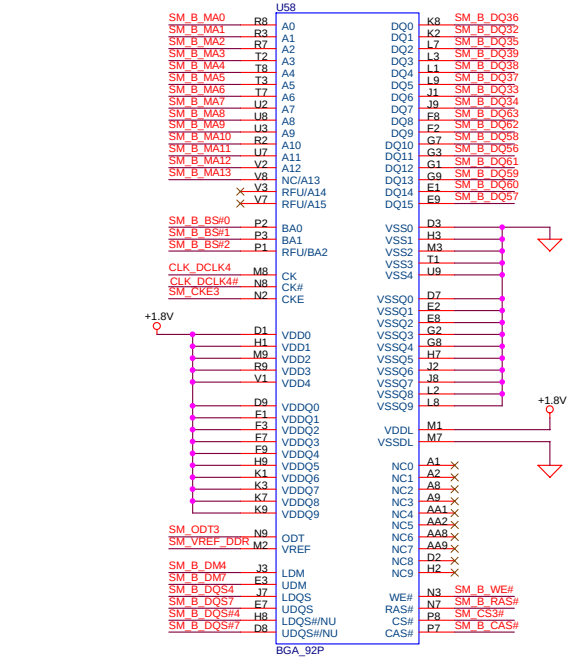


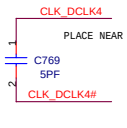
Layout Note: Place these Caps near Memory Module

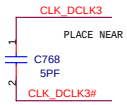


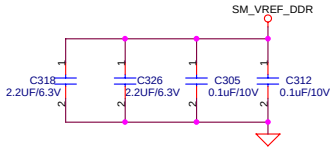












ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** DDR2 (2)	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 21 **OF** 61		**LIBRARY DATE :**

DESIGN ENGINEER :

SM_A_DQ[63:0] 10

SM_A_MA[13:0] 10,23

SM_A_DM[7:0] 10

SM_A_DQS[0:7]

SM_A_DQS[0:7] 10

SM_A_DQS#[0:7]

SM_A_DQS#[0:7] 10

NO STUFF

*

CLK_DCLK0

C723

PLACE NEAR SO-DIMM_1

10P @

CLK_DCLK0#

CLK_DCLK1

C724

PLACE NEAR SO-DIMM_1

10P @

CLK_DCLK1#

10,23 SM_A_MA[0:13]

CN28A

SM_A_MA0 SM_A_MA1 SM_A_MA2 SM_A_MA3 SM_A_MA4 SM_A_MA5 SM_A_MA6 SM_A_MA7 SM_A_MA8 SM_A_MA9 SM_A_MA10 SM_A_MA11 SM_A_MA12 SM_A_MA13

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2

10,23 SM_A_BS#2

10,23 SM_A_BS#0

10,23 SM_A_BS#1

9,23 SM_CS0#

9,23 SM_CS1#

9 CLK_DCLK0

9 CLK_DCLK0#

9 CLK_DCLK1

9 CLK_DCLK1#

9,23 SM_CKE0

9,23 SM_CKE1

10,23 SM_A_CAS#

10,23 SM_A_RAS#

10,23 SM_A_WE#

BA0 BA1 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

SA0 SA1

6,7,42 SMBCK_3S

6,7,42 SMBDA_3S

SCL SDA

R328 10KOhm

R329 10KOhm

9,23 SM_ODT0

9,23 SM_ODT1

ODT0 ODT1

10 SM_A_DM[0..7]

SM_A_DM0 SM_A_DM1 SM_A_DM2 SM_A_DM3 SM_A_DM4 SM_A_DM5 SM_A_DM6 SM_A_DM7

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

10 SM_A_DQS[0..7]

SM_A_DQS0 SM_A_DQS1 SM_A_DQS2 SM_A_DQS3 SM_A_DQS4 SM_A_DQS5 SM_A_DQS6 SM_A_DQS7

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

10 SM_A_DQS#[0..7]

SM_A_DQS#0 SM_A_DQS#1 SM_A_DQS#2 SM_A_DQS#3 SM_A_DQS#4 SM_A_DQS#5 SM_A_DQS#6 SM_A_DQS#7

DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

SM_A_DQ[0:63] 10

SM_A_DQ0 SM_A_DQ5 SM_A_DQ2 SM_A_DQ7 SM_A_DQ4 SM_A_DQ1 SM_A_DQ6 SM_A_DQ3 SM_A_DQ13 SM_A_DQ12 SM_A_DQ10 SM_A_DQ11 SM_A_DQ8 SM_A_DQ9 SM_A_DQ14 SM_A_DQ15 SM_A_DQ16 SM_A_DQ20 SM_A_DQ22 SM_A_DQ23 SM_A_DQ17 SM_A_DQ21 SM_A_DQ18 SM_A_DQ19 SM_A_DQ24 SM_A_DQ25 SM_A_DQ27 SM_A_DQ31 SM_A_DQ29 SM_A_DQ28 SM_A_DQ26 SM_A_DQ30 SM_A_DQ32 SM_A_DQ33 SM_A_DQ39 SM_A_DQ34 SM_A_DQ36 SM_A_DQ37 SM_A_DQ38 SM_A_DQ35 SM_A_DQ45 SM_A_DQ40 SM_A_DQ47 SM_A_DQ46 SM_A_DQ44 SM_A_DQ41 SM_A_DQ43 SM_A_DQ42 SM_A_DQ49 SM_A_DQ48 SM_A_DQ55 SM_A_DQ54 SM_A_DQ52 SM_A_DQ53 SM_A_DQ50 SM_A_DQ51 SM_A_DQ56 SM_A_DQ60 SM_A_DQ63 SM_A_DQ62 SM_A_DQ61 SM_A_DQ57 SM_A_DQ58 SM_A_DQ59

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

DDR_DIMM_200P

+3VS

C700 0.1UF

C699 0.1UF

+1.8V

CN28B

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12

VDDSPD

NC1 NC2 NC3 NC4 NCTEST

VREF

GND0 GND1

NP_NC1 NP_NC2

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57

DDR_DIMM_200P

M_VREF_DIMM1

9,20,21 SM_VREF_DDR

C657 2.2uF/6.3V

C643 0.1UF

Layout Note: Place these Caps near SO DIMM 1

+1.8V

C286 0.1UF

C285 0.1UF

C284 0.1UF

C283 0.1UF

Layout Note: Place these Caps near SO DIMM 1

+1.8V

C278 2.2uF/6.3V

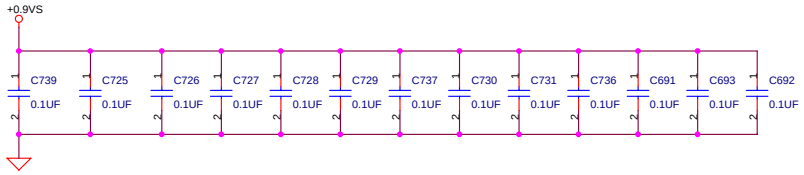
C277 2.2uF/6.3V

C279 2.2uF/6.3V

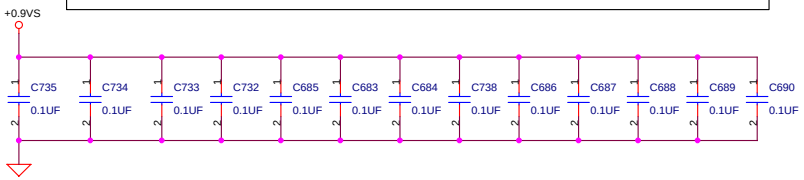
C275 2.2uF/6.3V

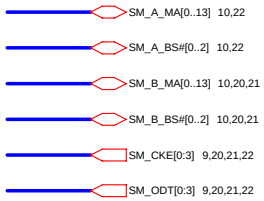
C274 2.2uF/6.3V

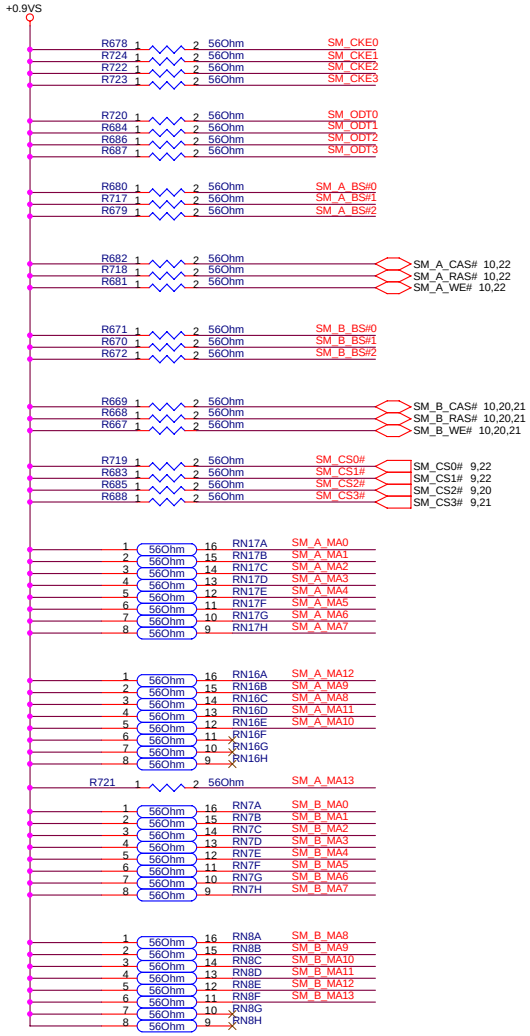
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: STANDARD DDR2 SO-DIMM	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 22 OF 61		LIBRARY DATE :	



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



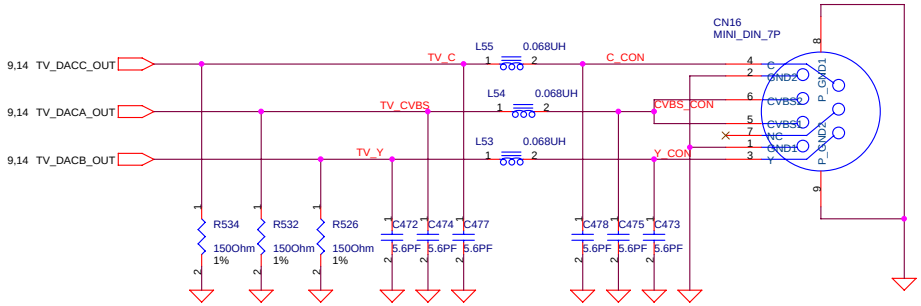


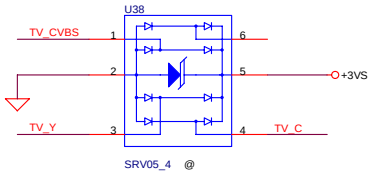


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME : <Doc>
		SHEET 23 OF 61		LIBRARY DATE :

DESIGN ENGINEER :

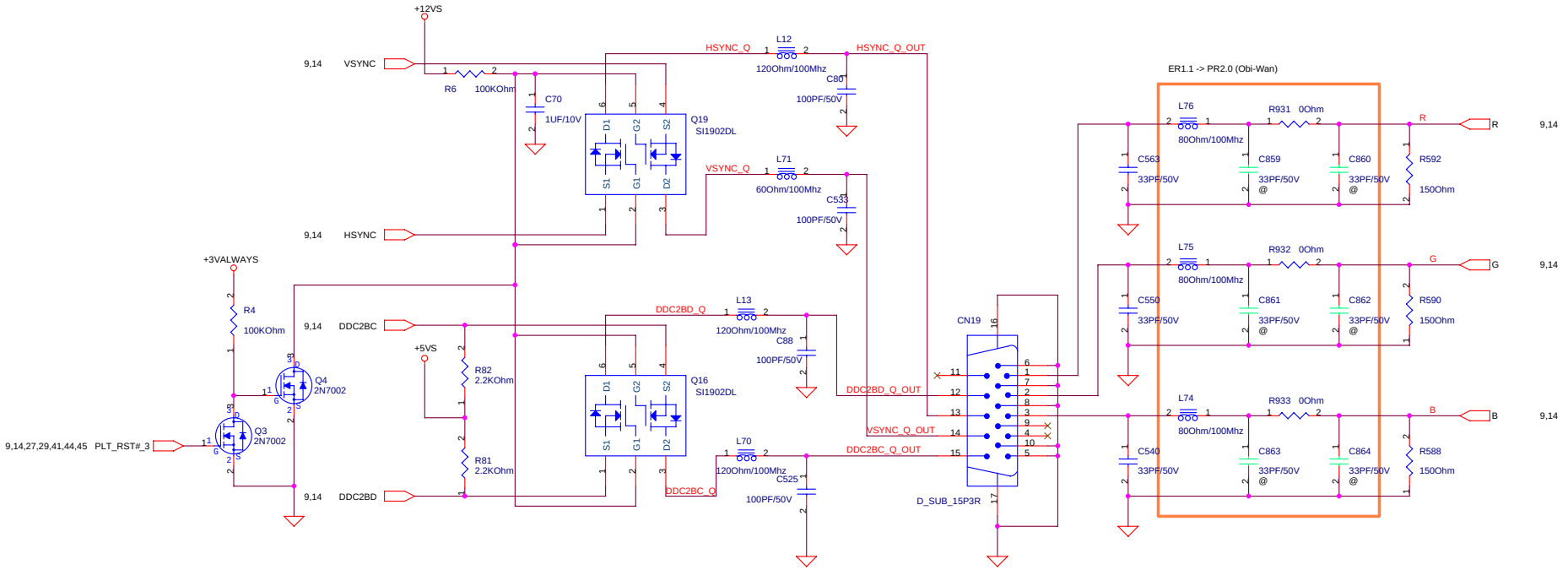
TV OUT





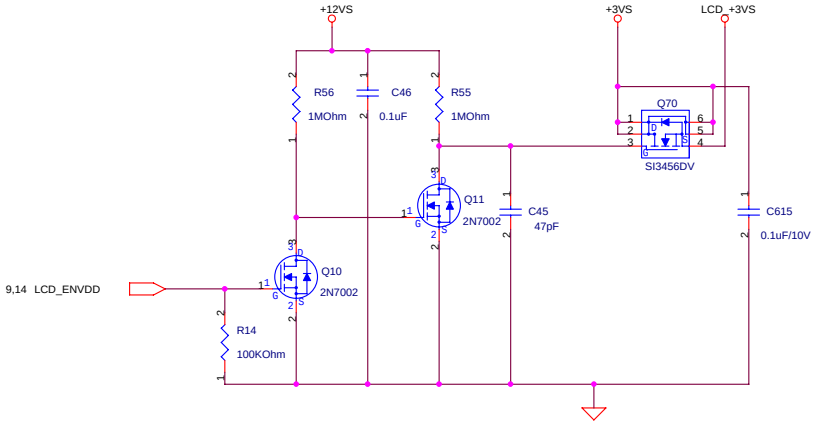
PLACE ESD Diodes near U44

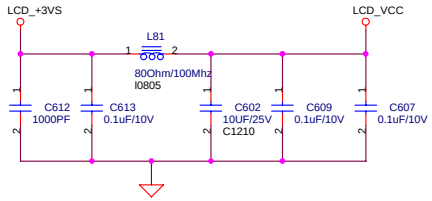
CRT Connector

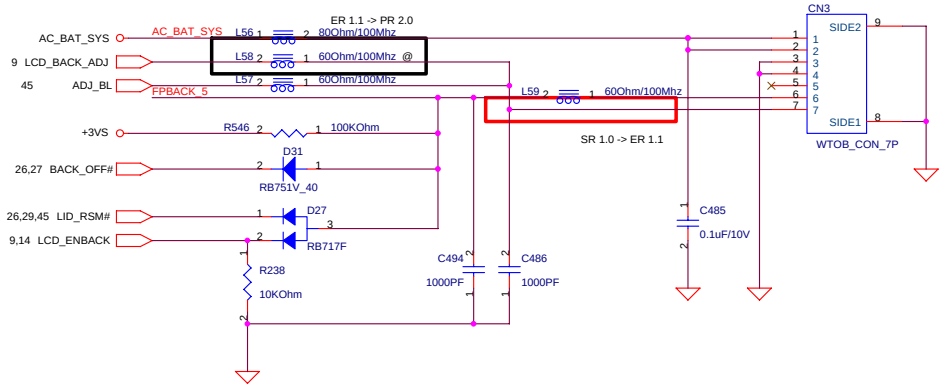


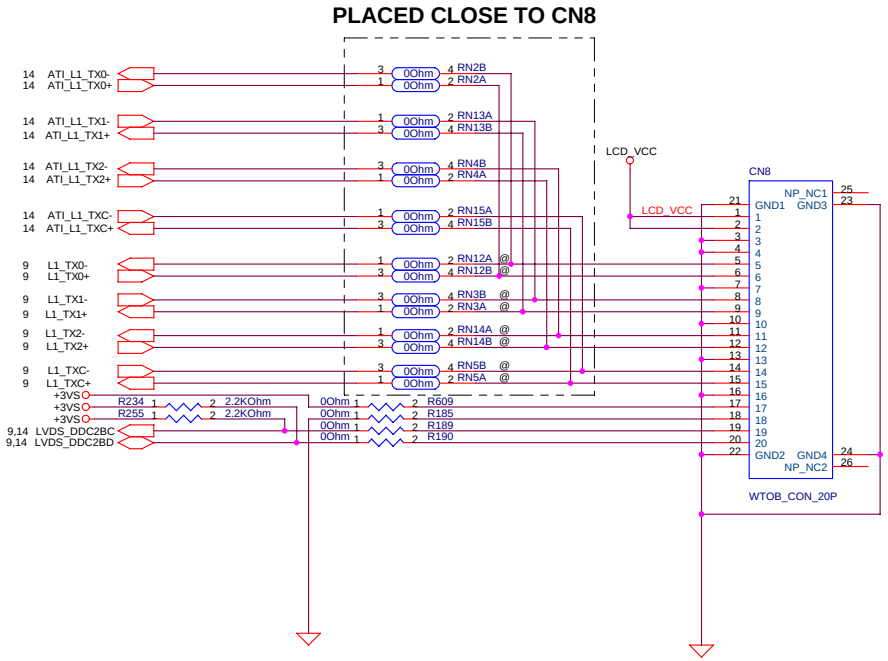
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: CRT & TV OUT	SCHEMATIC FILE NAME : <Doc>
		SHEET 24 OF 61		LIBRARY DATE :

DESIGN ENGINEER :



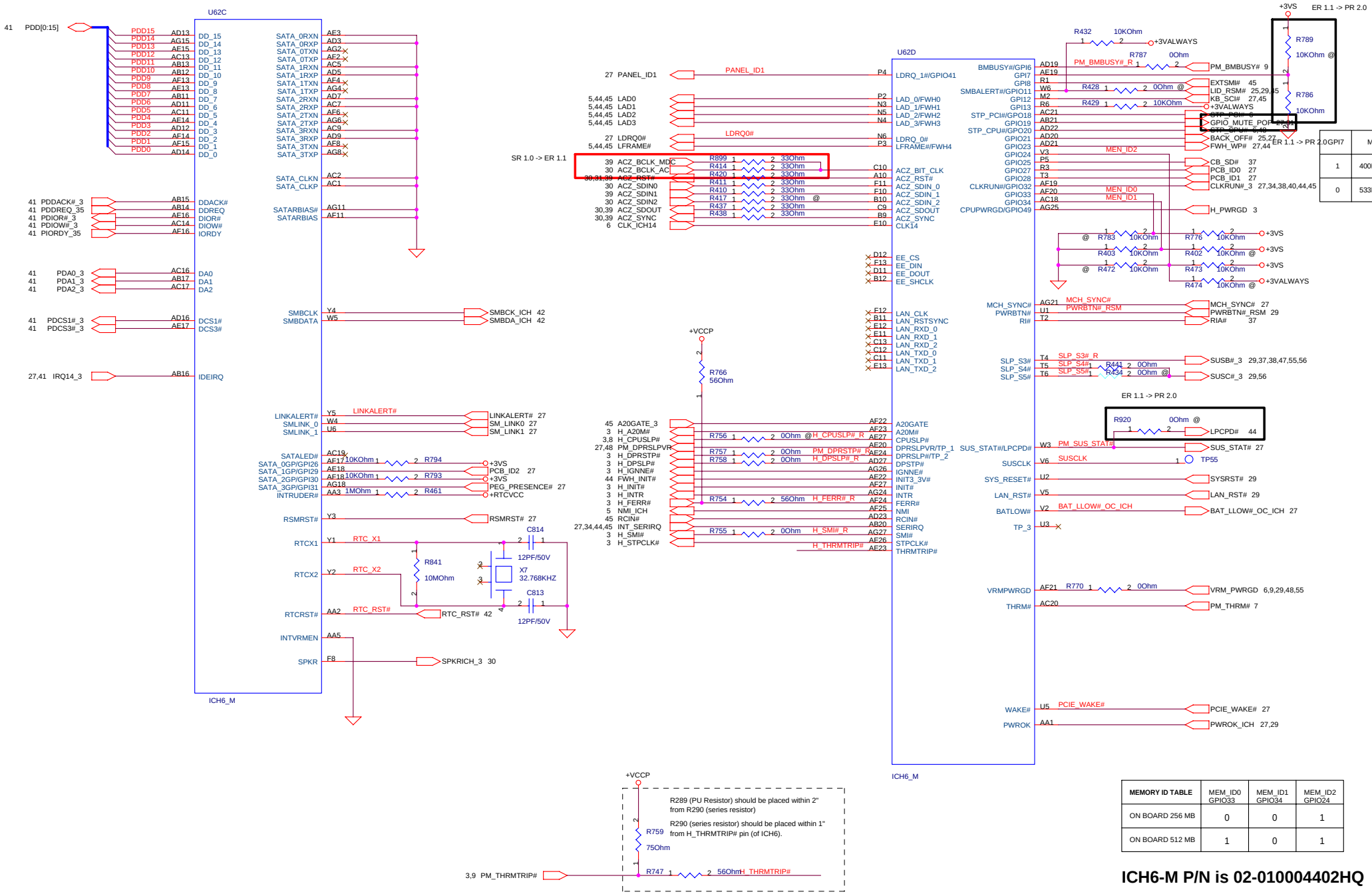






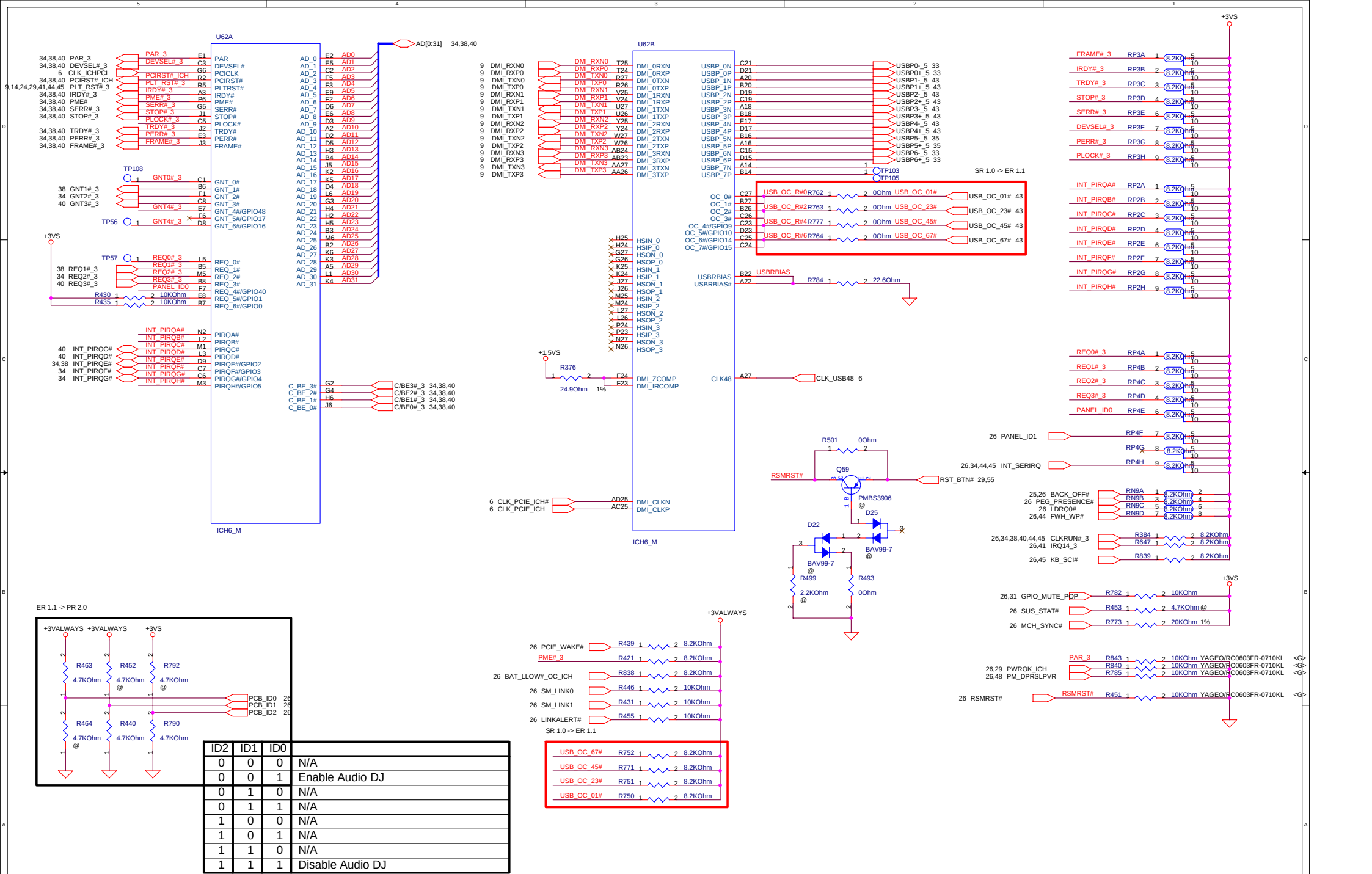
ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** LCD & INVERTER	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 25 **OF** 61		**LIBRARY DATE :**

DESIGN ENGINEER :



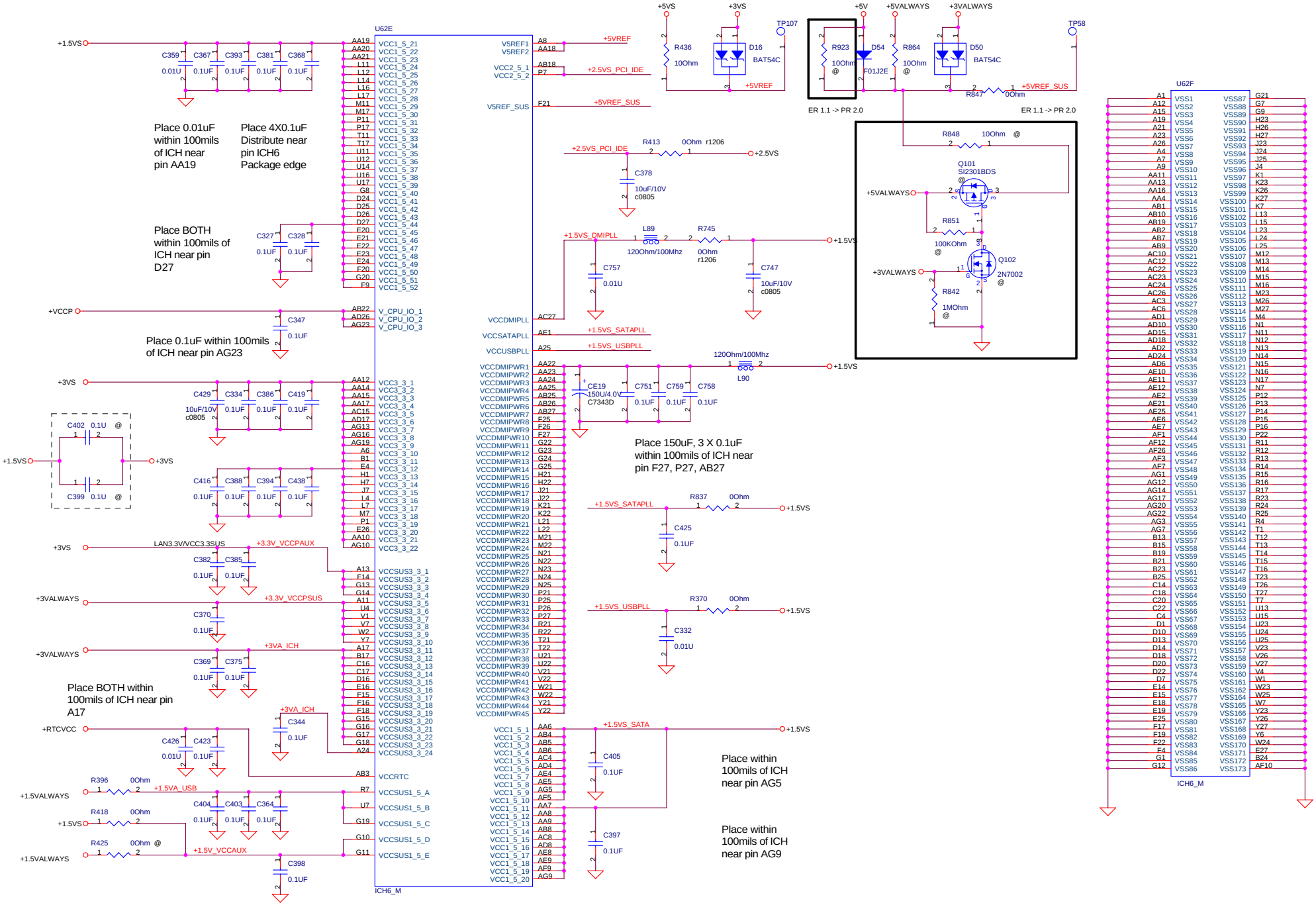
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: ICH6M - LPC & IDE (1)	SCHEMATIC FILE NAME : <Doc>
		SHEET 26 OF 61		LIBRARY DATE :

DESIGN ENGINEER :

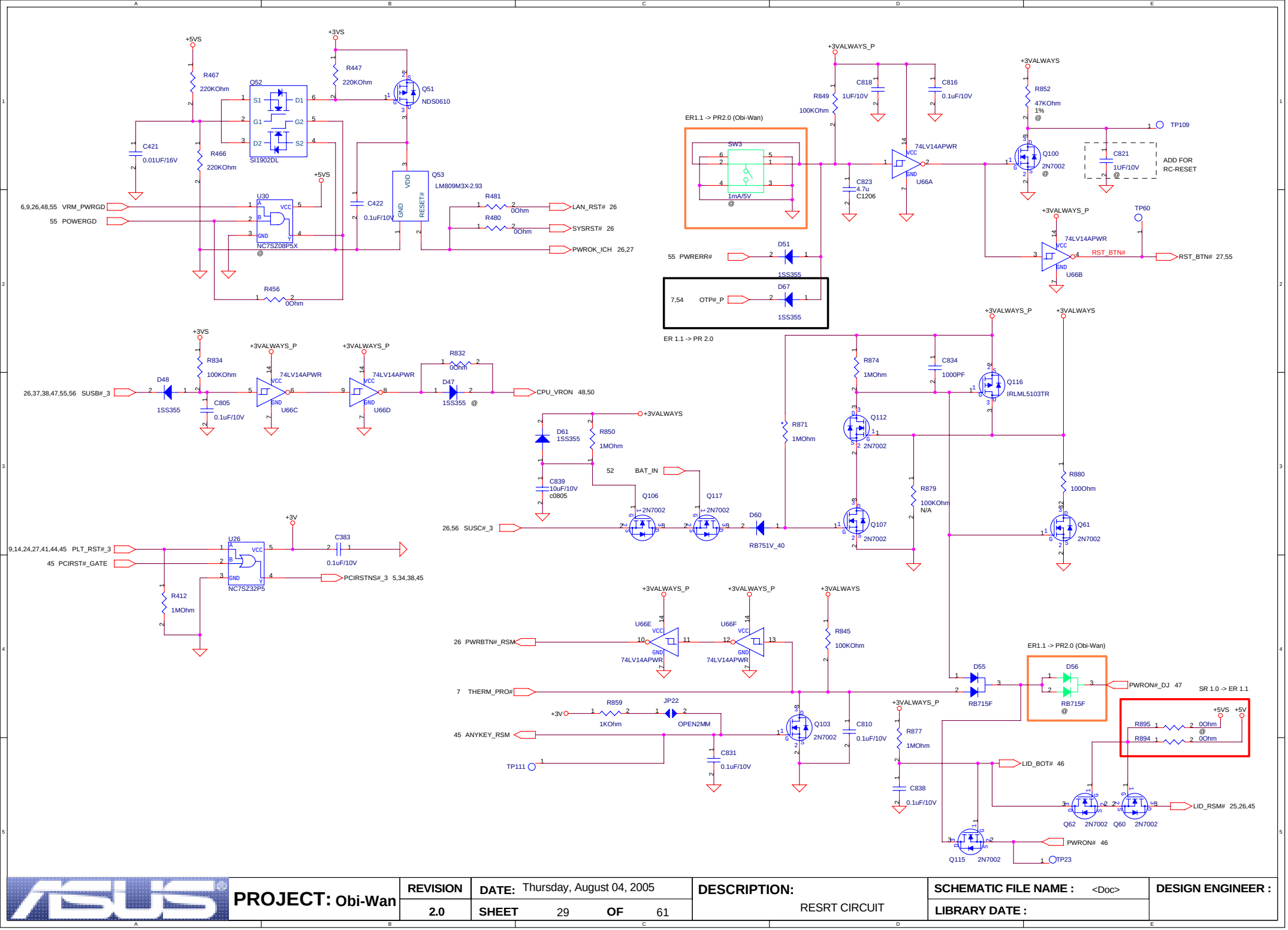


ID2	ID1	ID0	
0	0	0	N/A
0	0	1	Enable Audio DJ
0	1	0	N/A
0	1	1	N/A
1	0	0	N/A
1	0	1	N/A
1	1	0	N/A
1	1	1	Disable Audio DJ

PROJECT: Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** ICH6M - USB&PCI-E&PMIO (2)
		SHEET 27 **OF** 61	**SCHEMATIC FILE NAME :** <Doc>
			LIBRARY DATE :
			DESIGN ENGINEER :

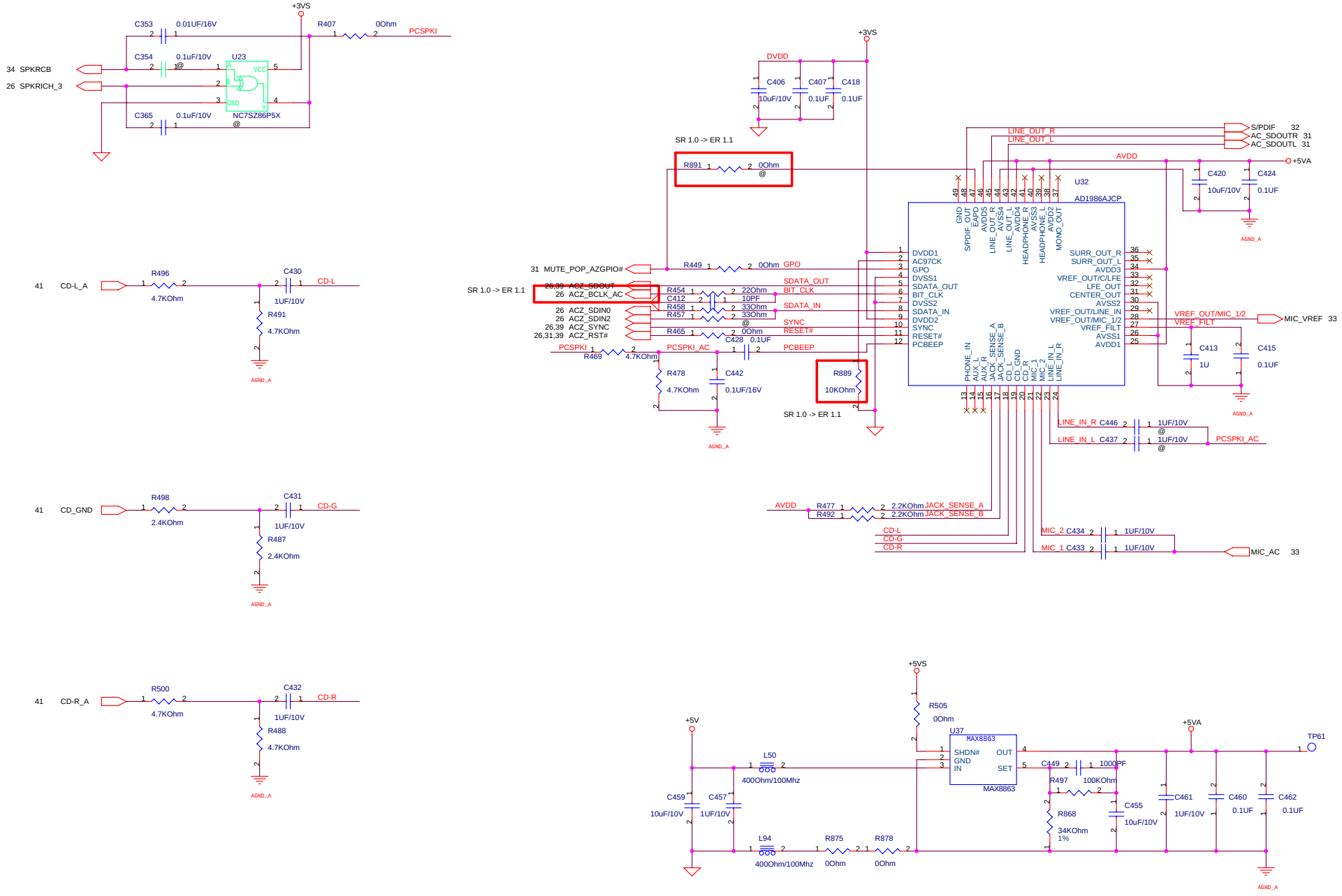


PROJECT: Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** ICH6M - PWR & GND (3)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 28 **OF** 61		**LIBRARY DATE :**	

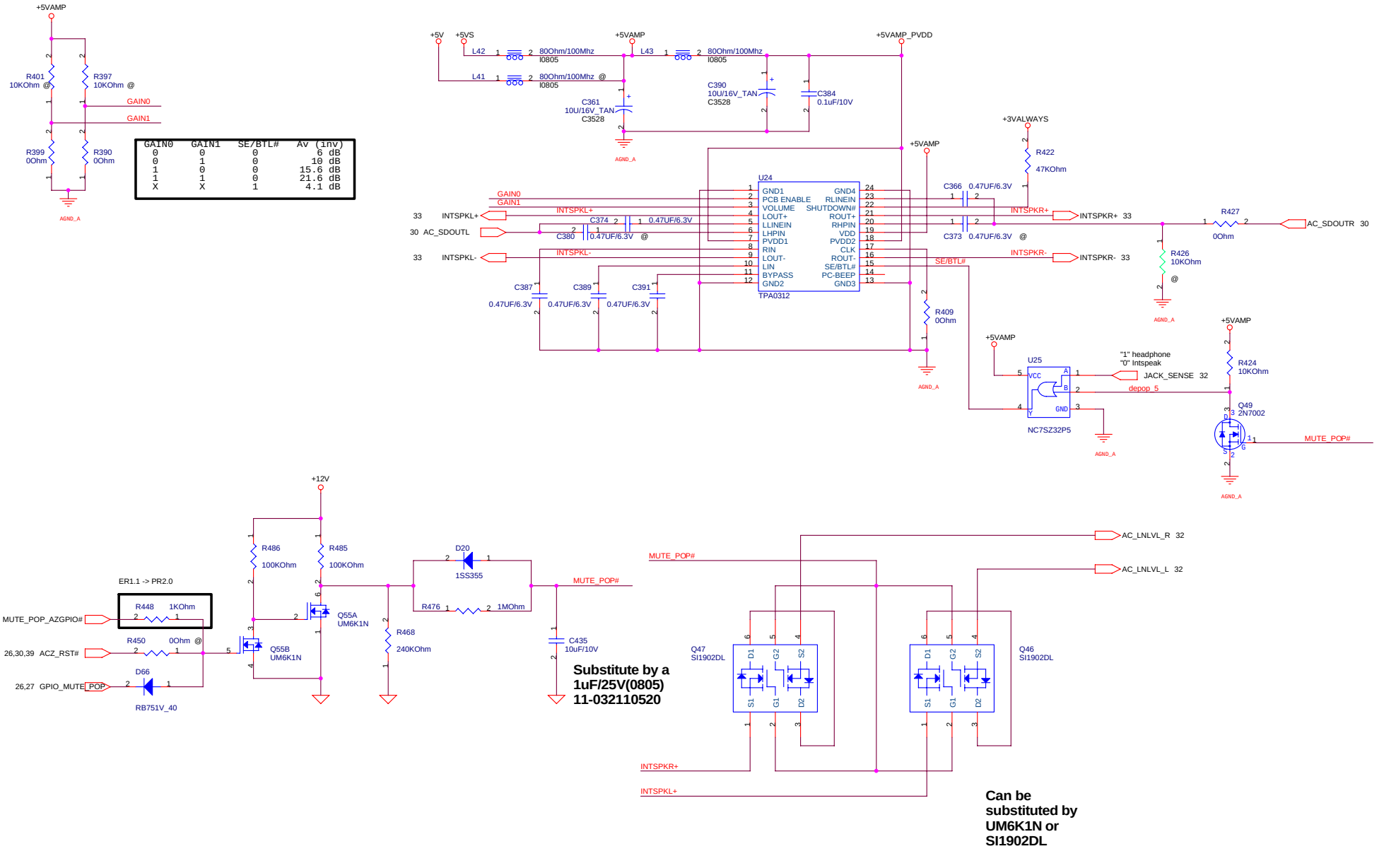


ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** RESRT CIRCUIT	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 29 **OF** 61		**LIBRARY DATE :**

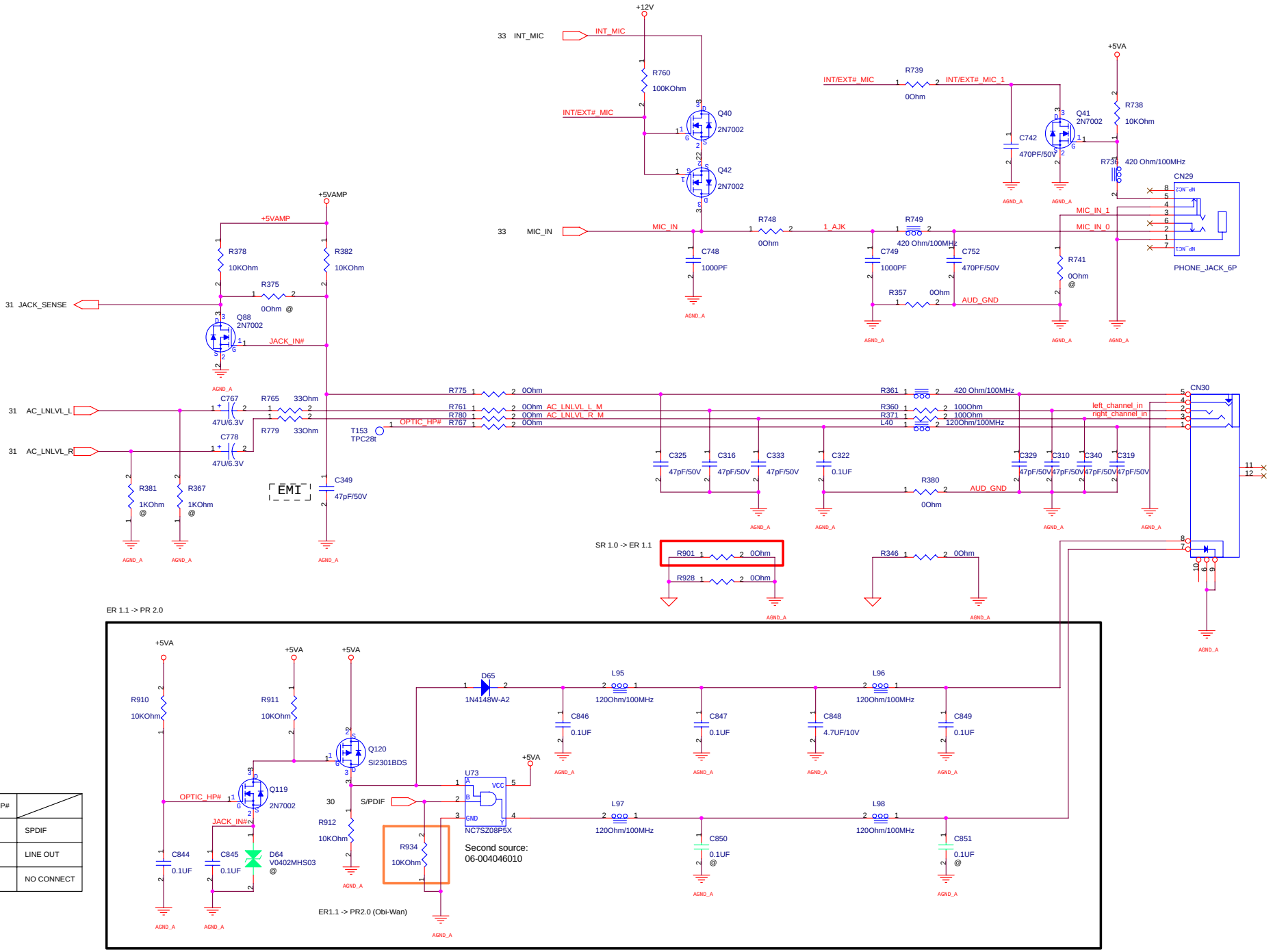
DESIGN ENGINEER :



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: AZALIA AD1986A	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 30 OF 61		LIBRARY DATE :	



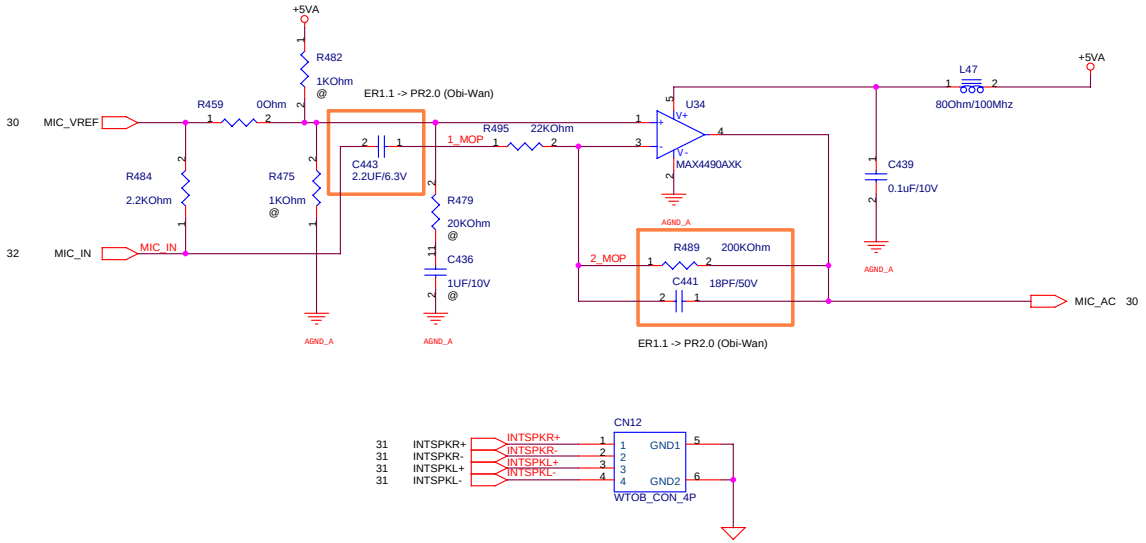
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: AUDIO AMP & INT SPK	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 31 OF 61		LIBRARY DATE :	



JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT

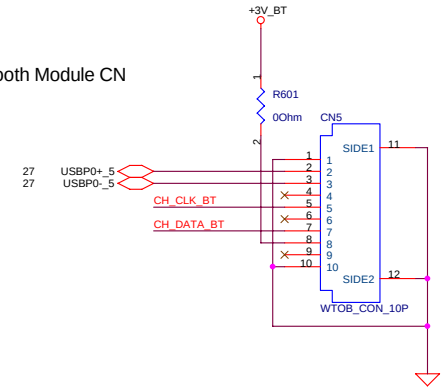
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: PHONE JACK	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 32 OF 61		LIBRARY DATE :	

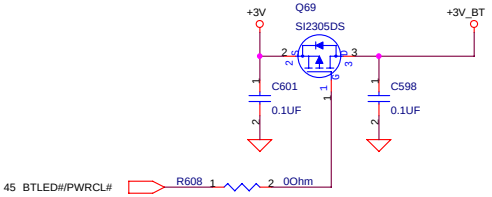
MIC PreAmp & Mic Jack

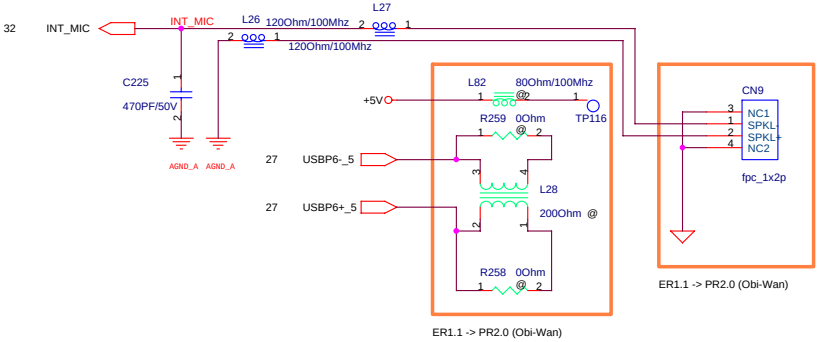


External Modules

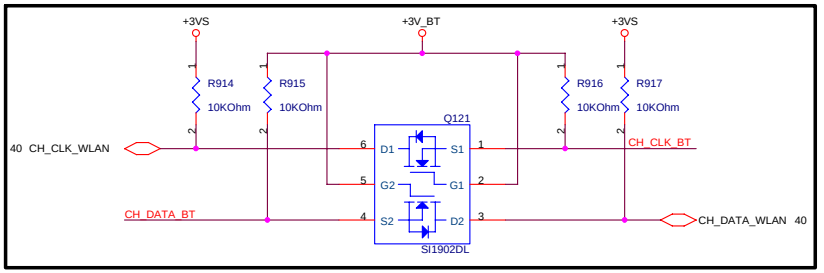
Bluetooth Module CN



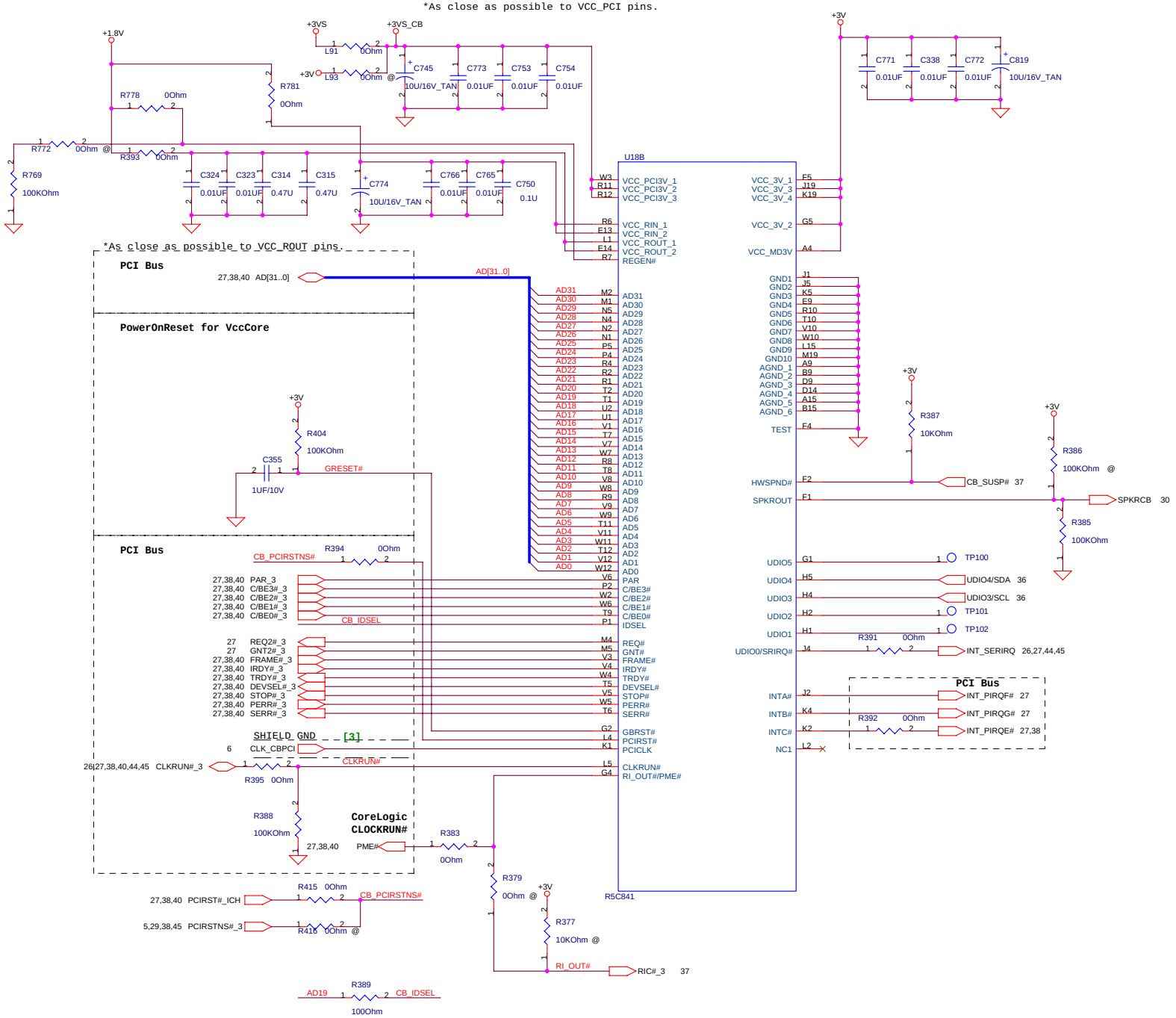




ER1.1 -> PR2.0



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: MIC PRE AMP & MIC JACK & ExtCN	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 33 OF 61		LIBRARY DATE :	



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: CardBus RICOH R5C841/PCI_B	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 34 OF 61		LIBRARY DATE :	

[1] NOT INSTALLED

[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

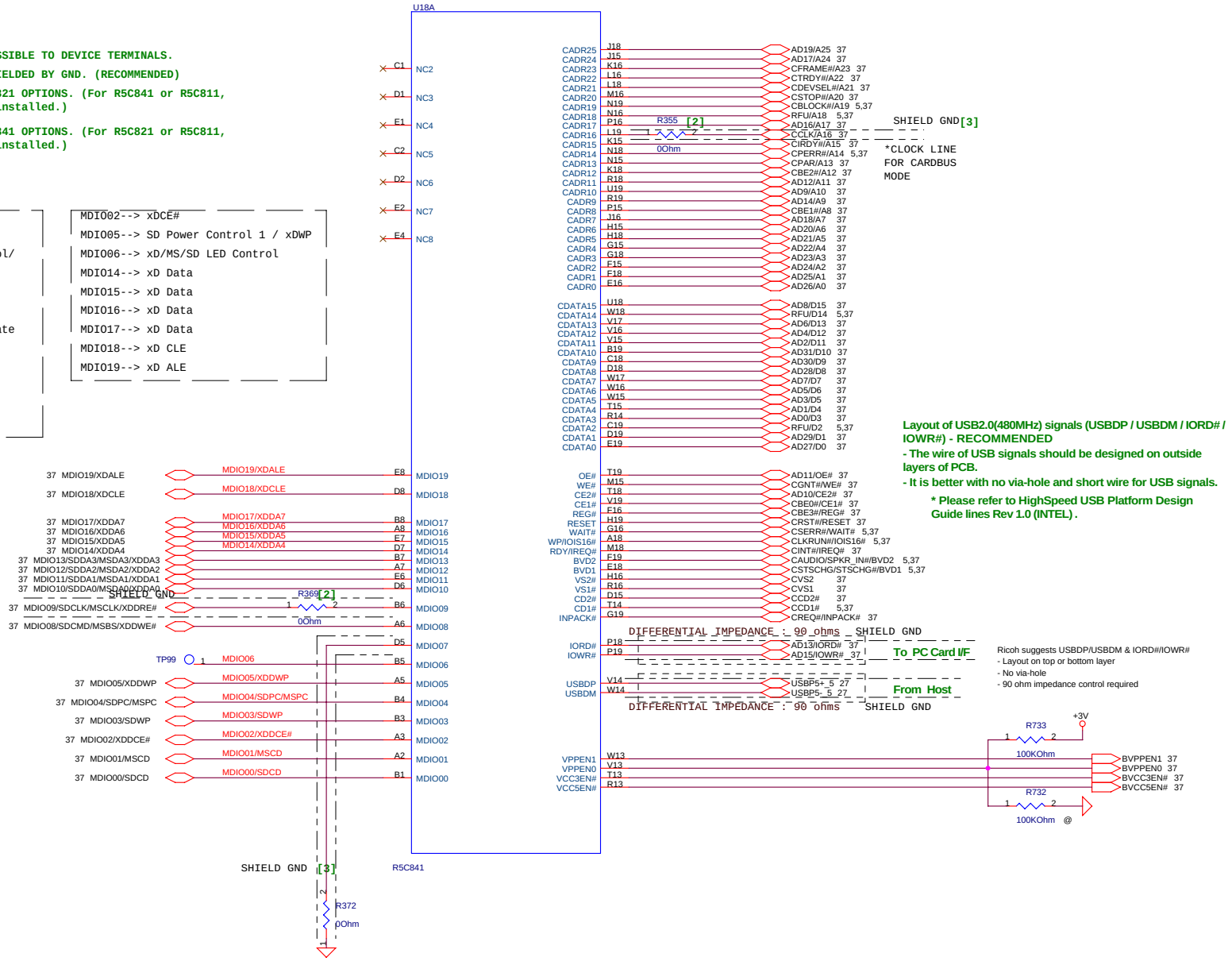
[3] CLK LINES : SHIELDED BY GND. (RECOMMENDED)

[4] R5C851 and R5C821 OPTIONS. (For R5C841 or R5C811, these parts are NOT installed.)

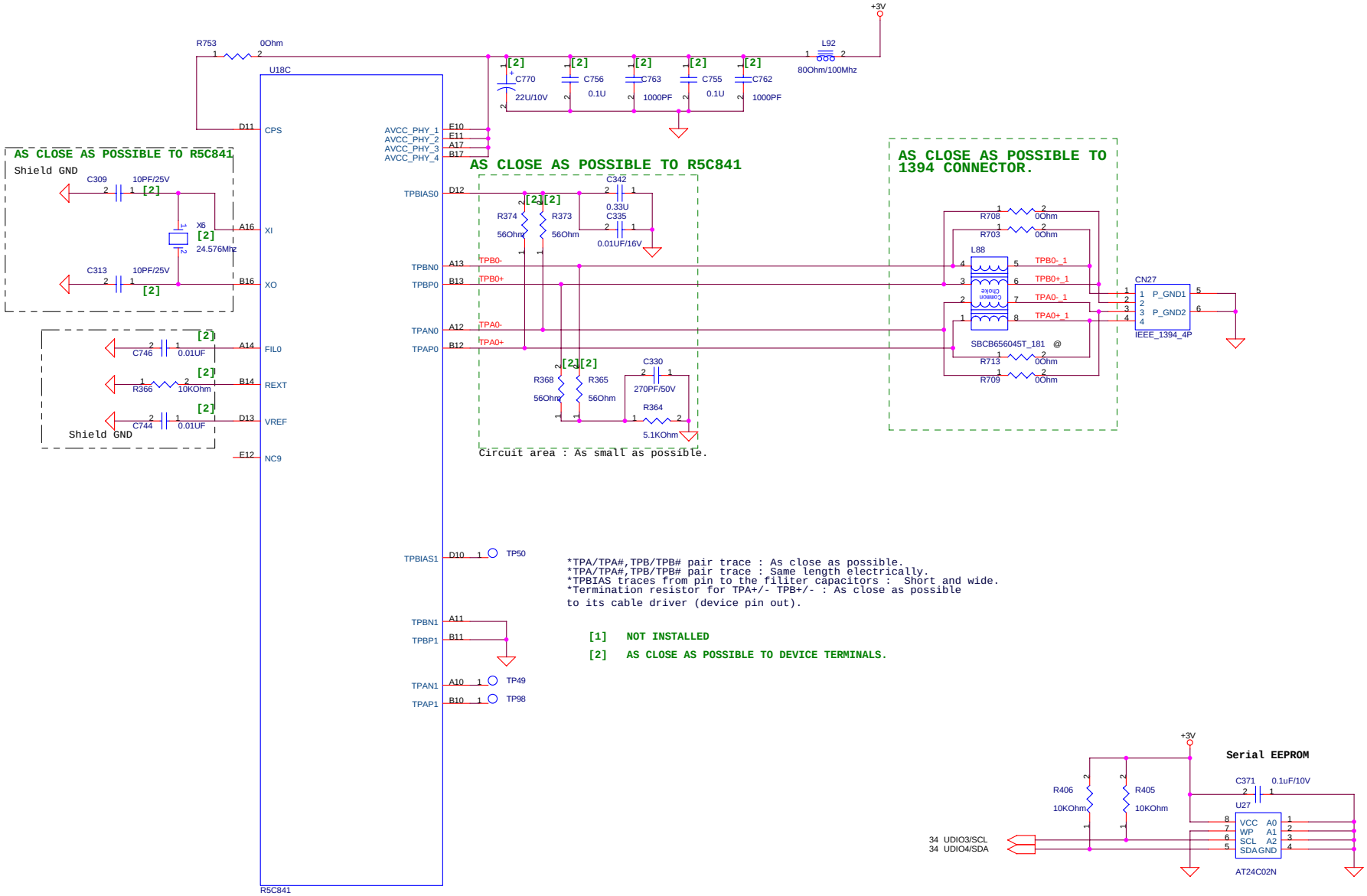
[5] R5C851 and R5C841 OPTIONS. (For R5C821 or R5C811, these parts are NOT installed.)

MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/ MS Power Control
MDIO07--> SD External Clock/ MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

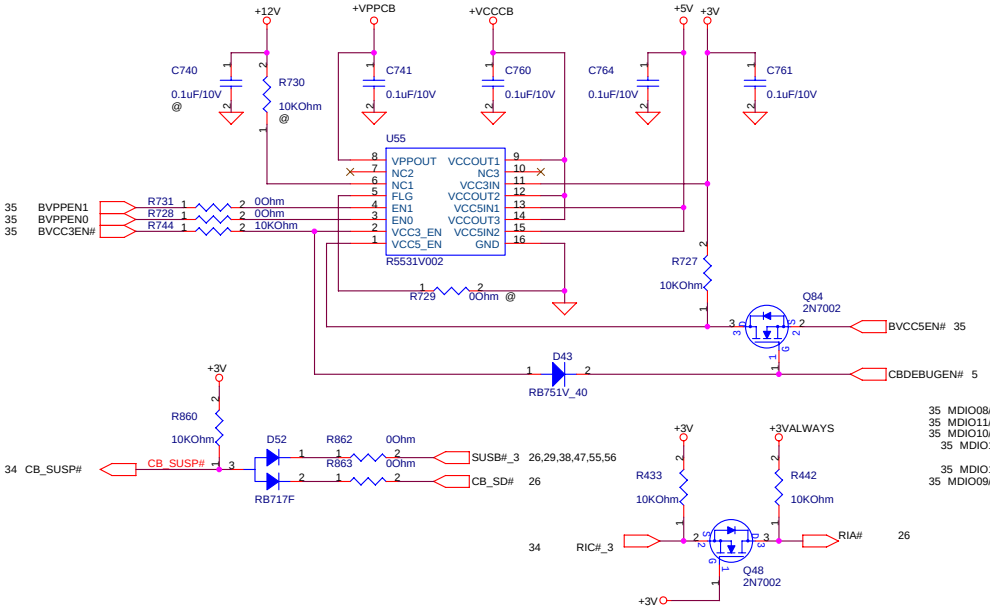


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: CardBus RICOH R5C841/PCI_A	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 35 OF 61		LIBRARY DATE :	

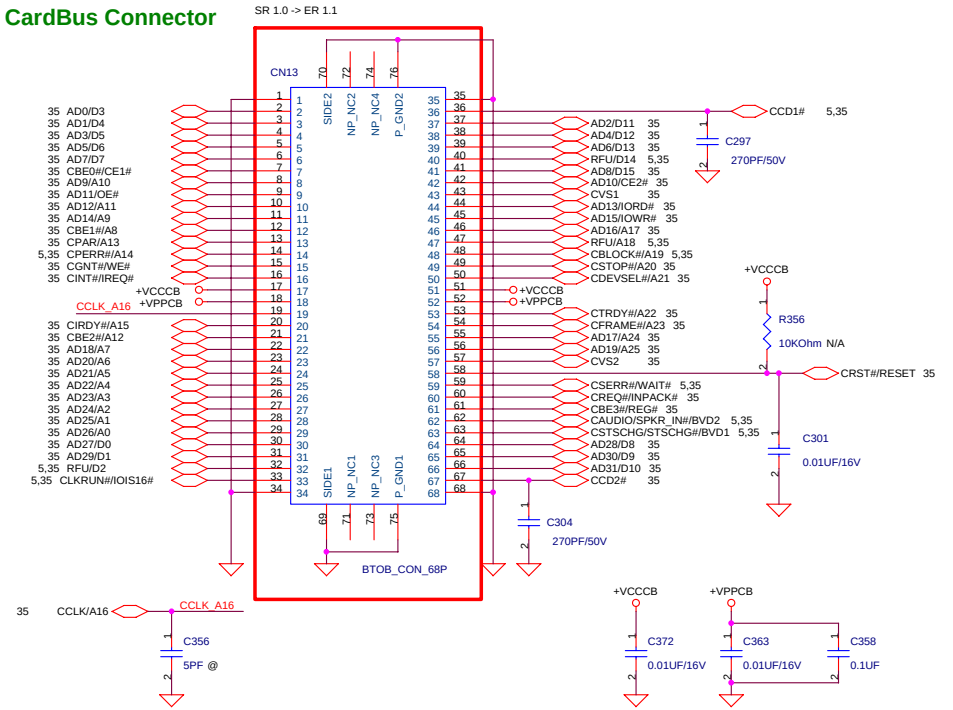


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: CardBus RICOH R5C841/PCI_C	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 36 OF 61		LIBRARY DATE :	

Power Switch



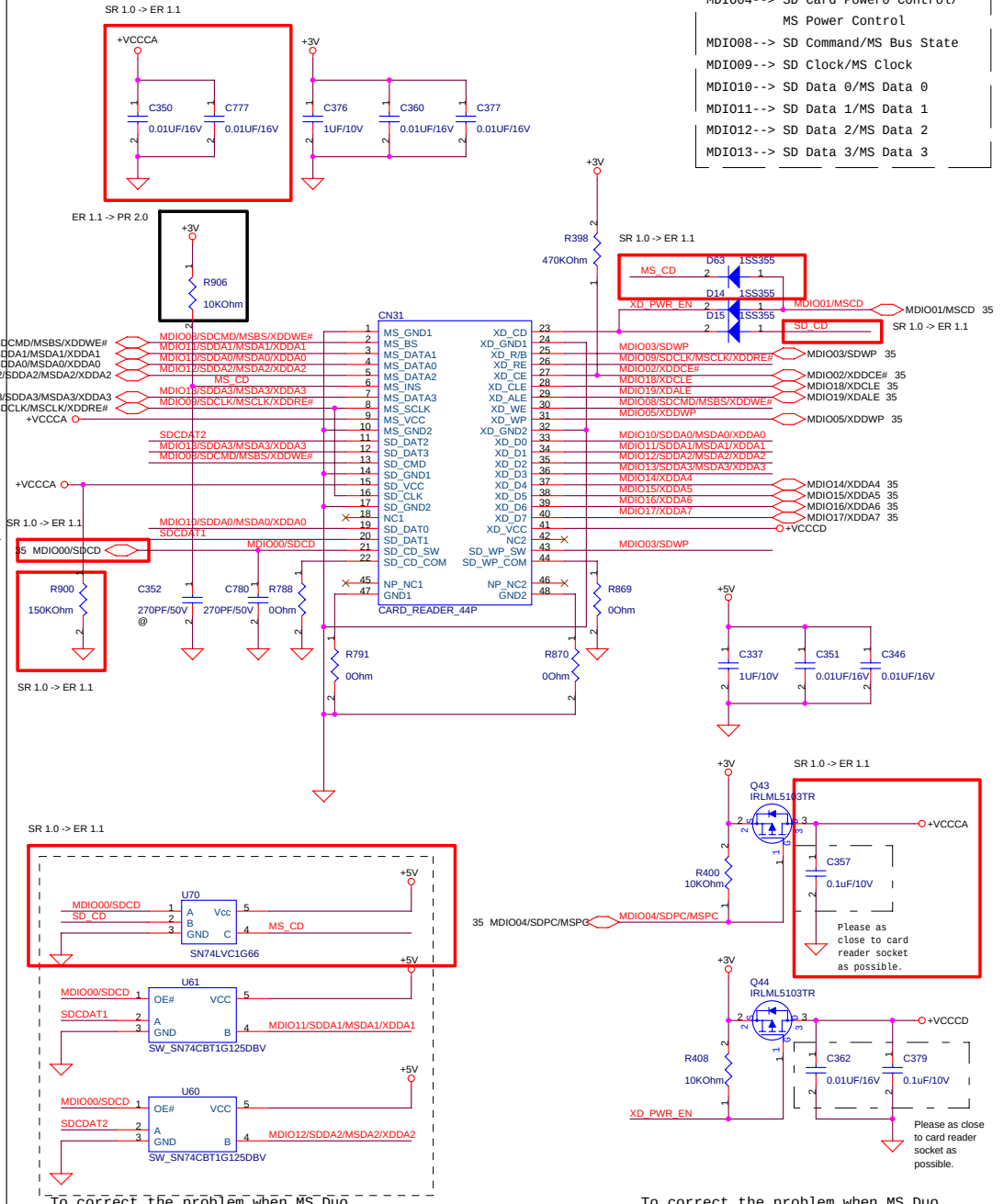
CardBus Connector



SD/MMC/MS/MS-PRO Card Reader Socket

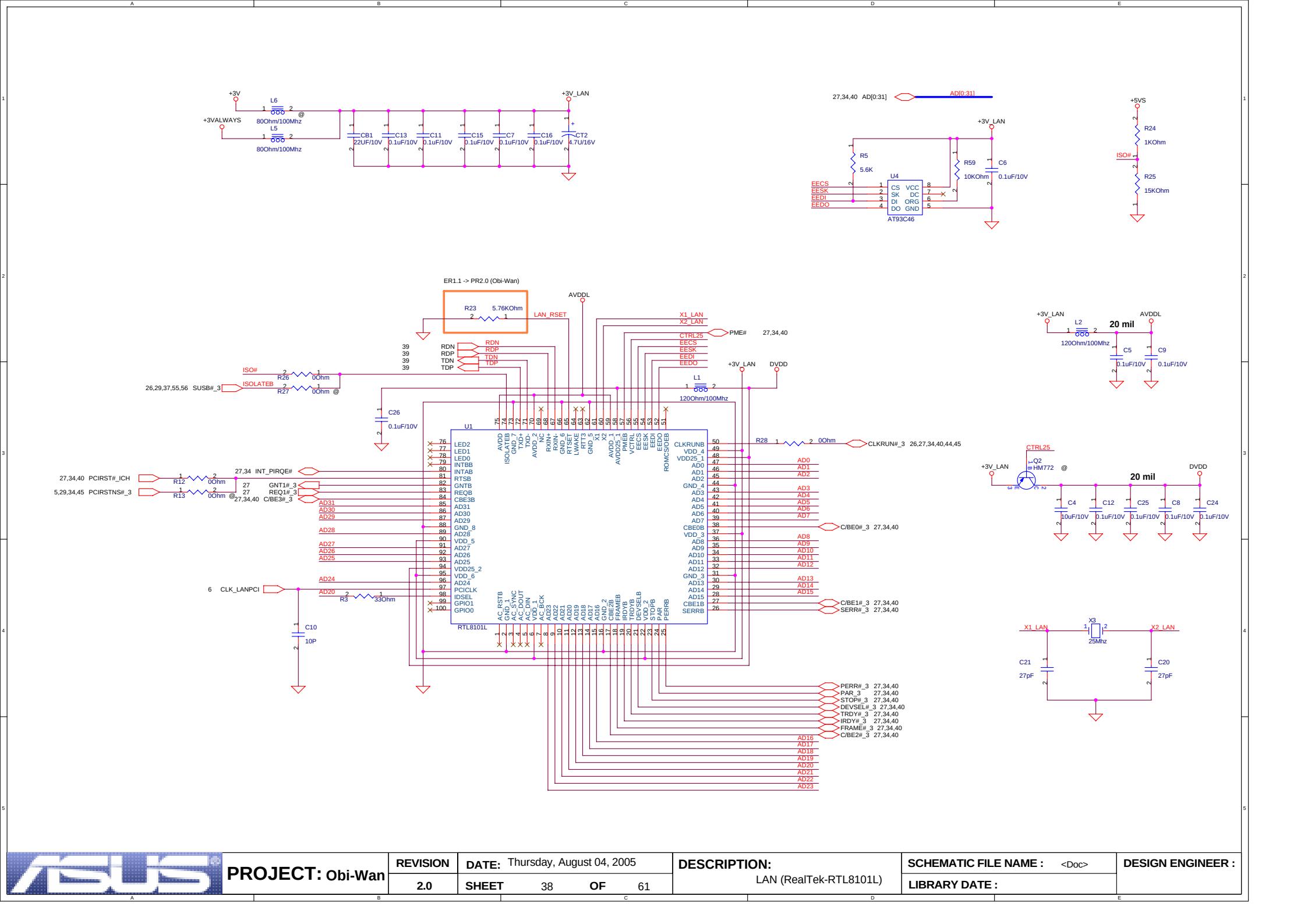
[3] CLK LINE : SHIELDED BY GND. (RECOMMENDED) [5] R5C841 OPTIONS.

```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```



PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: Cardbus & CardReader & PwrSw	SCHEMATIC FILE NAME : <Doc>
		SHEET 37 OF 61		LIBRARY DATE :

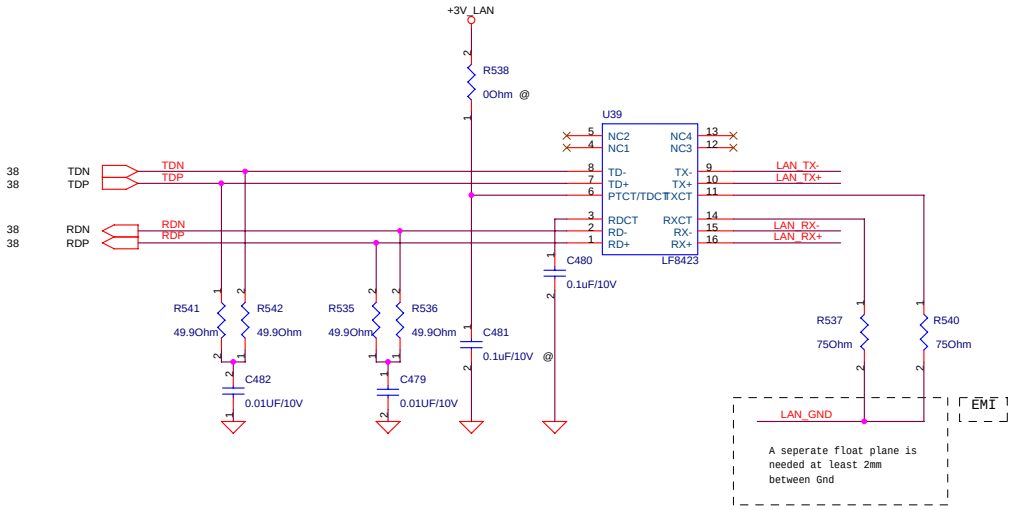
DESIGN ENGINEER :



ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** LAN (RealTek-RTL8101L)	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 38 **OF** 61		**LIBRARY DATE :**

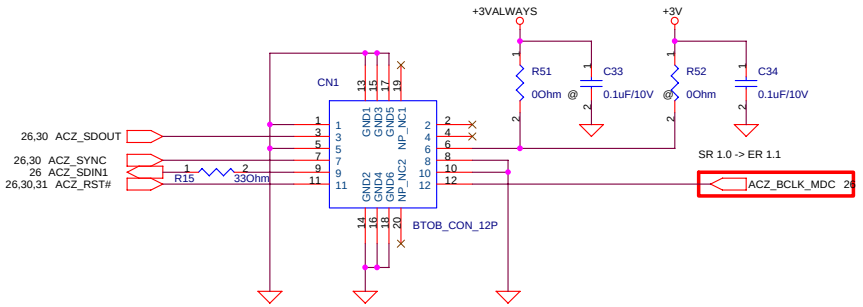
DESIGN ENGINEER :

Transformer

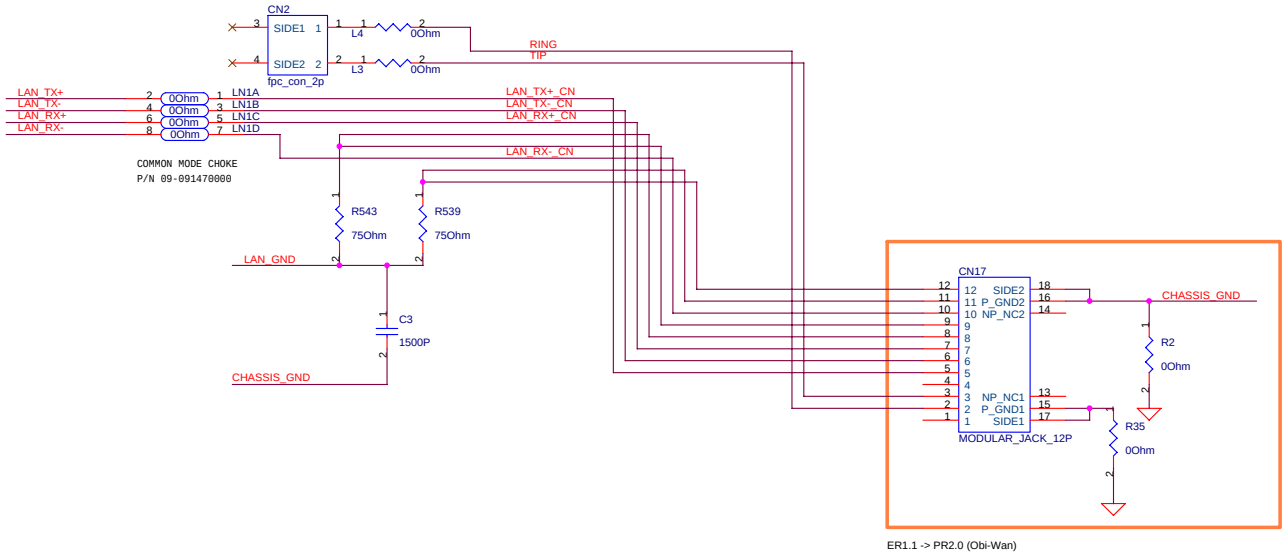


MDC Connector

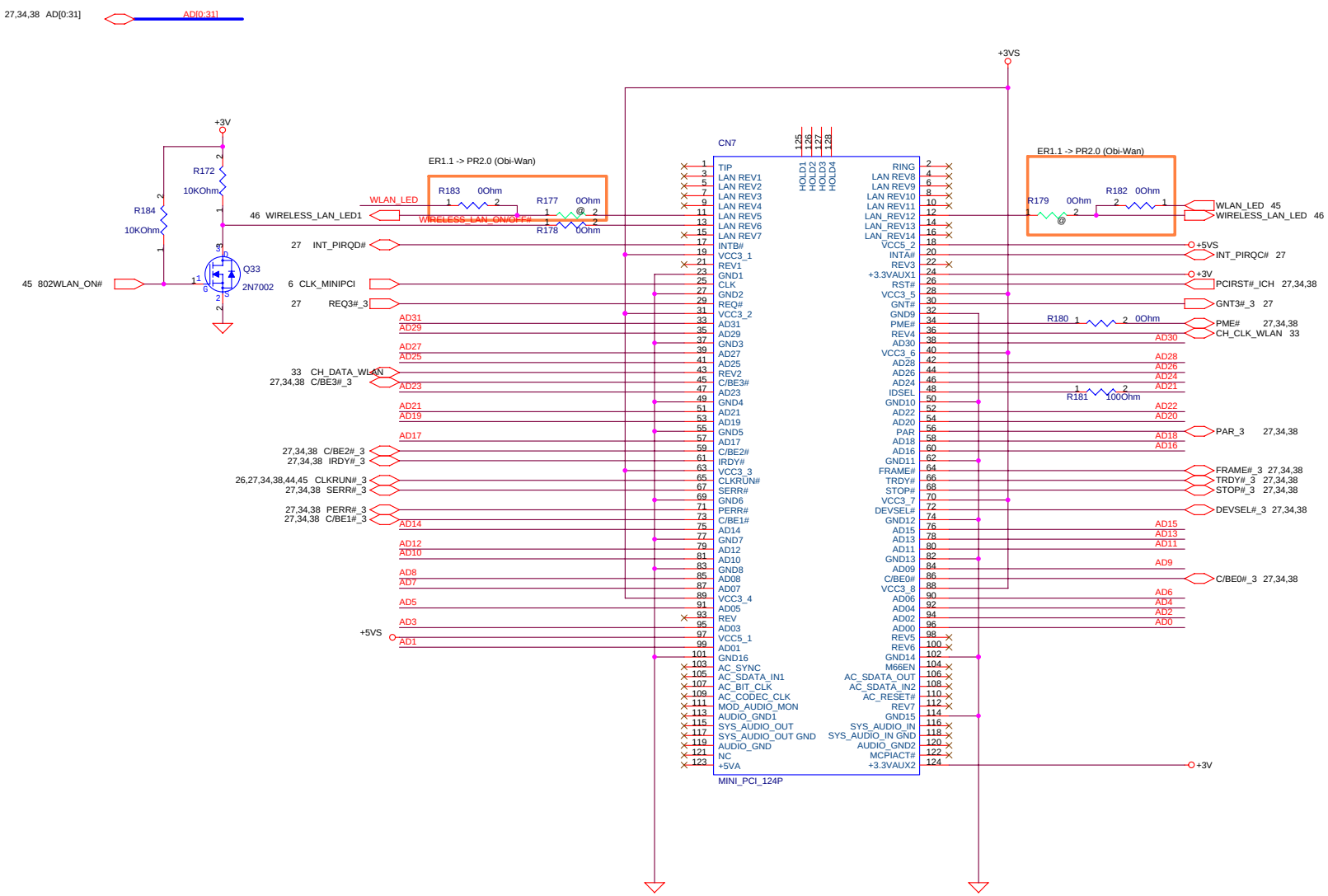
FOR MDC



RJ11/RJ45 Connector

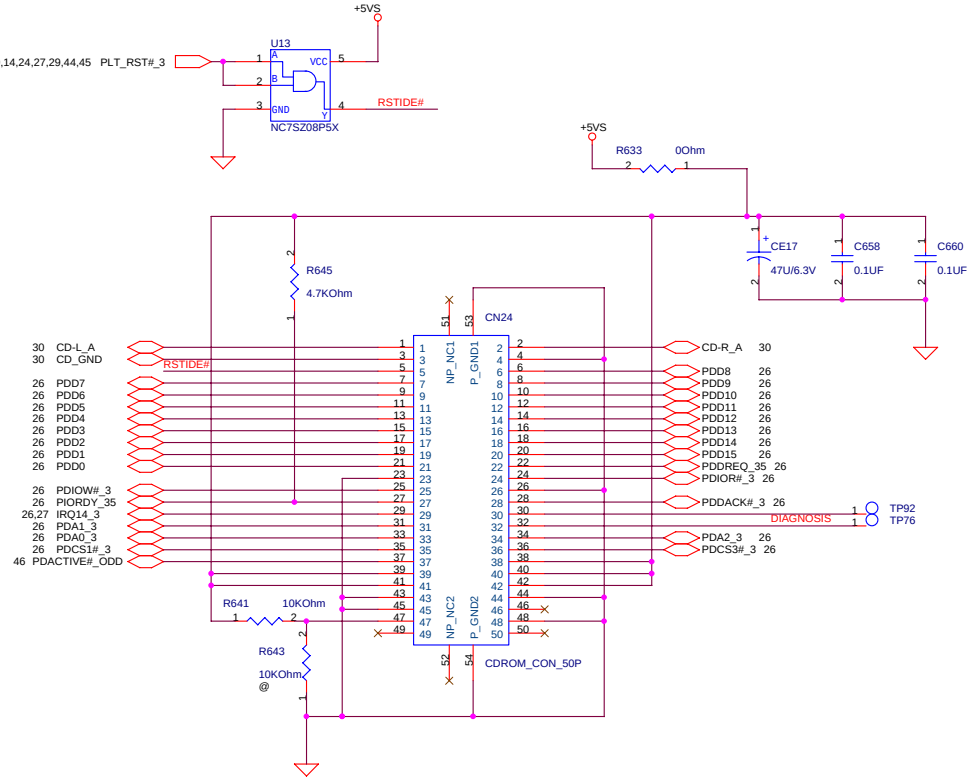


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: LAN IO & MDC	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 39 OF 61		LIBRARY DATE :	

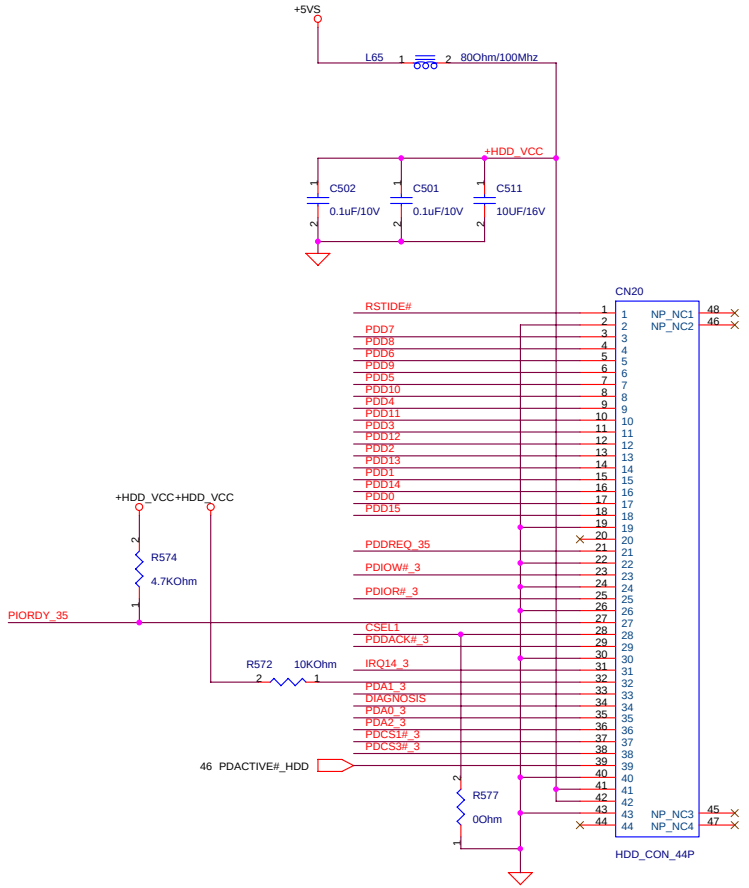


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: MiniPCI	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 40 OF 61		LIBRARY DATE :	

ODD Connector

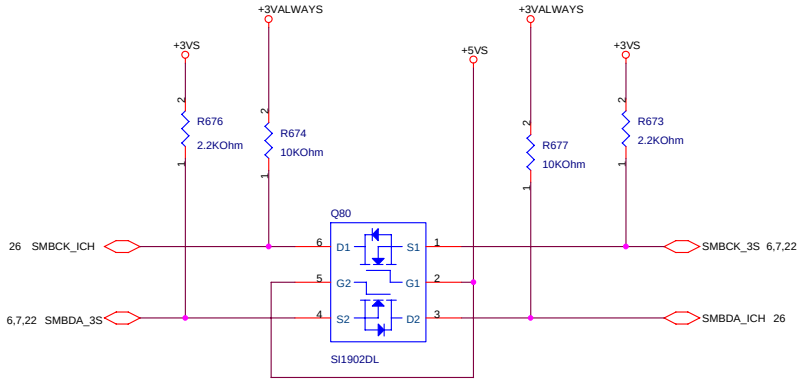


HDD Connector

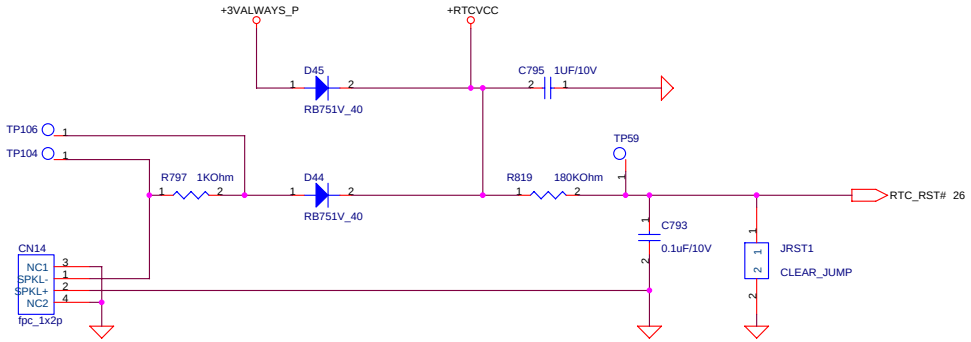


ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005 **SHEET** 41 **OF** 61	**DESCRIPTION:** HDD & CDROM CN	**SCHEMATIC FILE NAME :** <Doc> **LIBRARY DATE :** **DESIGN ENGINEER :**

SM BUS



RTC Connector



+V1.8S_PROC_VCCA3 — +V1.8S_PROC_VCCA3 3
+V1.8S_PROC_VCCA2 — +V1.8S_PROC_VCCA2 3
+V1.8S_PROC_VCCA1 — +V1.8S_PROC_VCCA1 3
+V1.8S_PROC — +V1.8S_PROC 3
+VCCP — +VCCP 3,4,5,6,8,9,11,12,26,28,50
+1.8VS — +1.8VS 3,14,15,16,56,57
+1.5VS — +1.5VS 3,9,11,16,27,28,50
+VCORE — +VCORE 4,5,7,48
+3V — +3V 5,7,29,33,34,35,36,37,38,39,40,43,44,45,46,47,51,56
+5V — +5V 5,9,28,29,30,31,33,37,43,45,46,47,56,57
+3VALWAYS — +3VALWAYS 5,24,26,27,28,29,31,37,38,39,45,47,51
+3VS — +3VS 6,7,11,14,15,16,17,22,24,25,26,27,28,29,30,33,34,40,43,44,45,47,48,51,56,57
+3VS_CLK — +3VS_CLK 6
+5VS — +5VS 7,9,24,28,29,30,31,38,40,41,43,45,46,47,56
+12V — +12V 7,31,32,37,49,56
+2.5VS — +2.5VS 9,11,13,16,28,50,57
+1.8V — +1.8V 9,11,12,20,21,22,34,50,51
+2.5VS_SYNC — +2.5VS_SYNC 9,11,13,16,28,50,57
+2.5VS_CRTDAC — +2.5VS_CRTDAC 11
+1.5VS_MPLL — +1.5VS_MPLL 11
+VCCP_GMCH — +VCCP_GMCH 3,4,5,6,8,9,11,12,26,28,50
+2.5VS_3GBG — +2.5VS_3GBG 11
+1.5VS_3GPLL — +1.5VS_3GPLL 11
+1.5VS_DDRDLL — +1.5VS_DDRDLL 11
+1.5VS_DLVDS — +1.5VS_DLVDS 3,9,11,16,27,28,50
+2.5VS_ALVDS — +2.5VS_ALVDS 9,11,13,16,28,50,57
+2.5VS_HV — +2.5VS_HV 9,11,13,16,28,50,57
+1.5VS_TVDAC — +1.5VS_TVDAC 3,9,11,16,27,28,50
+1.5VS_QTVDAC — +1.5VS_QTVDAC 11
+3VS_TVDACA — +3VS_TVDACA 11
+3VS_TVDACB — +3VS_TVDACB 11
+3VS_TVDACC — +3VS_TVDACC 11
+3VS_TVBG — +3VS_TVBG 11
+1.5VS_HPLL — +1.5VS_HPLL 11
+1.5VS_DPLLB — +1.5VS_DPLLB 11
+1.5VS_DPLLA — +1.5VS_DPLLA 11
+1.5VS_HMPLL — +1.5VS_HMPLL 11
+VCC_GMCH_CORE — +VCC_GMCH_CORE 11,12,50,51
+VCC_GMCH — +VCC_GMCH 11,12,50,51
SM_VREF_DDR — SM_VREF_DDR 9,20,21,22
M_VREF_DIMM1 — M_VREF_DIMM1 9,20,21,22
+0.9VS — +0.9VS 23,51
+12VS — +12VS 24,25,56
LCD_+3VS — LCD_+3VS 25
LCD_VCC — LCD_VCC 25
AC_BAT_SYS — AC_BAT_SYS 25,48,49,50,51,52,53,57
+RTCVCC — +RTCVCC 26,28
+1.5VALWAYS — +1.5VALWAYS 28,51
+5VALWAYS — +5VALWAYS 28,50
+3VALWAYS_P — +3VALWAYS_P 29,46,47,51
+5VA — +5VA 30,32,33
+5VAMP — +5VAMP 31,32
+5VAMP_PVDD — +5VAMP_PVDD 31
+3V_BT — +3V_BT 33
+3VS_CB — +3VS_CB 34
+VCCCA — +VCCCA 37
+VCCCD — +VCCCD 37
+VCCCB — +VCCCB 37
+VPPCB — +VPPCB 37

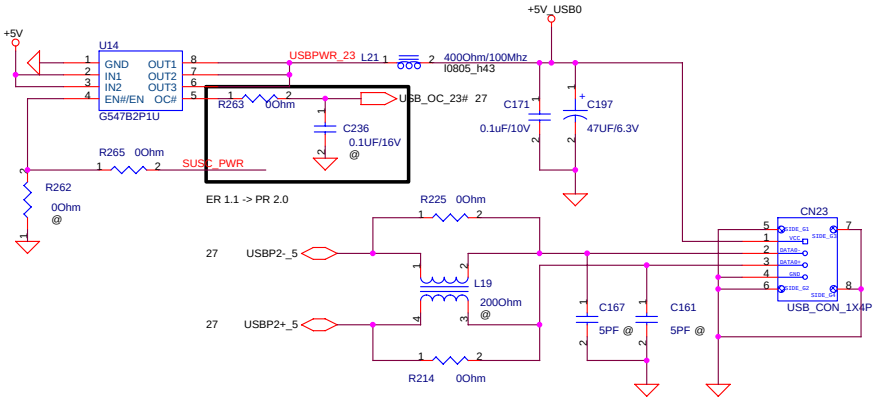
+5VS_FAN1 — +5VS_FAN1 7
+3V_LAN — +3V_LAN 38,39
AVDDL — AVDDL 38
DVDD — DVDD 38
+HDD_VCC — +HDD_VCC 41
+5V_USB0 — +5V_USB0 43
+5V_USB1 — +5V_USB1 43
+5V_USB2 — +5V_USB2 43
+5V_USB3 — +5V_USB3 43
A/D_DOCK_IN — A/D_DOCK_IN 44,52,53
+5VLCM — +5VLCM 45,46,52,55
+1.2VSP — +1.2VSP 14,16,57
+ATI_MEM — +ATI_MEM 15,16,18,19,56
LVDDR — LVDDR 16,57
+ATI_VCORE — +ATI_VCORE 16,57

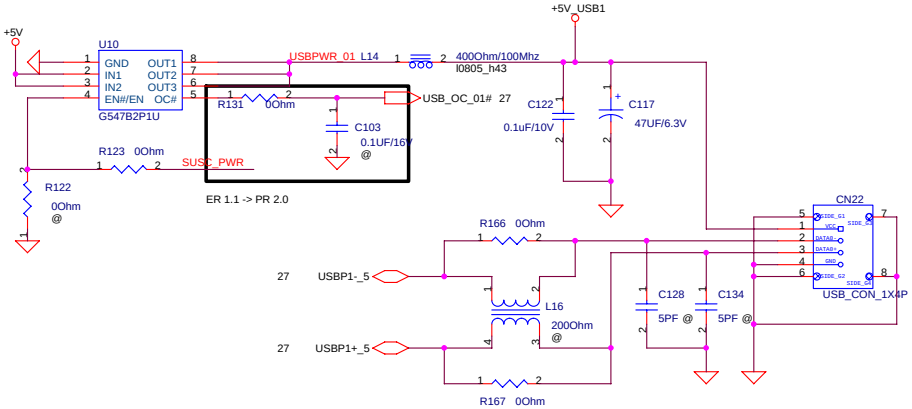
POWER

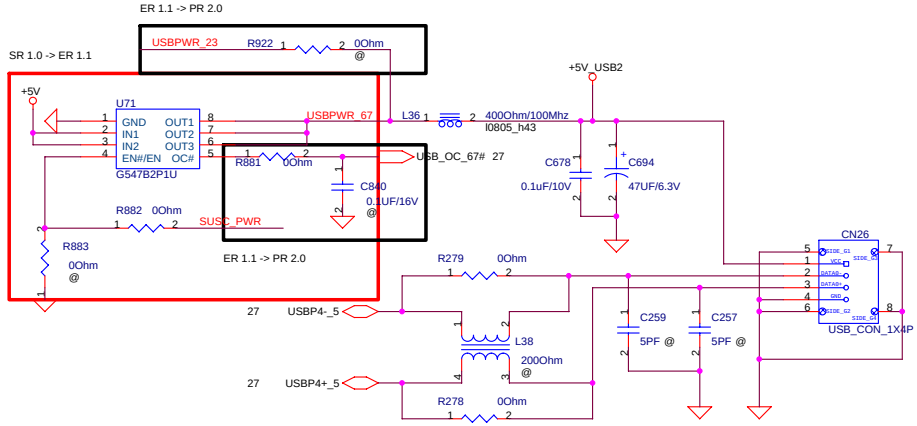
+3VO — +3VO 48,49,50,56
+5VO — +5VO 48,49,50,52,56
+3VAO — +3VAO 49,51,55,56
+5VAO — +5VAO 49
+12VO — +12VO 7,31,32,37,49,56
VREF5 — VREF5 50,54,56
+2.5VO — +2.5VO 50
+1.8VO — +1.8VO 50,56
+1.5VO — +1.5VO 50
+1.05VO — +1.05VO 50
+1.5VAO — +1.5VAO 51
A/D_VIN — A/D_VIN 52,53
A/D_VIN_O — A/D_VIN_O 52,53
BAT — BAT 52,53,54
+5VCHG — +5VCHG 52,53
+2.5VREF — +2.5VREF 52
BAT_S — BAT_S 52,54
MAX1909_LDO — MAX1909_LDO 53

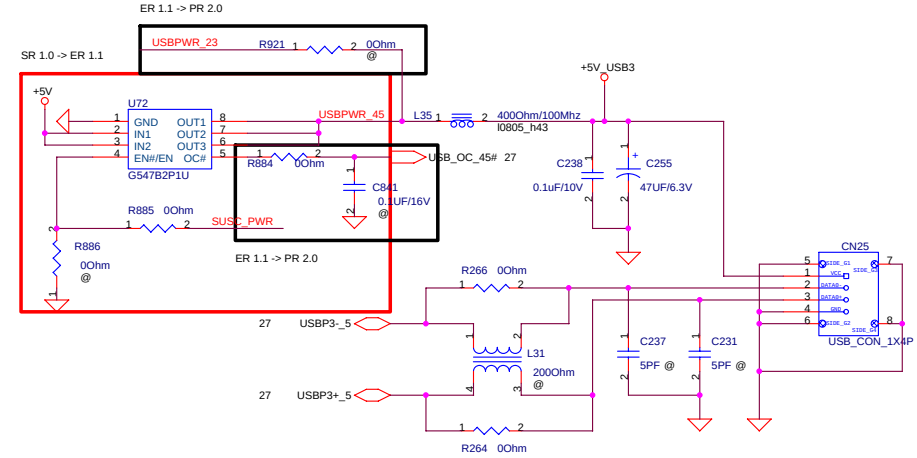
ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** SM_BUS & RTC CN	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 42 **OF** 61		**LIBRARY DATE :**

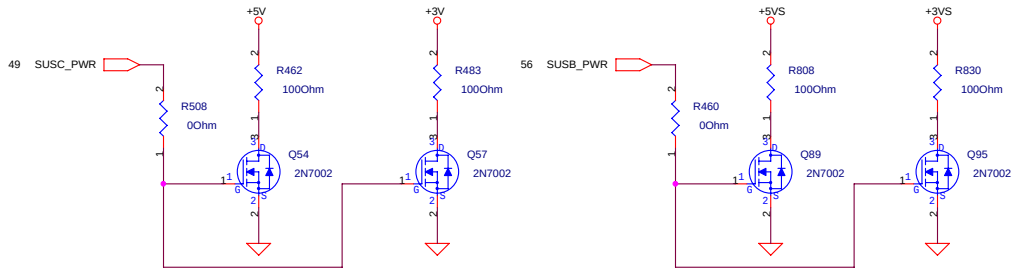
DESIGN ENGINEER :









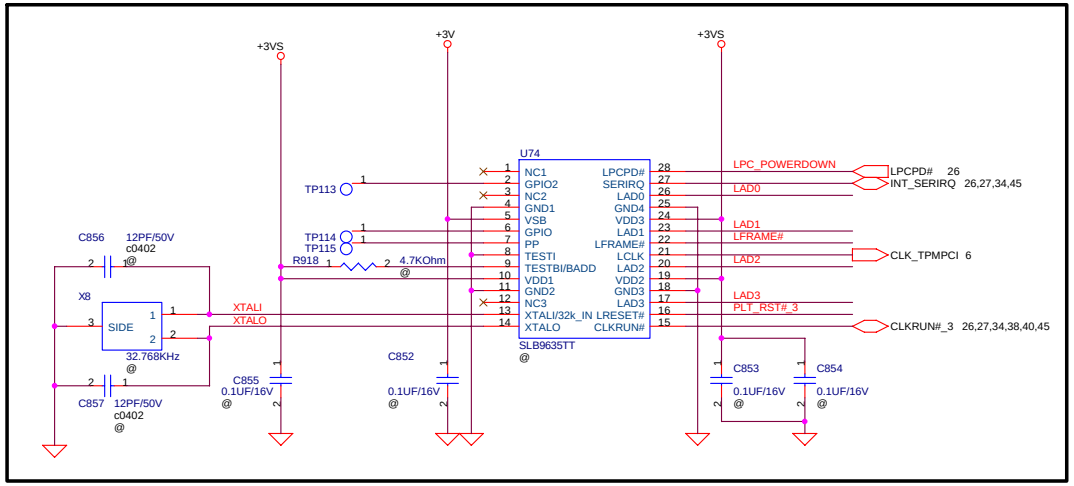


PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: 4*USB2.0 CN	SCHEMATIC FILE NAME : <Doc>
		SHEET 43 OF 61		LIBRARY DATE :

DESIGN ENGINEER :

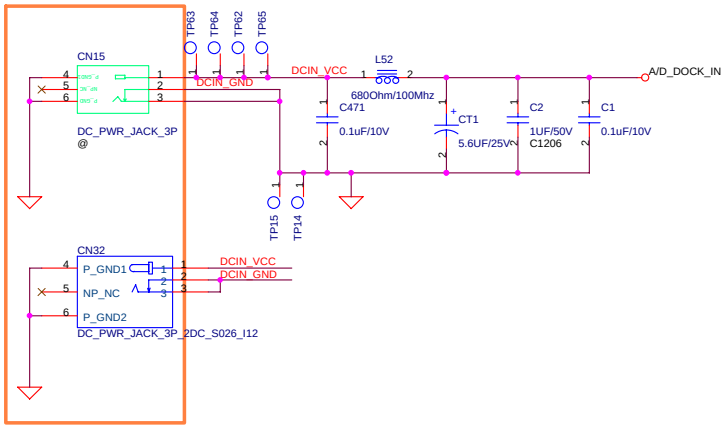
TPM 1.2 Infieon

ER 1.1 -> PR 2.0



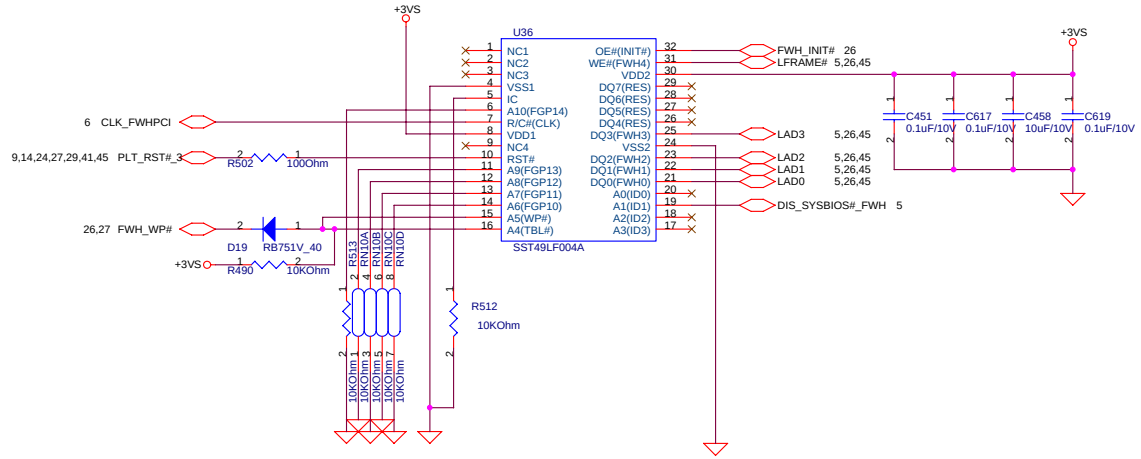
DCIN JACK

Co-Layout

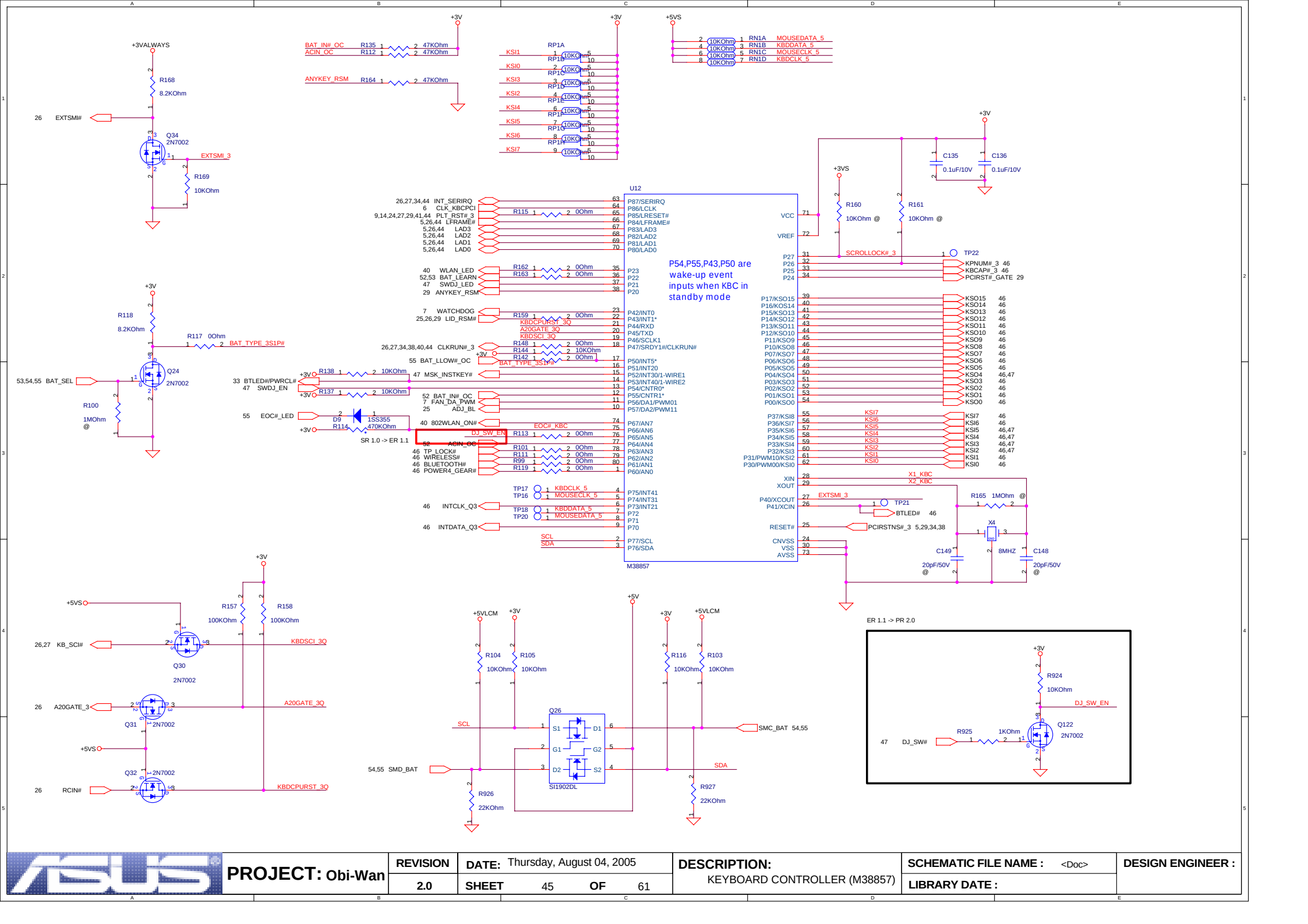


ER1.1 -> PR2.0 (Obi-Wan)

FWH



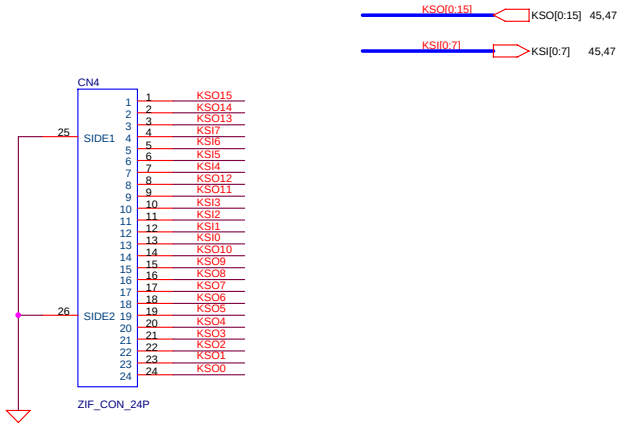
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: DCIN Jack & FWH	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 44 OF 61		LIBRARY DATE :	



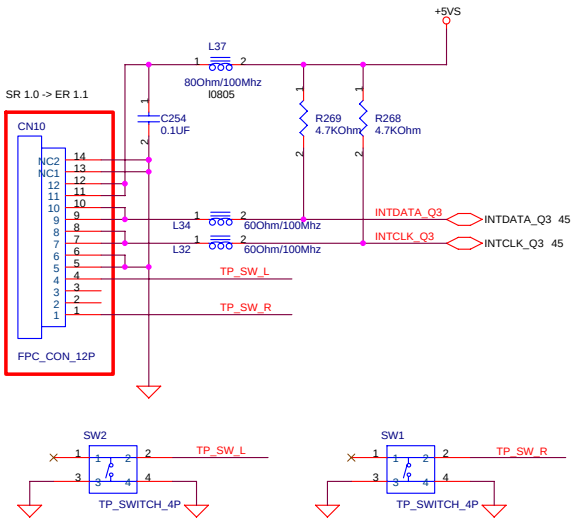
ASUS	**PROJECT:** Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** KEYBOARD CONTROLLER (M38857)	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 45 **OF** 61		**LIBRARY DATE :**

DESIGN ENGINEER :

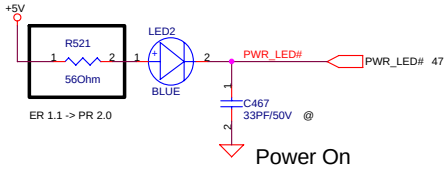
Internal Keyboard



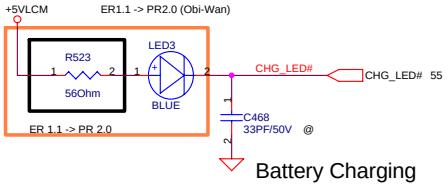
TP



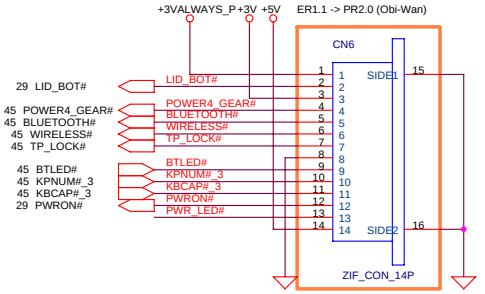
LEDs

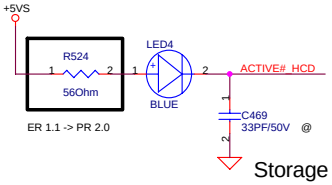


Power On

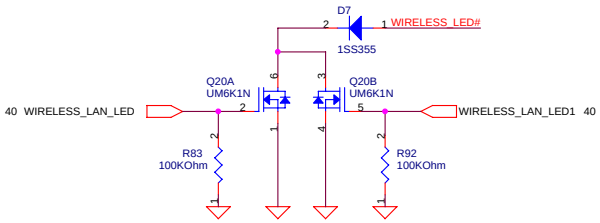


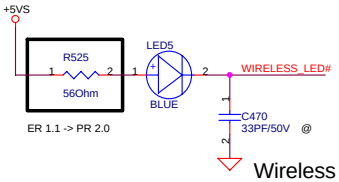
Battery Charging



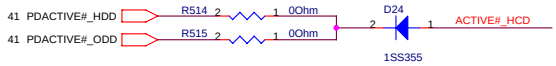


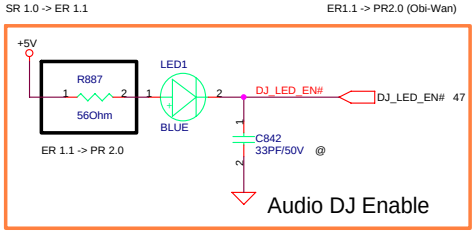
Storage Access





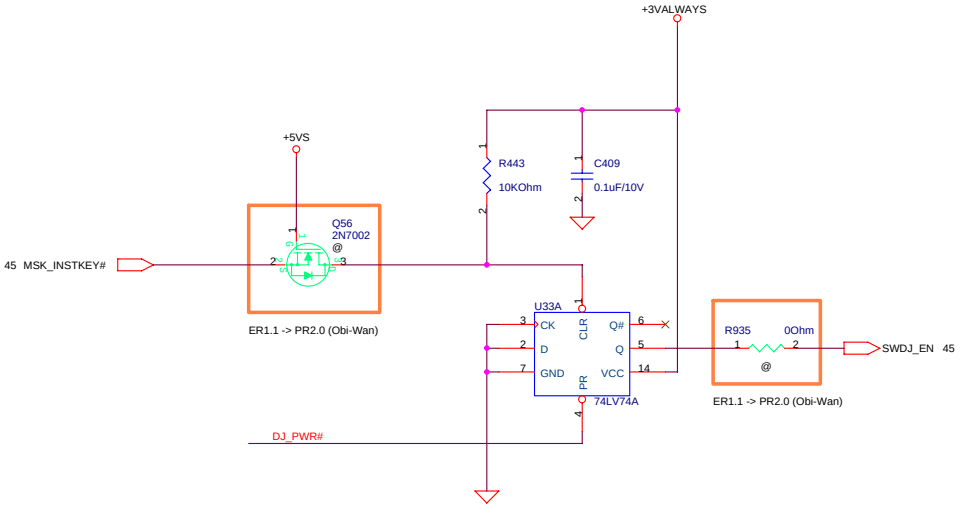
Wireless Enabling

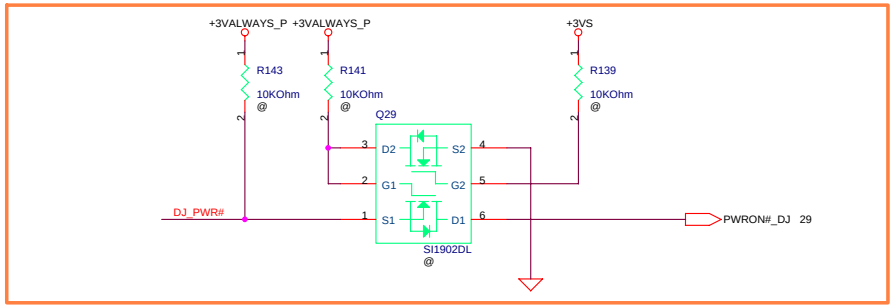


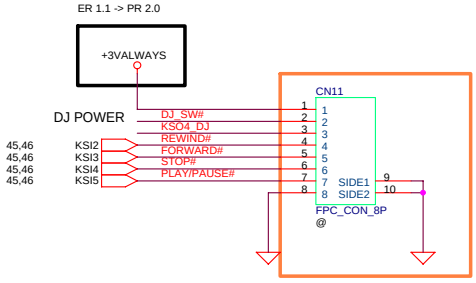


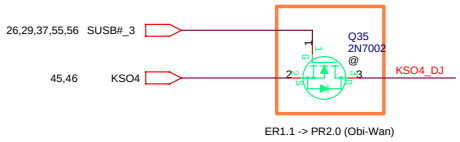
Audio DJ Enable

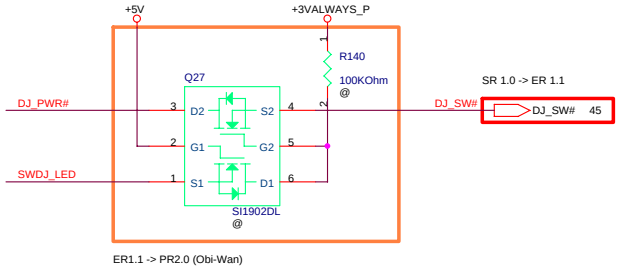
PROJECT: Obi-Wan	REVISION 2.0	DATE: Thursday, August 04, 2005	DESCRIPTION: LEDs & Internal KB TP	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 46 OF 61		LIBRARY DATE :	

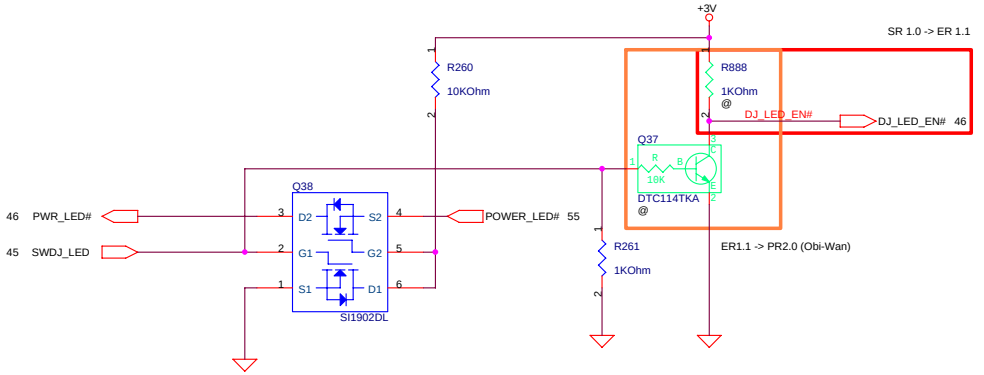




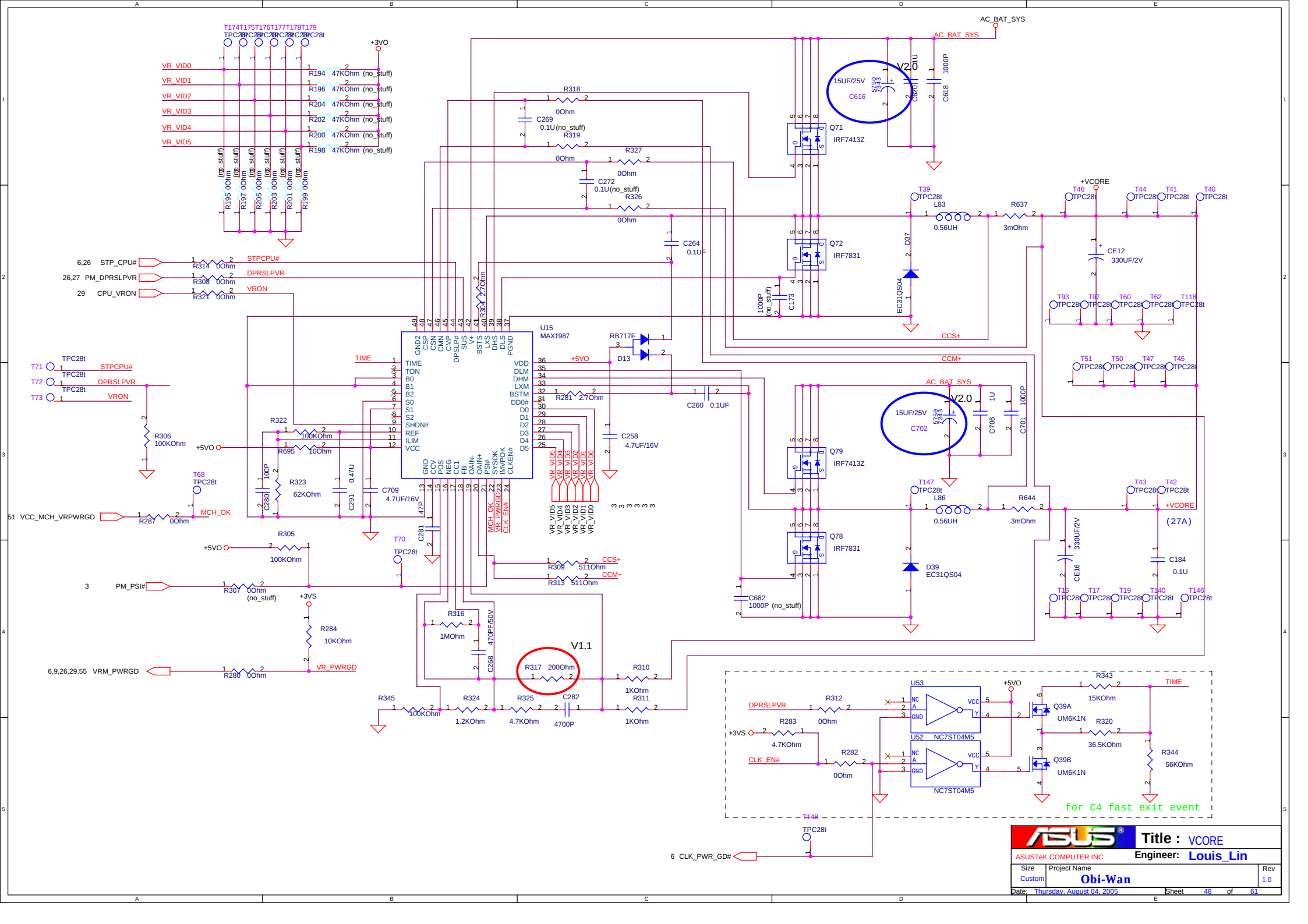








PROJECT: Obi-Wan	**REVISION** 2.0	**DATE:** Thursday, August 04, 2005	**DESCRIPTION:** AUDIO DJ	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 47 **OF** 61		**LIBRARY DATE :**	



Title :	VCORE
ASUSTeK COMPUTER INC	Engineer: Louis_Lin
Size: Custom	Project Name: Obi-Wan
Rev	1.0
Date:	Thursday, August 04, 2005
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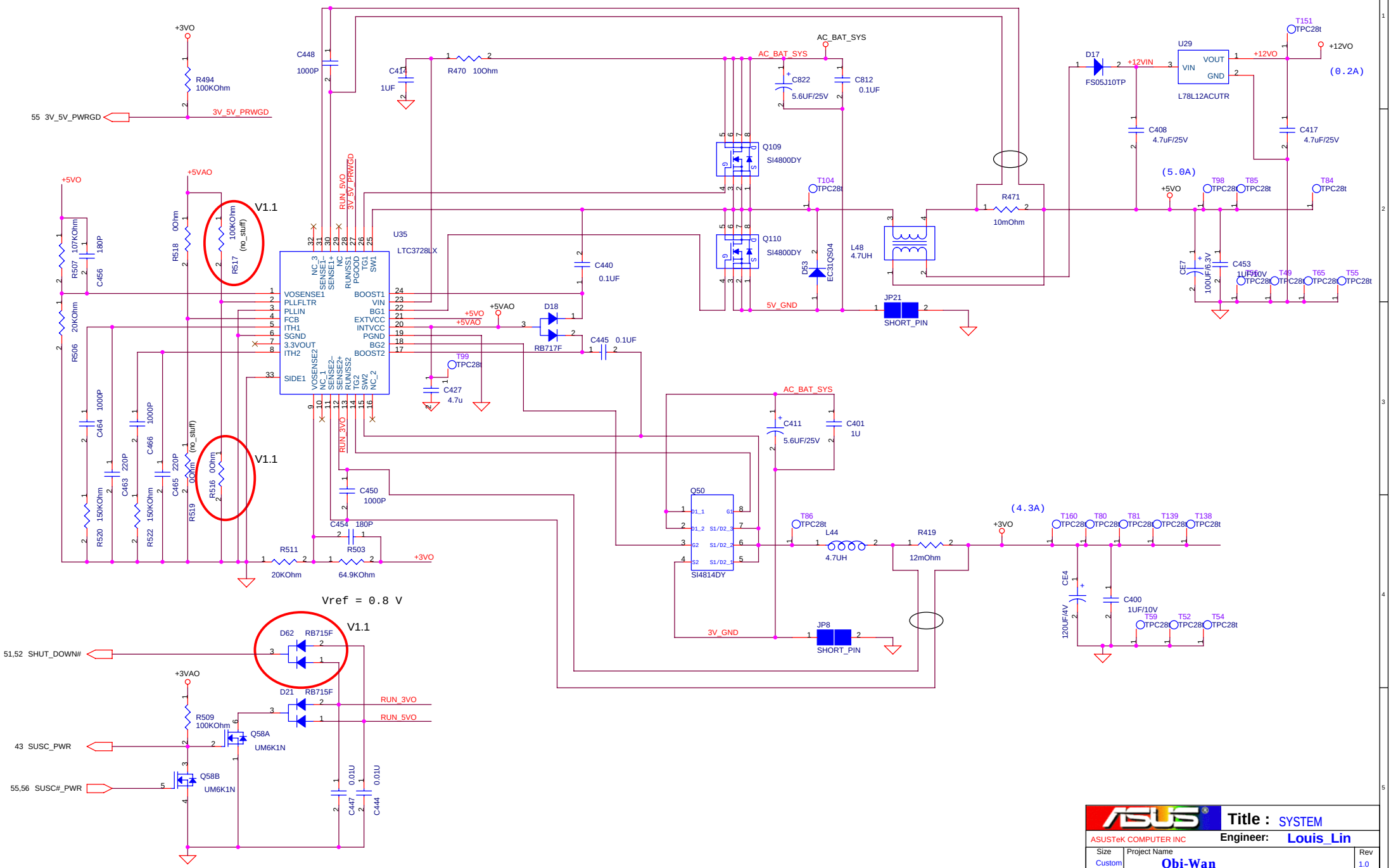
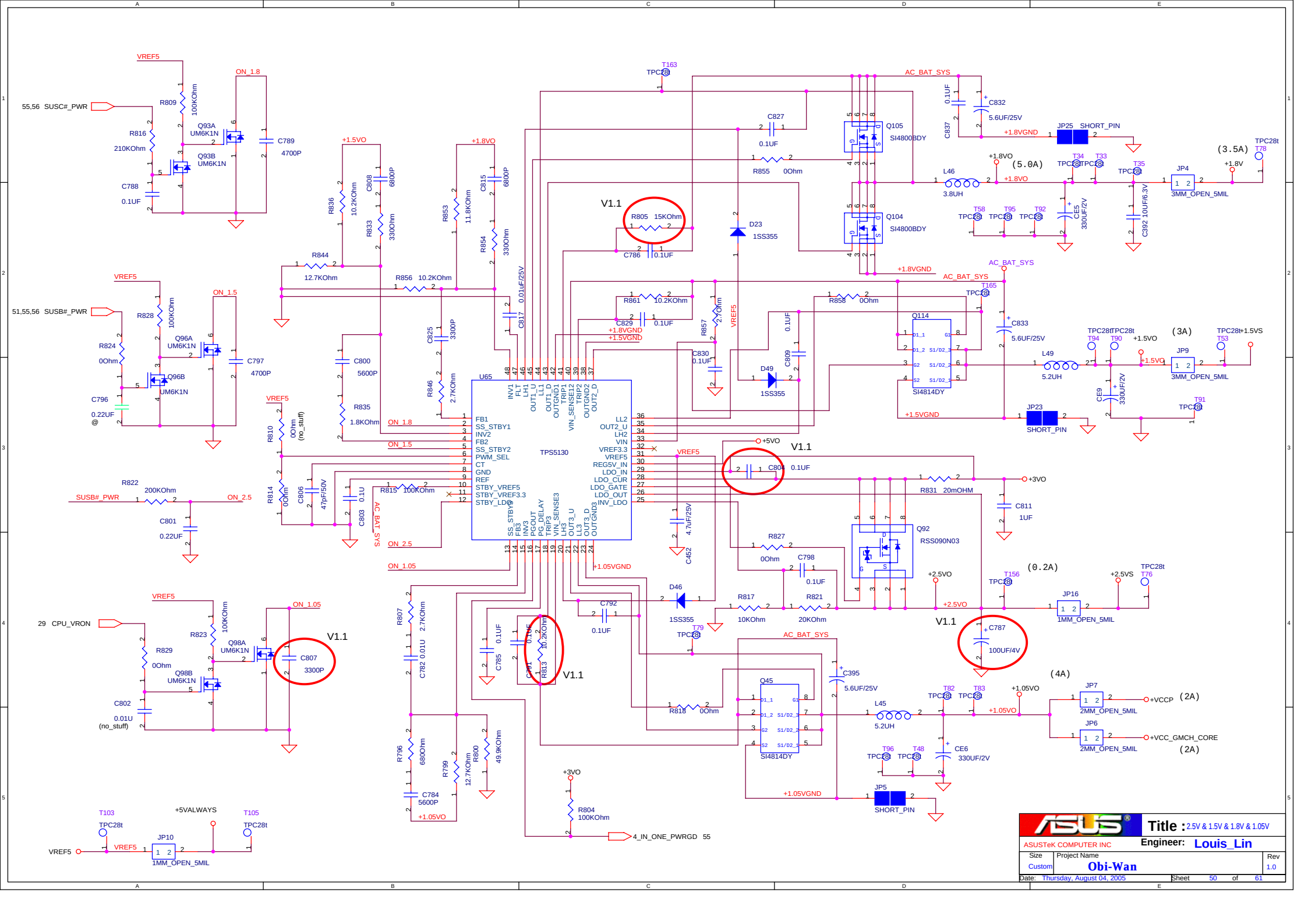
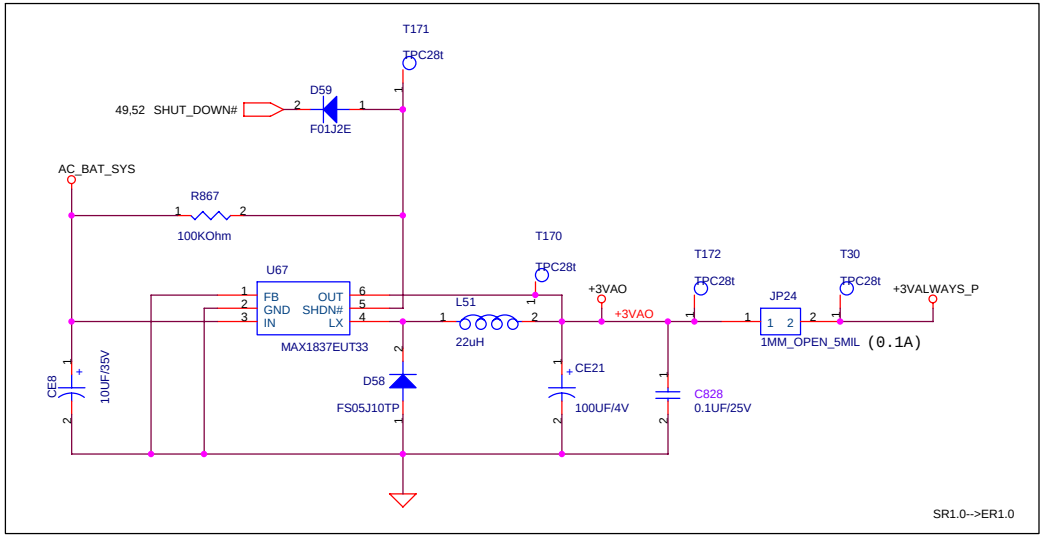
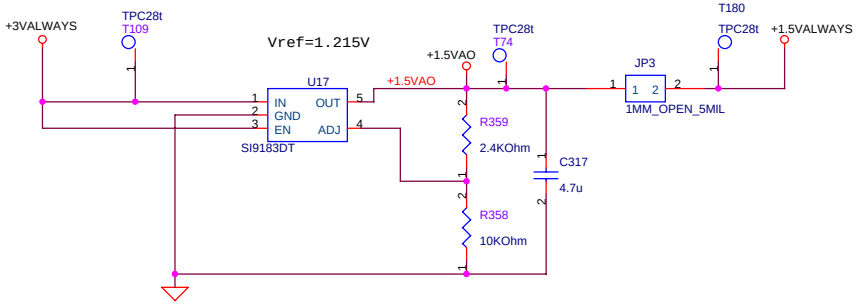
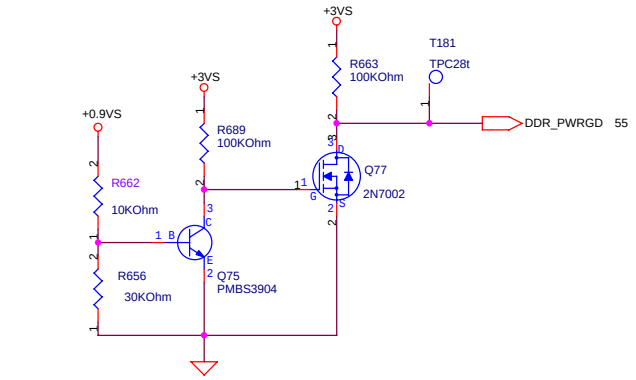


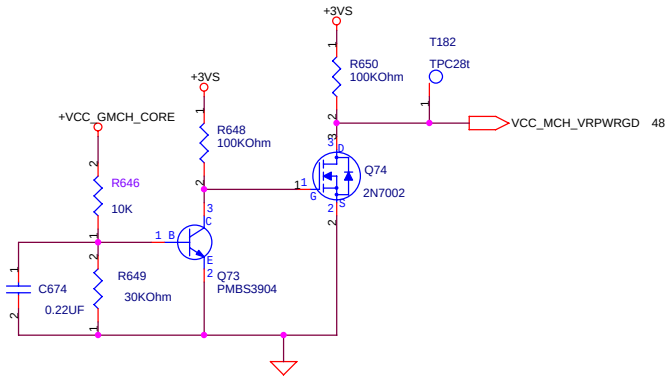
ASUSTeK COMPUTER INC	Title : SYSTEM	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 49 of 61	

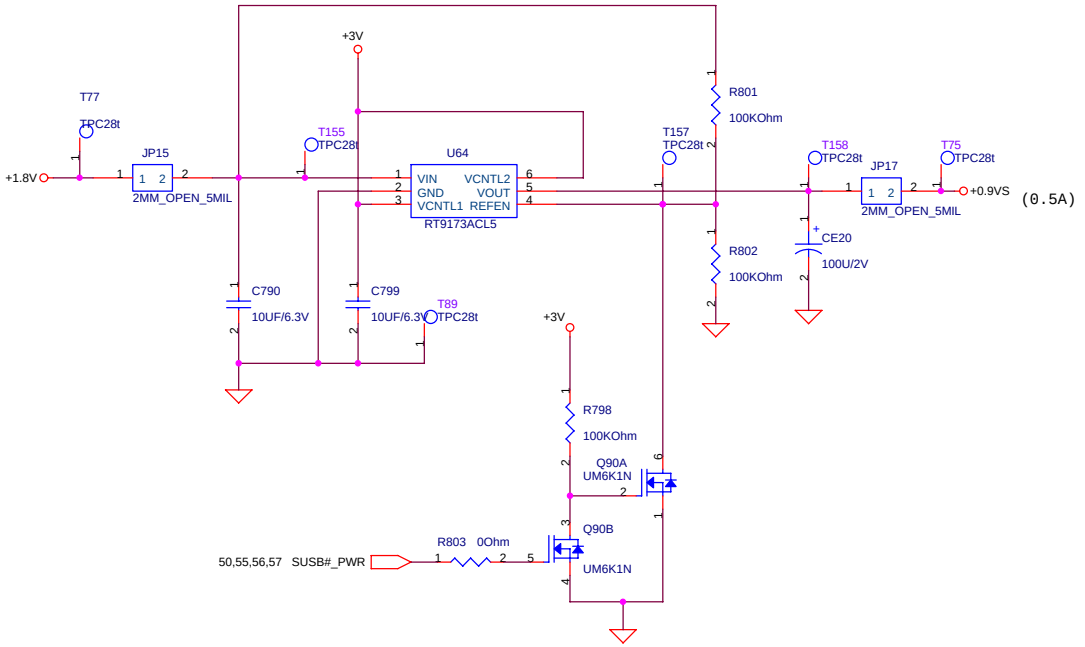

TPS5130
U65
VREF5
ON_1.8
ON_1.5
ON_2.5
ON_1.05
AC_BAT_SYS
+1.8VGND
+1.5VGND
+1.05VGND
+5VO
+3VO
+2.5VO
+1.8VO
+1.5VO
+1.05VO
+2.5VS
+5VALWAYS
V1.1
55,56 SUSC#_PWR
51,55,56 SUSB#_PWR
29 CPU_VRON
SUSB#_PWR
4_IN_ONE_PWRGD 55
Q105 SI4800BDY
Q104 SI4800BDY
Q114 SI4814DY
Q45 SI4814DY
Q92 RSS090N03
Q93A UM6K1N
Q93B UM6K1N
Q96A UM6K1N
Q96B UM6K1N
Q98A UM6K1N
Q98B UM6K1N
D23 1SS355
D49 1SS355
D46 1SS355
L46 3.8UH
L49 5.2UH
L45 5.2UH
JP25 SHORT_PIN
JP23 SHORT_PIN
JP5 SHORT_PIN
JP4 3MM_OPEN_5MIL
JP9 3MM_OPEN_5MIL
JP16 1MM_OPEN_5MIL
JP7 2MM_OPEN_5MIL
JP6 2MM_OPEN_5MIL
JP10 1MM_OPEN_5MIL
(3.5A)
(5.0A)
(3A)
(0.2A)
(4A)
(2A)
(2A)
Title : 2.5V & 1.5V & 1.8V & 1.05V
ASUSTeK COMPUTER INC
Engineer: Louis_Lin
Size: Custom
Project Name: Obi-Wan
Rev: 1.0
Date: Thursday, August 04, 2005
Sheet 50 of 61



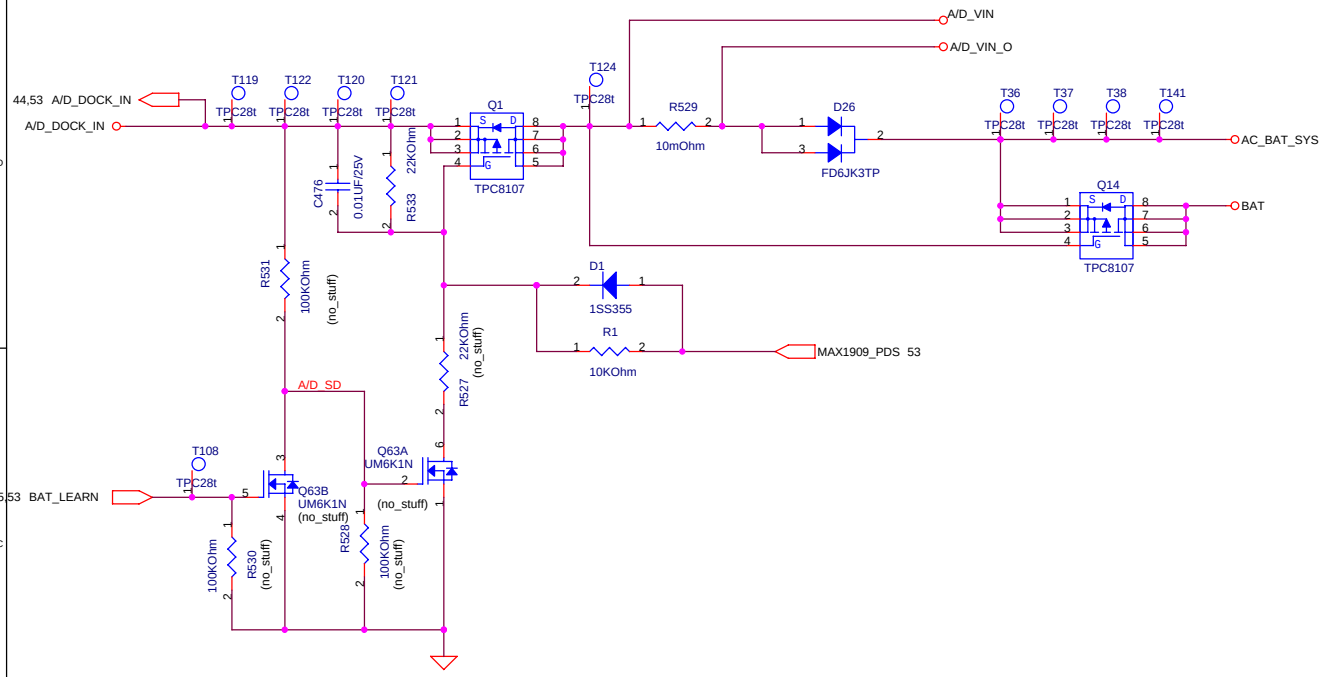




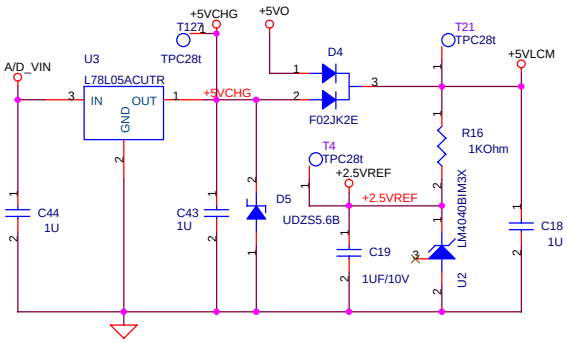




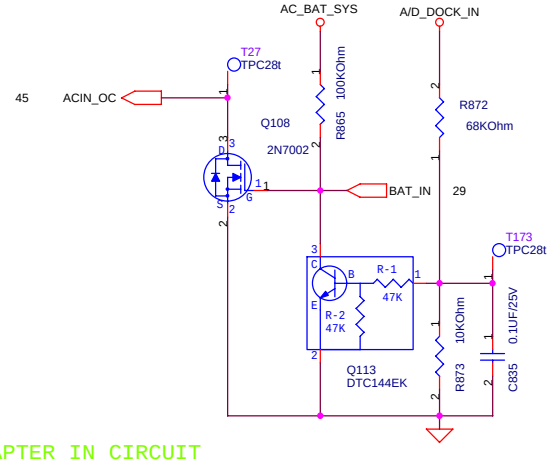
ASUSTeK COMPUTER INC	Title : 1.5VA & DDR2	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 51 of 61	



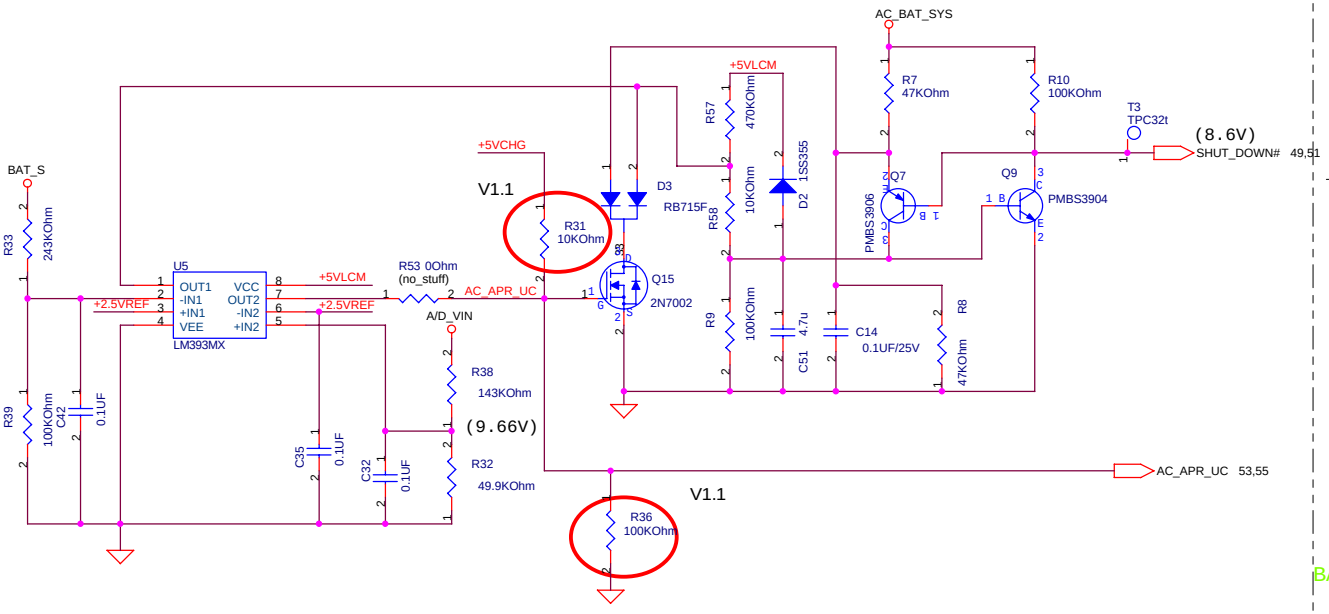
AC_BAT_SYS, BATTERY LEARN CIRCUIT



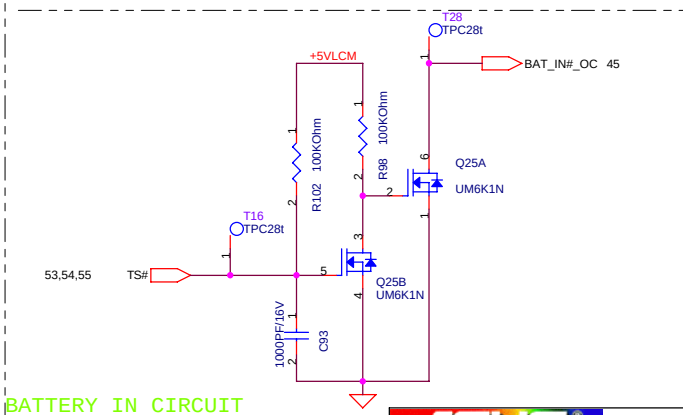
+5VCHG, +5VLCM, +2.5VREF



ADAPTER IN CIRCUIT



AC_IN & BATTERY SHUT_DOWN



BATTERY IN CIRCUIT

ASUSTeK COMPUTER INC

Title : BATLOW/SD#

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	Obi-Wan	1.0

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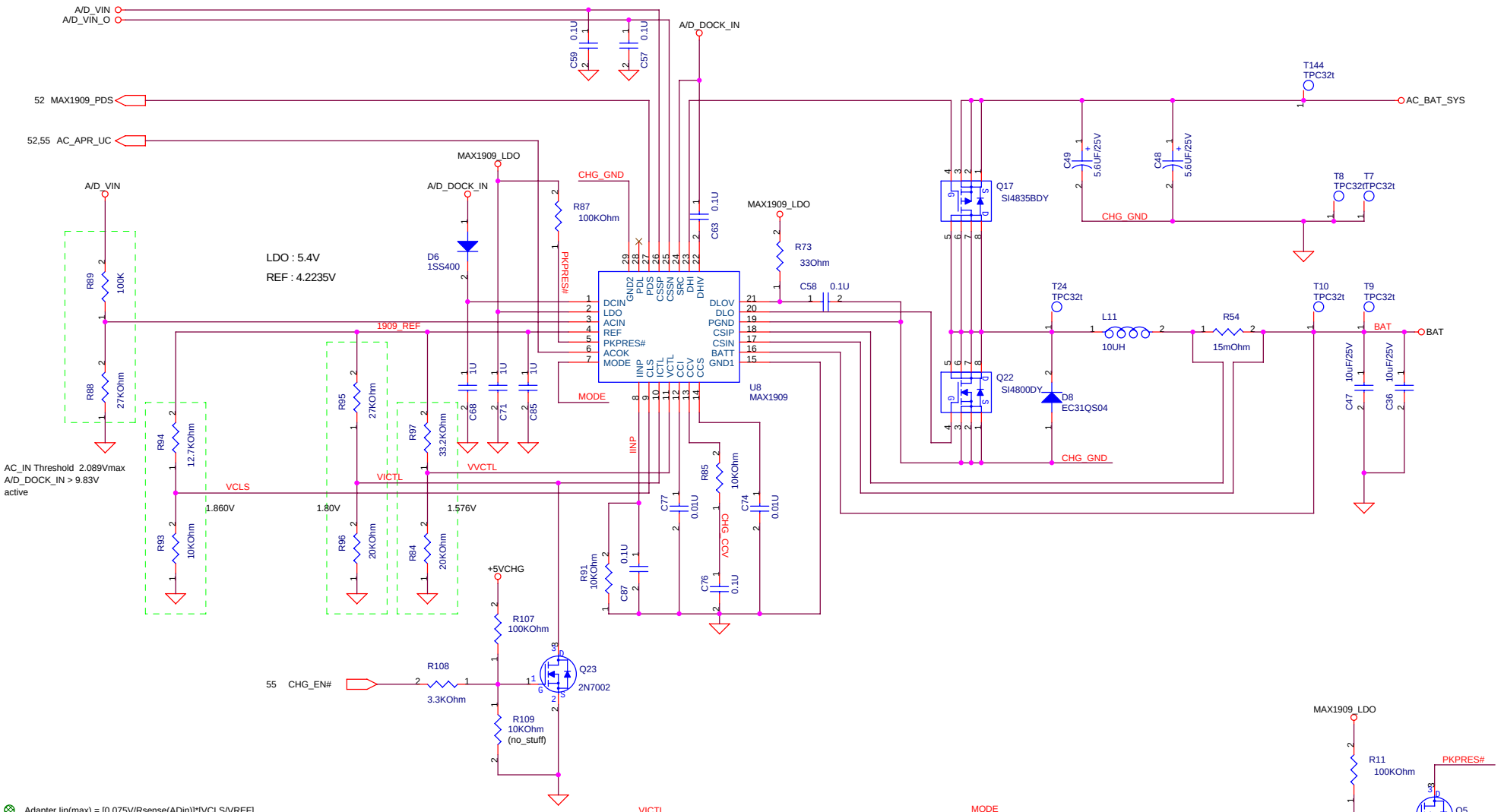
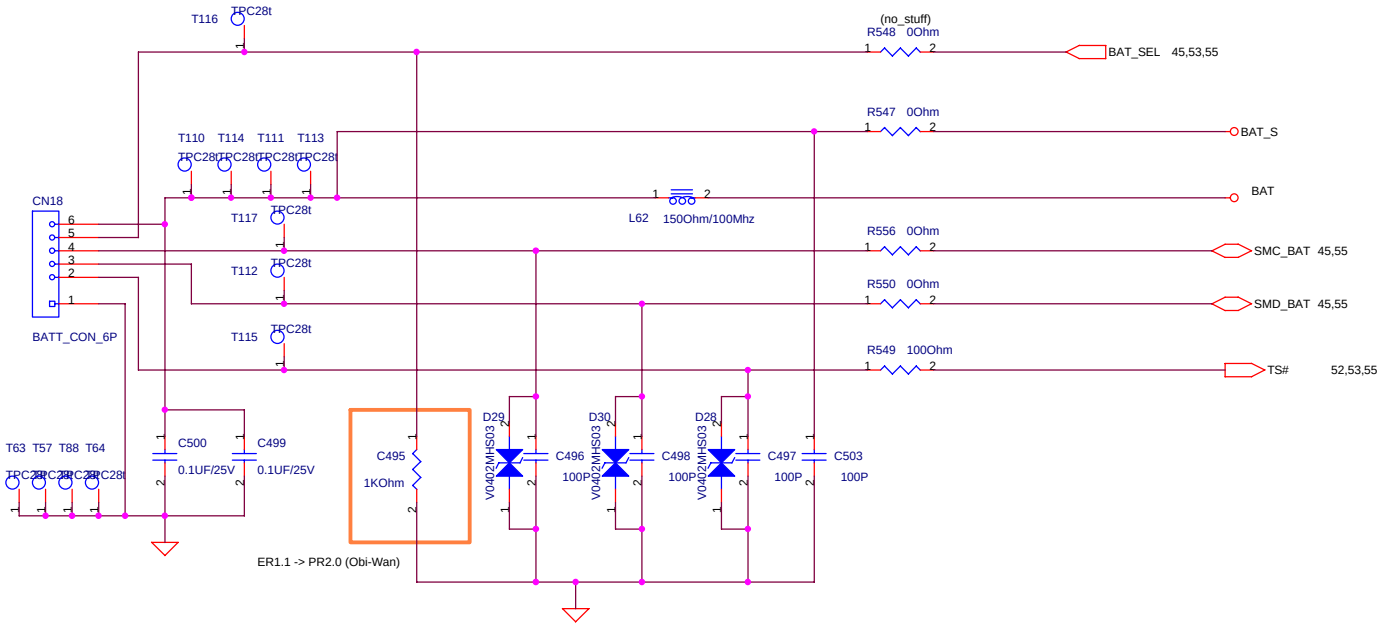


- Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
  Rsense(ADin)=0.01 ohm
  VCLS=1.864V
  => Iin(max)=3.41A
  => Constant Power = 19 * 3.41= 64.79W
- Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
  Rsense(CHG)=0.015 ohm
  VICTL= 1.8V
  => Ichg = 2.5A
- Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
  VCTL= 1.576V
  => Vbatt = 4.2V
- Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
  2.0 > Vmode > 1.6V (floating) ----> 3 Cells
  0.8 > Vmode (trie to GND) ----> Learning mode
- VICTL< 0.8V or DCIN < 7V -->Charger Disable
- Pre_CHG_V = 3.1V
  Pre_CHG_I = 300mA

ASUSTeK COMPUTER INC	Title : CHARGER	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 53 of 61	

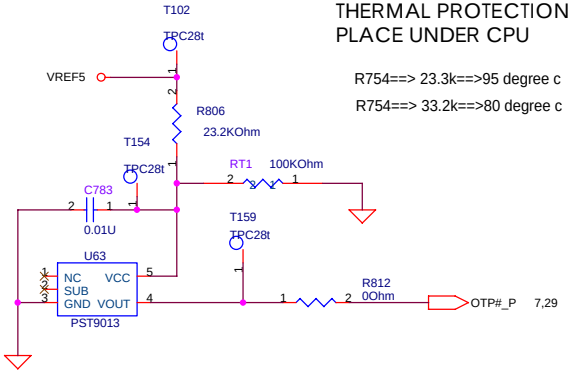


95 DEGREE C

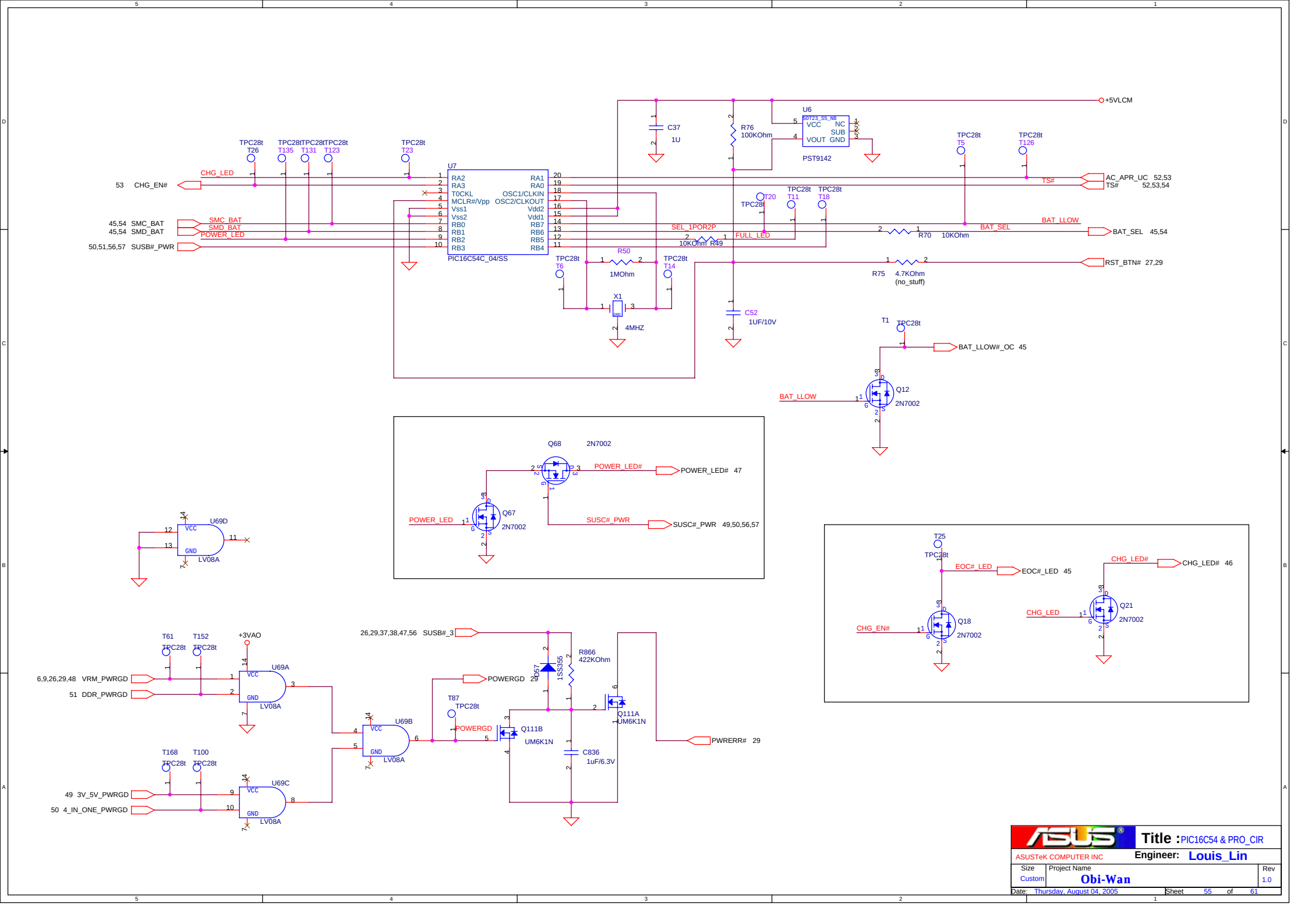
THERMAL PROTECTION
PLACE UNDER CPU

R754==> 23.3k==>95 degree c

R754==> 33.2k==>80 degree c



ASUSTeK COMPUTER INC	Title : BAT CONNECT	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 54 of 61	


+5VLCM
U6
S0123_S5_NB
VCC NC
SUB
VOUT GND
PST9142
C37
1U
R76
100KOhm
U7
PIC16C54C_04/SS
RA2 RA1
RA3 RA0
T0CKL OSC1/CLKIN
MCLR#/Vpp OSC2/CLKOUT
Vss1 Vdd2
Vss2 Vdd1
RB0 RB7
RB1 RB6
RB2 RB5
RB3 RB4
CHG_LED
53 CHG_EN#
45,54 SMC_BAT
45,54 SMD_BAT
SMC_BAT
SMD_BAT
POWER_LED
50,51,56,57 SUSB#_PWR
SEL_1POR2P
FULL_LED
R49 10KOhm
R50
1MOhm
X1
4MHZ
C52
1UF/10V
R75 4.7KOhm
(no_stuff)
RST_BTN# 27,29
TS#
AC_APR_UC 52,53
TS# 52,53,54
BAT_SEL
BAT_LLOW
R70 10KOhm
BAT_SEL 45,54
BAT_LLOW#_OC 45
Q12
2N7002
Q68 2N7002
POWER_LED#
POWER_LED# 47
Q67
2N7002
SUSC#_PWR
SUSC#_PWR 49,50,56,57
U69D
LV08A
T25
EOC#_LED
EOC#_LED 45
CHG_LED#
CHG_LED# 46
Q18
2N7002
Q21
2N7002
CHG_EN#
CHG_LED
6,9,26,29,48 VRM_PWRGD
51 DDR_PWRGD
U69A
LV08A
+3VAO
U69B
LV08A
U69C
LV08A
49 3V_5V_PWRGD
50 4_IN_ONE_PWRGD
26,29,37,38,47,56 SUSB#_3
POWERGD 29
1S355
R866
422KOhm
Q111A
UM6K1N
Q111B
UM6K1N
C836
1uF/6.3V
PWRERR# 29
Title : PIC16C54 & PRO_CIR
ASUSTeK COMPUTER INC
Engineer: Louis_Lin
Size Custom
Project Name Obi-Wan
Rev 1.0
Date: Thursday, August 04, 2005
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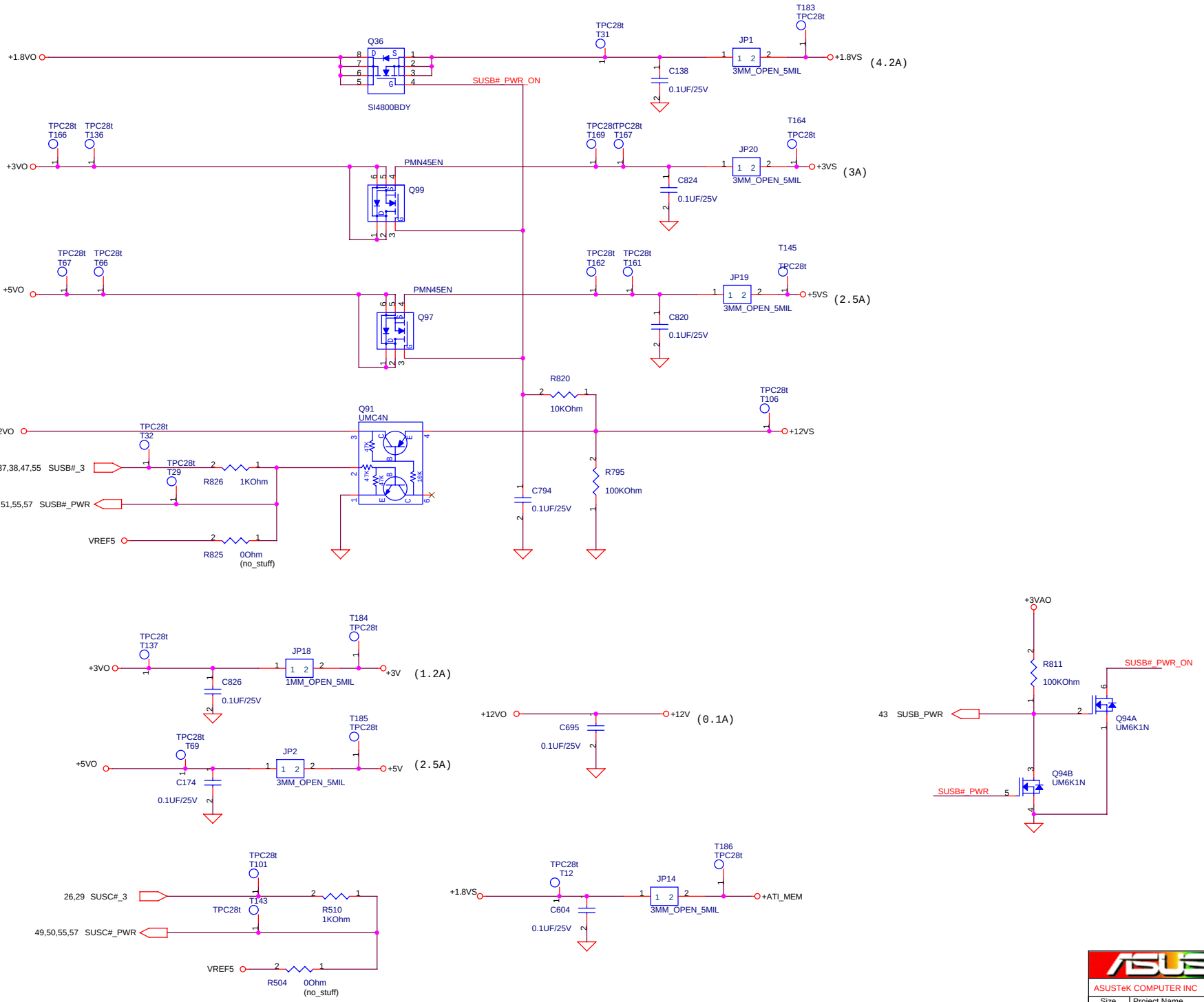
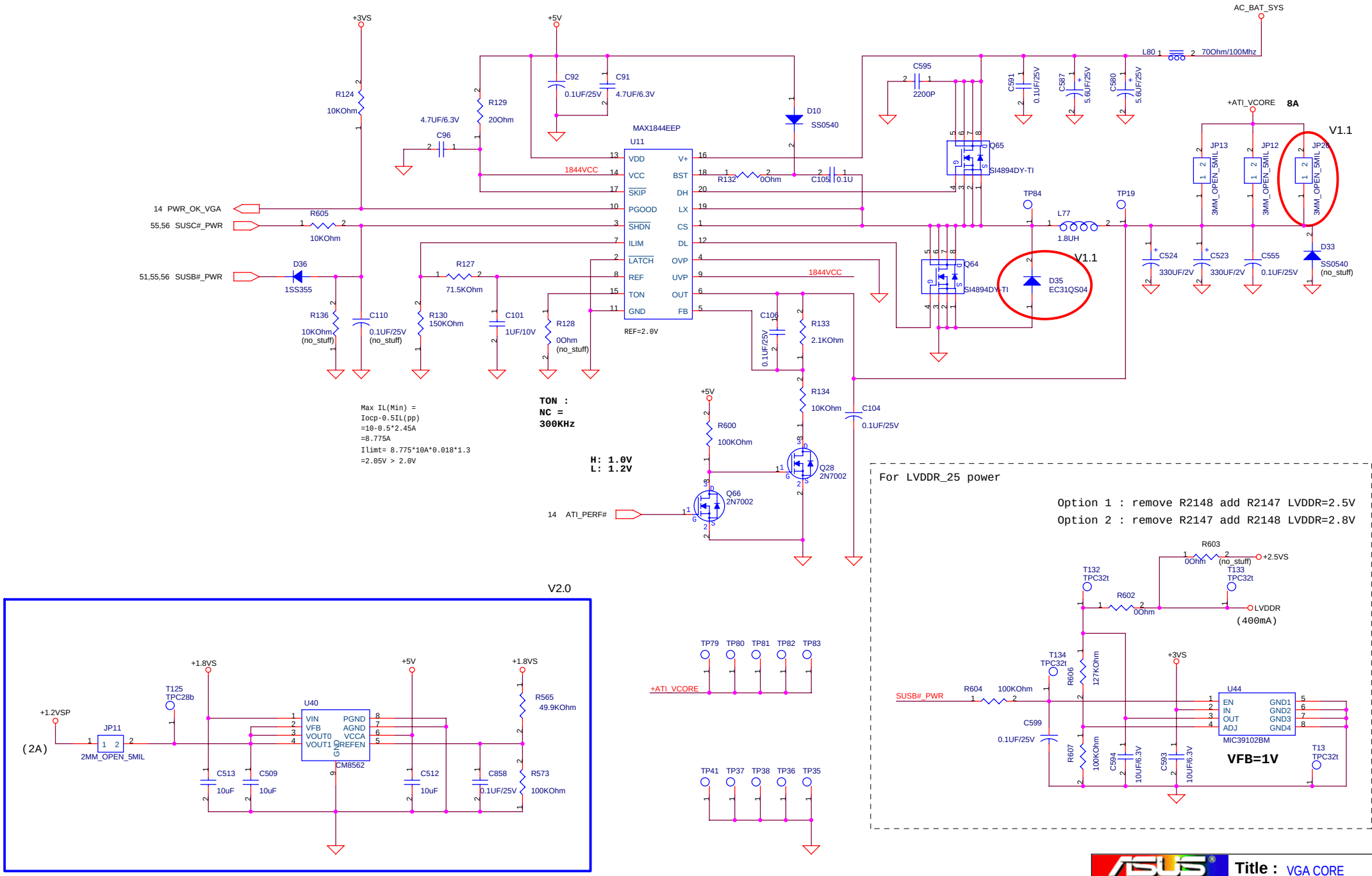
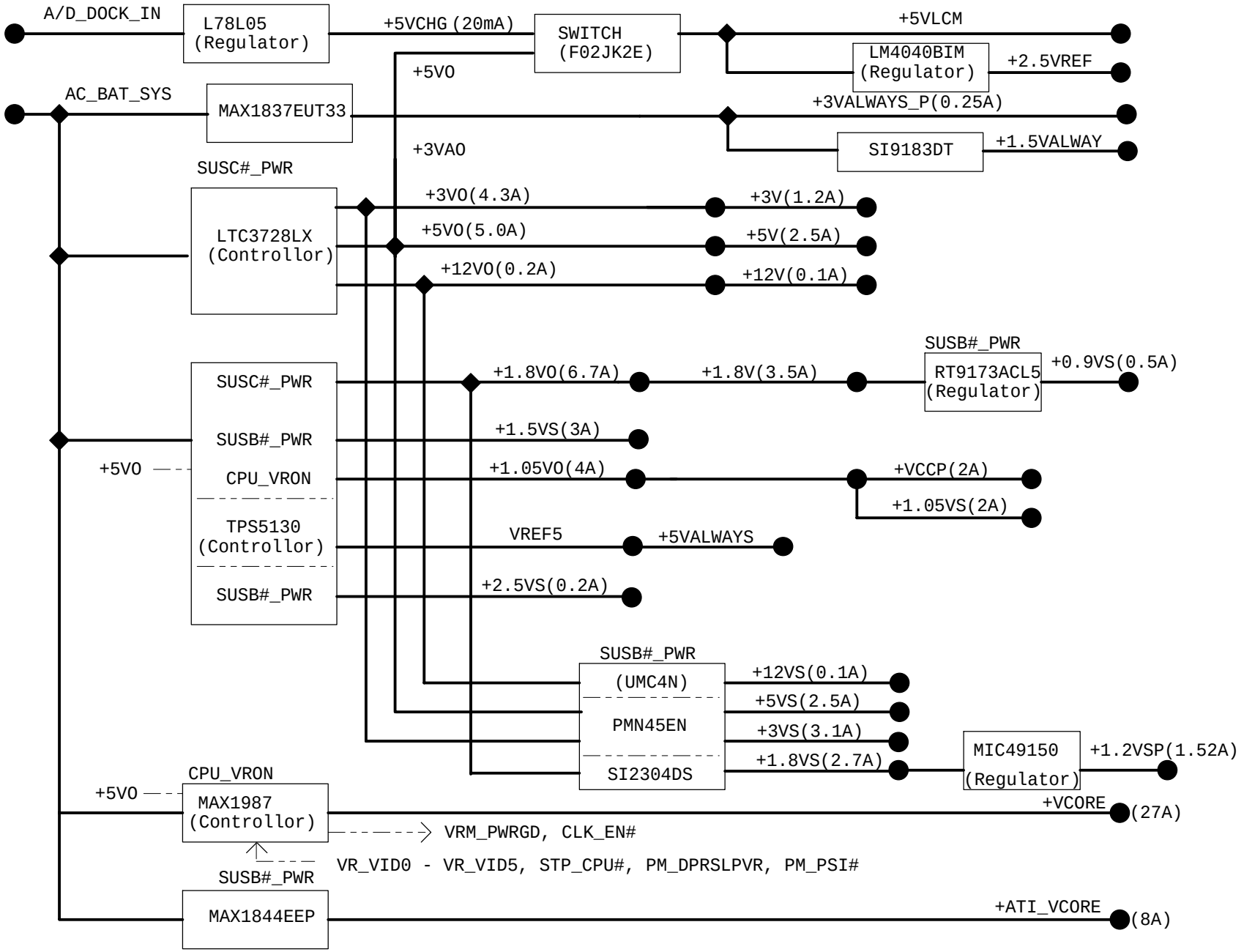


ASUSTeK COMPUTER INC	Title : LOAD SWITCH	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 56 of 61	



ASUSTeK COMPUTER INC	Title : VGA CORE	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 57 of 61	



ASUSTeK COMPUTER INC	Title : POWER FLOWCHART	
	Engineer: Louis_Lin	
Size: Custom	Project Name: Obi-Wan	Rev: 1.0
Date: Thursday, August 04, 2005	Sheet 58 of 61	

POWER REVISION HISTORY

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REVISION HISTORY

03/09 AUDIO CODEC REALTEK ALC880 ---> ADI AD1986A
03/22 RENAME
05/05 ADD U70, DEL C396, CHANGE CN21 3P--->4P, CHANGE U54 ADT7460--->ADT7473, CHANGE CN13, DEL R768, DEL R774, CHANGE CN10(P1<->P12), CHANGE CN3(P5<->P7), ADD U71, R881, R882, R883, C840, U72, R884, R885, R886, C841
05/06 DEL R267, ADD R887, R888, C842
05/09 UPDATE POWER SCHMATIC, ADD U32.P2 R889, R890, R891, DJ_SW# -> U12.P76
05/10 ADD R892, R893, R894, R895, R896, R897, R898
05/16 ADD R899, R900, R901, R902

SR1.0 -> ER1.1
Page5, Change H8,H3 from AM20~30 to AM20.
Page6, Change value of C267 and C271 from 12PF to 3PF.
Add net CLK_TPMPCI from pin8 of U16 to pin21 of U74 and add R919 on this net.
Page7, Change CN21 from WTOB_CON_3P to WTOB_CON_4P.
Add net PWN1 from pin4 of CN21 to pin15 of U54 and add R902 on this net.
Page9, Add R896,R897,R898 on pinA15,C16,A17 of U48F . Add R903,R904,R905 on pinD21,B20,B19 of U48F for option.
Page14, Add net LVDS_DDC2BC,LVDS_DDC2BD on pinAE13,AE14 of U9A.
Page25, Swap pin5,7 of CN3.
Page26, Add net ACZ_BCLK_MDC through R899 on pinC10 of U62D.
Rename net ACZ_BCLK to ACZ_BCLK_AC.
Page27, Change net name on pinC27,B27 of U62B from USB_OC_012# to USB_OC_01#.
Change net name on pinB26,C26 of U62B from USB_OC_3# to USB_OC_23#.
Change net name on pinC23,D23 of U62B from USB_OC_045# to USB_OC_45#.
Change net name on pinC25 of U62B from USB_OC_06# to USB_OC_67#.
Change net name on pinC24 of U62B from USB_OC_07# to USB_OC_67#. Remove R774.
Page29, Add R895(Un-mount),R894.
Page30, Rename net ACZ_BCLK to ACZ_BCLK_AC.
Add R891 on pin47 of U32.(Un-mount).
Add R889 from pin2 of U32 pull down to ground.
Add R901.
Page32, Add R901,R902 to connect digital and analog ground.
Page37, Remove C348,C345.
Change CN13 from CARD_BUS_68P to BTOB_CON_68P.
Add R900 on pin15 of CN31 to pull down to ground.
Add D63,U70. Remove C345. Add net SD_CD,MS_CD.
Change inter-sheet port MDIO00/SDCD from pin23 to pin21 of CN31.
Page39, Rename net ACZ_BCLK to ACZ_BCLK_MDC.
Page43, Add U71,U72,R881~6,C840,C841 for over current function.
Page45, Replace power plane +VCORE with inter-sheet port DJ_SW# on pin76 of U12.
Page46, Change connections of CN10.
Add R887,C842,VCC +5V of LED1. Add inter-sheet port DJ_LED_EN# on pin2 of LED1.

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+3V
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+3V
VRM_PWRGD	I	+3V
CPU_STP#	O	+3V
CHG_LED	I	+3V
RST_BTN#	O	+3V
OTP_RESET#	I	+3V
SHUT_DOWN#	I	+3V
+V5_LCM	PWR	+5V
PM_SLPDLY_S3#	O	+3V
PM_SLP_S4#	O	+3V
BAT_LEARN	I	+3V
BAT_LLOW#_OC	I	+3V
BAT1_IN#_OC	I	+3V
BAT2_IN#_OC	I	+3V
ACIN_OC	I	+3V
CHG_EN_OC	I	+3V
PM_DPRSLPVR	O	+3V
ACIN_3VA	I	+3V
+5VAO	PWR	+3V
EN_+3VALWAYS	O	+3V
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMCLK_BAT1	IO	+3V
SMDATA_BAT1	IO	+3V
SMCLK_BAT2	IO	+3V
SMDATA_BAT2	IO	+3V
BAT_LOW#	I	+5VLCM
1.5V_PWRGD	I	+3V
1.8V_PWRGD	I	+3V

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.32A
+VCC_GMCH	1.05V	3.9A
+0.9VS	1.25V	2.28A
+1.5VS	1.5V	4.69A
+1.5VA	1.5V	270 mA
+1.8V	1.8V	7.89A
+1.8VS	1.8V	3.2A
+2.5VS	2.5V	200 mA
+3VS	3.3V	2.69A
+3V	3.3V	2.17A
+3VA	3.3V	435 mA
+5VS	5V	5.37A
+5V	5V	4.3A
+12V	12V	50 mA
+12VS	12V	10 mA
ATI_+VCORE	1.0V - 1.2V	8 A
+1.2VSP	1.2V	1.5 A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/IN3/BOT	14 mils
IN1/IN2	16.5 mils

37.5 OHM	WIDTH
TOP/IN3/BOT	8.5 mils
IN1/IN2	10 mils

42 OHM	WIDTH
TOP/IN3/BOT	7 mils
IN1/IN2	8.5 mils

55 OHM	WIDTH
TOP/IN3/BOT	4 mils
IN1/IN2	4.5 mils

60 OHM	WIDTH
TOP/IN3/BOT	3 mils
IN1/IN2	4 mils

Differential

70 OHM	WIDTH/SPACE
TOP/IN3/BOT	8 mils/ 5 mils
IN1/IN2	8 mils/ 4.5 mils

90 OHM	WIDTH/SPACE
TOP/IN3/BOT	5 mils/ 8 mils
IN1/IN2	5 mils/ 6 mils

100 OHM	WIDTH/SPACE
TOP/IN3/BOT	4 mils/ 9 mils
IN1/IN2	4.5 mils/ 7.5 mils

PCI INTERFACE

PCI_REQ#

LAN	PCI_REQ#1
CB&1394	PCI_REQ#2
MINIPCI	PCI_REQ#3

IDSEL

LAN	PCI_AD16
CB&1394	PCI_AD17
MINIPCI	PCI_AD19

PCB STACK-UP

PCB THICKNESS: 1.2 mm

L1 TOP
L2 GND1
L3 IN1
L4 IN2
L5 VCC
L6 IN3
L7 GND2
L8 BOT

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SIGNAL	IN:	VR_VID0 - 5 PM_DPRSLPVR STP_CPU# PM_PSI# IMVP_VR_ON
	OUT:	DELAY_VR_PWRGD VR_PWDGD_CK410#
POWER	IN:	AC_BAT_SYS +5VO +3VO
	OUT:	+VCORE

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SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12VO +3VO +5VO

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SIGNAL	IN:	SUSB#_PWR SUSC#_PWR
POWER	IN:	AC_BAT_SYS +3VO
	OUT:	+1.8V +1.5V +2.5V +VCC_GMCH_CORE +5VALWAYS +3VALWAYS

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SIGNAL	IN:	SUSB#_PWR
	OUT:	VCC_MCH_VRPWRGD IMVP_VR_ON
POWER	IN:	+3VA +3V +1.8V +VCC_GMCH_CORE
	OUT:	+0.9VS +1.5VA +VCCP

PROJECT: M9V	REVISION: 1.1	DATE: Thursday, August 04, 2005	DESCRIPTION: REVISION HISTORY	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
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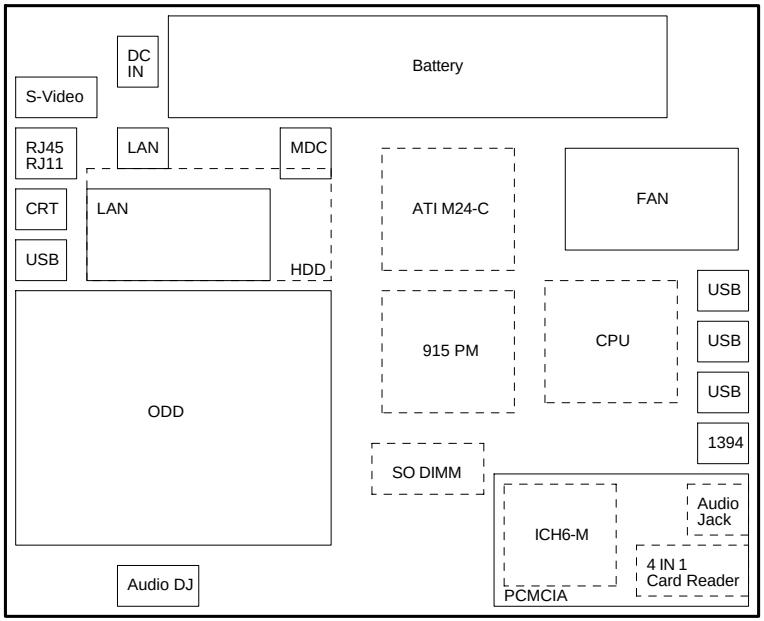

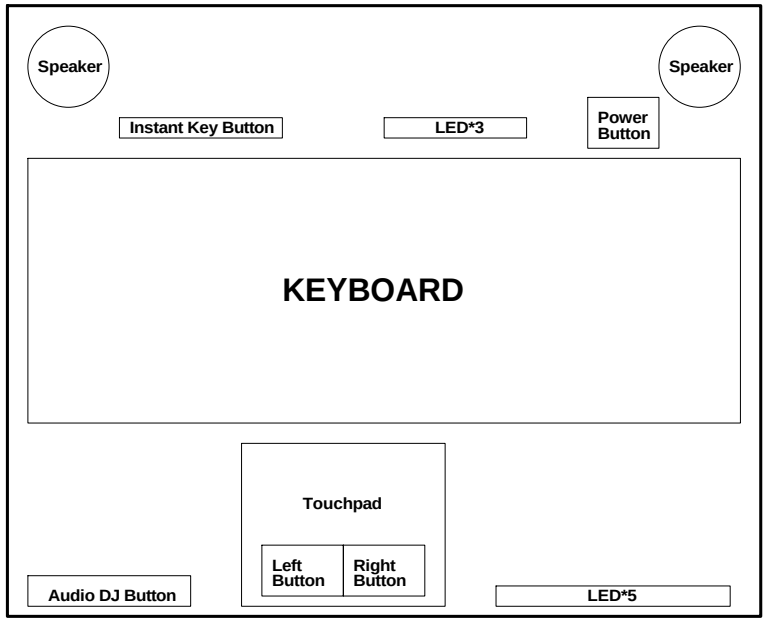

Page47, Change Rename net DJ_LED_EN to DJ_LED_EN# and change inter-sheet port from pin2 to pin3 of Q37.
Add inter-sheet port DJ_SW# on pin4 of Q27. Add R888.
Page48, Change value of R317 from 360 to 200 Ohm.
Page49, Un-mount R517. Mount R516. Add D62,inter-sheet port SHUT_DOWN#.
Page50, Change value R805 from 12.7K to 15K Ohm.
Change value C807 from 2200P to 3300P.
Change value R813 from 12.7K to 10.2K Ohm.
Change value C787 from 10UF to 100UF. Un-mount C804.
Page52, Change value R31 from 47K to 10K Ohm.
Change value R36 from 15K to 100K Ohm.
Page57, Add JP26. Change Diode D35 form SS0540 to EC31QS04.

ER1.1 -> PR2.0
Page5, Add H26,H27.
Page7, Change U54 VCC from +3VS to +VCORE.
Add Q118 on net VGA_THERM_DA,VGA_THERM_DC and Un-mount.
Page14, Change U47 VCC from +5VS to +3Vs. Add R907,C843,R906,R909.
Un-mount R553,R554.
Page25, Un-mount L58. Mount L57.
Page26, Un-mount R789. Mount R786.
Change net name of pinAB21 of U62D from PWRLED_1HZ to GPIO_MUTE_POP.
Add net LPCPD# through R920 to pinW3 of U62D and Un-mount R920.
Page27, Mount R463,R440,R790. Un-mount R464,R452,R792.
Page28 Un-mount R848,Q101,R851,Q102,R842. Add R923(un-mount).
Page29, Add net OTP#_P through D67 on pin1 of U66A.
Page31, Change value of C448 from 0 to 1K Ohm.
Page32, Add C844,C845,C846,C847,C848,C849,C850,C851,D64,D65,L95,L96,L97,L98,Q119, Q120,R910,R911,R912,U73 for SPIDIF function.
Page33, Add R914~R917,Q121 to prevent current leakage.
Page37, Add R906 on pin6 of CN31 to pull high to +3V.
Page43, Change value of R263,R131,R881,R884 from 10K to 0 Ohm. Un-mount C236,C840,C103,C841.

Page44, Add C852,C853,C854,C855,C856,C857,R918,U74,X8 for TPM 2.1 function.
Page45, Add R924,R925,Q122, net DJ_SW# to inverse net DJ_SW_EN.
Page46, Change value of R521,R523,R524,R525,R887 from 300 to 56 Ohm.
Page47, Change CN11 VCC from +3V to +3VALWAYS.

ER1.1 -> PR2.0 (Obi-Wan)
Page6, Un-mount C261. Improve clock quality to meet reduce rise & fall time specification.
Add R929,R930 from net CLK_PCIE_PEG,CLK_PCIE_PEG# pull down to ground for termination.
Page24, Change value of L76,L75,L74 from 120 to 80 Ohm/100MHz and add R931,R932,R933,C859~C864(un-mount) to improve signal quality.
Page29, Un-mount SW3 for HP request. Un-mount D56 to disable Audio DJ function.
Page32, Add R934 on net S/PDIF to pull down ground.
Page33, Un-mount L82,R259,R258 to disable CMOS camera.
Change value of C443 from 1u to 2.2u ; R489 from 300k to 200k ; C441 from 150p to 18p to improve clock quality to meet specification.
Change CN9 from WTOB_CON_7P to fpc_1x2p.
Page38, Change value of R23 from 5.6k to 5.76k Ohm to meet LAN specification.
Page39, Change CN17 from LAN_12P to MODULAR_JACK_12P.
Page40, Un-mount R177,R179 and mount R183,R182 for Wireless LED controlled by EC.
Page44, Add CN32 to replace CN15. (HP request)
Page46, Un-mount R887,LED1 to disable Audio DJ function.
Change color of LED3 from orange to blue.(HP request)
Change CN6 from FPC CON_13P to ZIF_CON_14P and add net PWR_LED# on pin13.
Change value of R523 from 470 to 56Ohm.
Page47, Un-mount Q56,Q35,Q27,R140,R143,R139,Q29,CN11,R888,Q37 to disable Audio DJ function. Add R935 (un-mount) on net SWDJ_EN to prevent current leakage to EC.
Page54, Change C495 from 100P to 1K Ohm.

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