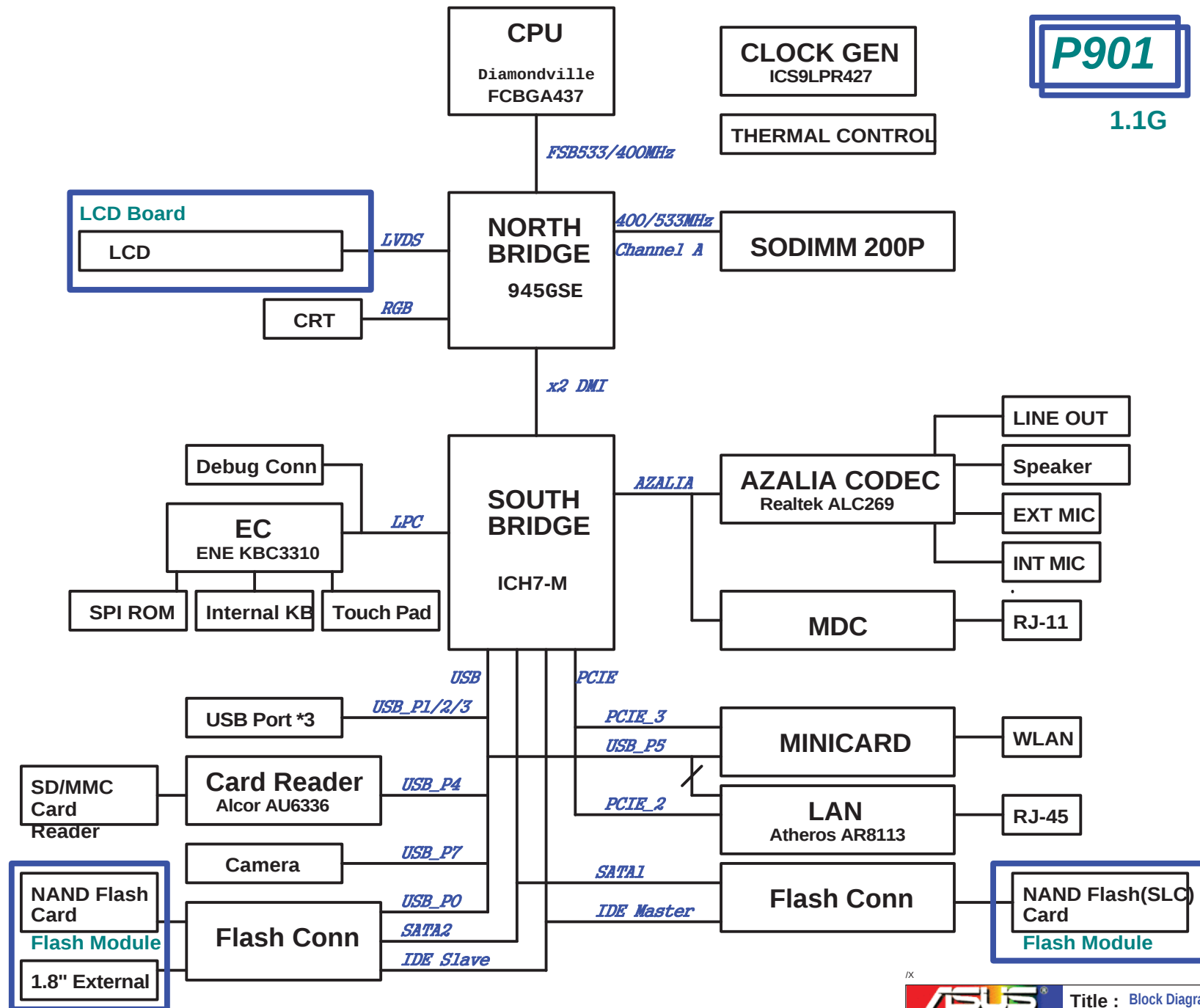


- 01_Block Diagram
- 02_System Setting
- 03_Power Sequence
- 04_Clock Gen_ICS9LPR426
- 05_Diamondville_BUS
- 06_Diamondville_PWR
- 07_NB-945GMS(HOST)
- 08_NB-945GMS(DMI)
- 09_NB-945GMS(GRAPHIC)
- 10_NB-945GMS(DDR2)
- 11_NB-945GMS(PWR)
- 12_NB-945GMS(PWR2)
- 13_NB-945GMS(GND)
- 14_SB-ICH7M(PWR)
- 15_SB-ICH7M(1)
- 16_SB-ICH7M(2)
- 17_SB-ICH7M(3)
- 18_DDR2_SODIMM
- 19_DDR2_Termination
- 20_Onboard VGA
- 21_LCD Conn_LID
- 22_PCIEx 3.5G & Ext. Antenna
- 23_Mini WIFI+ BT
- 24_LAN_Atheros AR8113
- 25_MDC_RJ11_RJ45
- 26_HD + Flash Conn
- 27_USB Port
- 28_Camera Conn
- 29_Card Reader_AU6336C52
- 30_Codec_ALC269
- 31_Audio_AMP_Jack
- 32_EC_ENE KB3310
- 33_EC_UART controller
- 34_Switch_SPI ROM_Debug Conn
- 35_Thermal Sensor_FAN
- 36_KB_Touch Pad
- 37_LED_THERMTRIP
- 38_Discharge
- 39_PWR Jack
- 40_Srew Hole
- 41_EMI
- 42_POWER FLOW
- 43_Vcore
- 44_Power System
- 45_Power_+1.8V & VTTDDR
- 46_Power_VCCP
- 47_Power_+1.5VS & +2.5VS
- 48_Power_Charger
- 49_EC Pin Define
- 49_History



EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

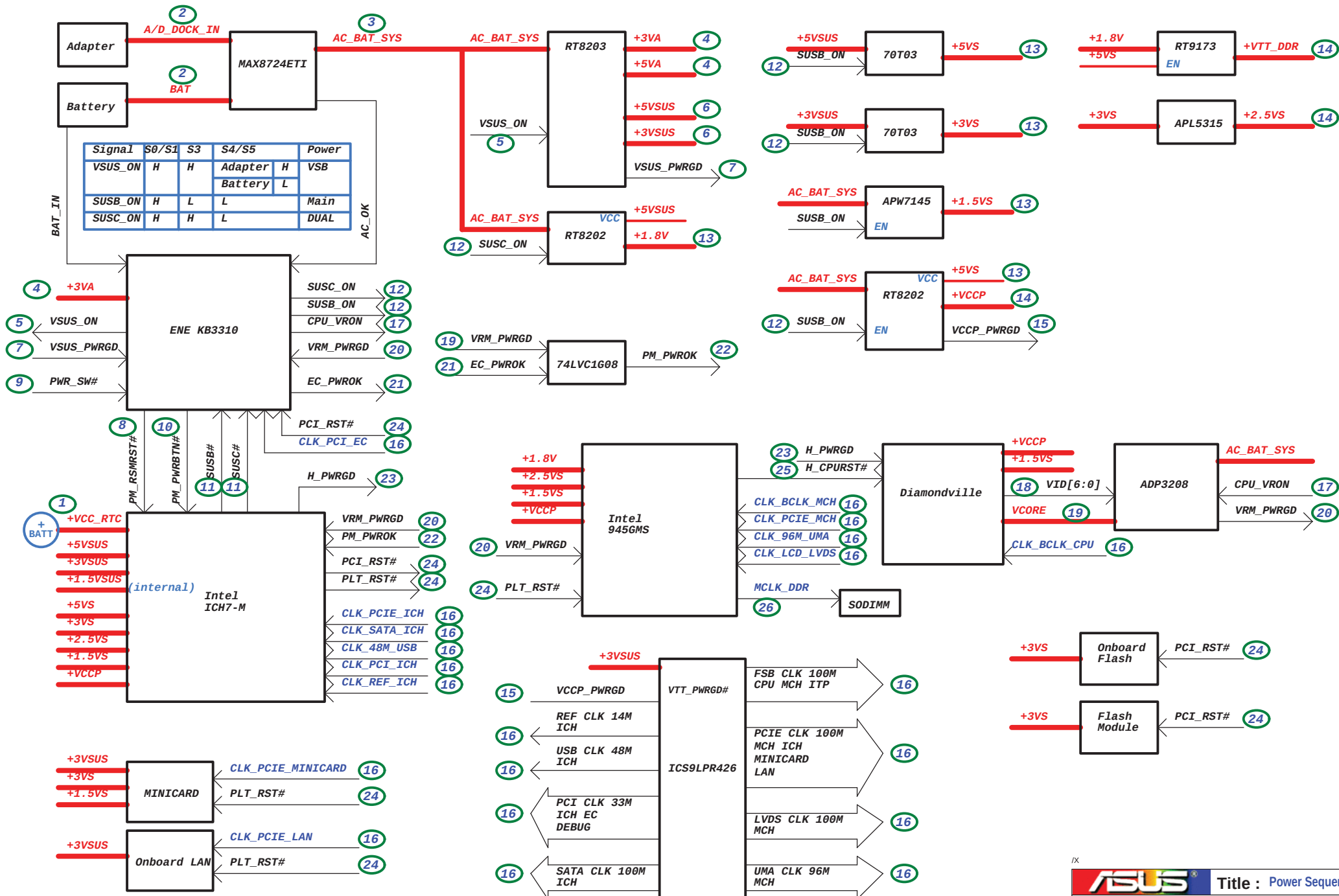
USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	NC
USB 7	Camera

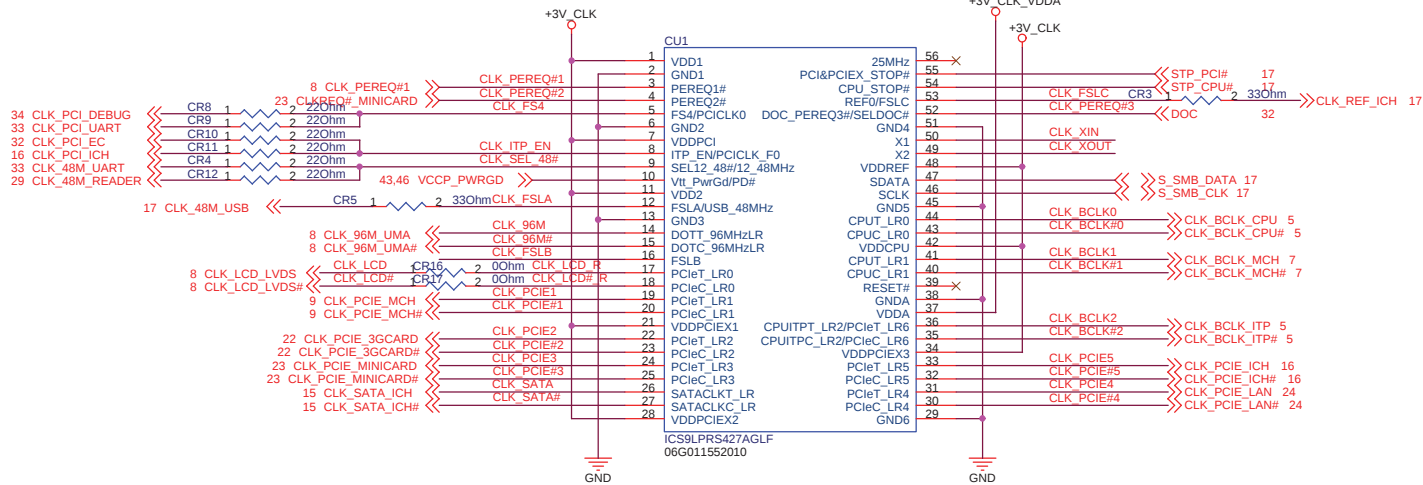
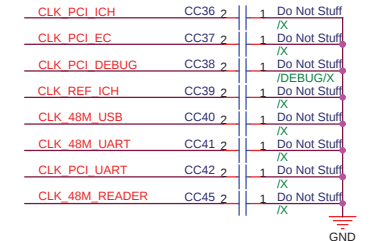
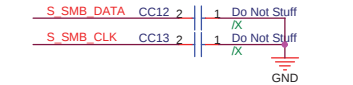
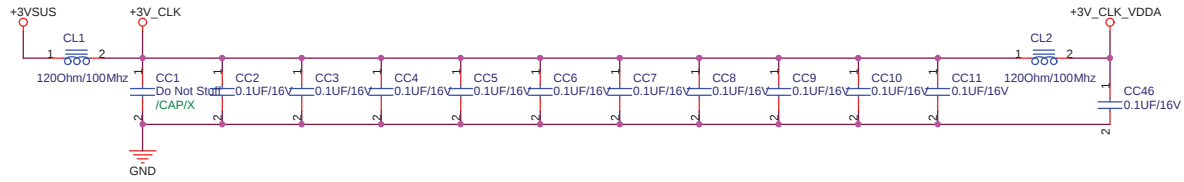
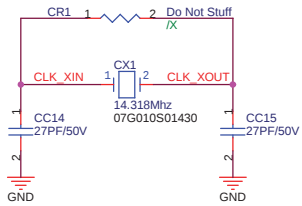
PCIE

PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM
ACZ_SDIN2	NC

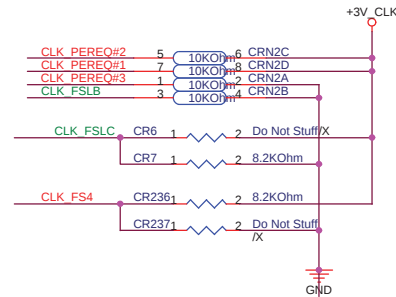
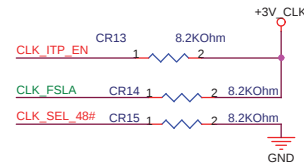


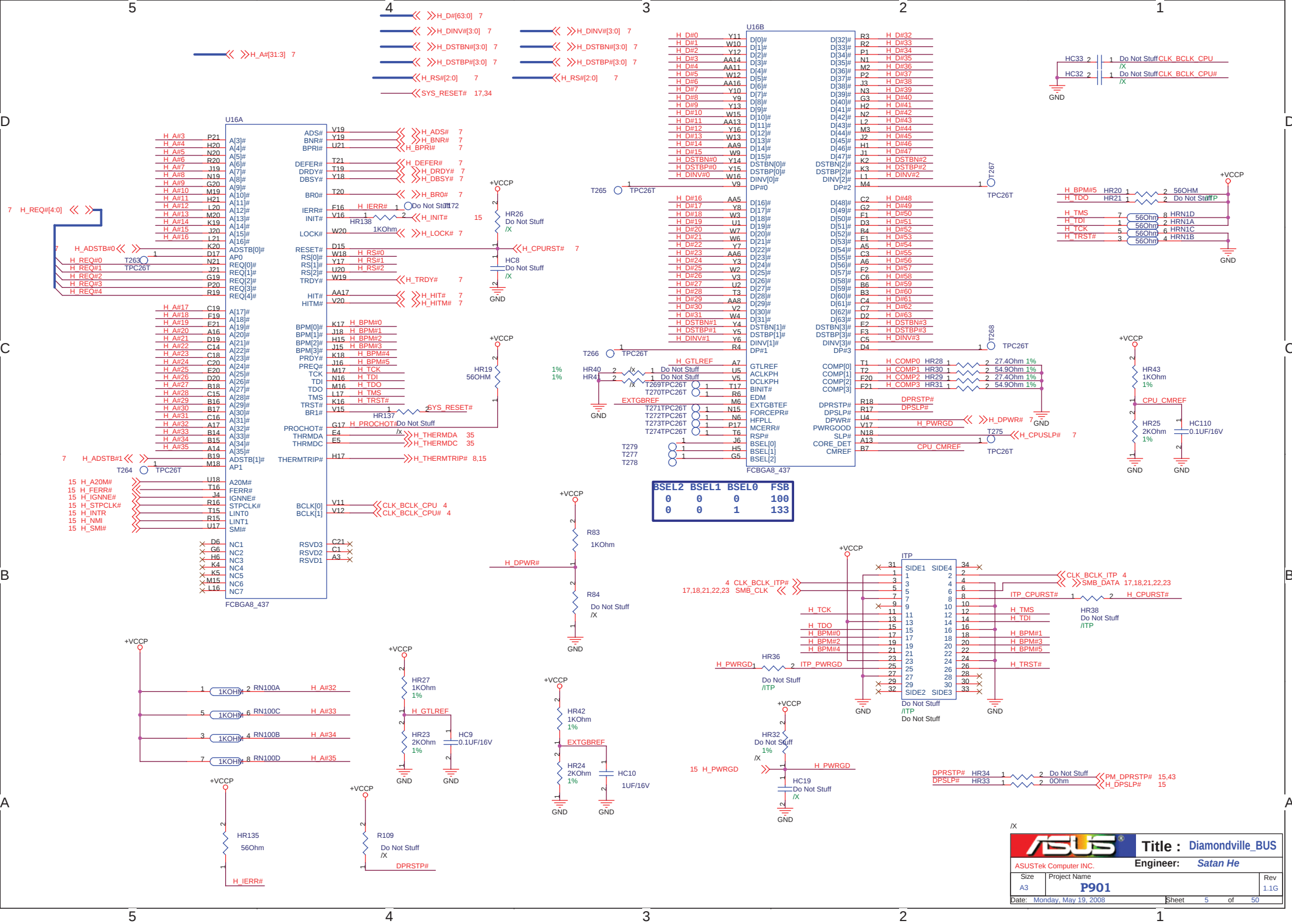


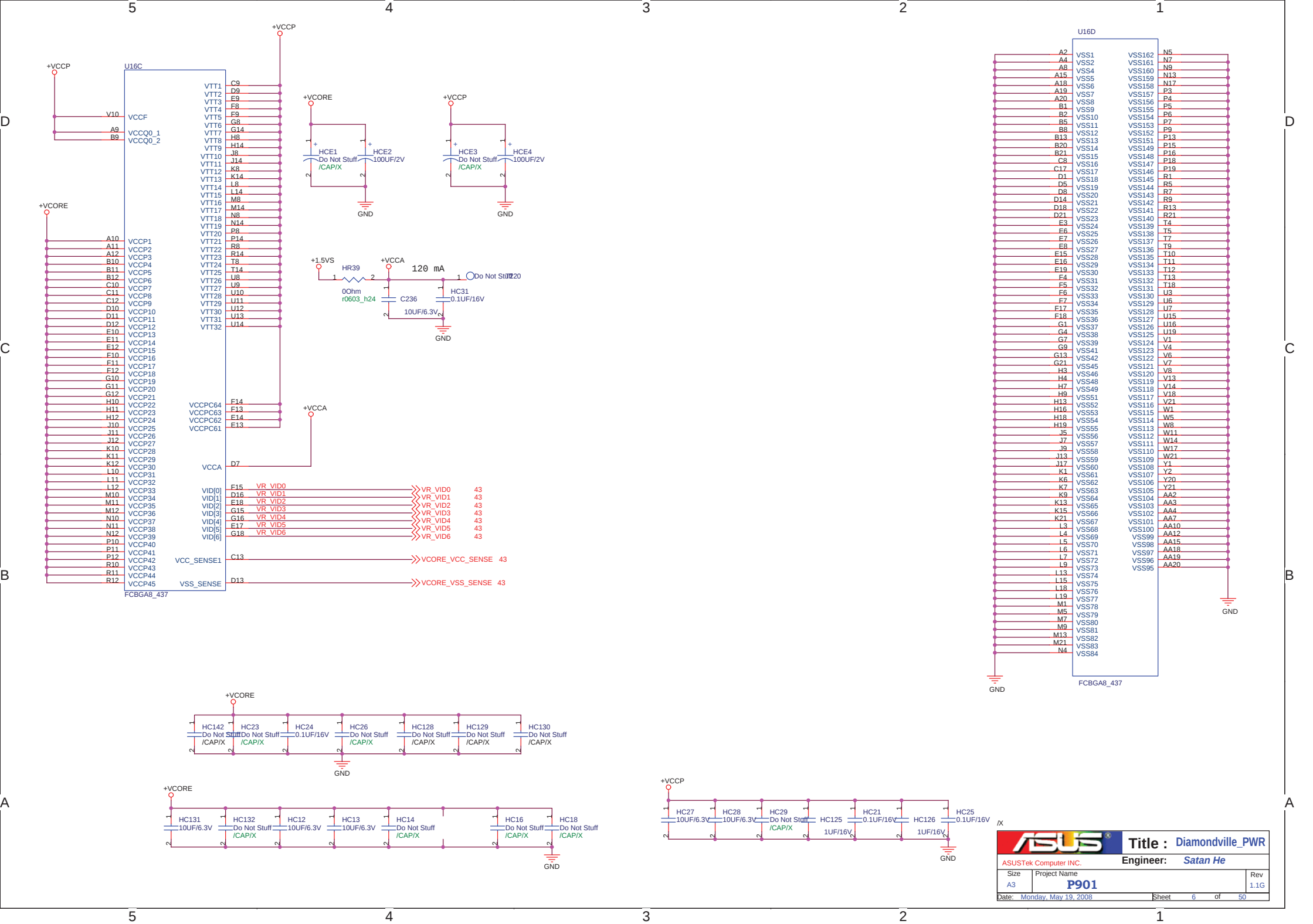
1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100



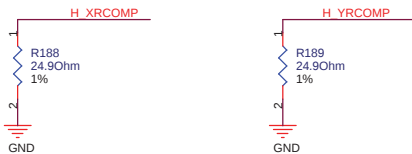




**Power :
+VCCP**

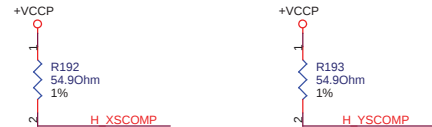
RCOMP

For Calibrating the FSB I/O Buffer



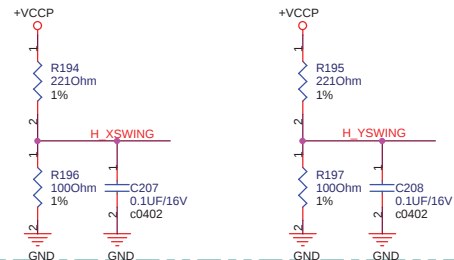
SCOMP

For Slew Rate Compensation on the FSB

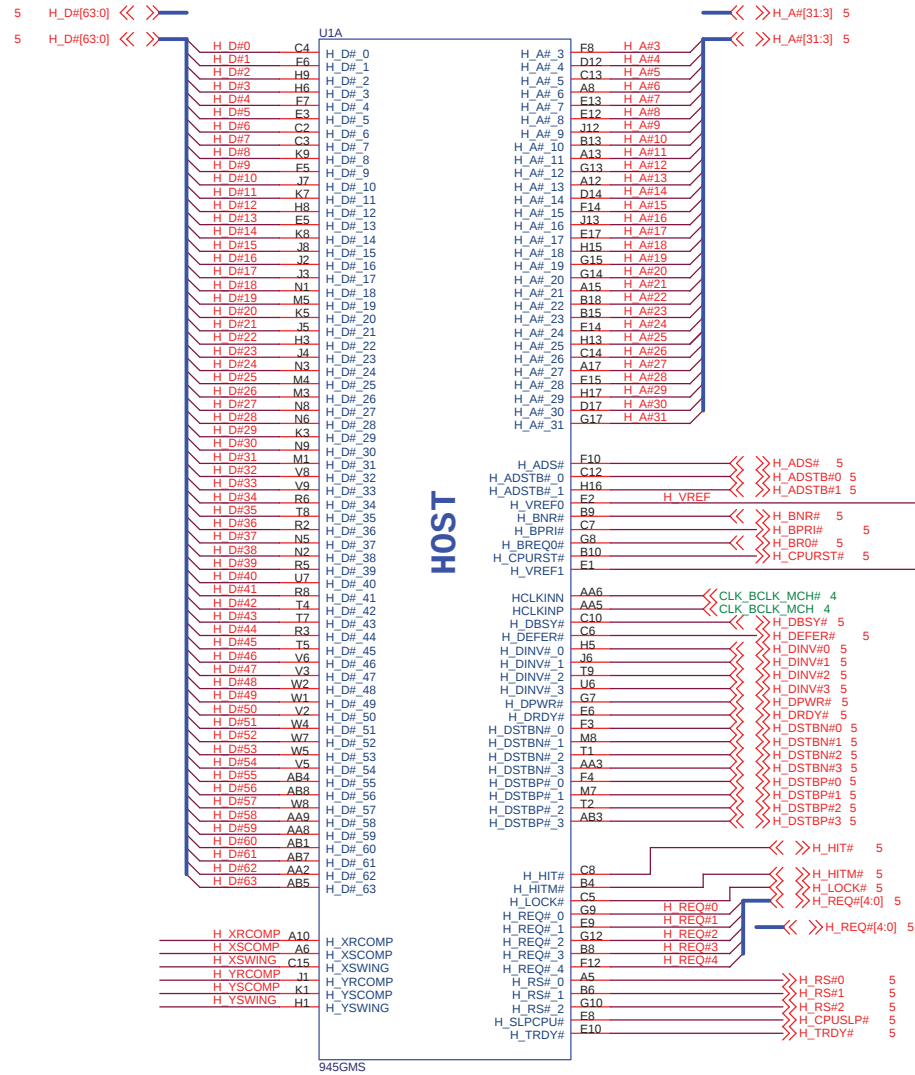


Voltage Swing

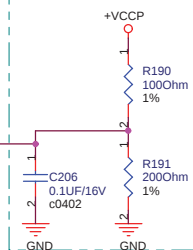
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing

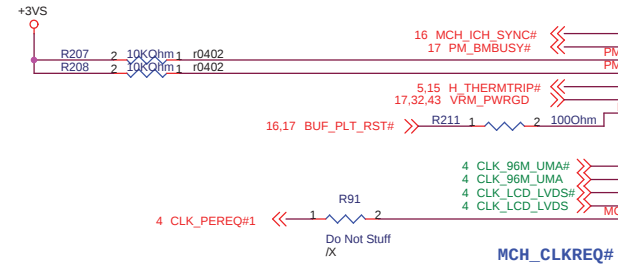


AGTL+ I/O Voltage Reference

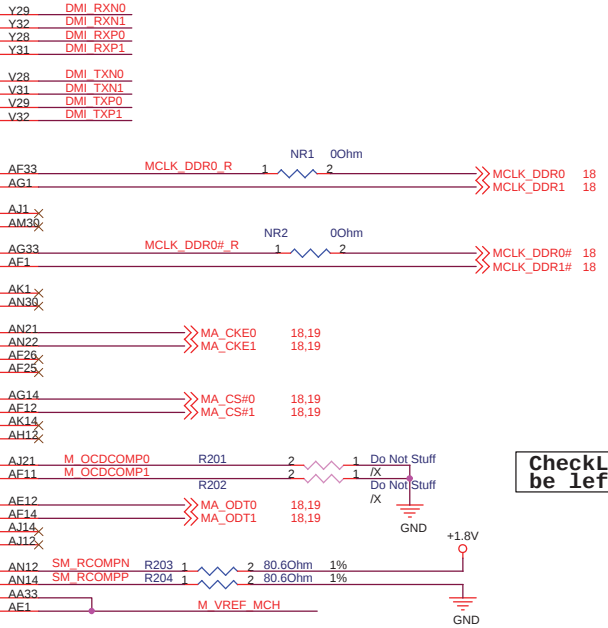
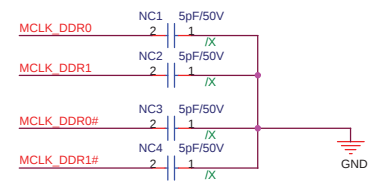
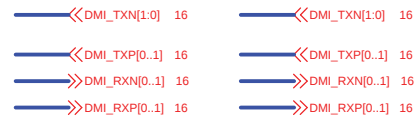
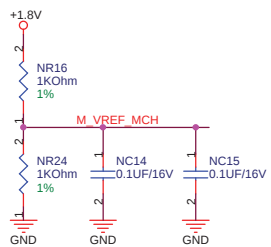
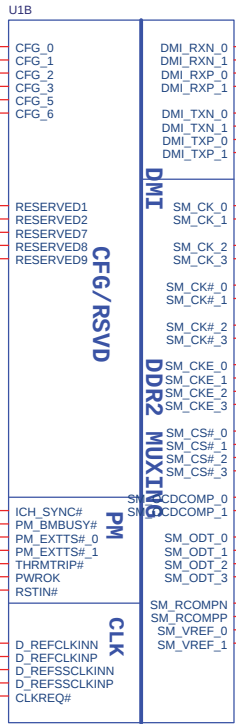


Layout Note:
0.1uF should be placed 100mils or
less from GMCH pin.

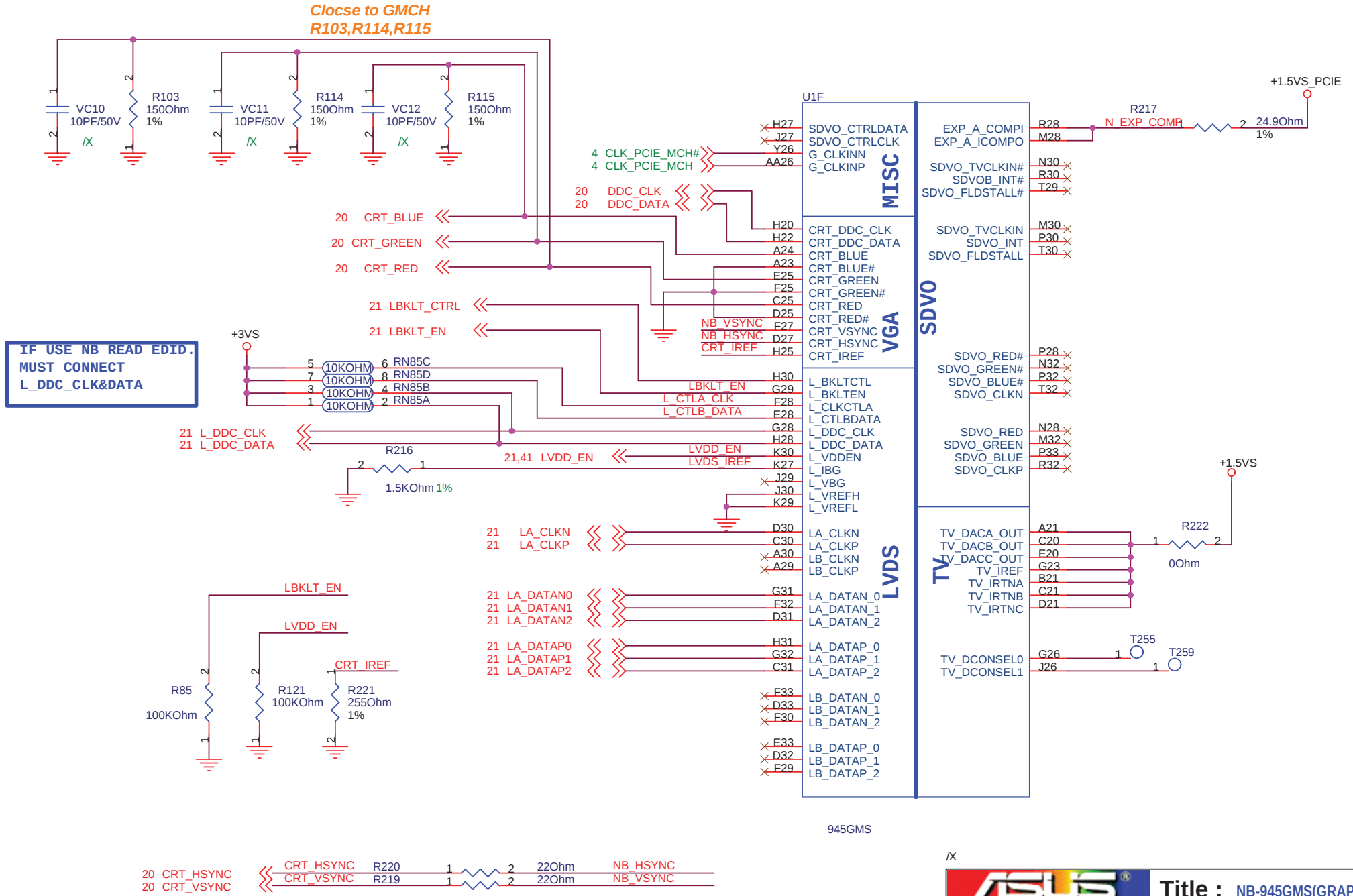
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



MCH_CLKREQ# is OD pin

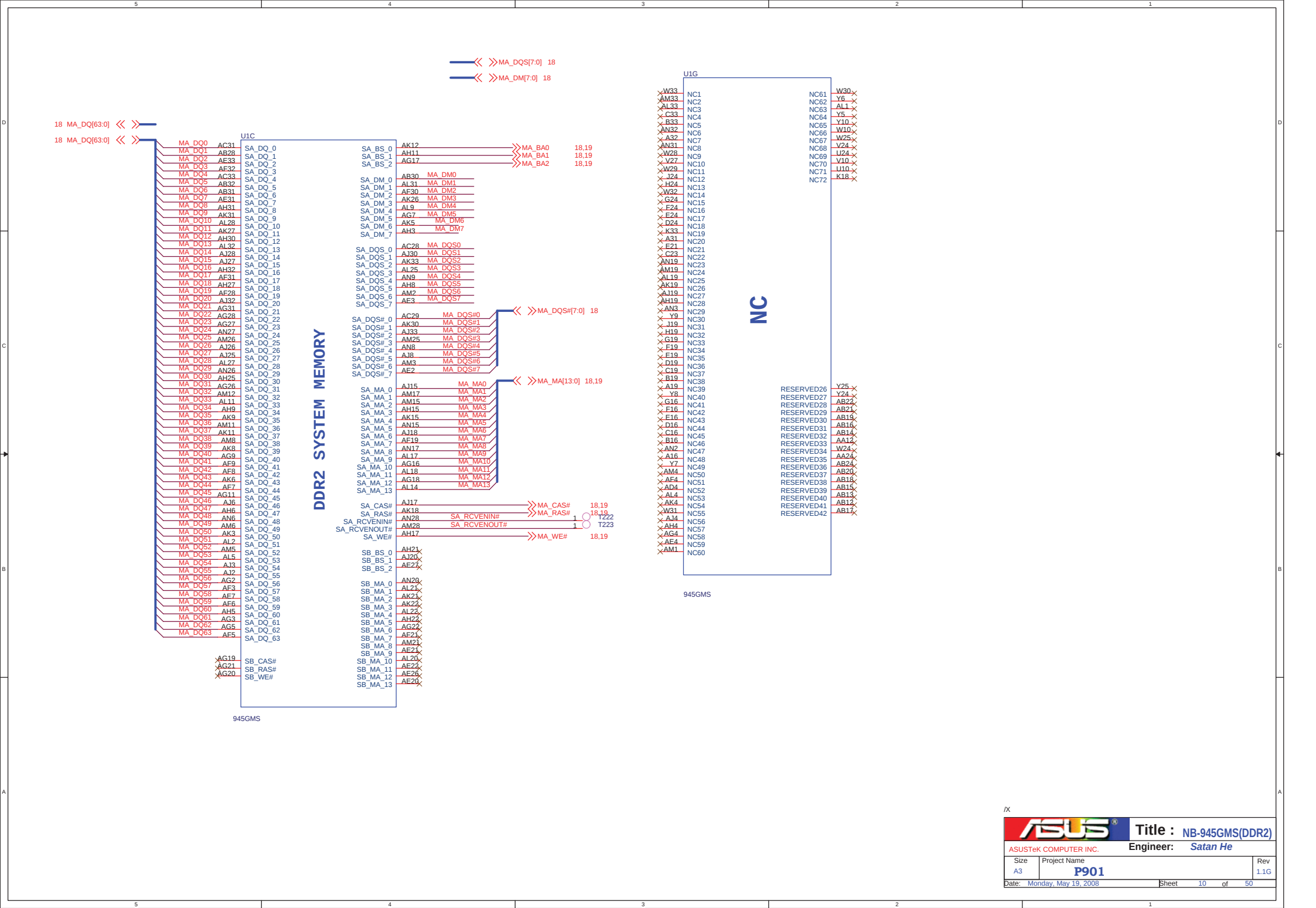


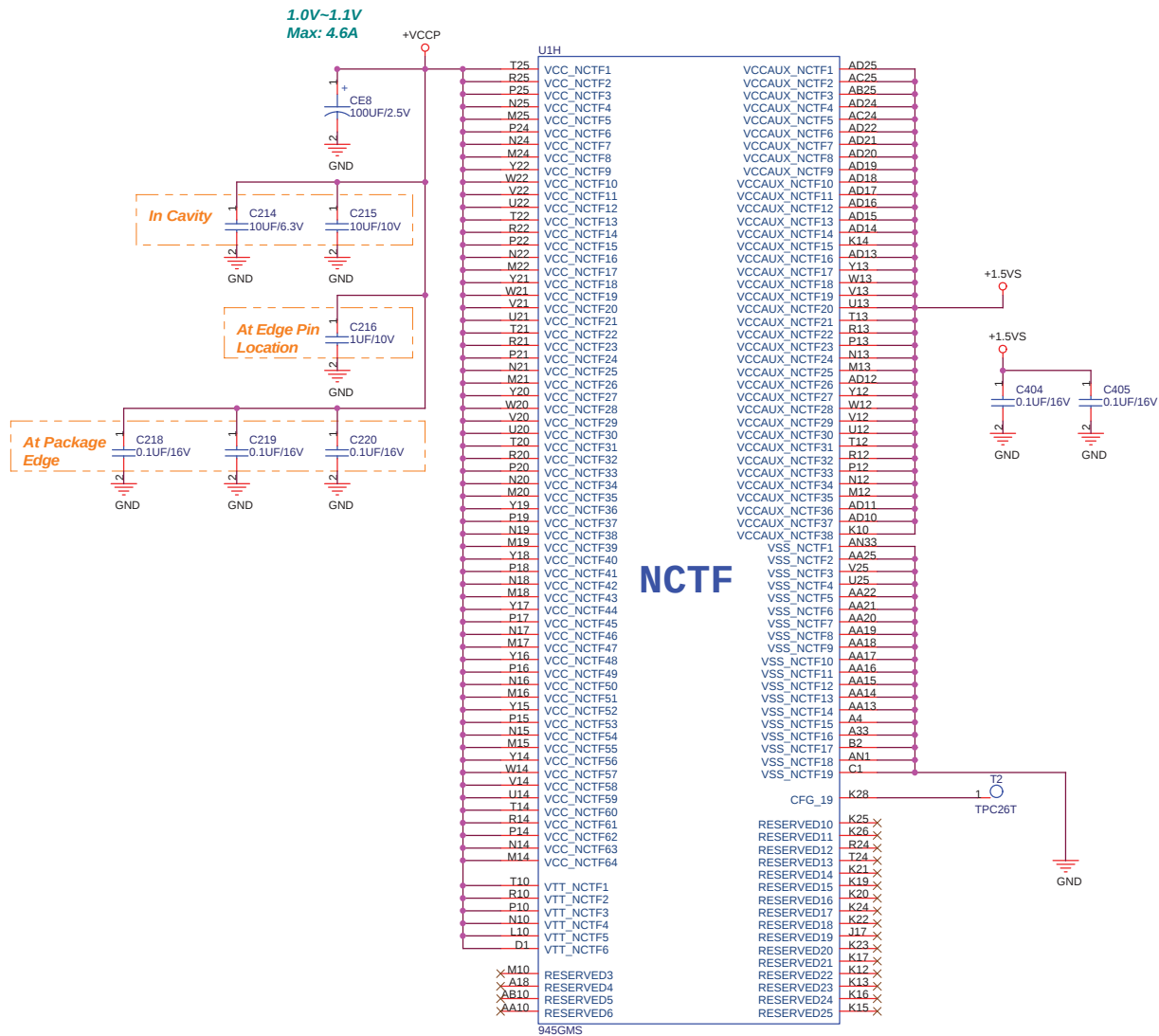
CheckList notes :Can be left as NC



/X

ASUS		Title : NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		Engineer: Satan_He	
Size A4	Project Name P901		Rev 1.1G
Date: Monday, May 19, 2008		Sheet 9 of 50	





CFG_19(K28) Strapping :
DMI LANE Reversal:
0:Normal Operation (Default)
1.:Reversal Lanes, 3->0,2->1..etc
Note:945GMS doesn't support DMI Lane Reversal

D

C

B

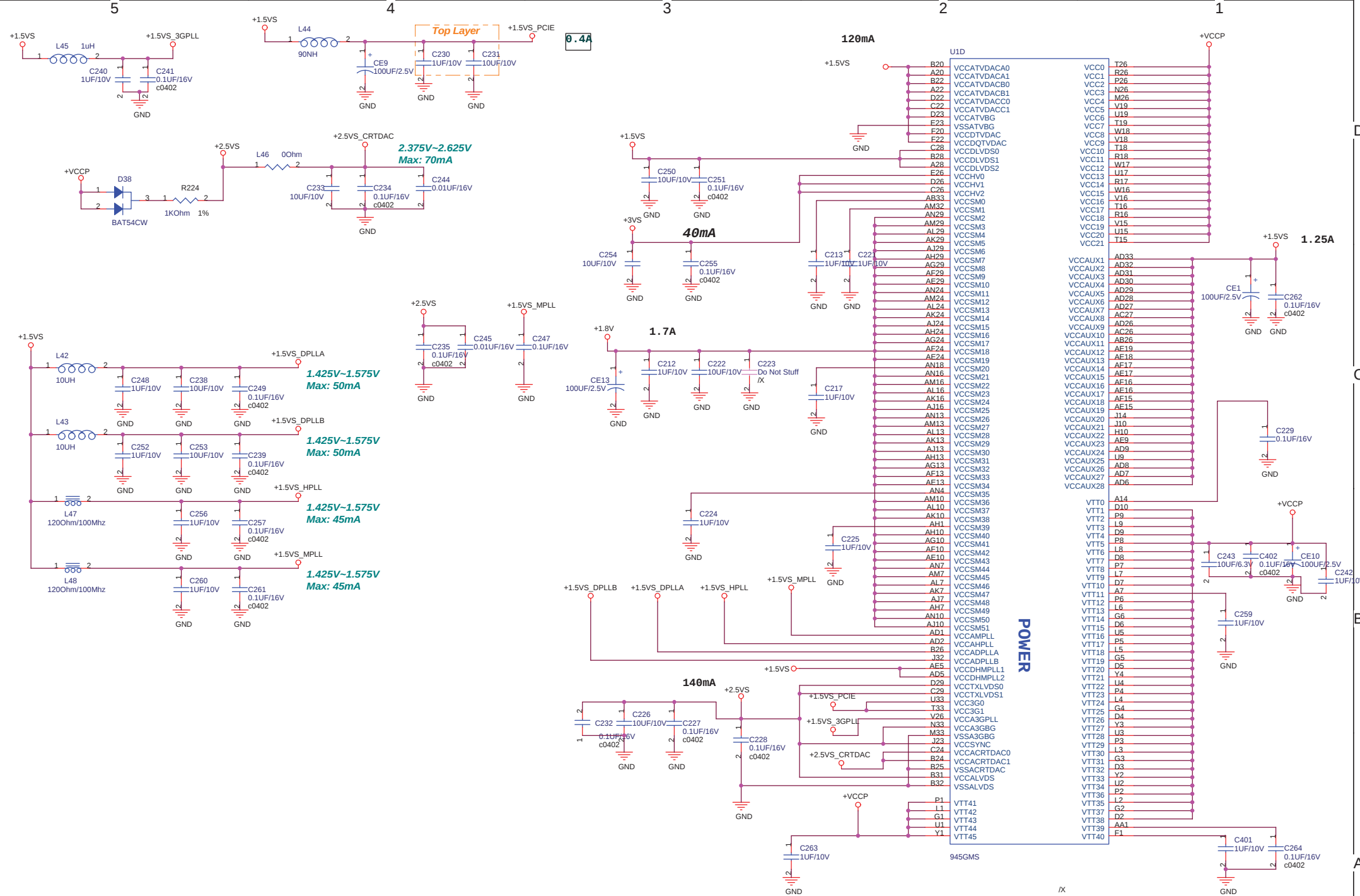
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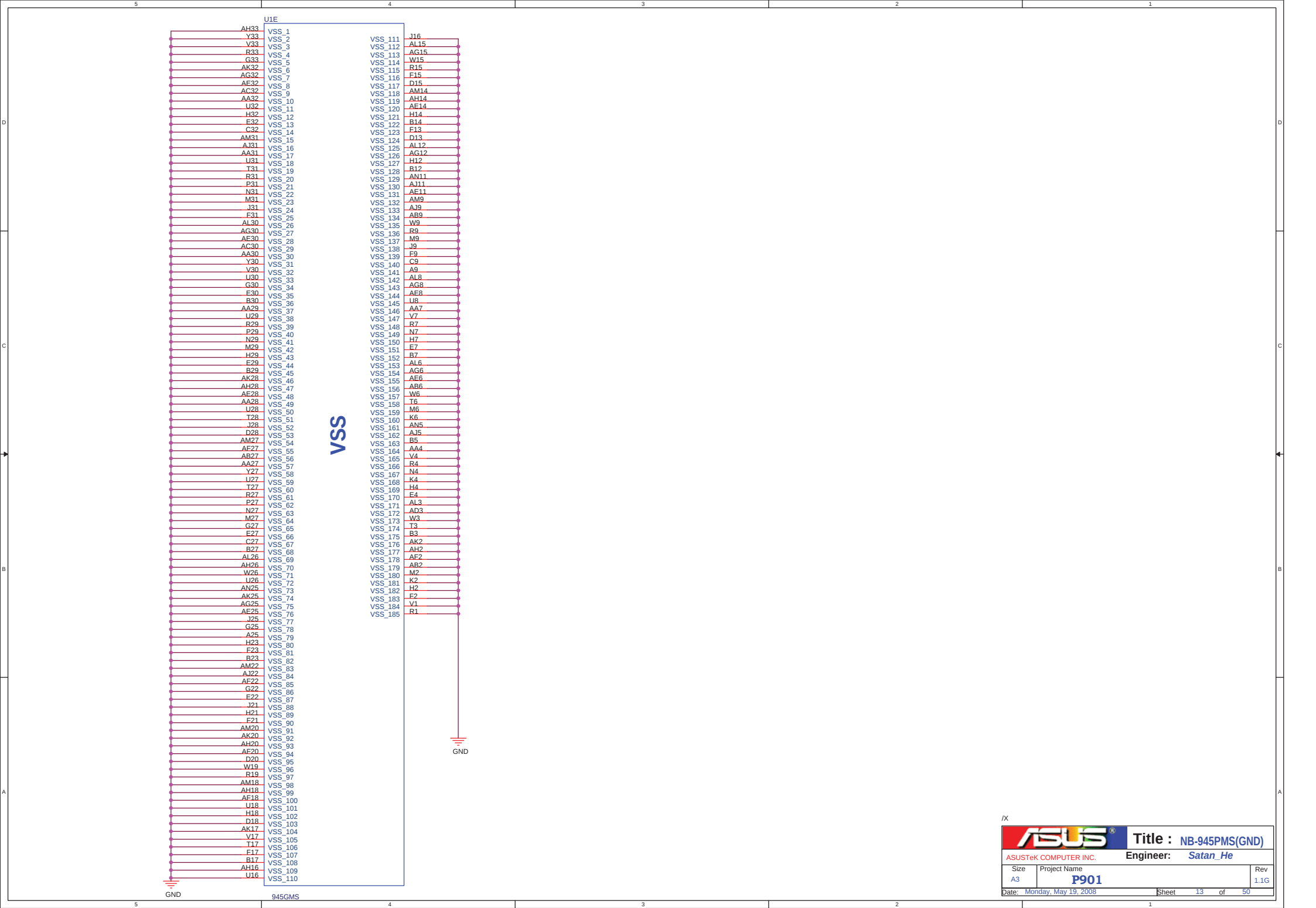
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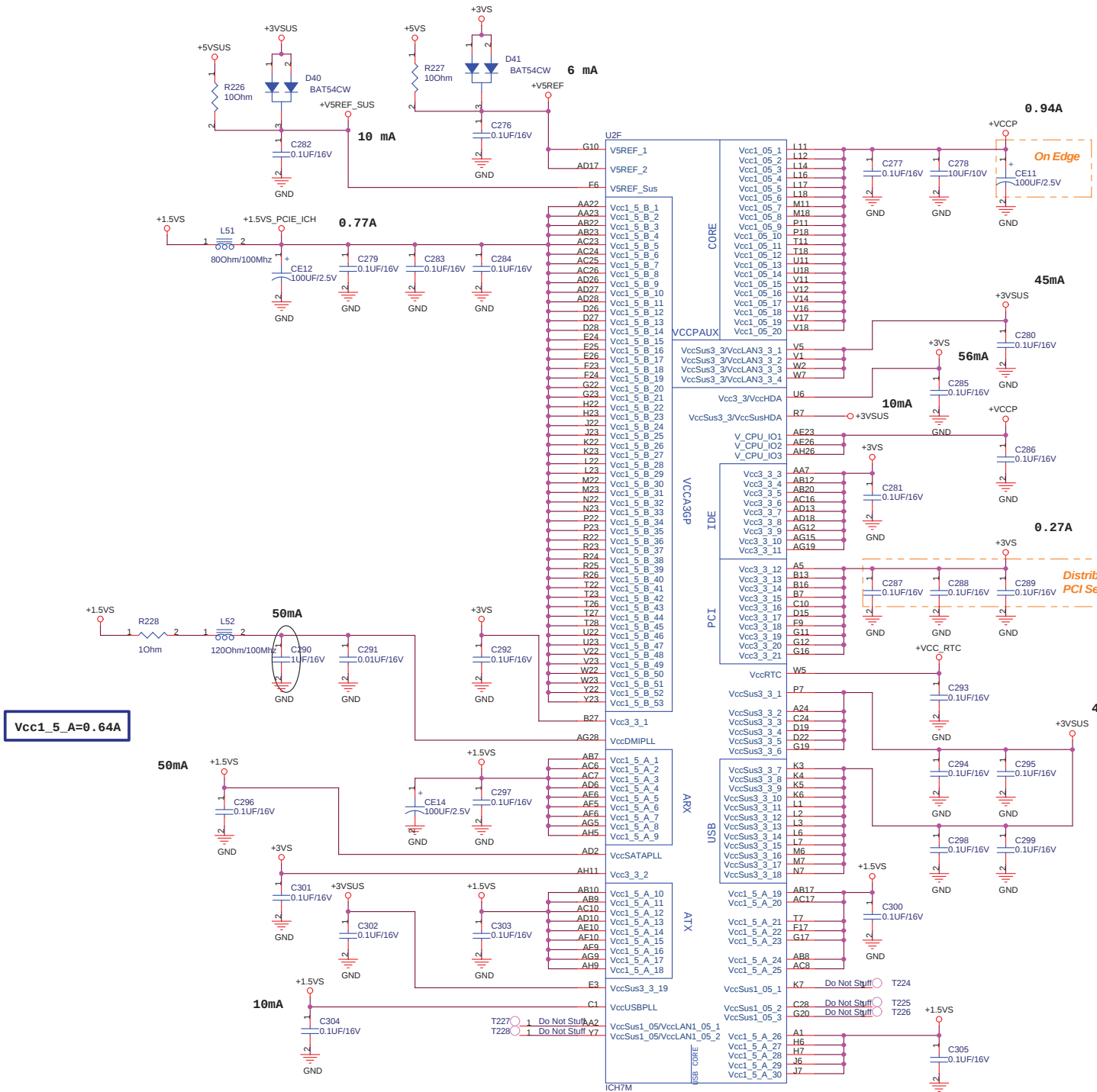
C

B

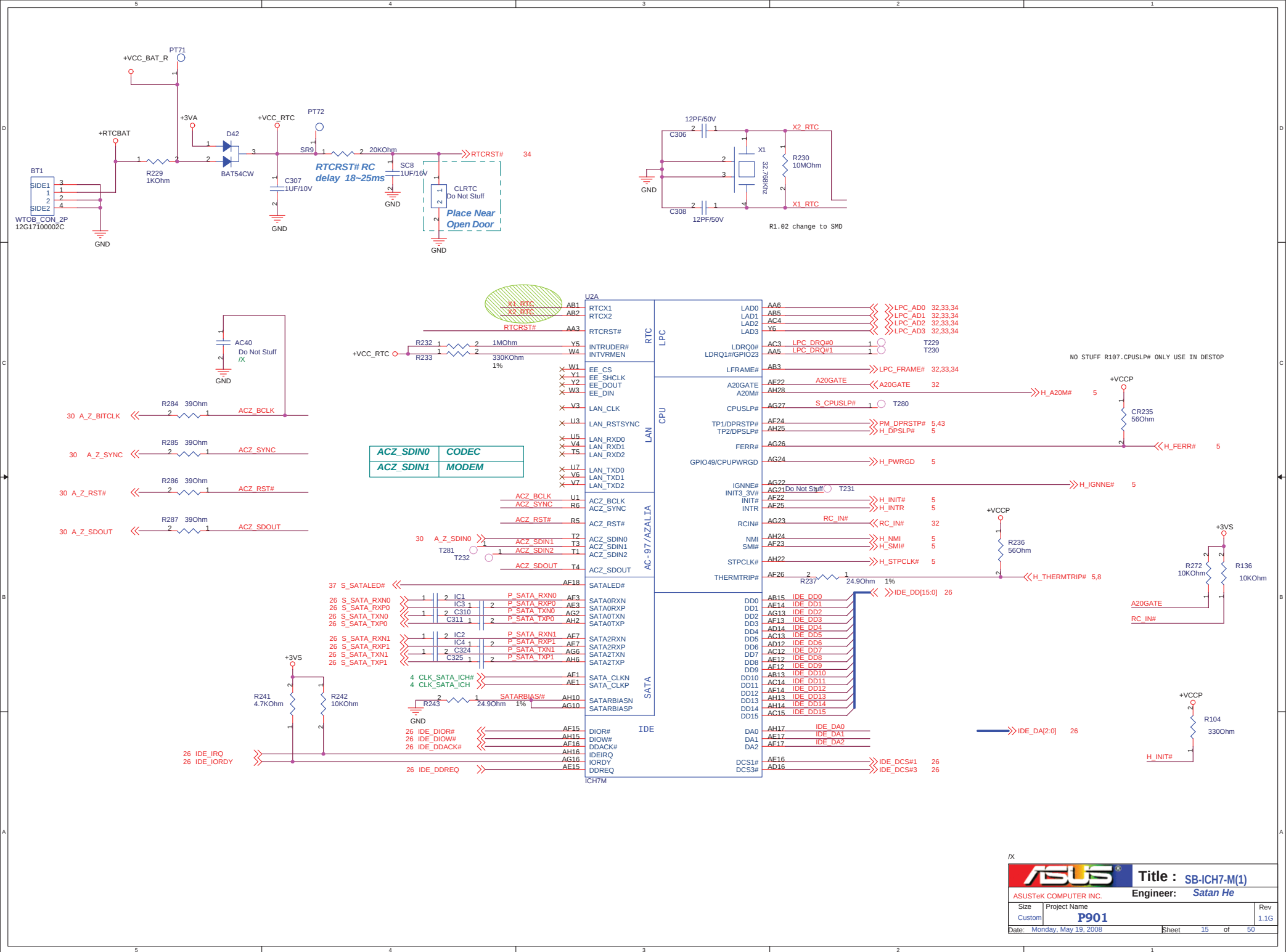
A

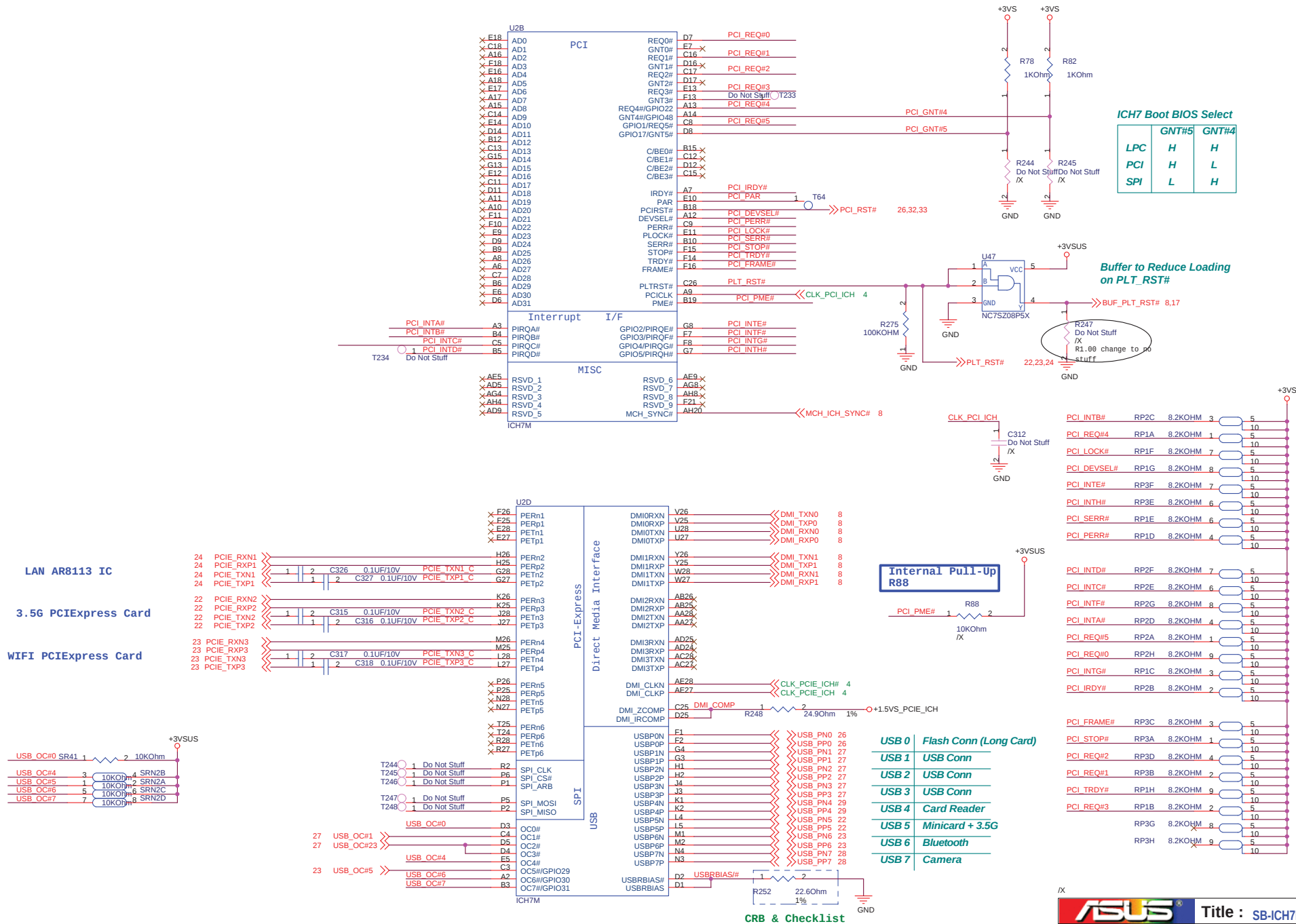


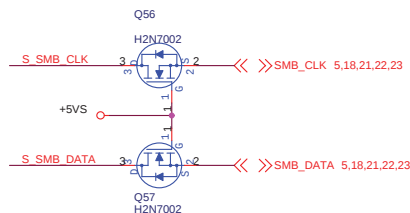
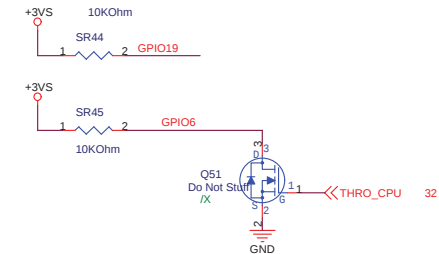




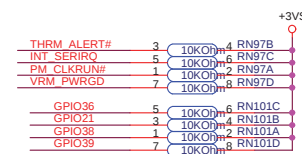
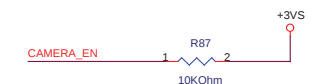
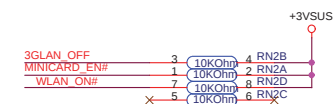
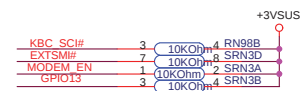
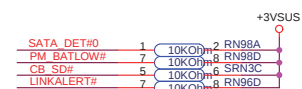
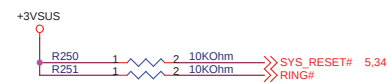
A4	Vss1	Vss98	P28
A23	Vss2	Vss99	R1
B1	Vss3	Vss100	R11
B8	Vss4	Vss101	R12
B11	Vss5	Vss102	R13
B14	Vss6	Vss103	R14
B17	Vss7	Vss104	R15
B20	Vss8	Vss105	R16
B26	Vss9	Vss106	R17
B28	Vss10	Vss107	R18
C2	Vss11	Vss108	T6
C6	Vss12	Vss109	T12
C27	Vss13	Vss110	T13
D10	Vss14	Vss111	T14
D13	Vss15	Vss112	T15
D18	Vss16	Vss113	T16
D21	Vss17	Vss114	T17
D24	Vss18	Vss115	U4
E1	Vss19	Vss116	U12
E2	Vss20	Vss117	U13
E4	Vss21	Vss118	U14
E8	Vss22	Vss119	U15
F15	Vss23	Vss120	U16
F4	Vss24	Vss121	U17
F5	Vss25	Vss122	U24
F12	Vss26	Vss123	U25
F22	Vss27	Vss124	U26
F28	Vss28	Vss125	V13
G1	Vss29	Vss126	V15
G2	Vss30	Vss127	V16
G5	Vss31	Vss128	V24
G6	Vss32	Vss129	V27
G9	Vss33	Vss130	V28
G14	Vss34	Vss131	W6
G18	Vss35	Vss132	W24
G21	Vss36	Vss133	W25
G24	Vss37	Vss134	W26
G25	Vss38	Vss135	Y2
G26	Vss39	Vss136	Y24
H3	Vss40	Vss137	Y27
H4	Vss41	Vss138	Y28
H5	Vss42	Vss139	AA1
H24	Vss43	Vss140	AA24
H27	Vss44	Vss141	AA25
H28	Vss45	Vss142	AA26
J1	Vss46	Vss143	AB4
J2	Vss47	Vss144	AB6
J5	Vss48	Vss145	AB11
J24	Vss49	Vss146	AB14
J25	Vss50	Vss147	AB16
J26	Vss51	Vss148	AB19
K24	Vss52	Vss149	AB21
K27	Vss53	Vss150	AB24
K28	Vss54	Vss151	AB27
L15	Vss55	Vss152	AB28
L24	Vss56	Vss153	AC2
L25	Vss57	Vss154	AC5
L26	Vss58	Vss155	AC9
L27	Vss59	Vss156	AC11
M3	Vss60	Vss157	AD1
M4	Vss61	Vss158	AD3
M5	Vss62	Vss159	AD4
M12	Vss63	Vss160	AD7
M13	Vss64	Vss161	AD8
M14	Vss65	Vss162	AD11
M15	Vss66	Vss163	AD15
M16	Vss67	Vss164	AD19
M17	Vss68	Vss165	AD23
M24	Vss69	Vss166	AE4
M27	Vss70	Vss167	AE8
M28	Vss71	Vss168	AE11
N1	Vss72	Vss169	AE13
N2	Vss73	Vss170	AE18
N5	Vss74	Vss171	AE21
N6	Vss75	Vss172	AE24
N11	Vss76	Vss173	AE25
N12	Vss77	Vss174	AE2
N13	Vss78	Vss175	AE2
N14	Vss79	Vss176	AE4
N15	Vss80	Vss177	AE8
N16	Vss81	Vss178	AE11
N17	Vss82	Vss179	AE27
N18	Vss83	Vss180	AE28
N24	Vss84	Vss181	AG1
N25	Vss85	Vss182	AG3
N26	Vss86	Vss183	AG7
P2	Vss87	Vss184	AG11
P4	Vss88	Vss185	AG14
P12	Vss89	Vss186	AG17
P13	Vss90	Vss187	AG20
P14	Vss91	Vss188	AG25
P15	Vss92	Vss189	AH1
P16	Vss93	Vss190	AH3
P17	Vss94	Vss191	AH7
P24	Vss95	Vss192	AH12
P27	Vss96	Vss193	AH23
P27	Vss97	Vss194	AH27

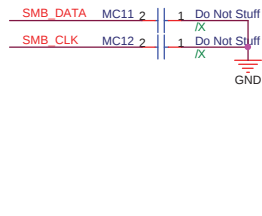
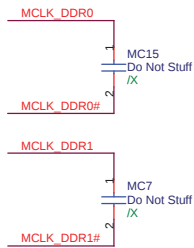




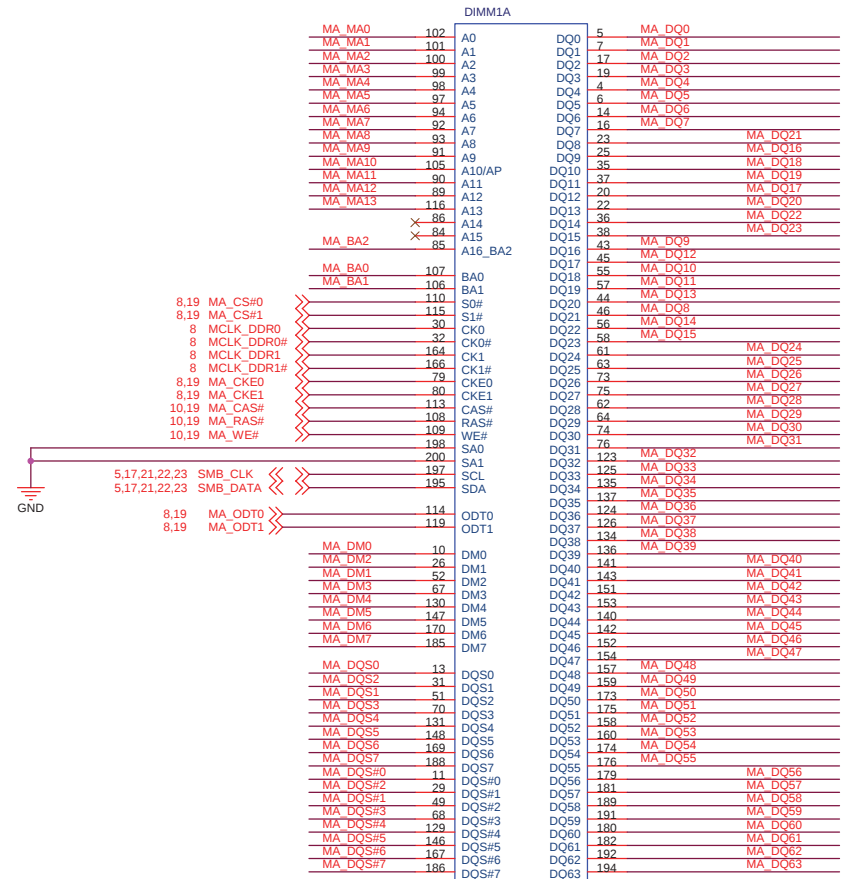


WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x

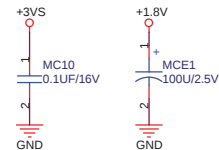
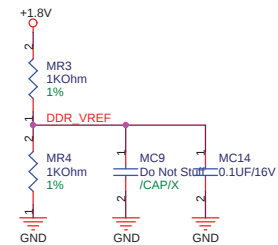
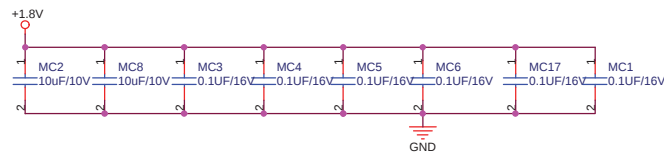




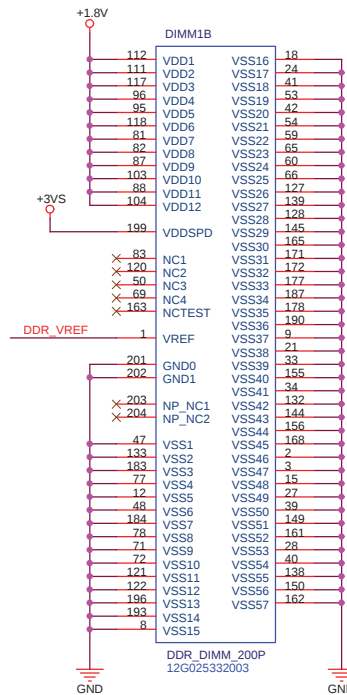
STD Type



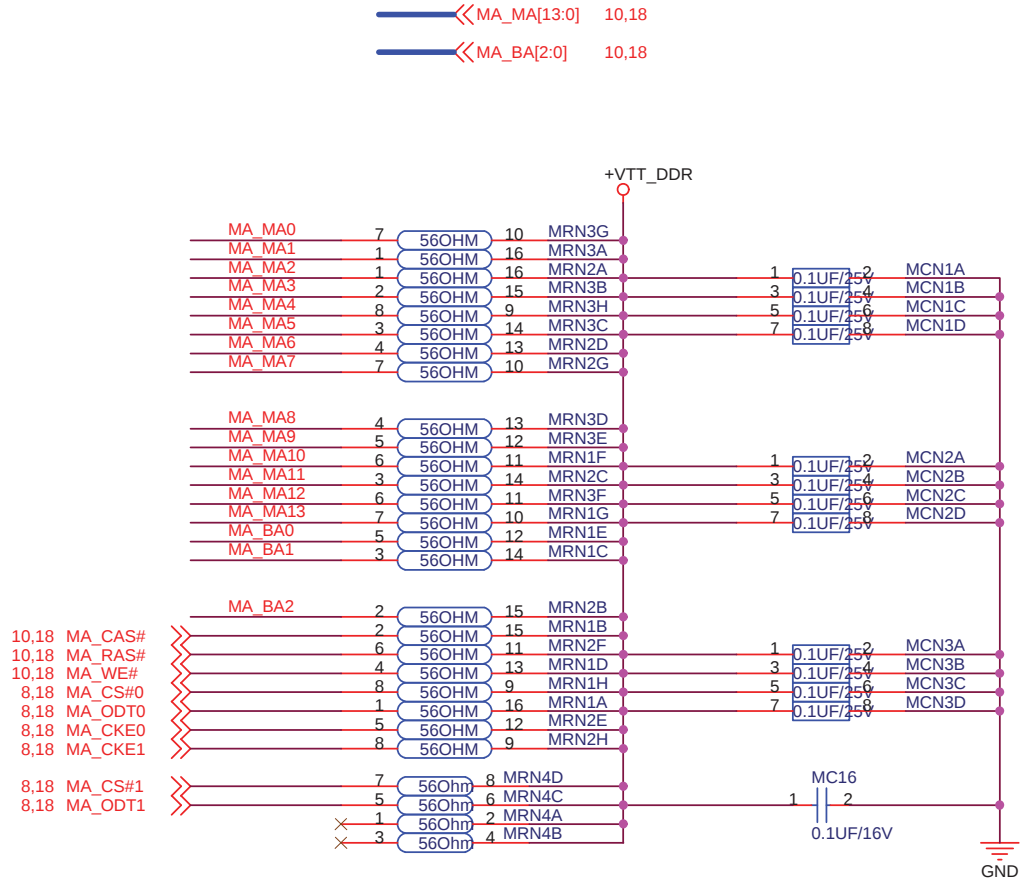
DDR_DIMM_200P
12G025332003



GROUP1
GROUP2
SWAP

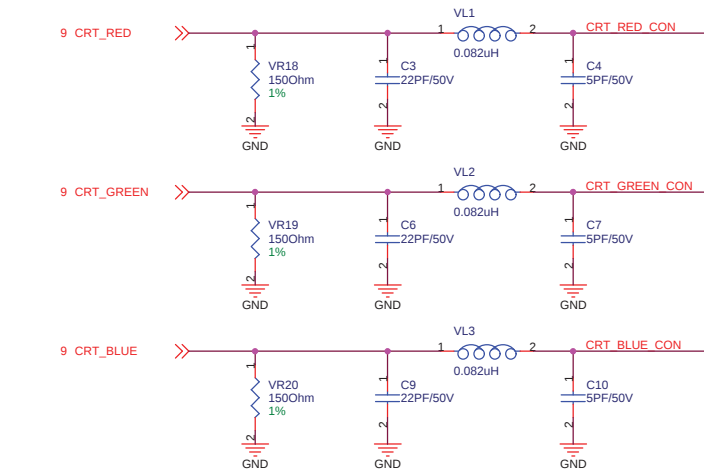


DDR_DIMM_200P
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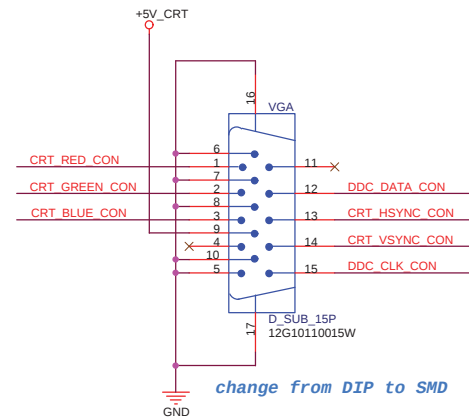
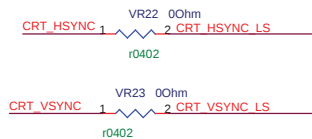
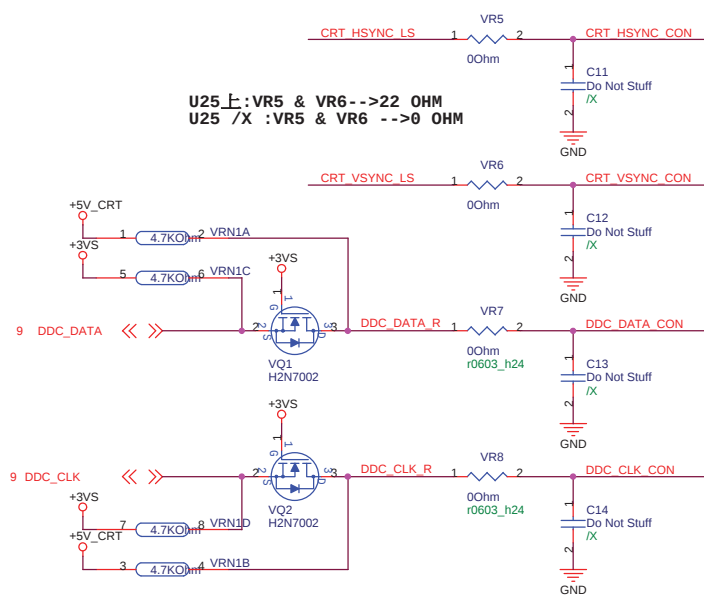


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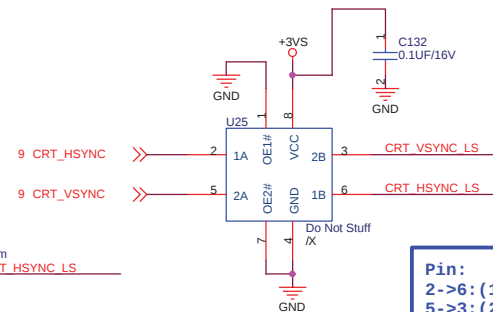
ASUS®		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name P901	Rev 1.1G	
Date: Monday, May 19, 2008		Sheet	19 of 47



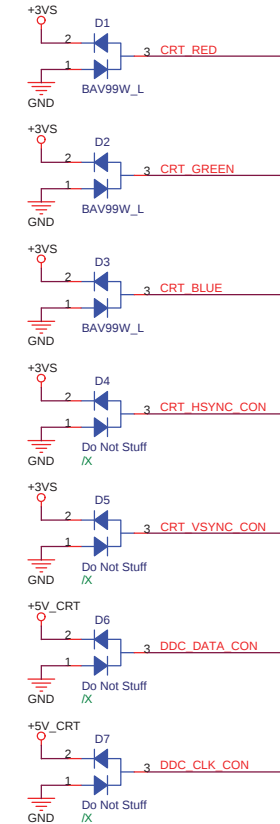
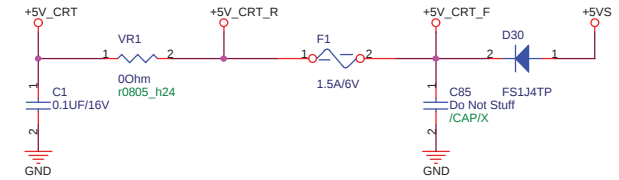
U25上:VR5 & VR6-->22 OHM
U25 /X :VR5 & VR6 -->0 OHM

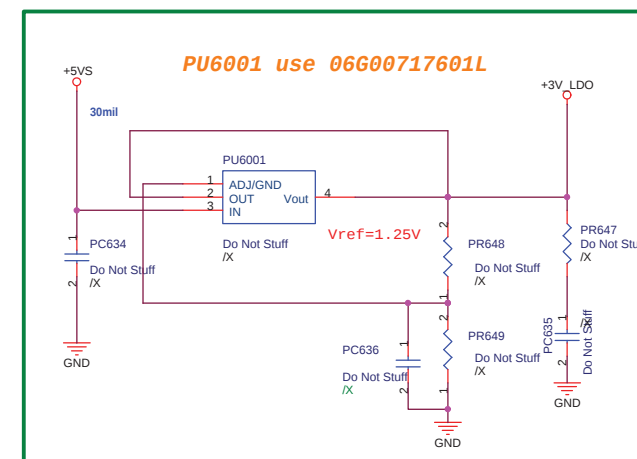
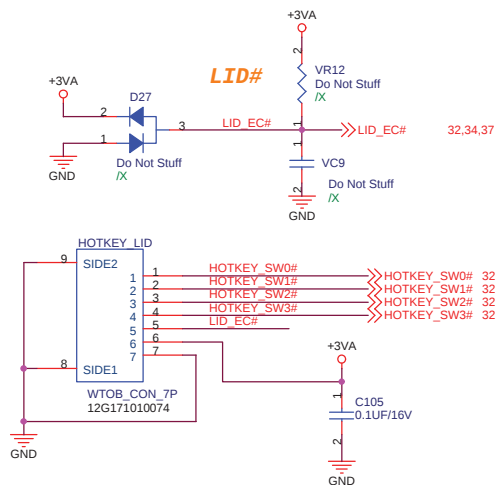


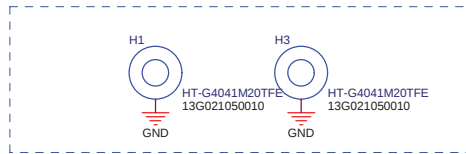
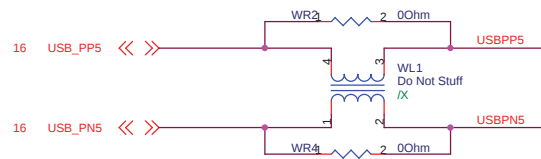
VGA use 12G10110015W & 12G10110015N



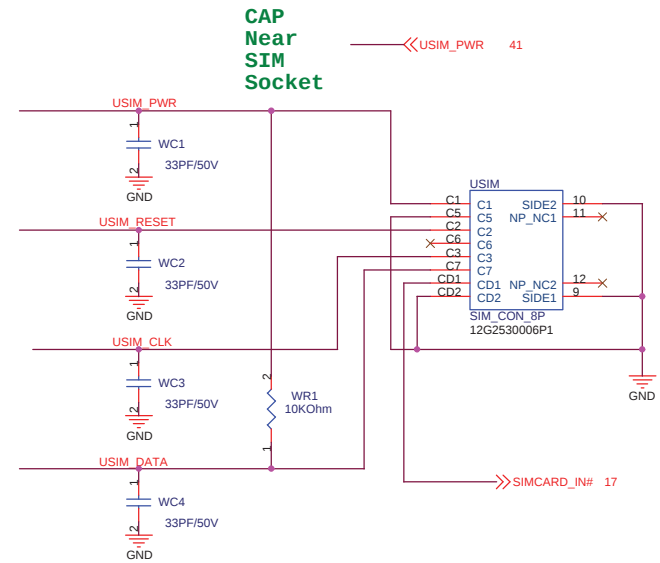
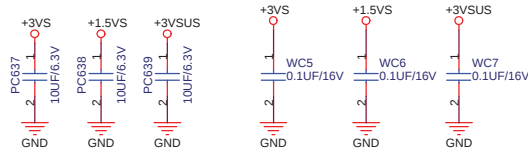
Pin:
2->6: (1A->1B)
5->3: (2A->2B)



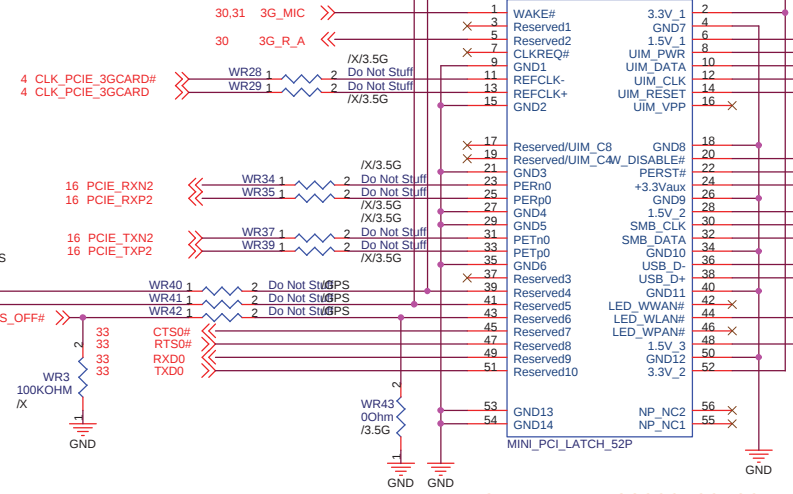




MINI CARD NUT(1.6mm) *2

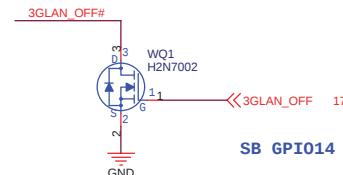
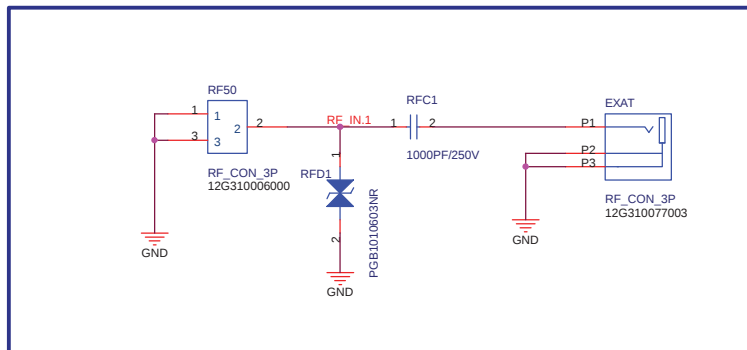


CAP
Near
SIM
Socket



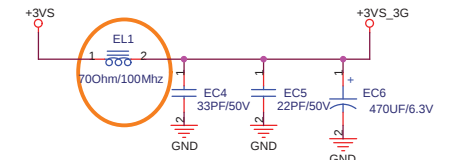
MINICARD use 12G03010052Q

External Antenna

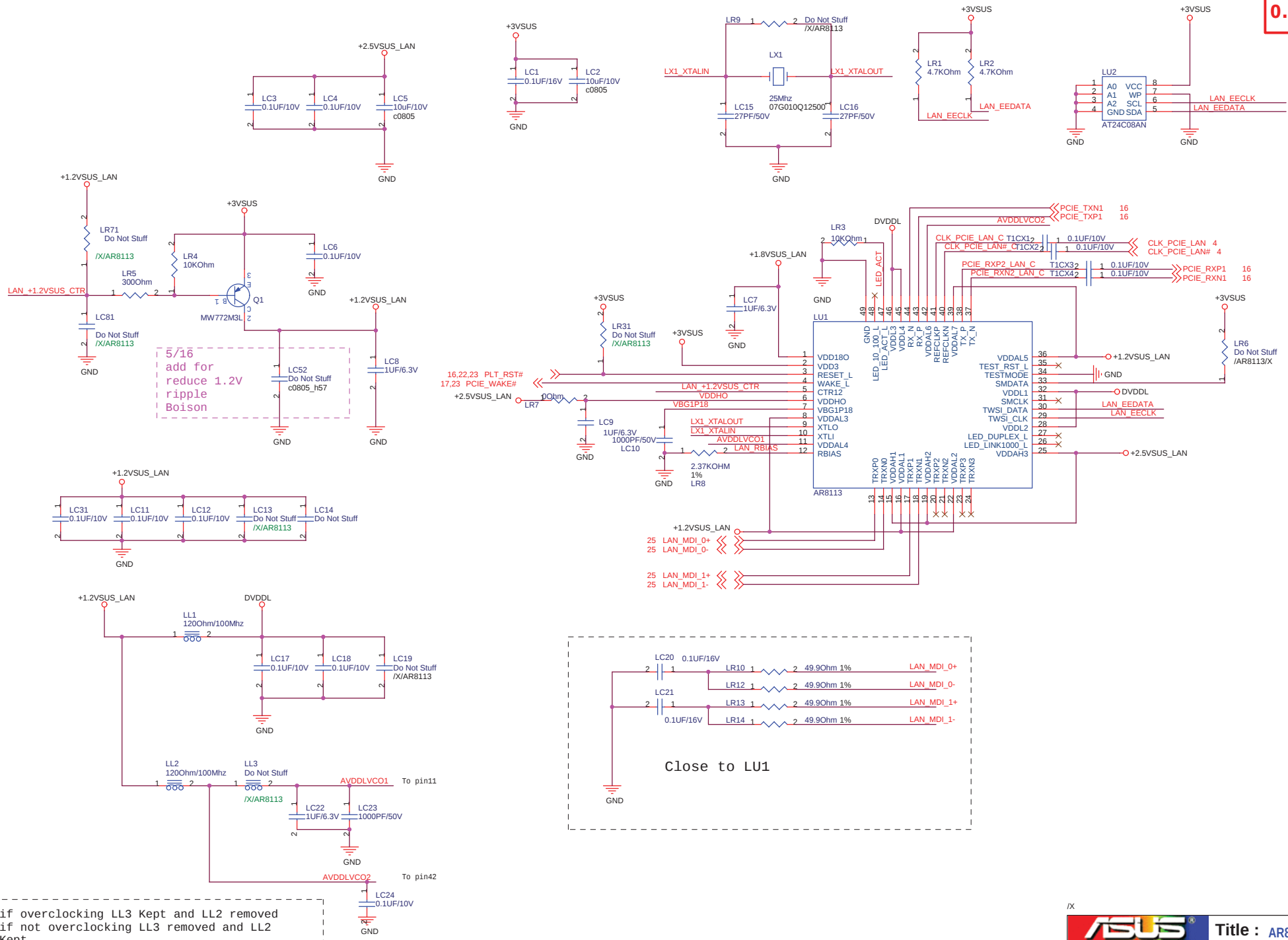


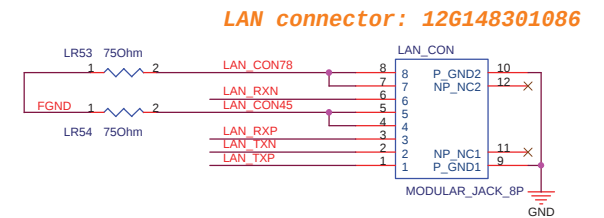
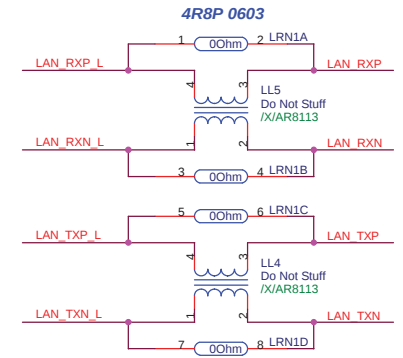
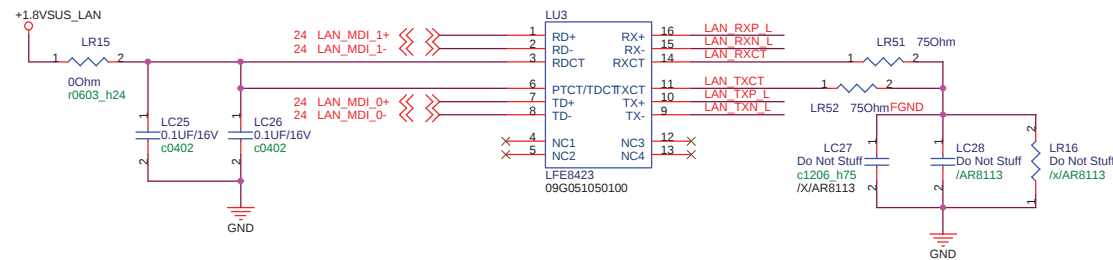
SB 6PI014

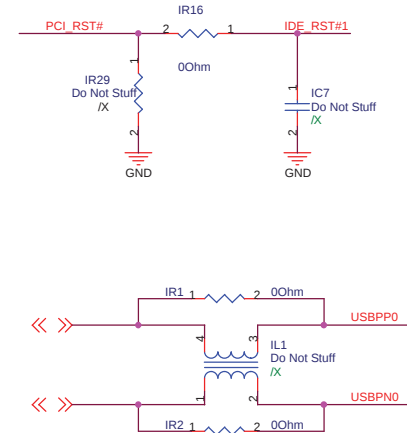
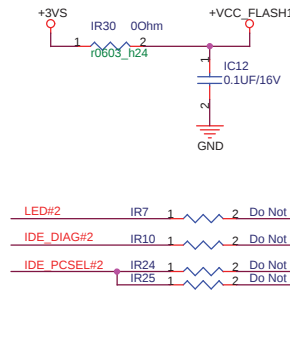
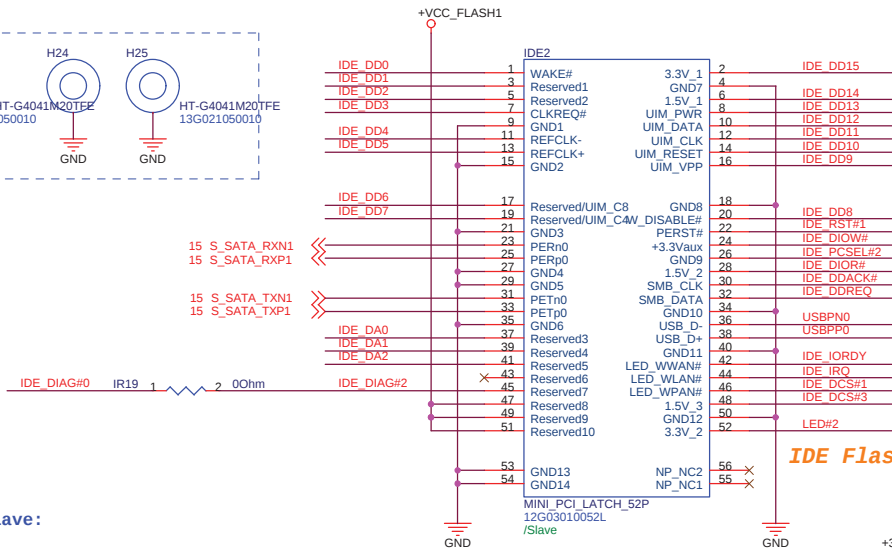
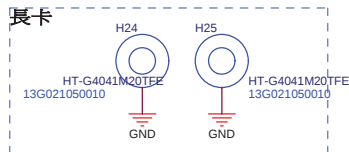
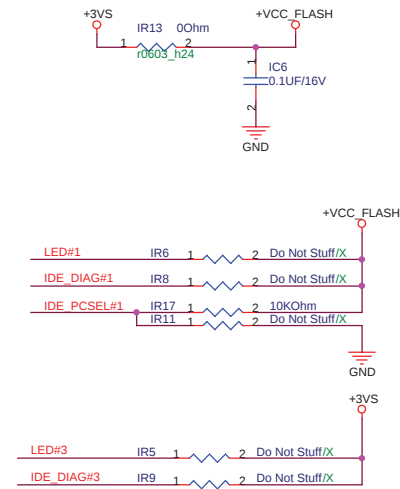
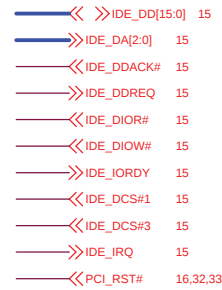
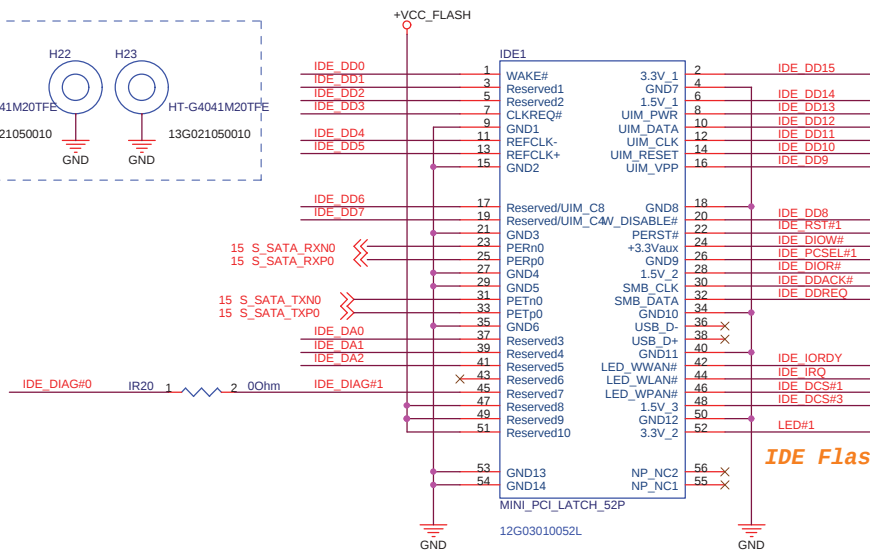
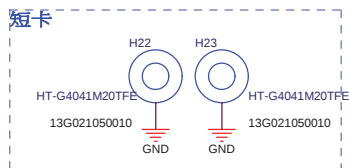
2008/03/11 change



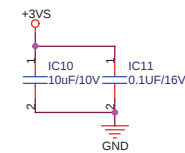
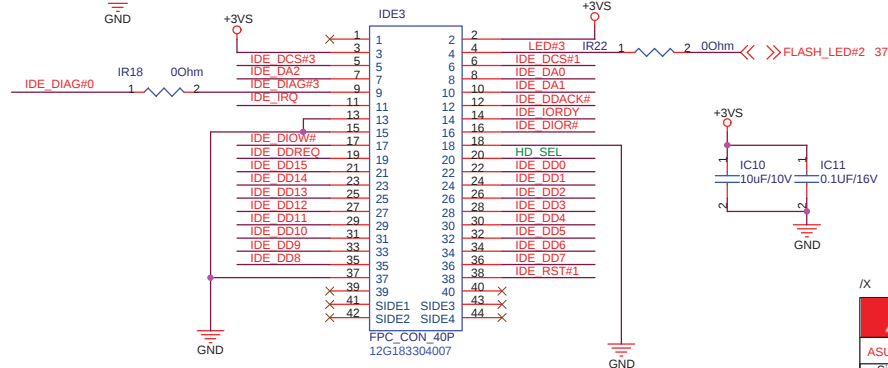
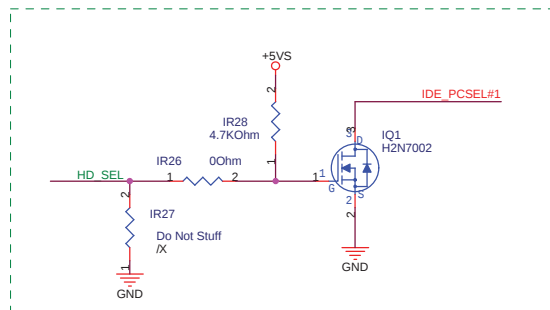
3.5G Module & External Antenna			
ASUS		Title :	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size	Project Name		Rev
A3	P901		1.1G
Date: Monday, May 19, 2008		Sheet	22 of 47



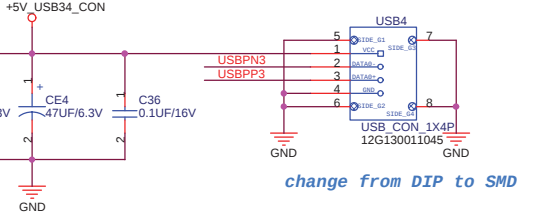
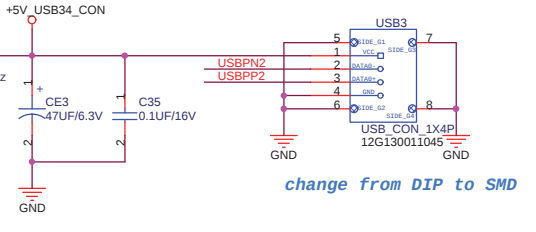
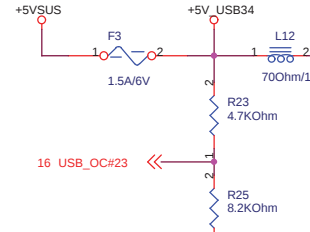
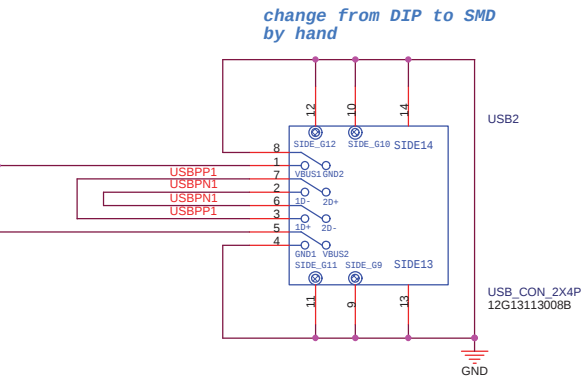
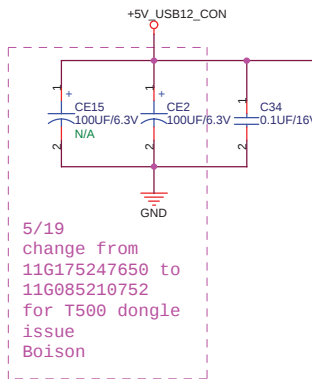
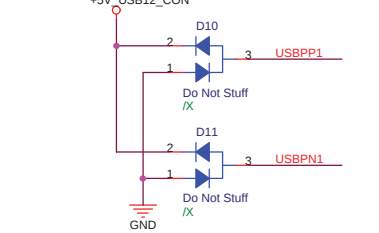
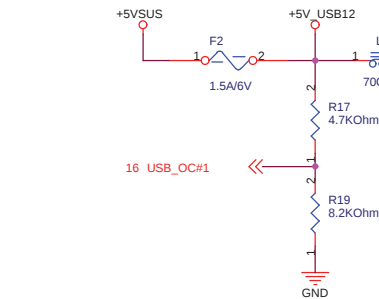
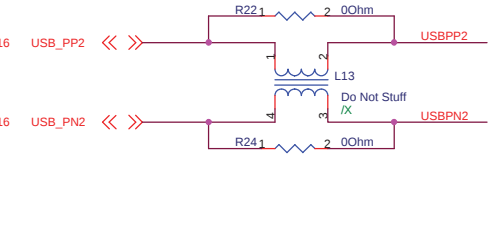
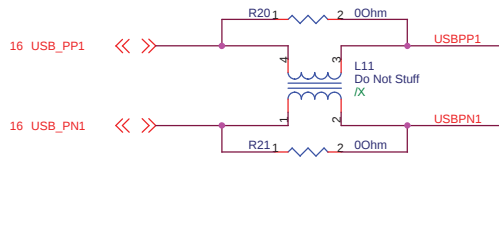




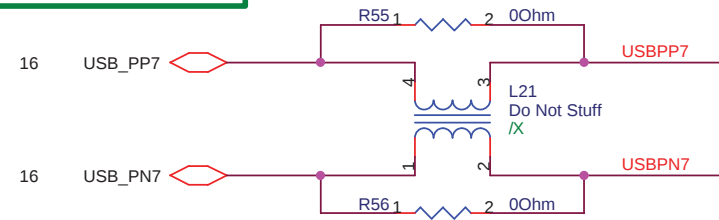
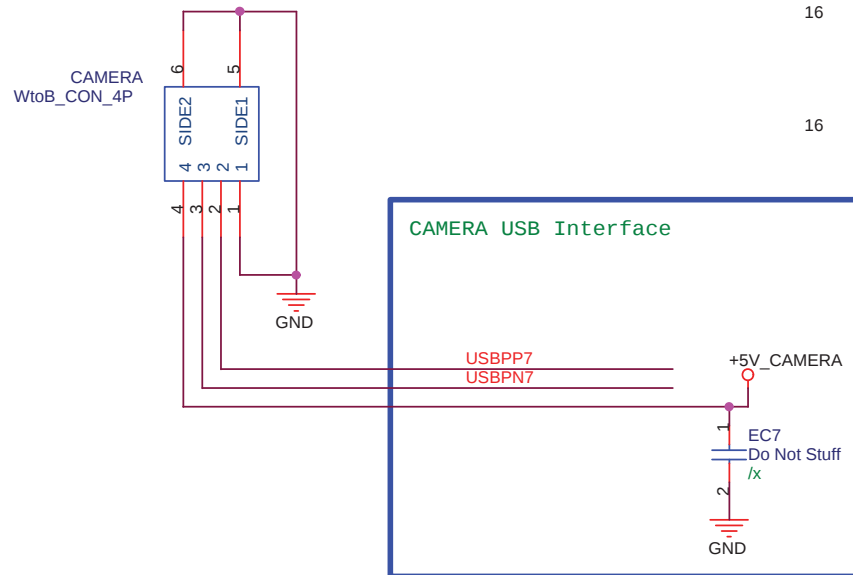
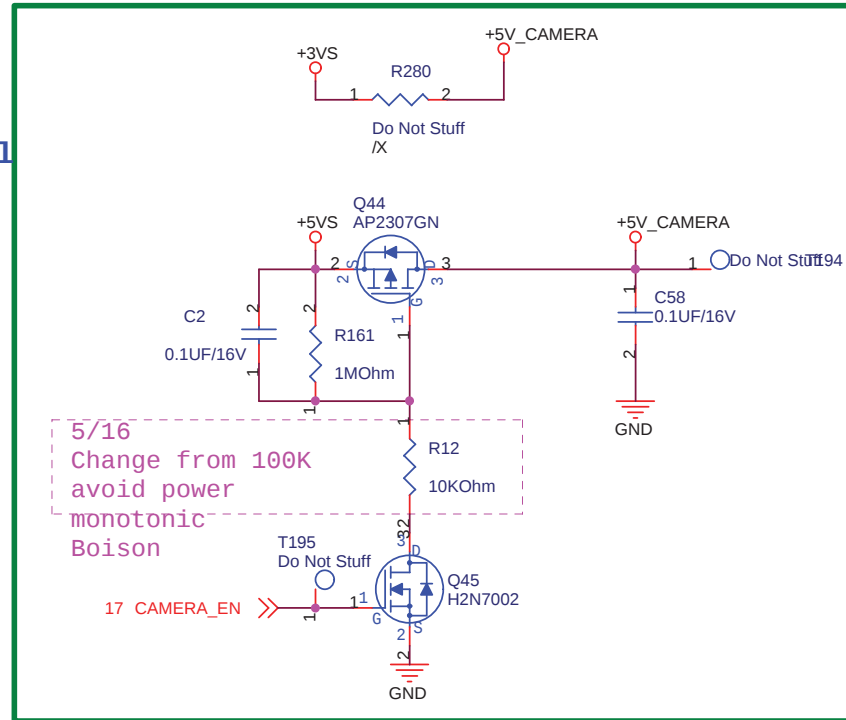
```
HD Master/Slave:
Master:Low
Slave :NC or High
Default :High
```



Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?

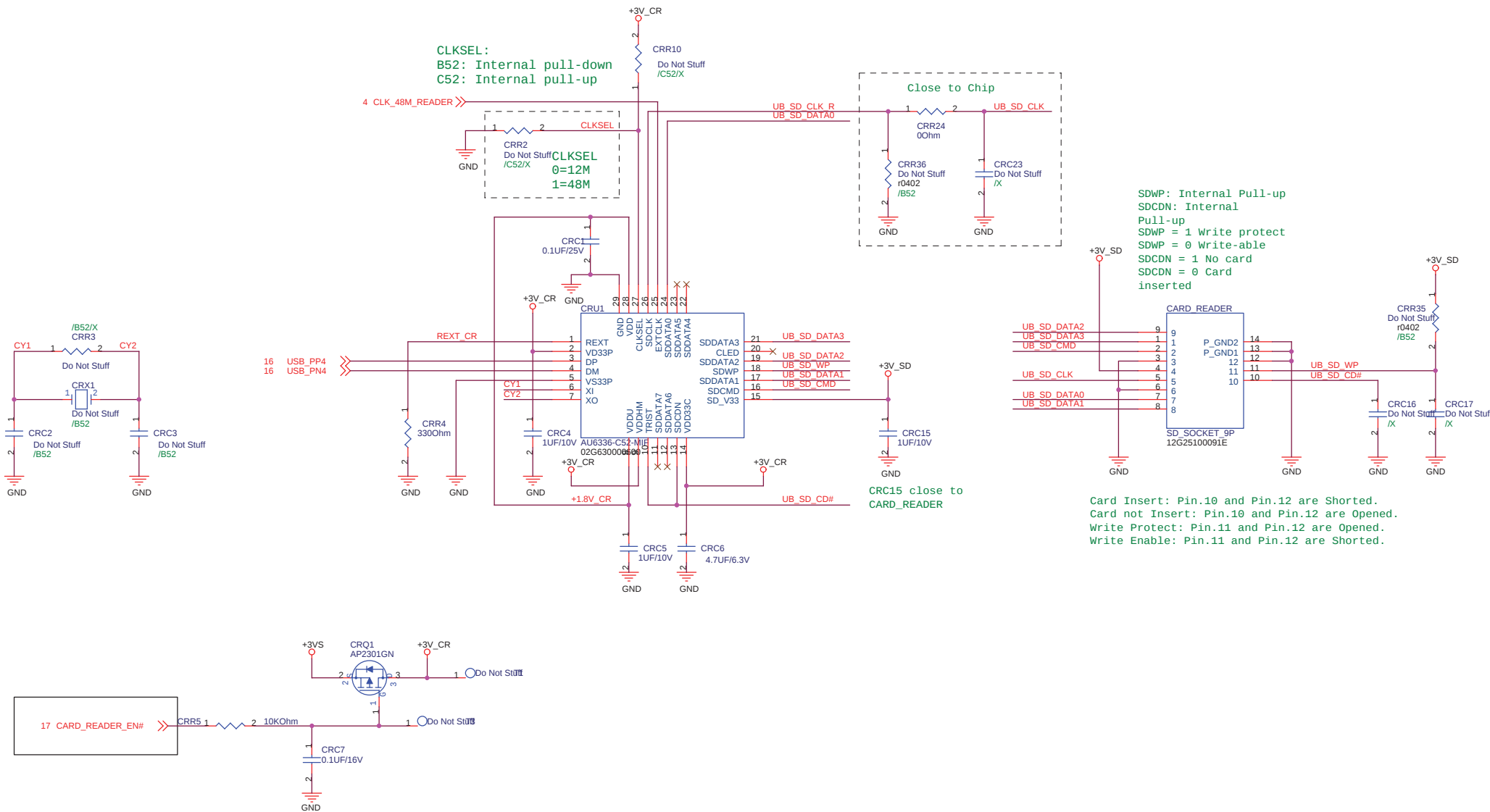


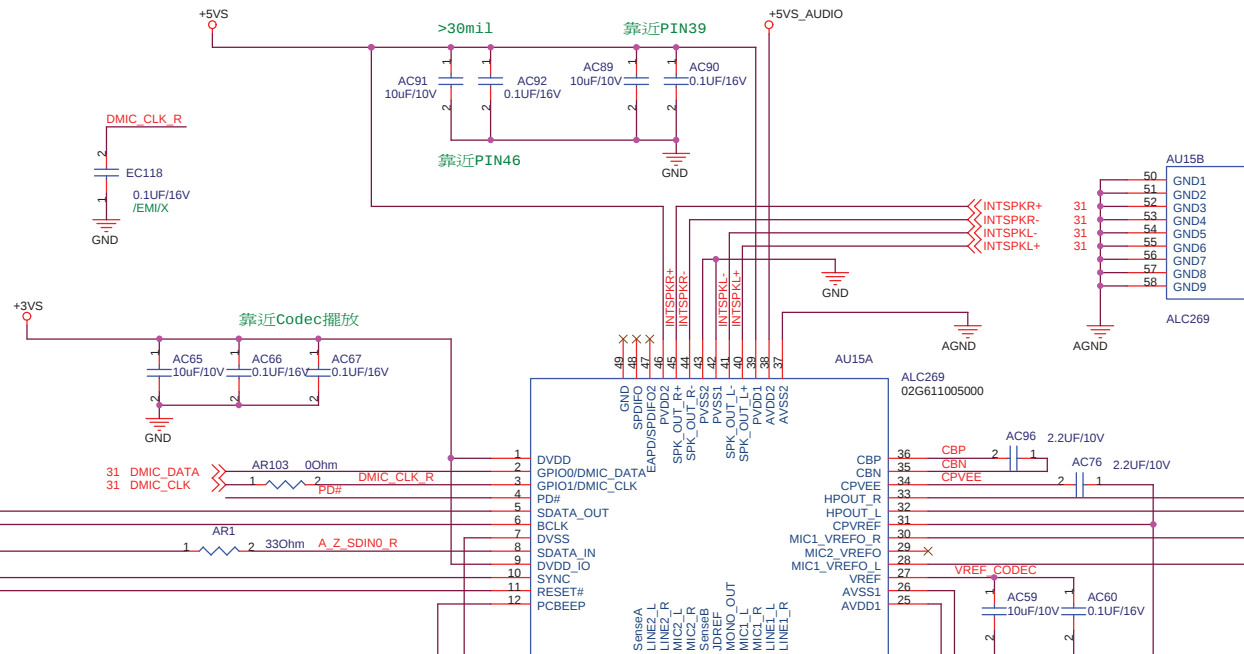
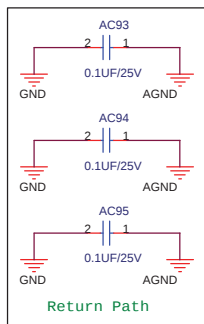
Power Control



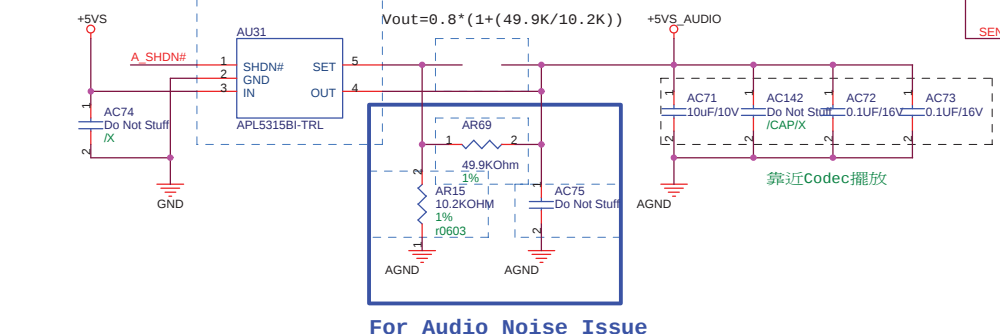
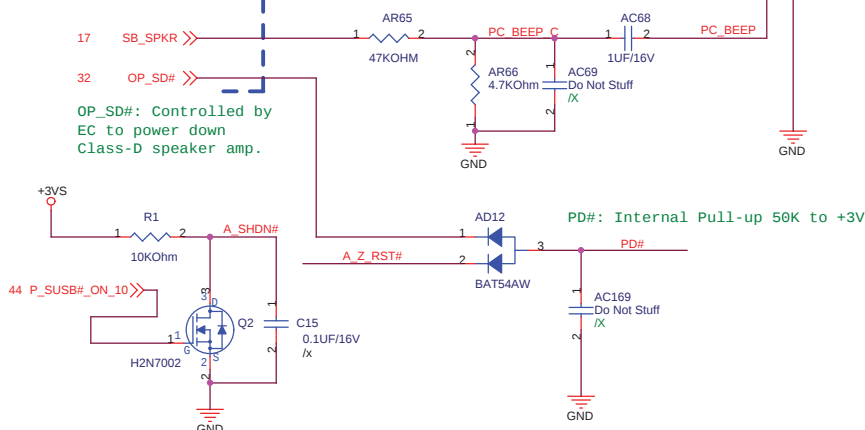
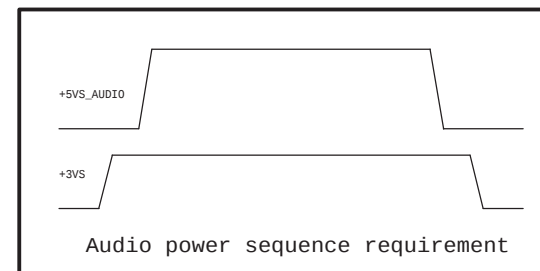
/X

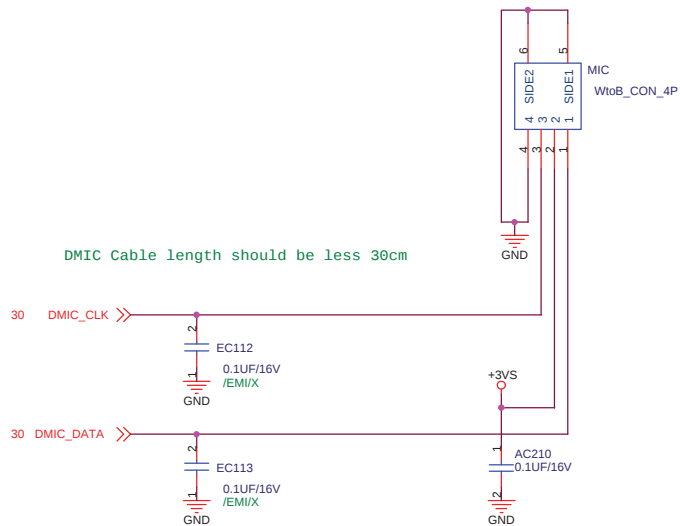
ASUS		Title : Camera Power	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name P901		Rev 1.1G
Date: Monday, May 19, 2008	Sheet 28	of 47	



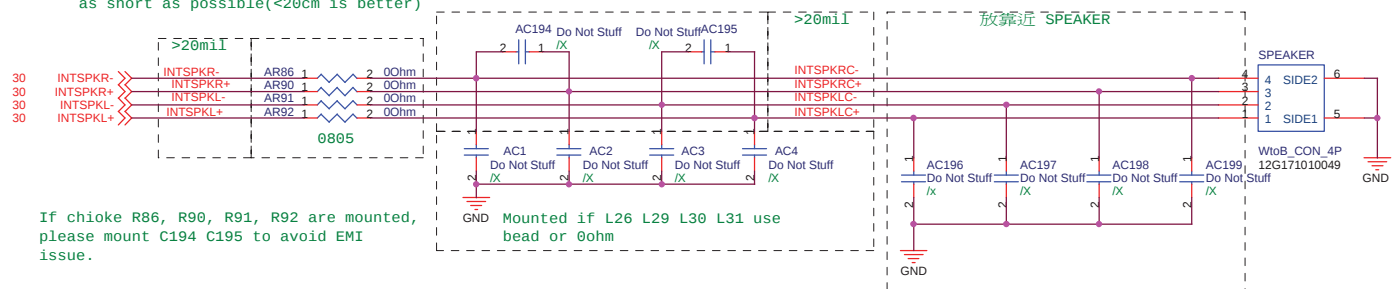


- Change Note
1. Remove AR34, AR63 for cost down
 2. Add +5VS_AUDIO shut_down control
 3. Remove net name +3VS_AUDIO
 4. Add diagram for power sequence requirement

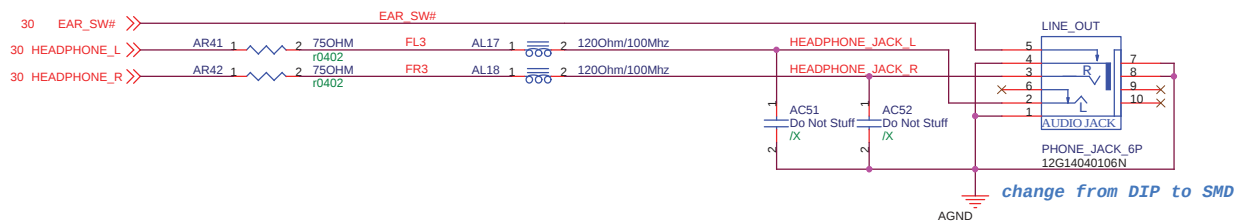




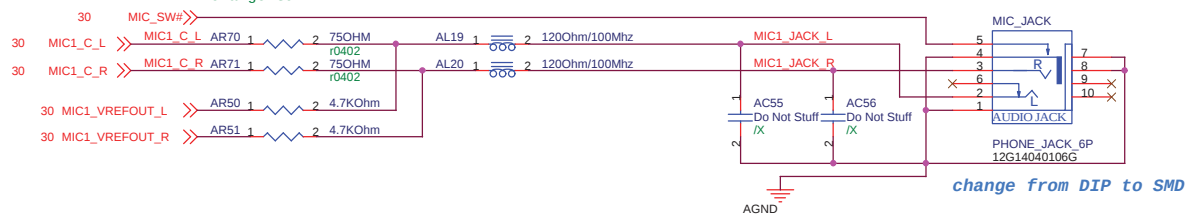
Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)

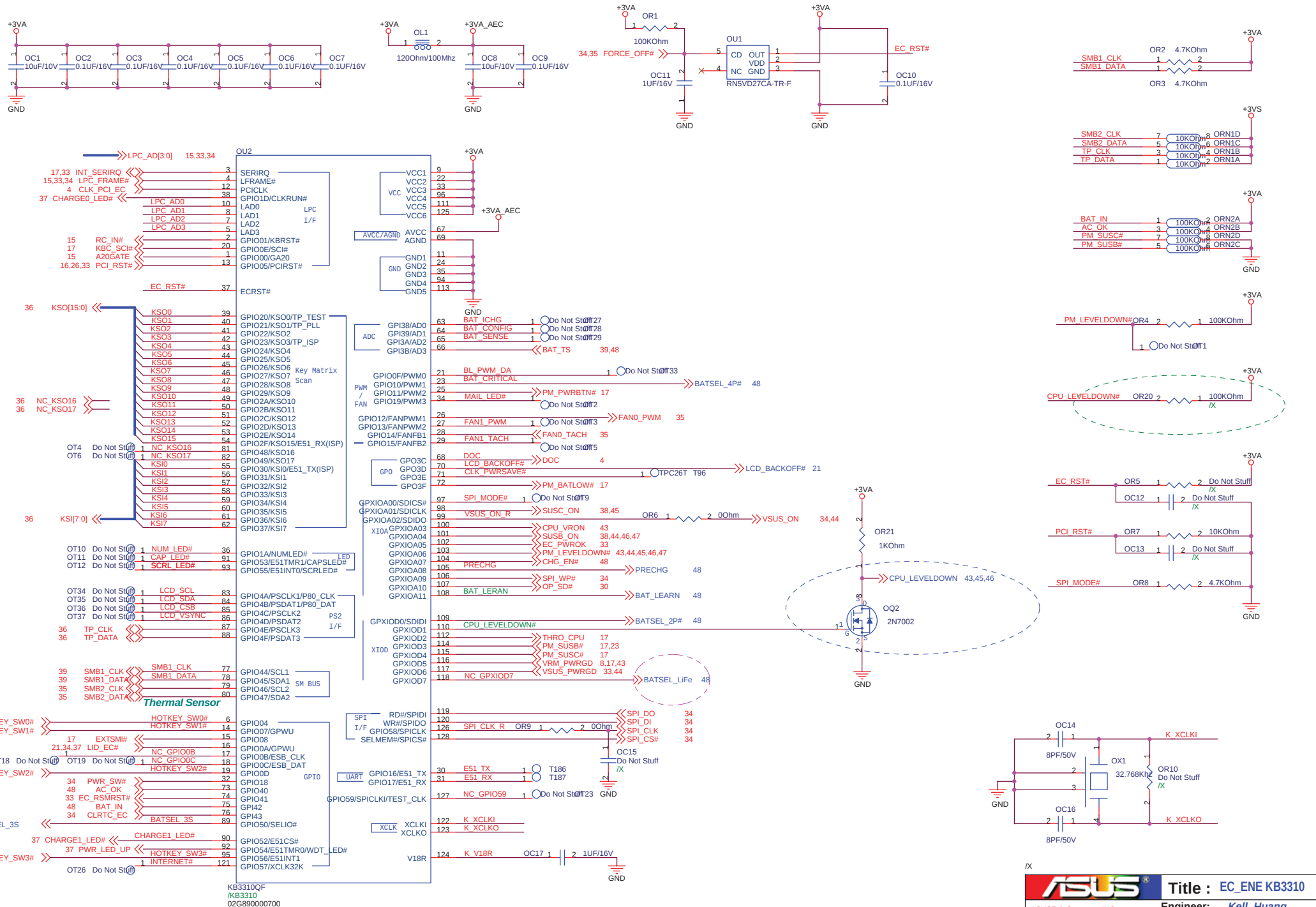


LINE_OUT use 12G14040106N

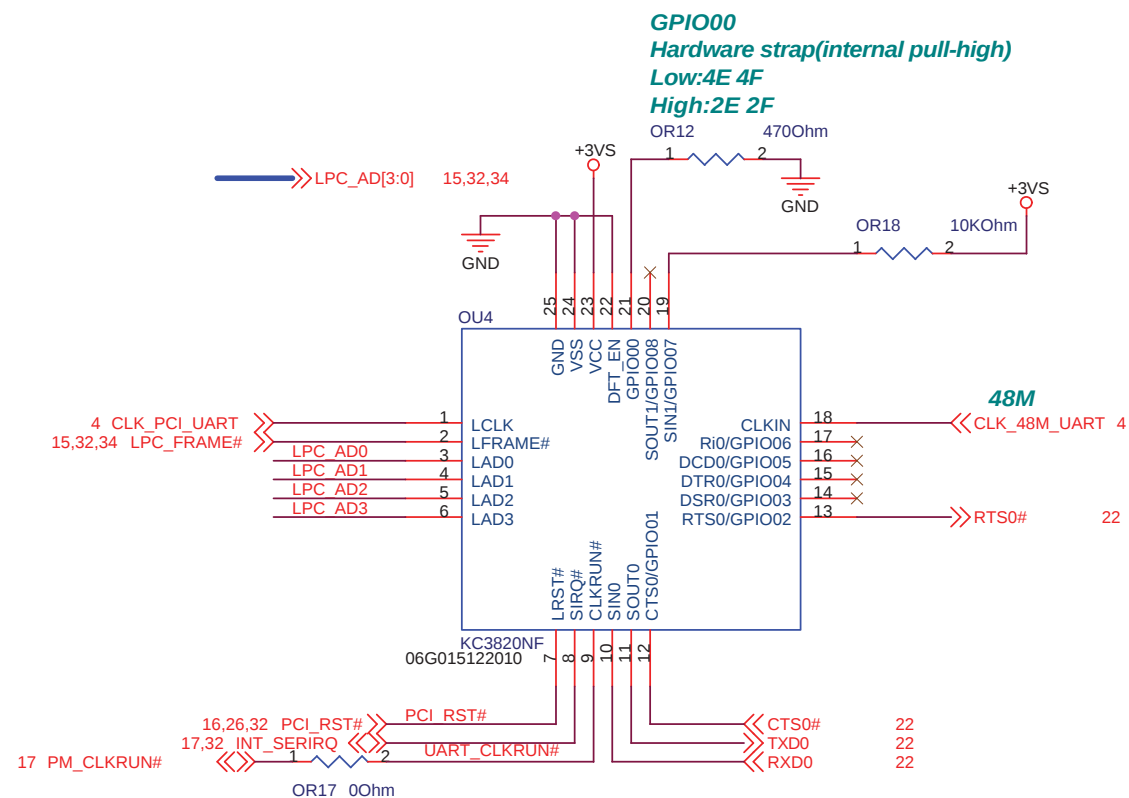
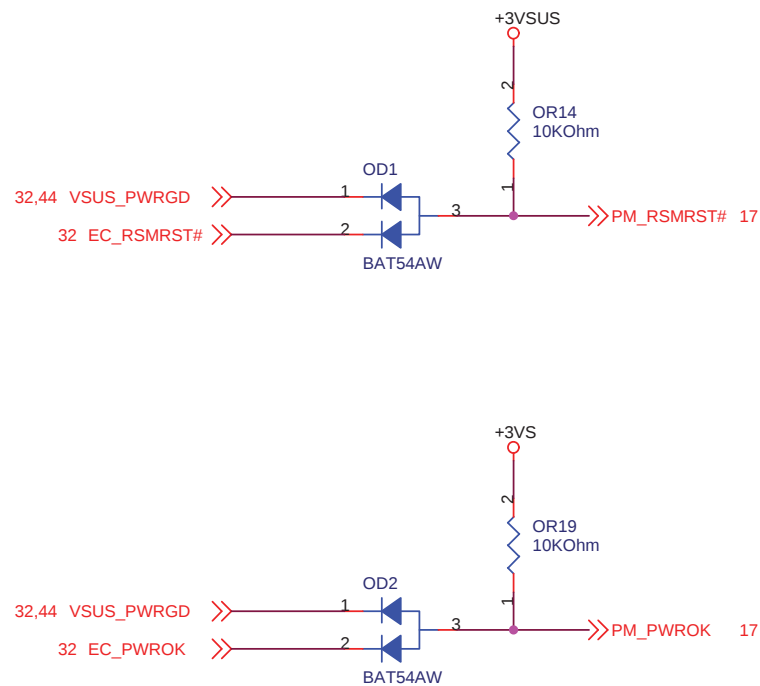


MIC_JACK use 12G14040106G





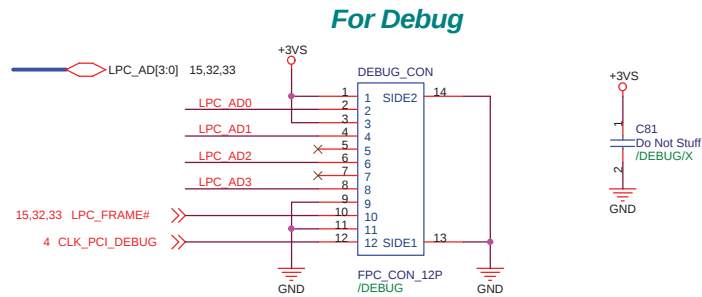
R1.2G to resolve auto-boot issue



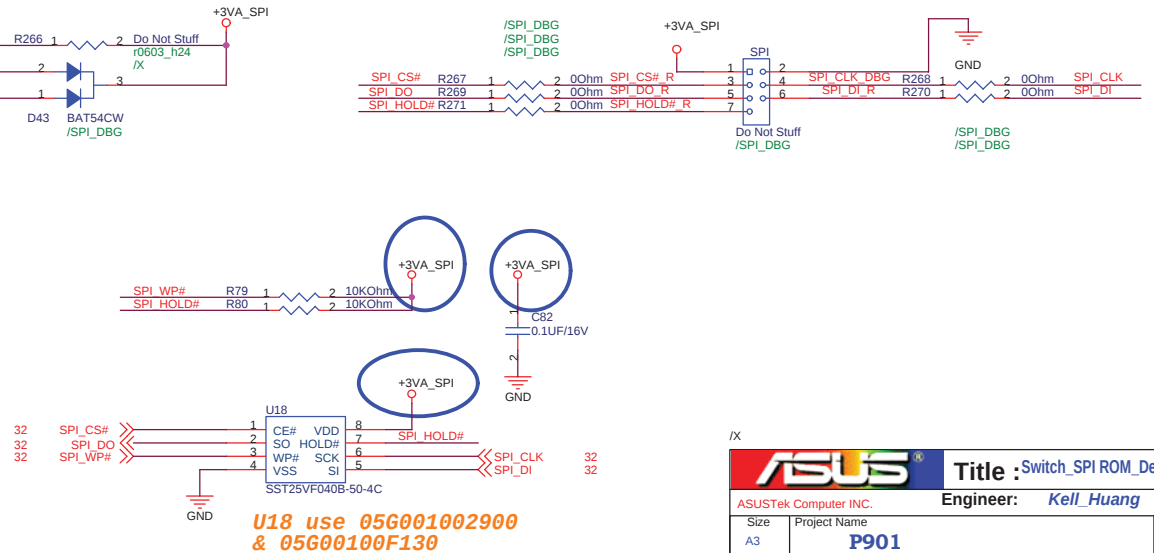
UART Control
IC for using
GPS module due
to no UART on
ENE EC

prevent system power on when LCD close

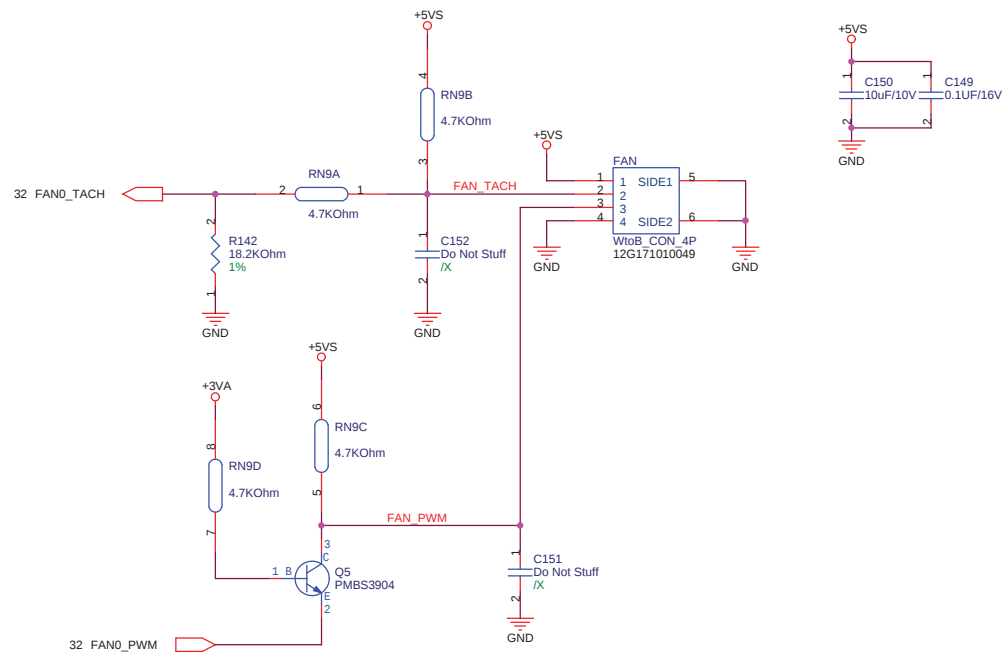
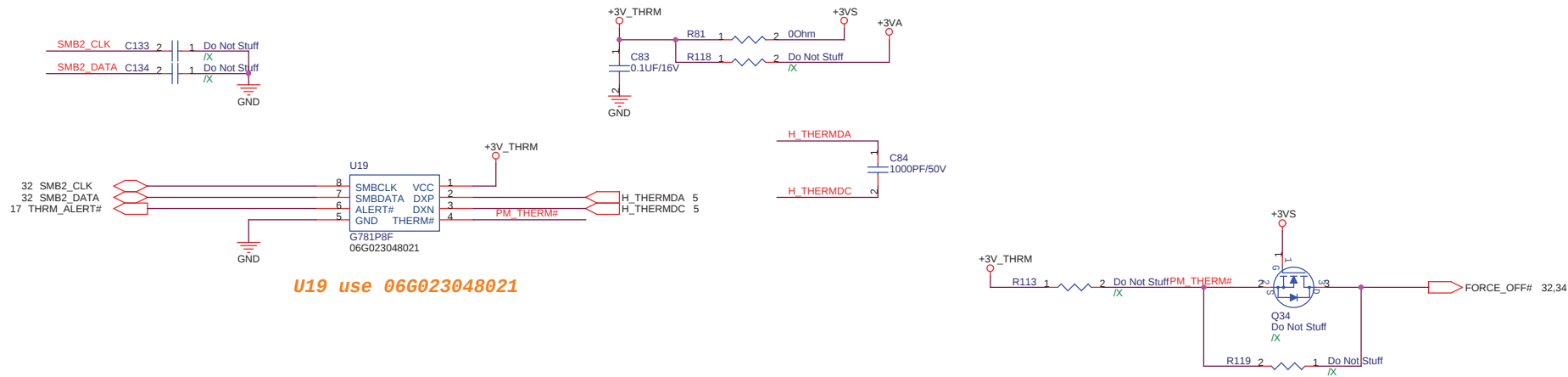
prevent system auto power on when CMOS clear



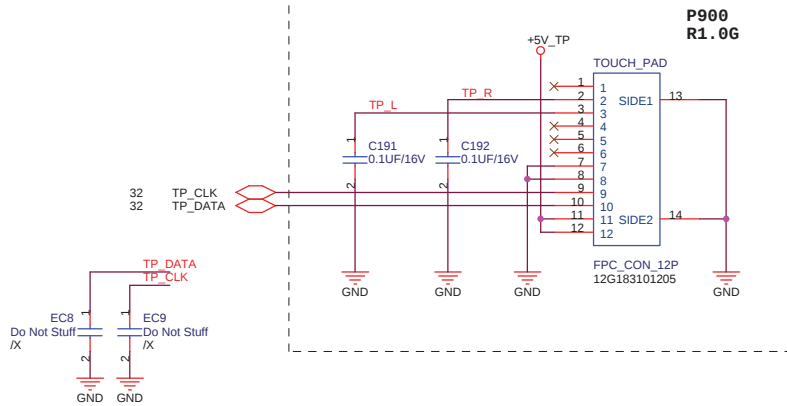
Debug Card cable use Z96 Touch Pad cable, P/N:
14G124110126, 14G124110120, 14G124110121
14G124110124, 14G124110125



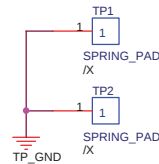
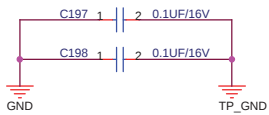
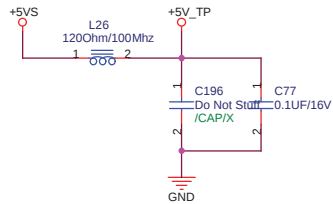
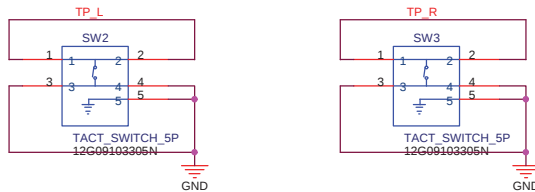
ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size	Project Name		
A3	P901		
Date: Monday, May 19, 2008	Sheet	34	of 47
		Rev	1.1G



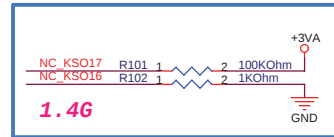
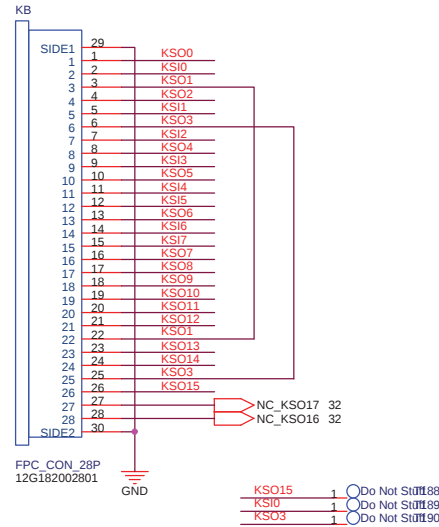
For Touch-Pad



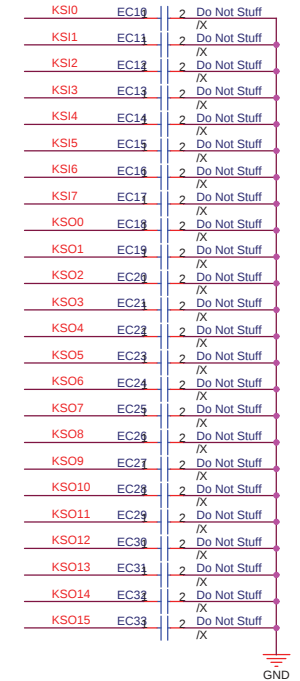
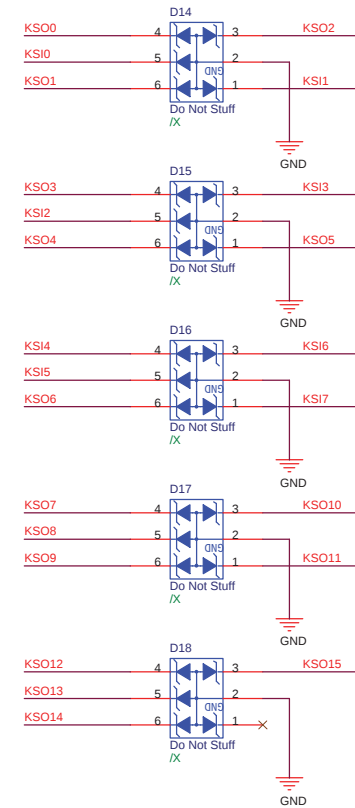
SW2, SW3 use 12G09103305N



For Keyboard Connector

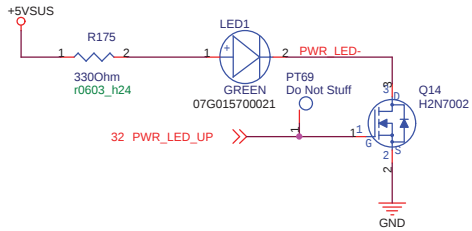


KSO[15:0] 32
KSI[7:0] 32

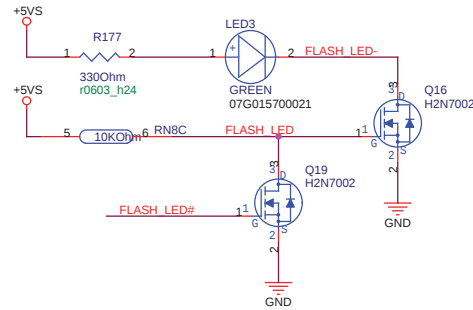


IX

for POWER LED

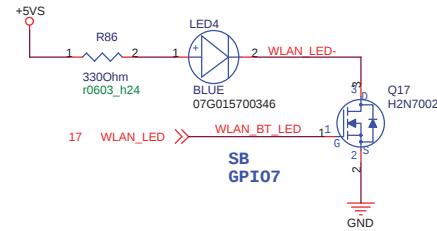


for FLASH LED

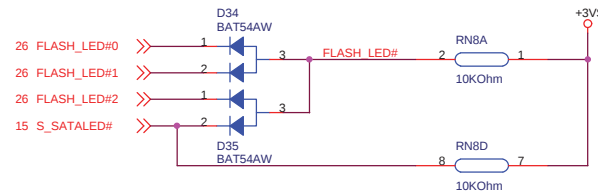
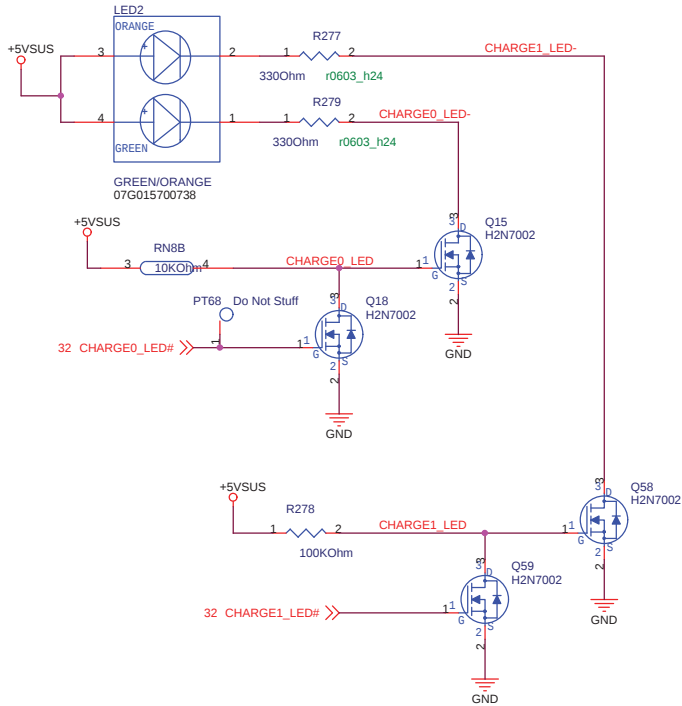


for WLAN/BlueTooth LED

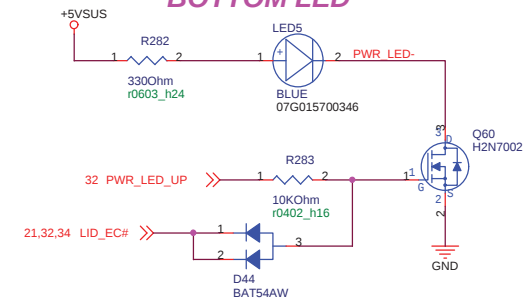
R86 use 4.7K 0Hm 10G213472003030

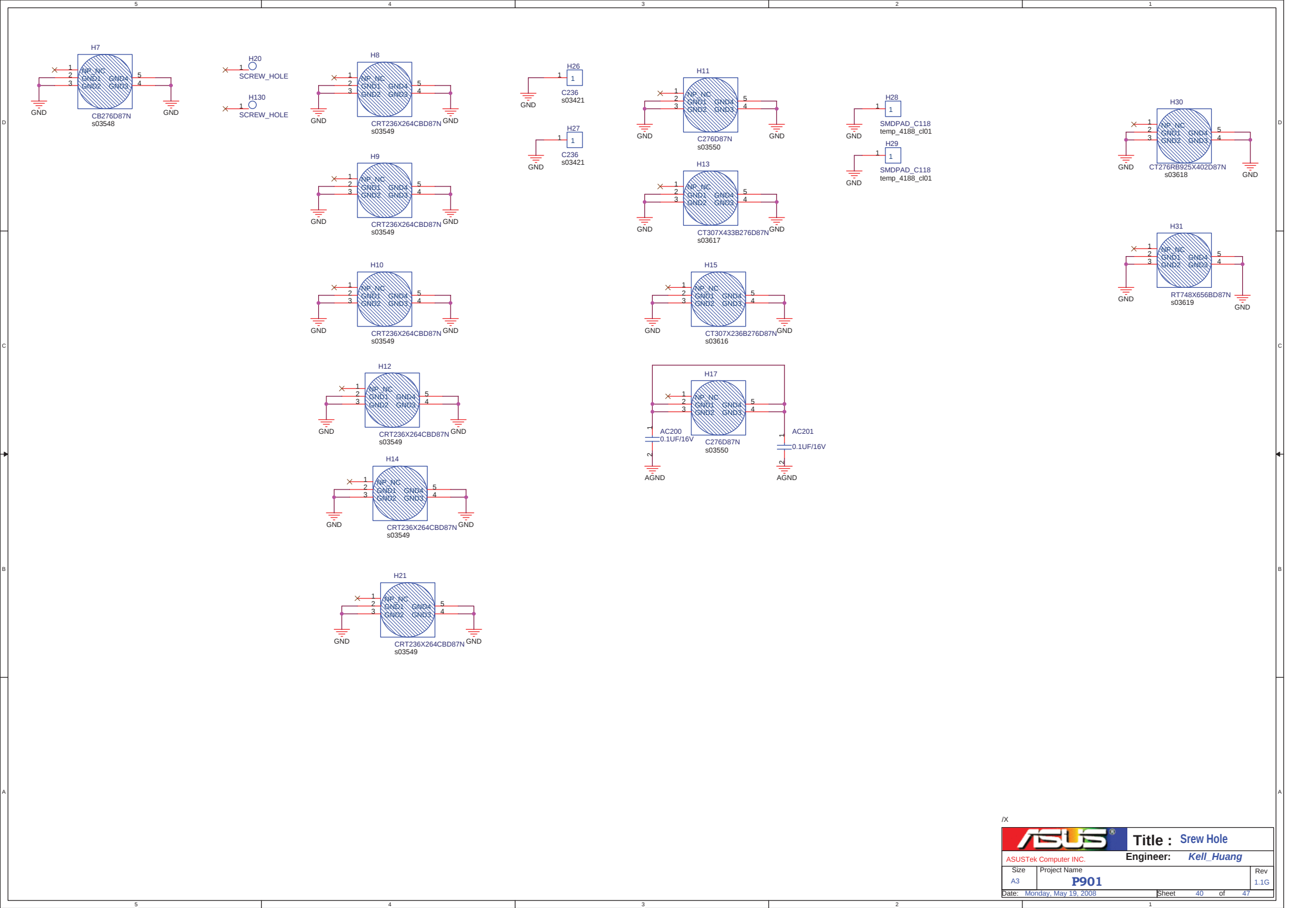


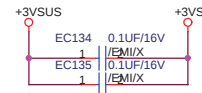
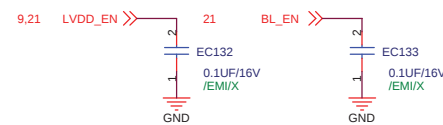
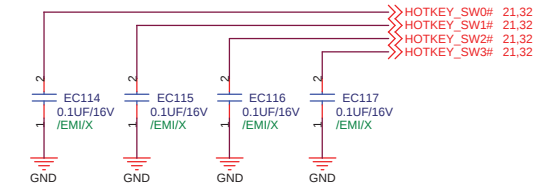
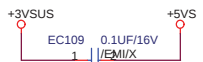
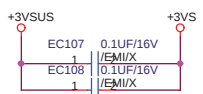
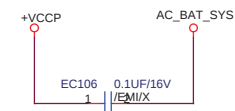
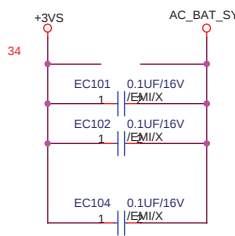
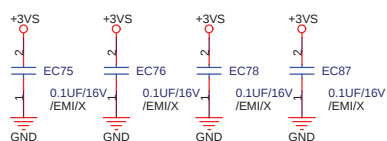
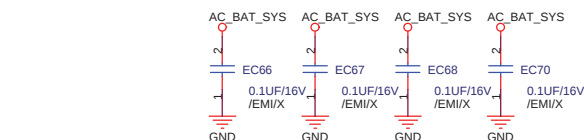
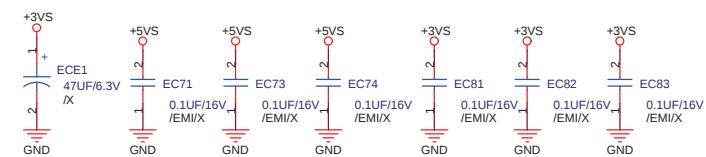
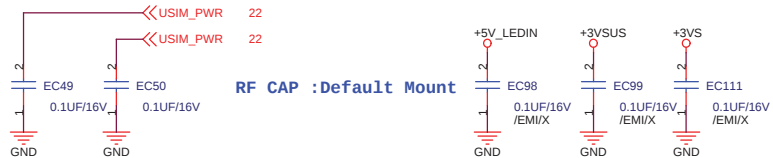
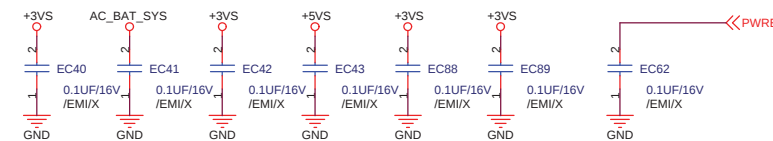
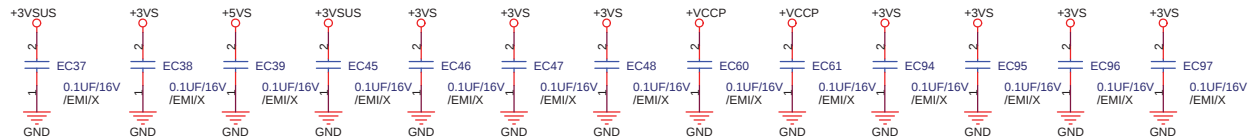
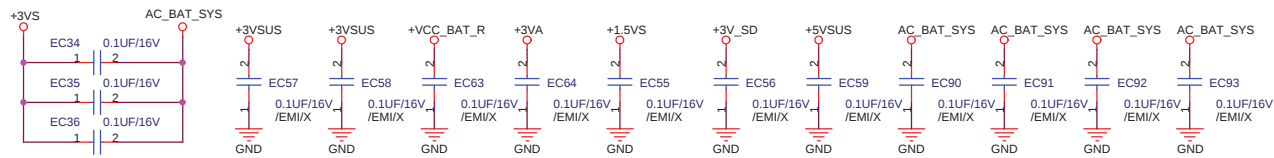
for CHARGE LED

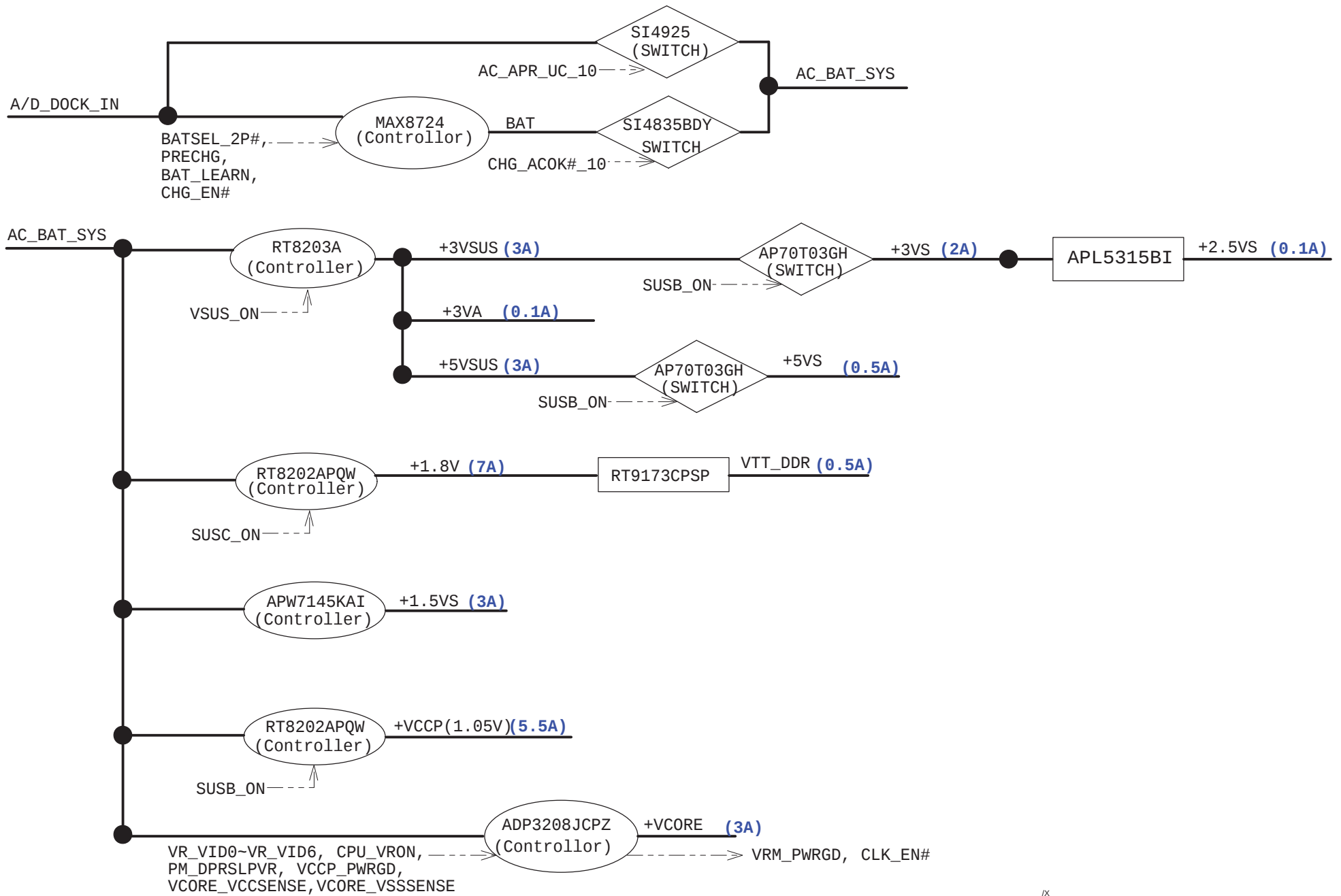


for POWER BOTTOM LED









5.15 PM_DPRSTP# >>>
 STP_CPU# = 0, CPU is in Deep Sleep Mode

8.17 PM_DPRSLPVR >>>
 PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled

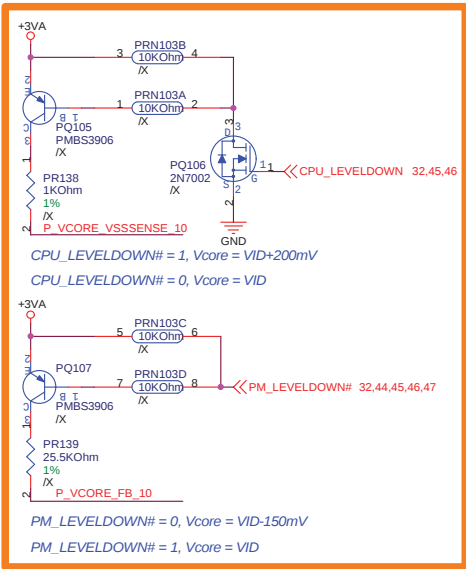
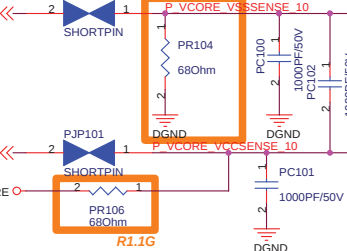
32 CPU_VRON >>>
 CPU_VRON = 1, Vcore Regulator Enabled

4.46 VCCP_PWRGD >>>
 VCCP_PWRGD = 1, Vcore Regulator Enabled

8.17.32 VRM_PWRGD <<<
 VRM_PWRGD = 1, Vcore Power OK

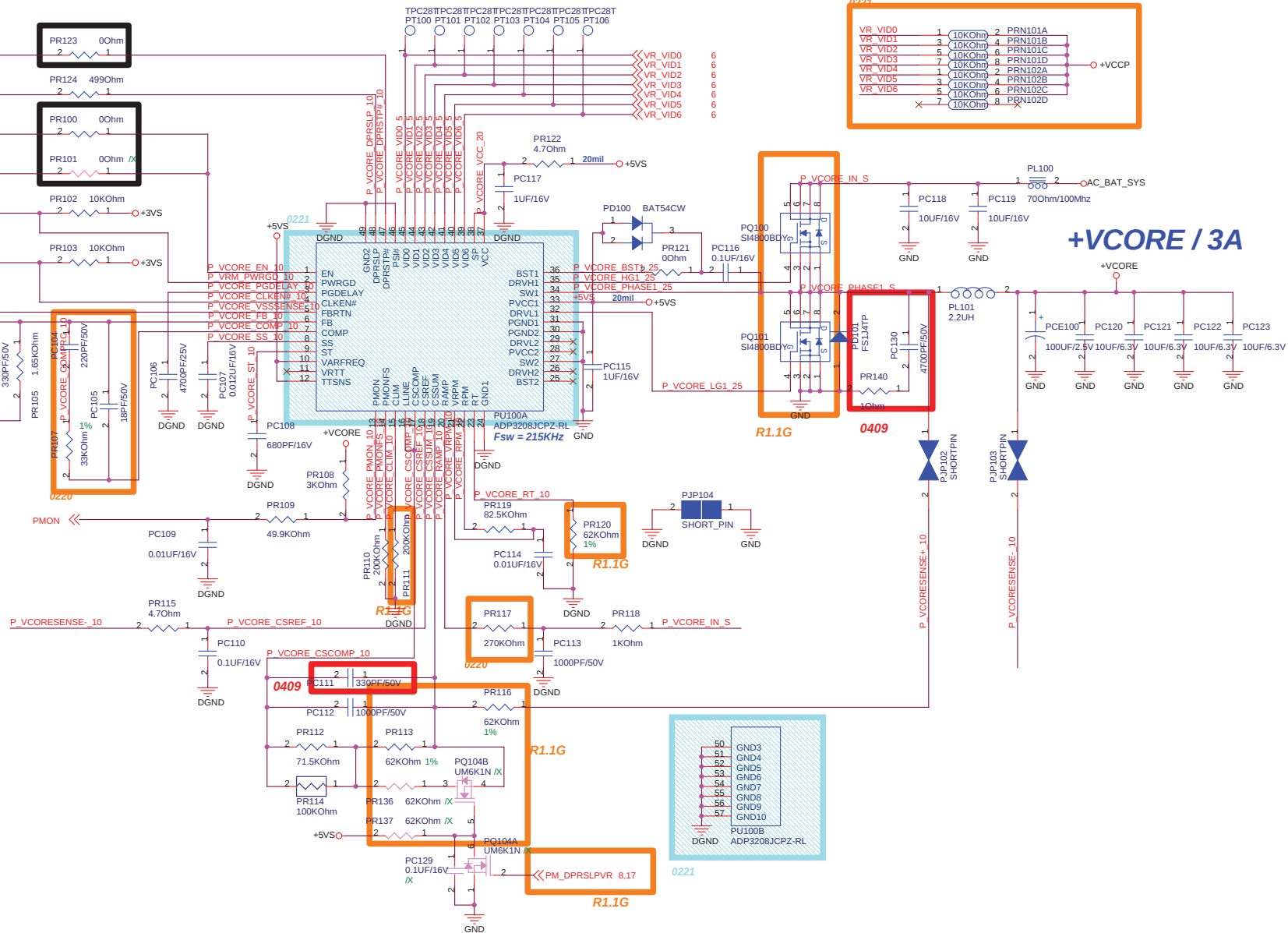
CLK_EN# <<<
 CLK_EN# = 0, Clock is enabled

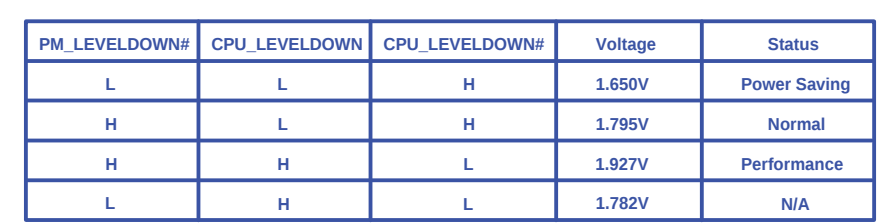
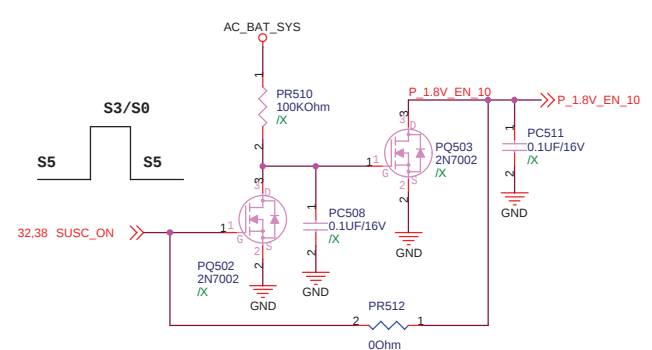
R1.1G

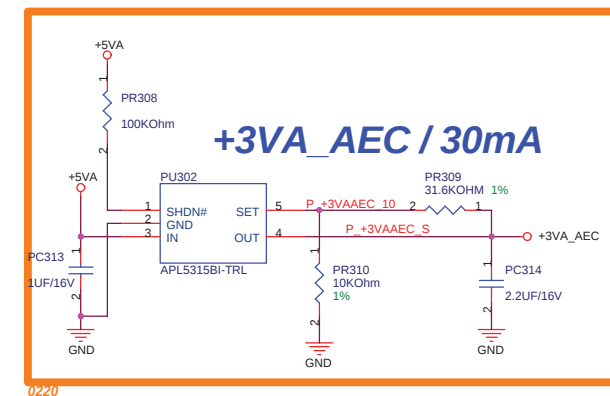
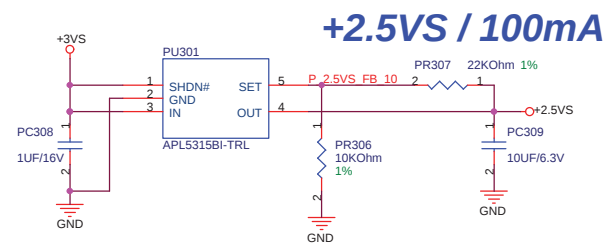
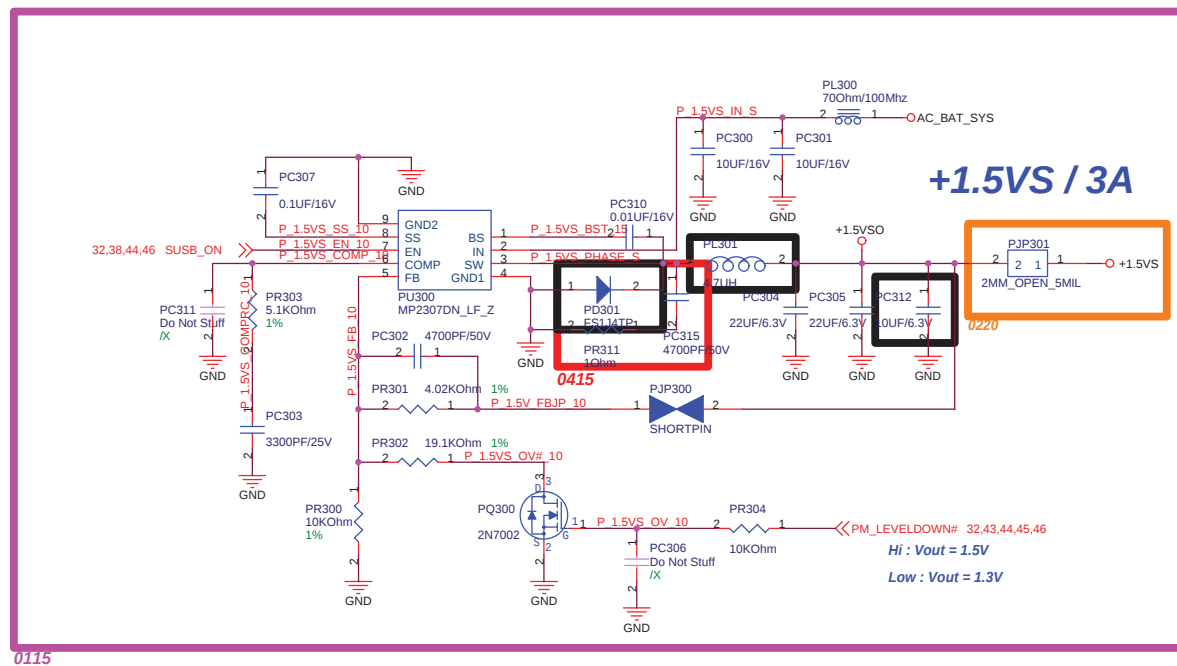


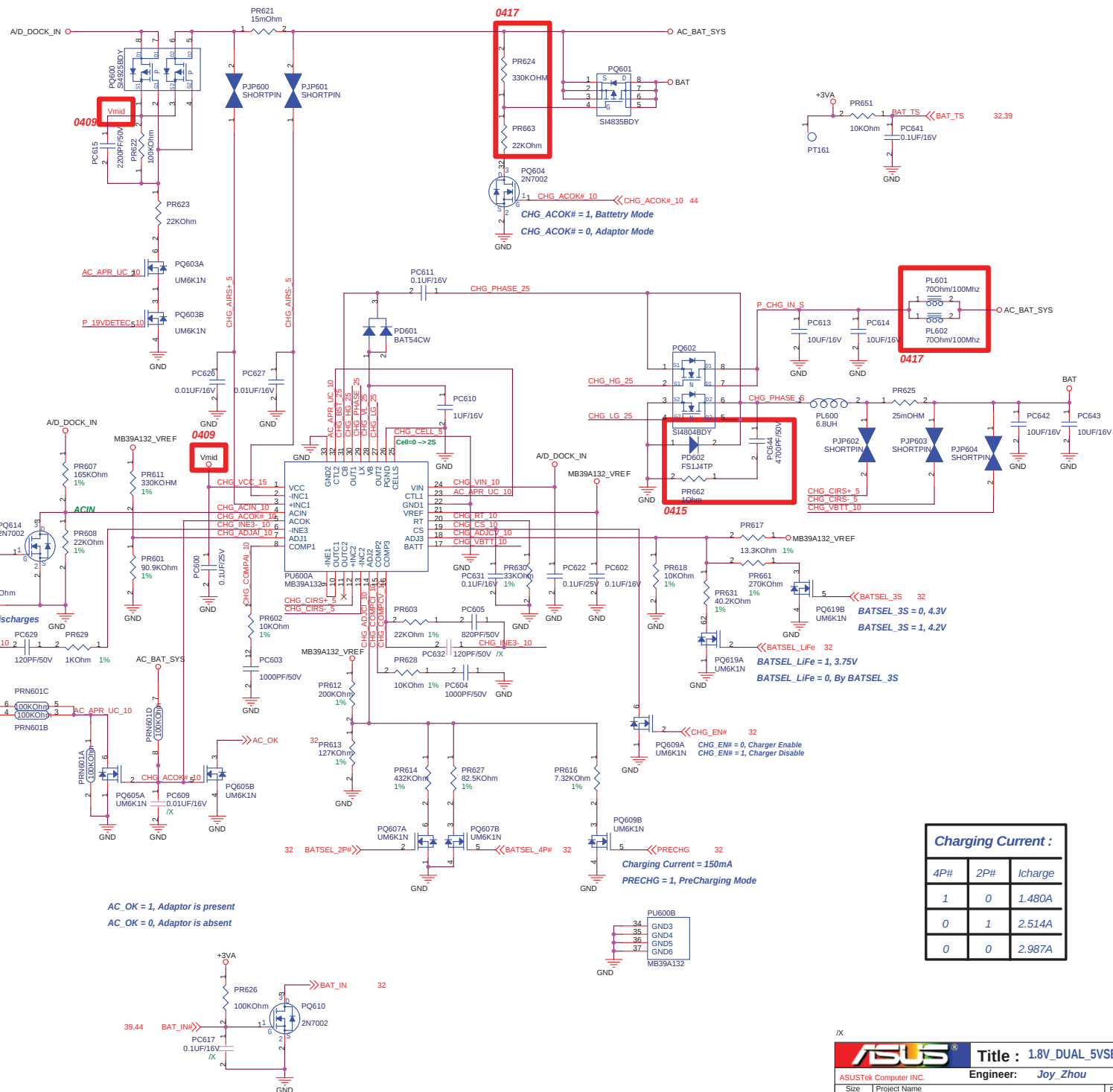
R1.1G

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A









VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)

VTH of -IN1: $5V / 62 * (100+62) = 13.06V$

VTH of ACIN: $1.25V / 25 * (185+25) = 10.5V$
Change PR607 and PR608 value

Prevent Input from 19V :

Adaptor > 13.06V, PQ603B Turn-off
Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :

BAT_ID = 1, 2 Cells; Vadj2 = 0.998V

$$\Rightarrow I_{\text{charge}} = 1.477 \text{ A}$$

BAT ID = 0, 4/6 Cells: Vadj2 = 1.648V

$$\Rightarrow I_{\text{charge}} = 2.517 \text{ A}$$

Pre-Charging Mode :

Precharging current = 150mA
 $V_{adj2} = 168.75\text{mV}$

Adaptor Max. Current :

PR600=235.8K; $I_{limit} = 2.170A$; 20.615W (9.5V/22W)

PR600=185.3K: Ilimit = 2.677A: 32.124W (12V/36W)

ACIN Threshold = 1.25V

Adaptor > 10.5V, System Powered by Adaptor

Adaptor < 10.5V, System Powered by Battery

Battery Charging Voltage :

Vadi3 > 4.1V ==> Vbat = 4.2V /cell

$$2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3}$$

Battery Charging Current :

$$4.4V > V_{adj2} \geq 0V \Rightarrow$$

Ichg =

Input Adaptor Max. Current Limit :

$$I_{limit_current} = (V_{adi1} - 0.075) / (25 * R_s)$$

Charging Current :

4P#	2P#	lcharge
1	0	1.480A
0	1	2.514A
0	0	2.987A

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMIH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SCI#	EXT_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	



Title : EC Pin Define

ASUSTek Computer INC.

Engineer: **Satan He**

Size
A3

Project Name
P901

Rev
1.1G

Date: Monday, May 19, 2008

Sheet 49 of 50