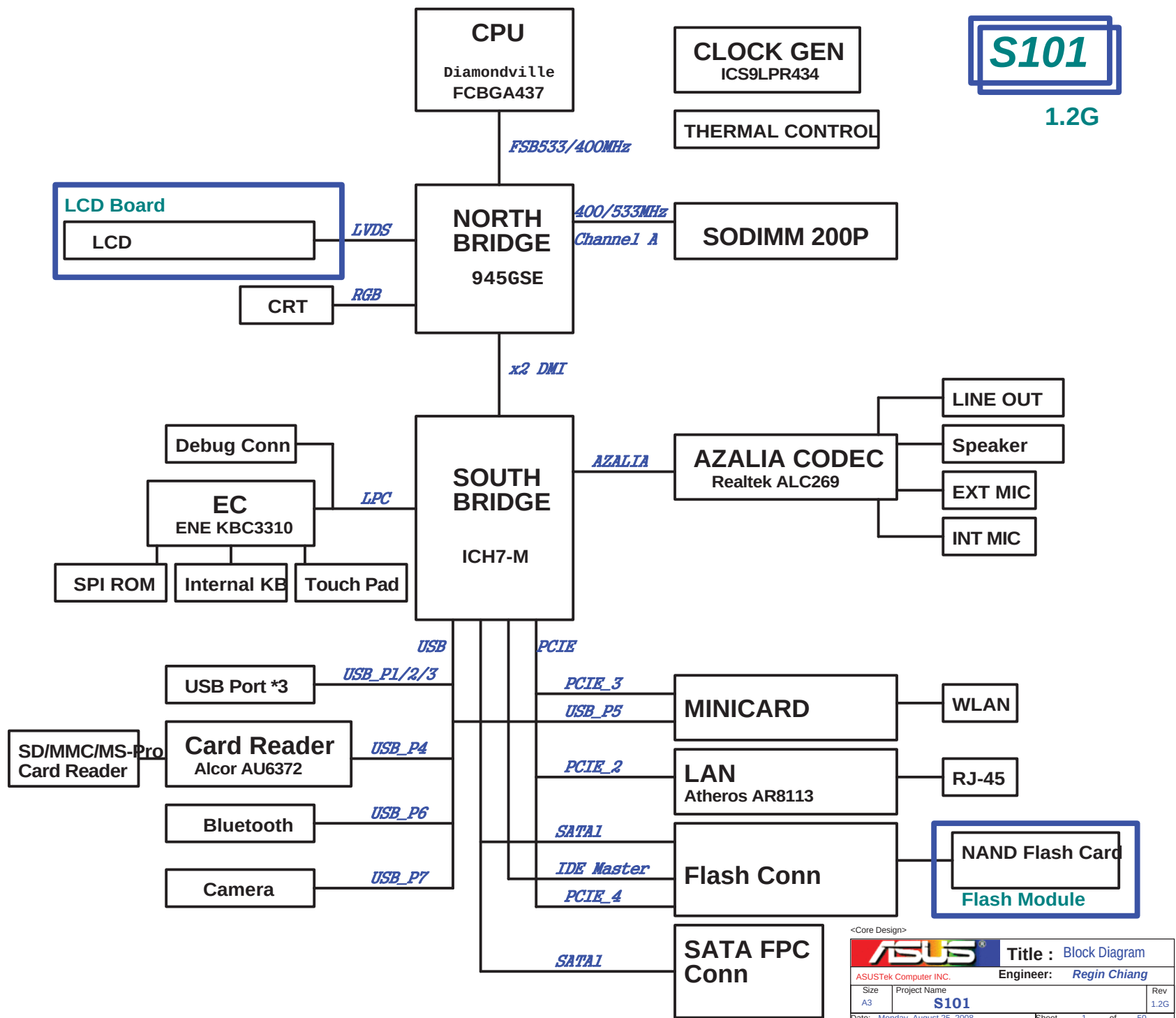


01_ Block Diagram
02_ System Setting
03_ Power Sequence
04_ Clock Gen_ICS9LPR434
05_ Diamondville_BUS
06_ Diamondville_PWR
07_NB-945GMS(HOST)
08_NB-945GMS(DMI)
09_NB-945GMS(GRAPHIC)
10_NB-945GMS(DDR2)
11_NB-945GMS(PWR)
12_NB-945GMS(PWR2)
13_NB-945GMS(GND)
14_SB-ICH7M(PWR)
15_SB-ICH7M(1)
16_SB-ICH7M(2)
17_SB-ICH7M(3)
18_DDR2 SODIMM
19_DDR2_Termination
20_Onboard VGA
21_LCD Conn_LID
22_Blank
23_Mini WIFI+ BT
24_LAN_Atheros AR8113
25_RJ45
26_Flash Conn
27_USB Port
28_Camera Conn
29_Card Reader_AU6372A51
30_Codec_ALC269
31_Audio_AMP_Jack
32_EC_ENE KB3310
33_EC
34_Switch_SPI ROM_Debug Conn
35_Thermal Sensor_FAN
36_KB_Touch Pad
37_LED_THERMTRIP
38_Discharge
39_PWR Jack
40_Srew Hole
41_EMI
42_POWER FLOW
43_Vcore
44_Power System
45_Power_+1.8V & VTTDDR
46_Power_VCCP
47_Power_+1.5VS & +2.5VS
48_Power_Charger
49_EC Pin Define
49_History



EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera

PCIE

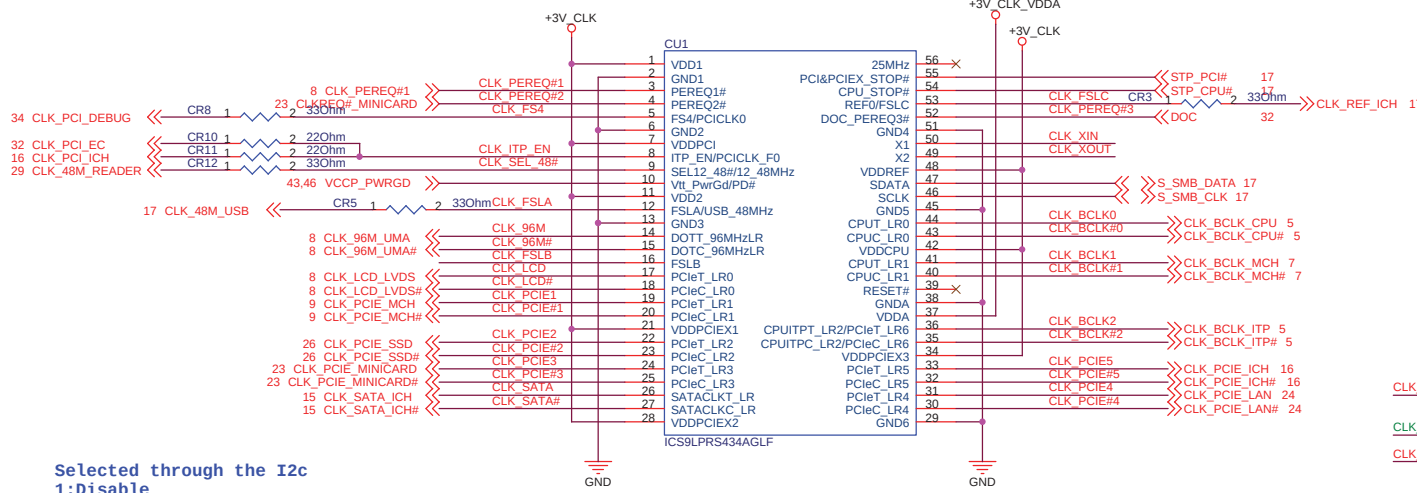
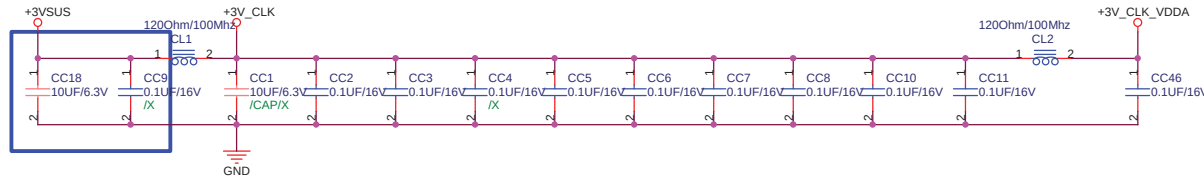
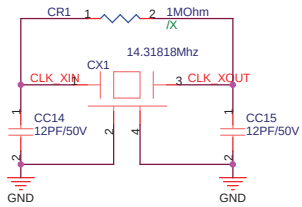
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

<Core Design>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Satan_He	
Size	Project Name		Rev
A3	S101		1.2G
Date: Monday, August 25, 2008		Sheet	2 of 50

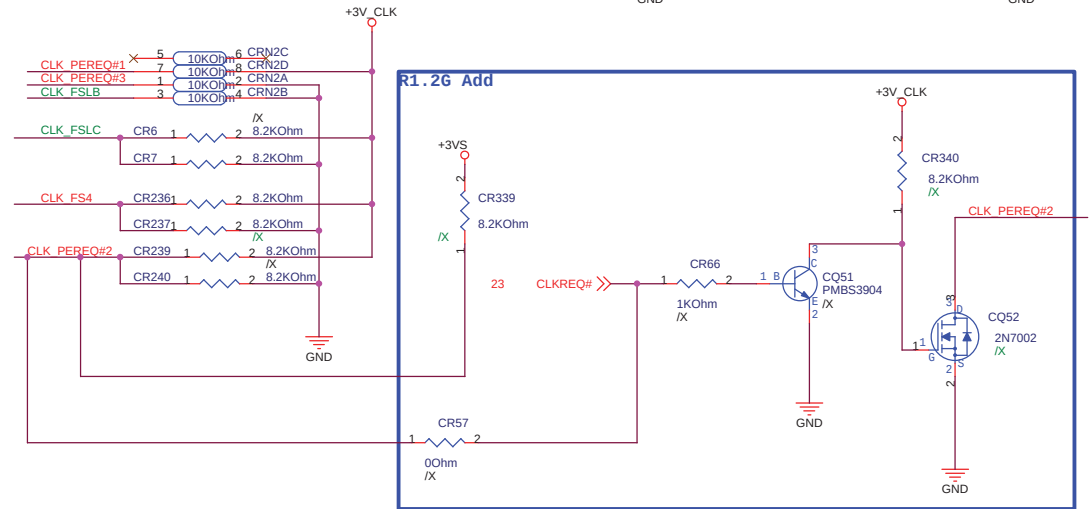
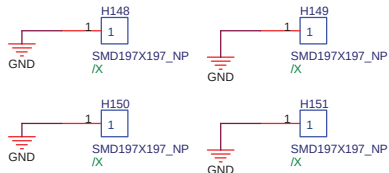


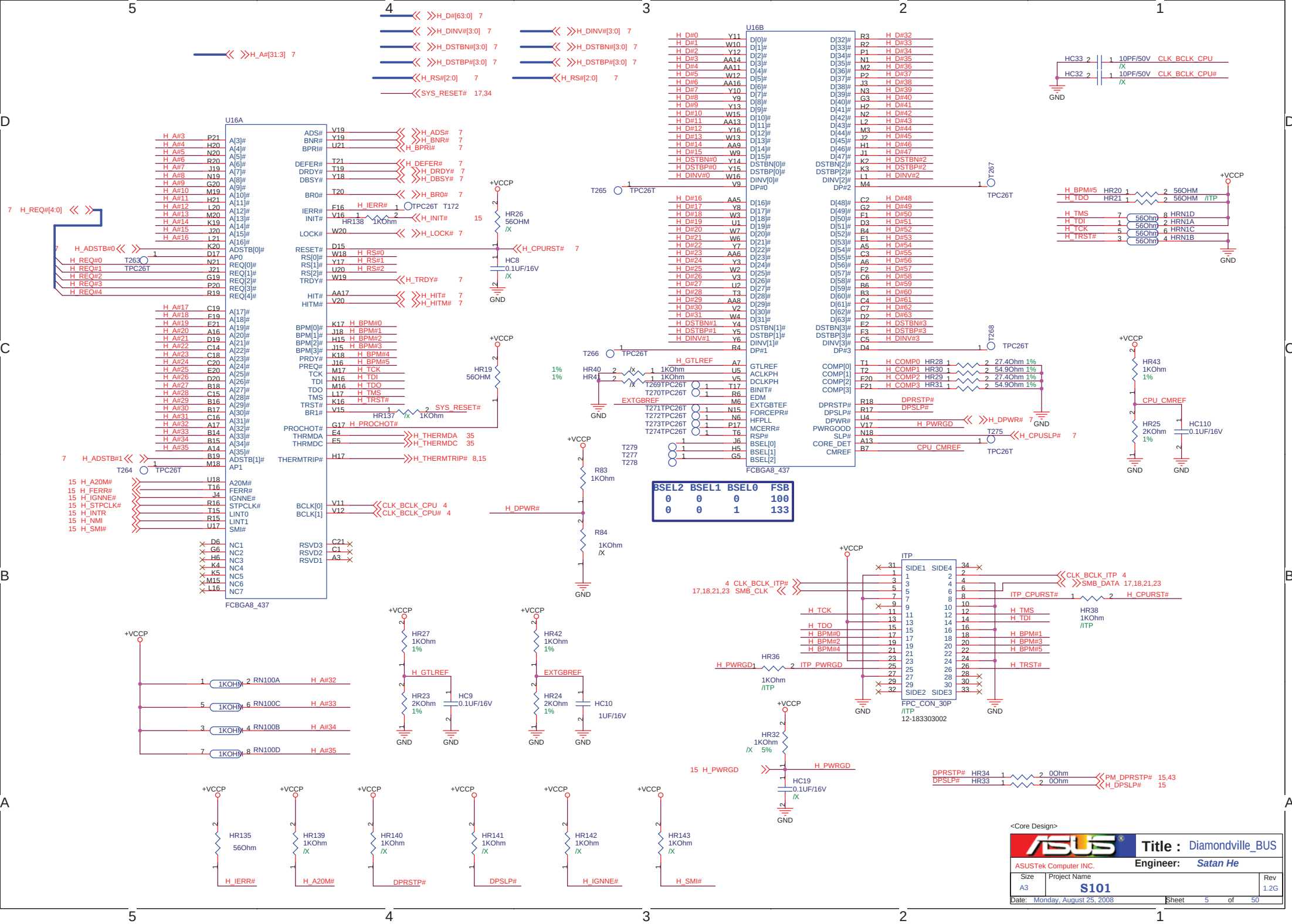
Selected through the I2c
1:Disable
0:Enable

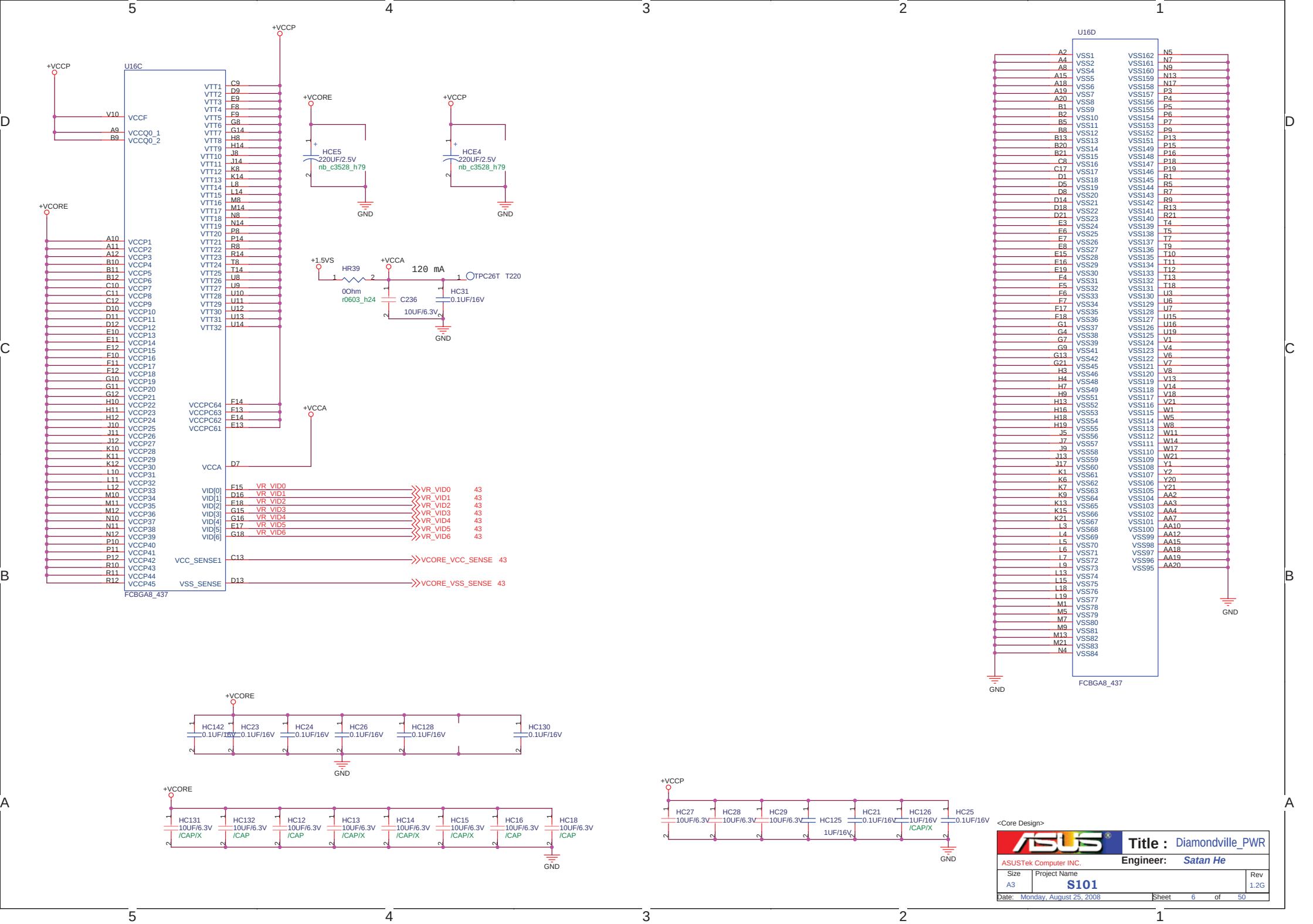
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100

H148-H151 reserve to place GASKET for EMI



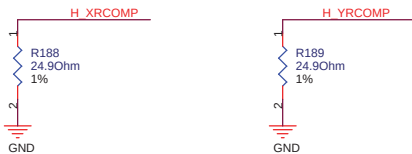




**Power :
+VCCP**

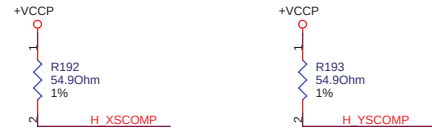
RCOMP

For Calibrating the FSB I/O Buffer



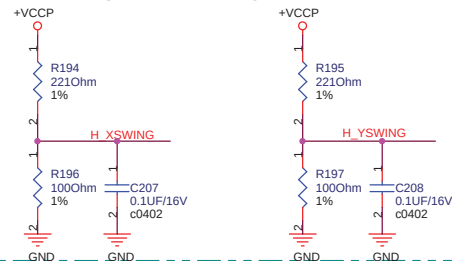
SCOMP

For Slew Rate Compensation on the FSB

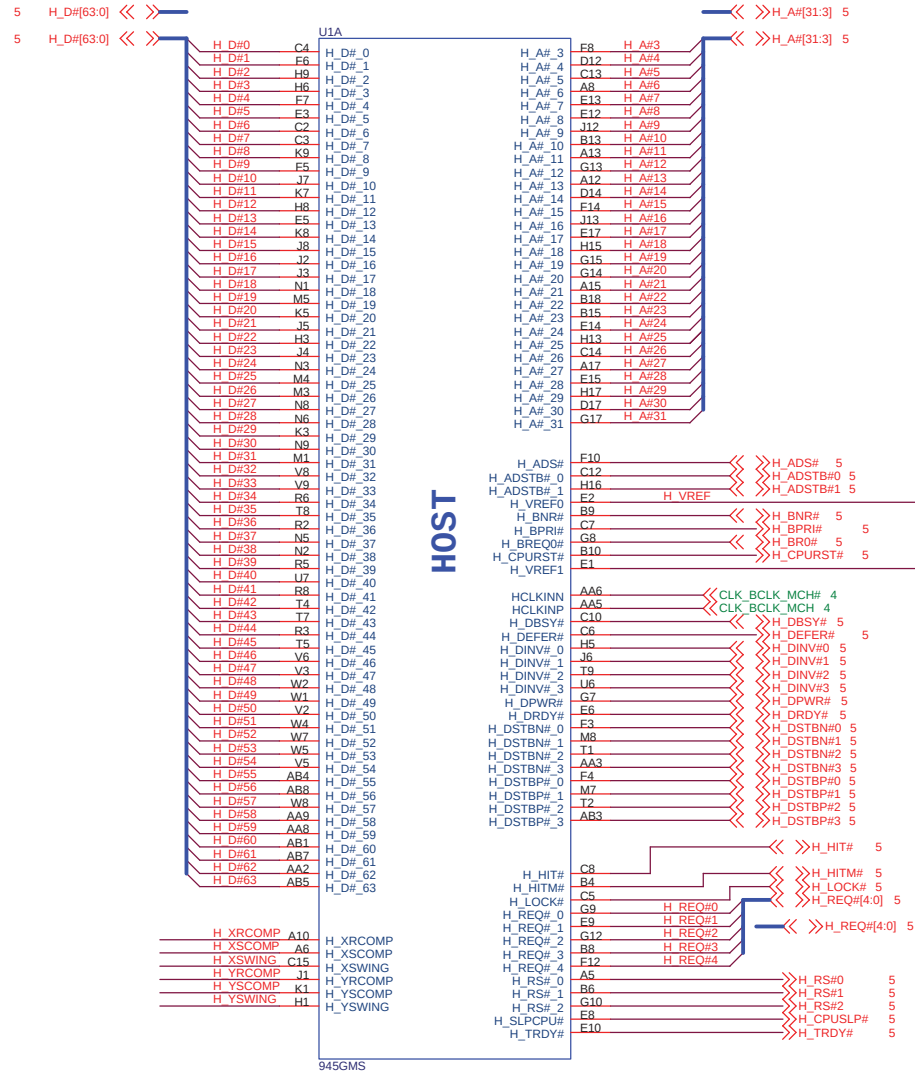


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



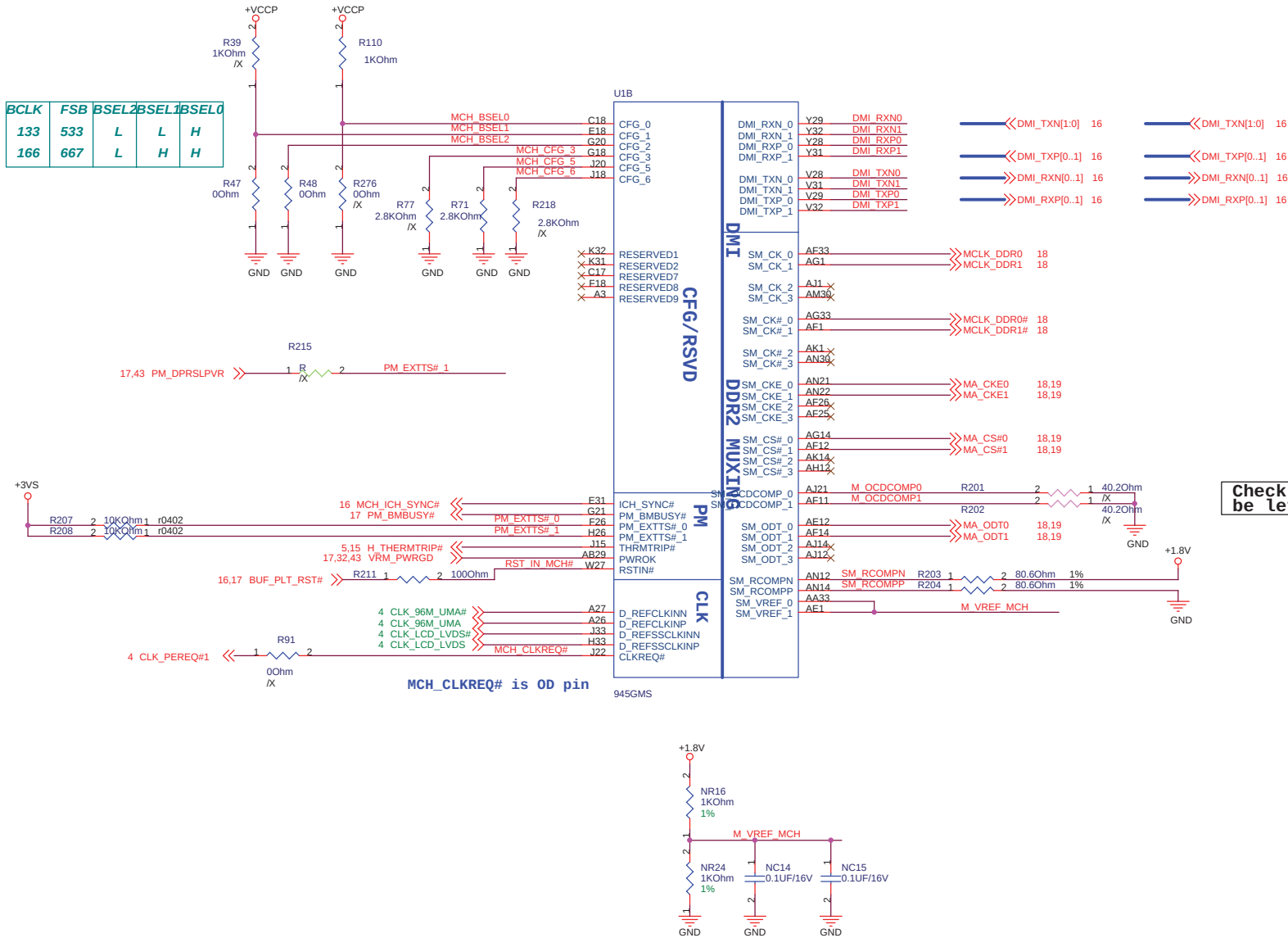
Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



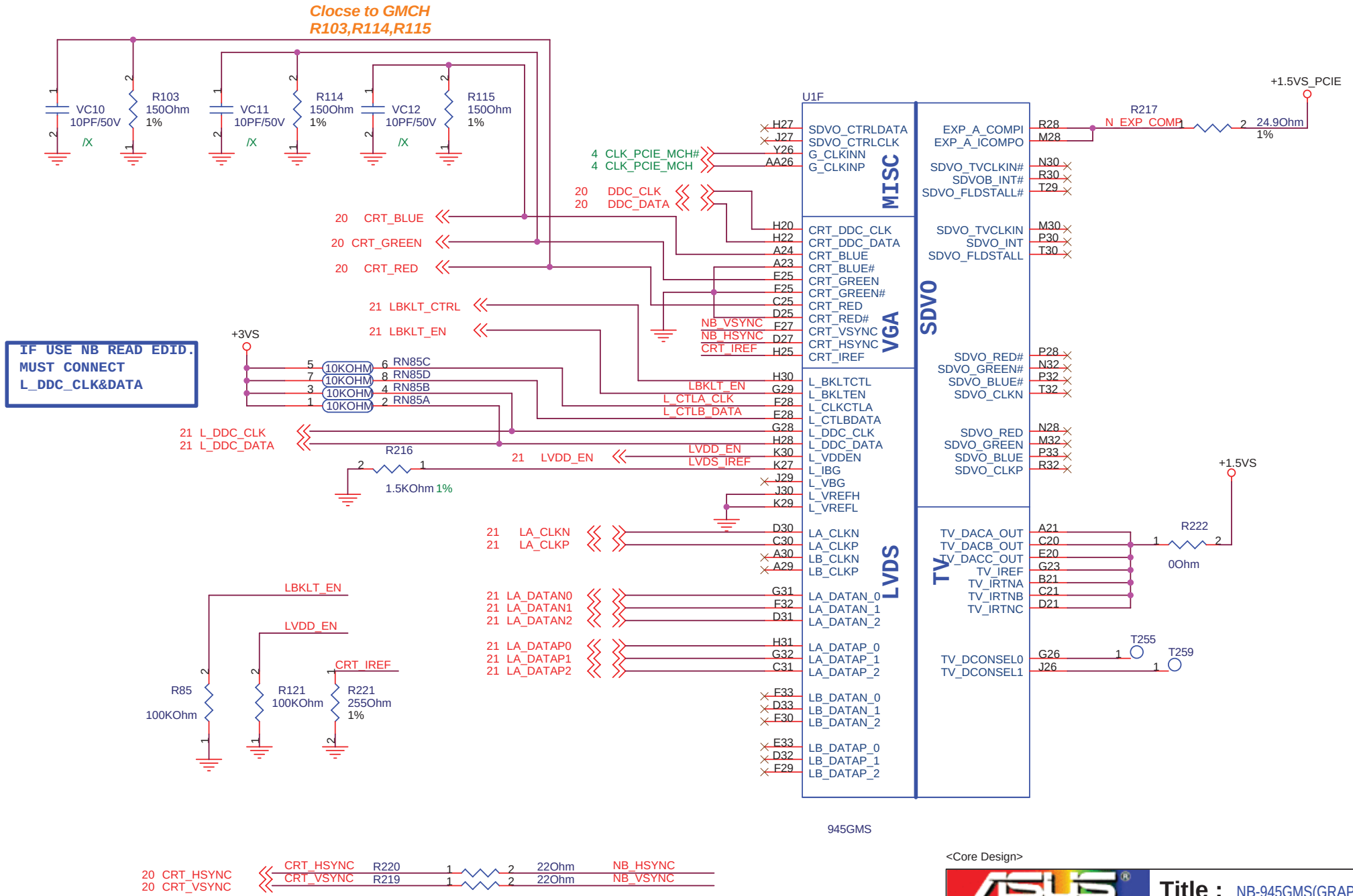
<Core Design>

ASUS		Title : NB-945GMS(HOST)	
ASUSTek COMPUTER INC.		Engineer: Satan He	
Size A3	Project Name S101	Rev 1.2G	
Date: Monday, August 25, 2008	Sheet 7 of 50		

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

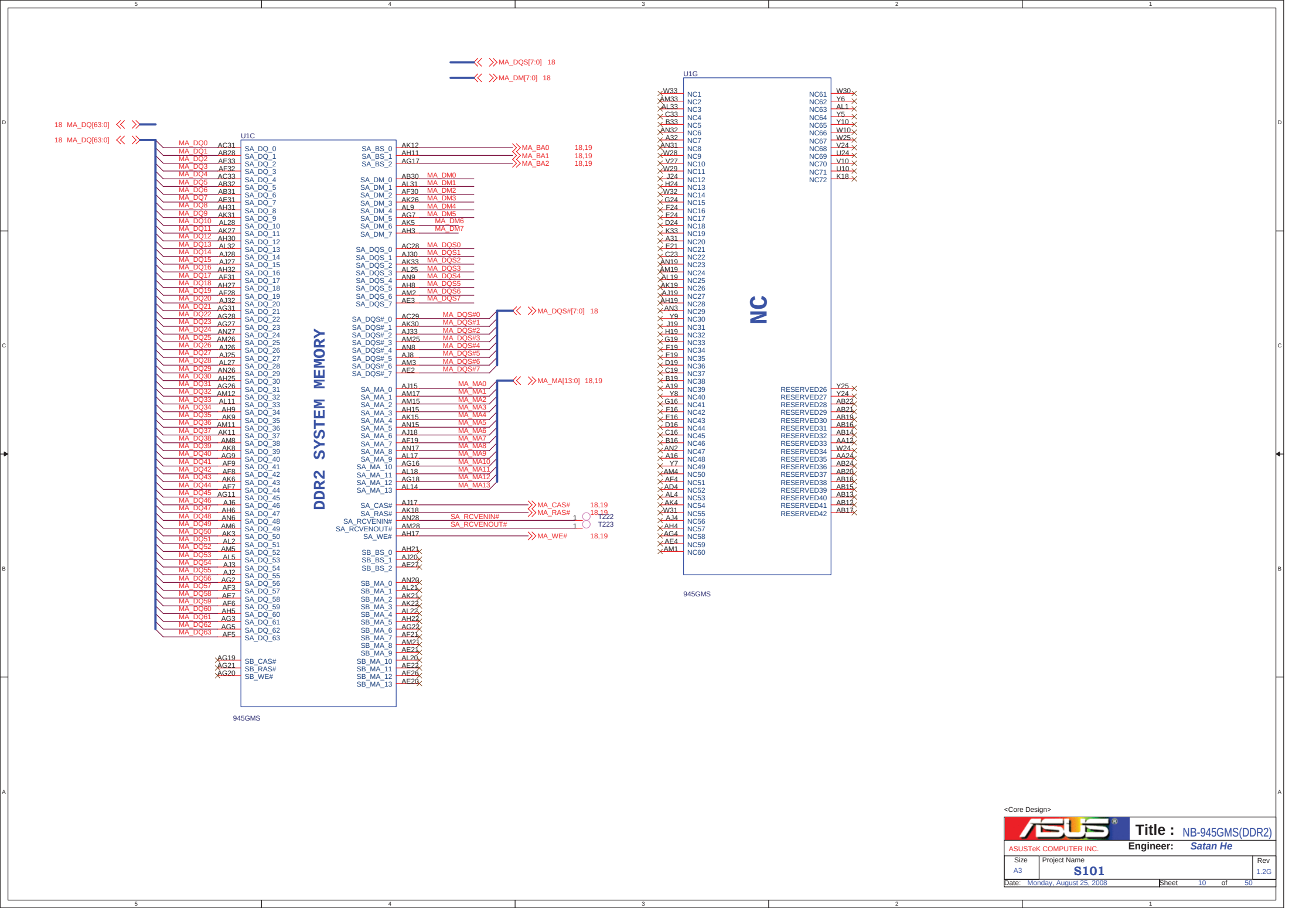


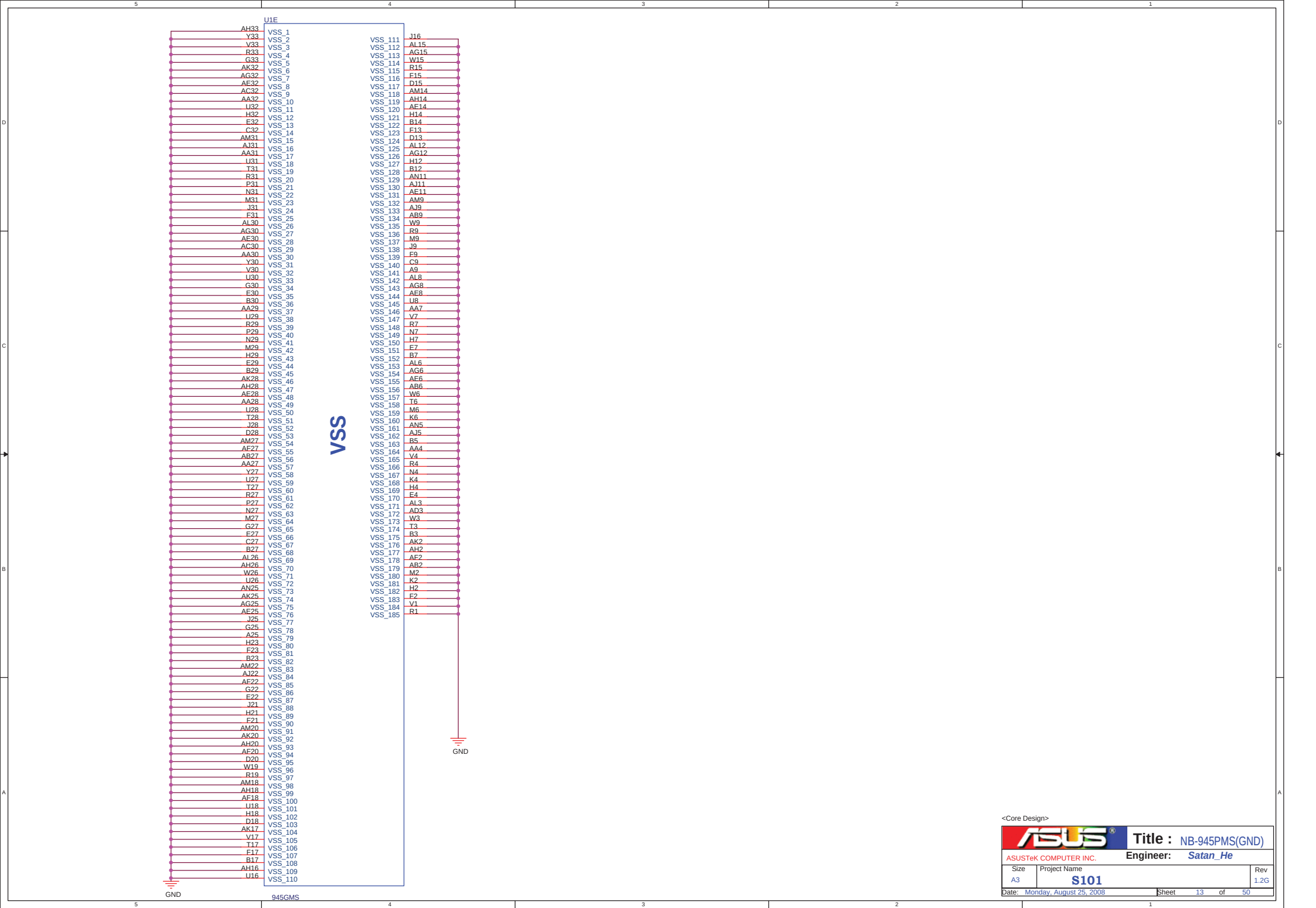
CheckList notes :Can be left as NC



<Core Design>

ASUS		Title : NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		Engineer: Satan_He	
Size A4	Project Name S101		Rev 1.2G
Date: Monday, August 25, 2008	Sheet	9 of 50	





Vcc1_5_A=0.64A

1.1G change to +3VS to follow CRB
VccSus3_3 only for desktop

0.27A

45mA

<Core Design>



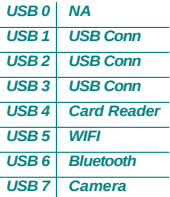
Title : SB-ICH7M(PWR)

ASUSTek COMPUTER INC. Engineer: Satan He

Size Project Name Rev
Custom S101 1.2G

Date: Monday, August 25, 2008 Sheet 14 of 50





<Core Design>



ASUSTeK COMPUTER INC.

Engineer: *Satan He*

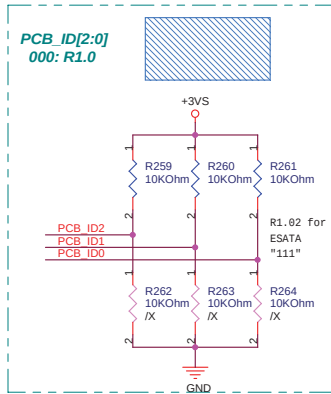
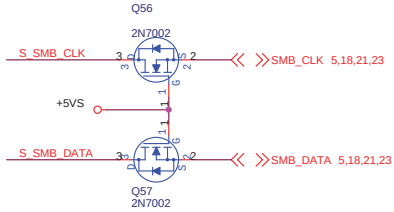
Size Custom	Project Name S101	Rev 1.2G
Date: <u>Monday, August 25, 2008</u>		Sheet <u>16</u> of <u>50</u>

Isolate alert# signal from thermal IC

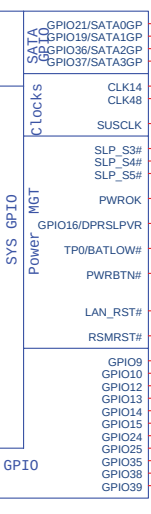
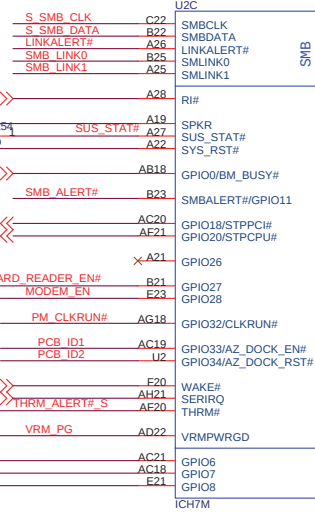


05/12/30, refer Z96J R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.

S SMB_CLK >>> S_SMB_CLK 4
S SMB_DATA >>> S_SMB_DATA 4

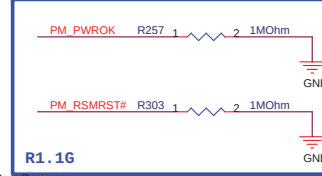
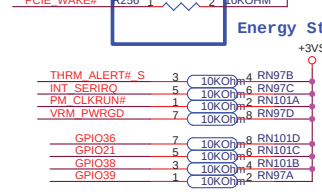
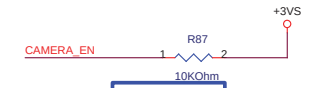
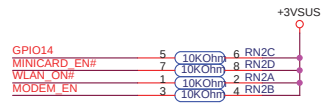
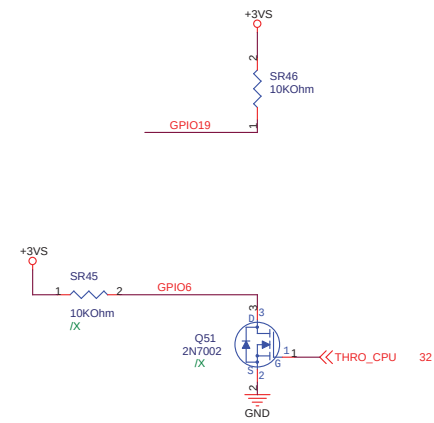
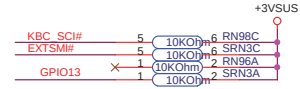
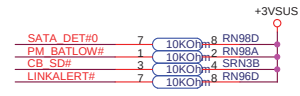
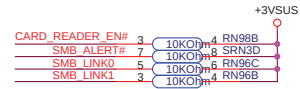
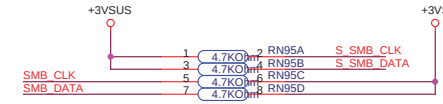
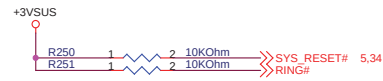


PCB_VID3 : PROJECT CODE



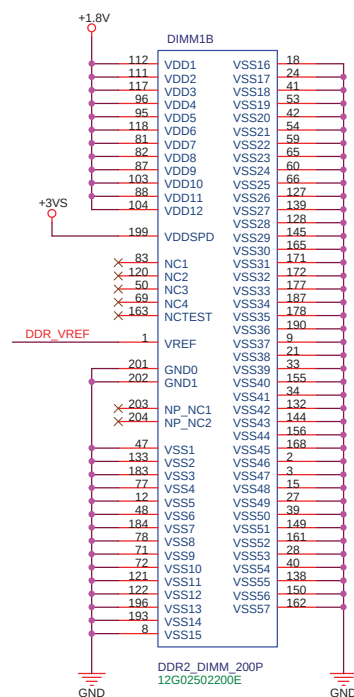
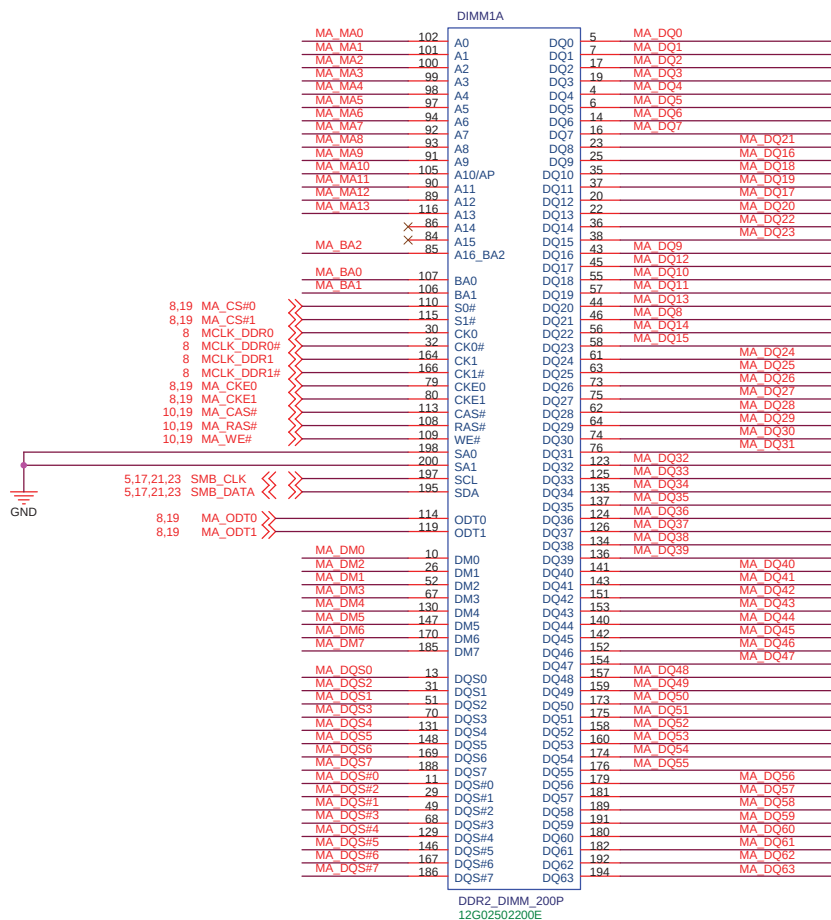
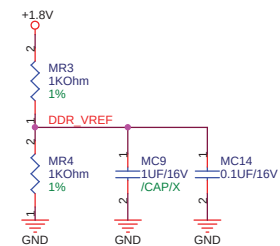
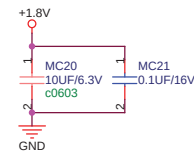
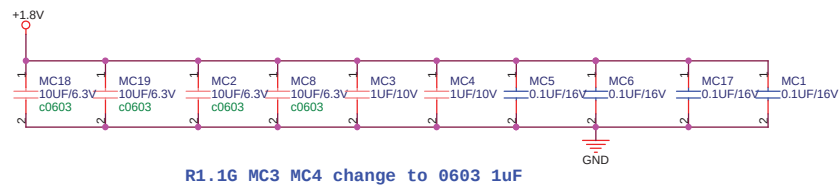
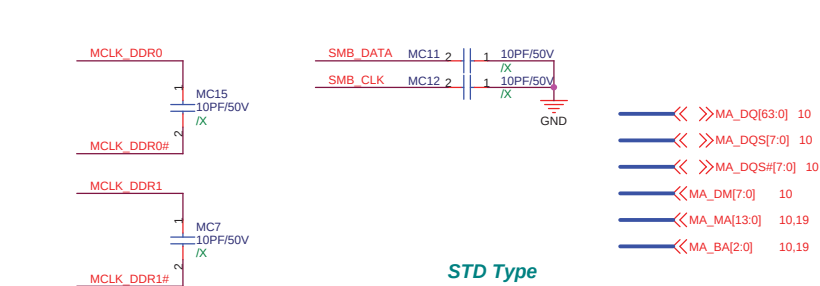
GPIO25 Internal PU 20K For +1.5V DIMM Power

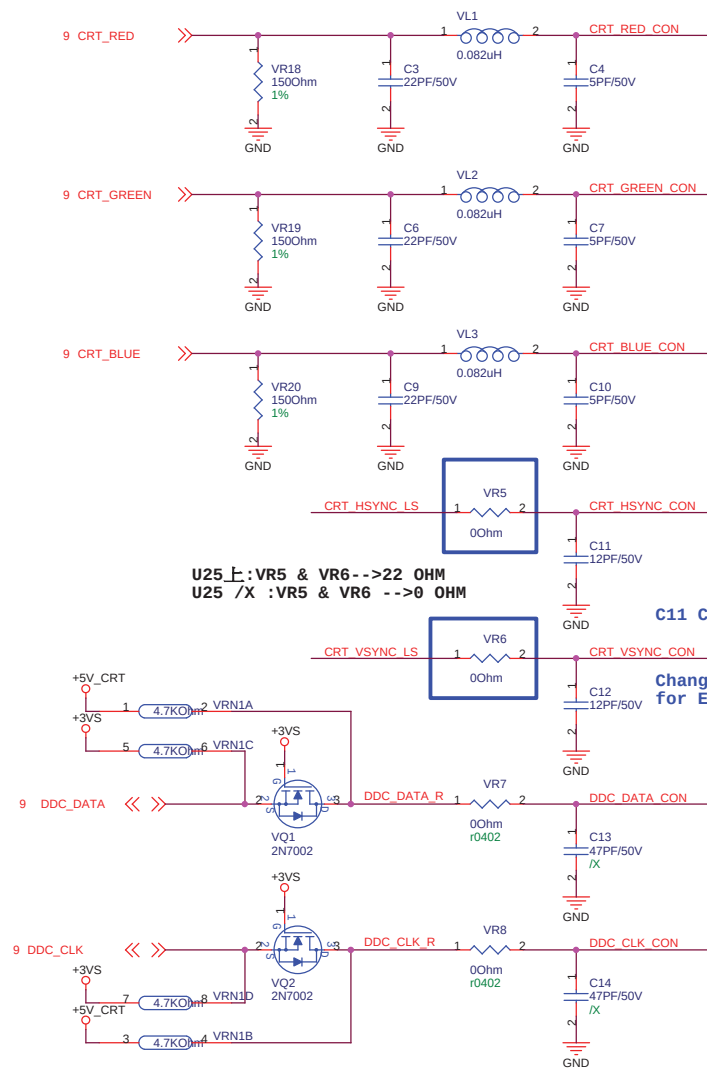
WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x



<Core Design>

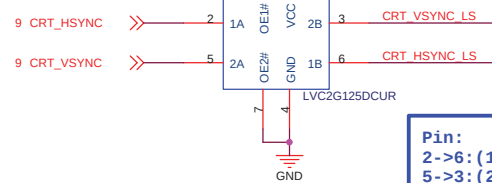
ASUS		Title : SB-ICH7M(3)	
ASUSTek COMPUTER INC		Engineer: Satan He	
Size	Project Name	Rev	
Custom	S101	1.2G	
Date: Monday, August 25, 2008	Sheet	17	of 50



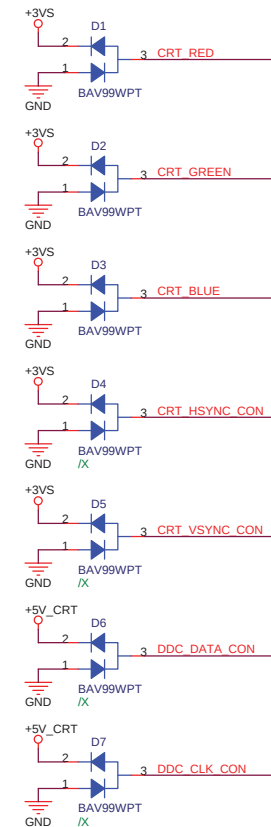
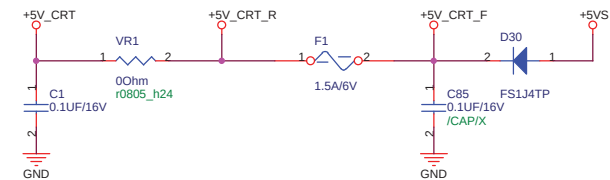


C11 C12 for EA measurement

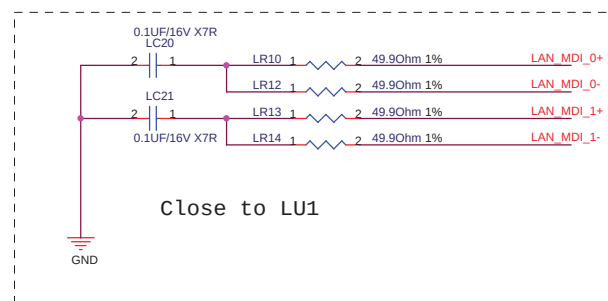
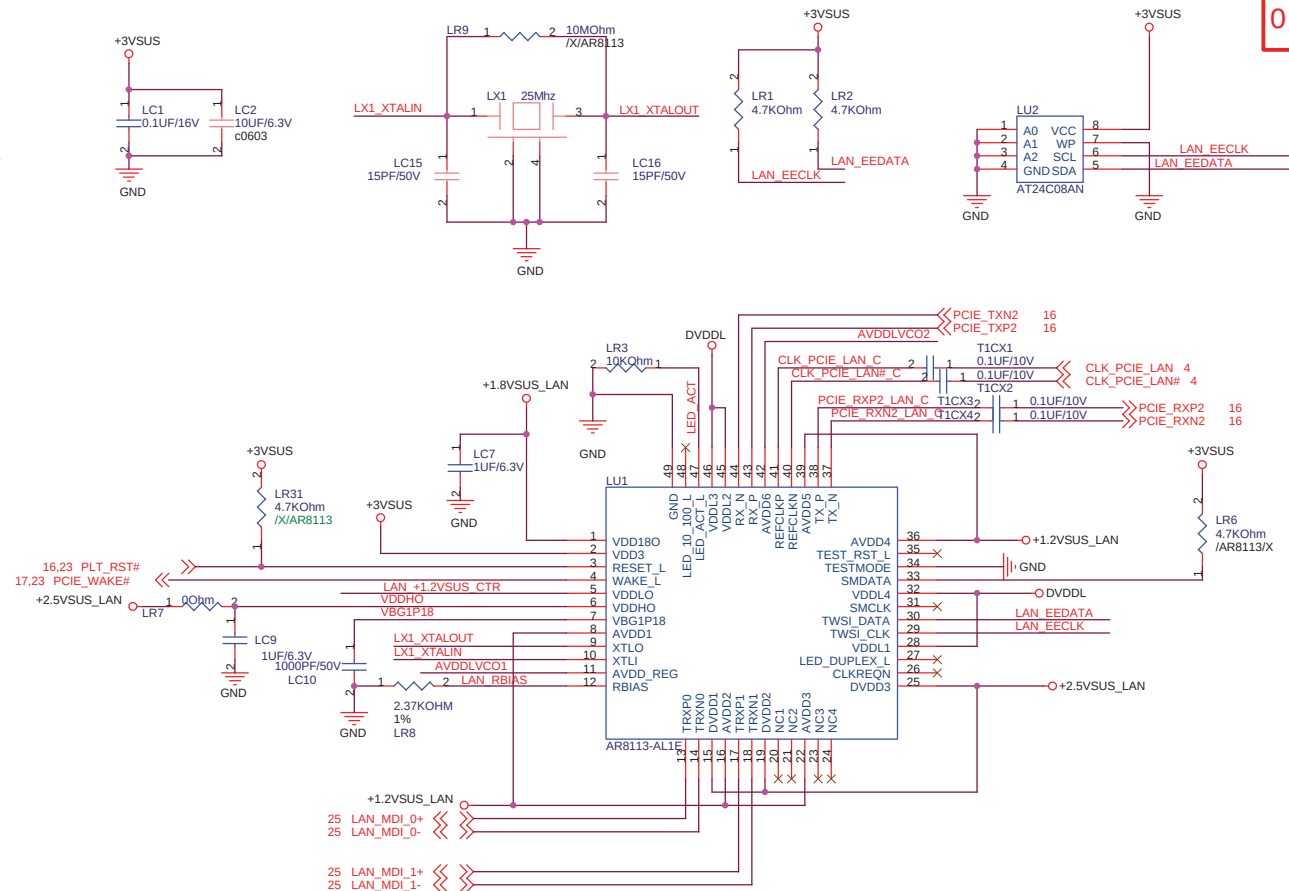
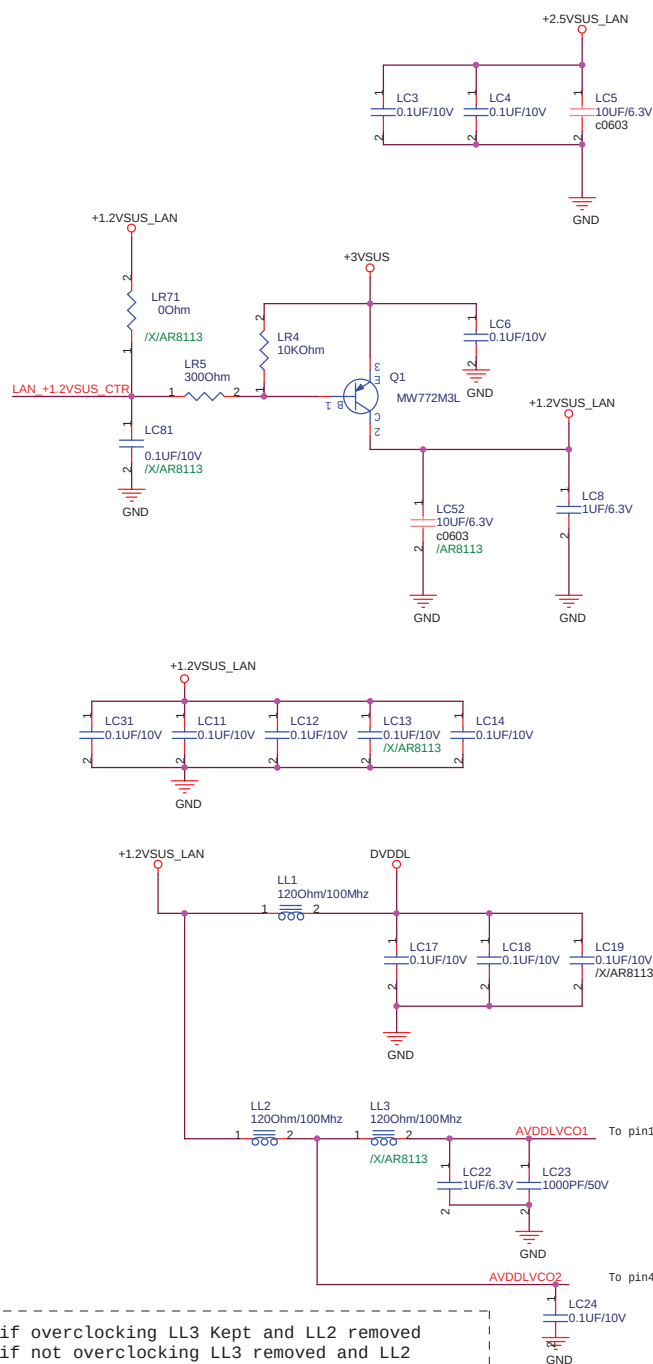
Change VR5 and VR6 to 0 ohm for EA measurement result



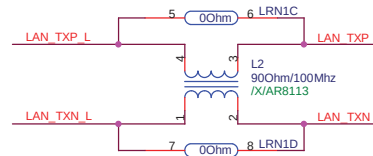
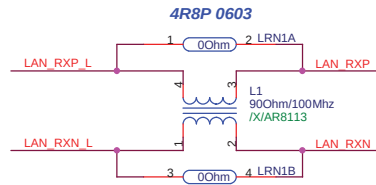
Pin:
2->6: (1A->1B)
5->3: (2A->2B)



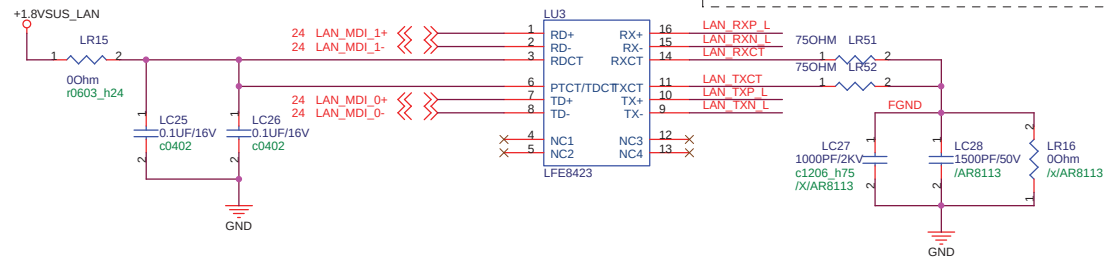
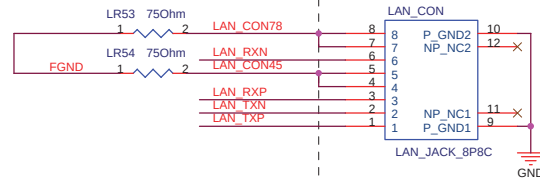




```
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2
Kept
```

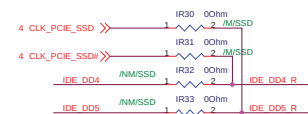


**LAN connector: 126148101086
SMT type**

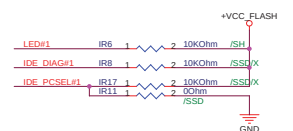
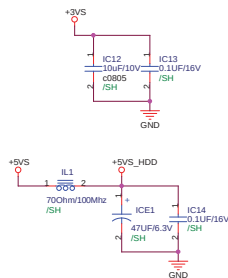


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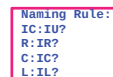
ASUS		Title : RJ45	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		Rev
A3	S101		1.2G
Date: Monday, August 25, 2008		Sheet	25 of 50



/SH for SATA HDD

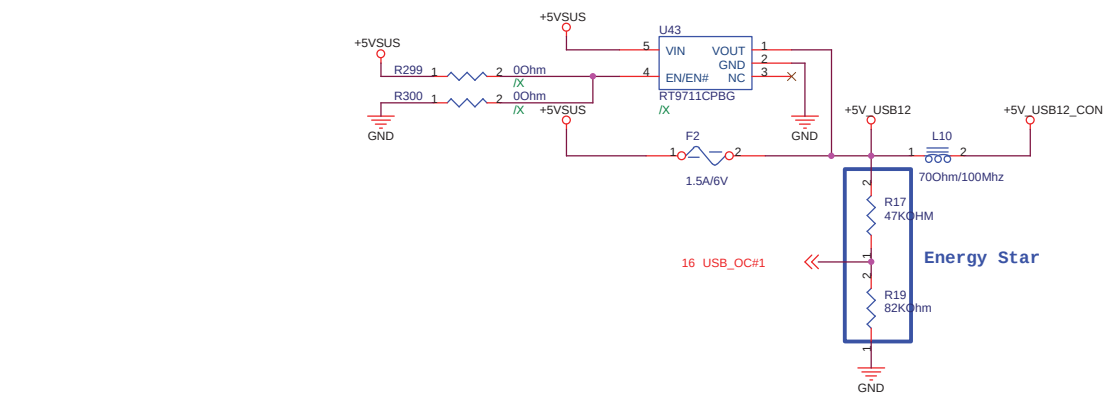


HD Master/Slave:
Master:Low
Slave :NC or
High



<Core Design>

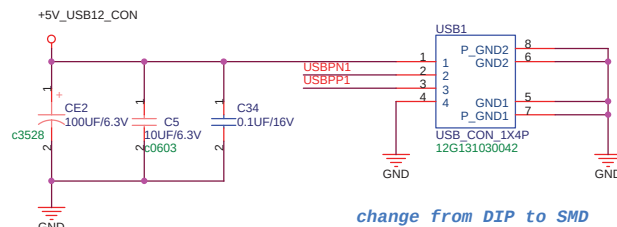
		Title : HD + Flash Conn	
ASUSTek Computer INC.		Engineer: <u>Kell Huang</u>	
Size A2	Project Name S101	Rev 1.2G	
Date: Monday, August 25, 2008		Sheet 26 of 50	



16 USB_OC#1

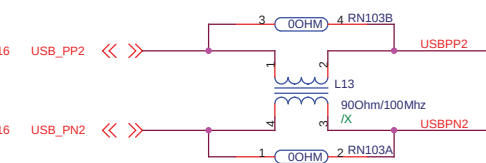
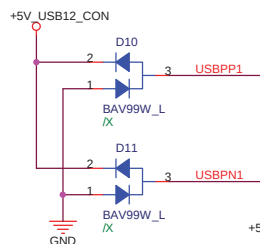
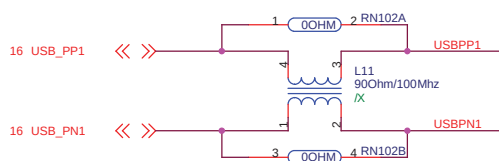
Energy Star

1.1G change USB con. to 12G131030042



change from DIP to SMD

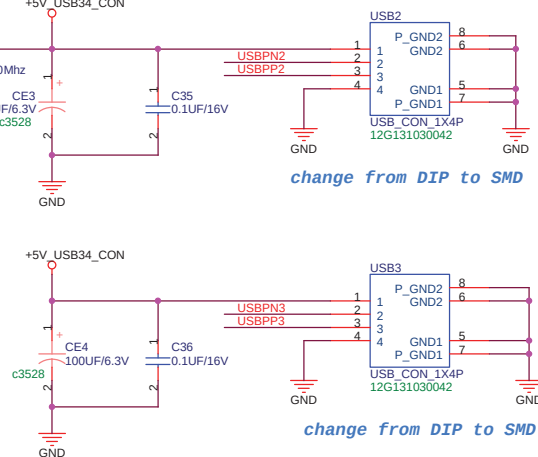
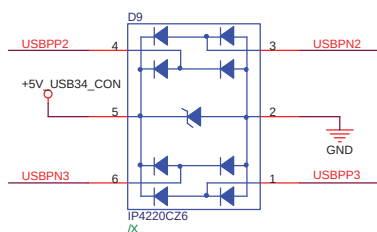
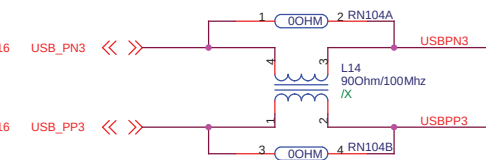
1.1G change CE2 CE3 CE4 to POSCAP, 100uF/6.3V



16 USB_OC#23

Energy Star

change from DIP to SMD

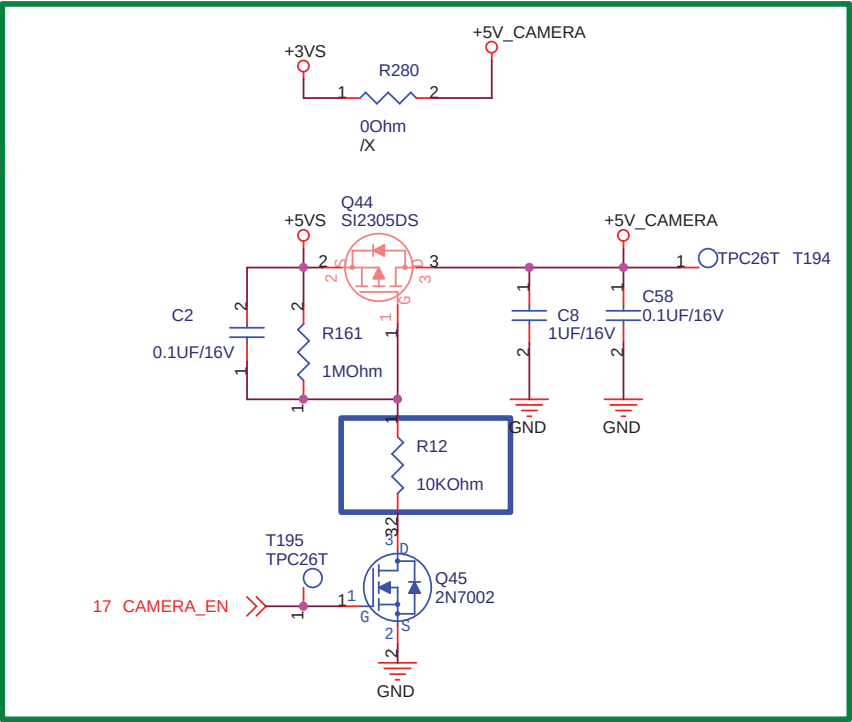


change from DIP to SMD

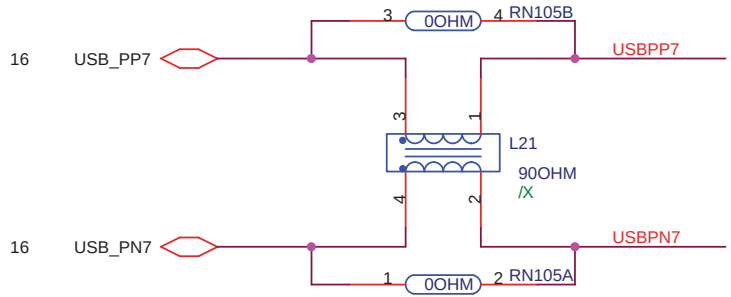
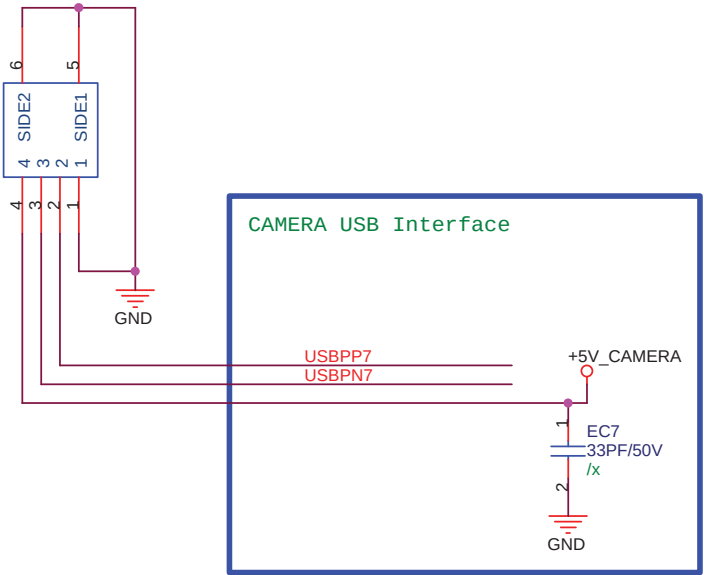
<Core Design>

ASUS		Title : USB Port	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	S101	1.2G	
Date: Monday, August 25, 2008	Sheet	27	of 50

Power Control

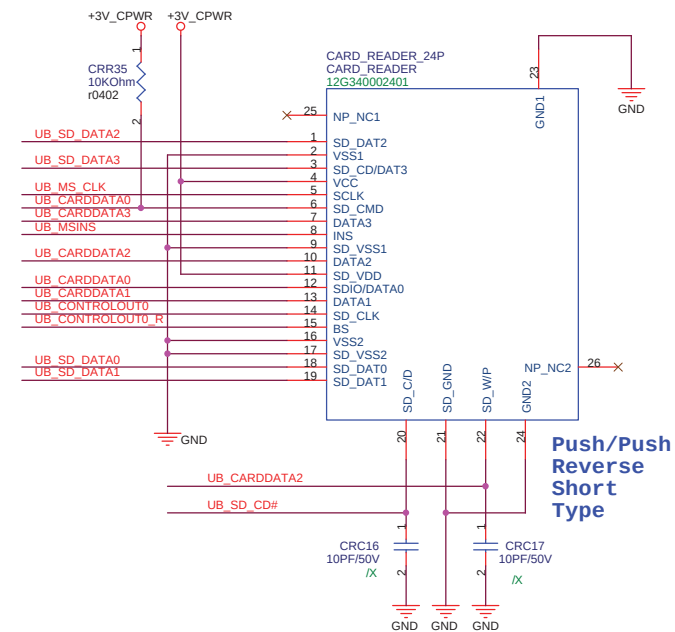


CAMERA
WTOB_CON_4P
12G171030040



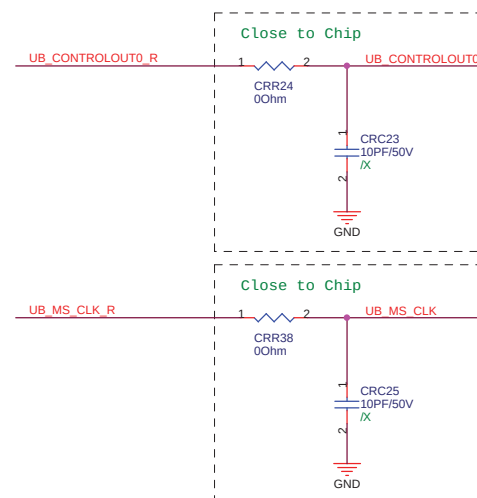
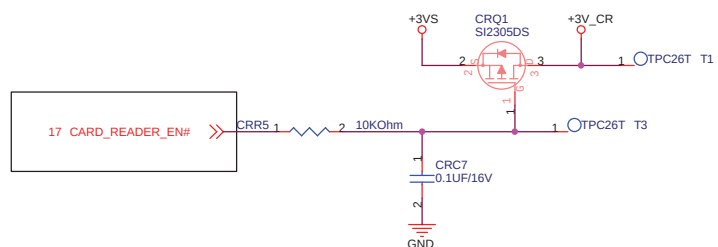
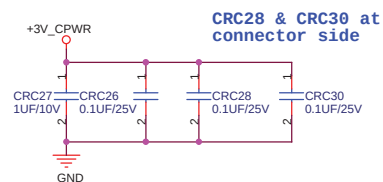
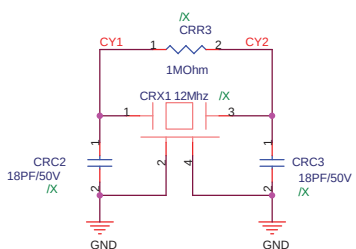
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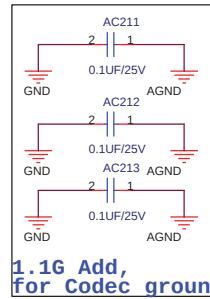
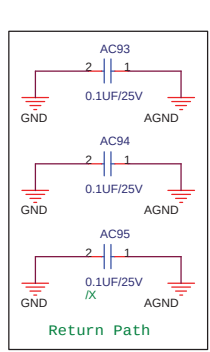
ASUS		Title : Camera Power	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name S101	Rev 1.2G	
Date: Monday, August 25, 2008		Sheet 28	of 50



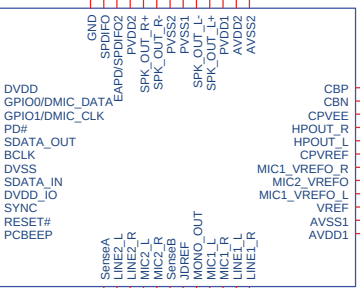
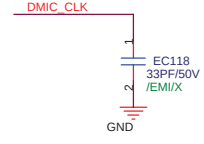
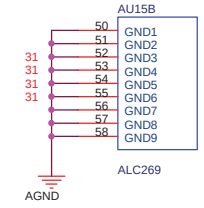
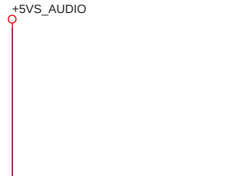
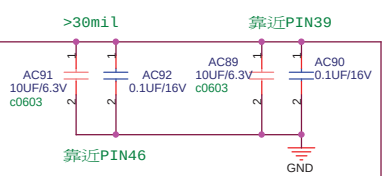
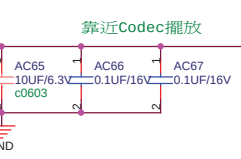
```
SDWP: Internal Pull-up
SDCDN: Internal Pull-up
SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card inserted
```

Card Insert: Pin.20 and Pin.21 are Shorted.
Card not Insert: Pin.20 and Pin.21 are Opened.
Write Protect: Pin.22 and Pin.21 are Opened.
Write Enable: Pin.22 and Pin.21 are Shorted.



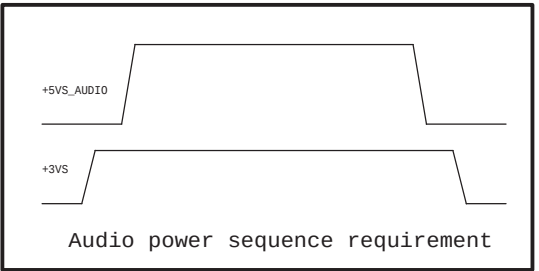
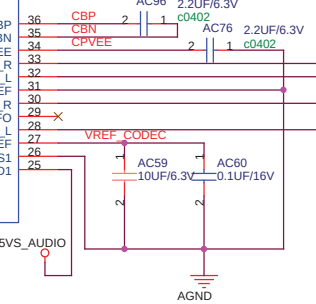


1.1G Add,
for Codec ground ring

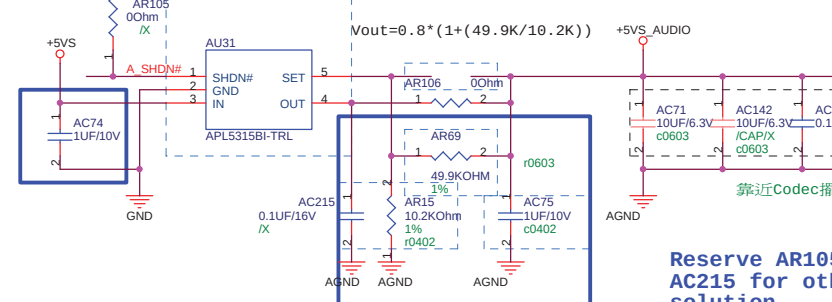
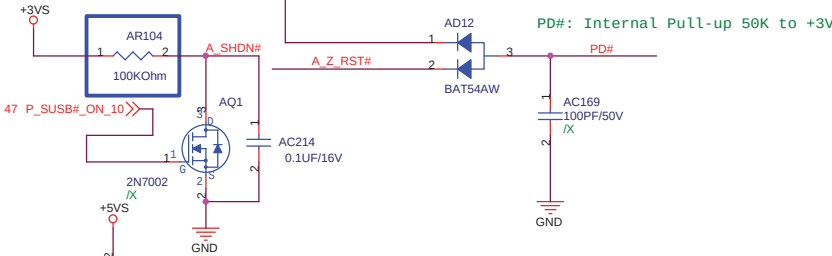
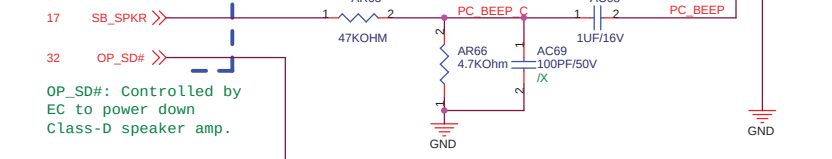
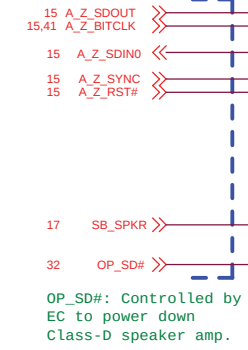


02G611005001 in the BOM

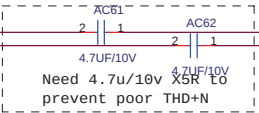
1.1G AC96 AC76 change to 0402 type



Analog: Pin.13-Pin.38
Digital: Pin.1-Pin.12
and Pin.39-Pin.48



Reserve AR105 AR106
AC215 for other LDO
solution

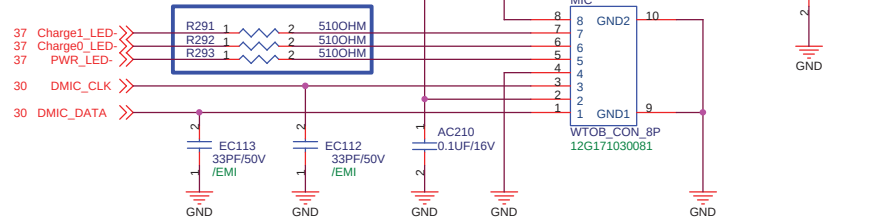


<Core Design>		Title : ALC269-1	
ASUSTek Computer Inc.		Engineer: Mick	
Size	Project Name	Rev	
A3	S101	1.2G	
Date: Monday, August 25, 2008	Sheet	30	of 50

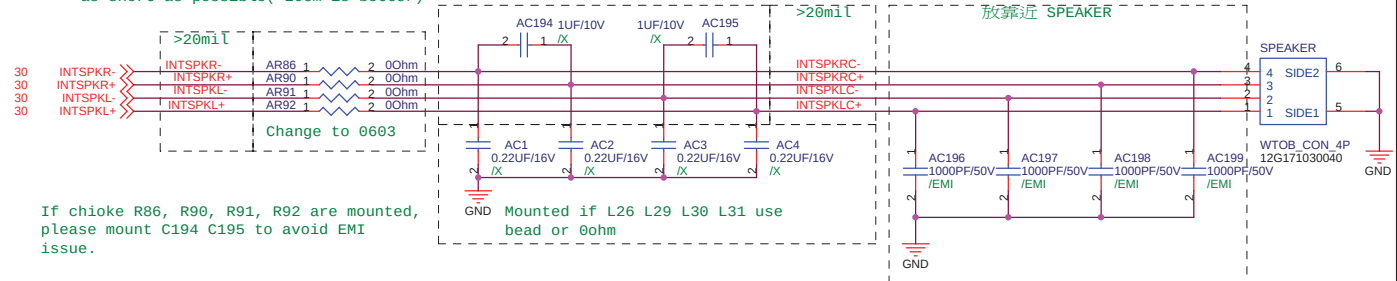
1.1G add PWR LED and Charge LED

DMIC Cable length should be less 30cm

Change R291 R292 R293 to 510 Ohm

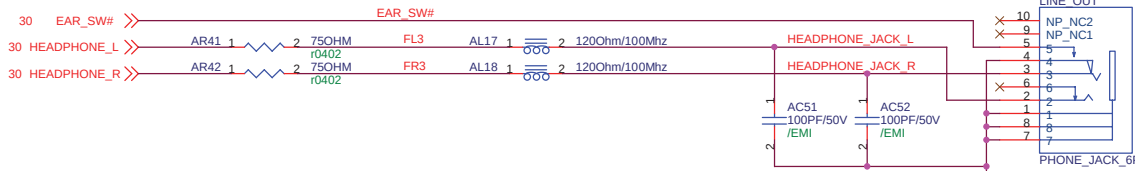


Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)



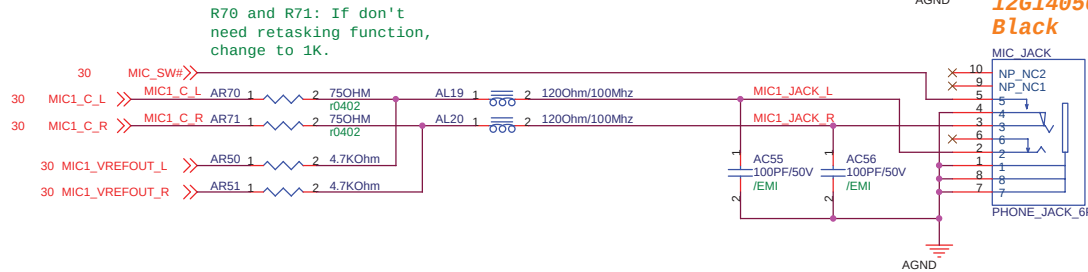
If chioke R86, R90, R91, R92 are mounted, please mount C194 C195 to avoid EMI issue.

LINE_OUT use
12G14050106P(SINGATRON)
Black



1.1G Change audio con. to black
change from DIP to SMD

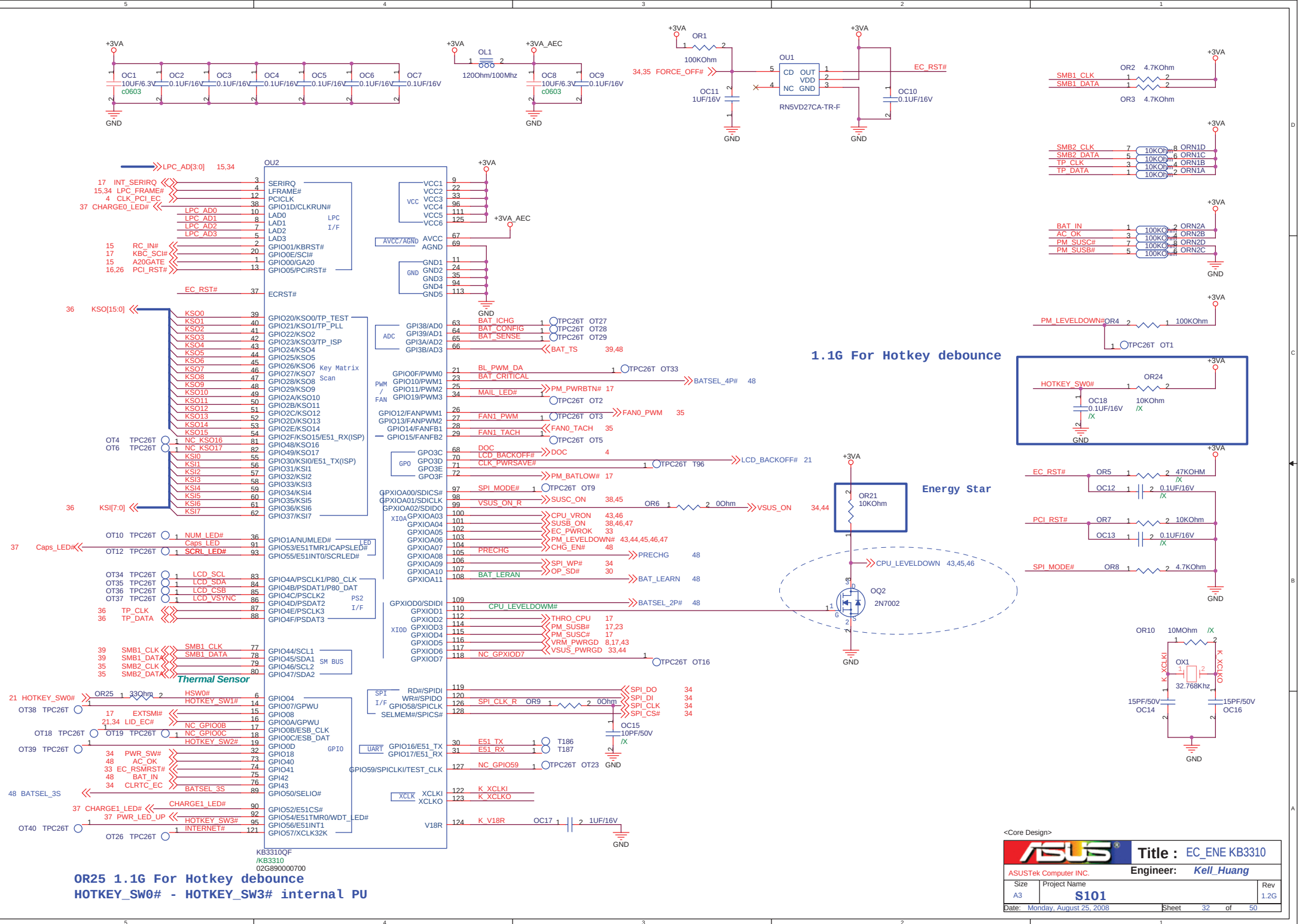
MIC JACK use
12G14050106P(SINGATRON)
Black

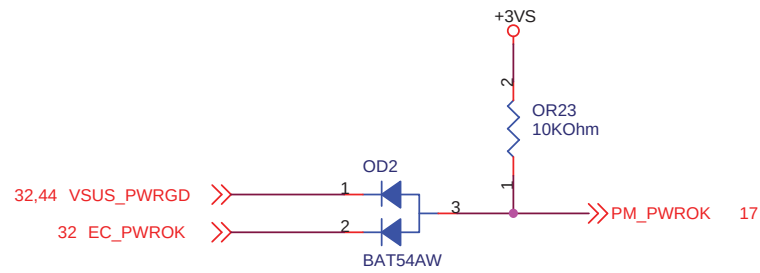
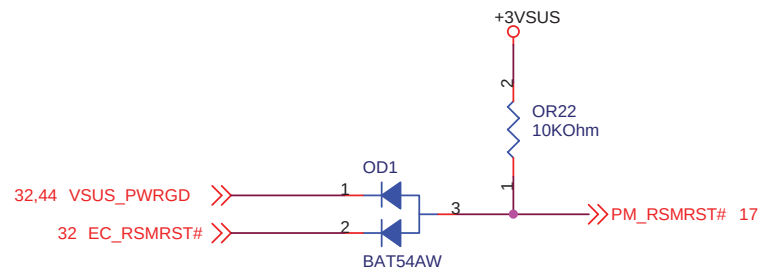


1.1G Change audio con. to black
change from DIP to SMD

<Core Design>

ASUS		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer: MICK	
Size A3	Project Name S101		Rev 1.2G
Date Monday, August 25, 2008	Sheet 31	of 50	





<Core Design>

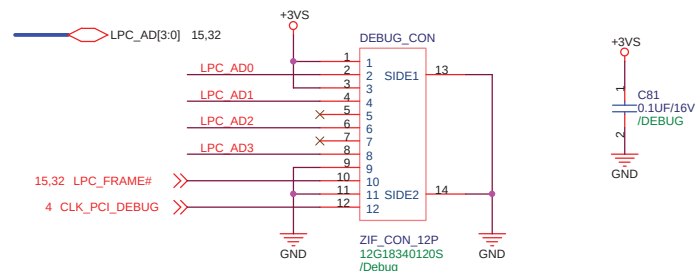
		Title : EC_UART_KC3820	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name S101		Rev 1.2G
Date: Monday, August 25, 2008		Sheet	33 of 50

prevent system power on when LCD close

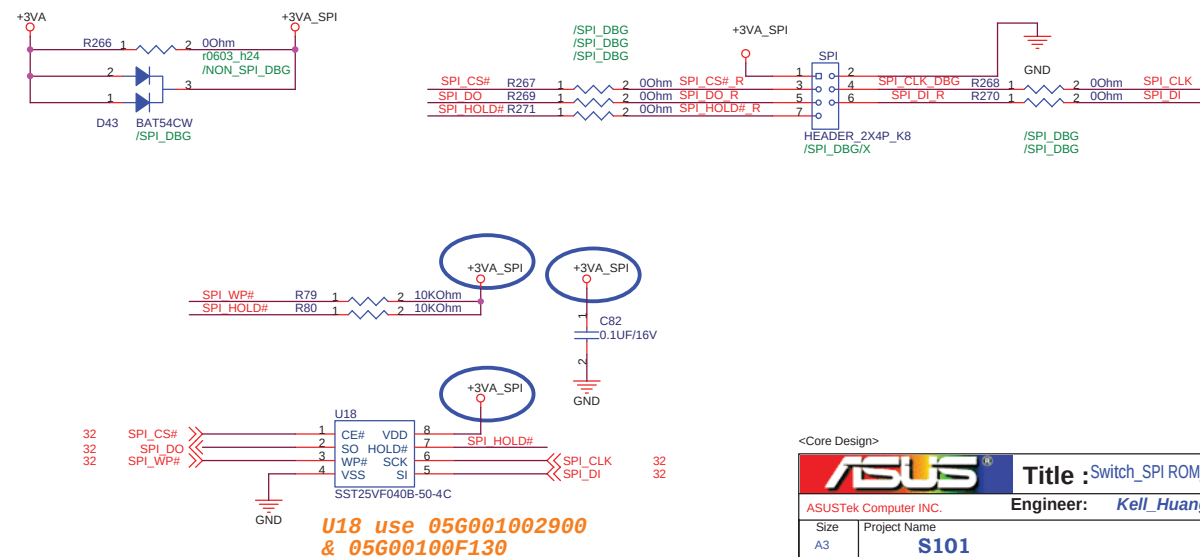
H152&H154 : Pad for EMI

prevent system auto power on when CMOS clear

For Debug



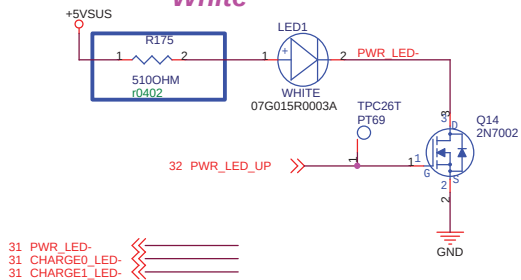
Debug Card cable use Z96 Touch Pad cable, P/N:
14G124110126, 14G124110120, 14G124110121
14G124110124, 14G124110125



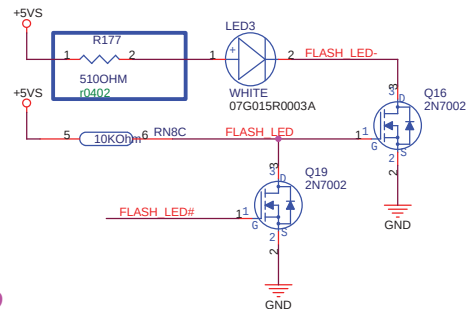
U18 use 05G001002900
& 05G00100F130

ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Kell Huang	
Size	A3	Project Name	S101
Date:	Monday, August 25, 2008	Sheet	34 of 50

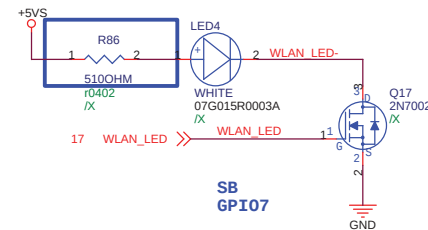
for POWER LED White



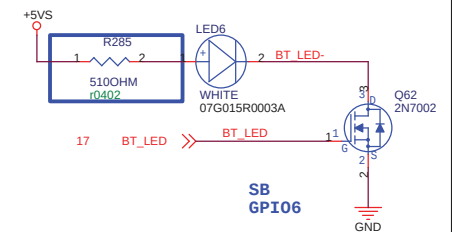
for FLASH LED White



White /X

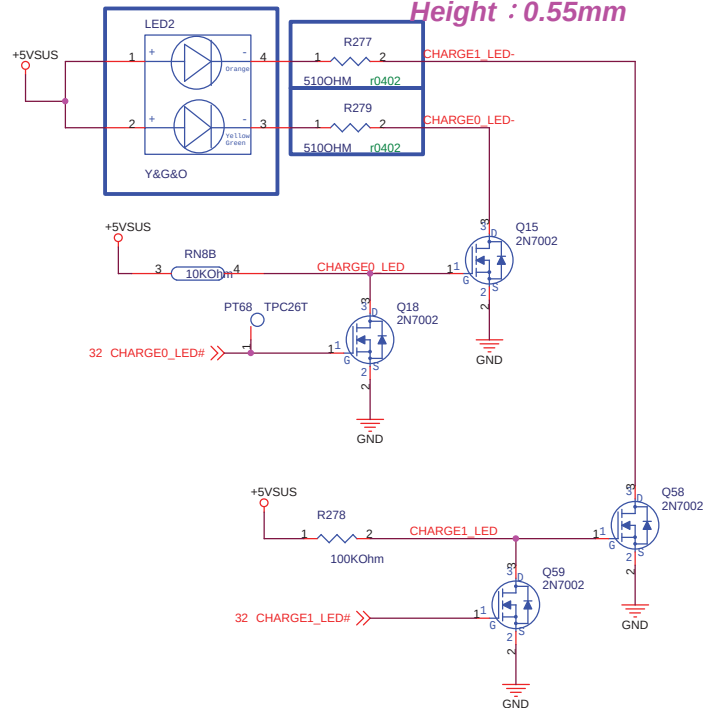


for WIFI/BlueTooth LED White

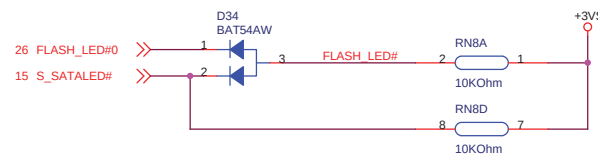


1.1G change to EVERLIGHT

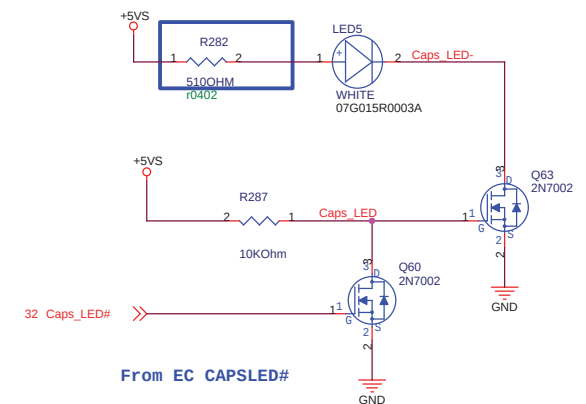
for CHARGE LED Height : 0.55mm



Change LED resistor to 510
Ohm, about 4mA



for Caps Lock LED White



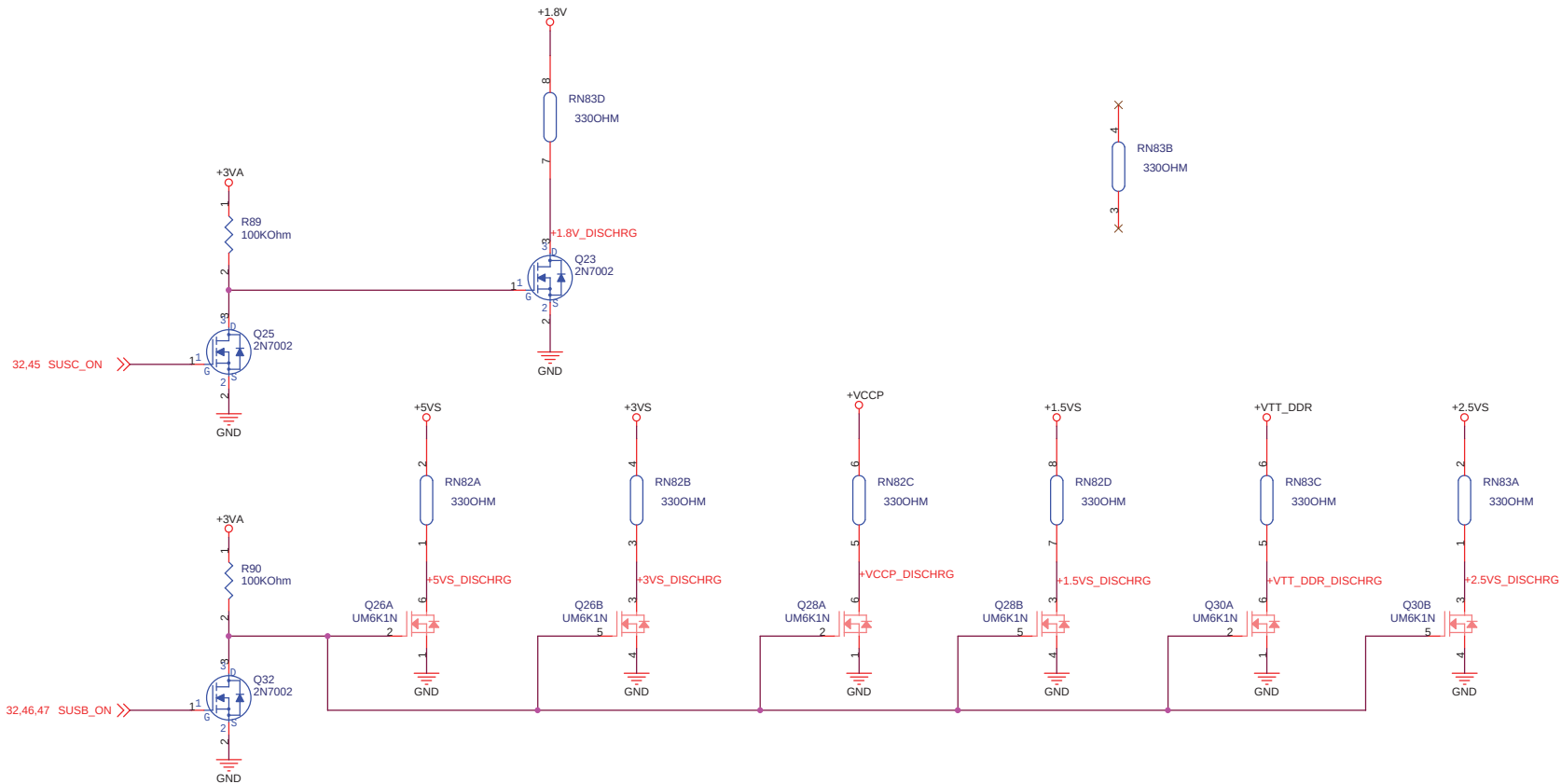
The battery charge indicator (LED) shows the status of the battery's power as follows:

scenario	Adapter mode	Battery mode
Battery power is between 100%~80%	Orange ON	Green ON
Battery power is between 80%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	Off

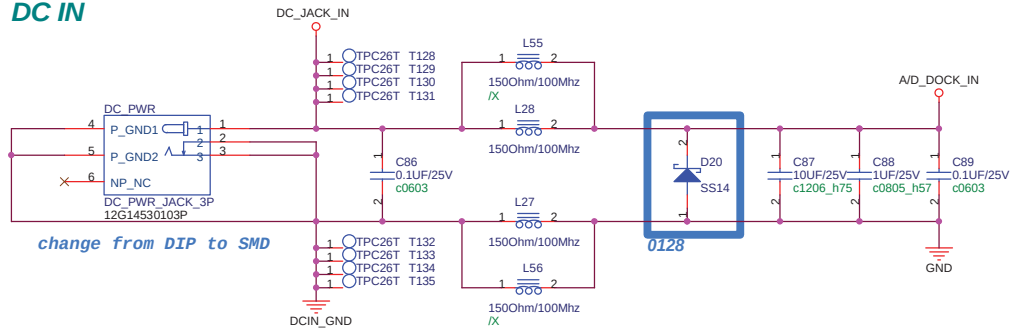
Note: The BATTERY LED should be off when the machine has no battery attached.

<Core Design>

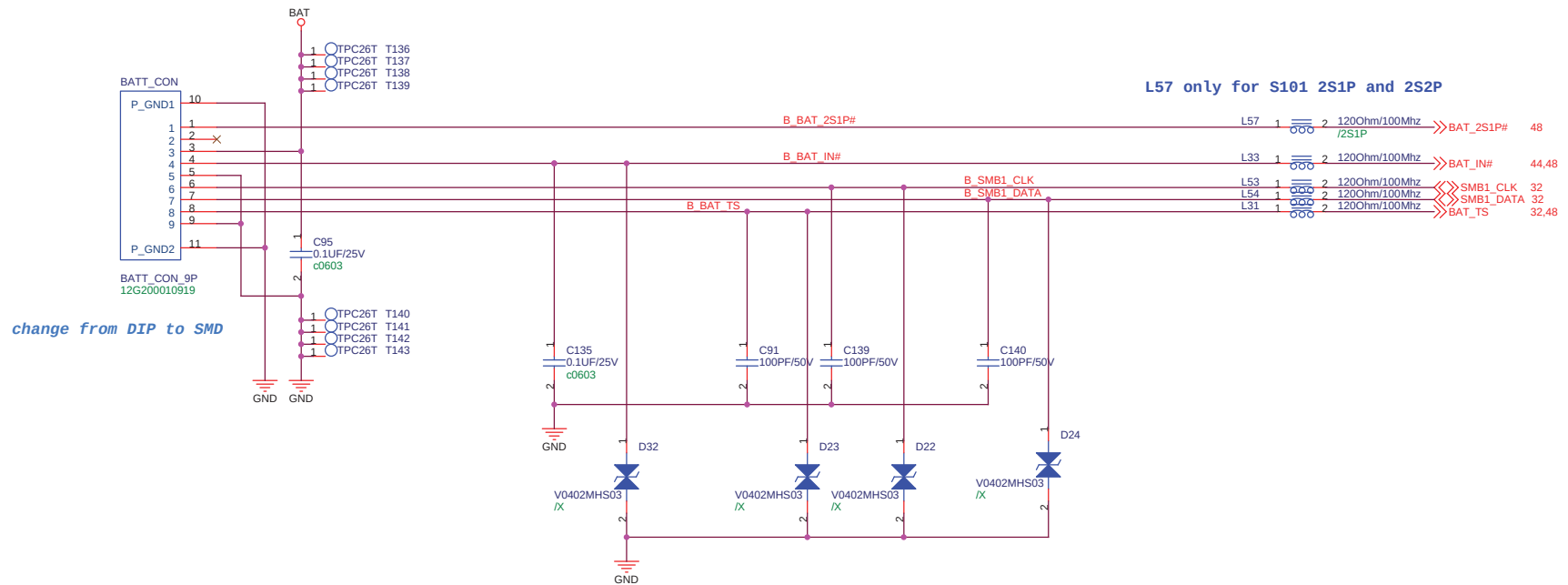
ASUS®		Title : LED	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	S101	1.2G	
Date: Monday, August 25, 2008	Sheet	37	of 50



DC IN

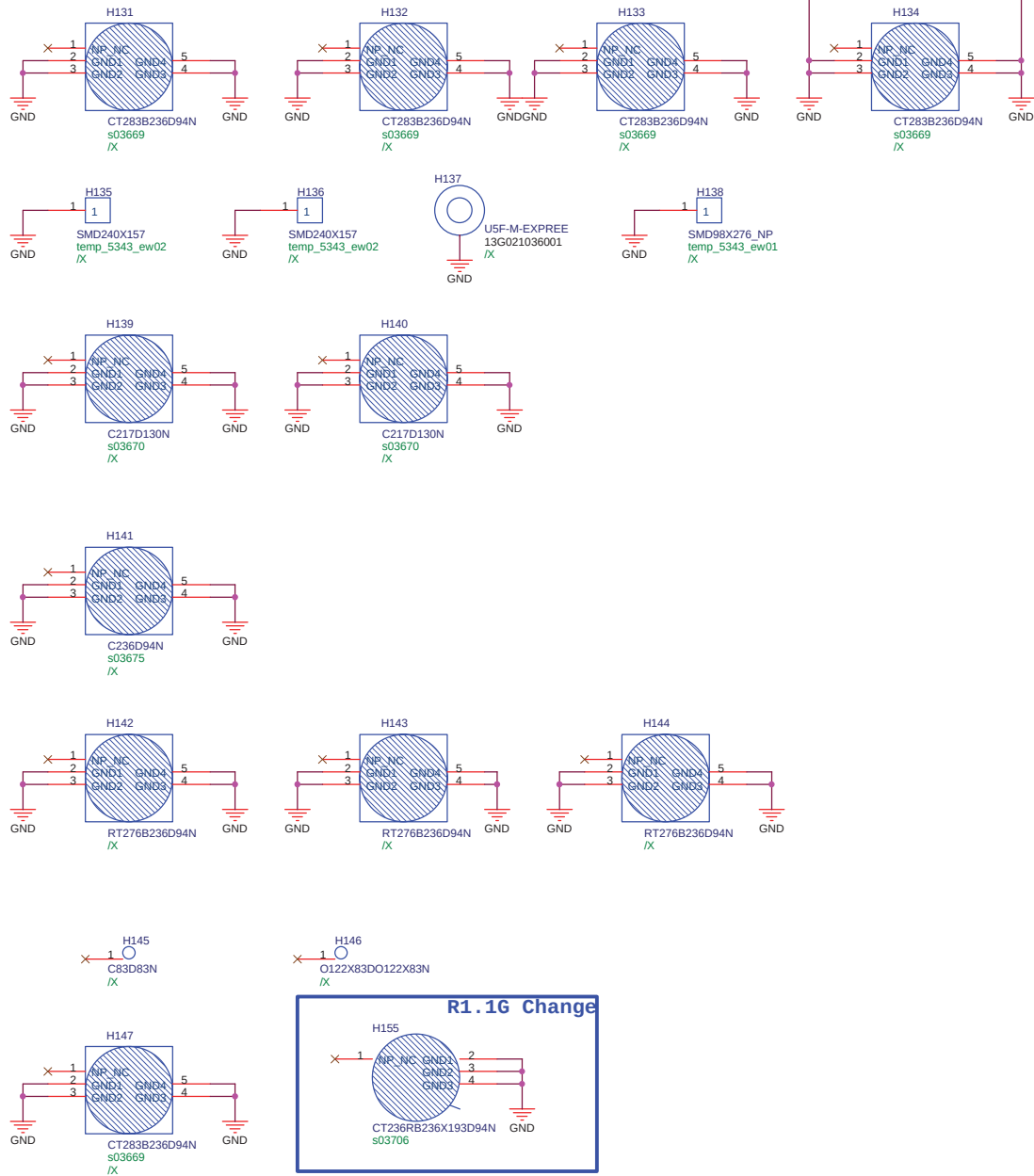


BAT IN



<Core Design>

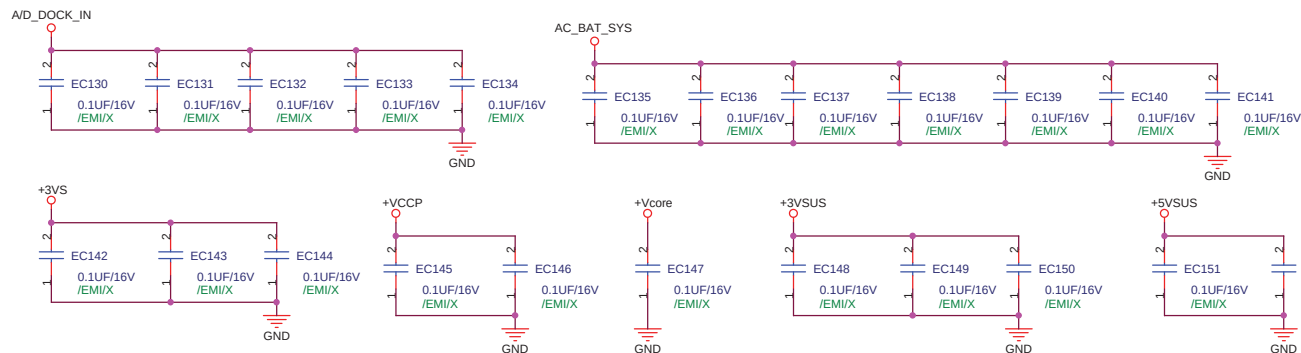
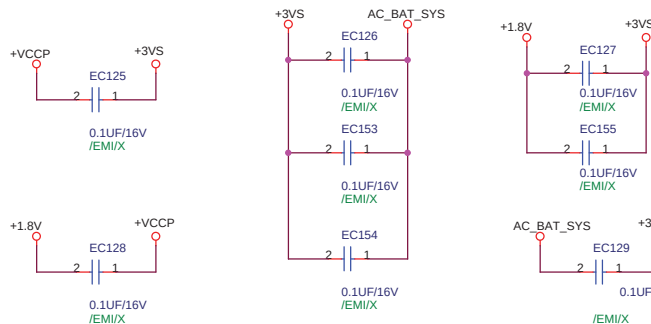
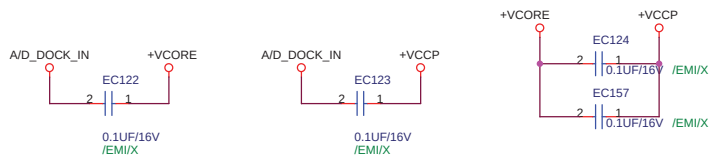
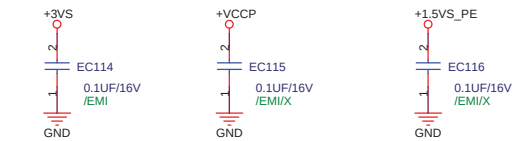
ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	S101	1.2G	
Date: Monday, August 25, 2008		Sheet	39 of 50



R1.16 Change

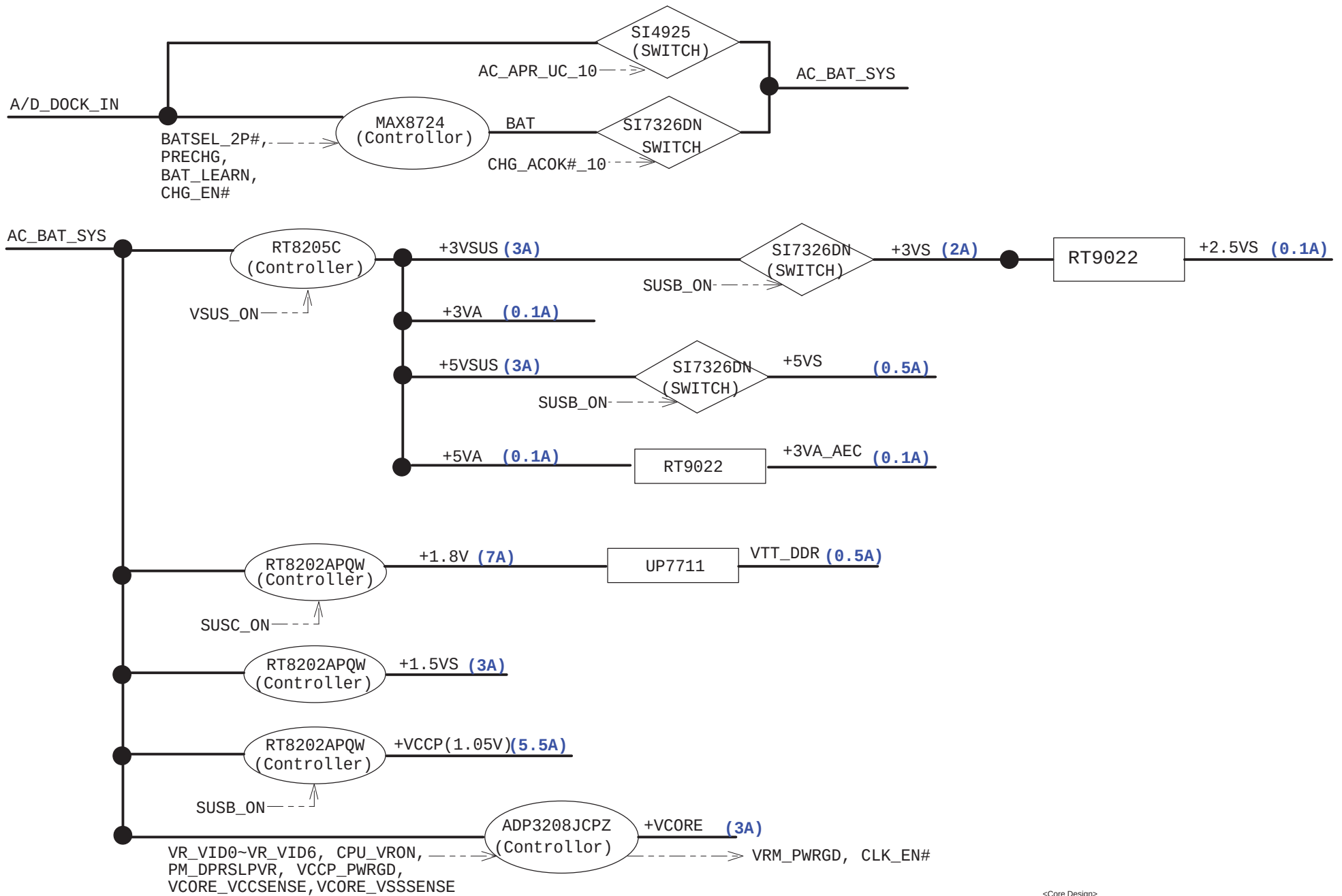
<Core Design>

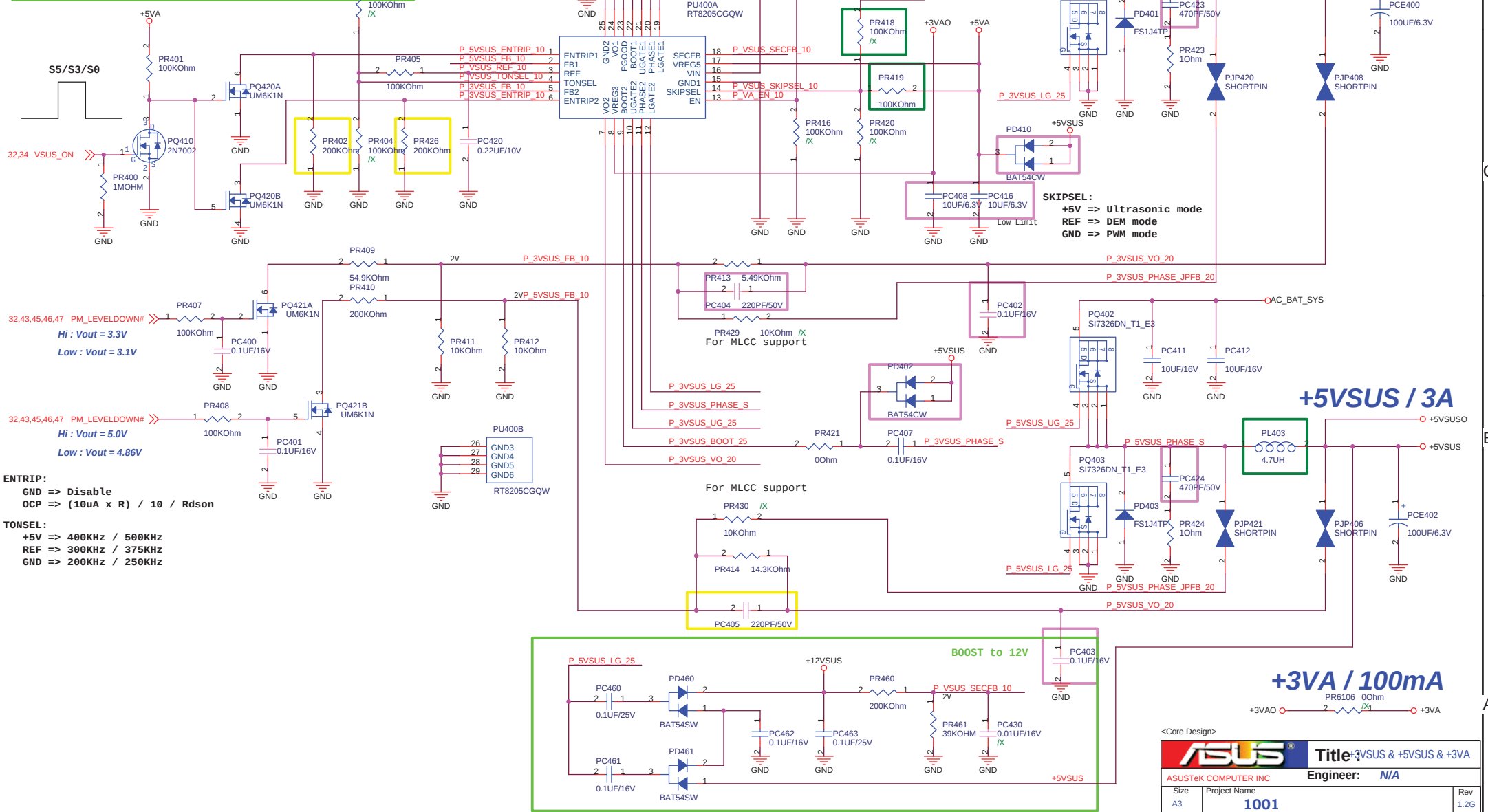
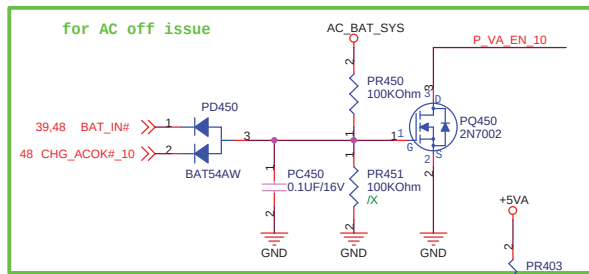
ASUS®		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	S101		1.2G
Date: Monday, August 25, 2008		Sheet	40 of 50

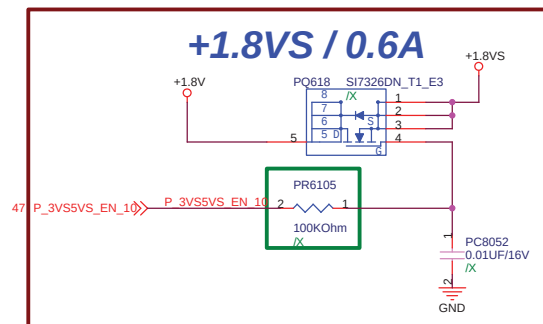
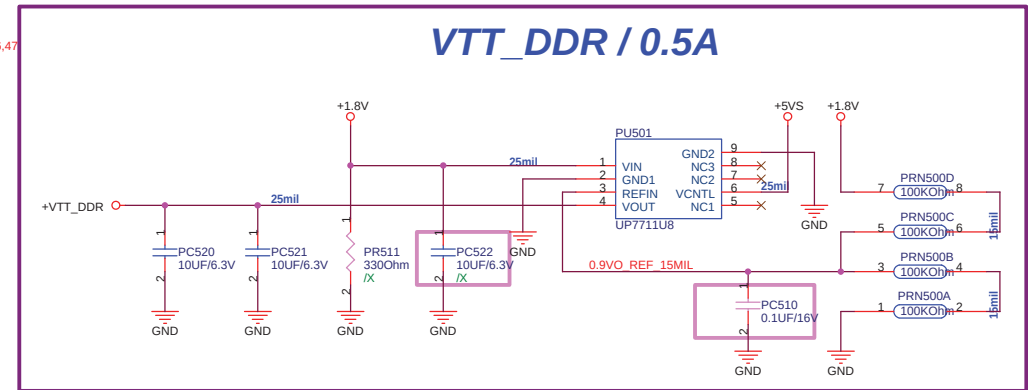
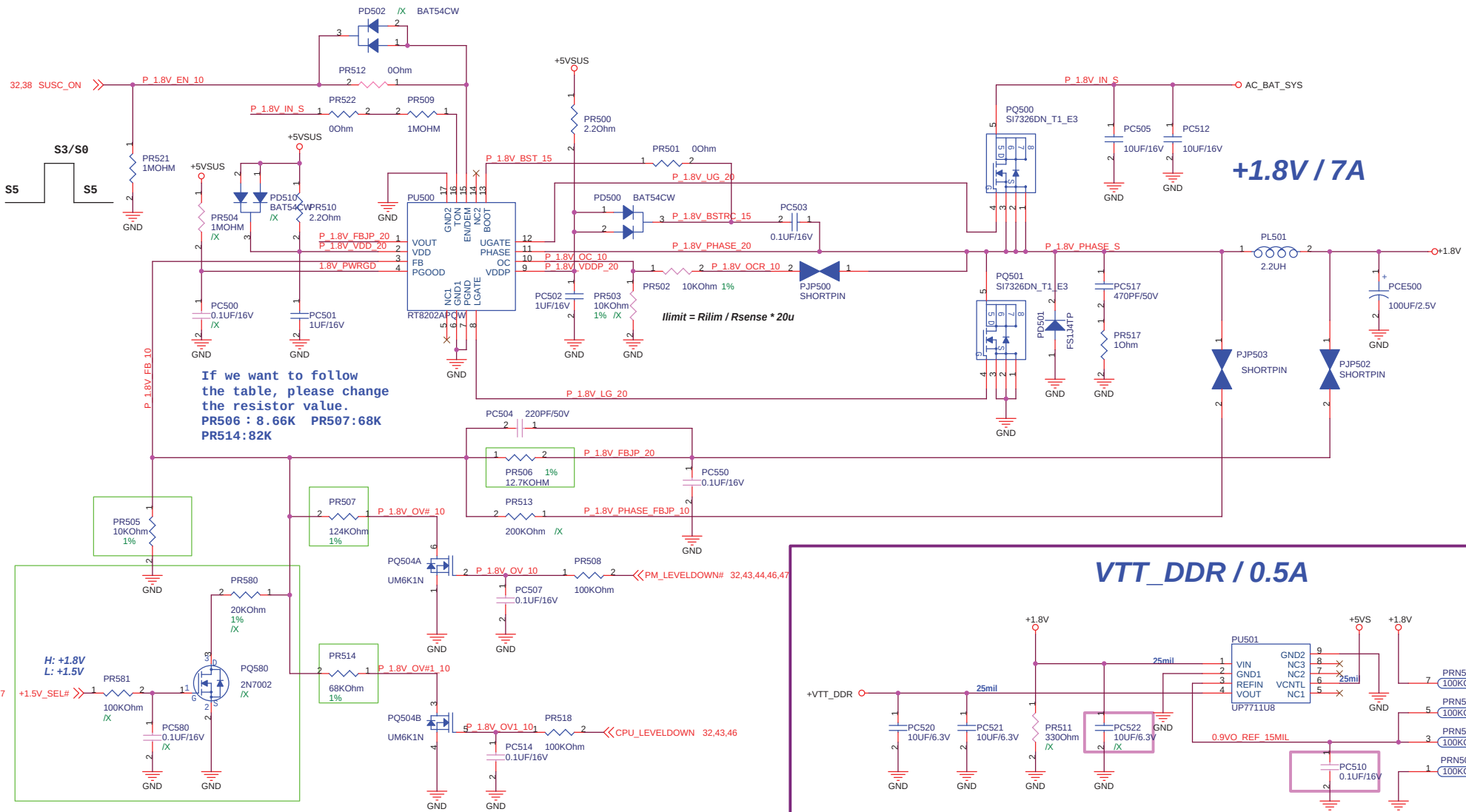


<Core Design>

ASUS		Title : EMI	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	S101		1.2G
Date: Monday, August 25, 2008		Sheet	41 of 50





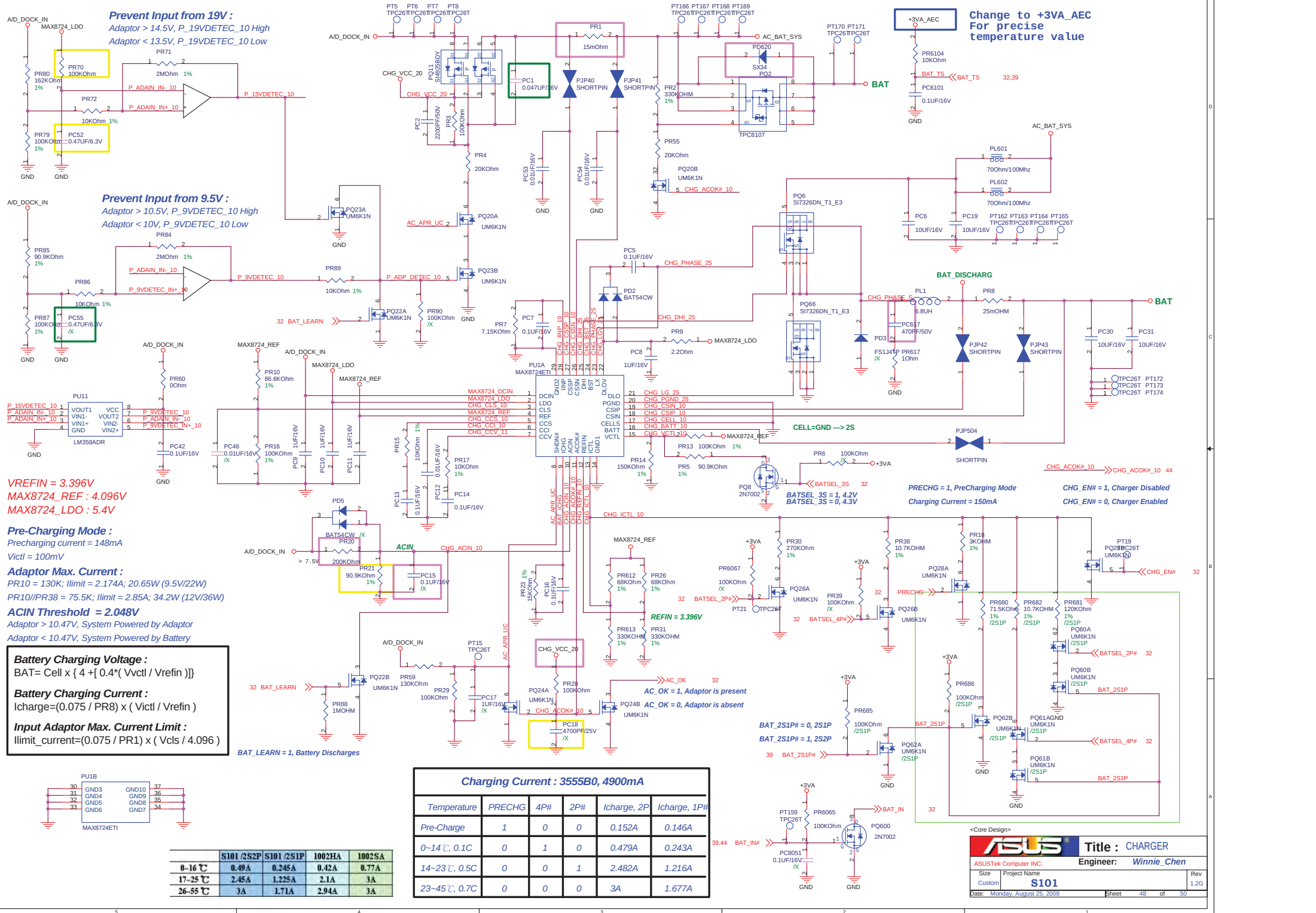


+1.5V_SEL#	PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
H	L	L	H	1.72V	Power Saving
H	H	L	H	1.82V	Normal
H	H	H	L	1.9V	Performance
H	L	H	L	1.782V	N/A
L	L	L	H	1.4V	Power Saving
L	H	L	H	1.5V	Normal
L	H	H	L	1.58V	Performance

<Core Design>

		Title : VCCP	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size A3	Project Name 1001	Rev 1.20	
Date: Monday, August 25, 2008		Sheet 46 of 50	

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A



Prevent Input from 19V :
Adaptor > 14.5V, P_19VDETEC_10 High
Adaptor < 13.5V, P_19VDETEC_10 Low

Prevent Input from 9.5V :
Adaptor > 10.5V, P_9VDETEC_10 High
Adaptor < 10V, P_9VDETEC_10 Low

VREFIN = 3.396V
MAX8724_REF = 4.096V
MAX8724_LDO = 5.4V

Pre-Charging Mode :
Precharging current = 148mA
Vicl = 100mV
Adaptor Max. Current :
PR10 = 130K; Ilimit = 2.174A; 20.65W (9.5V/22W)
PR10/PR38 = 75.5K; Ilimit = 2.85A; 34.2W (12V/36W)
ACIN Threshold = 2.048V
Adaptor > 10.47V, System Powered by Adaptor
Adaptor < 10.47V, System Powered by Battery

Battery Charging Voltage :
 $BAT = Cell \times \{ 4 + [0.4 \times (V_{vcl} / V_{refin})] \}$
Battery Charging Current :
 $I_{charge} = (0.075 / PR8) \times (V_{icl} / V_{refin})$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (0.075 / PR1) \times (V_{cls} / 4.096)$

MAX8724ETI

	S101/2S2P	S101/2S1P	1002HA	1002SA
0-16 °C	0.49A	0.245A	0.42A	0.77A
17-25 °C	2.45A	1.225A	2.1A	3A
26-55 °C	3A	1.71A	2.94A	3A

Charging Current : 3555B0, 4900mA

Temperature	PRECHG	4P#	2P#	Icharge, 2P	Icharge, 1P#
Pre-Charge	1	0	0	0.152A	0.146A
0-14 °C, 0.1C	0	1	0	0.479A	0.243A
14-23 °C, 0.5C	0	0	1	2.482A	1.216A
23-45 °C, 0.7C	0	0	0	3A	1.677A

Change to +3VA_AEC
For precise
temperature value

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Internal Pull Up
15	GPIO08	EXTSMIH#	OD	10K ohm Pull Up to +3VSU
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	HOTKEY_SW2#	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	OD	10K ohm Pull Up to +3VSUS
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL_4P#	O	Battery charging current setting
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	O	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GP138/AD0	BAT_ICHG	I	
64	GP139/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GP142	BAT_IN	I	
76	GP143	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Core Design>



Title : EC Pin Define

ASUSTek Computer INC.

Engineer: **Satan He**

Size
A3

Project Name
S101

Rev
1.2G

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D					
C					
B					
A					

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		Title : History	
ASUSTek Computer INC.		Engineer: Satan He	
Size	Project Name		Rev
A3	S101		1.2G
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