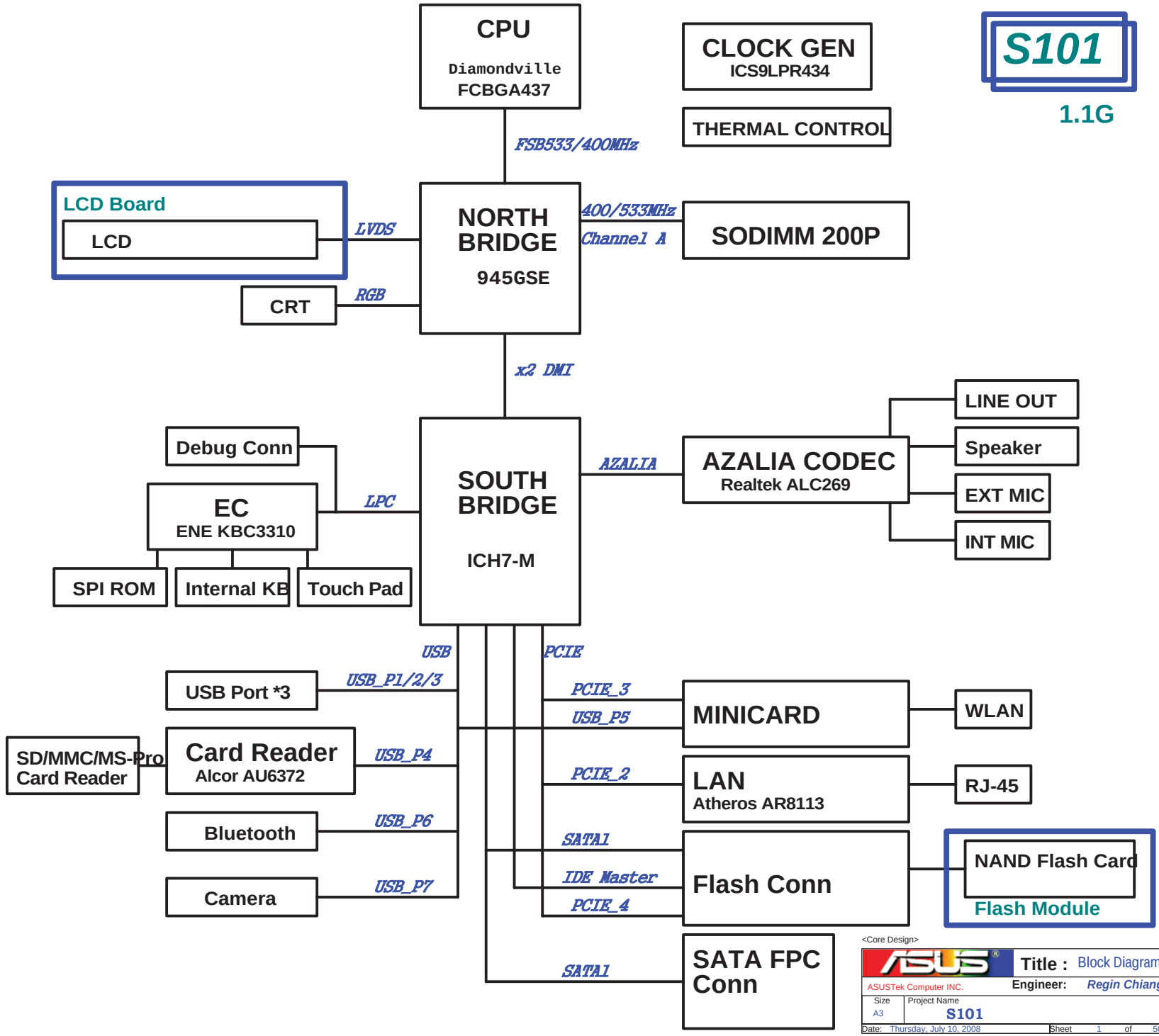


<Core Design>

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Regin Chiang

Size	Project Name	Rev
A3	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 1 of 50

EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera

PCIE

PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

<Core Design>

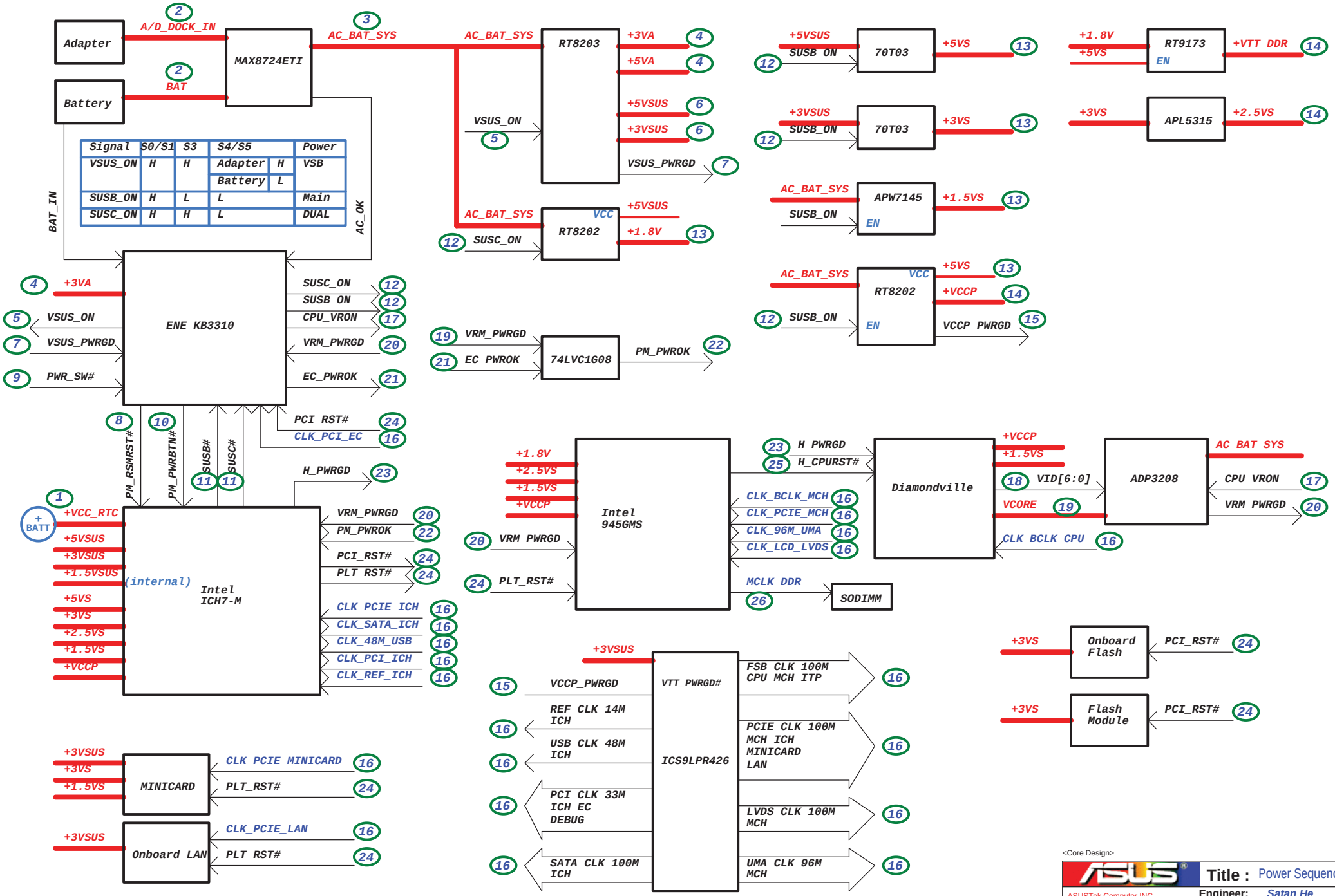
ASUSTek Computer INC.

Title : System Setting

Engineer: Satan_He

Size	Project Name	Rev
A3	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 2 of 50



<Core Design>

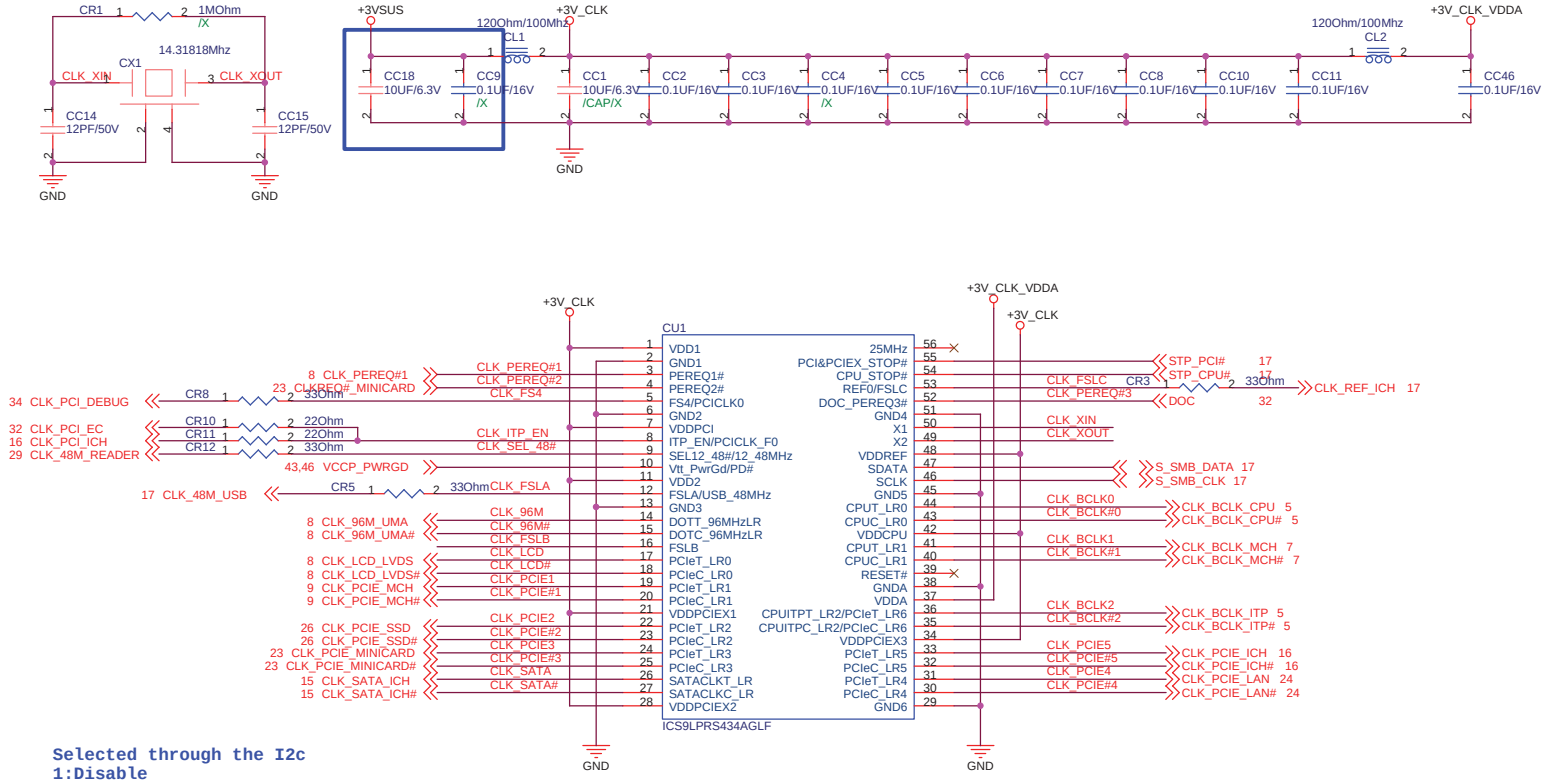
ASUSTek Computer INC.

Title : Power Sequence

Engineer: Satan He

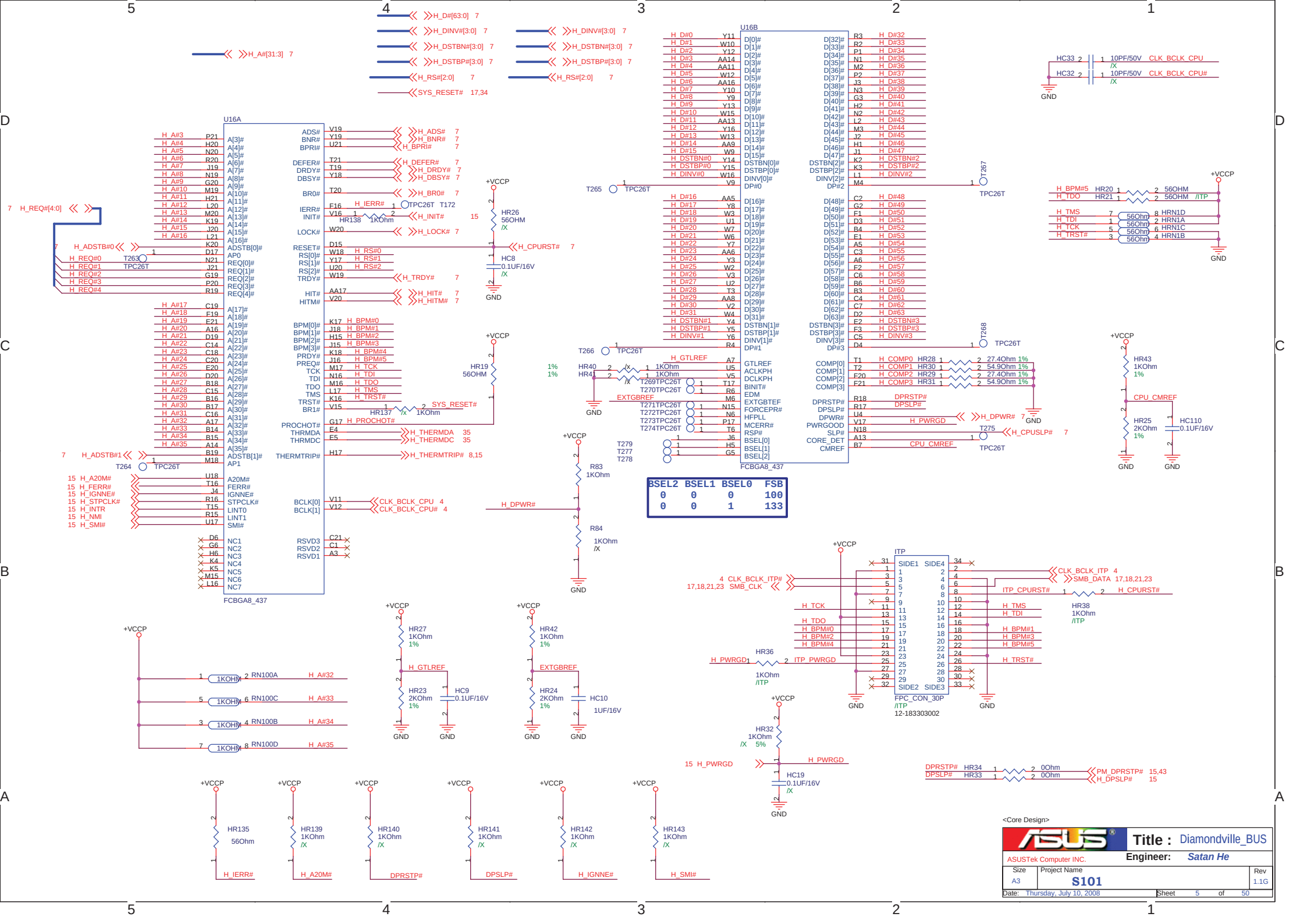
Size	Project Name	Rev
A3	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 3 of 50



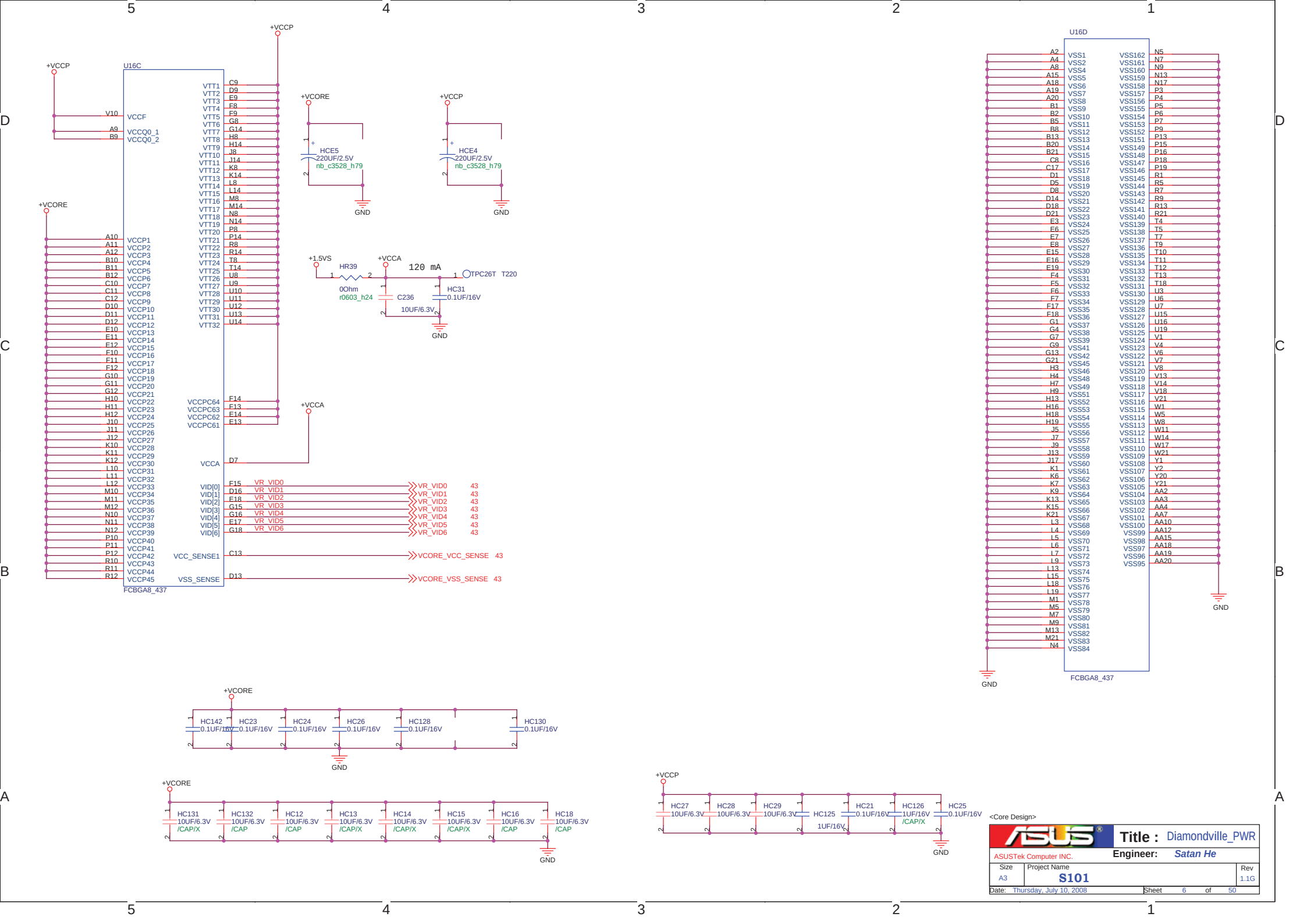
<Core Design>

ASUSTek Computer INC.	Title : Clock Gen_ICS9LPRS434	
	Engineer: Satan He	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 4 of 50	



<Core Design>

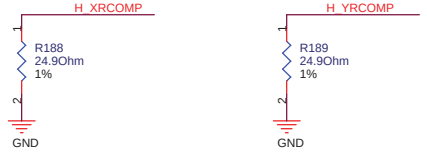
ASUSTek Computer INC.	Title : Diamondville_BUS	
	Engineer: Satan He	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 5 of 50	


U16C
FCBGA8_437
+VCCP
+VCORE
+VCCA
+1.5VS
HR39
0Ohm
r0603_h24
C236
10UF/6.3V
HC31
0.1UF/16V
120 mA
TPC26T T220
HCE5
220UF/2.5V
nb_c3528_h79
HCE4
220UF/2.5V
nb_c3528_h79
GND
VCCF
VCCQ0_1
VCCQ0_2
VCCP1
VCCP2
VCCP3
VCCP4
VCCP5
VCCP6
VCCP7
VCCP8
VCCP9
VCCP10
VCCP11
VCCP12
VCCP13
VCCP14
VCCP15
VCCP16
VCCP17
VCCP18
VCCP19
VCCP20
VCCP21
VCCP22
VCCP23
VCCP24
VCCP25
VCCP26
VCCP27
VCCP28
VCCP29
VCCP30
VCCP31
VCCP32
VCCP33
VCCP34
VCCP35
VCCP36
VCCP37
VCCP38
VCCP39
VCCP40
VCCP41
VCCP42
VCCP43
VCCP44
VCCP45
VTT1
VTT2
VTT3
VTT4
VTT5
VTT6
VTT7
VTT8
VTT9
VTT10
VTT11
VTT12
VTT13
VTT14
VTT15
VTT16
VTT17
VTT18
VTT19
VTT20
VTT21
VTT22
VTT23
VTT24
VTT25
VTT26
VTT27
VTT28
VTT29
VTT30
VTT31
VTT32
VCCPC64
VCCPC63
VCCPC62
VCCPC61
VCCA
VID[0]
VID[1]
VID[2]
VID[3]
VID[4]
VID[5]
VID[6]
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
VCC_SENSE1
VSS_SENSE
VCORE_VCC_SENSE
VCORE_VSS_SENSE
U16D
FCBGA8_437
HC142
HC23
HC24
HC26
HC128
HC130
0.1UF/16V
HC131
HC132
HC12
HC13
HC14
HC15
HC16
HC18
10UF/6.3V
/CAP/X
/CAP
HC27
HC28
HC29
HC125
HC21
HC126
HC25
1UF/16V
/CAP/X
<Core Design>
Title : Diamondville_PWR
ASUSTek Computer INC.
Engineer: Satan He
Size A3
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 6 of 50

Power :
+VCCP

RCOMP

For Calibrating the FSB I/O Buffer

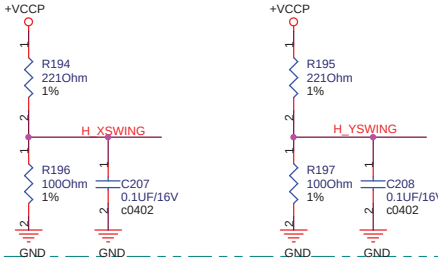


SCOMP

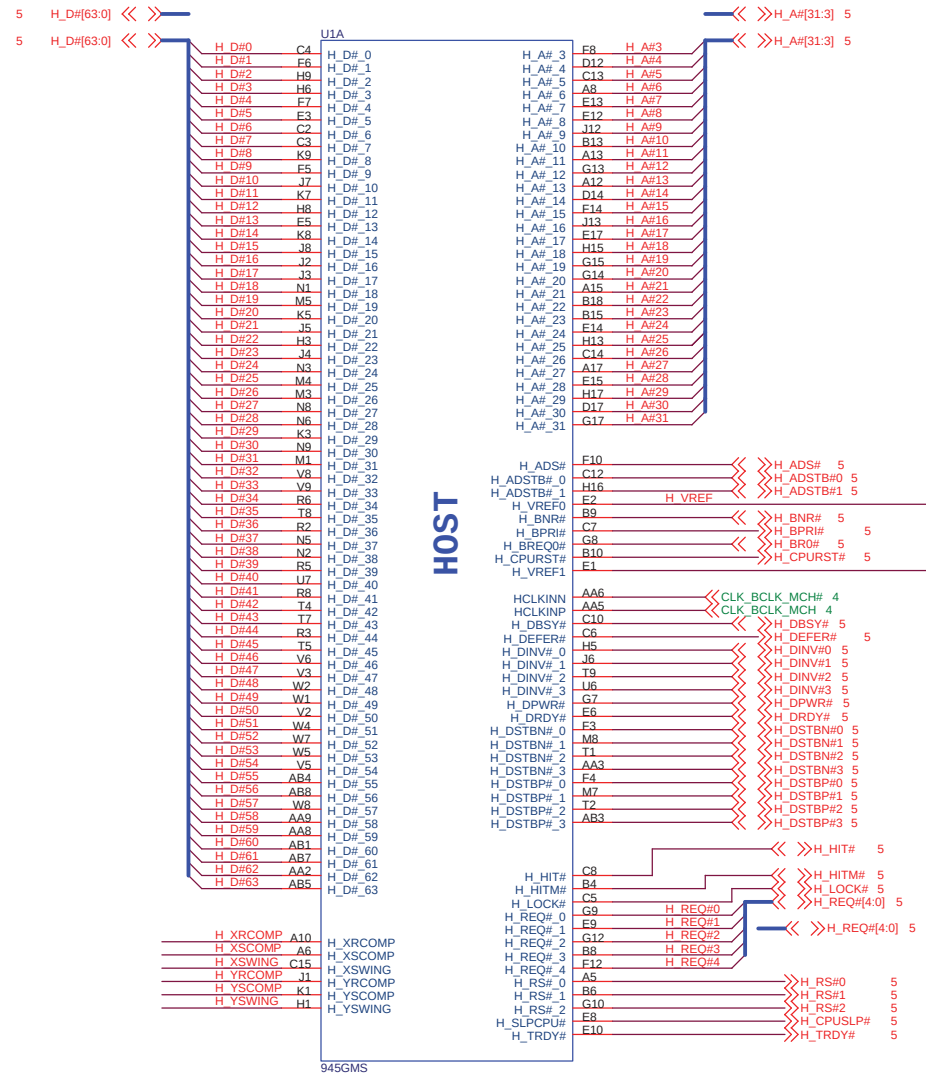
For Slew Rate Compenssation on the FSB

Voltage Swing

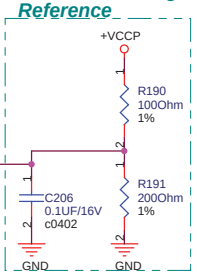
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



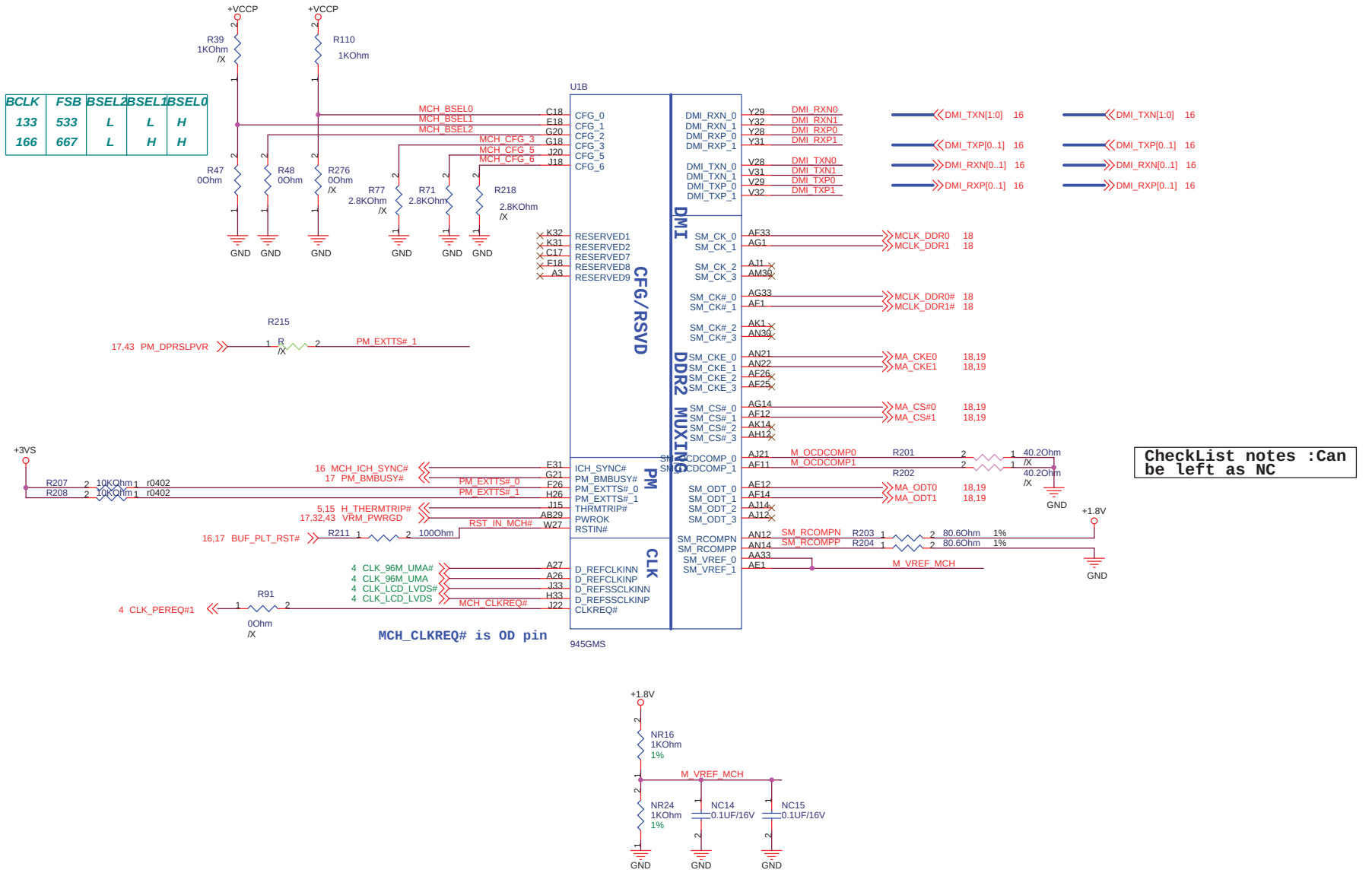
AGTL+ I/O Voltage Reference



Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

<Core Design>

Title : NB-945GMS(HOST)		
ASUSTeK COMPUTER INC.	Engineer: Satan He	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 7 of 50	



<Core Design>

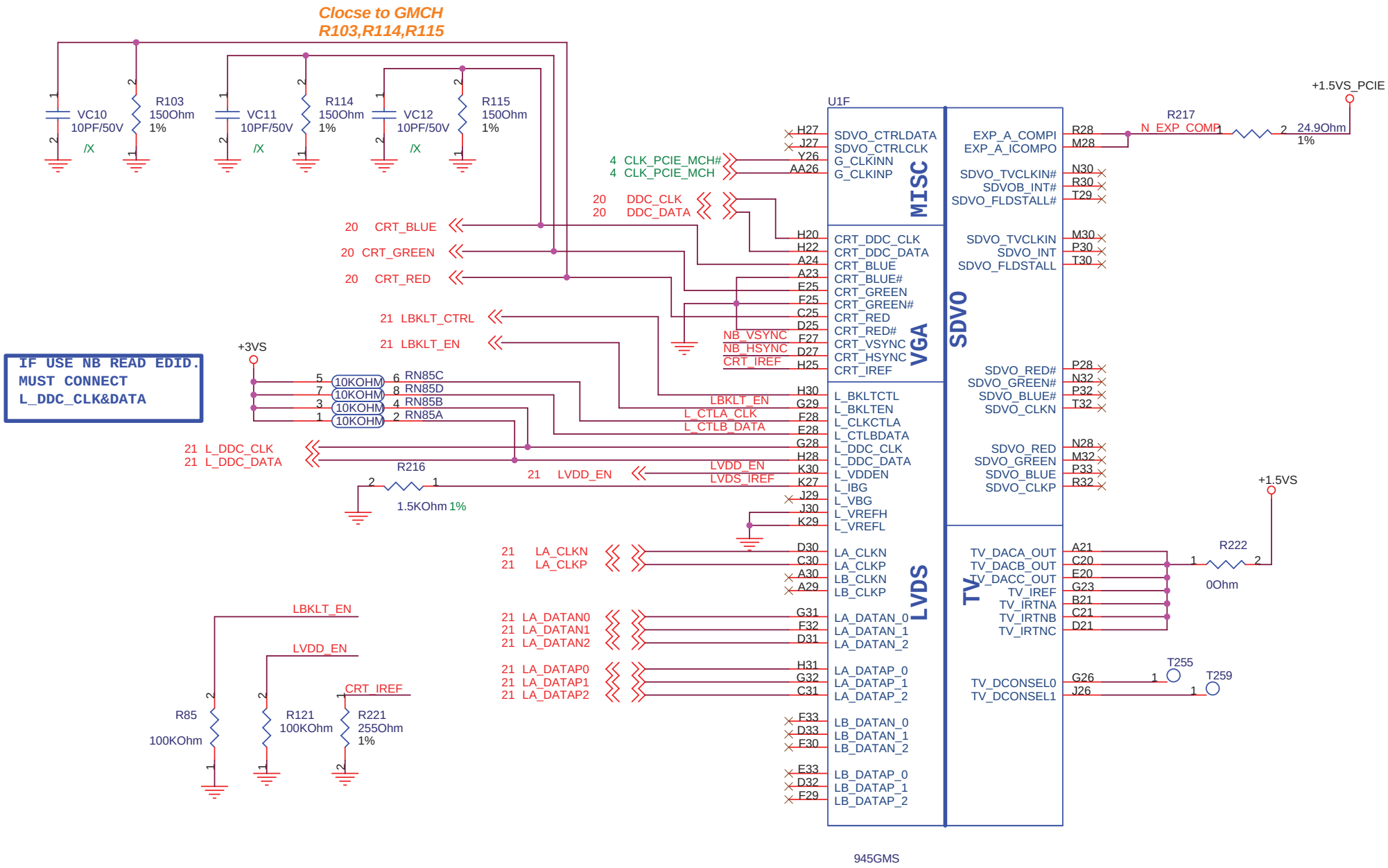
ASUSTeK COMPUTER INC.

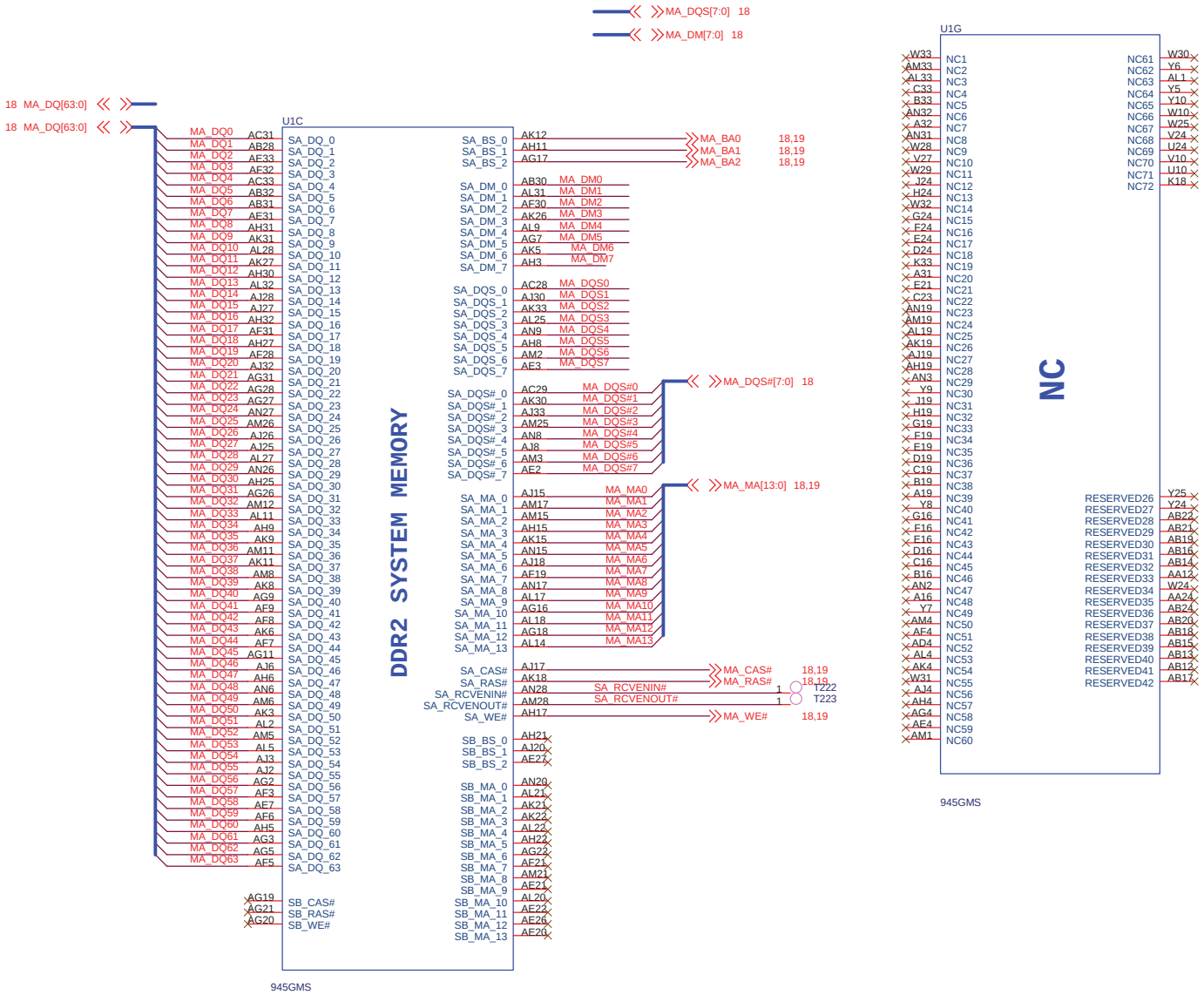
Title : NB-945GMS(DMI & CFG)

Engineer: Satan He

Size	Project Name	Rev
A3	S101	1.1G

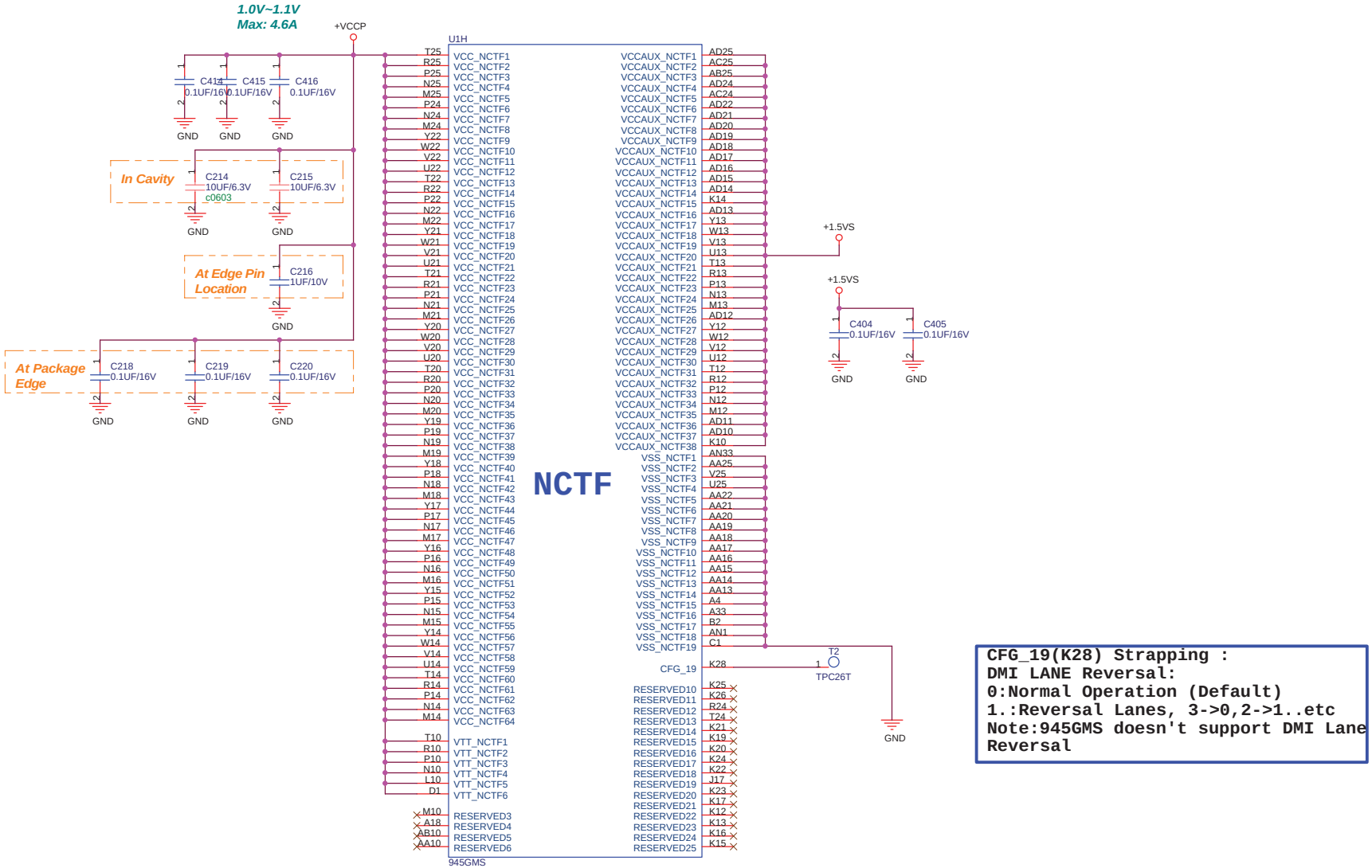
Date: Thursday, July 10, 2008 Sheet 8 of 50


Clocse to GMCH
R103,R114,R115
VC10
10PF/50V
/X
R103
150Ohm
1%
VC11
10PF/50V
/X
R114
150Ohm
1%
VC12
10PF/50V
/X
R115
150Ohm
1%
U1F
SDVO_CTRLDATA
SDVO_CTRLCLK
G_CLKINN
G_CLKINP
MISC
4 CLK_PCIE_MCH#
4 CLK_PCIE_MCH
20 DDC_CLK
20 DDC_DATA
20 CRT_BLUE
20 CRT_GREEN
20 CRT_RED
21 LBKLT_CTRL
21 LBKLT_EN
NB_VSYNC
NB_HSYNC
CRT_IREF
CRT_DDC_CLK
CRT_DDC_DATA
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_VSYNC
CRT_HSYNC
CRT_IREF
VGA
SDVO
EXP_A_COMPI
EXP_A_ICOMPO
R217
N_EXP_COMP
24.9Ohm
1%
+1.5VS_PCIE
SDVO_TVCLKIN#
SDVOB_INT#
SDVO_FLDSTALL#
SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL
SDVO_RED#
SDVO_GREEN#
SDVO_BLUE#
SDVO_CLKN
SDVO_RED
SDVO_GREEN
SDVO_BLUE
SDVO_CLKP
IF USE NB READ EDID.
MUST CONNECT
L_DDC_CLK&DATA
+3VS
RN85C
RN85D
RN85B
RN85A
10KOHM
LBKLT_EN
L_CTLA_CLK
L_CTLB_DATA
21 L_DDC_CLK
21 L_DDC_DATA
R216
1.5KOhm 1%
21 LVDD_EN
LVDD_EN
LVDS_IREF
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CTLBDATA
L_DDC_CLK
L_DDC_DATA
L_VDDEN
L_IBG
L_VBG
L_VREFH
L_VREFL
LVDS
21 LA_CLKN
21 LA_CLKP
LA_CLKN
LA_CLKP
LB_CLKN
LB_CLKP
21 LA_DATAN0
21 LA_DATAN1
21 LA_DATAN2
LA_DATAN_0
LA_DATAN_1
LA_DATAN_2
21 LA_DATAP0
21 LA_DATAP1
21 LA_DATAP2
LA_DATAP_0
LA_DATAP_1
LA_DATAP_2
LB_DATAN_0
LB_DATAN_1
LB_DATAN_2
LB_DATAP_0
LB_DATAP_1
LB_DATAP_2
TV
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
R222
0Ohm
+1.5VS
TV_DCONSEL0
TV_DCONSEL1
T255
T259
LBKLT_EN
LVDD_EN
CRT_IREF
R85
100KOhm
R121
100KOhm
R221
255Ohm
1%
20 CRT_HSYNC
20 CRT_VSYNC
CRT_HSYNC
CRT_VSYNC
R220
R219
22Ohm
22Ohm
NB_HSYNC
NB_VSYNC
Clocse to GMCH
945GMS
<Core Design>
ASUSTeK COMPUTER INC.
Title : NB-945GMS(GRAPHIC)
Engineer: Satan_He
Size A4
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 9 of 50



<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(DDR2)	
	Engineer: Satan He	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 10 of 50	



<Core Design>

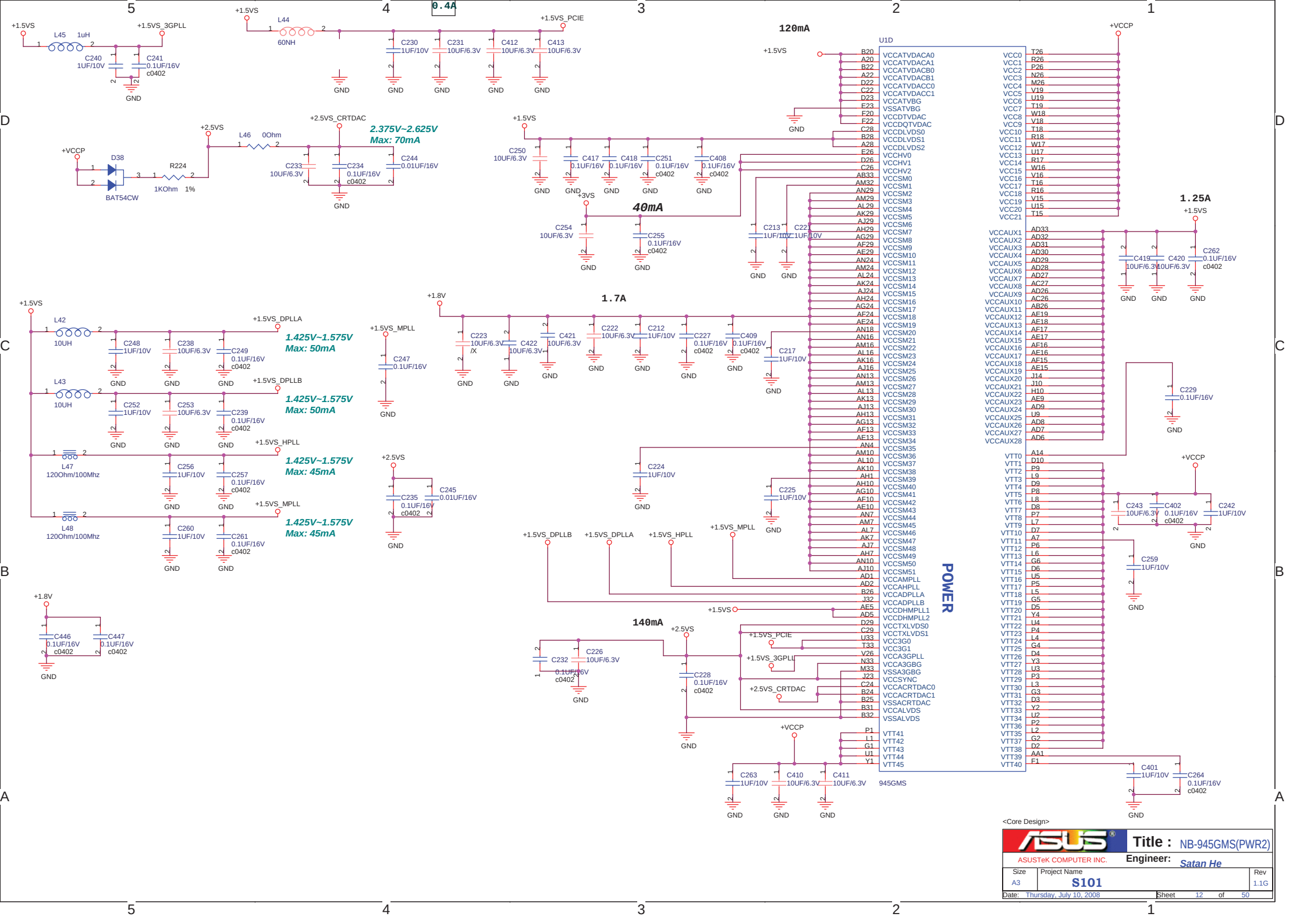
ASUSTeK COMPUTER INC.

Title : NB-945GMs(PWR)

Engineer: Satan_He

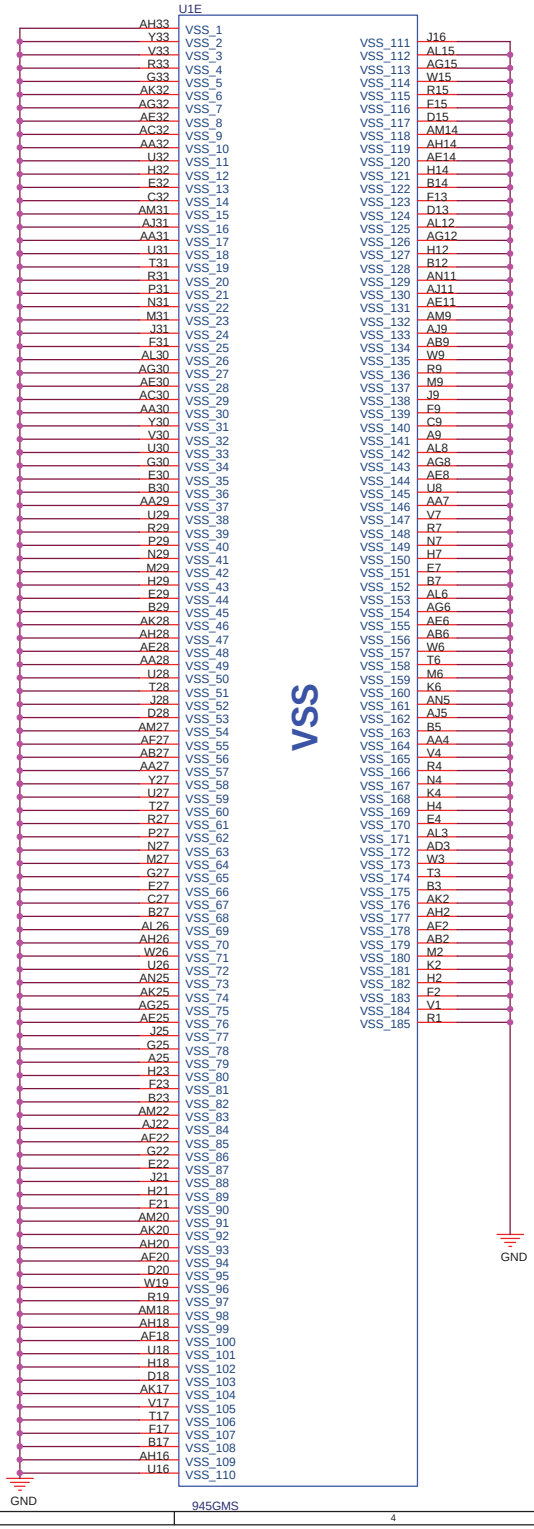
Size	Project Name	Rev
A3	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 11 of 50



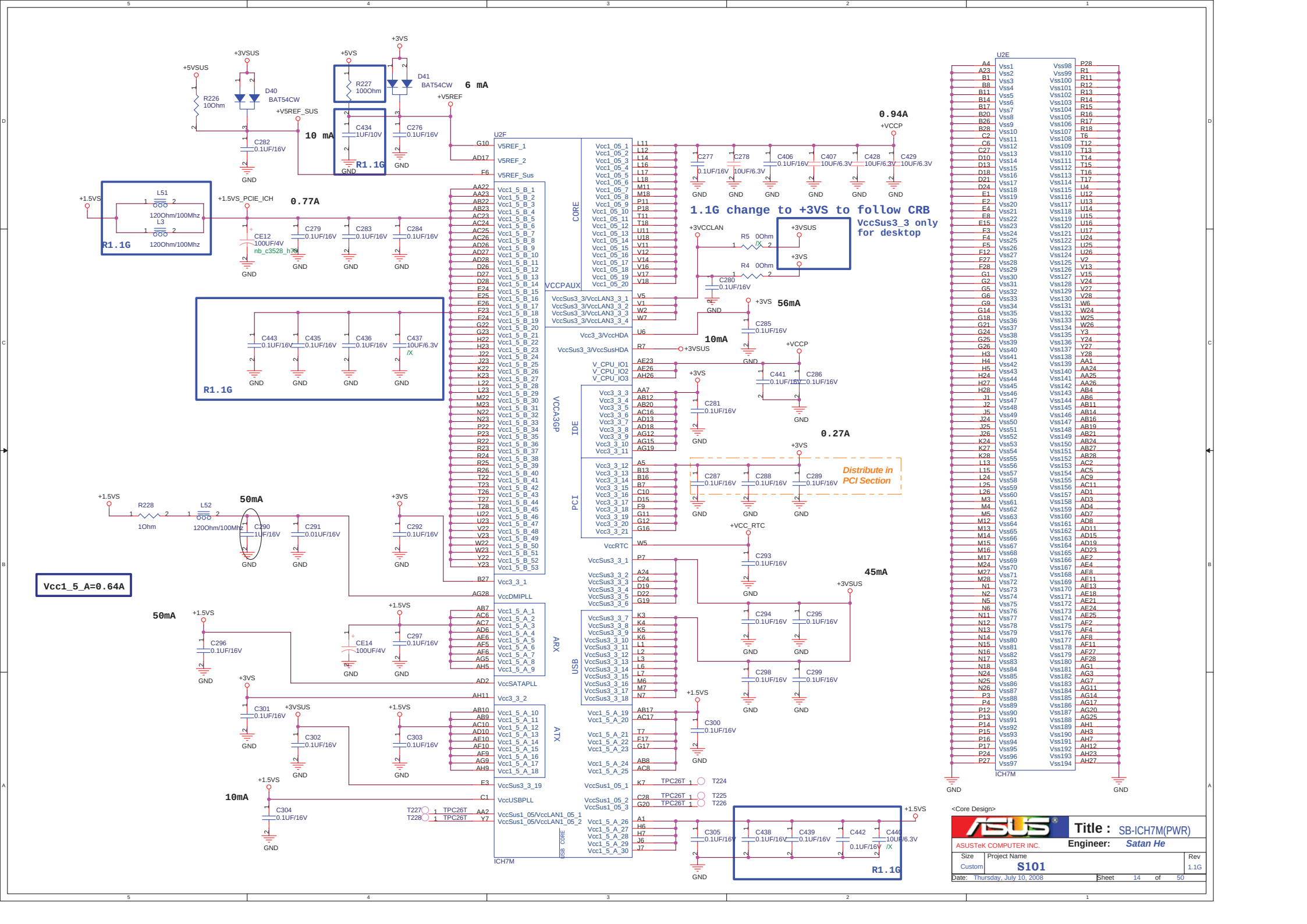
<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(PWR2)	
	Engineer: Satan He	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 12 of 50	



<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945PMS(GND)	
	Engineer: Satan_He	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 13 of 50	


+3VSUS
+5VSUS
+5VS
+3VS
+V5REF
+V5REF_SUS
R226 10Ohm
D40 BAT54CW
R227 100Ohm
D41 BAT54CW
6 mA
10 mA
C282 0.1UF/16V
C434 1UF/10V
C276 0.1UF/16V
R1.1G
GND
U2F
V5REF_1
V5REF_2
V5REF_Sus
+1.5VS
L51 120Ohm/100Mhz
L3 120Ohm/100Mhz
+1.5VS_PCIE_ICH
0.77A
CE12 100UF/4V nb_c3528_h7
C279 0.1UF/16V
C283 0.1UF/16V
C284 0.1UF/16V
Vcc1_5_B_1
Vcc1_5_B_2
Vcc1_5_B_3
Vcc1_5_B_4
Vcc1_5_B_5
Vcc1_5_B_6
Vcc1_5_B_7
Vcc1_5_B_8
Vcc1_5_B_9
Vcc1_5_B_10
Vcc1_5_B_11
Vcc1_5_B_12
Vcc1_5_B_13
Vcc1_5_B_14
Vcc1_5_B_15
Vcc1_5_B_16
Vcc1_5_B_17
Vcc1_5_B_18
Vcc1_5_B_19
Vcc1_5_B_20
Vcc1_5_B_21
Vcc1_5_B_22
Vcc1_5_B_23
Vcc1_5_B_24
Vcc1_5_B_25
Vcc1_5_B_26
Vcc1_5_B_27
Vcc1_5_B_28
Vcc1_5_B_29
Vcc1_5_B_30
Vcc1_5_B_31
Vcc1_5_B_32
Vcc1_5_B_33
Vcc1_5_B_34
Vcc1_5_B_35
Vcc1_5_B_36
Vcc1_5_B_37
Vcc1_5_B_38
Vcc1_5_B_39
Vcc1_5_B_40
Vcc1_5_B_41
Vcc1_5_B_42
Vcc1_5_B_43
Vcc1_5_B_44
Vcc1_5_B_45
Vcc1_5_B_46
Vcc1_5_B_47
Vcc1_5_B_48
Vcc1_5_B_49
Vcc1_5_B_50
Vcc1_5_B_51
Vcc1_5_B_52
Vcc1_5_B_53
CORE
C443 0.1UF/16V
C435 0.1UF/16V
C436 0.1UF/16V
C437 10UF/6.3V /X
R1.1G
VCCA3GP
IDE
PCI
ARX
USB
ATX
Vcc3_3_1
VccDMIPLL
VccSATAPLL
Vcc3_3_2
VccSus3_3_19
VccUSBPLL
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
ICH7M
+1.5VS
R228 1Ohm
L52 120Ohm/100Mhz
50mA
C290 1UF/16V
C291 0.01UF/16V
C292 0.1UF/16V
Vcc1_5_A=0.64A
C296 0.1UF/16V
CE14 100UF/4V
C297 0.1UF/16V
C301 0.1UF/16V
C302 0.1UF/16V
C303 0.1UF/16V
10mA
C304 0.1UF/16V
T227 TPC26T
T228 TPC26T
Vcc1_5_A_1
Vcc1_5_A_2
Vcc1_5_A_3
Vcc1_5_A_4
Vcc1_5_A_5
Vcc1_5_A_6
Vcc1_5_A_7
Vcc1_5_A_8
Vcc1_5_A_9
Vcc1_5_A_10
Vcc1_5_A_11
Vcc1_5_A_12
Vcc1_5_A_13
Vcc1_5_A_14
Vcc1_5_A_15
Vcc1_5_A_16
Vcc1_5_A_17
Vcc1_5_A_18
USB_CORE
VCCPAUX
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
VccRTC
VccSus3_3_1
VccSus3_3_2
VccSus3_3_3
VccSus3_3_4
VccSus3_3_5
VccSus3_3_6
VccSus3_3_7
VccSus3_3_8
VccSus3_3_9
VccSus3_3_10
VccSus3_3_11
VccSus3_3_12
VccSus3_3_13
VccSus3_3_14
VccSus3_3_15
VccSus3_3_16
VccSus3_3_17
VccSus3_3_18
Vcc1_5_A_19
Vcc1_5_A_20
Vcc1_5_A_21
Vcc1_5_A_22
Vcc1_5_A_23
Vcc1_5_A_24
Vcc1_5_A_25
VccSus1_05_1
VccSus1_05_2
VccSus1_05_3
Vcc1_5_A_26
Vcc1_5_A_27
Vcc1_5_A_28
Vcc1_5_A_29
Vcc1_5_A_30
T224
T225
T226
0.94A
+VCCP
C277 0.1UF/16V
C278 10UF/6.3V
C406 0.1UF/16V
C407 10UF/6.3V
C428 10UF/6.3V
C429 10UF/6.3V
1.1G change to +3VS to follow CRB
VccSus3_3 only for desktop
+3VCCLAN
R5 0Ohm /X
R4 0Ohm
C280 0.1UF/16V
56mA
C285 0.1UF/16V
10mA
C441 0.1UF/16V
C286 0.1UF/16V
0.27A
Distribute in PCI Section
C287 0.1UF/16V
C288 0.1UF/16V
C289 0.1UF/16V
+VCC_RTC
C293 0.1UF/16V
45mA
C294 0.1UF/16V
C295 0.1UF/16V
C298 0.1UF/16V
C299 0.1UF/16V
C300 0.1UF/16V
C305 0.1UF/16V
C438 0.1UF/16V
C439 0.1UF/16V
C442 0.1UF/16V
C440 10UF/6.3V /X
R1.1G
U2E
ICH7M
<Core Design>
ASUSTeK COMPUTER INC.
Title : SB-ICH7M(PWR)
Engineer: Satan He
Size Custom
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 14 of 50

Change to rechargeable RTC battery

Height : 3.4 mm

R1.1G change +3VA net to +3VA_AEC

RTCRST# RC delay 18~25ms

Place Near Open Door

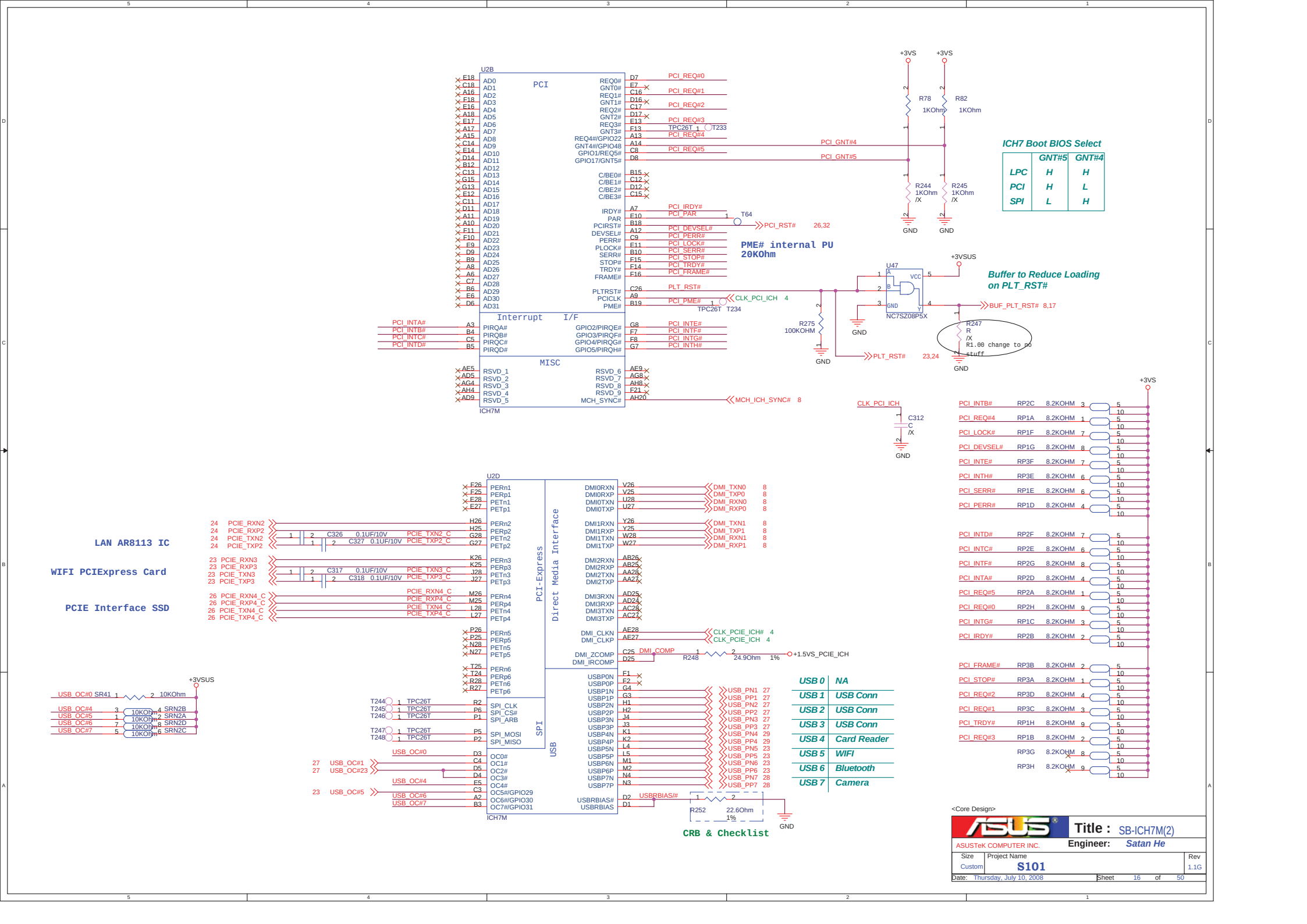
Over Discharge Protection Circuit

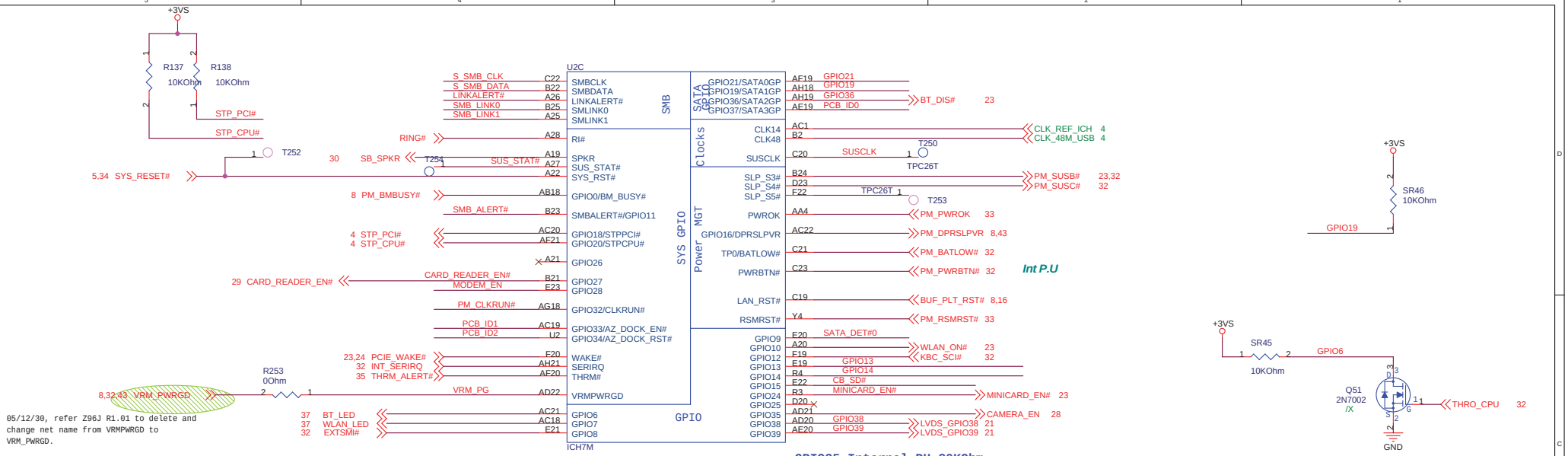
ACZ_SDIN0	CODEC
ACZ_SDIN1	NA

NO STUFF R107.CPUSLP# ONLY USE IN DESTOP

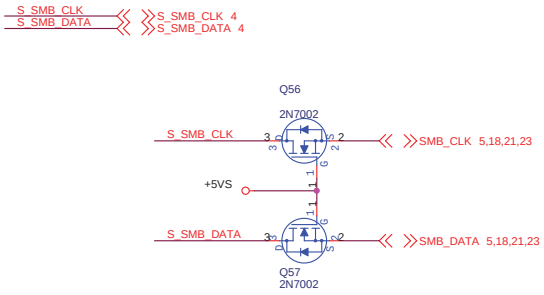
<Core Design>

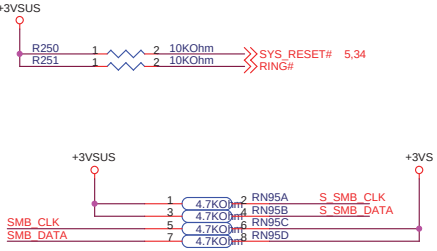
ASUSTeK COMPUTER INC.	Title : SB-ICH7-M(1)	
	Engineer: Satan He	
Size: Custom	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 15 of 50	

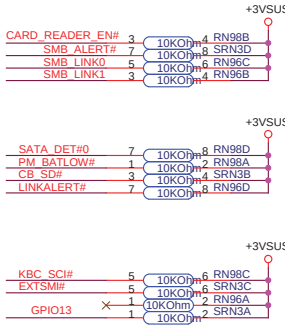

U2B
PCI
Interrupt I/F
MISC
ICH7M
PME# internal PU 20KOhm
Buffer to Reduce Loading on PLT_RST#
NC7SZ08P5X
R247 R /X R1.00 change to no stuff
ICH7 Boot BIOS Select
LPC H H
PCI H L
SPI L H
LAN AR8113 IC
WIFI PCIExpress Card
PCIE Interface SSD
U2D
PCI-Express
Direct Media Interface
USB
SPI
ICH7M
USB 0 NA
USB 1 USB Conn
USB 2 USB Conn
USB 3 USB Conn
USB 4 Card Reader
USB 5 WIFI
USB 6 Bluetooth
USB 7 Camera
CRB & Checklist
<Core Design>
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Satan He
Size Custom
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 16 of 50

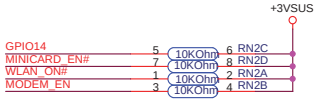


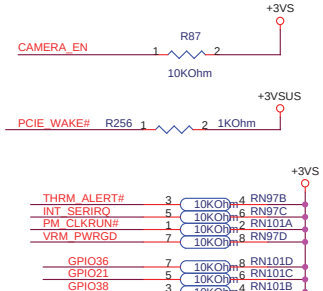
WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x

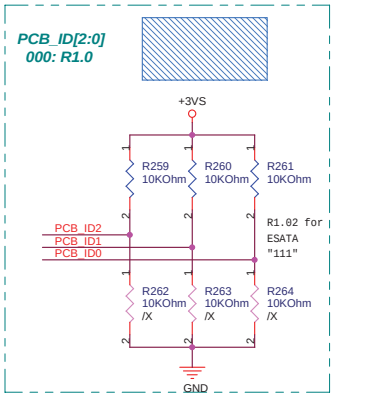












PCB_VID3 : PROJECT CODE

<Core Design>

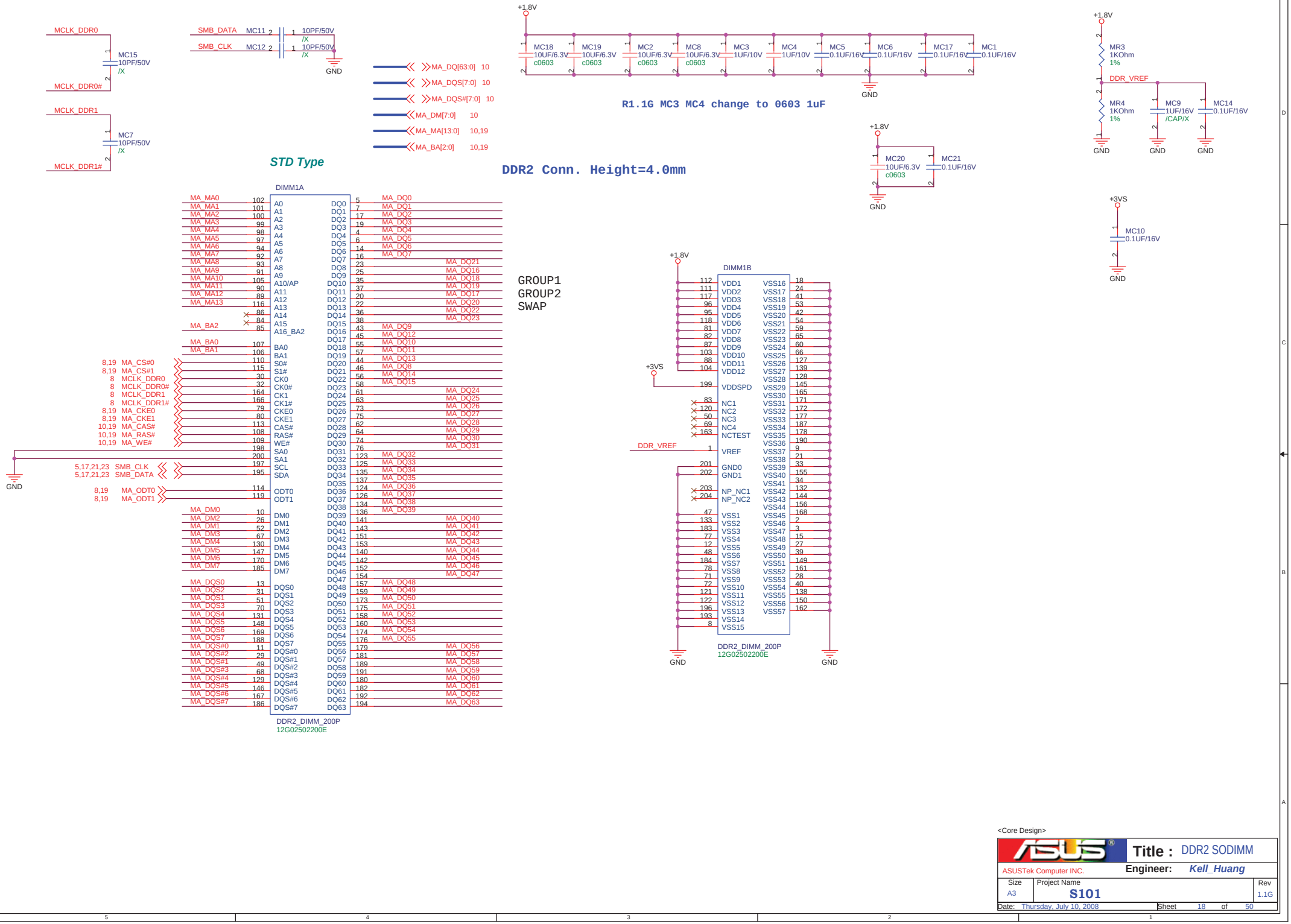
ASUSTeK COMPUTER INC

Title : SB-ICH7M(3)

Engineer: Satan He

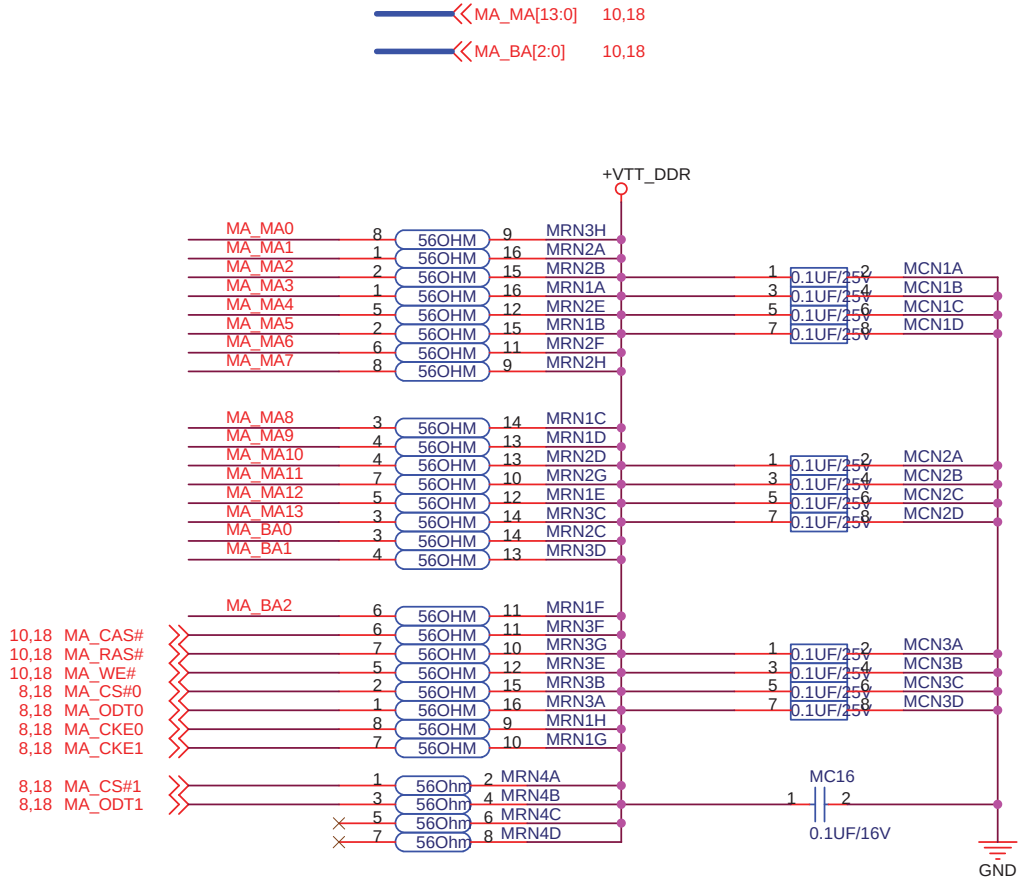
Size	Project Name	Rev
Custom	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 17 of 50



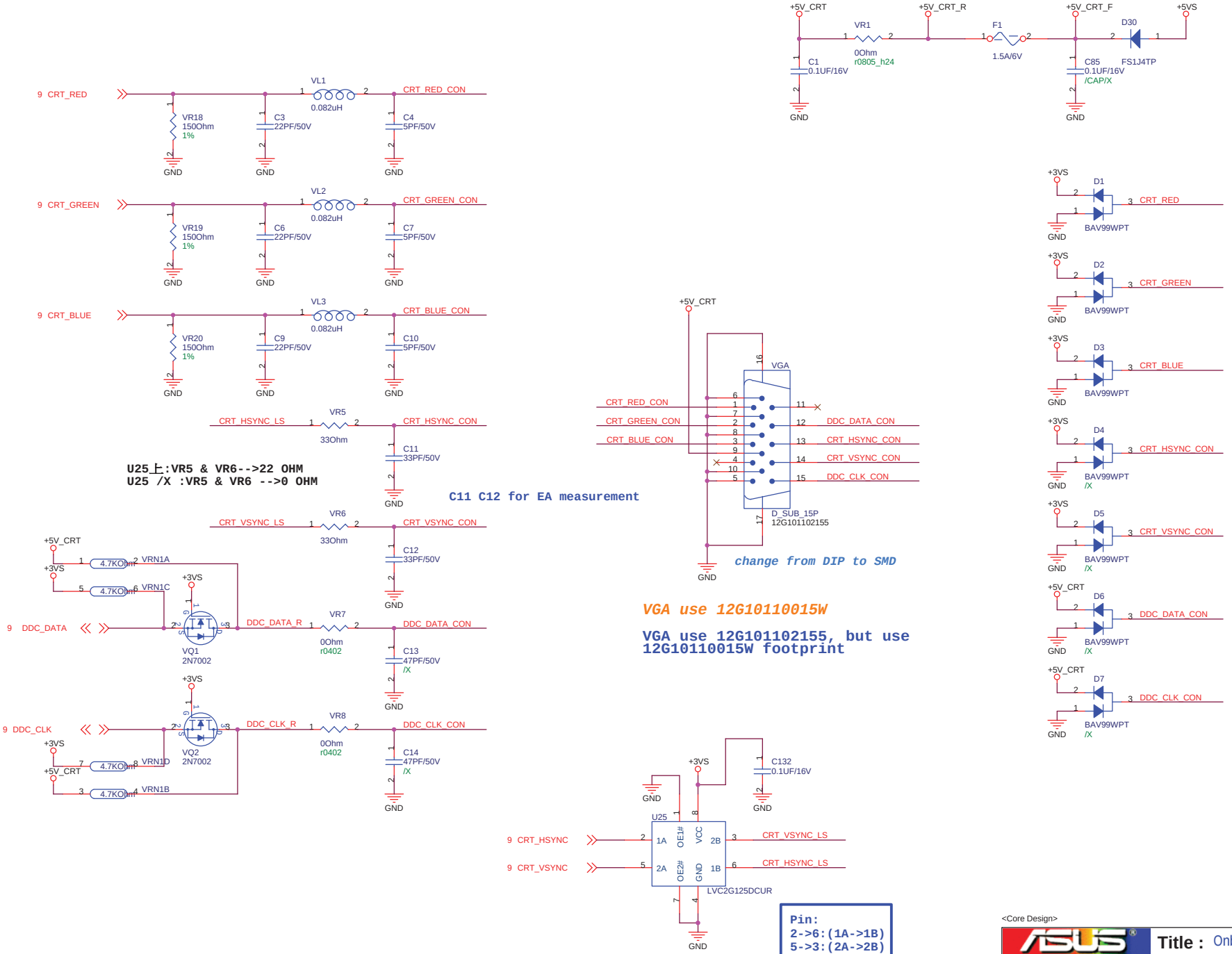
<Core Design>

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 18 of 50	



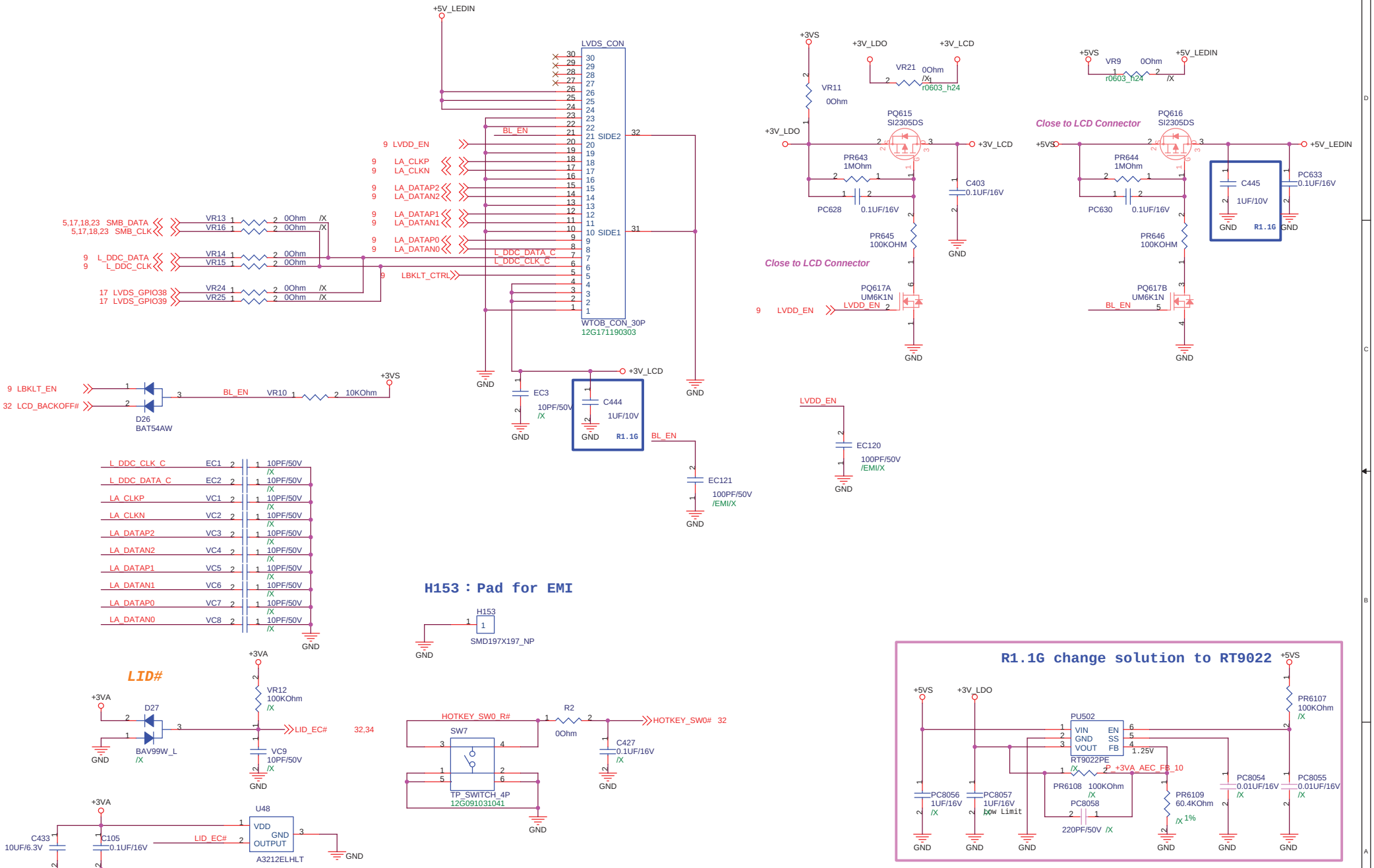
<Core Design>

ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: Kell_Huang	
Size: A4	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 19 of 50	



<Core Design>

ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 20 of 50	

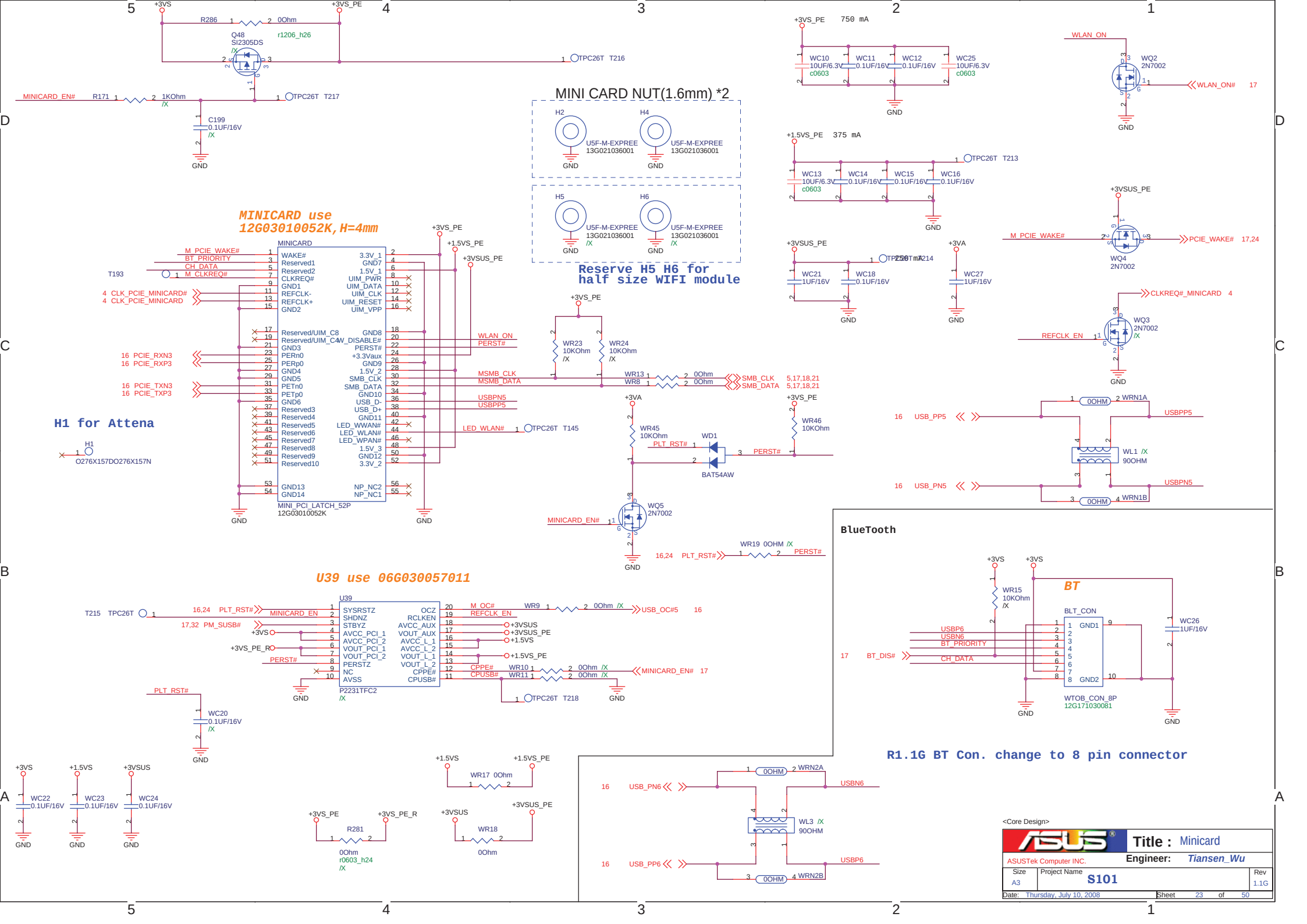


<Core Design>

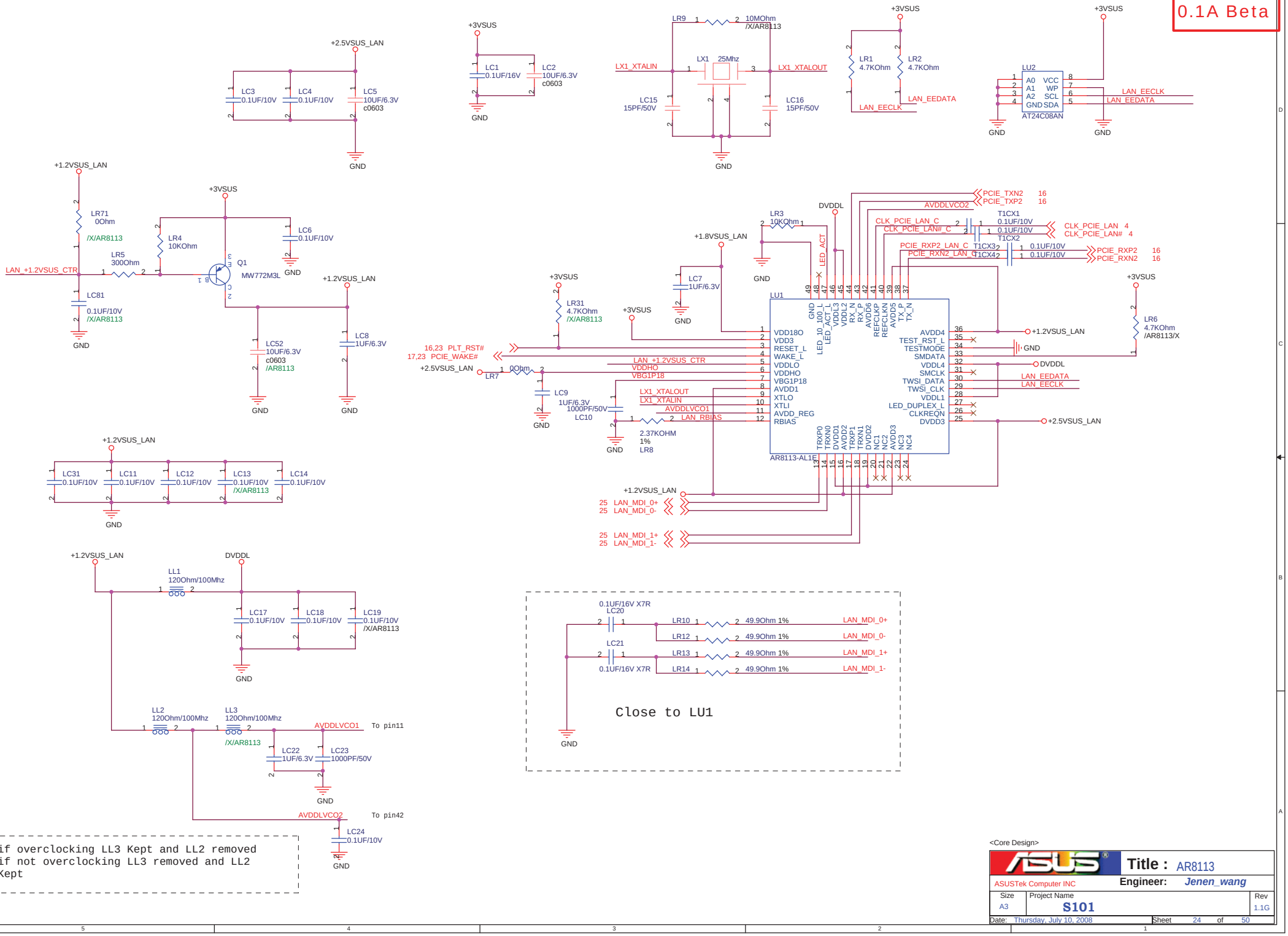
ASUSTek Computer INC.	Title : LVDS Conn_LID	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 21 of 50	

<Core Design>

ASUSTek Computer INC.	Title : Blank	
	Engineer: *Kell_Huang*	
Size: A3	Project Name: **S101**	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 22 of 50	


MINI CARD NUT(1.6mm) *2
MINICARD use 12G03010052K,H=4mm
Reserve H5 H6 for half size WIFI module
H1 for Attena
U39 use 06G030057011
BlueTooth
BT
R1.1G BT Con. change to 8 pin connector
MINICARD
MINI_PCI_LATCH_52P
12G03010052K
P2231TFC2
WTOB_CON_8P
12G171030081
<Core Design>
Title : Minicard
ASUSTek Computer INC.
Engineer: Tiansen_Wu
Project Name S101
Size A3
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 23 of 50

0.1A Beta



<Core Design>

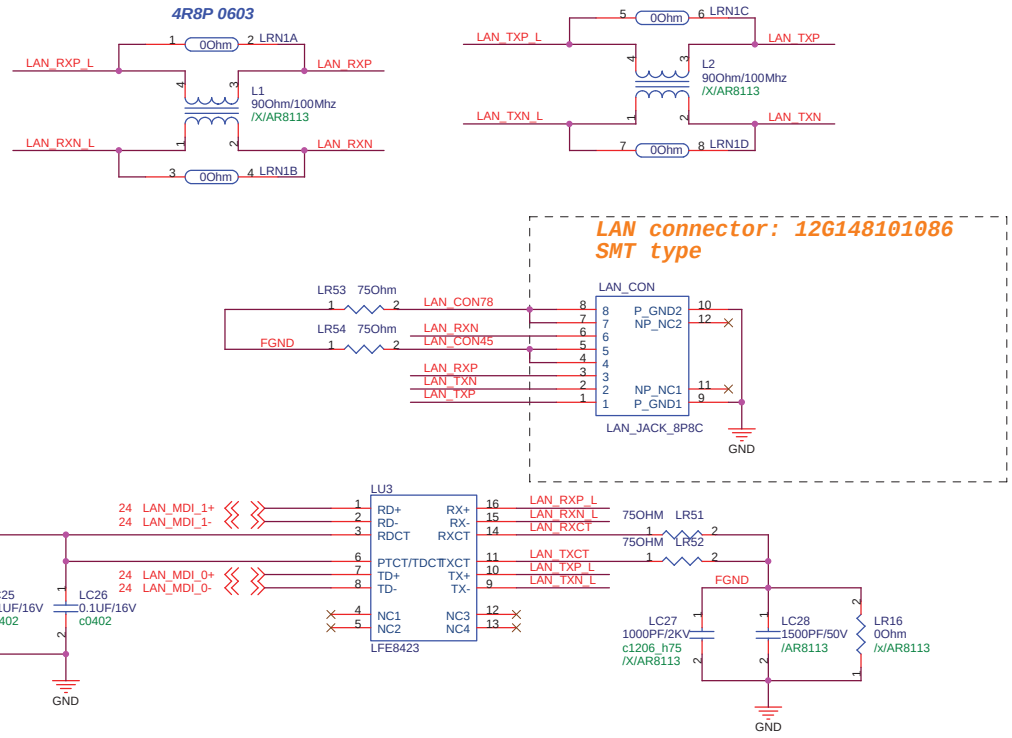
Title : AR8113

ASUSTek Computer INC

Engineer: Jenen_wang

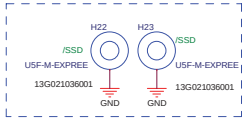
Size	Project Name	Rev
A3	S101	1.1G

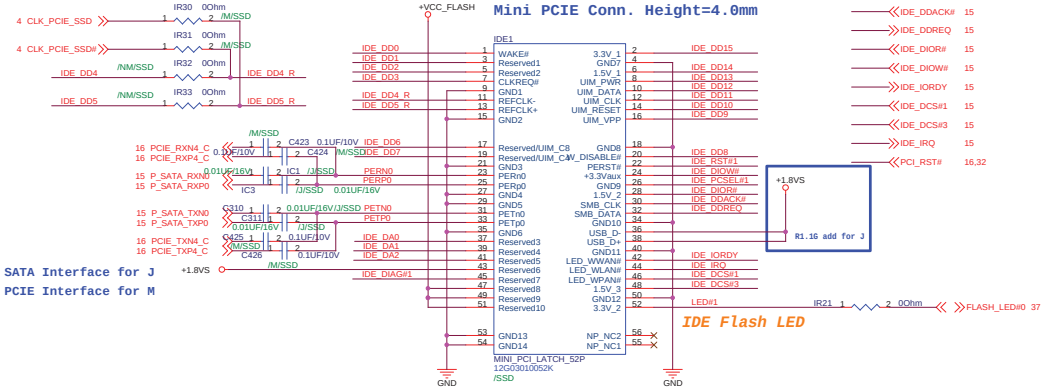
Date: Thursday, July 10, 2008 Sheet 24 of 50

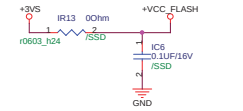


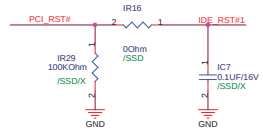
<Core Design>

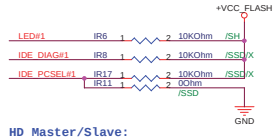
ASUSTek Computer INC.	Title : RJ45	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 25 of 50	









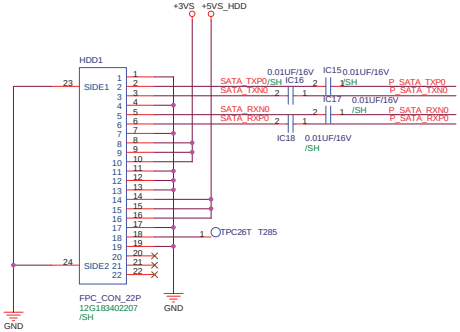


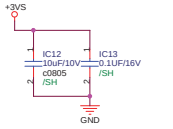
HD Master/Slave:
Master:Low
Slave :NC or
High

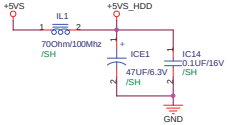
SATA HDD Connector

FPC Connector with Mylar

/SH for SATA HDD



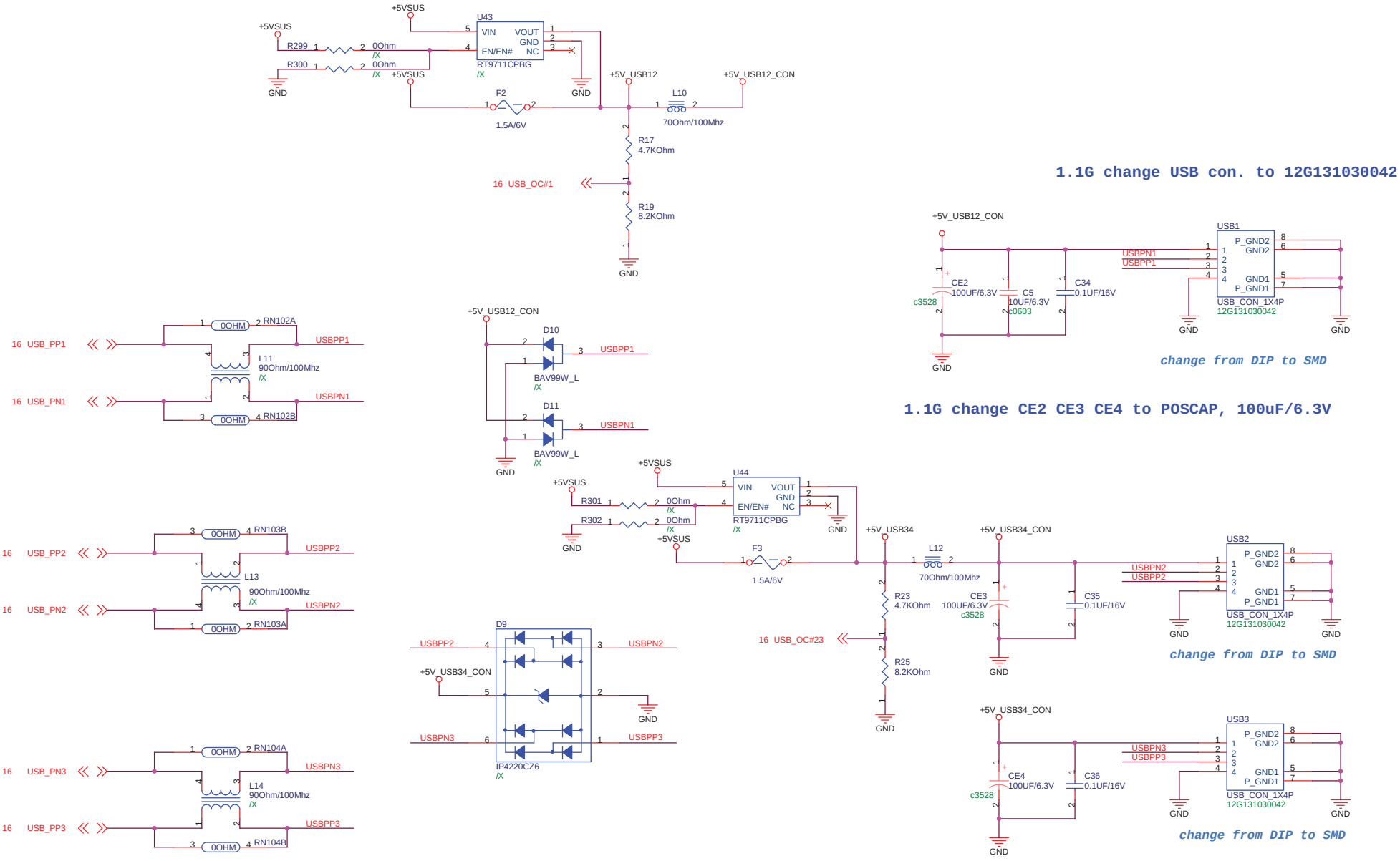




Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?

<Core Design>

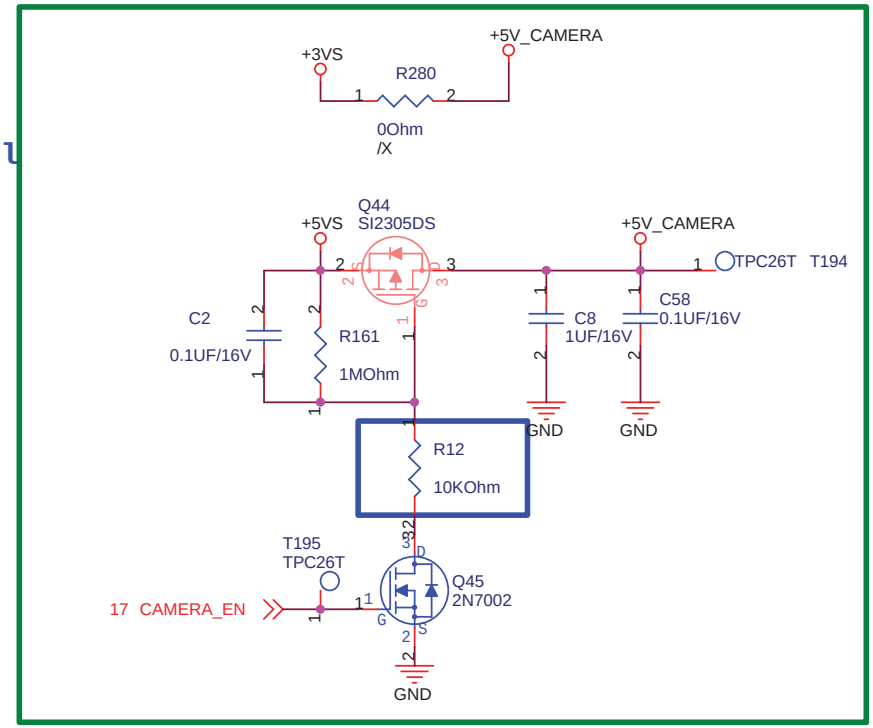
ASUSTek Computer INC.	Title : HD + Flash Conn	
	Engineer: Kell_Huang	
Size: A2	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 26 of 50	

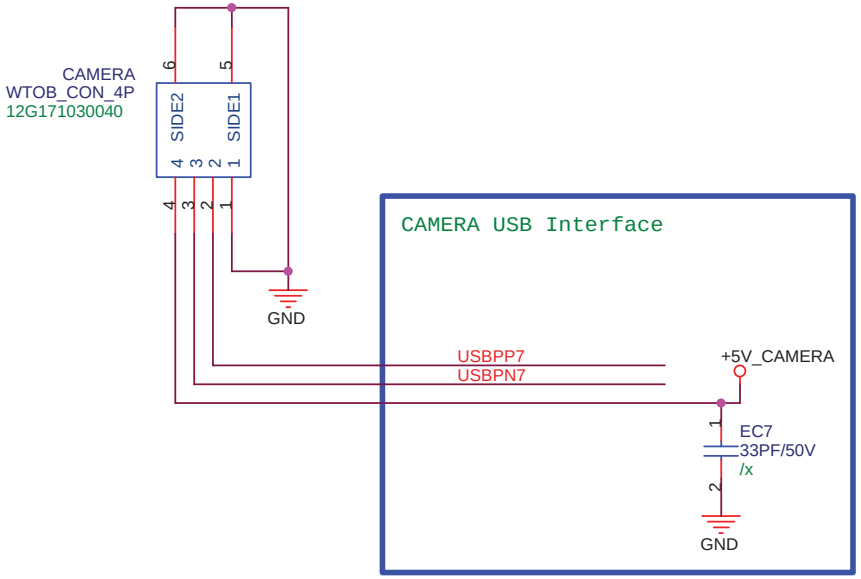


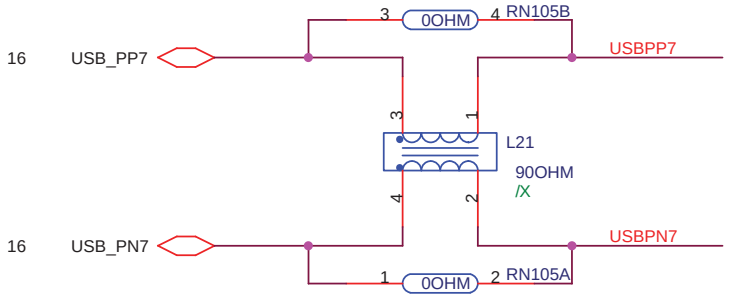
<Core Design>

ASUSTek Computer INC.	Title : USB Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 27 of 50	

Power Control

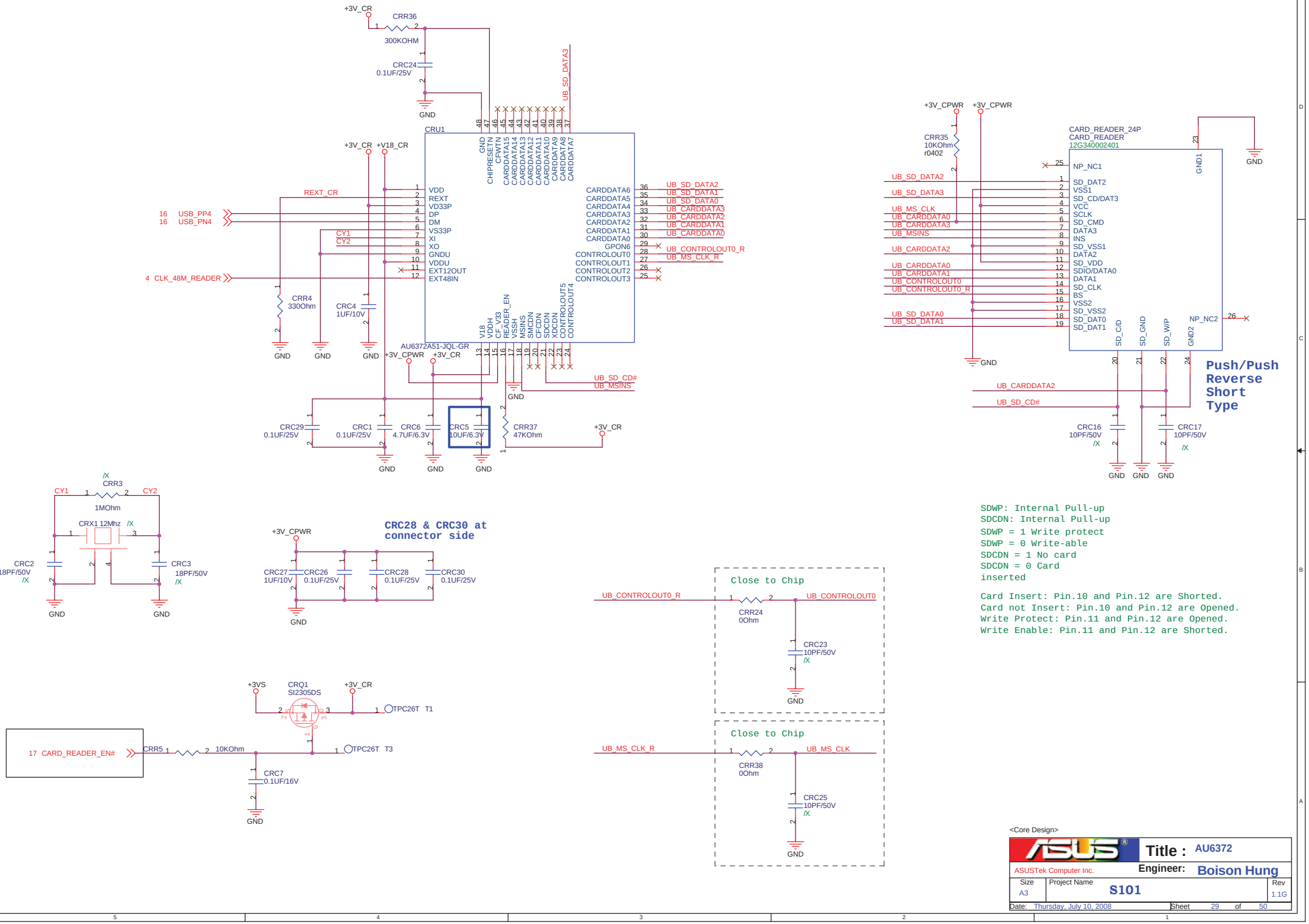


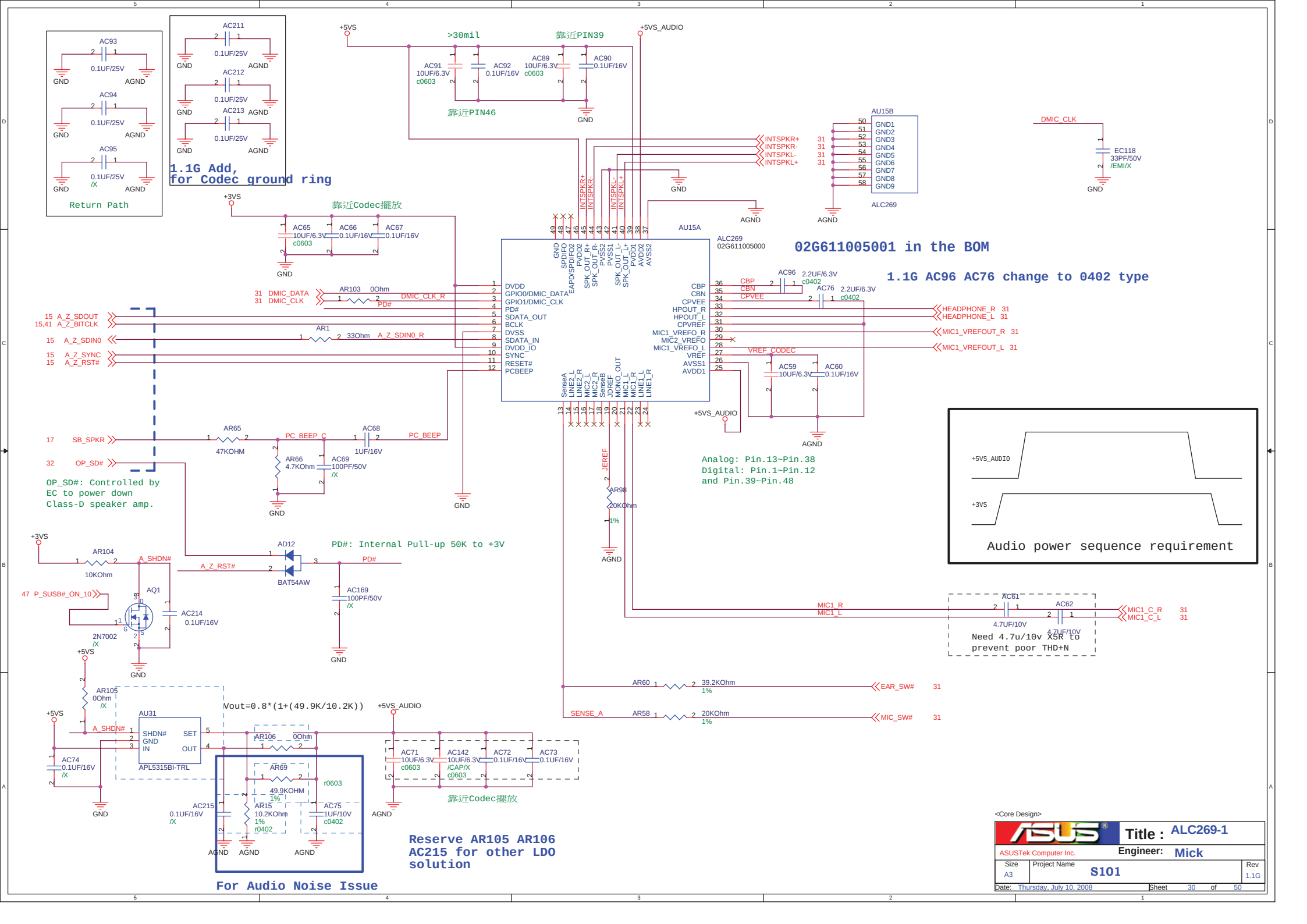




<Core Design>

ASUSTek Computer INC.	Title : Camera Power	
	Engineer: Kell_Huang	
Size: A4	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 28 of 50	


+3V_CR
CRR36
300KOHM
CRC24
0.1UF/25V
GND
UB_SD_DATA3
CRU1
+3V_CR +V18_CR
REXT_CR
16 USB_PP4
16 USB_PN4
CY1
CY2
4 CLK_48M_READER
CRR4
330Ohm
CRC4
1UF/10V
GND
GND
GND
AU6372A51-JQL-GR
+3V_CPWR
+3V_CR
CRC29
0.1UF/25V
CRC1
0.1UF/25V
CRC6
4.7UF/6.3V
CRC5
10UF/6.3V
CRR37
47KOhm
+3V_CR
GND
GND
GND
UB_SD_CD#
UB_MSINS
GND
CARDDATA6
CARDDATA5
CARDDATA4
CARDDATA3
CARDDATA2
CARDDATA1
CARDDATA0
GPON6
CONTROLOUT0
CONTROLOUT1
CONTROLOUT2
CONTROLOUT3
UB_SD_DATA2
UB_SD_DATA1
UB_SD_DATA0
UB_CARDDATA3
UB_CARDDATA2
UB_CARDDATA1
UB_CARDDATA0
UB_CONTROLOUT0_R
UB_MS_CLK_R
+3V_CPWR
+3V_CPWR
CRR35
10KOhm
r0402
CARD_READER_24P
CARD_READER
12G340002401
NP_NC1
SD_DAT2
VSS1
SD_CD/DAT3
VCC
SCLK
SD_CMD
DATA3
INS
SD_VSS1
DATA2
SD_VDD
SDIO/DATA0
DATA1
SD_CLK
BS
VSS2
SD_VSS2
SD_DAT0
SD_DAT1
NP_NC2
GND1
GND2
SD_C/D
SD_GND
SD_W/P
GND
UB_SD_DATA2
UB_SD_DATA3
UB_MS_CLK
UB_CARDDATA0
UB_CARDDATA3
UB_MSINS
UB_CARDDATA2
UB_CARDDATA0
UB_CARDDATA1
UB_CONTROLOUT0
UB_CONTROLOUT0_R
UB_SD_DATA0
UB_SD_DATA1
UB_CARDDATA2
UB_SD_CD#
CRC16
10PF/50V
/X
CRC17
10PF/50V
/X
GND
GND
GND
Push/Push
Reverse
Short
Type
/X
CRR3
CY1
CY2
1MOhm
CRX1 12Mhz /X
CRC2
18PF/50V
/X
CRC3
18PF/50V
/X
GND
GND
+3V_CPWR
CRC27
1UF/10V
CRC26
0.1UF/25V
CRC28
0.1UF/25V
CRC30
0.1UF/25V
GND
CRC28 & CRC30 at
connector side
SDWP: Internal Pull-up
SDCDN: Internal Pull-up
SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card
inserted
Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.
+3VS
CRQ1
SI2305DS
+3V_CR
TPC26T T1
17 CARD_READER_EN#
CRR5
10KOhm
TPC26T T3
CRC7
0.1UF/16V
GND
UB_CONTROLOUT0_R
Close to Chip
CRR24
0Ohm
UB_CONTROLOUT0
CRC23
10PF/50V
/X
GND
UB_MS_CLK_R
Close to Chip
CRR38
0Ohm
UB_MS_CLK
CRC25
10PF/50V
/X
GND
<Core Design>
Title : AU6372
ASUSTek Computer Inc.
Engineer: Boison Hung
Size A3
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 29 of 50

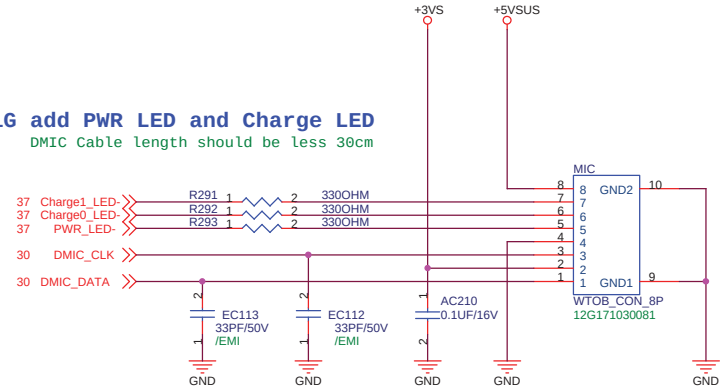


<Core Design>
ASUSTek Computer Inc.
Engineer: Mick

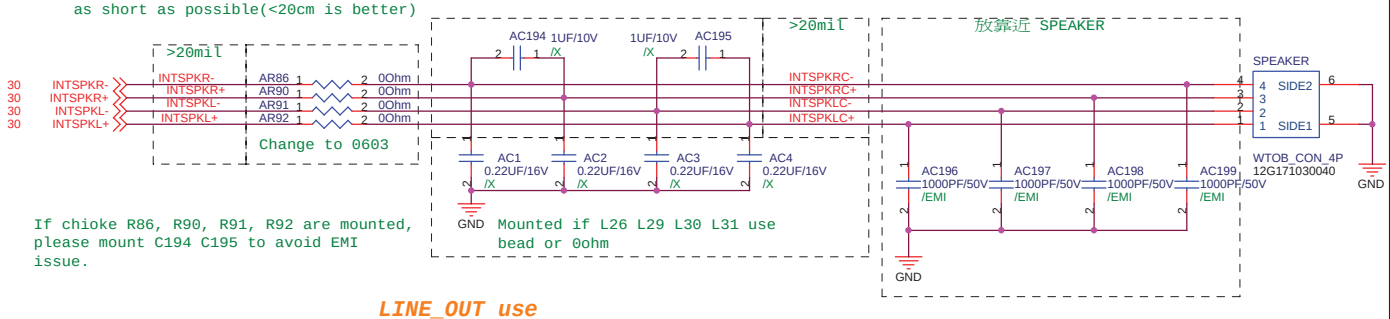
Title : ALC269-1		
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 30 of 50	

1.1G add PWR LED and Charge LED

DMIC Cable length should be less 30cm



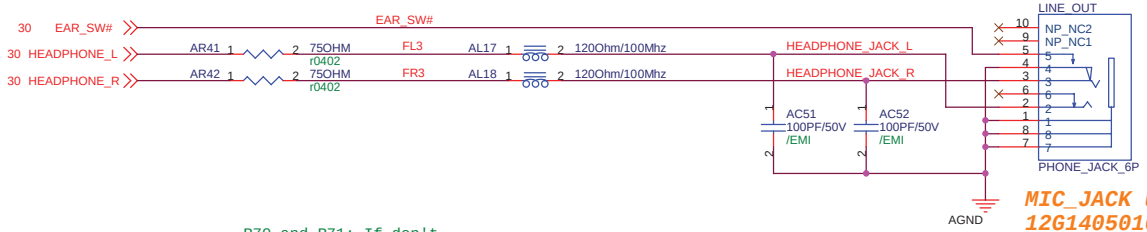
Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)



If chioke R86, R90, R91, R92 are mounted, please mount C194 C195 to avoid EMI issue.

Mounted if L26 L29 L30 L31 use bead or 0ohm

LINE_OUT use 12G14050106P(SINGATRON) Black

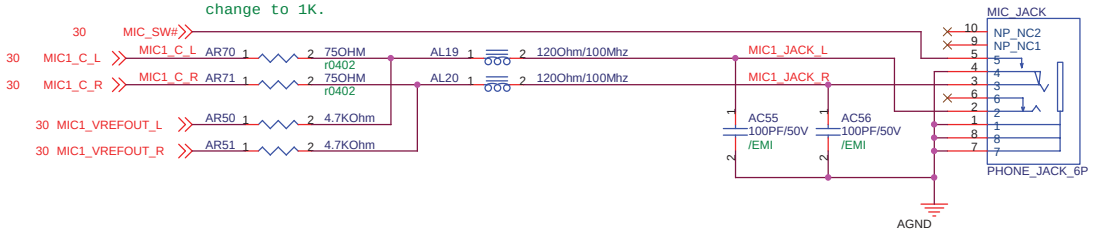


1.1G Change audio con. to black

change from DIP to SMD

MIC_JACK use 12G14050106P(SINGATRON) Black

R70 and R71: If don't need retasking function, change to 1K.

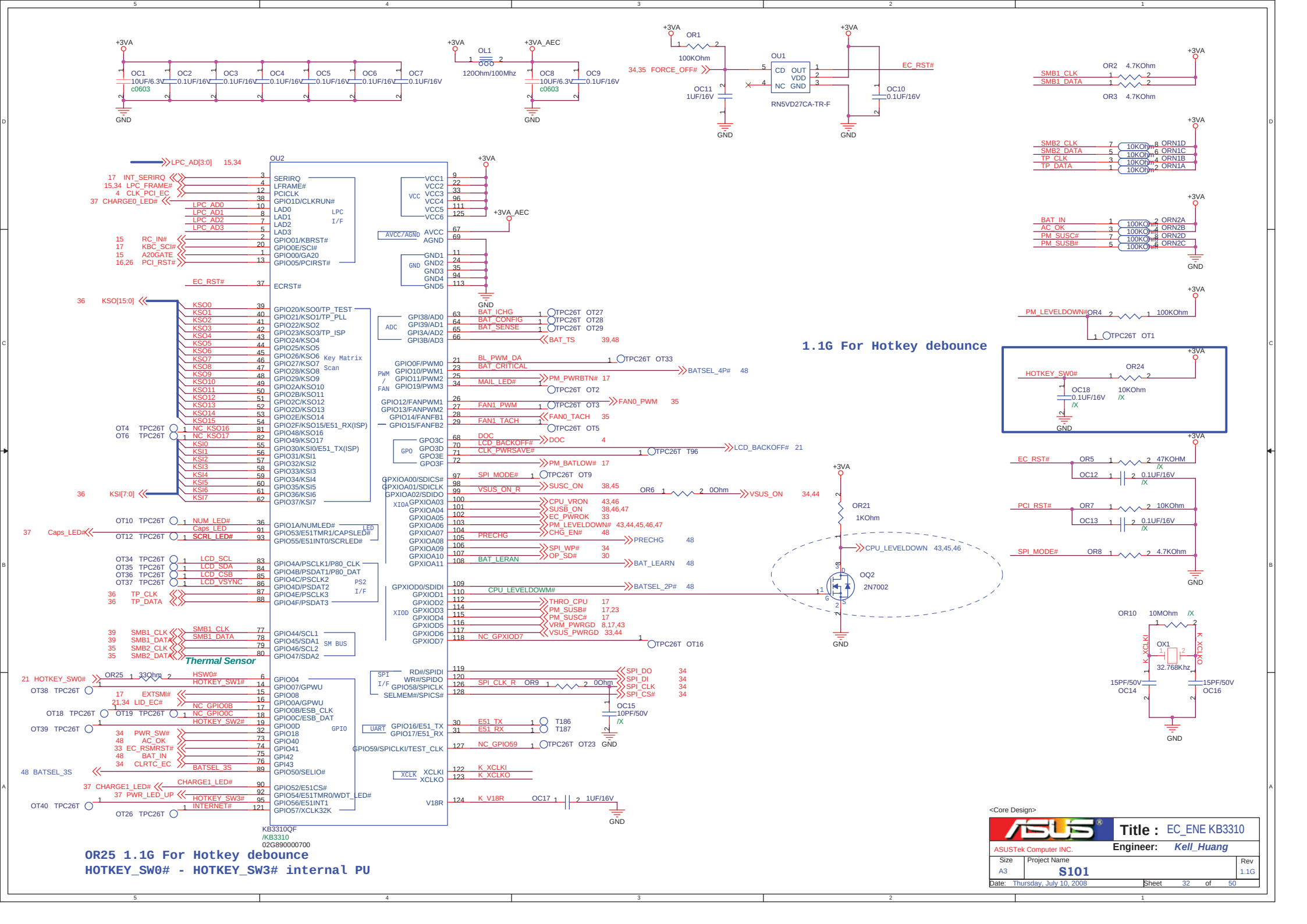


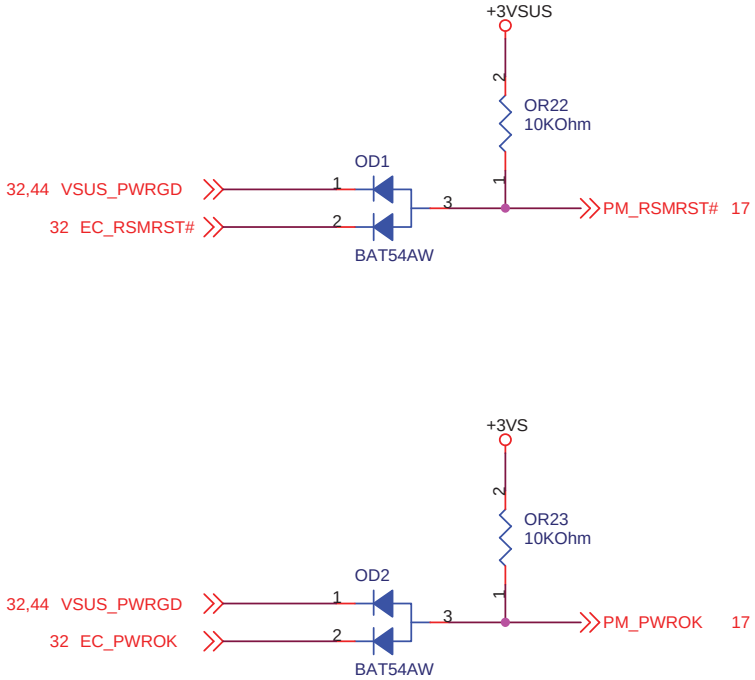
1.1G Change audio con. to black

change from DIP to SMD

<Core Design>

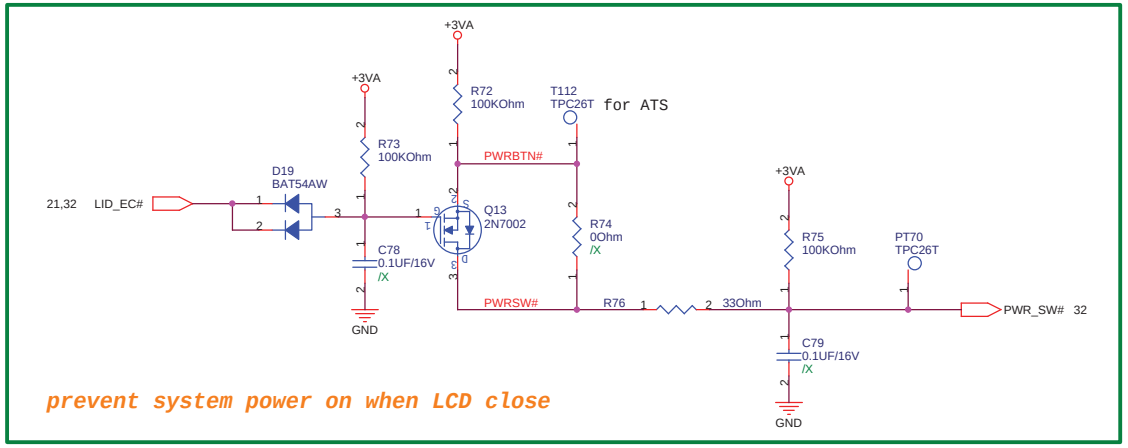
ASUSTek Computer Inc.	Title : ALC269-2	
	Engineer: MICK	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 31 of 50	

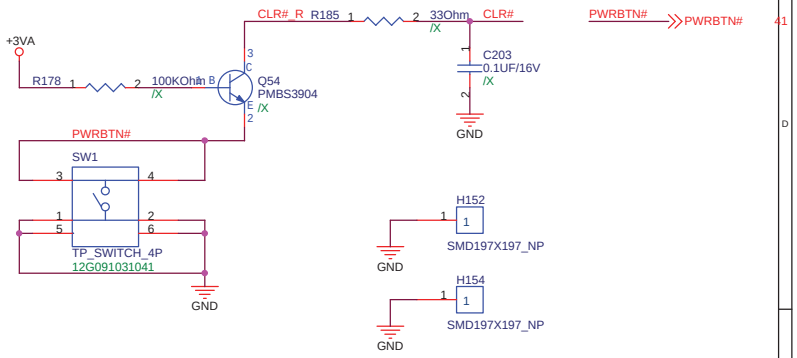

OU2
KB3310QF
/KB3310
02G890000700
1.1G For Hotkey debounce
OR25 1.1G For Hotkey debounce
HOTKEY_SW0# - HOTKEY_SW3# internal PU
Thermal Sensor
<Core Design>
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: Kell_Huang
Size A3
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 32 of 50

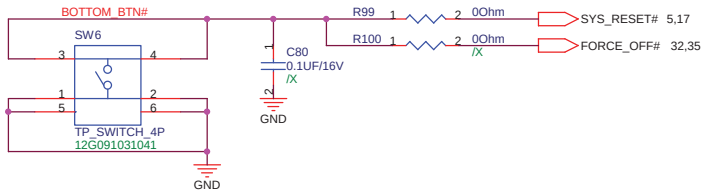


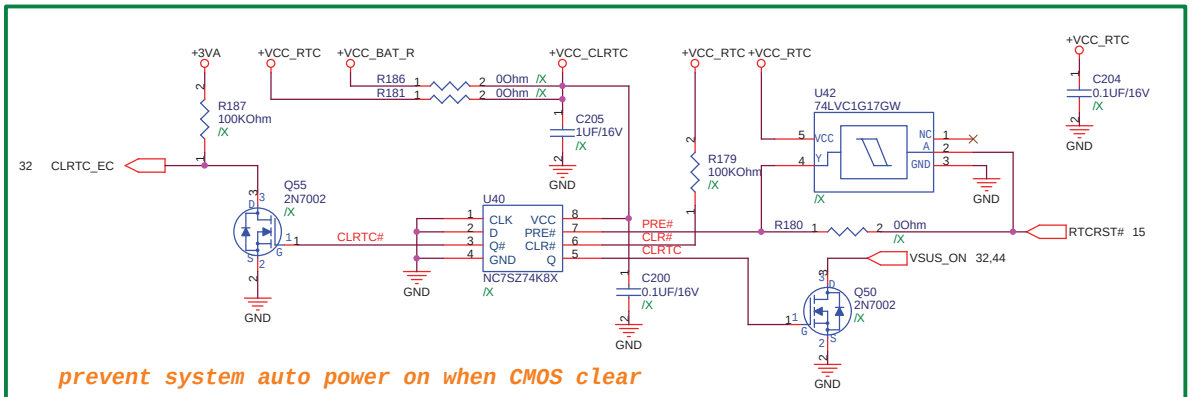
<Core Design>

ASUSTek Computer INC.	Title : EC_UART_KC3820	
	Engineer: Kell_Huang	
Size: A4	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 33 of 50	

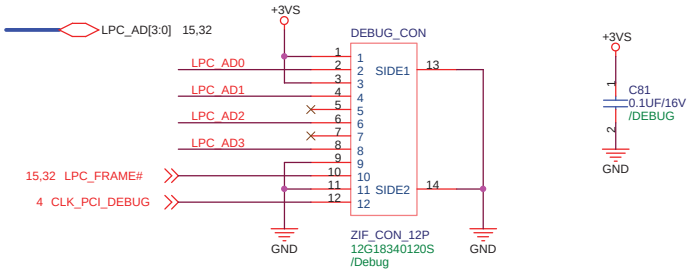




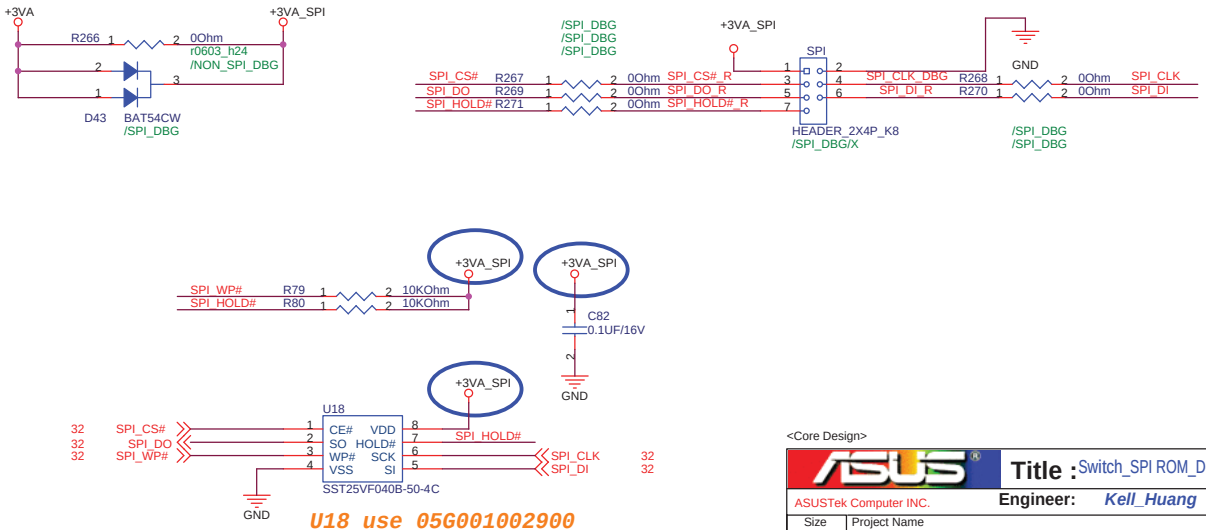




For Debug

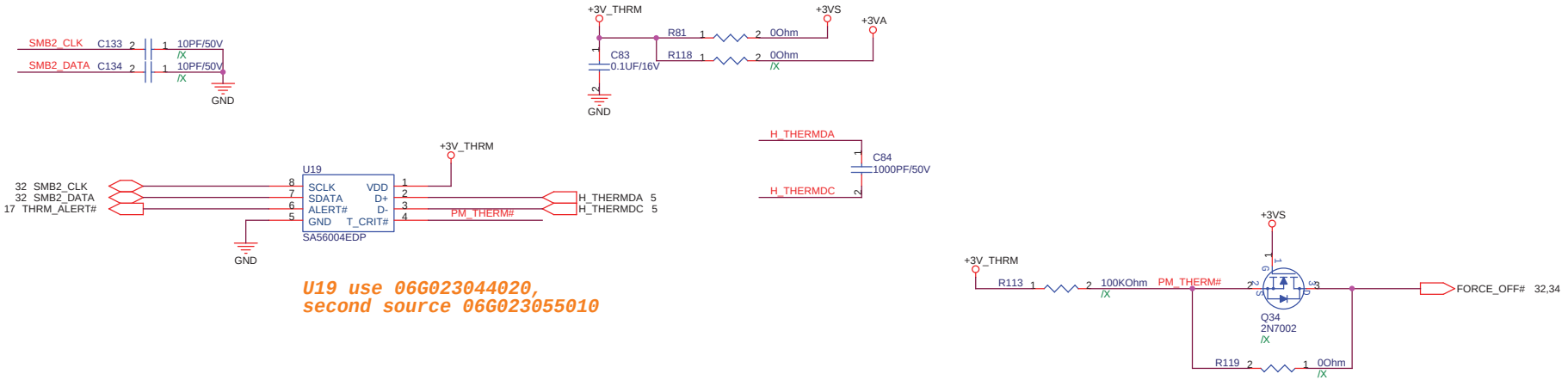


Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125

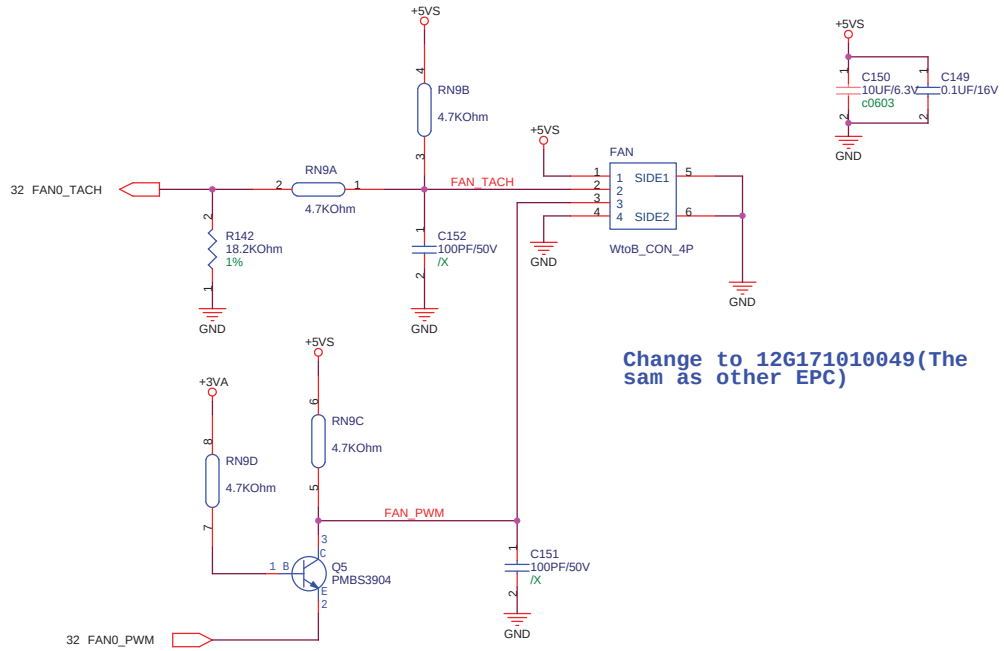


<Core Design>
ASUSTek Computer INC.
Engineer: Kell_Huang

Title : Switch_SPI ROM_Debug		
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 34 of 50	



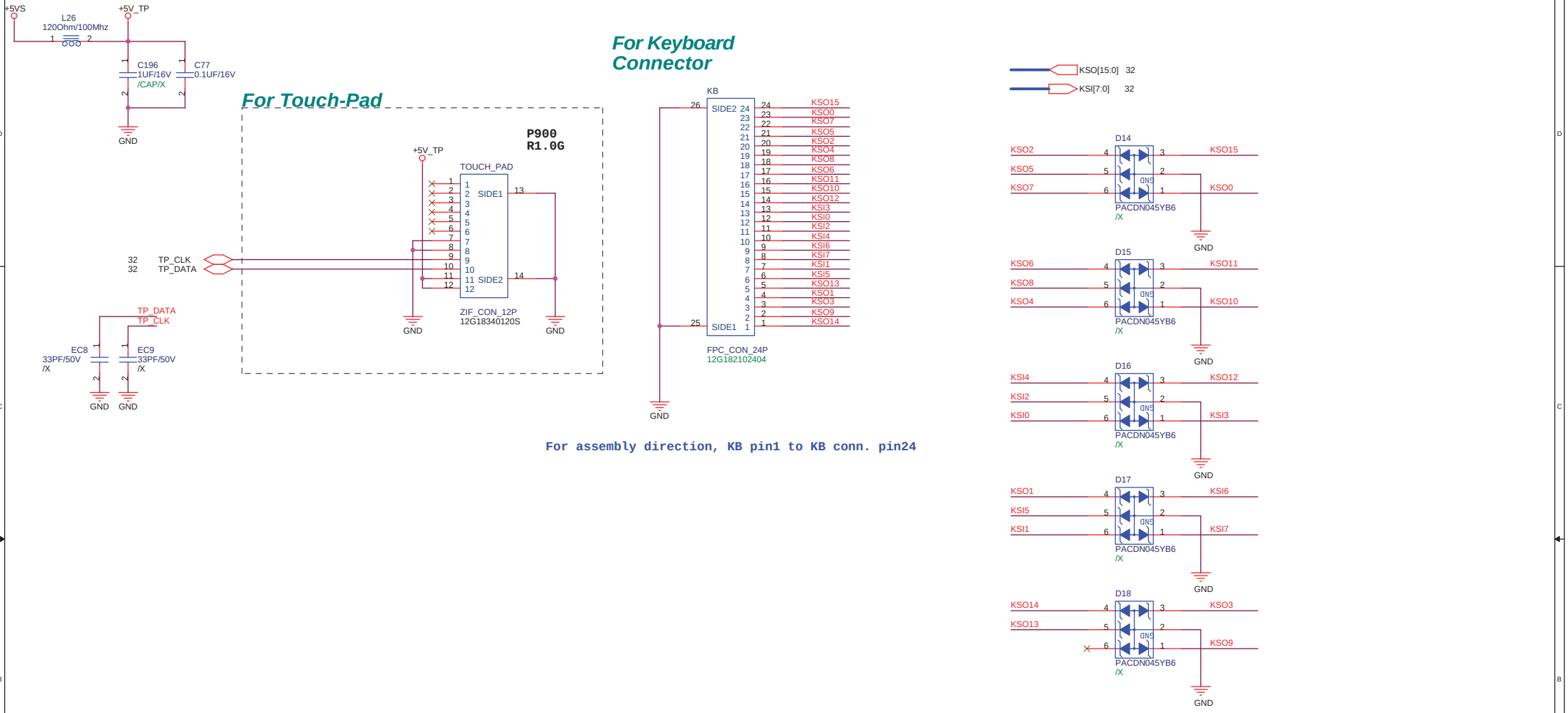
U19 use 06G023044020, second source 06G023055010



Change to 12G171010049(The sam as other EPC)

<Core Design>

ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 35 of 50	

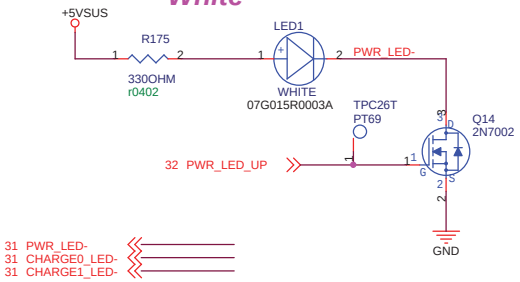


For assembly direction, KB pin1 to KB conn. pin24

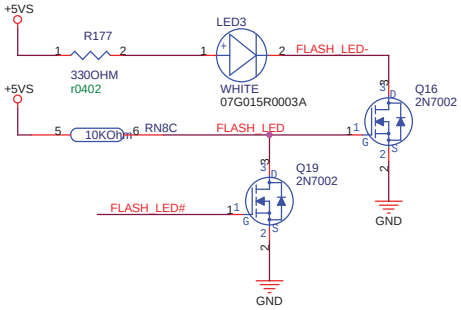
<Core Design>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: *Kell_Huang*	
Size: A3	Project Name: **S101**	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 36 of 50	

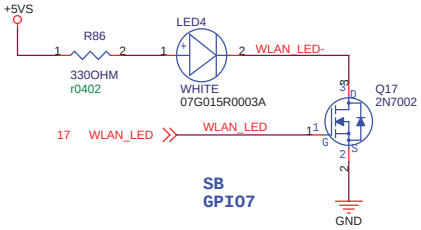
for POWER LED White



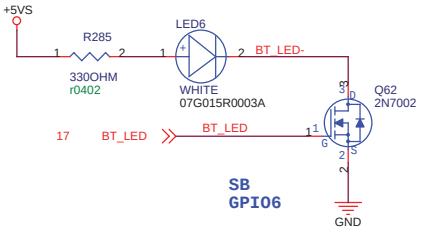
for FLASH LED White



for WLAN LED White

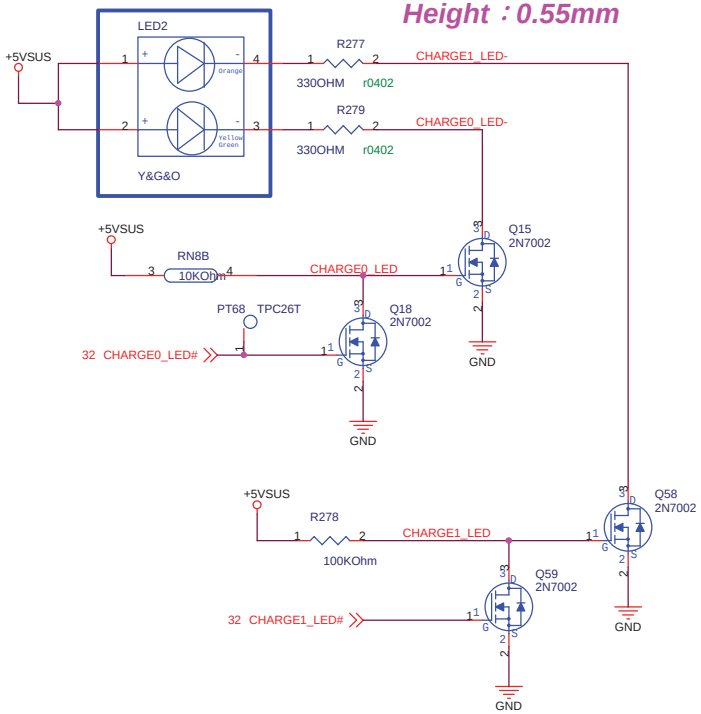


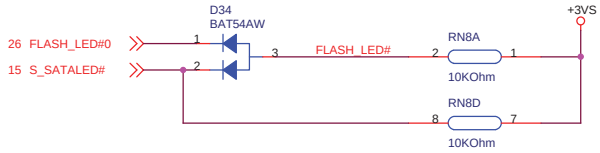
for BlueTooth LED White



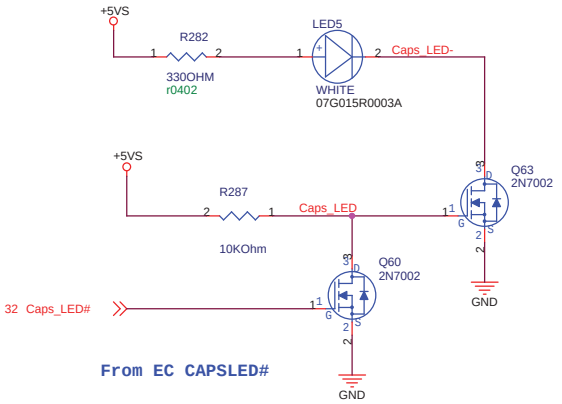
1.1G change to EVERLIGHT

for CHARGE LED Height：0.55mm





for Caps Lock LED White



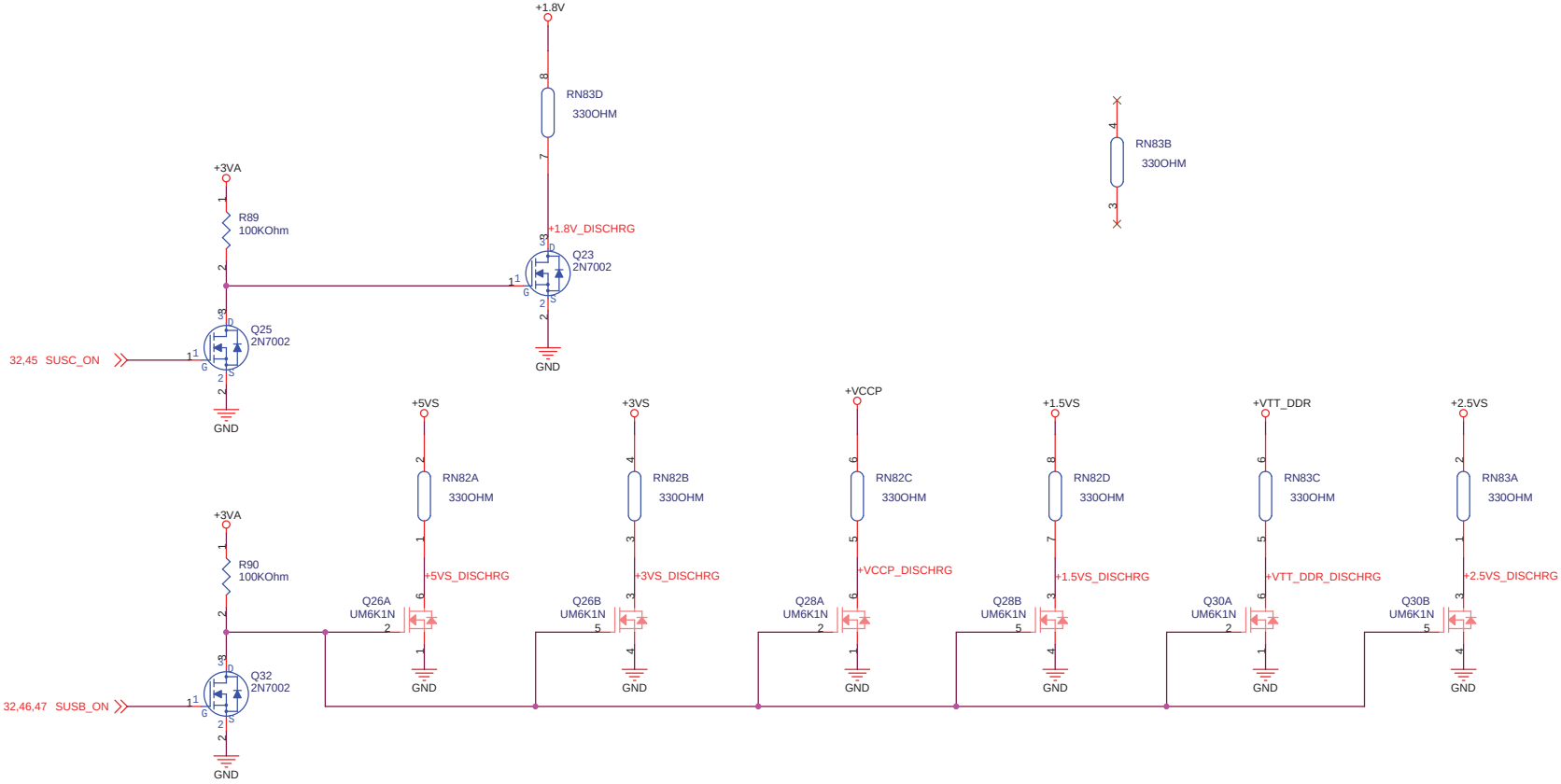
The battery charge indicator (LED) shows the status of the battery' s power as follows:

cenario	Adapter mode	Battery mode
Battery power is between 100%~80%	Orange ON	Green ON
Battery power is between 80%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	Off

Note: The BATTERY LED should be off when the machine has no battery attached.

<Core Design>

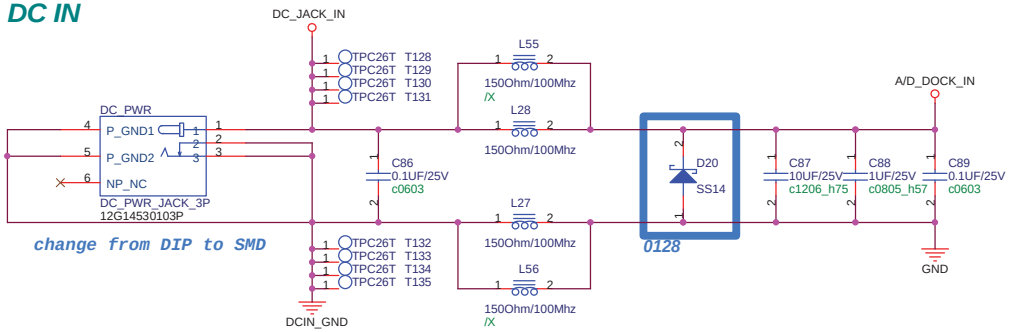
ASUSTek Computer INC.	Title : LED	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 37 of 50	



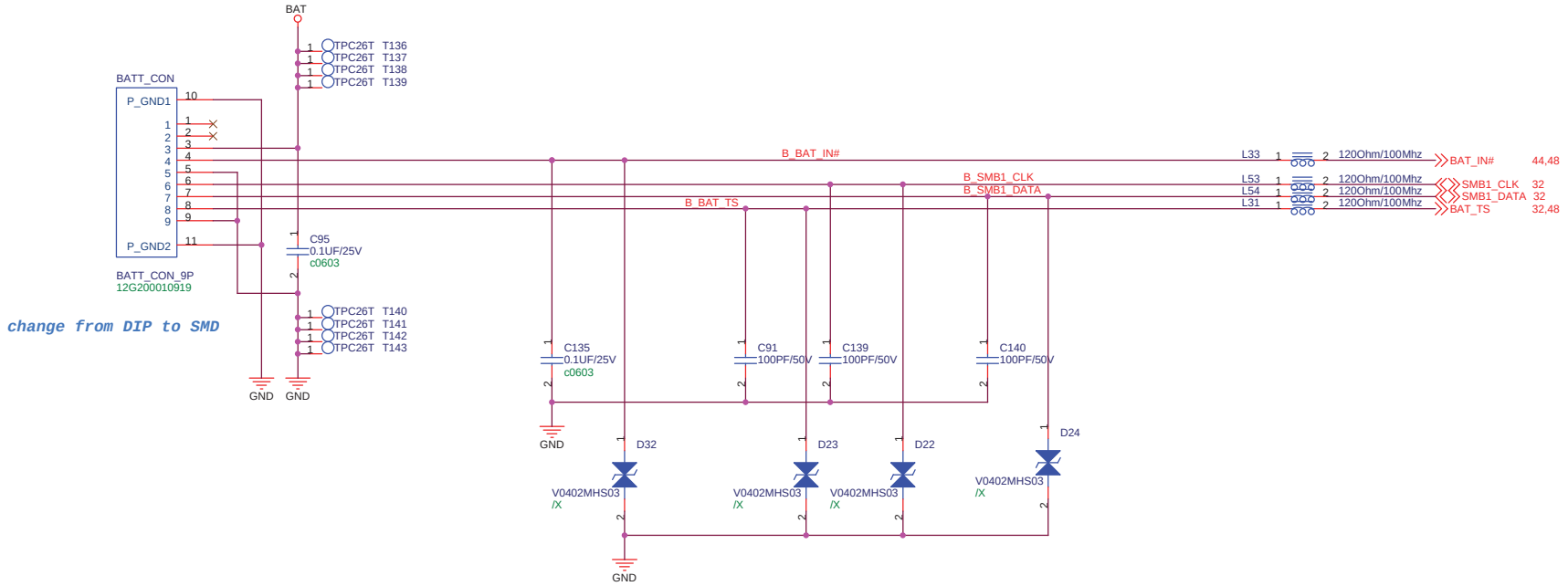
<Core Design>

ASUSTek Computer INC.	Title : Discharge	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 38 of 50	

DC IN

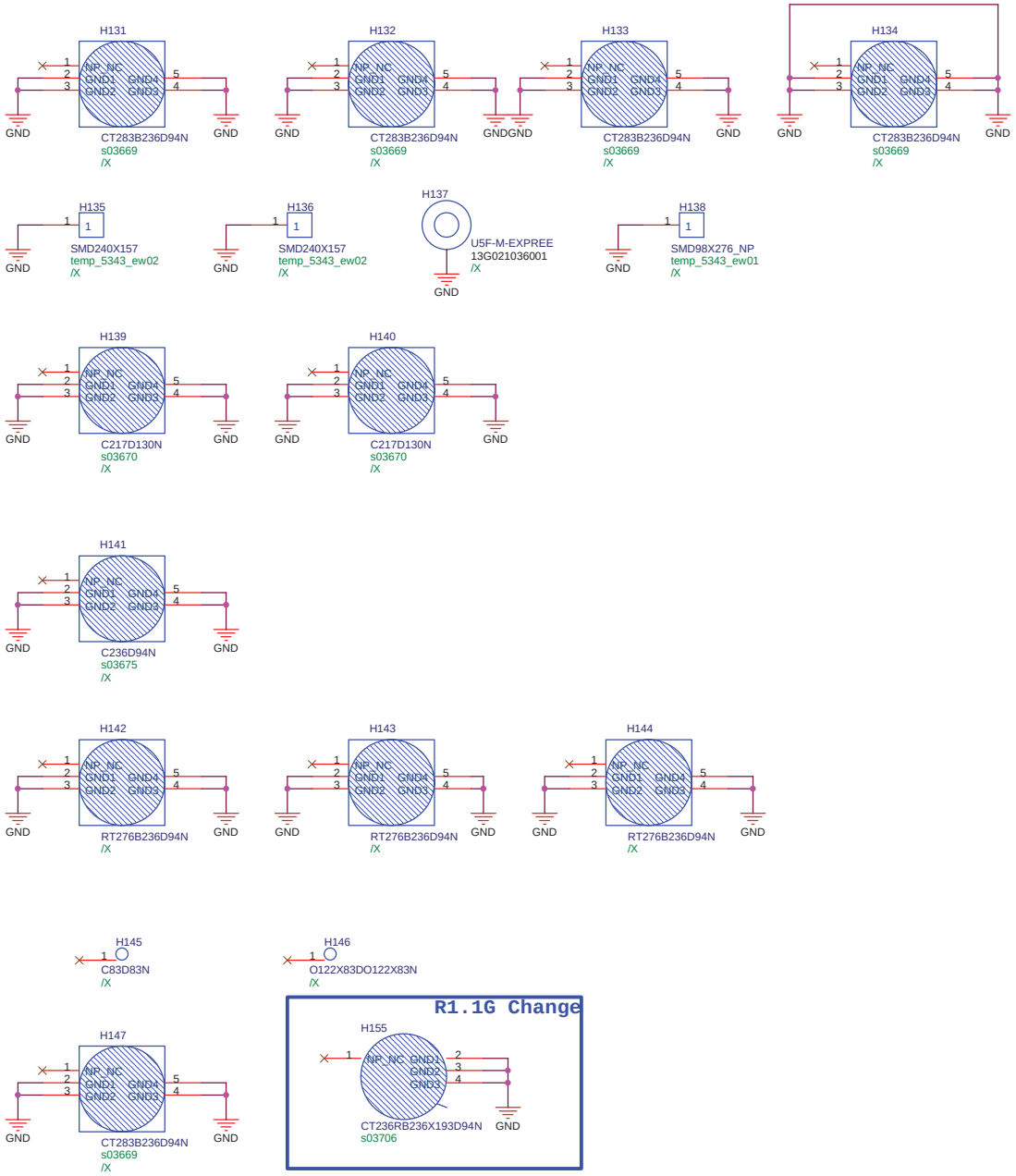


BAT IN



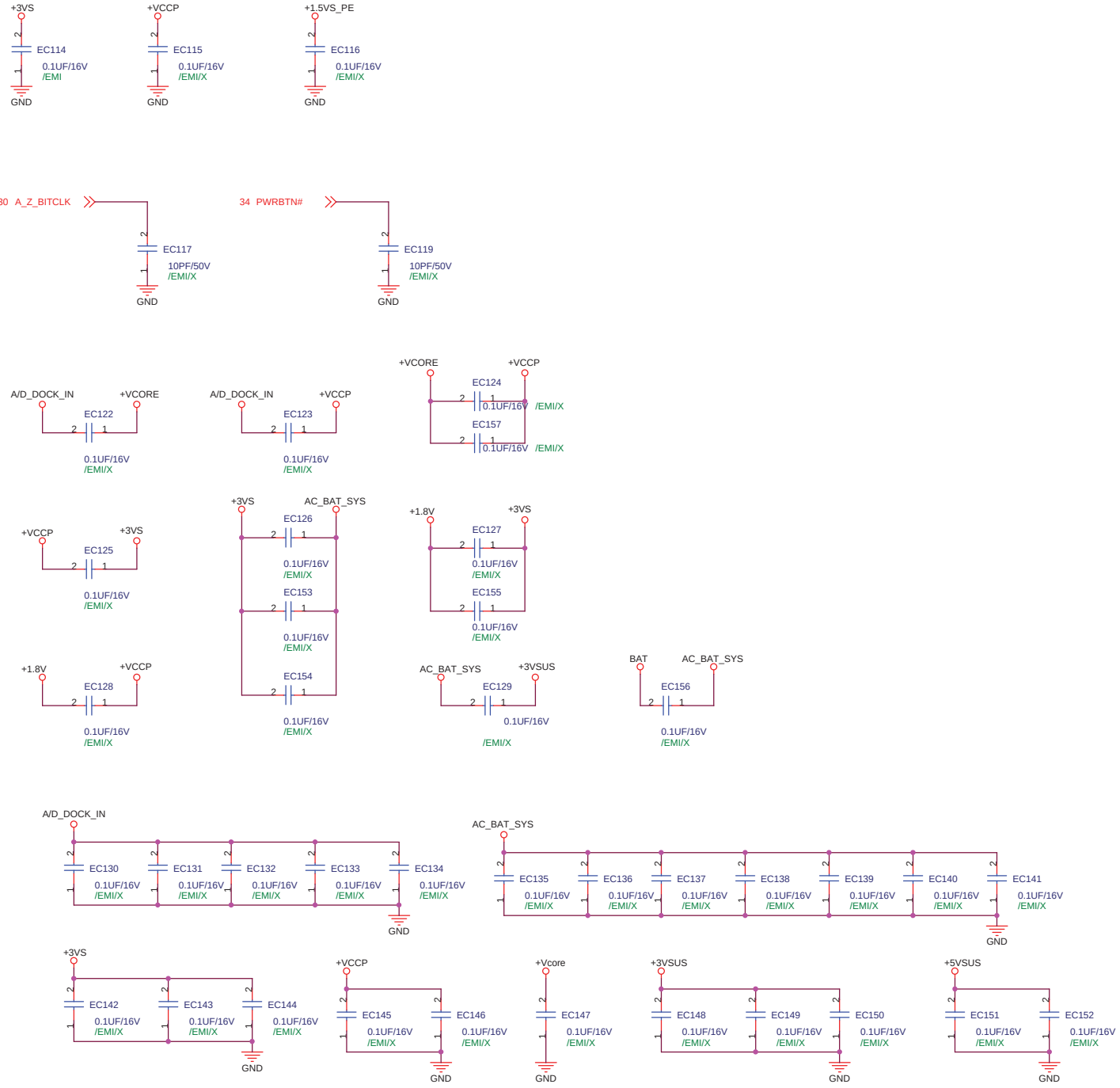
<Core Design>

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 39 of 50	



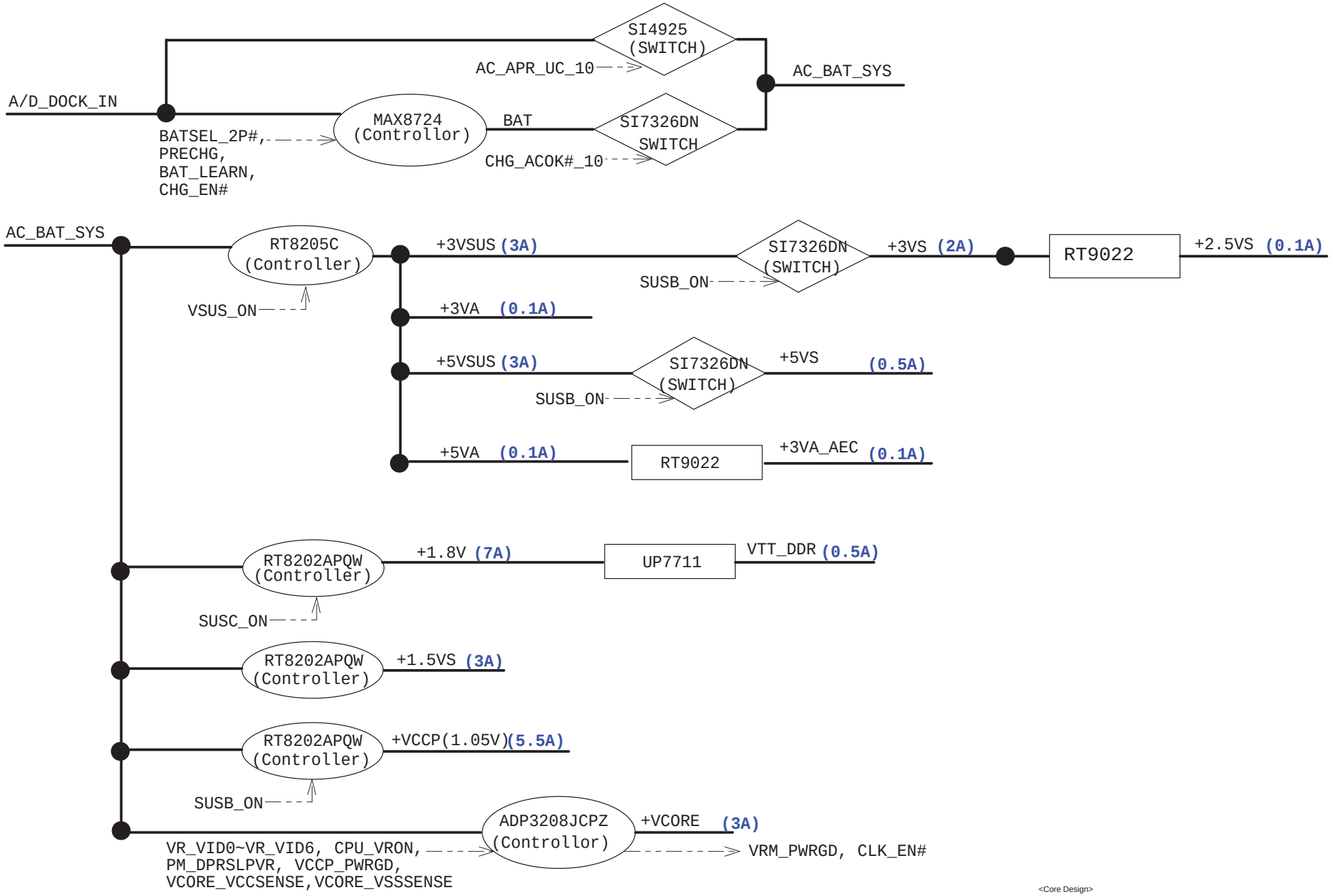
<Core Design>

ASUSTek Computer INC.	Title : Srew Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 40 of 50	



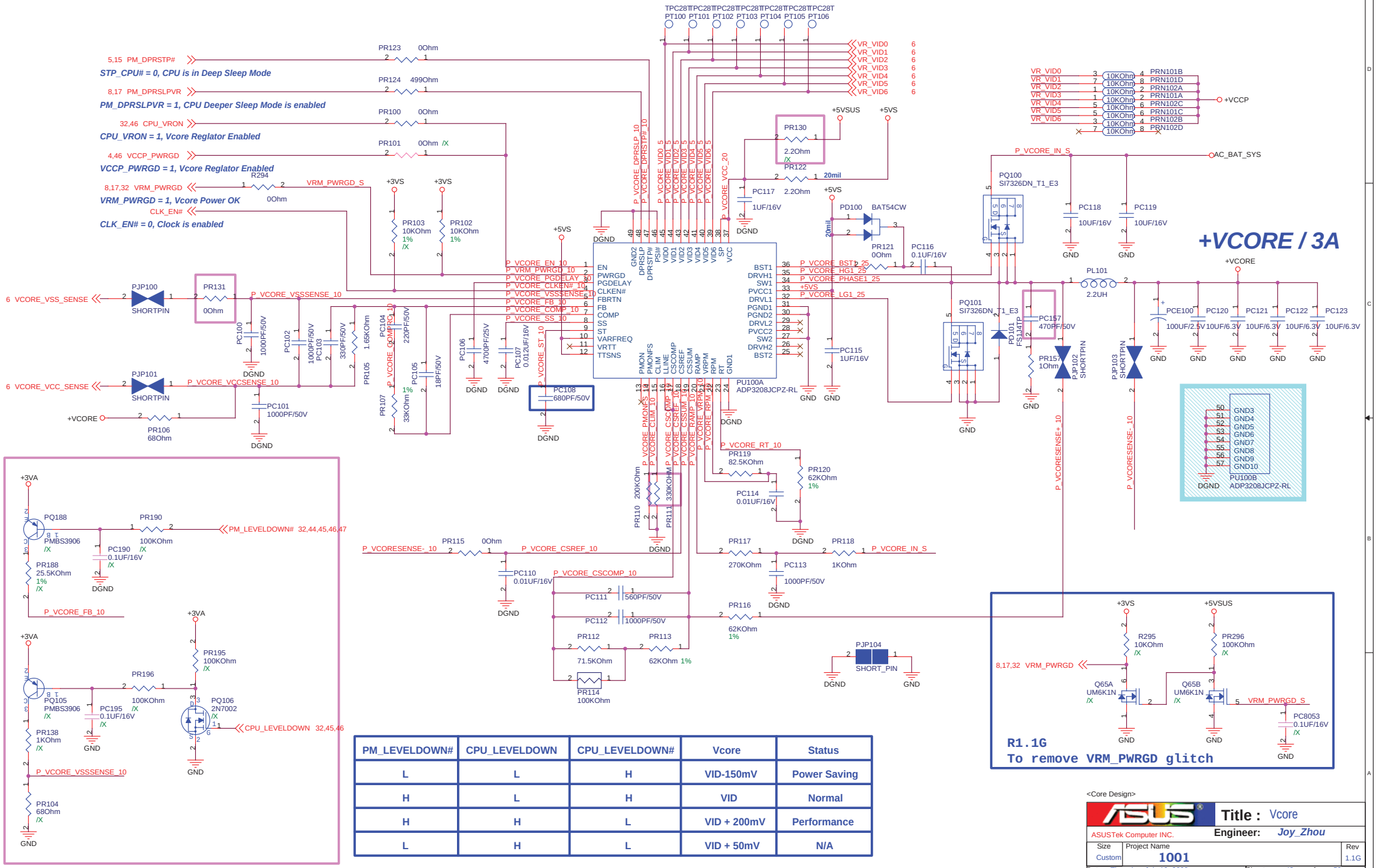
<Core Design>

ASUSTek Computer INC.	Title : EMI	
	Engineer: Kell_Huang	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 41 of 50	



<Core Design>

ASUSTek Computer INC.	Title : Power Flow	
	Engineer: Joy_Zhou	
Size: A3	Project Name: S101	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 42 of 50	



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

<Core Design>

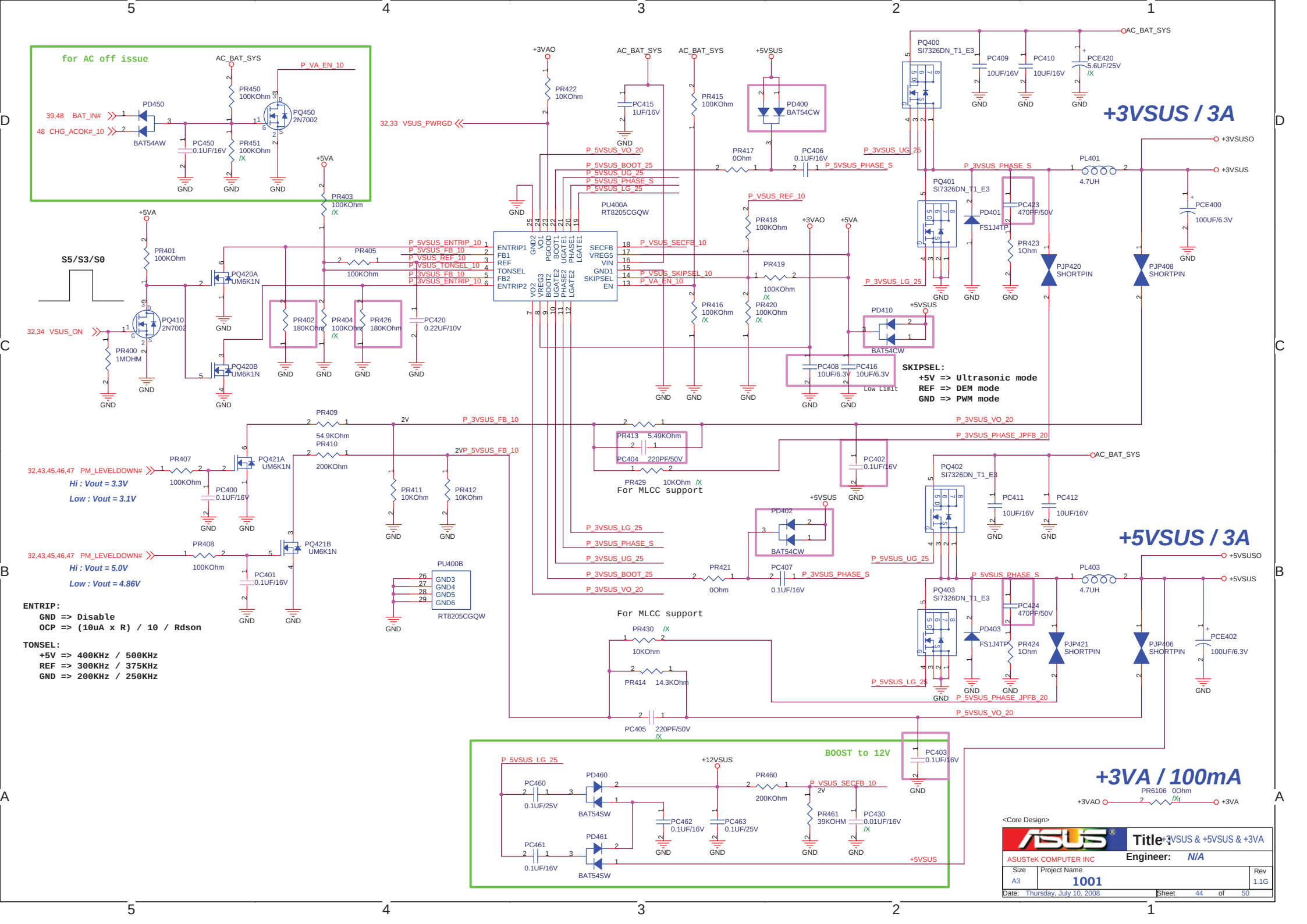
ASUSTek Computer INC.

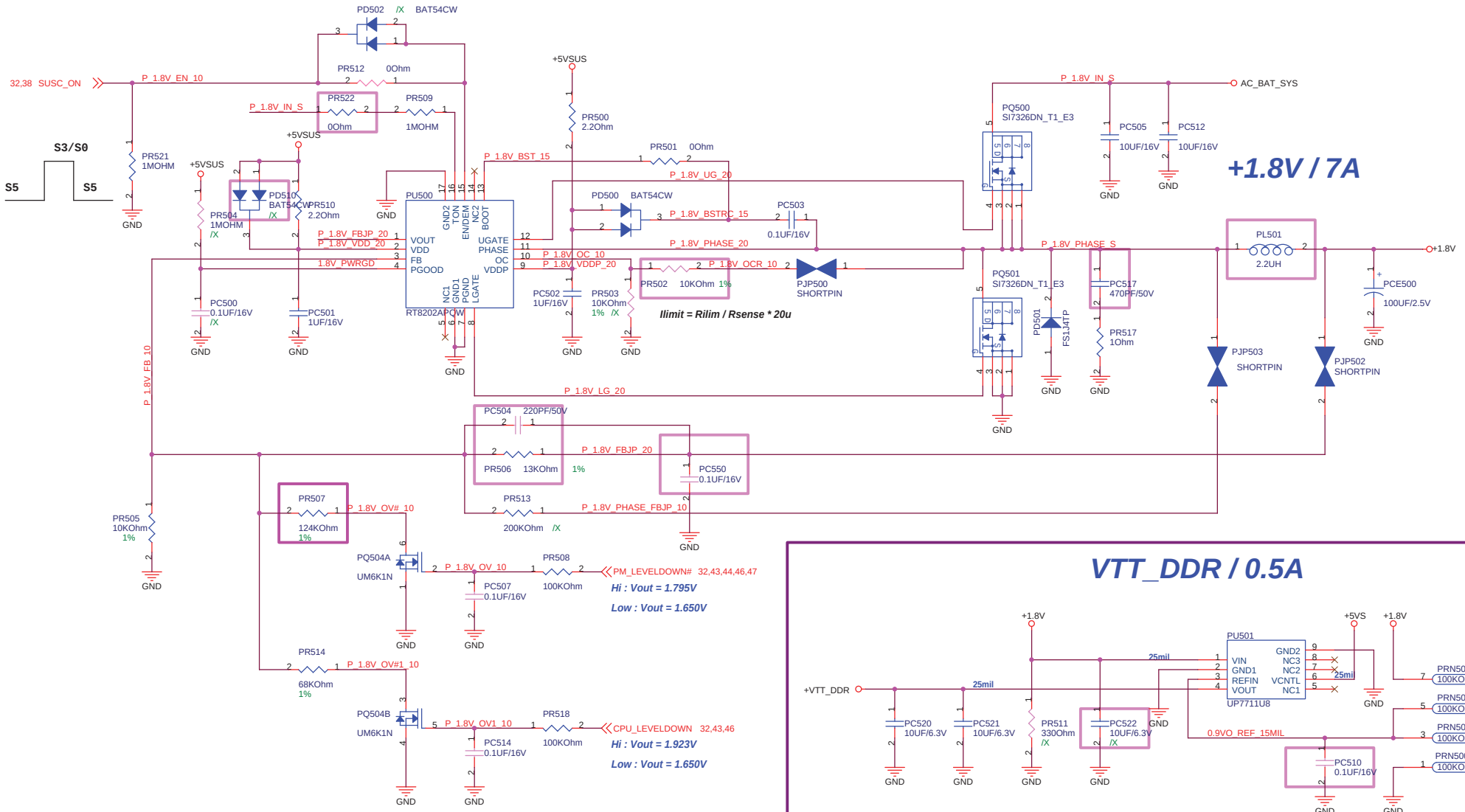
Title : Vcore

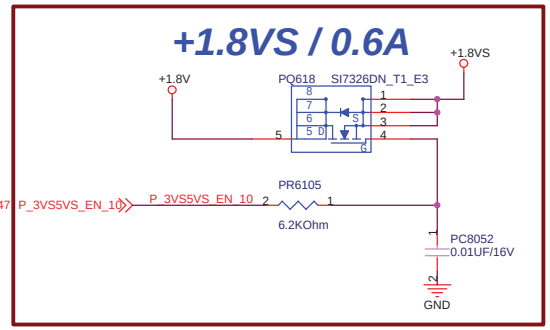
Engineer: Joy_Zhou

Size	Project Name	Rev
Custom	1001	1.1G

Date: Thursday, July 10, 2008 Sheet 43 of 50


for AC off issue
AC_BAT_SYS
P_VA_EN_10
PD450
39,48 BAT_IN#
48 CHG_ACOK#_10
BAT54AW
PR450 100KOhm
PQ450 2N7002
PC450 0.1UF/16V
PR451 100KOhm /X
GND
+5VA
PR403 100KOhm /X
S5/S3/S0
PR401 100KOhm
PQ420A UM6K1N
PQ420B UM6K1N
PQ410 2N7002
32,34 VSUS_ON
PR400 1MOHM
PR402 180KOhm
PR404 100KOhm /X
PR426 180KOhm
PC420 0.22UF/10V
PR405 100KOhm
+3VAO
PR422 10KOhm
32,33 VSUS_PWRGD
PC415 1UF/16V
PR415 100KOhm
+5VSUS
PD400 BAT54CW
PR417 0Ohm
PC406 0.1UF/16V
PU400A RT8205CGQW
P_5VSUS_ENTRIP_10
P_5VSUS_FB_10
P_VSUS_REF_10
P_VSUS_TONSEL_10
P_3VSUS_FB_10
P_3VSUS_ENTRIP_10
P_5VSUS_VO_20
P_5VSUS_BOOT_25
P_5VSUS_UG_25
P_5VSUS_PHASE_S
P_5VSUS_LG_25
P_VSUS_SECFB_10
P_VSUS_SKIPSEL_10
P_VA_EN_10
PR418 100KOhm
PR419 100KOhm /X
PR420 100KOhm /X
PR416 100KOhm /X
PD410 BAT54CW
PC408 10UF/6.3V
PC416 10UF/6.3V
Low Limit
SKIPSEL:
+5V => Ultrasonic mode
REF => DEM mode
GND => PWM mode
PR409 54.9KOhm
PR410 200KOhm
2V
P_3VSUS_FB_10
2VP_5VSUS_FB_10
PR413 5.49KOhm
PC404 220PF/50V
PR429 10KOhm /X
For MLCC support
P_3VSUS_VO_20
P_3VSUS_PHASE_JPFB_20
PC402 0.1UF/16V
32,43,45,46,47 PM_LEVELDOWN#
Hi : Vout = 3.3V
Low : Vout = 3.1V
PR407 100KOhm
PQ421A UM6K1N
PC400 0.1UF/16V
PR411 10KOhm
PR412 10KOhm
PD402 BAT54CW
P_3VSUS_LG_25
P_3VSUS_PHASE_S
P_3VSUS_UG_25
P_3VSUS_BOOT_25
P_3VSUS_VO_20
PR421 0Ohm
PC407 0.1UF/16V
PR408 100KOhm
PQ421B UM6K1N
PC401 0.1UF/16V
Hi : Vout = 5.0V
Low : Vout = 4.86V
PU400B RT8205CGQW
GND3
GND4
GND5
GND6
ENTRIP:
GND => Disable
OCP => (10uA x R) / 10 / Rdson
TONSEL:
+5V => 400KHz / 500KHz
REF => 300KHz / 375KHz
GND => 200KHz / 250KHz
For MLCC support
PR430 /X 10KOhm
PR414 14.3KOhm
PC405 220PF/50V /X
BOOST to 12V
+12VSUS
PC460 0.1UF/25V
PD460 BAT54SW
PD461 BAT54SW
PC461 0.1UF/16V
PC462 0.1UF/16V
PC463 0.1UF/25V
PR460 200KOhm
PR461 39KOHM
PC430 0.01UF/16V /X
PC403 0.1UF/16V
+3VSUS / 3A
PQ400 SI7326DN_T1_E3
PC409 10UF/16V
PC410 10UF/16V
PCE420 5.6UF/25V /X
PQ401 SI7326DN_T1_E3
PD401 FS1J4TP
PC423 470PF/50V
PR423 1Ohm
PJP420 SHORTPIN
PJP408 SHORTPIN
PL401 4.7UH
PCE400 100UF/6.3V
+3VSUSO
+3VSUS
+5VSUS / 3A
PQ402 SI7326DN_T1_E3
PC411 10UF/16V
PC412 10UF/16V
PQ403 SI7326DN_T1_E3
PD403 FS1J4TP
PC424 470PF/50V
PR424 1Ohm
PJP421 SHORTPIN
PJP406 SHORTPIN
PL403 4.7UH
PCE402 100UF/6.3V
+5VSUSO
+5VSUS
+3VA / 100mA
PR6106 0Ohm /X
+3VAO
+3VA
<Core Design>
ASUSTeK COMPUTER INC
Title: +3VSUS & +5VSUS & +3VA
Engineer: N/A
Size A3
Project Name 1001
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 44 of 50





PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.72V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

<Core Design>

ASUSTek Computer INC.

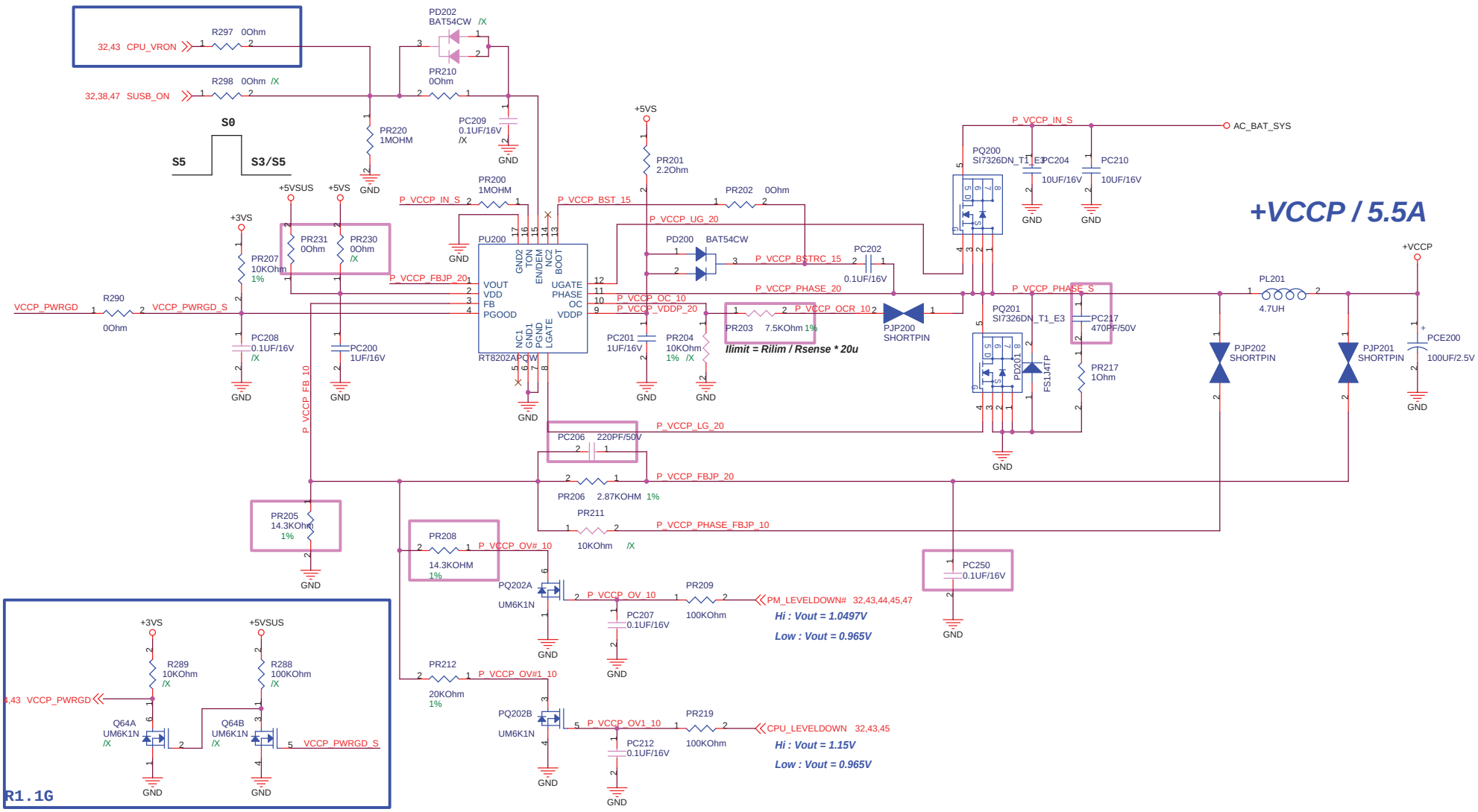
Title : +1.8V & VTTDDR

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1001	1.1G

Date: Thursday, July 10, 2008 Sheet 45 of 50

1.1G change Enable signal from CPU_VRON

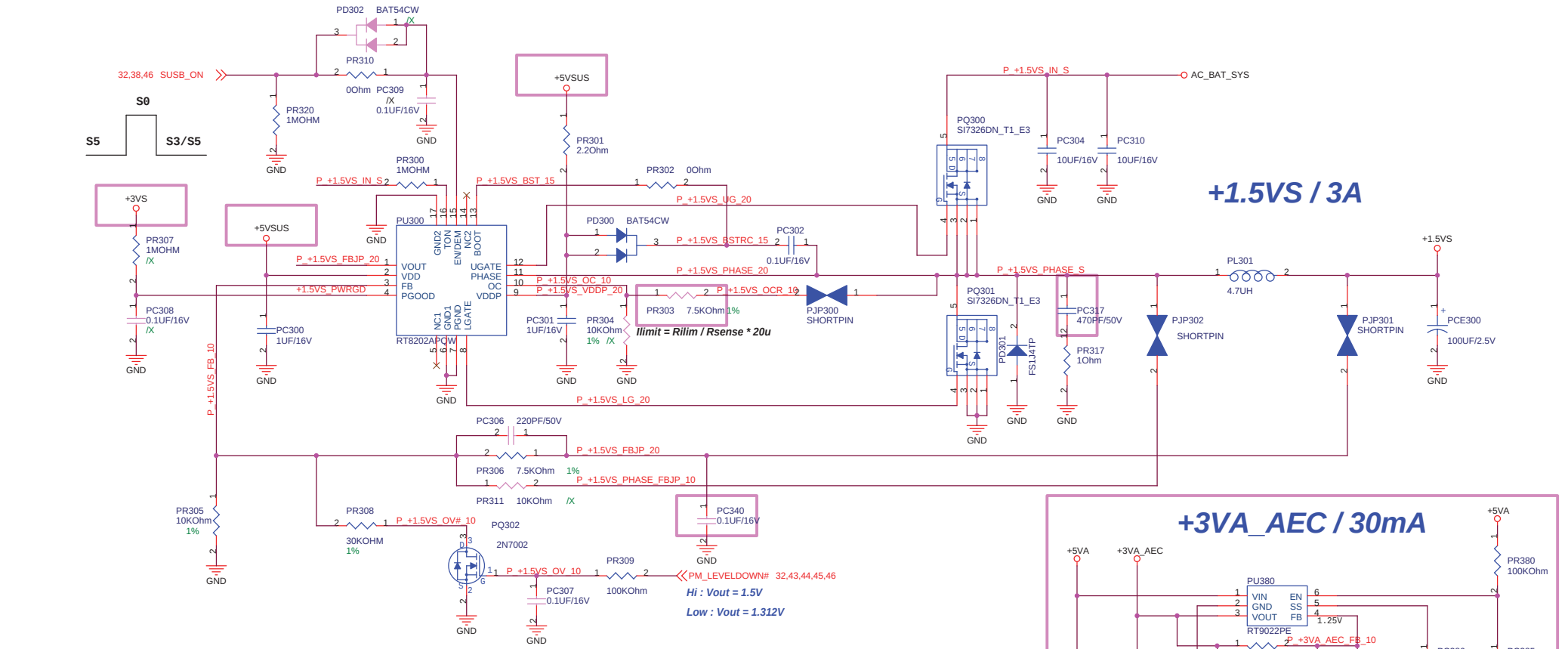


To remove VCCP_PWRGD glitch

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

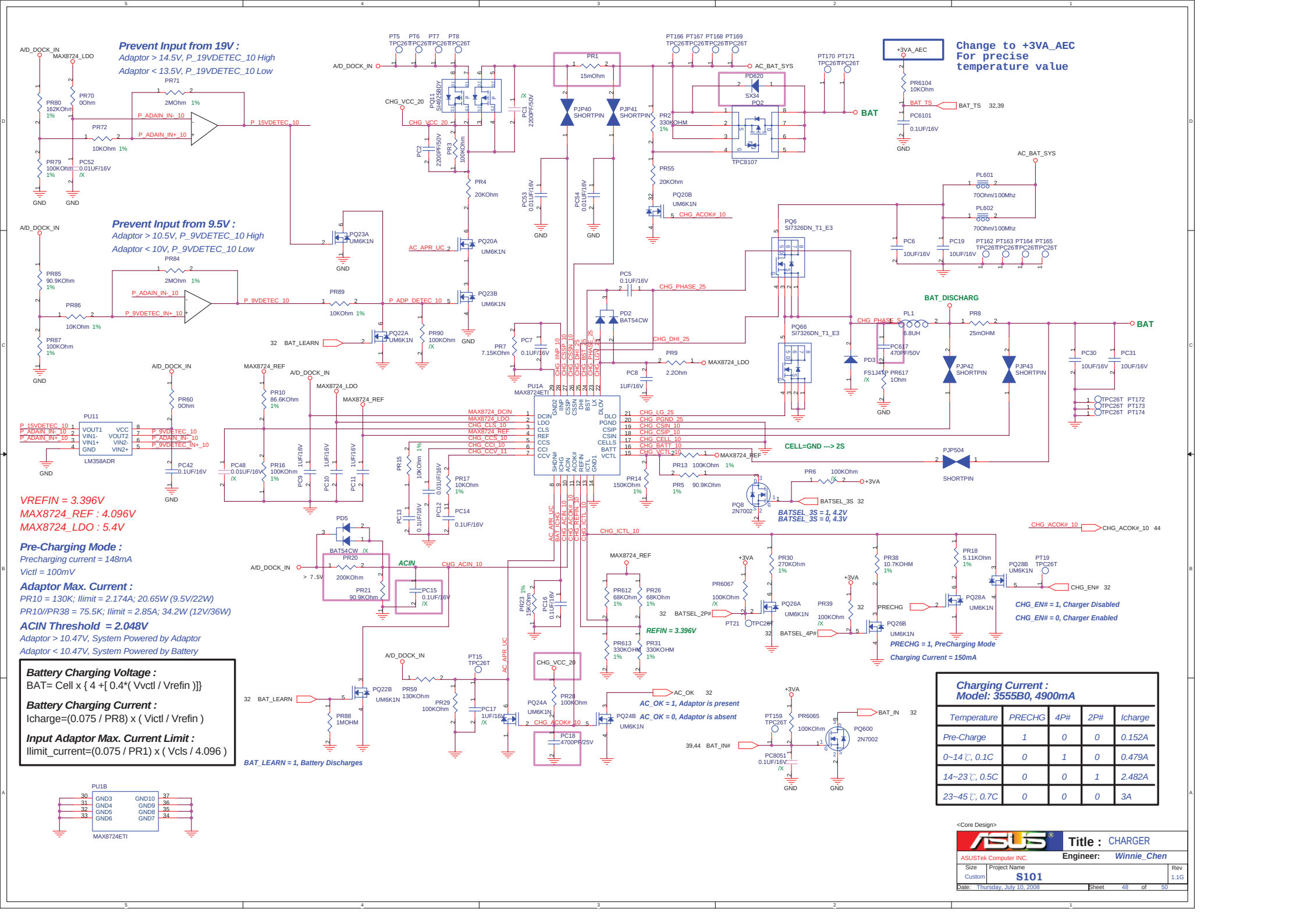
<Core Design>

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1001	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 46 of 50	



<Core Design>

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1001	Rev: 1.1G
Date: Thursday, July 10, 2008	Sheet 47 of 50	


Prevent Input from 19V :
Adaptor > 14.5V, P_19VDETEC_10 High
Adaptor < 13.5V, P_19VDETEC_10 Low
Prevent Input from 9.5V :
Adaptor > 10.5V, P_9VDETEC_10 High
Adaptor < 10V, P_9VDETEC_10 Low
Change to +3VA_AEC For precise temperature value
VREFIN = 3.396V
MAX8724_REF : 4.096V
MAX8724_LDO : 5.4V
Pre-Charging Mode :
Precharging current = 148mA
VictI = 100mV
Adaptor Max. Current :
PR10 = 130K; Ilimit = 2.174A; 20.65W (9.5V/22W)
PR10//PR38 = 75.5K; Ilimit = 2.85A; 34.2W (12V/36W)
ACIN Threshold = 2.048V
Adaptor > 10.47V, System Powered by Adaptor
Adaptor < 10.47V, System Powered by Battery
Battery Charging Voltage :
BAT= Cell x { 4 +[0.4*(Vvctl / Vrefin)]}
Battery Charging Current :
Icharge=(0.075 / PR8) x (Victl / Vrefin)
Input Adaptor Max. Current Limit :
Ilimit_current=(0.075 / PR1) x (Vcls / 4.096)
CELL=GND ---> 2S
BATSEL_3S = 1, 4.2V
BATSEL_3S = 0, 4.3V
ACIN
REFIN = 3.396V
PRECHG = 1, PreCharging Mode
Charging Current = 150mA
CHG_EN# = 1, Charger Disabled
CHG_EN# = 0, Charger Enabled
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent
BAT_LEARN = 1, Battery Discharges
Charging Current :
Model: 3555B0, 4900mA
Temperature | PRECHG | 4P# | 2P# | Icharge
Pre-Charge | 1 | 0 | 0 | 0.152A
0~14℃, 0.1C | 0 | 1 | 0 | 0.479A
14~23℃, 0.5C | 0 | 0 | 1 | 2.482A
23~45℃, 0.7C | 0 | 0 | 0 | 3A
<Core Design>
Title : CHARGER
ASUSTek Computer INC.
Engineer: Winnie_Chen
Size Custom
Project Name S101
Rev 1.1G
Date: Thursday, July 10, 2008
Sheet 48 of 50

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Internal Pull Up
15	GPIO08	EXTSMI#	OD	10K ohm Pull Up to +3VSU
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	HOTKEY_SW2#	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	OD	10K ohm Pull Up to +3VSUS
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL_4P#	O	Battery charging current setting
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	O	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configureation
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSAVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Core Design>

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Satan He

Size	Project Name	Rev
A3	S101	1.1G

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<Core Design>

ASUSTek Computer INC.	Title : History	
	Engineer: *Satan He*	
Size: A3	Project Name: **S101**	Rev: 1.1G
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